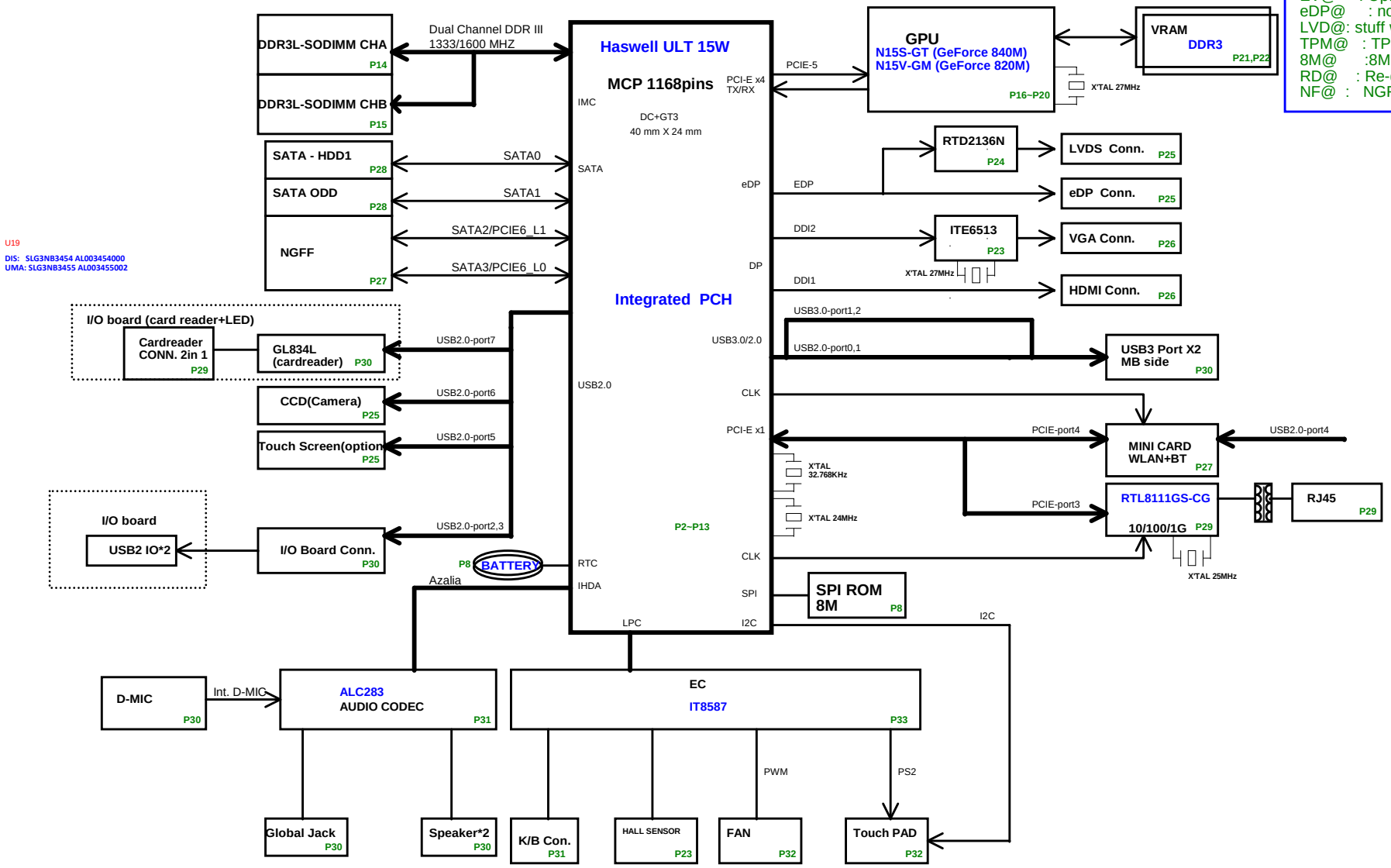
ZYW ULT SYSTEM BLOCK DIAGRAM

01

BOM

IV@ : iGPU
EV@ : Optimus
eDP@ : no stuff when use LVDS
LVD@: stuff when use LVDS
TPM@ : TPM
8M@ :8M FLASH ROM
RD@ : Re-driver SATA
NF@ : NGFF card



U19
DIS: SLG3NB3454 AL003454000
UMA: SLG3NB3455 AL003455002

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PROJECT : ZYW
Block Diagram
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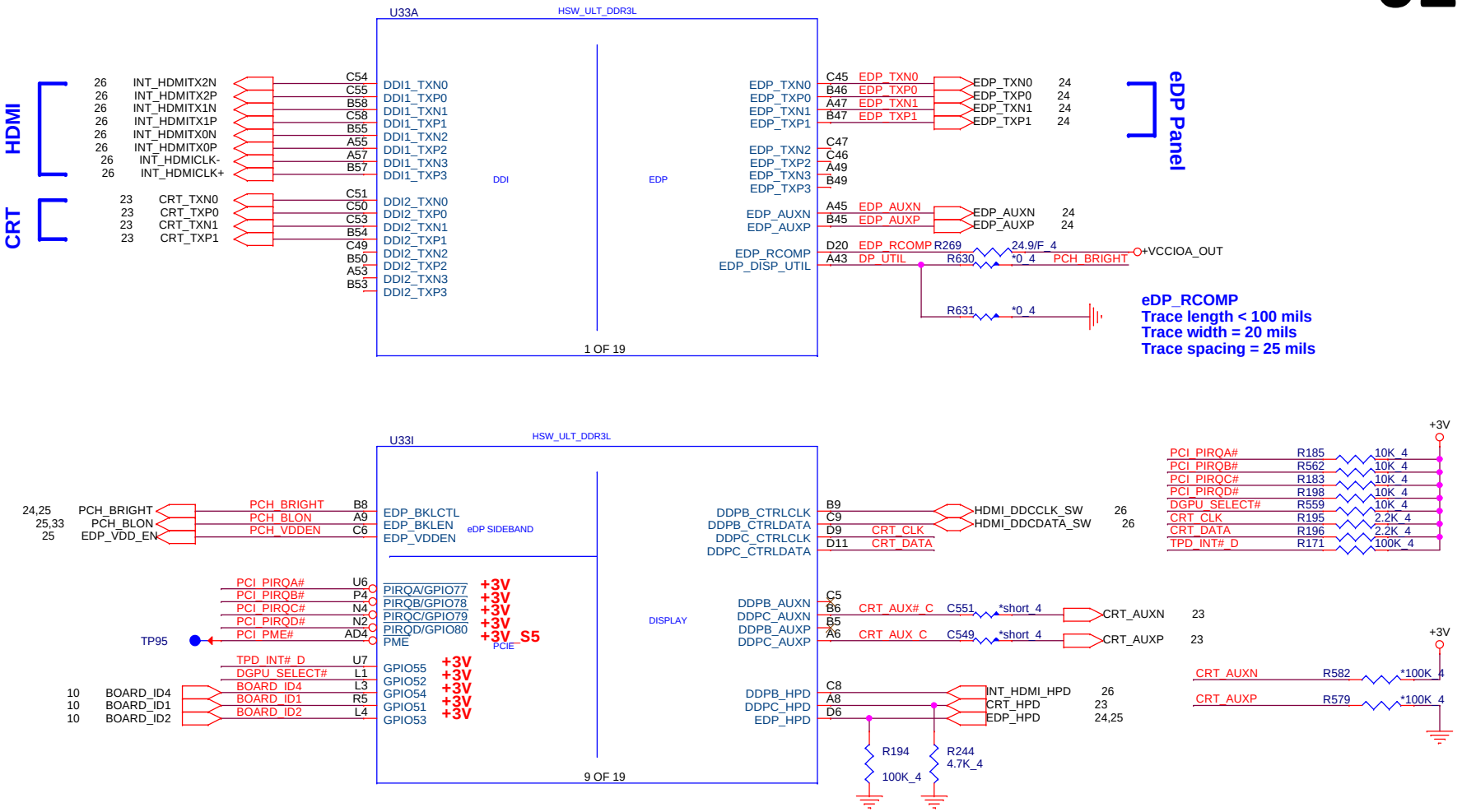
Haswell ULT (DISPLAY,eDP)

02



Quanta Computer Inc.		
PROJECT : ZYW		
Size	Document Number: Haswell 3/5 (DDI/eDP)	Rev 3A
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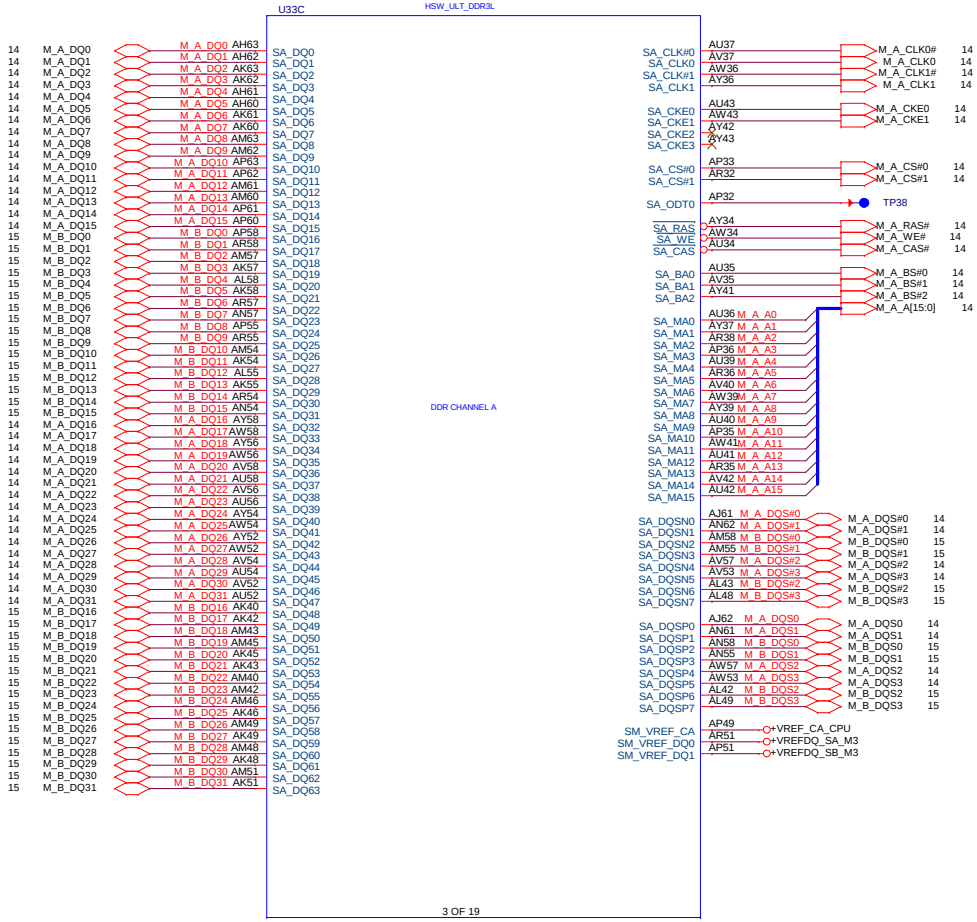
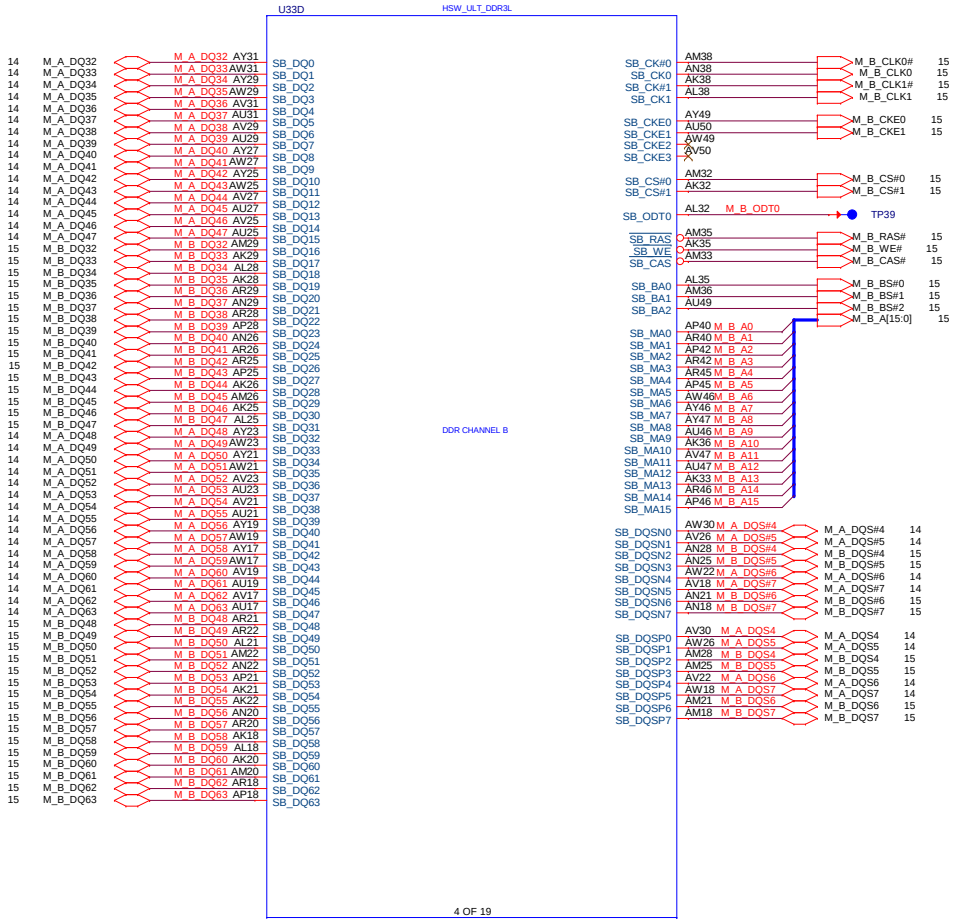
Haswell ULT (DDR3L)



Haswell Processor (DDR3)



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PROJECT : ZYW

Size	Document Number	Rev
	Haswell 2/5 (DDR3 I/F)	3A

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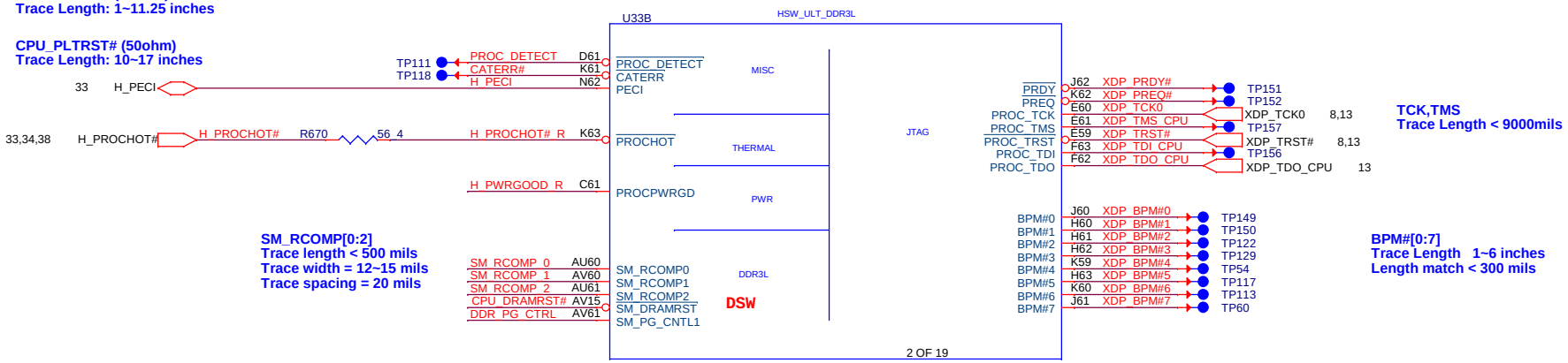
Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

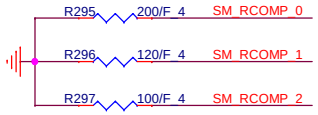


SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

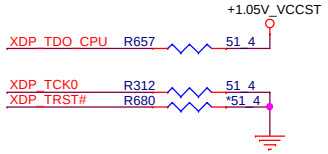
TCK,TMS
Trace Length < 9000mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

DRAM COMP

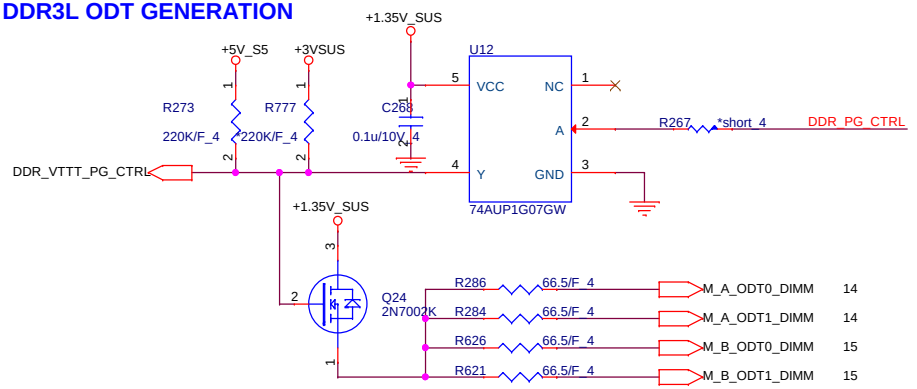


XDP PU/PD

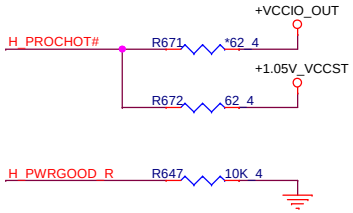


37

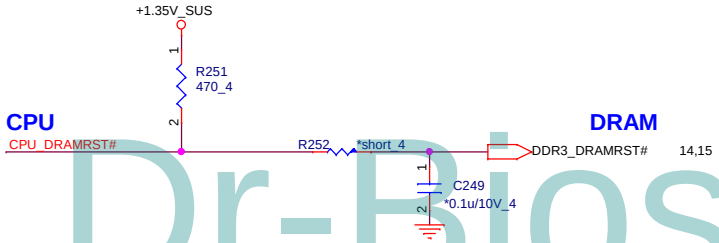
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	Haswell 1/5 (PEG/DMI/FDI)	3A
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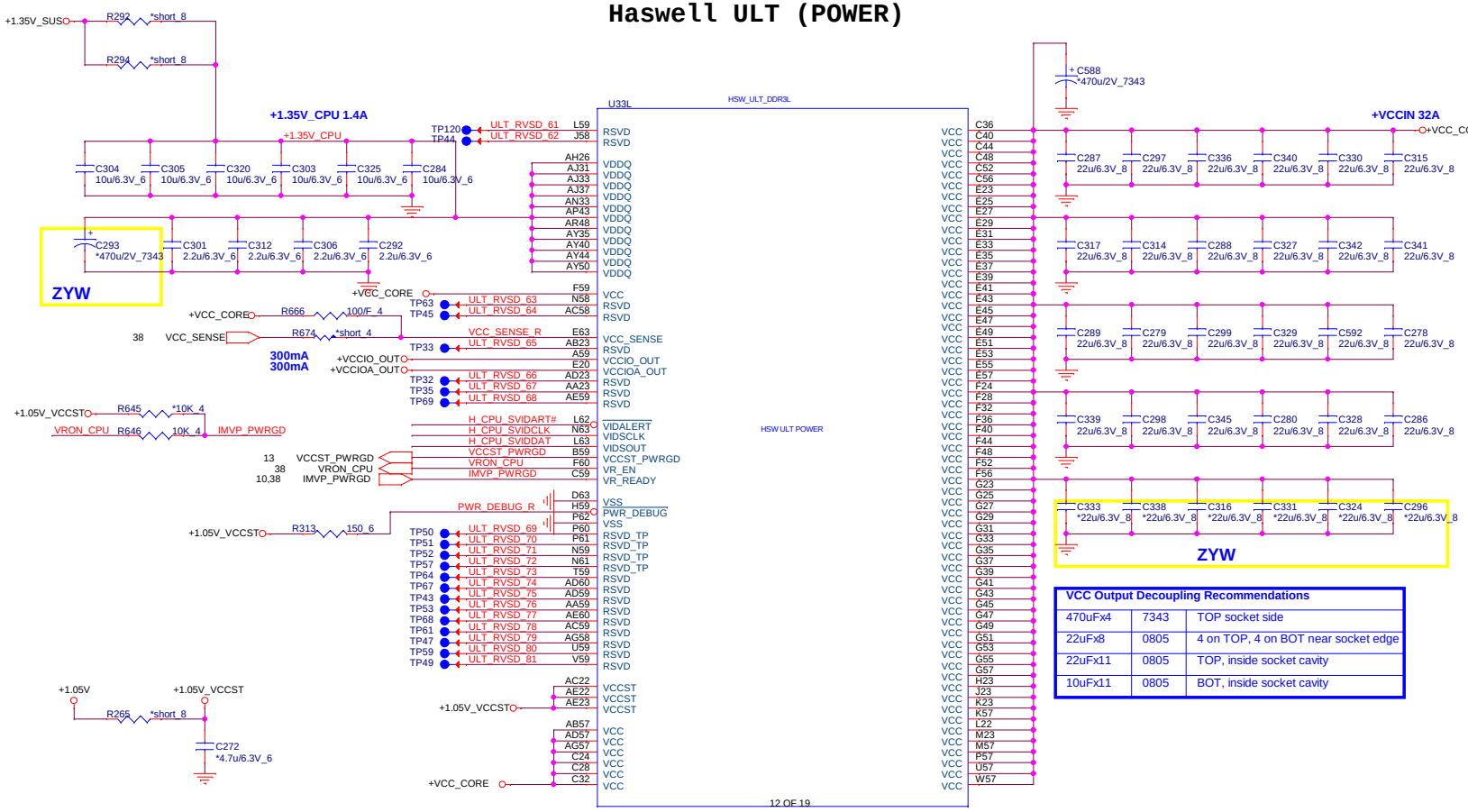
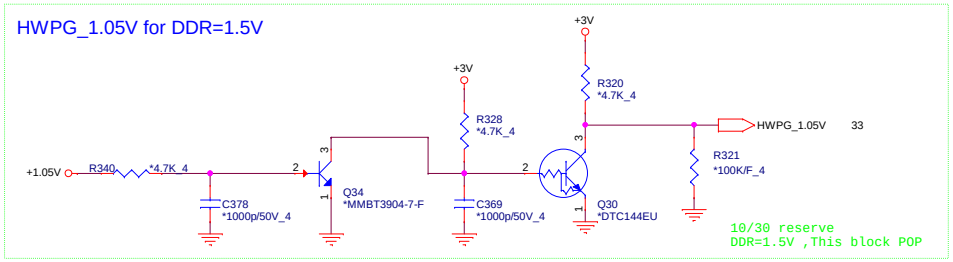
Haswell ULT (POWER)



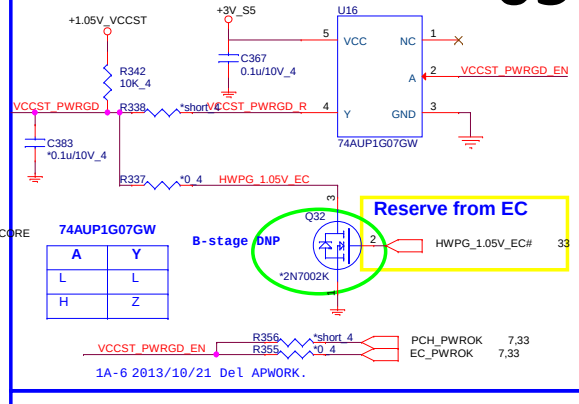
VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

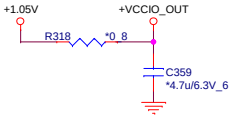


VCCST PWRGD

CRB is via +1.05V PG

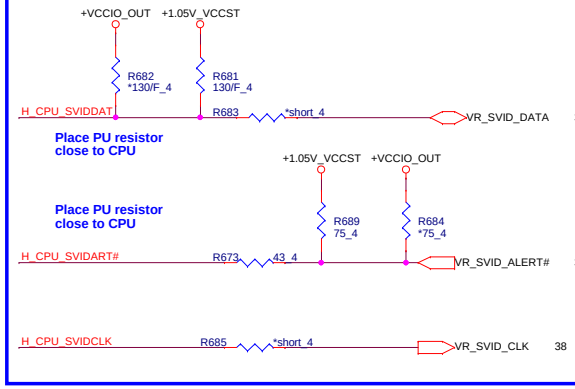
05





SVID

Layout note: need routing together and ALERT need between CLK and DATA.



Quanta Computer Inc.	
PROJECT : ZYW	
Size	Document Number: Haswell 4/5 (POWER) — Rev 3A
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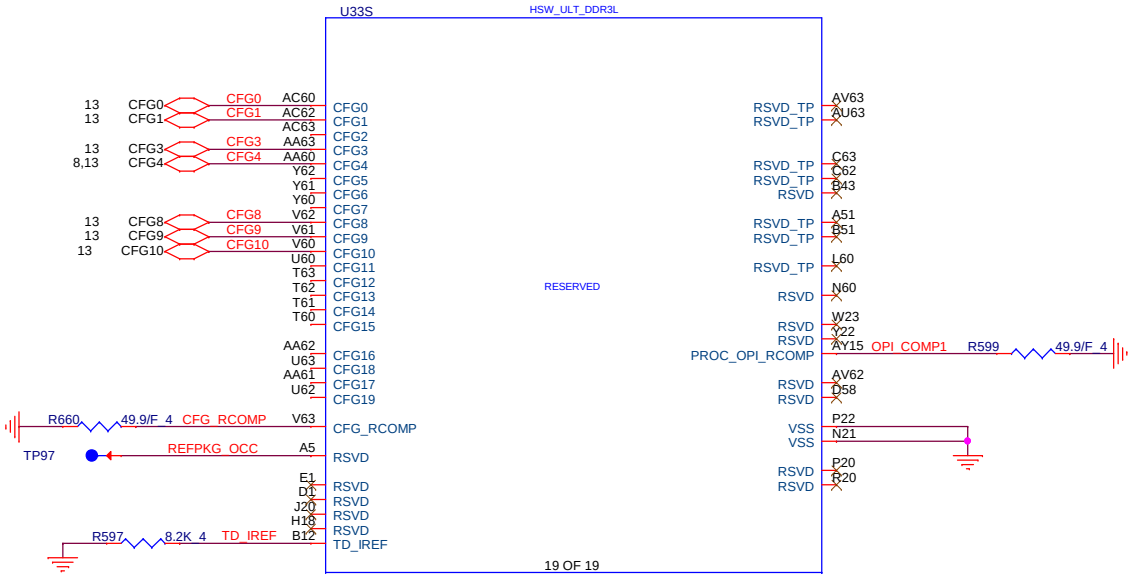
Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R306 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R688 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R687 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R686 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R676 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R307 *1K_4

Quanta Computer Inc.
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	Haswell 5/5 (CFG/GND)	3A

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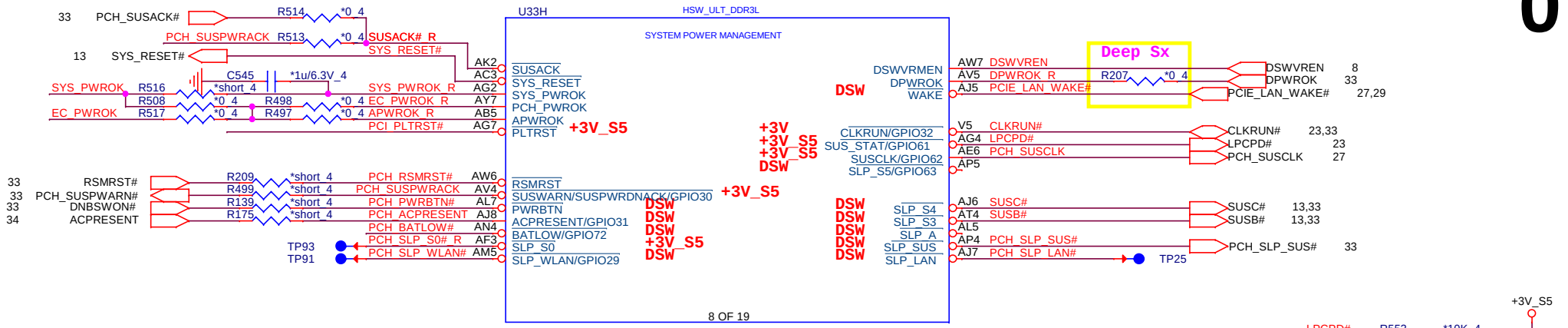
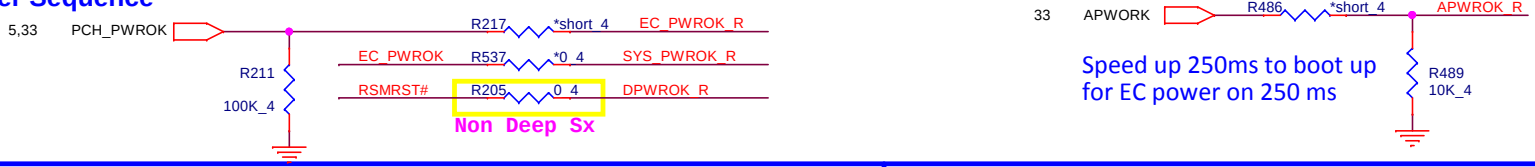
Haswell ULT PCH (PM)

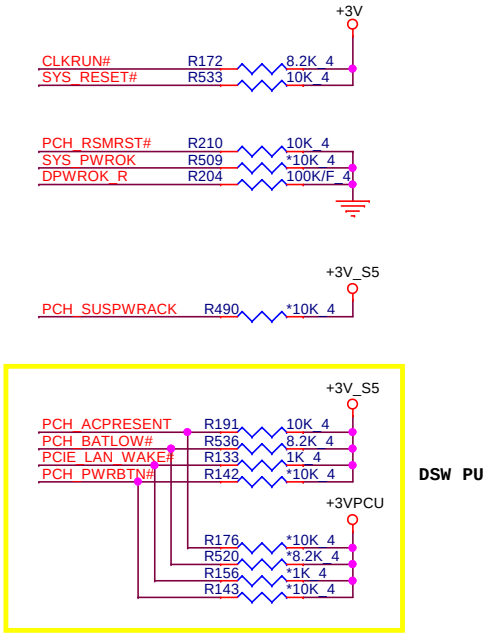
07



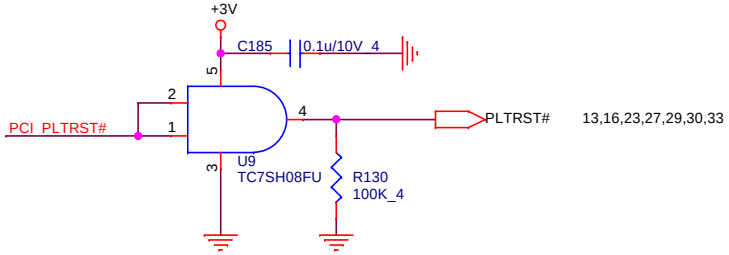
Power Sequence



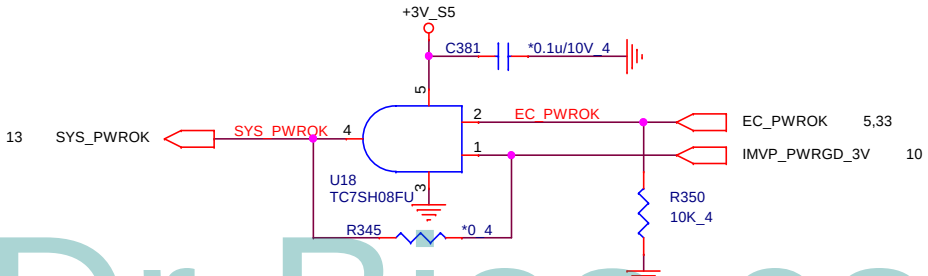
PCH PM PU/PD



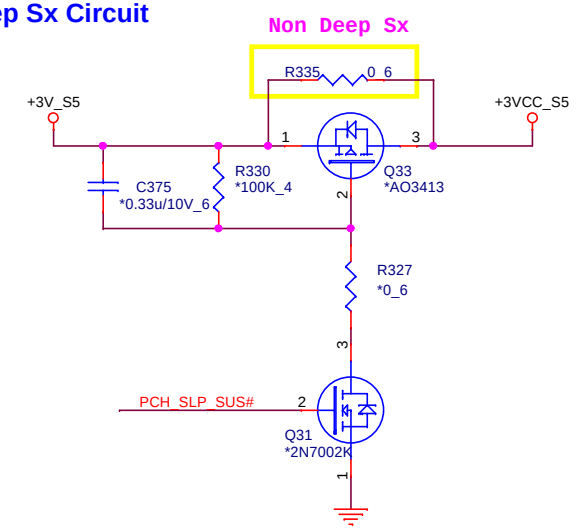
PLTRST# Buffer



SYSPWOK



Deep Sx Circuit



Quanta Computer Inc.		
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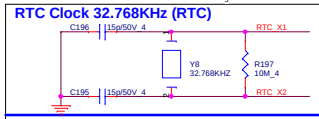
Haswell ULT PCH (RTC/HDA/SATA/SPI)

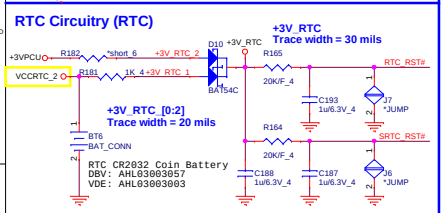
Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)

08

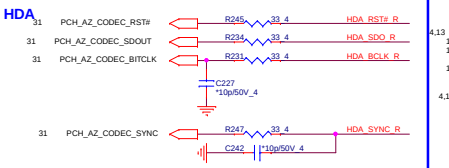
RTC Clock 32.768KHz (RTC)



RTC Circuitry (RTC)



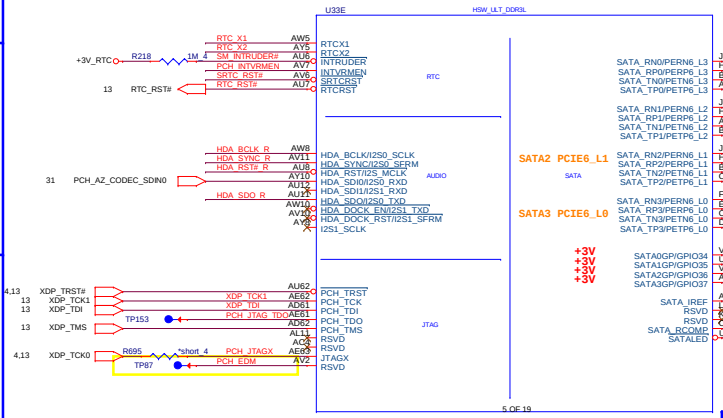
HDA

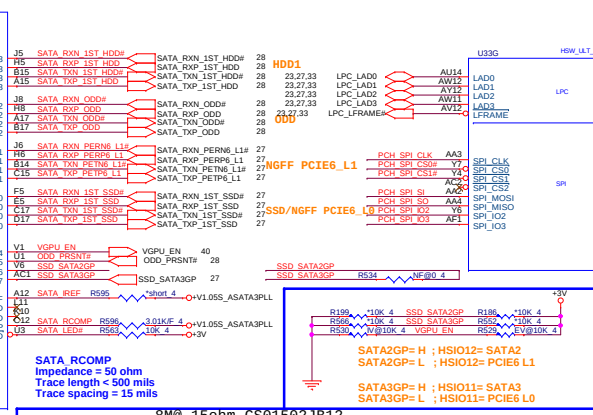


PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

MP remove(Intel)



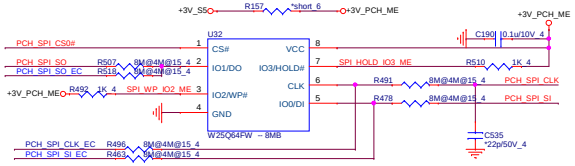


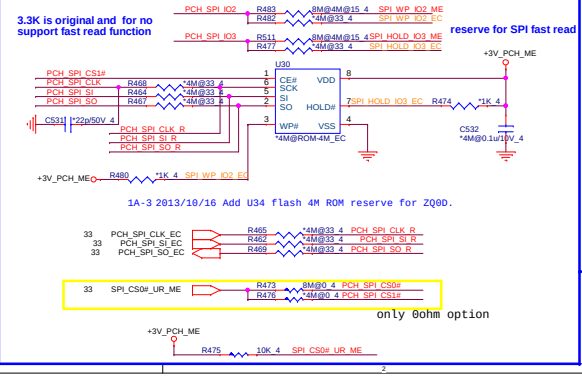
SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

PCH SPI ROM(8M)

8M@ 15ohm CS015021B12
4M@ 330ohm CS033021B29

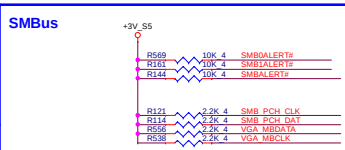
8M@4M@ 15ohm (when one SPI device)
8M@4M@ 330ohm (when two SPI device)



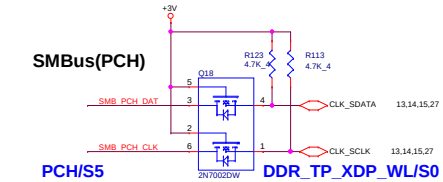


AKE3EFP0N07	Winbond	W25Q64FVSSIQ
AKE3EZN0Q01	EON	EN25QH64-104HIP
AKE3EGN0Q01	GD	GD25B64BSIGR

SMBus

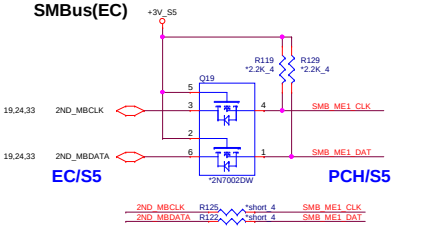


SMBus(PCH)



PCH/S5 DDR_TP_XDP_WL/S0

SMBus(EC)



EC/S5 PCH/S5

ULT Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	+3V R549 *1K_4 SPKR — SPKR 10,31
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	HDA_SDO_R R233 *short_4 — ME_WR# 33
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	+3V_RTC R228 330K_4 PCH_INTVRMEN R227 *330K_4
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	10 GPIO66 — +3V R147 *1K_4 GPIO66 R162 *1K_4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	10 GPIO86 — +3V R128 *1K_4 GPIO86 R136 *1K_4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	10 GPIO15 — +3V_S5 R188 8.2K_4 GPIO15 R202 *1K_4
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	6,13 CFG4 — CFG4 R690 1K_4
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	7 DSWVREN — +3V_RTC R226 330K_4 DSWVREN R225 *330K_4

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	LPT 2/6 (SATA/HDA/SPI)	3A
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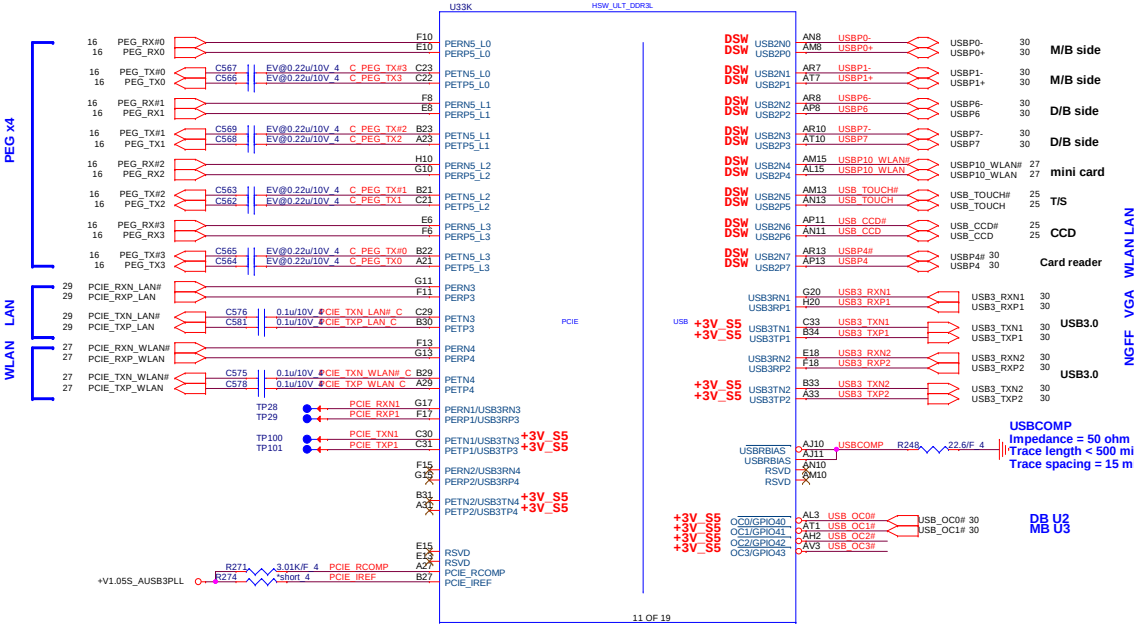
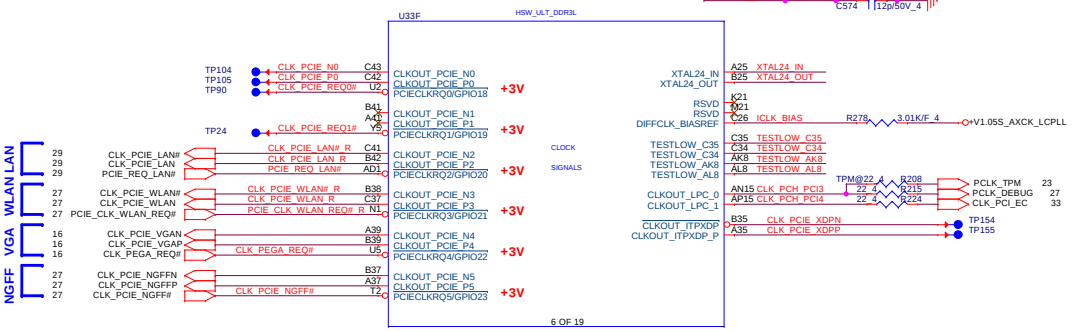
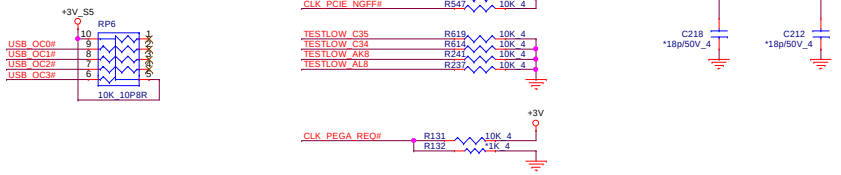
Haswell ULT PCH (PCIE,USB3.0,USB2.0)



Haswell ULT PCH (CLOCK)



USB Overcurrent



Quanta Computer Inc.		
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	LPT 3/6 (PCIE/USB/CLK)	3A
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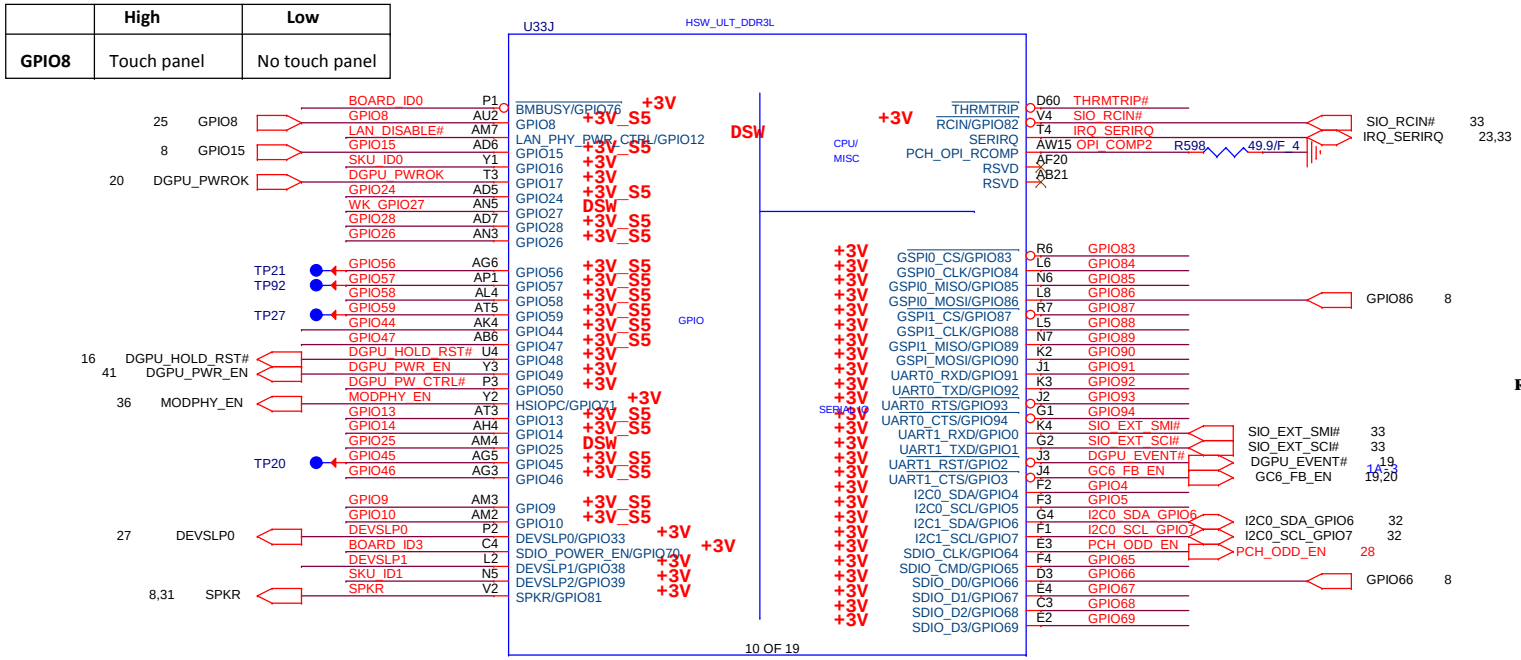
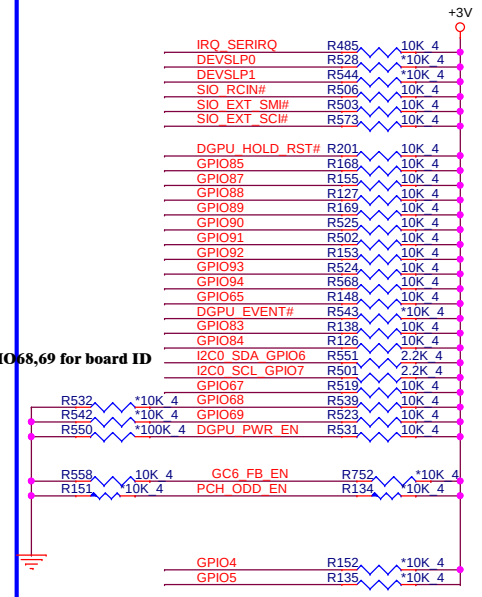
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

	High	Low
GPIO8	Touch panel	No touch panel

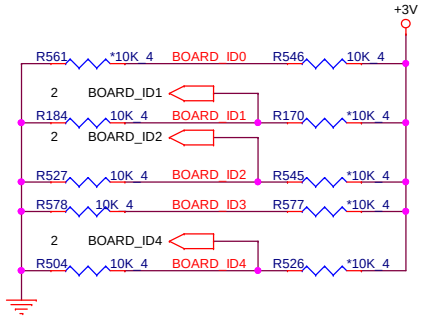


PCH GPIO PU/PD



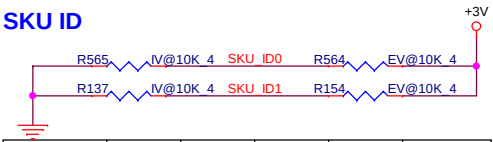
Reserve GPIO68,69 for board ID

Board ID



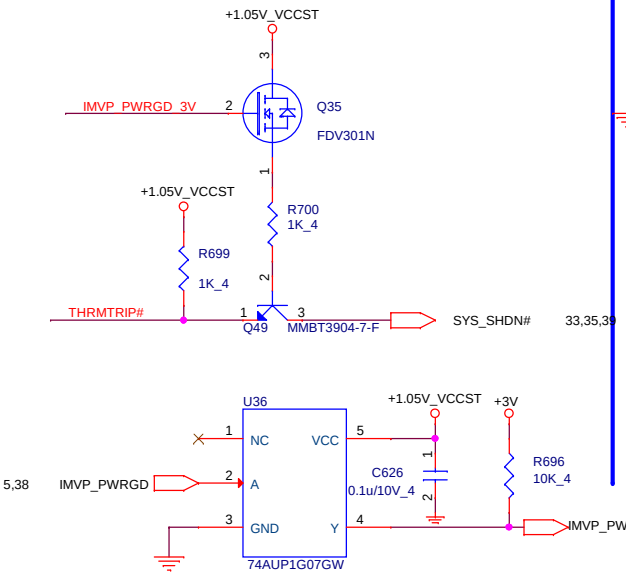
	Low	High
BOARD_ID0	N15V-GL-B	N15V-GM-B (Default)
BOARD_ID1	Reserved (Default)	Reserved
BOARD_ID2	Reserve for Touch pad, default(low)	
BOARD_ID3	WO/dTPM (Default)	W/dTPM
BOARD_ID4	w/VGA (Default)	wo/VGA

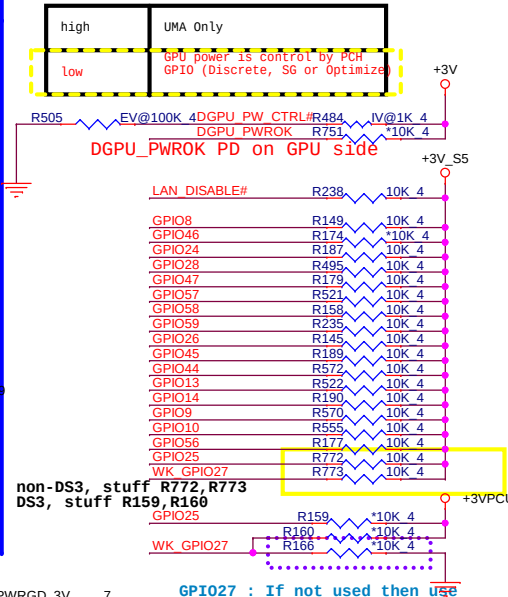
SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip





Quanta Computer Inc.
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	LPT 4/6 (GPIO/MISC)	3A
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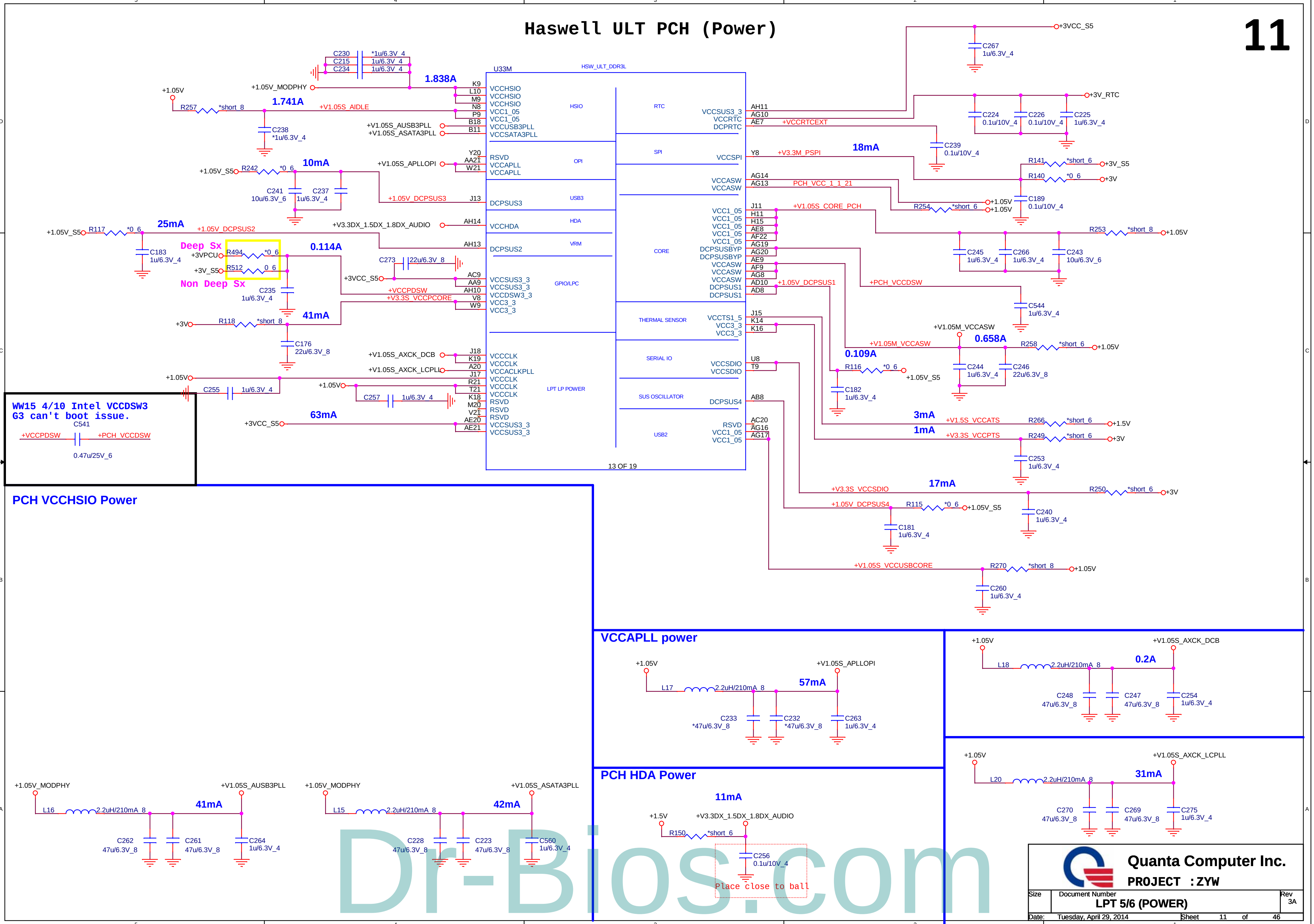
Haswell ULT PCH (Power)
11
U33M
HSW_ULT_DDR3L
HSIO
RTC
SPI
OPI
USB3
HDA
VRM
CORE
GPIO/LPC
THERMAL SENSOR
SERIAL IO
SUS OSCILLATOR
LPT LP POWER
USB2
13 OF 19
VCCHSIO
VCCHSIO
VCCHSIO
VCC1_05
VCC1_05
VCCUSB3PLL
VCCSATA3PLL
RSVD
VCCAPLL
VCCAPLL
DCPSUS3
VCCHDA
DCPSUS2
VCCSUS3_3
VCCSUS3_3
VCCDSW3_3
VCC3_3
VCC3_3
VCCCLK
VCCCLK
VCCACLKPLL
VCCCLK
VCCCLK
VCCCLK
RSVD
RSVD
RSVD
VCCSUS3_3
VCCSUS3_3
VCCSUS3_3
VCCRTC
DCPRTC
VCCSPI
VCCASW
VCCASW
VCC1_05
DCPSUSBYP
VCCASW
DCPSUS1
VCCTS1_5
VCC3_3
VCCSDIO
DCPSUS4
RSVD
VCC1_05
1.838A
1.741A
10mA
25mA
0.114A
41mA
63mA
18mA
0.109A
0.658A
3mA
1mA
17mA
Deep Sx
Non Deep Sx
+1.05V_MODPHY
+1.05V
+V1.05S_AIDLE
+V1.05S_AUSB3PLL
+V1.05S_ASATA3PLL
+V1.05S_APLLOPI
+1.05V_S5
+1.05V_DCPSUS3
+1.05V_DCPSUS2
+V3.3DX_1.5DX_1.8DX_AUDIO
+3VPCU
+3V_S5
+3VCC_S5
+VCCPDSW
+V3.3S_VCCPCORE
+3V
+V1.05S_AXCK_DCB
+V1.05S_AXCK_LCPLL
+3V_RTC
+VCCRTCEXT
+V3.3M_PSPI
PCH_VCC_1_1_21
+V1.05S_CORE_PCH
+1.05V_DCPSUS1
+PCH_VCCDSW
+V1.05M_VCCASW
+1.5V
+V1.5S_VCCATS
+V3.3S_VCCPTS
+V3.3S_VCCSDIO
+1.05V_DCPSUS4
+V1.05S_VCCUSBCORE
WW15 4/10 Intel VCCDSW3
G3 can't boot issue.
C541
0.47u/25V_6
PCH VCCHSIO Power
VCCAPLL power
PCH HDA Power
0.2A
57mA
31mA
11mA
41mA
42mA
L16 2.2uH/210mA_8
L15 2.2uH/210mA_8
L17 2.2uH/210mA_8
L18 2.2uH/210mA_8
L20 2.2uH/210mA_8
R150 *short_6
Place close to ball
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Size
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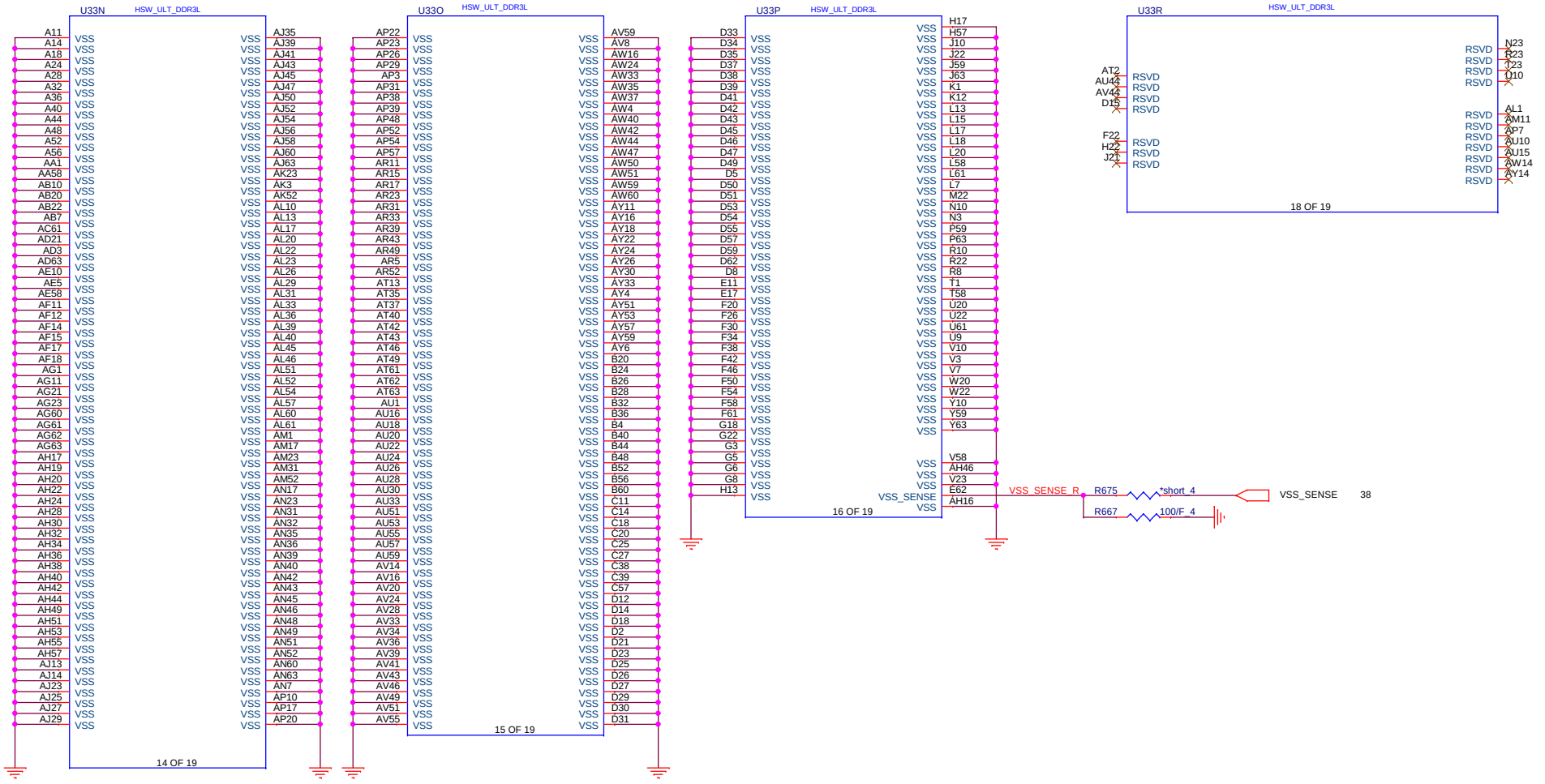
Haswell ULT (GND)



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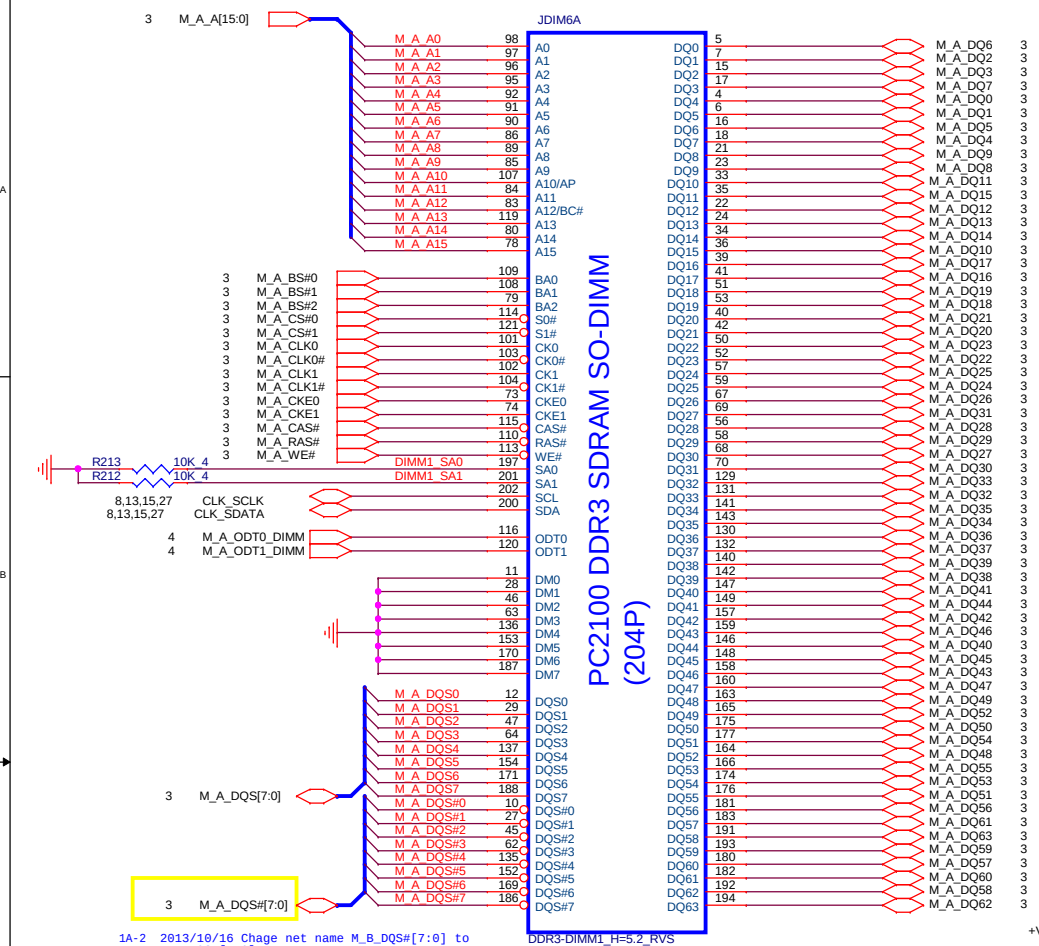
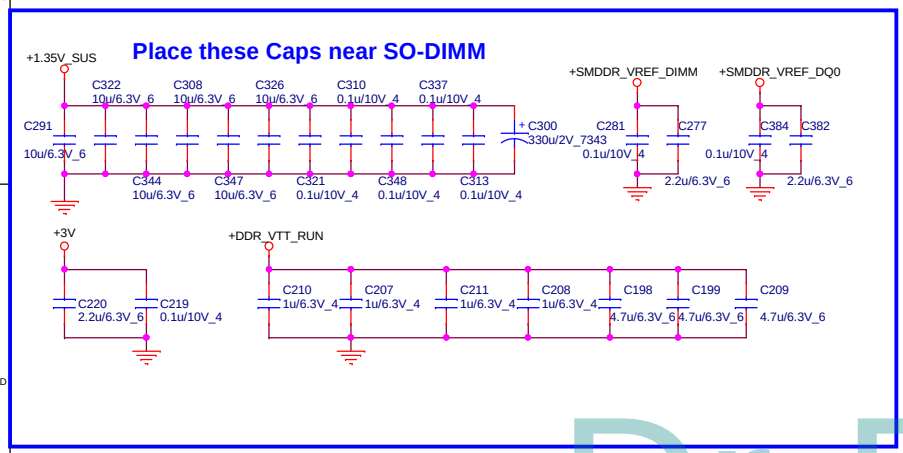
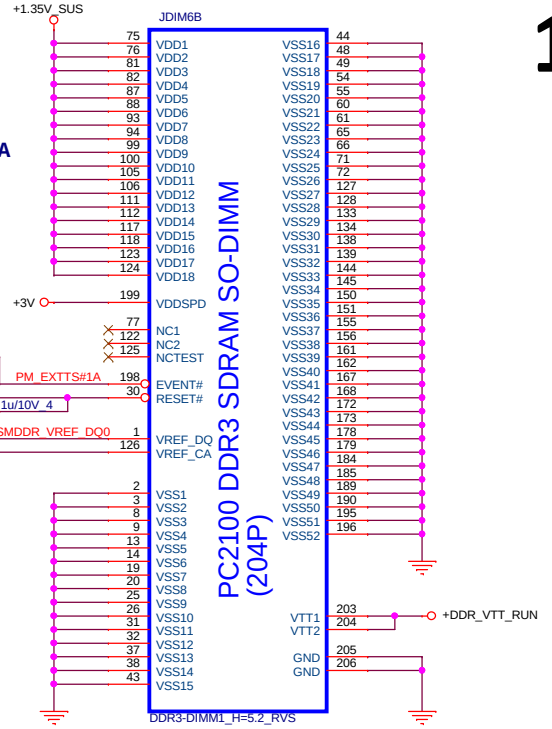
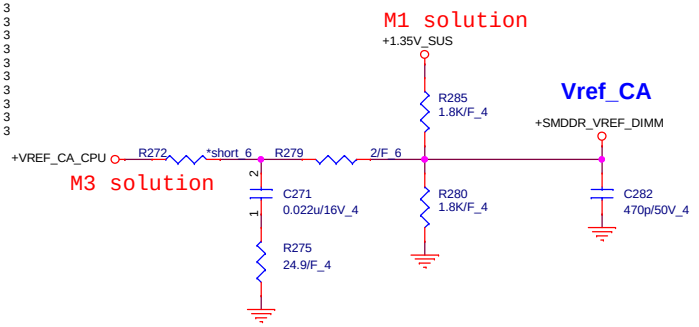
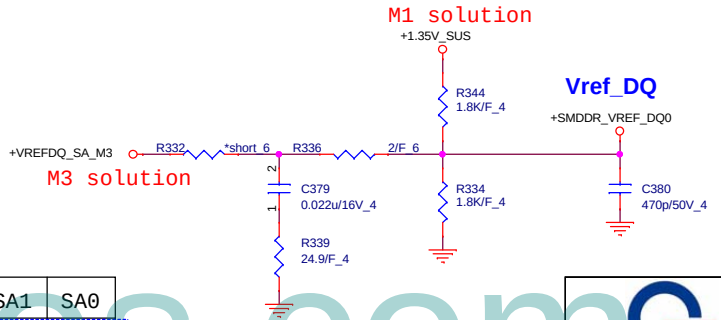


1A-2 2013/10/16 Chage net name M_B_DQS#[7:0] to M_A_DQS#[7:0].









	SA1	SA0
CHA	0	0
CHB	1	0

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Size	Document Number	Rev
	DDR3 MEMORY SO-DIMM A	3A

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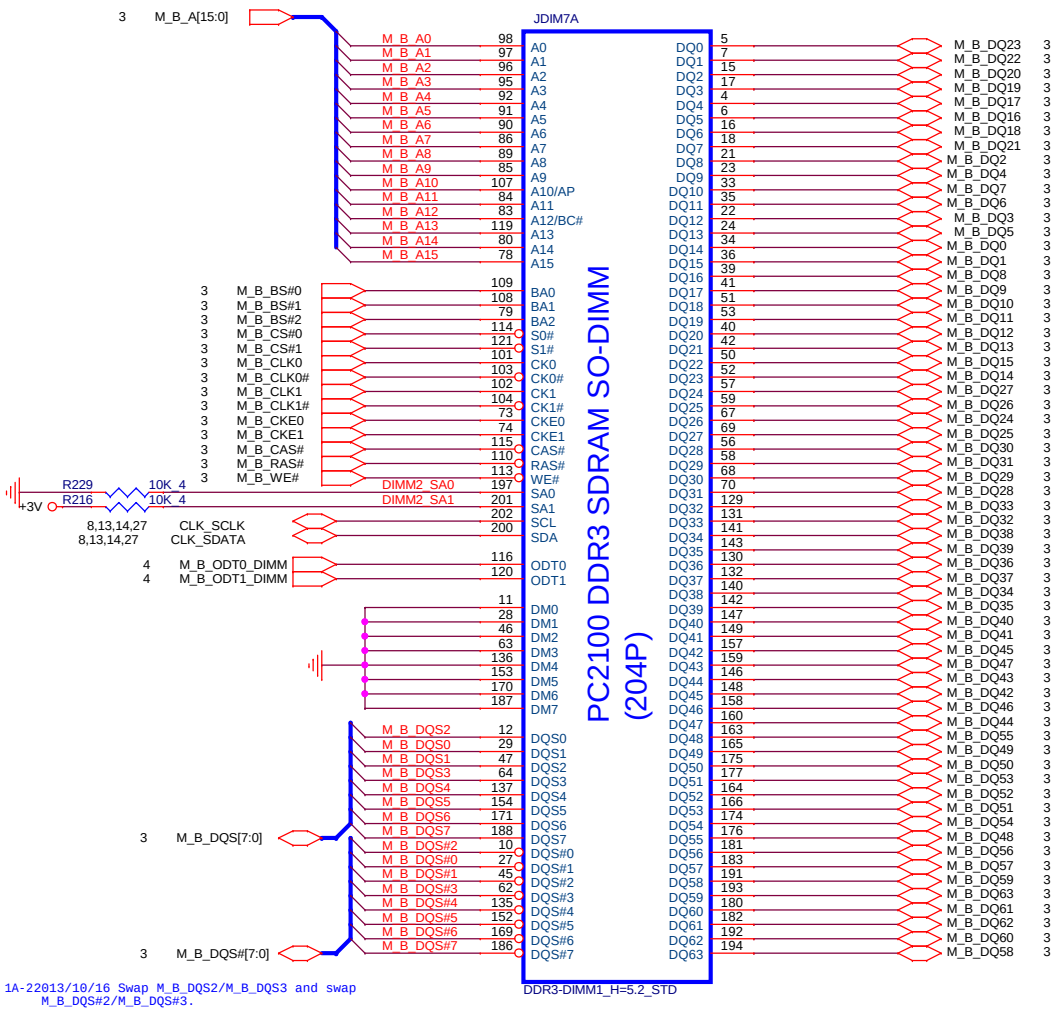
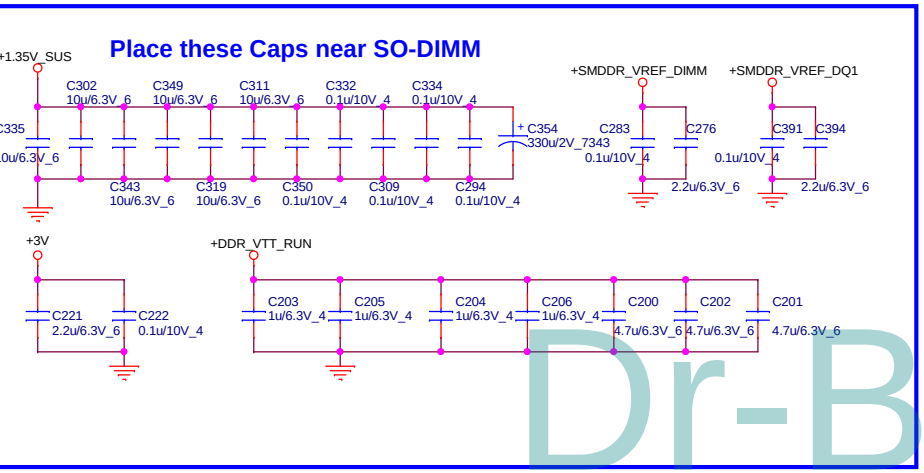
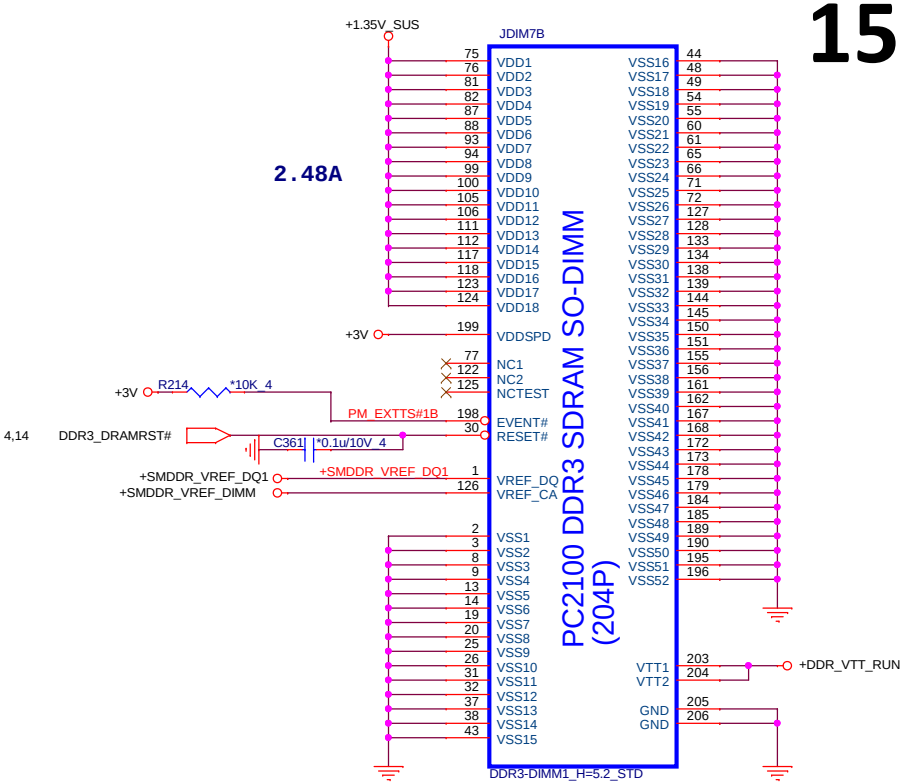
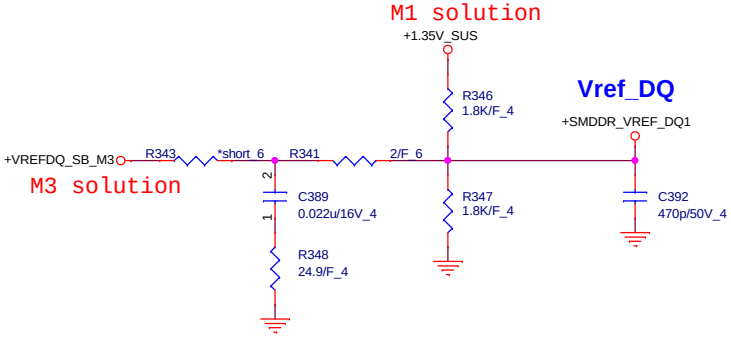


1A-22013/10/16 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.







	SA1	SA0
CHA	0	0
CHB	1	0

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	DDRIII Memory SO-DIMM B	3A
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<VGA>

1000mA

2500mA

210mA of +3V_GFX

PLACE UNDER GPU BALLS

PLACE NEAR GPU

47u x1 | 22u x7 stuff x 1 | 4.7u x6 stuff x 5 | 330u x1 RSVD by DG

4.7uF x 15 population x10

0.1uF x 8 population x 4

0817 RSVD more NVVDD caps by NV DG

not GC6 2.0 unstuff resistor

PLACE CLOSE TO BGA

PLACE CLOSE TO GPU BALLS L8/M8

0.4MM = 16mils

for meet Power down sequence for +3V_GFX

No stuff D8 when GC6 support.

GC6 2.0 PEGX_RST#

PCH control PEGX_RST#

8mils width (0.2MM)

PEX_PLLVDD : 0.3MM = 12mils (150mA)
RSVD R1 and C1 for GV2 co-layout sDDR3

N15x Power on sequance

PEX_RST timing

Trise >= 1uS

Tfail <=500nS

Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

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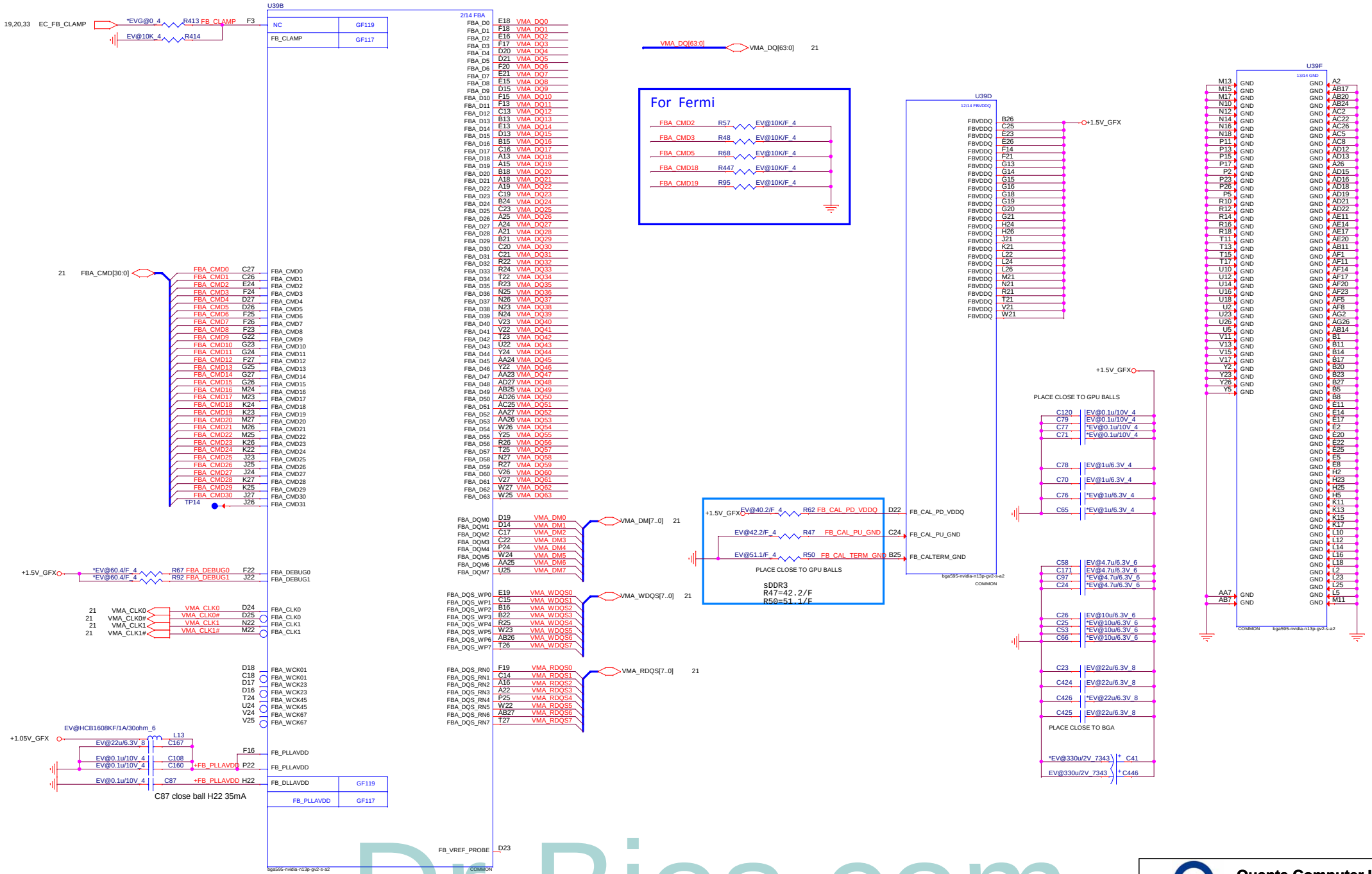
<VGA>



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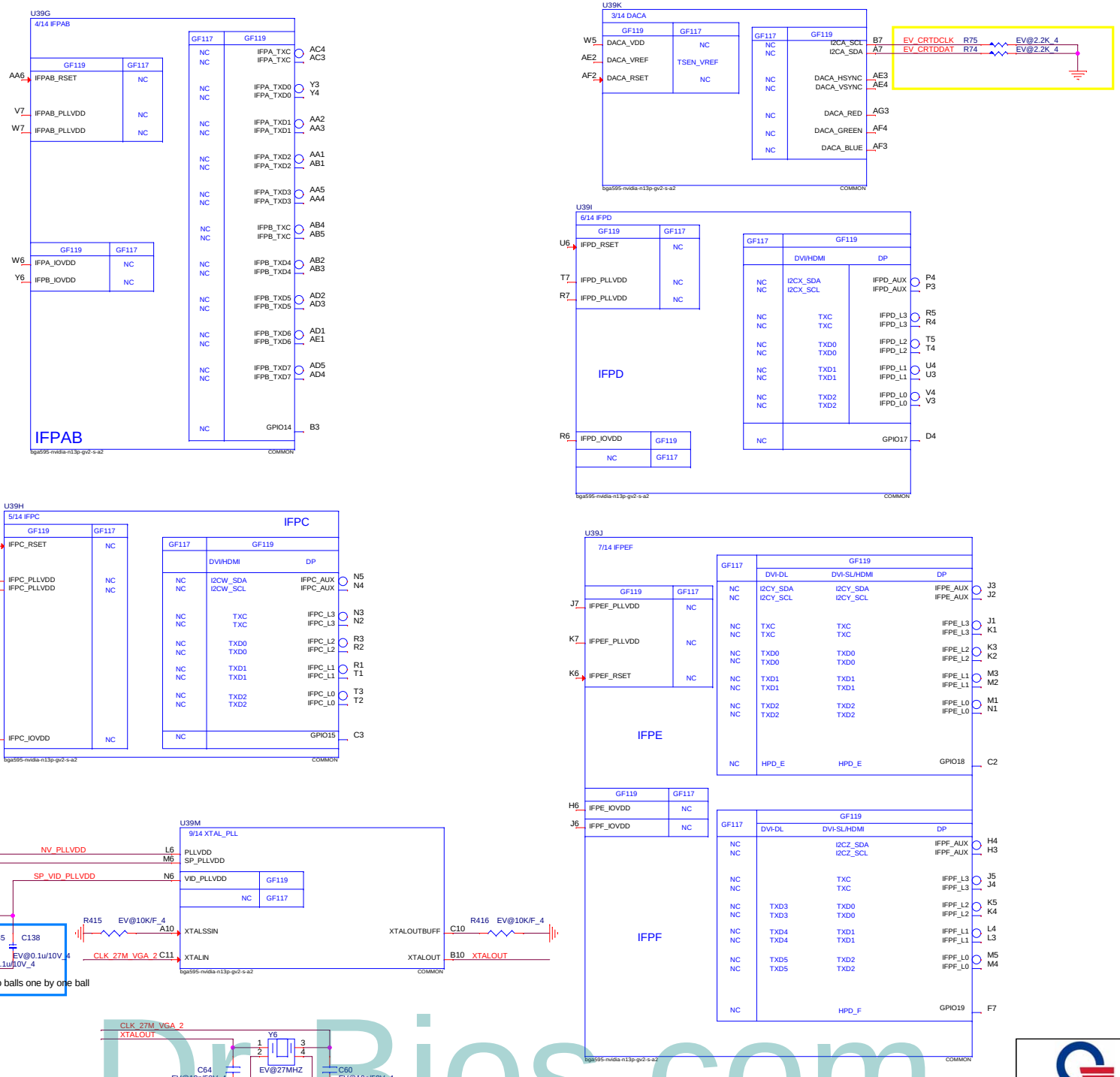
<VGA> <HDM> <CRT>



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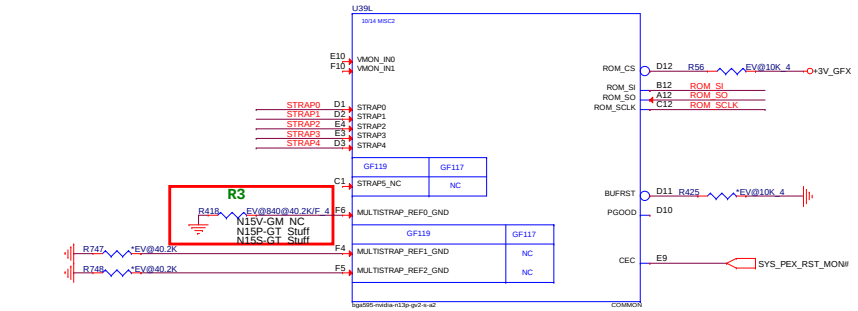
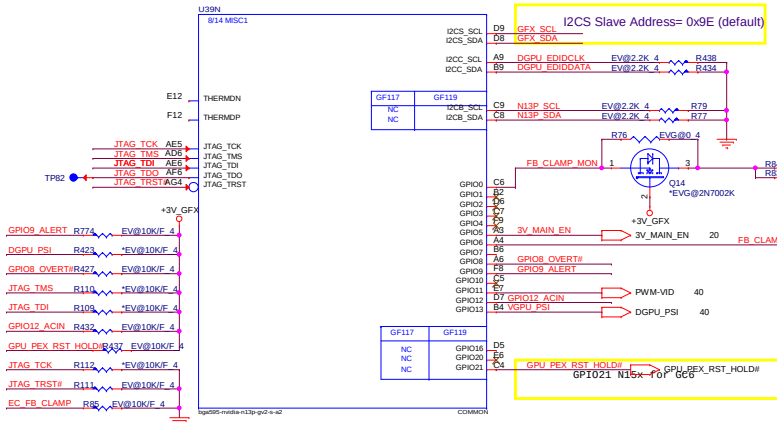
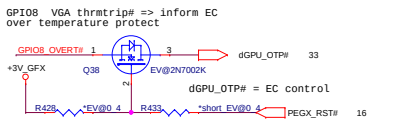
<VGA>

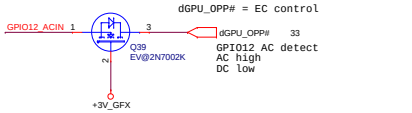
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	1000
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0000
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX SPEED	DP_PLL_VDD33	0111



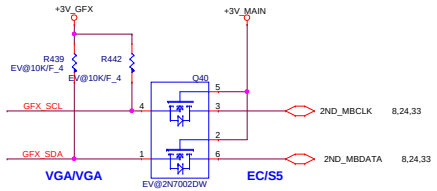


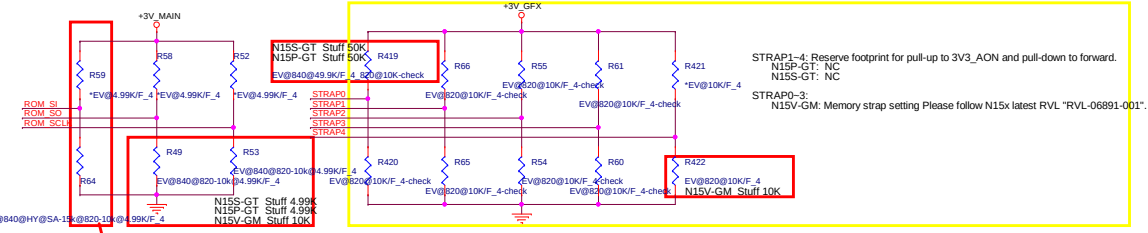


GPIO8 VGA thrmtrip# => inform EC over temperature protect



SMBus(VGA)





ROM_SI:
N15P-GT:
N15S-GT:
Please follow N15x latest RVL
N15V-GM:
Stuff 10K pull down

Mutil-level mode strapping:

For N15P-GT & N15S-GT :

R3=40.3k pull down.
1.ROM_SCLK =4.99K pull down
2.ROM_SO = 4.99K pull down
3.ROM_SI= Memory strap setting
3.STRAP0 = 50k Pull pu.
4.Strap4~1 = reserve Pull up and Pull down

Binary mode strapping:

For N15V-GM-B sku:
Board_ID0=
H=N15V-GM,L=N15V-GL
Device ID=0x1140
R3= N.C.
1.ROM_SCLK =10K pull down.
2.ROM_SI= 10k pull down
3.ROM_SO= 10k pull down
4.Strap3~0 = RVL memory binary mode setting.
5.Strap4 =10k pull down

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

STRAP3
Optimus ---> 4.99k PD

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K---> CS32492FB16
49.9K--> CS34992FB10
30.1K---> CS33012FB18
34.8K---> CS33482FB22
45.3K---> CS34532FB18

N15P-GT/ N15S-GT VRAM Configuration Table

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	
4Gb	0000 (0x0)	DDR3 256MBx16,1000MHz	HYNIX	H5TC4G63AFR-11C		AKD5PGWTW13
	0001 (0x1)	DDR3 256MBx16,1000MHz	MICRON	MT41J256M16HA-093G:E		
	0010 (0x2)	DDR3 256MBx16,1000MHz	SAMSUNG	K4W4G1646D-BC1A		
2Gb	0110 (0x6)	DDR3 128MBx16,1000MHz	HYNIX	H5TC2G63FFR-11C		AKD5MZDTW05
	0111 (0x7)	DDR3 128MBx16,1000MHz	MICRON	MT41J128M16JT-093G:K		
	1000 (0x8)	DDR3 128MBx16,1000MHz	SAMSUNG	K4W2G1646Q-BC1A		

N15V-GM VRAM Configuration Table:

	Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	
4Gb	0100 (0x4)	DDR3 256MBx16,1000MHz	HYNIX	H5TC4G63AFR-11C		
	1101 (0x3)	DDR3 256MBx16,1000MHz	MICRON	MT41J256M16HA-093G:E		
	1001 (0x9)	DDR3 256MBx16,1000MHz	SAMSUNG	K4W4G1646D-BC1A		
2Gb	1110 (0xE)	DDR3 128MBx16,1000MHz	SAMSUNG	K4W2G1646Q-BC1A		
	0001 (0x1)	DDR3 128MBx16,1000MHz	MICRON	MT41J128M16JT-093G:K		
	0101 (0x5)	DDR3 128MBx16,1000MHz	SAMSUNG	K4W2G1646E-BC1A		
	1100 (0xC)	DDR3 128MBx16,1000MHz	HYNIX	H5TC2G63FFR-11C		

	Brand Name	DevID
N15P-GT-A2	GeForce GTX 850M	0x1391
N15S-GT-B-A2	GeForce 840M	0x1341
N15V-GM-B-A2	GeForce 820M	0x1140

	Vendor P/N	QCI P/N
840M	N15S-GT-B-A2	AJ0N15S0T04
820M	N15V-GM-B-A2	AJ0N15V0T03

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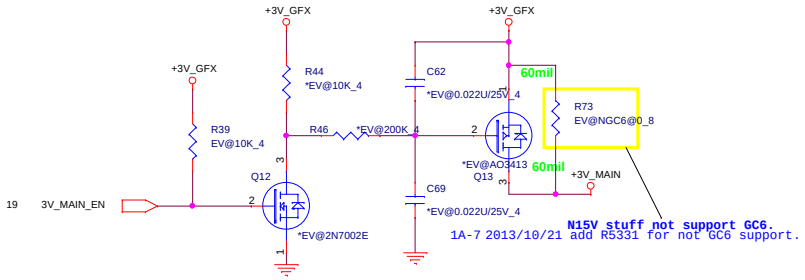
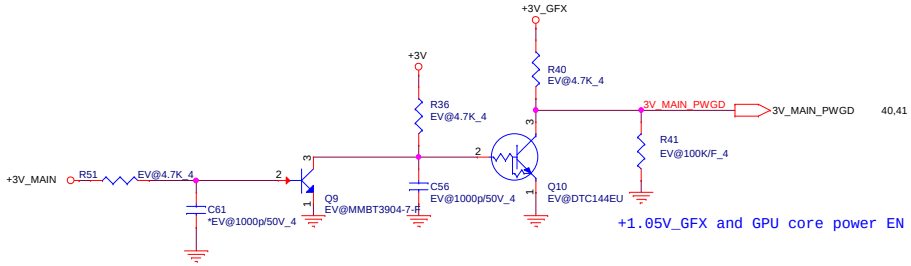
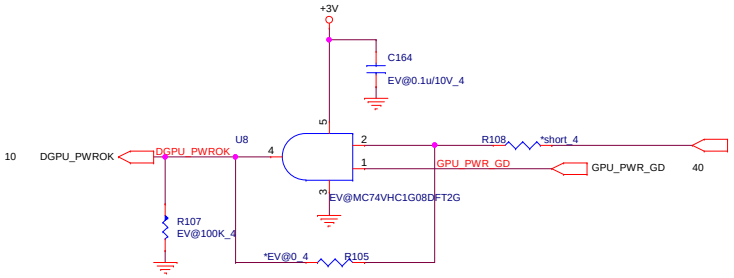
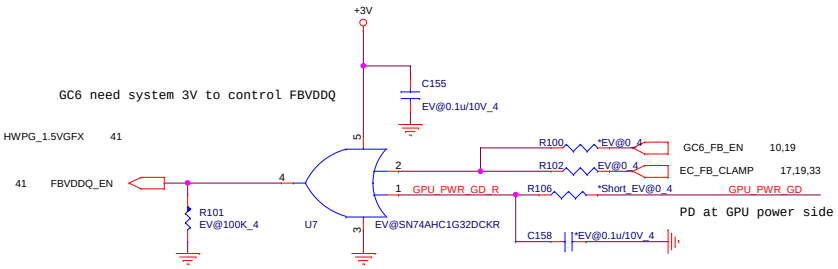
3V MAIN POWER







GC6 need system 3V to control FBVDDQ



PD at GPU power side

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CHANNEL A: 1024MB DDR3X16

17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

VRAM8 / VRAM12 / VRAM9 / VRAM13

VREFC_VMA1 M8
VREFD_VMA1 H1
FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7
FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3
VMA_CLK0 J7
VMA_CLK0# K7
FBA_CMD3 K9
FBA_CMD2 K1
FBA_CMD0 L2
FBA_CMD30 J3
FBA_CMD15 K3
FBA_CMD13 L3
VMA_WDQS1 F3
VMA_RDQS1 G3
VMA_DM1 E7
VMA_DM0 D3
VMA_WDQS0 C7
VMA_RDQS0 B7
FBA_CMD5 T2
VMA_ZQ1 L8
J1 NC#J1
L1 NC#L1
J9 NC#J9
L9 NC#L9

VREFC_VMA1 M8
VREFD_VMA1 H1
FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7
FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3
VMA_CLK0 J7
VMA_CLK0# K7
FBA_CMD3 K9
FBA_CMD2 K1
FBA_CMD0 L2
FBA_CMD30 J3
FBA_CMD15 K3
FBA_CMD13 L3
VMA_WDQS2 F3
VMA_RDQS2 G3
VMA_DM2 E7
VMA_DM3 D3
VMA_WDQS3 C7
VMA_RDQS3 B7
FBA_CMD5 T2
VMA_ZQ2 L8
J1 NC#J1
L1 NC#L1
J9 NC#J9
L9 NC#L9

VREFC_VMA3 M8
VREFD_VMA3 H1
FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7
FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3
VMA_CLK1 J7
VMA_CLK1# K7
FBA_CMD19 K9
FBA_CMD18 K1
FBA_CMD16 L2
FBA_CMD30 J3
FBA_CMD15 K3
FBA_CMD13 L3
VMA_WDQS5 F3
VMA_RDQS5 G3
VMA_DM5 E7
VMA_DM4 D3
VMA_WDQS4 C7
VMA_RDQS4 B7
FBA_CMD5 T2
VMA_ZQ3 L8
J1 NC#J1
L1 NC#L1
J9 NC#J9
L9 NC#L9

VREFC_VMA3 M8
VREFD_VMA3 H1
FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7
FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3
VMA_CLK1 J7
VMA_CLK1# K7
FBA_CMD19 K9
FBA_CMD18 K1
FBA_CMD16 L2
FBA_CMD30 J3
FBA_CMD15 K3
FBA_CMD13 L3
VMA_WDQS7 F3
VMA_RDQS7 G3
VMA_DM7 E7
VMA_DM6 D3
VMA_WDQS6 C7
VMA_RDQS6 B7
FBA_CMD5 T2
VMA_ZQ4 L8
J1 NC#J1
L1 NC#L1
J9 NC#J9
L9 NC#L9

+1.5V_GFX

Should be 240 Ohms +-1%

R63 EV@243/F_4
R426 EV@243/F_4
R94 EV@243/F_4
R446 EV@243/F_4

96-BALL SDRAM DDR3
EV@VRAM _DDR3_HYNIX_256MX16

VMA_CLK0
R45 EV@162/F_4
VMA_CLK0#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

+1.5V_GFX
R429 EV@1.33K/F_4
VREFC_VMA1
R430 EV@1.33K/F_4
C473 EV@0.1u/10V_4

+1.5V_GFX
R38 EV@1.33K/F_4
VREFD_VMA1
R43 EV@1.33K/F_4
C59 EV@0.1u/10V_4

17 FBA_CMD17 TP12
17 FBA_CMD1 TP10
10/14 modify

VMA_CLK1
R96 EV@162/F_4
VMA_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

+1.5V_GFX
R93 EV@1.33K/F_4
VREFC_VMA3
R90 EV@1.33K/F_4
C130 EV@0.1u/10V_4

+1.5V_GFX
R453 EV@1.33K/F_4
VREFD_VMA3
R452 EV@1.33K/F_4
C512 EV@0.1u/10V_4

+1.5V_GFX
C170 EV@1u/10V_4
C517 EV@1u/10V_4
C161 EV@1u/10V_4
C510 EV@1u/10V_4

+1.5V_GFX
C75 EV@10u/6.3V_6
C528 EV@1u/10V_4
C471 EV@1u/10V_4
C505 EV@1u/10V_4
C467 EV@1u/10V_4
C54 EV@1u/10V_4

+1.5V_GFX
C458 EV@10u/6.3V_6
C466 EV@1u/10V_4
C514 EV@1u/10V_4
C163 EV@1u/10V_4
C83 EV@1u/10V_4
C149 EV@1u/10V_4
C55 EV@1u/10V_4
C468 EV@1u/10V_4

+1.5V_GFX
C518 EV@10u/6.3V_6
C166 EV@10u/6.3V_6
C465 EV@0.1u/10V_4
C470 EV@0.1u/10V_4
C527 EV@0.1u/10V_4
C469 EV@0.1u/10V_4
C151 EV@0.1u/10V_4

+1.5V_GFX
C51 EV@10u/6.3V_6
C457 EV@10u/6.3V_6
C509 EV@0.1u/10V_4
C156 EV@0.1u/10V_4
C57 EV@0.1u/10V_4

Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	N15P- DDR3 VRAM 1/2	3A
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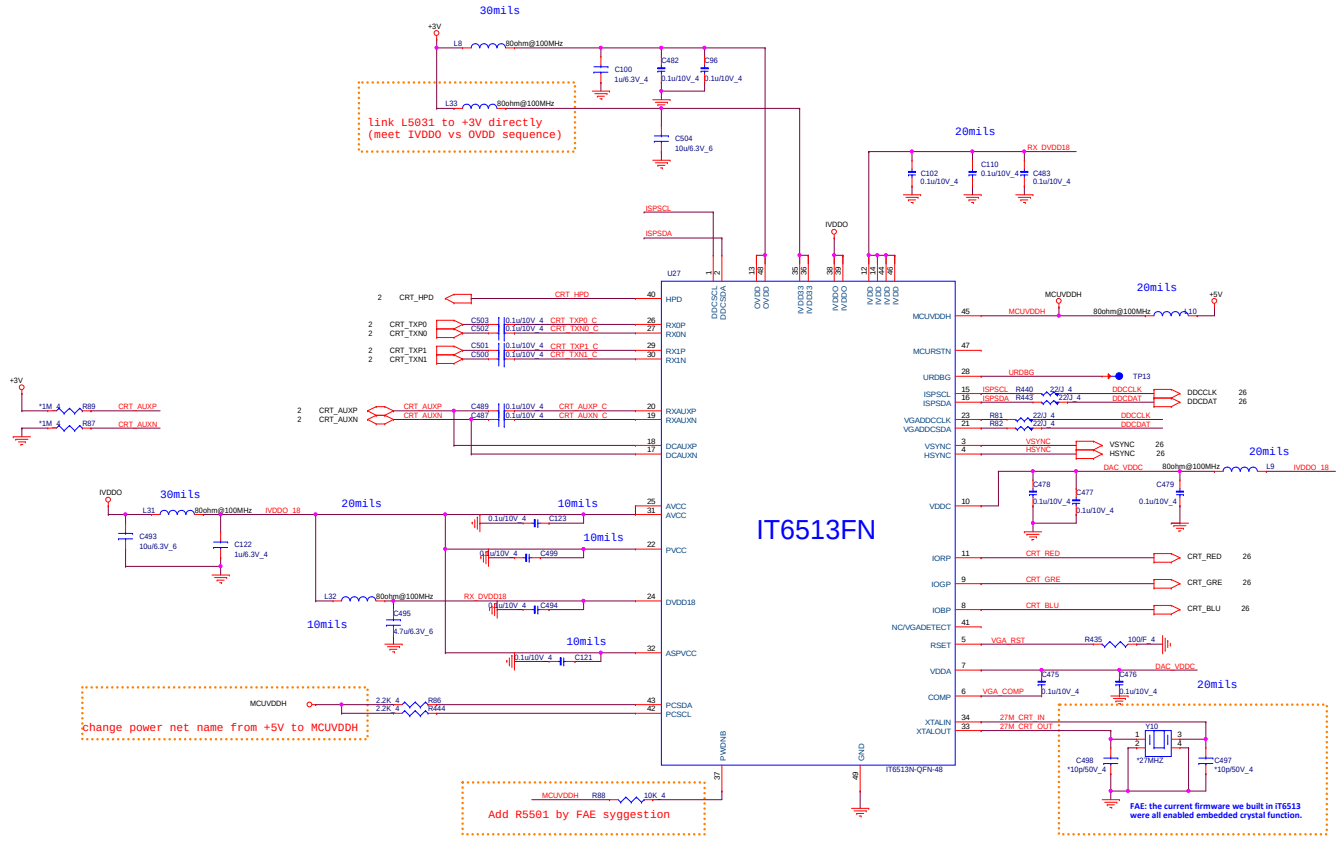
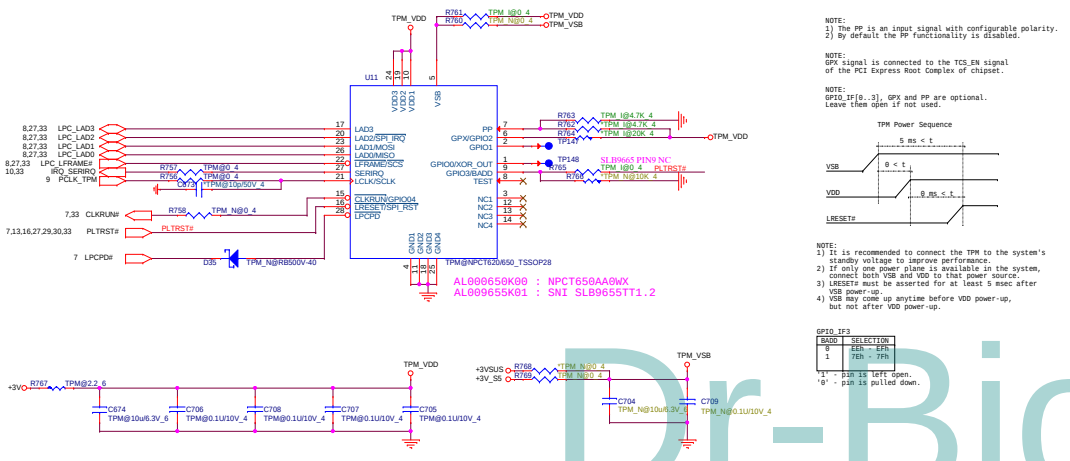
Quanta Computer Inc.		
PROJECT : ZYW		
Size	Document Number: N13P DDR3 VRAM 2/2	Rev: 3A
Date: Tuesday, April 29, 2014	Sheet 22 of 46	

DP TO VGA



TPM (TPM)



NPCT650AA0WX infromation:

NOTE:
1) The PP is an input signal with configurable polarity.
2) By default the PP functionality is disabled.

NOTE:
GPX signal is connected to the TCS_EN signal
of the PCI Express Root Complex of chipset.

NOTE:
GPIO_IF[0..3], GPX and PP are optional.
Leave them open if not used.

TPM Power Sequence

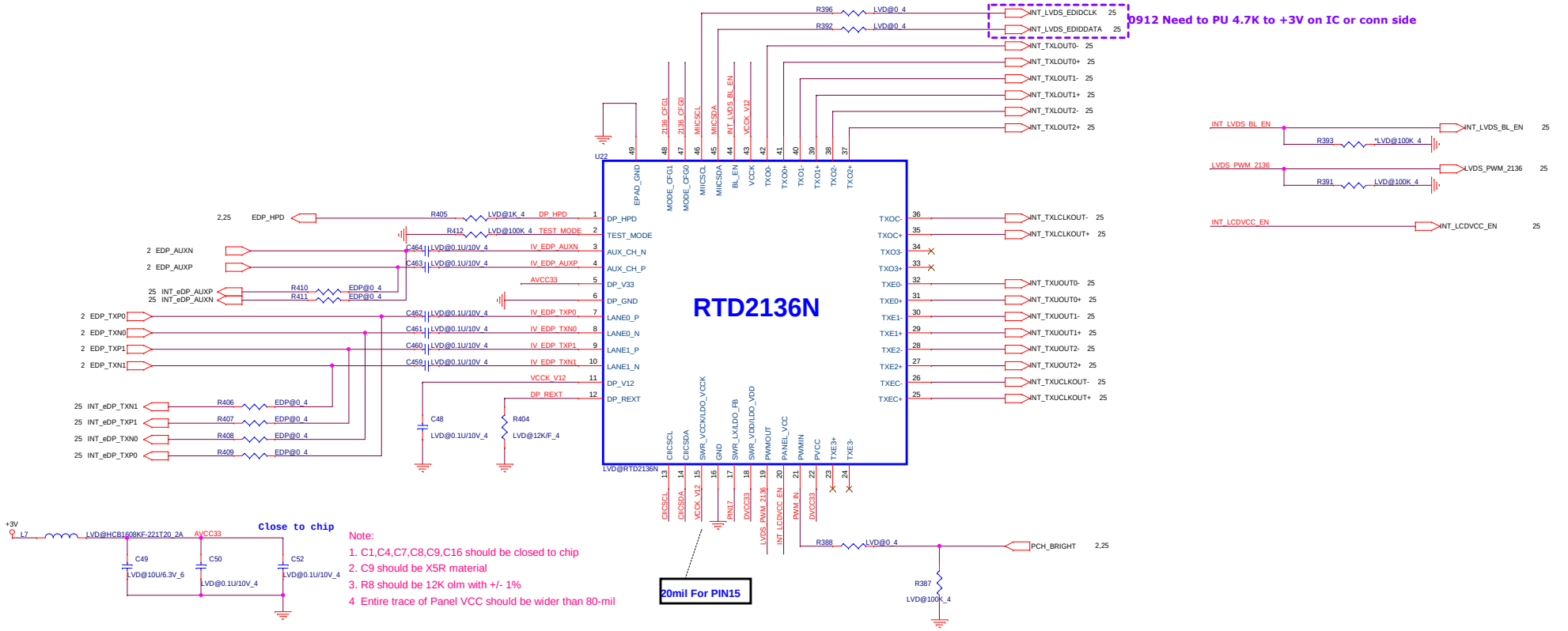
NOTE:
1) It is recommended to connect the TPM to the system's standby voltage to improve performance.
2) If only one power plane is available in the system, connect both VSB and VDD to that power source.
3) LRESET# must be asserted for at least 5 msec after VSB power-up.
4) VSB may come up anytime before VDD power-up, but not after VDD power-up.

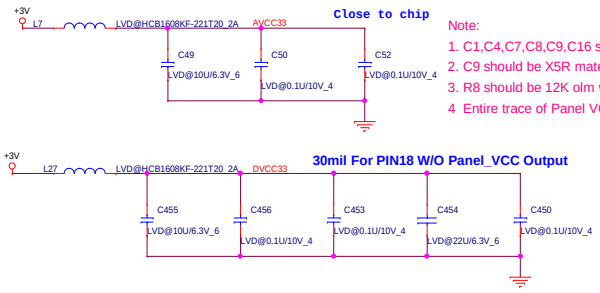
GPIO_IF3

BADD	SELECTION
0	EEh ~ EFh
1	7Eh ~ 7Fh

'1' - pin is left open.
'0' - pin is pulled down.

Quanta Computer Inc.
PROJECT : ZYW
Size | Document Number: Mini DP/HD3SS2521 | Rev 3A
Date: Tuesday, April 29, 2014 | Sheet 23 of 46



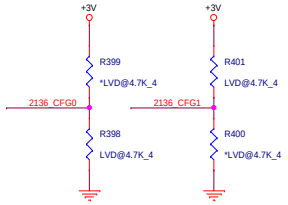


Note:
1. C1,C4,C7,C8,C9,C16 should be closed to chip
2. C9 should be X5R material
3. R8 should be 12K olm with +/- 1%
4 Entire trace of Panel VCC should be wider than 80-mil

Mode Configure Table(Power On Latch)

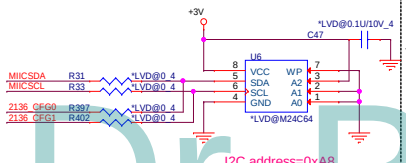
		CFG0	
		0	1
CFG1	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

ROM ONLY Mode : CFG0 4.7K pull low, CFG1 4.7K pull high
EP Mode : CFG0 4.7K pull high, CFG1 4.7K pull low
EEPROM Mode : CFG0 4.7K pull high, CFG1 4.7K pull high



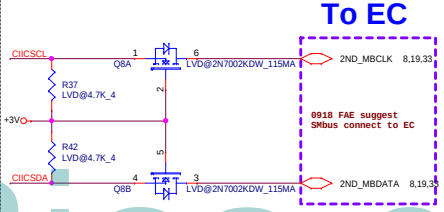
EEPROM Mode
In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.

1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8



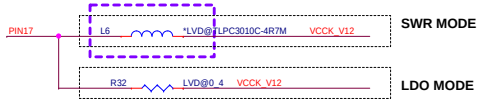
EP Mode
External device connect to DP2LVDS by
Pin13/Pin14, I2C protocol is used

Address=0x94&96x6A

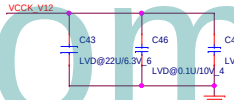


Dual Mode Regulator Configuration

	2.2-uH(L6)	0 Olm(R31)
SWR	Connect	NC
LDO	NC	Connect



1. C18 10-uF capacitor should be X5R material
2. Inductor should be withstand current >600-mA
3. Capacitors should be closed to PIN17



Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	eDP to LVDS	3A
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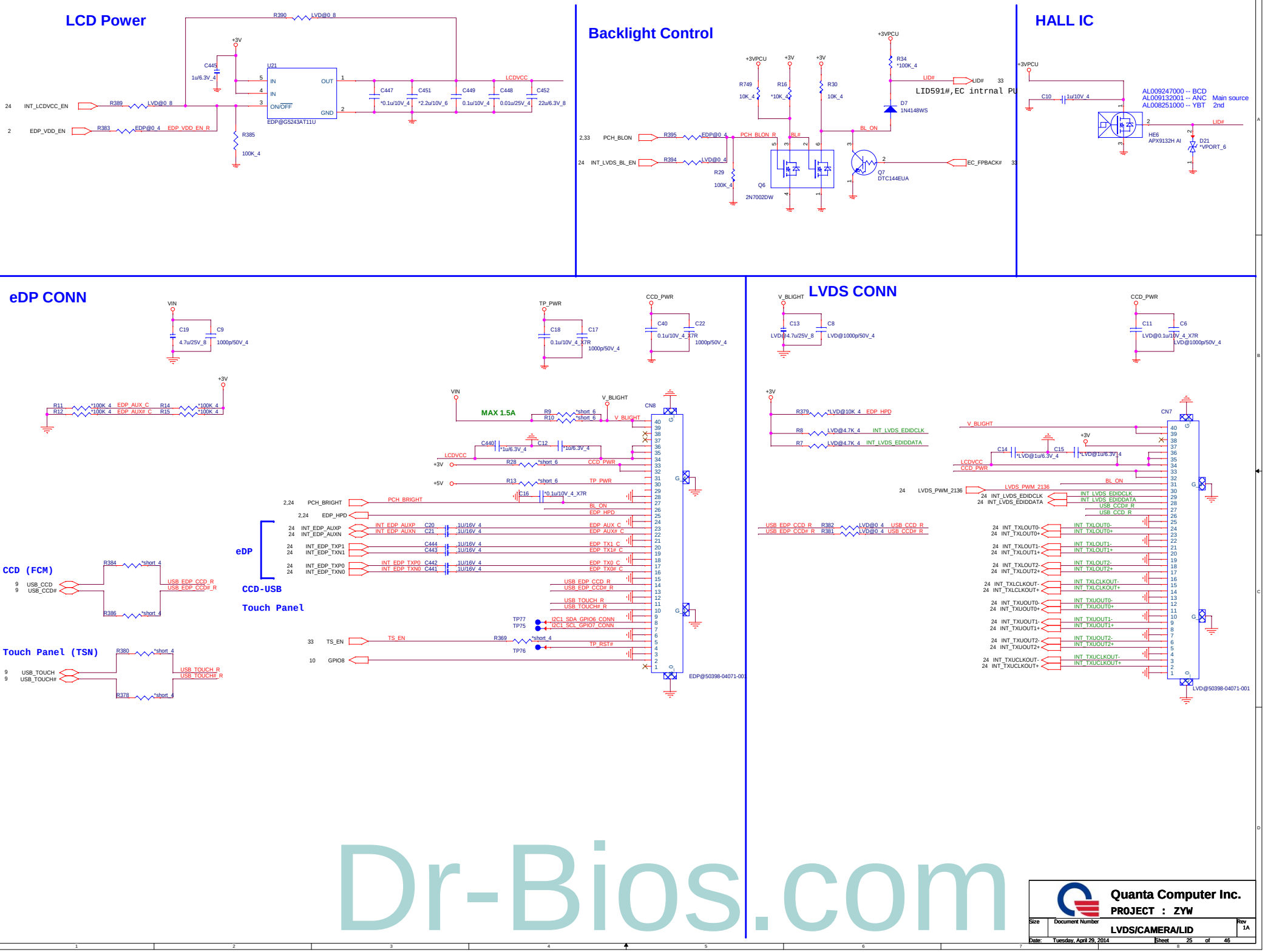
LCD Power
Backlight Control
HALL IC
eDP CONN
LVDS CONN
CCD (FCM)
Touch Panel (TSN)
Touch Panel
CCD-USB
eDP
MAX 1.5A
LID591#,EC intrnal PU
AL009247000 -- BCD
AL009132001 -- ANC Main source
AL008251000 -- YBT 2nd
EDP@G5243AT11U
EDP@50398-04071-001
LVD@50398-04071-001
Quanta Computer Inc.
PROJECT : ZYW
LVDS/CAMERA/LID
Tuesday, April 29, 2014
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HDMI

From PCH

INT_HDMITX2N
INT_HDMITX2P
INT_HDMITX1N
INT_HDMITX1P
INT_HDMITX0N
INT_HDMITX0P
INT_HDMICLK+
INT_HDMICLK-

C552 0.1u/10V_4 INT_HDMITX2N_C
C553 0.1u/10V_4 INT_HDMITX2P_C
C548 0.1u/10V_4 INT_HDMITX1N_C
C550 0.1u/10V_4 INT_HDMITX1P_C
C559 0.1u/10V_4 INT_HDMITX0N_C
C561 0.1u/10V_4 INT_HDMITX0P_C
C547 0.1u/10V_4 INT_HDMICLK+_C
C546 0.1u/10V_4 INT_HDMICLK-_C

R574 R576 R246 R243 R232 R230 R239 R236 470_4

EMI

INT_HDMITX2P_C — R583 *120/F_4 — INT_HDMITX2N_C
INT_HDMITX1P_C — R580 *120/F_4 — INT_HDMITX1N_C
INT_HDMITX0P_C — R594 *120/F_4 — INT_HDMITX0N_C
INT_HDMICLK+_C — R575 *120/F_4 — INT_HDMICLK-_C

+3V — R581 *100K/F_4 — Q45 2N7002K

+5V — Q22 AP2331SA-7 — C213 *220p/50V_4 — D13 *EGA_4

HDMI connector

CN12 HDMI connector

INT_HDMITX2P_C	1	D2+	
	2	D2 Shield	
INT_HDMITX2N_C	3	D2-	
INT_HDMITX1P_C	4	D1+	
	5	D1 Shield	
INT_HDMITX1N_C	6	D1-	
INT_HDMITX0P_C	7	D0+	
	8	D0 Shield	
INT_HDMITX0N_C	9	D0-	
INT_HDMICLK+_C	10	CK+	
	11	CK Shield	
INT_HDMICLK-_C	12	CK-	
	13	CE Remote	
	14	NC	
HDMI_DDCCLK_MB	15	DDC CLK	
HDMI_DDCDATA_MB	16	DDC DATA	
HDMI_5V	17	GND	
	18	+5V	
	19	HP DET	
	20	SHELL1	
	23	GND	
	22	GND	
	21	SHELL2	

HDMI_MB_HPD — R192 *short_4 — HP_DET_CN — R178 20K_4 — D24 D25 D23 *EGA_4

I2C

+3V — R557 2.2K_4 — Q43 2N7002K — R554 2.2K_4 — D11 RB501V-40 — +5V — HDMI_DDCCLK_MB

+3V — R571 2.2K_4 — Q44 2N7002K — R567 2.2K_4 — D12 RB501V-40 — +5V — HDMI_DDCDATA_MB

HDMI-detect

+3V — R203 1M_4 — Q20 2N7002K — HDMI_MB_HPD

INT_HDMI_HPD

From PCH

HDMI_DDCCLK_SW
HDMI_DDCDATA_SW

Power trace tracking

2,5,7,8,9,10,11,13,14,15,16,20,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,41 +3V
23,25,26,28,31,32,35,39 +5V

+5V — Q16 AP2331SA-7 — C95 *0.1u/10V_4 — CRTVDD5

23 CRT_RED — L30 BLM18BB470_6 — CRT_R1
23 CRT_GRE — L29 BLM18BB470_6 — CRT_G1
23 CRT_BLU — L28 BLM18BB470_6 — CRT_B1

R445 75/F_4 R441 75/F_4 R436 75/F_4 C488 5.6p/16V_4 C485 5.6p/16V_4 C480 5.6p/16V_4 C481 5.6p/16V_4 C484 5.6p/16V_4 C486 5.6p/16V_4

CN9 CRT CONN

CRT_R1	1	CRT_11 — TP11
CRT_G1	2	DDCDAT — DDCDAT 23
CRT_B1	3	CRTHSYNC
	4	CRTVSYNC
	5	DDCCLK — DDCCLK 23
	6	
	7	
	8	
	9	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	

DDCDAT — 2.2K_4 — R424 — CRTVDD5
DDCCLK — 2.2K_4 — R431

+5V — C85 0.1u/10V_4 — U40 M74VHC1GT125DF2G — 23 HSYNC — HSYNC — CRTHSYNC

+5V — C668 0.1u/10V_4 — U41 M74VHC1GT125DF2G — 23 VSYNC — VSYNC — CRTVSYNC

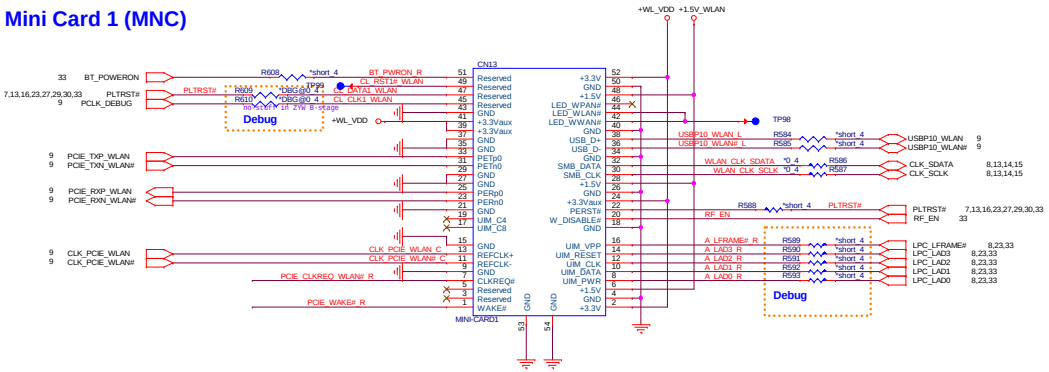
C68 0.22u/6.3V_4
C72 *220p/50V_4
C82 0.1u/10V_4 CRTVDD5
C63 10p/50V_4 CRTVSYNC
C86 10p/50V_4 CRTHSYNC
C474 *10p/50V_4 DDCCLK
C472 *10p/50V_4 DDCDAT

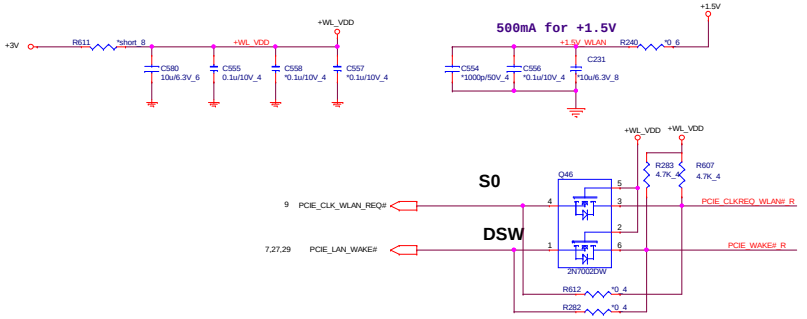
Power trace tracking

2,5,7,8,9,10,11,13,14,15,16,20,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,41 +3V
23,25,26,28,31,32,35,39 +5V

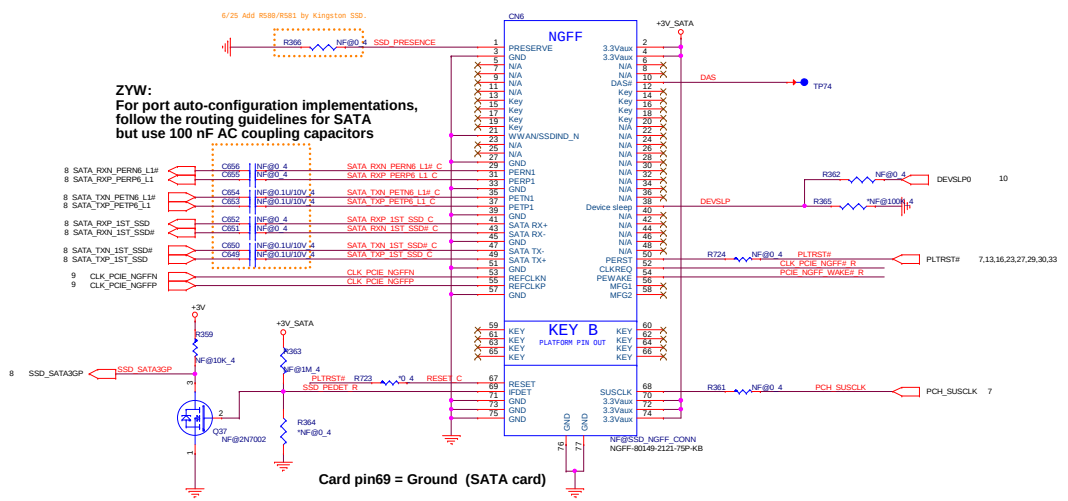
Quanta Computer Inc.		
PROJECT : ZYW		
Size	Document Number: HDMI (PS8101)	Rev 1A
Date: Tuesday, April 29, 2014	Sheet 26 of 46	

Mini Card 1 (MNC)

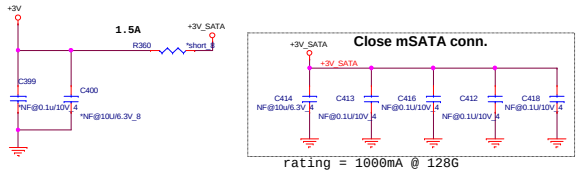


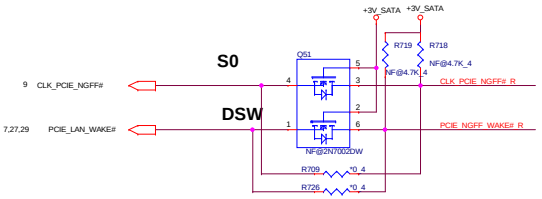


NGFF (NGF)



pin	Type	Description
1	PRESENCE	This pin is grounded on the SSD. May be used by host to determine if slot is empty or populated
10	DAS#	Device Activity Signal
21	WWAN/SSDIND_N	This pin connect to Ground
38	Device Sleep Signal	If system didn't support DEVSLP, set DEVSLP Sleep Signal pin power high and keep (from power on), device will ignore. If system support DEVSLP, set DEVSLP Sleep Signal pin power low (from power on) device, device will support DEVSLP function. Device Sleep Signal H: SSD enter sleep model. Device Sleep Signal L: SSD exit sleep model.
53	REFCLKN	no connect on SSD
55	REFCLKP	no connect on SSD
56	MFG1	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
58	MFG2	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
68	SUSCLK	no connect on SSD
69	IFDET	This pin connect to Ground



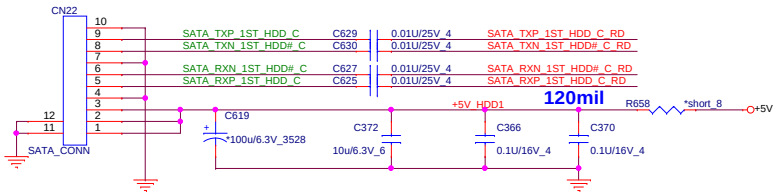


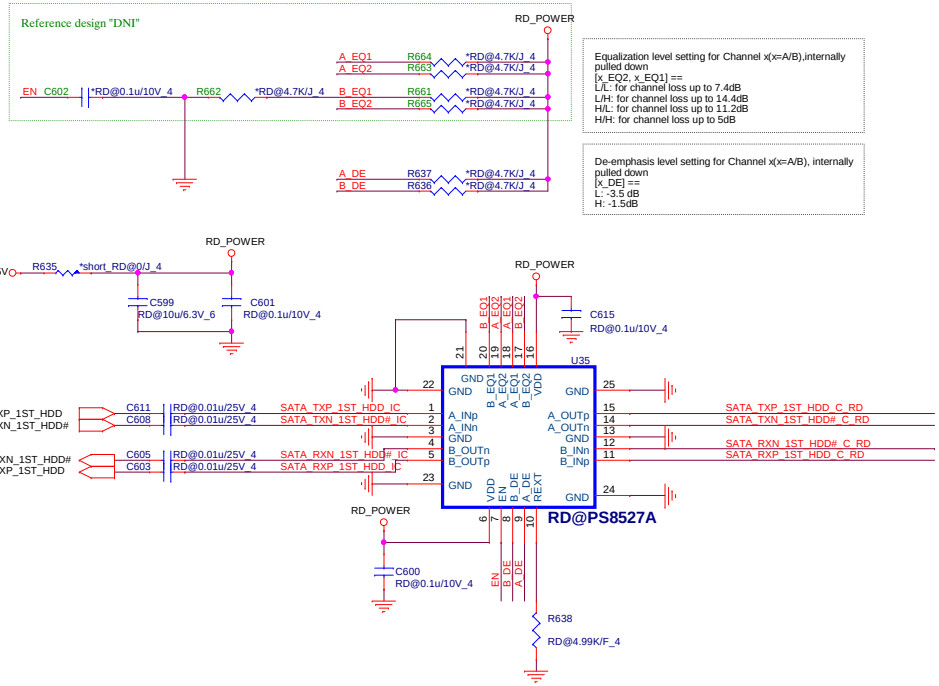
Quanta Computer Inc.	
PROJECT : ZYW	
Size	Document Number: Mini-Card/NGFF — Rev: 1A
Date: Tuesday, April 29, 2014	Sheet 27 of 46

SATA HDD1

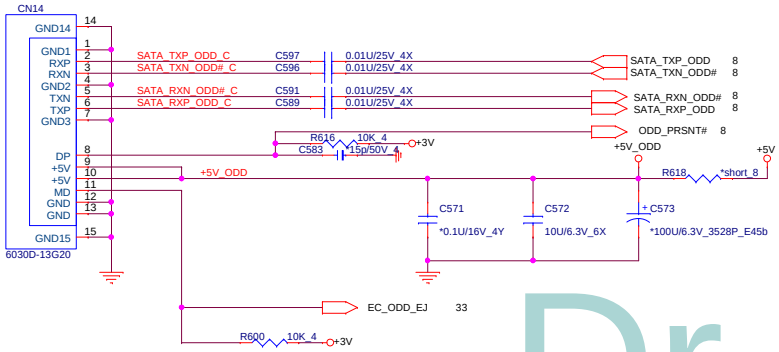
HDD1 SATA Re-driver

HDD1





ODD



Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	SATA HDD/LED/SW	1A
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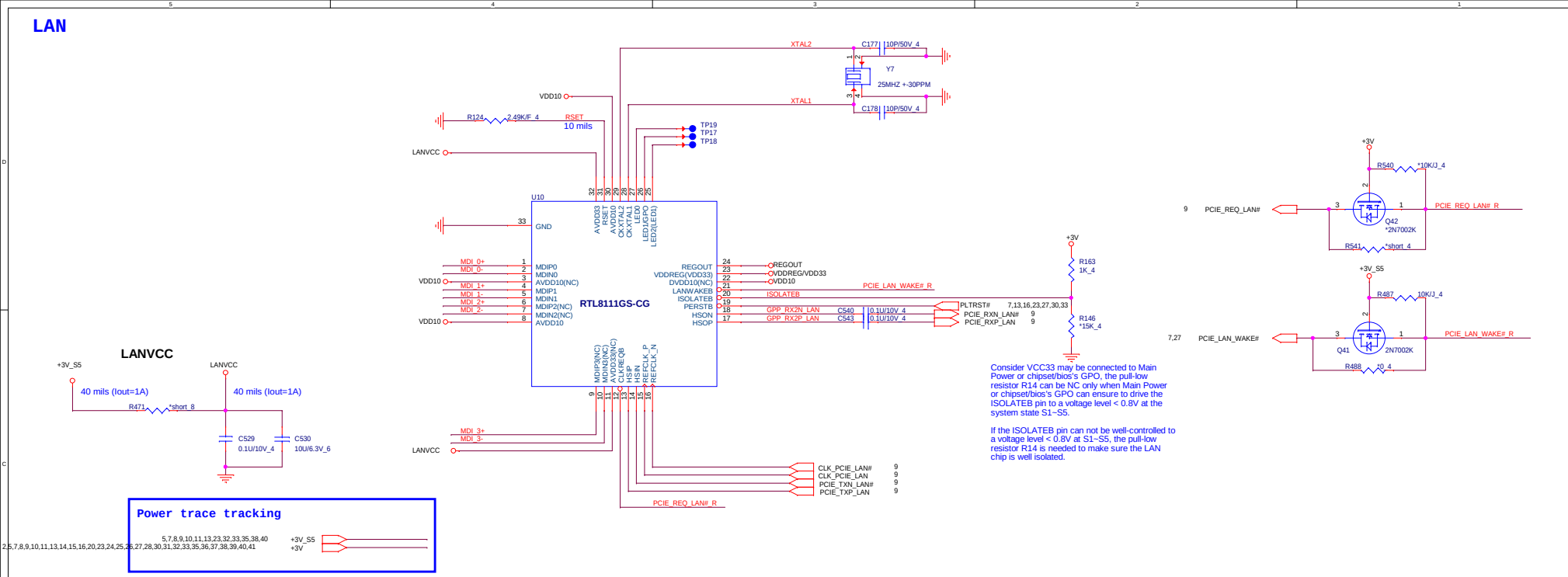
LAN

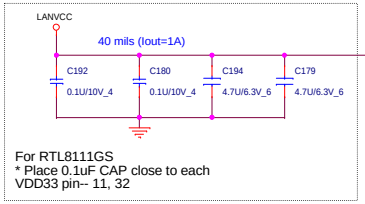


Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S1~S5.

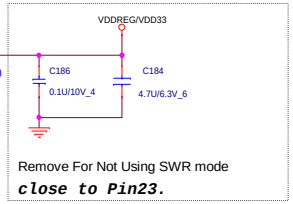
If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S1~S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

Power trace tracking

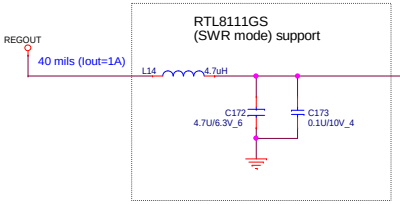
5,7,8,9,10,11,13,23,32,33,35,38,40 +3V_S5
2,5,7,8,9,10,11,13,14,15,16,20,23,24,25,26,27,28,30,31,32,33,35,36,37,38,39,40,41 +3V

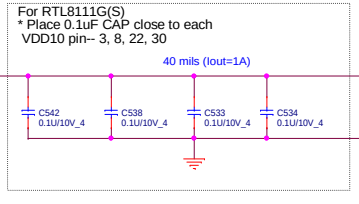


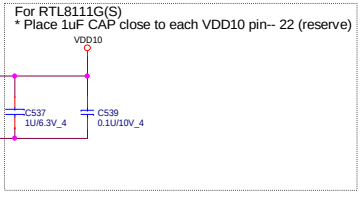
For RTL8111GS
* Place 0.1uF CAP close to each VDD33 pin-- 11, 32



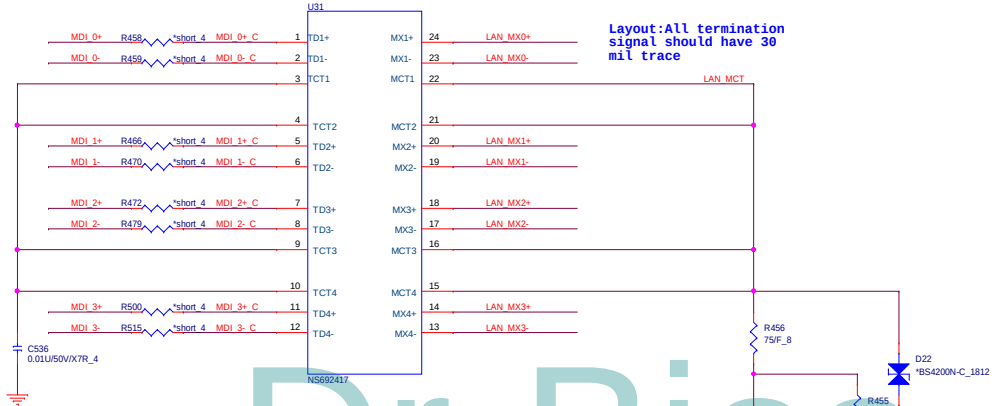
Remove For Not Using SWR mode
close to Pin23.





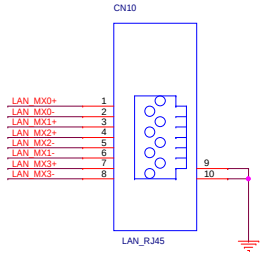


Tramsformer



Layout:All termination signal should have 30 mil trace

RJ45 Connector



Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	LAN	F3A

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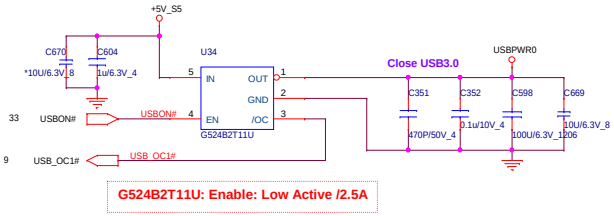
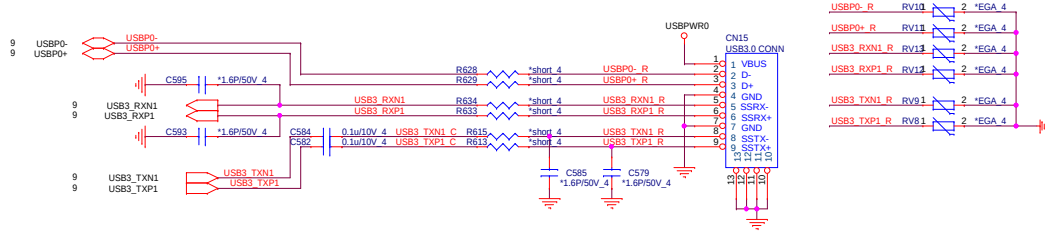
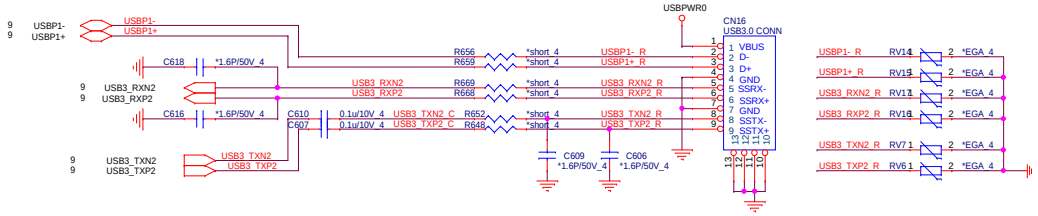
USB3.0 (UB3)

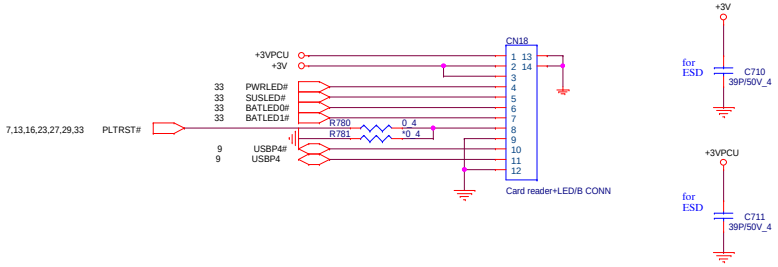


G524B2T11U: Enable: Low Active /2.5A

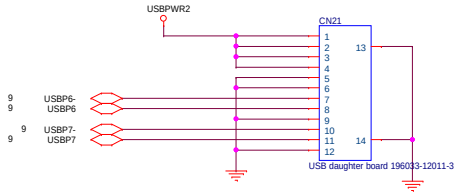


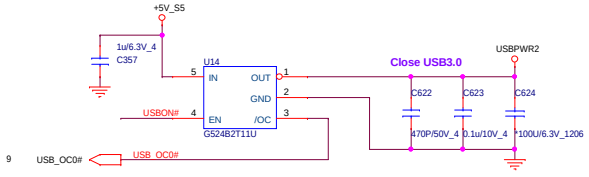


Card Reader+ LED/B Connector



USB D/B (UB2)

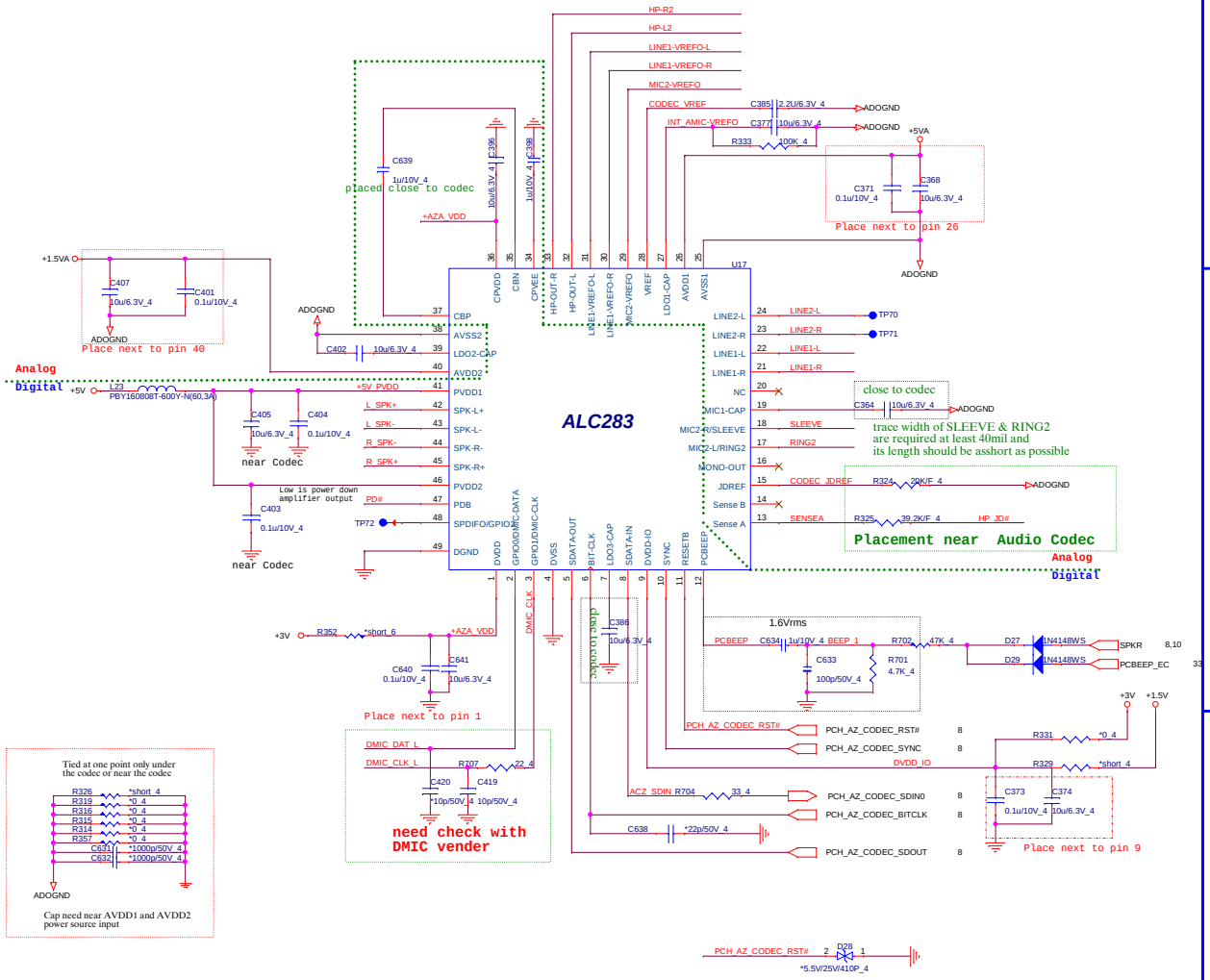




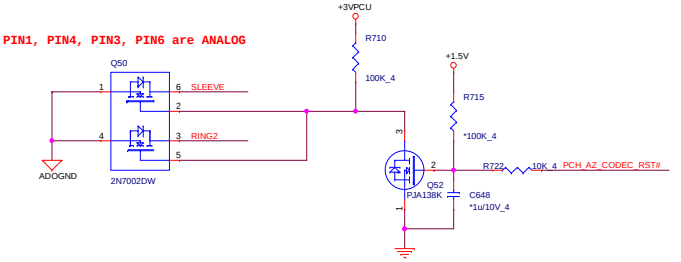
G524B2T11U: Enable: Low Active /2.5A

Quanta Computer Inc.		
PROJECT : ZYW		
Size	Document Number: USB3(S&C)	Rev: F3A
Date: Tuesday, April 29, 2014	Sheet 29 of 46	

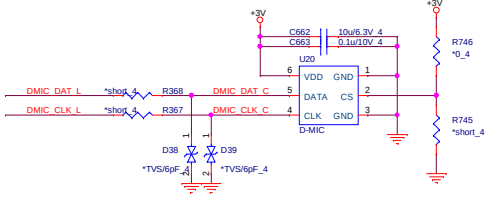
Codec(ADO)



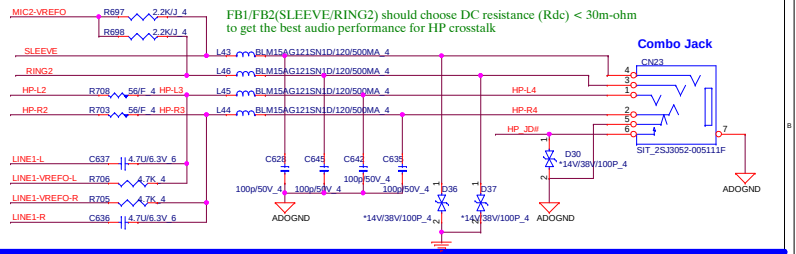
Grounding circuit(ADO)



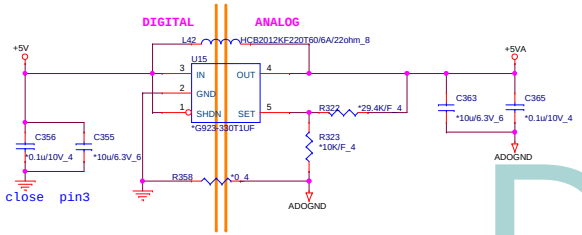
D-Mic



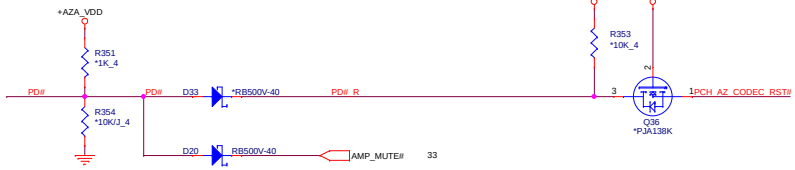
HEADPHONE/MIC/LINE combo (AMP)



Codec PWR 5V(ADO)



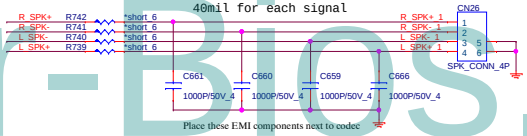
Mute(ADO)



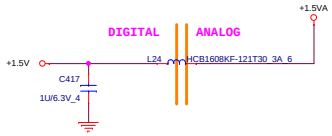
Level shift

Internal Speaker

Need Check P/N and F/P



Codec PWR 1.5V(ADO)



Quanta Computer Inc.		
PROJECT : ZYW		
Size	Document Number: Audio	Rev: F3A
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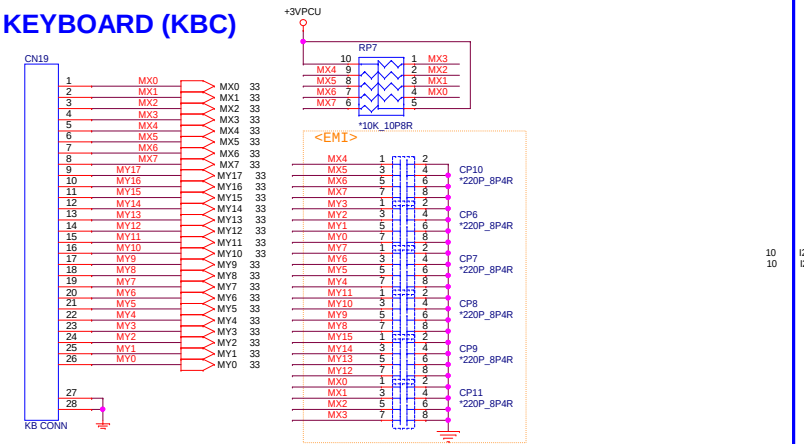
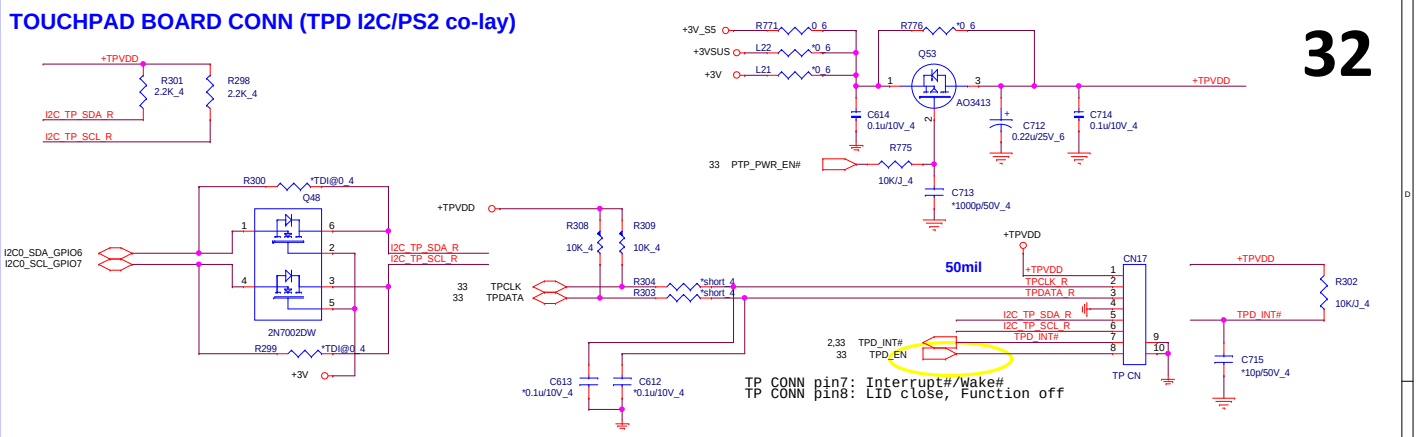
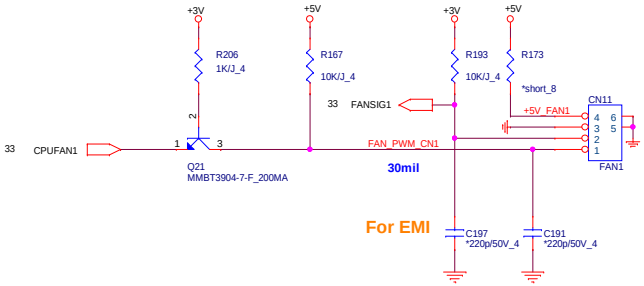
KEYBOARD (KBC)

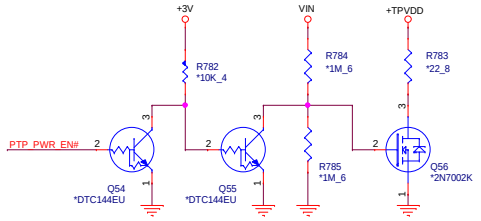


TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

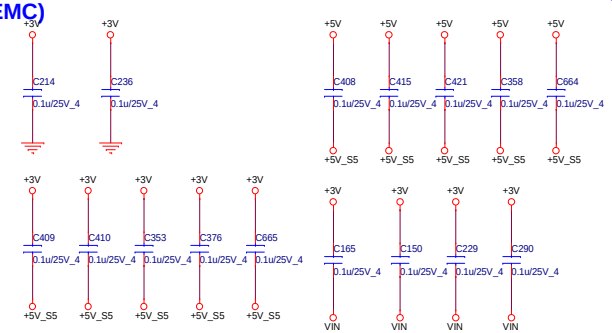


FAN1 For CPU (THM)

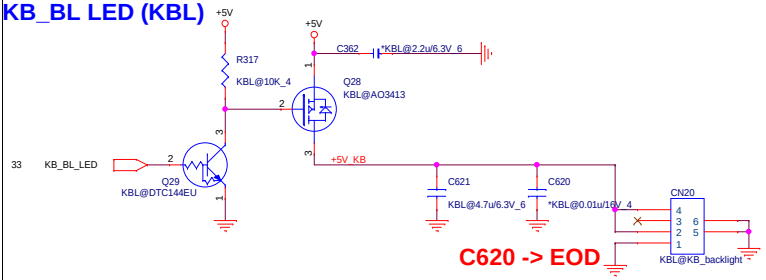




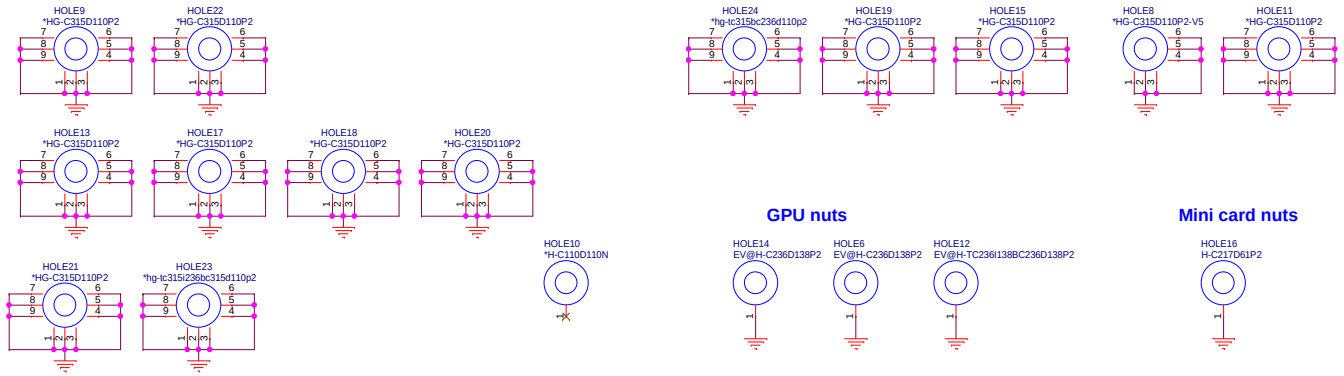
Stitch Caps (EMC)



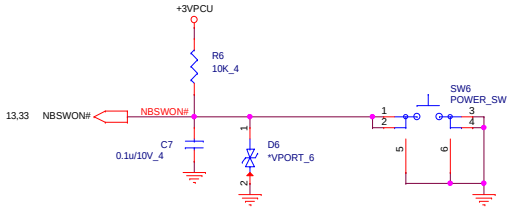
KB_BL LED (KBL)



NUT (OTH)



Power Switch. (FSW)



Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	KB/TP/FAN	3A

Date: Tuesday, April 29, 2014 Sheet 32 of 46

EC(KBC)

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

12 mils

12 mils

(For PLL Power)

IT8587

LPC

GPIO

PS/2

SM BUS

CIR

PWM

UART port

WAKE UP

EXTERNAL SERIAL FLASH

A/D D/A

SPI ENABLE

KBMX

CLOCK

Please do not place any pull-up resistor on GPG0, GPG2, and GPG6 (Reserved hardware strapping).

1A-5 2013/10/18 change U27.87 for Touch pad ID for I2C/PS2 solution switch.

ZYW use internal crystal, so if CK32K(Pin 128) N/A should be connect GND.

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

SM BUS PU(KBC)

HWPG(KBC)

DDR=1.5V, D1 DNP and D2 POP
DDR=1.35V, D1 POP and D2 DNP

3/5VPCU reset switch (FSW)

Quanta Computer Inc.			
PROJECT : ZYW			
Size	Document Number		Rev
	KBC IT8587		3A
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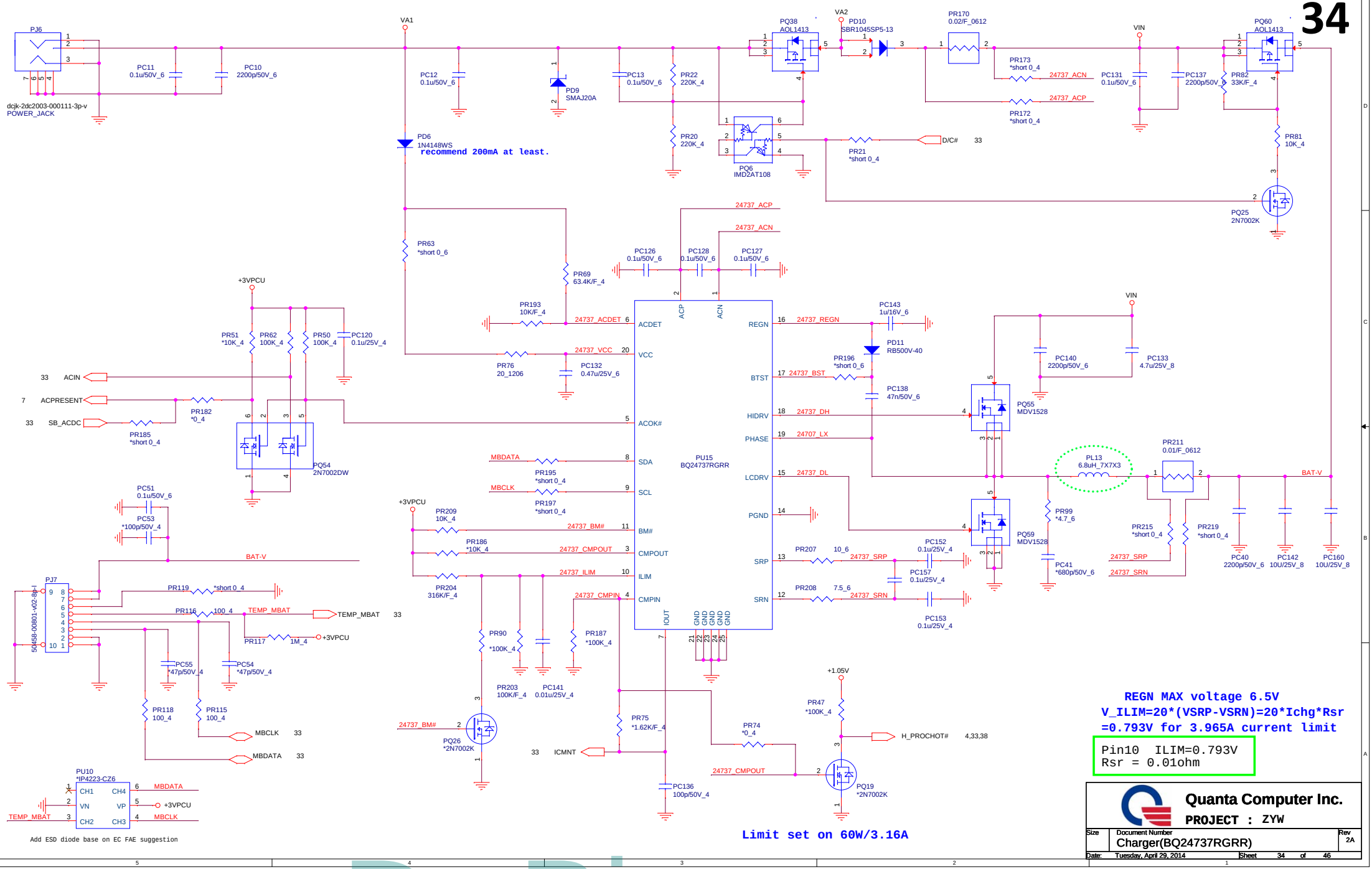
PJ6
dcjk-2dc2003-000111-3p-v
POWER_JACK
VA1
VA2
PD6
1N4148WS
recommend 200mA at least.
PD9
SMAJ20A
PD10
SBR1045SP5-13
PQ38
AOL1413
PQ60
AOL1413
PQ6
IMD2AT108
PQ25
2N7002K
PR170
0.02/F_0612
PR173
*short 0_4
PR172
*short 0_4
24737_ACN
24737_ACP
VIN
PR81
10K_4
PR82
33K/F_4
PR21
*short 0_4
D/C#
33
PR63
*short 0_6
PR69
63.4K/F_4
PC126
0.1u/50V_6
PC128
0.1u/50V_6
PC127
0.1u/50V_6
PR193
10K/F_4
24737_ACDET
24737_VCC
PR76
20_1206
PC132
0.47u/25V_6
+3VPCU
PR51
*10K_4
PR62
100K_4
PR50
100K_4
PC120
0.1u/25V_4
33 ACIN
7 ACPRESENT
33 SB_ACDC
PR182
*0_4
PR185
*short 0_4
PQ54
2N7002DW
PU15
BQ24737RGRR
ACDET
VCC
ACOK#
SDA
SCL
BM#
CMPOUT
ILIM
CMPIN
IOUT
ACP
ACN
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
GND
PC143
1u/16V_6
PD11
RB500V-40
PR196
*short 0_6
PC138
47n/50V_6
24737_REGN
24737_BST
24737_DH
24707_LX
24737_DL
PC140
2200p/50V_6
PC133
4.7u/25V_8
PQ55
MDV1528
PQ59
MDV1528
PL13
6.8uH_7X7X3
PR211
0.01/F_0612
BAT-V
PR99
*4.7_6
PC41
*680p/50V_6
PR215
*short 0_4
PR219
*short 0_4
24737_SRP
24737_SRN
PC40
2200p/50V_6
PC142
10U/25V_8
PC160
10U/25V_8
PC51
0.1u/50V_6
PC53
*100p/50V_4
PJ7
50458-00801-v02-8p-l
PR119
*short 0_4
PR116
100_4
TEMP_MBAT
PR117
1M_4
+3VPCU
PC55
*47p/50V_4
PC54
*47p/50V_4
PR118
100_4
PR115
100_4
MBCLK
33
MBDATA
33
PU10
*IP4223-CZ6
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
PR209
10K_4
PR186
*10K_4
PR204
316K/F_4
PR90
*100K_4
PR203
100K/F_4
PC141
0.01u/25V_4
PR187
*100K_4
PR75
*1.62K/F_4
PC136
100p/50V_4
24737_BM#
PQ26
*2N7002K
33 ICMNT
PR74
*0_4
24737_CMPOUT
PR47
*100K_4
+1.05V
H_PROCHOT#
4,33,38
PQ19
*2N7002K
PR207
10_6
PR208
7.5_6
PC152
0.1u/25V_4
PC157
0.1u/25V_4
PC153
0.1u/25V_4
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Pin10 ILIM=0.793V
Rsr = 0.01ohm
Limit set on 60W/3.16A
Quanta Computer Inc.
PROJECT : ZYW
Size
Document Number
Charger(BQ24737RGRR)
Rev
2A
Date: Tuesday, April 29, 2014
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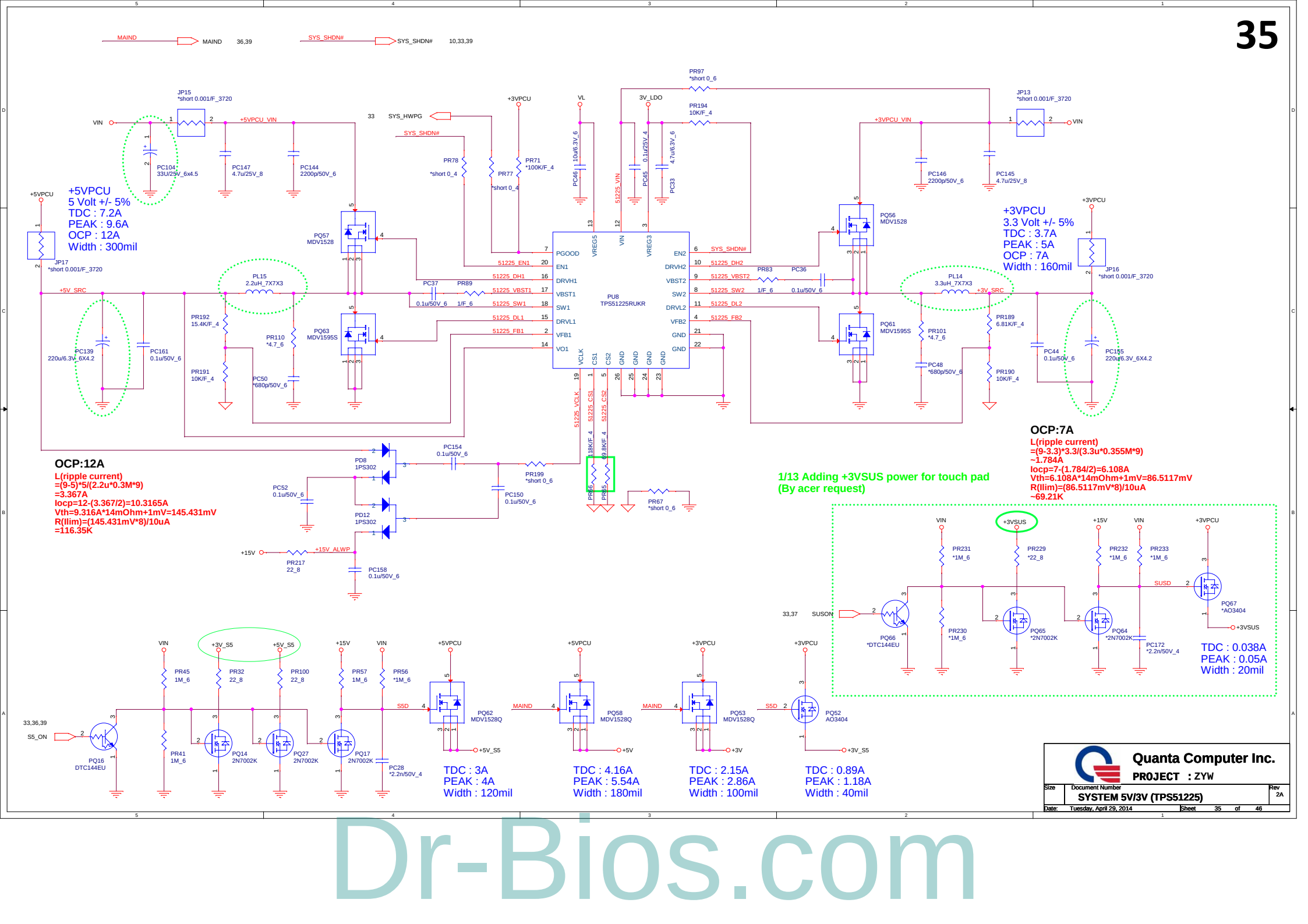
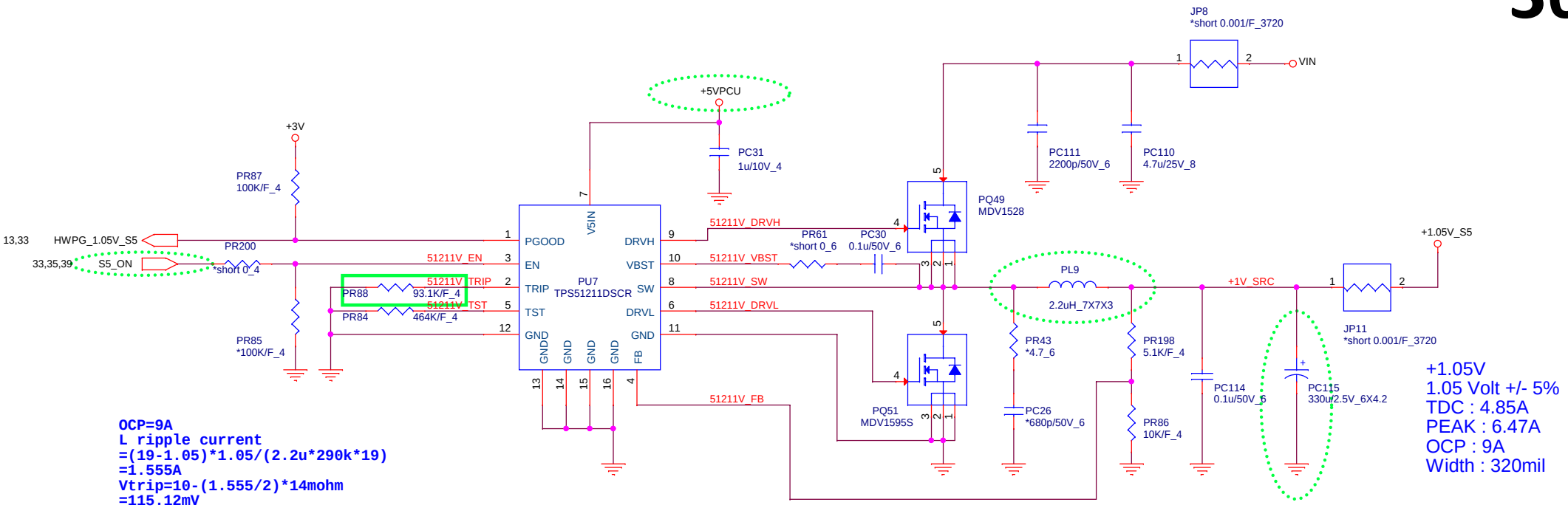


Quanta Computer Inc.
PROJECT : ZYW
Size | Document Number: SYSTEM 5V/3V (TPS51225) | Rev 2A
Date: Tuesday, April 29, 2014 | Sheet 35 of 46

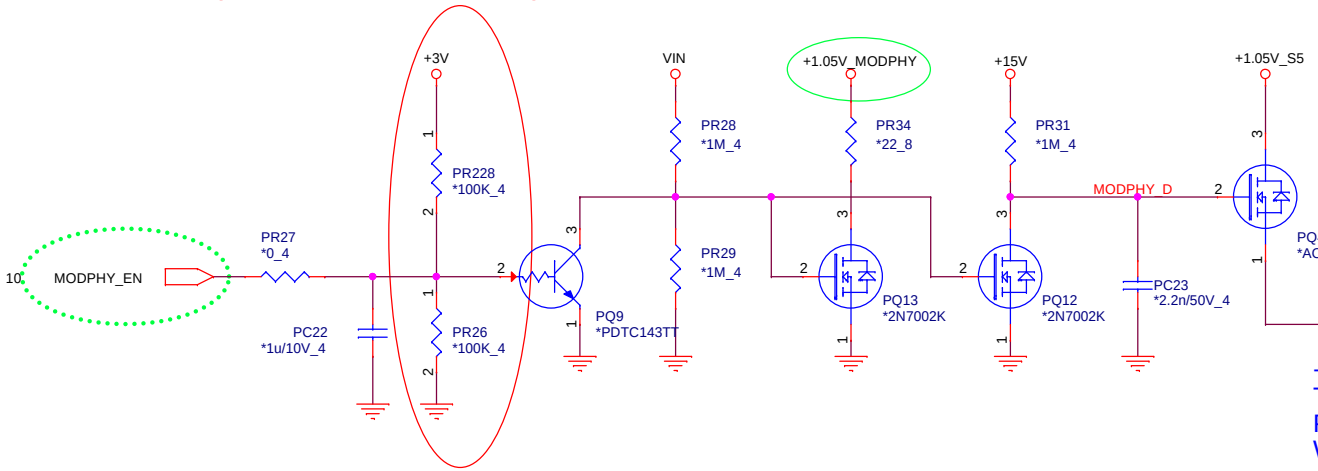


OCP=9A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=10-(1.555/2)*14mohm
=115.12mV
Rlimit=115.12mV/10uA*8=92.09Kohm

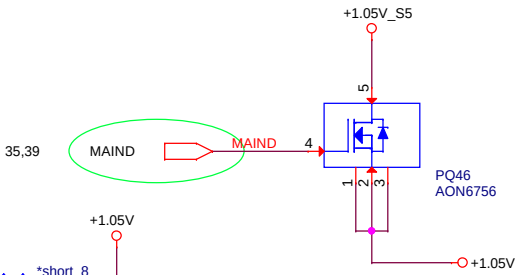
VFB=0.7V

+1.05V
1.05 Volt +/- 5%
TDC : 4.85A
PEAK : 6.47A
OCP : 9A
Width : 320mil

20131225 Modify power circuit for VCCSATA3PLL timing,
(add PR228 , no stuff PR26)



+1.05V_MODPHY
TDC : 1.43A
PEAK : 1.9A
Width : 80mil

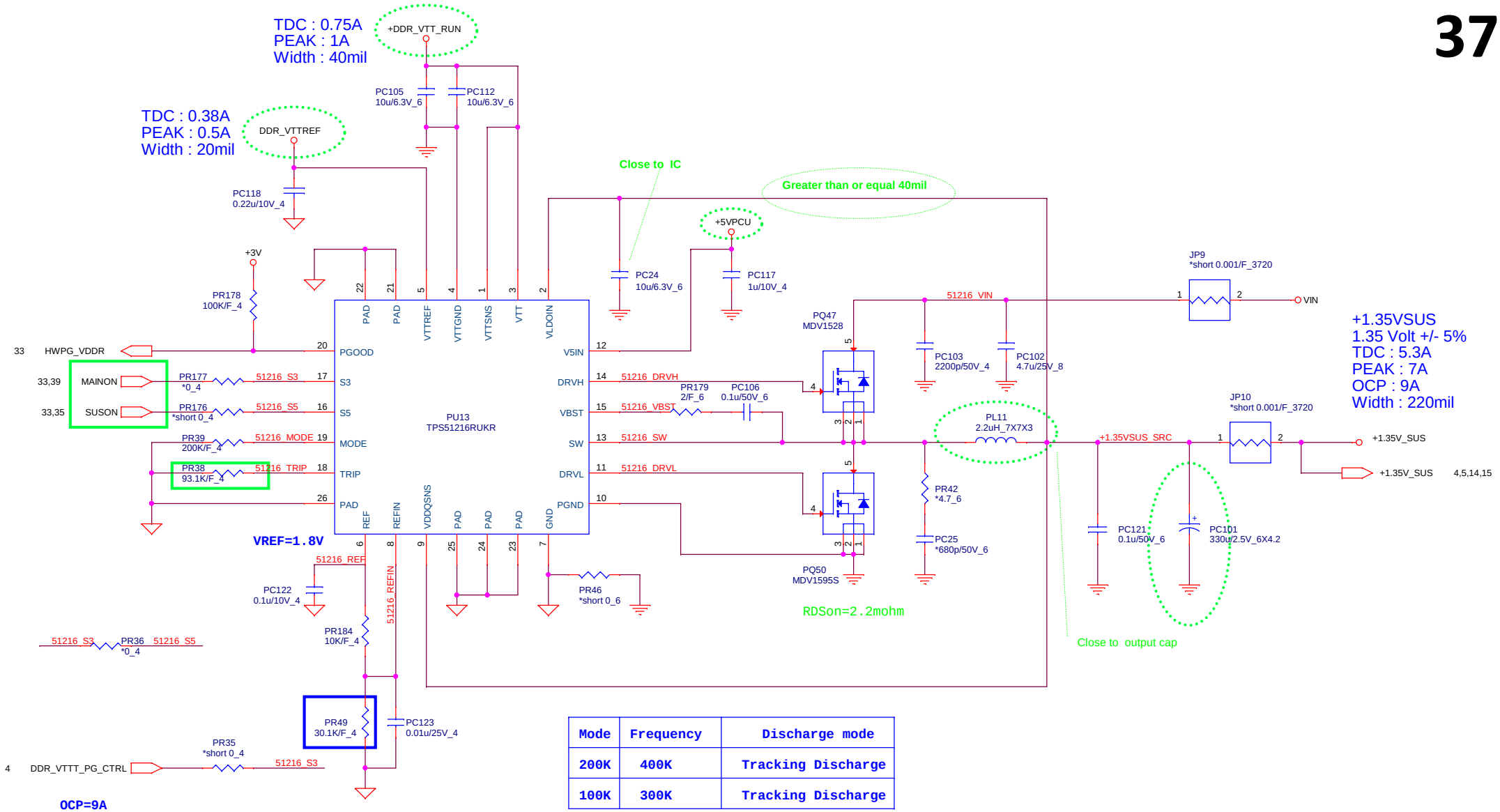


connect +1.05V power to VCCHSIO,VCCUSB3PLL and VCCSATAPLL directly

TDC : 4.85A
PEAK : 6.47A
Width : 200mil

Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	+1.05V_S5 (TPS51211)	2A
Date: Tuesday, April 29, 2014	Sheet 36 of 46	



Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=9A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=9-(1.425/2)*14mohm
=116.024mV
Rlimit=116.024mV/10uA*8=92.82Kohm

DDR=1.35V
OCP=9A
PR84=10K/F_4
PR86=30.1K/F_4

Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	2A

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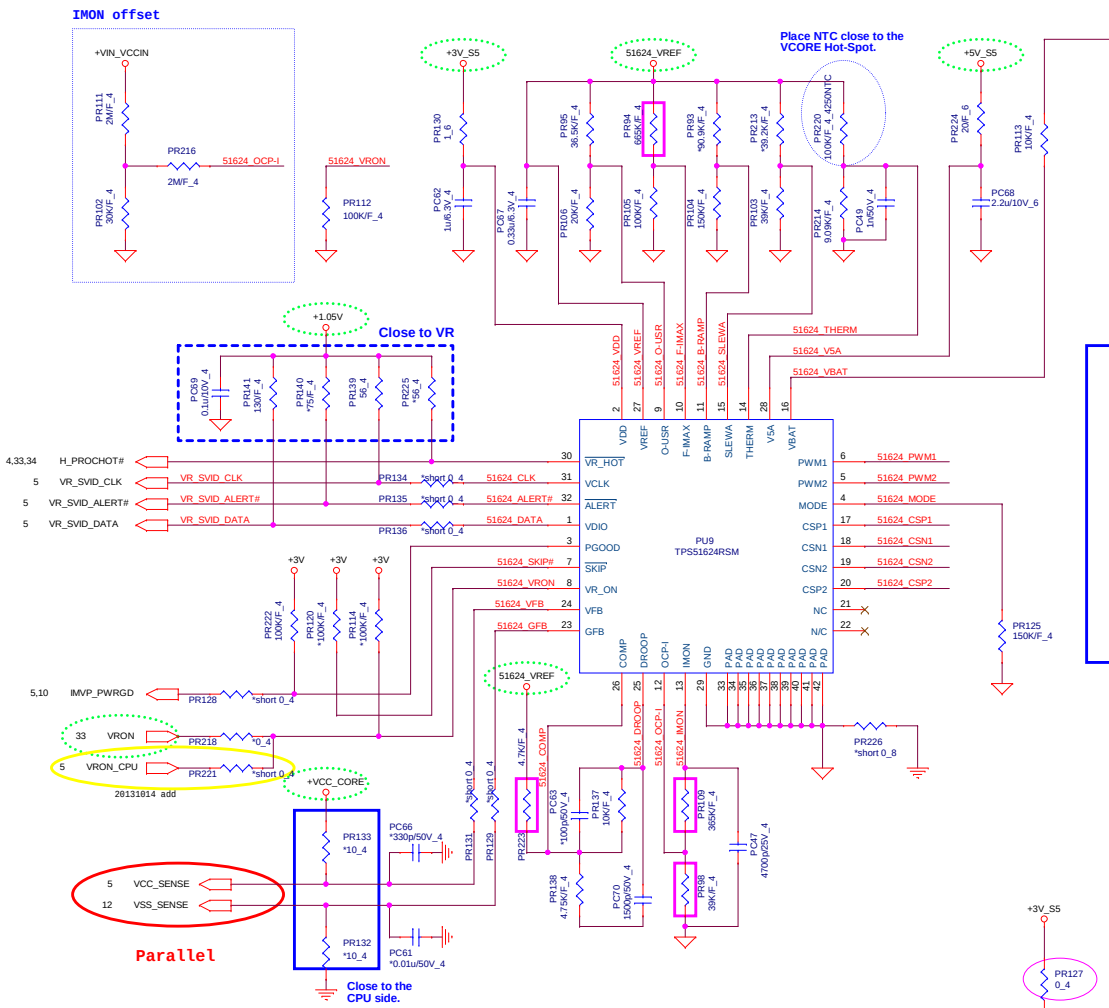
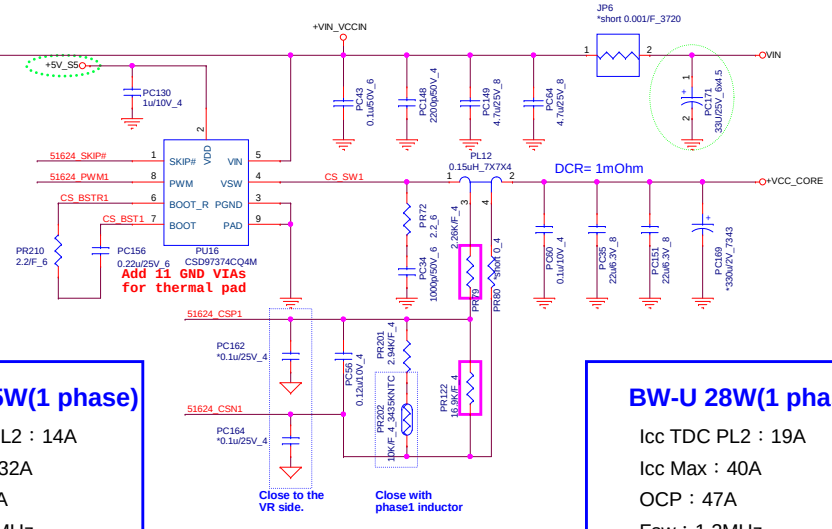




BW-U 15W(1 phase)

Icc TDC PL2：14A

Icc Max：32A

OCP：37A

Fsw：1.2MHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

Rmode		PS3	OSR
	100K Ohm	ON	ON
	150K Ohm	ON	OFF

BW-U 28W(1 phase)

Icc TDC PL2：19A

Icc Max：40A

OCP：47A

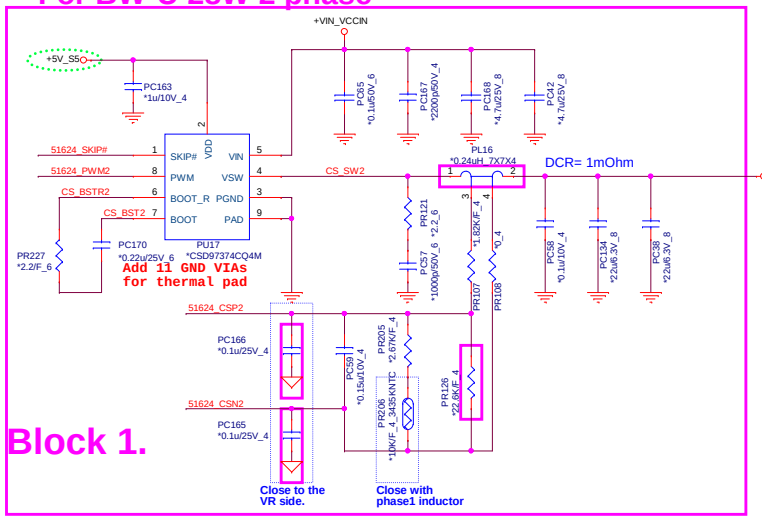
Fsw：1.2MHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

For BW-U 28W 2 phase



BW-U 28W 1 phase

Location	Value
PR79	CS22212FB11
PR122	CS32262FB15
PR94	CS45232FB00
PR223	CS24752FB12
PR98	CS35622FB10
PR109	CS44122FB00

BW-U 28W 2 phase

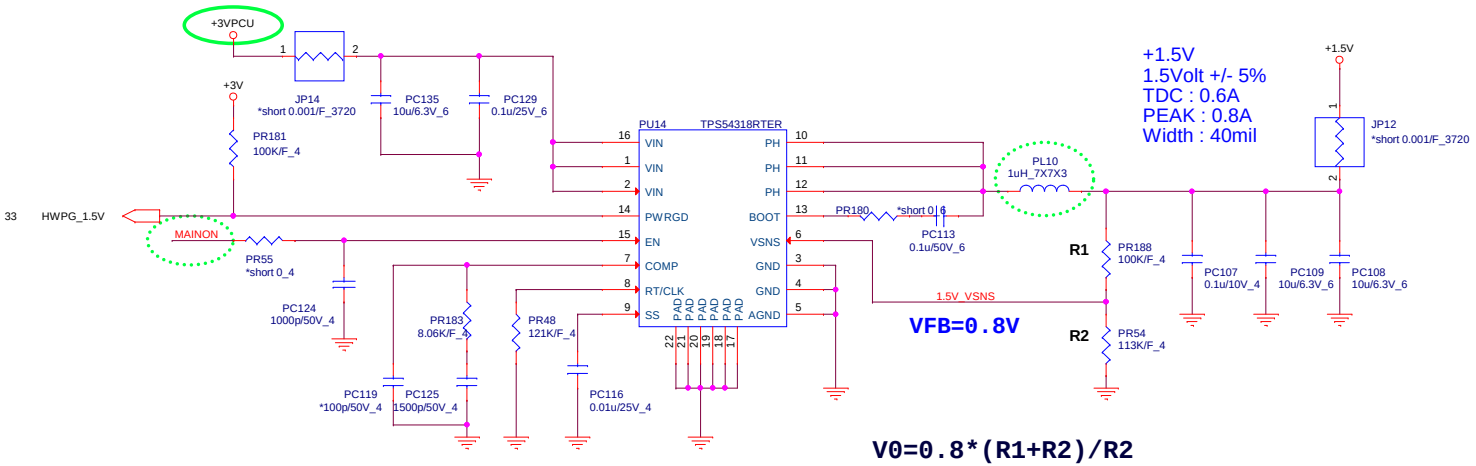
Location	Value	Location	Value
PL12、PL16	0.24uH_7X7X4	PR105	56.2K/F_4
PR79	1.82K/F_4	PR223	2.37K/F_4
PR122、PR126	*22.6K/F_4	PR138	10K/F_4
PR201	2.67K/F_4	PR109	150K/F_4
PC144	0.15u/10V_4	PR123、PR127	*0_4
PR94	294K/F_4	PC162、PC164 PC165、PC166	*0.1u/25V_4
Block 1.	Stuff		

Quanta Computer Inc.

PROJECT ：ZYW

Size	Document Number	Rev
	+VCCIN(TPS51624)	2A

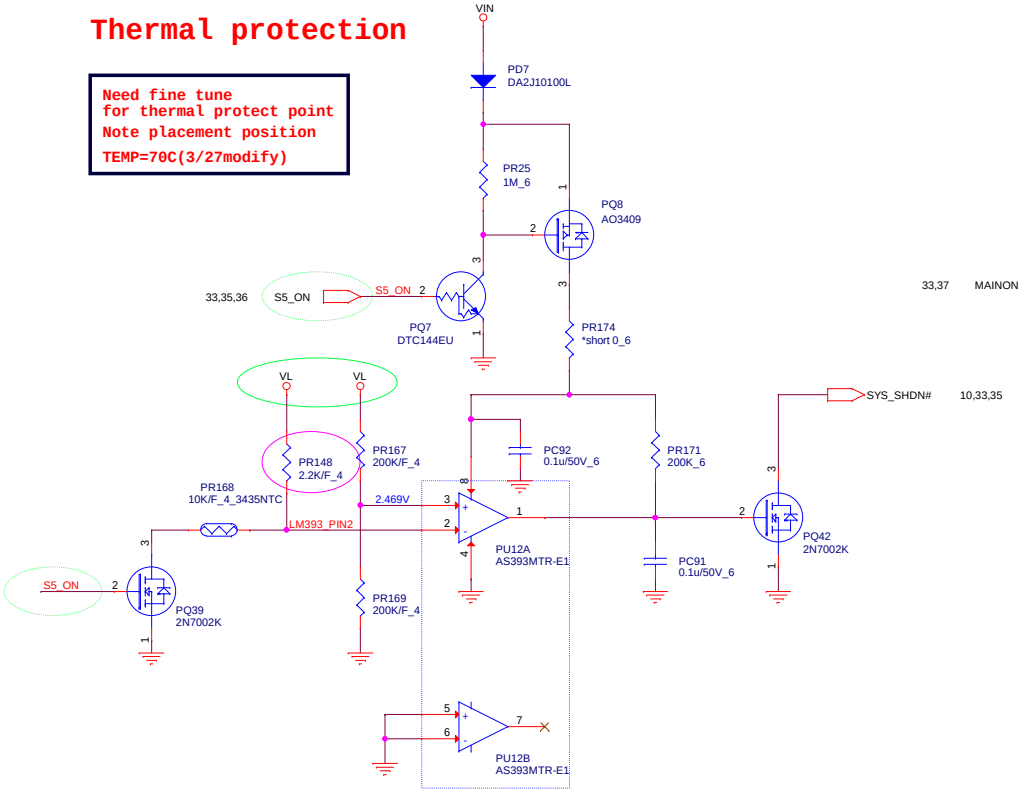
Date: Tuesday, April 29, 2014 Sheet 38 of 46

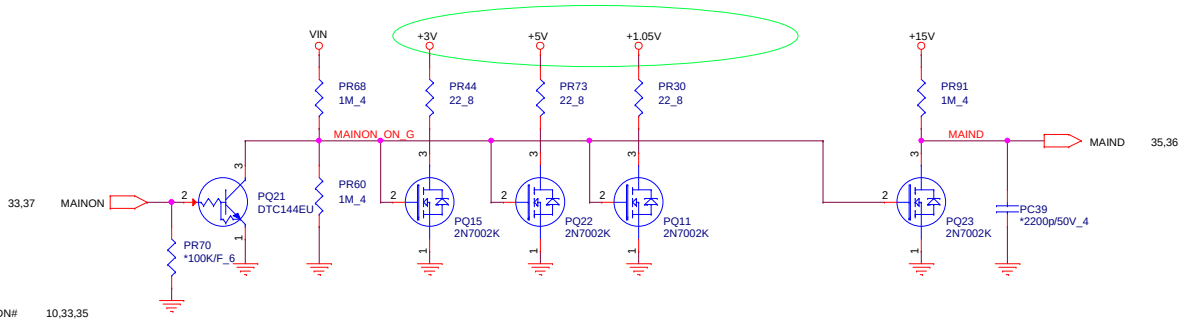


V0=0.8*(R1+R2)/R2

Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=70C(3/27modify)

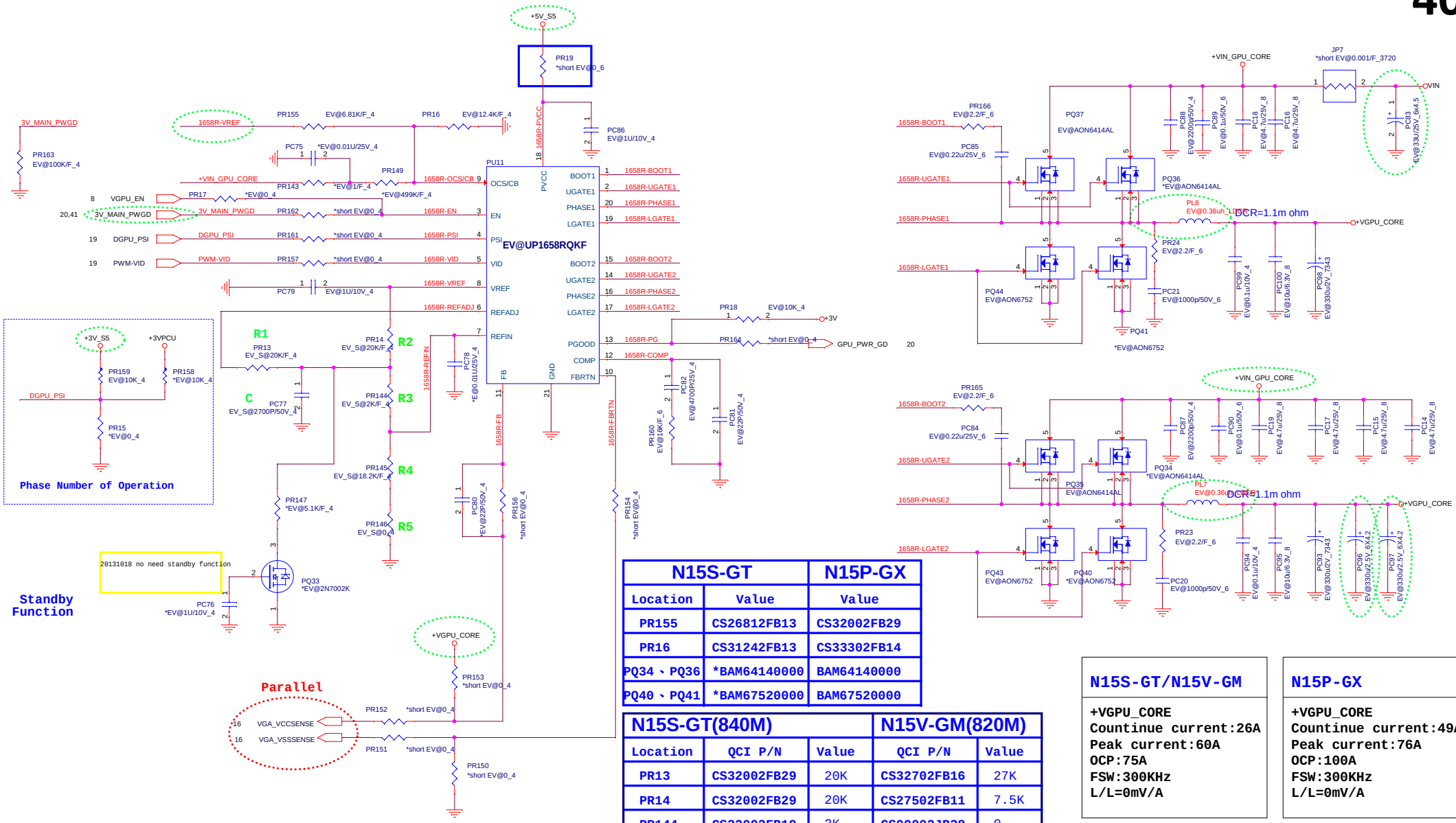




For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	+1.5V/Thermal Protect	2A
Date: Tuesday, April 29, 2014	Sheet 39 of 46	



N15S-GT	N15P-GX
Location	Value	Value
PR155	CS26812FB13	CS32002FB29
PR16	CS31242FB13	CS33302FB14
PQ34、PQ36	*BAM64140000	BAM64140000
PQ40、PQ41	*BAM67520000	BAM67520000

N15S-GT(840M)			N15V-GM(820M)	
Location	QCI P/N	Value	QCI P/N	Value
PR13	CS32002FB29	20K	CS32702FB16	27K
PR14	CS32002FB29	20K	CS27502FB11	7.5K
PR144	CS22002FB19	2K	CS00002JB38	0
PR145	CS31822FB16	18K	CS26202FB17	6.2K
PR146	CS00002JB38	0	CS21742FB00	1.74K
PC77	CH22706KB14	2.7N	CH25604KB18	5.6N

N15S-GT/N15V-GM

+VGPU_CORE
Countinue current:26A
Peak current:60A
OCP:75A
FSW:300KHz
L/L=0mV/A

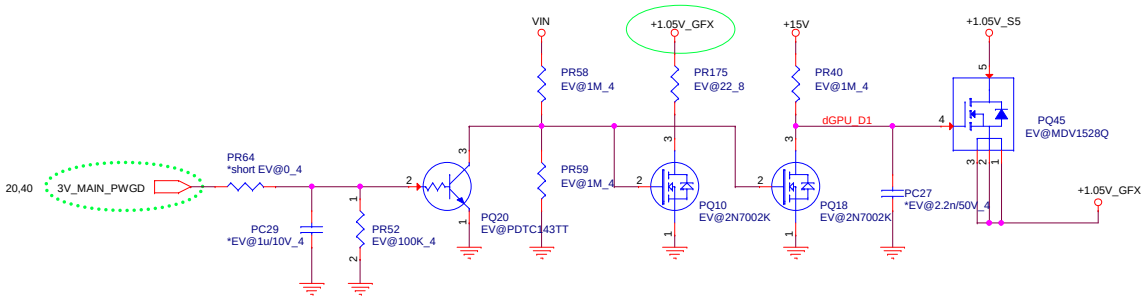
N15P-GX

+VGPU_CORE
Countinue current:49A
Peak current:76A
OCP:100A
FSW:300KHz
L/L=0mV/A

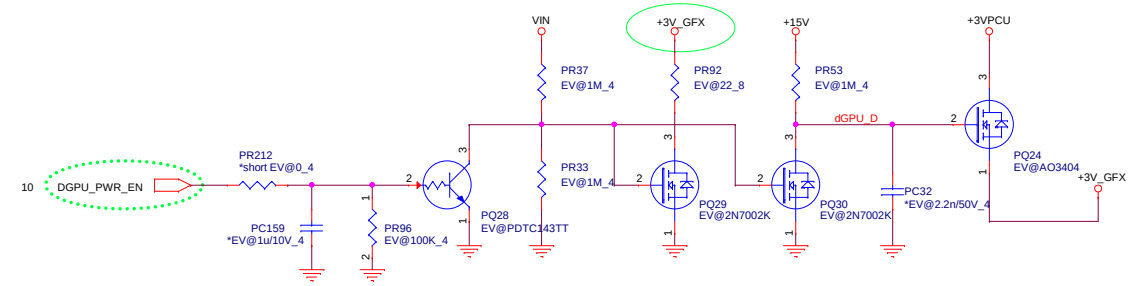
Quanta Computer Inc.
PROJECT : ZYW

Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	2A
Date: Tuesday, April 29, 2014	Sheet 40 of 46	

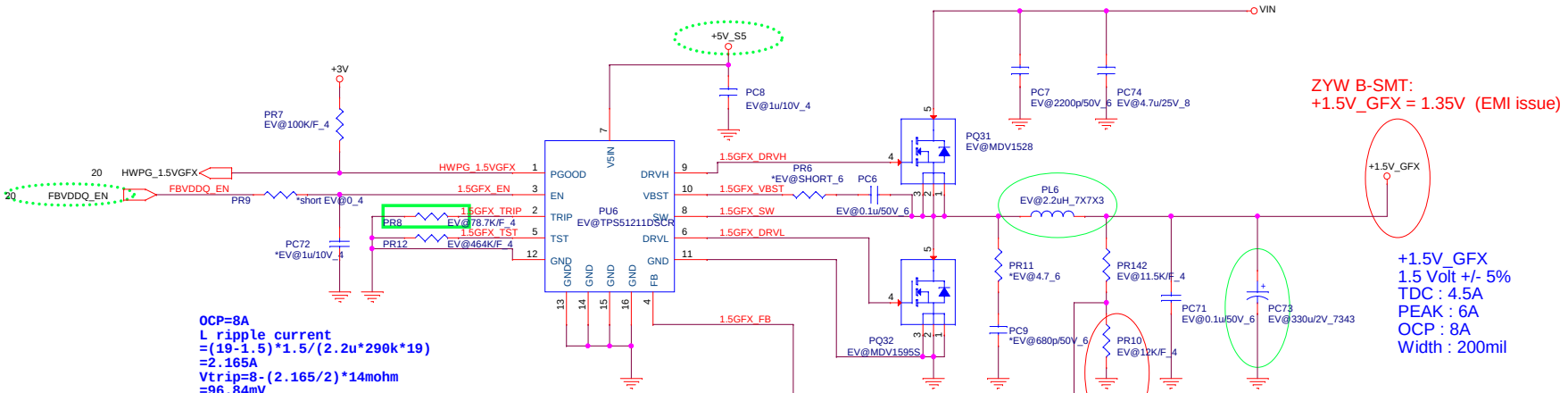
16,17,18 +1.05V_GFX
16,17,21 +1.5V_GFX
16,19,20,33 +3V_GFX



+1.05V_GFX
TDC : 2.7A
PEAK : 3.6A
Width : 120mil



+3V_GFX
TDC : 0.23A
PEAK : 0.3A
Width : 40mil



ZYW B-SMT:
+1.5V_GFX = 1.35V (EMI issue)

+1.5V_GFX
1.5 Volt +/- 5%
TDC : 4.5A
PEAK : 6A
OCP : 8A
Width : 200mil

OCP=8A
L ripple current
=(19-1.5)*1.5/(2.2u*290k*19)
=2.165A
Vtrip=8-(2.165/2)*14mohm
=96.84mV
Rlimit=96.84mV/10uA*8=77.47Kohm

ZYW B-SMT:
change PR10 from 10k to 12k

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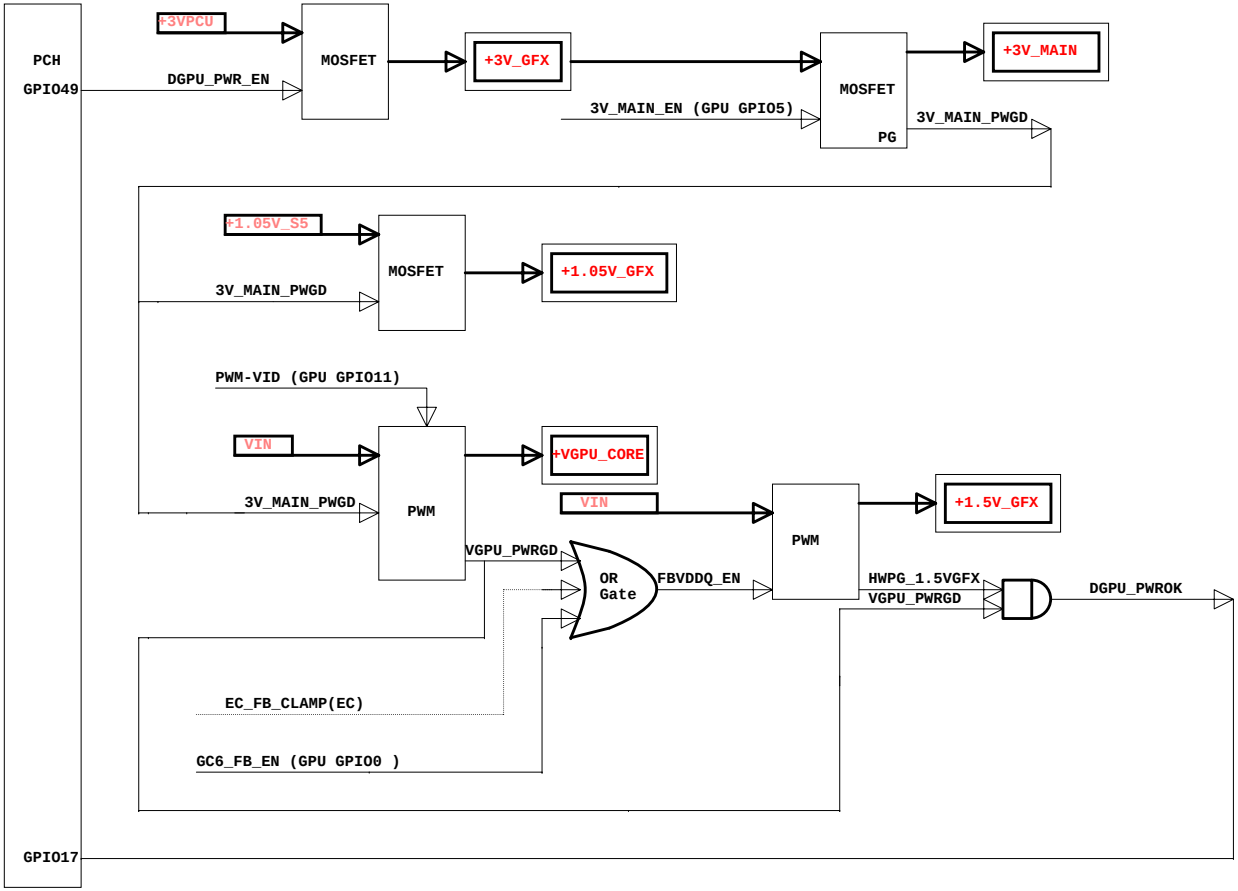
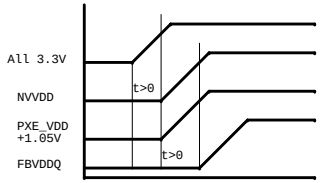
VGA power up sequence

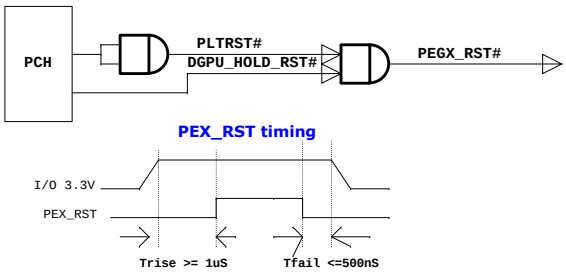




N15x Power on sequance

Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V inculdes all rails that are shared

VGA Reset



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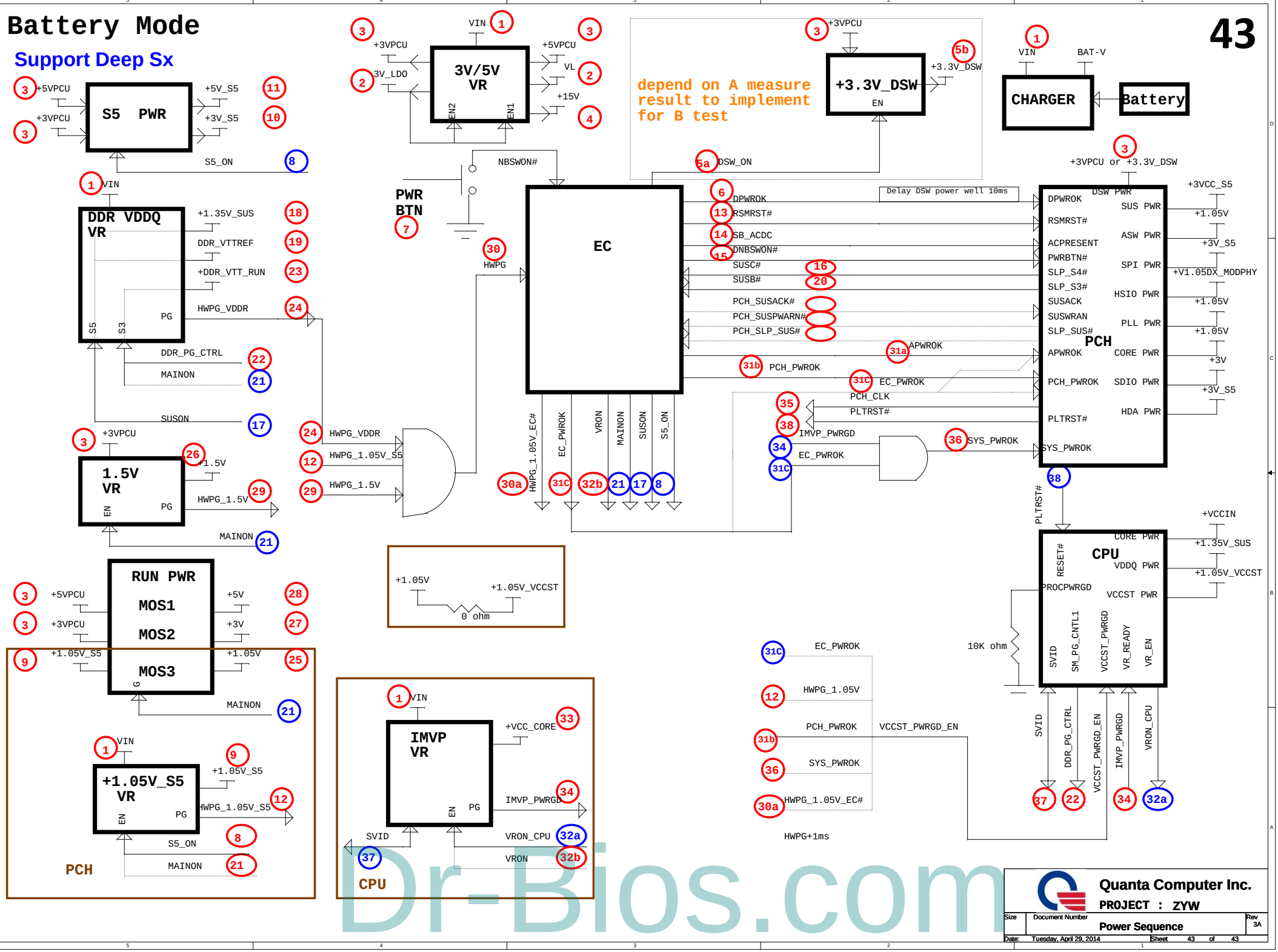
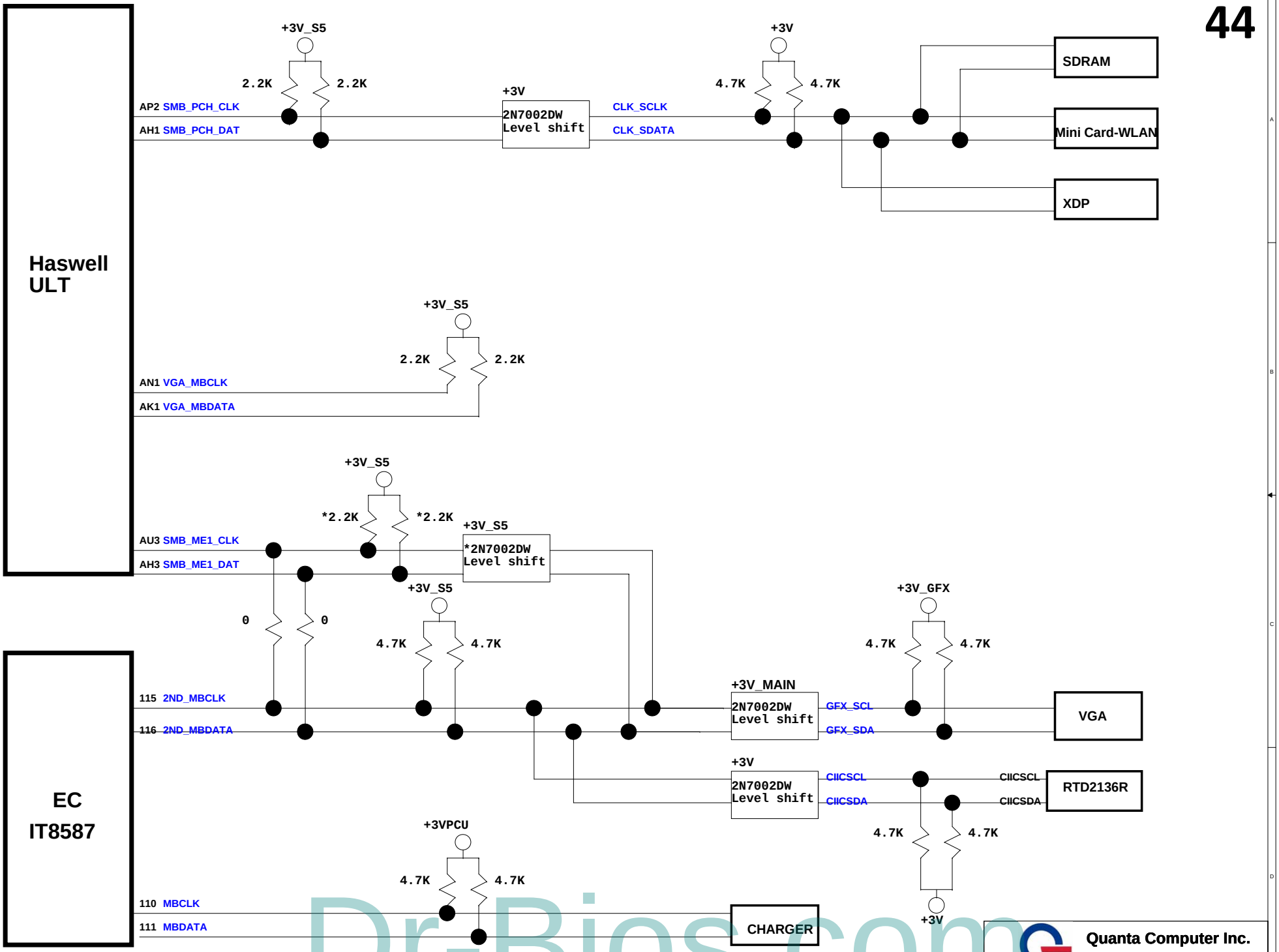
Battery Mode

Support Deep Sx





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	Block Diagram	
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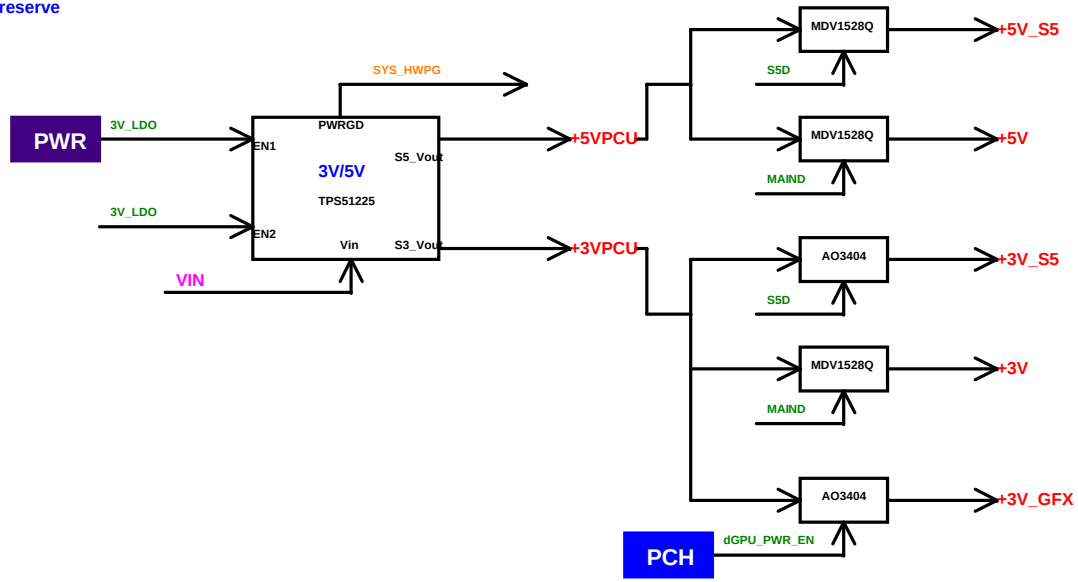
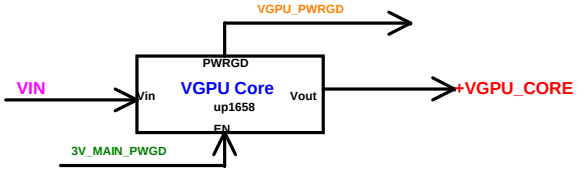
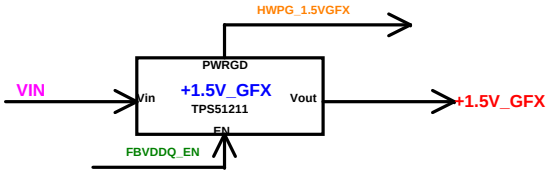
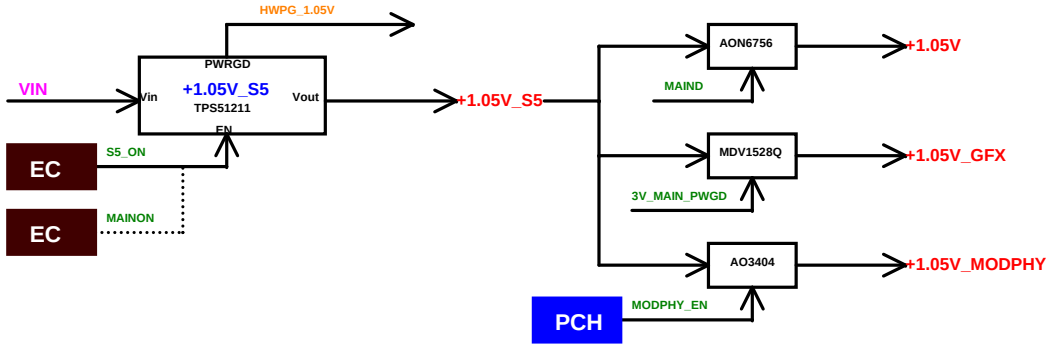
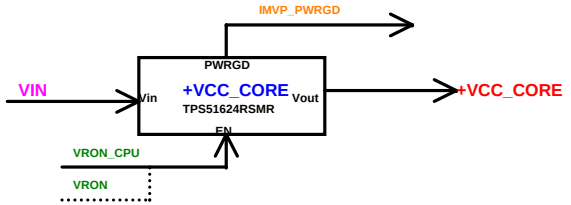
實線表defult
虛線表reserve

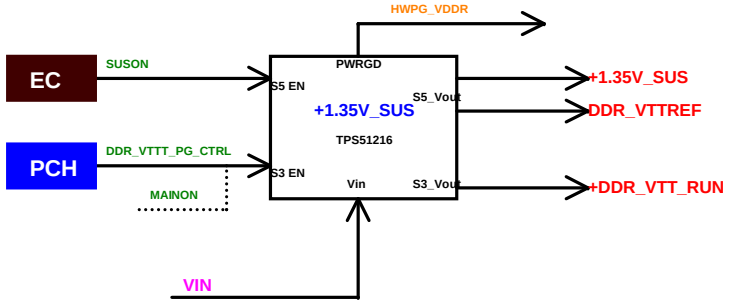


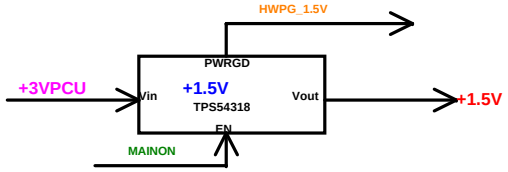












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