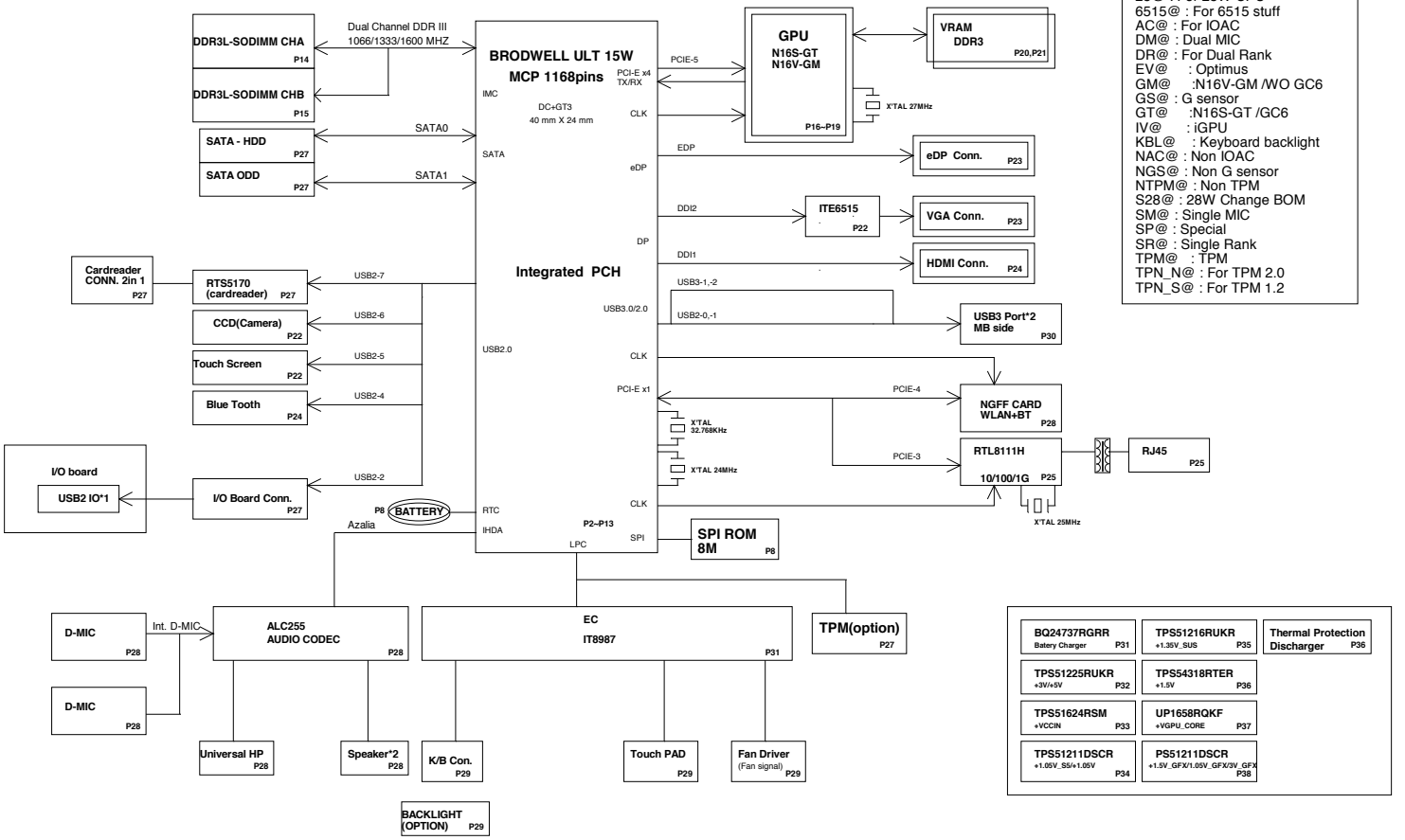
ZRT/ZRTA_GDDR3 BWD ULT SYSTEM BLOCK DIAGRAM

BOM

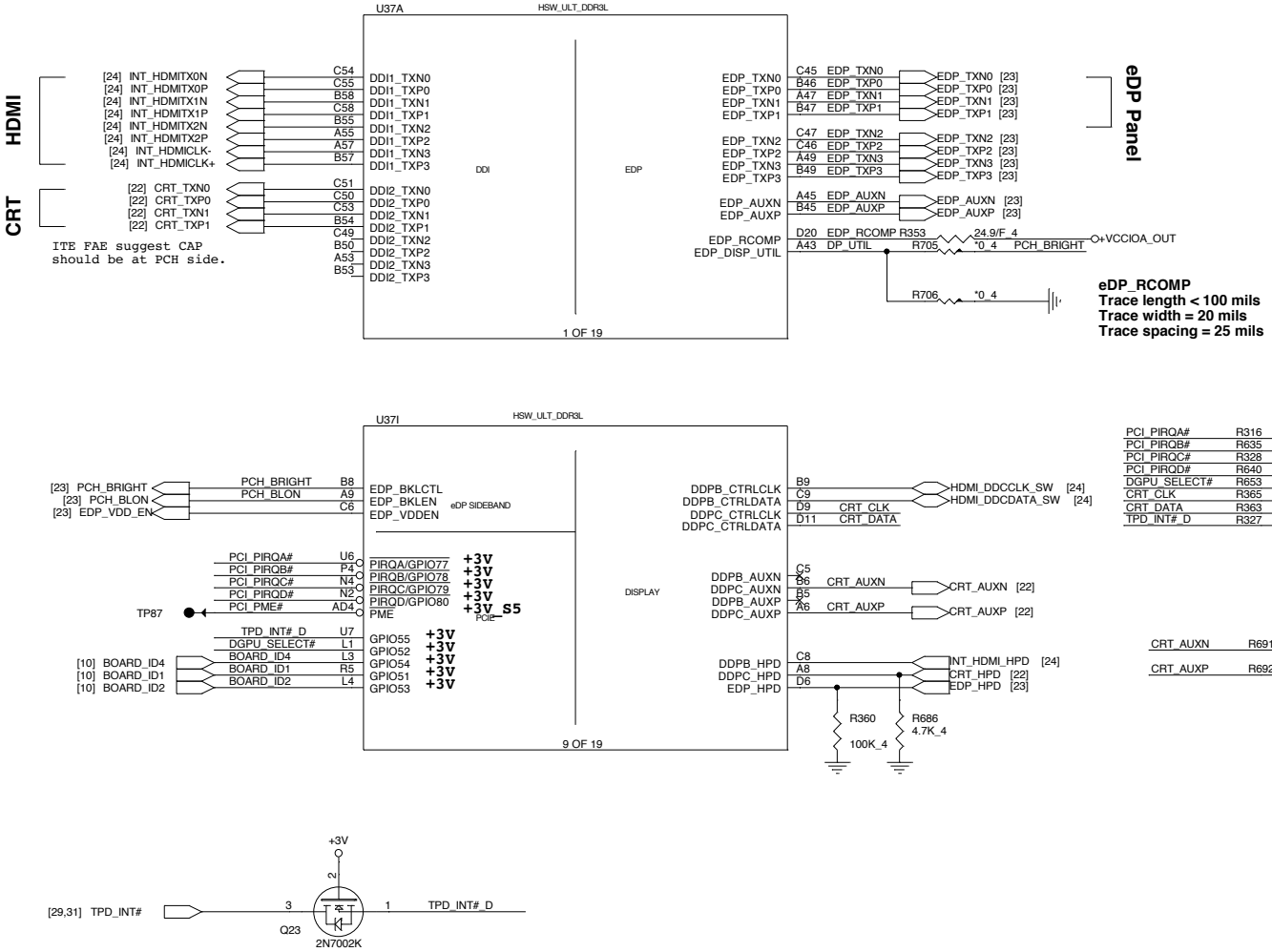
15@ : For 15W CPU
28@ : For 28W CPU
6515@ : For 6515 stuff
AC@ : For IOAC
DM@ : Dual MIC
DR@ : For Dual Rank
EV@ : Optimus
GM@ :N16V-GM /WO GC6
GS@ : G sensor
GT@ :N16S-GT /GC6
IV@ : iGPU
KBL@ : Keyboard backlight
NAC@ : Non IOAC
NGS@ : Non G sensor
NTPM@ : Non TPM
S28@ : 28W Change BOM
SM@ : Single MIC
SP@ : Special
SR@ : Single Rank
TPM@ : TPM
TPN_N@ : For TPM 2.0
TPN_S@ : For TPM 1.2



BQ24737RGRR Batery Charger P31	TPS51216RUKR +1.35V_SUS P35	Thermal Protection Discharger P36
TPS51225RUKR +3V/+5V P32	TPS54318RTER +1.5V P36	
TPS51624RSM +VCCIN P33	UP1658RQKF +VGPU_CORE P37	
TPS51211DSCR +1.05V_S5/+1.05V P34	PS51211DSCR +1.5V_GFX/1.05V_GFX/3V_GFX P38	

Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Block Diagram
Rev 3A
Date: Wednesday, February 11, 2015 Sheet 1 of 44

Haswell ULT (DISPLAY,eDP)



Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: Haswell 3/5 (DDI/eDP)	Rev: 3A
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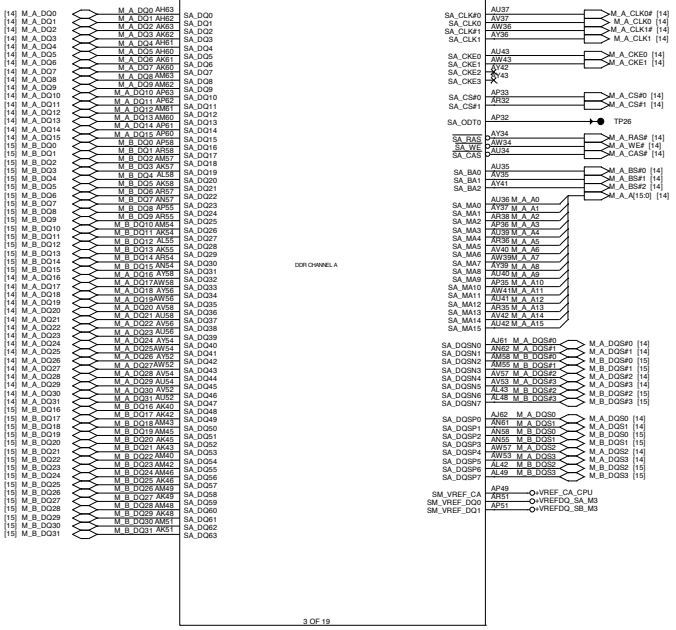
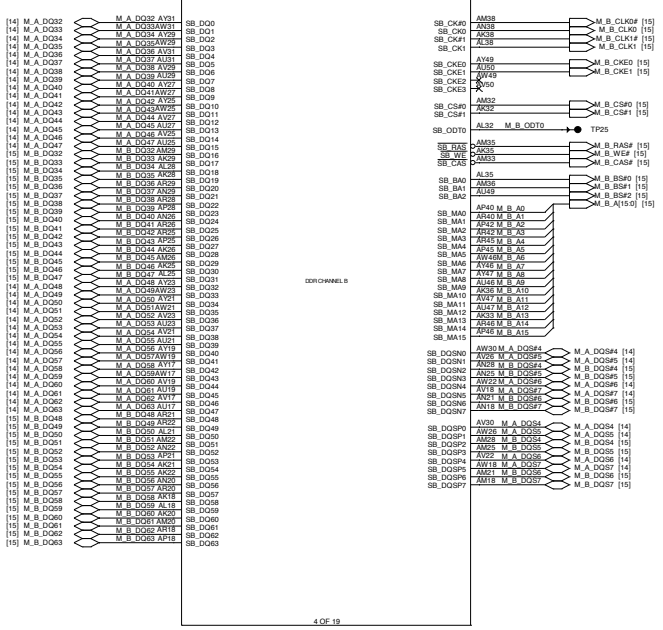
Change Data and DQS to interleave.

Haswell ULT (DDR3L)



Haswell Processor (DDR3)



Quanta Computer Inc.			
PROJECT : ZRT/ZRTA			
Size	Document Number		Rev
	Haswell 2/5 (DDR3 I/F)		3A
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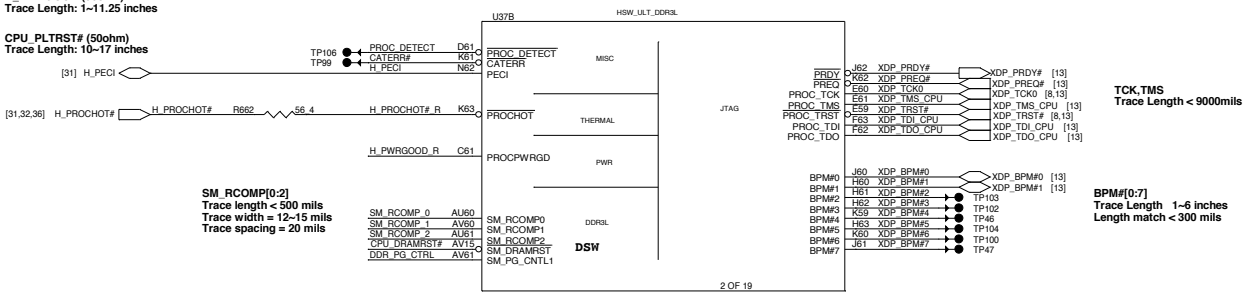
Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

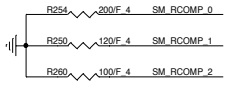


TCK,TMS
Trace Length < 9000mils

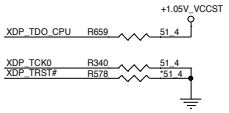
SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

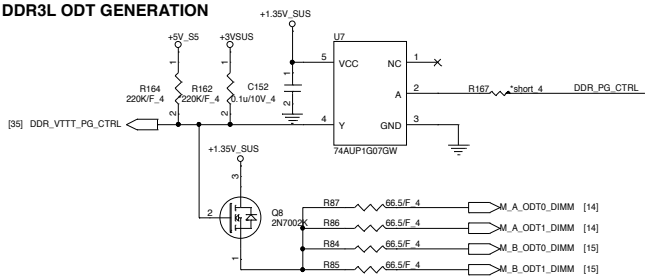
DRAM COMP



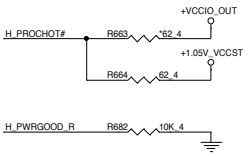
XDP PU/PD



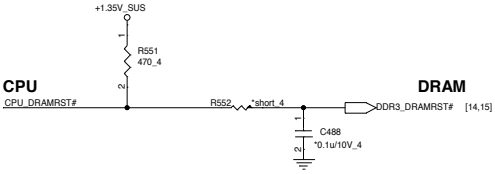
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
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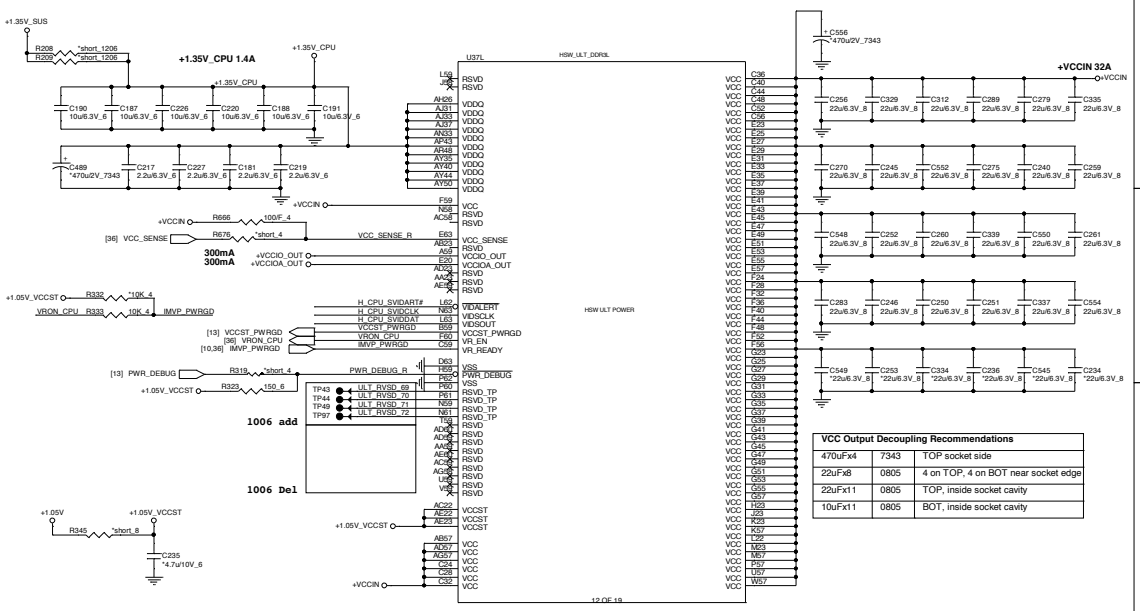
VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

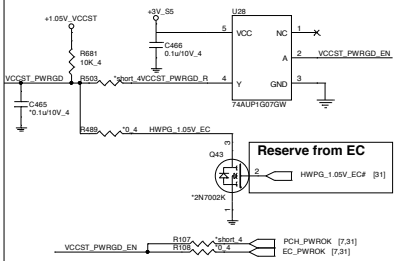
Haswell ULT (POWER)

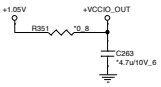


VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

VCCST PWRGD

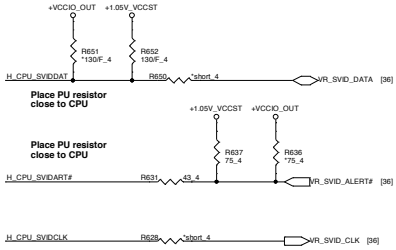
CRB is via +1.05V PG



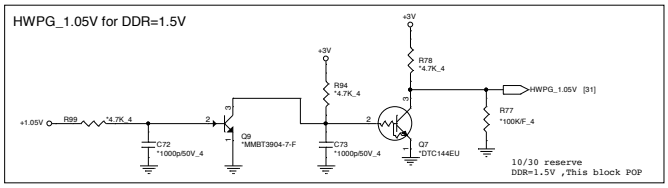


SVID

Layout note: need routing together and ALERT need between CLK and DATA.



HWPG_1.05V for DDR=1.5V



Quanta Computer Inc.			
PROJECT : ZRT/ZRTA			
Size	Document Number		Rev
	Haswell 4/5 (POWER)		3A
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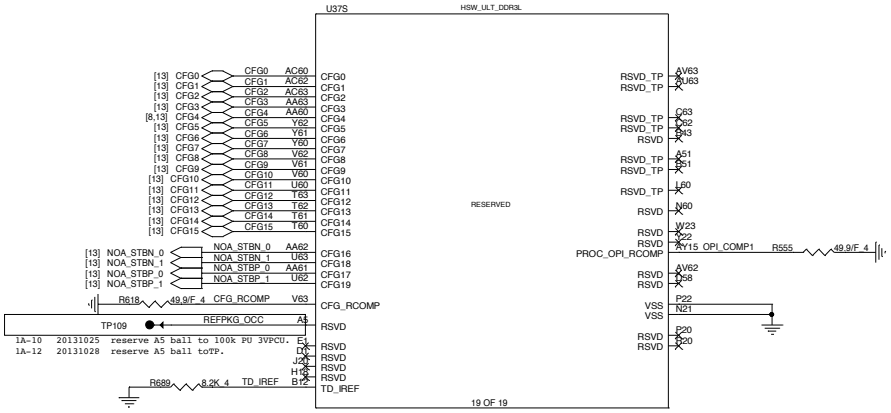
Haswell ULT (CFG,RSVD)



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R289 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R606 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R610 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R614 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R619 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R295 *1K_4

Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	3A

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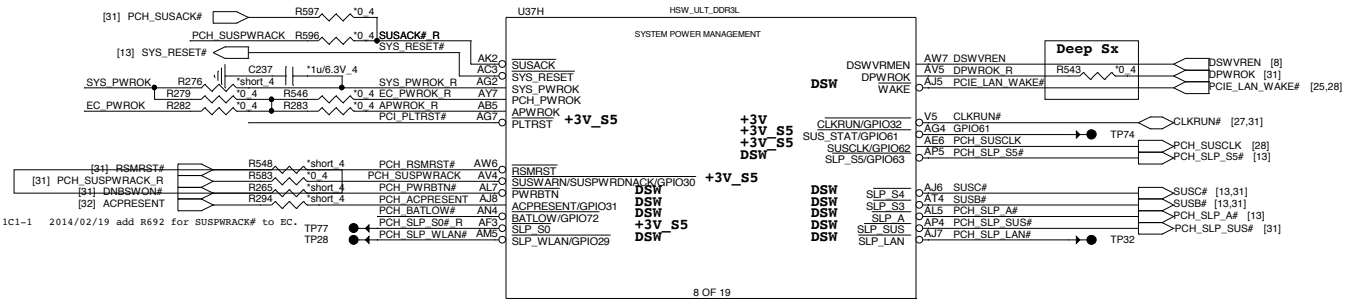
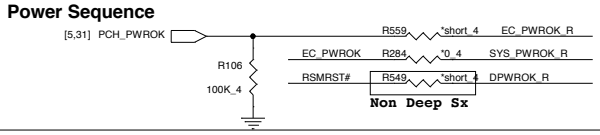
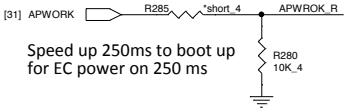
Haswell ULT PCH (PM)

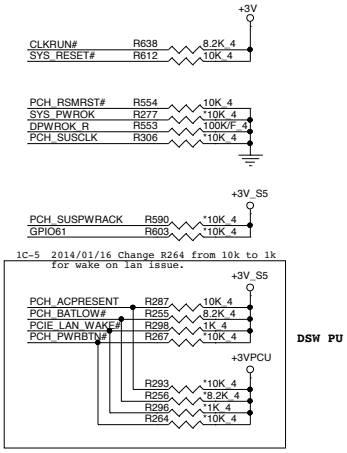


Power Sequence

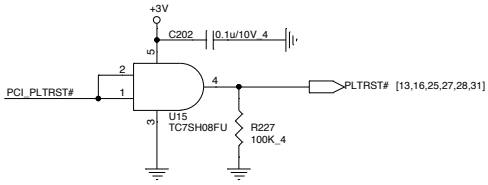




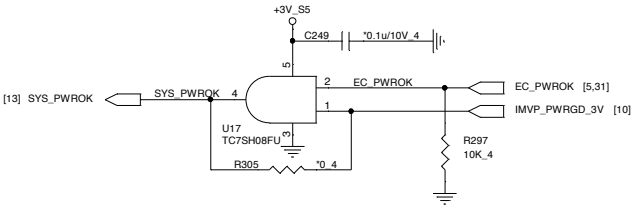
PCH PM PU/PD



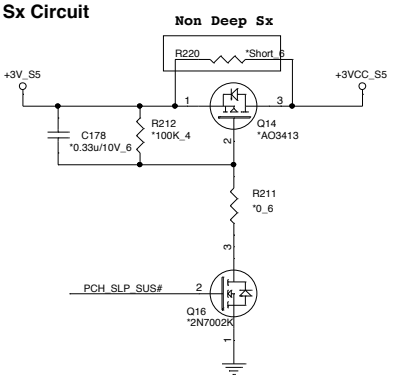
PLTRST# Buffer



SYSPWOK



Deep Sx Circuit



Quanta Computer Inc.		
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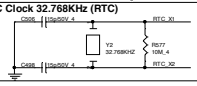
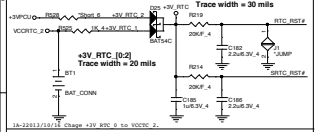
Haswell ULT PCH (RTC/HDA/SATA/SPI)

Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)

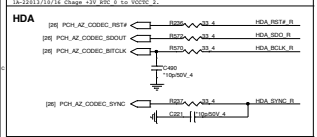
RTC Clock 32.768KHz (RTC)



RTC Circuitry (RTC)



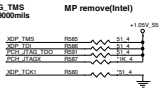
HDA

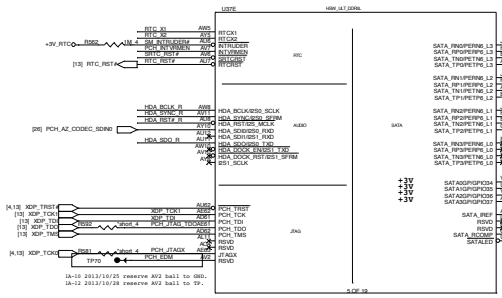


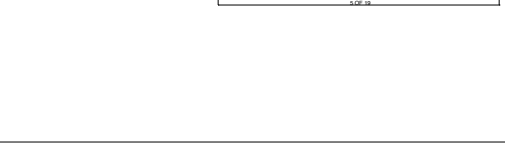
PCH JTAG

JTAG_TCK,JTAG_TMS Trace Length < 9000mils

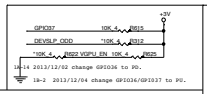
MP remove(Intel)

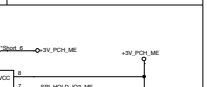






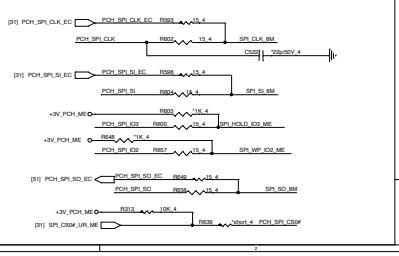
SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils



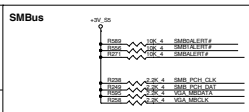


PCH SPI ROM(8M+4M)

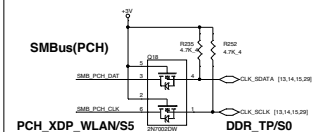
15ohm CS01502JB12



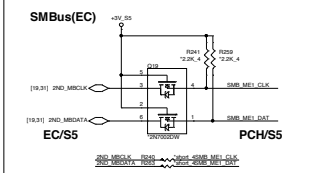
SMBus



SMBus(PCH)

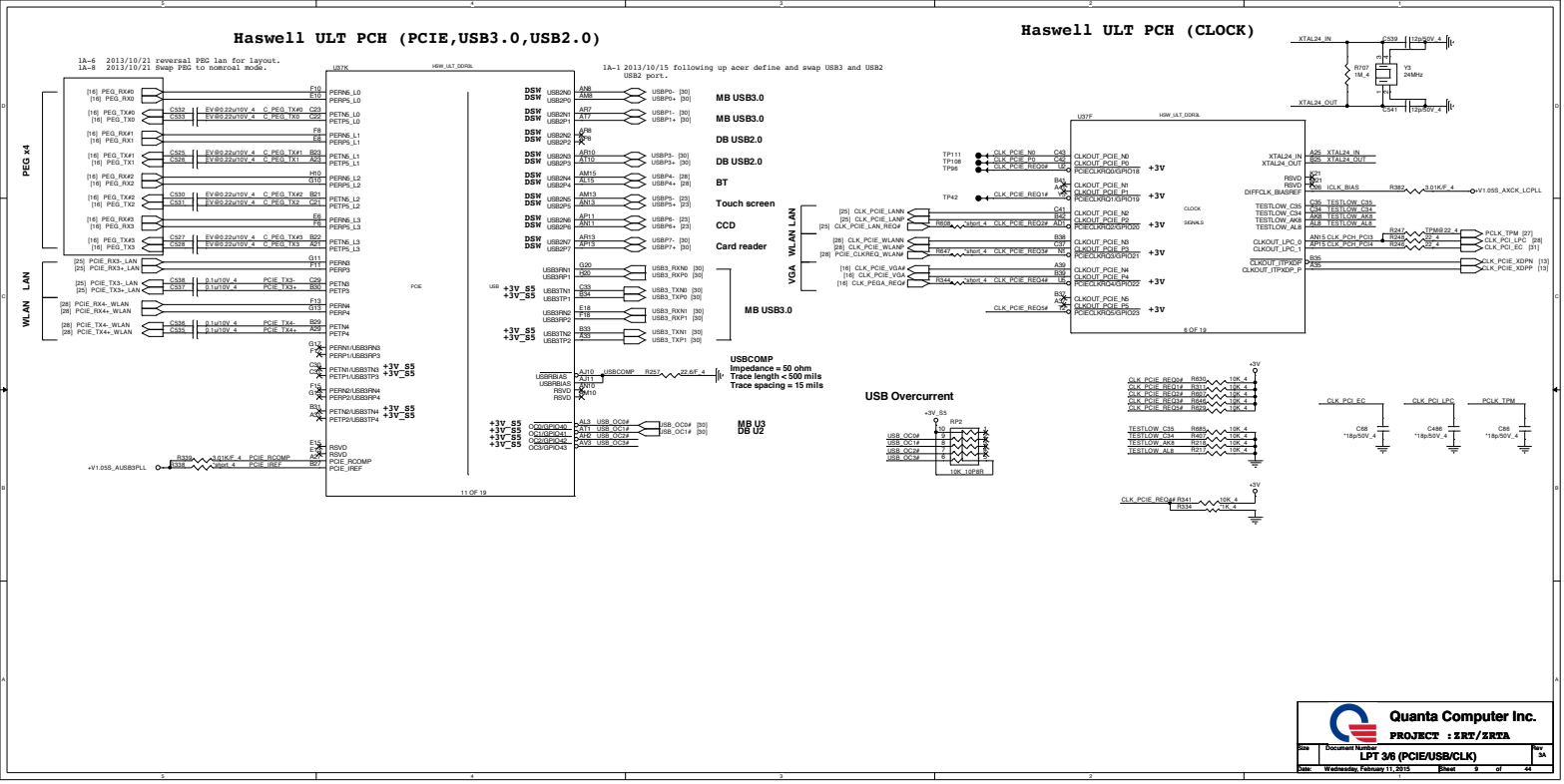


SMBus(EC)



ULT Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	**0 = Default enable (iPD 20K)** 1 =Disable No-Reboot mode	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	**0 = Default can program ME (iPD 20K)** 1 =can't program ME	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**1=Should be always pull-up**	
GPIO66	Top-Block Swap override		**0 = Default disable (iPD 20K)** 1 = Enable TBS function	
GPIO86	Boot BIOS Strap Bit		**0 = Default SPI (iPD 20K)** 1 =LPC	
GPIO15	TLS(Transport layer security)		**0 = Default enable w/o confidentiality(iPD 20K)** 1 =Default enable with confidentiality	
CFG4	DP presence strap		**0 = Enable an external display port is connected to the eDP** 1 =disable	
DSWVREN	Deep Sx well on die VR enable		**1=Should be always pull-up**	


Haswell ULT PCH (PCIE,USB3.0,USB2.0)
Haswell ULT PCH (CLOCK)
1A-6 2013/10/21 reversal PEG lan for layout.
1A-8 2013/10/21 Swap PEG to nomreal mode.
1A-1 2013/10/15 following up acer define and swap USB3 and USB2 USB2 port.
PEG x4
WLAN LAN
MB USB3.0
MB USB3.0
DB USB2.0
DB USB2.0
BT
Touch screen
CCD
Card reader
MB USB3.0
USBCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils
USB Overcurrent
MB U3
DB U2
11 OF 19
6 OF 19
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
LPT 3/6 (PCIE/USB/CLK)
Wednesday, February 11, 2015
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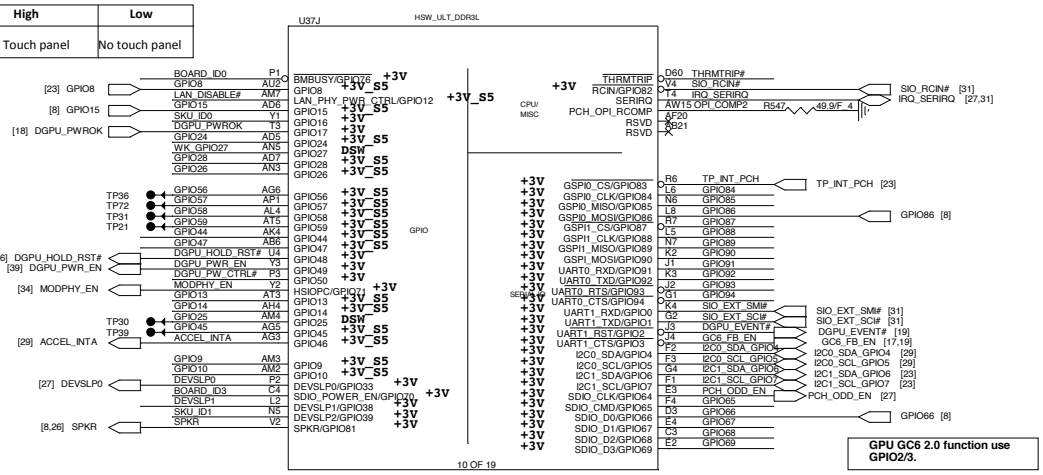
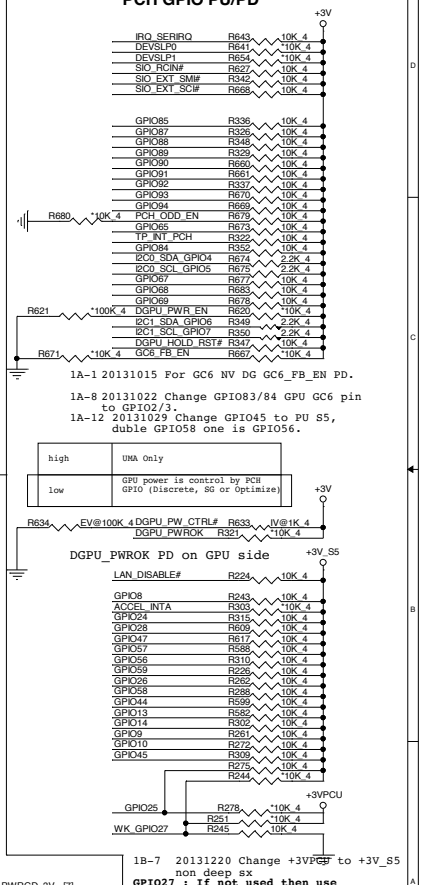
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

	High	Low
GPIO8	Touch panel	No touch panel



PCH GPIO PU/PD



1A-1 20131015 For GC6 NV DG GC6_FB_EN PD.

1A-8 20131022 Change GPIO83/84 GPU GC6 pin to GPIO2/3.

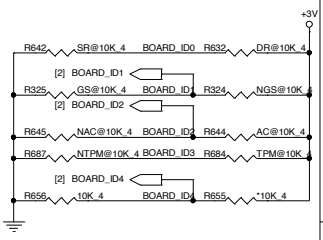
1A-12 20131029 Change GPIO45 to PU S5, duble GPIO58 one is GPIO56.

high	UMA Only
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

1B-7 20131220 Change +3VPCU to +3V_S5 non deep sx

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

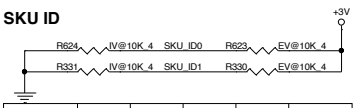
Board ID



	Low	High
BOARD_ID0	single rank SKU	Dual rank SKU
BOARD_ID1	Reserved (Default)	Reserve
BOARD_ID2	No IOAC	IOAC
BOARD_ID3	No TPM	TPM
BOARD_ID4	Non-Dolly (Default)	Dolly

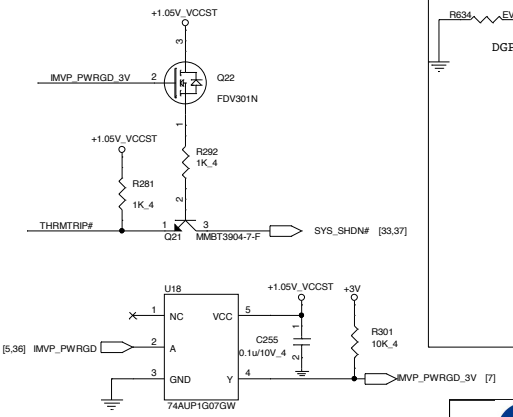
RAM ID

SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip



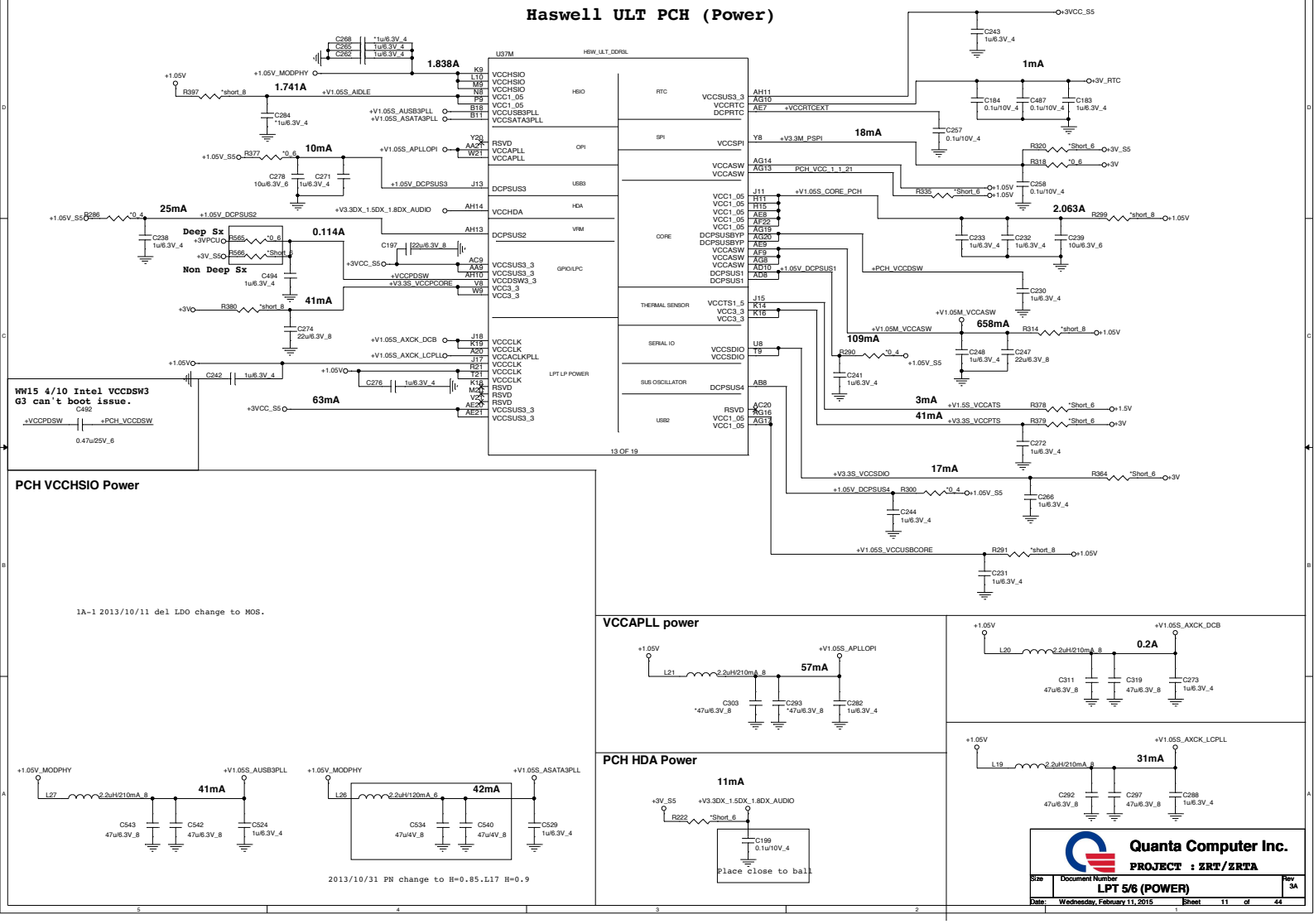
Quanta Computer Inc.

PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	3A

Date: Wednesday, February 11, 2015 Sheet 10 of 44

Haswell ULT PCH (Power)



PCH VCCHSIO Power

1A-1 2013/10/11 del LDO change to MOS.

VCCAPLL power

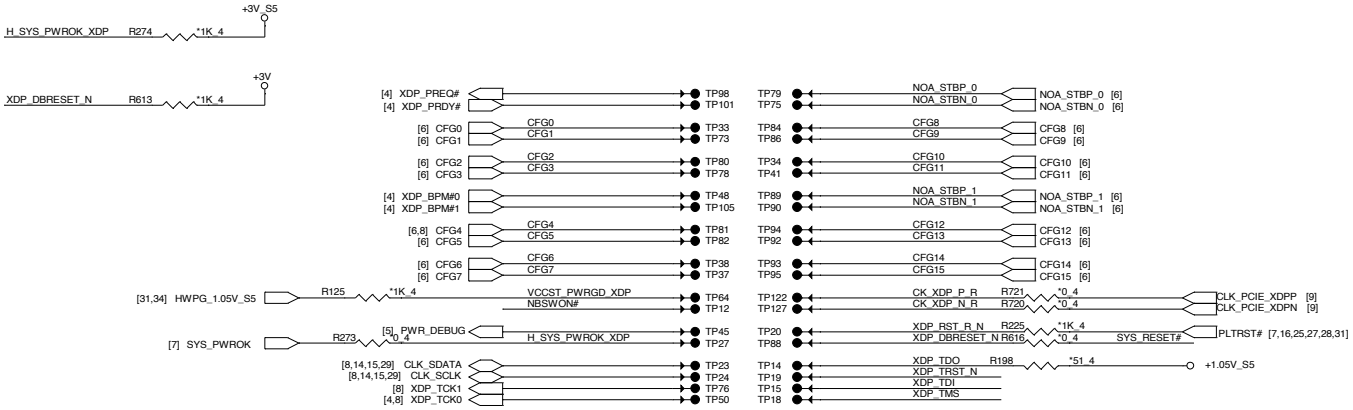
PCH HDA Power

2013/10/31 PN change to H=0.85.L17 H=0.9

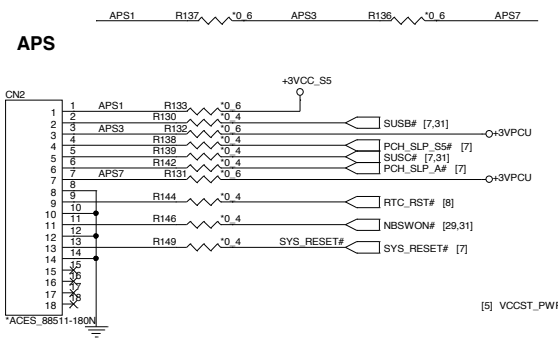
Quanta Computer Inc.			
PROJECT : ZRT/ZRTA			
Size	Document Number		Rev
	LPT 5/6 (POWER)		3A
Date: Wednesday, February 11, 2015	Sheet 11 of 44		

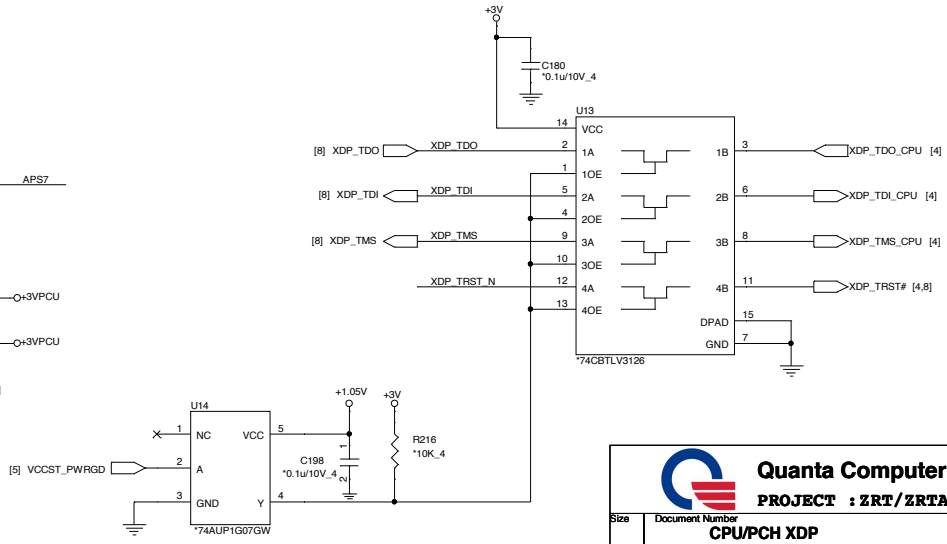
Haswell ULT (GND)

Quanta Computer Inc.			
PROJECT : ZRT/ZRTA			
Size	Document Number: LPT 6/6 (GND)		Rev 3A
Date: Wednesday, February 11, 2015	Sheet 12 of 44		



APS

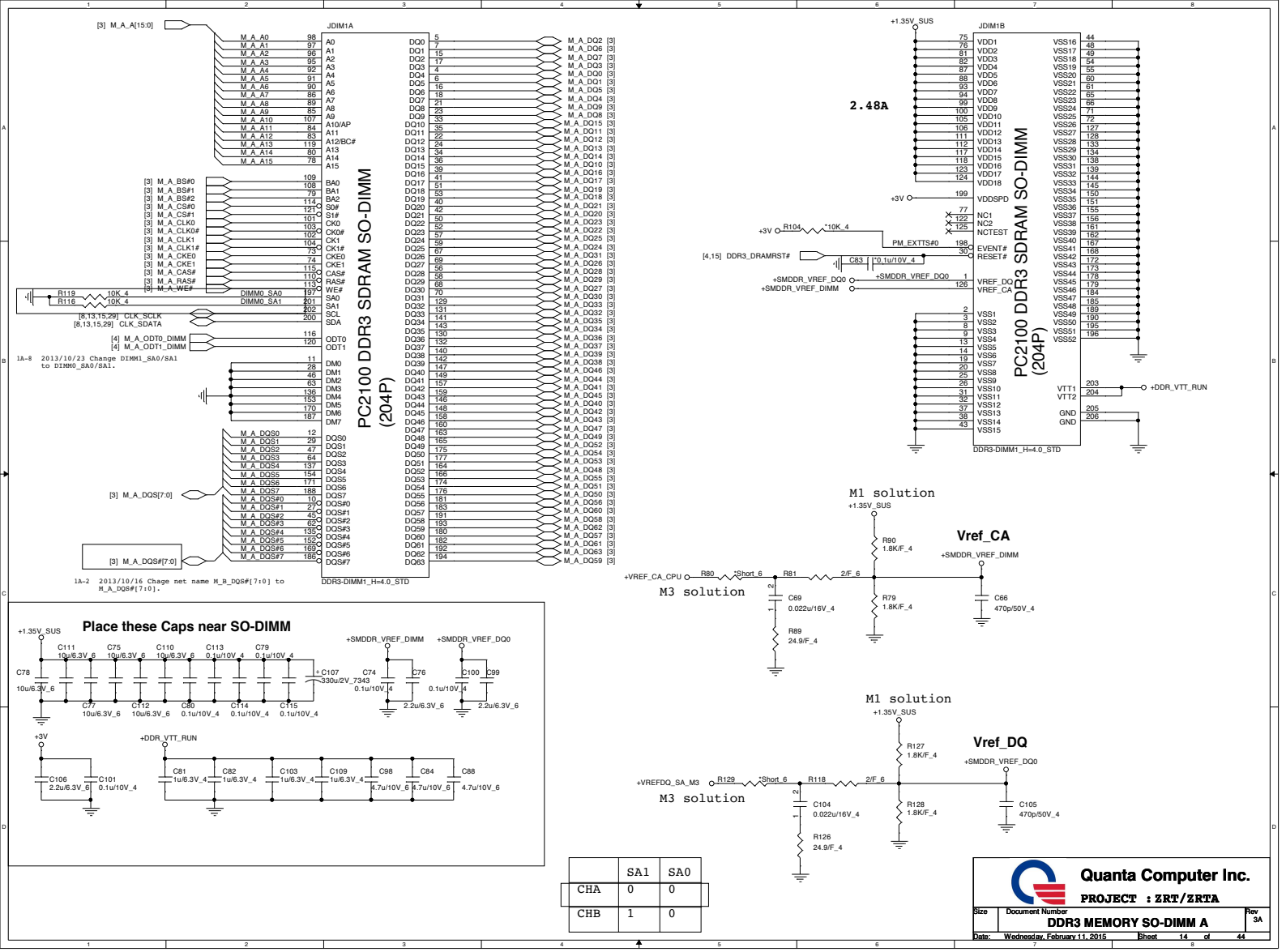




Quanta Computer Inc.

PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	CPU/PCH XDP	3A
Date: Wednesday, February 11, 2015	Sheet 13 of 44	



Place these Caps near SO-DIMM

M1 solution

M3 solution

M1 solution

M3 solution

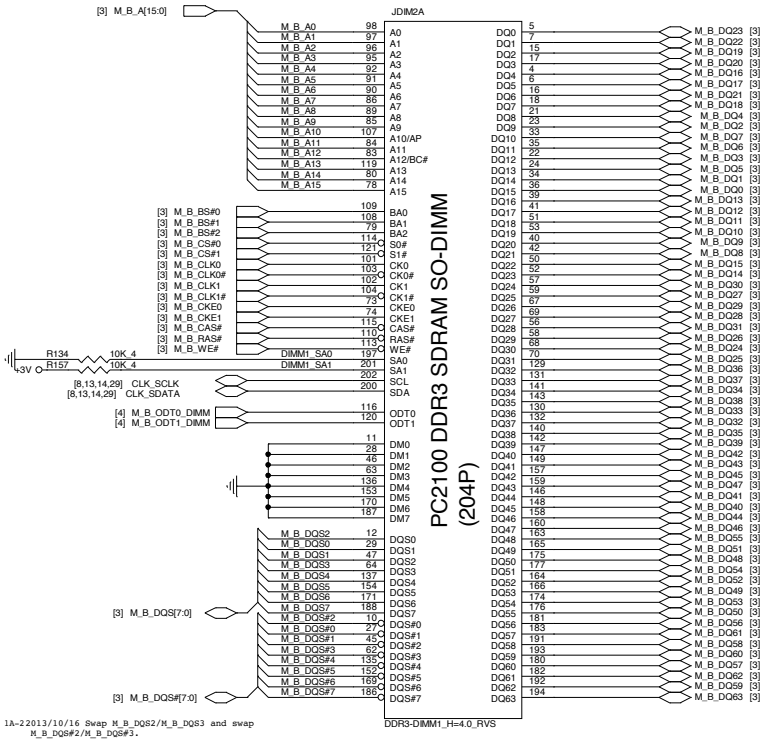
	SA1	SA0
CHA	0	0
CHB	1	0

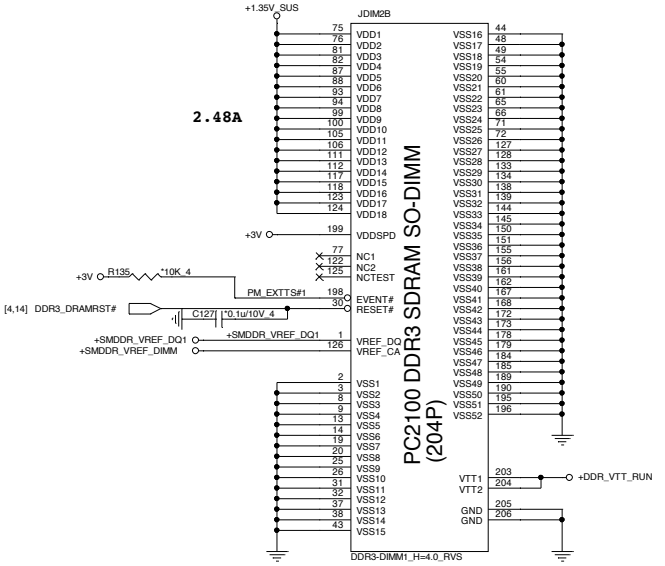
Quanta Computer Inc.

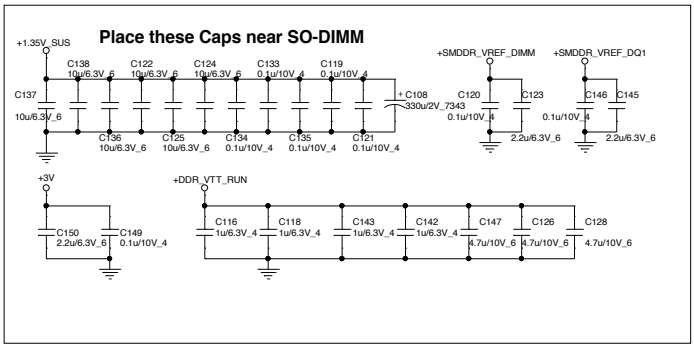
PROJECT : ZRT/ZRTA

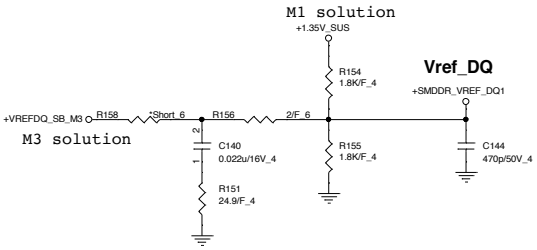
Size	Document Number	Rev
	DDR3 MEMORY SO-DIMM A	3A

Date: Wednesday, February 11, 2015 Sheet 14 of 44



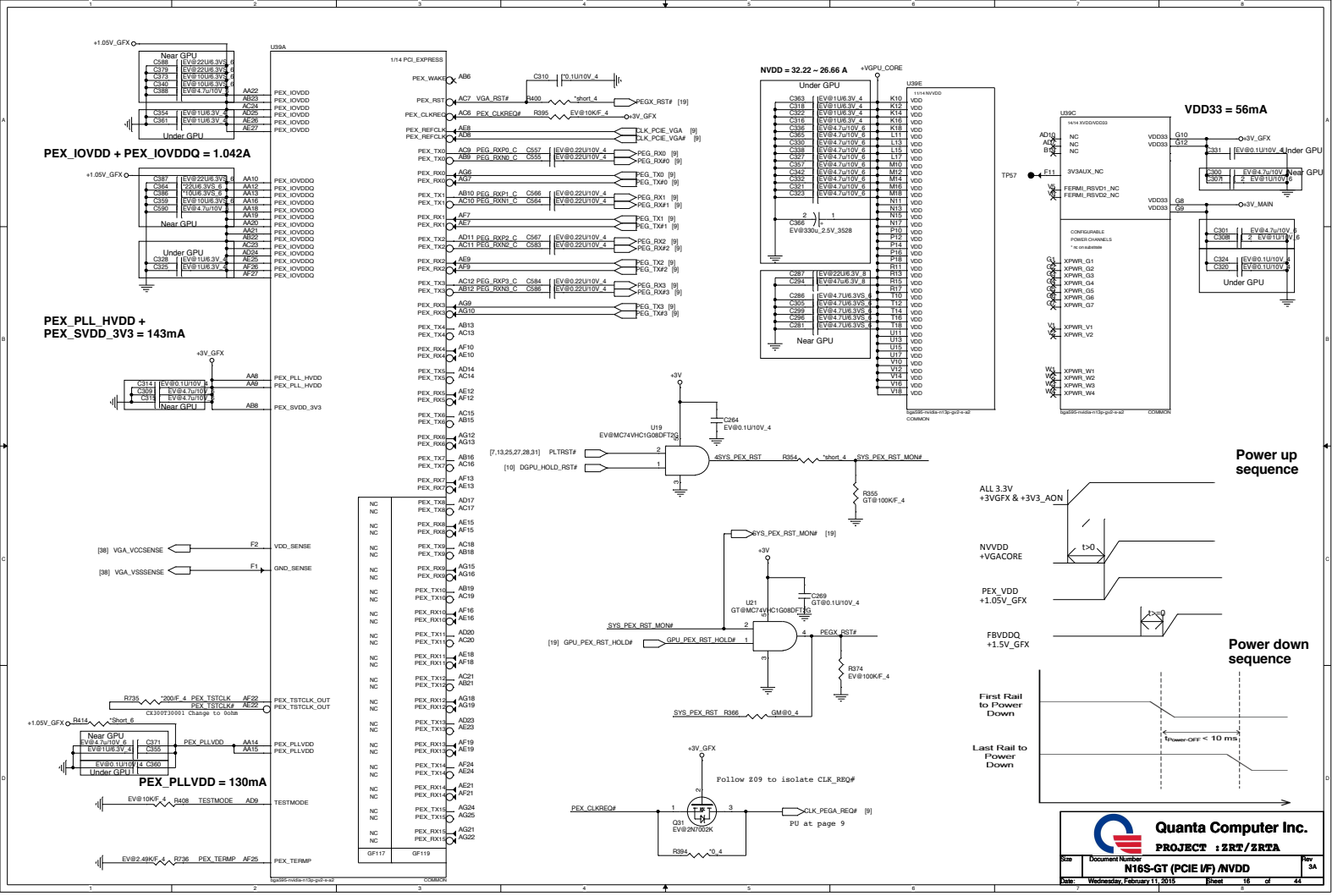


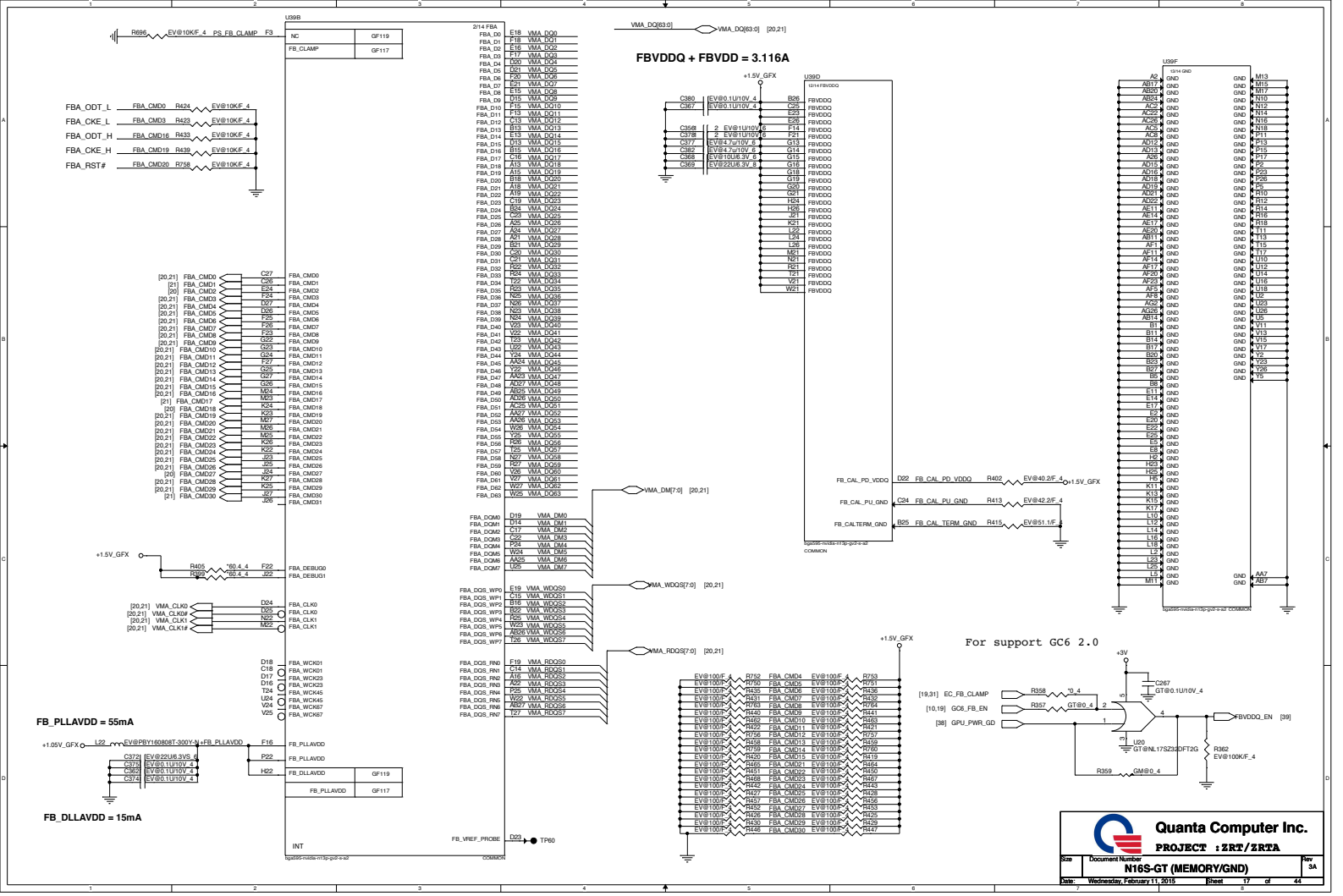


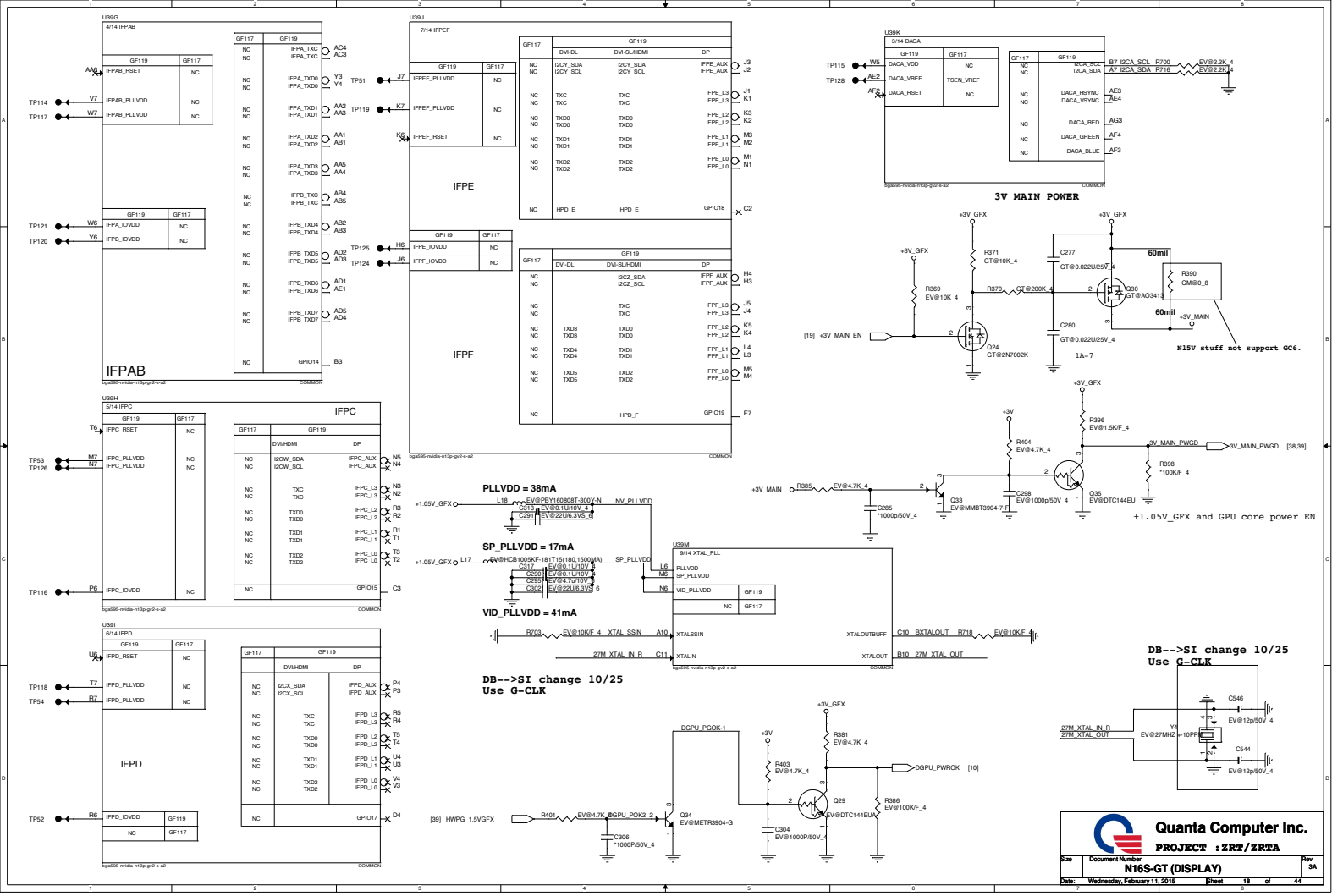


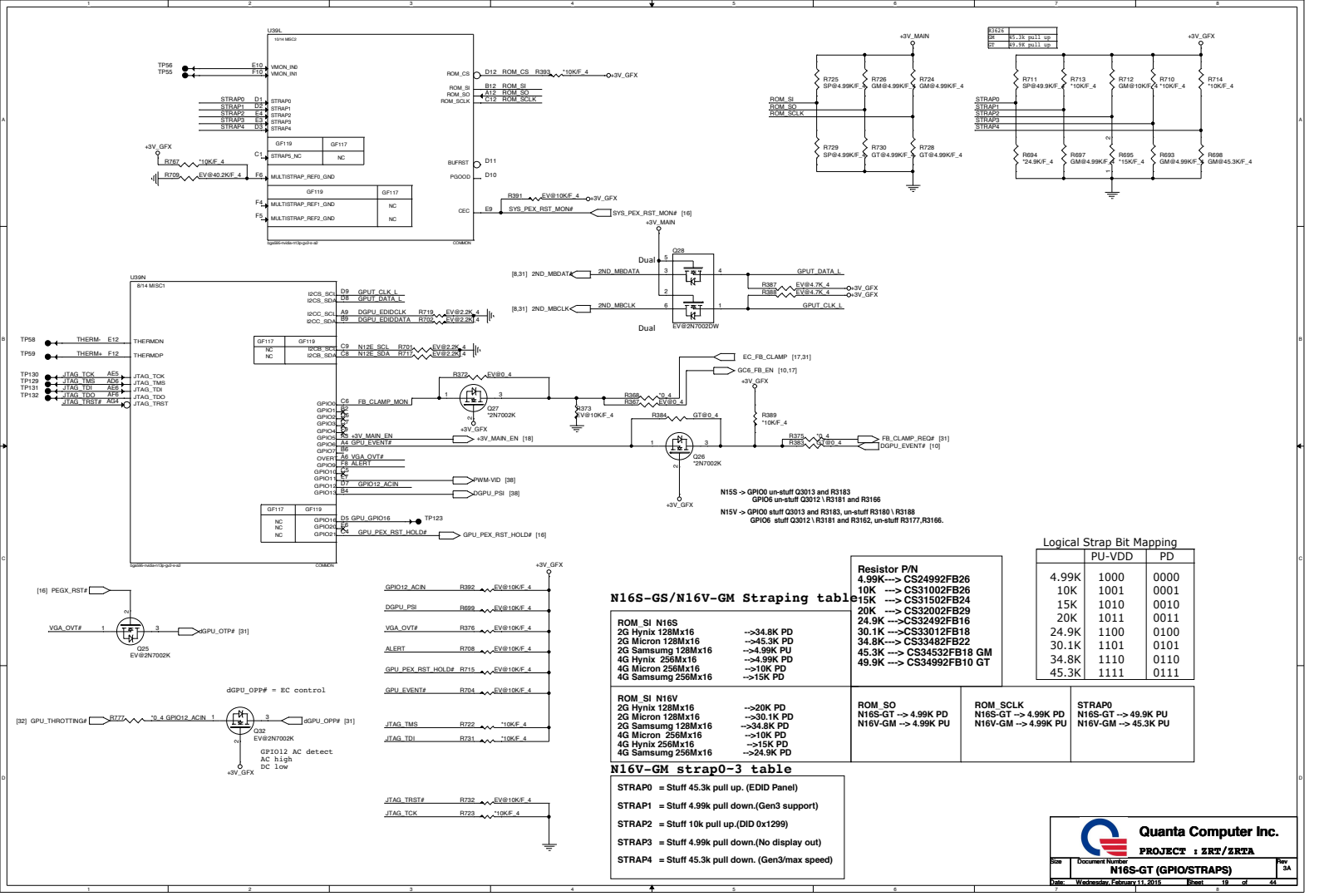
	SA1	SA0
CHA	0	0
CHB	1	0

Quanta Computer Inc.			
PROJECT : ZRT/ZRTA			
Size	Document Number: DDRIII Memory SO-DIMM B		Rev: 3A
Date: Wednesday, February 11, 2015	Sheet 15 of 44		


PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
Power up sequence
Power down sequence
ALL 3.3V
+3VGFX & +3V3_AON
NVVDD
+VGACORE
PEX_VDD
+1.05V_GFX
FBVDDQ
+1.5V_GFX
First Rail to Power Down
Last Rail to Power Down
Follow Z09 to isolate CLK_REQ#
PU at page 9
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
N16S-GT (PCIE I/F) /NVDD
Wednesday, February 11, 2015


FBVDDQ + FBVDD = 3.116A
FB_PLLAVDD = 55mA
FB_DLLAVDD = 15mA
For support GC6 2.0
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
N16S-GT (MEMORY/GND)
Wednesday, February 11, 2015


IFPAB
IFPE
IFPF
IFPC
IFPD
3V MAIN POWER
PLLVDD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
DB-->SI change 10/25
Use G-CLK
DB-->SI change 10/25
Use G-CLK
N15V stuff not support GC6.
+1.05V_GFX and GPU core power EN
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
N16S-GT (DISPLAY)
Wednesday, February 11, 2015
18
44



N16S-GS/N16V-GM Straping table

ROM_SI N16S	
2G Hynix 128Mx16	-->34.8K PD
2G Micron 128Mx16	-->45.3K PD
2G Samsumg 128Mx16	-->4.99K PU
4G Hynix 256Mx16	-->4.99K PD
4G Micron 256Mx16	-->10K PD
4G Samsumg 256Mx16	-->15K PD
ROM_SI N16V	
2G Hynix 128Mx16	-->20K PD
2G Micron 128Mx16	-->30.1K PD
2G Samsumg 128Mx16	-->34.8K PD
4G Micron 256Mx16	-->10K PD
4G Hynix 256Mx16	-->15K PD
4G Samsumg 256Mx16	-->24.9K PD

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K --->CS32492FB16
30.1K --->CS33012FB18
34.8K---> CS33482FB22
45.3K ---> CS34532FB18 GM
49.9K ---> CS34992FB10 GT

ROM_SO	ROM_SCLK	STRAP0
N16S-GT --> 4.99K PD N16V-GM --> 4.99K PU	N16S-GT --> 4.99K PD N16V-GM --> 4.99K PU	N16S-GT --> 49.9K PU N16V-GM --> 45.3K PU

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N16V-GM strap0-3 table

STRAP0 = Stuff 45.3k pull up. (EDID Panel)

STRAP1 = Stuff 4.99k pull down.(Gen3 support)

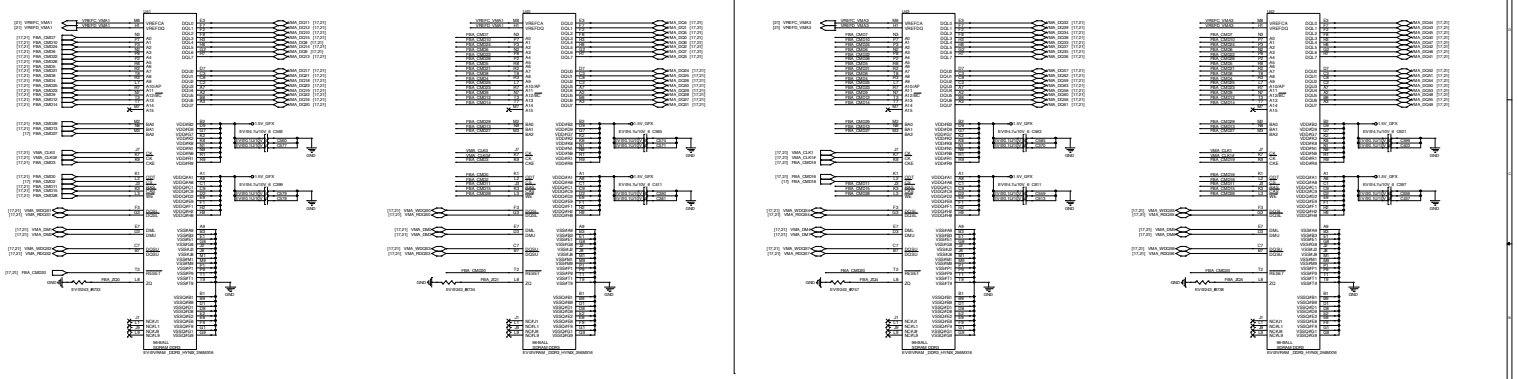
STRAP2 = Stuff 10k pull up.(DID 0x1299)

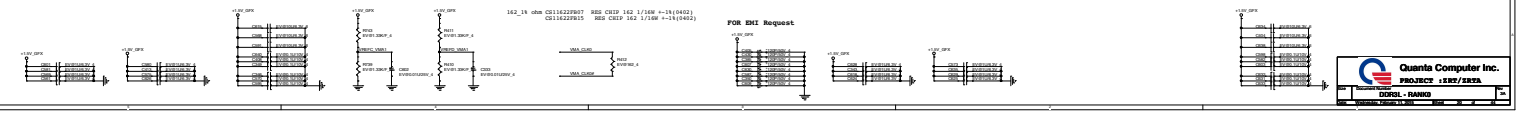
STRAP3 = Stuff 4.99k pull down.(No display out)

STRAP4 = Stuff 45.3k pull down. (Gen3/max speed)

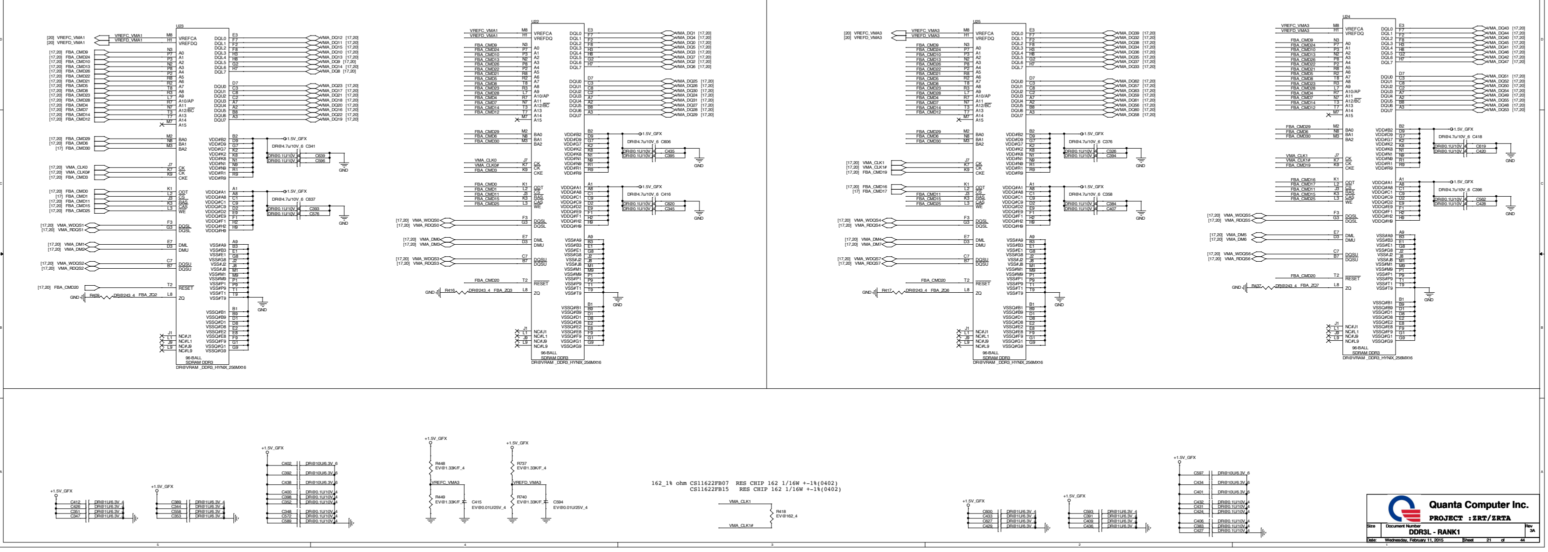
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Size | Document Number: N16S-GT (GPIO/STRAPS) | Rev: 3A
Date: Wednesday, February 11, 2015 | Sheet 19 of 44

NVU 256Mx16, K5TC4G63AFM-11C QBC PN : AKDSPGWTW07---TOP S/S PN : AKDSPGWTW07
HIC 256Mx16, MT41J2S6M16HA-093E:E QBC PN : AKDSPSTSL01---TOP S/S PN : AKDSPSTSL00
SAM 256Mx16, K4W6G1646D-BC1A QBC PN : AKDSPGWTS02---TOP S/S PN : AKDSPGWTS02





HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

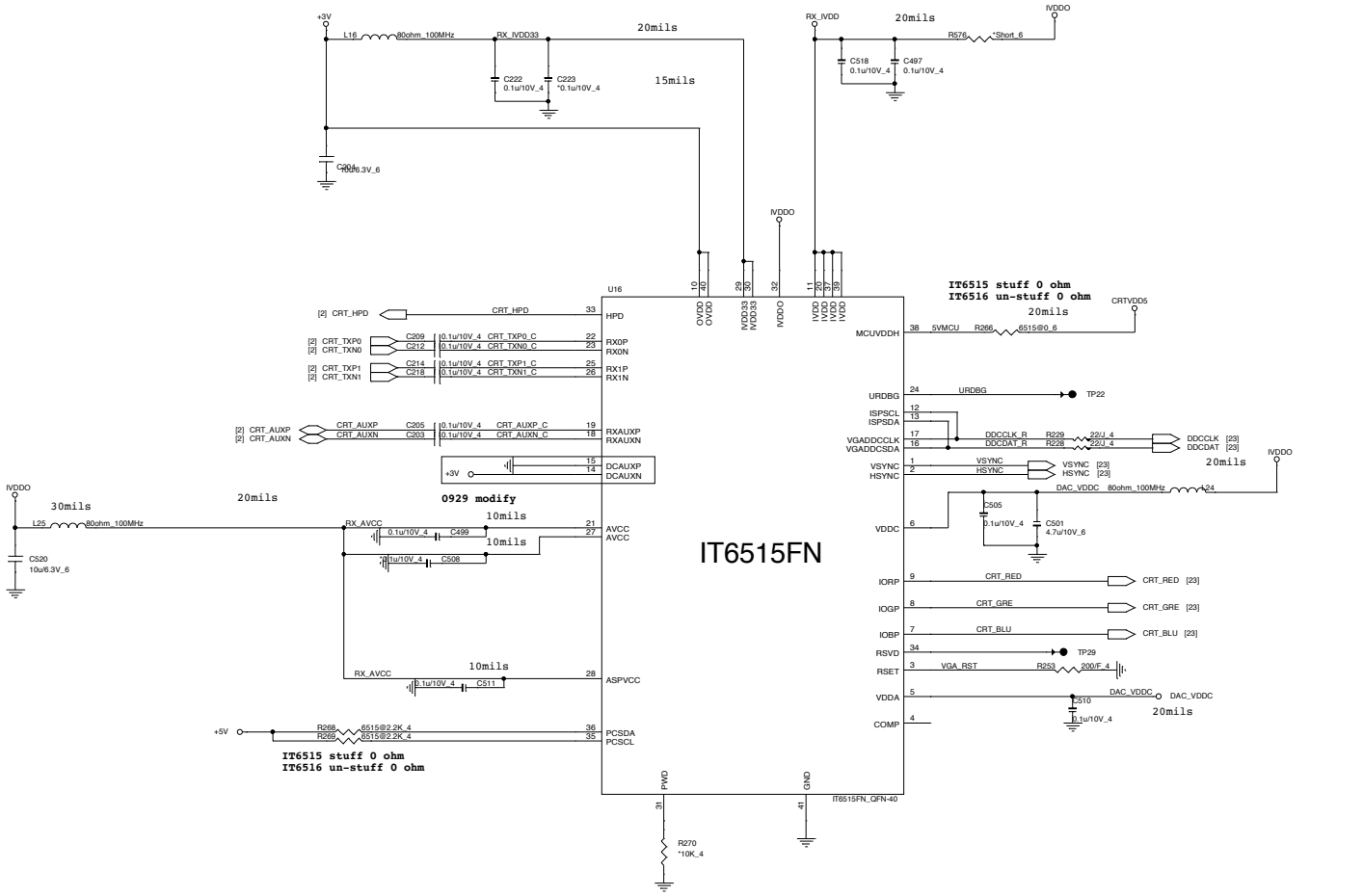
Quanta Computer Inc.

PROJECT :ZRT/ZRTA

Size	Document Number	Rev
	DDR3L - RANK1	3A

Date: Wednesday, February 11, 2015 Sheet 21 of 44

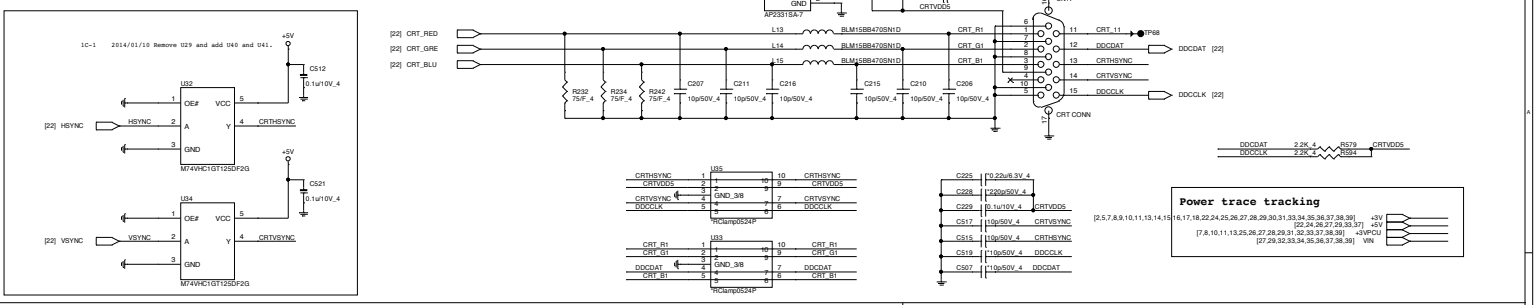
DP TO VGA



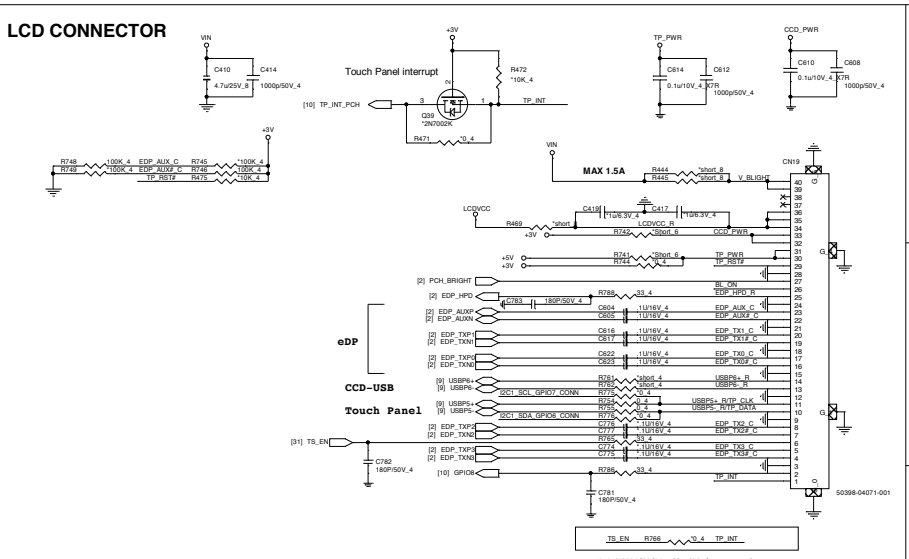
[2,5,7,8,9,10,11,13,14,15,16,17,18,23,24,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[23,24,26,27,29,33,37] +5V

Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: DP to VGA IT6165	Rev: 3A
Date: Wednesday, February 11, 2015	Sheet 22 of 44	

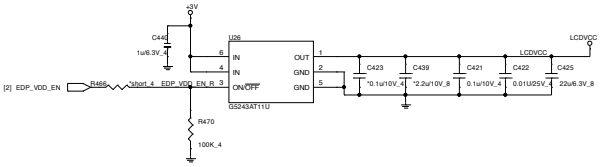
CRT



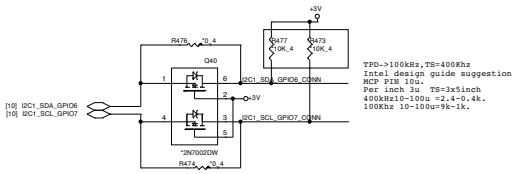
LCD CONNECTOR



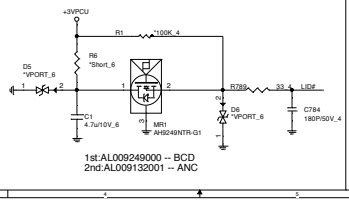
LCD Power

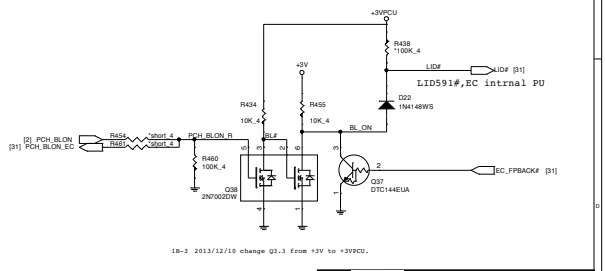


Touch screen level shift I2C(reserve)



Hall Sensor (HSR)





Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A
Date: Wednesday, February 11, 2015	Sheet 23 of 44	

HDMI

From PCH

[2] INT_HDMITX2N
[2] INT_HDMITX2P
[2] INT_HDMITX1N
[2] INT_HDMITX1P
[2] INT_HDMITX0N
[2] INT_HDMITX0P
[2] INT_HDMICLK+
[2] INT_HDMICLK-

C130 0.1u/10V_4 INT_HDMITX2N_C
C129 0.1u/10V_4 INT_HDMITX2P_C
C141 0.1u/10V_4 INT_HDMITX1N_C
C139 0.1u/10V_4 INT_HDMITX1P_C
C132 0.1u/10V_4 INT_HDMITX0N_C
C131 0.1u/10V_4 INT_HDMITX0P_C
C148 0.1u/10V_4 INT_HDMICLK+_C
C151 0.1u/10V_4 INT_HDMICLK-_C

R161 R159 R145 R148 R150 R153 R140 R143
470_4

IB-1 20131108 Change +5V to +3V for DG.

+5V
Q44
2N7002E
R521 *100K/F_4

HDMI connector

CN12
INT_HDMITX0P_C
INT_HDMITX0N_C
INT_HDMITX1P_C
INT_HDMITX1N_C
INT_HDMITX2P_C
INT_HDMITX2N_C
INT_HDMICLK+_C
INT_HDMICLK-_C
HDMI_DDCCLK_MB
HDMI_DDCDATA_MB
HDMI_5V
HDMI_MB_HPD_R527
*short_4HP_DET_CN
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL1
SHELL2
GND
HDMI connector

+5V
Q10
IN OUT GND
AP2331SA-7
C153 *220p/50V_4
D21 *AZ5125-01J
R529 20K_4

HDMI-detect

+3V
R526 1M_4
[2] INT_HDMI_HPD
Q47
2N7002K
HDMI_MB_HPD

I2C

From PCH

[2] HDMI_DDCCLK_SW
[2] HDMI_DDCDATA_SW

+3V
+5V
D24 RB501V-40
R519 2.2K_4
R520 2.2K_4
Q45
2N7002K
HDMI_DDCCLK_MB

D26 RB501V-40
R523 2.2K_4
R524 2.2K_4
Q46
2N7002K
HDMI_DDCDATA_MB

EMI

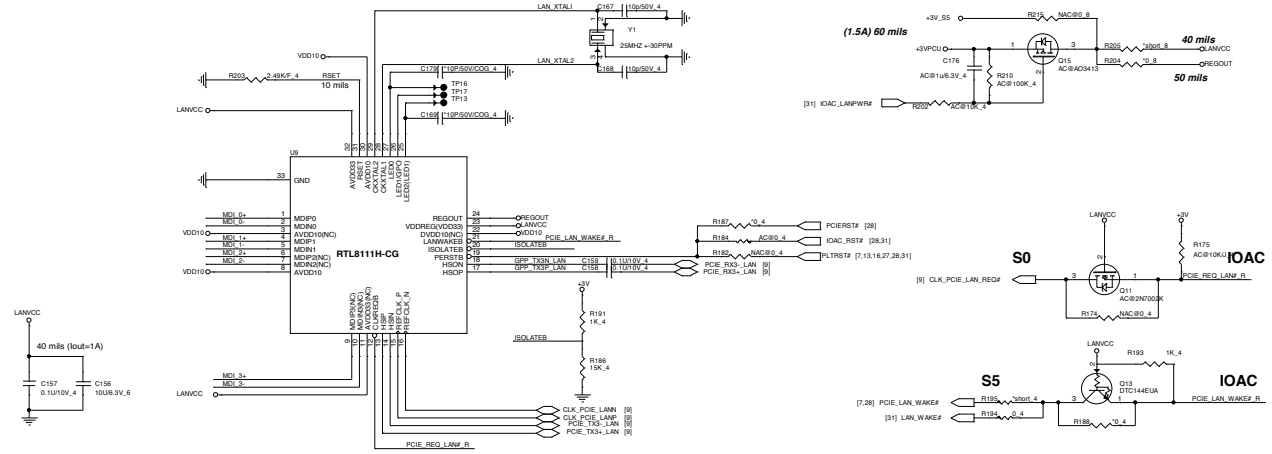
INT_HDMITX2P_C
R141 *120/F_4
INT_HDMITX2N_C
INT_HDMITX1P_C
R152 *120/F_4
INT_HDMITX1N_C
INT_HDMITX0P_C
R147 *120/F_4
INT_HDMITX0N_C
INT_HDMICLK+_C
R160 *120/F_4
INT_HDMICLK-_C

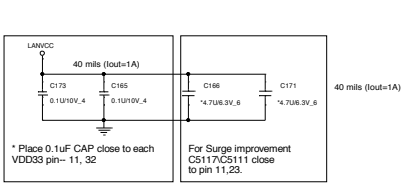
Power trace tracking

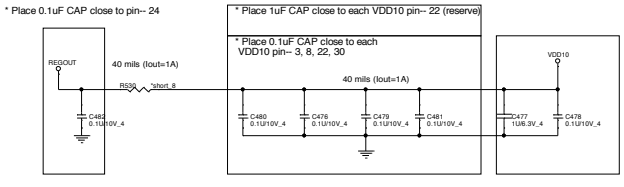
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[22,23,26,27,29,33,37] +5V

Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Size | Document Number | Rev
HDMI (PS8101) | 1A
Date: Wednesday, February 11, 2015 Sheet 24 of 44

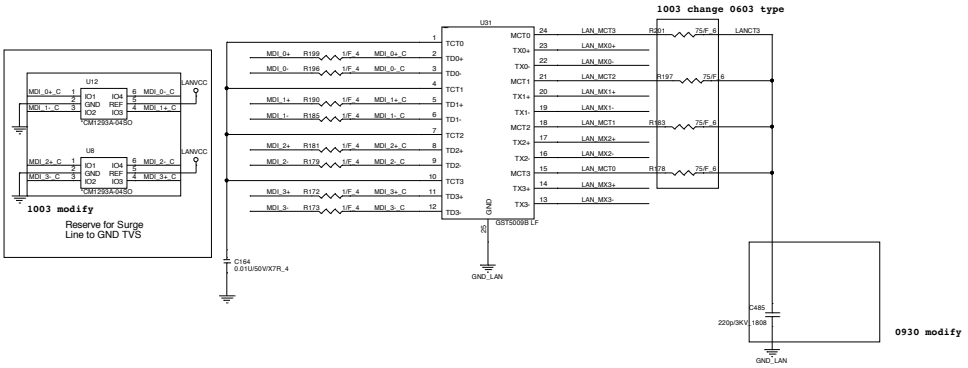
LAN



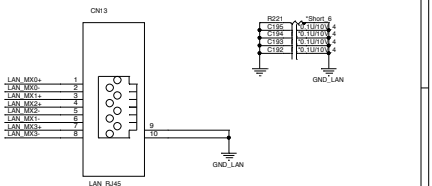




Tramsformer



RJ45 Connector



Power trace tracking

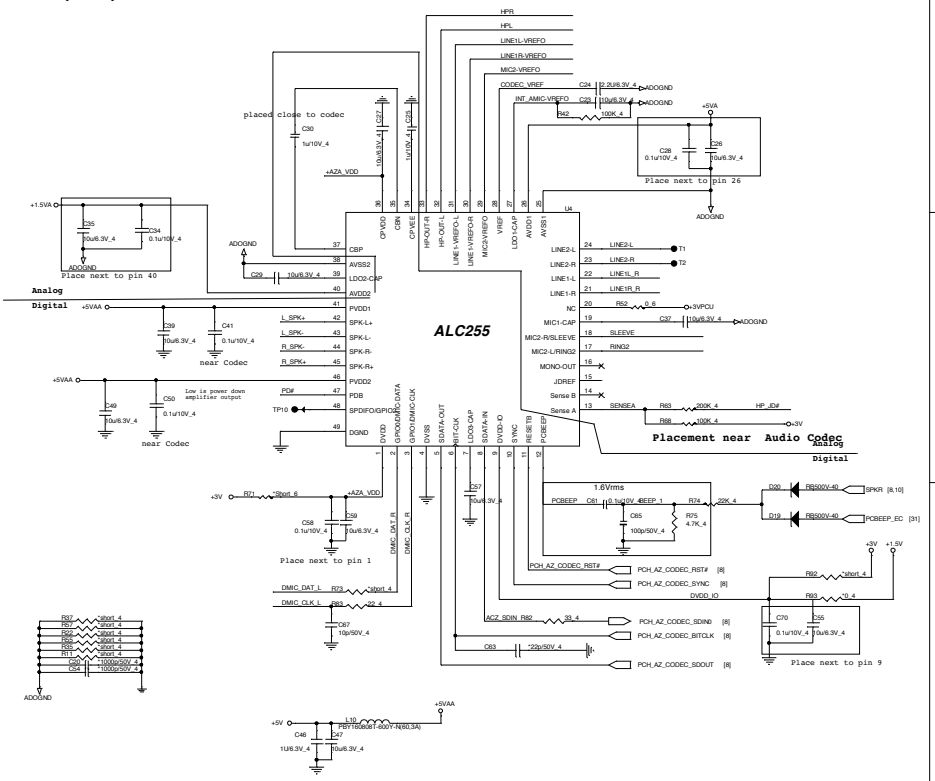
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[5,7,8,9,10,11,13,27,29,31,33,36,38] +3V_S5
[7,8,10,11,13,23,26,27,28,29,31,32,33,37,38,39] +3VPCU

Quanta Computer Inc.

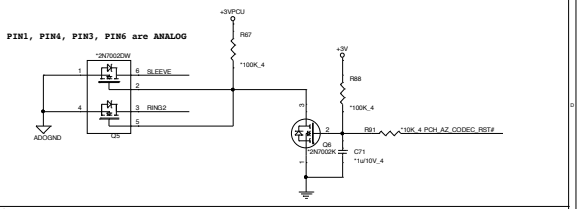
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	LAN (RTL8111GS)	1A
Date: Wednesday, February 11, 2015	Sheet 25 of 44	

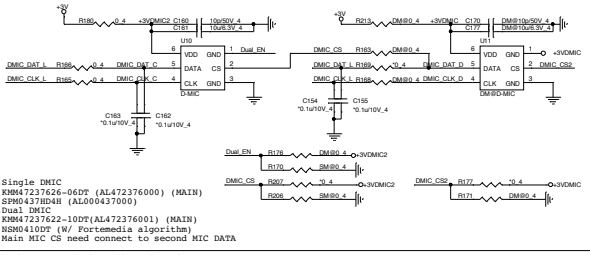
Codec(ADO)



Grounding circuit(ADO)

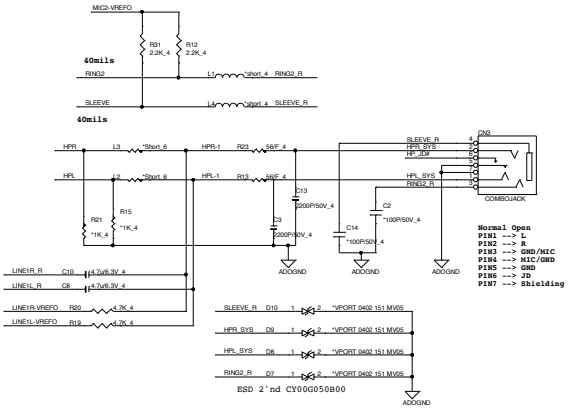


D-Mic



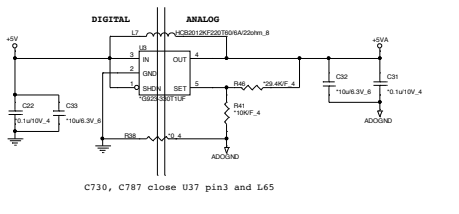
1.Single DMIC
KMM47237626-06DT (AL472376000) (MAIN)
SPM0437HD4H (AL000437000)
2.Dual DMIC
KMM47237622-10DT(AL472376001) (MAIN)
NSM0410DT (W/ Fortemedia algorithm)
Main MIC CS need connect to second MIC DATA

Universal Audio Jack



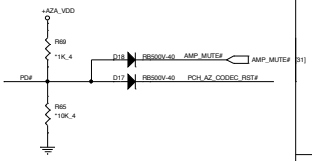
Normal Open
PIN1 --> L
PIN2 --> R
PIN3 --> GND/MIC
PIN4 --> MIC/GND
PIN5 --> GND
PIN6 --> JD
PIN7 --> Shielding

Codec PWR 5V(ADO)

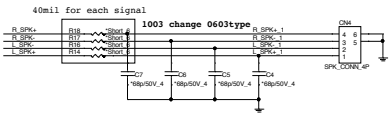


C730, C787 close U37 pin3 and L65

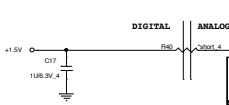
Mute(ADO)



Internal Speaker



Codec PWR 3V/1.5V(ADO)



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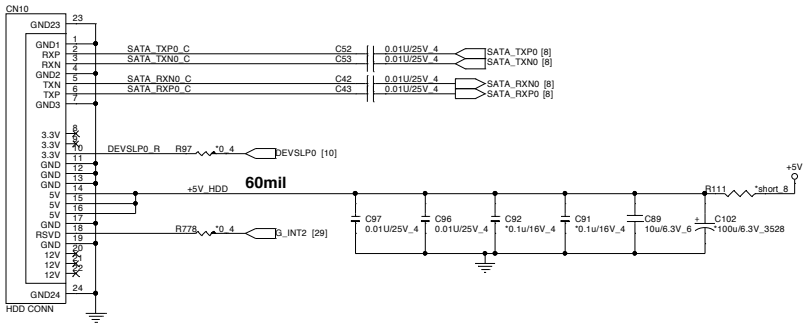
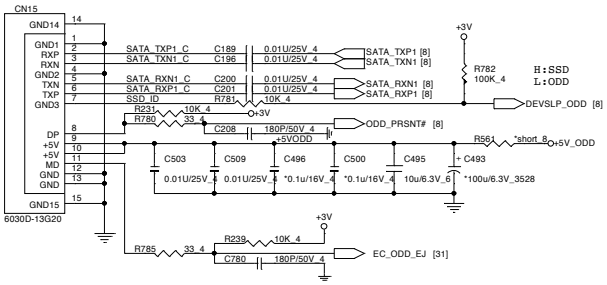
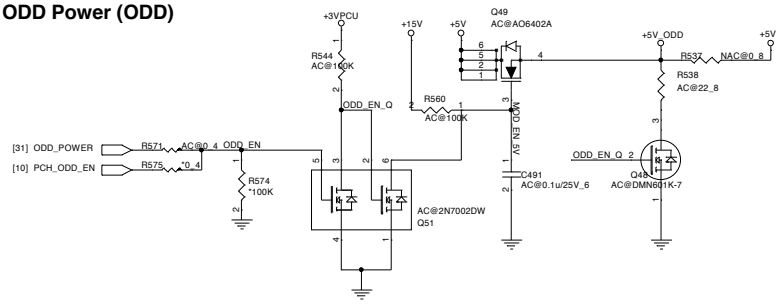
2.5" SATA HDD (HDD)



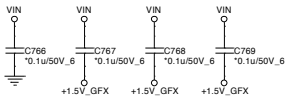
SATA ODD Connector(ODD)



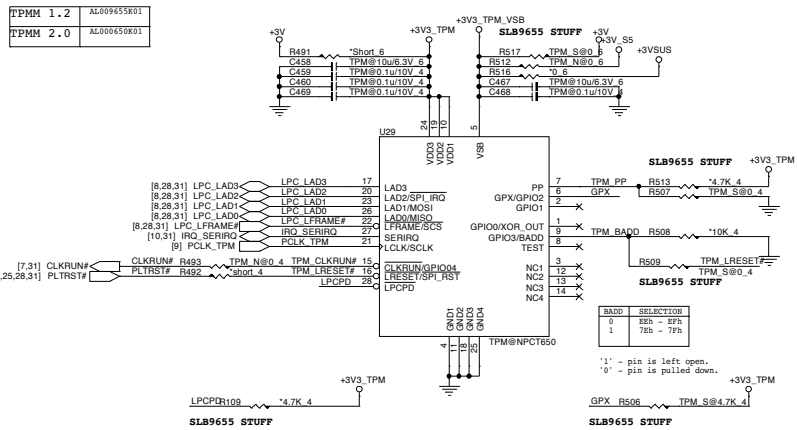
ODD Power (ODD)

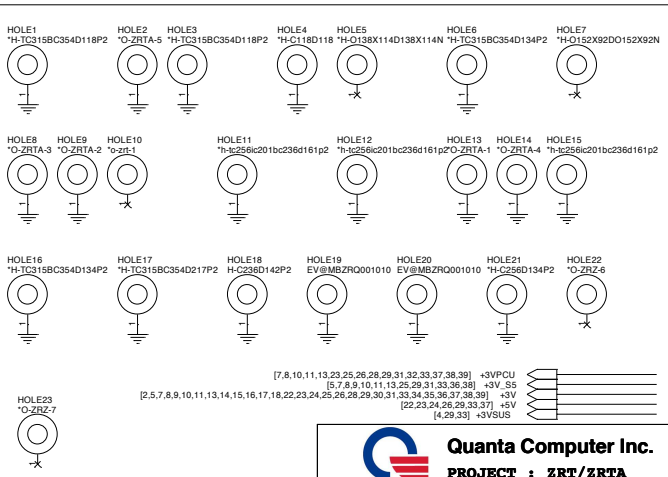


EMI



TPM NPCT650 (TPM)





[7,8,10,11,13,23,25,26,28,29,31,32,33,37,38,39] +3VPCU
[5,7,8,9,10,11,13,25,29,31,33,36,38] +3V_S5
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,25,26,28,29,30,31,33,34,35,36,37,38,39] +3V
[22,23,24,26,29,33,37] +5V
[4,29,33] +3VSUS

Quanta Computer Inc.
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Size	Document Number	Rev
	HDD/ODD/TPM NPCT650	1A
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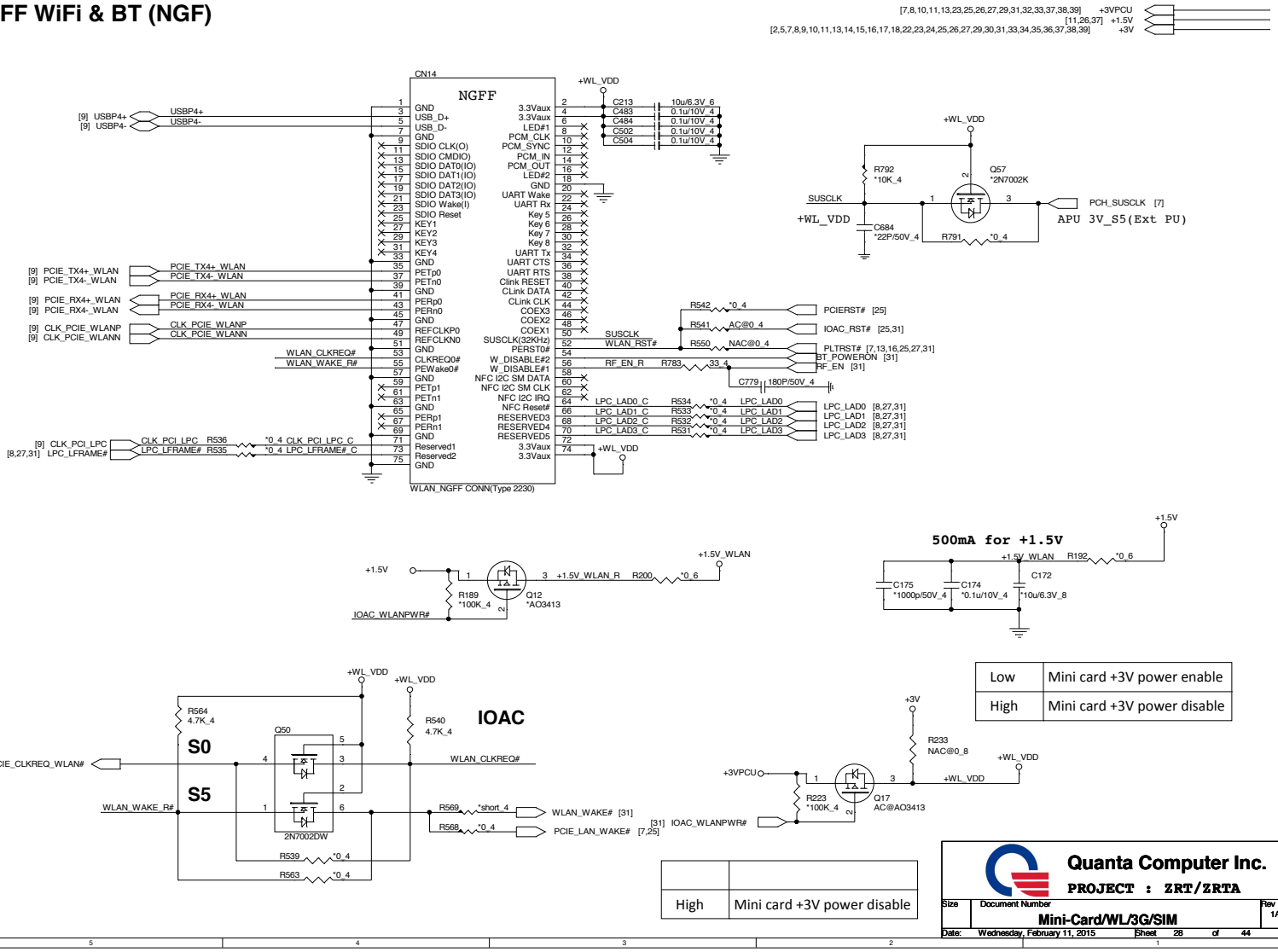
NGFF WiFi & BT (NGF)



Low	Mini card +3V power enable
High	Mini card +3V power disable

High	Mini card +3V power disable

Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: Mini-Card/WL/3G/SIM	Rev: 1A
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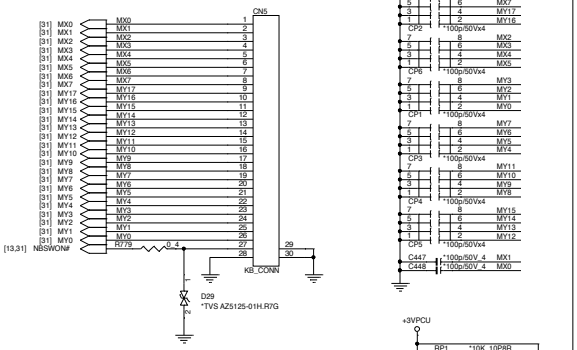
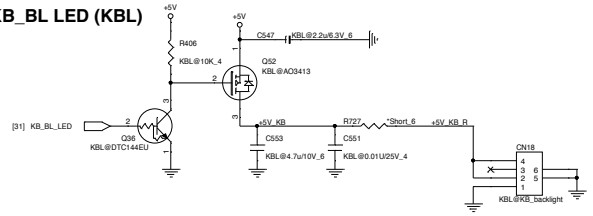
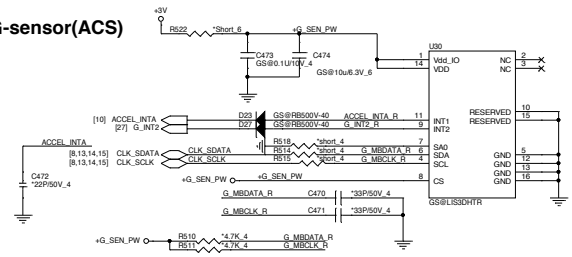
K/B (KBC)



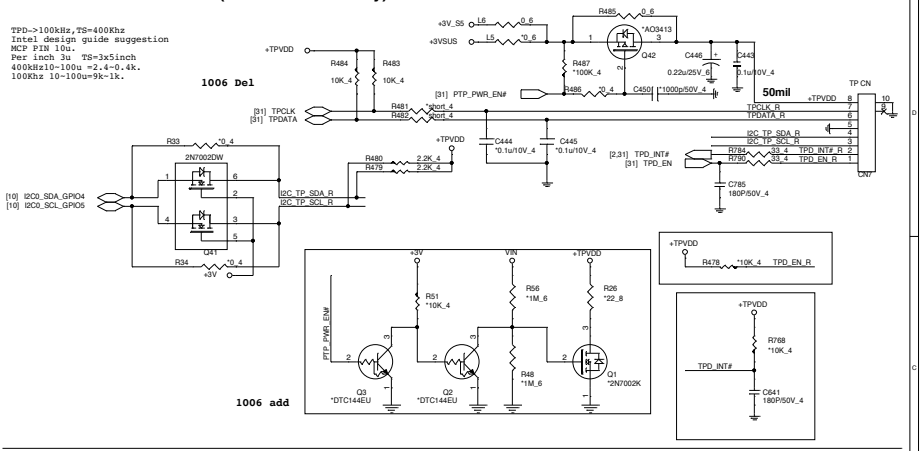
KB_BL LED (KBL)



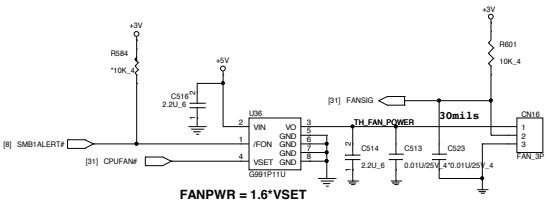
G-sensor(ACS)



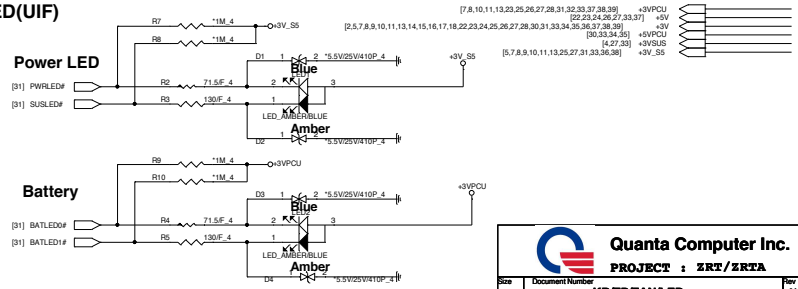
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



CPU FAN (THM)



POWER LED(UIF)



Quanta Computer Inc.
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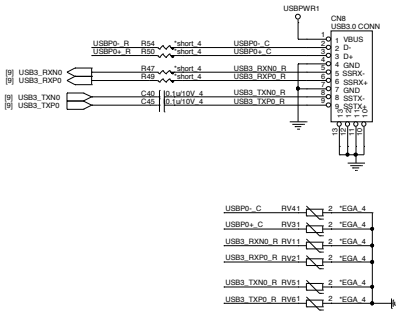
USB 3.0 Connector(UB3)



USB Charger for USB3.0 Port0 (UBC)

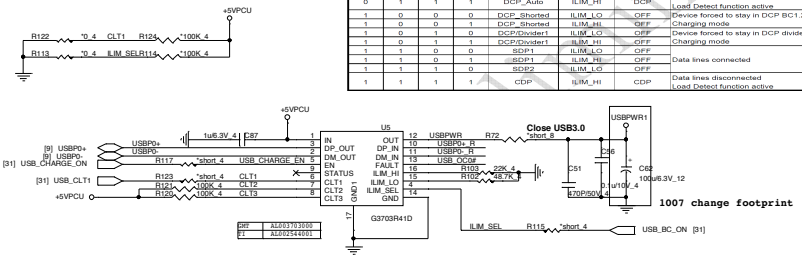
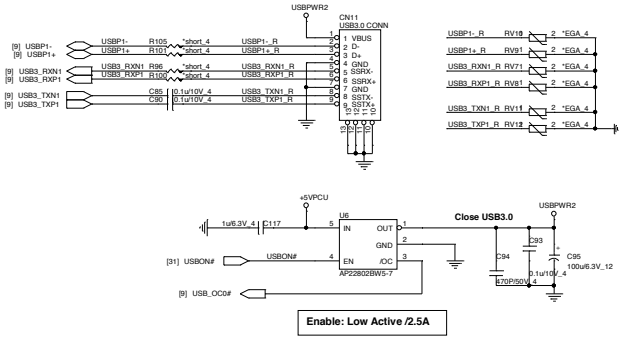


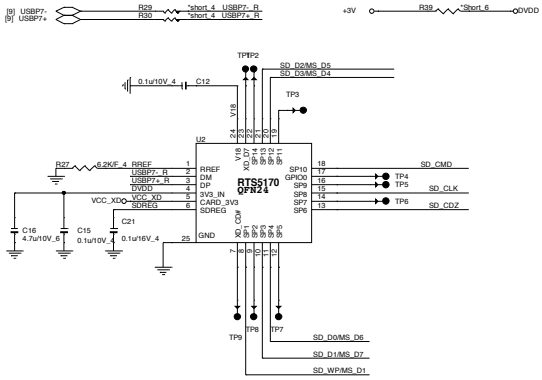
Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	
0	0	0	1	Discharge	NA	OFF	OUT held low
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	Charging mode
1	1	0	0	SDP1	ILIM_LO	OFF	
1	1	0	1	SDP1	ILIM_HI	OFF	Data lines connected
1	1	1	0	SDP2	ILIM_LO	OFF	
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active

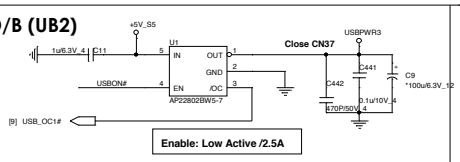
USB 3.0 Connector(UB3)



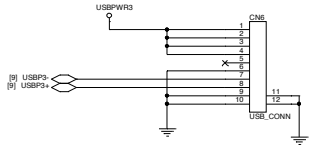
Card Reader (CRD)



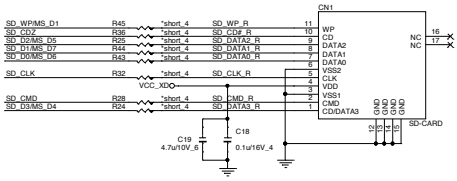
USB IO D/B (UB2)



D/B USB Port



SD/MMC CARD READER (CRD)



Quanta Computer Inc.		
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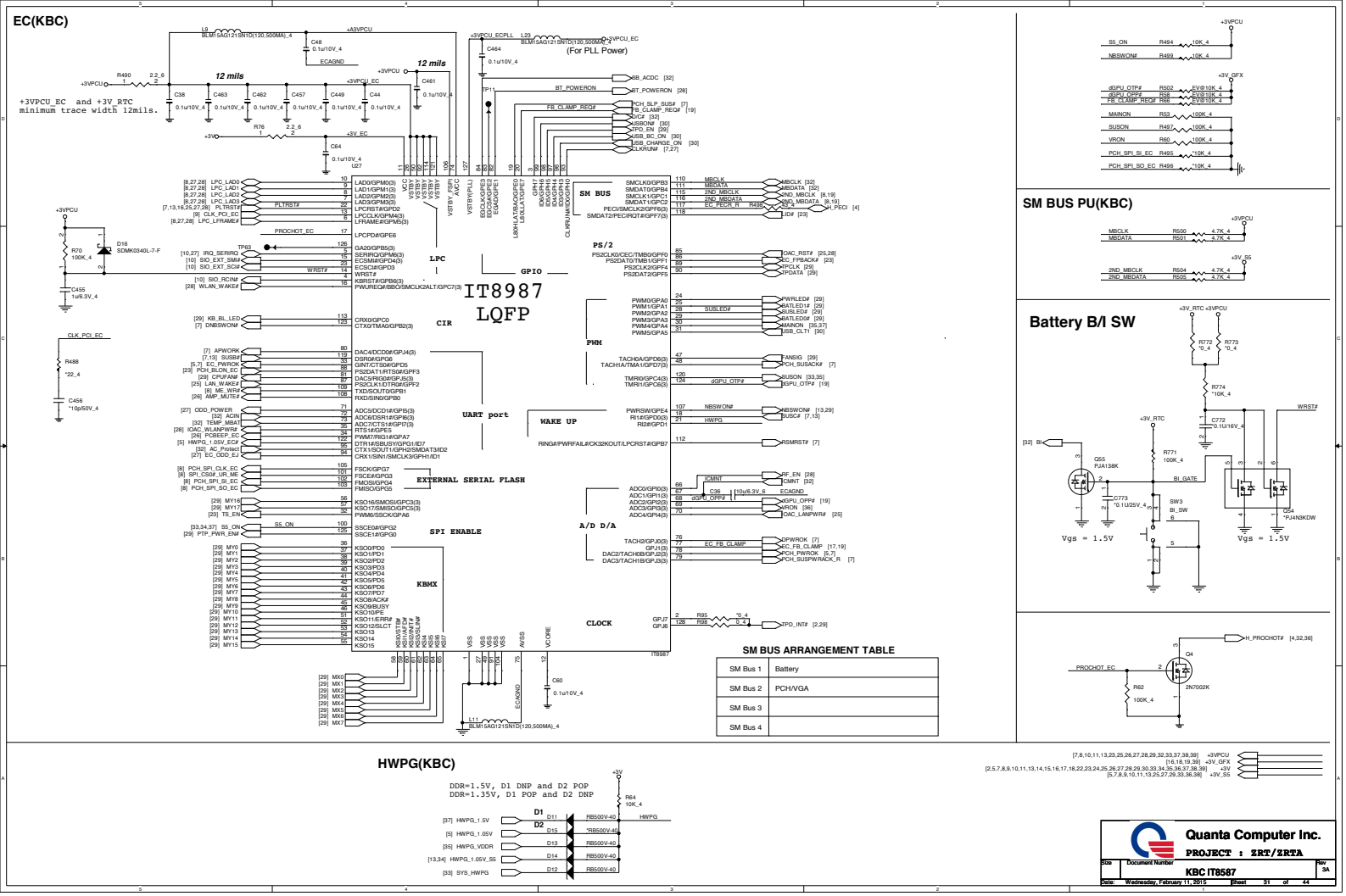

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

Quanta Computer Inc.			
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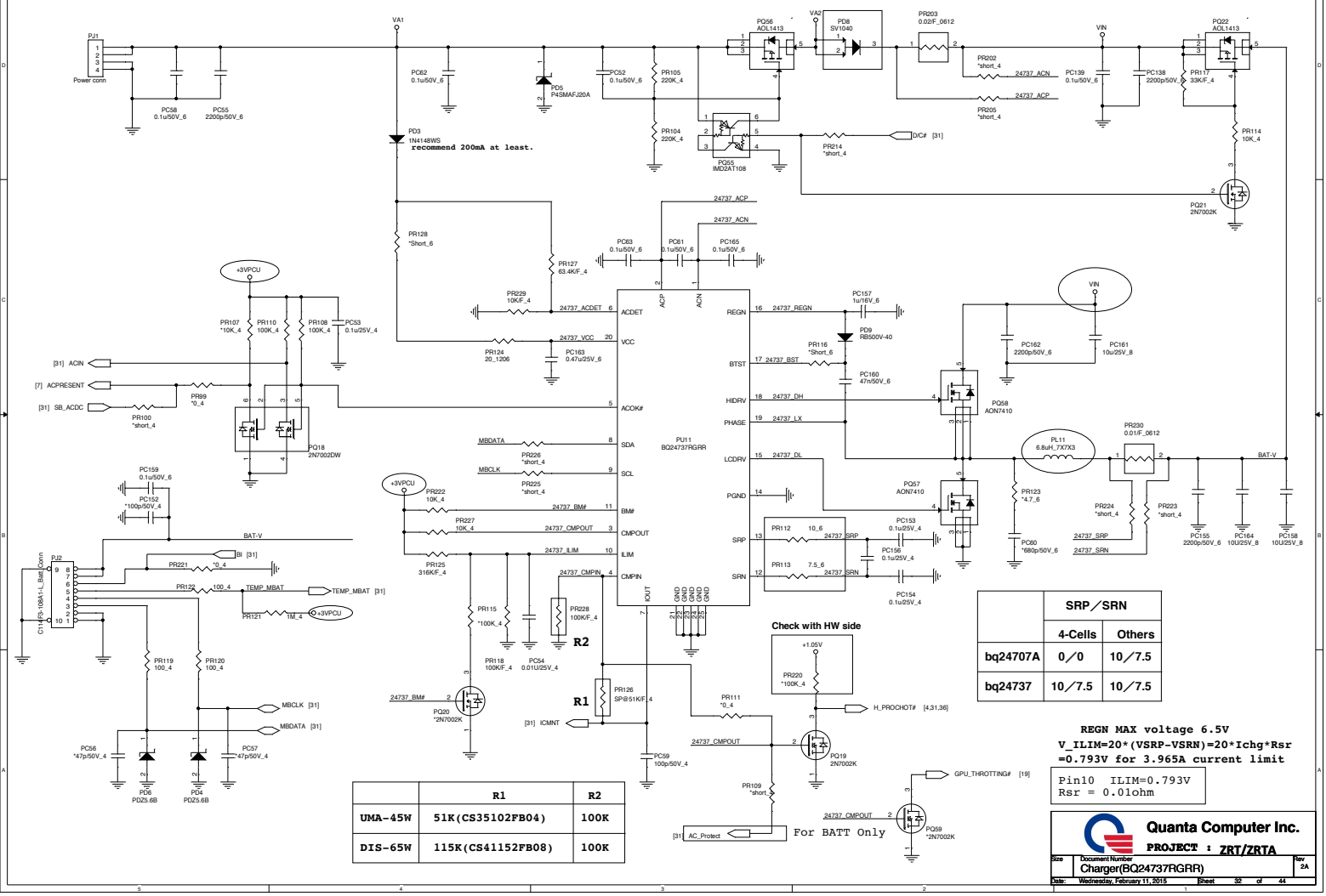

	SRP／SRN	
	4-Cells	Others
bq24707A	0／0	10／7.5
bq24737	10／7.5	10／7.5

	R1	R2
UMA-45W	51K(CS35102FB04)	100K
DIS-65W	115K(CS41152FB08)	100K

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

Pin10 ILIM=0.793V
Rsr = 0.01ohm

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PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	Charger(BQ24737RGRR)	2A
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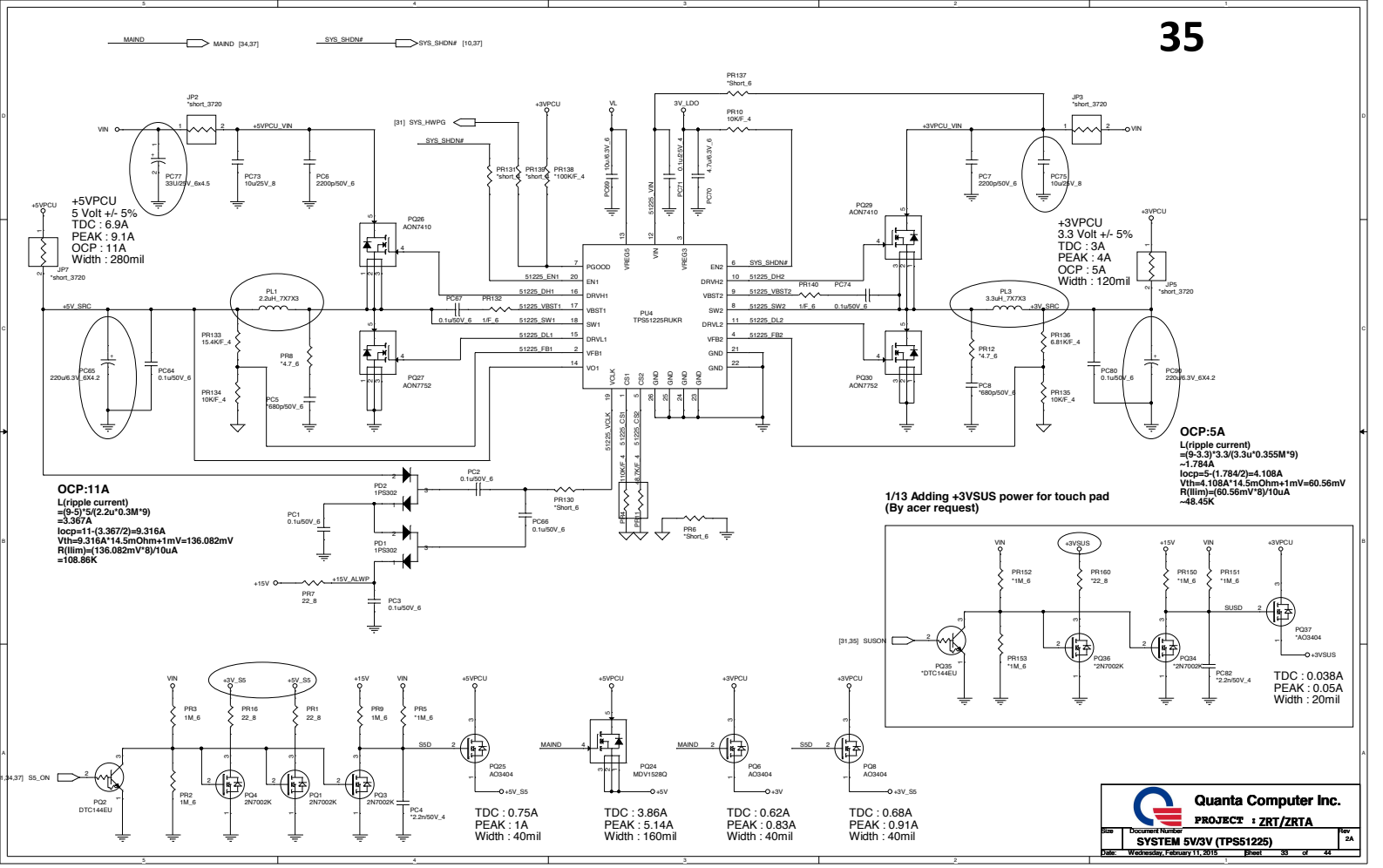
MAIND
MAIND [34,37]
SYS_SHDN#
SYS_SHDN# [10,37]
+5VPCU
5 Volt +/- 5%
TDC : 6.9A
PEAK : 9.1A
OCP : 11A
Width : 280mil
+3VPCU
3.3 Volt +/- 5%
TDC : 3A
PEAK : 4A
OCP : 5A
Width : 120mil
OCP:11A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=11-(3.367/2)=9.316A
Vth=9.316A*14.5mOhm+1mV=136.082mV
R(ilim)=(136.082mV*8)/10uA
=108.86K
OCP:5A
L(ripple current)
=(9-3.3)*3.3/(3.3u*0.355M*9)
~1.784A
Iocp=5-(1.784/2)=4.108A
Vth=4.108A*14.5mOhm+1mV=60.56mV
R(ilim)=(60.56mV*8)/10uA
~48.45K
1/13 Adding +3VSUS power for touch pad
(By acer request)
TDC : 0.038A
PEAK : 0.05A
Width : 20mil
TDC : 0.75A
PEAK : 1A
Width : 40mil
TDC : 3.86A
PEAK : 5.14A
Width : 160mil
TDC : 0.62A
PEAK : 0.83A
Width : 40mil
TDC : 0.68A
PEAK : 0.91A
Width : 40mil
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
SYSTEM 5V/3V (TPS51225)
Wednesday, February 11, 2015
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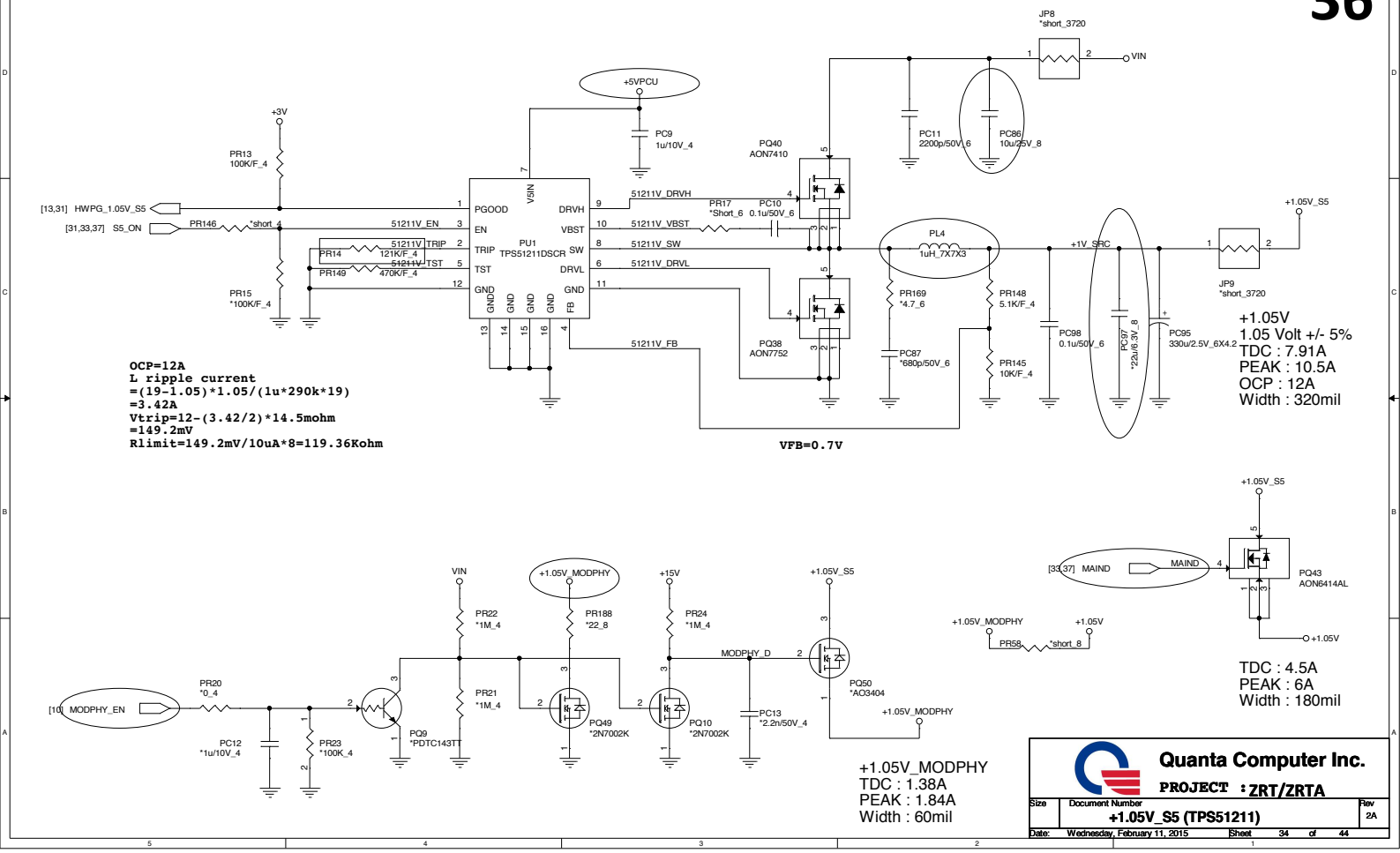

Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	+1.05V_S5 (TPS51211)	2A
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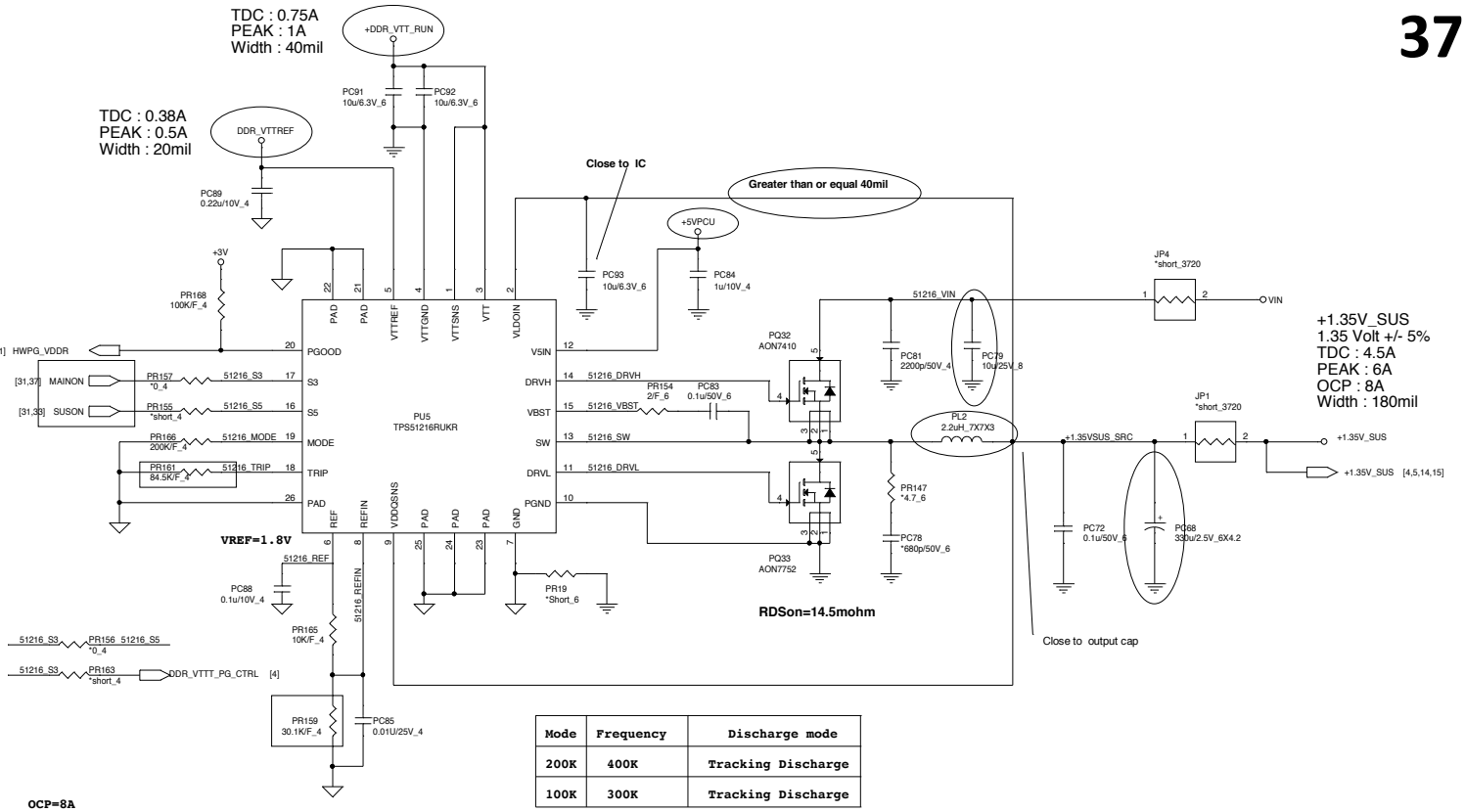

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=8A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=8-(1.425/2)*14.5mohm
=105.668mV
Rlimit=105.668mV/10uA*8=84.53Kohm

DDR=1.35V
PR84=10K/F_4
PR86=30.1K/F_4

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Size	Document Number	Rev
	DDR 1.35V(TPS51216)	2A
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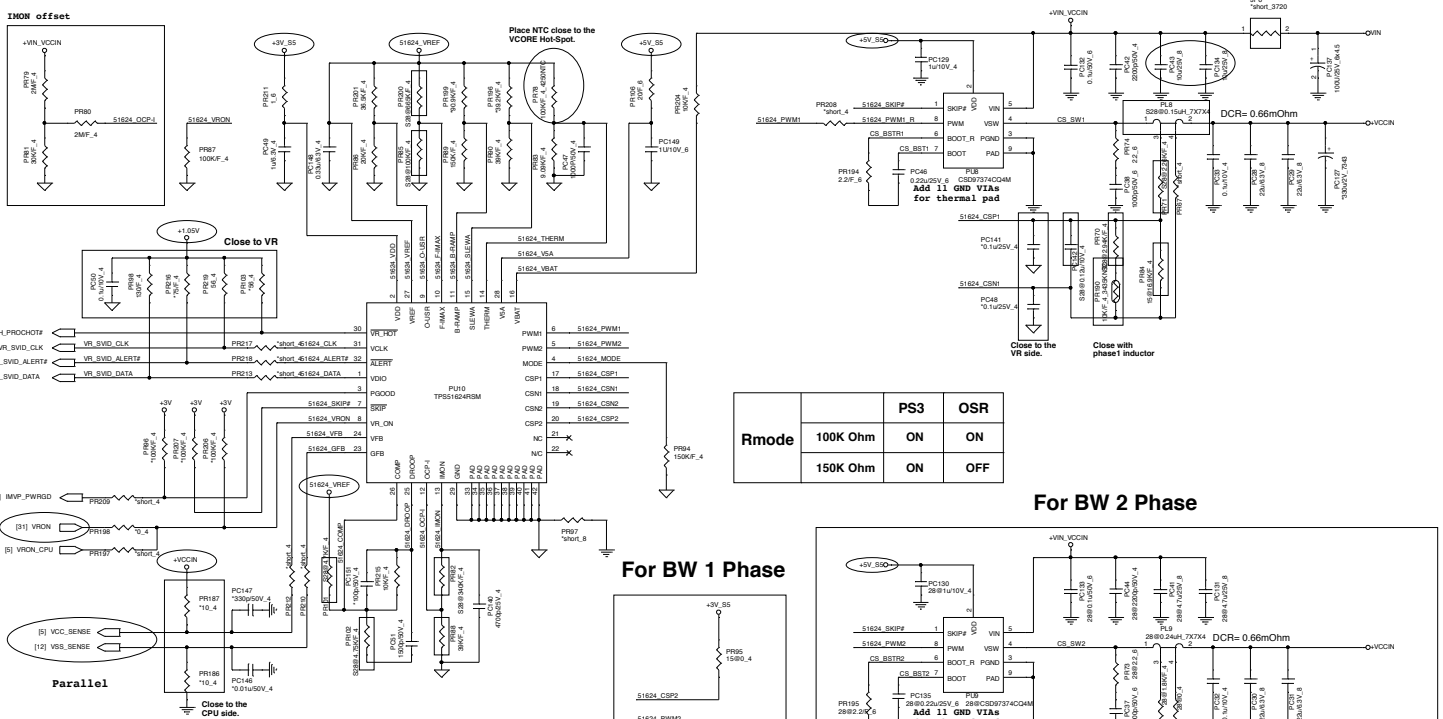
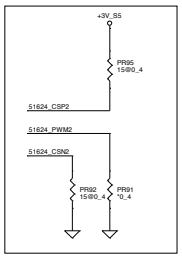


Rmode		PS3	OSR
	100K Ohm	ON	ON
	150K Ohm	ON	OFF

For BW 1 Phase



For BW 2 Phase

BW-U 15W (1 phase)

Icc TDC PL2：14A
Icc Max：32A
OCP：37A
Fsw：1.2MHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

BW-U 28W (1 phase)

Icc TDC PL2：19A
Icc Max：40A
OCP：47A
Fsw：800KHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

S28@

BW-U 28W 2 phase			
Location	Value	Location	Value
PL8	CV+24P0MZ00	PR85	CS35622FB10
PR71	CS21822FB14	PR101	CS22372FB11
PR82	CS41502FB18	PR102	CS31002FB26
PR70	CS22672FB12	PR200	CS42942FB13
PC142	CH4152K9B02		
Block 1.	Stuff		

PL9 0.24uH_7X7X4
PR84、PR93 *22.6K/F_4
PR92、PR95 *0_4
PC143、PC145 *0.1u/25V_4

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	+VCCIN(TPS51624)		2A
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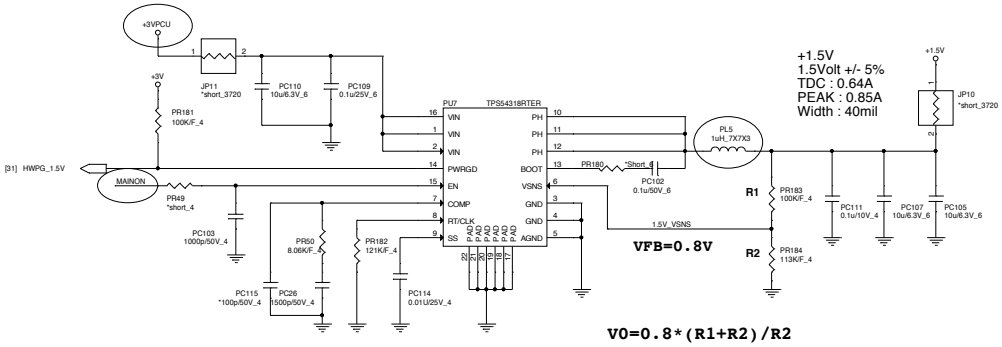
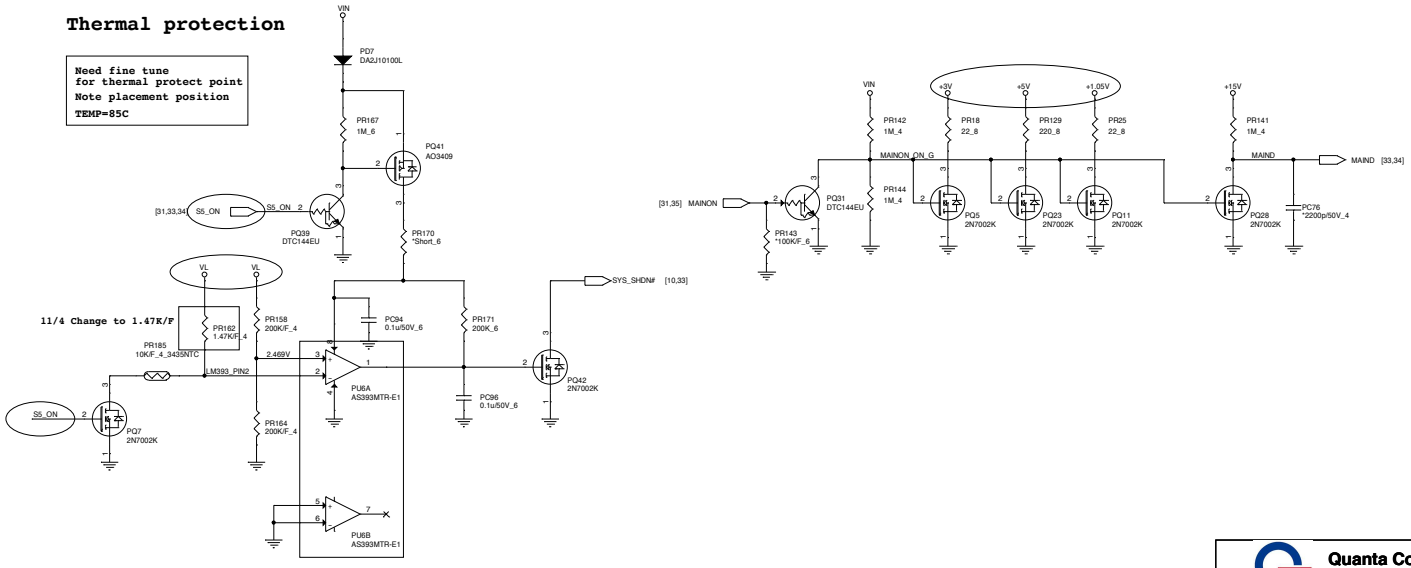


V0=0.8*(R1+R2)/R2

Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=85C



For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	+1.5V/Thermal Protect	2A
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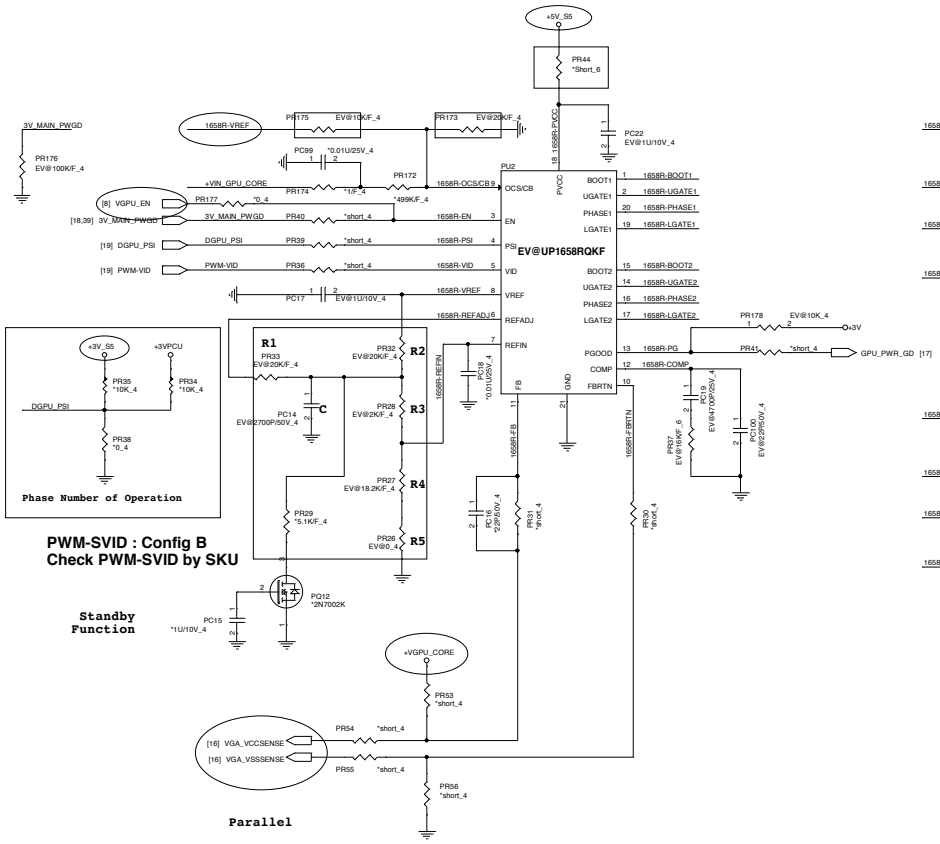

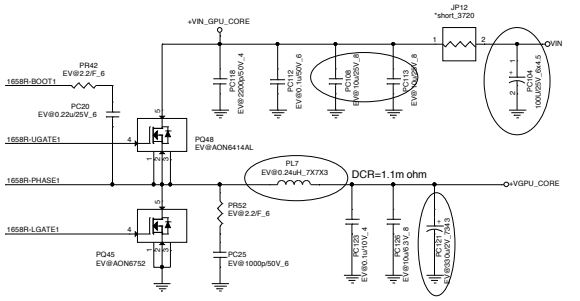

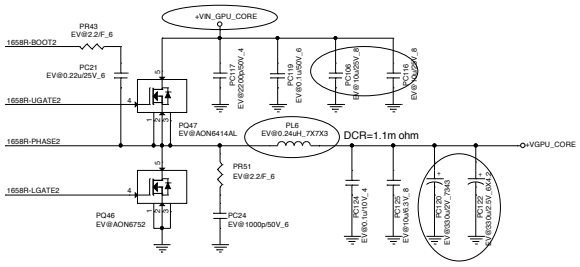

N16S-GT(23W)

+VGPU_CORE
Countinue current:26A
Peak current:51A
OCP:A
FSW:300KHz
L/L=0mV/A

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PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	2A
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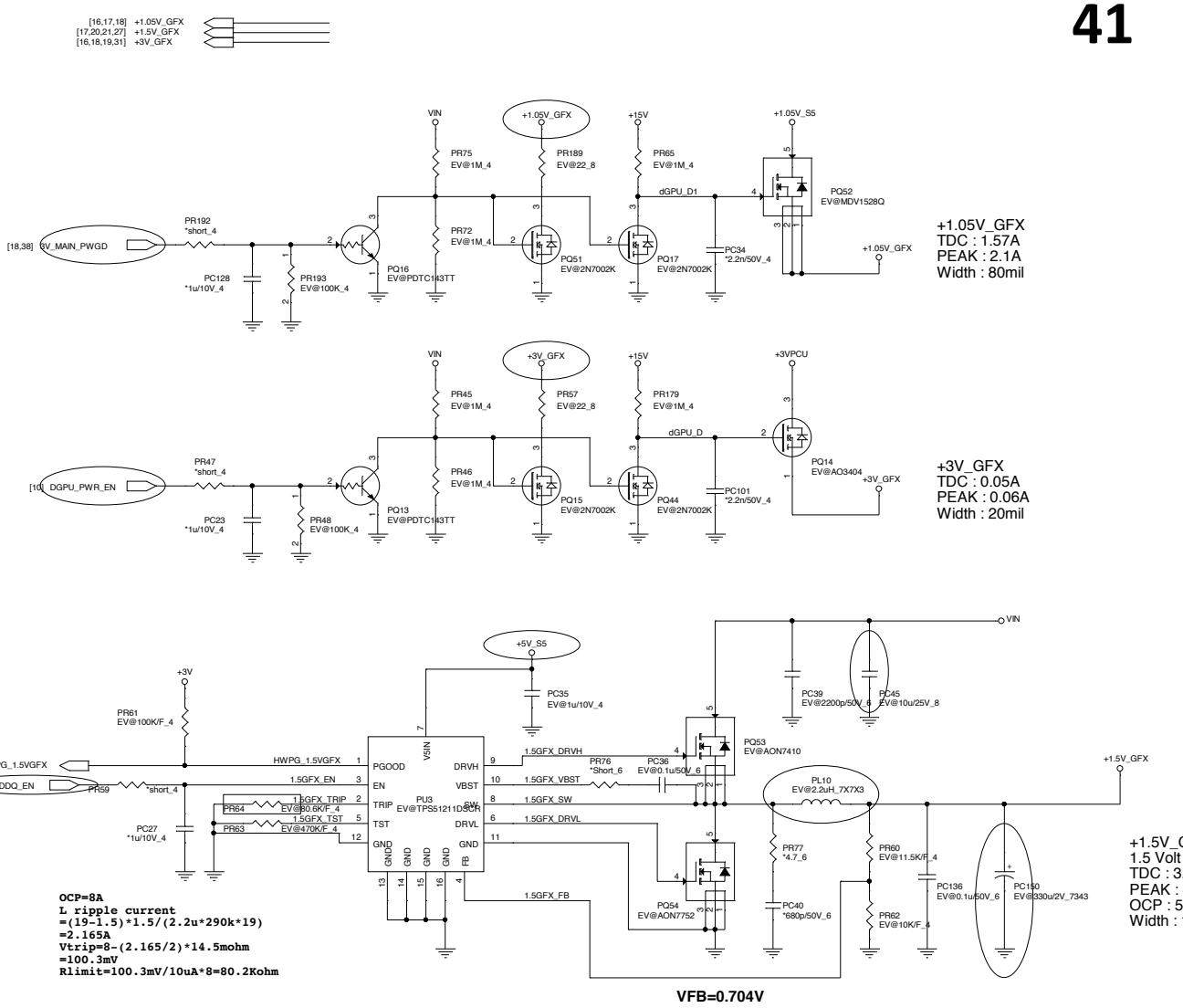

Quanta Computer Inc.			
PROJECT : ZRT/ZRTA			
Size	Document Number		Rev
	+1.5V_GFX/+1.05V_GFX/+3V_GFX		2A
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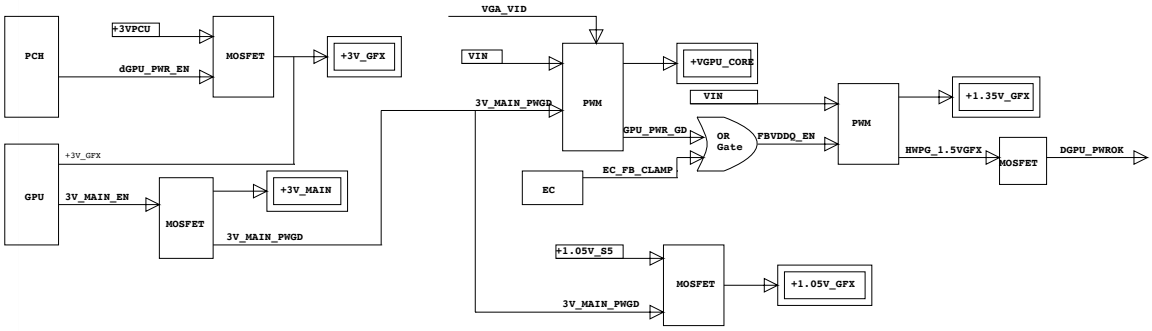
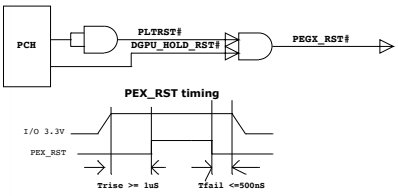
VGA power up sequence



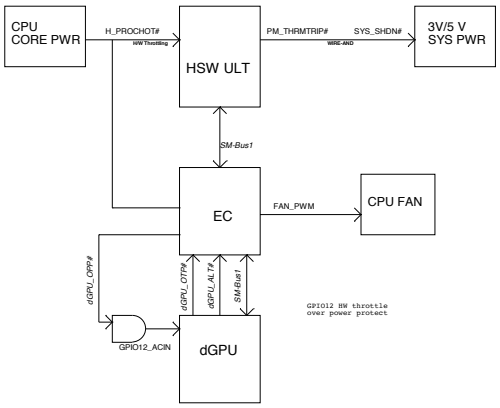
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+3V_GFX	variation	External GPU POWER	DGPU_PWR_EN	S0
+1.05V_GFX	+3.3V	External GPU POWER	3V_MAIN_EN	S0
+VGPU_CORE	+1.35V	External GPU POWER	3V_MAIN_EN	S0
+1.35V_GFX	+1.05V	External GPU POWER	FBVDDQ_EN	S0

Thermal Follow Chart



dGPU_OPP# EC notify HW throttle over power protect
dGPU_OTP# VGA thrMtrip# => inform EC over temperature protect

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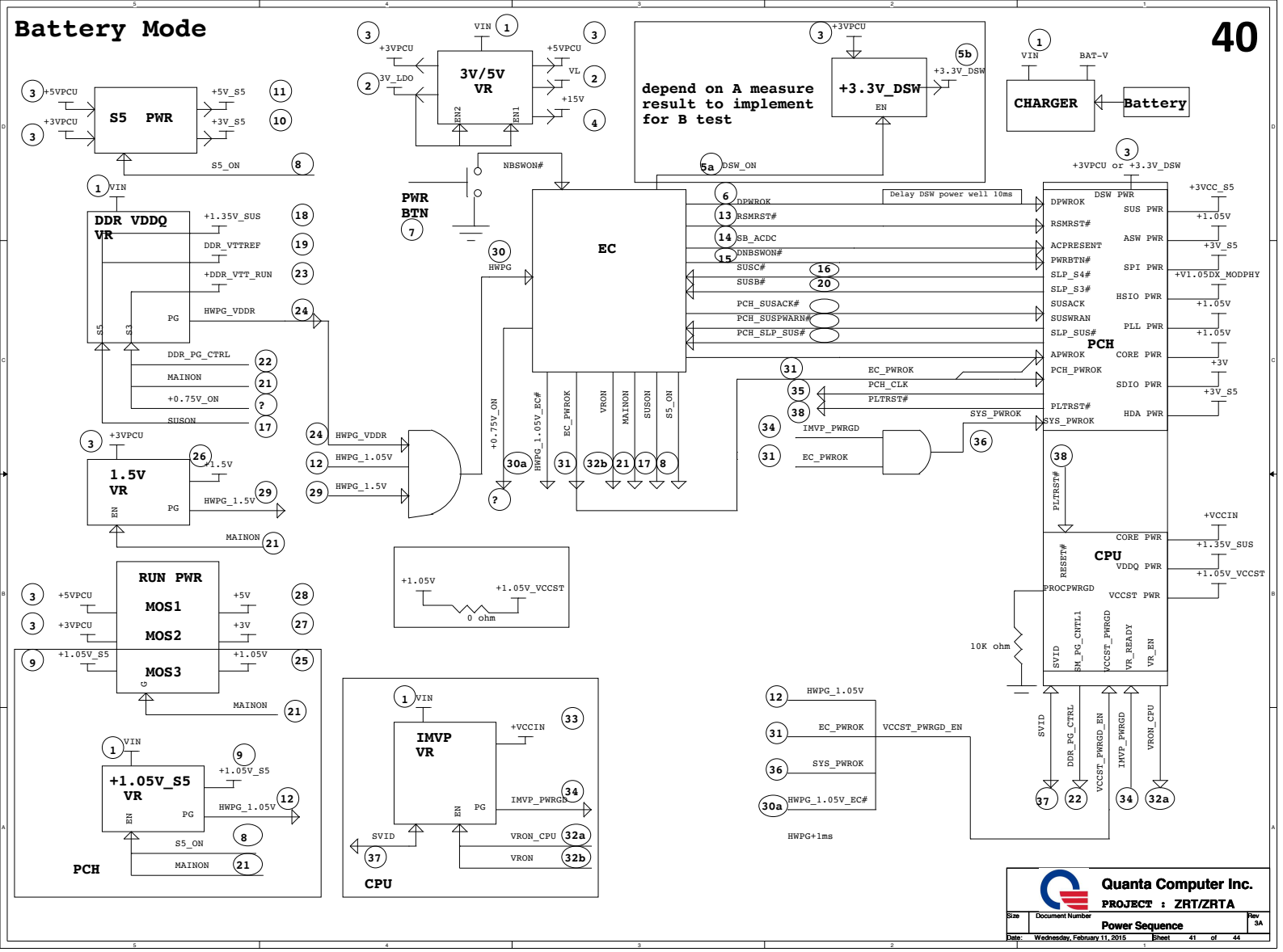
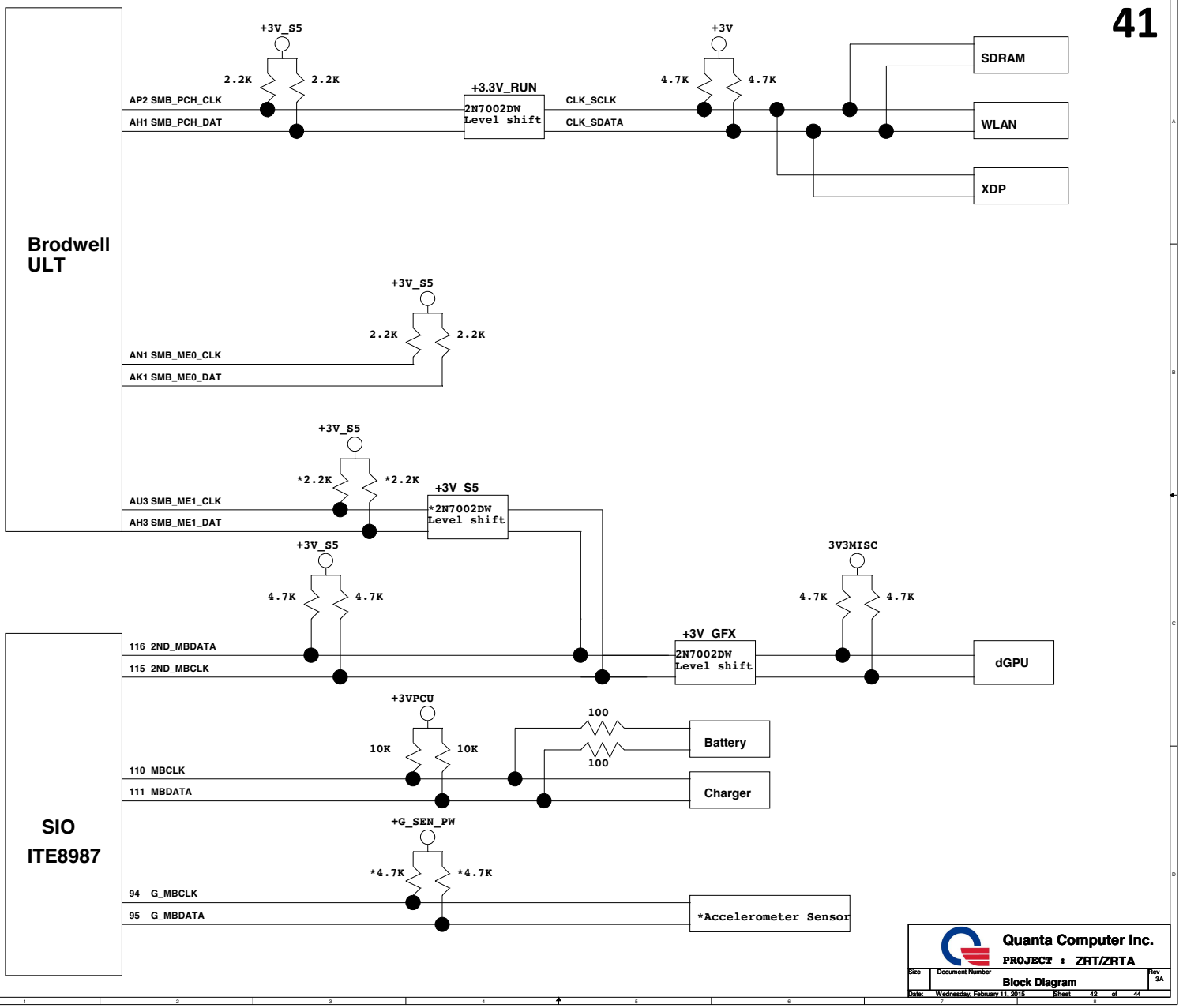
Battery Mode





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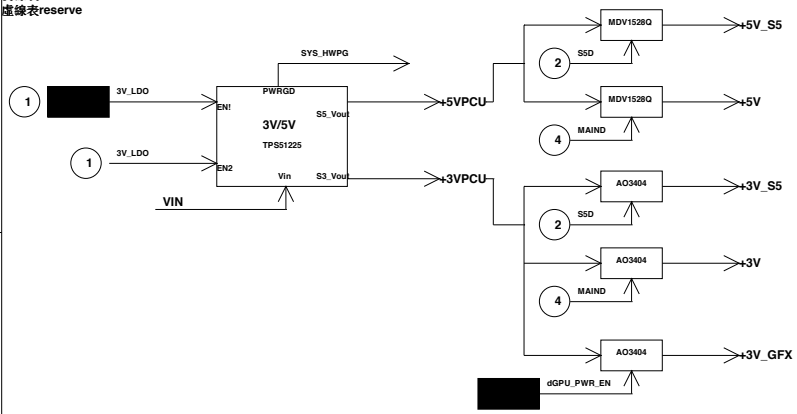
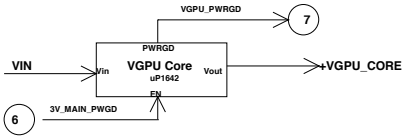
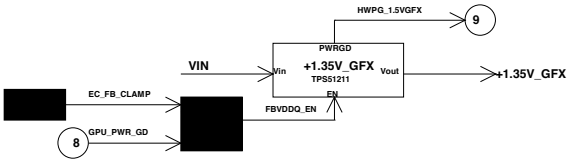
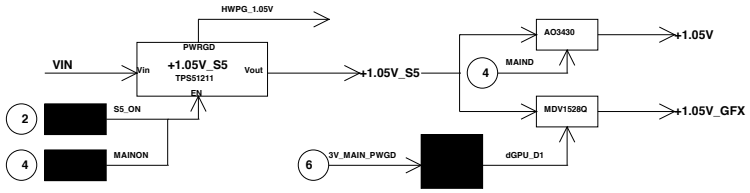
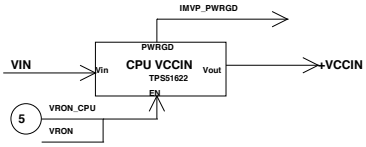
實線表defult
虛線表reserve

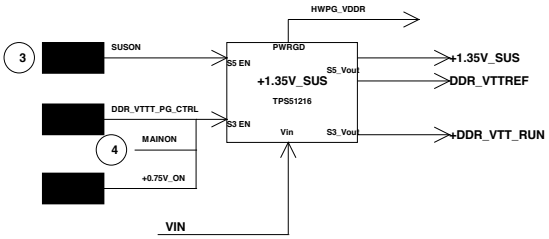


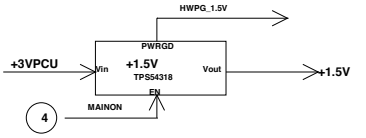












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ULT PWR CONTROL
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Model	Version		CHANGE LIST
ZQ0	1A-1	1	2013/10/15 change pin define and add pwm IC.(page31)
		2	2013/10/15 Change VGA ITE solution to NXP.(page 23)
		3	2013/10/15 power board CN change to 6pin.(Page 23)
		4	2013/10/15 U5017.12 change 27M crystal to VGA IC.(Page 23)
		5	2013/10/15 U5017.14 add power rail +3V_RTC(page23)
		6	2013/10/15 strap0 R672 DG 50k PU.(Page 19)
		7	2013/10/15 Change AND gat to Q63 D-MOS.(Page 19)
		8	2013/10/15 change pin define and add pwm IC U17.(Page 46)
		9	2013/10/15 for GC6 stuff R228\R1013\R226\R1012.un-stuff Q24\Q26\R227\R1011. (Page19)
		10	20131015 For GC6 NV DG GC6_FB_EN PD.(Page10)
		11	2013/10/15 following up acer define and swap USB3 and USB2 port.(Page9)
		12	2013/10/15 swap CAP C8579/C8580 to Vrefo and resistor R5214/R5215 to Line in.(Page30)
		13	2013/10/15 U27.30/U27.31 del fan Pwm signal.(Page32)
		14	20131015 change LVDS\USB3\RJ45\FAN\TPD\USB DB CN\DC-IN CN\Power Button\Cardreader\KB BLK CN\Power board, footprint.
	1A-2	1	2013/10/16 JDIM5 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.(page15)
		2	2013/10/16 JDIM6 Chage net name M_B_DQS#[7:0] to M_A_DQS#[7:0].(page14)
		3	2013/10/16 Add RTC charge circuit.(page8)
		4	2013/10/16 BT1.1 Chage +3V_RTC_0 to VCCTC_2.(page8)
		5	2013/10/15 change power rail from +3V_RTC_0 to VCCRTC_2.(page23)

DOC NO.	PROJECT MODEL :	ZQ0	APPROVED BY:		DATE:	Quanta Computer Inc. PROJECT : ZRT/ZRTA
	PART NUMBER:		DRAWING BY:		REVISON:	Size: Document Number: Rev: 3A; Change list-1; Date: Wednesday, February 11, 2015 Sheet 44 of 44