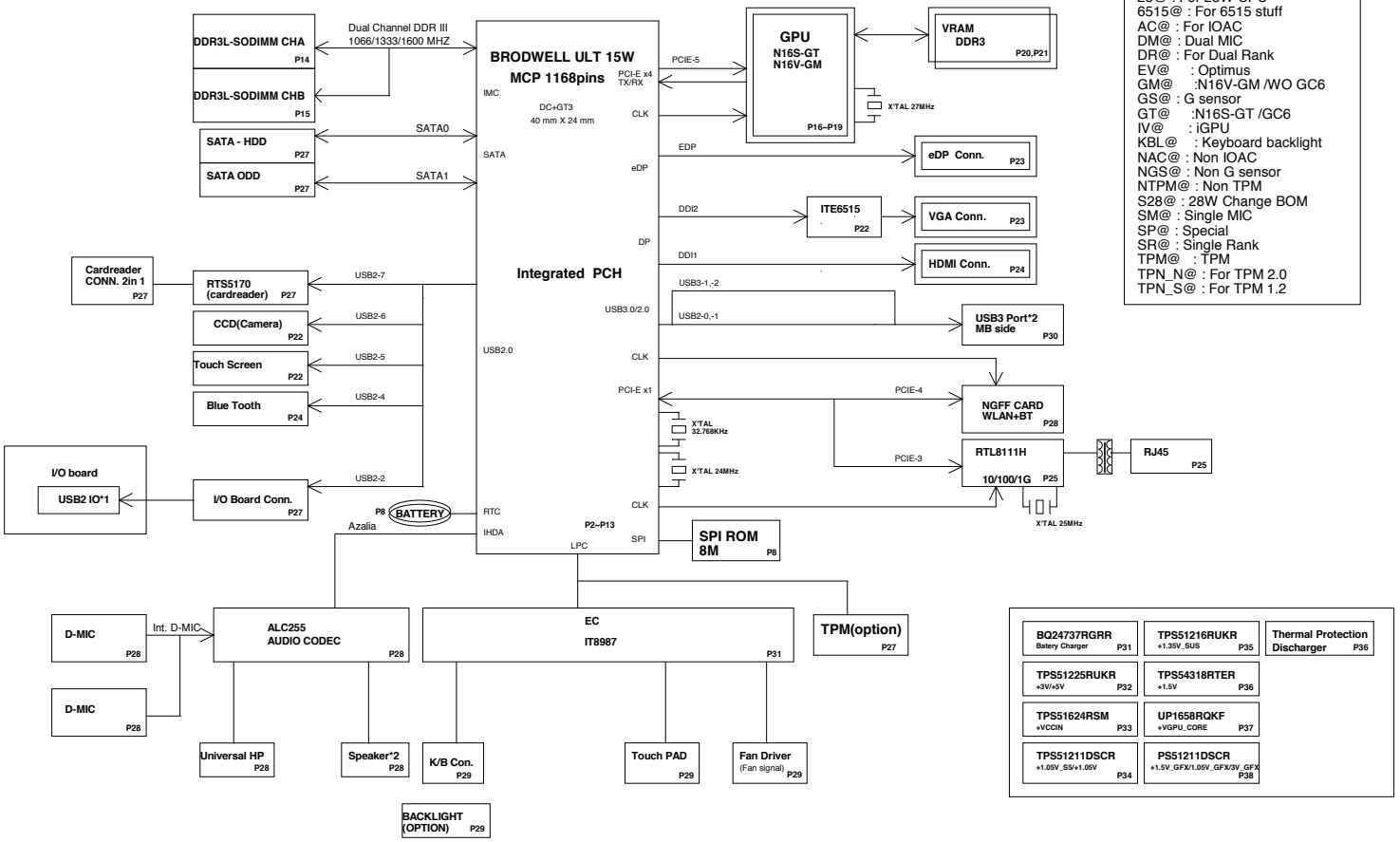
ZRT/ZRTA_GDDR3 BWD ULT SYSTEM BLOCK DIAGRAM

BOM

15@ : For 15W CPU
28@ : For 28W CPU
6515@ : For 6515 stuff
AC@ : For IOAC
DM@ : Dual MIC
DR@ : For Dual Rank
EV@ : Optimus
GM@ :N16V-GM /WO GC6
GS@ : G sensor
GT@ :N16S-GT /GC6
IV@ : iGPU
KBL@ : Keyboard backlight
NAC@ : Non IOAC
NGS@ : Non G sensor
NTPM@ : Non TPM
S28@ : 28W Change BOM
SM@ : Single MIC
SP@ : Special
SR@ : Single Rank
TPM@ : TPM
TPN_N@ : For TPM 2.0
TPN_S@ : For TPM 1.2



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Block Diagram
Size | Document Number | Rev 3A
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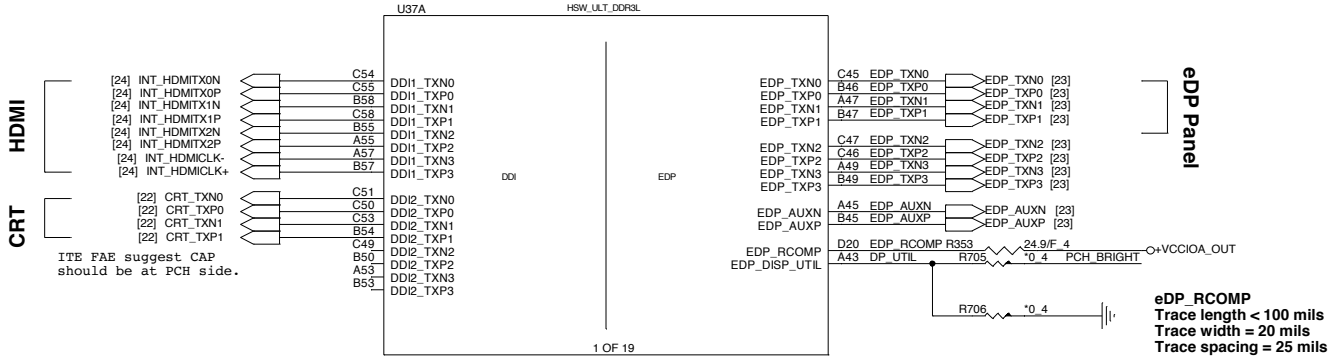
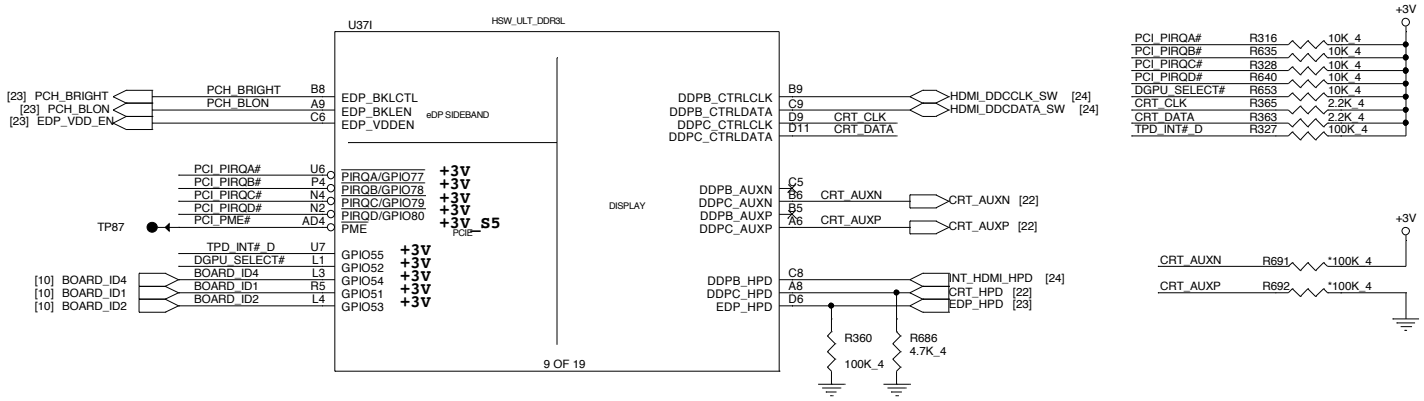
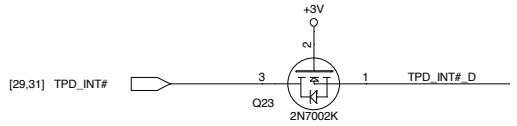
Haswell ULT (DISPLAY,eDP)







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Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	3A
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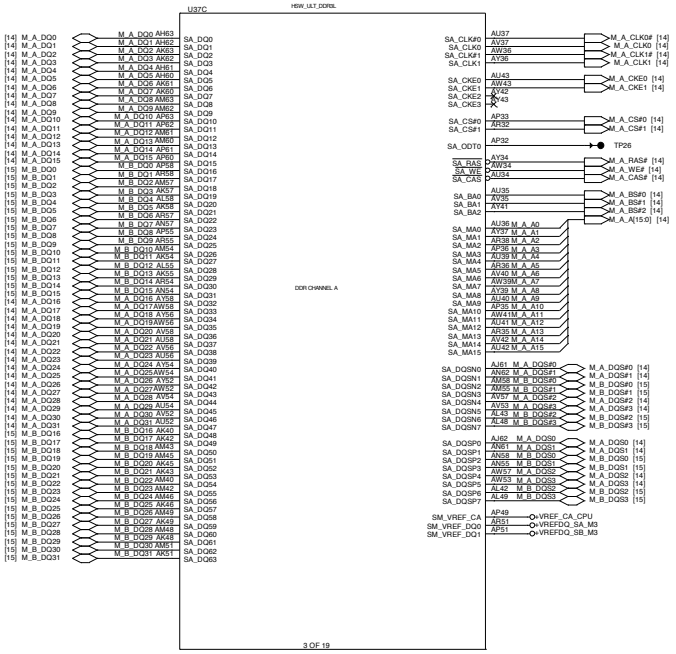
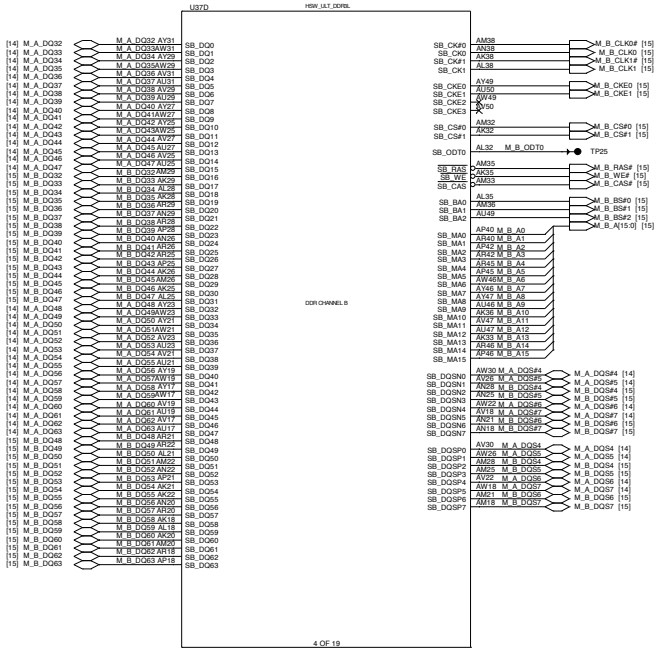
Change Data and DQS to interleave.

Haswell ULT (DDR3L)



Haswell Processor (DDR3)



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PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	Haswell 2/5 (DDR3 I/F)	3A
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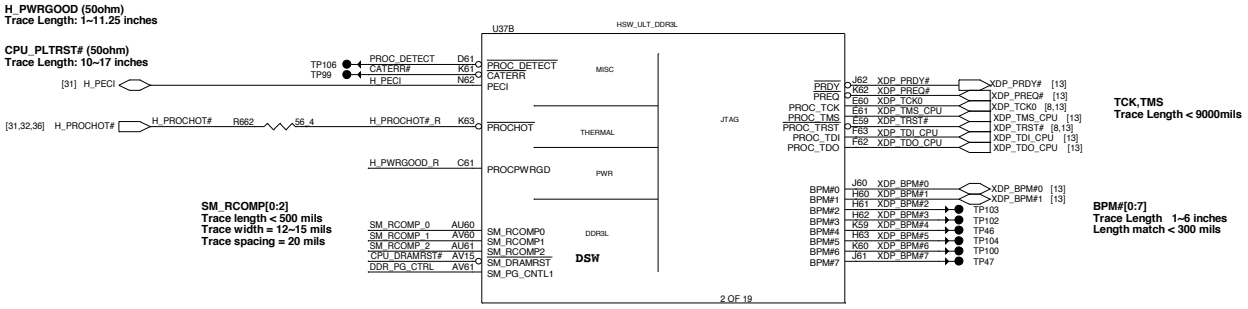
Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

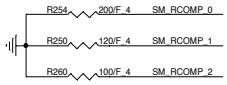


TCK,TMS
Trace Length < 9000mils

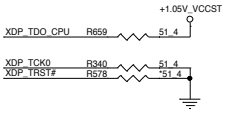
SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

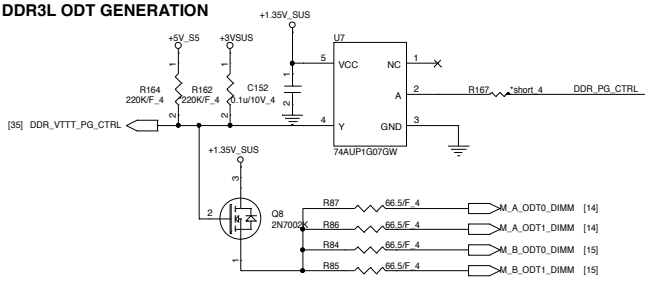
DRAM COMP



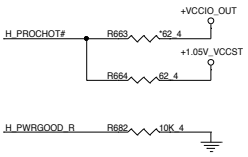
XDP PU/PD



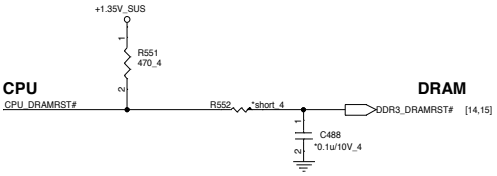
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



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	Haswell 1/5 (PEG/DMI/FDI)	3A
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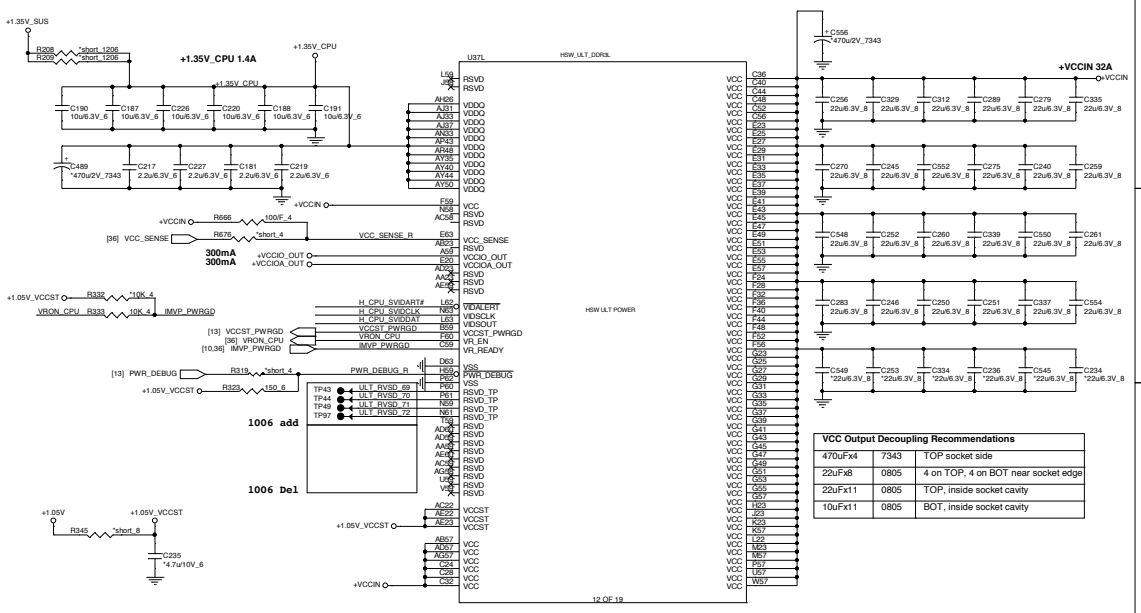
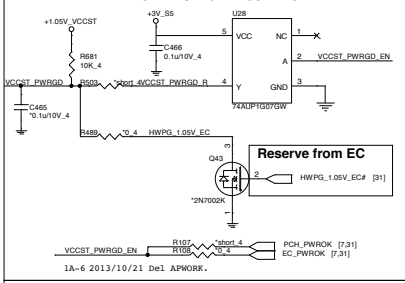
VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

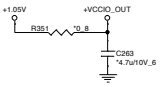
Haswell ULT (POWER)



VCCST PWRGD

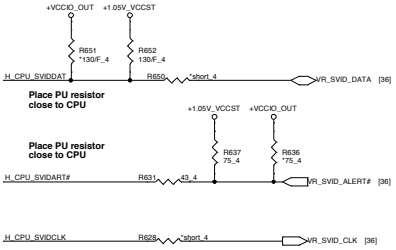
CRB is via +1.05V PG



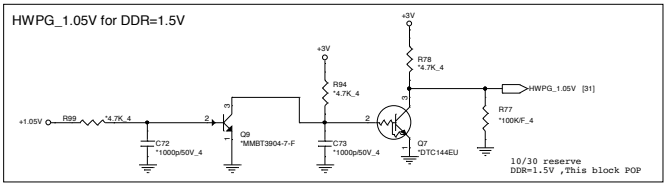


SVID

Layout note: need routing together and ALERT need between CLK and DATA.



HWPG_1.05V for DDR=1.5V



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PROJECT : ZRT/ZRTA			
Size	Document Number		Rev
	Haswell 4/5 (POWER)		3A
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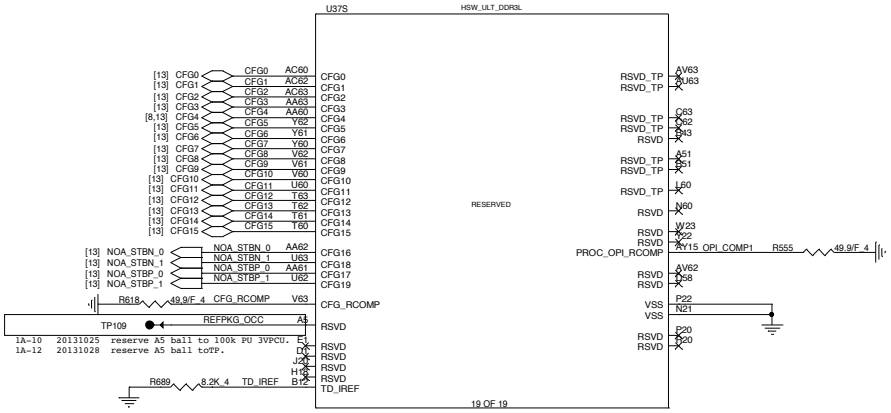
Haswell ULT (CFG,RSVD)



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R289 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R606 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R610 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R614 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R619 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R295 *1K_4

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	Haswell 5/5 (CFG/GND)	3A

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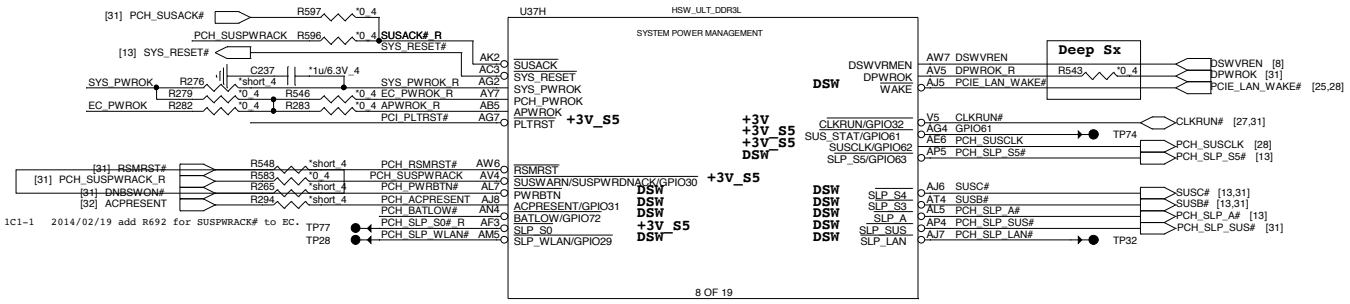
Haswell ULT PCH (PM)



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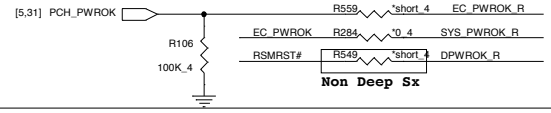
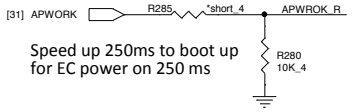
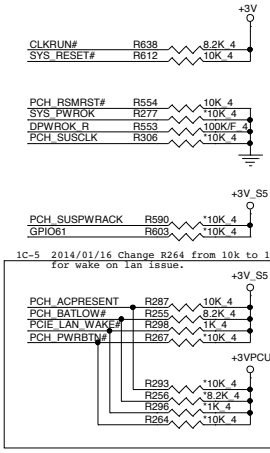
Power Sequence



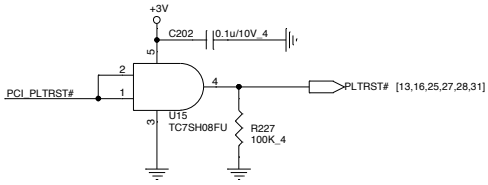


Speed up 250ms to boot up for EC power on 250 ms

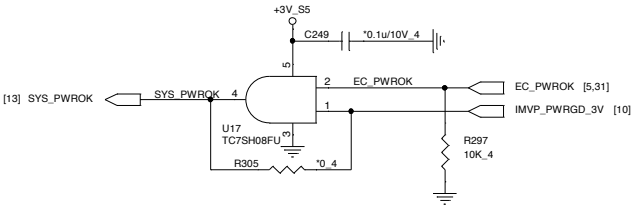
PCH PM PU/PD



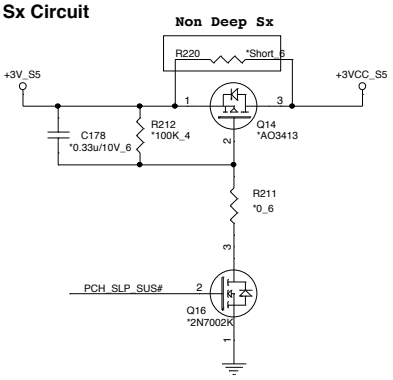
PLTRST# Buffer



SYSPWOK



Deep Sx Circuit



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	LPT 1/6 (DMI/FDI/VGA)	3A
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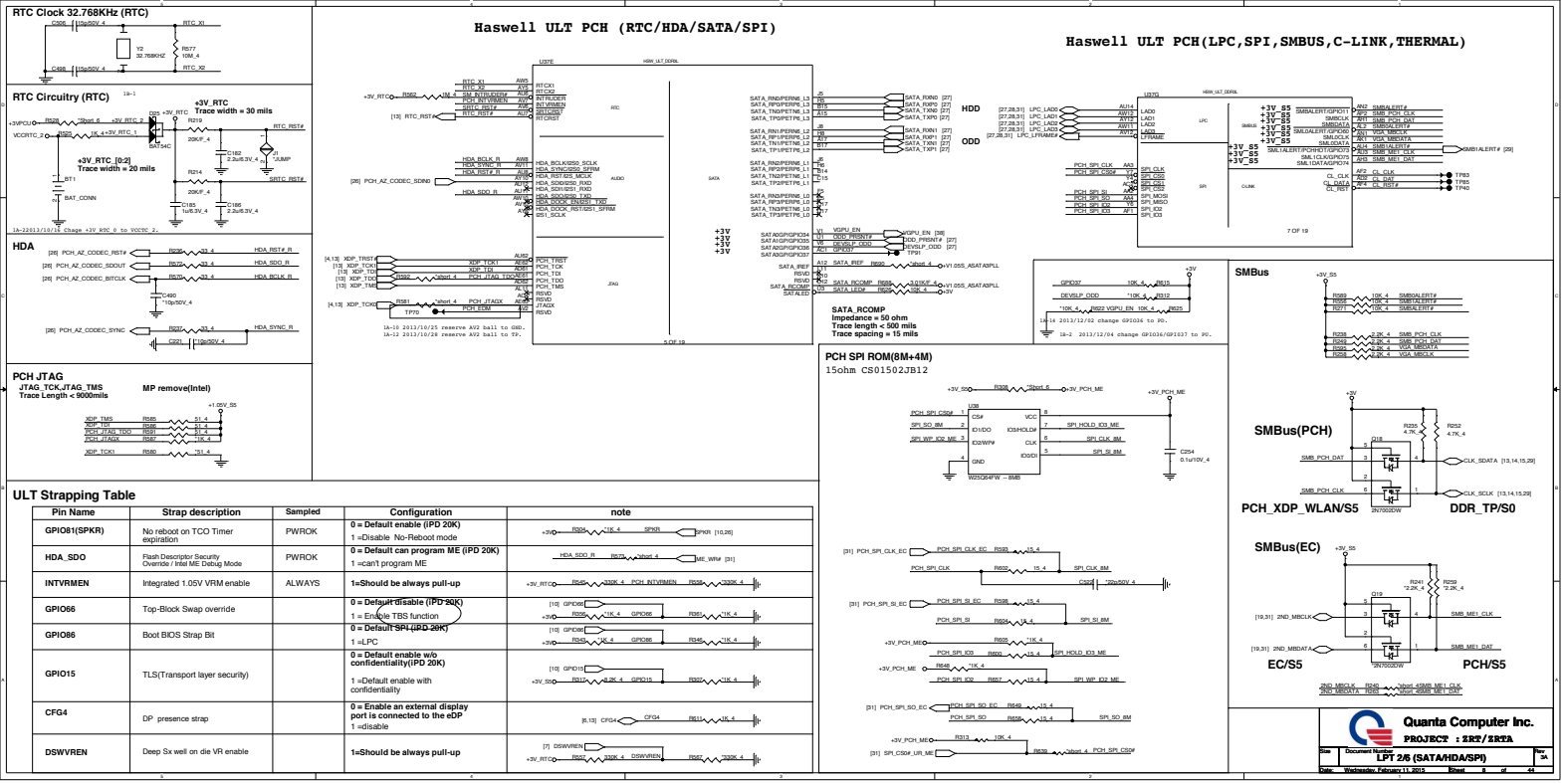

ULT Strapping Table

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	

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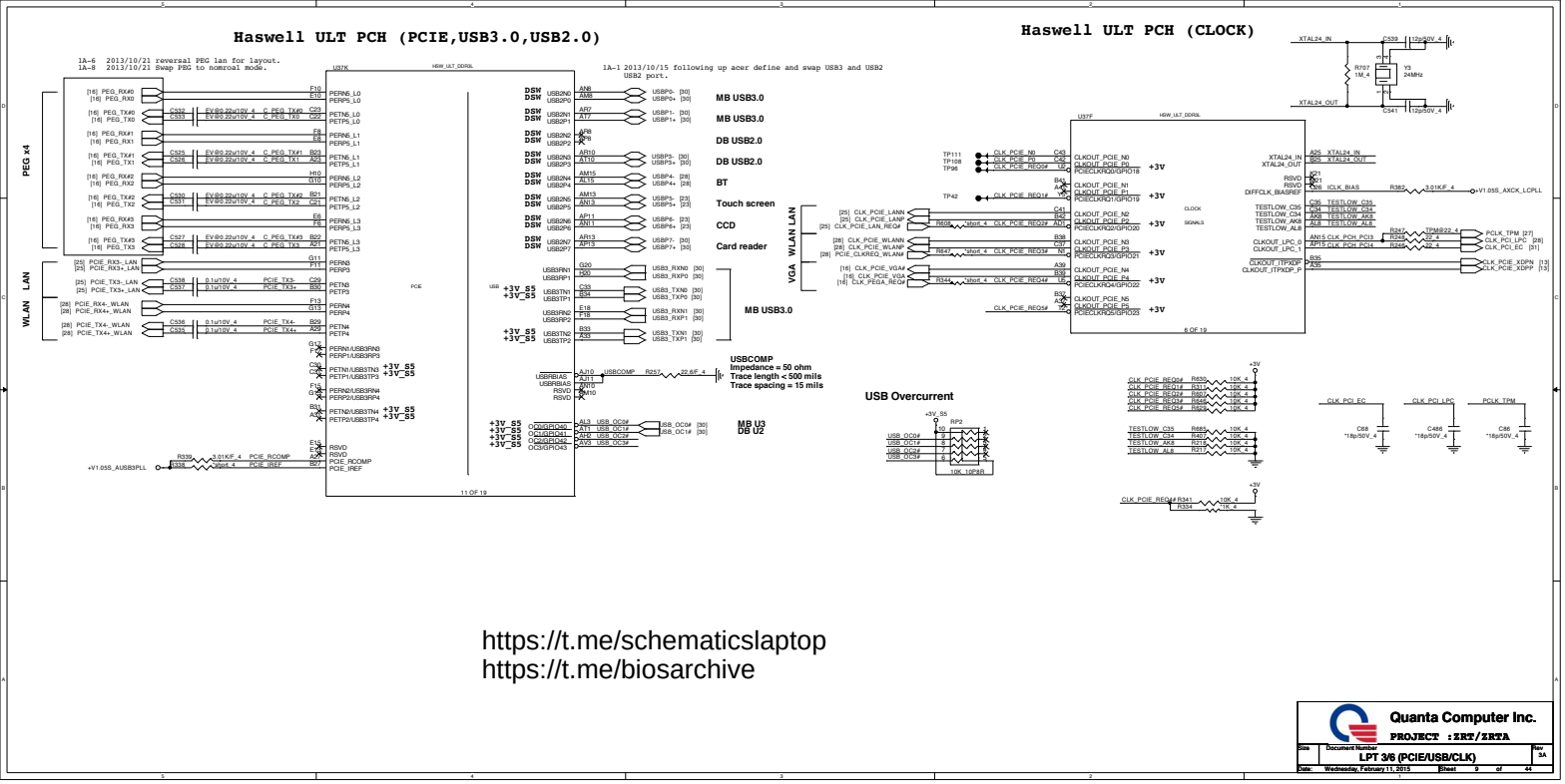

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PROJECT : ZRT/ZRTA			
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	LPT 3/6 (PCIE/USB/CLK)		3A
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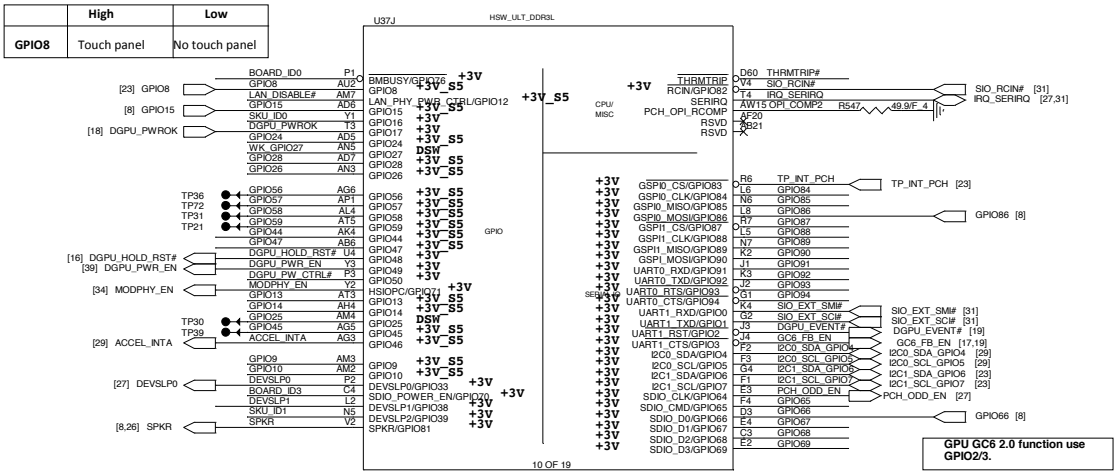
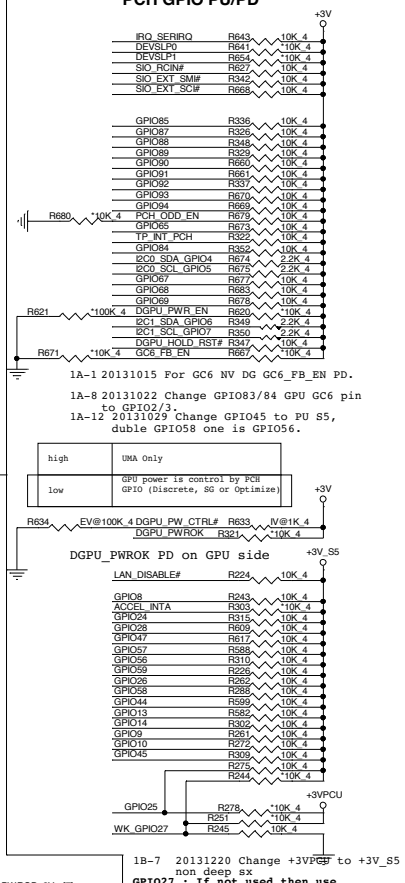
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

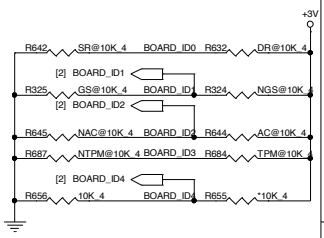
	High	Low
GPIO8	Touch panel	No touch panel



PCH GPIO PU/PD



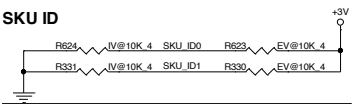
Board ID



	Low	High
BOARD_ID0	single rank SKU	Dual rank SKU
BOARD_ID1	Reserved (Default)	Reserve
BOARD_ID2	No IOAC	IOAC
BOARD_ID3	No TPM	TPM
BOARD_ID4	Non-Dolly (Default)	Dolly

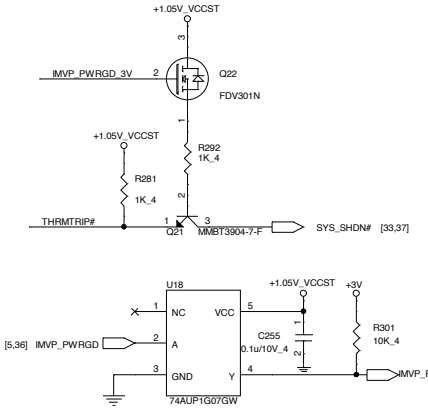
RAM ID

SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip



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Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	3A

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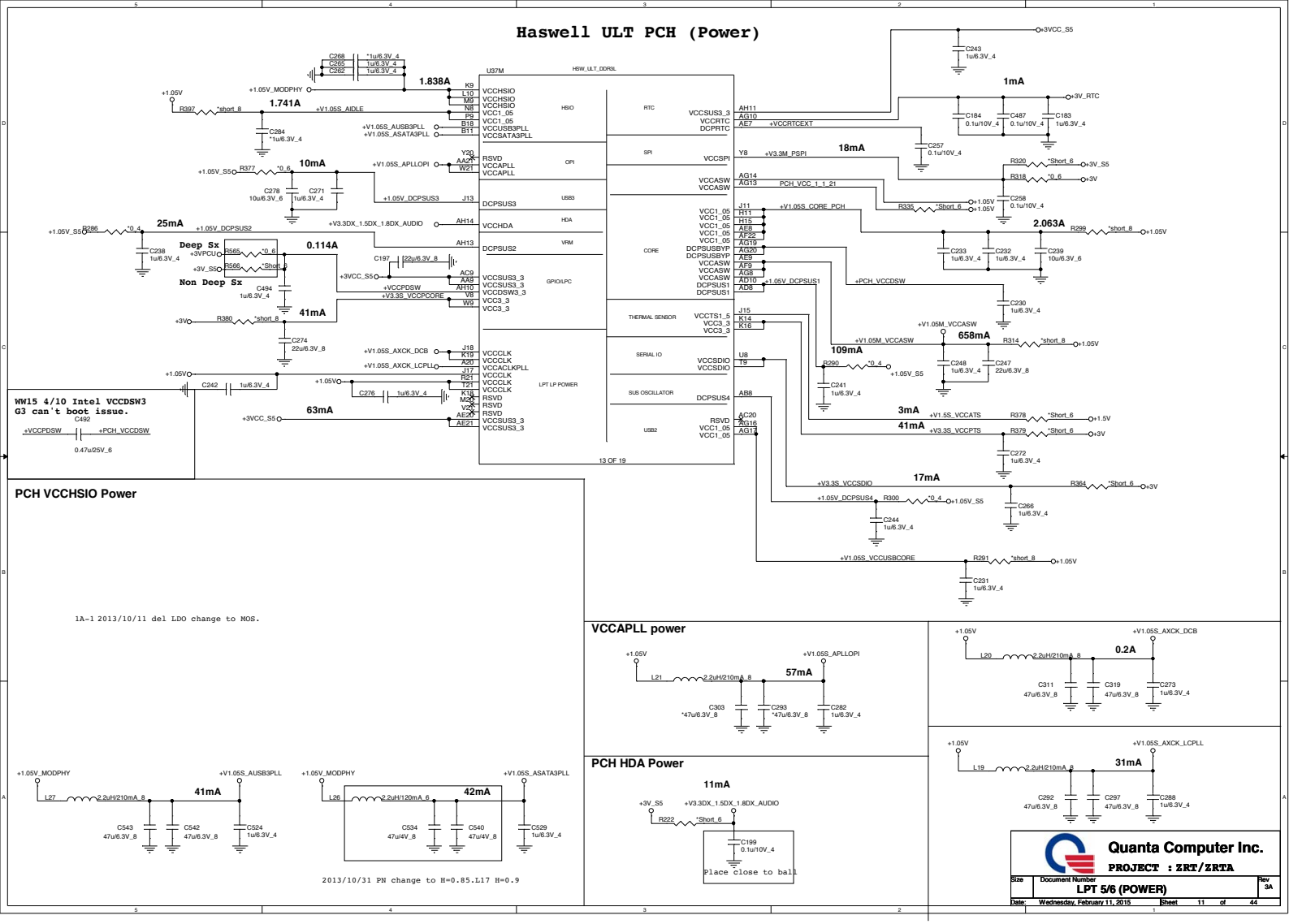

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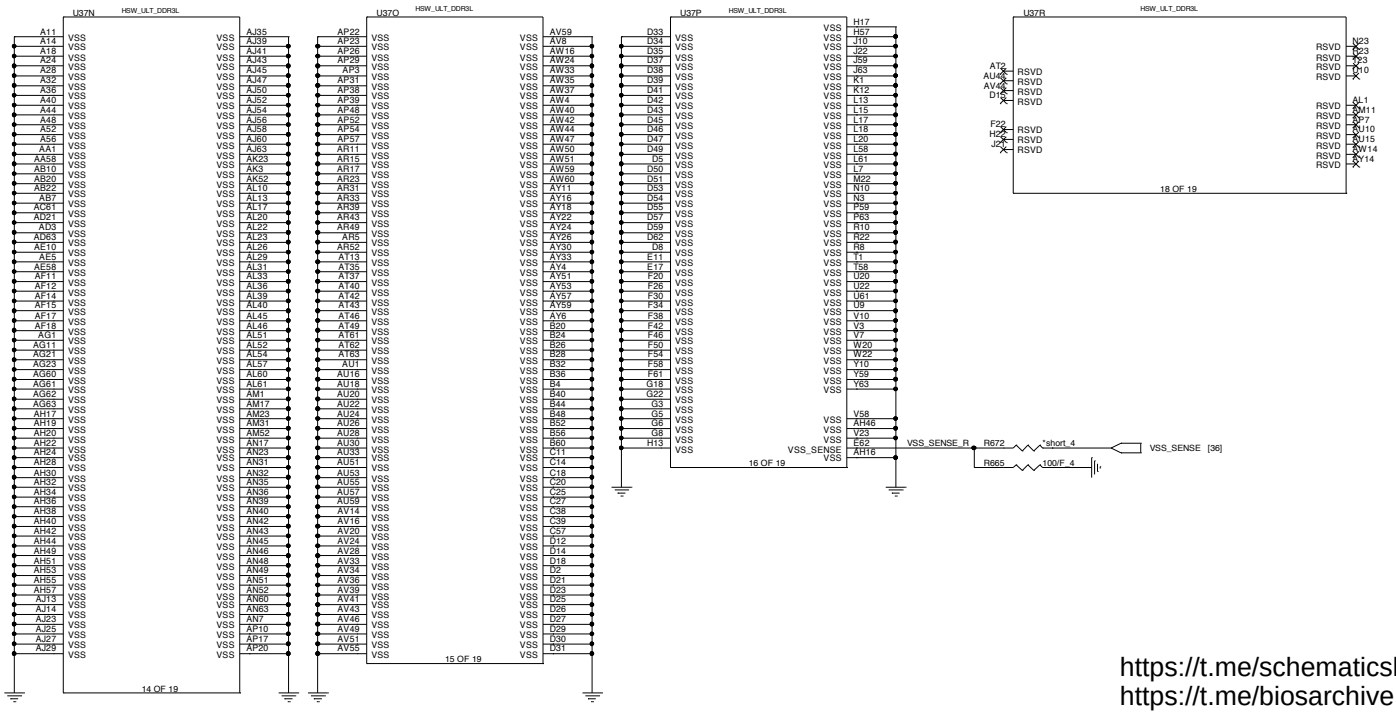
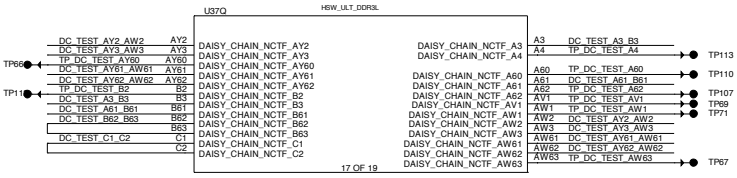
Haswell ULT (GND)





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PROJECT : ZRT/ZRTA		
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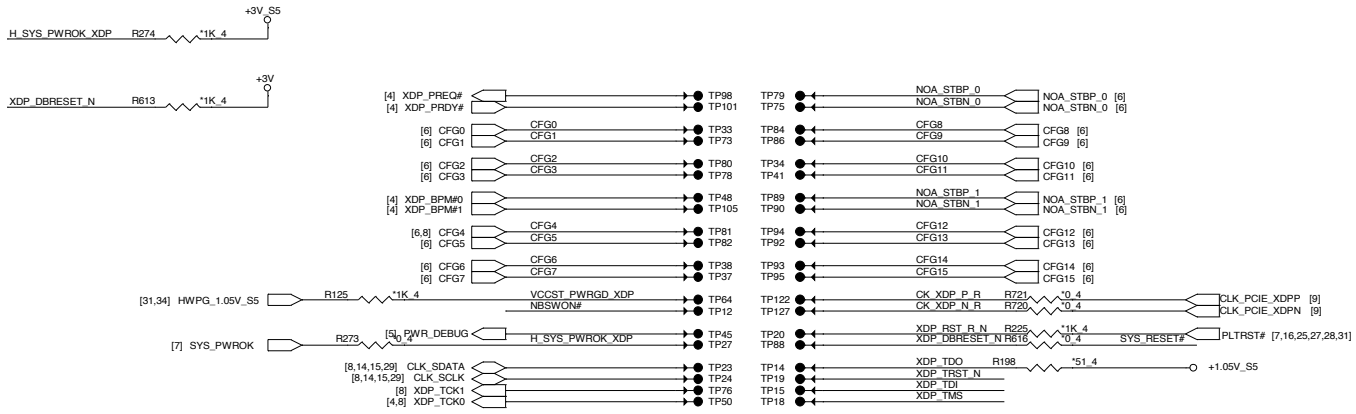

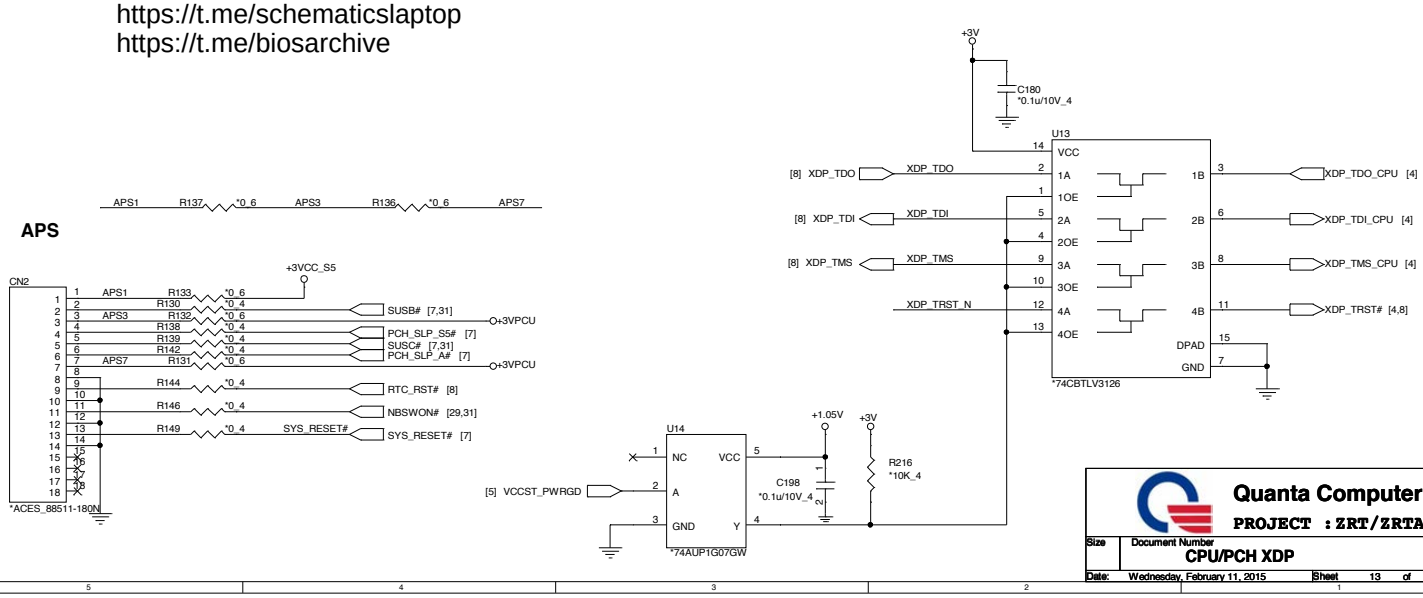

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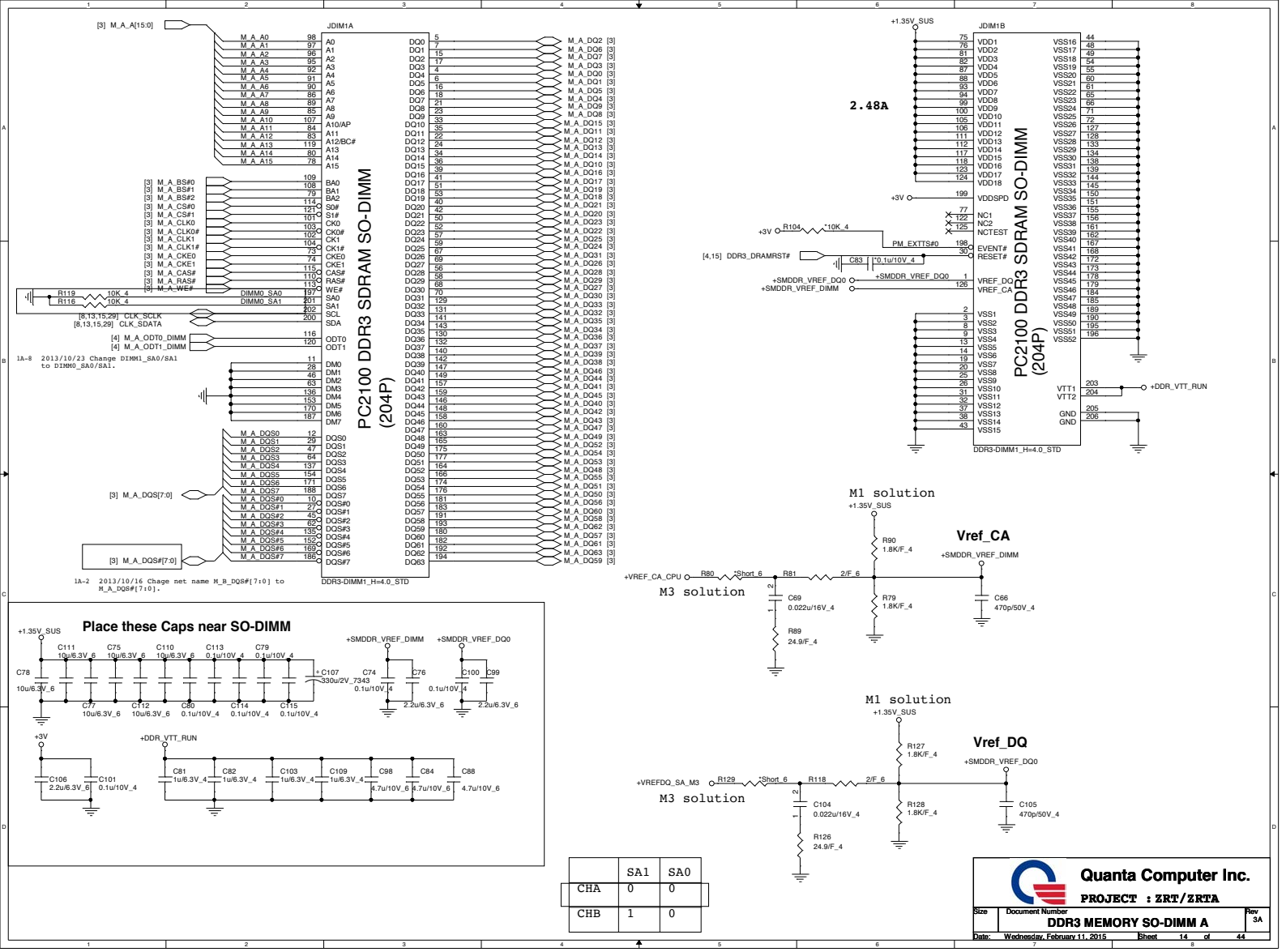

	SA1	SA0
CHA	0	0
CHB	1	0

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Size	Document Number	Rev
	DDR3 MEMORY SO-DIMM A	3A

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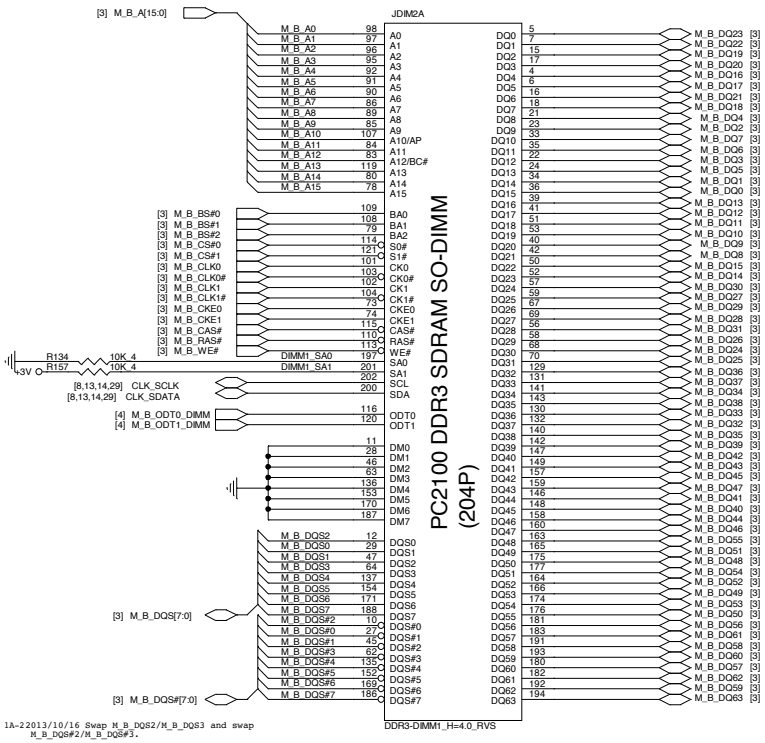

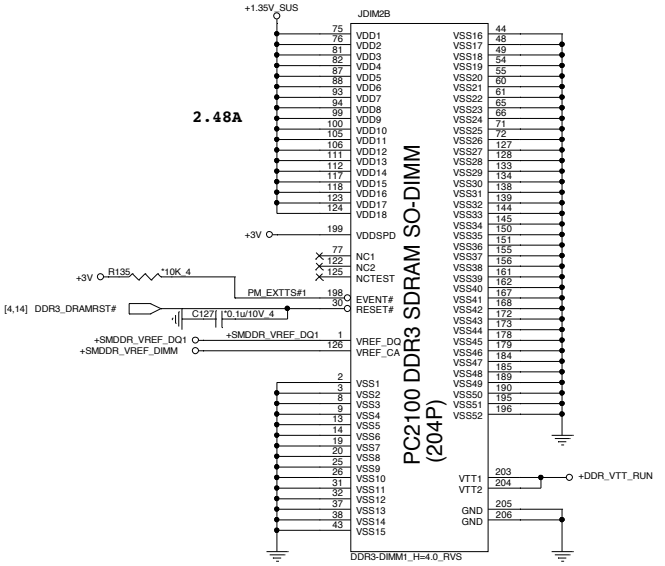

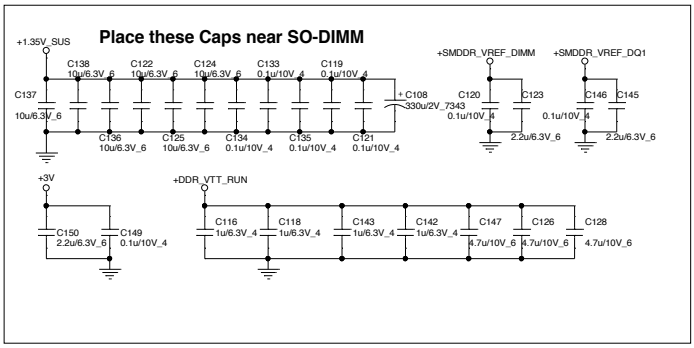

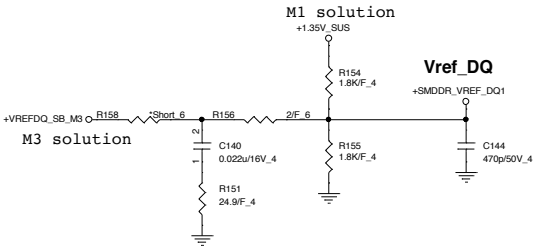

	SA1	SA0
CHA	0	0
CHB	1	0

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PROJECT : ZRT/ZRTA			
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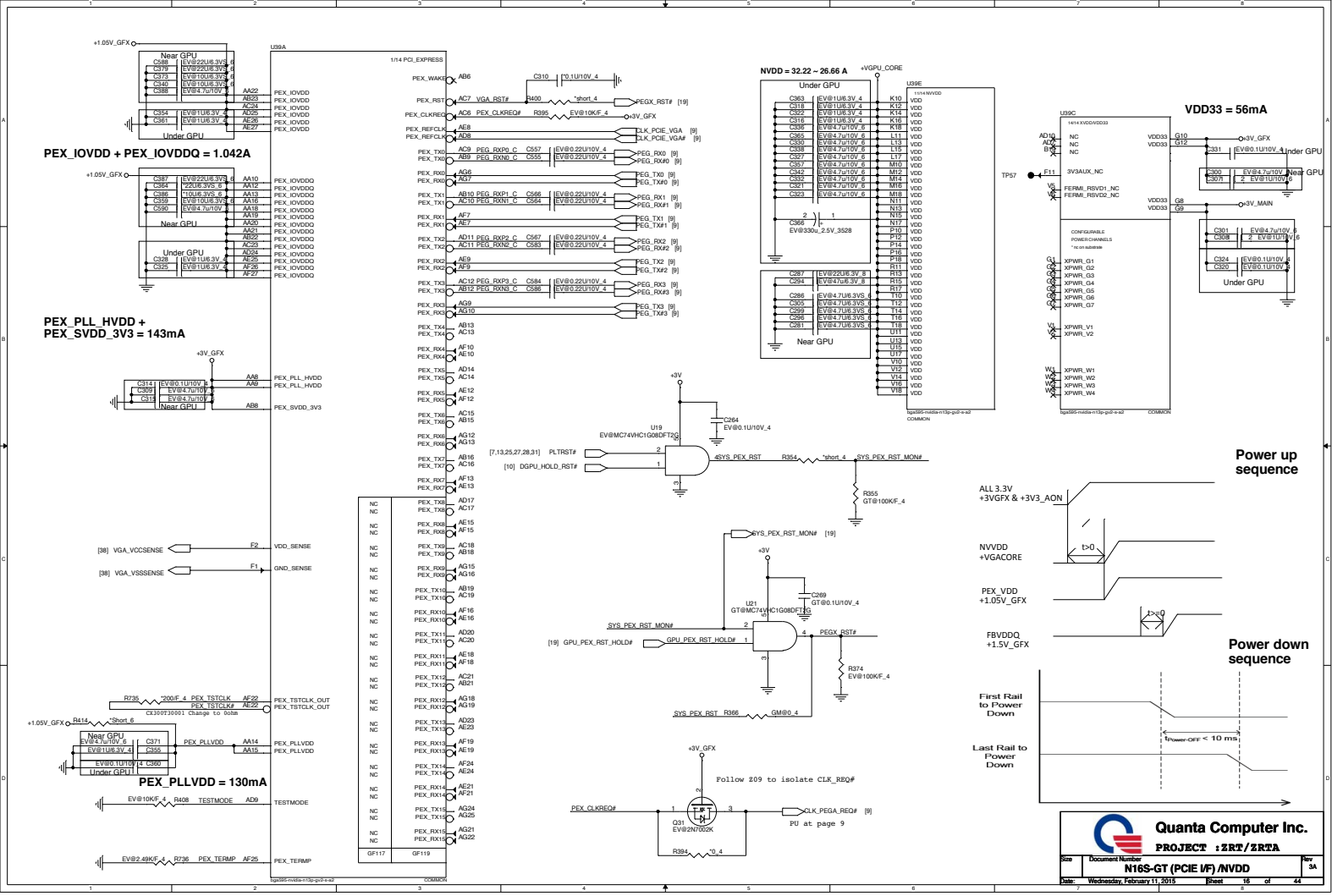

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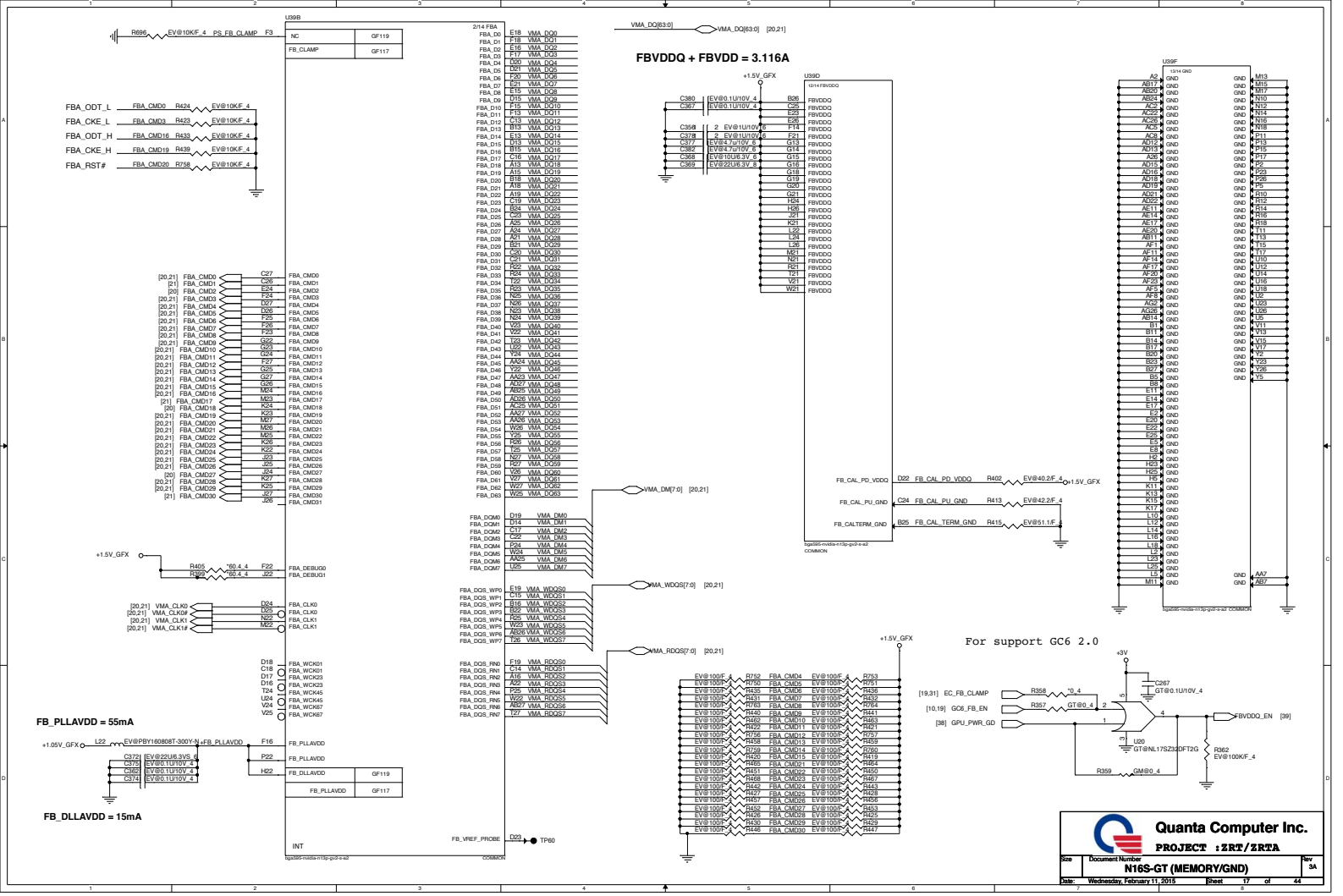
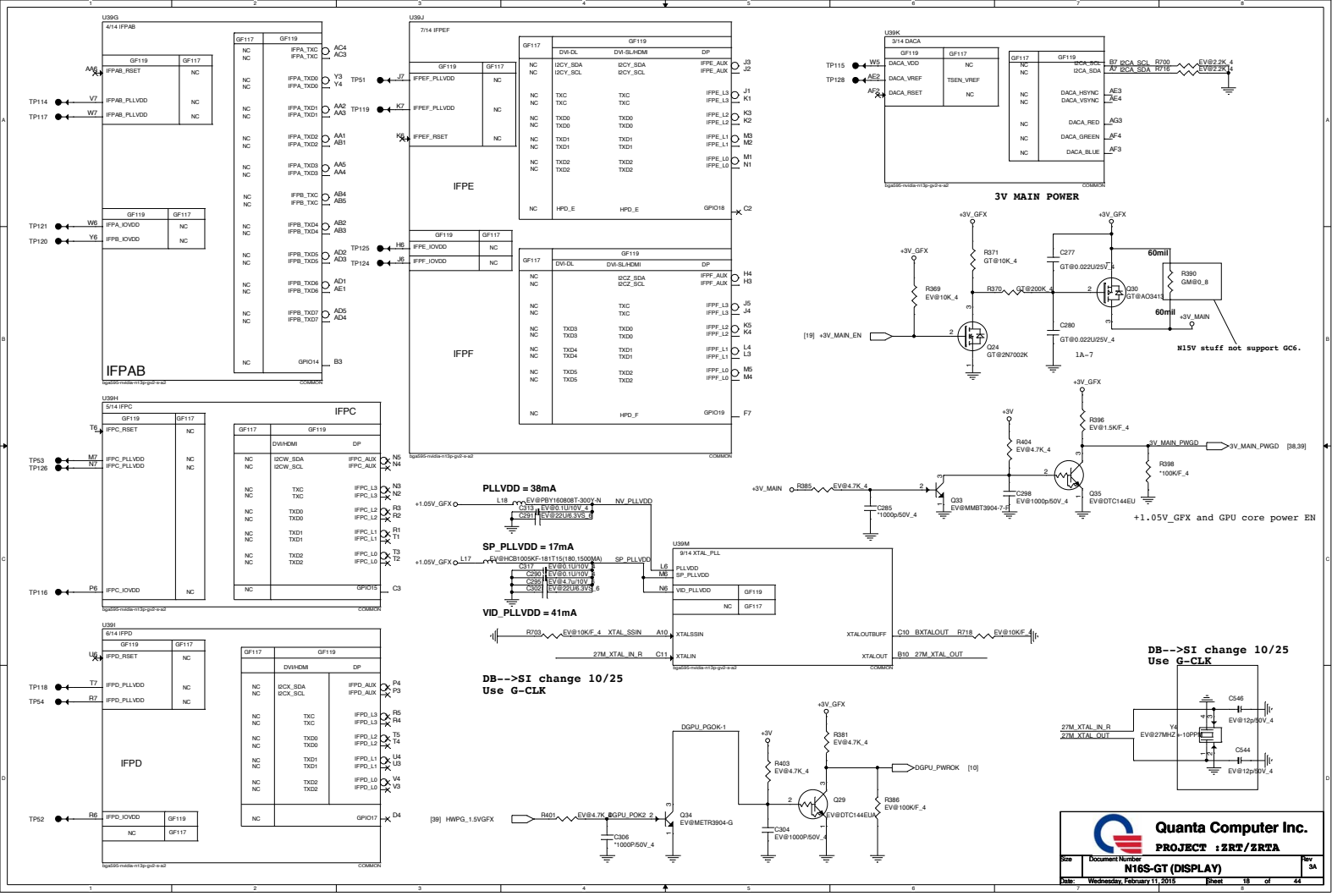


https://t.me/schematicslaptop
https://t.me/biosarchive



https://t.me/schematicslaptop
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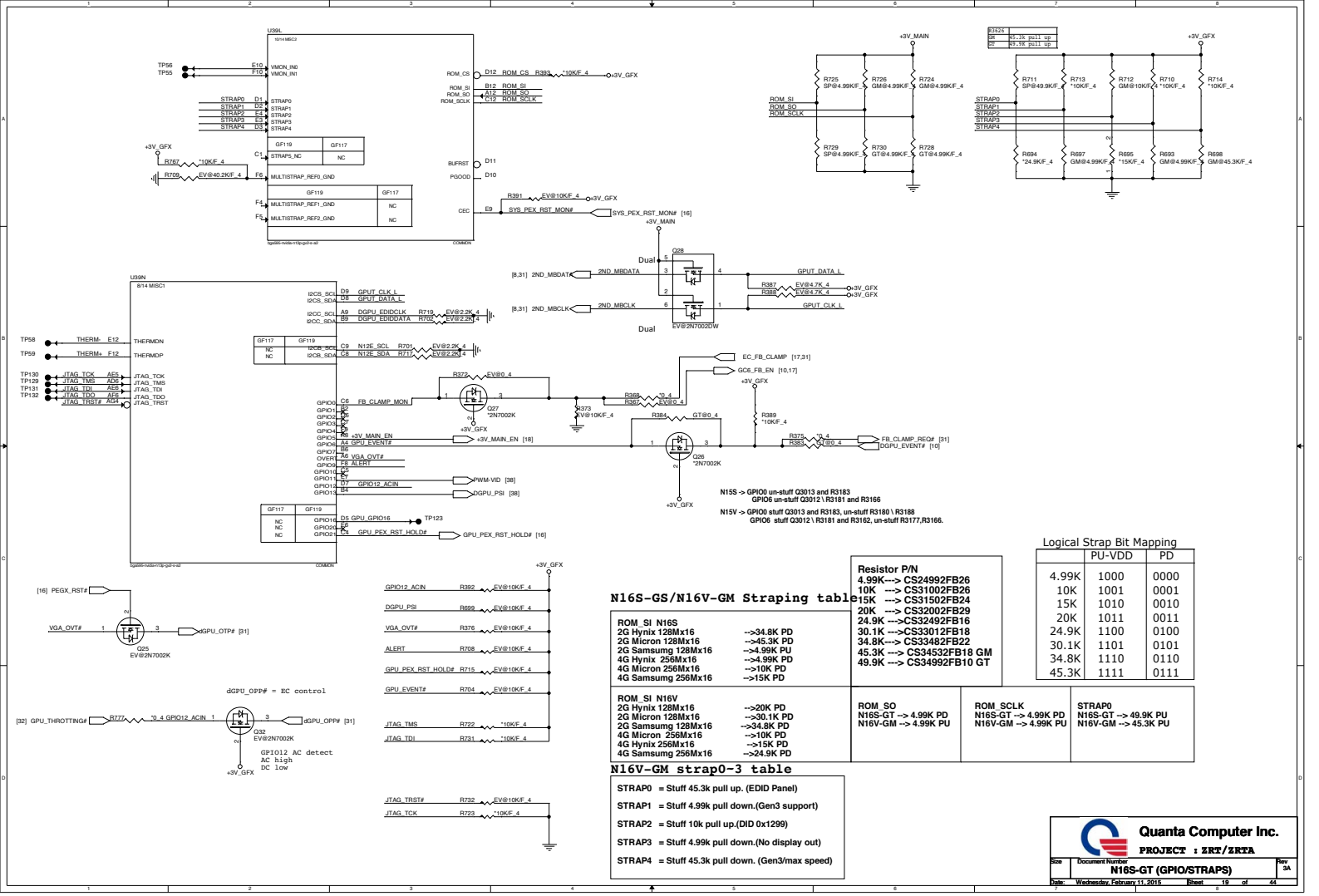
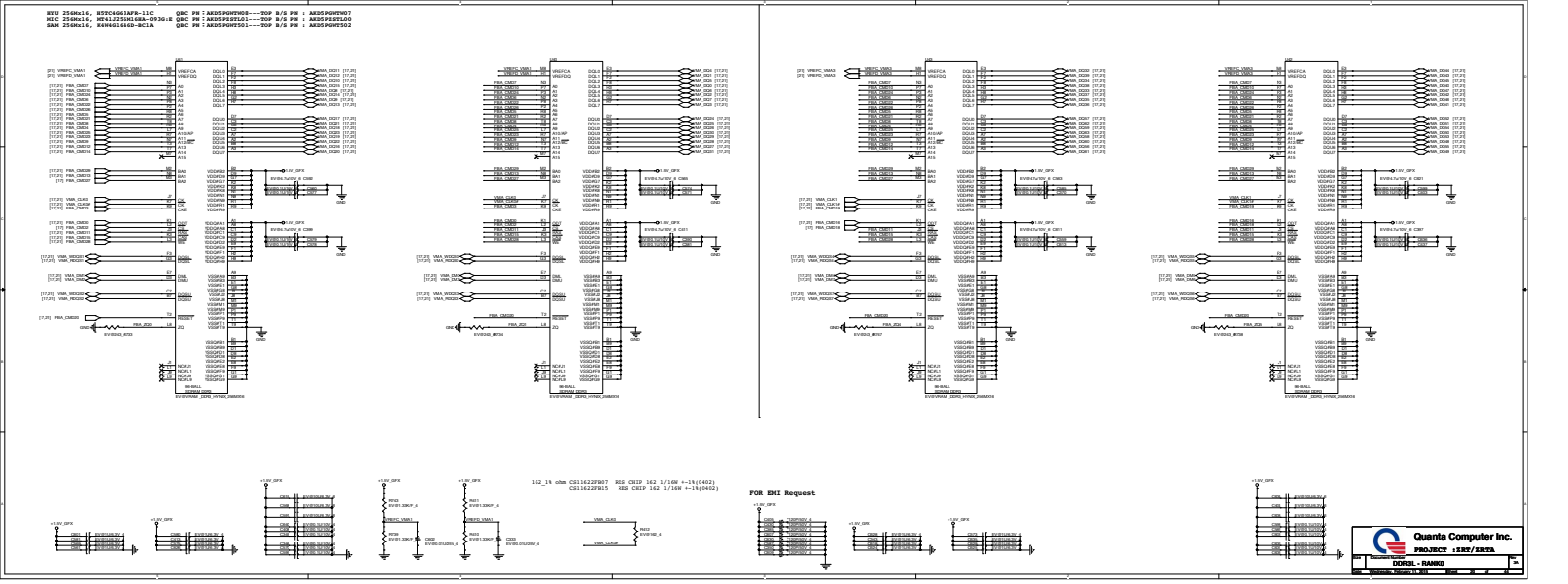
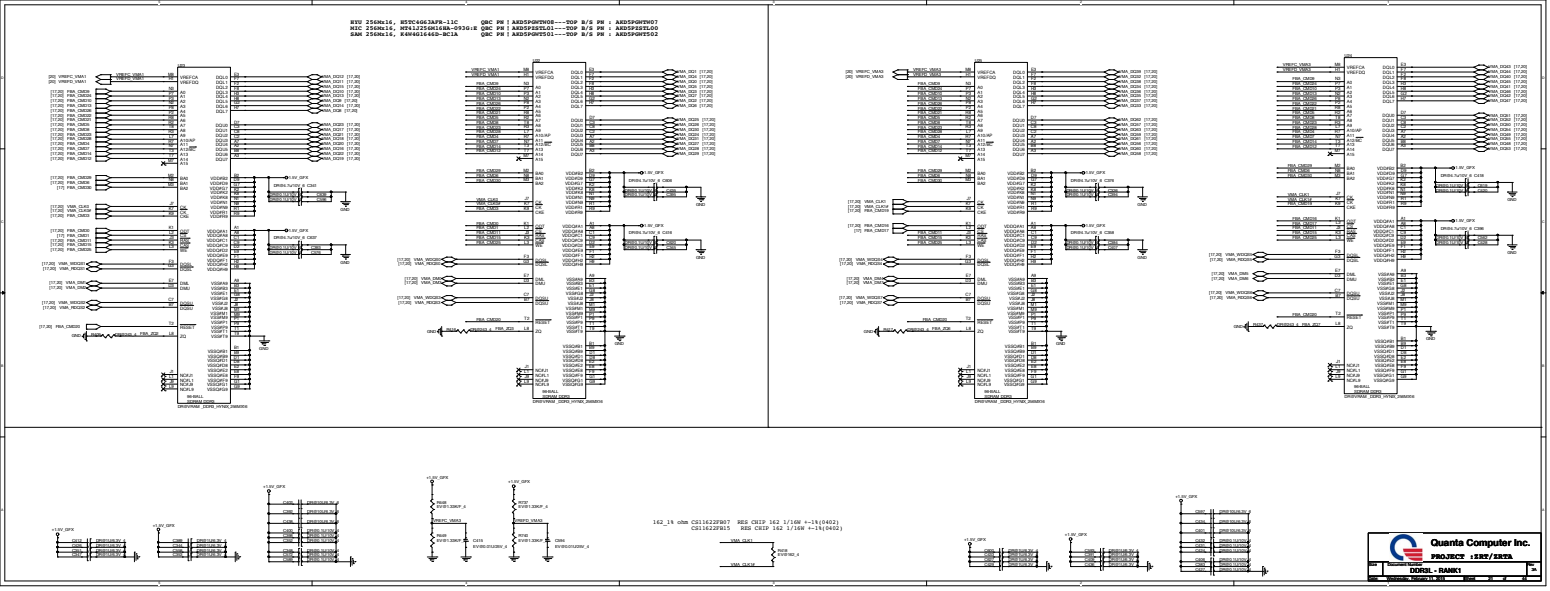


https://t.me/schematicslaptop
https://t.me/biosarchive

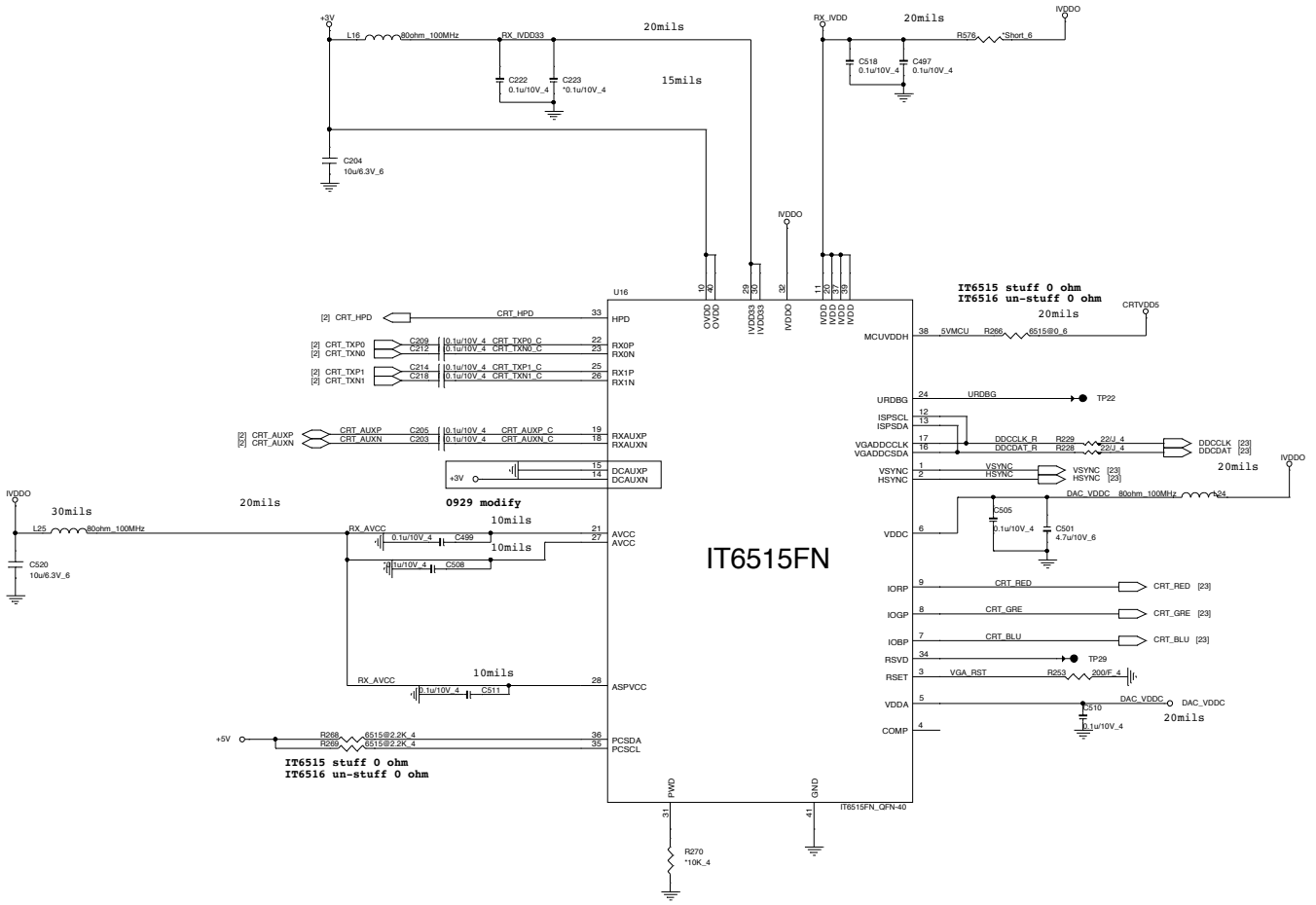


https://t.me/schematicslaptop
https://t.me/biosarchive



https://t.me/schematicslaptop
https://t.me/biosarchive

DP TO VGA



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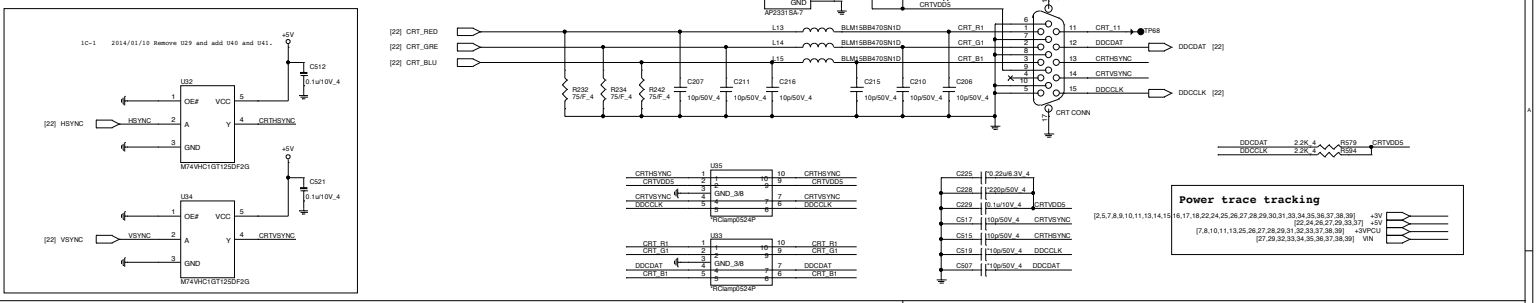
https://t.me/biosarchive

[2,5,7,8,9,10,11,13,14,15,16,17,18,23,24,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[23,24,26,27,29,33,37] +5V

Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: DP to VGA IT6165	Rev: 3A
Date: Wednesday, February 11, 2015	Sheet 22 of 44	

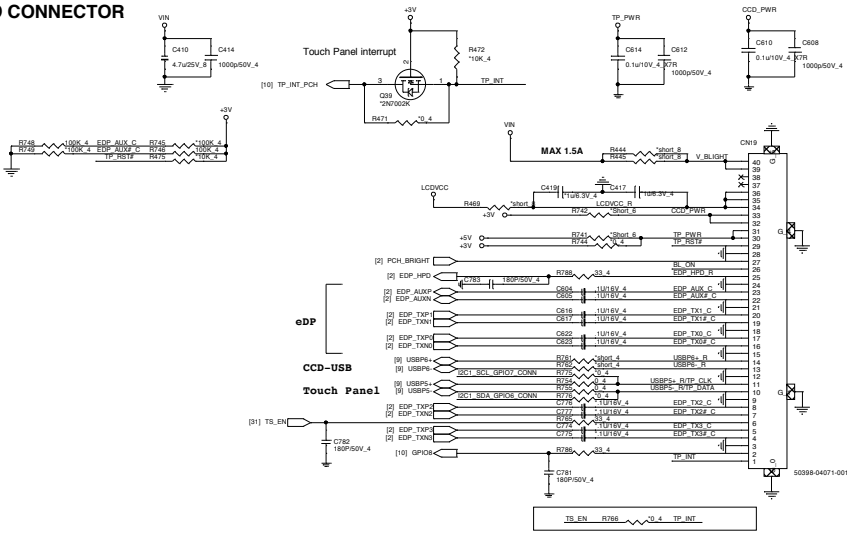
CRT



Power trace tracking

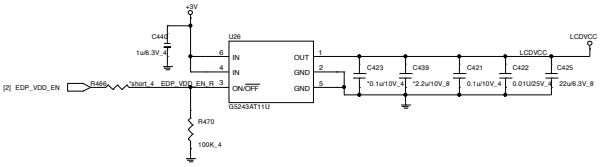
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,24,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[22,24,26,27,29,33,37] +5V
[7,8,10,11,13,25,26,27,28,29,31,32,33,37,38,39] +3VPCU
[27,29,32,33,34,35,36,37,38,39] VIN

LCD CONNECTOR

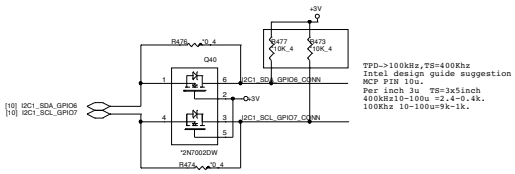


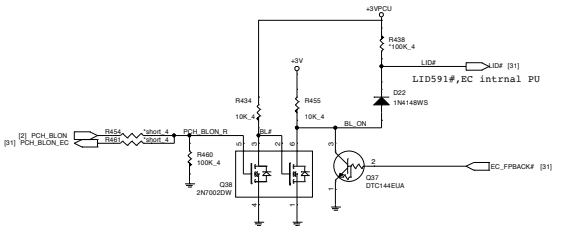
1C1-2 2014/03/11 Add R698 for TS_EN short TP_INT, for issue debug.

LCD Power



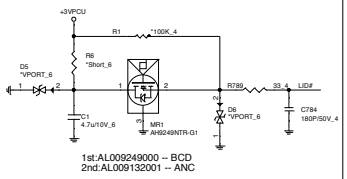
Touch screen level shift I2C(reserve)





1B-3 2013/12/10 change Q3.3 from +3V to +3VPCU.

Hall Sensor (HSR)



1st:AL009249000 -- BCD
2nd:AL009132001 -- ANC

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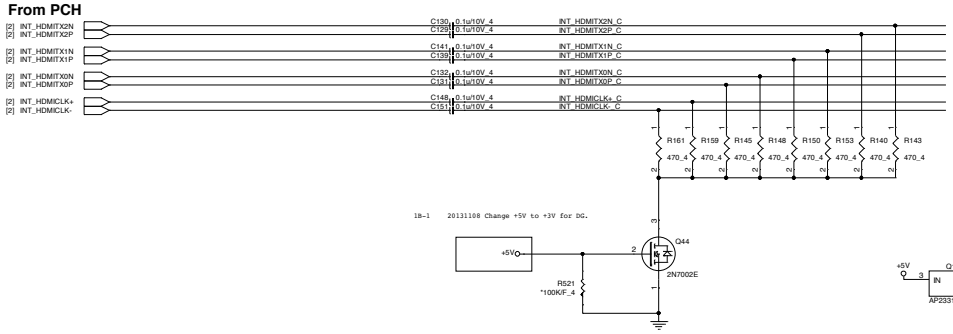
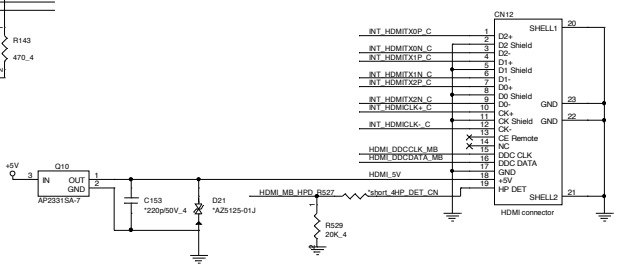
Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number	Rev 1A
	CRT/LVDS/CAMERA/LID	
Date: Wednesday, February 11, 2015	Sheet 23 of 44	

HDMI

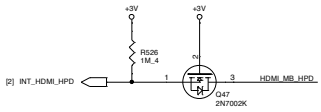
From PCH



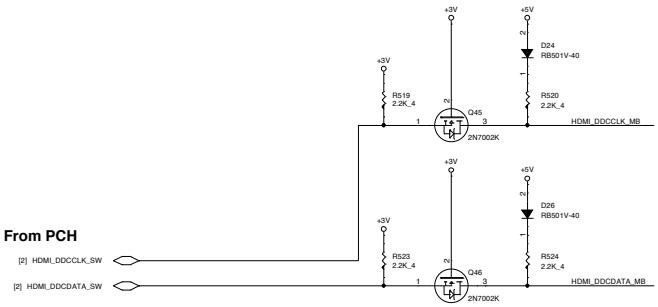
HDMI connector



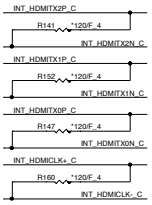
HDMI-detect



I2C



EMI



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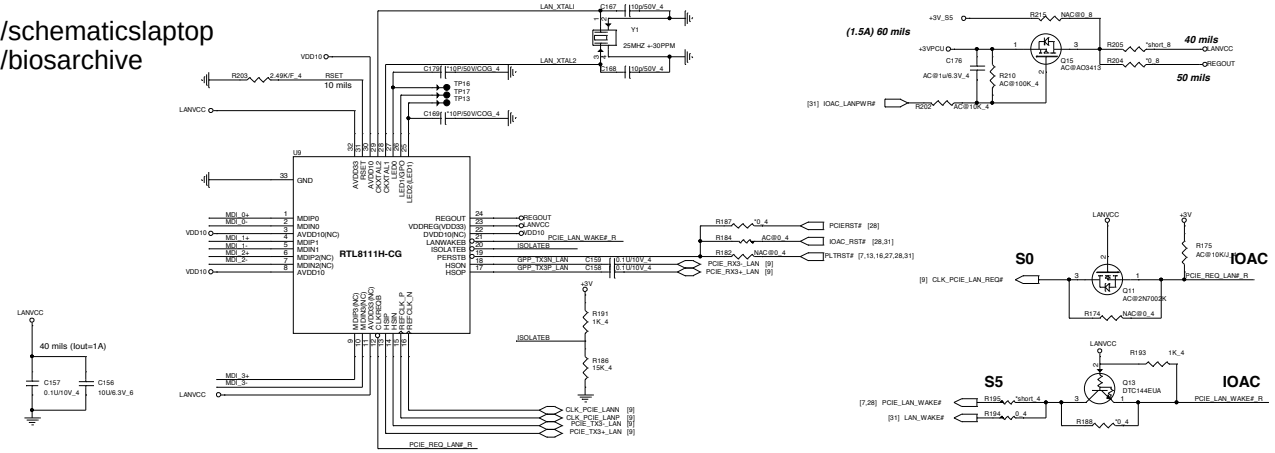
Power trace tracking

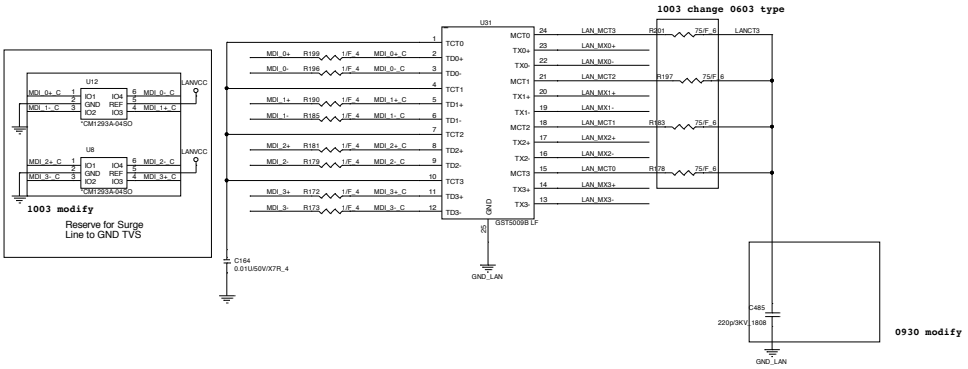
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[22,23,26,27,29,33,37] +5V

Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number	Rev
	HDMI (PS8101)	1A
Date: Wednesday, February 11, 2015	Sheet 24 of 44	

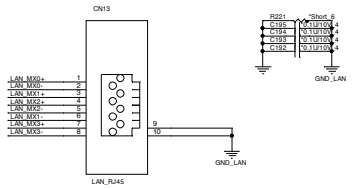
LAN



Tramsformer



RJ45 Connector



Power trace tracking

[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[5,7,8,9,10,11,13,27,29,31,33,36,38] +3V_S5
[7,8,10,11,13,23,26,27,28,29,31,32,33,37,38,39] +3VPCU

Quanta Computer Inc.

PROJECT :ZRT/ZRTA

Size	Document Number	Rev
	LAN (RTL8111GS)	1A
Date: Wednesday, February 11, 2015	Sheet 25 of 44	

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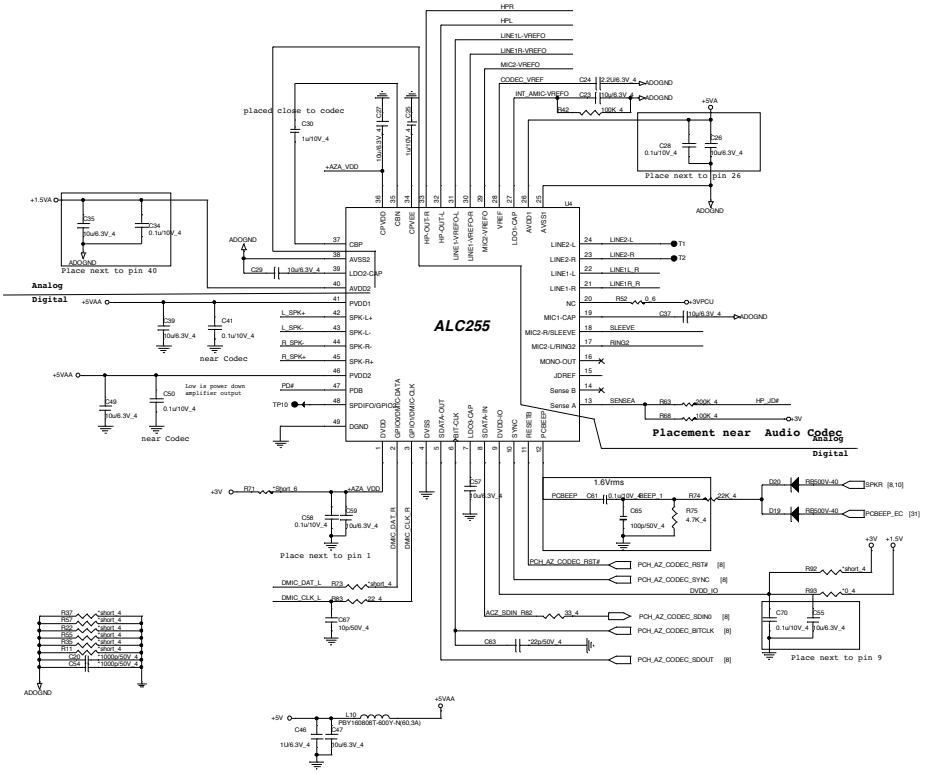
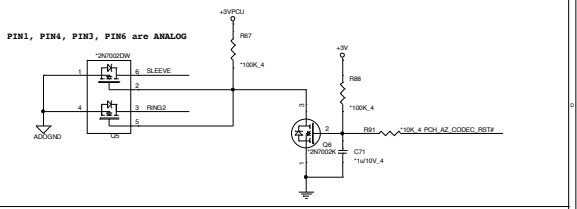
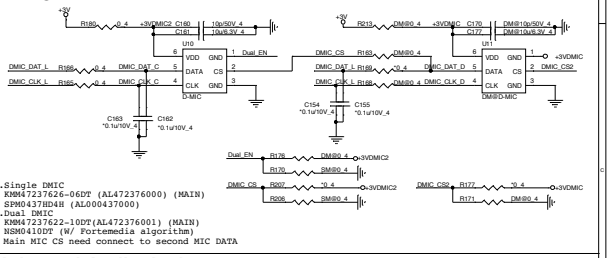
Codec(ADO)



Grounding circuit(ADO)

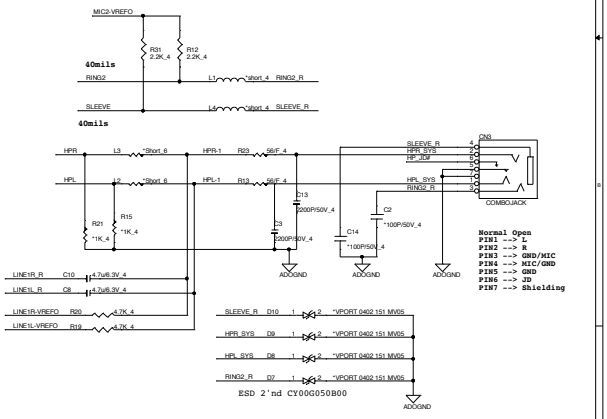


D-Mic

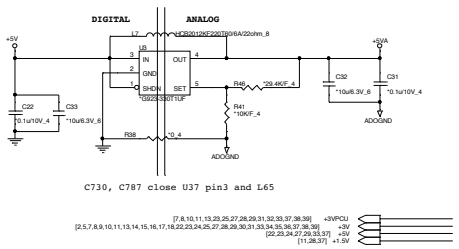


1.Single DMIC
KMM47237626-06DT (AL472376000) (MAIN)
SPM0437HD4H (AL000437000)
2.Dual DMIC
KMM47237622-10DT(AL472376001) (MAIN)
NSM0410DT (W/ Portemedia algorithm)
Main MIC CS need connect to second MIC DATA

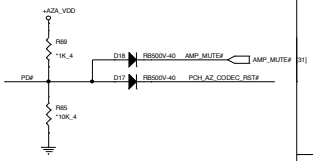
Universal Audio Jack



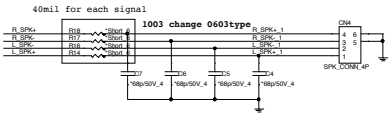
Codec PWR 5V(ADO)



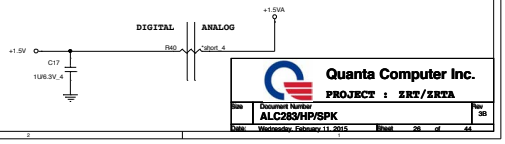
Mute(ADO)



Internal Speaker

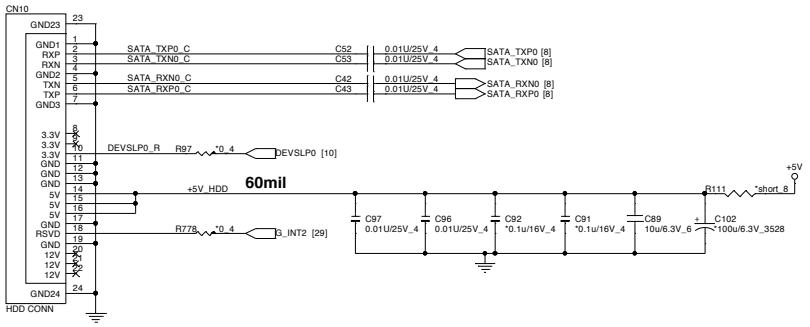


Codec PWR 3V/1.5V(ADO)

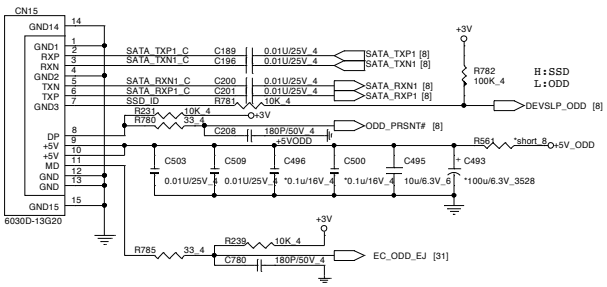


Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: ALC283/HP/SPK	Rev: 3S
Date: Wednesday, February 11, 2015	Sheet 36 of 44	

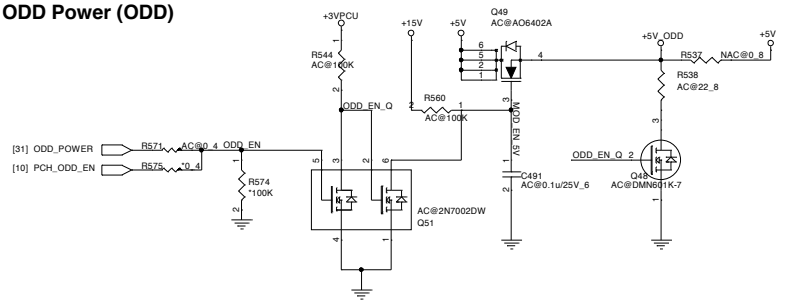
2.5" SATA HDD (HDD)



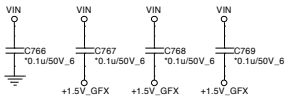
SATA ODD Connector(ODD)



ODD Power (ODD)

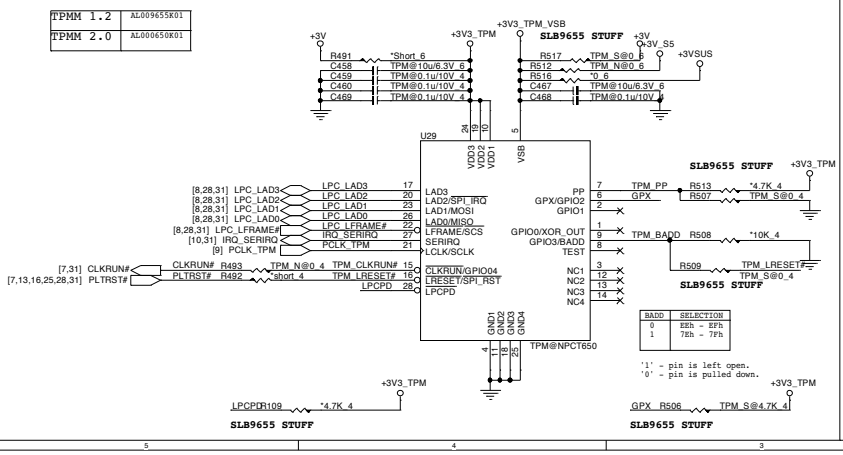


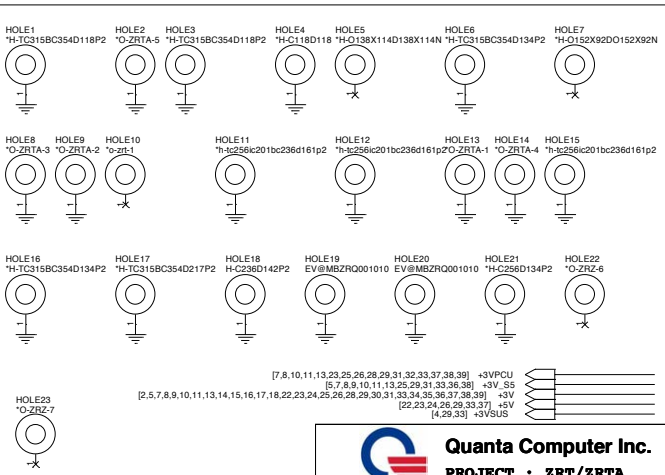
EMI



TPM NPCT650 (TPM)

TPMM 1.2	AL009655X01
TPMM 2.0	AL000650X01



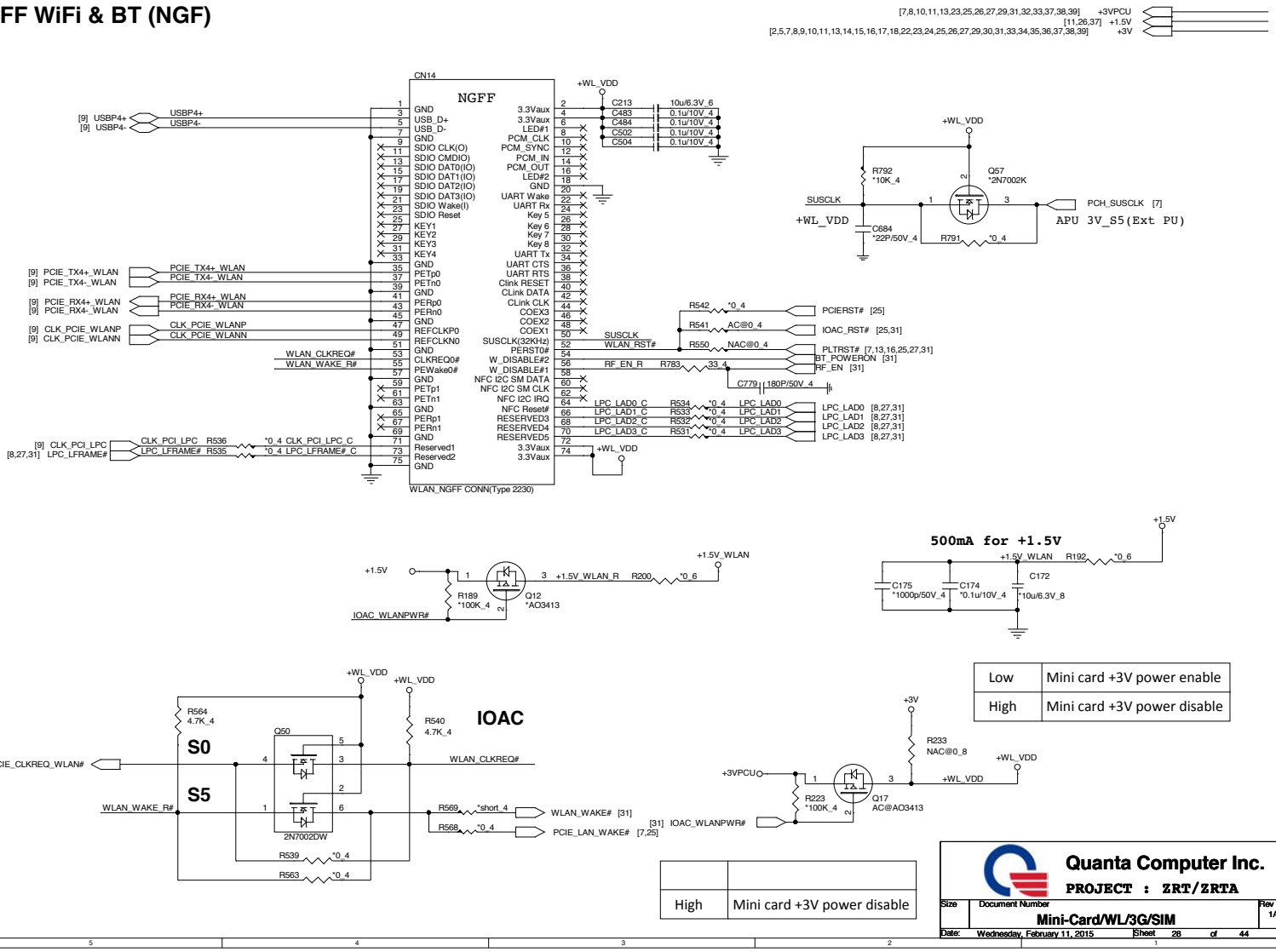


[7,8,10,11,13,23,25,26,28,29,31,32,33,37,38,39] +3VPCU
[5,7,8,9,10,11,13,25,29,31,33,36,38] +3V_S5
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,25,26,28,29,30,31,33,34,35,36,37,38,39] +3V
[22,23,24,26,29,33,37] +5V
[4,29,33] +3VSUS

Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	HDD/ODD/TPM NPCT650	1A
Date: Wednesday, February 11, 2015	Sheet 27 of 44	

NGFF WiFi & BT (NGF)

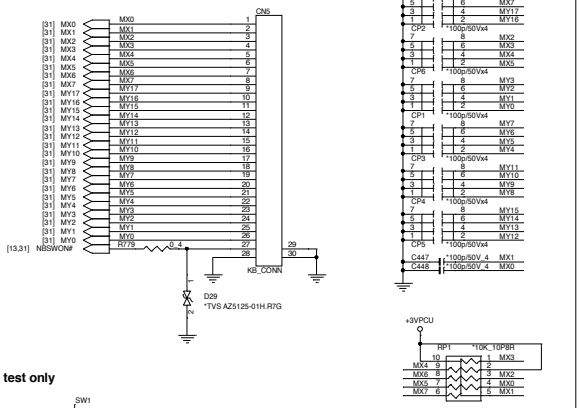


Low	Mini card +3V power enable
High	Mini card +3V power disable

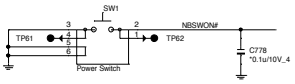
High	Mini card +3V power disable

Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Size: Document Number: Mini-Card/WL/3G/SIM Rev: 1A
Date: Wednesday, February 11, 2015 Sheet 28 of 44

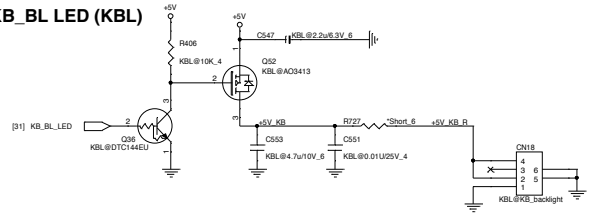
K/B (KBC)



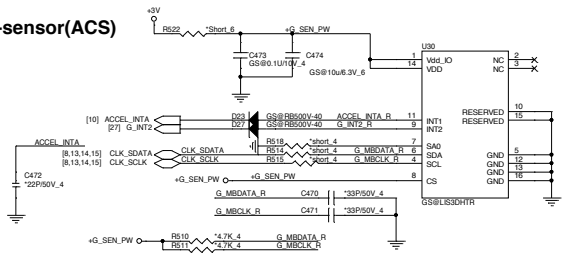
For test only



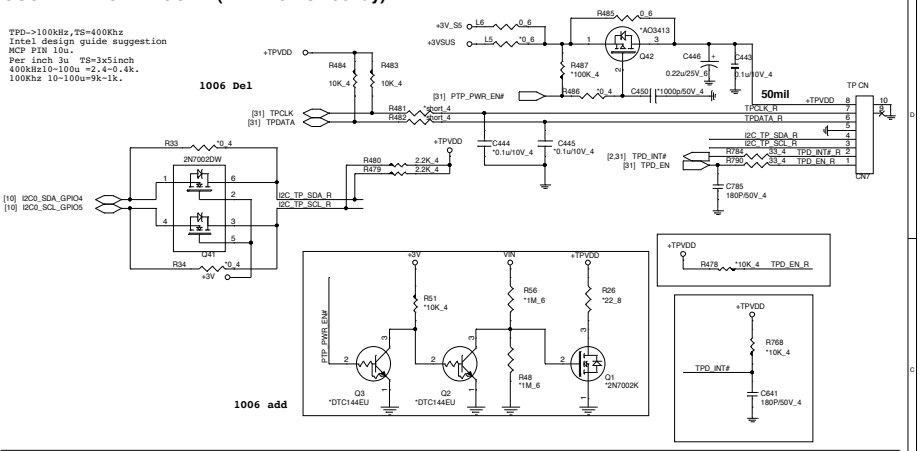
KB_BL LED (KBL)



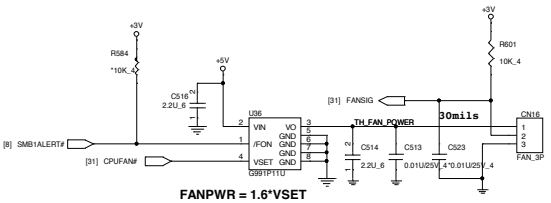
G-sensor(ACS)



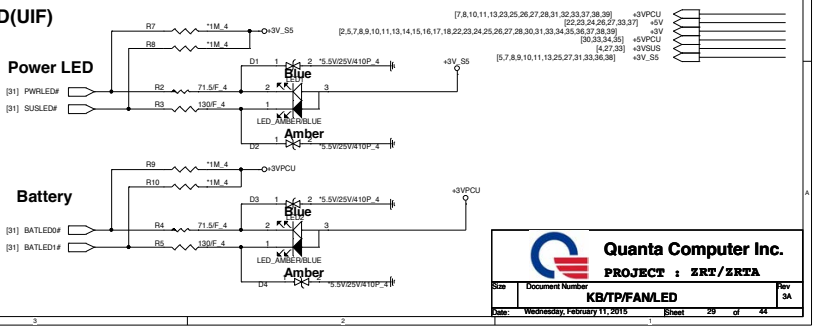
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



CPU FAN (THM)

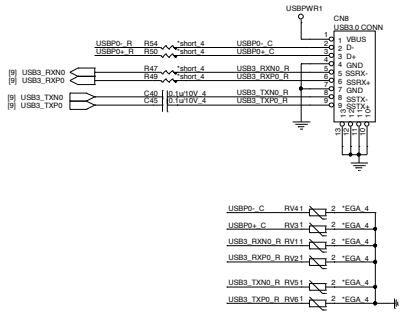


POWER LED(UIF)

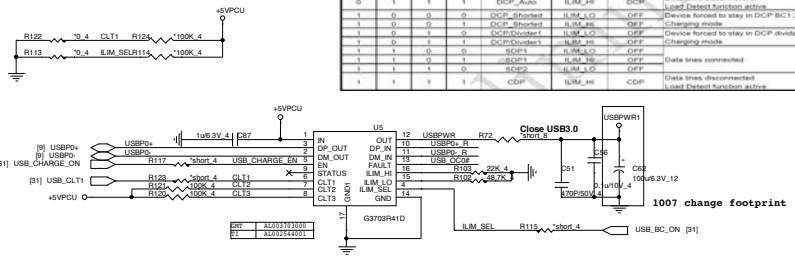


Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number	Rev
	KB/TP/FAN/LED	3A
Date: Wednesday, February 11, 2015	Sheet 29 of 44	

USB 3.0 Connector(UB3)

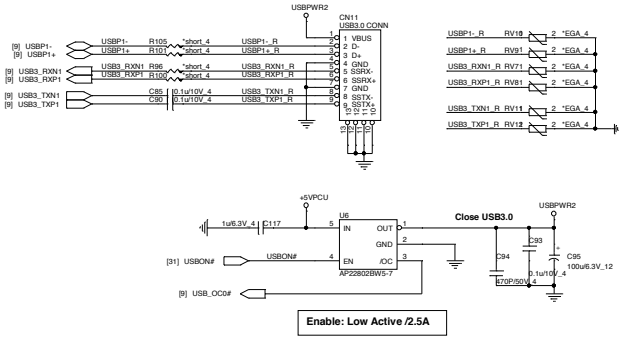


USB Charger for USB3.0 Port0 (UBC)

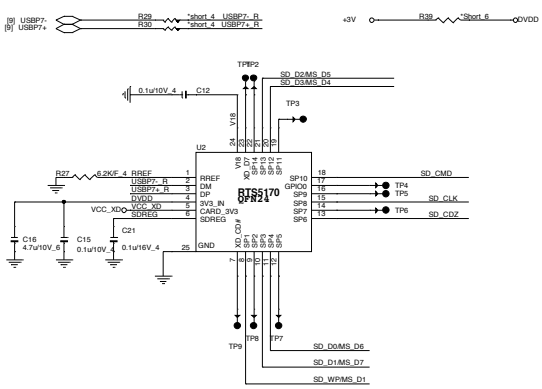


CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	
0	0	0	1	Discharge	NA	OFF	OUT held low
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	Charging mode
1	1	0	0	SDP1	ILIM_LO	OFF	
1	1	0	1	SDP1	ILIM_HI	OFF	Data lines connected
1	1	1	0	SDP2	ILIM_LO	OFF	
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active

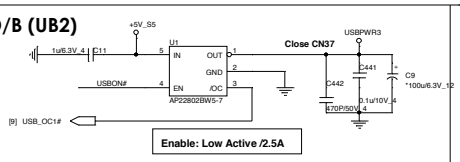
USB 3.0 Connector(UB3)



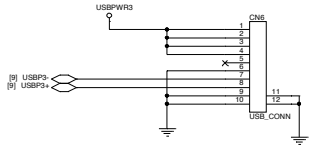
Card Reader (CRD)



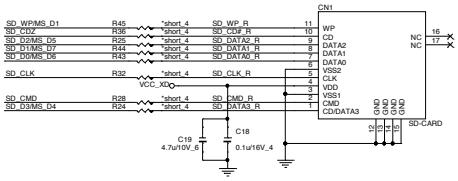
USB IO D/B (UB2)



D/B USB Port



SD/MMC CARD READER (CRD)



[4,33,36,38,39] +5V_S5
[33,34,35] +5VPCU
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,25,26,27,28,29,31,33,34,35,36,37,38,39] +3V

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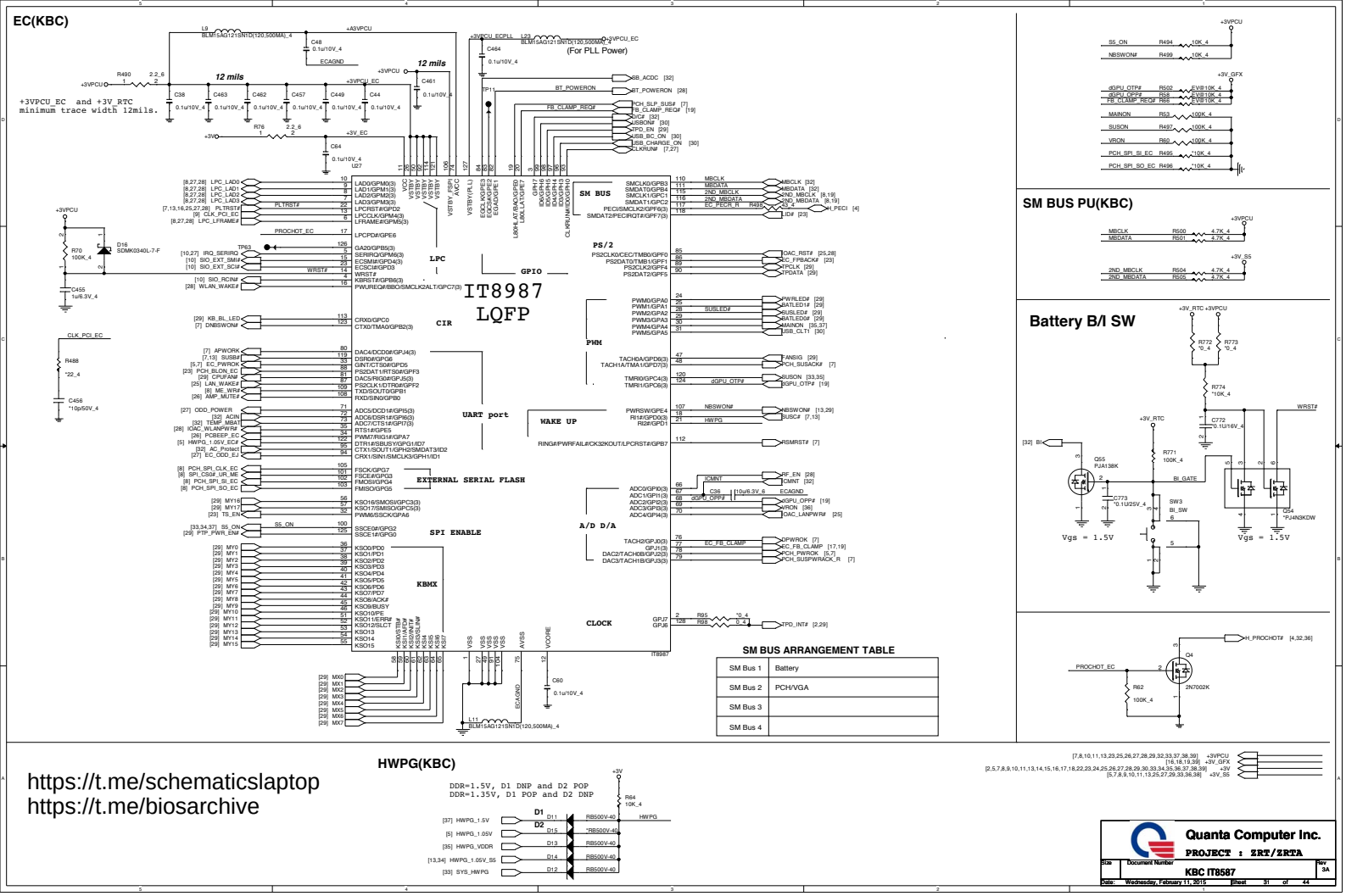
Size	Document Number	Rev
	USB Port/ DB	1A
Date: Wednesday, February 11, 2015	Sheet 30 of 44	



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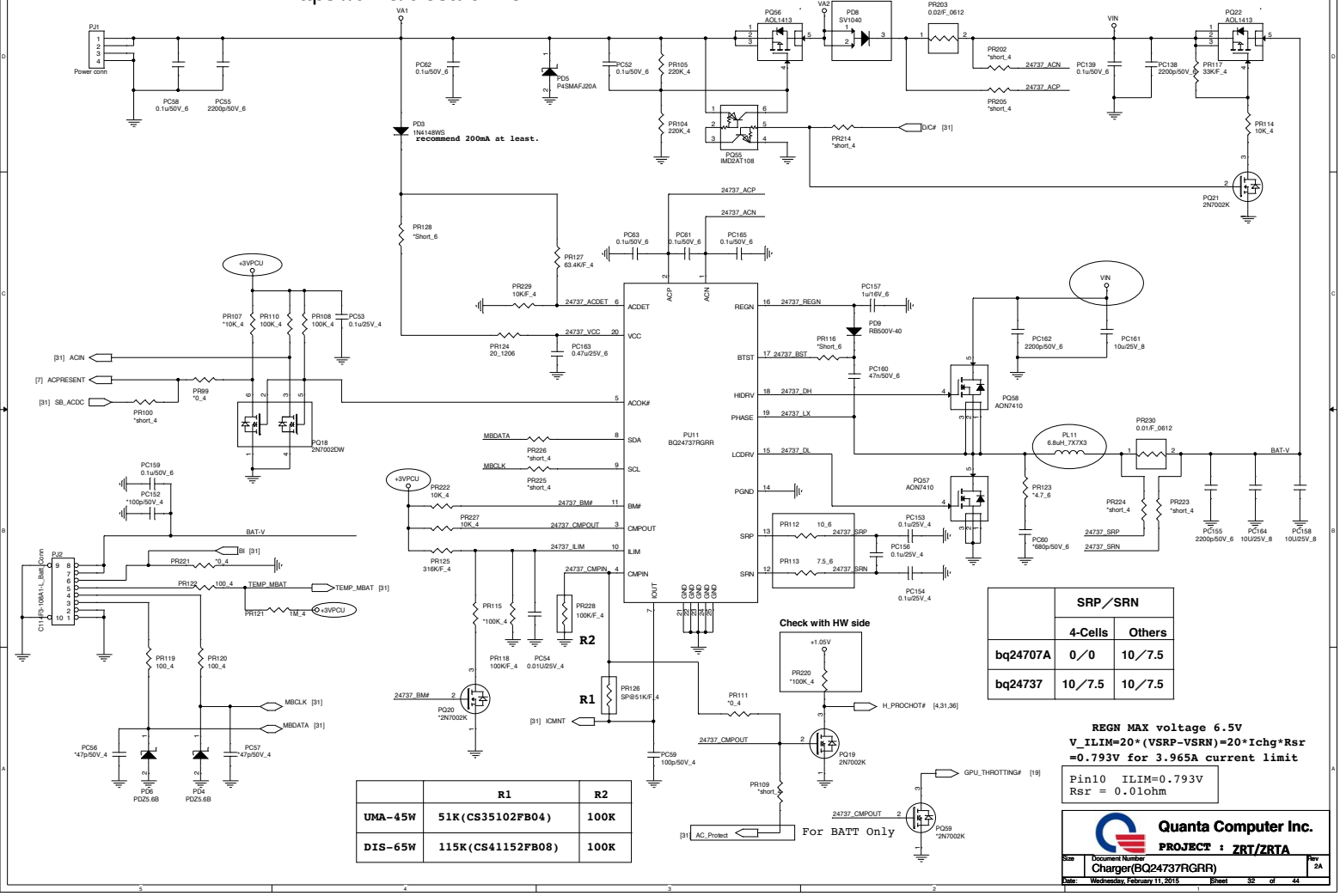

	SRP／SRN	
	4-Cells	Others
bq24707A	0／0	10／7.5
bq24737	10／7.5	10／7.5

	R1	R2
UMA-45W	51K(CS35102FB04)	100K
DIS-65W	115K(CS41152FB08)	100K

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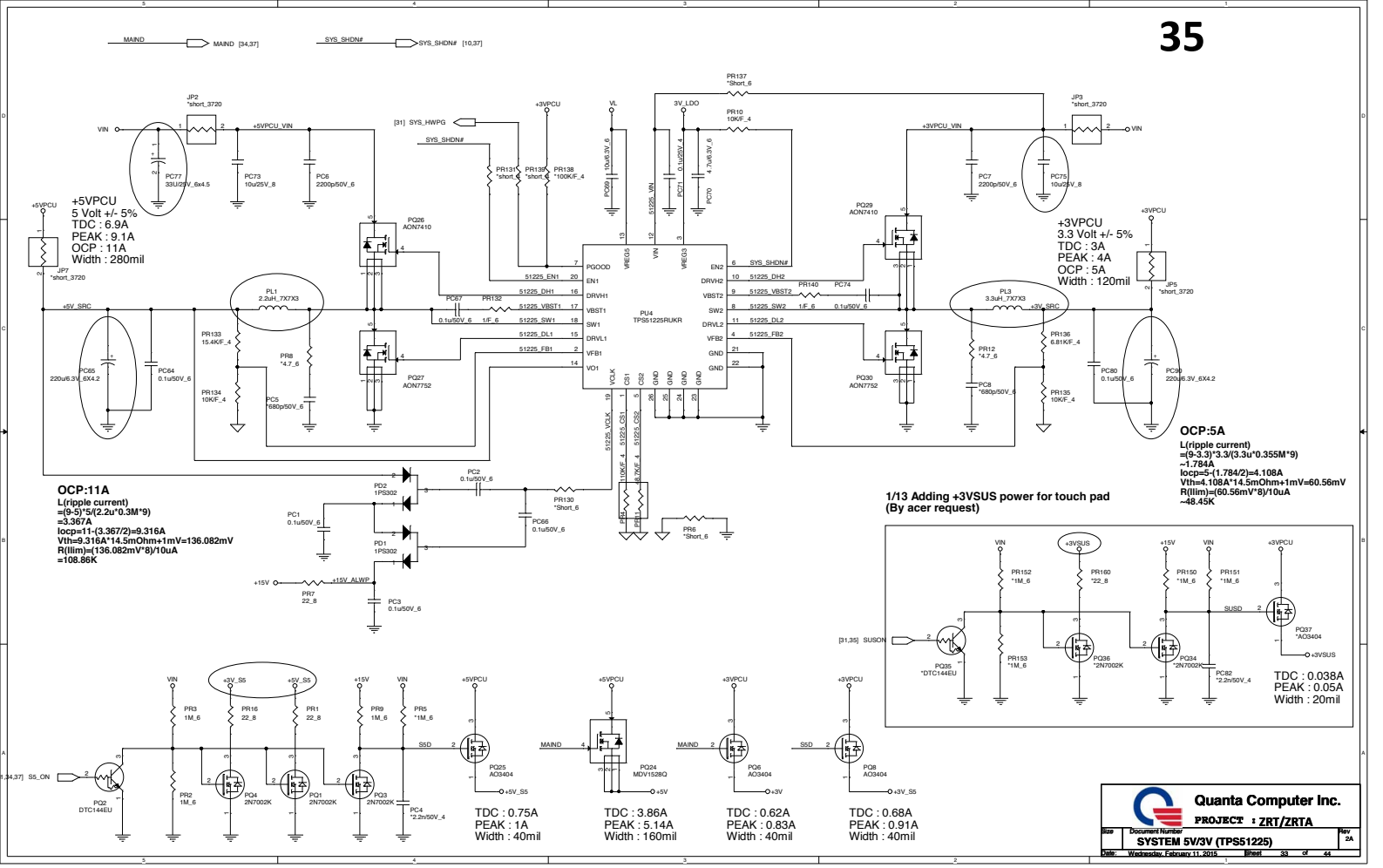
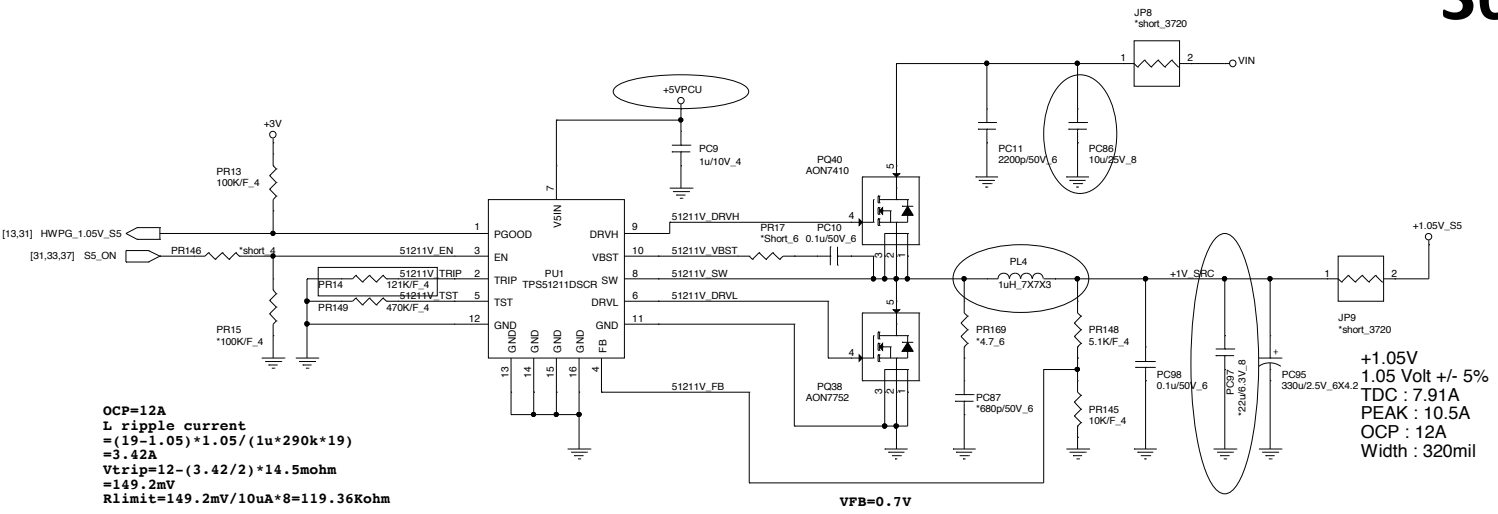
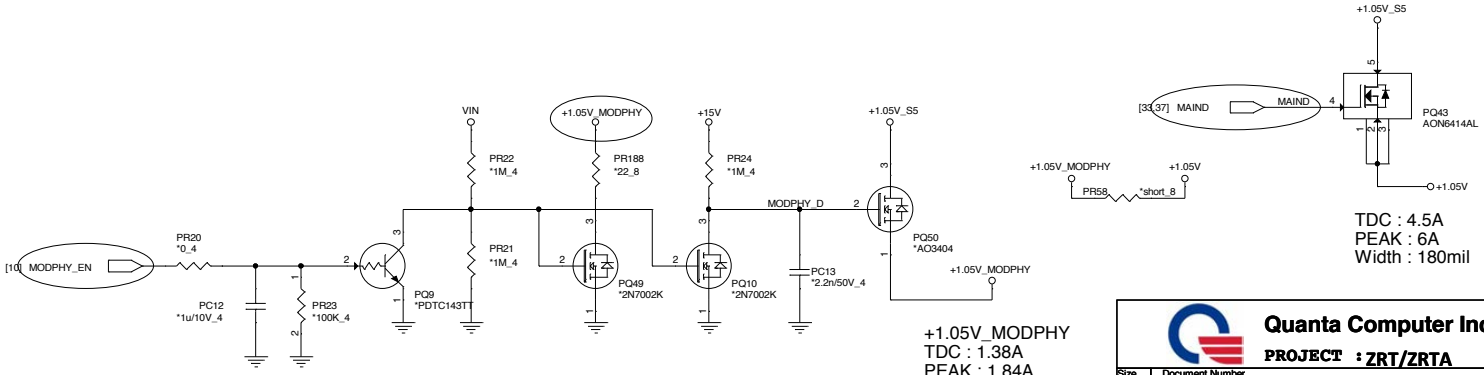
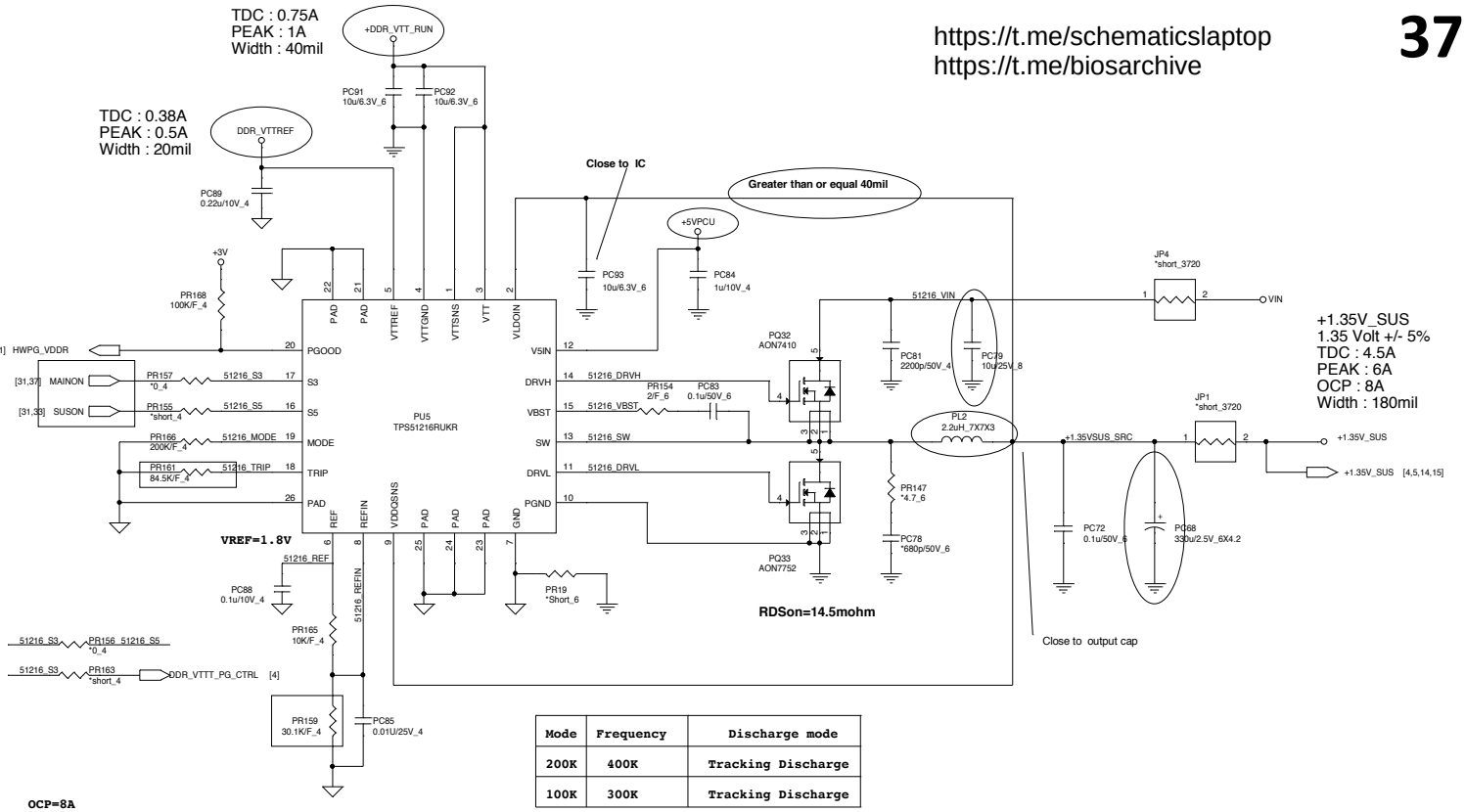






Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: +1.05V_S5 (TPS51211)	Rev: 2A
Date: Wednesday, February 11, 2015	Sheet 34 of 44	



Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=8A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=8-(1.425/2)*14.5mohm
=105.668mV
Rlimit=105.668mV/10uA*8=84.53Kohm

DDR=1.35V
PR84=10K/F_4
PR86=30.1K/F_4

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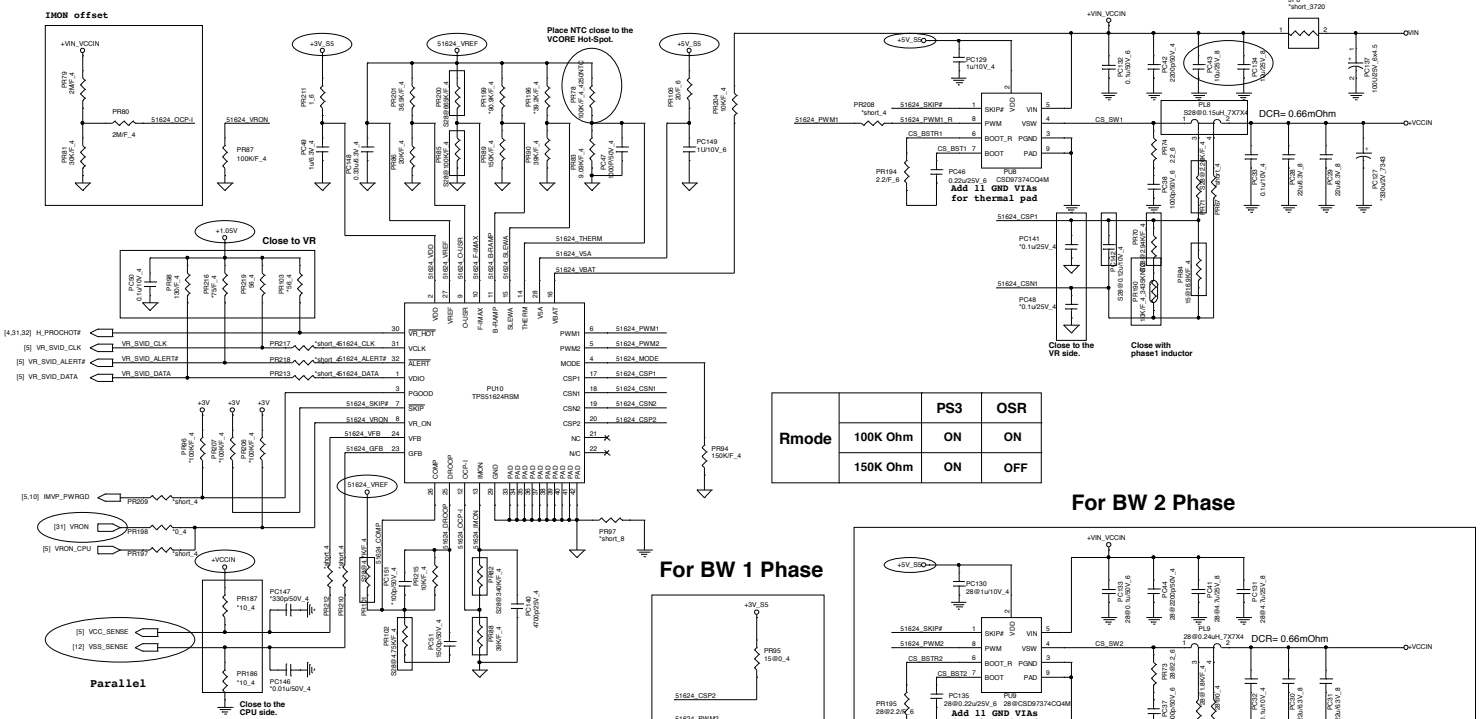
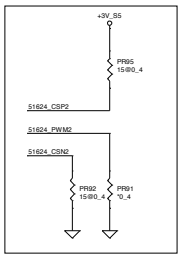
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	2A
Date: Wednesday, February 11, 2015	Sheet 35 of 44	



Rmode		PS3	OSR
	100K Ohm	ON	ON
	150K Ohm	ON	OFF

For BW 1 Phase



For BW 2 Phase

BW-U 15W (1 phase)

Icc TDC PL2：14A
Icc Max：32A
OCP：37A
Fsw：1.2MHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

BW-U 28W (1 phase)

Icc TDC PL2：19A
Icc Max：40A
OCP：47A
Fsw：800KHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

S28@

BW-U 28W 2 phase			
Location	Value	Location	Value
PL8	CV+24P0MZ00	PR85	CS35622FB10
PR71	CS21822FB14	PR101	CS22372FB11
PR82	CS41502FB18	PR102	CS31002FB26
PR70	CS22672FB12	PR200	CS42942FB13
PC142	CH4152K9B02		
Block 1.	Stuff		

PL9 0.24uH_7X7X4
PR84、PR93 *22.6K/F_4
PR92、PR95 *0_4
PC143、PC145 *0.1u/25V_4

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VCCIN(TPS51624)
Rev 2A
Date: Wednesday, February 11, 2015 Sheet 38 of 44

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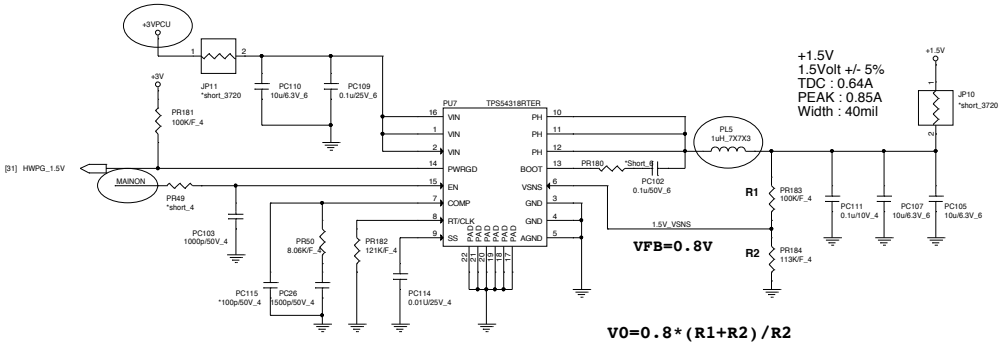
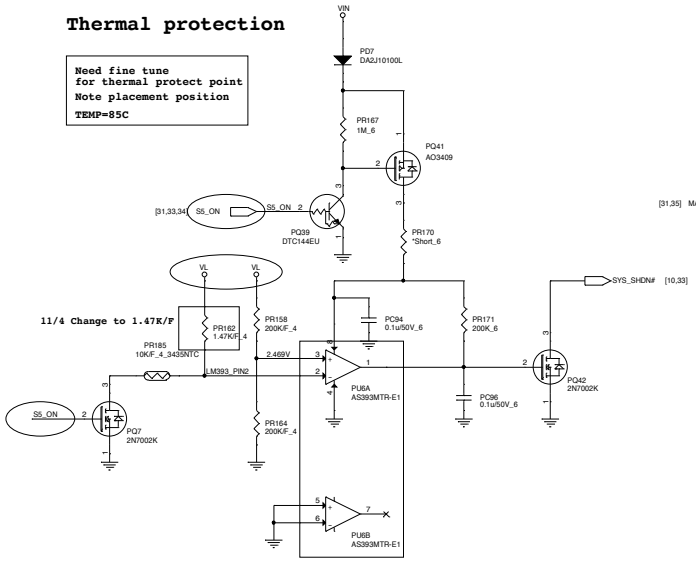


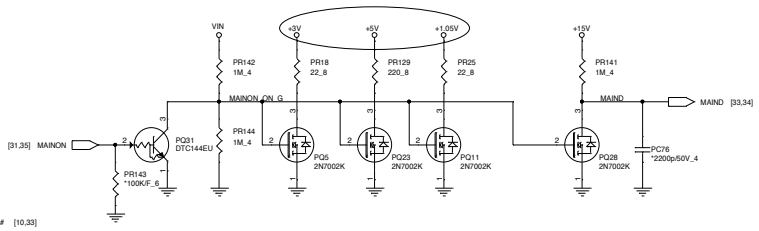
V0=0.8*(R1+R2)/R2

Thermal protection

Need fine tune
for thermal protect point
Note placement position

TEMP=85C





For EC control thermal protection (output 3.3V)

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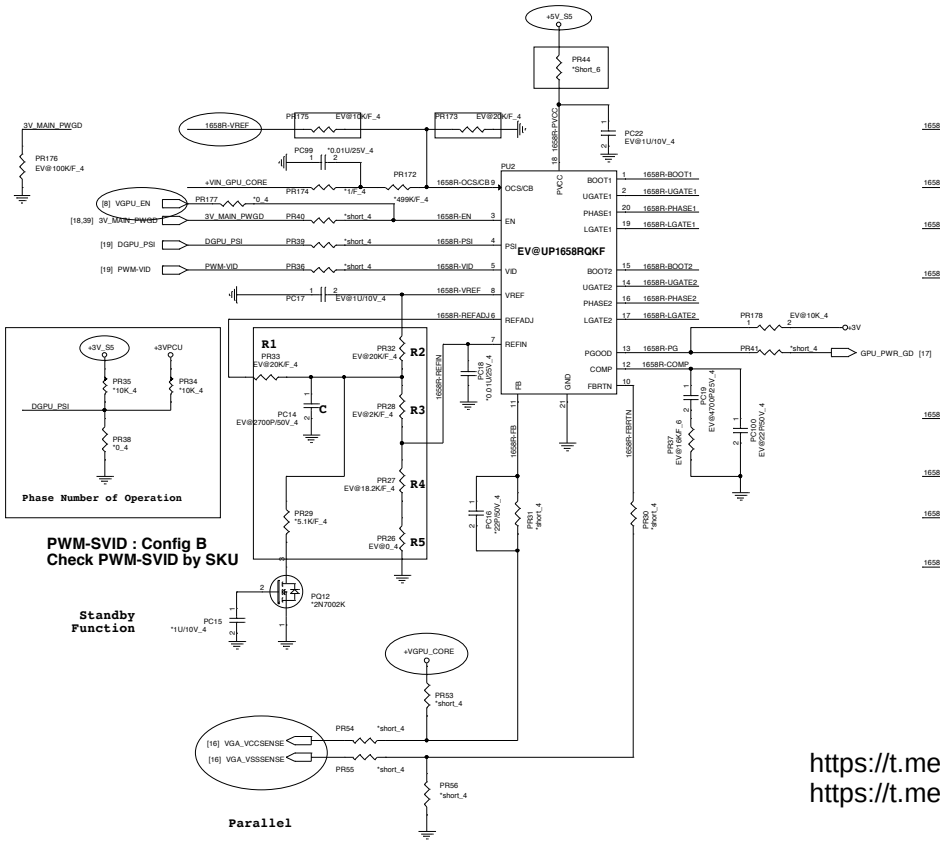
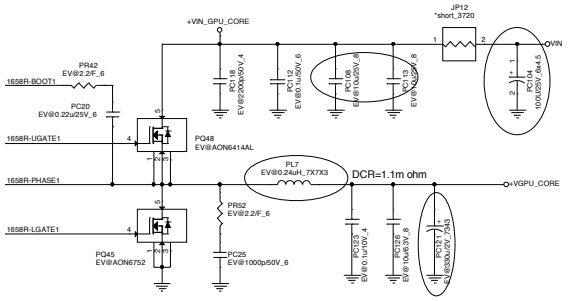
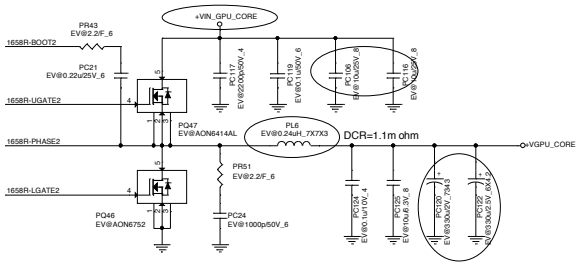
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	+1.5V/Thermal Protect	2A
Date: Wednesday, February 11, 2015	Sheet 37 of 44	







N16S-GT(23W)
+VGPU_CORE Countinue current:26A Peak current:51A OCP:A FSW:300KHz L/L=0mV/A

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Size	Document Number: +VGPU_CORE(UP1642PQAG)	Rev: 2A
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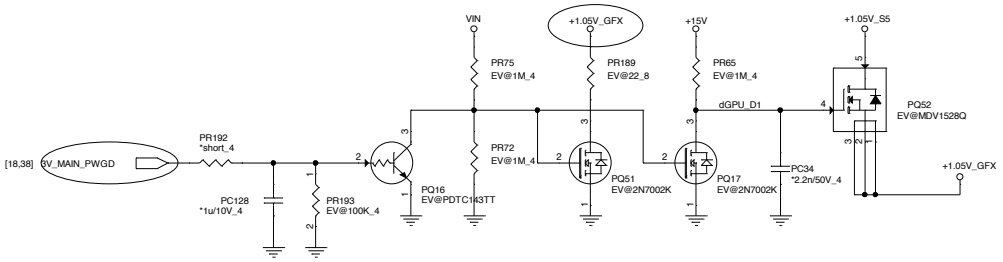
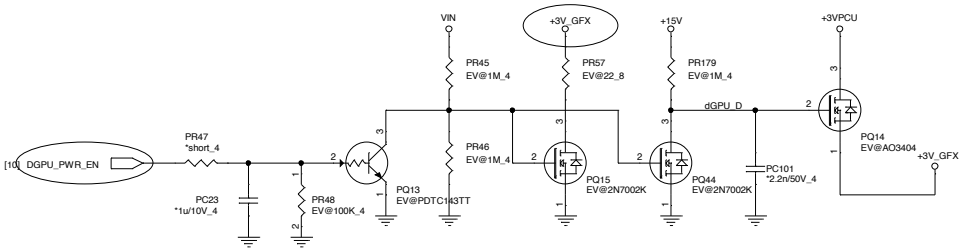
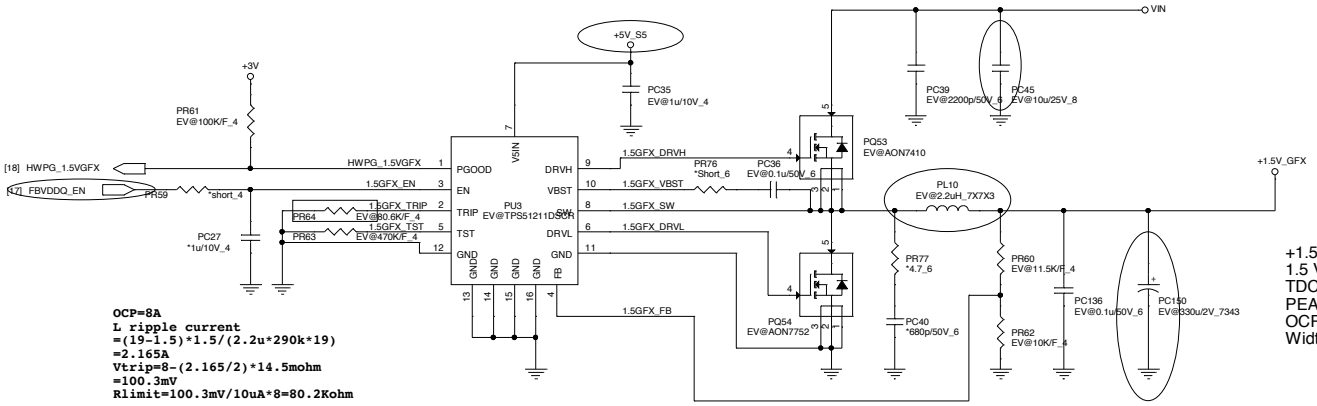
[16,17,18] +1.05V_GFX
[17,20,21,27] +1.5V_GFX
[16,18,19,31] +3V_GFX



+1.05V_GFX
TDC : 1.57A
PEAK : 2.1A
Width : 80mil



+3V_GFX
TDC : 0.05A
PEAK : 0.06A
Width : 20mil



OCP=8A
L ripple current
=(19-1.5)*1.5/(2.2u*290k*19)
=2.165A
Vtrip=8-(2.165/2)*14.5mohm
=100.3mV
Rlimit=100.3mV/10uA*8=80.2Kohm

VFB=0.704V

+1.5V_GFX
1.5 Volt +/- 5%
TDC : 3.06A
PEAK : 4.08A
OCP : 5A
Width : 140mil

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Size	Document Number	Rev
	+1.5V_GFX/+1.05V_GFX/+3V_GFX	2A
Date: Wednesday, February 11, 2015	Sheet 39 of 44	

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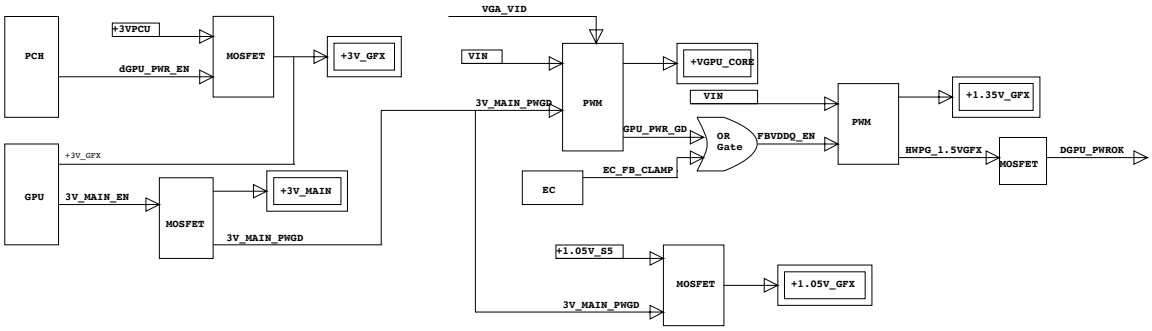
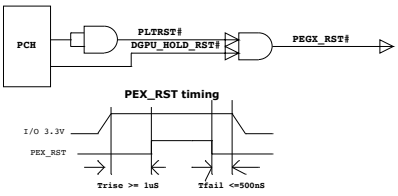
VGA power up sequence



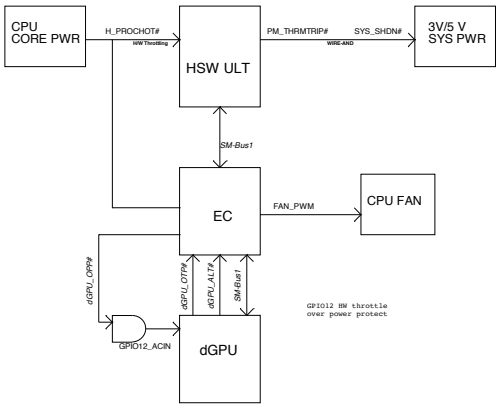
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+3V_GFX	variation	External GPU POWER	DGPU_PWR_EN	S0
+1.05V_GFX	+3.3V	External GPU POWER	3V_MAIN_EN	S0
+VGPU_CORE	+1.35V	External GPU POWER	3V_MAIN_EN	S0
+1.35V_GFX	+1.05V	External GPU POWER	FBVDDQ_EN	S0

Thermal Follow Chart



dGPU_OPP# EC notify HW throttle over power protect
dGPU_OTP# VGA thrmtrip# => inform EC over temperature protect

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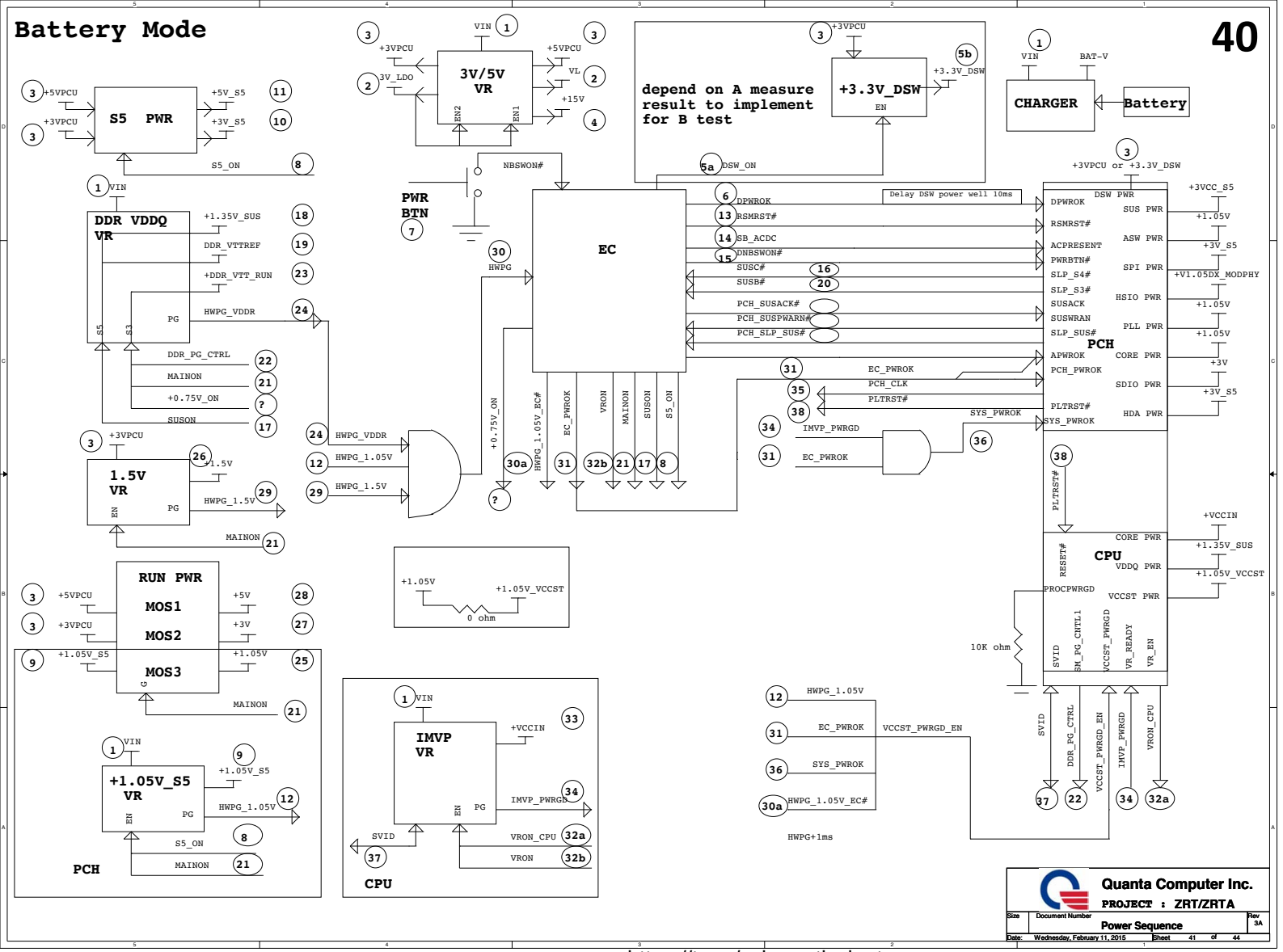
Size | Document Number | Rev 5A
PWR Status & GPU PWR CRL & THRM
Date: Wednesday, February 11, 2015 | Sheet 40 of 44



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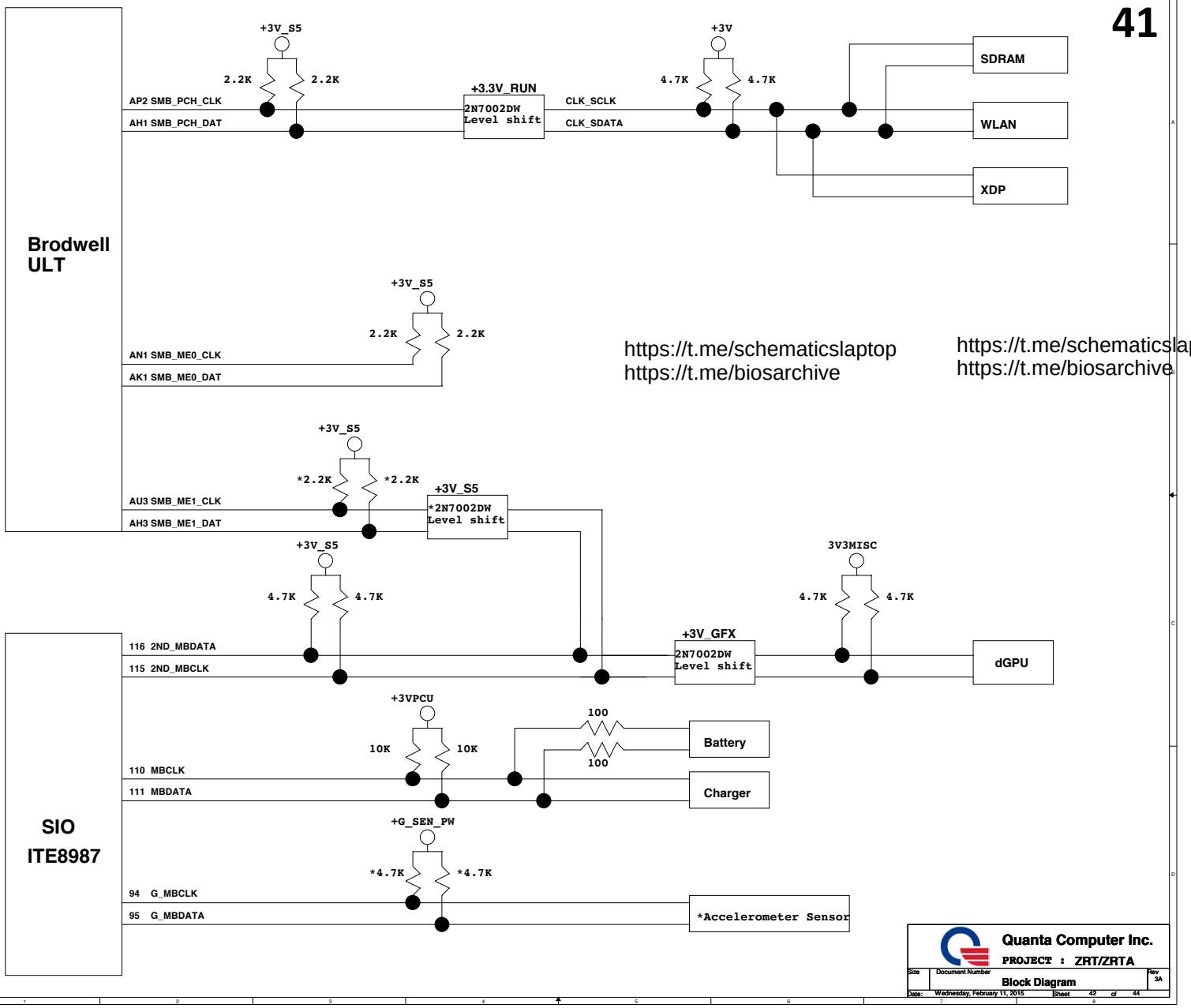

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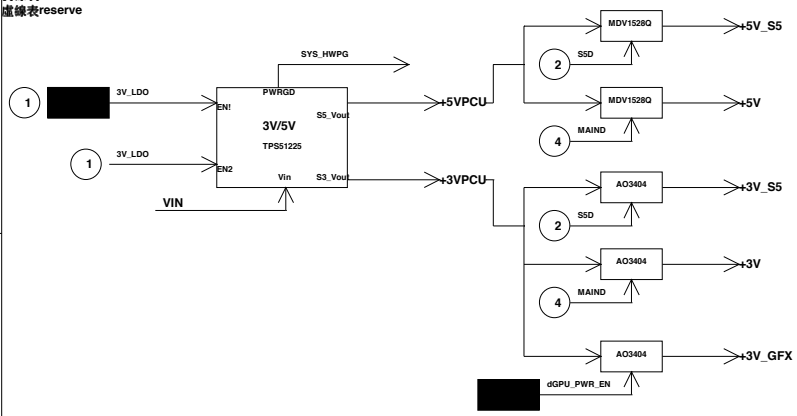
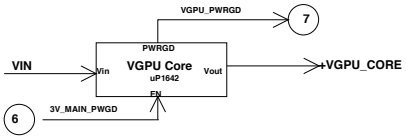
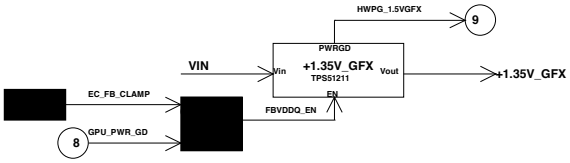
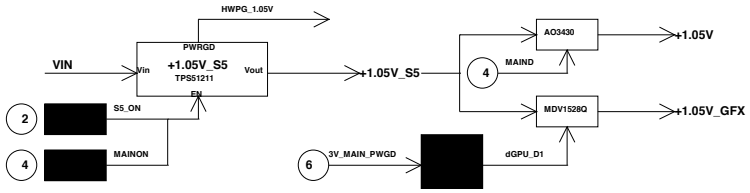
PROJECT : ZRT/ZRTA
Size | Document Number | Rev 3A
Block Diagram
Date: Wednesday, February 11, 2015 | Sheet 42 of 44

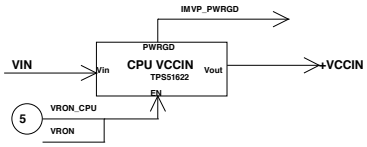
實線表defult
虛線表reserve

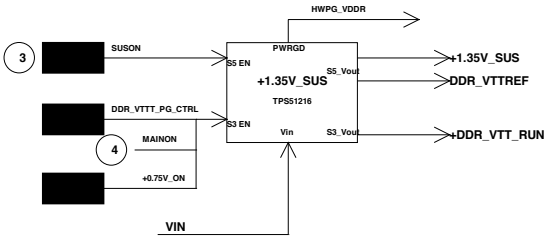


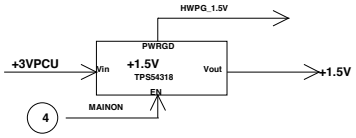












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PROJECT : ZRT/ZRTA
Size | Document Number | Rev 3A
ULT PWR CONTROL
Date: Wednesday, February 11, 2015 | Sheet 43 of 44

Model	Version	CHANGE LIST
ZQ0	1A-1	1 2013/10/15 change pin define and add pwm IC.(page31)
		2 2013/10/15 Change VGA ITE solution to NXP.(page 23)
		3 2013/10/15 power board CN change to 6pin.(Page 23)
		4 2013/10/15 U5017.12 change 27M crystal to VGA IC.(Page 23)
		5 2013/10/15 U5017.14 add power rail +3V_RTC(page23)
		6 2013/10/15 strap0 R672 DG 50k PU.(Page 19)
		7 2013/10/15 Change AND gat to Q63 D-MOS.(Page 19)
		8 2013/10/15 change pin define and add pwm IC U17.(Page 46)
		9 2013/10/15 for GC6 stuff R228\R1013\R226\R1012.un-stuff Q24\Q26\R227\R1011. (Page19)
		10 20131015 For GC6 NV DG GC6_FB_EN PD.(Page10)
		11 2013/10/15 following up acer define and swap USB3 and USB2 port.(Page9)
		12 2013/10/15 swap CAP C8579/C8580 to Vrefo and resistor R5214/R5215 to Line in.(Page30)
		13 2013/10/15 U27.30/U27.31 del fan Pwm signal.(Page32)
		14 20131015 change LVDS\USB3\RJ45\FAN\TPD\USB DB CN\DC-IN CN\Power Button\Cardreader\KB BLK CN\Power board, footprint.
	1A-2	1 2013/10/16 JDIM5 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.(page15)
		2 2013/10/16 JDIM6 Chage net name M_B_DQS#[7:0] to M_A_DQS#[7:0].(page14)
		3 2013/10/16 Add RTC charge circuit.(page8)
		4 2013/10/16 BT1.1 Chage +3V_RTC_0 to VCCTC_2.(page8)
		5 2013/10/15 change power rail from +3V_RTC_0 to VCCRTC_2.(page23)

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DOC NO.	PROJECT MODEL :	ZQ0	APPROVED BY:		DATE:		Quanta Computer Inc. PROJECT : ZRT/ZRTA
	PART NUMBER:		DRAWING BY:		REVISON:		Size: Document Number: Change list-1 Rev: 3A
							Date: Wednesday, February 11, 2015 Sheet 44 of 44