

# Compal Confidential

## EA50\_KV M/B Schematics Document

### AMD Kaveri(FP3) + Bolton(M3)

AMD UMA

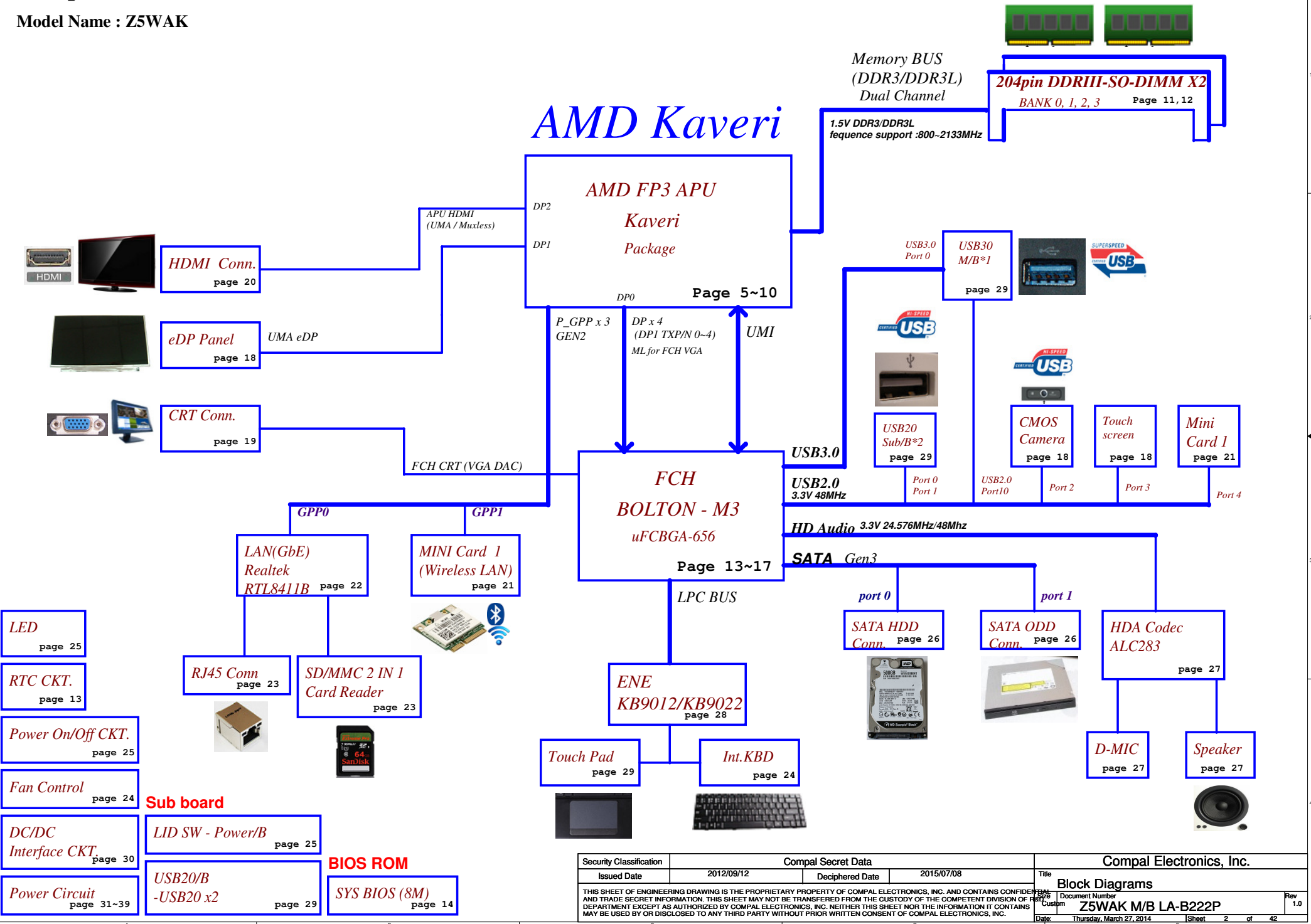
2014-03-25

REV : 1.0

|   |                    |                 |            |                                |               |
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|   |                    |                 |            | Document Number                | Rev           |
|   |                    |                 |            | Z5WAK M/B LA-B222P             | 1.0           |
|   |                    |                 |            | Date: Thursday, March 27, 2014 | Sheet 1 of 42 |

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Model Name : Z5WAK



|   |                    |                 |                          |                 |
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| Date: Thursday, March 27, 2014  |                    |                 |                          | Rev 1.0         |
| Date: Thursday, March 27, 2014  |                    |                 |                          | Sheet 2 of 42   |

# Voltage Rails

| Power Plane  | Description                                  | S0 | S3   | S4    | S5    |
|--------------|--|----|------|-------|-------|
| VIN          | Adapter power supply (19V)                   | ON | ON   | ON    | ON    |
| B+           | AC or battery power rail for power circuit.  | ON | ON   | ON    | ON    |
| +CPU_CORE    | Core voltage for APU                         | ON | OFF  | OFF   | OFF   |
| +CPU_CORE_NB | Voltage for VDDNB                            | ON | OFF  | OFF   | OFF   |
| +0.75VS      | 0.75V switched power rail for DDR terminator | ON | OFF  | OFF   | OFF   |
| +1.1VALW     | 1.1V switched power rail for FCH             | ON | ON   | AC/DC | AC/DC |
| +1.1VS       | 1.1V switched power rail for FCH             | ON | OFF  | OFF   | OFF   |
| +1.05VS      | 1.05VS switched power rail for APU           | ON | OFF  | OFF   | OFF   |
| +1.5V        | 1.5V power rail for CPU VDDIO and DDR        | ON | ON   | OFF   | OFF   |
| +1.5VS       | 1.5VS switched power rail                    | ON | OFF  | OFF   | OFF   |
| +1.8VS       | 1.8VS for CPU_VDDA                           | ON | OFF  | OFF   | OFF   |
| +3VALW       | 3.3V always on power rail                    | ON | ON   | ON    | ON    |
| +3V_LAN      | 3.3V power rail for LAN                      | ON | ON   | WOL   |       |
| +3VS_WLAN    | 3.3V power rail for WLAN                     | ON | IOAC | IOAC  | OFF   |
| +3VS         | 3.3V switched power rail                     | ON | OFF  | OFF   | OFF   |
| +5VALW       | 5V always on power rail                      | ON | ON   | ON    | ON    |
| +5VS         | 5V switched power rail                       | ON | OFF  | OFF   | OFF   |
| +RTCVCC      | RTC power                                    | ON | ON   | ON    | ON    |

## EC SM Bus1 address

| Device        | Address   | HEX | Device               | Address   | HEX |
|---------------|-----------|-----|----------------------|-----------|-----|
| Smart Battery | 0001 011X | 16H | SB-TSI (APU)         | 1001 100X | 96H |
|               |           |     | VGA Internal Thermal |           |     |

## EC SM Bus2 address

| Device | Address | HEX | Device | Address | HEX |
|--------|---------|-----|--------|---------|-----|
|        |         |     |        |         |     |

## FCH SM Bus 0 address

| Device    | Address    | HEX | Device | Address | HEX |
|-----------|------------|-----|--------|---------|-----|
| DDR DIMM1 | 1010 000Xb | A0H |        |         |     |
| DDR DIMM2 | 1010 001Xb | A2H |        |         |     |
| MINI CARD |            |     |        |         |     |

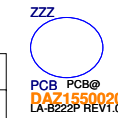
## FCH SM Bus 1 address

| Device | Address | HEX | Device | Address | HEX |
|--------|---------|-----|--------|---------|-----|
|        |         |     |        |         |     |

| STATE                 | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V  | +VS | Clock |
|-----------------------|--------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON               |        | HIGH    | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | ON    |
| S1 (Power On Suspend) |        | LOW     | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | LOW   |
| S3 (Suspend to RAM)   |        | LOW     | LOW     | HIGH    | HIGH    | ON    | ON  | OFF | OFF   |
| S4 (Suspend to Disk)  |        | LOW     | LOW     | LOW     | HIGH    | ON    | OFF | OFF | OFF   |
| S5 (Soft OFF)         |        | LOW     | LOW     | LOW     | LOW     | ON    | OFF | OFF | OFF   |

## Board ID / SKU ID Table for AD channel

| Vcc      | 3.3V        |        |        |        |             |
|----------|-------------|--------|--------|--------|-------------|
| Ra       | 100K +/- 1% |        |        |        |             |
| Board ID | Rb          | V min  | V typ  | V max  | EC AD       |
| 0        | 0           |        | 0.000V | 0.300V | 0x00 - 0x0B |
| 1        | 12K +/- 1%  | 0.347V | 0.354V | 0.360V | 0x0C - 0x1C |
| 2        | 15K +/- 1%  | 0.423V | 0.430V | 0.438V | 0x1D - 0x26 |
| 3        | 20K +/- 1%  | 0.541V | 0.550V | 0.559V | 0x27 - 0x30 |
| 4        | 27K +/- 1%  | 0.691V | 0.702V | 0.713V | 0x31 - 0x3B |
| 5        | 33K +/- 1%  | 0.807V | 0.819V | 0.831V | 0x3C - 0x46 |
| 6        | 43K +/- 1%  | 0.978V | 0.992V | 1.006V | 0x47 - 0x54 |
| 7        | 56K +/- 1%  | 1.169V | 1.185V | 1.200V | 0x55 - 0x64 |
| 8        | 75K +/- 1%  | 1.398V | 1.414V | 1.430V | 0x65 - 0x76 |
| 9        | 100K +/- 1% | 1.634V | 1.650V | 1.667V | 0x77 - 0x87 |
| 10       | 130K +/- 1% | 1.849V | 1.865V | 1.881V | 0x88 - 0x96 |
| 11       | 160K +/- 1% | 2.015V | 2.031V | 2.046V | 0x97 - 0xA3 |
| 12       | 200K +/- 1% | 2.185V | 2.200V | 2.215V | 0xA4 - 0xAD |
| 13       | 240K +/- 1% | 2.316V | 2.329V | 2.343V | 0xAE - 0xB7 |
| 14       | 270K +/- 1% | 2.395V | 2.408V | 2.421V | 0xB8 - 0xC0 |
| 15       | 330K +/- 1% | 2.521V | 2.533V | 2.544V | 0xC1 - 0xC9 |
| 16       | 430K +/- 1% | 2.667V | 2.677V | 2.687V | 0xCA - 0xD3 |
| 17       | 560K +/- 1% | 2.791V | 2.800V | 2.808V | 0xD4 - 0xDC |
| 18       | 750K +/- 1% | 2.905V | 2.912V | 2.919V | 0xDD - 0xE6 |
| 19       | NC          | 3.000V | 3.300V |        | 0xE7 - 0xFF |



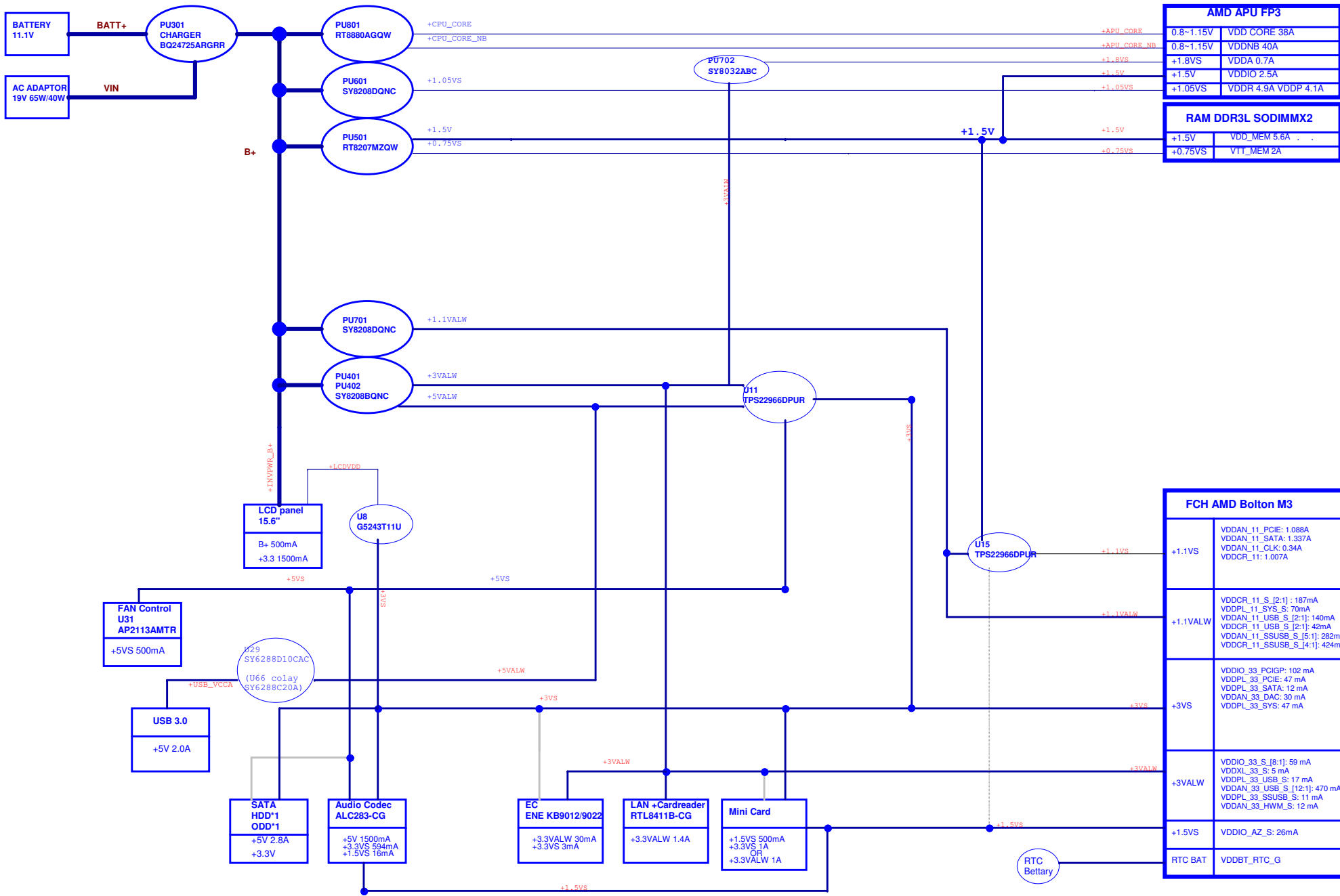
## BOARD ID Table

| Board ID | PCB Revision |
|----------|--------------|
| 10       | EVT          |
| 11       | PVT          |
| 12       | Pre MP       |
| 13       |              |
| 14       |              |
| 15       |              |
| 16       |              |
| 17       |              |

## BOM Option Table

| BOM Structure | Description                        |
|---------------|------------------------------------|
| 9022@         | Use EC 9022                        |
| 9012@         | Use EC 9012                        |
| UMA@          | Display output from APU (UMA only) |
| BL@           | KB Backlight                       |
| AL@           | Use Auto load EC code function     |
| AC@           | Support AC Function                |
| NOAC@         | No Support AC Function             |
| TPM@          | Support D TPM function             |
| CONN@         | Connector (Control by ME)          |
| HDT@          | Debug Connector                    |
| EMC@          | EMC Component                      |
| XEMC@         | Reservec for EMC                   |
| TPSM@         | Use APU SMBus for T/P              |
| TPBRI@        | Use USB to I2C IC for T/P          |
| USBTP@        | Use USB T/P                        |
| MOS@          | Use MOSART solution USB to I2C TP  |
| @             | Unpop                              |

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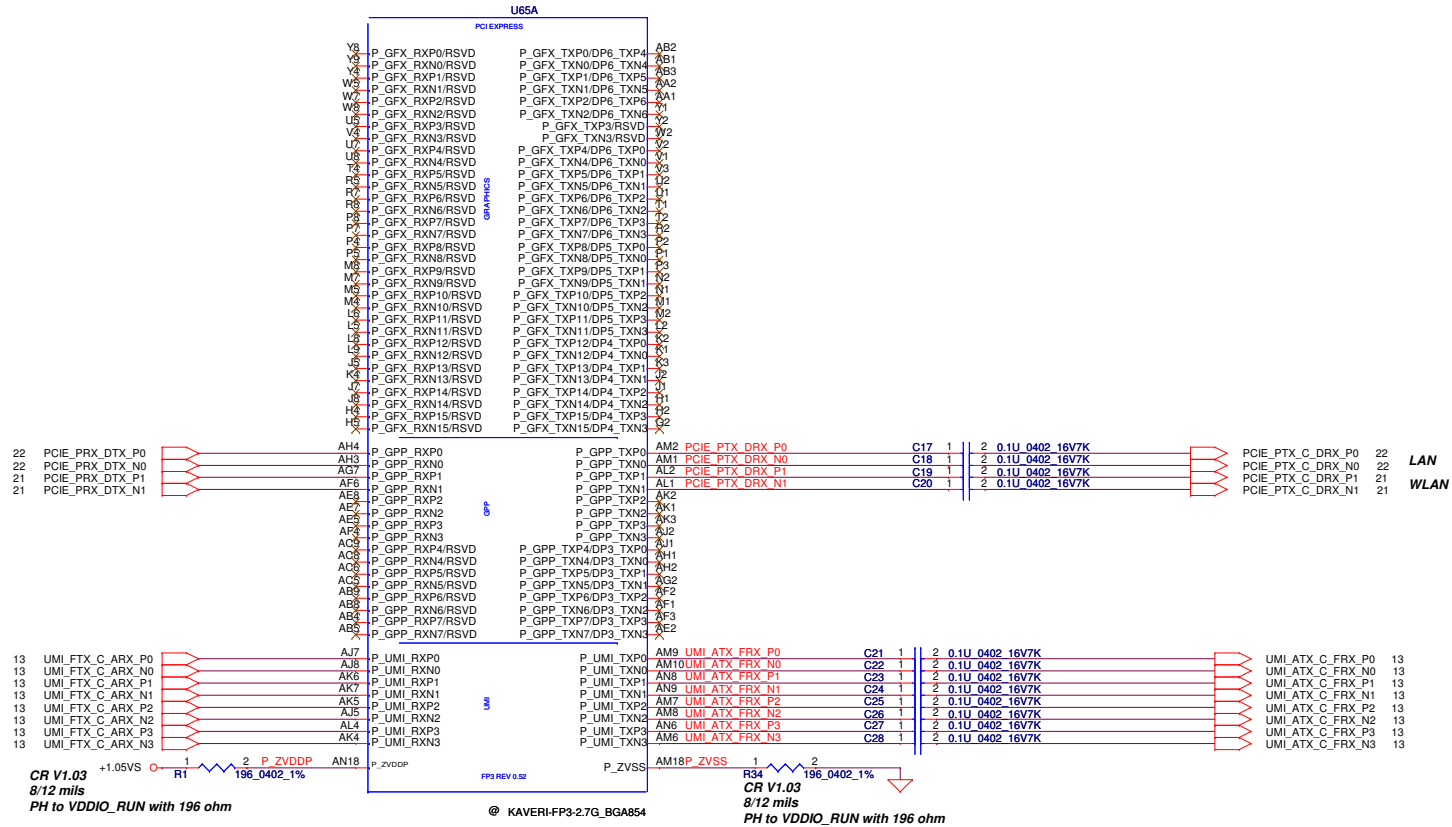


| AMD APU FP3 |                     |
|-------------|---------------------|
| 0.8-1.15V   | VDD CORE 38A        |
| 0.8-1.15V   | VDDNB 40A           |
| +1.8VS      | VDDA 0.7A           |
| +1.5V       | VDDIO 2.5A          |
| +1.05VS     | VDDR 4.9A VDDP 4.1A |

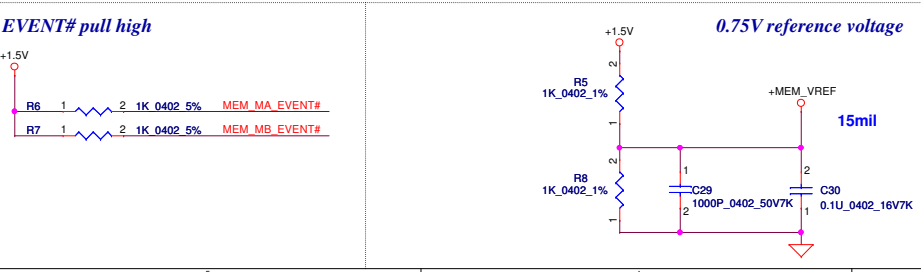
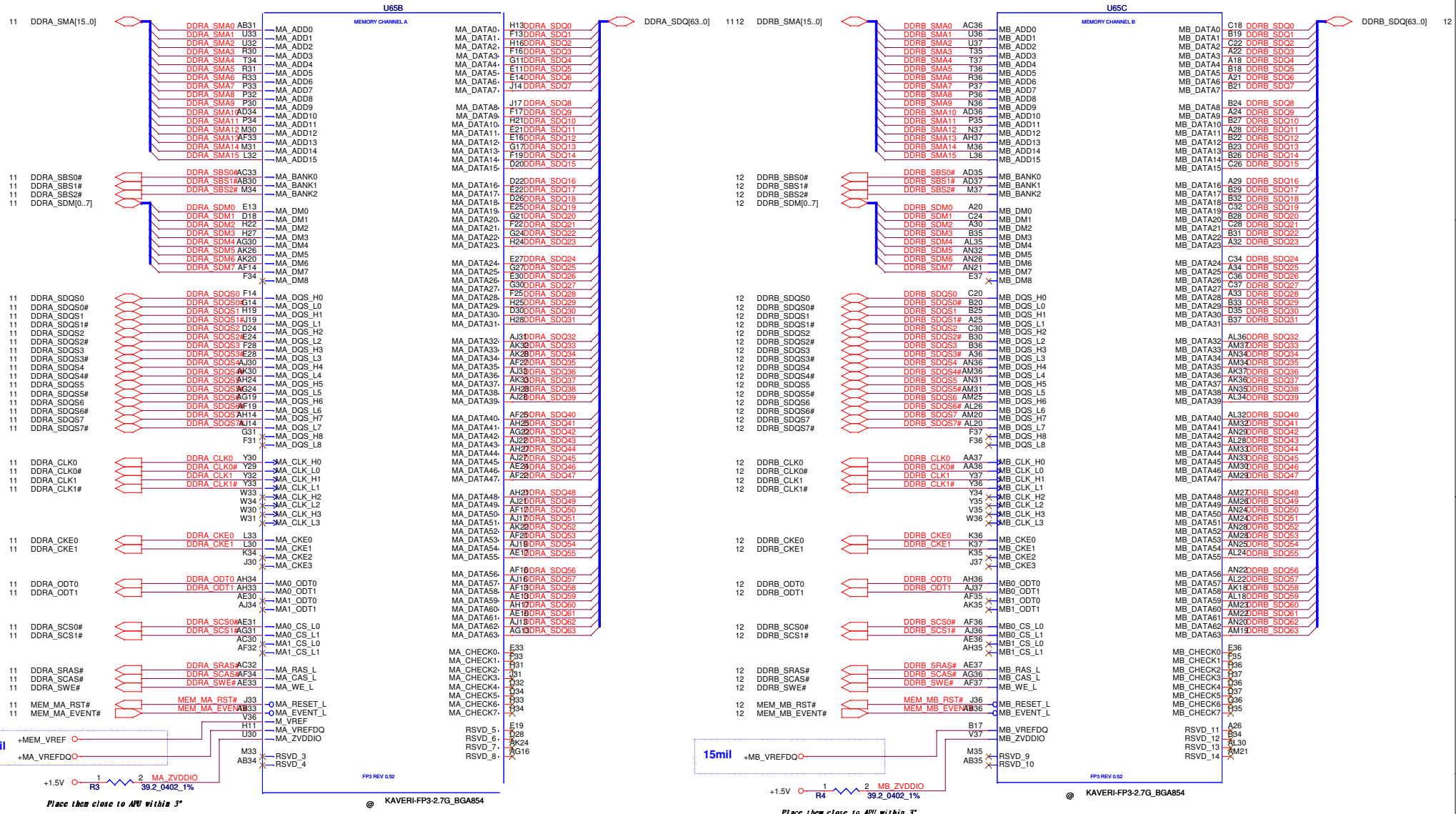
  

| RAM DDR3L SODIMM X2 |              |
|---------------------|--------------|
| +1.5V               | VDD_MEM 5.6A |
| +0.75VS             | VTT_MEM 2A   |

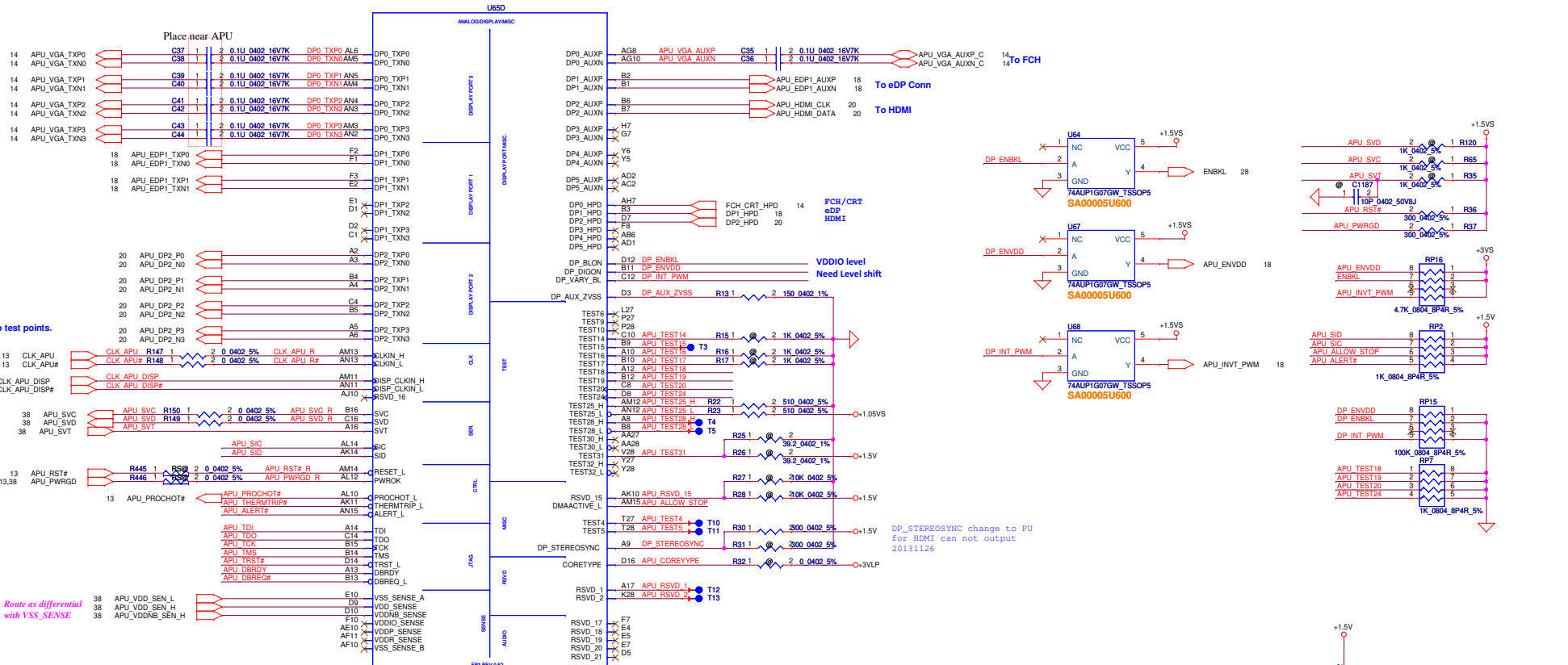
| FCH AMD Bolton M3 |   |
|-------------------|---|
| +1.1VS            | VDDAN_11_PCIE: 1.088A<br>VDDAN_11_SATA: 1.337A<br>VDDAN_11_CLK: 0.34A<br>VDDCR_11: 1.007A   |
| +1.1VALW          | VDDCR_11_S_1[2:1]: 187mA<br>VDDPL_11_SYS_S: 70mA<br>VDDAN_11_USB_S_1[2:1]: 140mA<br>VDDCR_11_USB_S_1[2:1]: 42mA<br>VDDAN_11_SSUSB_S_1[5:1]: 282mA<br>VDDCR_11_SSUSB_S_1[4:1]: 424mA |
| +3VS              | VDDIO_33_PCIE: 102 mA<br>VDDPL_33_PCIE: 47 mA<br>VDDPL_33_SATA: 12 mA<br>VDDAN_33_DAC: 30 mA<br>VDDPL_33_SYS: 47 mA   |
| +3VALW            | VDDIO_33_S_1[8:1]: 59 mA<br>VDDXL_33_S: 5 mA<br>VDDPL_33_USB_S: 17 mA<br>VDDAN_33_USB_S_1[12:1]: 470 mA<br>VDDPL_33_SSUSB_S: 11 mA<br>VDDAN_33_HWM_S: 12 mA                         |
| +1.5VS            | VDDIO_AZ_S: 26mA  |
| RTC BAT           | VDDBT_RTC_G   |



|   |                    |                 |                          |  |
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|   |                    |                 |                          | FP3 PCIE/UMI                                 |
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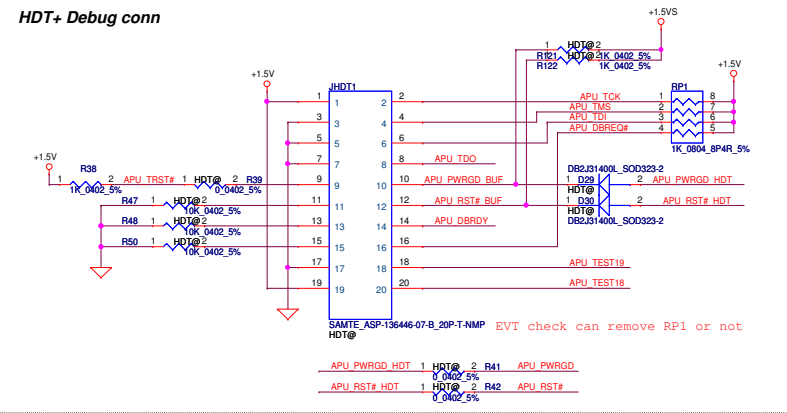
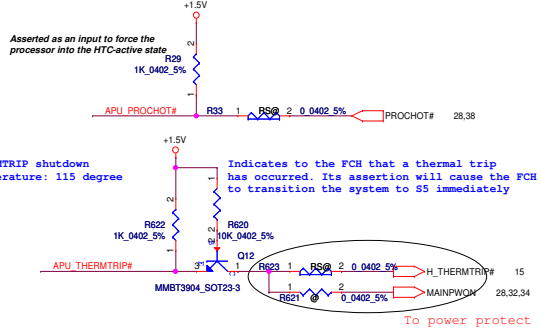
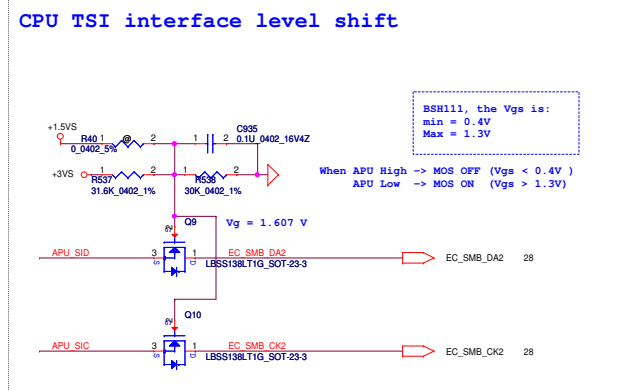
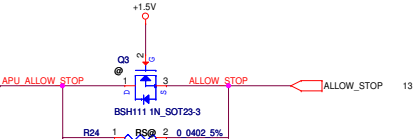
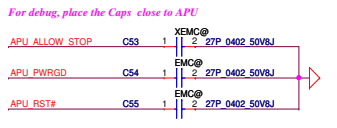
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CLK net has no test points.

Route as differential with VSS\_SENSE

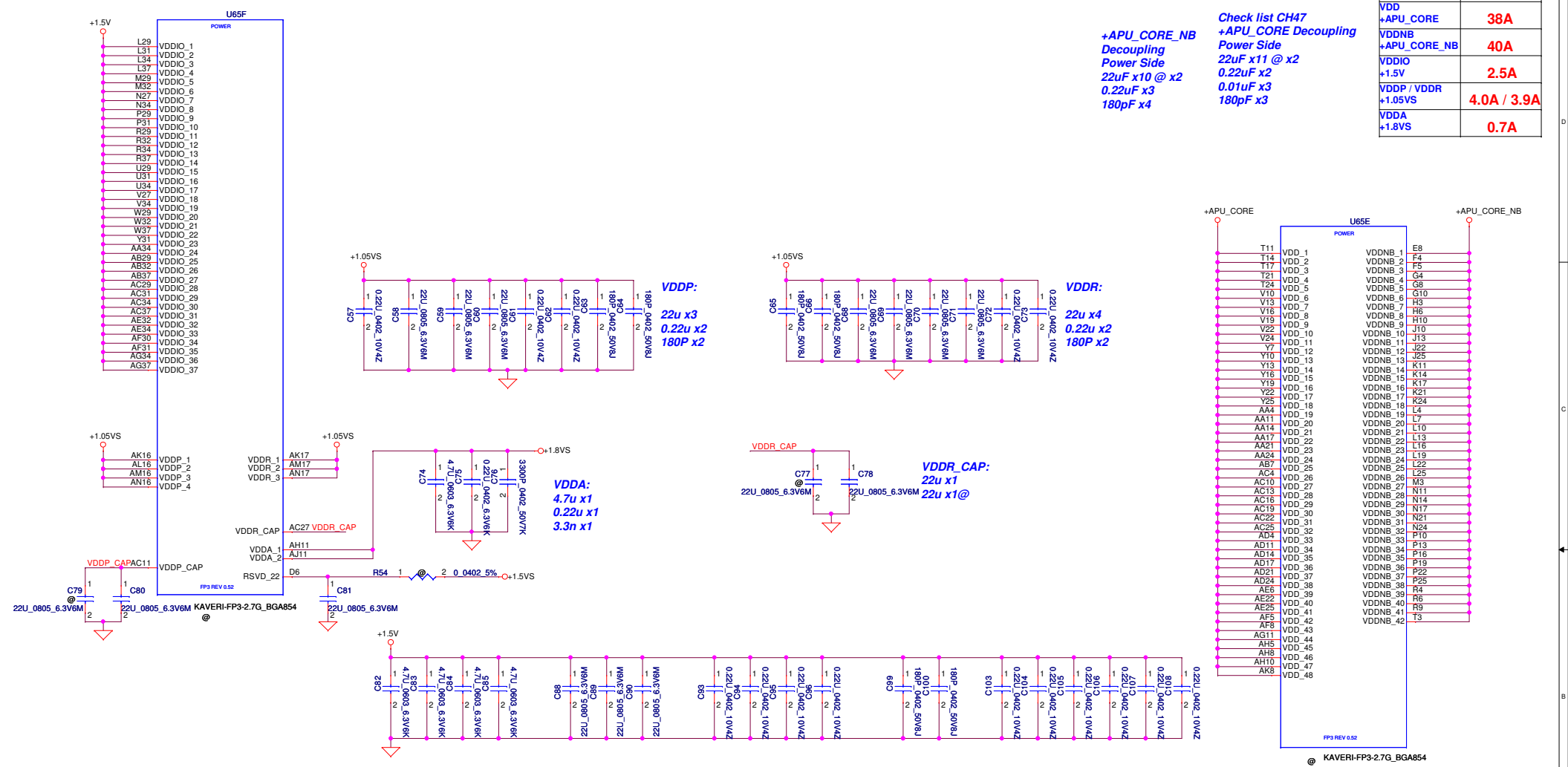
DP\_STEREBOSYNC change to PU for HDMI can not output 20131126



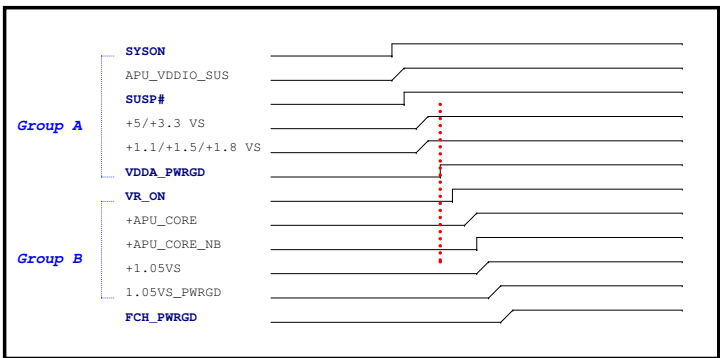
| Power Name             | Consumption |
|------------------------|-------------|
| VDD<br>+APU_CORE       | 38A         |
| VDDNB<br>+APU_CORE_NB  | 40A         |
| VDDIO<br>+1.5V         | 2.5A        |
| VDDP / VDDR<br>+1.05VS | 4.0A / 3.9A |
| VDDA<br>+1.8VS         | 0.7A        |

**+APU\_CORE\_NB  
Decoupling  
Power Side**  
 22uF x10 @ x2  
 0.22uF x3  
 180pF x4

**Check list CH47  
+APU\_CORE Decoupling  
Power Side**  
 22uF x11 @ x2  
 0.22uF x2  
 0.01uF x3  
 180pF x3

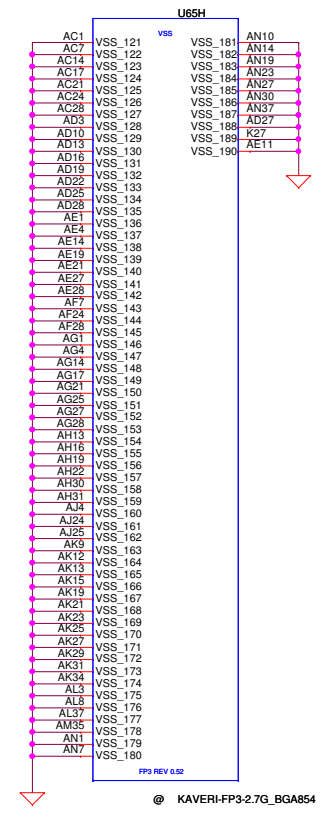
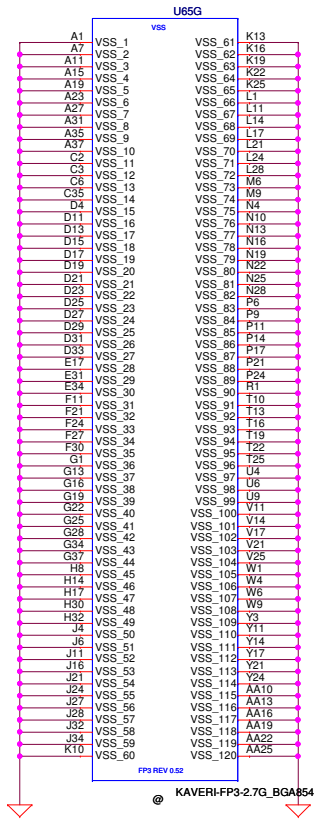


APU sequence : GROUP A need ramp before GROUP B



|   |                    |                 |            |                                |               |
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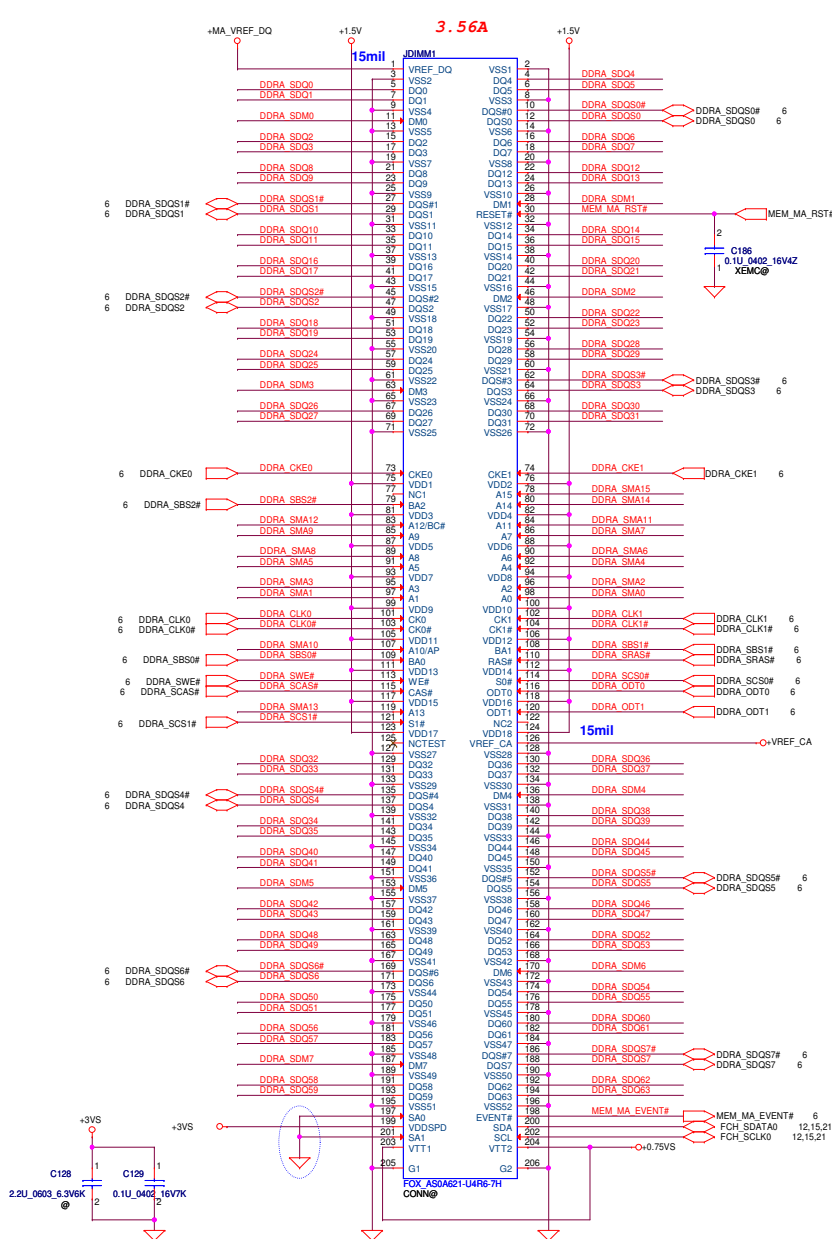
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Panel ENBKL

Panel ENVDD

Panel PWM

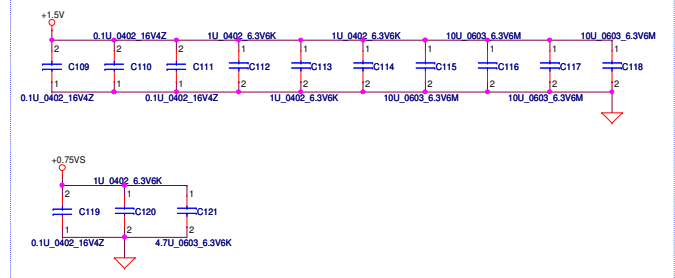
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| Issued Date   | 2011/07/08 | Deciphered Date    | 2015/07/08 | AMD FS1R2 Singal Level Shifter |                    |
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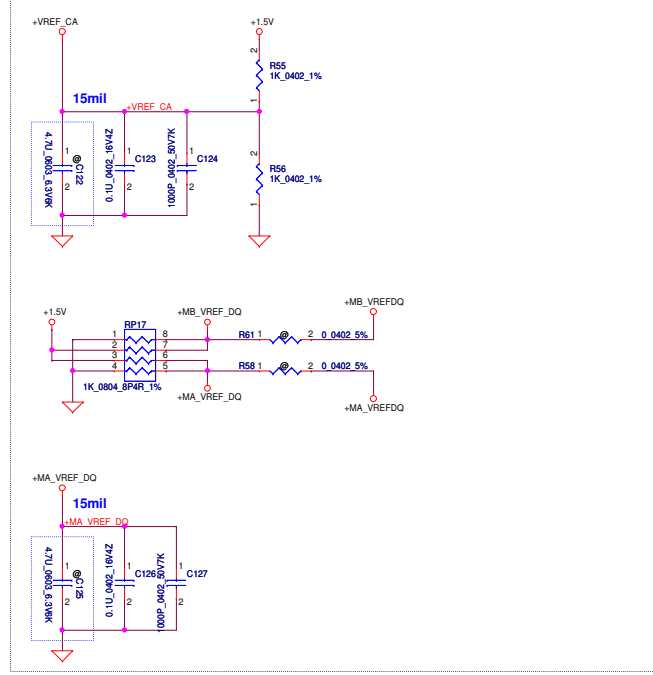
**DIMM\_A STD H:9.2mm**  
 <Address: 00>

- DDRA\_SDO0(0.63) ⇨ DDRA\_SDO(0.63) 6
- DDRA\_SDM(0.7) ⇨ DDRA\_SDM(0.7) 6
- DDRA\_SMA(0.15) ⇨ DDRA\_SMA(0.15) 6

**Place near DIMM1**

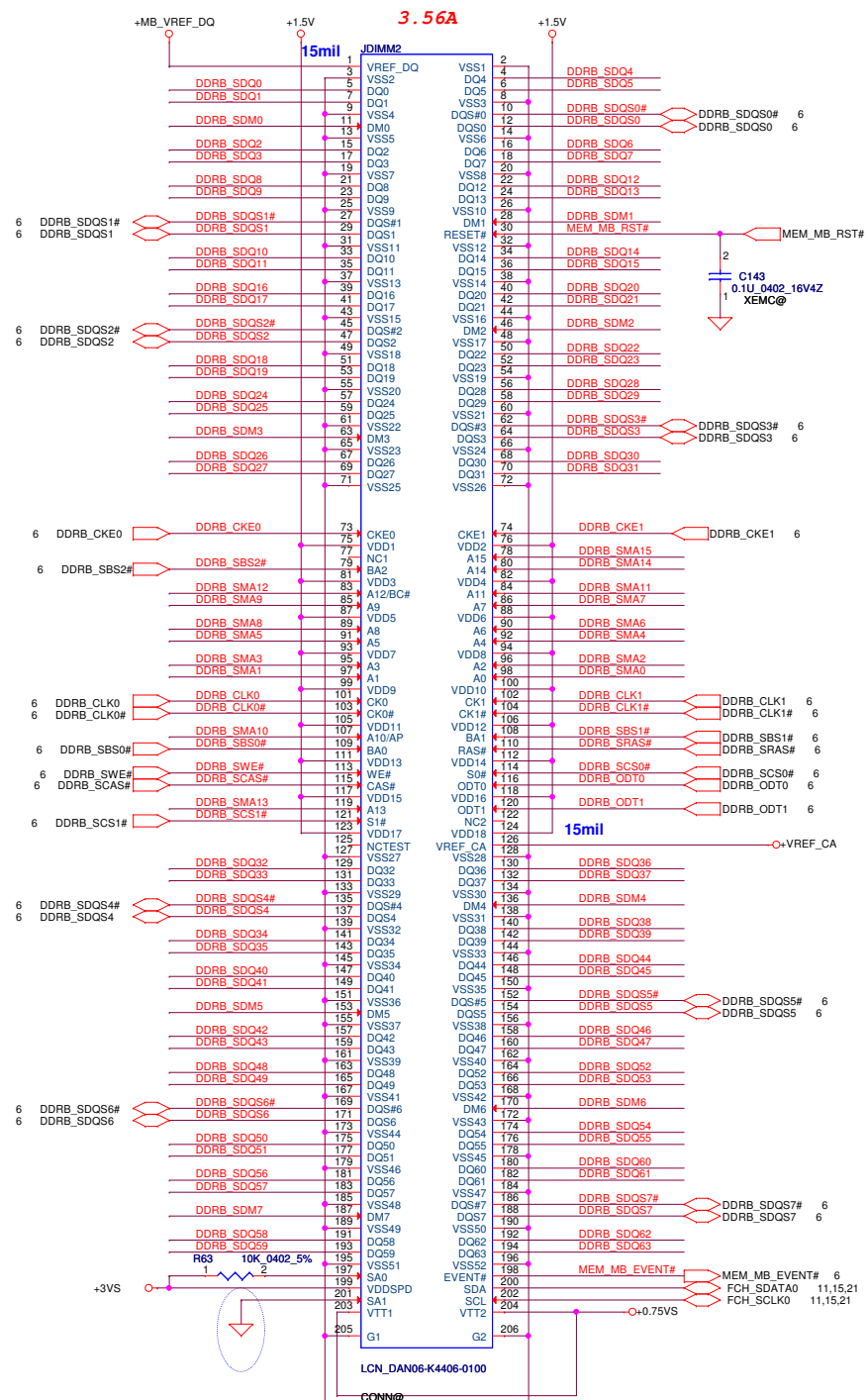


**Follow CRB design**

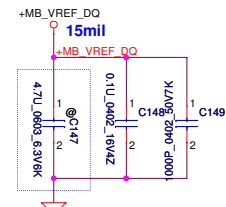
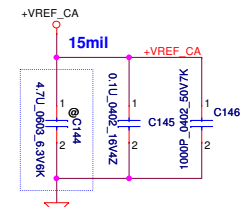
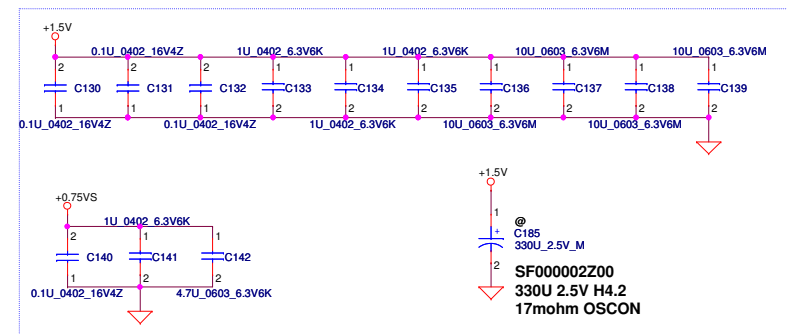


follow CRB design

|   |                          |                 |                          |     |     |
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| Size  | C                        | Document Number | Z5WAK M/B LA-B222P       | Rev | 1.0 |
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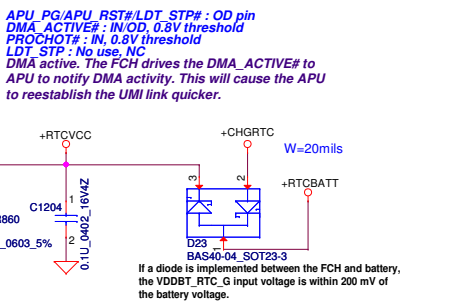
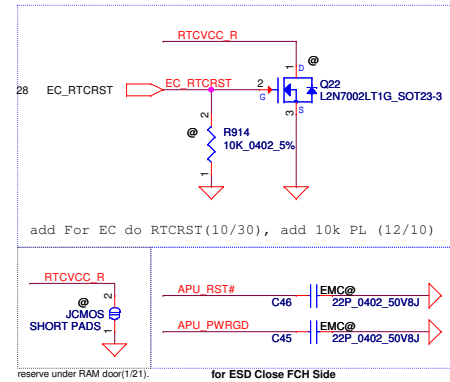
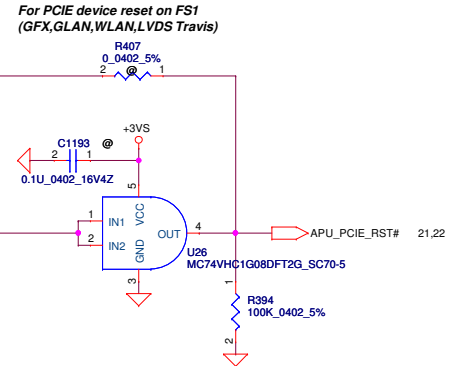
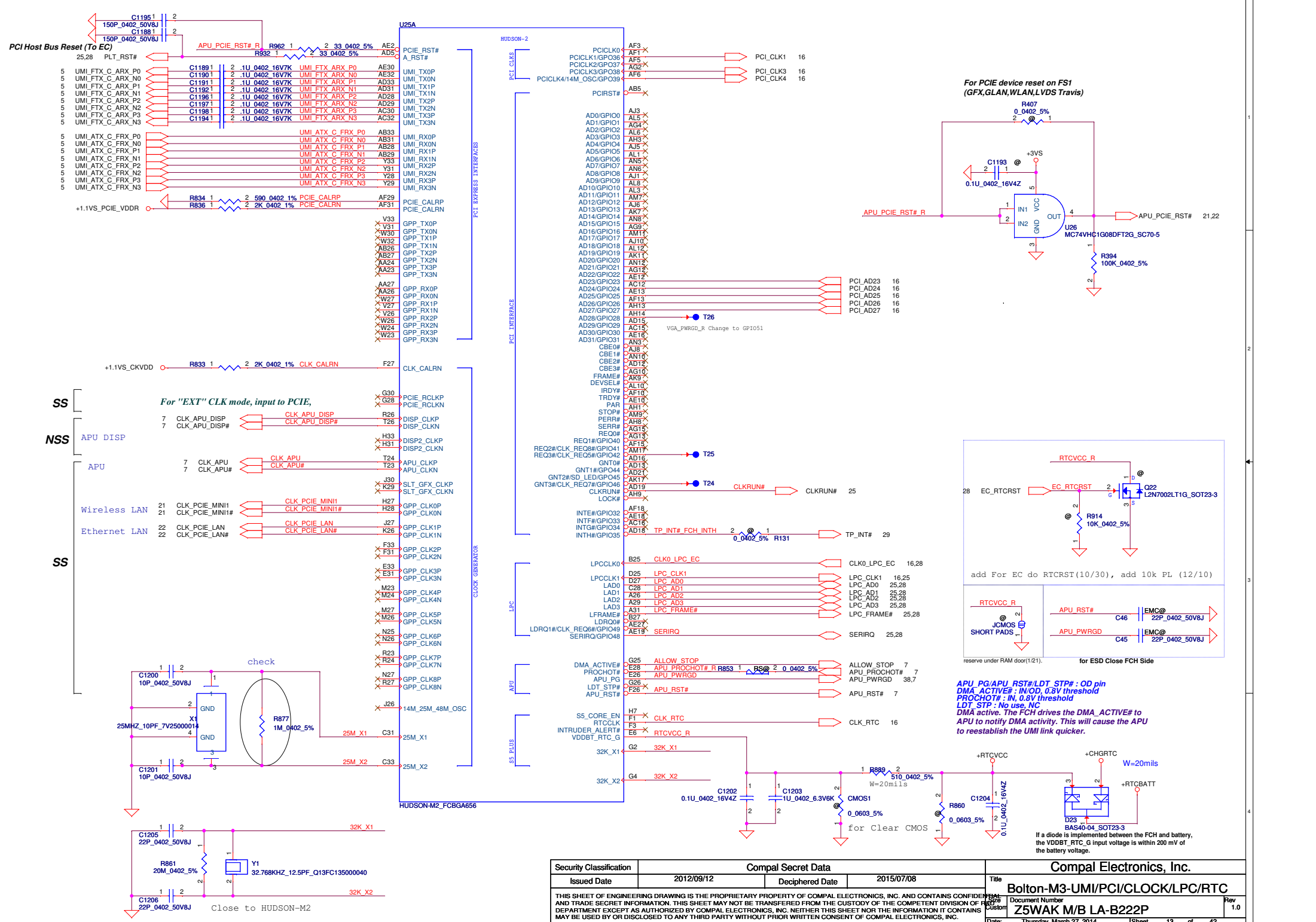


Place near DIMM2

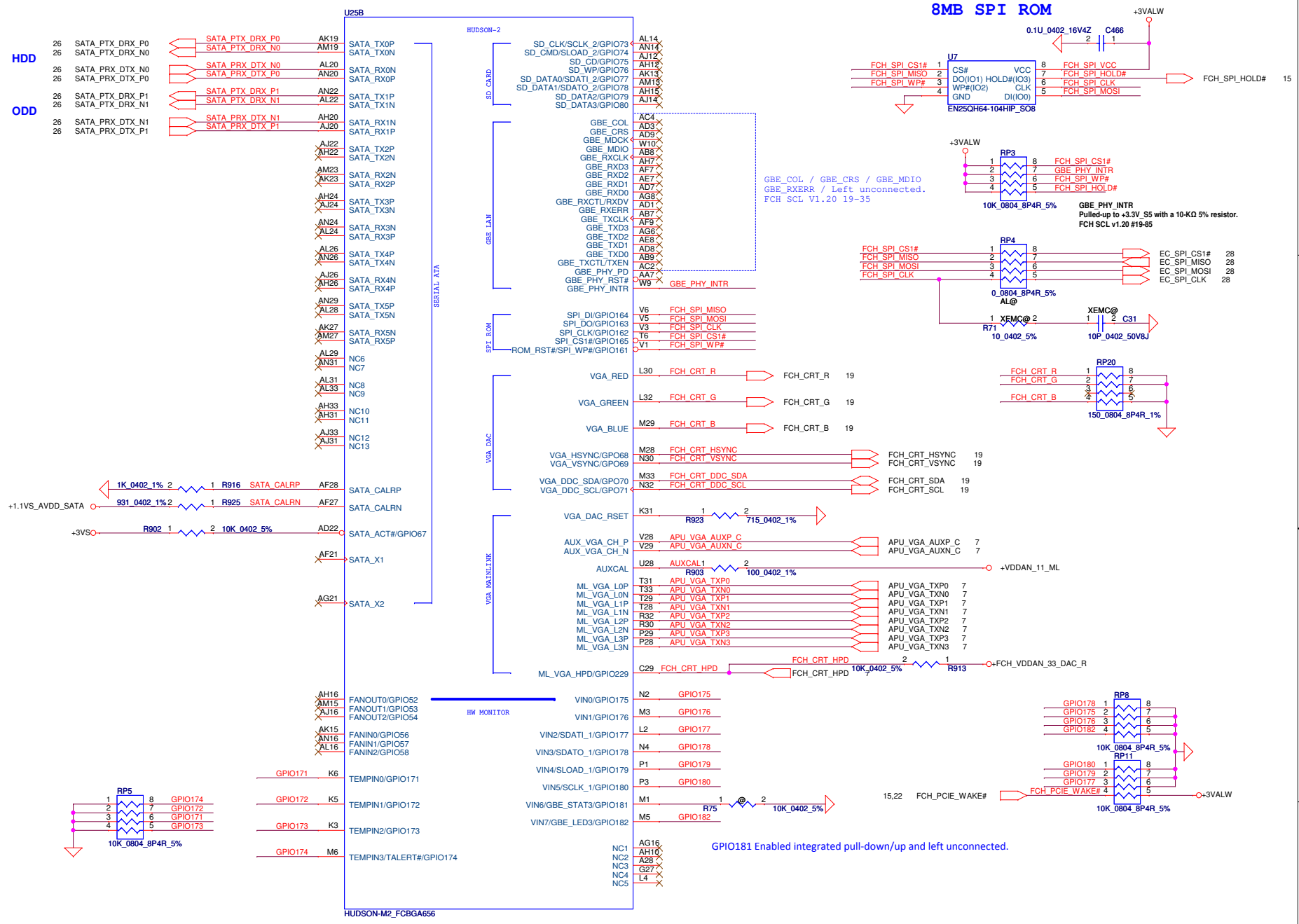


**DIMM\_B STD H:5.2mm**  
 <Address: 01>

|  |                    |                 |                          |   |
|--|--------------------|-----------------|--------------------------|---|
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|  |                    |                 |                          | Rev 1.0<br>Page 13 of 42  |

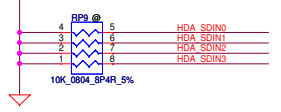
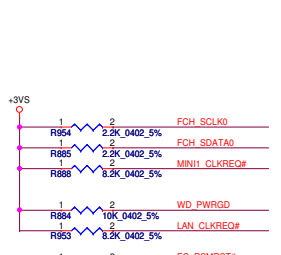
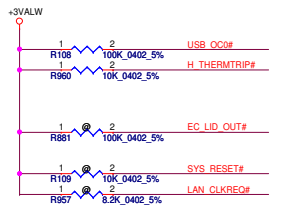


|   |                    |                 |                          |                           |
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|   |                    |                 |                          | <b>Z5WAK M/B LA-B222P</b> |
| Date: Thursday, March 27, 2014  |                    |                 |                          | Sheet 14 of 42            |

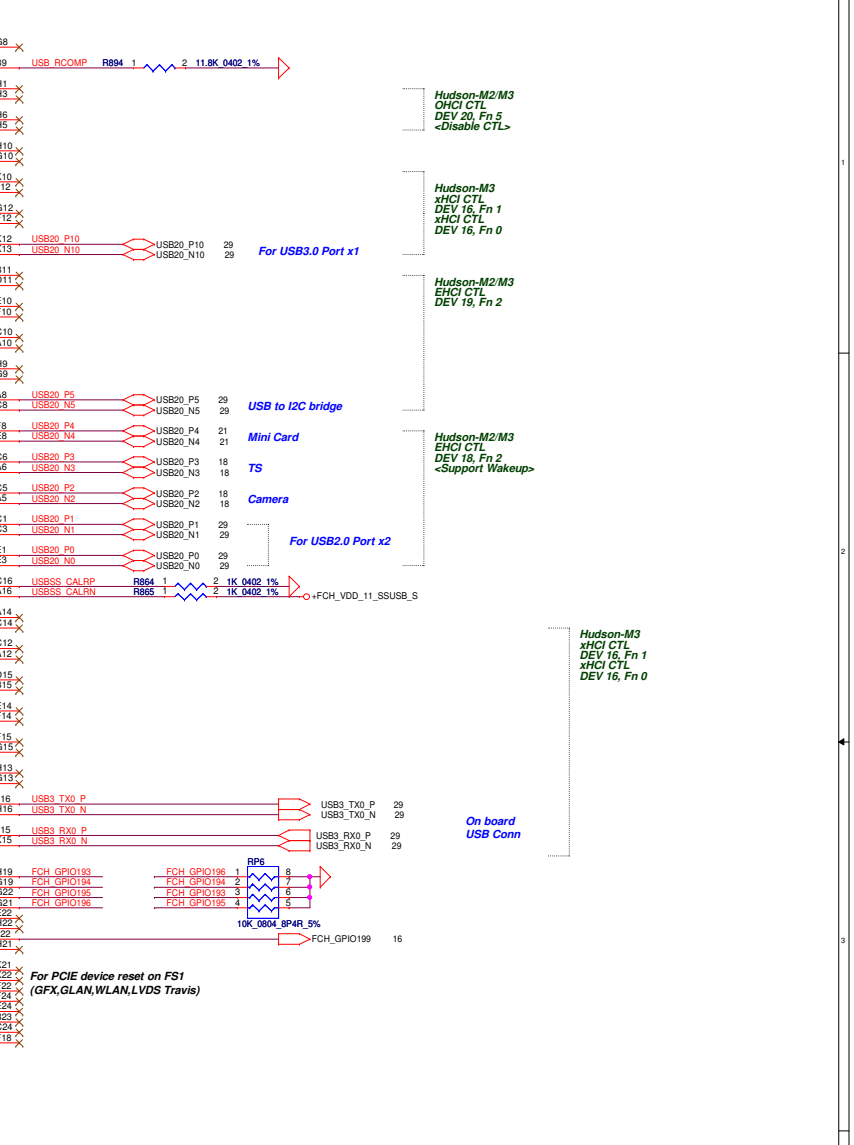
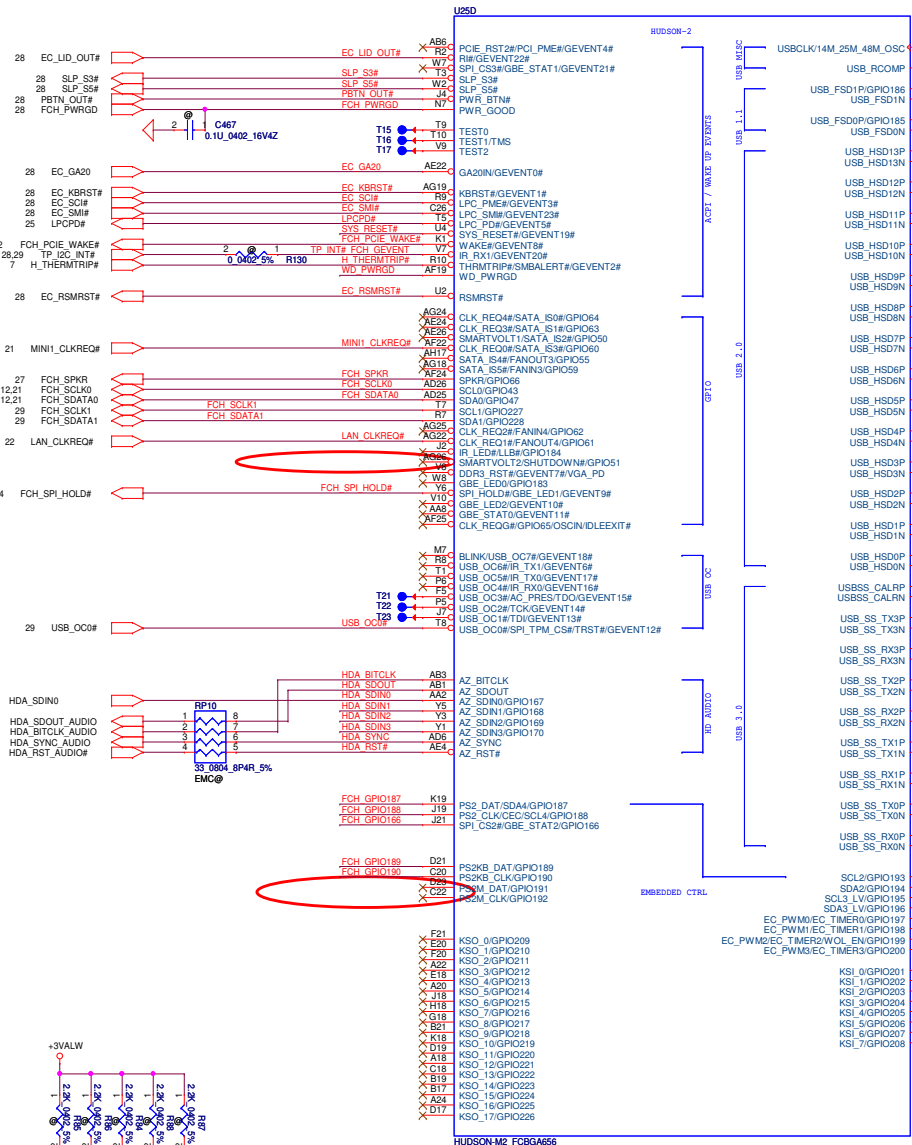
**THERMTRIP:**  
Need level shift from +3VALW to +1.5V  
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0-->S0 PWR domain  
SM bus 1-->S5 PWR domain

PH on TP side



| Project SKU ID    | Value     |
|-------------------|-----------|
| GPIO189 (use VGA) | Low (UMA) |
| GPIO190           |           |
| GPIO188           |           |
| GPIO187           |           |
| GPIO166           |           |



Hudson-M2/M3  
OHCI CTL  
DEV 20, Fn 5  
-<Disable CTL>

Hudson-M3  
xHCI CTL  
DEV 16, Fn 1  
xHCI CTL  
DEV 16, Fn 0

Hudson-M2/M3  
EHCI CTL  
DEV 19, Fn 2

Hudson-M2/M3  
EHCI CTL  
DEV 16, Fn 2  
-<Support Wakeup>

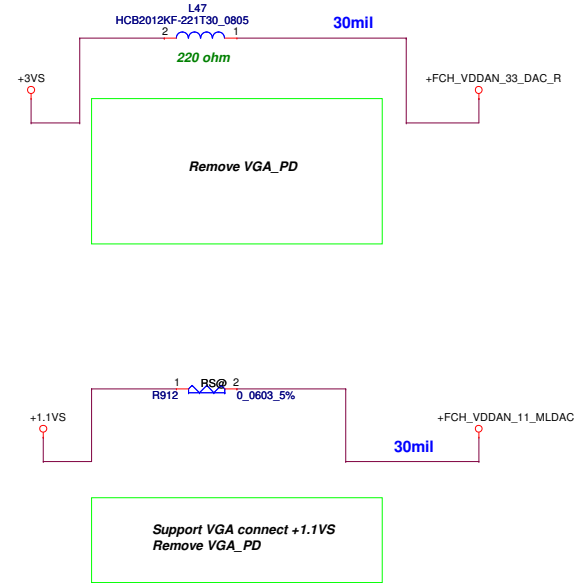
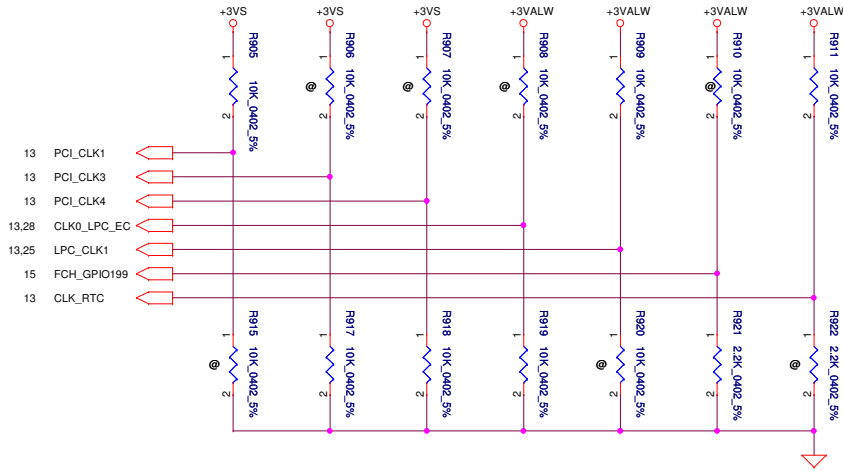
Hudson-M3  
xHCI CTL  
DEV 16, Fn 1  
xHCI CTL  
DEV 16, Fn 0

On board  
USB Conn

For PCIe device reset on FS1  
(GFX, GLAN, WLAN, LVDS Travis)

# STRAP PINS

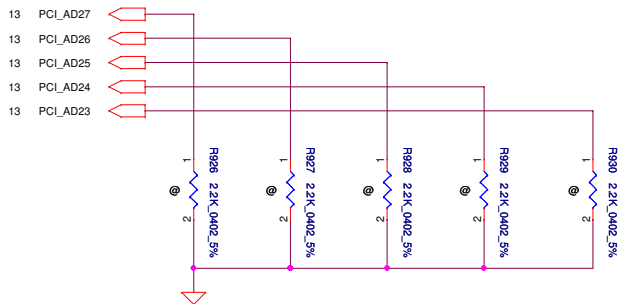
|                  | PCI_CLK1                          | PCI_CLK3                             | PCI_CLK4                            | LPC_CLK0                          | LPC_CLK1                         | FCH_GPIO199               | CLK_RTC                                 |
|------------------|-----------------------------------|--------------------------------------|-------------------------------------|-----------------------------------|----------------------------------|---------------------------|---|
| <b>PULL HIGH</b> | ALLOW PCIE GEN2<br><b>DEFAULT</b> | USE DEBUG STRAPS                     | NON_FUSION CLOCK MODE               | FCH EC ENABLED                    | CLKGEN ENABLED<br><b>DEFAULT</b> | LPC ROM                   | S5 PLUS MODE DISABLED<br><b>DEFAULT</b> |
| <b>PULL LOW</b>  | FORCE PCIE GEN1                   | IGNORE DEBUG STRAP<br><b>DEFAULT</b> | FUSION CLOCK MODE<br><b>DEFAULT</b> | FCH EC DISABLED<br><b>DEFAULT</b> | CLKGEN DISABE                    | SPI ROM<br><b>DEFAULT</b> | S5 PLUS MODE ENABLED                    |



# DEBUG STRAPS

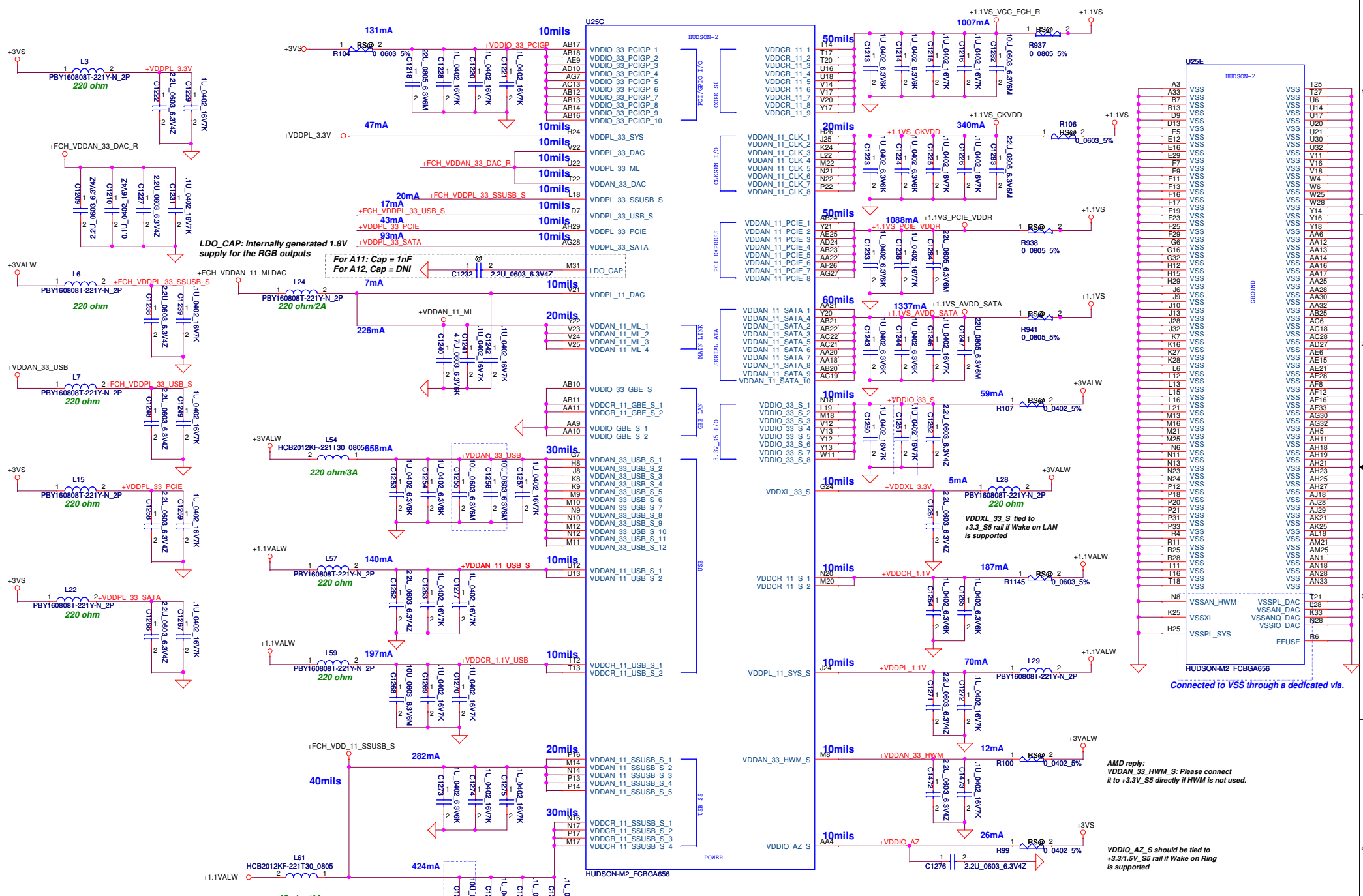
FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

|                  | PCI_AD27                      | PCI_AD26                   | PCI_AD25                                    | PCI_AD24                                  | PCI_AD23                               |
|------------------|-------------------------------|----------------------------|---|---|--|
| <b>PULL HIGH</b> | USE PCI PLL<br><b>DEFAULT</b> | RESERVED<br><b>DEFAULT</b> | NORMAL REFCLK TERMINATION<br><b>DEFAULT</b> | USE DEFAULT PCIE STRAPS<br><b>DEFAULT</b> | DISABLE PCI MEM BOOT<br><b>DEFAULT</b> |
| <b>PULL LOW</b>  | BYPASS PCI PLL                | RESERVED                   | INVERT REFCLK TERMINATION                   | USE EEPROM PCIE STRAPS                    | ENABLE PCI MEM BOOT                    |



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|  |                    |                 |                          | Rev 1.0                        |
|  |                    |                 |                          | Date: Thursday, March 27, 2014 |
|  |                    |                 |                          | Sheet 16 of 42                 |



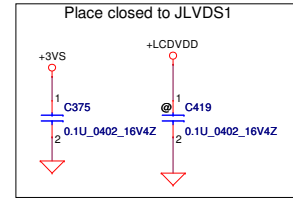
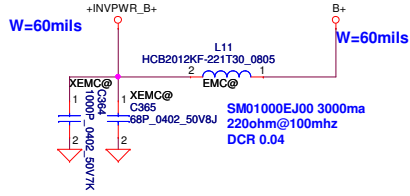
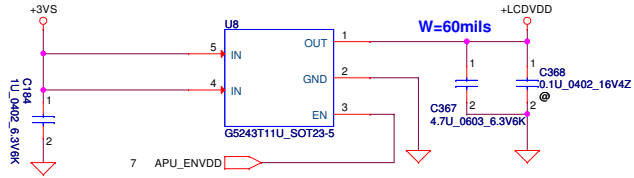


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| Date:   | Thursday, March 27, 2014 | Sheet           | 17 of 42   |

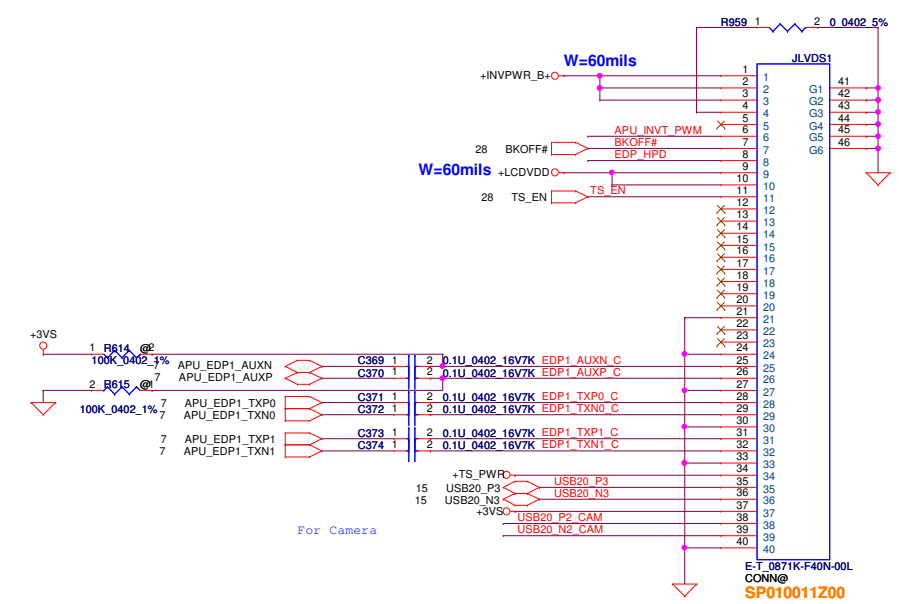
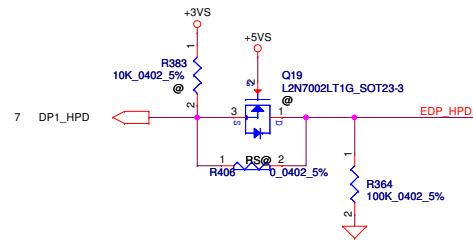
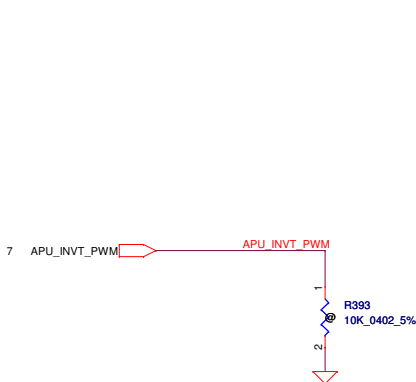
**Compal Electronics, Inc.**

**Hudson-M2/M3-POWER/GND**

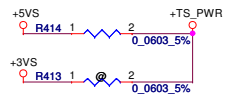
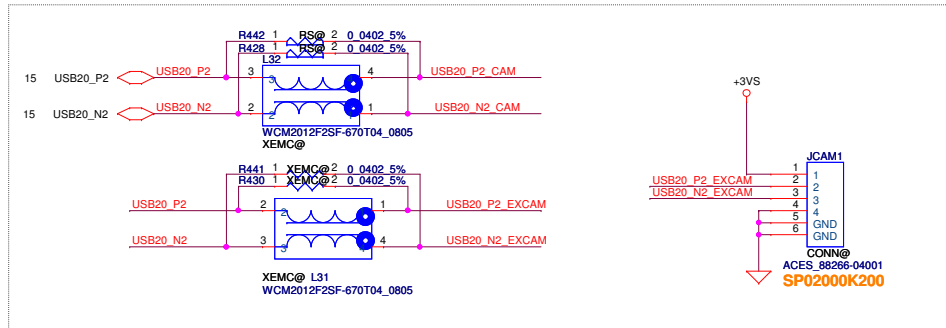
# LCD POWER CIRCUIT



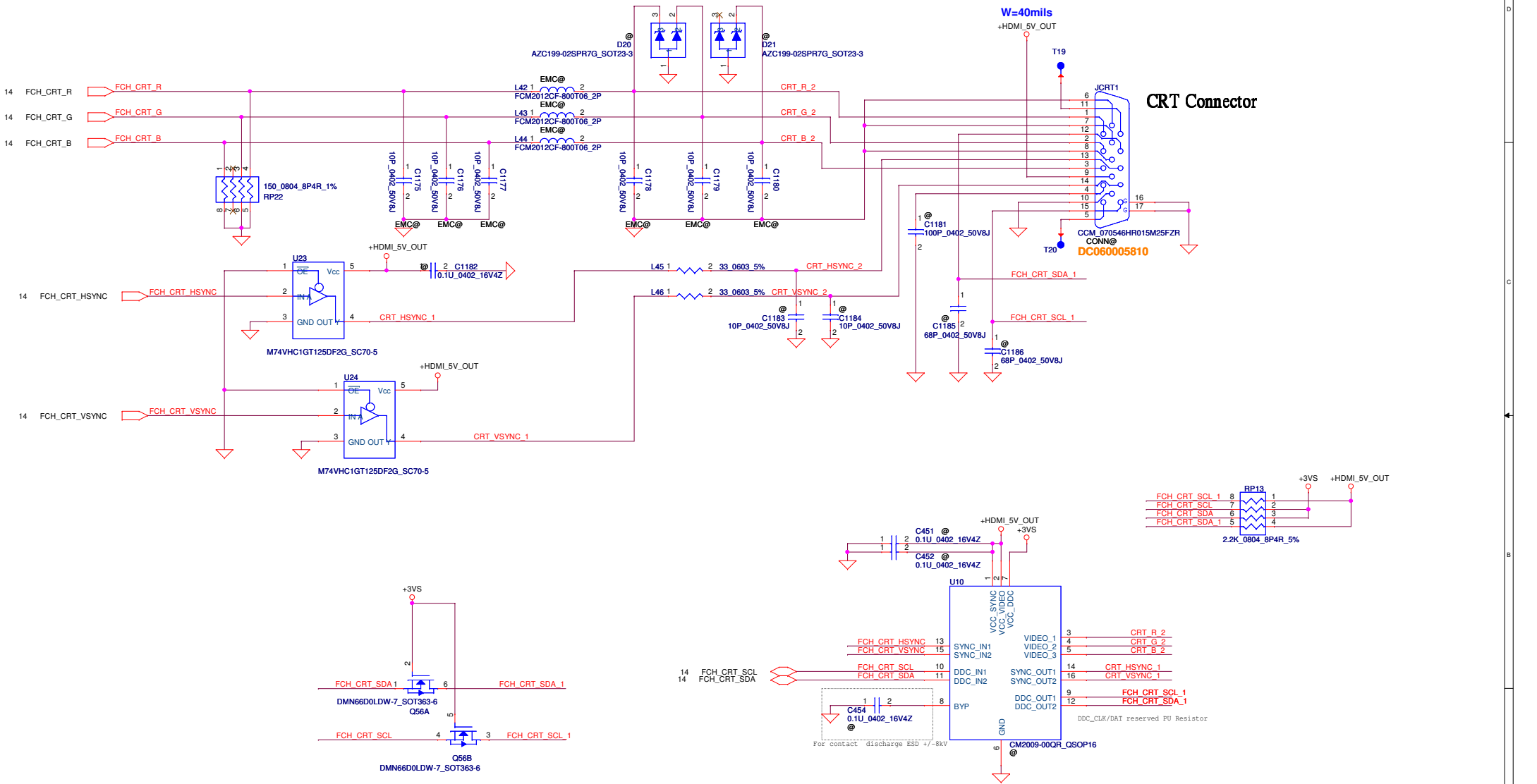
## LCD/ LED PANEL Conn.



### CMOS co-layout 4pin conn & eDP conn

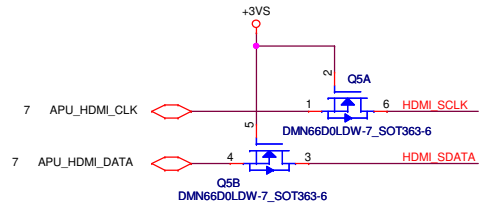
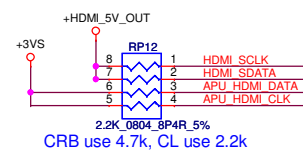
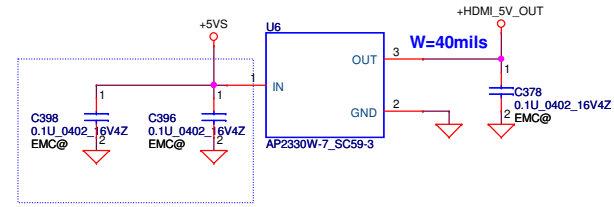
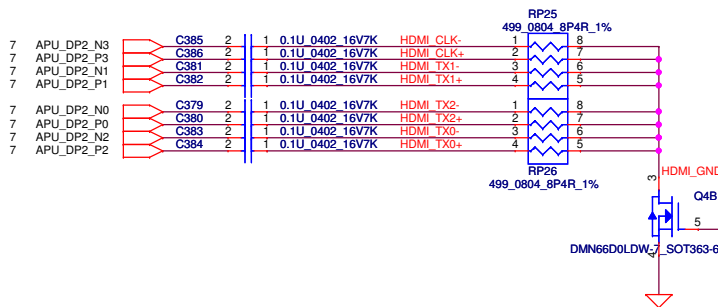


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|  |            |                    |            | Z5WAK M/B LA-B222P             | 1.0            |
|  |            |                    |            | Date: Thursday, March 27, 2014 | Sheet 18 of 42 |

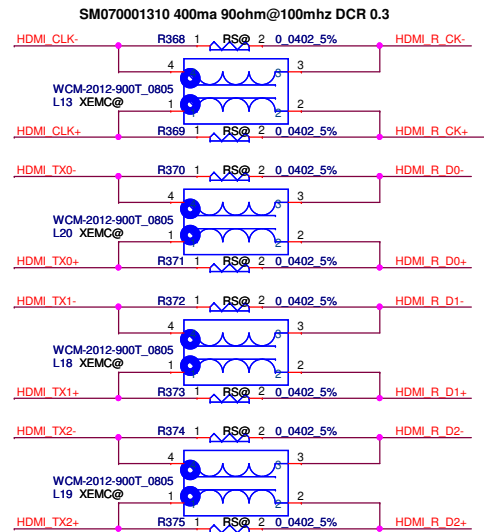
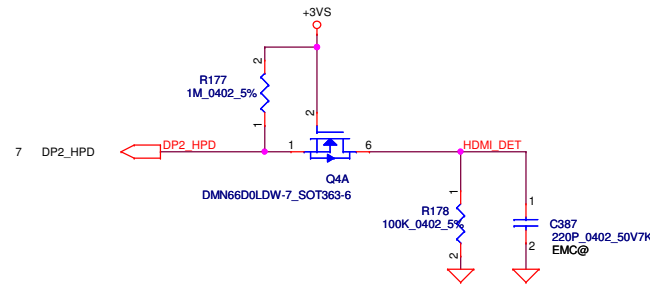


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|  |                    |                 |                          | <b>CRT Connector.</b>  |
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|  |                    |                 |                          | Rev<br><b>1.0</b><br>Sheet 19 of 42  |

EVT : Check List CH41 - 665 1%  
change to 500 ohm 12/27 (interlock V1.2)

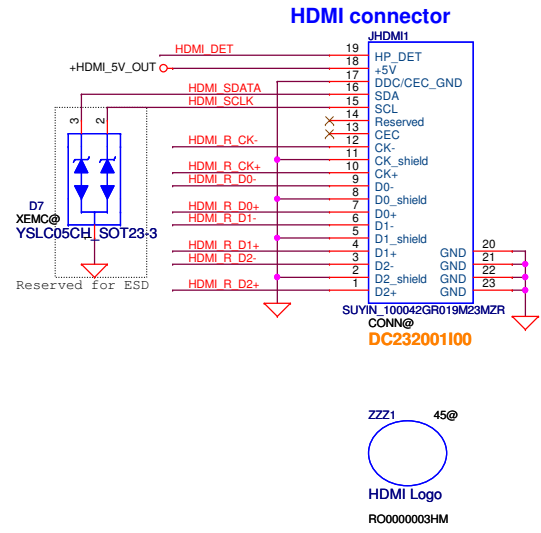


Reserved for ESD



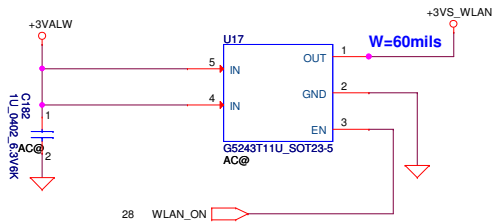
|            |   |   |                |
|------------|---|---|----------------|
| HDMI R_CK- | 1 | 2 |                |
| XEMC@ C585 |   |   | 10P_0402_50V8J |
| HDMI R_CK+ | 1 | 2 | 10P_0402_50V8J |
| XEMC@ C566 |   |   | 10P_0402_50V8J |
| HDMI R_D0- | 1 | 2 | 10P_0402_50V8J |
| XEMC@ C568 |   |   | 10P_0402_50V8J |
| HDMI R_D0+ | 1 | 2 | 10P_0402_50V8J |
| XEMC@ C569 |   |   | 10P_0402_50V8J |
| HDMI R_D1- | 1 | 2 | 10P_0402_50V8J |
| XEMC@ C571 |   |   | 10P_0402_50V8J |
| HDMI R_D1+ | 1 | 2 | 10P_0402_50V8J |
| XEMC@ C572 |   |   | 10P_0402_50V8J |
| HDMI R_D2- | 1 | 2 | 10P_0402_50V8J |
| XEMC@ C579 |   |   | 10P_0402_50V8J |
| HDMI R_D2+ | 1 | 2 | 10P_0402_50V8J |
| XEMC@ C580 |   |   | 10P_0402_50V8J |

Reserve for EMI 10/09

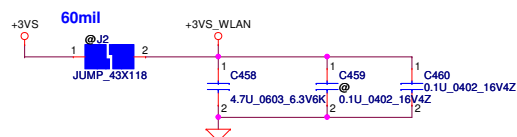
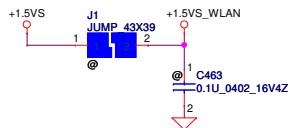
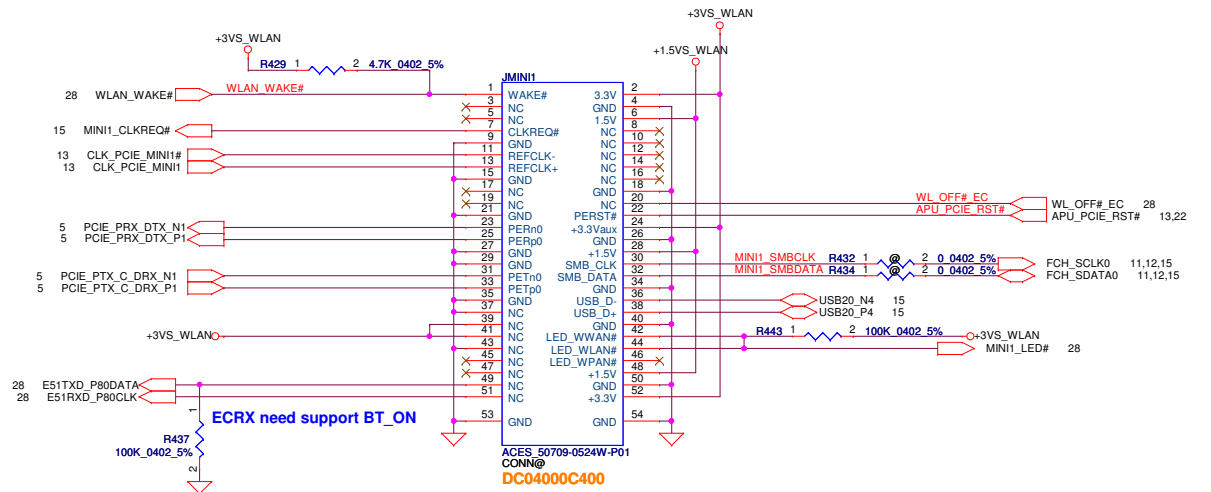


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|   |            |                    |            | Custom                   | 1.0                      |
|   |            |                    |            | Date:                    | Thursday, March 27, 2014 |
|   |            |                    |            | Sheet                    | 20 of 42                 |

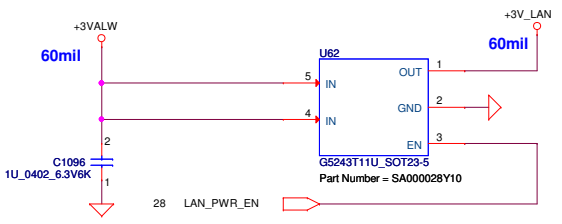
# Mini-Express Card for WLAN/WiMAX(Half)



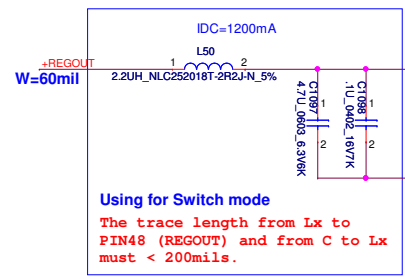
## Mini-Express Card(WLAN) Mini Card Power Rating



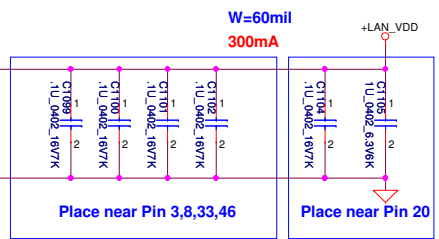
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| Security Classification  |            | Compal Secret Data |            | Compal Electronics, Inc. |                          |
| Issued Date  | 2012/09/12 | Deciphered Date    | 2012/07/29 | Title                    | MINI Card                |
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|  |            |                    |            | Date                     | Thursday, March 27, 2014 |
|  |            |                    |            | Sheet                    | 21 of 42                 |
|  |            |                    |            | Rev                      | 1.0                      |



**From EC**  
 High active.  
 EN threshold voltage min:1.2V typ:1.6V max:2.0V  
 Current limit threshold 1.5-2.8A  
**+3V\_LAN Rising time must >0.5ms and <100ms**

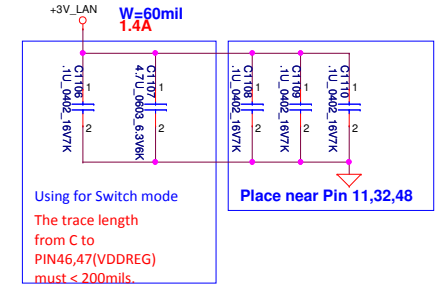


Using for Switch mode  
 The trace length from Lx to PIN48 (REGOUT) and from C to Lx must < 200mils.



Place near Pin 3,8,33,46

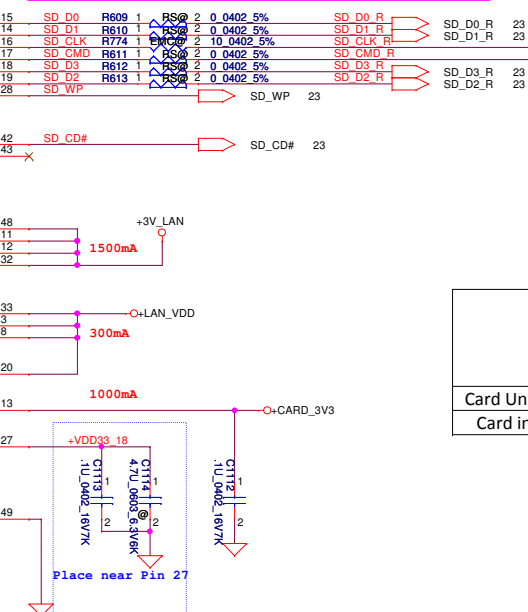
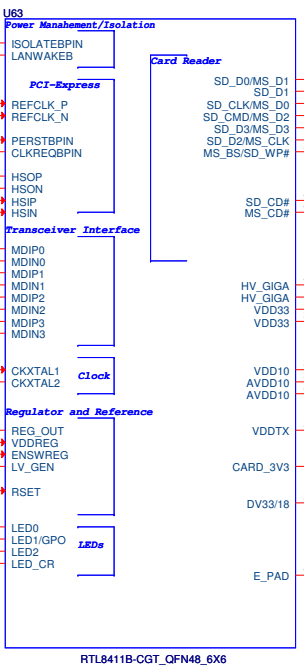
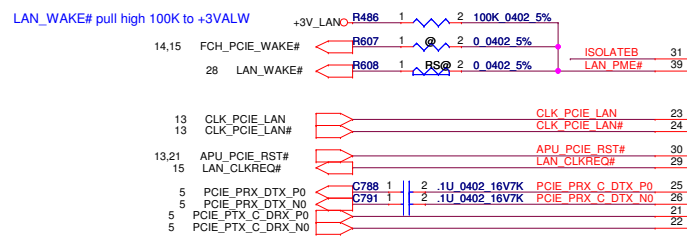
Place near Pin 20



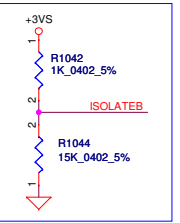
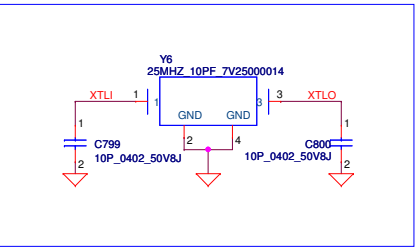
Using for Switch mode  
 The trace length from C to PIN46,47(VDDREG) must < 200mils.

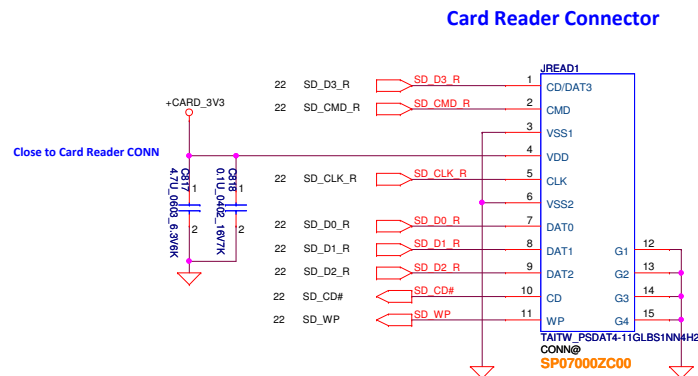
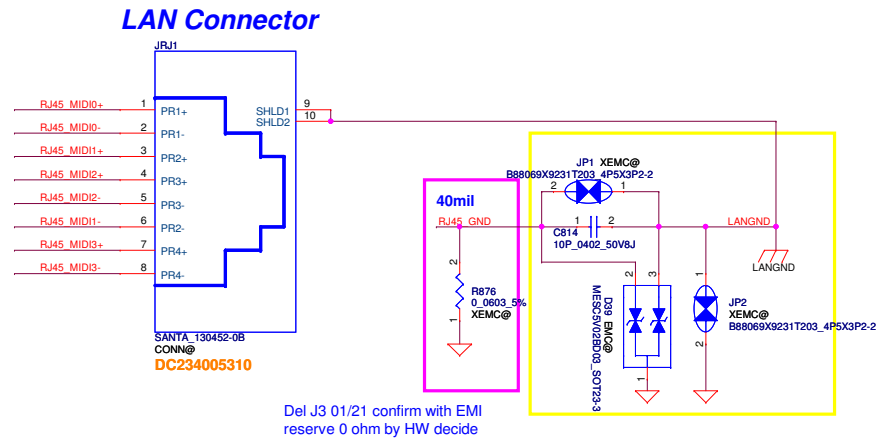
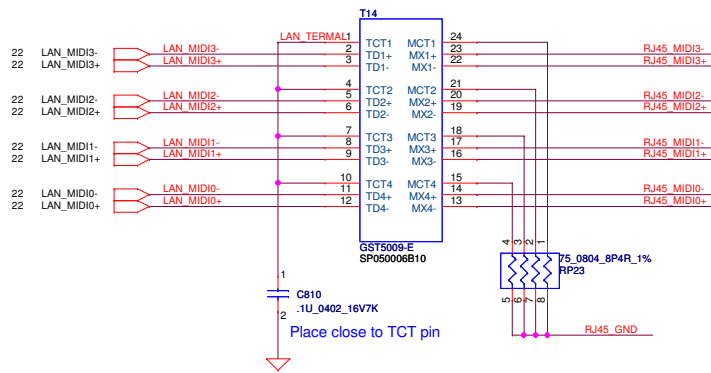
Place near Pin 11,32,48

Reserve for EMI please close to IC



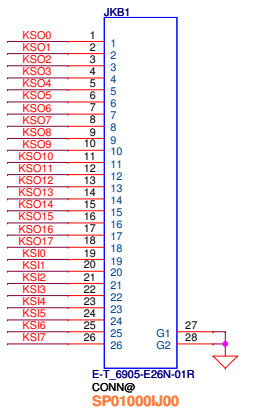
|               | Protect cotact       | Card contact          |
|---------------|----------------------|-----------------------|
|               | Write protect (Lock) | Write Enable (Unlock) |
| Card Uninsert | Open                 | Open                  |
| Card insert   | Open                 | Close                 |



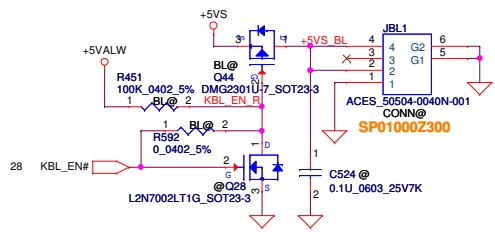


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| Size  | Custom                   | Document Number | Z5WAK M/B LA-B222P | Rev 1.0                  |
| Date:   | Thursday, March 27, 2014 | Sheet           | 23                 | of 42                    |

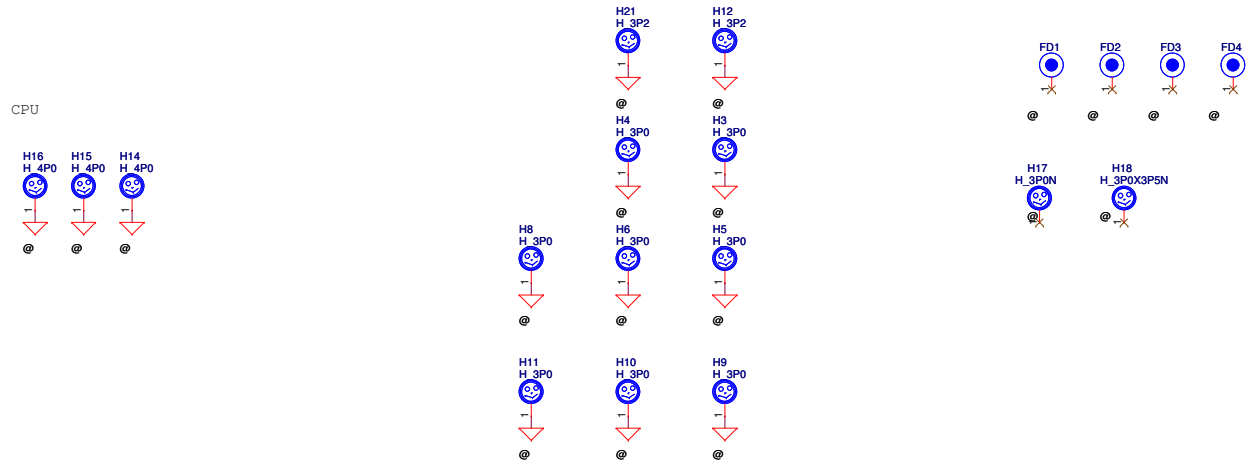
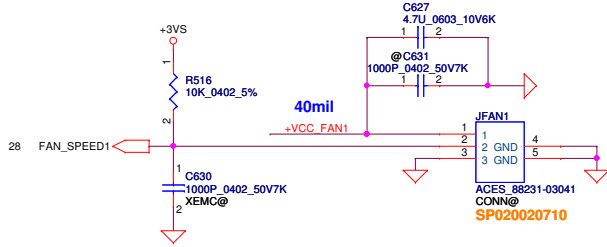
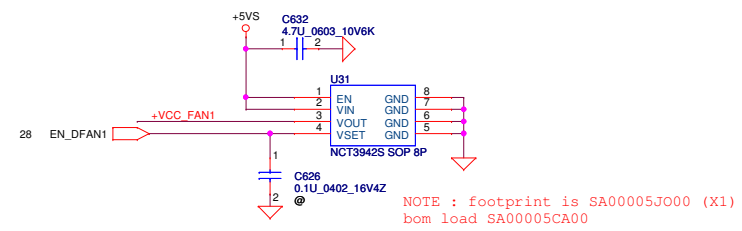
**KB Conn.**



**KB BackLight Conn. Reserve**



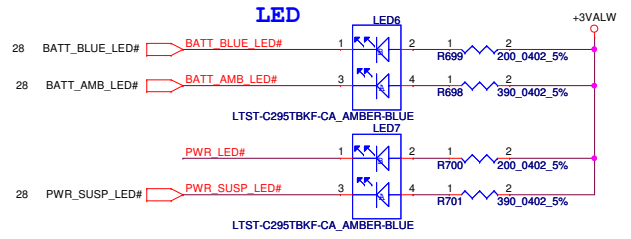
**FAN1 Conn**



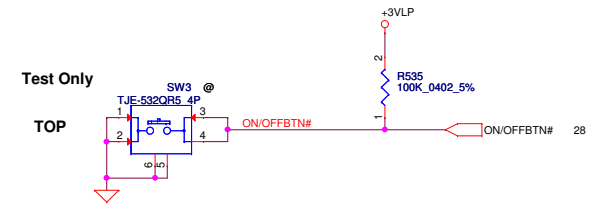
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| Issued Date   | 2012/09/12         | Deciphered Date | 2012/07/29 | Compal Electronics, Inc. |
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| Date: Thursday, March 27, 2014  |                    |                 |            | Sheet 24 of 42           |



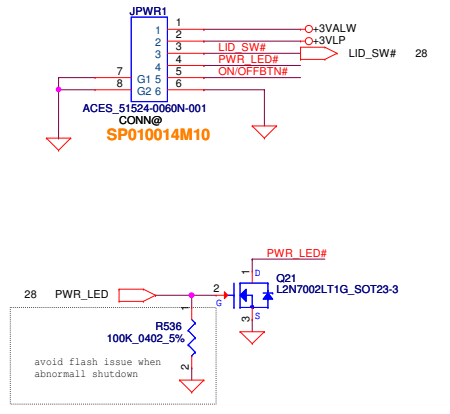
# LED



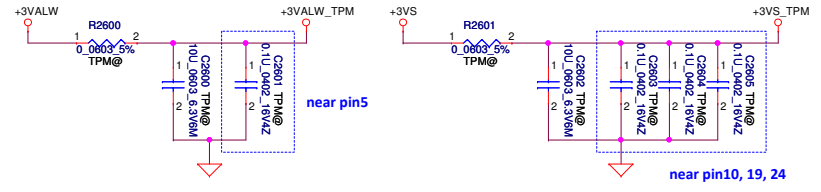
# ON/OFF BTN



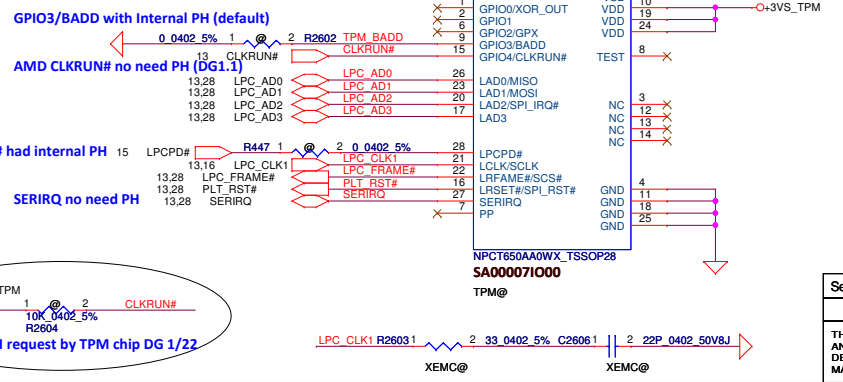
# PWR/B



# TPM Board



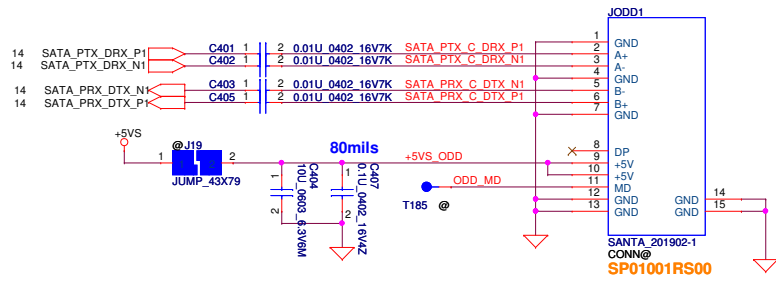
| BADD | SELECTION |
|------|-----------|
| 0    | EEh - EFh |
| * 1  | 7Eh - 7Fh |



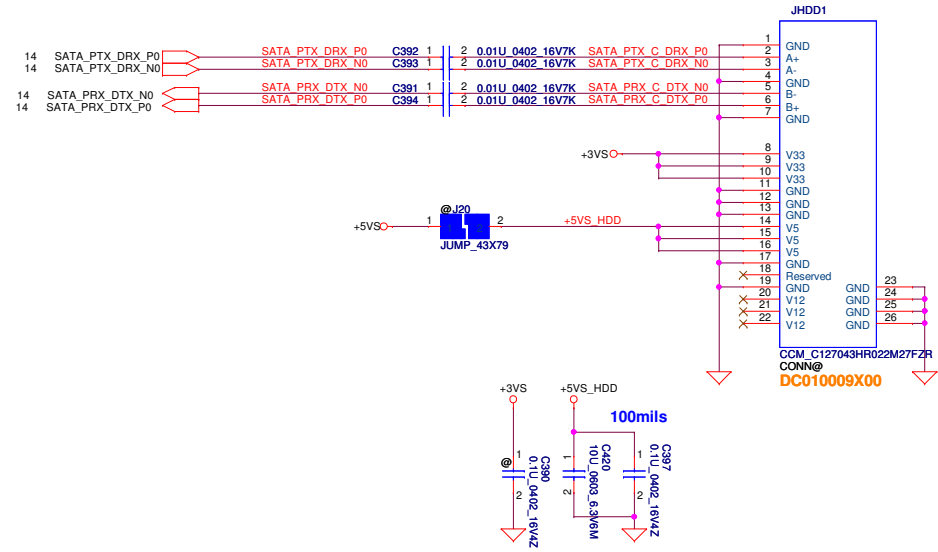
# G-sensor

DEL G-sensor circuit

### SATA ODD Conn.

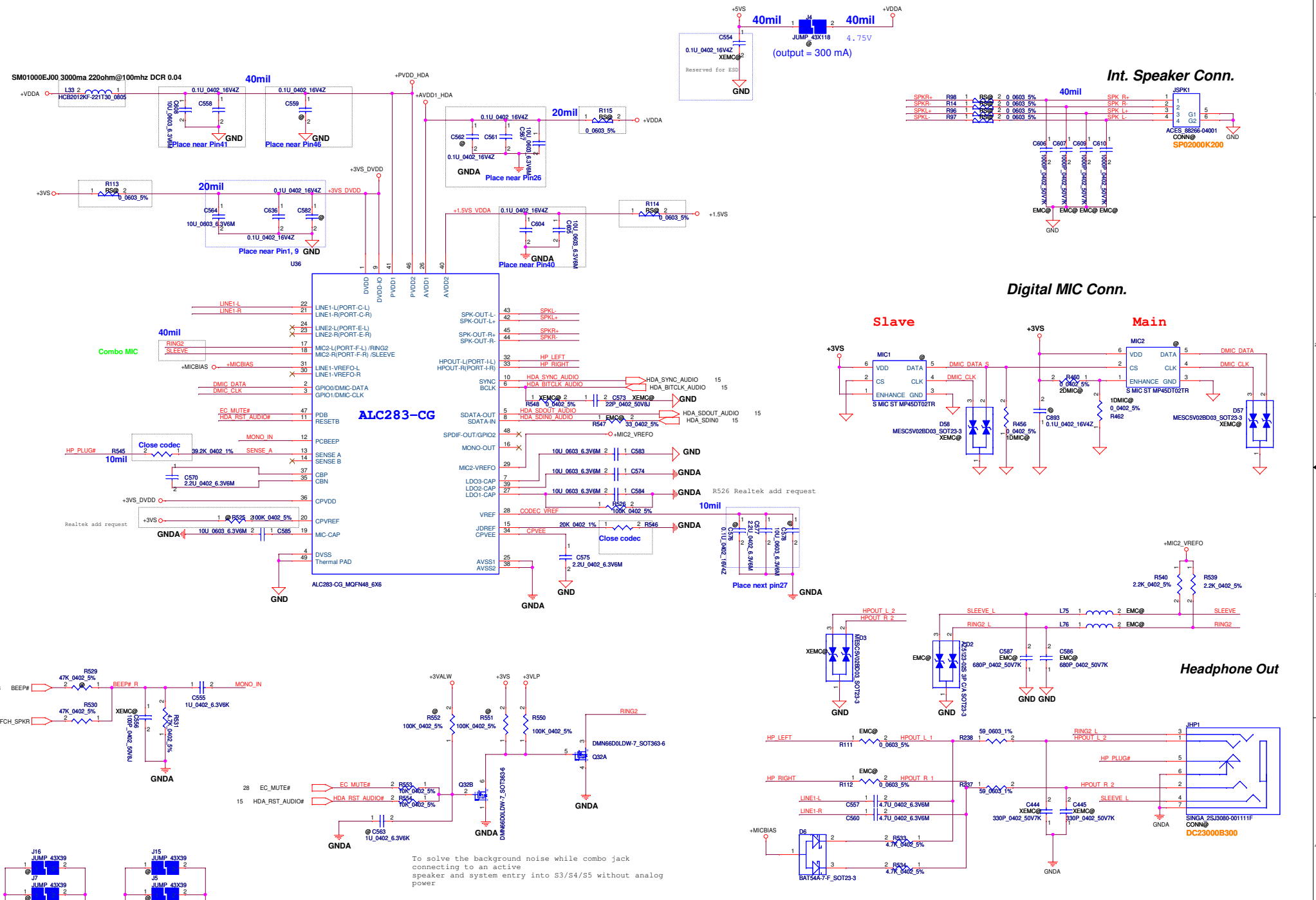


### SATA HDD Conn.



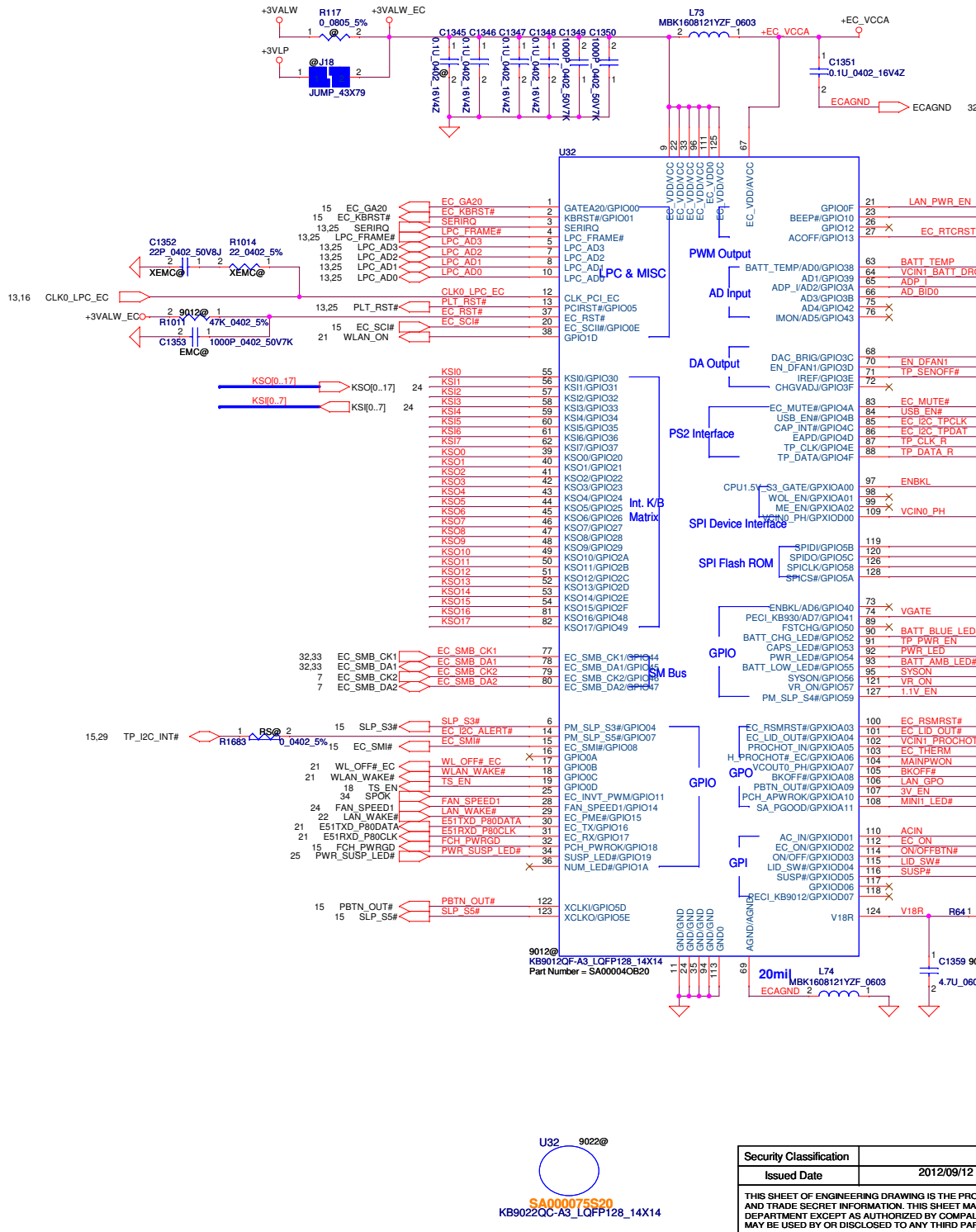
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|  |                    |                 |                          | HDD/ODD Conn   |
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| Date: Thursday, March 27, 2014   |                    |                 |                          | Sheet 26 of 42 |

# HD Audio Codec

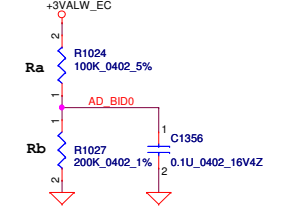


To solve the background noise while combo jack connecting to an active speaker and system entry into S3/S4/S5 without analog power

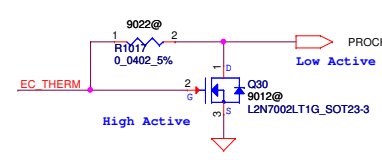
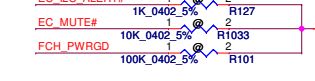
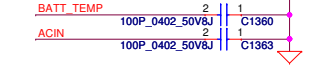
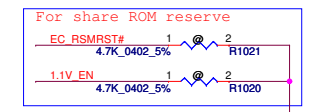
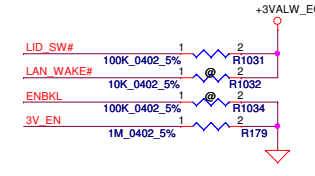
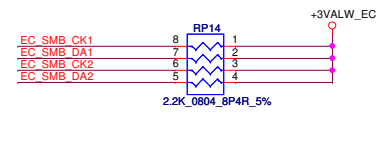
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|   |                    |                 |                          | Rev 1.0   |
|   |                    |                 |                          | Date: Thursday, March 27, 2014   Sheet 27 of 42 |



### Analog Board ID definition



### Pre MP BID=12

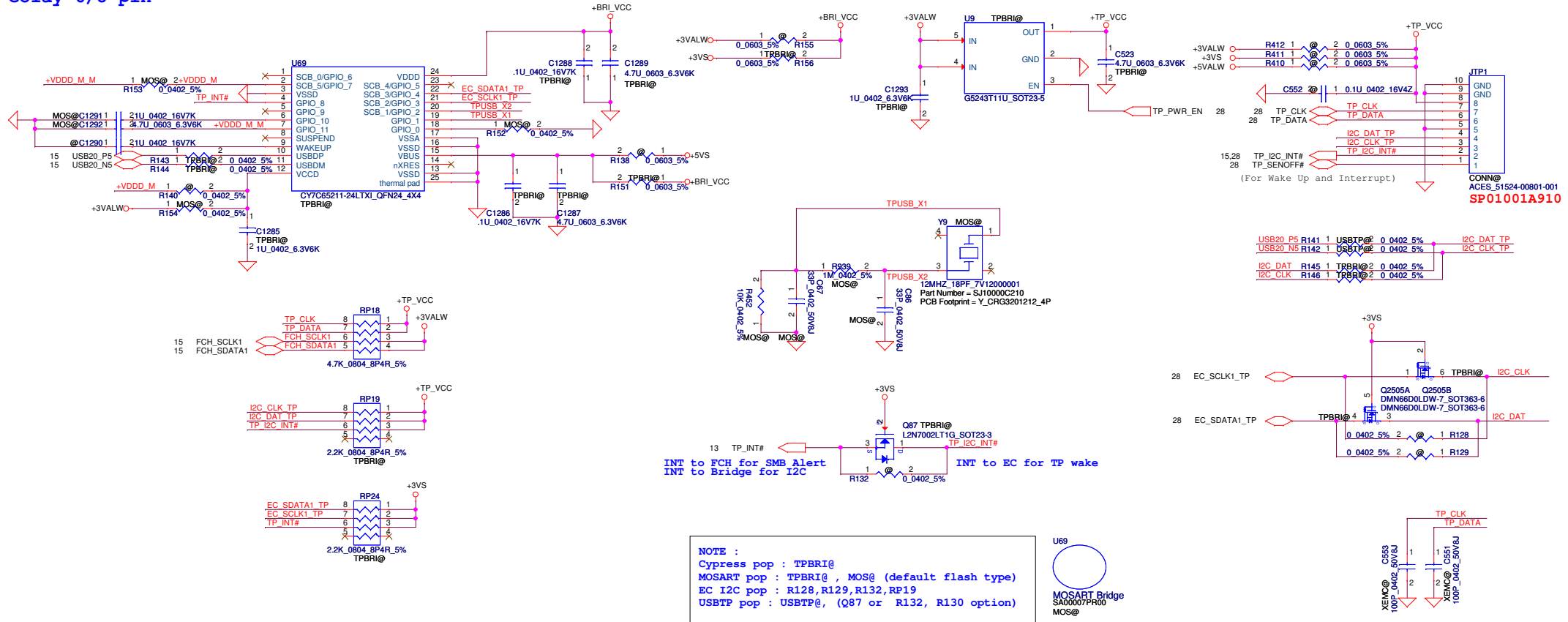


U32 9012@  
SA000075S20  
KB9022QC-A3\_LQFP128\_14X14

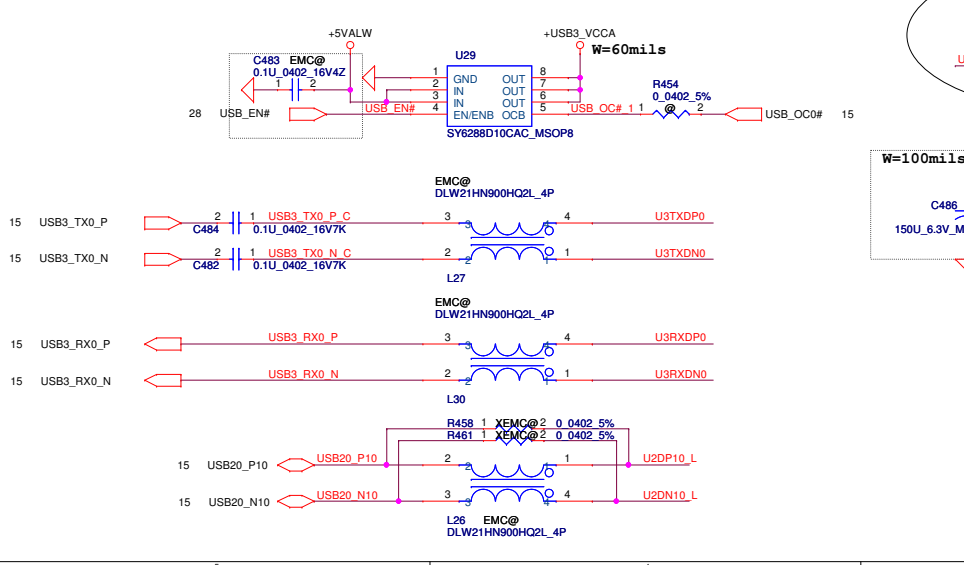
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|---|--------------------|-----------------|
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| Compal Electronics, Inc. |                          |
|--------------------------|--------------------------|
| Title                    | EC KB9012 /KB9022        |
| Document Number          | Z5WAK M/B LA-B222P       |
| Date                     | Thursday, March 27, 2014 |
| ISheet                   | 26 of 42                 |

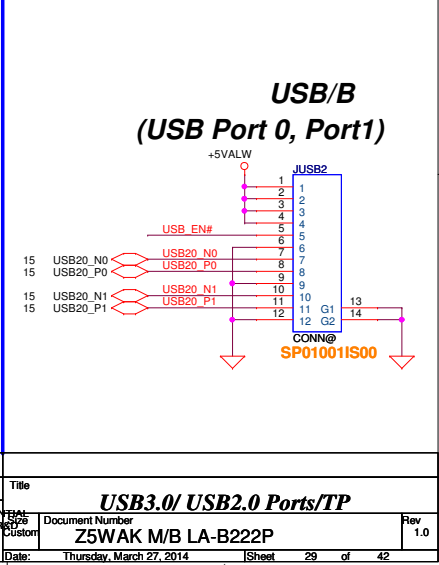
# To TP/B Conn. Colay 6/8 pin



## USB3.0

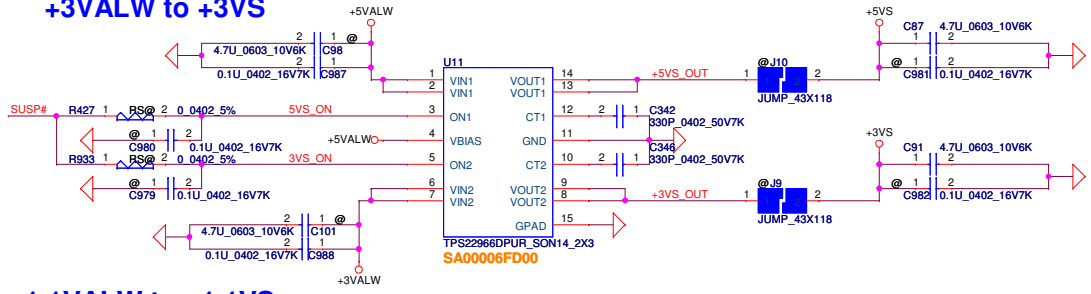


## USB2.0 CONN

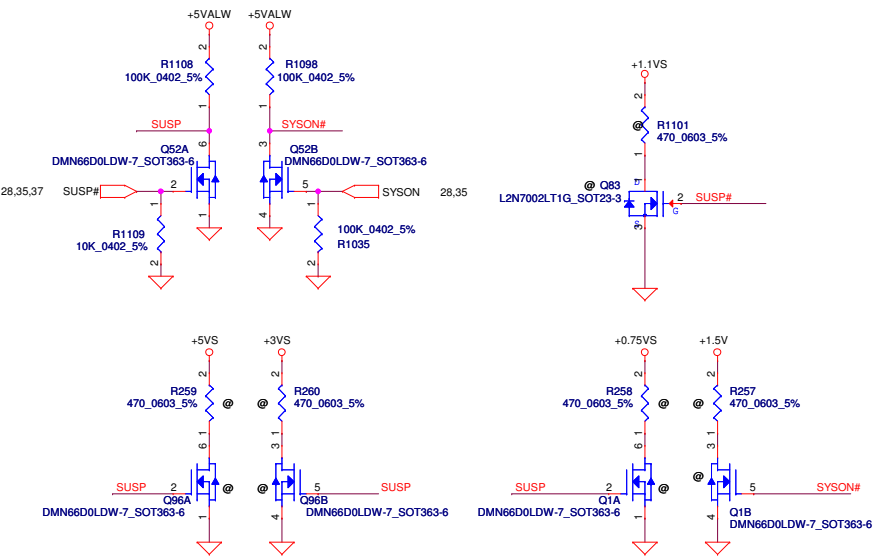
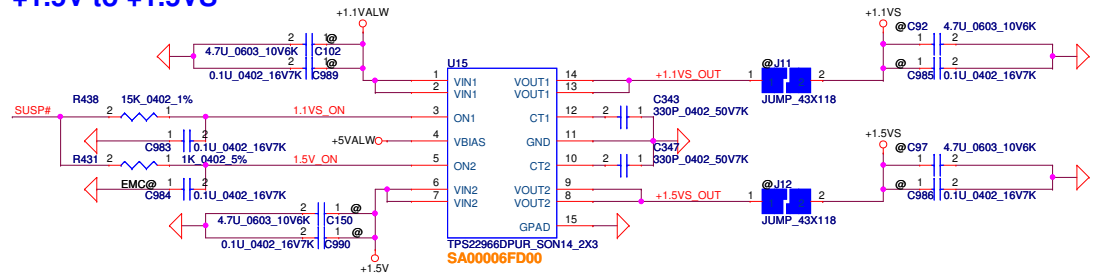


| Security Classification  | Compal Secret Data       |                 |
|--|--------------------------|-----------------|
| Issued Date  | 2012/09/12               | Deciphered Date |
|  |                          | 2013/11/12      |
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| Title  |                          | Rev             |
| USB3.0/ USB2.0 Ports/TP  |                          | 1.0             |
| Document Number  |                          | Customer        |
| Z5WAK M/B LA-B222P   |                          |                 |
| Date:  | Thursday, March 27, 2014 | Sheet 29 of 42  |

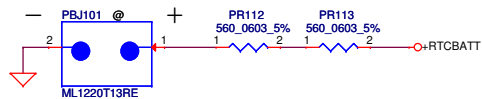
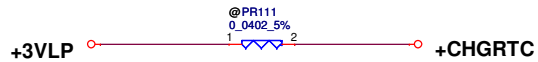
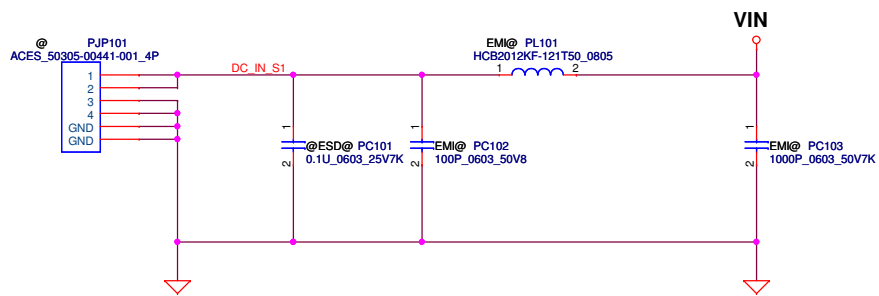
**+5VALW to +5VS**  
**+3VALW to +3VS**



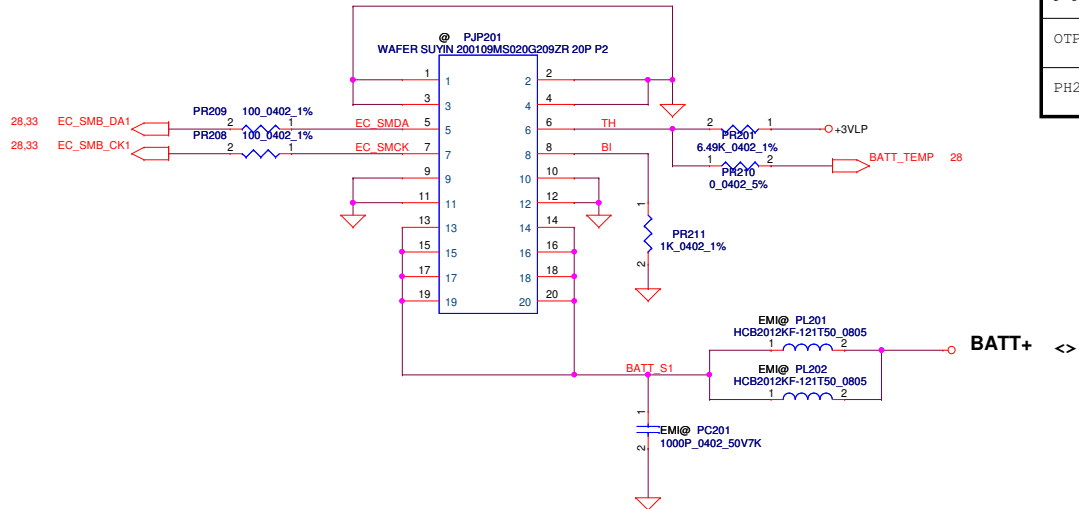
**+1.1VALW to +1.1VS**  
**+1.5V to +1.5VS**



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|   |                    |                 |                          | DC Interface   |
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| Date: Thursday, March 27, 2014  |                    |                 |                          | Sheet 30 of 42 |

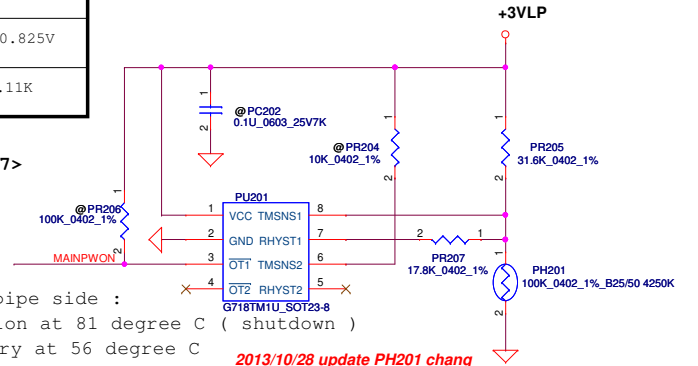


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| Date:   | Thursday, March 27, 2014 | Sheet           | 31                       | of 42   |



| For Thermal pipe OTP | Active      | Recovery    |
|----------------------|-------------|-------------|
| OTP1 (V)             | 81C, 0.825V | 56C, 0.825V |
| PH201 (ohm)          | 10.5K       | 26.11K      |

<45, 47>



PH201 under thermal pipe side :  
 pipe thermal protection at 81 degree C ( shutdown )  
 Recovery at 56 degree C

2013/10/28 update PH201 chang  
 Common part SL200002H00

---Battery\_pin define---

- PIN1 GND
- PIN2 GND
- PIN3 SMD
- PIN4 SMC
- PIN5 TS
- PIN6 B/I
- PIN7 Batt+
- PIN8 Batt+

---Battery Con\_pin define---

- PIN8 GND
- PIN7 GND
- PIN6 SMD
- PIN5 SMC
- PIN4 TS
- PIN3 B/I
- PIN2 Batt+
- PIN1 Batt+

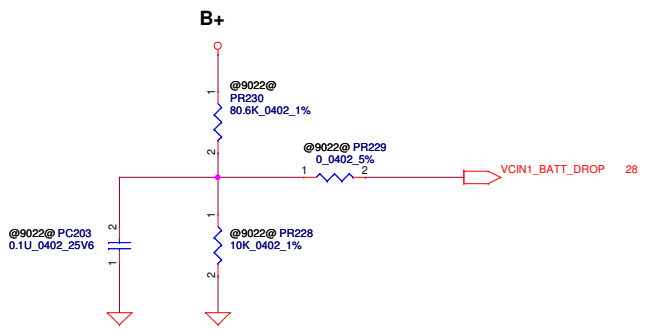
| For KB9022 OTP | Active  | Recovery    |
|----------------|---------|-------------|
| VCIN0_PH (V)   | 92C, 1V | 56C, 2.044V |
| PH202 (ohm)    | 6.99K   | 26.03K      |

| For KB9012 sense 20mΩ | Active        | Recovery     |
|-----------------------|---------------|--------------|
| 40W                   | 42.8W, 0.73V  | 34.4W, 0.59V |
| 65W                   | 69.55W, 0.73V | 55.9W, 0.59V |

PH201 under CPU botten side :  
 CPU thermal protection at 92 degree C ( shutdown )  
 Recovery at 56 degree C +EC\_VCCA

2013/10/02  
 Add for ENE9022 Battery Voltage drop detection.  
 Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.  
 B+=9V

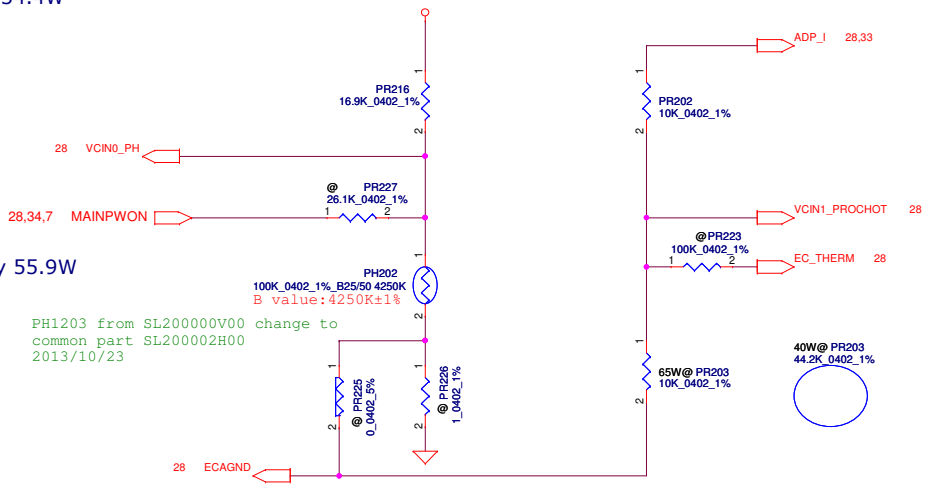


For 40W adapter==>action 42.8W , Recovery 34.4W  
 42.8W:  
 $I_{ada} = 0 \sim 2.253A$  ( $42.8W/19V=2.253A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 2.253 * 0.02 = 0.901$   
 34.4W:  
 $I_{ada} = 0 \sim 1.811A$  ( $34.4W/19V=1.811A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 1.811 * 0.02 = 0.724$

CP=40W\*0.85=34W

For 65W adapter==>action 69.55W , Recovery 55.9W  
 69.55W:  
 $I_{ada} = 0 \sim 3.661A$  ( $69.55W/19V=3.661A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 3.661 * 0.02 = 1.464$   
 55.9W:  
 $I_{ada} = 0 \sim 2.942A$  ( $55.9W/19V=2.942A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 2.942 * 0.02 = 1.177$

CP=65W\*0.85=55.25W



PH1203 from SL200000V00 change to  
 common part SL200002H00  
 2013/10/23



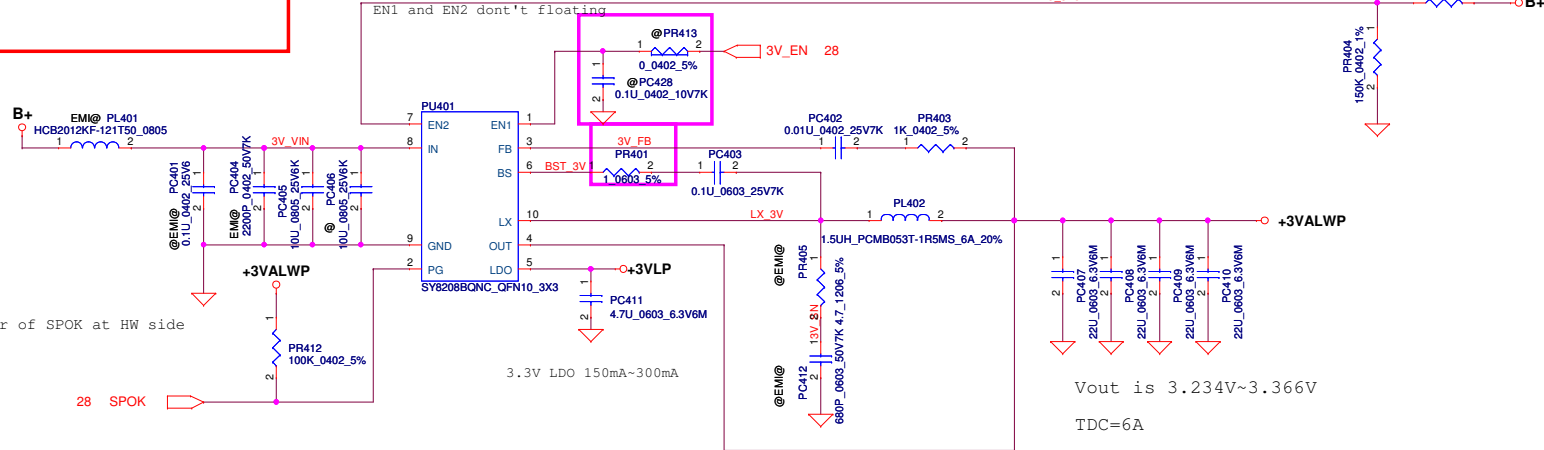


Module model information

SY8208B\_V2.mdd  
SY8208C\_V2.mdd

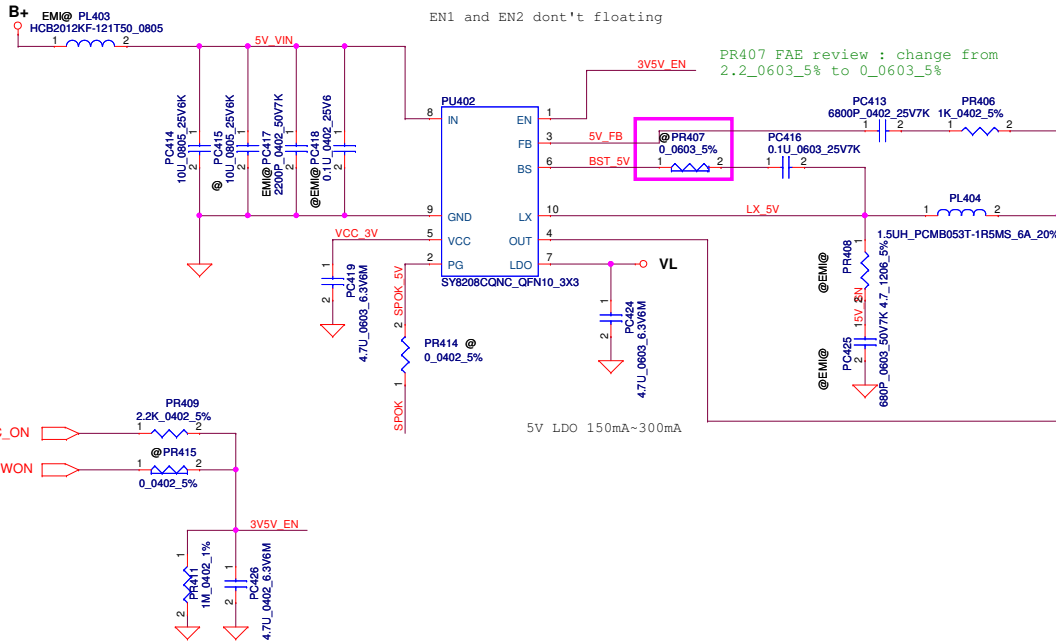
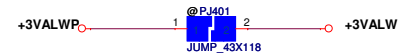
PR401 FAE review : change from 2.2\_0603\_5% to 1\_0603\_5%  
HW request add PR413, and PC428-un-pop

EN1 and EN2 dont't floating



Check pull up resistor of SPOK at HW side

Vout is 3.234V~3.366V  
TDC=6A



PR407 FAE review : change from 2.2\_0603\_5% to 0\_0603\_5%

EN1 and EN2 dont't floating

Vout is 4.998V~5.202V  
TDC=6A

Add PC427 for 22U\_0603 size

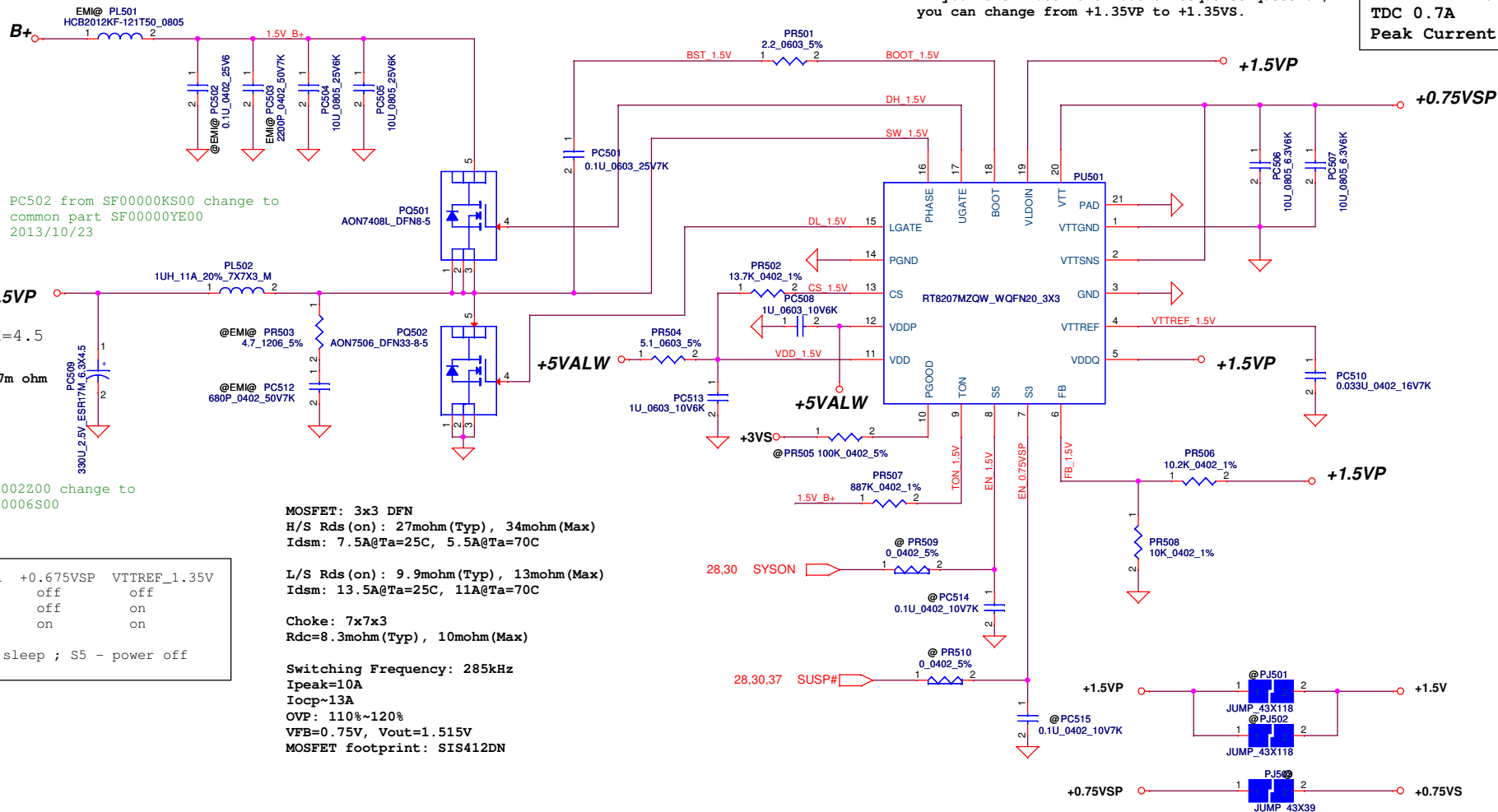
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|   |                    |                 |            | +3VALWP/+5VALW           |
|   |                    |                 |            | Rev 1.0                  |
| Date: Thursday, March 27, 2014  |                    |                 |            | Sheet 34 of 42           |

Module model information

RT8207M\_v1.mdd For Single layer  
RT8207M\_v2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%  
TDC 0.7A  
Peak Current 1A



PC502 from SF00000KS00 change to  
common part SF00000YE00  
2013/10/23

SF000006S00 H=4.5

ESR=17m ohm

PC509 from SF000002Z00 change to  
common part SF000006S00  
2013/10/23

|      |       |           |              |
|------|-------|-----------|--------------|
| Mode | Level | +0.675VSP | VTTREF_1.35V |
| S5   | L     | off       | off          |
| S3   | L     | off       | on           |
| S0   | H     | on        | on           |

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN  
H/S Rds (on) : 27mohm (Typ), 34mohm (Max)  
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on) : 9.9mohm (Typ), 13mohm (Max)  
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

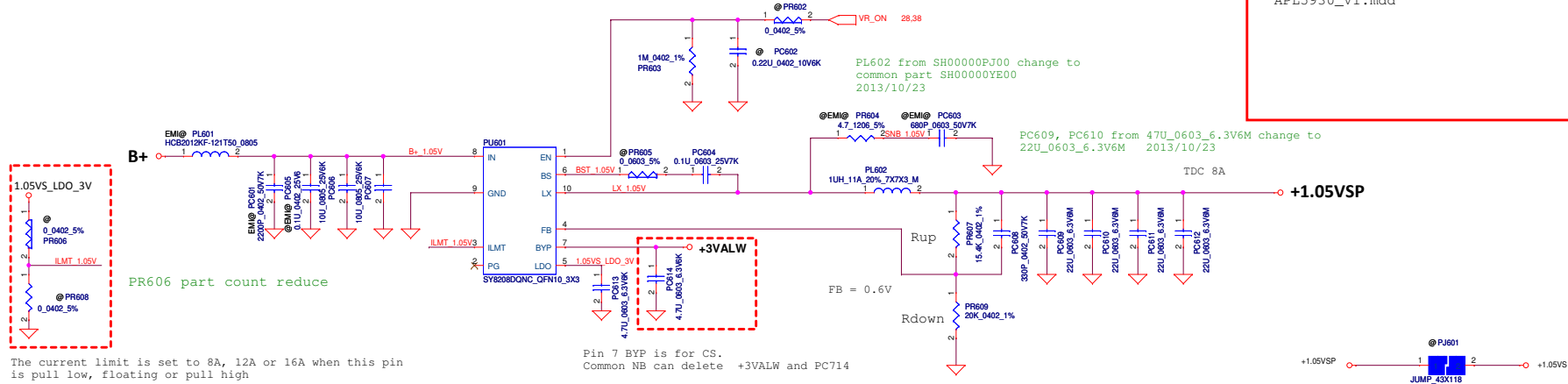
Choke: 7x7x3  
Rdc=8.3mohm (Typ), 10mohm (Max)

Switching Frequency: 285kHz  
Ipeak=10A  
Iocp~13A  
OVP: 110%~120%  
VFB=0.75V, Vout=1.515V  
MOSFET footprint: SIS412DN

|   |                 |                    |            |                          |                          |
|---|-----------------|--------------------|------------|--------------------------|--------------------------|
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| Size  | Document Number |                    |            | Rev                      | 1.0                      |
| Custom  |                 |                    |            | Date:                    | Thursday, March 27, 2014 |
|   |                 |                    |            | Sheet                    | 35 of 42                 |

EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2

Module model information  
SY8208D\_V1.mdd  
APL5930\_V1.mdd



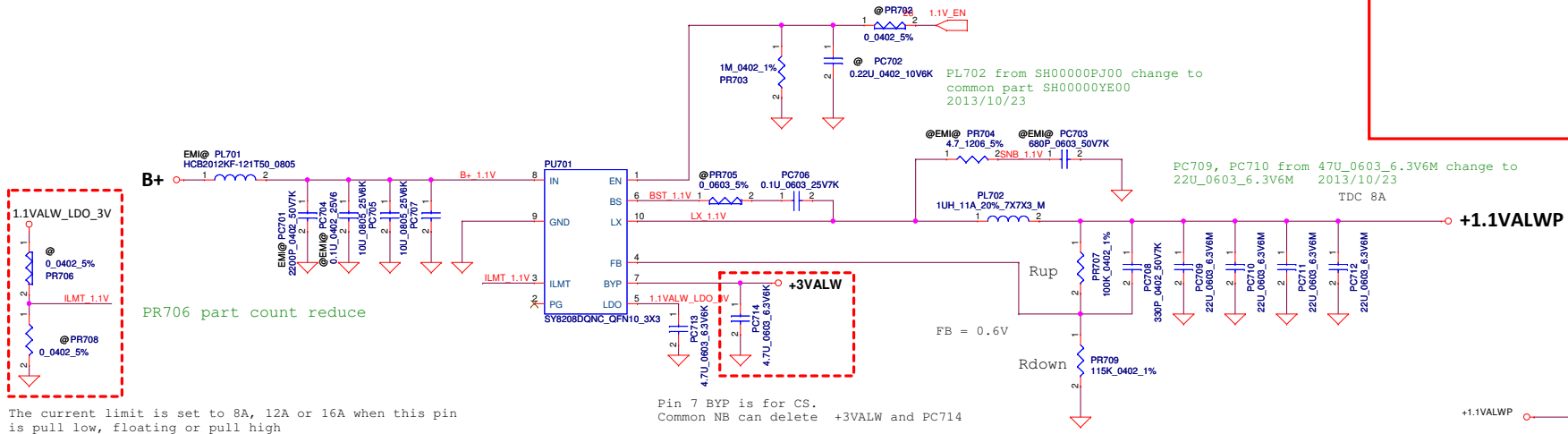
The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

VFB=0.6V  
Vout=0.6V\* (1+Rup/Rdown)  
Vout=1.062V

|   |                          |                    |            |                          |     |
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| Size  | C                        | Document Number    |            | Rev                      | 1.0 |
| Date:   | Thursday, March 27, 2014 | Sheet              | 36         | of                       | 42  |

EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2

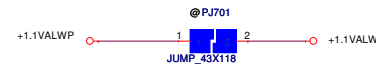
Module model information  
SY8208D\_V1.mdd



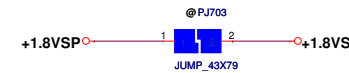
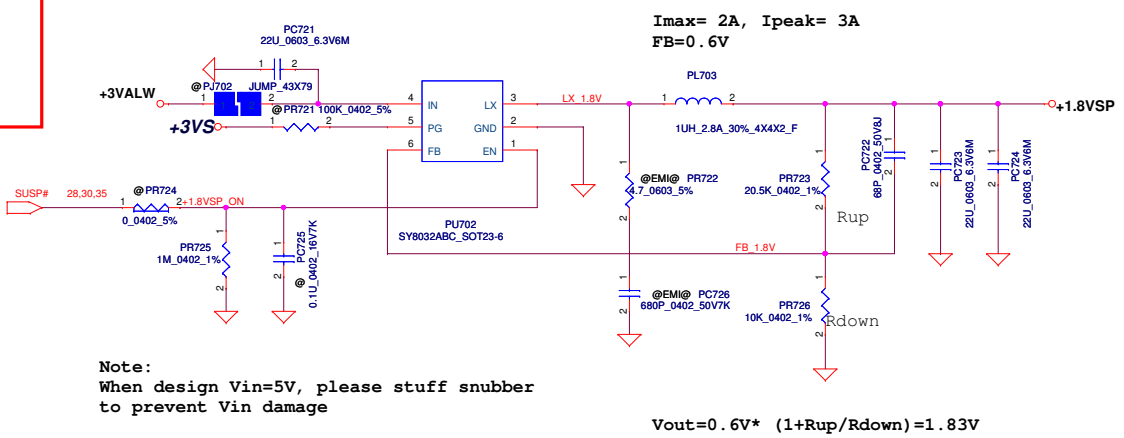
The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.  
Common NB can delete +3VALW and PC714

VFB=0.6V  
 $V_{out} = 0.6V * (1 + R_{up}/R_{down})$   
 $V_{out} = 1.12V$

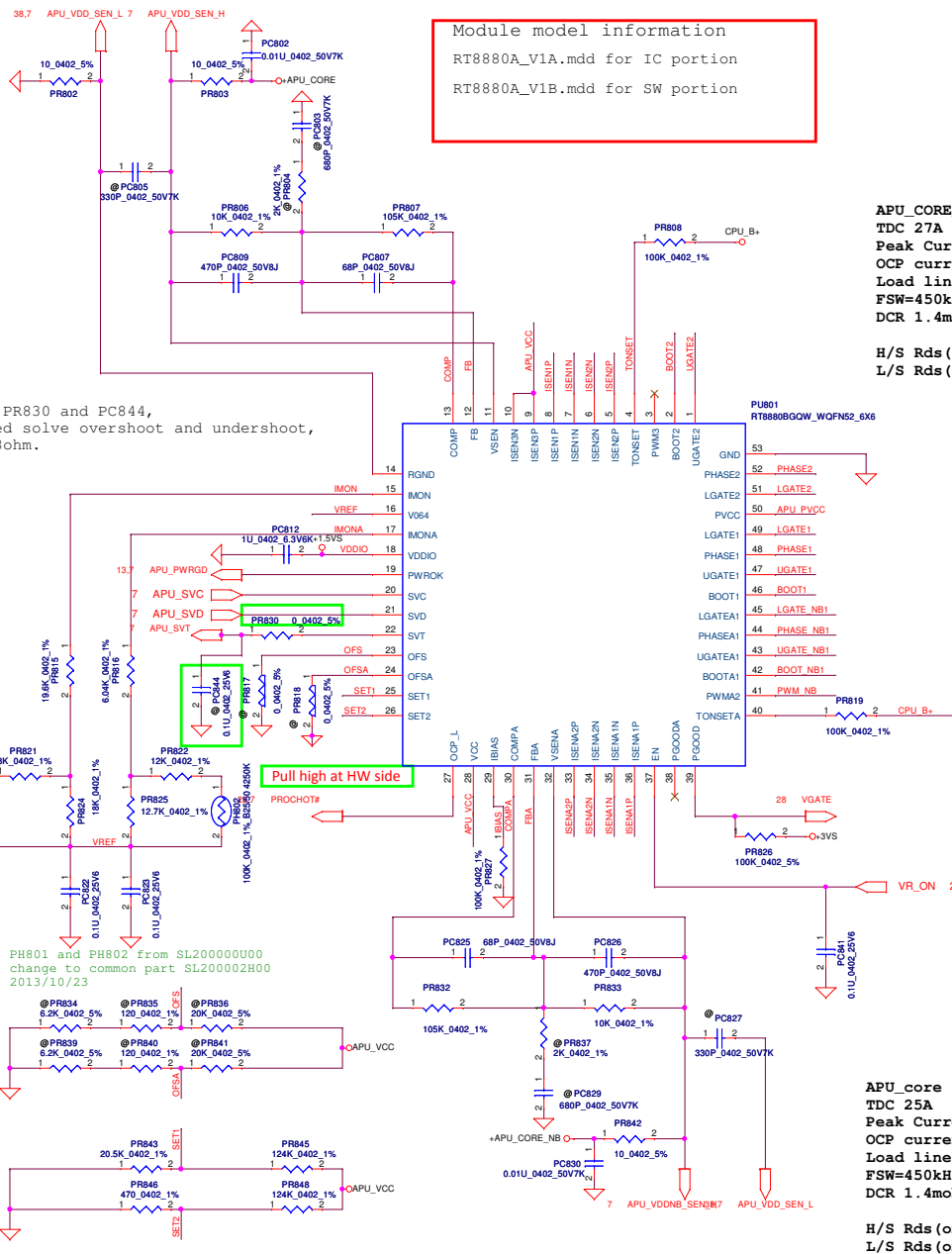


Module model information  
SY8032\_V2.mdd



$V_{out} = 0.6V * (1 + R_{up}/R_{down}) = 1.83V$

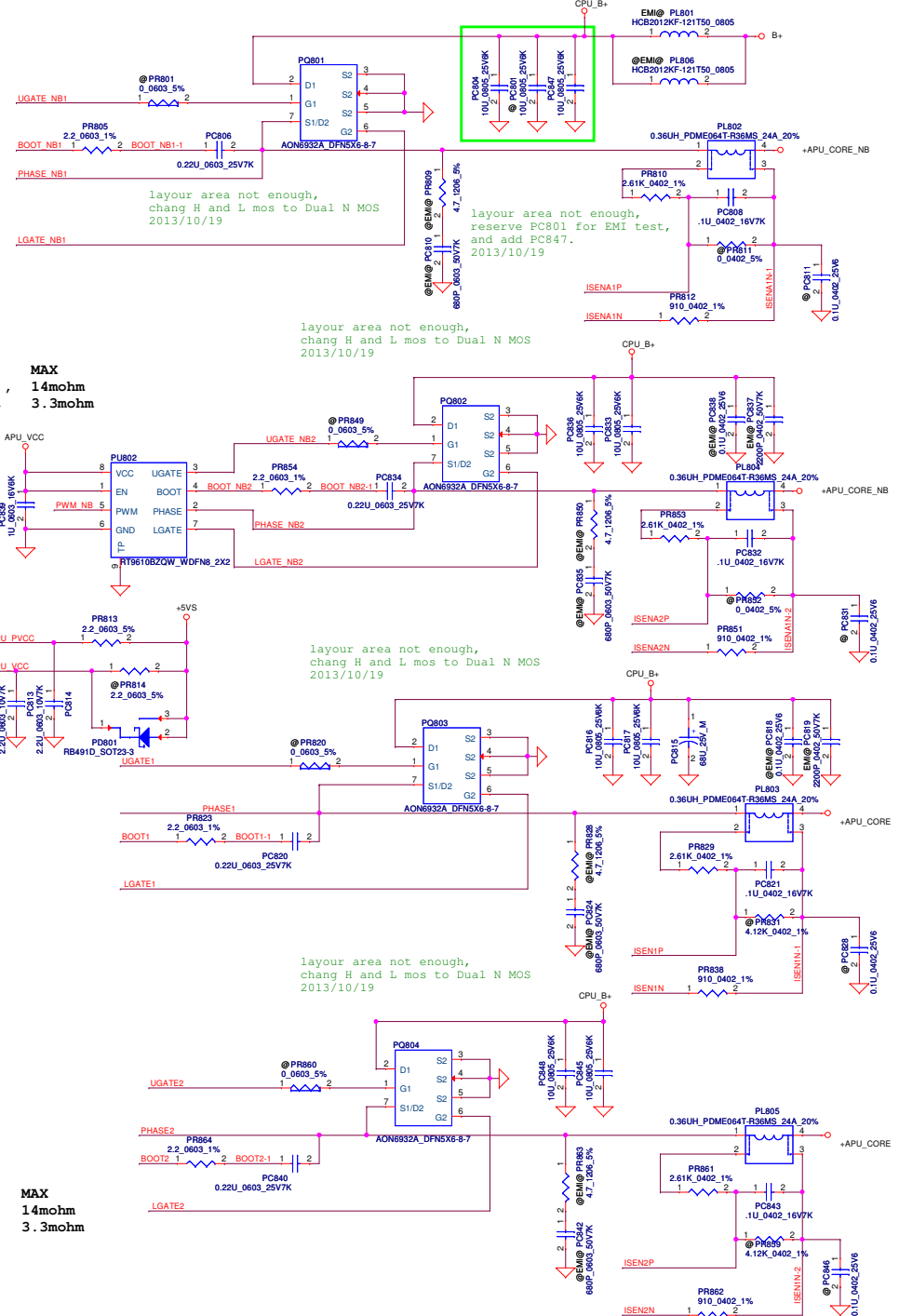
|   |                          |                    |            |                   |     |
|---|--------------------------|--------------------|------------|-------------------|-----|
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| Issued Date   | 2011/06/15               | Deciphered Date    | 2013/10/01 | +1.1VALWP/+1.8VSP |     |
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SVT reserve PR830 and PC844,  
 PR830 if need solve overshoot and undershoot,  
 change to 18ohm.

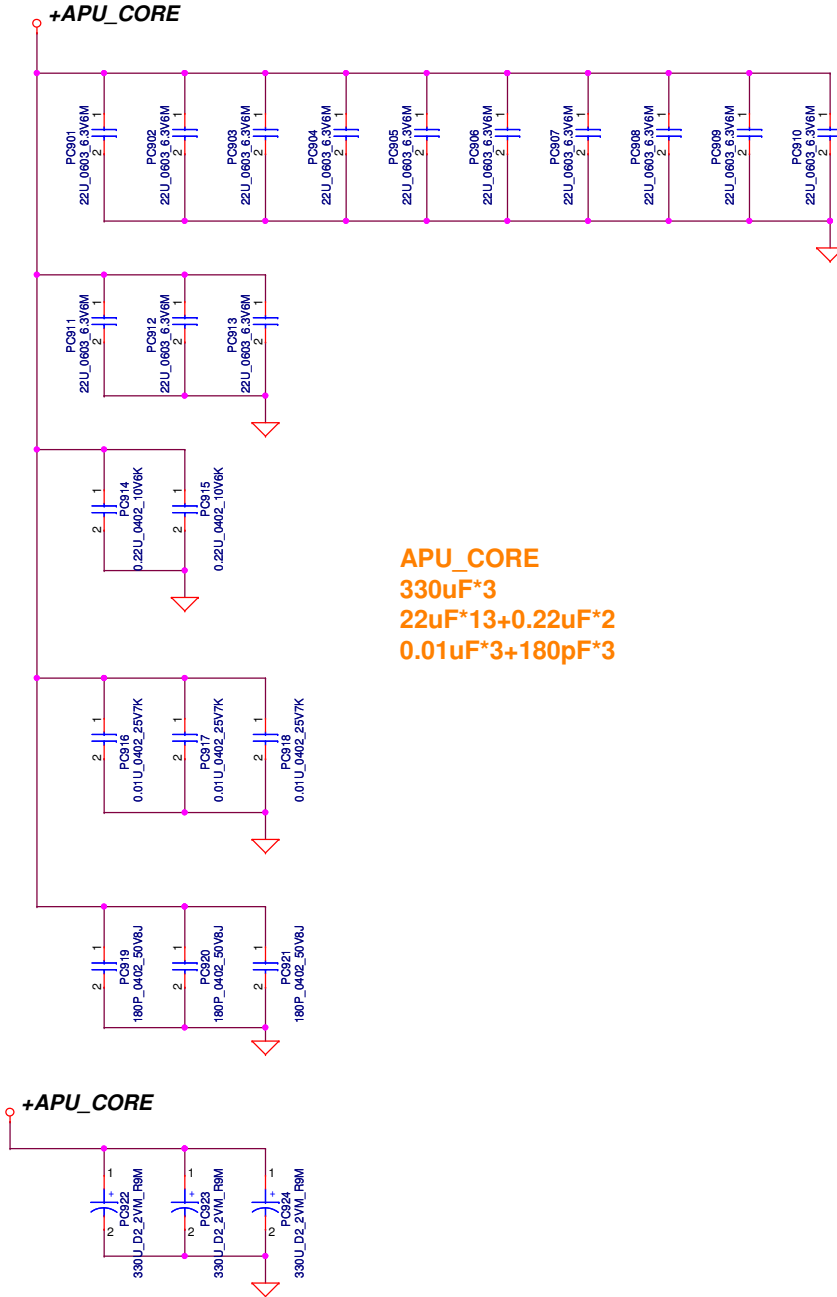
PH801 and PH802 from SL200000U00  
 change to common part SL200002H00  
 2013/10/23

Pull high at HW side



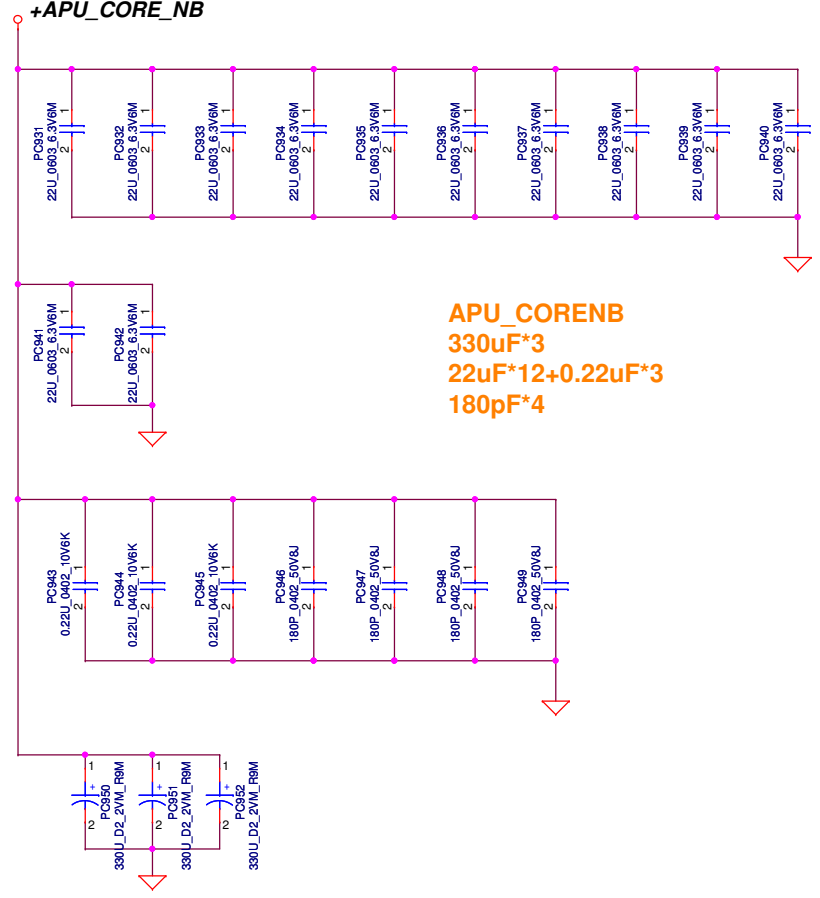
|  |                          |                 |            |
|--|--------------------------|-----------------|------------|
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| Title  | +CPU CORE/+CPU CORE NB   |                 |            |
| Size   | Document Number          | Revision        |            |
| Custom   | Z5WAK                    | 1.0             |            |
| Date:  | Thursday, March 27, 2014 | Sheet           | 38 of 42   |

**+APU\_CORE**



**APU\_CORE**  
**330uF\*3**  
**22uF\*13+0.22uF\*2**  
**0.01uF\*3+180pF\*3**

**+APU\_CORE\_NB**



**APU\_CORENB**  
**330uF\*3**  
**22uF\*12+0.22uF\*3**  
**180pF\*4**

|   |                          |                    |            |                          |    |
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| Size  | Document Number          |                    |            | Rev                      |    |
|   | VS50_AMD                 |                    |            | 1.0                      |    |
| Date:   | Thursday, March 27, 2014 | Sheet              | 39         | of                       | 42 |

| Item | Fixed Issue | Reason for change   | Rev. | PG#                 | Modify List   | Date  | Phase    |
|------|-------------|---|------|---------------------|---|-------|----------|
| 1    |             | layout area not enough  |      | APU_CORE            | PQ801;PQ803;PQ807;PQ808 FDMS7698 and PQ802;PQ804;PQ806;PQ809 MDU1511 change to Dual N AON6932A  | 10/09 | EVT      |
| 2    |             | EMI bead "HCB2012KF-121T50_0805" derating 5A, need 2pcs for APU_CORE and APU_CORENB         |      | APU_CORE            | Add PL806 EMI bead "HCB2012KF-121T50_0805" from 1pcs to 2pcs at B+, for APU_CORE and APU_CORENB   | 10/15 | EVT      |
| 3    |             | RT8880A FAE review  |      | APU_CORE            | PR813 from 0402 change to 0603, delete PR844, PR847   | 10/16 | EVT      |
| 4    |             | HW: EC share ROM, modify 3VALW and 1.1VALW enable net-name                                  |      | 3VALW<br>5VALW      | change 3VALW enable net name from 3V5V_EN to 3V_EN<br>change 1.1VALW enable net name from SUSP# to 1.1V_EN  | 10/17 | EVT      |
| 5    |             | Choke, OS-CON cap, Thermistor change to standard part                                       |      |                     |   | 10/23 | EVT      |
| 6    |             | RT8880A vendor EOL, change to RT8880B   |      | APU_CORE            | CPU_CORE IC from RT8880A SA000066V00 change to RT8880B SA000066V10  | 10/23 | EVT      |
| 7    |             | Battery connector BATT+ bead, 1pcs for UMA, 2pcs for DIS.                                   |      | BATT<br>CONN        | Add PL202 HCB2012KF-121T50_0805 for DIS only  | 10/28 | EVT      |
| 8    |             | 22U_0603_6.3V6M cheaper than 47U_0603_6.3V6M  |      | +1.05VS<br>+1.1VALW | PC609, PC610 and PC709, PC710 from 47U_0603_6.3V6M change to 22U_0603_6.3V6M  | 10/30 | EVT      |
| 9    |             | HW request Add PR1107, and unpop PR1104, VGA_PG is default setting for VGA sequence control |      | +0.95V              | Add location PR1107 0_0402_5%, and unpop PR1104 0_0402_5%   | 10/31 | EVT      |
| 10   |             | HW request add RC at 3VALW enable   |      | +3VALW              | Add PR413 0_0402_5%, and PC428 0.1U_0402_10V7K _ un-pop   | 10/31 | EVT      |
| 11   |             | adjust 1.05V output voltage   |      | +1.05VSP            | change PR607 from 100K ohm to 15.4K ohm, change PR609 from 133K ohm to 20K ohm, change 1.05V output from 1.05V to 1.062V  | 12/02 | DVT      |
| 12   |             | adjust 1.8VSP output voltage  |      | +1.8VSP             | change PR723 from 20K ohm to 20.5K ohm, change 1.05V output from 1.8V to 1.83V  | 12/10 | DVT      |
| 13   |             | adjust 1.1VALW output voltage   |      | +1.1VALW            | change PR709 from 118K ohm to 115K ohm, change 1.1VALW output from 1.108V to 1.121V   | 12/10 | DVT      |
| 14   |             | Part count reduce   |      |                     | change enable resistor PR413, PR602, PR702, PR724 from 0 ohm to R-Short, change EMI High side and Low side resistor PR308, PR407, PR605, PR705, PR801, PR820, PR849, PR860, PR1216, PR1232 from 0 ohm to R-Short. | 12/10 | DVT      |
| 15   |             | adjust VGA Vboot voltage  |      | VGA                 | change PR1205 from pop to un-pop, change PR1211 from un-pop to pop.   | 12/13 | DVT      |
| 16   |             | reserve PD801   |      | CPU_CORE            | reserve PD801 for AMD CPU leakage voltage from APU_SVD  | 12/13 | DVT      |
| 17   |             | delete VCIN0 and VCIN1 hysteresis   |      | OTP                 | change PR216 from 22.6K to 16K, change PR227 from 26.1K to un-pop, change PR202 from UMA/10.5K and DIS/11.3K to 10K, change PR223 from UMA/162K and DIS/100K to un-pop.   | 12/24 | DVT      |
| 18   |             | ABO request BI pin short to GND   |      | BATT CONN           | change PR210 from 1k to 0 ohm.  | 12/26 | DVT MEMO |
| 19   |             | 65W and 40W VCIN0 set at the same voltage active and recovery                               |      | OTP                 | change UMA SKU PR203 from 10K to 44.2K<br>Add PC426   | 12/26 | DVT MEMO |

|  |                    |                 |                          |                                 |
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|  |                    |                 |                          | Rev<br>1.0                      |
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| <small>Date:</small> Thursday, March 27, 2014   |                    |                 | <small>Rev</small><br>1.0 | <small>Sheet</small> 42 of 42                  |

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