

# Compal Confidential

Model Name : A4WAB

File Name : LA-C341P

# Compal Confidential

## M/B Schematics Document

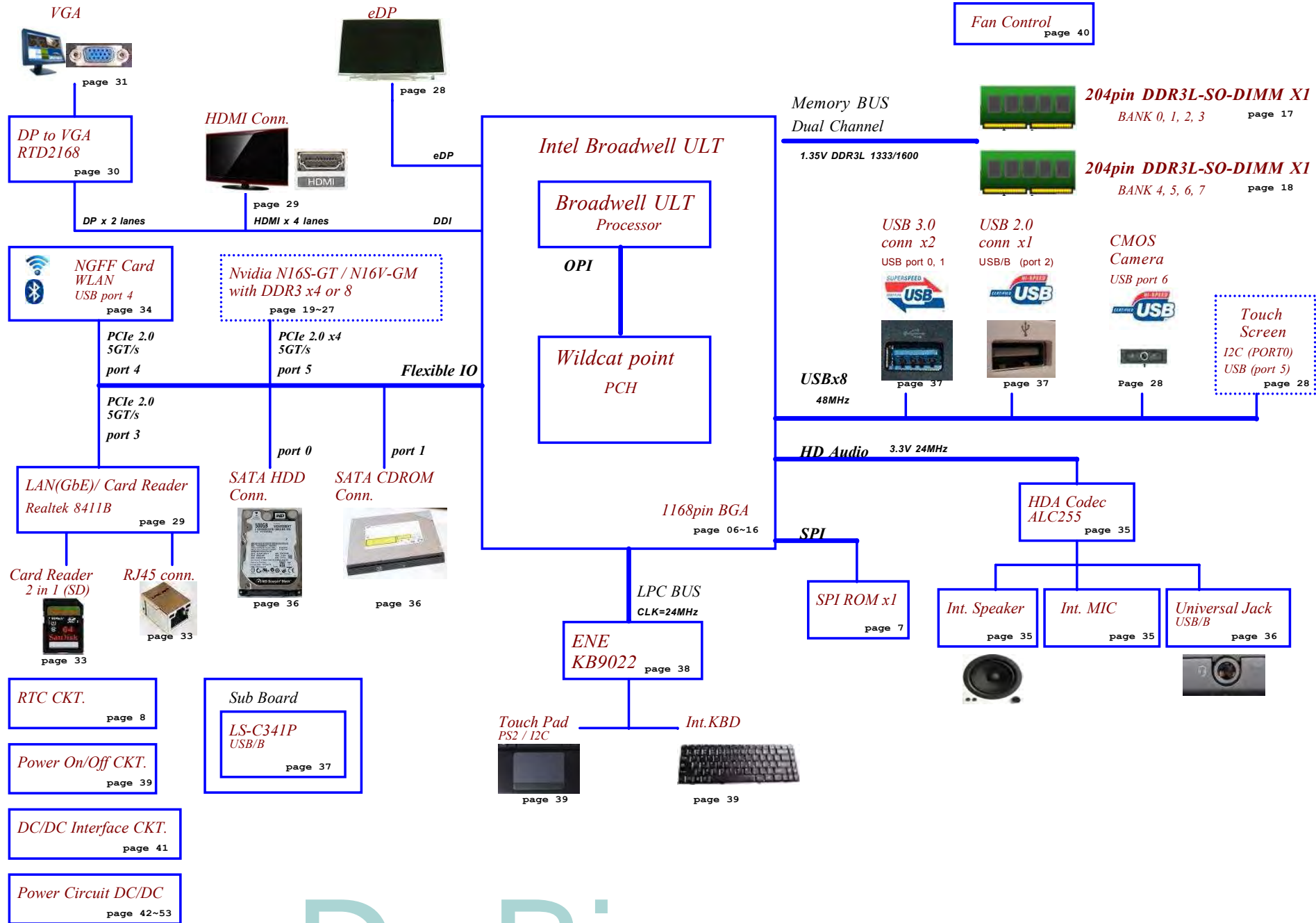
Intel Broadwell ULT (Broadwell + Wildcat point)

Nvidia N16S-GT / N16V-GM

2015-03-18

REV: 1.0

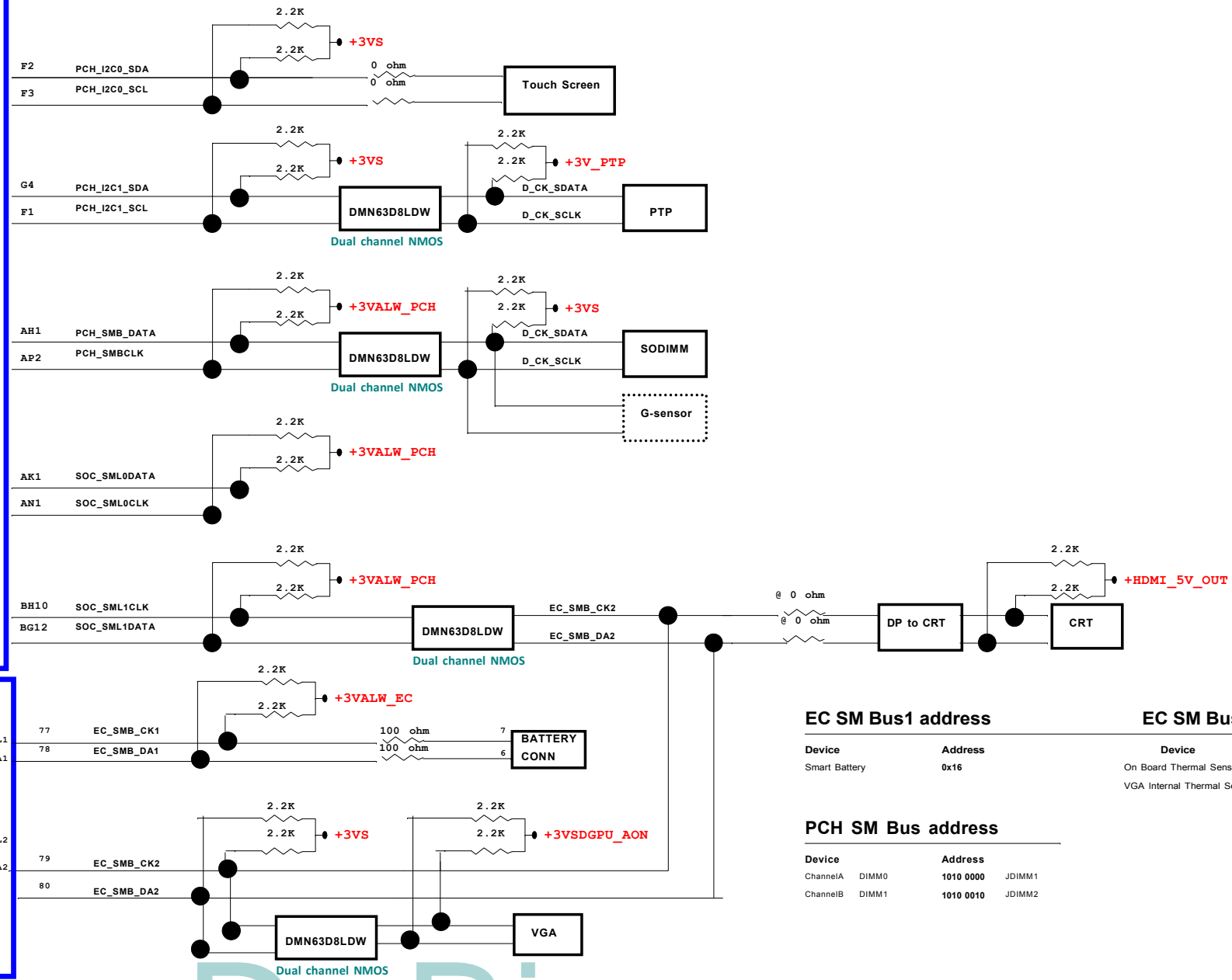
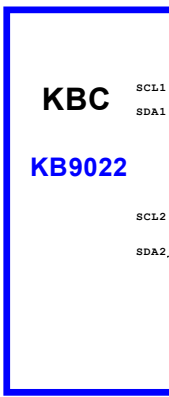
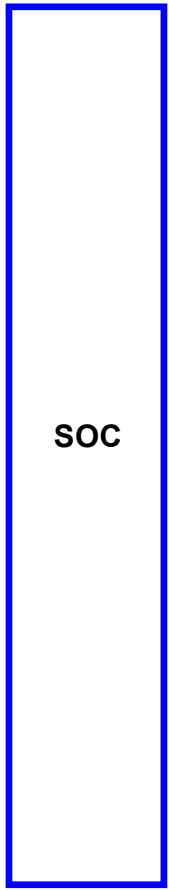
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**EC SM Bus1 address**

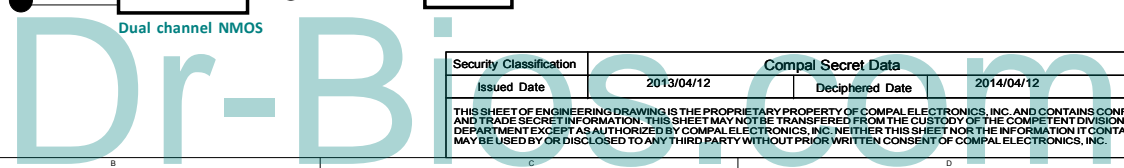
Device	Address
Smart Battery	0x16

**EC SM Bus2 address**

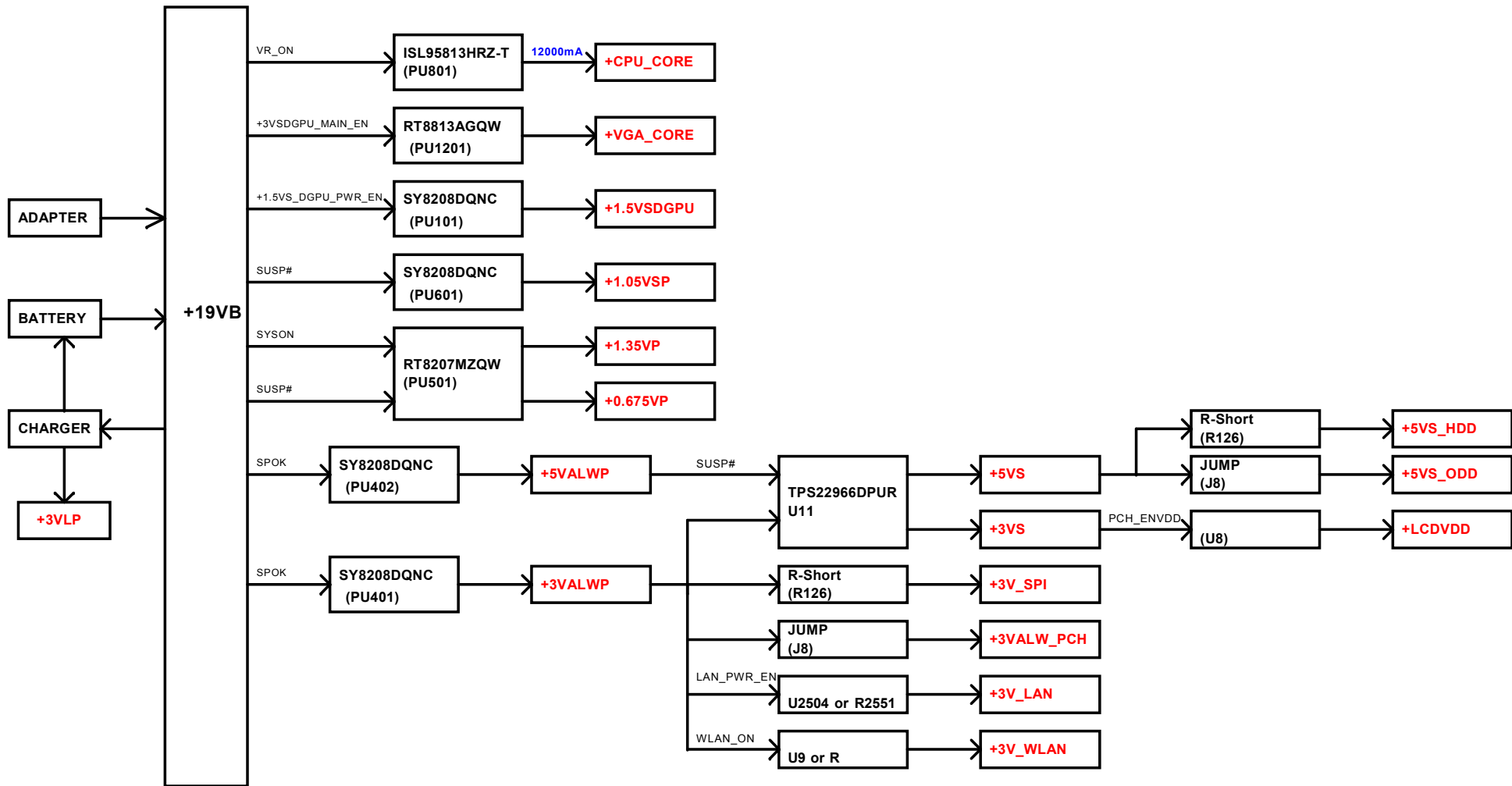
Device	Address
On Board Thermal Sensor	0x96
VGA Internal Thermal Sensor	0x9E

**PCH SM Bus address**

Device	Address
ChannelA DIMM0	1010 0000 JDIMM1
ChannelB DIMM1	1010 0010 JDIMM2



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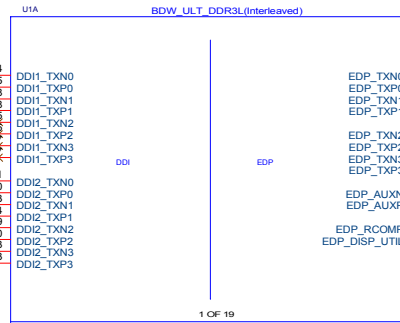


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DP to CRT

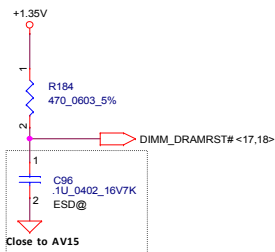
HDMI



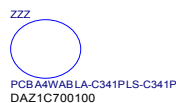
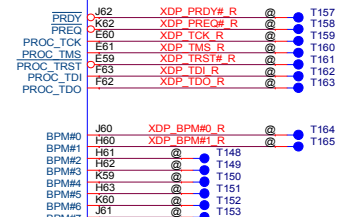
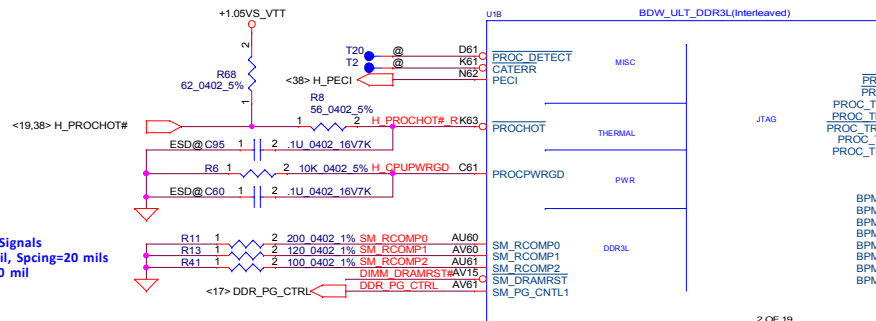
eDP reserve to support 4K2K

eDP Panel

Trace width=20 mils, Spacing=25mil, Max length=100mils



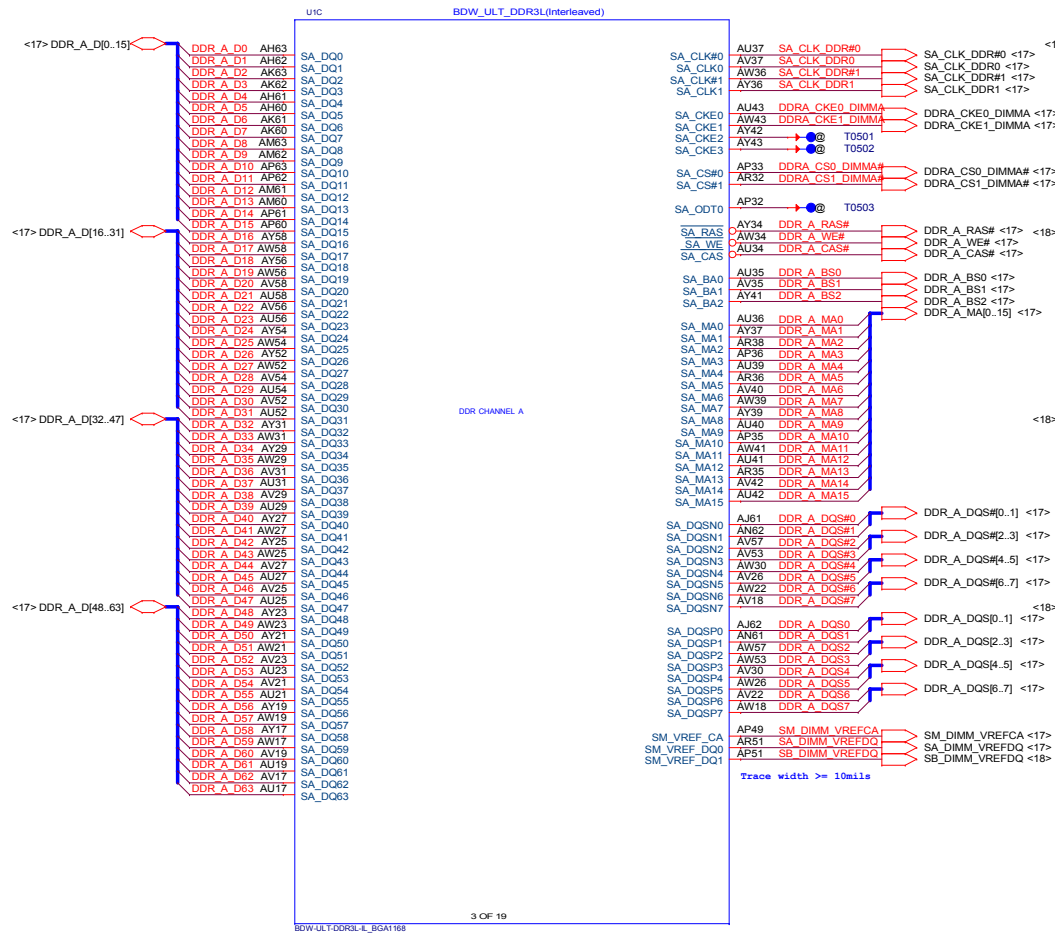
DDR3 Compensation Signals  
Trace width=12-15 mil, Spacing=20 mils  
Max trace length= 500 mil



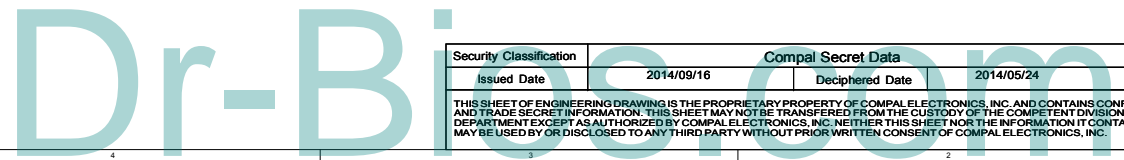
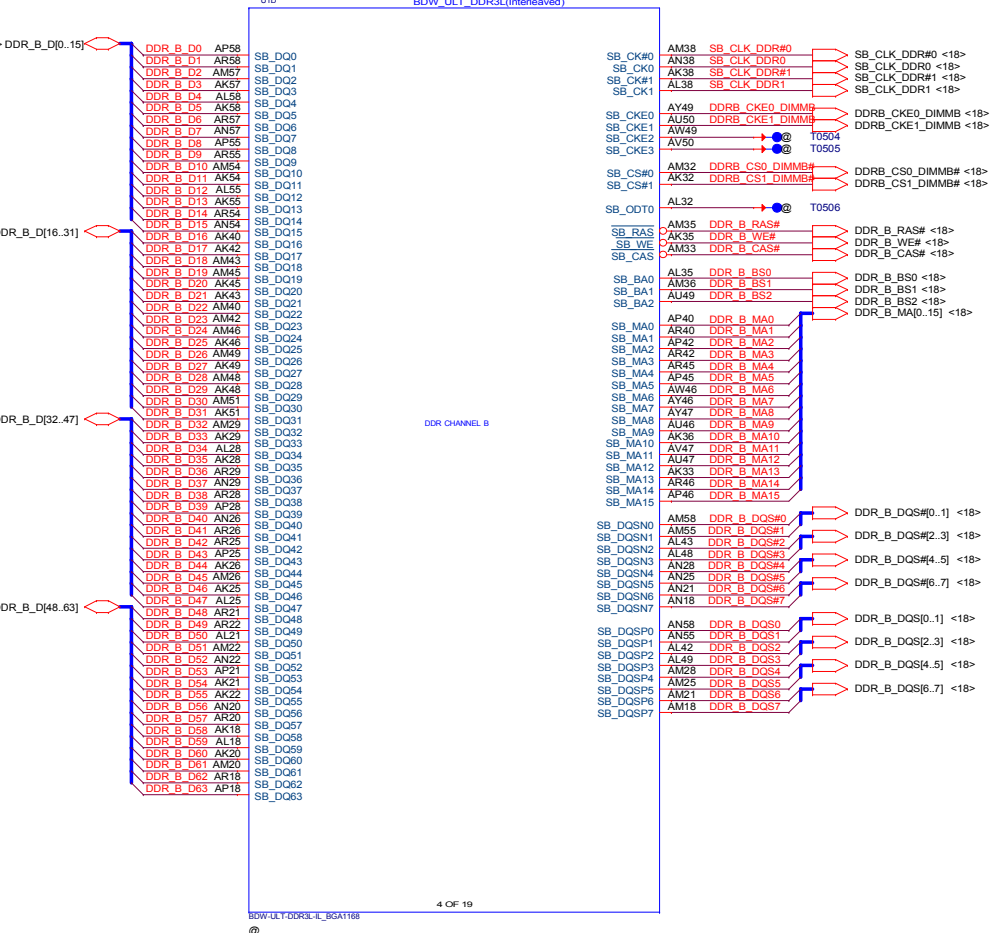
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DDR interleave routing

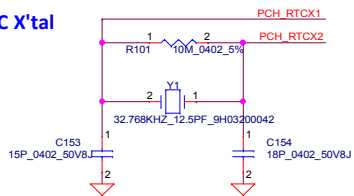


DDR interleave routing



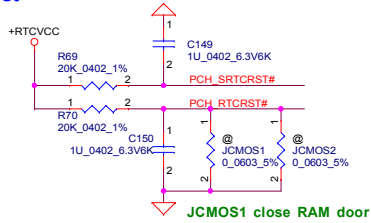
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Issued Date	2014/09/16	Deciphered Date	2014/05/24	BDW MCP(2/1) DDRIII	
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### RTC X'tal



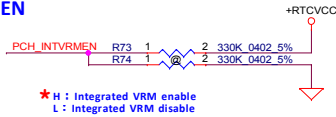
For BDW,  
Crystal change to SJ1000LV00 (ESR=50K Ohm)

### RTC Reset



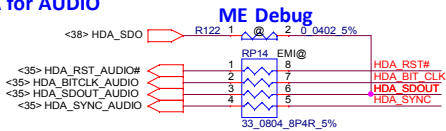
JCMOS1 close RAM door

### INTVRMEN

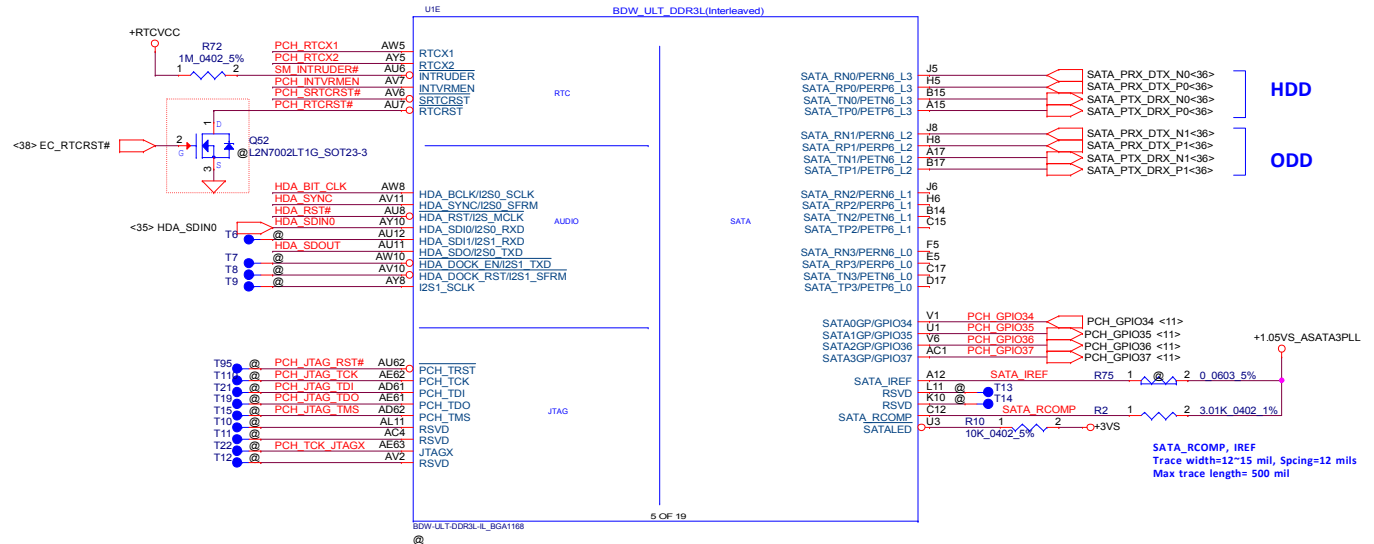
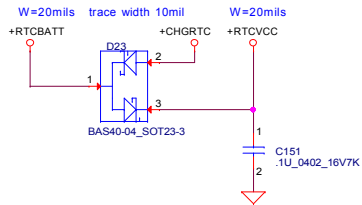


\* H : Integrated VRM enable  
L : Integrated VRM disable

### HDA for AUDIO

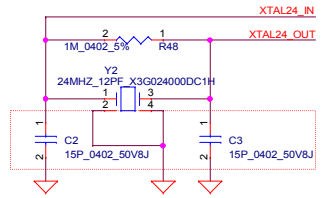


### RTC Battery

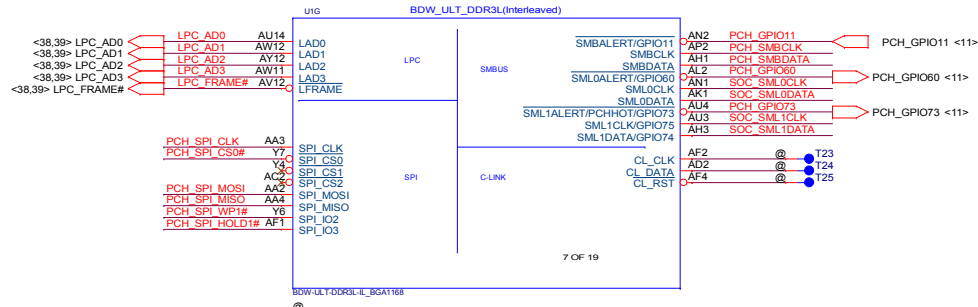
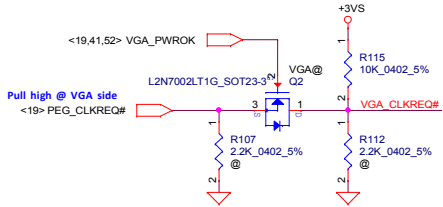
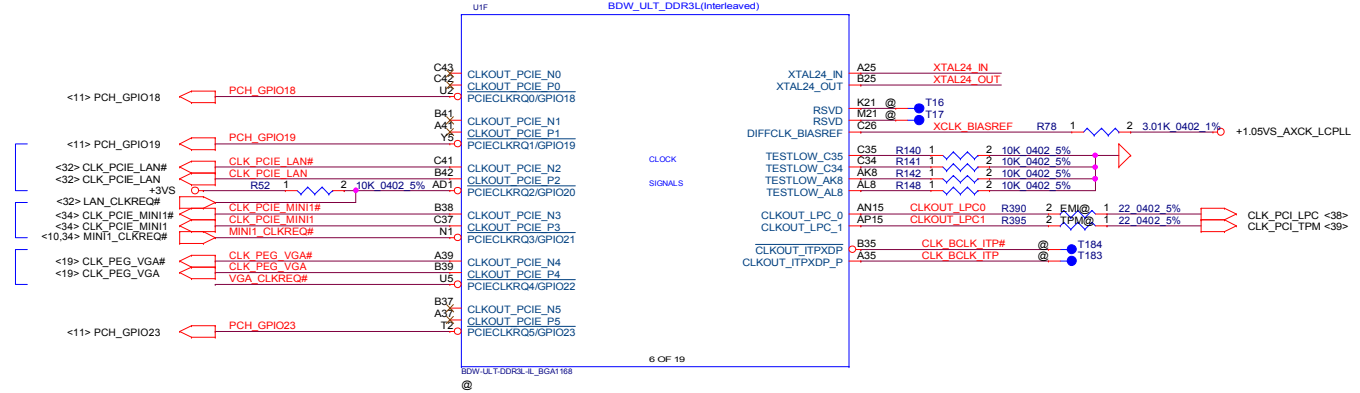


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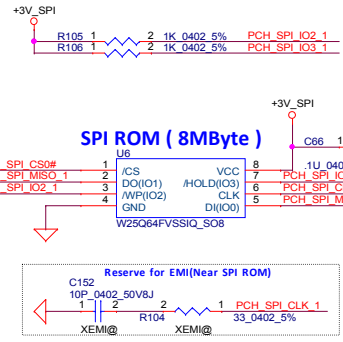




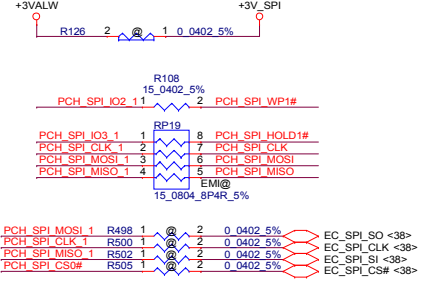
PCIE LAN  
WLAN  
VGA



SPI ROM

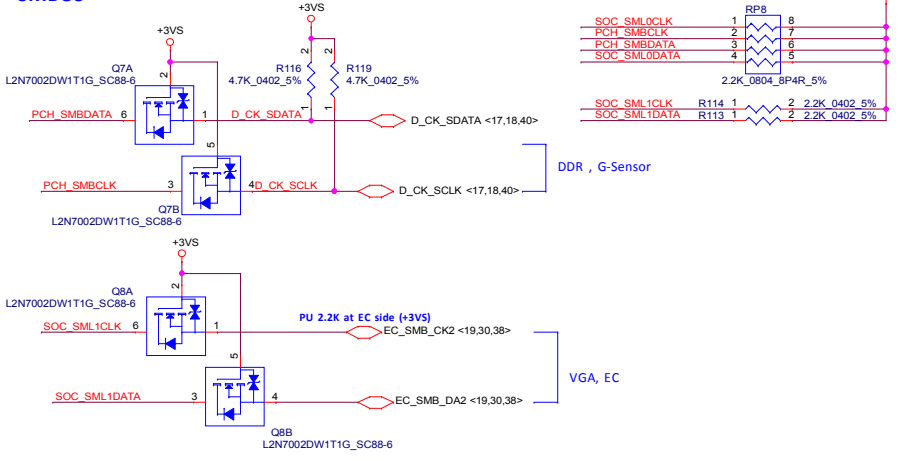


for Share EC ROM, +3VS change to +3VALW



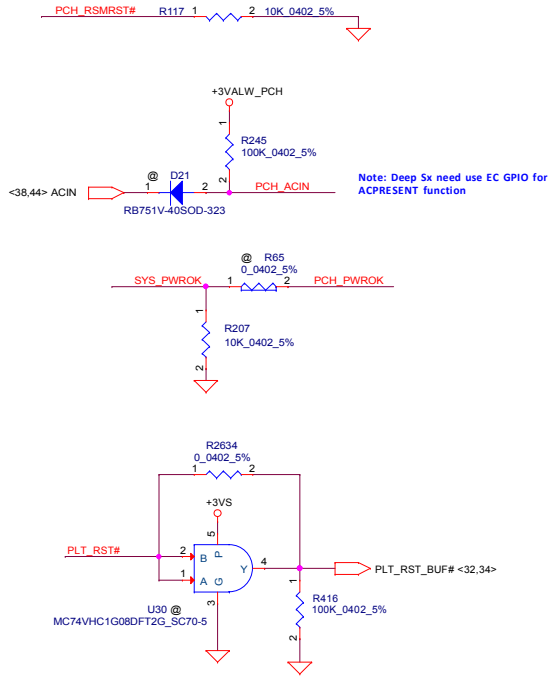
10/20: 2015 project not implement auto load, change R498, R500, R502, R502 to non-pop.

SMBUS

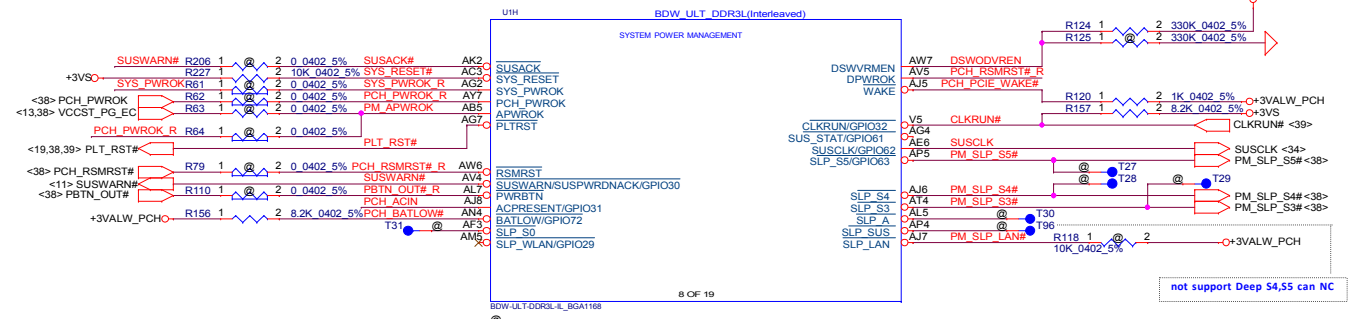


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# System Power Management

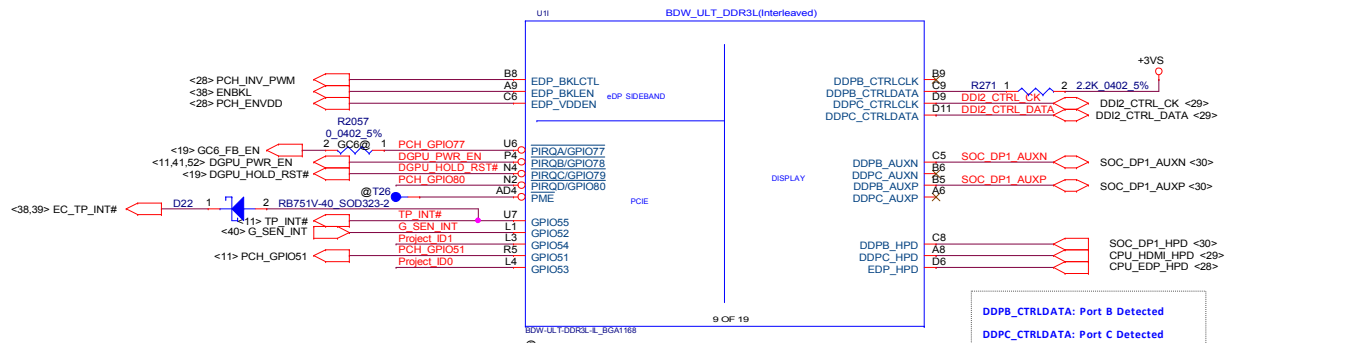


Note: Deep Sx need use EC GPIO for ACPRESENT function

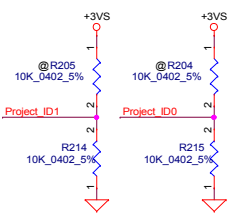
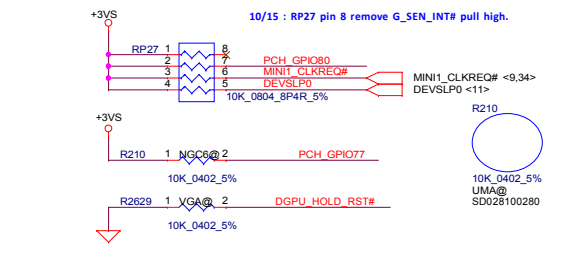


DSWODVREN - On Die DSW VR Enable  
 \* H : Enable(DEFAULT)  
 L : Disable

not support Deep S4,S5 can NC



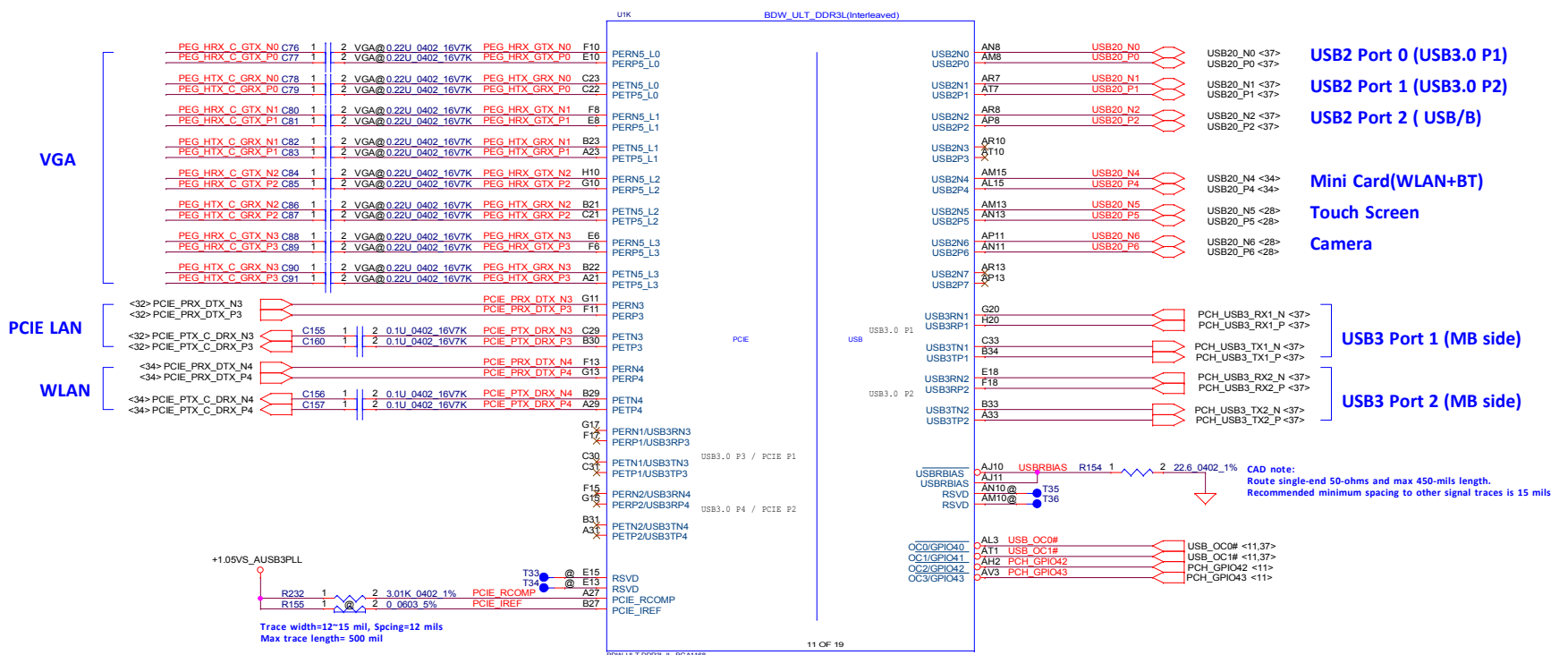
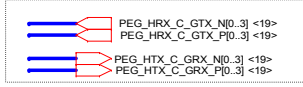
DDPB\_CTRLDATA: Part B Detected  
 DDPC\_CTRLDATA: Part C Detected  
 \* 1: Port B or C is detected  
 0: Port B or C is not detected  
 (Have internal PD)



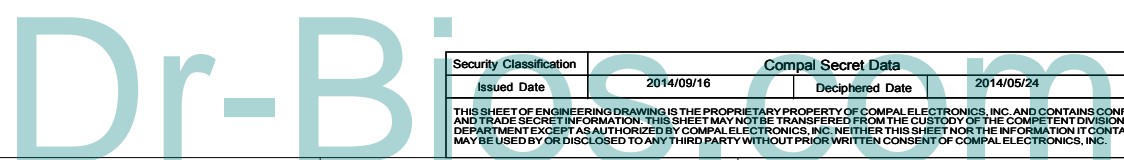
Project ID	Project_ID1 GPIO54	Project_ID0 GPIO53
* A4WAB	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

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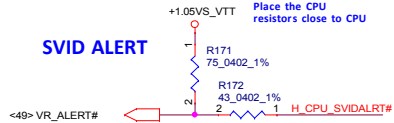




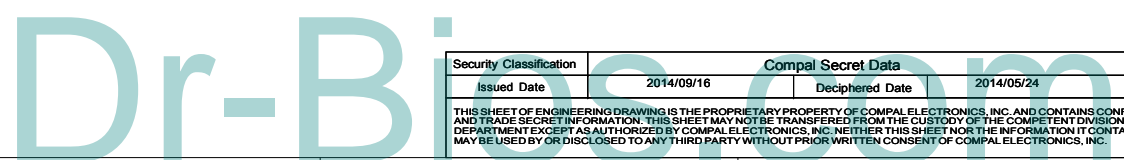
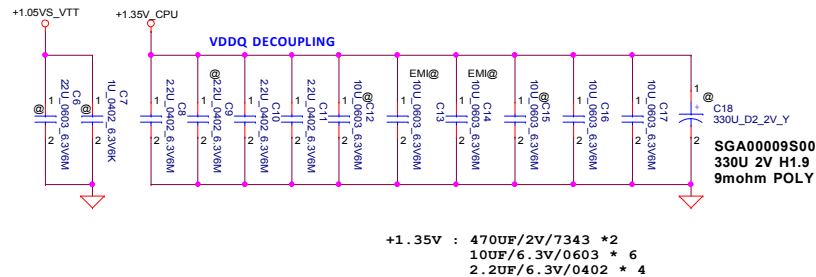
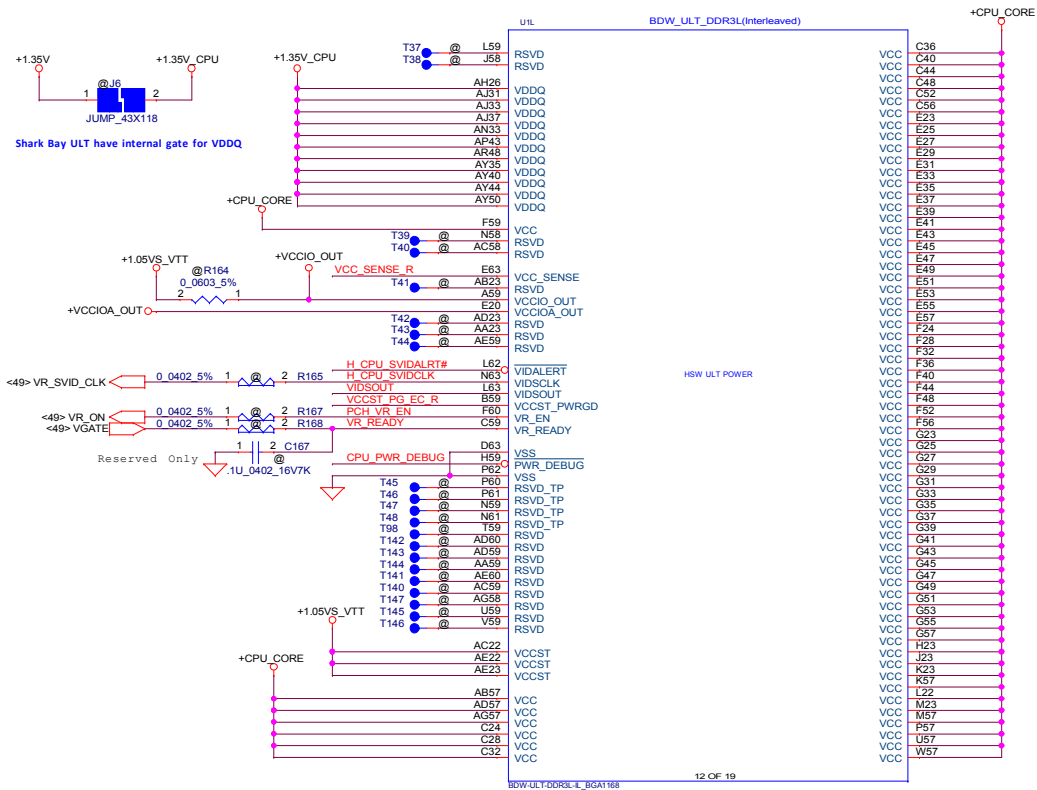
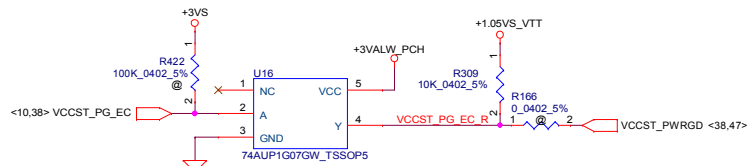
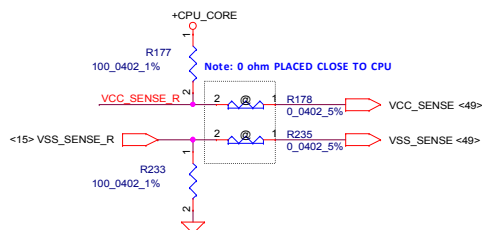
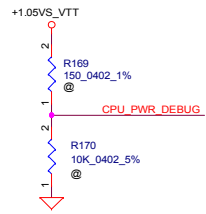
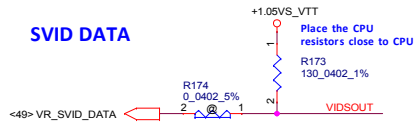
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**SVID ALERT**

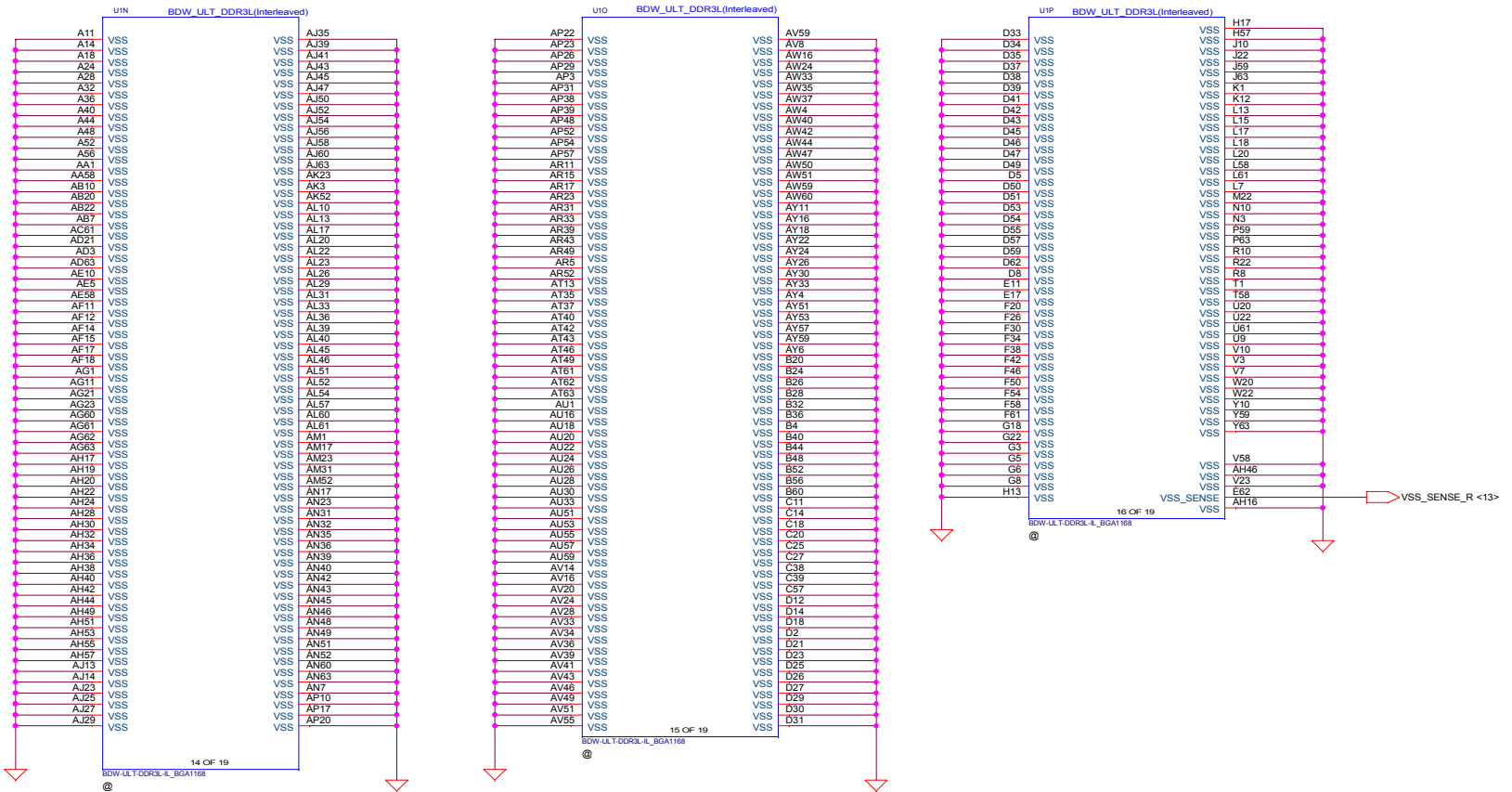


**SVID DATA**



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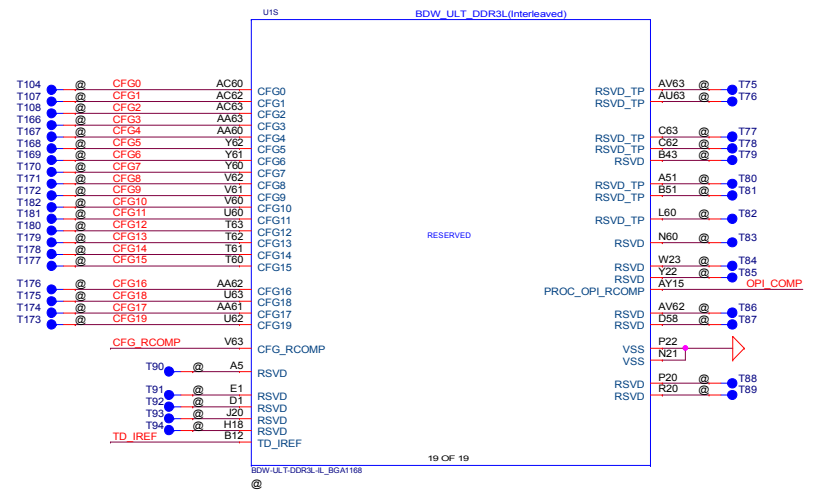
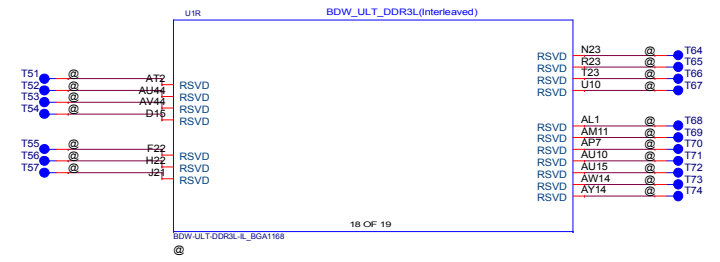
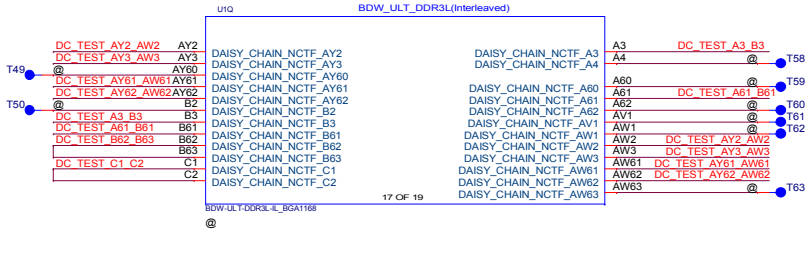




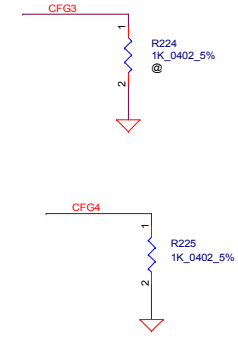
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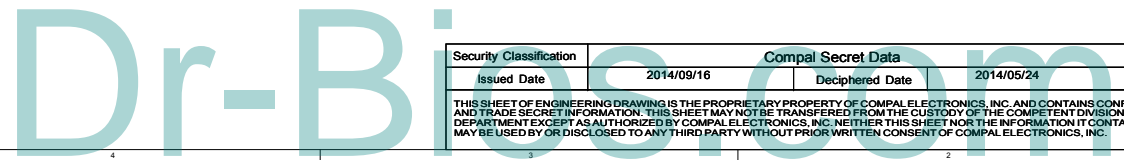
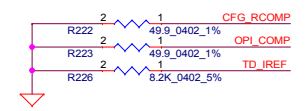


**CFG Straps for Processor**



Physical Debug Enable (DFX Privacy)	
CFG3	1 : DISABLED 0 : ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



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				Date: Wednesday, March 18, 2015	Sheet 16 of 56

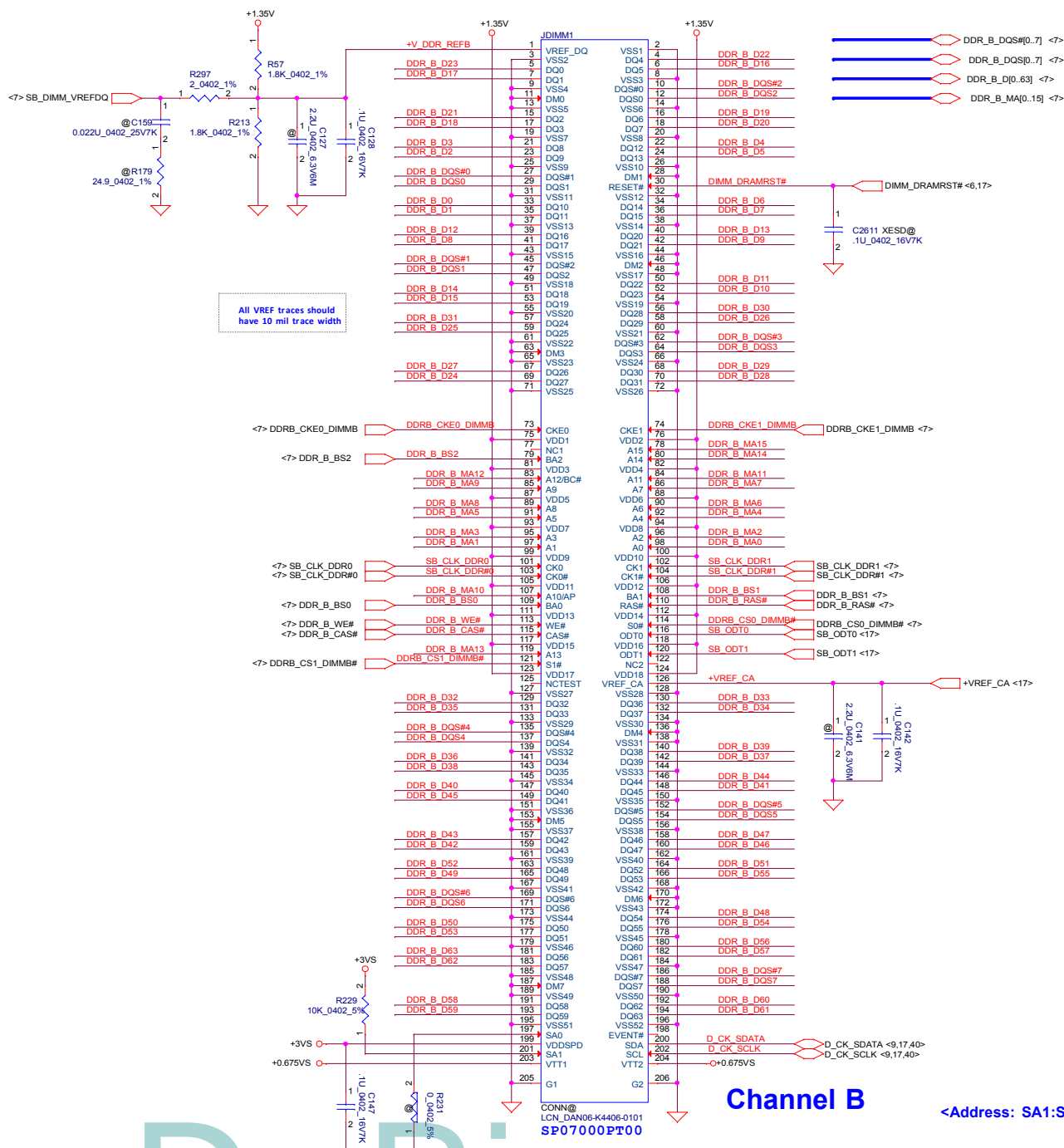




# Channel B

## DIMM\_2 H:4mm

### Reverse

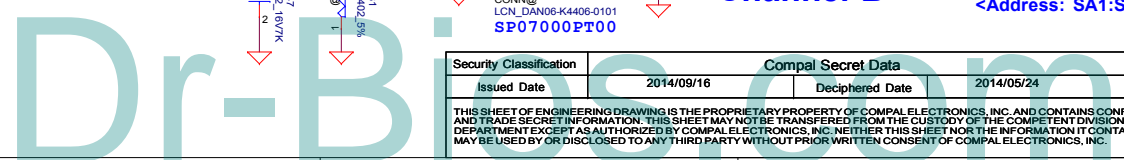


Layout Note:  
Place near J1DIMM2

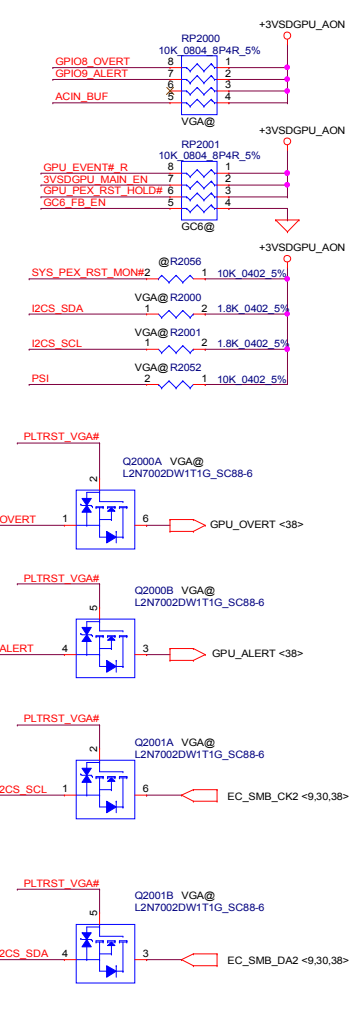
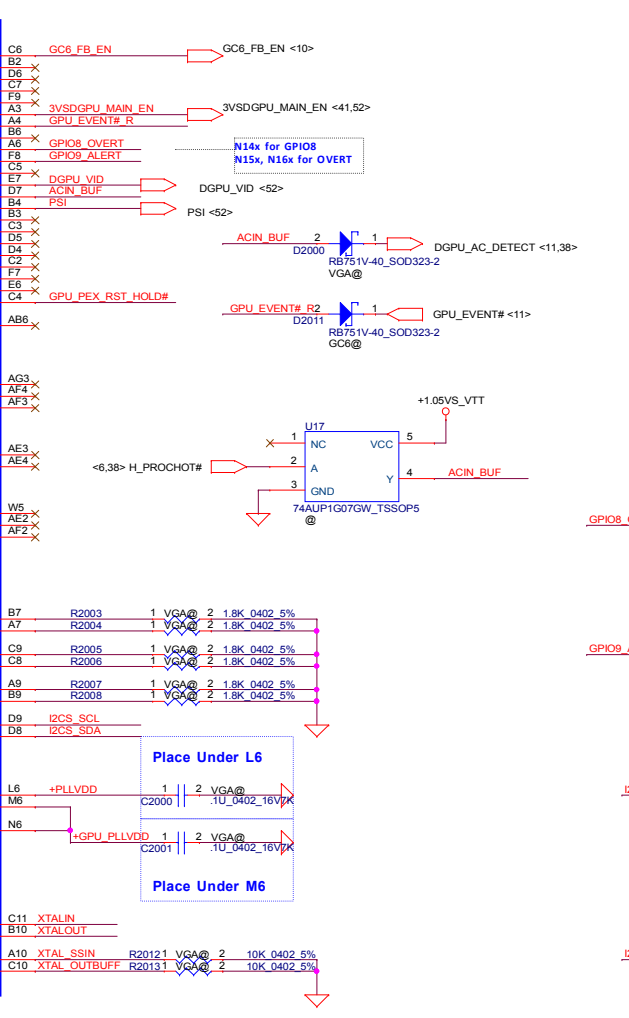
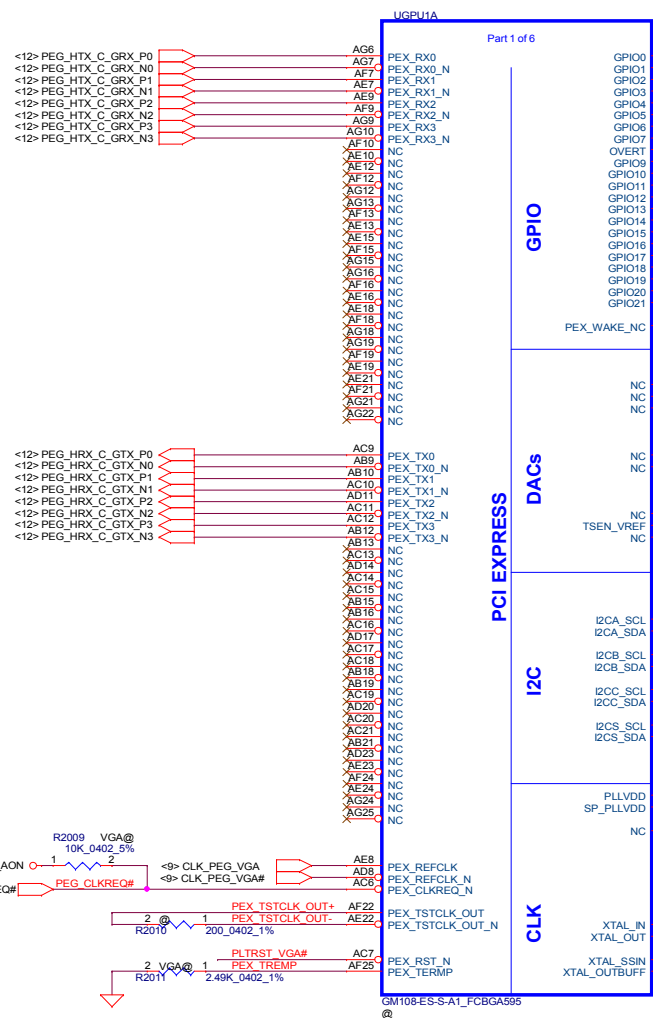
All VREF traces should  
have 10 mil trace width

Layout Note:  
Place near J1DIMM2.203,204

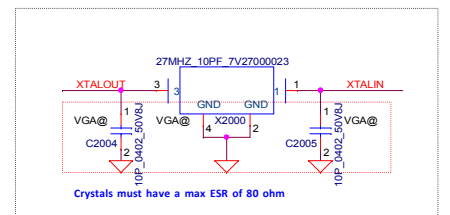
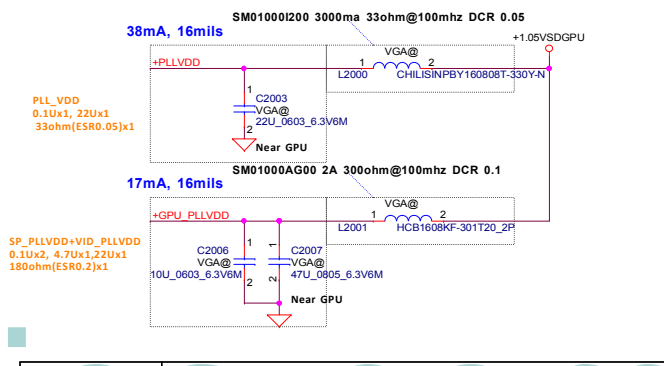
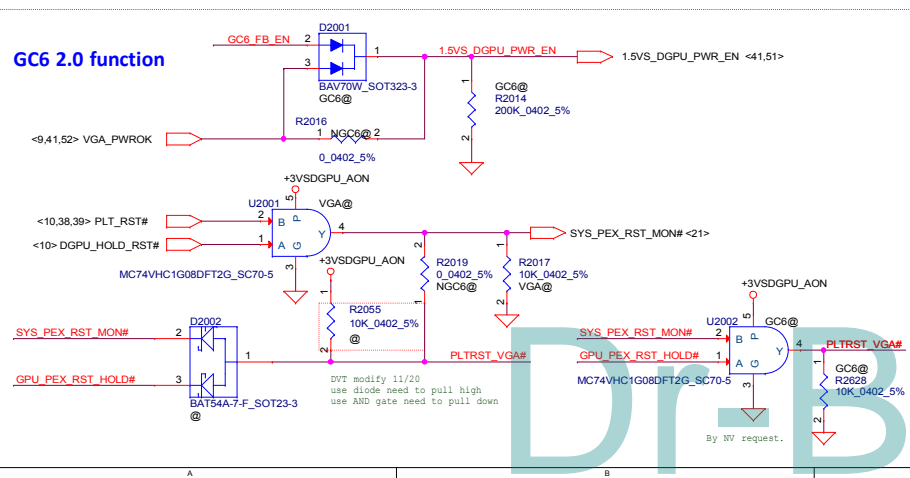
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Customer Number				Rev	
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Date				Sheet	
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GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		



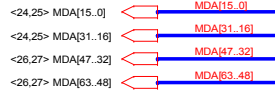
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<b>Issued Date</b>	2013/10/01	<b>Deciphered Date</b>	2014/05/24	<b>Title</b>	<b>N16X PEG &amp; GPIO 1/9</b>
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				<b>Rev</b>	0.2
				<b>Date</b>	Wednesday, March 18, 2015
				<b>Sheet</b>	19 of 56

# VRAM Interface



N16S-GT  
SGT@  
SA000087F10

R3 P/N:



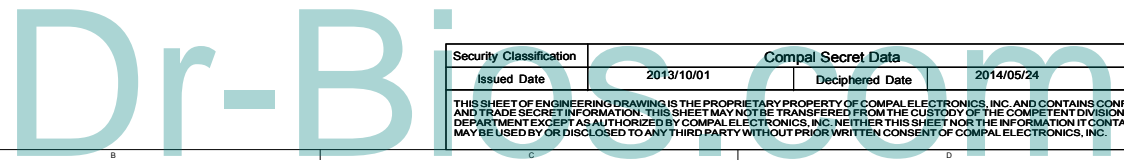
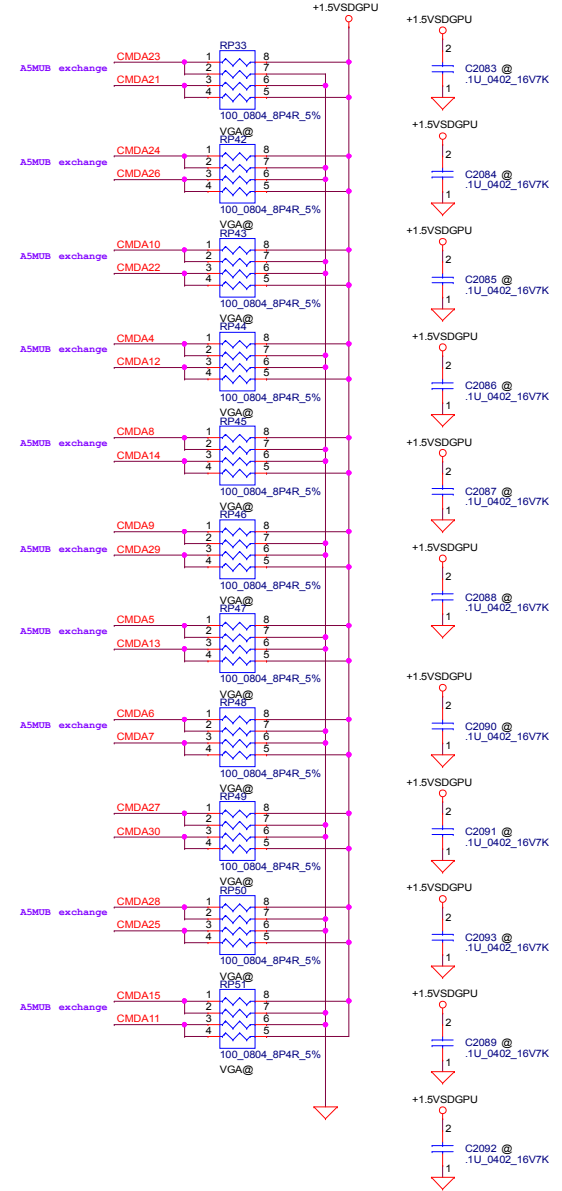
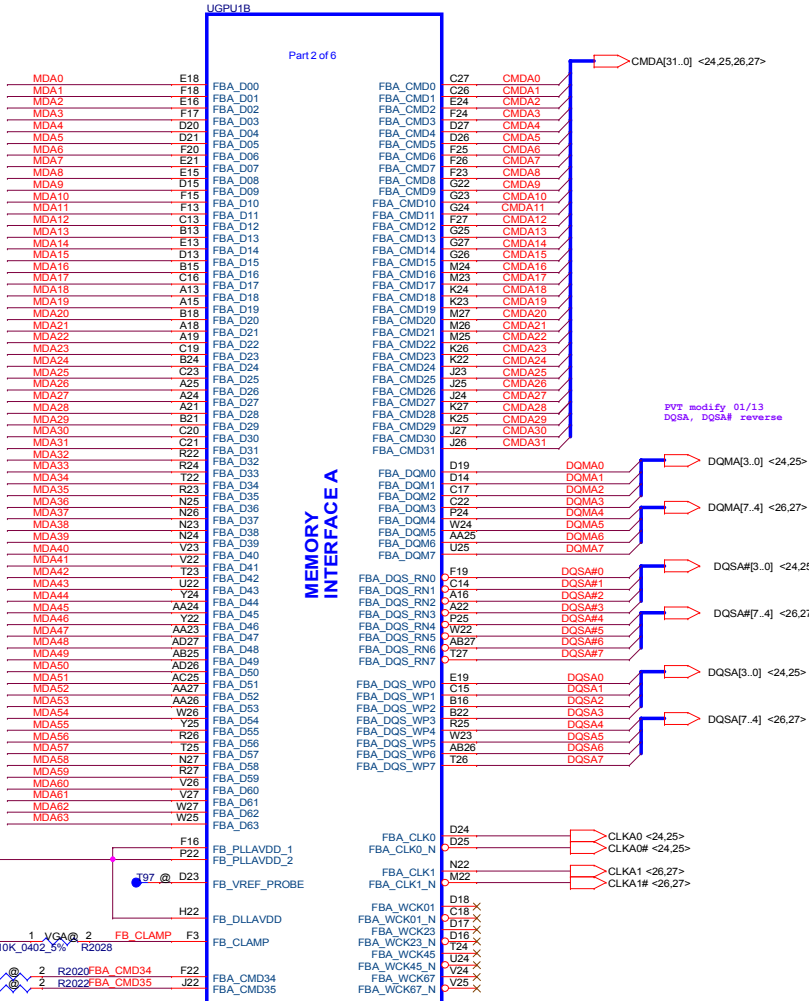
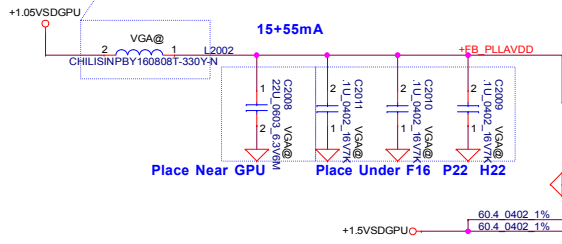
N16V-GM  
VGM@  
SA000088R20

R3 P/N:

NV 15x DG-06803-V03  
NV 16x DG-07158-V04

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	FBx_PL1_AVDD	0.1 µF X7R	040Z	2	Under GPU
	FB_DLL_AVDD Combined	22 µF X5R Bead Type 30 Ω (ESR=0.010 Ω)	0805	1	near GPU

SM010001200 3000ma 33ohm@100mhz DCR 0.05



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Date	Wednesday, March 18, 2015	Sheet	20	Rev	0.2

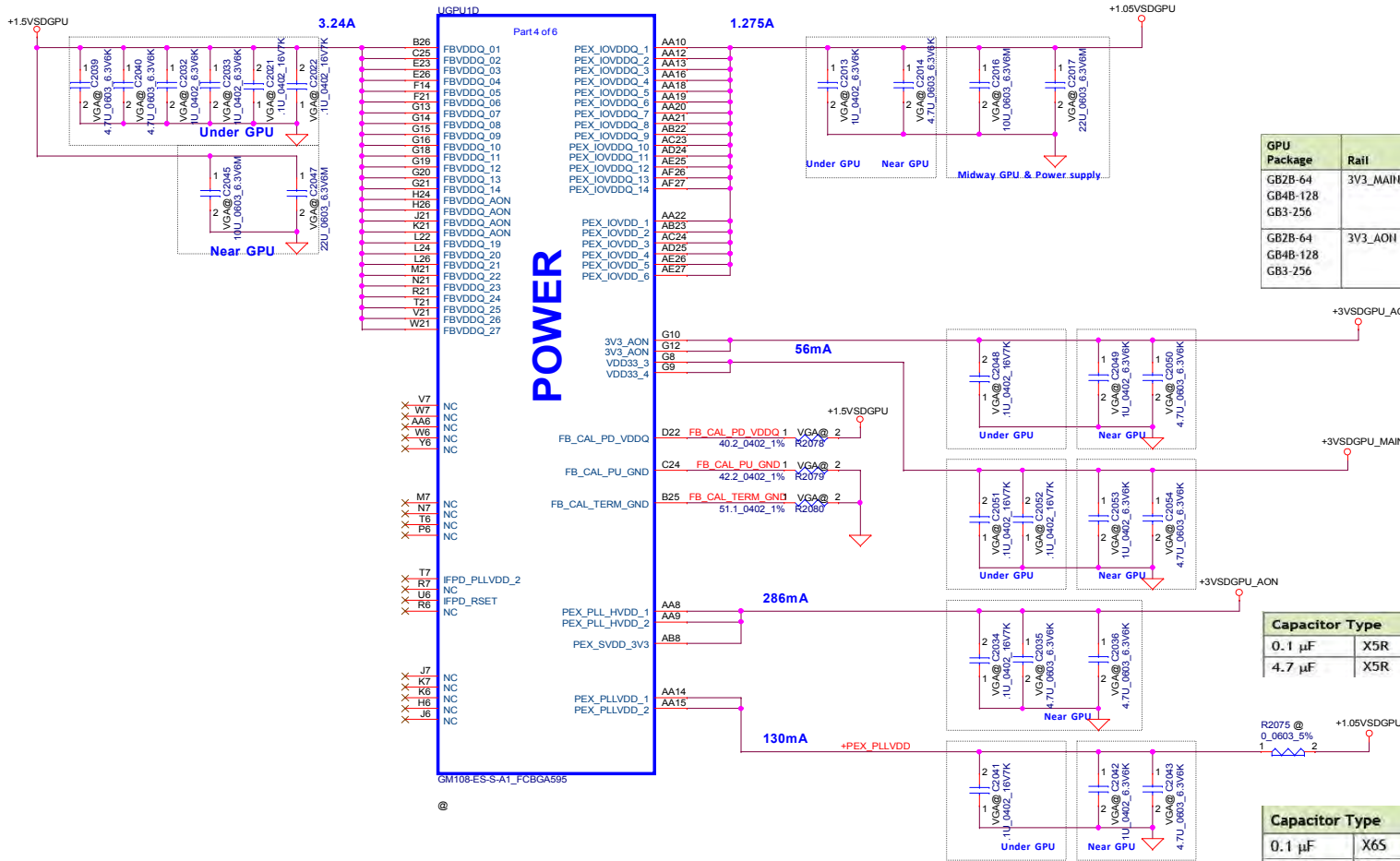




NV 15x DG-06803-V03  
 NV 16x DG-07158-V04

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64 DDR3	0.1µF	X7R 0402	2	Under GPU
	1µF	X7R 0603	2	Under GPU
	4.7µF	X6S 0603	2	Under GPU
	10µF	X5R 0805	1	Near GPU
	22µF	X5R 0805	1	Near GPU

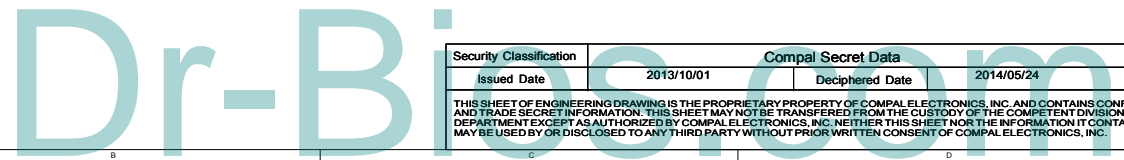
GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0µF	X6S 0402	1	Under GPU
	4.7µF	X6S 0603	1	Near GPU
	10µF	X5R 0805	1	Midway between GPU and Power Supply
	22µF	X5R 0805	1	Midway between GPU and Power Supply

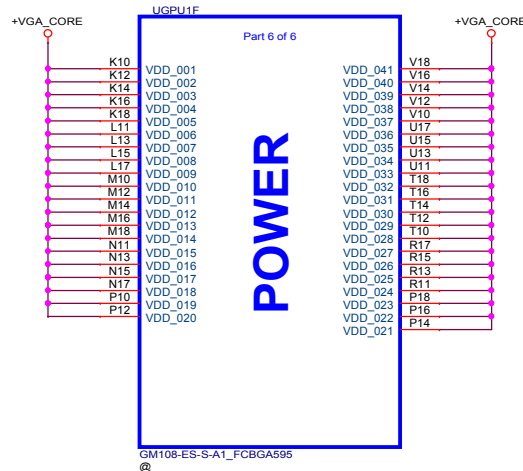
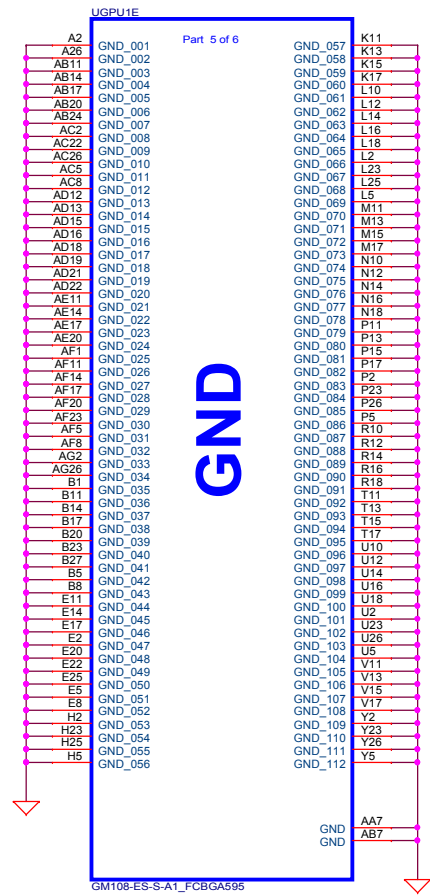


GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIH	0.1µF	X6S 0402	2	Under GPU
		1µF	X5R 0603	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_A0H	0.1µF	X6S 0402	1	Under GPU
		1µF	X5R 0603	1	Near GPU

Capacitor Type	Footprint	Population	Location
0.1µF	X5R	0402	1
4.7µF	X5R	0603	2

Capacitor Type	Footprint	Population	Location
0.1µF	X6S	0402	1
1.0µF	X5R	0603	1
4.7µF	X5R	0805	1





**NV 15x DG-06803-V03**  
**NV 16x DG-07158-V04**

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments	
GB2B-64	4.7 $\mu$ F	X65	0603	10	10	Under GPU
	1 $\mu$ F	X65	0402	4	4	Under GPU
	47 $\mu$ F	X5R	0805	1	1	Near GPU
	22 $\mu$ F	X5R	0805	1	1	Near GPU
	4.7 $\mu$ F	X5R	0805	5	5	Near GPU
	330 $\mu$ F	POS	7343	1	1	Near GPU ESR $\leq$ 6 m $\Omega$

**DA-07312-V02**

Table 6. EDP-Peak<sup>3</sup>

Products	VRM Type	GPU Core	GPU FBIO		FB Total <sup>1,5</sup>	1.05V Total <sup>2</sup>
		(A)	(A)	(A)	(A)	(A)
H165-GT	DDR3/L	51	2.56	2.18	4.08	3.63
H165-GM	DDR3/L	32	2.56	2.18	4.08	3.62
H165-LP	DDR3L	29	N/A	2.13	N/A	3.54

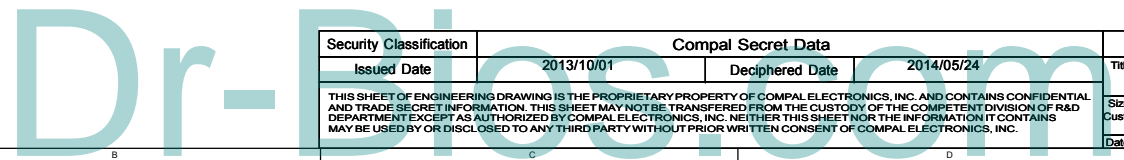
- Notes:
1. FB Total = GPU FBIO + VRAM IO + VRAM Core = FBVDD + FBVDDQ
  2. 1.05V Total includes the PCIe and other 1.05V power rails.
  3. Worst case current is observed at the temperature of the GPS Thermal Control Limit defined in Table 3.
  4. Power supply rail voltages set to maximum DC tolerance.
  5. VRAM Total power is for reference only. For absolute ratings, please contact VRAM manufacturer.

**DA-07314-V02**

Table 6. EDP-Peak<sup>3</sup>

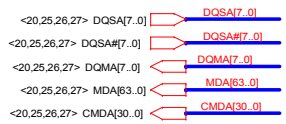
Products	VRM Type	GPU Core	GPU FBIO	FB Total <sup>1,5</sup>	1.05V Total <sup>2</sup>
		(A)	(A)	(A)	(A)
H16V-GM	DDR3/L	40.97	3.87	5.86	1.74

- Notes:
1. FB Total = GPU FBIO + VRAM IO + VRAM Core = FBVDD + FBVDDQ
  2. 1.05V Total includes the PCIe and other 1.05V power rails.
  3. Worst case current is observed at the temperature of the GPS Thermal Control Limit defined in Table 3.
  4. Power supply rail voltages set to maximum DC tolerance.
  5. VRAM Total power is for reference only. For absolute ratings, please contact VRAM manufacturer.



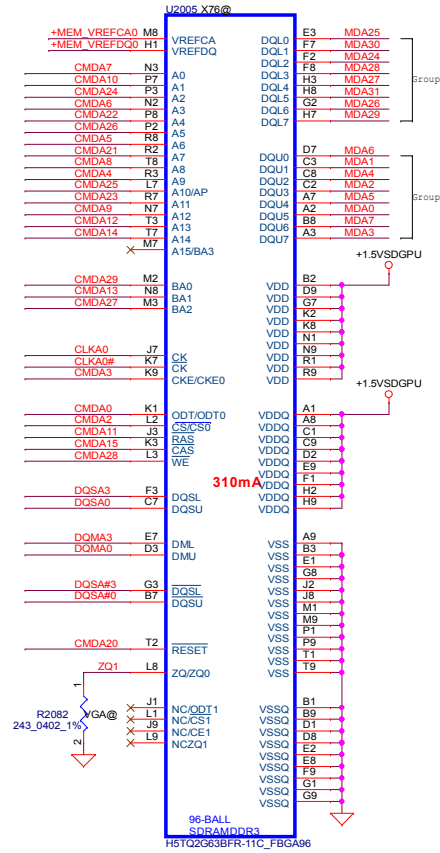
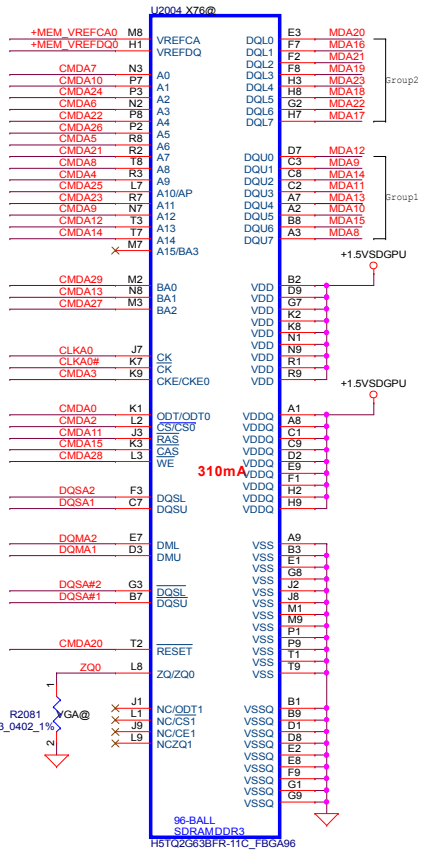
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				A4WAB M/B LA-C341P	
				Date:	Wednesday, March 18, 2015
				Sheet	23 of 56
				Rev	0.2

# VRAM DDR3 chips



## Lower Rank 0 BOT SIDE

VRAM P/N: SA00006E840

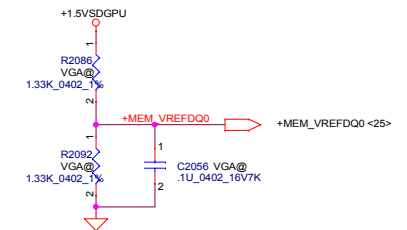
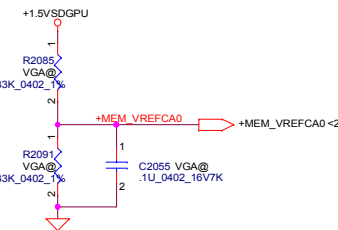
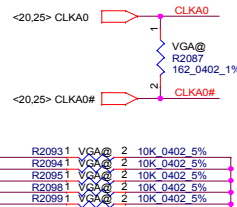
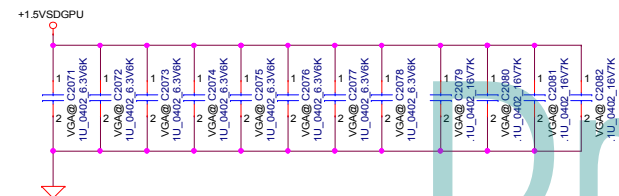


Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type	Population		
	FBVDDQ	FBVDD	Location
FBVDD/Q Combined			
0.1 μF	X7R	0402	2 Under DRAM
1.0 μF	X7R	0603	4 Under DRAM
10 μF	X5R	0805	0 Close to DRAM

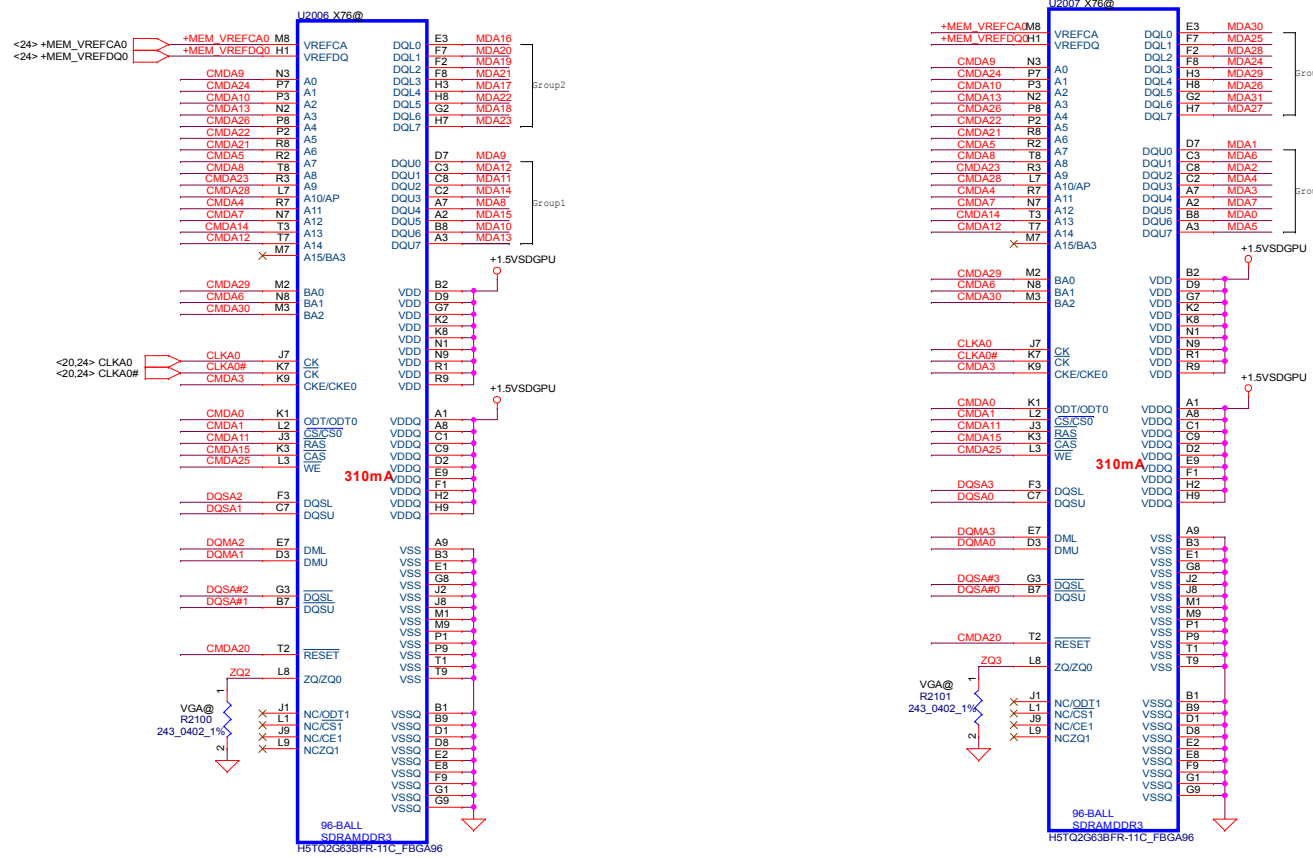




# VRAM DDR3 chips

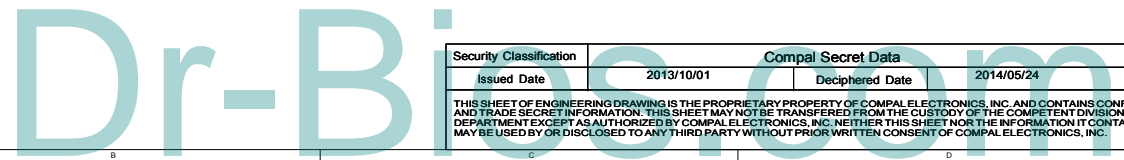
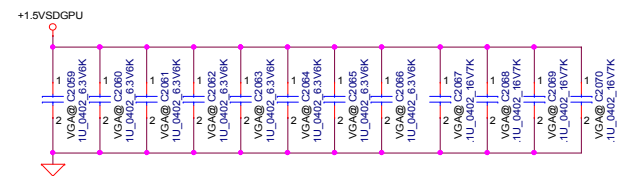
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- <20,24,26,27> DQSA# [7..0] → DQSA# [7..0]
- <20,24,26,27> DQMA [7..0] → DQMA [7..0]
- <20,24,26,27> MDA [63..0] → MDA [63..0]
- <20,24,26,27> CMDA [30..0] → CMDA [30..0]

## Lower Rank 1 TOP SIDE

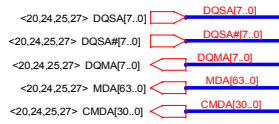


Mode E Address	Rank0		Rank1	
	0...31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
CMD31	Not Available			

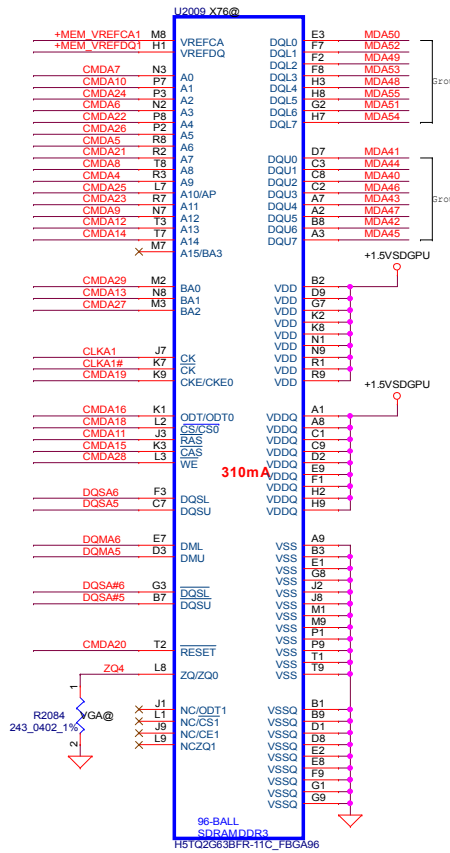
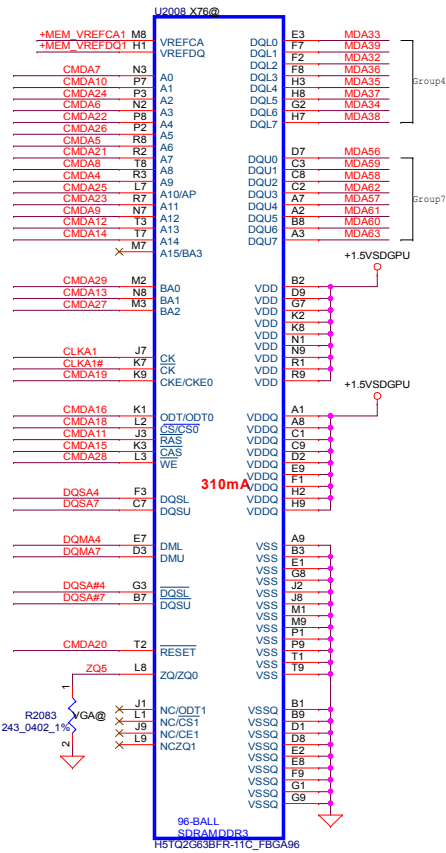
Command Bit	Default	Pull-down
ODT#	10k	
CKE#	10k	
RST	10k	
CS*	No Termination	



# VRAM DDR3 chips

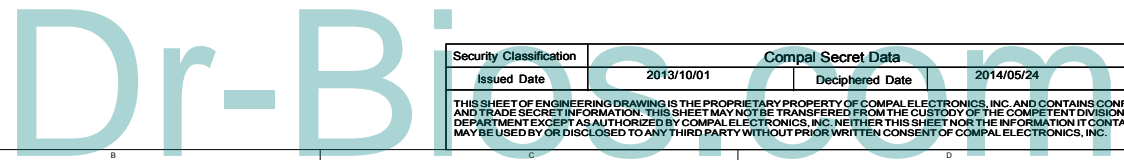
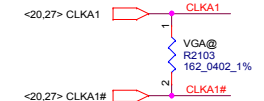
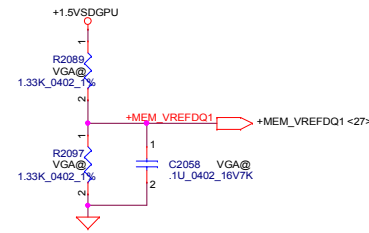
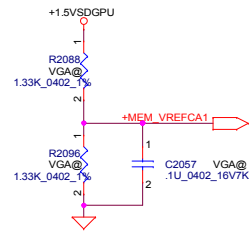
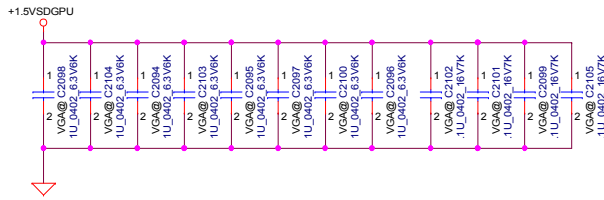


## Upper Rank 0 BOT SIDE

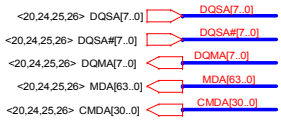


Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

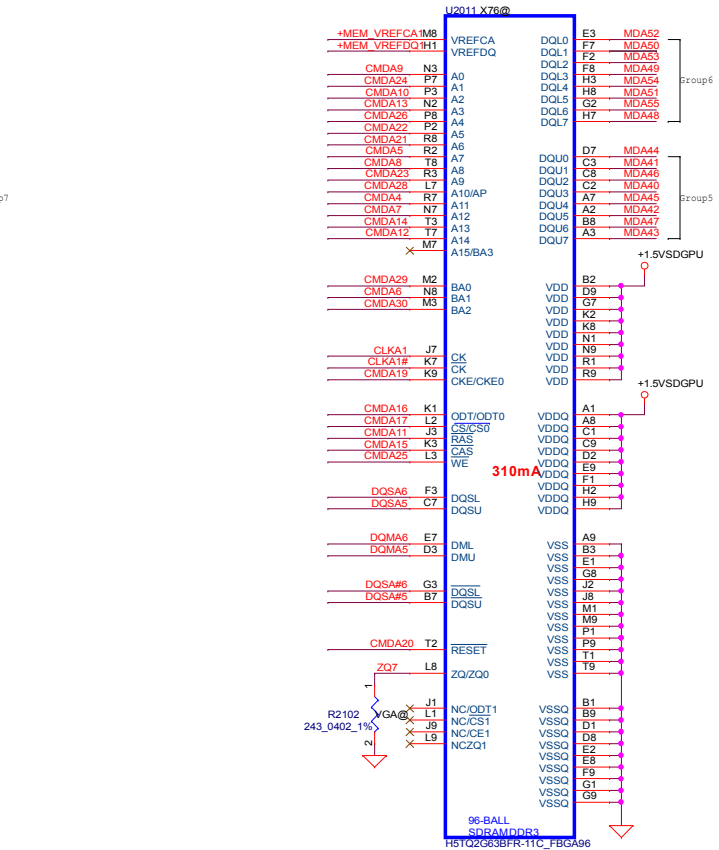
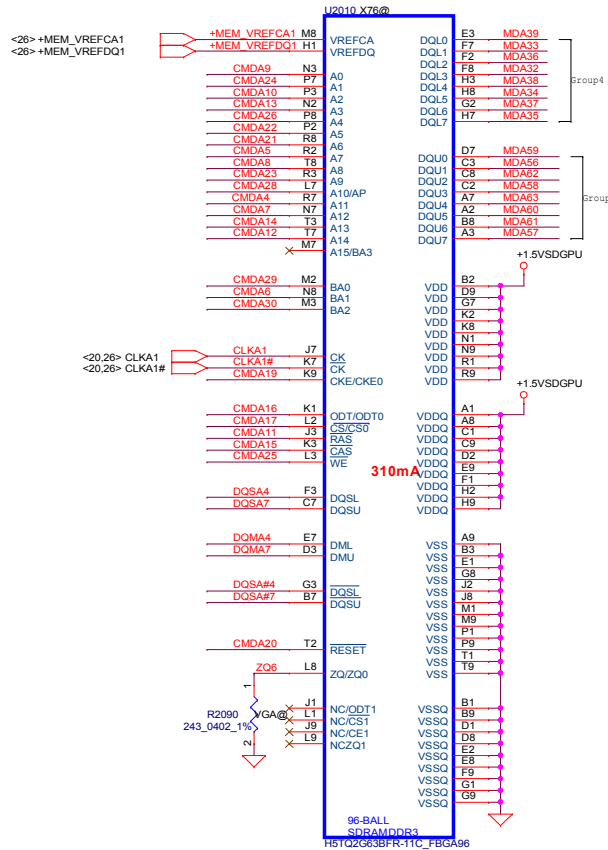
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



# VRAM DDR3 chips



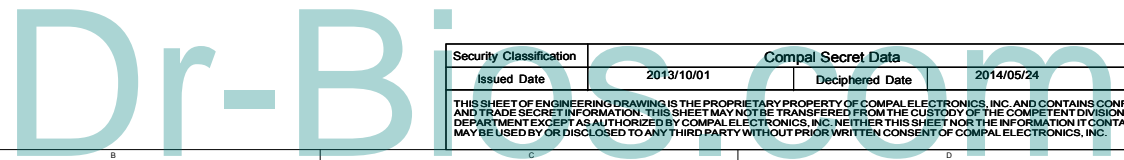
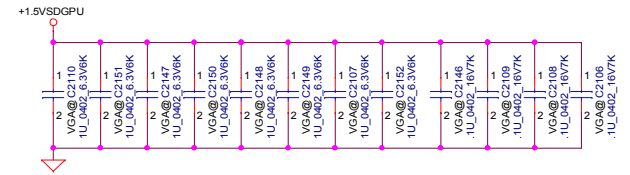
## Upper Rank 1 TOP SIDE



ASMUB SWAP

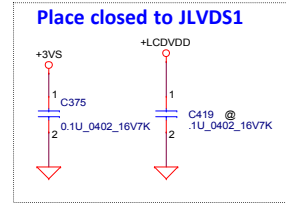
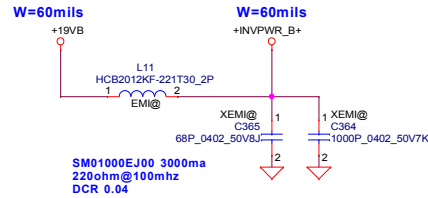
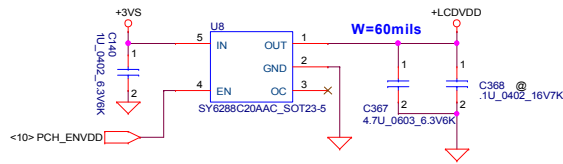
Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

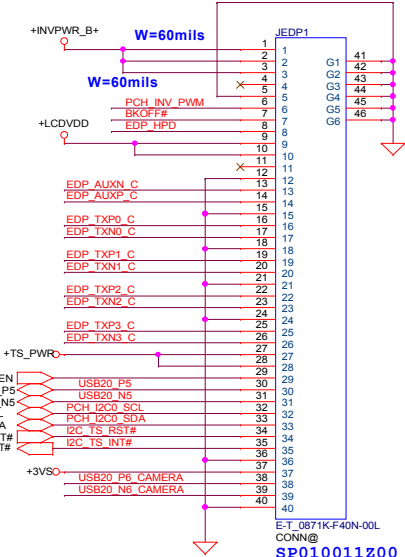
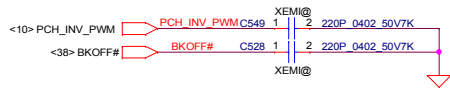
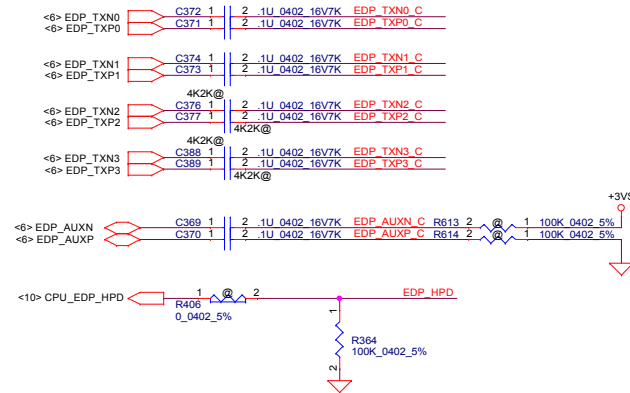


# EDP / LVDS conn.

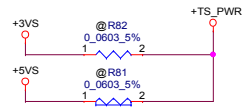
## LCD POWER CIRCUIT



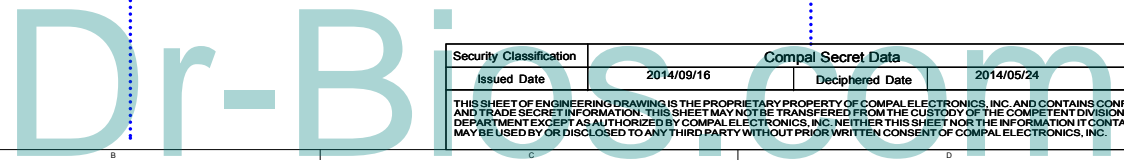
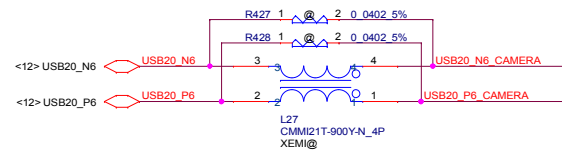
Follow A4QAS pin assignment  
LCD/ LED PANEL Conn.



## Touch Screen

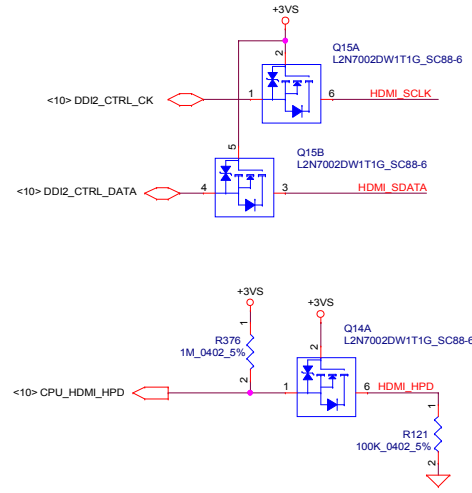
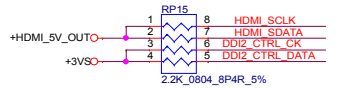
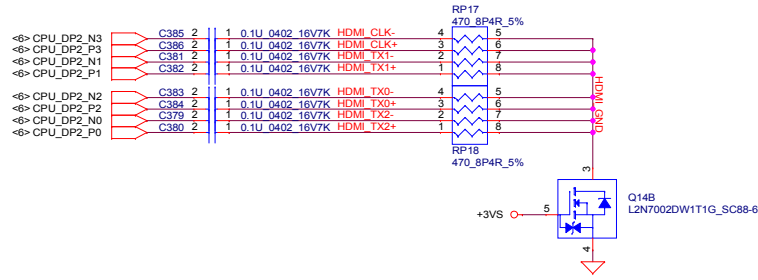
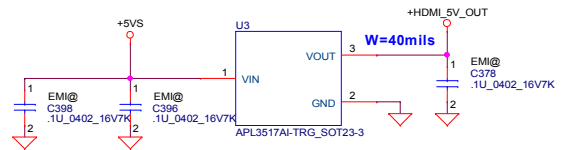


## Camera

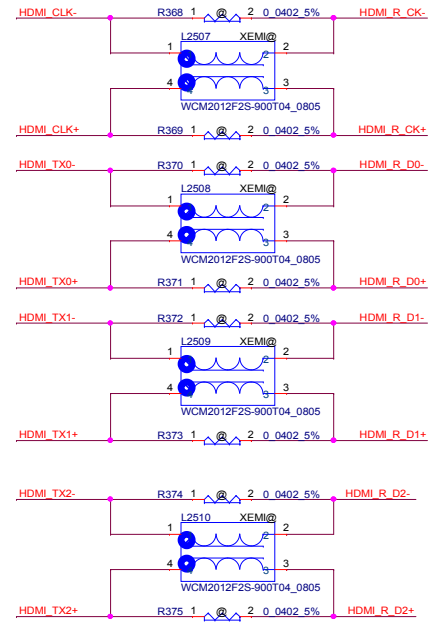


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				A4WAB M/B LA-C341P	
				Date	Wednesday, March 18 2015
				Sheet	28 of 56

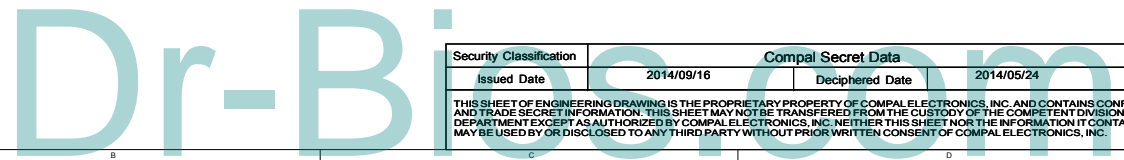
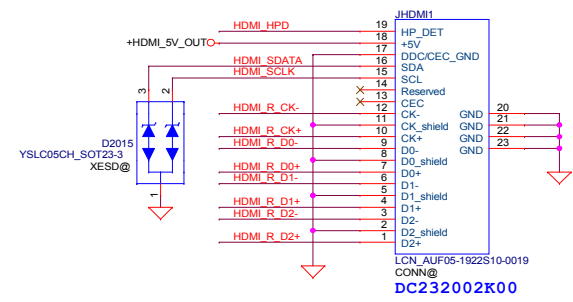
# HDMI conn.



SM70001310 400ma 90ohm@100mhz DCR 0.3

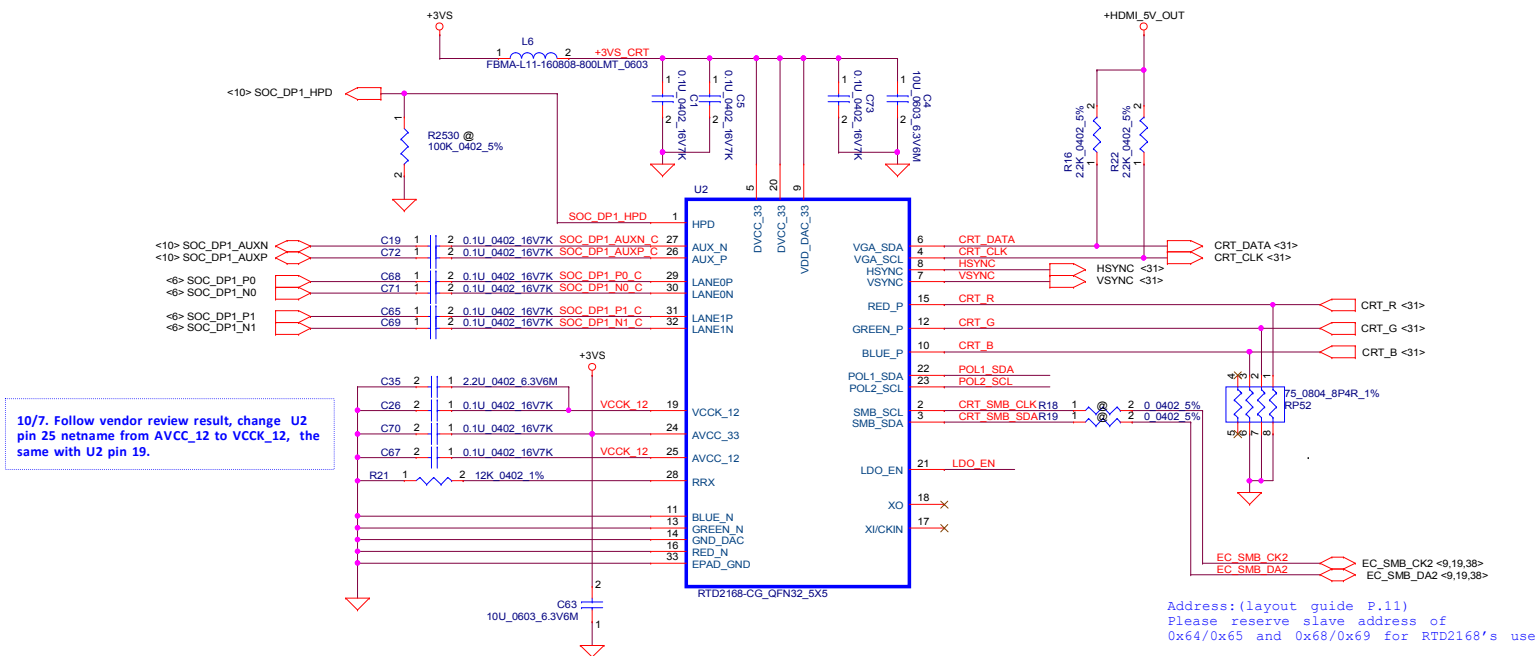


## HDMI connector



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Date:	Wednesday, March 18, 2015	Sheet	29	of	56	Rev	0.2

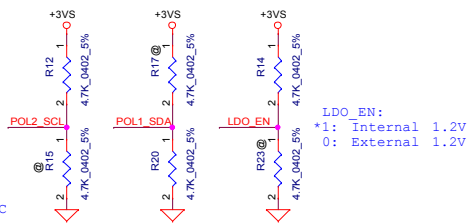
# DP to VGA Realtek RTD2168



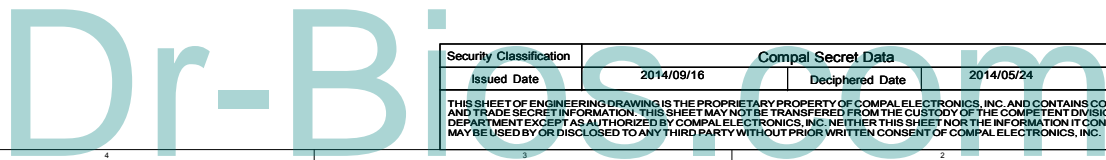
10/7. Follow vendor review result, change U2 pin 25 netname from AVCC\_12 to VCCCK\_12, the same with U2 pin 19.

			POL_SDA
		0	1
POL_SCL	0	X	EP
	1	*ROM	EEPROM

ROM: Internal ROM  
 EP: Programmed external EC  
 EEPROM: External ROM

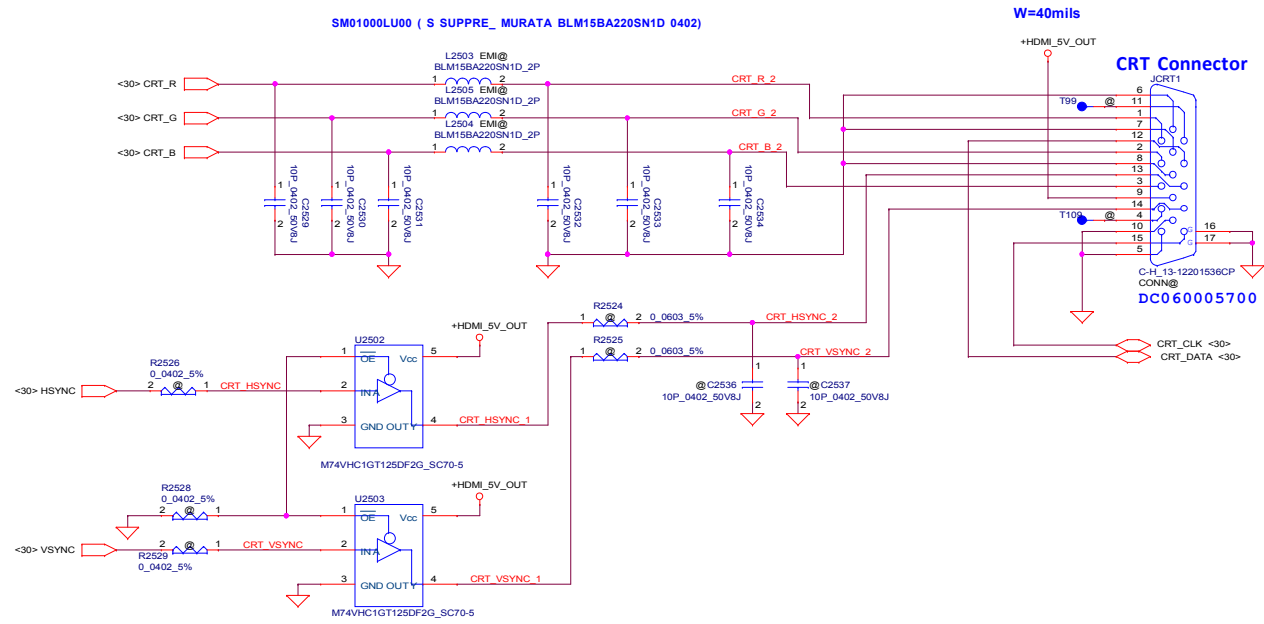


LDO\_EN:  
 \*1: Internal 1.2V  
 0: External 1.2V



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Date	Wednesday, March 18 2015	Sheet	30	of	56

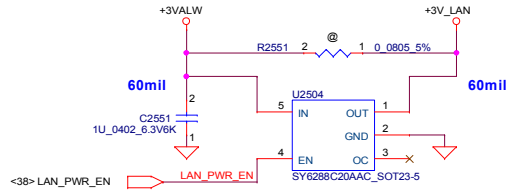
# CRT conn.



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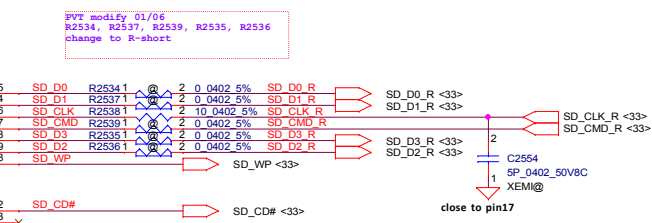
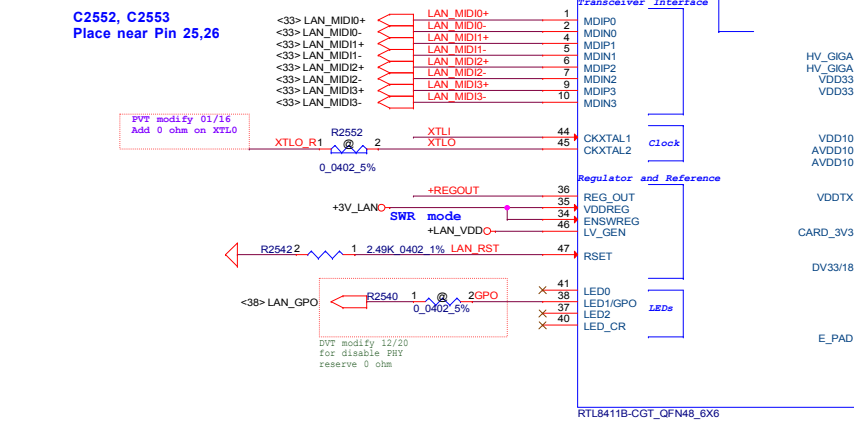
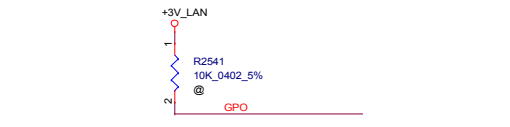
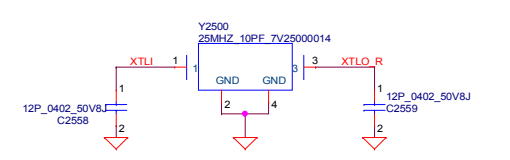
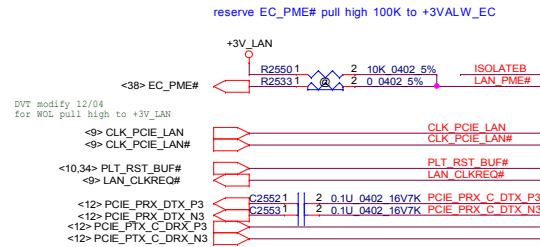
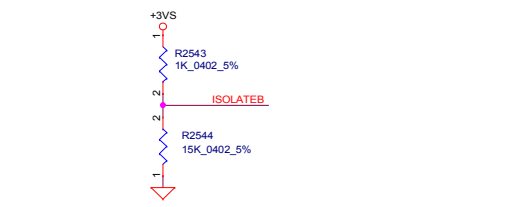
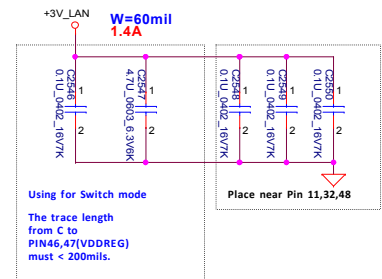
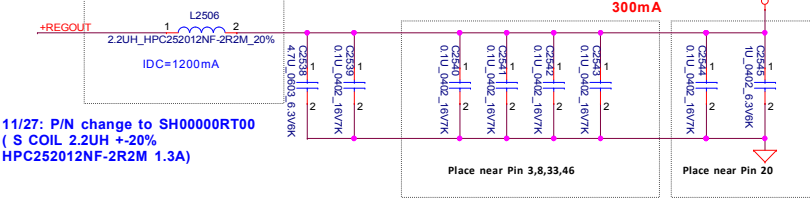
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Size	Customer	Document Number	Rev	Date	
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# LAN-RTL8411B

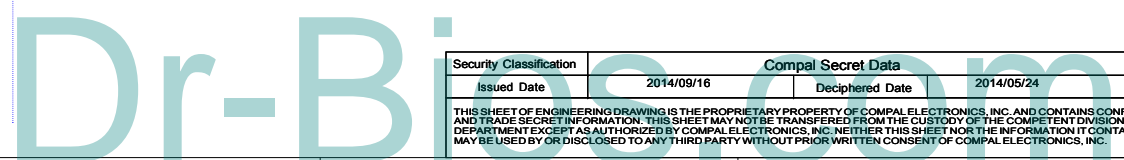
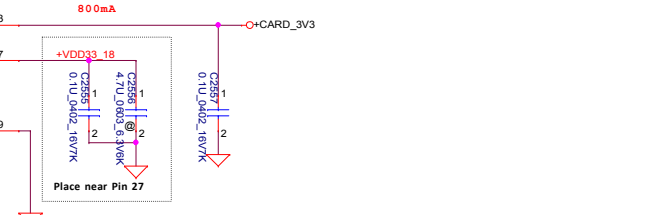


**From EC**  
 High active.  
 EN threshold voltage min:1.2V typ:1.6V max:2.0V  
 Current limit threshold 1.5~2.8A  
 +3V\_LAN Rising time must >0.5ms and <100ms

**Using for Switch mode**  
 The trace length from Lx to PIN48 (REGOUT) and from C to Lx must < 200mils.

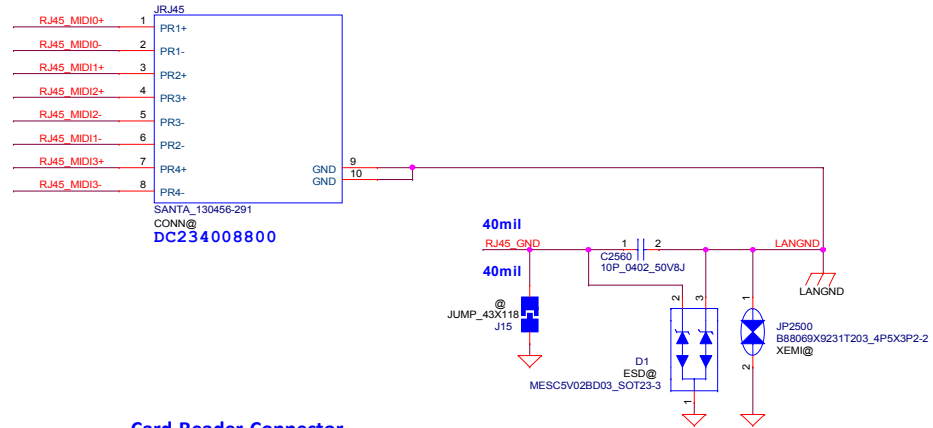
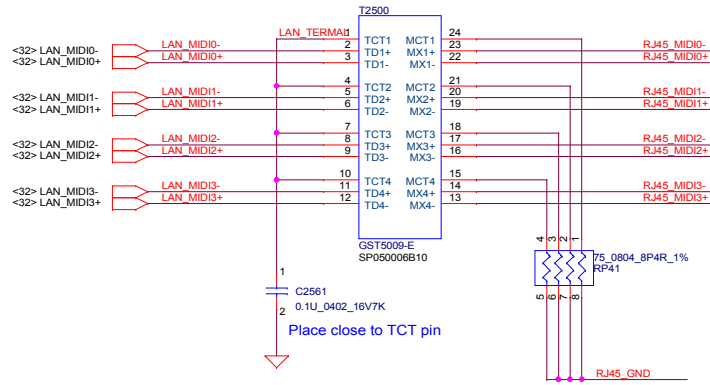


	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

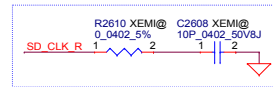
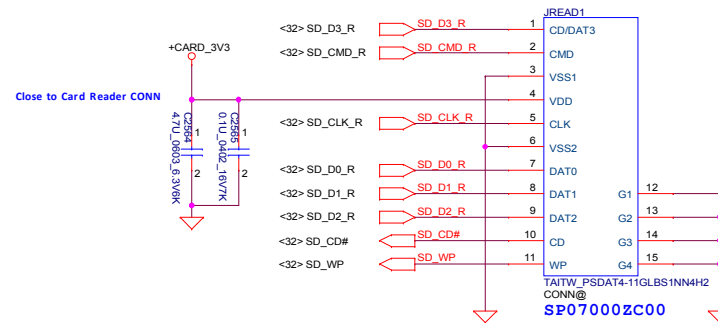




# RJ45 / Card Reader conn.



Card Reader Connector



Close to JREAD1 for EMI

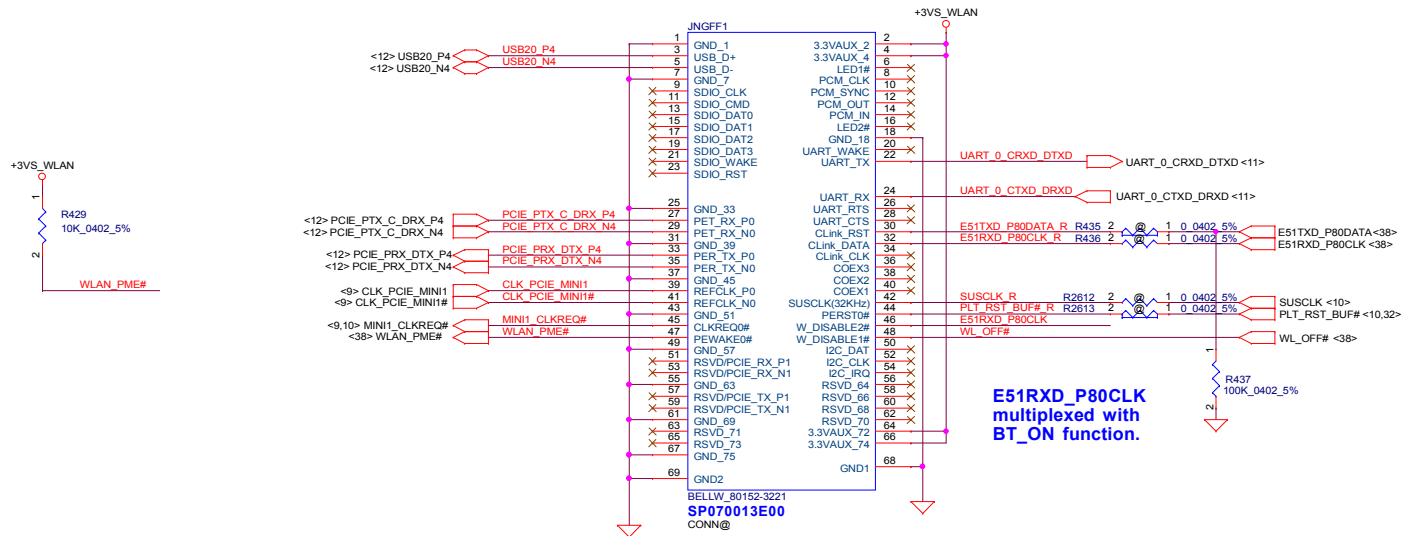
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				Custom	0.2
				Date	Wednesday, March 18, 2015
				Sheet	33 of 56

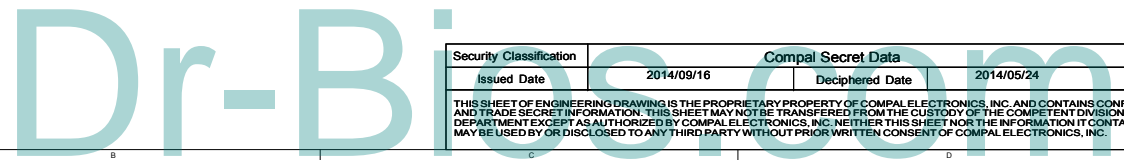
# Wireless LAN



## NGFF Card E key module pin define

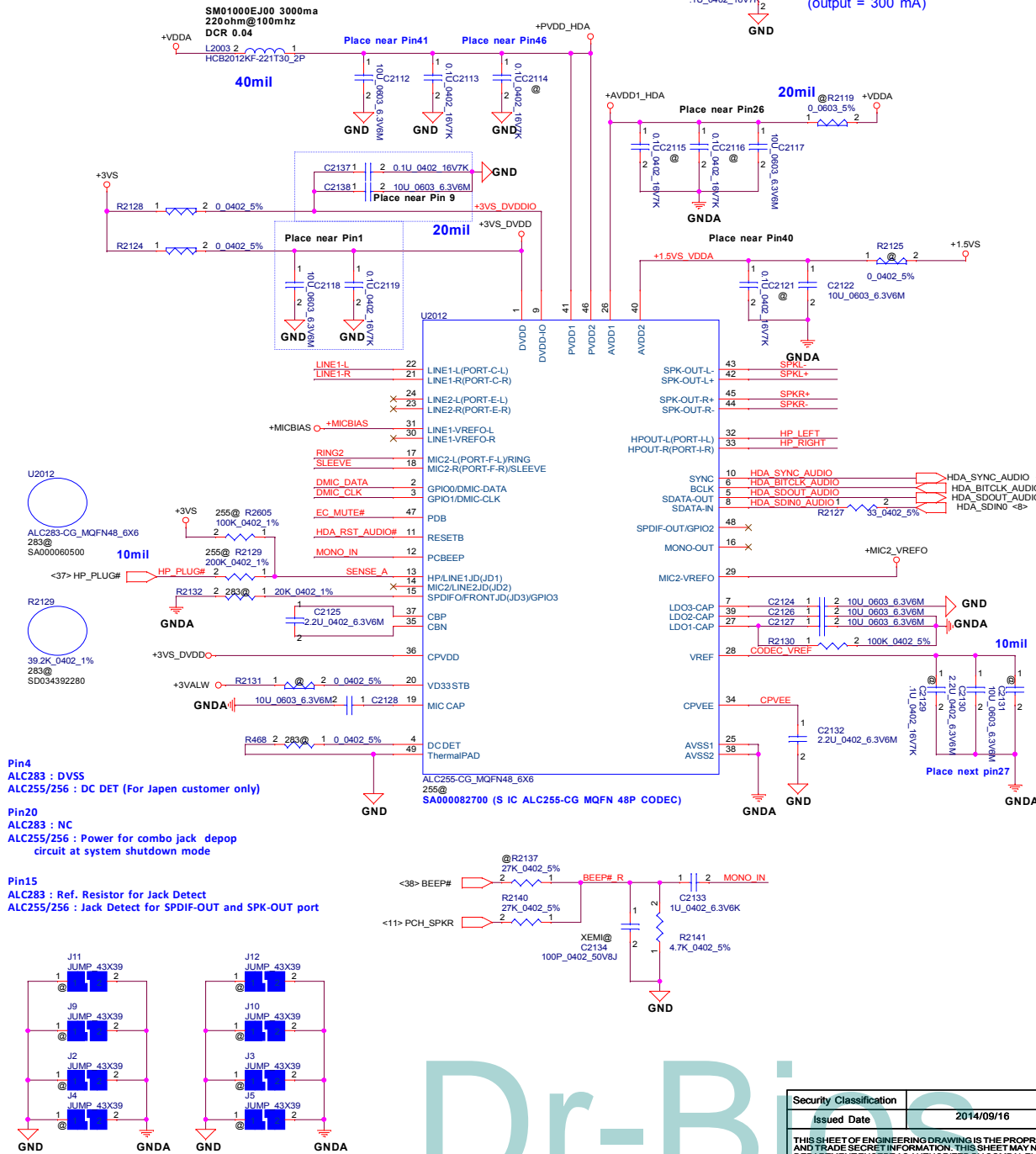


E51RXD\_P80CLK  
multiplexed with  
BT\_ON function.

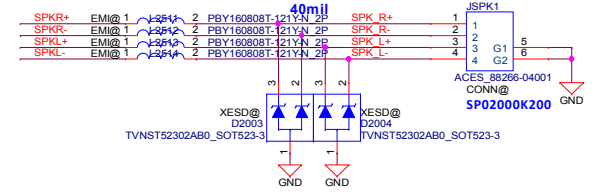


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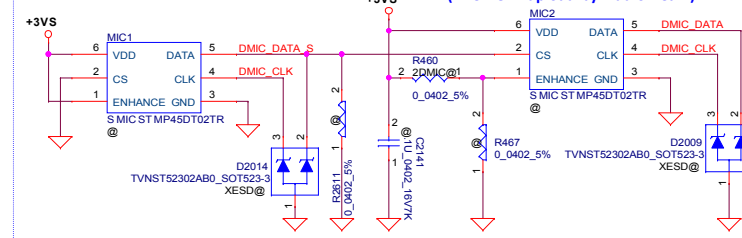
# HD Audio Codec



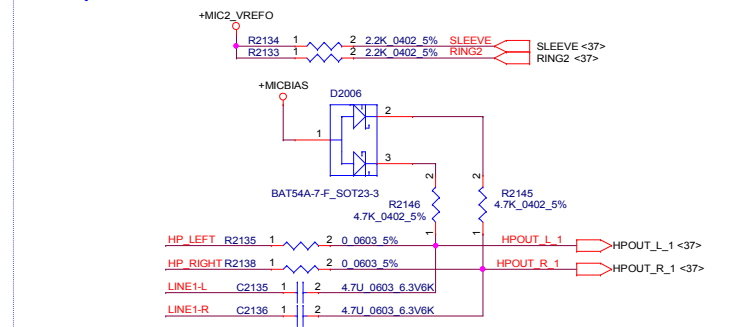
## Int. Speaker Conn.



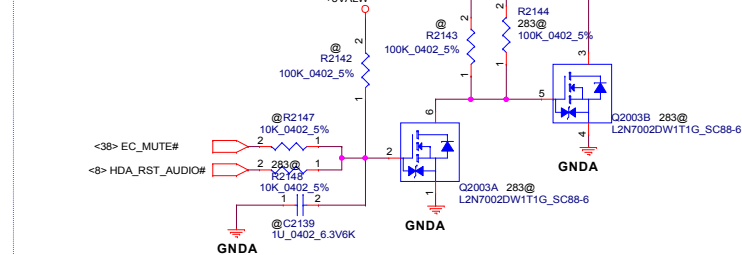
## Digital Mic



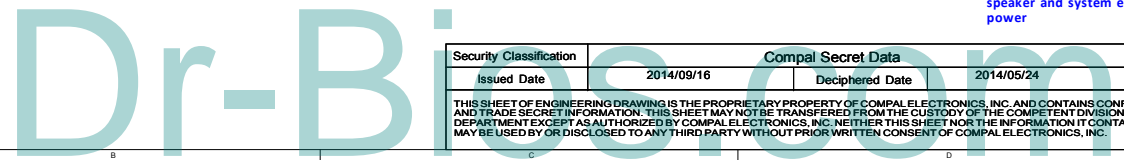
## Headphone out



## 255 involve this circuit already.



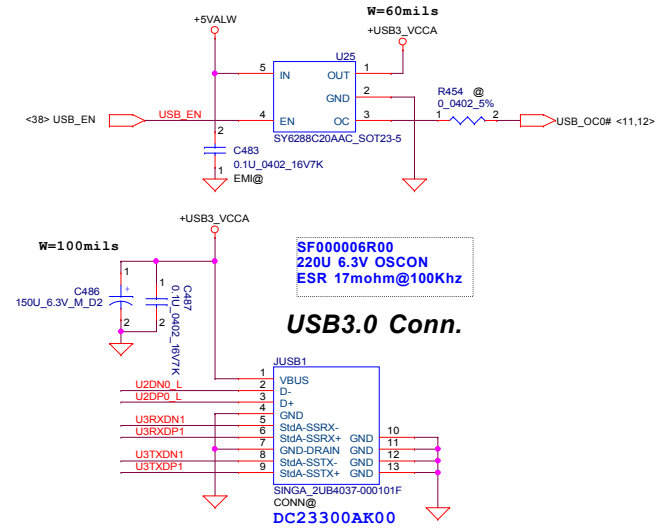
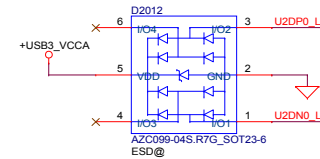
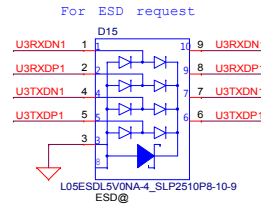
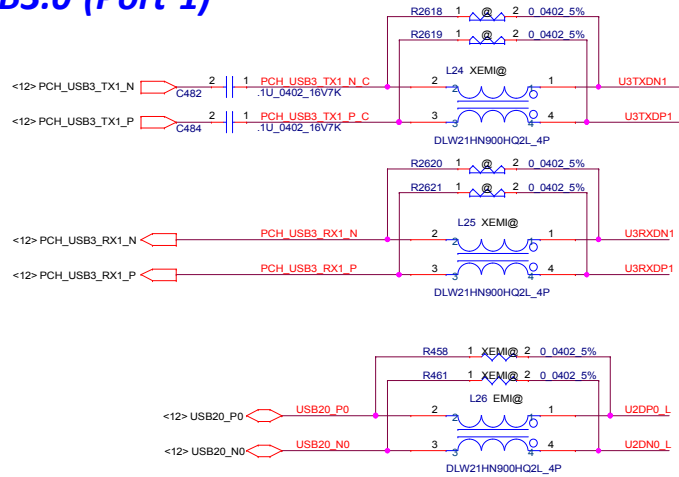
To solve the background noise while combo jack connecting to an active speaker and system entry into S3/S4/S5 without analog power



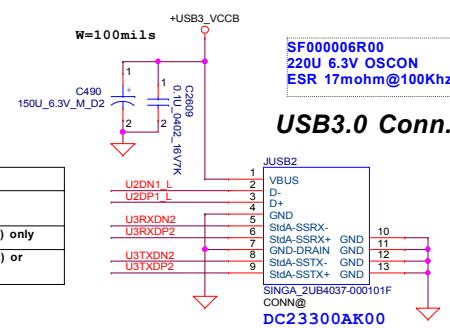
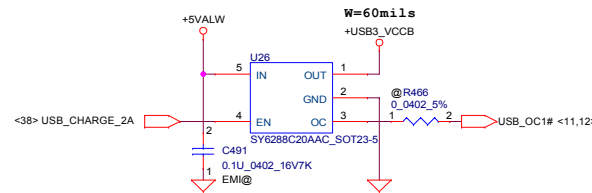
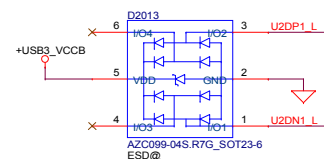
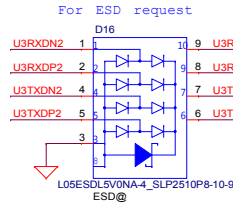
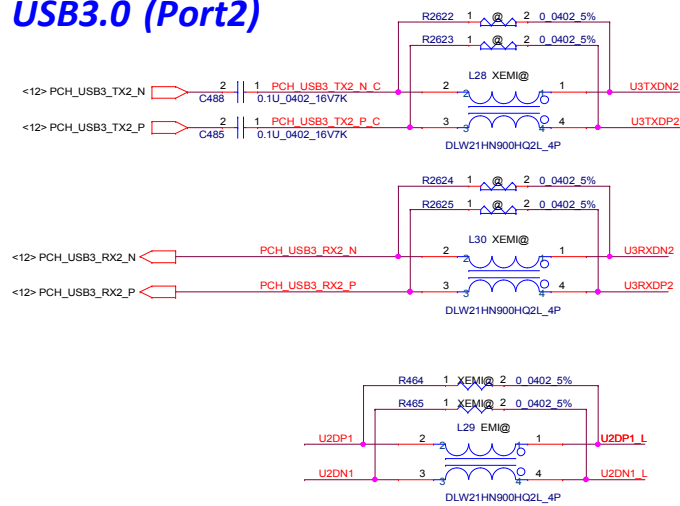
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Issued Date	2014/09/16	Deciphered Date	2014/05/24	HD Audio Codec ALC255	
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## USB3.0 (Port 1)

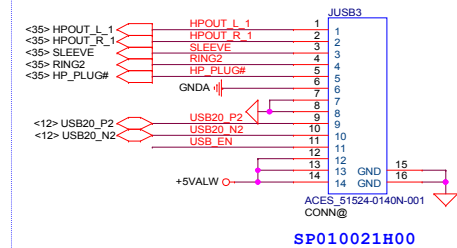


## USB3.0 (Port2)



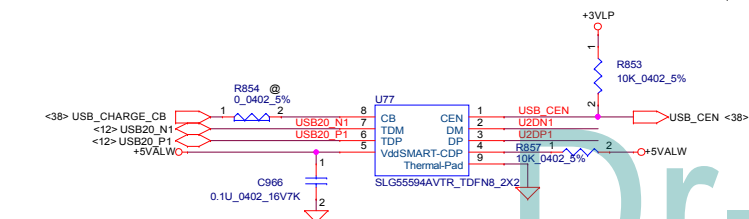
## USB/B (USB 2.0 + AUDIO)

Need check Audio Pin Sequence



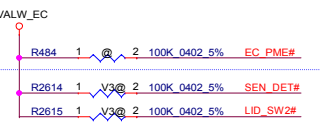
## USB Host Charger

CB	SELCDP	Description
0	X	DCP(Dedicated Keyboard Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only

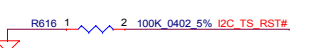
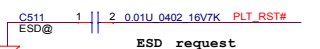
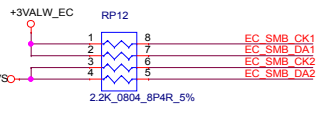




9022: ECRST# is internally pull-up to VCC via 40Kohm resistor, so can remove external pull-up resistor and capacitor.



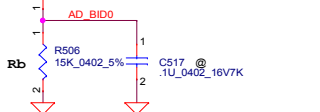
Reserve for 15" V3



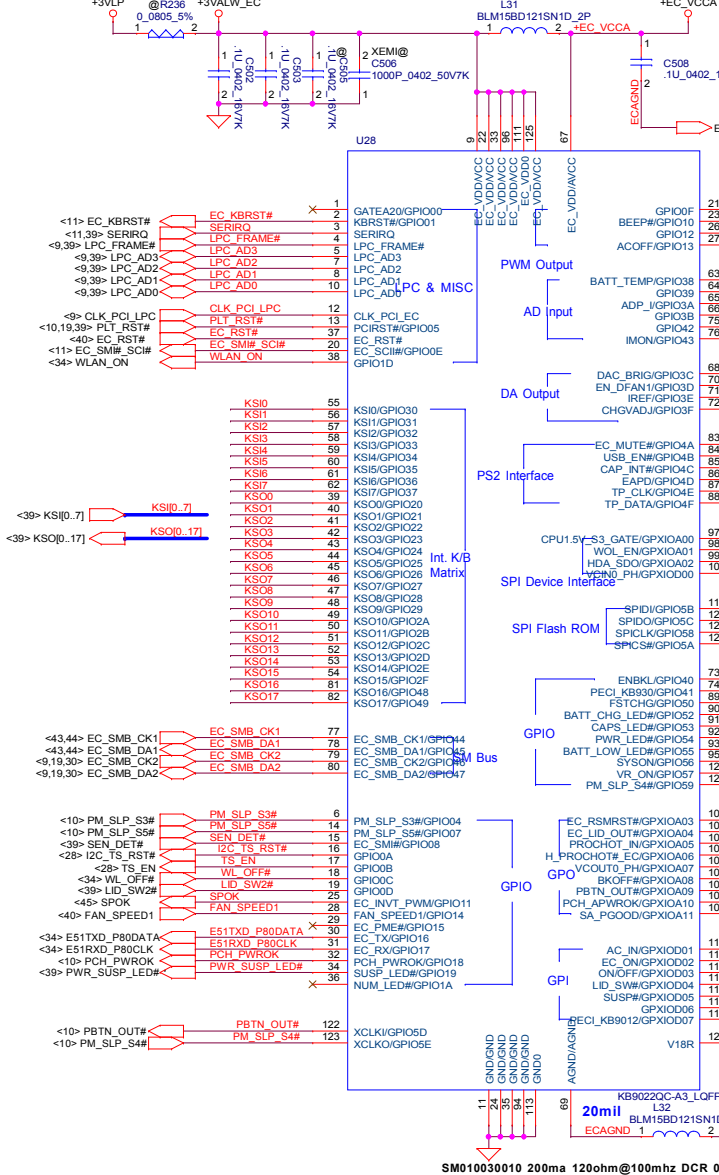
For abnormal shutdown



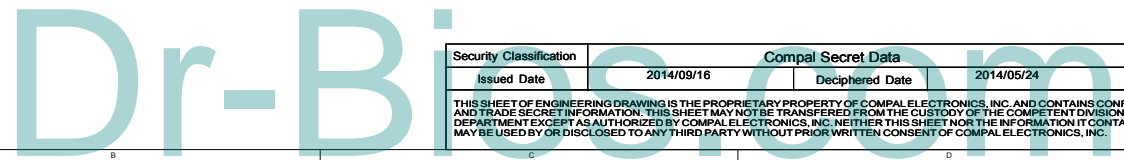
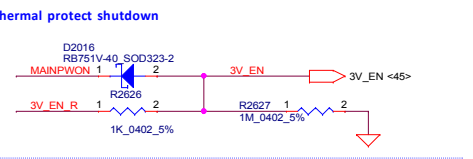
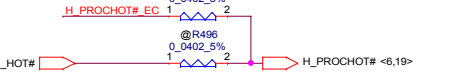
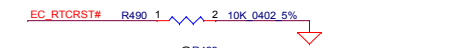
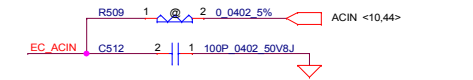
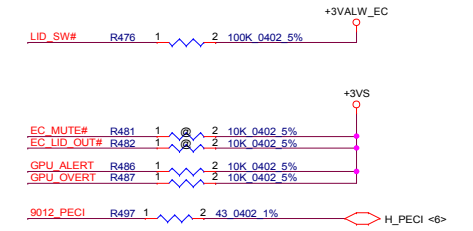
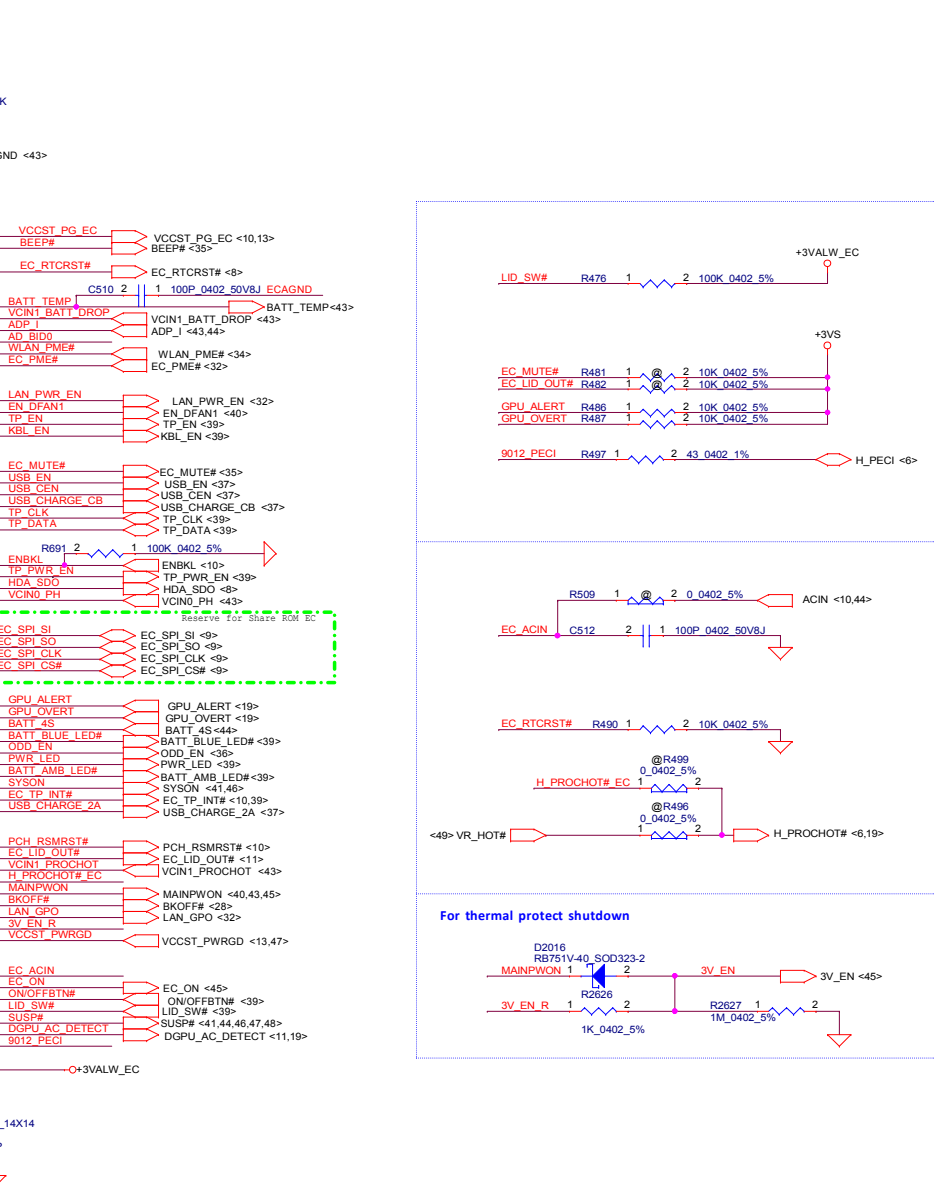
Board ID  
Analog Board ID definition,  
Please see page 3.



SM010030010 200ma 120ohm@100mhz DCR 0.2

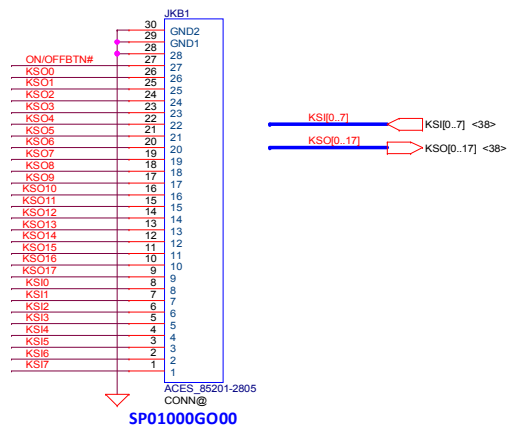


SM010030010 200ma 120ohm@100mhz DCR 0.2

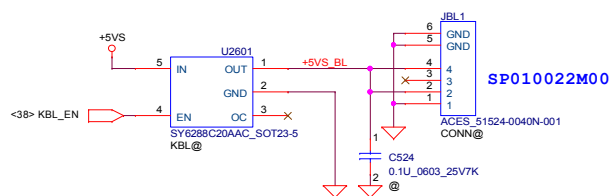


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2014/09/16		2014/05/24		Document Number	
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A4WAB/M/B LA-C341P		Date		0.2	
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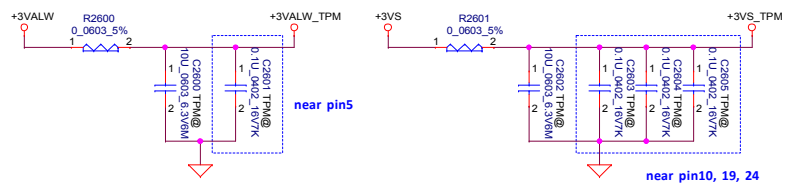
### KB Conn.



### KB BackLight



### TPM

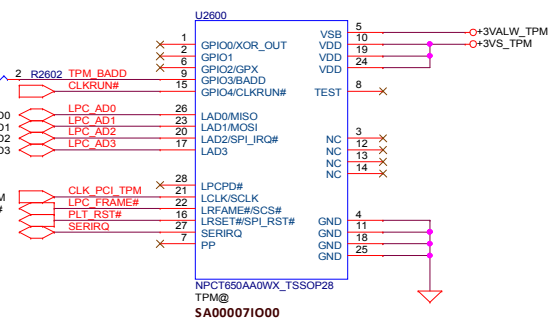


### GPIO3/BADD with Internal PH (default)

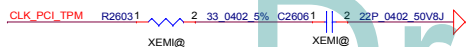
### CLKRUN PH 10K to +3VS at PCH side

### LPCPD# had internal PH

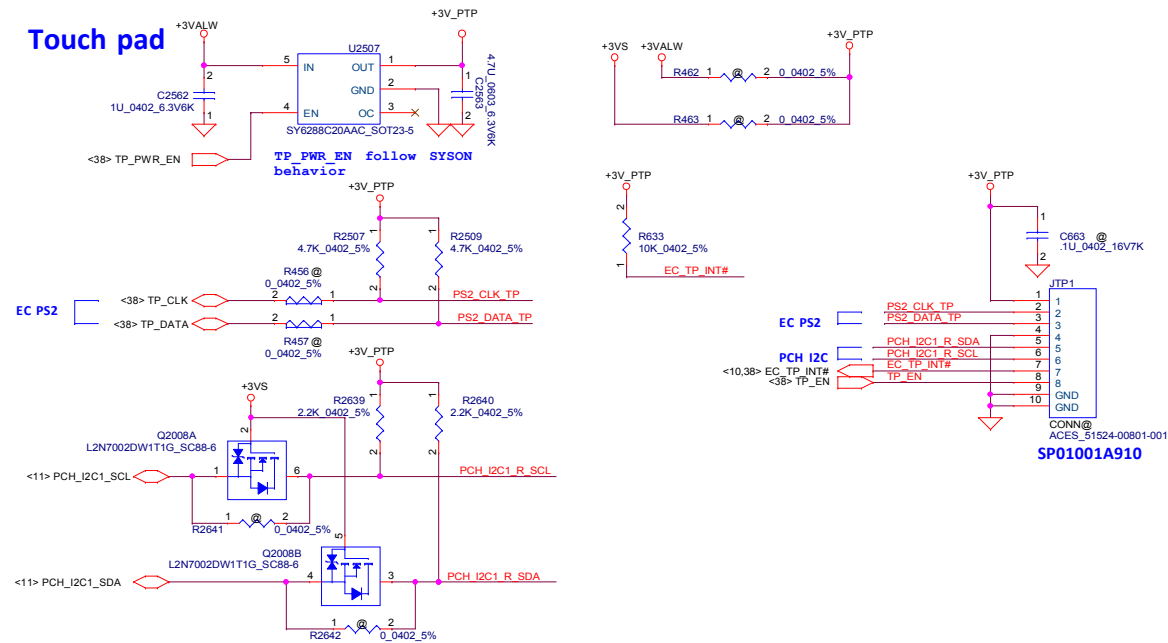
- <9,38> LPC\_ADD0
- <9,38> LPC\_ADD1
- <9,38> LPC\_ADD2
- <9,38> LPC\_ADD3
- <9,38> LPC\_FRAME#
- <10,19,38> PLT\_RST#
- <11,38> SERIRQ



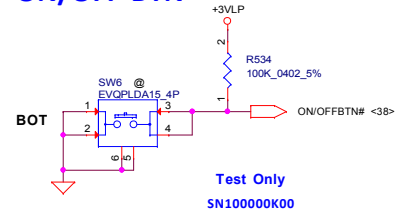
BADD	SELECTION
0	Eh - EfH
* 1	7h - 7Fh



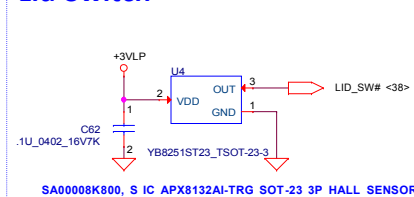
### Touch pad



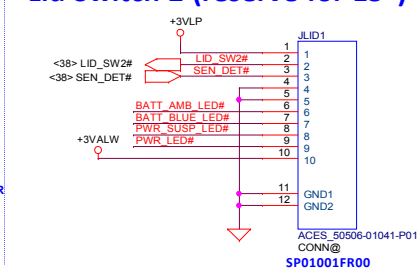
### ON/OFF BTN



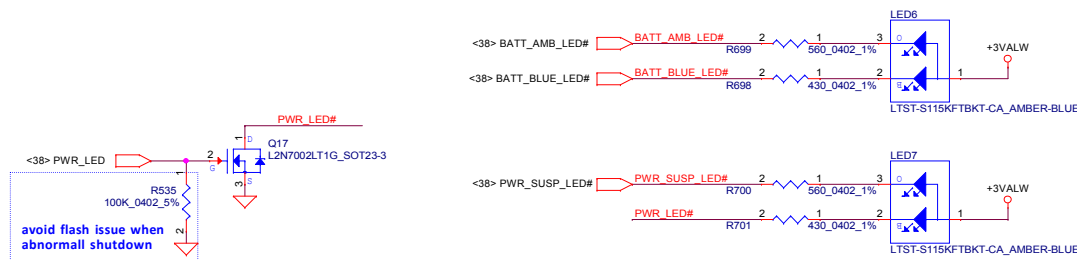
### Lid Switch



### Lid Switch 2 (reserve for 15")



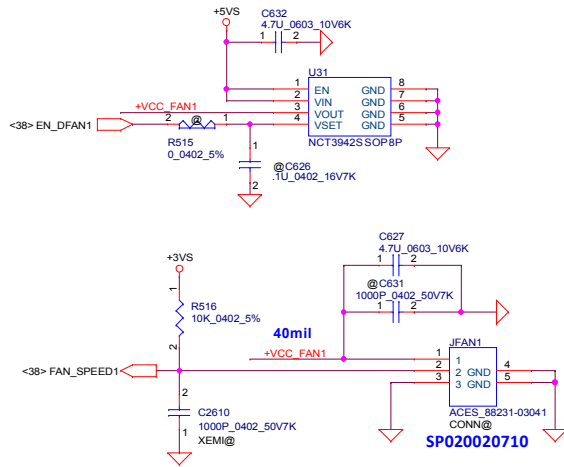
### LED



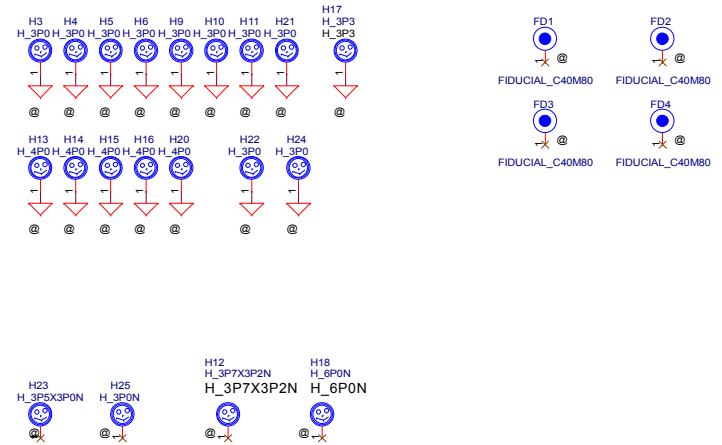
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/09/16	Deciphered Date	2014/05/24	
Title			KB & TP & TPM Connector & LED	
Document Number			A4WAB M/B LA-C341P	
Date			Wednesday, March 18 2015	
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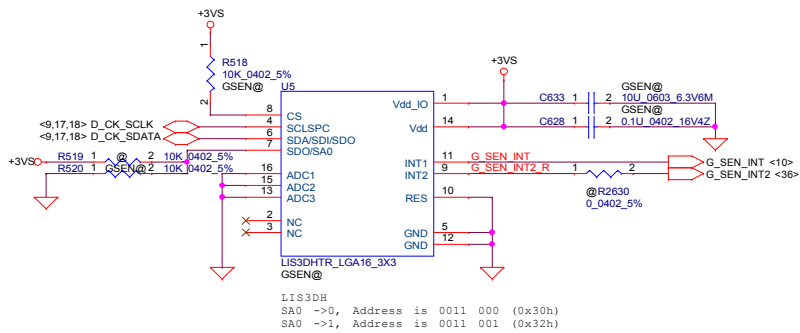
# FAN1 Conn



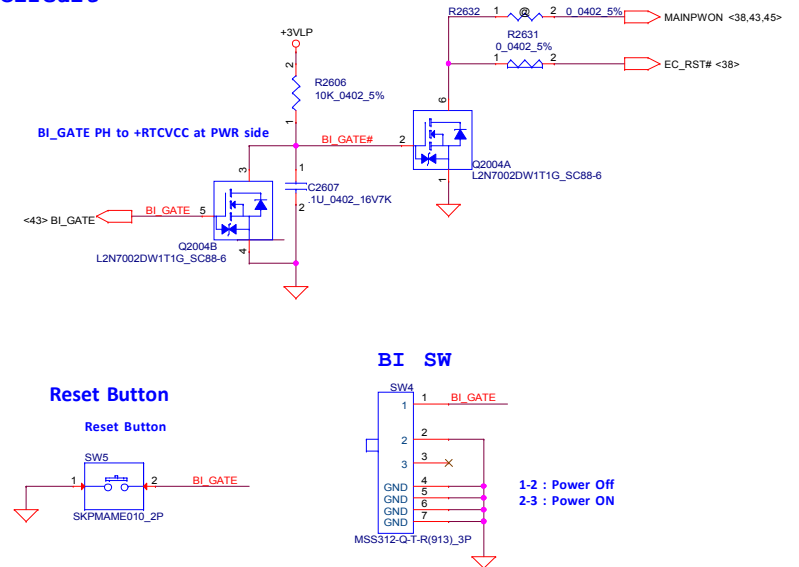
# Screw Hole



# G-Sensor



# Reset Circuit

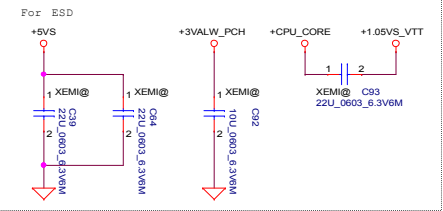
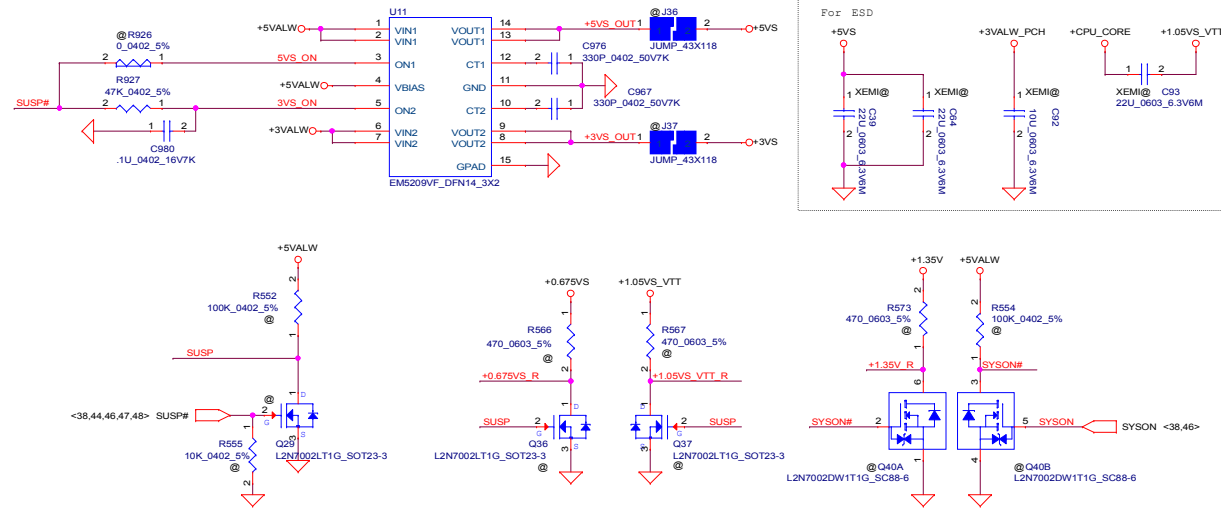


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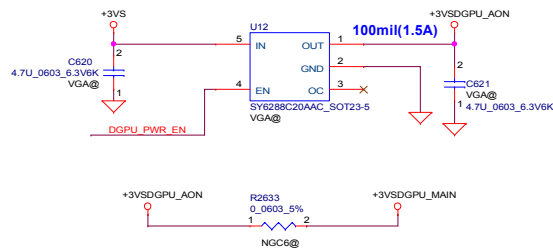
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/09/16	Deciphered Date	2014/05/24	Title
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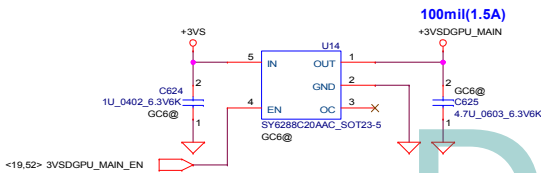
# DC & VGA Interface



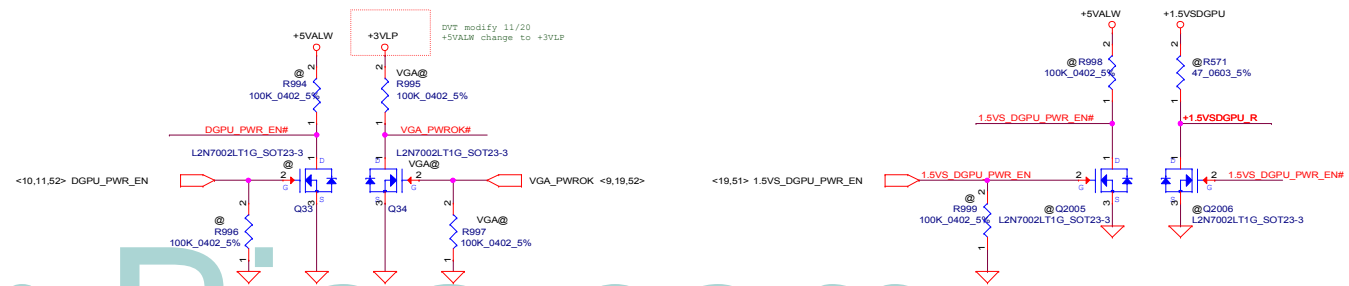
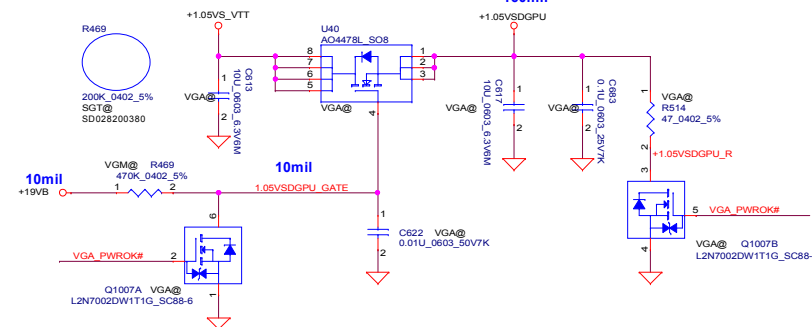
## +3VS to +3VSDGPU\_AON for GPU



## +3VS to +3VSDGPU\_MAIN for GC6-2.0

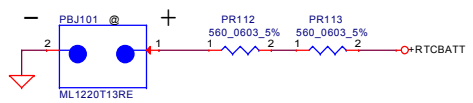
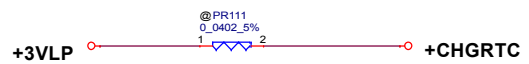
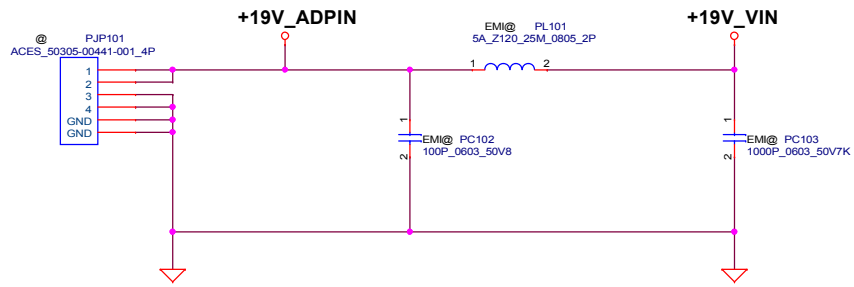


## +1.05VS\_VTT to +1.05VSDGPU



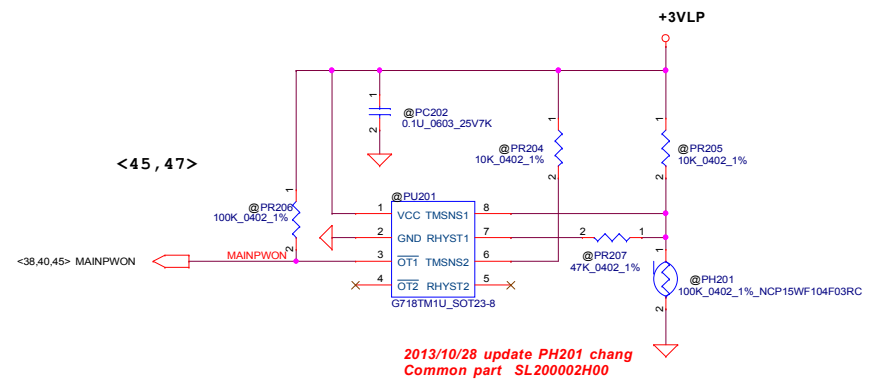
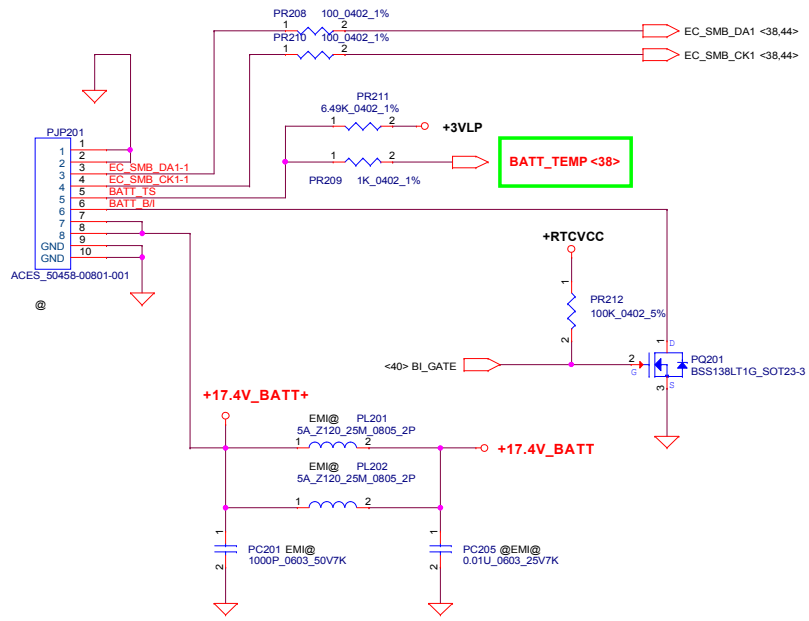
3VSDGPU\_MAIN\_EN From GPU

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		DC Interface	
2014/03/16		2014/05/24		Customer Number	
				A4WAB M/B LA-C341P	
				Rev	
				0.2	
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				Size	Document Number
			Custom	1.0	
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2013/10/28 update PH201 chang  
Common part SL200002H00

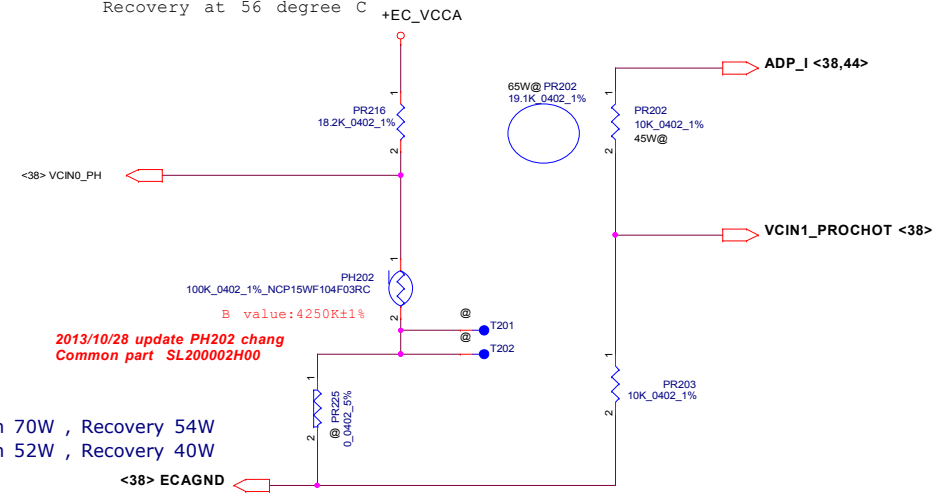
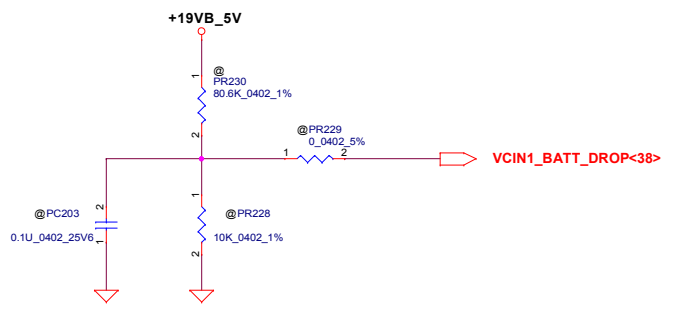
2014/09/30 update

For KB9022 sense 20mg2	Active	Recovery
45W PR202 10K ohm SD034100280	58.5W, 0.61V	45W, 0.47V
65W PR202 19.1K ohm SD034191280	84.5W, 0.61V	65W, 0.47V

PH202 under CPU bottom side :  
CPU thermal protection at 90 degree C ( shutdown )  
Recovery at 56 degree C

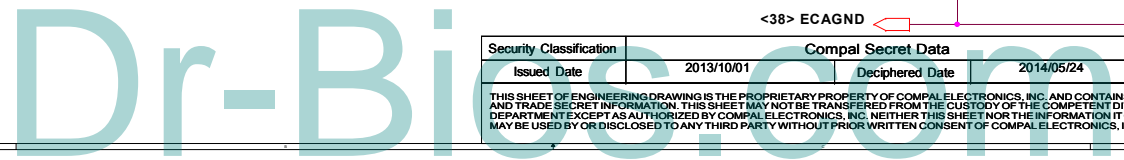
2013/10/02  
Add for ENE9022 Battery Voltage drop detection.  
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.  
B+=9V



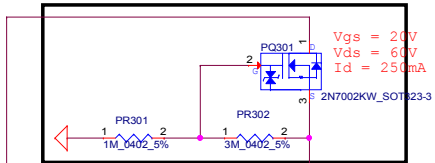
2013/10/28 update PH202 chang  
Common part SL200002H00

For 65W adapter==>action 70W , Recovery 54W  
For 40W adapter==>action 52W , Recovery 40W



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				Custom	Rev 1.0
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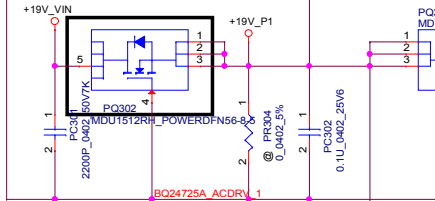
Protection for reverse input



Vgs = 20V  
Vds = 60V  
Id = 250mA

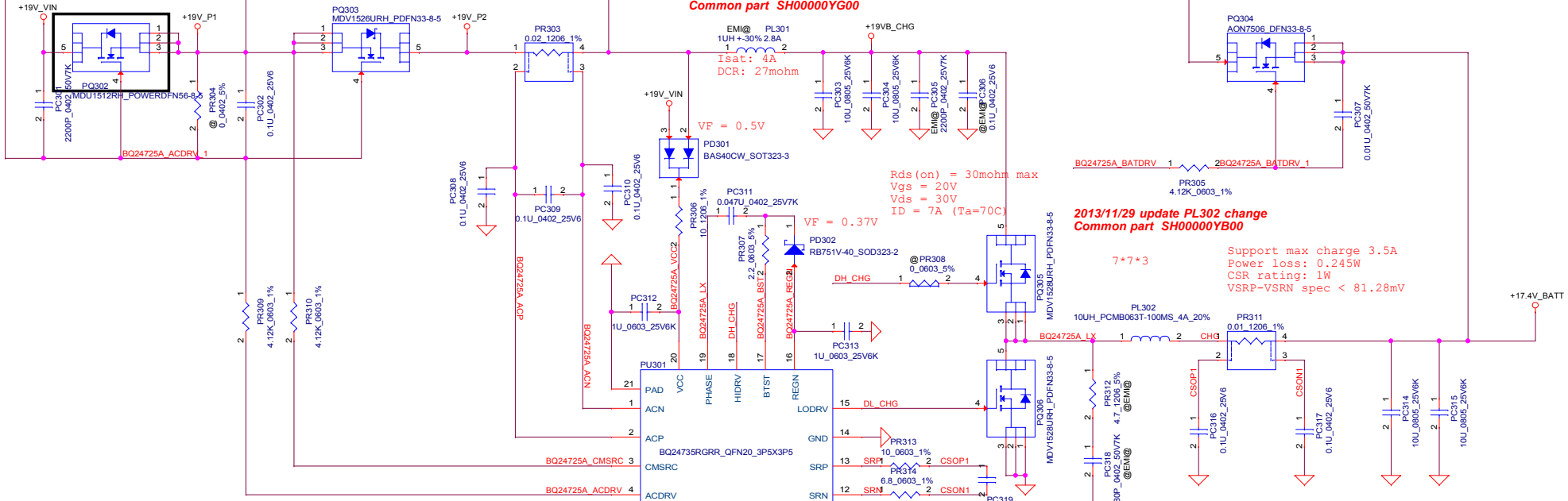
2013/10/14  
PR303 10m ohm chang -->20m ohm  
SD00000S120

Need check the SOA for inrush



2014/01/21 update PL301 change  
Common part SH00000YG00

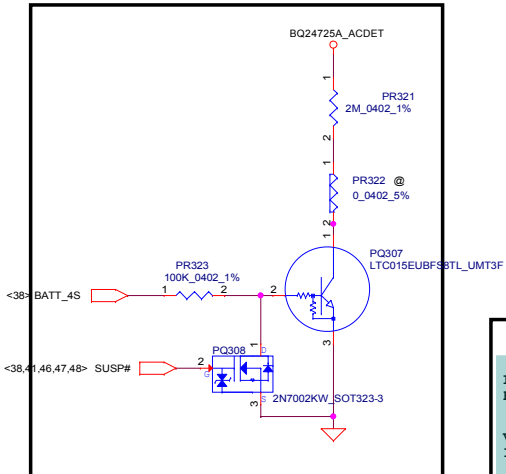
2014/09/30 update PQ303&PQ304 change  
Common part SB0000010A00



Module model information

BQ24735A\_V1.mdd  
BQ24735A\_V2.mdd

For 4S per cell 4.35V battery



Vin Detector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

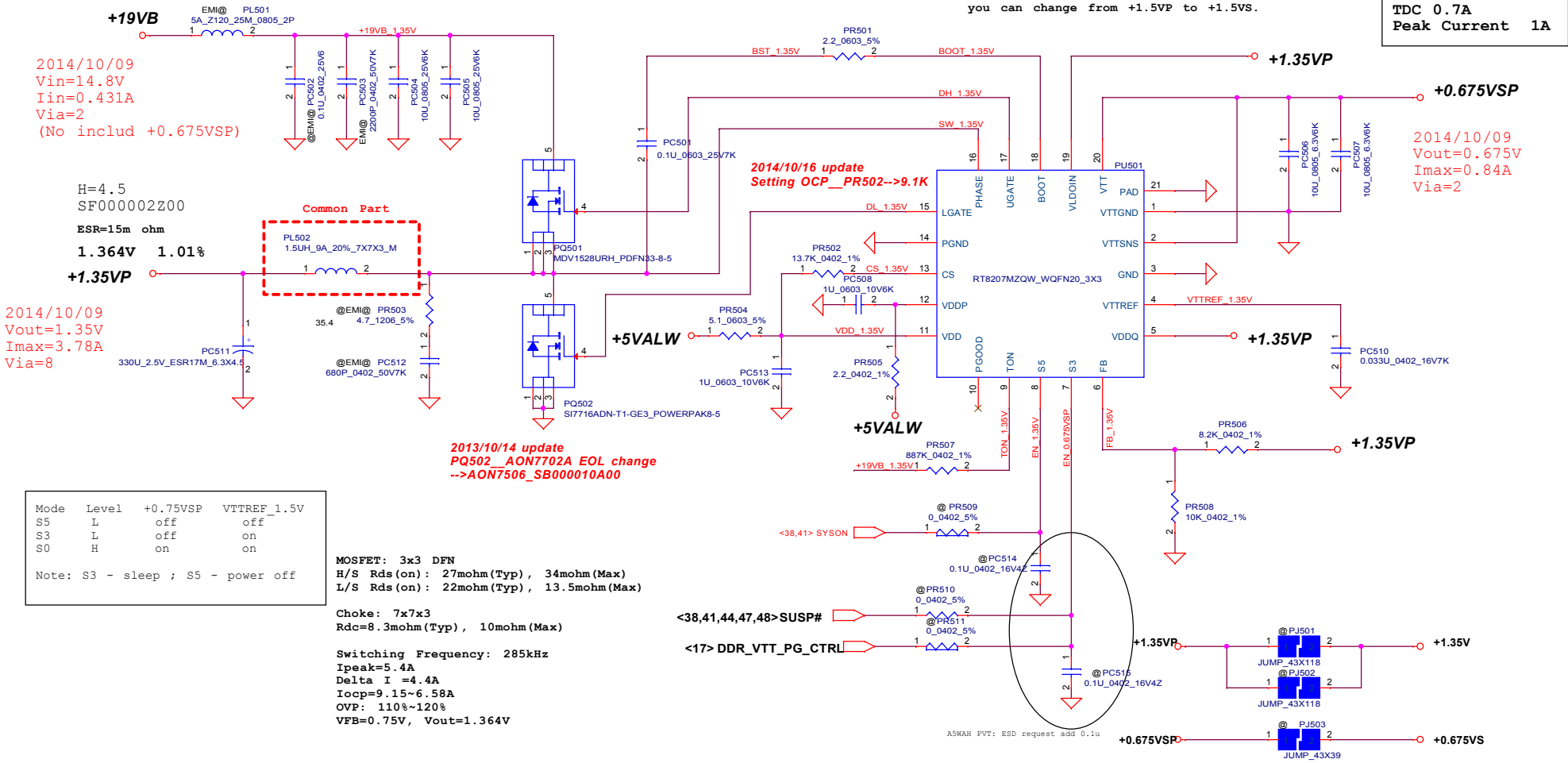
VILIM = 20 \* ILIM \* Rsr  
ILIM = 3.3 \* 100 / (100 + 316) / 20 / 0.01  
= 3.966 A

**\*\*Design Notes\*\***  
 #For 65 /90W system, 3S1P/3S2P battery  
 Maximum Charging current 3.5A  
 Battery discharge power 55W  
 #Register Setting  
 1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke  
 2. 0X12 bit3 set 1 (default 0) to enable turbo boost function  
 3. Disable turbo when AC only  
 #Circuit Design  
 1. ACOK, ILIM pull high voltage need base on 3/5V enable control  
 Charge current 3.5A  
 Power loss : 1.82W  
 Power density : 0.81 (15X15)  
 2. If use 4S per cell 4.35V battery, need additional circuit for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)  
 3. PC223 2200p is for quick response when AC plug out.  
 4. For hybrid design, need double check PQ202, PQ203, PQ204, PQ205 component rating  
 #Protect function  
 1. ACOVP : ACDET voltage > 3.14V  
 2. Charger timeout : No communication within 175s (default)  
 3. ACOG : 3.33 X Input current DAC setting (default)  
 4. CHOC : 3/4 5/6A based on current setting  
 5. BATOV : 103-106%  
 6. BATTLEW : 2.5V  
 7. TSHUT : 155C  
 8. IFAULT HI : 750mV (default)  
 9. IFAULT LOW : 110mV (default)

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				Document Number
				Common Circuit
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Module model information  
 RT8207M\_V1.mdd For Single layer  
 RT8207M\_V2.mdd For Dual layer

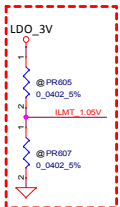


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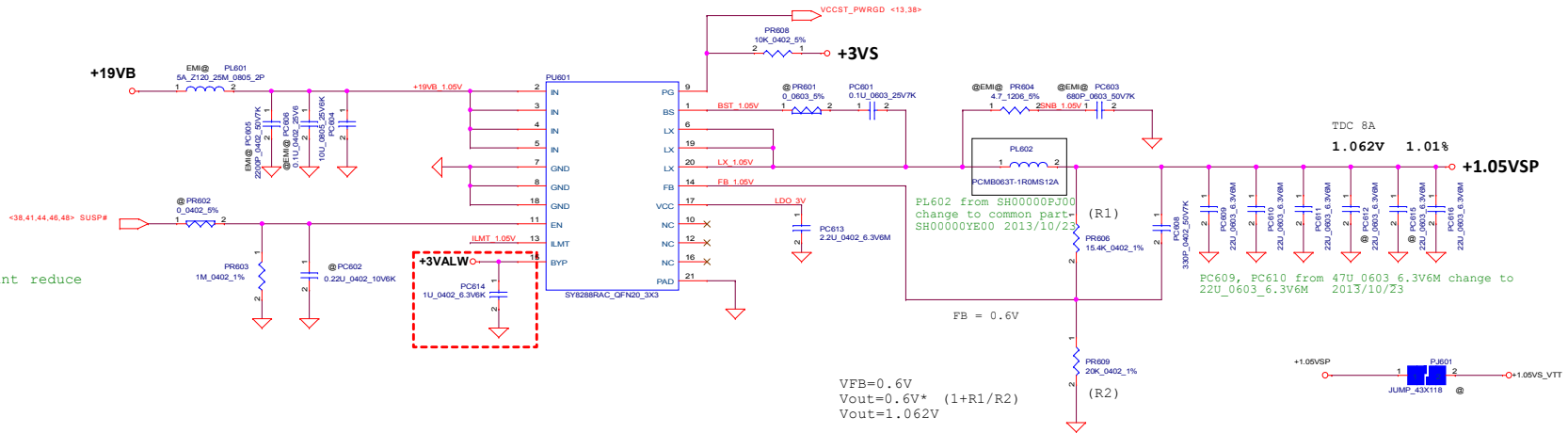
Compal Electronics, Inc.			
<b>+1.35VP/+0.675VSP</b>			
Title	Document Number	Sheet	Rev
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Module model information  
SY8208D\_v1.mdd

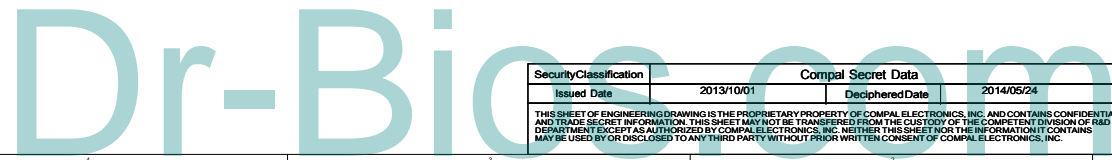
EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



PR606 part count reduce

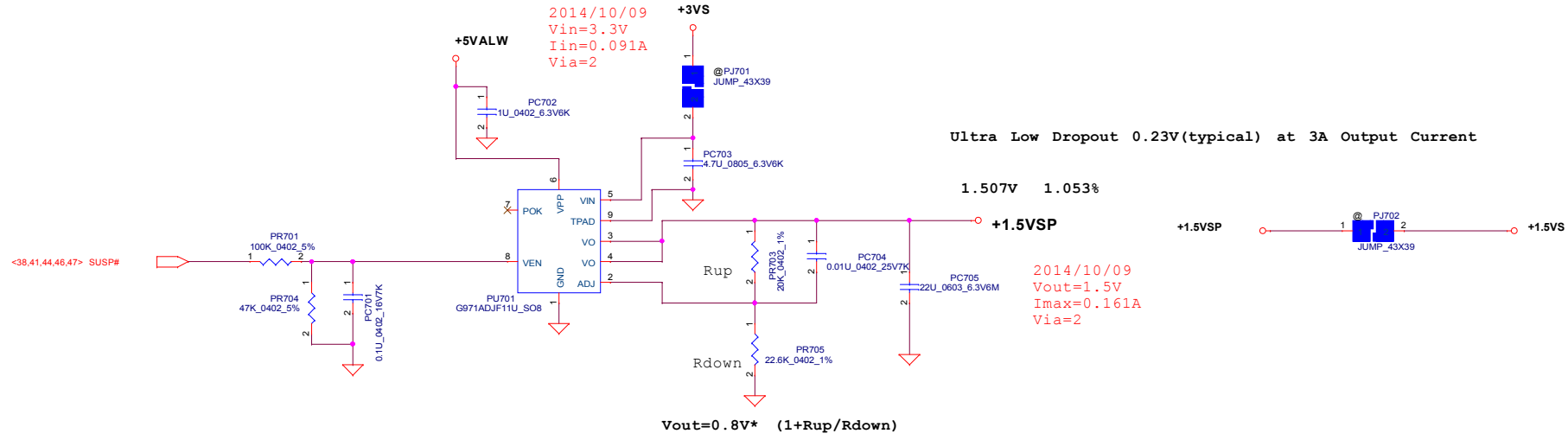


Module model information  
SY8208D\_v1.mdd



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				<b>+1.05VSP</b>
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Module model information:  
ISL95813 (for 15W & 28W CPU)

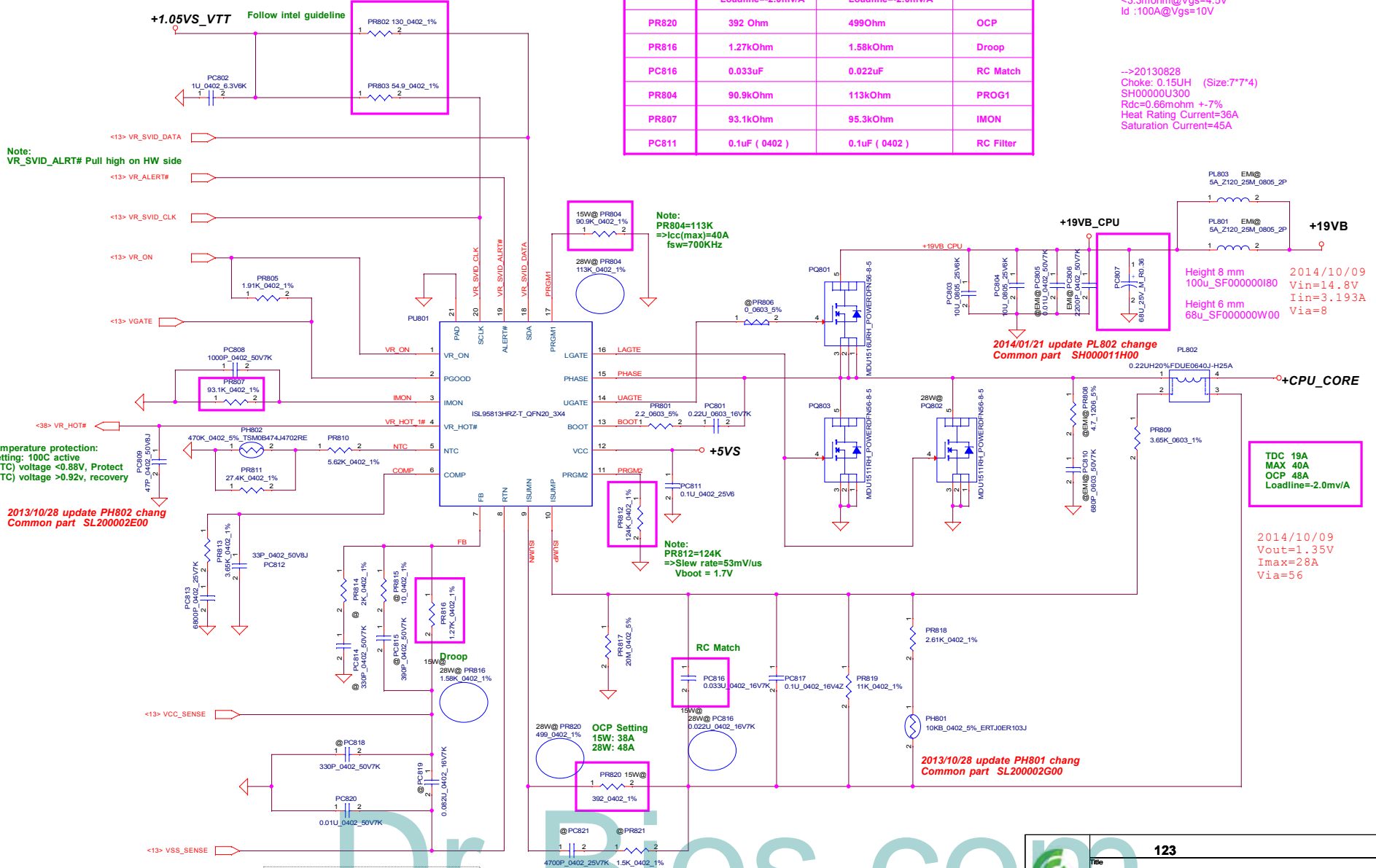
Base on BDW PDDG Rev\_0\_73

Location	15W	28W	Note
	TDC	14A	
MAX	32A	40A	
OCF	38.4A	48A	
Loadline	-2.0mV/A	-2.0mV/A	
PR820	392 Ohm	499Ohm	OCF
PR816	1.27kOhm	1.58kOhm	Droop
PC816	0.033uF	0.022uF	RC Match
PR804	90.9kOhm	113kOhm	PROG1
PR807	93.1kOhm	95.3kOhm	IMON
PC811	0.1uF (0402)	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH  
Rds(on):  
<10.1mohm@Vgs=10V  
<14.0mohm@Vgs=4.5V  
Id :24A@Vgs=10V

L-side MOS: MDU1511RH  
Rds(on):  
<2.4mohm@Vgs=10V  
<3.3mohm@Vgs=4.5V  
Id :100A@Vgs=10V

-->20130828  
Choke: 0.15uH (Size:7\*7\*4)  
SH0000U1300  
Rdc=0.66mohm +7%  
Heat Rating Current=36A  
Saturation Current=45A



Note:  
VR\_SVID\_ALERT# Pull high on HW side

Note:  
PR804=113K  
=>lcc(max)=40A  
fsw=700KHz

Over temperature protection:  
OTP Setting: 100C active  
Pin5 (NTC) voltage <0.88V, Protect  
Pin5 (NTC) voltage >0.92V, recovery

2013/10/28 update PH802 chang  
Common part SL200002E00

2014/01/21 update PL802 change  
Common part SH000011H00

TDC 19A  
MAX 40A  
OCF 48A  
Loadline=-2.0mV/A

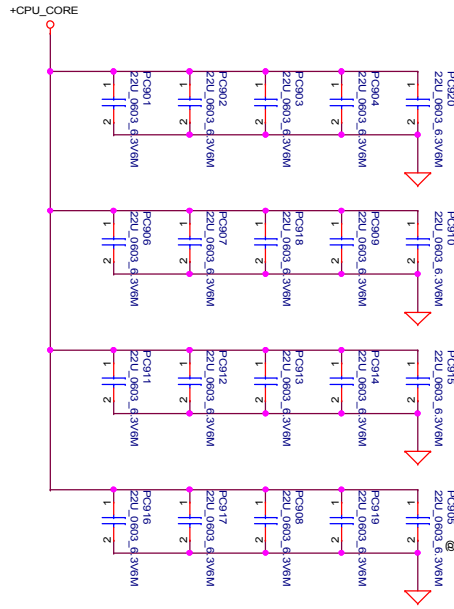
2014/10/09  
Vout=1.35V  
Imax=28A  
Via=56

Local sense put on HW site



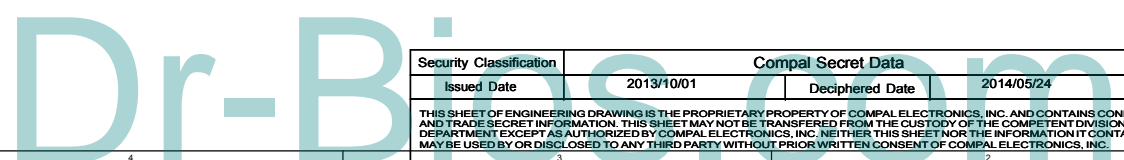
123	
CPU CORE/GFX CORE	
Size	DocumentNumber
A4WAB M/B LA-C341P	
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PWR Rule  
 需確認最新SPEC.  
 Modify 8/6.



30 X 22uF 0805  
 2012/10/23  
 check the output cap Qty!!!  
 2012/10/24  
 23 pcs 22uF and reserve 7 pcs  
 2013/01/14  
 22uF\*17 unpop:22uF\*3

20130828  
 15W: 22uF\*14  
 28W: 22uF\*16



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Module model information:  
RT8813A\_V1A for IC module  
RT8813A\_V1B for SW module

Vboot=Vvref\*Rref2/(Rref1+Rref2+Rboot)  
Rt=Rrefadj // (Rboot+Rref2)  
Vmin= Vvref\*[Rref2/(Rref2+Rboot)]\*[Rt/(Rref1+Rt)]  
Vmax=Vvref\*Rref2/[(Rref1/Rrefadj)+Rboot+Rref2]  
Vout=Vmin+N\*Vstep  
Vstep=(Vmax-Vmin)/Nmax

PWM-VID Spec and component Values

PWM-VID Spec	Config B	Config C	Config D
Vmin	0.6V	0.65V	0.9V
Vmax	1.2V	1.15V	1.15V
Vboot	0.9V	0.9V	1.028V
Voltage step	6.25mV	25mV	12.5mV
N of Voltage level	96	20	20
Rrefadj	PR1209	20K	39K
Rref1	PR1208	20K	30K
Rboot	PR1211	2K	3K
Rref2=PR1210 +PR1224	PR1210	18K	24K
	PR1224	0	3K
C	PC1210	2.7nf	1.8nf
			5.6nf

N15S-GT N15V-GL N15V-GM  
N16S-GT  
N16V-GM

PSI :  
1 phase with DEM 0V to 0.8V  
1 phase with CCM 1.2V to 1.8V  
2 phase with CCM 2.4V to 5.5V

EN High Threshold = 1.6V

Current Limit threshold setting  
Rocset=(Ivalley \* Rds(on) + 40 mV) / 10uA

I\_ripple=(19-0.9)\*0.9/  
(304.89KHz\*0.36u\*19)=7.811A

OCP=54A/2=27A per phase  
Ivalley=27A-7.811A/2=23.1A

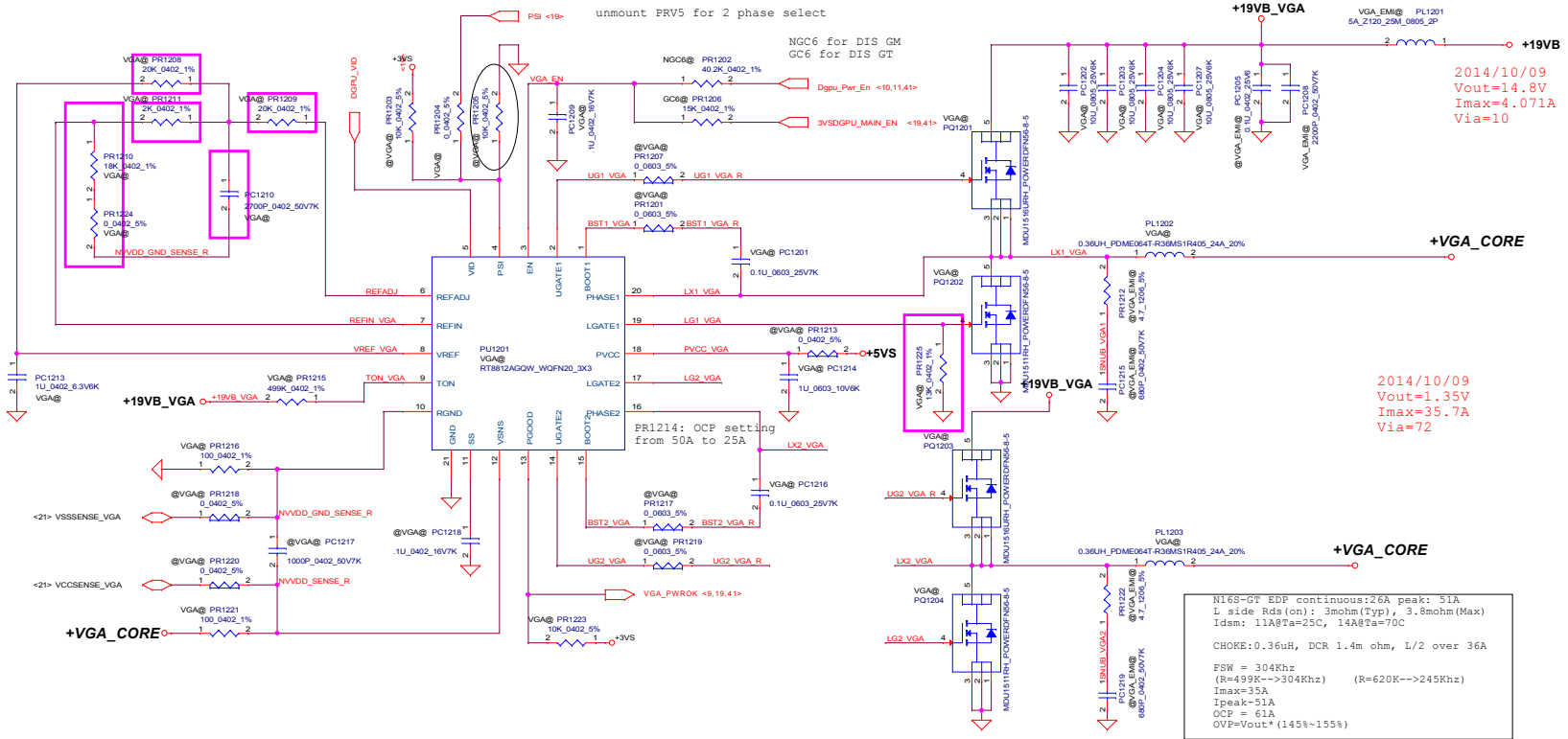
H-side MOS:AON6552 Rds(on):  
5.6mohm@Vgs=10V  
6.7mohm@Vgs=4.5V  
Id :20A@Ta=25 degC  
L-side MOS:AON6554 Rds(on):  
3.2mohm@Vgs=10V  
3-3.8mohm@Vgs=4.5V  
Id :85A@Ta=25 degC

Choke: 0.22uH (Size:7\*7\*4)  
Rdc=0.97mohm +/-5%  
Heat Rating Current=34A  
Saturation Current=25A

C=3\*330uF (9mohm)=990uF  
Vripple=Iripple\*ESR(min)=7.811A\*3mohm=23.4mV

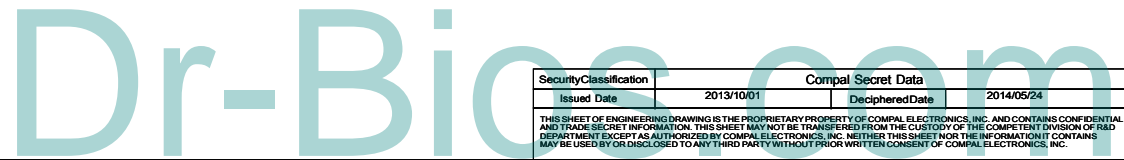
Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config C
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@



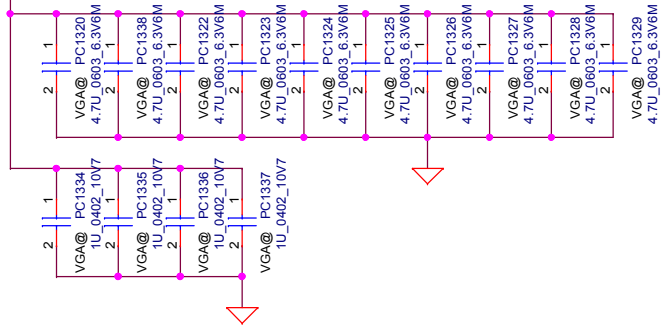
N16S-GT EDP continuous:26A peak: 51A  
L side Rds(on): 3mohm(Typ), 3.8mohm(Max)  
Idsm: 11A@Ta=25C, 14A@Ta=70C  
CHOKER:0.36uH, DCR 1.4m ohm, L/2 over 36A  
FSW = 304KHz (R=499K-->304KHz) (R=620K-->245KHz)  
Imax=35A  
Ipeak=51A  
OCP = 61A  
OVP=Vout\*(145%-155%)

Remove GPU OTP circuit for HW request

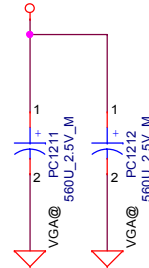


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**+VGA\_CORE Under GPU Core GB4-128 package**



**+VGA\_CORE**

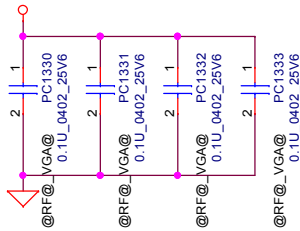


N15x 2013/12/10  
 Under  
 4.7uF\_0603\_10pcs  
 1uF\_0402\_4pcs  
 Near  
 47uF\_0805\_1pcs  
 22uF\_0603\_1pcs (2PCS unpop)  
 4.7uF\_0805\_5pcs

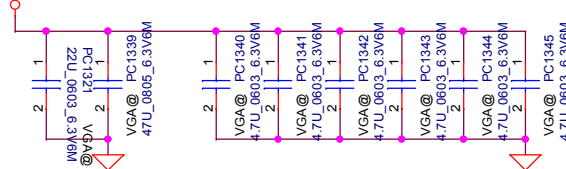
N15x2013/10/17  
 Under  
 4.7uF\_0603\_15pcs  
 1uF\_0402\_8pcs  
 Near  
 47uF\_0805\_0pcs  
 22uF\_0603\_9pcs (2PCS unpop)  
 4.7uF\_0805\_5pcs

N15x2013/10/07  
 Under  
 4.7uF\_0603\_15pcs  
 1uF\_0402\_8pcs  
 Near  
 47uF\_0805\_0pcs  
 22uF\_0805\_9pcs (2PCS unpop)  
 4.7uF\_0805\_5pcs

**+VGA\_CORE**



**+VGA\_CORE Near GPU Core**



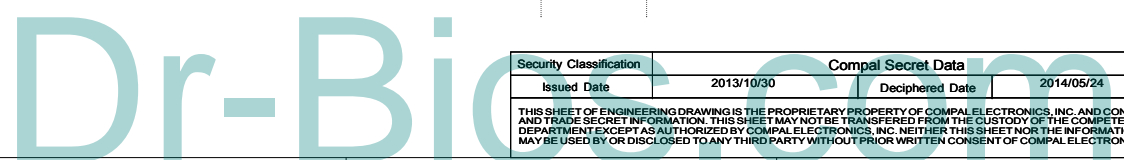
N15x2013/10/02  
 Under  
 4.7uF\_0603\_15pcs  
 1uF\_0402\_8pcs  
 Near  
 47uF\_0805\_0pcs  
 22uF\_0805\_14pcs  
 4.7uF\_0805\_5pcs

N14x  
 Under  
 4.7uF\_0603\_10pcs  
 0.1uF\_0402\_4pcs  
 Near  
 47uF\_0805\_1pcs  
 22uF\_0805\_1pcs  
 4.7uF\_0805\_5pcs

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Version change list (P.I.R. List)

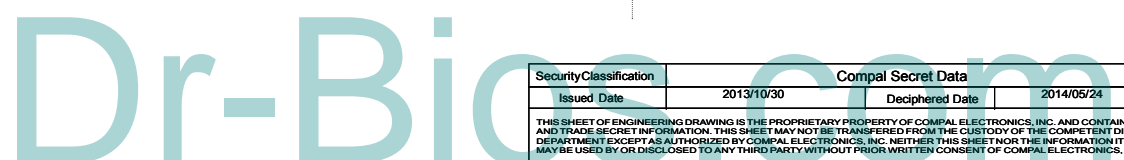
Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
1	Design Update	BOM Structure Identical	P.51	Add GT GM2G for PR1005	20141120	DVT
2	Design Update	IC will Stop Production	P.48	Change the PU701 from APL5930KAI to G971ADJF11U	20141120	DVT
3	Design Update	Nvidia N16S-GT and N16V-GM Open VReg Configuration both use B	P.52	PR1208:20kOhm, PR1209:20kOhm, PR1210:18kOhm PR1211:2kOhm, PR1224:0Ohm, PC1210:2700pF PR1225:13kOhm	20141120	DVT
4	Design Update	CPU Load Line Request	P.49 P.50	Change the PR817 from 4.99MOhm to 20MOhm. Change the PR807 from 121kOhm to 93.1kOhm. Change the PR813 from 1.91kOhm to 3.65kOhm. Change the PC917 PC908 and PC919 from @ to 22uF.	20141128	DVT
5	Design Update	Solution Change	P.45 P.47 P.51	Change the PU401 from SYX198BQNC to SY8286BRAC Change the PU402 from SYX198CQNC to SY8286CRAC Change the PU601 from SYX198DQNC to SY8288RAC Change the PU1001 from SYX198DQNC to SY8288RAC	20141128	DVT
6	Design Update	RC Value for GPU Sequence Fine Tune GC6 Function	P.51 P.52	GM: PR1002:15kOhm, PC1002:0.1uF. GT: PR1002:4.7kOhm, PC1002:0.1uF. GM(No Support GC6, Use DGPU_PWR_EN) PR1202:40.2kOhm, PC1209:0.1uF. GT(Support GC6, Use 3VSDGPU_MAIN_EN) PR1206:20kOhm, PC1209:0.1uF.	20141128	DVT
7	Design Update	EMI request	P.44	Add PL301 Delete PJ301	20141203	DVT
8	Design Update	FAE request	P.45 P.47 P.51	Change the PC403、PC416、PC601、PC1001 from 1000P_0402_25V8J to 0.1U_0603_25V7K	20141204	DVT
9	Design Update	FAE request	P.45	Change the PC411 from 4.7U_0603_6.3V6M to 4.7U_0402_6.3V6M	20141205	DVT
10	Design Update	Solution Change	P.51	Change the PR1002 from 15K 0402 5% to 15K 0402 1% at GM Change the PR1002 from 4.7K_0402_5% to 10K_0402_1% at GT	20141215	DVT
11	Design Update	Solution Change	P.46	Change the PU501 from RT8207P to RT8207M	20150105	PVT
12	Design Update	GPU sequence fine tune RC value	P.51 P.52	GT: PR1002 change to 0 ohm and depop PC1002. GT: PR1206 change to 15k ohm.	20150119	PVT
13	Design Update	Solution Change	P.44 P.46 P.49	PQ303 change to MDV1526URH. PQ305,PQ306,PQ501 change to MDV1528URH. PQ502 change to SI7716ADN. PQ801,PQ1201,PQ1203 change to MDU1516URH. PQ802,PQ803,PQ1202,PQ1204 change to MDU1511RH.	20150119	PVT
14	Design Update	Thermal request	P.43	Change the PR216 from 16.9K to 18.2K	20150122	PVT
15	Design Update	Solution Change	P.44~47 P.49 P.51~52	Change the PR308 PR401 PR407 PR511 PR601 PR602 PR806 PR1001 PR1002 PR1201 PR1207 PR1217 PR1219 from 0ohm to R-short	20150122	PVT
16	Design Update	DFX request	P.43	Change the PJP201 footprint from ACES_50458-00801-001_8P-T to CVILU_CI9908M2HR0-NH_8P	20150122	PVT



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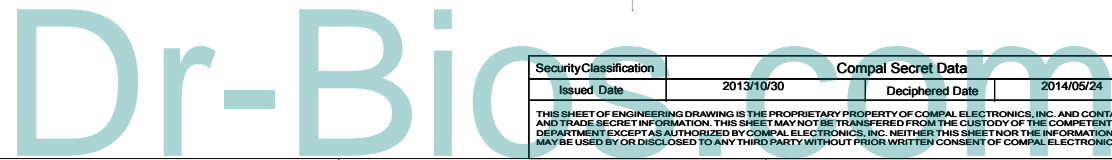


Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	35	Codec	11/10	PC Beep is digital signal	Change C2134 pin 2 connect from GNDA to GND.	DVT	0.2
2	37	USB charger	11/12	USB charger function abnormal.	Change U25 pin 4 from USB_CHARGE_2A to USB_EN Change U26 pin 4 from USB_EN to USB_CHARGE_2A	DVT	0.2
3	37	USB charger	11/17	Board ID change for DVT.	Change R506 from 0_0402_5% to 12K_0402_5%.	DVT	0.2
4	02	Block Diagram	11/19	Some block diagram descirptoin mistake.	Correct block diagram description.	DVT	0.2
5	38	EC	11/19	To solve 3V_EN need to connect to "Fixed code drive high" pin	change 3V_EN from pin 86 to 107, and original pin107 "DGPU_AC_DETECT" signal connect to EC pin 117 (NC now)	DVT	0.2
6	37	USB2.0	11/ 20	Follow EMI's request mail 1120.	Change L26 & L29 from CMMI21T-900Y-N_4P (0805 size) to MCM1012B900F06BP_4P (0504 size), and remove R458, R461, R454, R465 0_0402_5% co-lay resistors.	DVT	0.2
7	37	USB	11/ 26	JUSB3 change from bottom to top side.	Reverse JUSB3 pin connection.	DVT	0.2
8	32	LAN	11/ 27	Request by DFb	Change L2506 from SHI0000AA00 (S INDUC 2.2UH +-5% NLC252018T-2R2J-N) [2.2mm height] to SH00000RT00 (S COIL 2.2UH +-20% HPC252012NF-2R2M 1.3A) [1.2mm height]	DVT	0.2
9	39	LED	11/ 27	LED light test	Change R699 & R700 from 301_0402_1% to 470_0402_1%.	DVT	0.2
10	32	Crystal	11/ 27	Crystal EA.	Change C2558 & C2559 from 10P_0402_50V8J to 12P_0402_50V8J	DVT	0.2
11	40	Reset switch	12/ 01	RESET button 接EC_RST# or MAINPWON?	Add R2632 R-short connect to MAINPWON.	DVT	0.2
12	24, 25 26, 27	VRAM	12/ 01	fine tune VRAM	Swap U2004 & U2006 group2 connection. Swap U2008 & U2010 group4 connection.	DVT	0.2
13	40	Batt Switch	12/ 01	DFb request	Change SW4 from DE100000T00 to SN200003I00.	DVT	0.2
14	36	FFC HDD	12/ 01	FFC type HDD could pass Gen2 & Gen3 TX and iEMT EA	Add C413~C416, C538~C541 cap for co-layout without re-driver path.	DVT	0.2
15	19	NV	12/ 02	NV and EC didn't implement GPU_OVERT & GPU_ALERT code.	Change Q2000 from VGA@ to @.	DVT	0.2
16	19	NV	12/ 02	Follow NV's suggestion	1. Change D2002 & R2055 from GC6@ to @, change U2002 & R2628 from @ to GC6@. 2. Change Q2001 pin 2 & 5 from connect +3VSDGPU_MAIN to PLTRST_VGA#.	DVT	0.2
17	41	NV	12/ 03	N16V-GM not support GC6 2.0	Change J14 jumper to R2633 0_0603_5%	DVT	0.2
18	31	CRT	12/ 03	CRT EA RGB rise time fail	Change L2503 from SM01000FH00 (S SUPPRE_ MURATA BLM15BB470SN1D 0402) to SM01000LU00 ( S SUPPRE_ MURATA BLM15BA220SN1D 0402)	DVT	0.2
19	35	Part Reference	12/ 03	Correct part refererence type	Change R2120~R2123 to L2511~L2514	DVT	0.2



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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
42	40	Reset button	1/21	follow 2015 project design. Press reset button to pull down EC_RST# signal.	Change R2632 from R-short to non-pop. Change R2631 from non-pop to R-short.	PVT	1.0
43		NPI confirm	1/22	NPI test confirm ready.	1. Change R65, R427, R428, R368~R375,R2552, R2125, R2131, R2611, R467, R2618~R2626, R854 from 0_0402_5% to R-short. 2. Change R2075, R81 from 0_0603_5% to R-short.	PVT	1.0
44	39	update footprint	1/22	Link LED symbol to CIS.	Correct LED6 & LED7 footprint from LED_HT-210UD5-NB5_3P to LED_LTST-S115KFTBKT-CA_3P	PVT	1.0
45	37	USB power switch	1/22	Follow 2015 project USB power switch OC pin design.	Change R454 & R466 from R-short to non-pop.	PVT	1.0



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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
21	17	Test	12/05	Test plan	Reserve Q2007 , place close to U45.	DVT	0.2
22	10	Test	12/05	Test plan	Reserve R2634 , place close to U30.	DVT	0.2
23	13,17	DRAM	12/10	Choose cap. for better placement.	Depop C18, pop C118.	DVT	0.2
24	39	Lid SW	12/10	Change main source.	Change U4 PN to SA00008K800.	DVT	0.2
25	37	USB20 choke	12/17	SM070003K00 will shift when SMT and prohibit by factory.	Change L26 & L29 to SM070003Y00.	DVT	0.2
26	19	NV	12/17	To prevent could not read or read wrong graphic temperature via I2C and cause over temperature.	Add Q2000 to let GPU_OVERT work.	DVT	0.2
27	19	NV	12/17	VGA_PWROK pull high to +3VS via 10K ohm, but R2014 10K pull down will make VGA_PWROK high voltage level out of spec.	Change R2014 from 10K to 200K ohm. (Follow NV reference schematic.)	DVT	0.2
28	38	Board ID	12/22	Change board ID for PCB Revision 0.3	Change R506 from SD028120280 12K ohm to SD028150280 15K ohm	PVT	1.0
29	13, 17	POS Cap	12/22	Follow schematic design common rule, POS Cap should use Serial P/N	Change C18 & C118 from SGA20331E10 to SGA00009500	PVT	1.0
30	39	ON/OFF button	12/30	SW6 is for RD test at NPI phase only.	Change SW6 from DB@ to @.	PVT	1.0
31	39	LED	12/30	LED test with DVT ME module.	Change R699 & R700 from 470 ohm (SD034470080) to 560 ohm (SD000008380) Change R698 & R701 from 390 ohm (SD00000QZ00) to 430 ohm (SD00000LM00 )	PVT	1.0
32	19	NV	12/30	GPU throttle test.	Reserve U17 for test.	PVT	1.0
33	39	NV	12/30	Reserve level shift circuit to prevent Elan touch pad back drive issue.	Reserve Q2008, R2640~R2642 level shift circuit.	PVT	1.0
34		Component	1/7	Follow standard part	Change Q7, Q8, Q14, Q15, Q40, Q1007, Q2000, Q2001, Q2003, Q2004, Q2008 from SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6) to SB00000PV00 (S TR L2N7002DW1T1G 2N SC88-6)	PVT	1.0
35	36	Test	1/8	Reserve G-SEN_INT2 connector to JHDD2.	Reserve R2643 & R2644.	PVT	1.0
36	34	WLAN	1/12	SUSCLK will back drive to +3VS_WLAN when S3 or S5 with Broadcom NFA435 module. Check module datasheet not support SUSCLK, and intel module could define as NC.	Change R2612 from R-short to non-pop.	PVT	1.0
37	40	Screw hole	1/12	ME change NGFF standoff hole from 3.2 change to 3.3mm	Change H17 Footprint from H_3P2 to H_3P3.	PVT	1.0
38	35	Codec	1/19	ALC255 have PC beep in detect ciucuit in chip. Signal level under 400mV will disable PC Beep function.	Change R2140 from SD028470280 (47K_0420_5%) to SD028270280 (27K_0402_5%)	PVT	1.0
39	41	NV	1/19	To meet N16S-GT power sequence	Add virtual symbol R469 for SGT@, change vaule from 47K_0402_5% to 20K_0402_5%. Original R469 change from VGA@ to VGM@.	PVT	1.0
40	37	USB Charger	1/19	USB charger CB pin need a dedicate pin to control behavior.	Change USB charger CB control pin from SUSP# to USB_CHARGE_CB connect to EC pin 86.	PVT	1.0
41	18	ESD	1/21	ESD Jason request to reserve a cap for DIMM_DRAMRST#.	Reserve C2611.	PVT	1.0

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				Custom	Z5WAH M/B LA-B161P
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