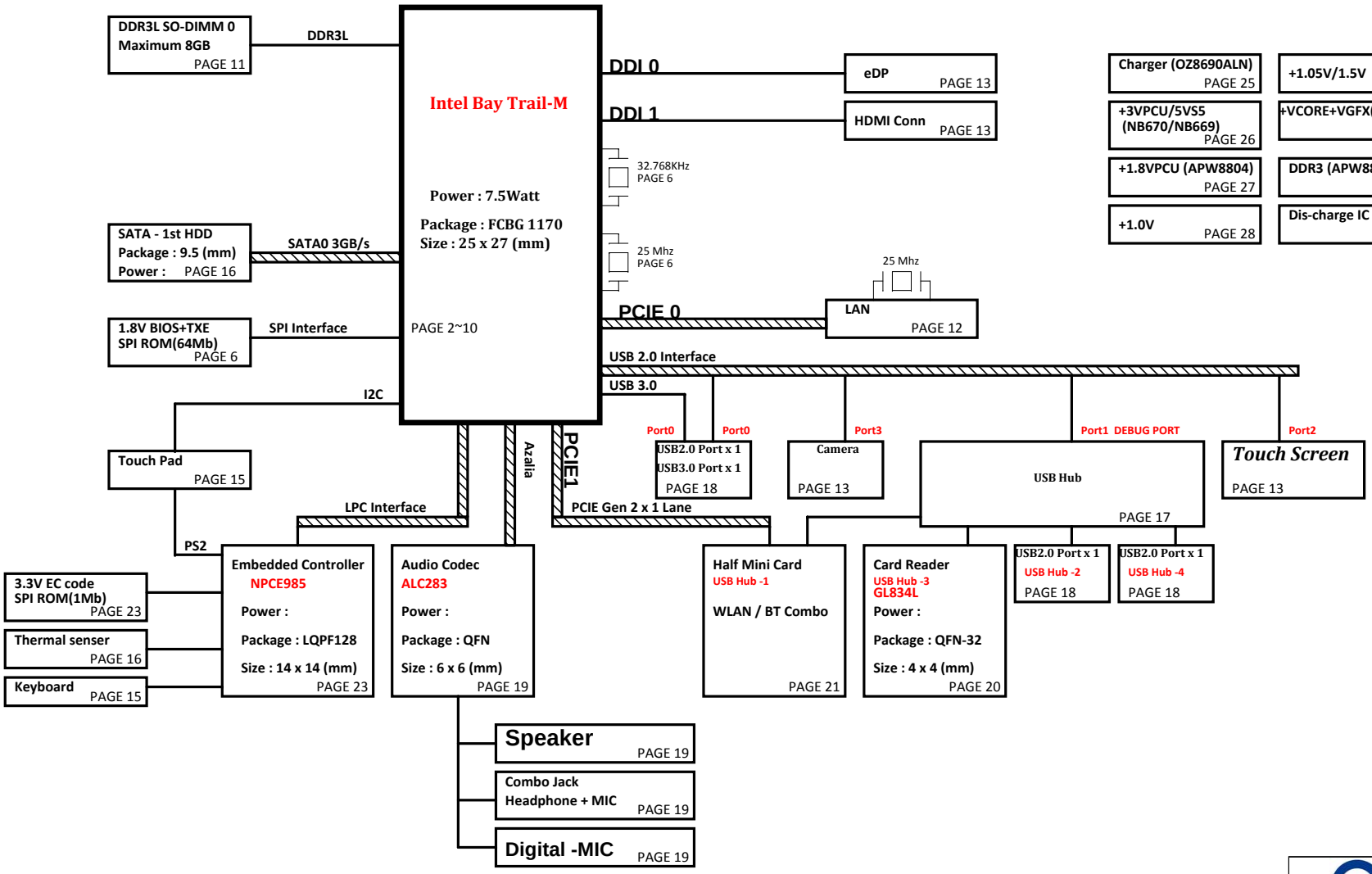
Roxy UMA(11.6")

Intel Bay Trail-M Platform Block Diagram

PCB 6L STACK-UP

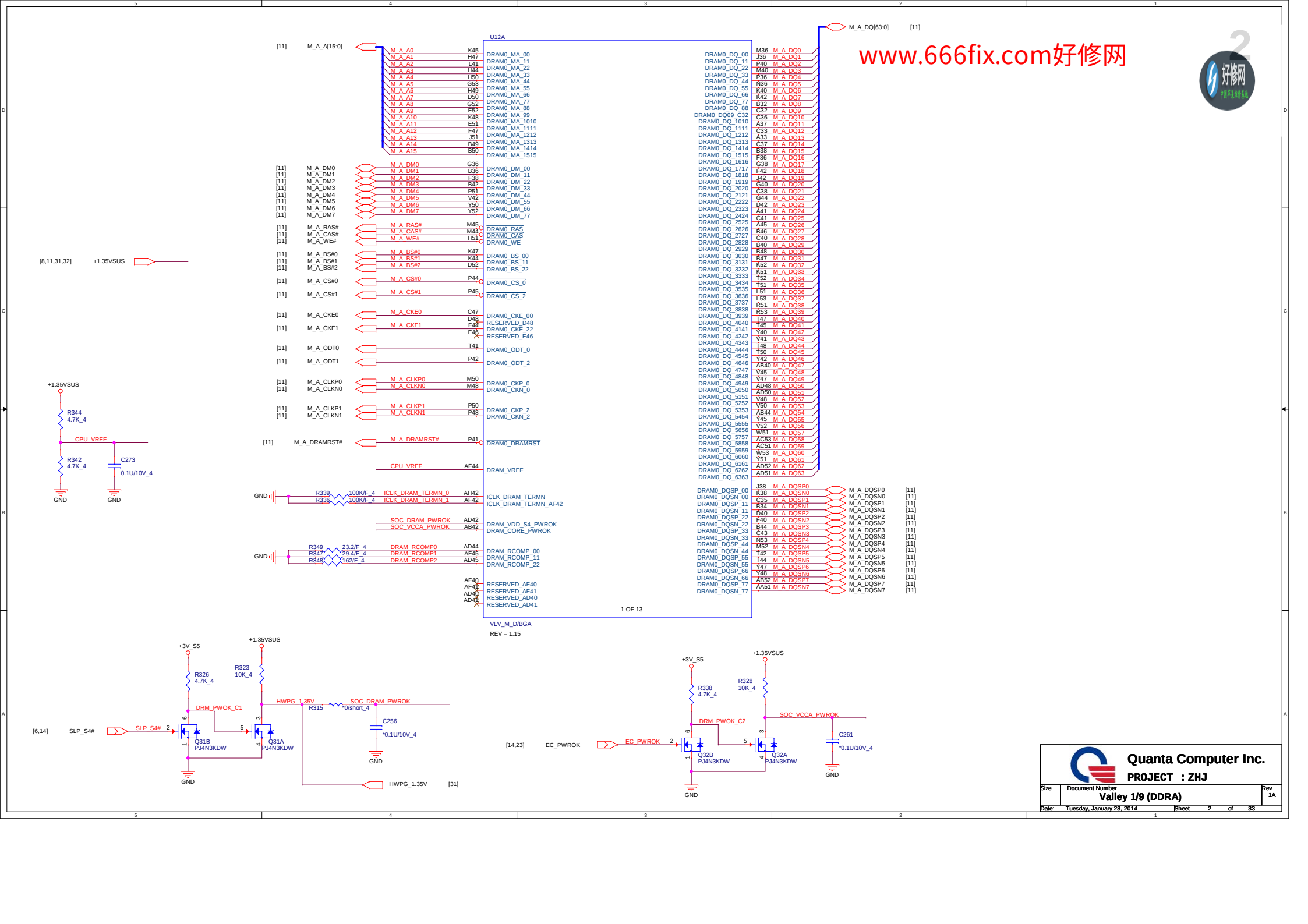
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

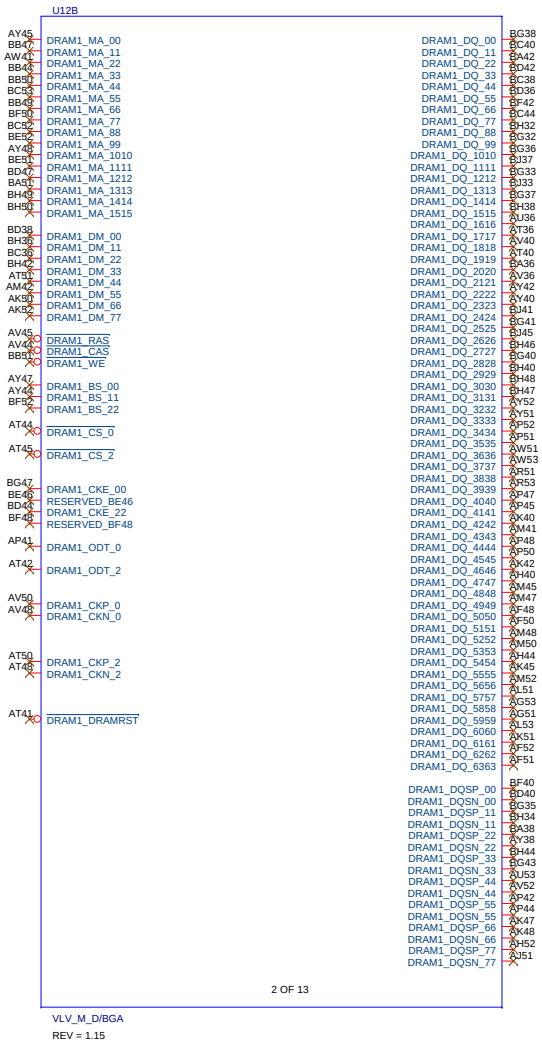


Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	Intel Block Diagram	1A

Date: Tuesday, January 28, 2014 Sheet 1 of 33


www.666fix.com好修网
U12A
M_A_DQ[63:0]
[11]
M_A_A[15:0]
M_A_A0
M_A_A1
M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
M_A_A7
M_A_A8
M_A_A9
M_A_A10
M_A_A11
M_A_A12
M_A_A13
M_A_A14
M_A_A15
M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_BS#0
M_A_BS#1
M_A_BS#2
M_A_CS#0
M_A_CS#1
M_A_CKE0
M_A_CKE1
M_A_ODT0
M_A_ODT1
M_A_CLKP0
M_A_CLKN0
M_A_CLKP1
M_A_CLKN1
M_A_DRAMRST#
CPU_VREF
SOC_DRAM_PWROK
SOC_VCCA_PWROK
DRAM_RCOMP0
DRAM_RCOMP1
DRAM_RCOMP2
RESERVED_AF40
RESERVED_AF41
RESERVED_AD40
RESERVED_AD41
1 OF 13
VLV_M_D/BGA
REV = 1.15
[8,11,31,32]
+1.35VSUS
R344 4.7K_4
R342 4.7K_4
C273 0.1U/10V_4
GND
R339 100K/F_4
R336 100K/F_4
ICLK_DRAM_TERMN_0
ICLK_DRAM_TERMN_1
R349 23.2/F_4
R347 29.4/F_4
R348 162/F_4
+3V_S5
R326 4.7K_4
R323 10K_4
DRM_PWOK_C1
HWPG_1.35V
R315 *0/short_4
C256 *0.1U/10V_4
[6,14]
SLP_S4#
Q31B PJ4N3KDW
Q31A PJ4N3KDW
[31]
[14,23]
EC_PWROK
R338 4.7K_4
R328 10K_4
DRM_PWOK_C2
C261 *0.1U/10V_4
Q32B PJ4N3KDW
Q32A PJ4N3KDW
Quanta Computer Inc.
PROJECT : ZHJ
Size
Document Number
Valley 1/9 (DDRA)
Rev 1A
Date: Tuesday, January 28, 2014
Sheet 2 of 33

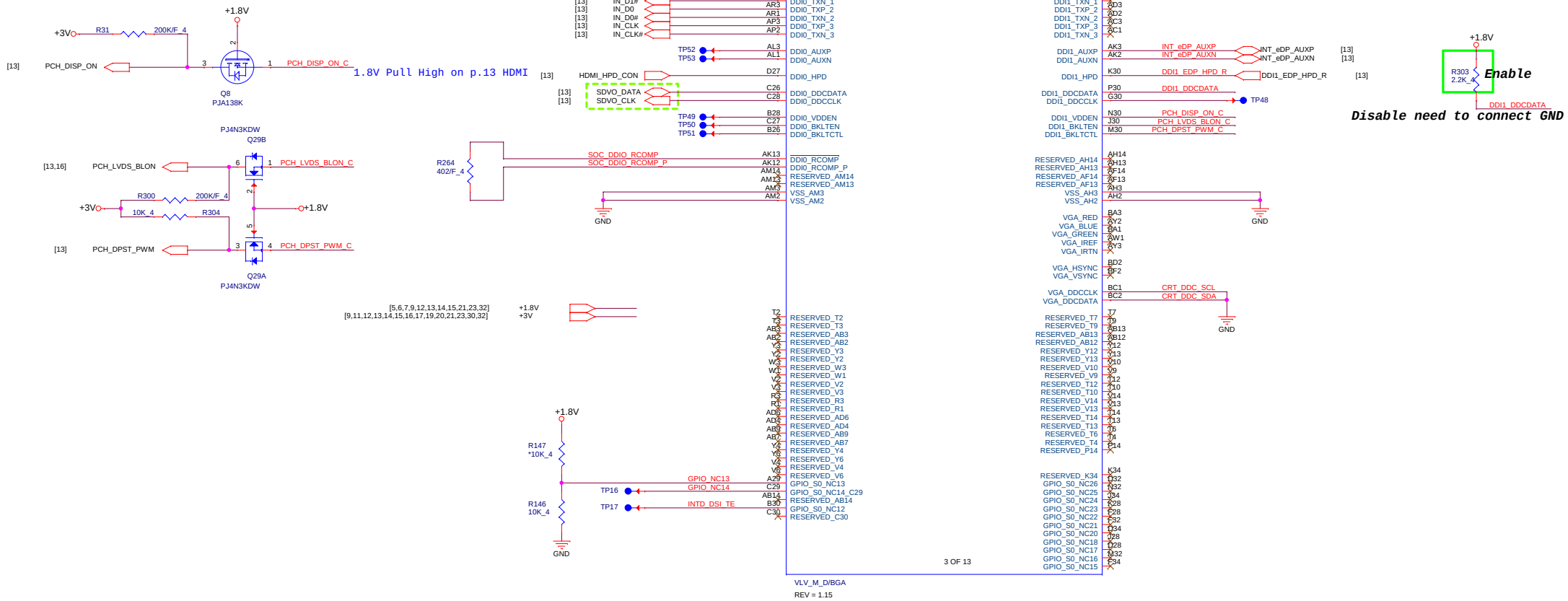


Quanta Computer Inc.

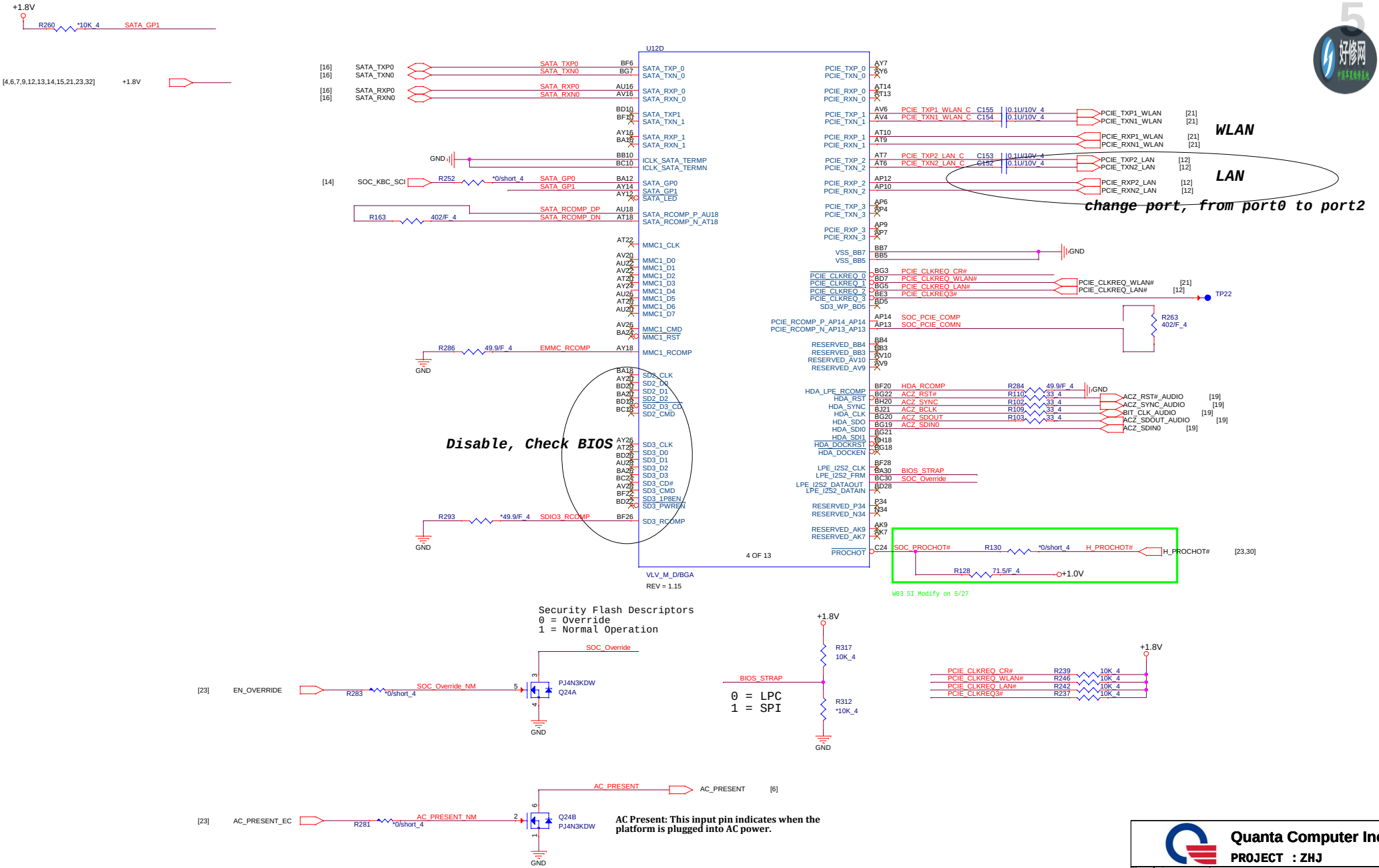
PROJECT : ZHJ

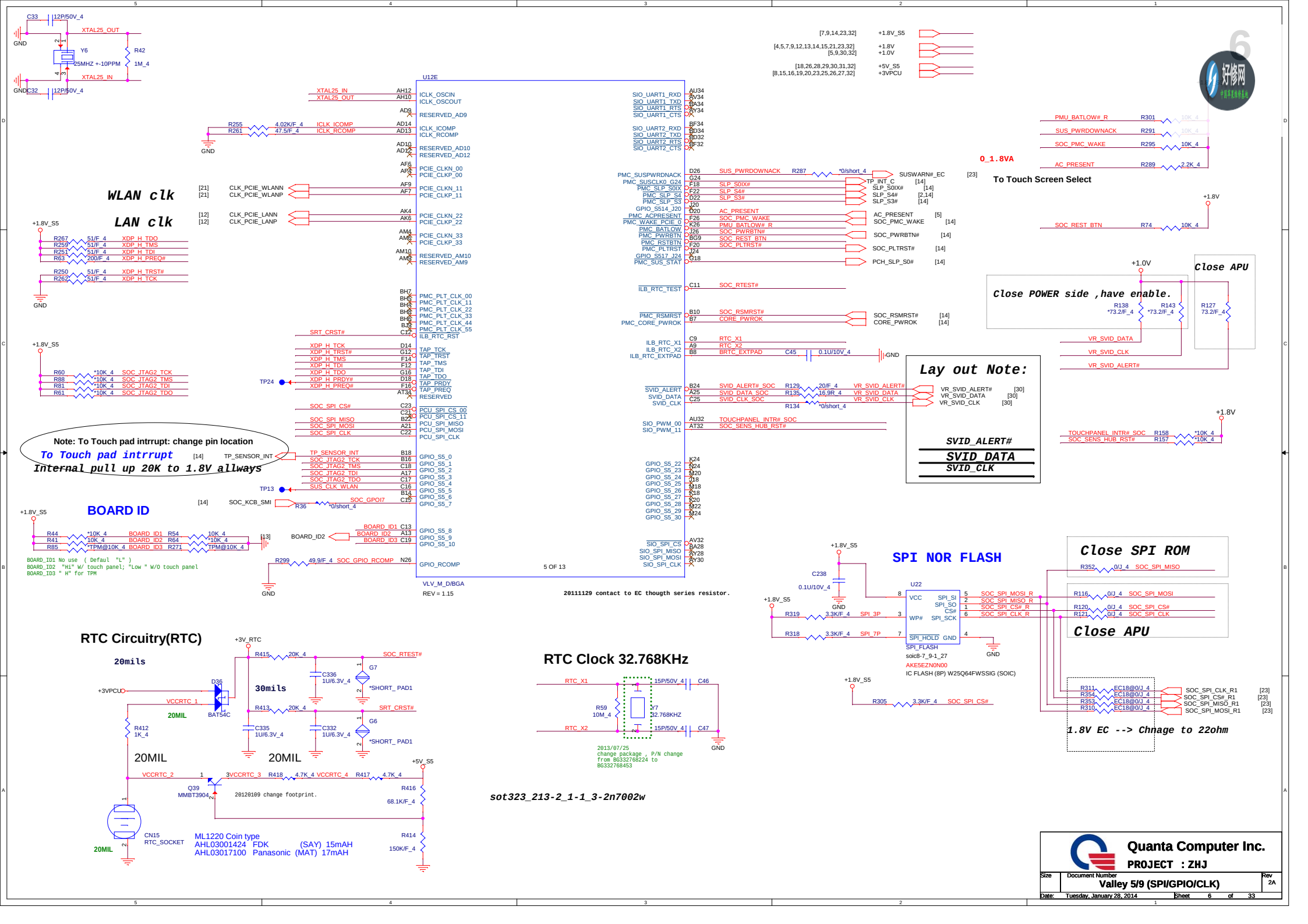
Size	Document Number	Rev
	Valley 2/9 (DDRB)	1A

Date: Tuesday, January 28, 2014 Sheet 3 of 33



Quanta Computer Inc.			
PROJECT : ZHJ			
Size	Document Number		Rev
	Valley 3/9 (Display)		2A
Date: Tuesday, January 28, 2014		Sheet 4 of 33	


+1.8V
R260 *10K_4 SATA_GP1
[4,6,7,9,12,13,14,15,21,23,32] +1.8V
U12D
[16] SATA_TXP0
[16] SATA_TXN0
[16] SATA_RXP0
[16] SATA_RXN0
SATA_TXP0 BF6
SATA_TXN0 BG7
SATA_RXP0 AU16
SATA_RXN0 AV16
SATA_TXP_0
SATA_TXN_0
SATA_RXP_0
SATA_RXN_0
BD10 SATA_TXP1
BF10 SATA_TXN_1
AY16 SATA_RXP_1
BA16 SATA_RXN_1
GND
BB10 ICLK_SATA_TERMP
BC10 ICLK_SATA_TERMN
[14] SOC_KBC_SCI
R252 *0/short_4
SATA_GP0 BA12
SATA_GP1 AY14
AY12 SATA_LED
R163 402/F_4
SATA_RCOMP_DP AU18
SATA_RCOMP_DN AT18
SATA_RCOMP_P_AU18
SATA_RCOMP_N_AT18
AT22 MMC1_CLK
AV20 MMC1_D0
AU22 MMC1_D1
AV22 MMC1_D2
AT20 MMC1_D3
AY24 MMC1_D4
AU26 MMC1_D5
AT26 MMC1_D6
AU20 MMC1_D7
AV26 MMC1_CMD
BA24 MMC1_RST
R286 49.9/F_4
EMMC_RCOMP AY18
MMC1_RCOMP
BA18 SD2_CLK
AY20 SD2_D0
BD20 SD2_D1
BA20 SD2_D2
BD18 SD2_D3_CD
BC18 SD2_CMD
AY26 SD3_CLK
AT28 SD3_D0
BD26 SD3_D1
AU28 SD3_D2
BA26 SD3_D3
BC28 SD3_CD#
AV28 SD3_CMD
BF22 SD3_1P8EN
BD22 SD3_PWREN
R293 *49.9/F_4
SDIO3_RCOMP BF26
SD3_RCOMP
Disable, Check BIOS
4 OF 13
VLV_M_D/BGA
REV = 1.15
PCIE_TXP_0 AY7
PCIE_TXN_0 AY6
PCIE_RXP_0 AT14
PCIE_RXN_0 AT13
PCIE_TXP_1 AV6
PCIE_TXN_1 AV4
PCIE_TXP1_WLAN_C C155 0.1U/10V_4
PCIE_TXN1_WLAN_C C154 0.1U/10V_4
PCIE_TXP1_WLAN [21]
PCIE_TXN1_WLAN [21]
PCIE_RXP_1 AT10
PCIE_RXN_1 AT9
PCIE_RXP1_WLAN [21]
PCIE_RXN1_WLAN [21]
WLAN
PCIE_TXP_2 AT7
PCIE_TXN_2 AT6
PCIE_TXP2_LAN_C C153 0.1U/10V_4
PCIE_TXN2_LAN_C C152 0.1U/10V_4
PCIE_TXP2_LAN [12]
PCIE_TXN2_LAN [12]
PCIE_RXP_2 AP12
PCIE_RXN_2 AP10
PCIE_RXP2_LAN [12]
PCIE_RXN2_LAN [12]
LAN
change port, from port0 to port2
PCIE_TXP_3 AP6
PCIE_TXN_3 AP4
PCIE_RXP_3 AP9
PCIE_RXN_3 AP7
VSS_BB7 BB7
VSS_BB5 BB5
GND
PCIE_CLKREQ_0 BG3 PCIE_CLKREQ_CR#
PCIE_CLKREQ_1 BD7 PCIE_CLKREQ_WLAN#
PCIE_CLKREQ_2 BG5 PCIE_CLKREQ_LAN#
PCIE_CLKREQ_3 BE3 PCIE_CLKREQ3#
PCIE_CLKREQ_WLAN# [21]
PCIE_CLKREQ_LAN# [12]
TP22
SD3_WP_BD5 BD5
PCIE_RCOMP_P_AP14_AP14 AP14 SOC_PCIE_COMP
PCIE_RCOMP_N_AP13_AP13 AP13 SOC_PCIE_COMN
R263 402/F_4
RESERVED_BB4 BB4
RESERVED_BB3 BB3
RESERVED_AV10 AV10
RESERVED_AV9 AV9
HDA_LPE_RCOMP BF20 HDA_RCOMP
HDA_RST BG22 ACZ_RST#
HDA_SYNC BH20 ACZ_SYNC
HDA_CLK BJ21 ACZ_BCLK
HDA_SDO BG20 ACZ_SDOUT
HDA_SDI0 BG19 ACZ_SDIN0
HDA_SDI1 BG21
HDA_DOCKRST BH18
HDA_DOCKEN BG18
R284 49.9/F_4
R110 33_4
R102 33_4
R109 33_4
R103 33_4
ACZ_RST#_AUDIO [19]
ACZ_SYNC_AUDIO [19]
BIT_CLK_AUDIO [19]
ACZ_SDOUT_AUDIO [19]
ACZ_SDIN0 [19]
LPE_I2S2_CLK BF28
LPE_I2S2_FRM BA30 BIOS_STRAP
LPE_I2S2_DATAOUT BC30 SOC_Override
LPE_I2S2_DATAIN BD28
RESERVED_P34 P34
RESERVED_N34 N34
RESERVED_AK9 AK9
RESERVED_AK7 AK7
PROCHOT C24
SOC_PROCHOT# R130 *0/short_4 H_PROCHOT#
H_PROCHOT# [23,30]
R128 71.5/F_4 +1.0V
W03 SI Modify on 5/27
Security Flash Descriptors
0 = Override
1 = Normal Operation
SOC_Override
[23] EN_OVERRIDE
R283 *0/short_4
SOC_Override_NM
PJ4N3KDW
Q24A
GND
BIOS_STRAP
R317 10K_4
R312 *10K_4
0 = LPC
1 = SPI
PCIE_CLKREQ_CR# R239 10K_4
PCIE_CLKREQ_WLAN# R246 10K_4
PCIE_CLKREQ_LAN# R242 10K_4
PCIE_CLKREQ3# R237 10K_4
AC_PRESENT
AC_PRESENT [6]
[23] AC_PRESENT_EC
R281 *0/short_4
AC_PRESENT_NM
Q24B
PJ4N3KDW
AC Present: This input pin indicates when the platform is plugged into AC power.
Quanta Computer Inc.
PROJECT : ZHJ
Size
Document Number
Valley 4/9 (SD/PCIE/SATA)
Rev 2A
Date: Tuesday, January 28, 2014
Sheet 5 of 33


WLAN clk
LAN clk
Note: To Touch pad intrrupt: change pin location
To Touch pad intrrupt
Internal pull up 20K to 1.8V allways
BOARD ID
RTC Circuitry(RTC)
RTC Clock 32.768KHz
SPI NOR FLASH
Lay out Note:
SVID_ALERT#
SVID_DATA
SVID_CLK
Close APU
Close POWER side ,have enable.
Close SPI ROM
Close APU
1.8V EC --> Chnage to 22ohm
To Touch Screen Select
0_1.8VA
20111129 contact to EC thougth series resistor.
sot323_213-2_1-1_3-2n7002w
ML1220 Coin type
AHL03001424 FDK (SAY) 15mAH
AHL03017100 Panasonic (MAT) 17mAH
Quanta Computer Inc.
PROJECT : ZHJ
Valley 5/9 (SPI/GPIO/CLK)
Tuesday, January 28, 2014

[6,9,14,23,32] +1.8V_S5

[4,5,6,9,12,13,14,15,21,23,32] +1.8V

[4,9,11,12,13,14,15,16,17,19,20,21,23,30,32] +3V

U12F

+1.8V_S5

R48 *10K_4 SOC_PWR_BUT

Port 1 is debug port

USB 2.0 / 3.0 Base

HUB1

Touch Panel

CAMERA

[18] USBP0+ [18] USBP0- — M16 K16 USB_DP0 USB_DN0

[17] USB_H1_P [17] USB_H1_N — J14 G14 USB_DP1 USB_DN1

[13] USBP2+ [13] USBP2- — K12 J12 USB_DP2 USB_DN2

[13] USBP3+ [13] USBP3- — K10 H10 USB_DP3 USB_DN3

R249 1K/F_4 ICLK_USB_TERMN_0 — D10 ICLK_USB_TERMN_D10

R248 1K/F_4 ICLK_USB_TERMN_1 — F10 ICLK_USB_TERMN

GND

[18] SOC_USB_OC0

R105 10K_4

R104 10K_4

+1.8V_S5

C20 B20 USB_OC_00 USB_OC_11

[18] SOC_USB_OC1

R247 45.3/F_4 USB_RCOMP — D6 C7 USB_RCOMPO USB_RCOMPI

GND

R270 *0/J_4 — M13 USB_PLL_MON

GND

B4 B5 USB_HSIC0_DATA USB_HSIC0_STROBE

E2 D2 USB_HSIC1_DATA USB_HSIC1_STROBE

GND R55 45.3/F_4 USB_HSIC_RCOMP — A7 USB_HSIC_RCOMP

R285 49.9/F_4

LPC_RCOMP — BF18 LPC_RCOMP

12.5 Ohm

[15,21,23] LAD0 — LAD0 BH16 ILB_LPC_AD_00

[15,21,23] LAD1 — LAD1 BJ17 ILB_LPC_AD_11

[15,21,23] LAD2 — LAD2 BJ13 ILB_LPC_AD_22

[15,21,23] LAD3 — LAD3 BG14 ILB_LPC_AD_33

[15,21,23] LFRAME# — LFRAME# BG17 ILB_LPC_FRAME

[15] PCLK_TPM — R98 22_4 — SOC_CLKOUT_0 BG15 ILB_LPC_CLK_00

[23] CLK_24M_KBC — R90 22_4 — SOC_CLKOUT_1 BH14 ILB_LPC_CLK_11

[21] CLK_24M_DEBUG — R274 22_4

[15,23] CLKRUN# — R279 22_4 — SOC_CLKRUN# BG16 ILB_LPC_CLKRUN

[14] SOC_SERIRQ — SOC_SERIRQ BG13 ILB_LPC_SERIRQ

[14] SMB_SOC_DATA

[14] SMB_SOC_CLK

+1.8V

R79 2.2K_4 SMB_SOC_DATA — BG12 PCU_SMB_DATA

R73 2.2K_4 SMB_SOC_CLK — BH10 PCU_SMB_CLK

R80 2.2K_4 SMB_SOC_ALERTB_C — BG11 PCU_SMB_ALERT

R7386 follow CRB and check list change to 2.2K

GPIO_S5_31 G2

GPIO_S5_32 M3

GPIO_S5_33 L1

GPIO_S5_34 K2

GPIO_S5_35 K3

GPIO_S5_36 M2

GPIO_S5_37 N3

GPIO_S5_38 P2

GPIO_S5_39 L3

GPIO_S5_40 J3

GPIO_S5_41 P3

GPIO_S5_42 H3

GPIO_S5_43 B12

RESERVED_M10 M10

RESERVED_M9 M9

RESERVED_P7 P7

RESERVED_P6 P6

RESERVED_M7 M7

USB3_REXT0 M12 USB3_P0_REXT R258 1.24K/F_4

GND

RESERVED_P10 P10

RESERVED_P12 P12

RESERVED_M4 M4

RESERVED_M6 M6

USB3_RXP0 D4 USB30_RX1+ [18]

USB3_RXN0 E3 USB30_RX1- [18]

USB3_TXP0 K6 USB30_TX1+ [18]

USB3_TXN0 K7 USB30_TX1- [18]

+1.8V

TOUCH_PANEL_SOC_RST# R269 *10K_4

SOC_SENSOR_HUB_WAKE R265 *10K_4

RESERVED_H8 H8

RESERVED_H7 H7

RESERVED_H5 H5

RESERVED_H4 H4

Top Swap (A16 Override)
0 = Top address bit is unchanged
1 = Top address bit is inverted

+1.8V

R253 *10K_4

R254 *10K_4

GND

GPIO_S0_SC_55 BD12

GPIO_S0_SC_56 BC12 GPIO_S0_SC_56

GPIO_S0_SC_57 BD14 SOC_UART_TX

GPIO_S0_SC_58 BC14

GPIO_S0_SC_59 BF14 SOC_SENSOR_HUB_WAKE

GPIO_S0_SC_60 BD16 TOUCH_PANEL_SOC_RST#

GPIO_S0_SC_61 BC16 SOC_UART_RX

ILB_8254_SPKR BH12 ACZ_SPKR [19]

SOC_UART_TX R273 *0_4 SOC_UART_RX

Un-Stuff for Test Only

+1.8V

I2C_6_SDA R118 560_4

I2C_6_SCL R119 560_4

I2C_1_SDA R123 *2.2K_4

I2C_1_SCL R125 *2.2K_4

I2C_2_SDA_R R126 *2.2K_4

I2C_2_SCL_R R132 *2.2K_4

I2C_3_SDA R136 *2.2K_4

I2C_3_SCL R137 *2.2K_4

I2C_4_SDA R142 *2.2K_4

I2C_4_SCL R141 *2.2K_4

I2C_5_SDA R140 *2.2K_4

I2C_5_SCL R145 *2.2K_4

I2C_66_SDA R151 *2.2K_4

I2C_66_SCL R152 *2.2K_4

TP_NC R155 *2.2K_4

TP_NC1 R156 *2.2K_4

SIO_I2C0_DATA BH22 I2C_0_SDA R108 22_4 I2C_6_SDA I2C_6_SDA [14]

SIO_I2C0_CLK BG23 I2C_0_SCL R117 22_4 I2C_6_SCL I2C_6_SCL [14]

SIO_I2C1_DATA BG24 I2C_1_SDA

SIO_I2C1_CLK BH24 I2C_1_SCL

SIO_I2C2_DATA BG25 I2C_2_SDA_R

SIO_I2C2_CLK BJ25 I2C_2_SCL_R

SIO_I2C3_DATA BG26 I2C_3_SDA

SIO_I2C3_CLK BH26 I2C_3_SCL

SIO_I2C4_DATA BF27 I2C_4_SDA

SIO_I2C4_CLK BG27 I2C_4_SCL

SIO_I2C5_DATA BH28 I2C_5_SDA

SIO_I2C5_CLK BG28 I2C_5_SCL

SIO_I2C6_DATA BJ29 I2C_66_SDA

SIO_I2C6_CLK BG29 I2C_66_SCL

GPIO_S0_SC_092 BH30 TP_NC

GPIO_S0_SC_093 BG30 TP_NC1

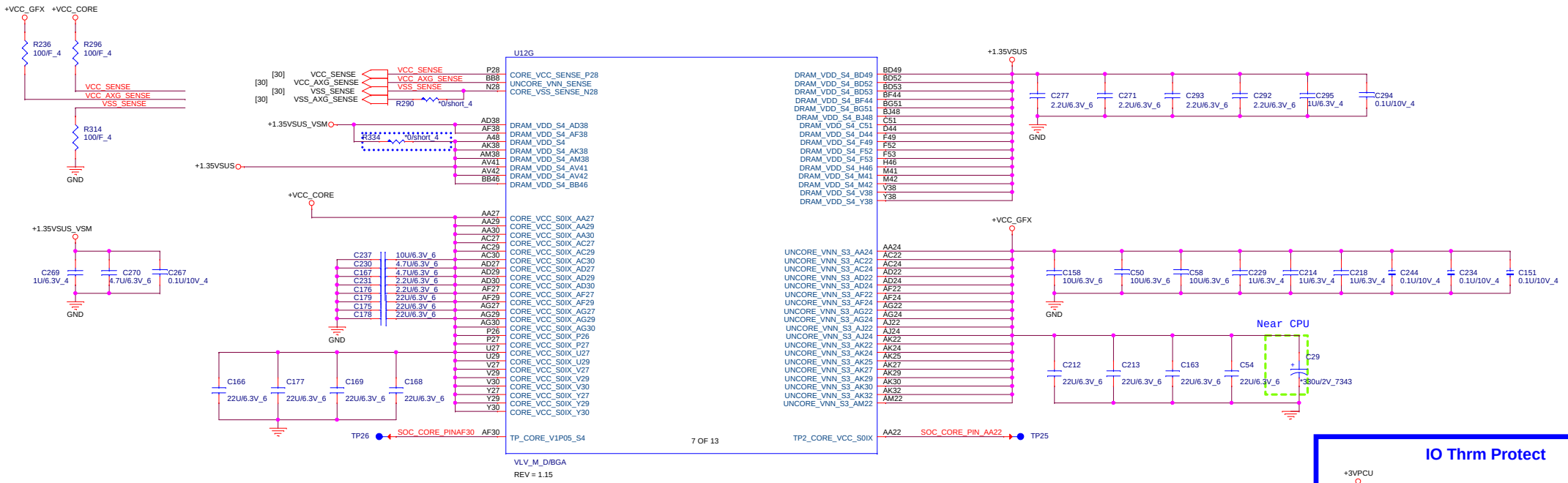
I2C pull up:
Standard/ Fast Mode --> 560 ohm
Hight speed mode --> CLK- 560 ohm;
DATA- 910 ohm

6 OF 13

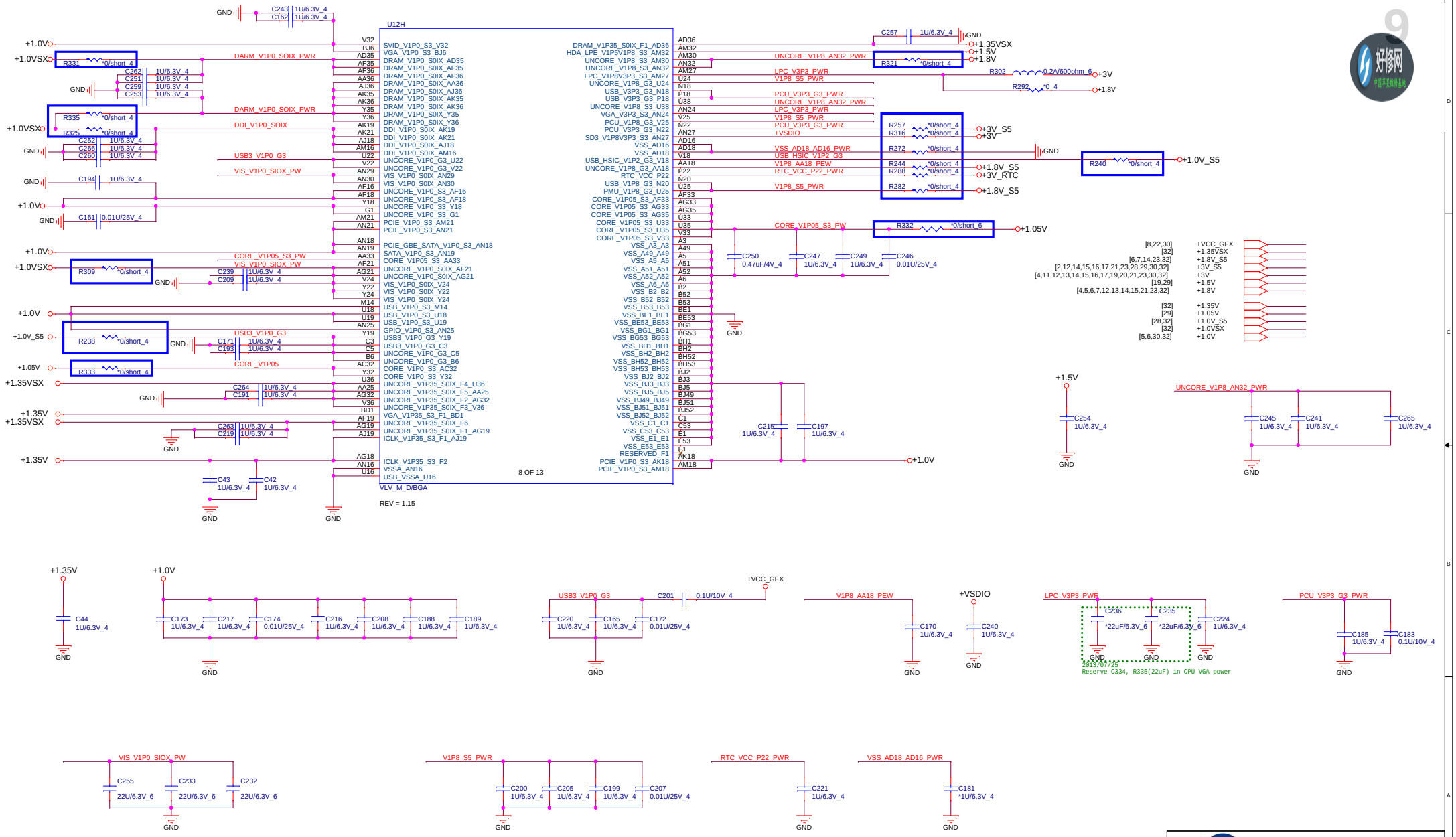
VLV_M_D/BGA

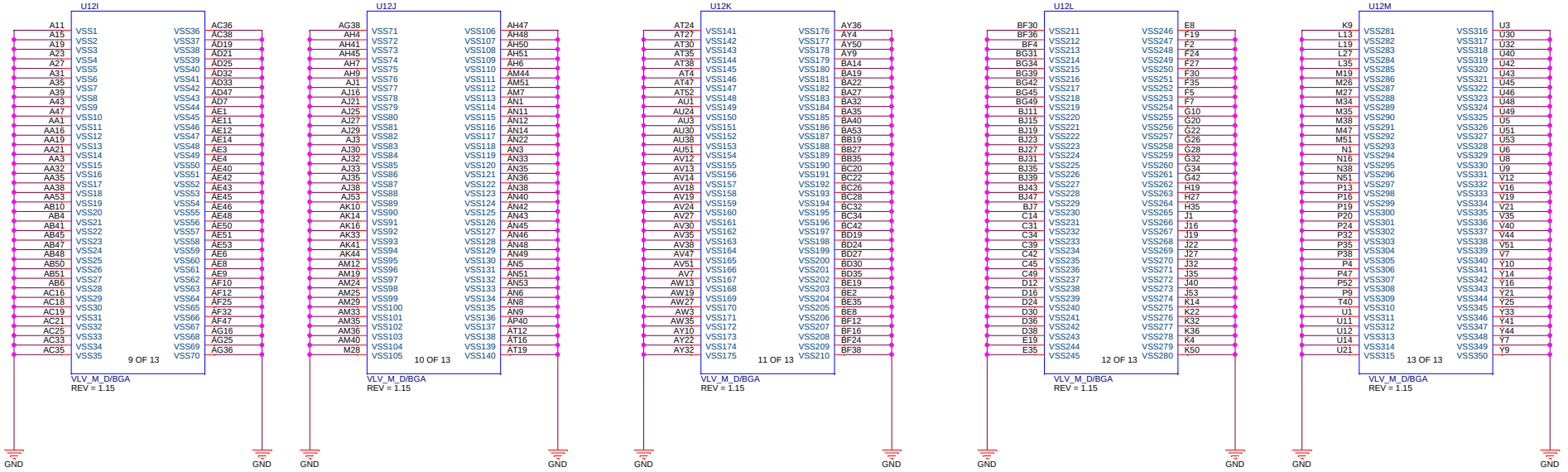
REV = 1.15

Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: Valley 6/9 (USB/LPC/I2C)	Rev 2A
Date: Tuesday, January 28, 2014	Sheet 7 of 33	



Quanta Computer Inc.	PROJECT : ZHJ	
Size	Document Number: Valley 7/9 (Power 1)	Rev: 2A
Date: Tuesday, January 28, 2014	Sheet 8 of 33	

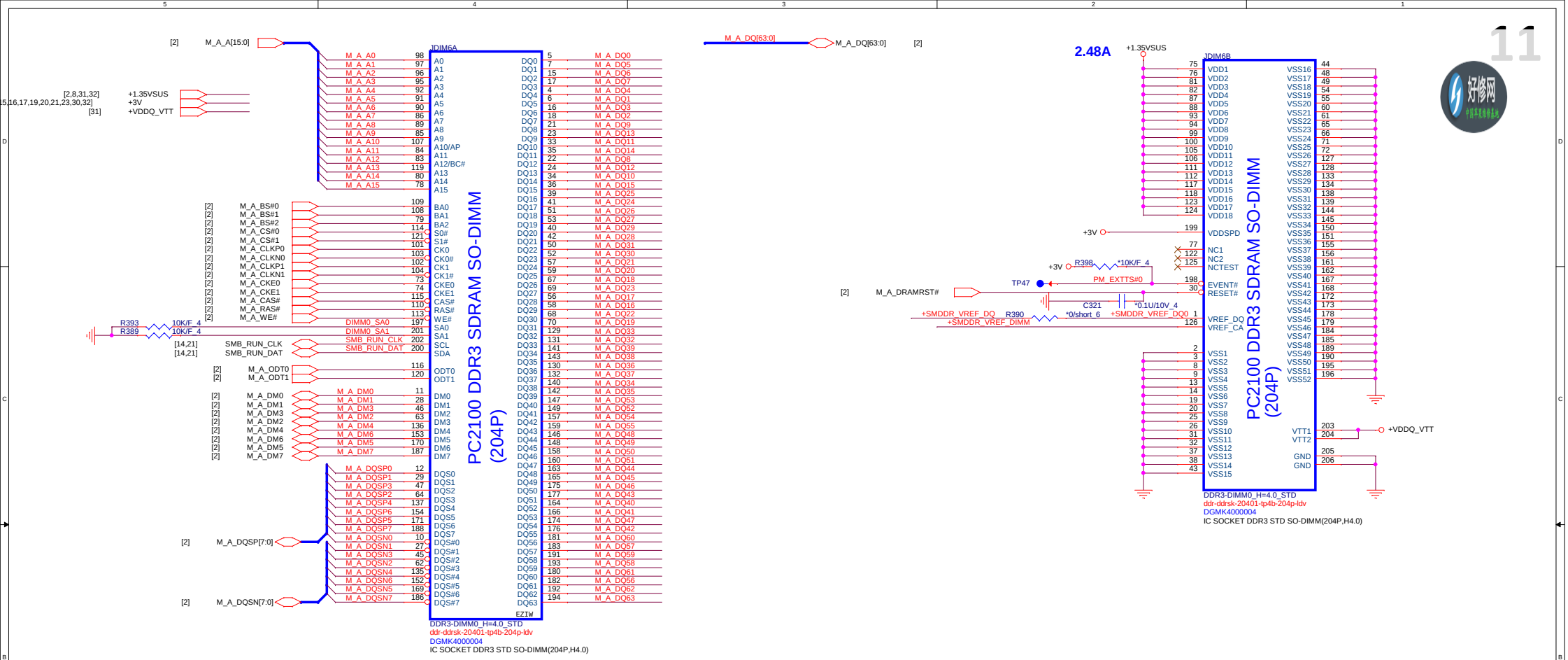

U12H
8 OF 13
VLV_M_D/BGA
REV = 1.15
DARM_V1P0_SOIX_PWR
DDI_V1P0_SOIX
USB3_V1P0_G3
VIS_V1P0_SIOX_PW
CORE_V1P05_S3_PW
CORE_V1P05
UNCORE_V1P8_AN32_PWR
LPC_V3P3_PWR
V1P8_S5_PWR
PCU_V3P3_G3_PWR
VSS_AD18_AD16_PWR
USB_HSIC_V1P2_G3
RTC_VCC_P22_PWR
+VSDIO
+VCC_GFX
V1P8_AA18_PEW
Reserve C334, R335(22uF) in CPU VGA power
Quanta Computer Inc.
PROJECT : ZHJ
Valley 8/9 (Power 2)
Rev 1A
Tuesday, January 28, 2014
Sheet 9 of 33



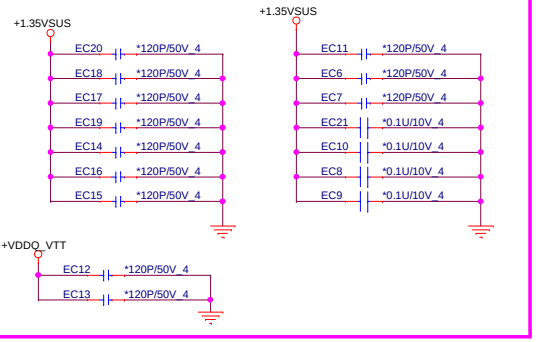
Quanta Computer Inc.

PROJECT : ZHJ

Size	Document Number	Rev
	Valley 9/9 (GND)	1A
Date: Tuesday, January 28, 2014	Sheet 10 of 33	

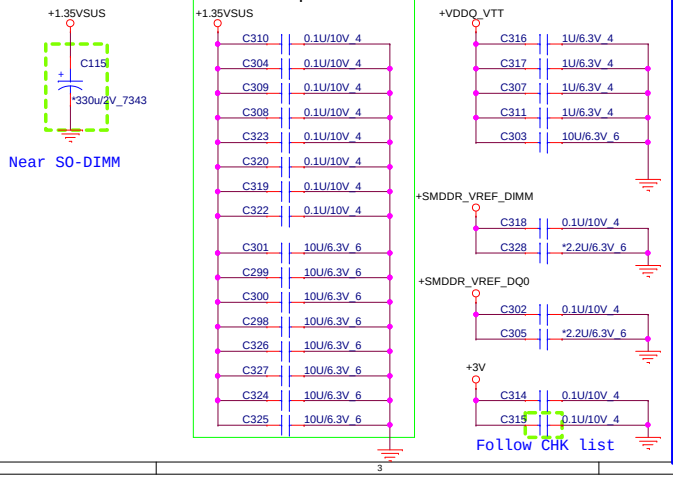


For EMI RESERVE

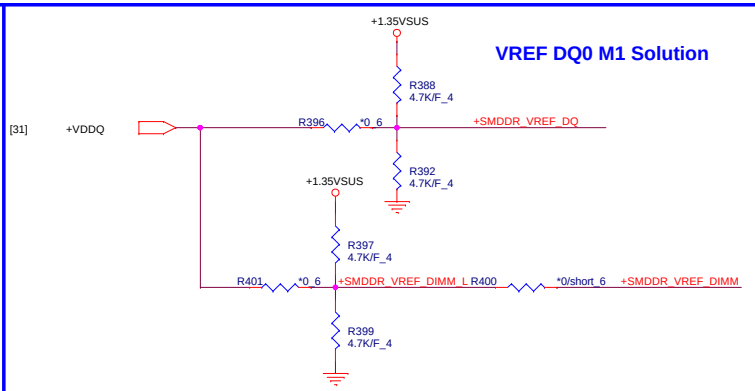


Place these Caps near So-Dimm0.

0.1uF/10uF 4pcs on each side of connector



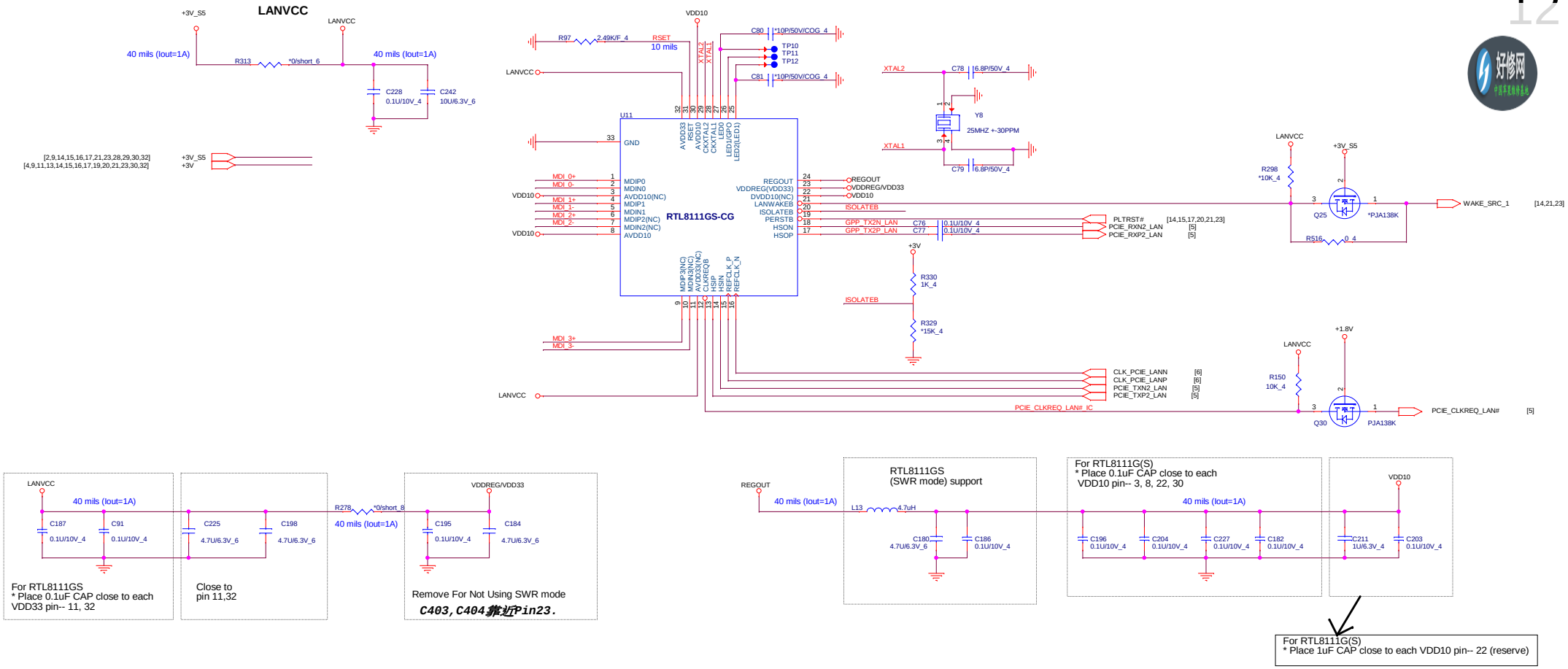
VREF DQ0 M1 Solution



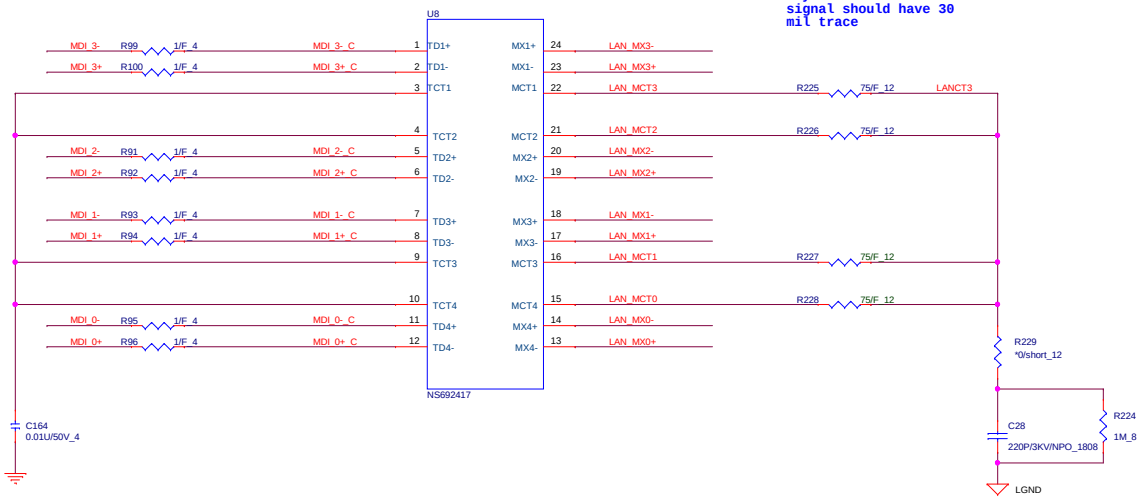
Quanta Computer Inc.

PROJECT : ZHJ

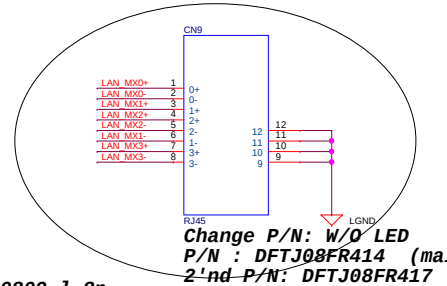
Size	Document Number	Rev
	DDR3 DIMM0-STD(4.0H)	1A
Date: Tuesday, January 28, 2014	Sheet 11 of 33	



Tramsformer



RJ45 Connector

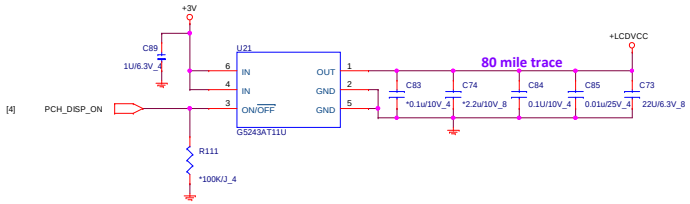


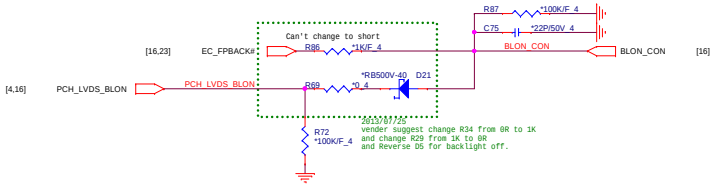
Change P/N: W/O LED
P/N : DFTJ08FR414 (main)
2'nd P/N: DFTJ08FR417
change footprint

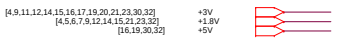
rj45-c100mp-10809-l-8p

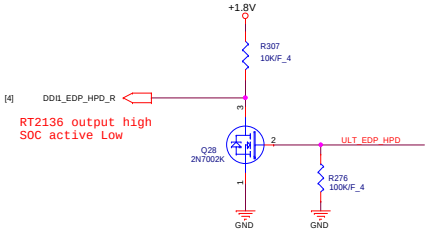
Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: LAN (RTL8111GS)	Rev: 2A
Date: Tuesday, January 28, 2014	Sheet 12 of 33	

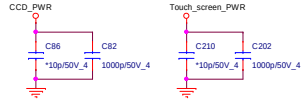
LVDS Conn.

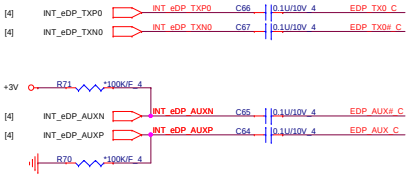


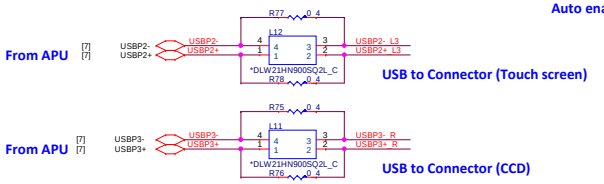


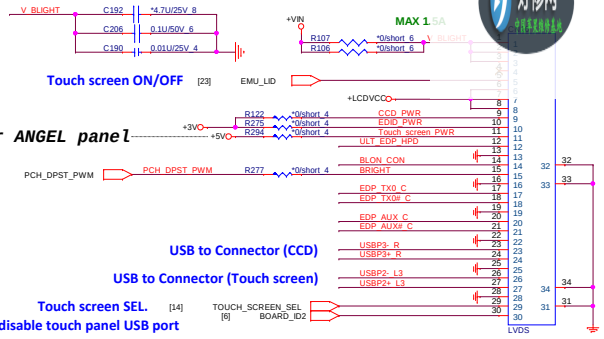




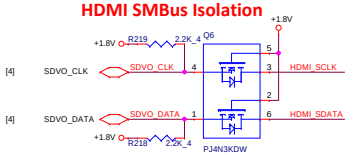


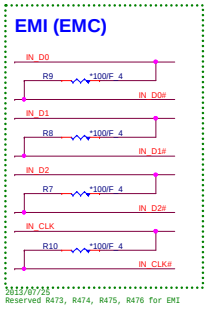


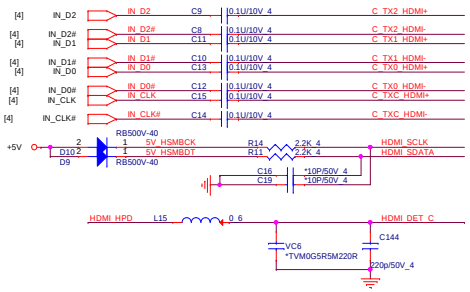


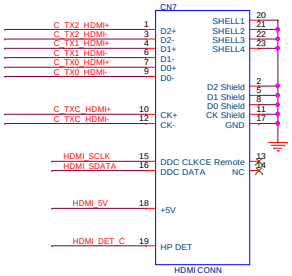


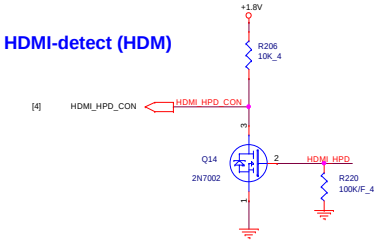
HDMI Conn.

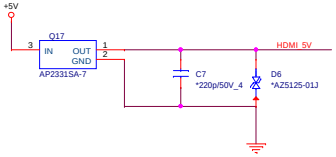


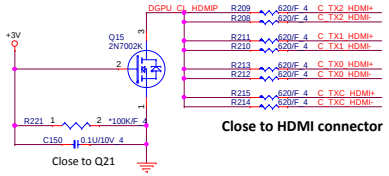








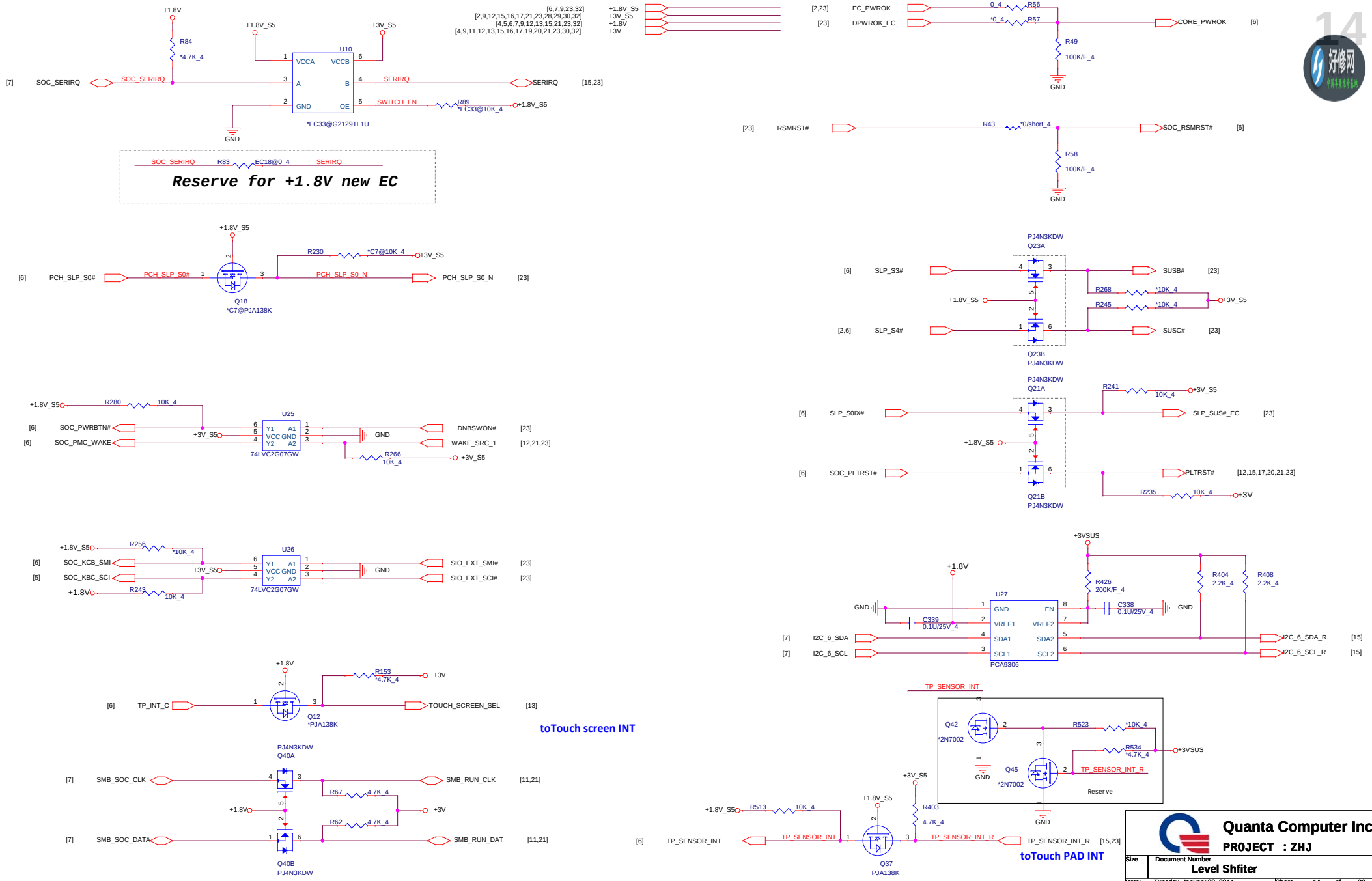




Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	LCD/HDMI/Camera	2A

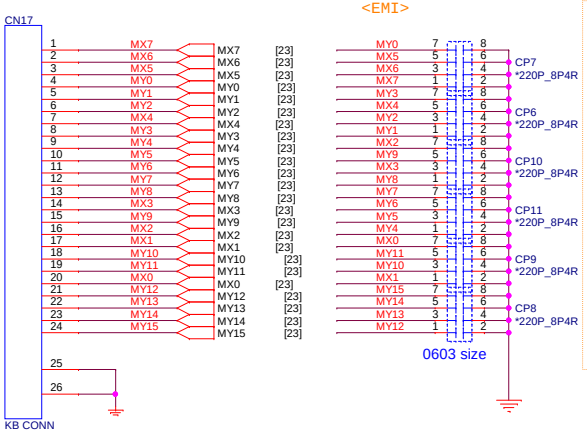
Date: Tuesday, January 28, 2014 Sheet 13 of 33


+1.8V
R84
*4.7K_4
+1.8V_S5
+3V_S5
U10
VCCA
VCCB
A
B
GND
OE
[7] SOC_SERIRQ
SOC_SERIRQ
SERIRQ
SERIRQ [15,23]
SWITCH_EN
R89
*EC33@10K_4
+1.8V_S5
*EC33@G2129TL1U
[6,7,9,23,32] +1.8V_S5
[2,9,12,15,16,17,21,23,28,29,30,32] +3V_S5
[4,5,6,7,9,12,13,15,21,23,32] +1.8V
[4,9,11,12,13,15,16,17,19,20,21,23,30,32] +3V
[2,23] EC_PWROK
[23] DPWROK_EC
0_4 R56
*0_4 R57
CORE_PWROK [6]
R49
100K/F_4
SOC_SERIRQ R83 EC18@0_4 SERIRQ
Reserve for +1.8V new EC
[23] RSMRST#
R43 *0/short_4
SOC_RSMRST# [6]
R58
100K/F_4
[6] PCH_SLP_S0#
PCH_SLP_S0#
R230 *C7@10K_4
+3V_S5
PCH_SLP_S0_N
PCH_SLP_S0_N [23]
Q18
*C7@PJA138K
PJ4N3KDW
Q23A
[6] SLP_S3#
SUSB# [23]
R268 *10K_4
R245 *10K_4
+3V_S5
[2,6] SLP_S4#
SUSC# [23]
Q23B
PJ4N3KDW
+1.8V_S5
R280 10K_4
U25
[6] SOC_PWRBTN#
[6] SOC_PMC_WAKE
+3V_S5
Y1 A1
VCC GND
Y2 A2
74LVC2G07GW
GND
DNBSWON# [23]
WAKE_SRC_1 [12,21,23]
R266 10K_4
+3V_S5
PJ4N3KDW
Q21A
[6] SLP_S0IX#
R241 10K_4
+3V_S5
SLP_SUS#_EC [23]
+1.8V_S5
[6] SOC_PLTRST#
PLTRST# [12,15,17,20,21,23]
R235 10K_4
+3V
Q21B
PJ4N3KDW
+1.8V_S5
R256 *10K_4
U26
[6] SOC_KCB_SMI
[5] SOC_KBC_SCI
+3V_S5
74LVC2G07GW
GND
SIO_EXT_SMI# [23]
SIO_EXT_SCI# [23]
+1.8V
R243 10K_4
+3VSUS
+1.8V
U27
GND
VREF1
SDA1
SCL1
EN
VREF2
SDA2
SCL2
PCA9306
C339 0.1U/25V_4
C338 0.1U/25V_4
R426 200K/F_4
R404 2.2K_4
R408 2.2K_4
[7] I2C_6_SDA
[7] I2C_6_SCL
I2C_6_SDA_R [15]
I2C_6_SCL_R [15]
+1.8V
R153 *4.7K_4
+3V
[6] TP_INT_C
TOUCH_SCREEN_SEL [13]
Q12
*PJA138K
toTouch screen INT
TP_SENSOR_INT
Q42
*2N7002
R523 *10K_4
R534 *4.7K_4
+3VSUS
Q45
*2N7002
TP_SENSOR_INT_R
Reserve
PJ4N3KDW
Q40A
[7] SMB_SOC_CLK
SMB_RUN_CLK [11,21]
R67 4.7K_4
+1.8V
+3V
R62 4.7K_4
[7] SMB_SOC_DATA
SMB_RUN_DAT [11,21]
Q40B
PJ4N3KDW
+1.8V_S5
R513 10K_4
+3V_S5
R403 4.7K_4
+1.8V_S5
[6] TP_SENSOR_INT
TP_SENSOR_INT
TP_SENSOR_INT_R
TP_SENSOR_INT_R [15,23]
Q37
PJA138K
toTouch PAD INT
Quanta Computer Inc.
PROJECT : ZHJ
Size
Document Number
Level Shfiter
Rev
2A
Date: Tuesday, January 28, 2014
Sheet 14 of 33

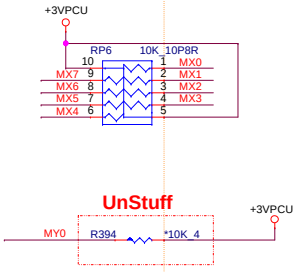
KEYBOARD (KBC)

<20110214(E1A)>
Change CP1~CP6 footprint from
8p4r-0402-smt to 8P4R, for SMT open issue.

<EMI>

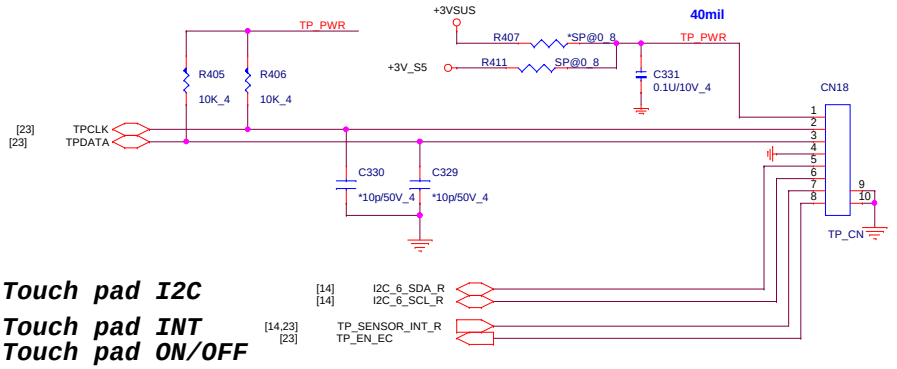


INTERNAL KEYBOARD STRIP SET (KBC)



TOUCH PAD (TPD)

note: change to +3V_S5
other level sheft need to change power rail



ACER DEFINE
VDD
PS2-CLK
PS2-DATA
GND
I2C-DATA
I2C-CLK
ATTN (INT)
SER-OFF.

Touch pad I2C
Touch pad INT
Touch pad ON/OFF

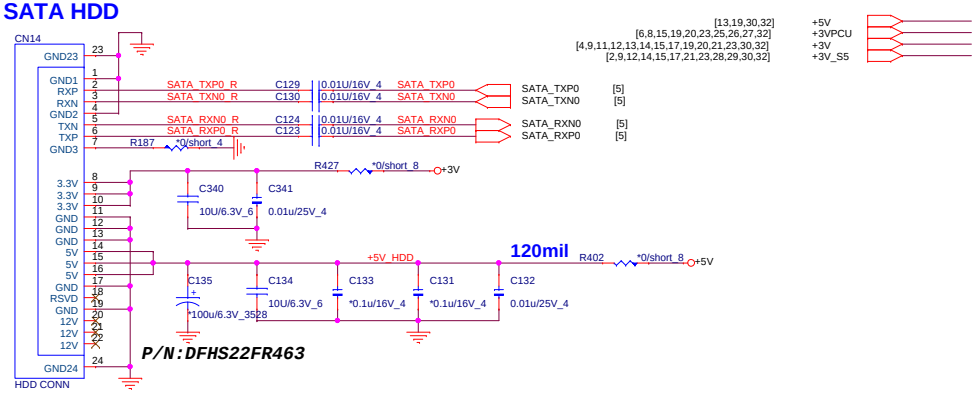
TPM (TPM)

note: serie need to add level shift

TPM_N for 新 唐
TPM_I for 英飛凌---- default

Quanta Computer Inc.			
PROJECT : ZHJ			
Size	Document Number		Rev
	KB/BT/TP		2A
Date: Tuesday, January 28, 2014		Sheet 15 of 33	

SATA HDD

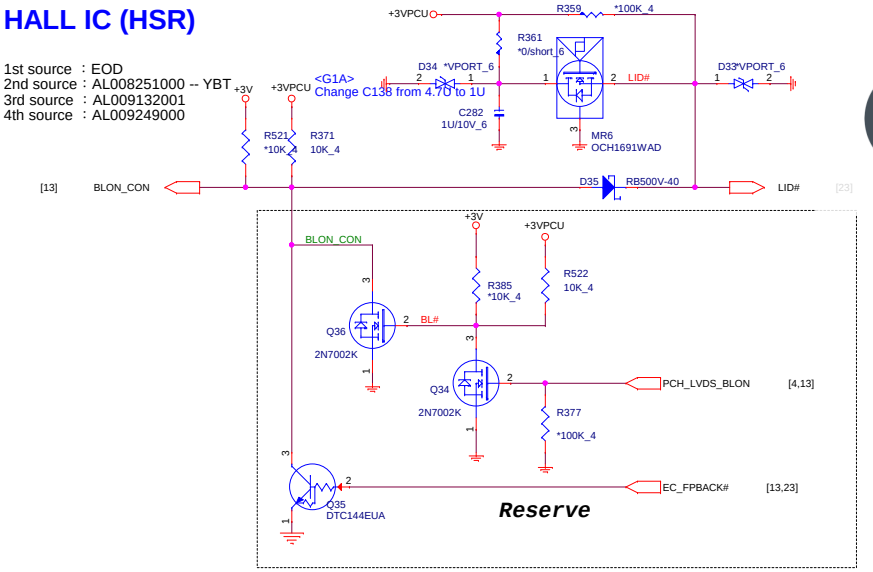


P/N:DFHS22FR463

eMMC

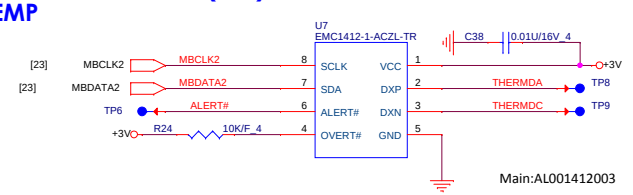
HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 -- YBT
3rd source : AL009132001
4th source : AL009249000



Reserve

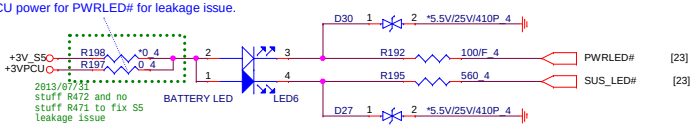
CPU Thermal sensor(THS) / MB Local TEMP



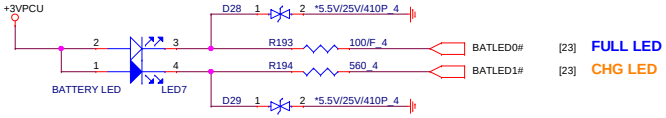
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

PWR indicator

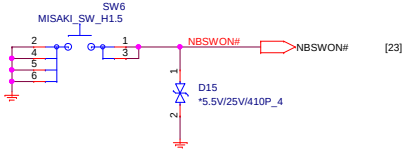
<20130722> Reserve +3VPCU power for PWRLED# for leakage issue.



Battery indicator



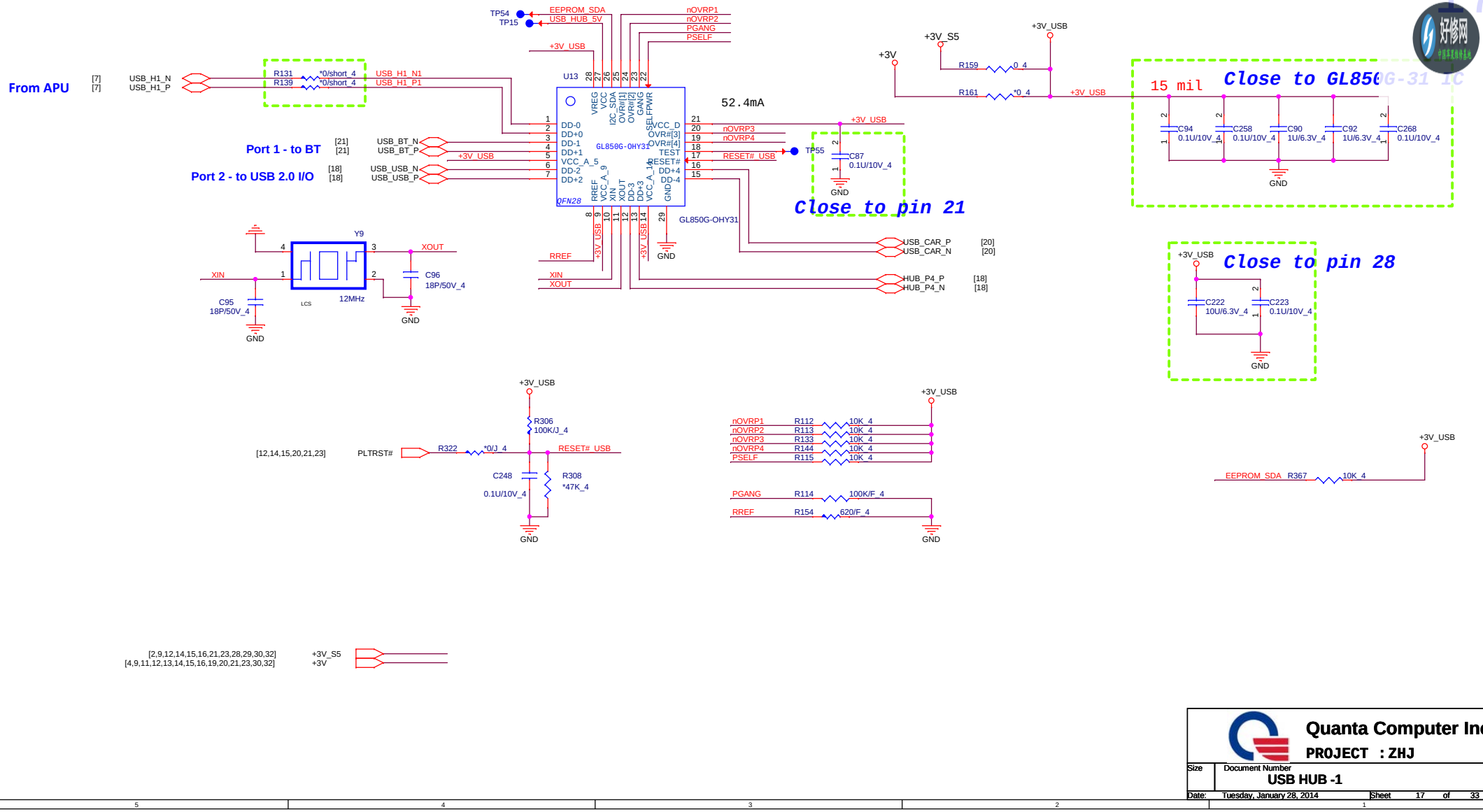
PWR button



Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	HDD/Hall/eMMC/LED	2A

Date: Tuesday, January 28, 2014 Sheet 16 of 33



Quanta Computer Inc.	
PROJECT : ZHJ	
Size	Document Number: USB HUB -1 — Rev: 1A
Date: Tuesday, January 28, 2014	Sheet 17 of 33

[6,26,28,29,30,31,32] +5V_S5

Close USB3.0

5VUSB_0 — C149 470P/50V_4 — C148 0.1U/10V_4 — C20 100U/6.3V_1206

USB2.0 connector P/N:
DFHS04FR487

CN6 USB3.0 CONN
1 VBUS
2 D-
3 D+
4 GND
5 SSRX-
6 SSRX+
7 GND
8 SSTX-
9 SSTX+

USB 3.0 Connector

From APU
[7] USBP0- → R18 0_4 → USBP0-_R
[7] USBP0+ → R17 0_4 → USBP0+_R

From APU
[7] USB30_RX1- → R12 18_4 → USB30_RX1-_R
[7] USB30_RX1+ → R13 18_4 → USB30_RX1+_R

From APU
[7] USB30_TX1- → C25 0.1U/10V_4 → USB30_TX1-_C → R19 18_4 → USB30_TX1-_R
[7] USB30_TX1+ → C26 0.1U/10V_4 → USB30_TX1+_C → R20 18_4 → USB30_TX1+_R

C17 *1.6P/50V_4 — C18 *1.6P/50V_4

From APU
[7] USB30_RX1- → USB30_RX1-
[7] USB30_RX1+ → USB30_RX1+

C23 *1.6P/50V_4 — C22 *1.6P/50V_4

USB 2.0 Connector

G547E2P81U: Enable: Low Active /2.5A — P2 - USB 2.0

+5V_S5 — C146 4.7U/10V_6 — U19 G524B2T11U (IN, OUT, GND, EN, /OC) — 2A

5VUSB_0

[23] USBON# → USBON#

[7] SOC_USB_OC0

From HUB

C21 100U/6.3V_1206 — <Layout note> Close to CONN — C145 0.1U/10V_4

USBP1-_CN
USBP1+_CN

D7 *5V/30V/0.2p_4 — D8 *5V/30V/0.2p_4

CN8 USB_CON
VDD GND5
D- GND6
D+ GND7
GND4 GND8

EMI

[17] USB_USB_N → USB_USB_N → L7 → USBP1-_CN
[17] USB_USB_P → USB_USB_P → L7 → USBP1+_CN

L7 EMI@MCM2012B900GBE/400mA/90ohm

G547E2P81U: Enable: Low Active /2.5A — P4 - USB 2.0

+5V_S5 — C93 4.7U/10V_6 — U14 G524B2T11U (IN, OUT, GND, EN, /OC) — 2A

5VUSB_1

USBON#

[7] SOC_USB_OC1 → SOC_USB_OC1

From HUB

C100 100U/6.3V_1206 — <Layout note> Close to CONN — C88 0.1U/10V_4

USBP4-_CN
USBP4+_CN

D23 *5V/30V/0.2p_4 — D22 *5V/30V/0.2p_4

CN12 USB_CON
VDD GND5
D- GND6
D+ GND7
GND4 GND8

USB 2.0 Connector

change P/N, footprint OK

EMI

[17] HUB_P4_N → HUB_P4_N → L16 → USBP4-_CN
[17] HUB_P4_P → HUB_P4_P → L16 → USBP4+_CN

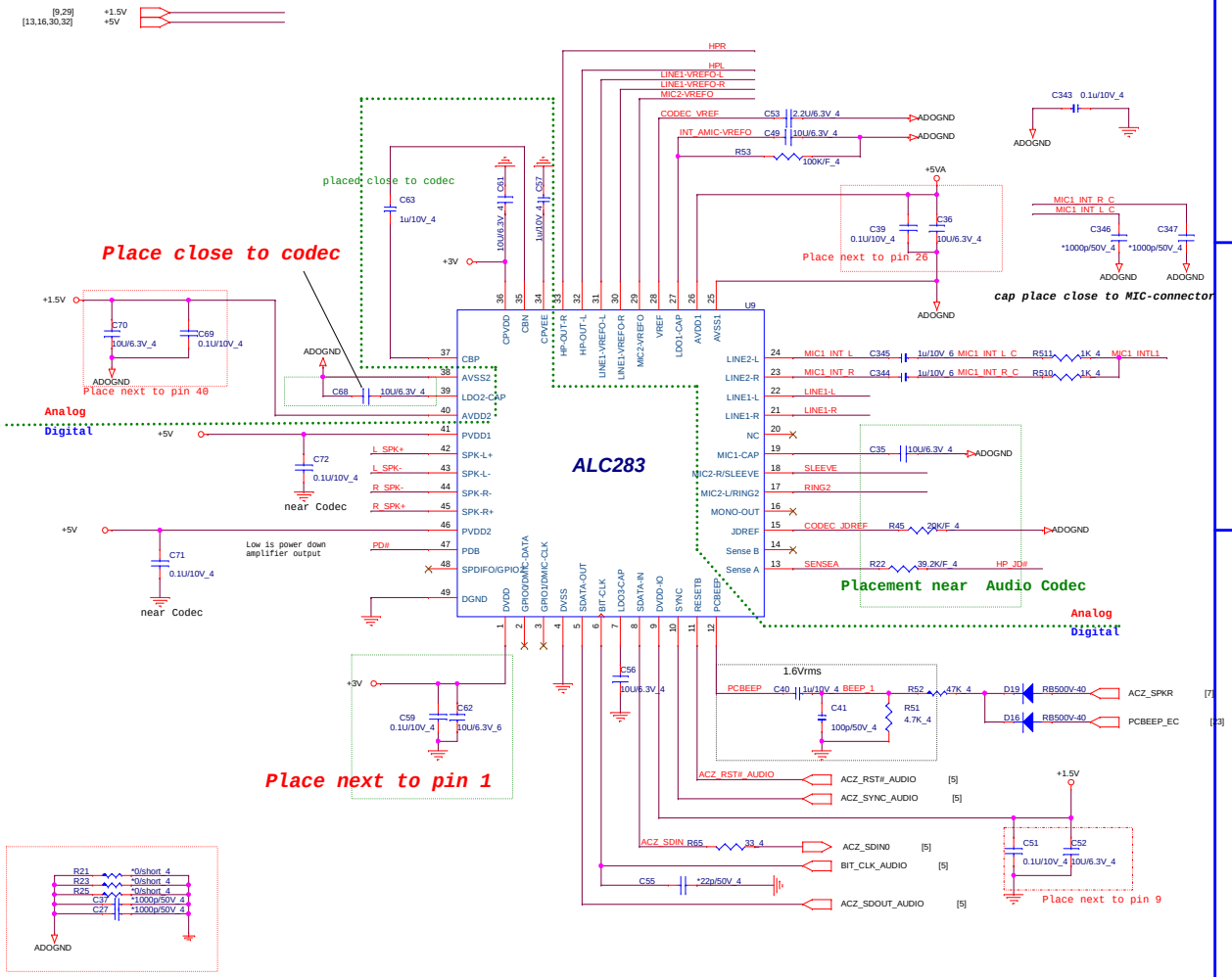
L16 EMI@MCM2012B900GBE/400mA/90ohm

Quanta Computer Inc.
PROJECT : ZHJ

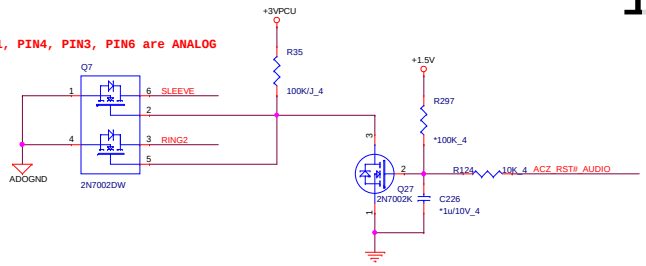
Size	Document Number	Rev
	USB / eMMC CONN	1A

Date: Tuesday, January 28, 2014 Sheet 18 of 33

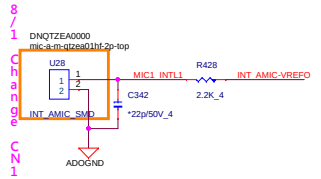
Codec(ADO)

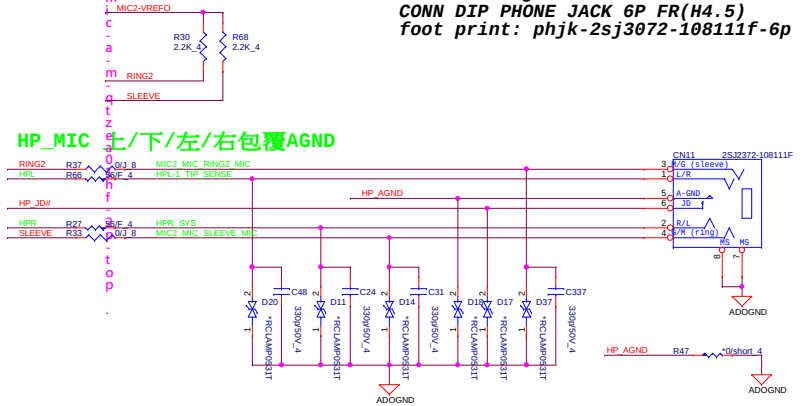


Grounding circuit(ADO)

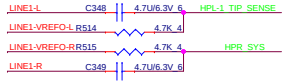


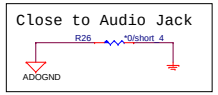
INT MIC array





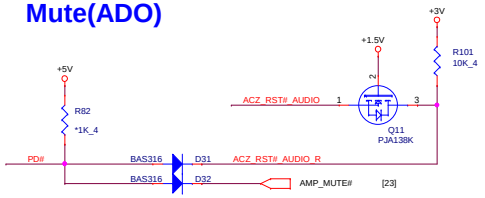
note : change next P/N: DFTJ06FR653
CONN DIP PHONE JACK 6P FR(H4.5)
foot print: phjk-2sj3072-108111f-6p



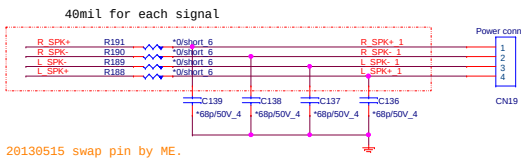


Codec PWR 5V(ADO)

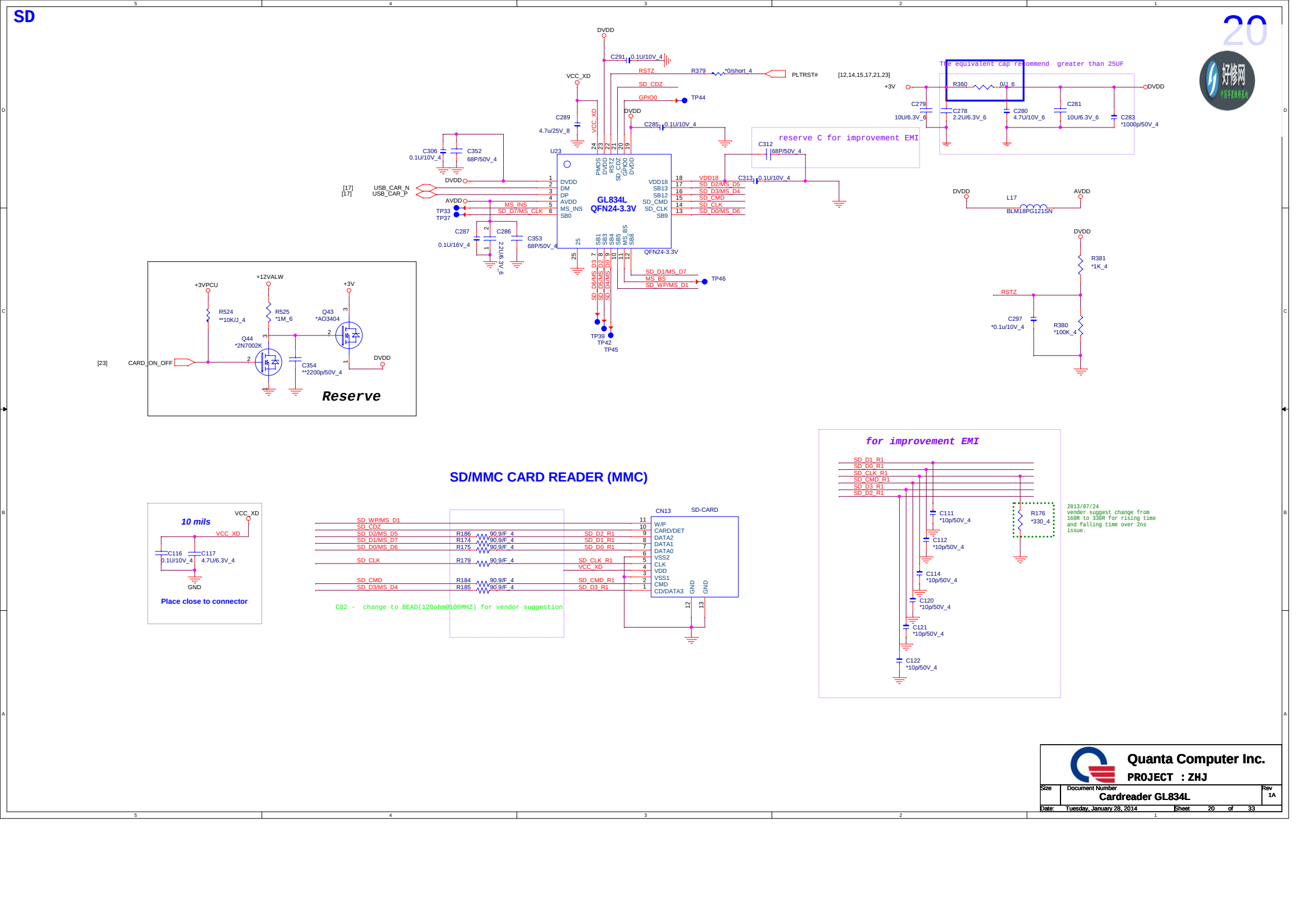
Mute(ADO)



Internal Speaker

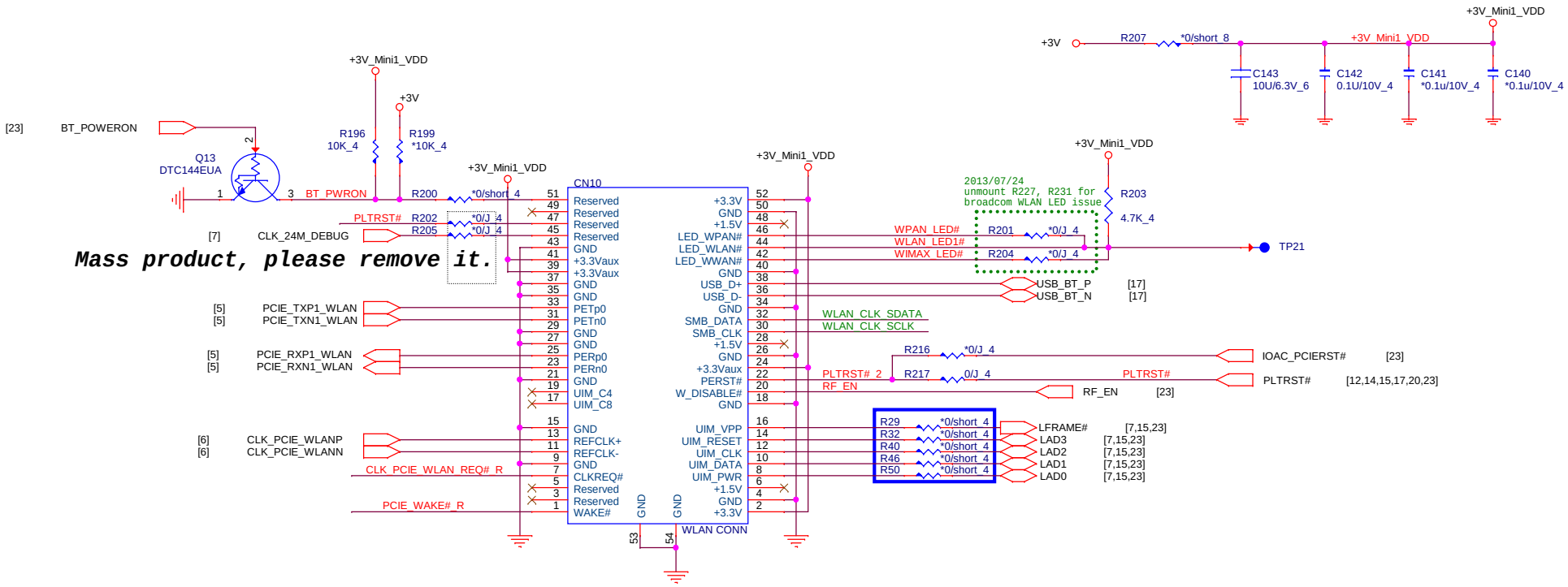


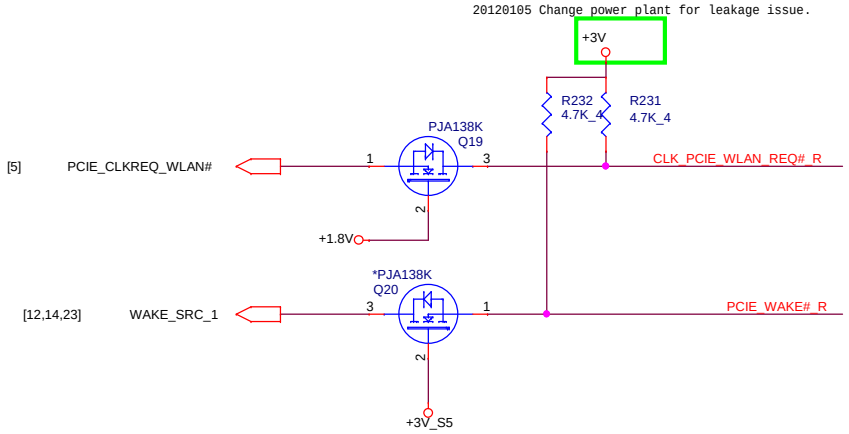
Quanta Computer Inc.			
PROJECT : ZHJ			
Size	Document Number		Rev
	ALC283/HP/SPK		2A
Date: Tuesday, January 28, 2014	Sheet 19	of 33	



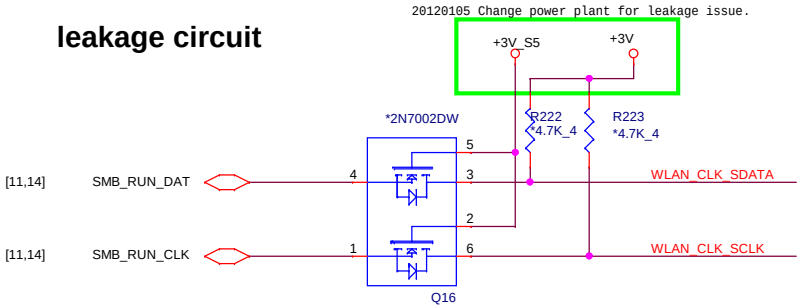
Quanta Computer Inc.	
PROJECT : ZHJ	
Size	Document Number: Cardreader GL834L — Rev: 1A
Date: Tuesday, January 28, 2014	Sheet 20 of 33

WLAN





leakage circuit



[4,5,6,7,9,12,13,14,15,23,32]	+1.8V
[4,9,11,12,13,14,15,16,17,19,20,23,30,32]	+3V
[2,9,12,14,15,16,17,23,28,29,30,32]	+3V_S5

Quanta Computer Inc.
PROJECT : ZHJ

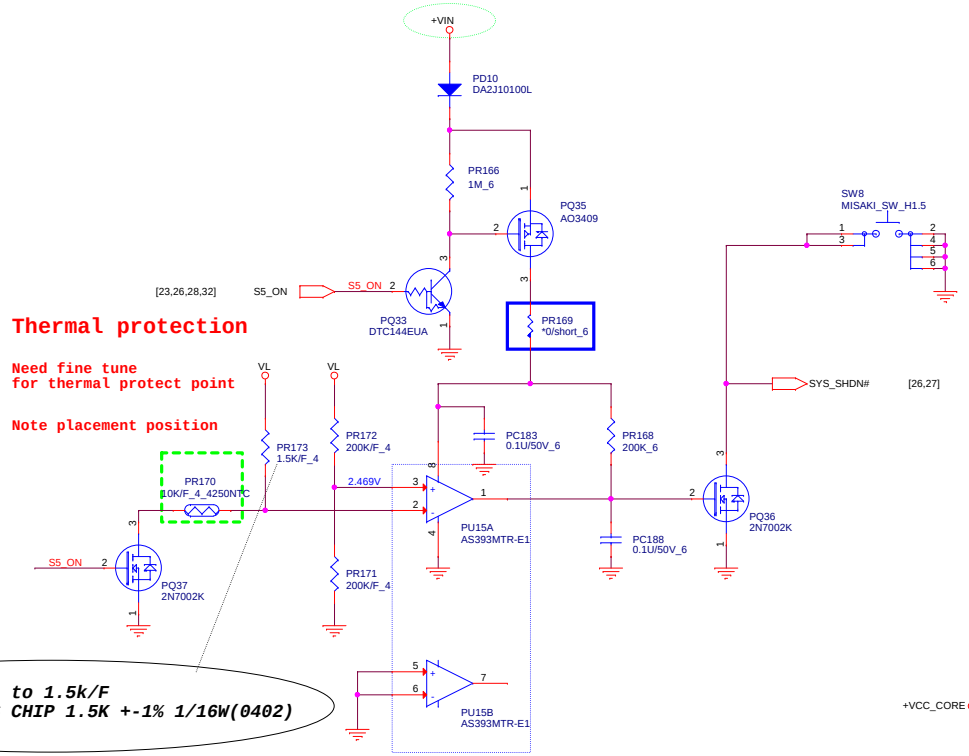
Size	Document Number	Rev
	WiFi & BT	1A
Date: Tuesday, January 28, 2014	Sheet 21 of 33	

HG-TC256BC354D118P2

Thermal protection

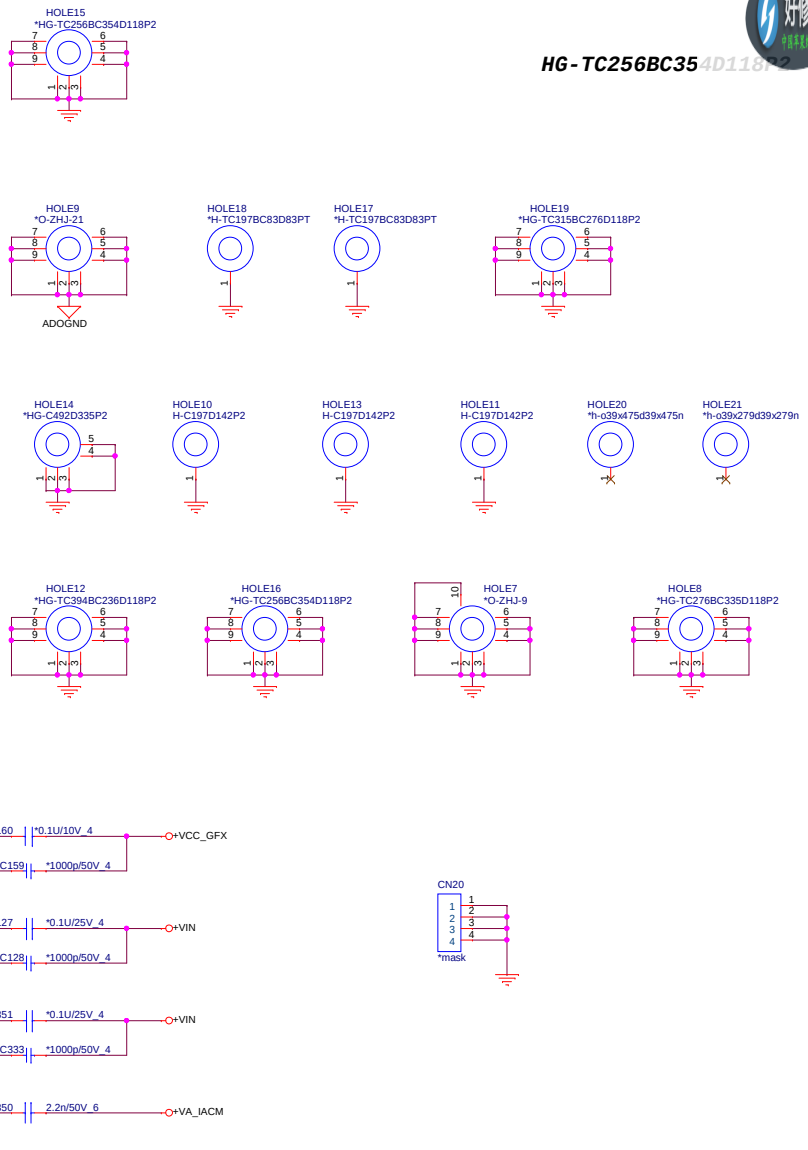
Need fine tune for thermal protect point

Note placement position



note: PR173 change to 1.5k/F
CS21502FB14 RES CHIP 1.5K +-1% 1/16W(0402)

For EC control thermal protection (output 3.3V)



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: Thermal / Hole	Rev: 2A
Date: Tuesday, January 28, 2014	Sheet 22 of 33	

1.8V p/n: AJ009850F02
Discription:IC CONTROLLER(128P)NPCE985LB1DX(LQFP)

note:
GPIO75 EMU_LIDTouch panel enable/disable#Follow ZEA -->ZHJ None
GPIO70 TP_EN_ECTouch pad enable/disable# -->ok
GPIO27 TP_INT_EC#Touch pad interrupt

EC(KBC)

985L-A0 connects to +3v / 985L-B1 connects to +1.8v

note:change EC p/n: into AJ009850F02

30mil

0.03A(30mils)

220121130 change to 39p capacitor for ESD

985L-A0 connects to +3vpcu / 985L-B1 connects to +1.8v_s5

LPC: LFRAME# LAD0 LAD1 LAD2 LAD3 LCLK CLK_24M_KBC CLKRUN# SIO_A20GATE SIO_RCIN# SIO_EXT_SCI# SIO_EXT_SMI# SERIRQ PLTRST# IOAC_PCIERST# AMP_MUTE#

A/D: GPIO90/AD0 GPIO91/AD1 GPIO92/AD2 GPIO93/AD3

D/A: GPIO94/DA0 GPI95/DA1 GPI96/DA2

GPIO: GPIO01/TB2 GPIO02 GPIO03 GPIO04 GPIO05 GPIO06/IOX_DOUT/RTS1 GPIO07 GPIO16 GPIO30 GPIO36/CTS1 GPIO41 GPIO42/SCL3B/TCK GPIO43/SDA3B/TMS GPIO44/TDI GPO47/SCL4 GPIO50/PSCLK3/TDO GPIO51 GPIO52/PSDAT3/RDY GPIO53/SDA4 GPIO70 GPIO71 GPIO72 GPIO75/SPI_SCK GPO76/SHBM GPIO77 GPIO81 GPO82/IOX_LDSH/TEST GPO84/IOX_SCLK/XORTR GPIO97

KB: KBSIN0 KBSIN1 KBSIN2 KBSIN3 KBSIN4 KBSIN5 KBSIN6 KBSIN7 KBSOUT0/JENK KBSOUT1/TCK KBSOUT2/TMS KBSOUT3/TDI KBSOUT4/JEN0 KBSOUT5/TDO KBSOUT6/RDY KBSOUT7 KBSOUT8 KBSOUT9/SDP_VIS KBSOUT10/P80_CLK KBSOUT11/P80_DAT KBSOUT12/GPIO64 KBSOUT13/GPIO63 KBSOUT14/GPIO62 KBSOUT15/GPIO61/XOR_OUT GPIO60/KBSOUT16 GPIO57/KBSOUT17

TIMER: GPIO56/TA1 GPIO20/TA2/IOX_DIN_DIO GPIO14/TB1 GPIO15/A_PWM GPIO21/B_PWM GPIO13/C_PWM GPIO32/D_PWM GPIO45/E_PWM GPIO40/F_PWM/RI1 GPIO66/G_PWM GPIO33/H_PWM/SOUT1

SMB: GPIO17/SCL1 GPIO22/SDA1 GPIO73/SCL2 GPIO74/SDA2 GPIO23/SCL3 GPIO31/SDA3

IR: GPIO87/CIRRXM/SIN_CR GPIO34/SIN1/CIRRXL GPIO46/CIRRXM/TRST GPO83/SOUT_CR/TRIST

PS/2: GPIO37/PSCLK1 GPIO35/PSDAT1 GPIO26/PSCLK2 GPIO27/PSDAT2 GPIO00/32KCLKIN

FIU: F_SDI/F_SDIO1 F_SDO/F_SDIO0 F_CS0 F_SCK GPIO55/CLKOUT/IOX_DIN_DIO

VCC_POR VREF VTT PECI

NPCE985LA0DX

note: gpio27 -->TOUCH_PAD_INT

Reserve for writing ME ROM

PECI interface should be used on Bay Trail platform, thus VTT pin can wire to GND and PECI signal can be left un-connected.

prevent leakage : EC internal pull high

Q41 2N7002K

Note: GPIO75 (pin82) for TOUCHPANEL_ON

pin91 in 985L is 1.8V only

For test

<20090721_FAE suggestion> Stuff 100K and close to EC side for improving power consumption

20111129 add 33ohm series resistor and for EC FAE suggestion contact to SPI 4M ROM and close to Flash.

Reserve R477, R478 for EC chip PU function issue.

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU

SM BUS PU(KBC)

SPI NOR FLASH

25mA

U15 soic8-6-1_27-pm25lv010a AKE35ZN0N00 IC FLASH(8P) W25X10CLSNIG(SOIC)

985L-A0 connects to +3vPCU / 985L-B1 connects to +1.8v_s5

HWPG(KBC)

<20130722>Change power from +3V to +3V_S5 for power sequence issue

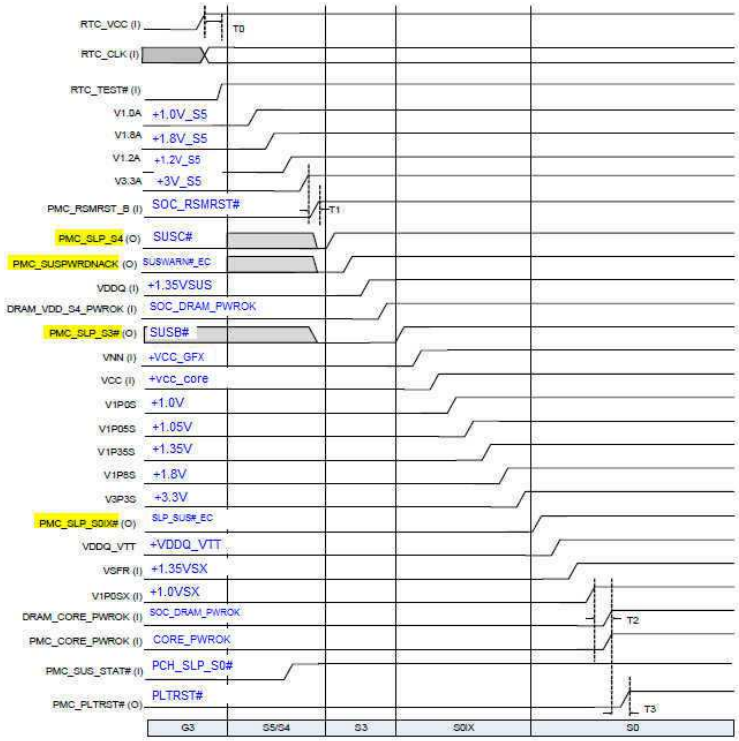
Q33 2N7002K

Q47 need Replacement at BOT layer.

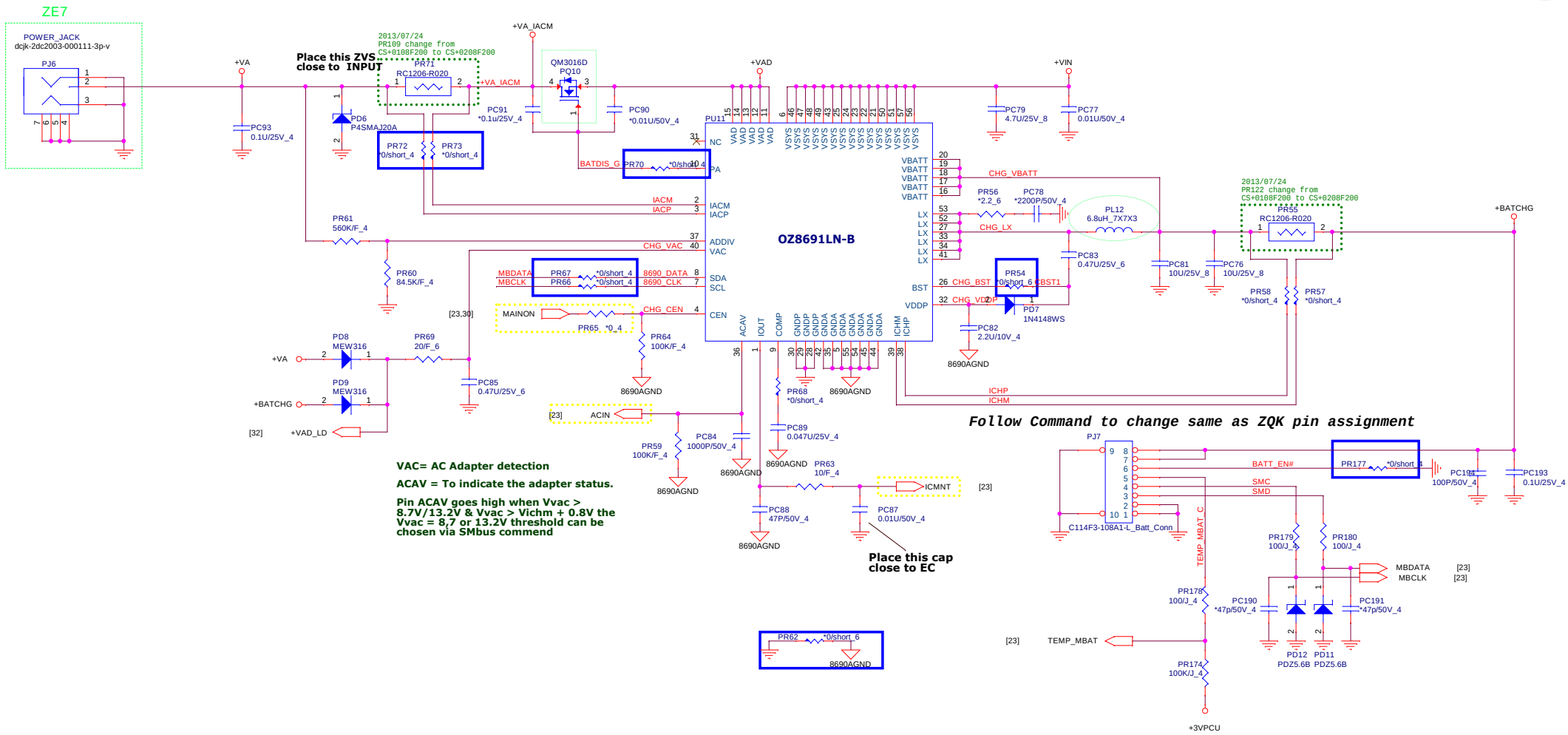
20120217 Change R630 from10k to 47k for S5 current reduc...

Quanta Computer Inc.	
PROJECT : ZHJ	
Size	Document Number: NPCE885/FLASH — Rev 2A
Date: Tuesday, January 28, 2014	Sheet 23 of 33

Bay Trail-M S4/S5 to S0 (Power Up) Sequence



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: Power sequence	Rev: 1A
Date: Tuesday, January 28, 2014	Sheet 24 of 33	



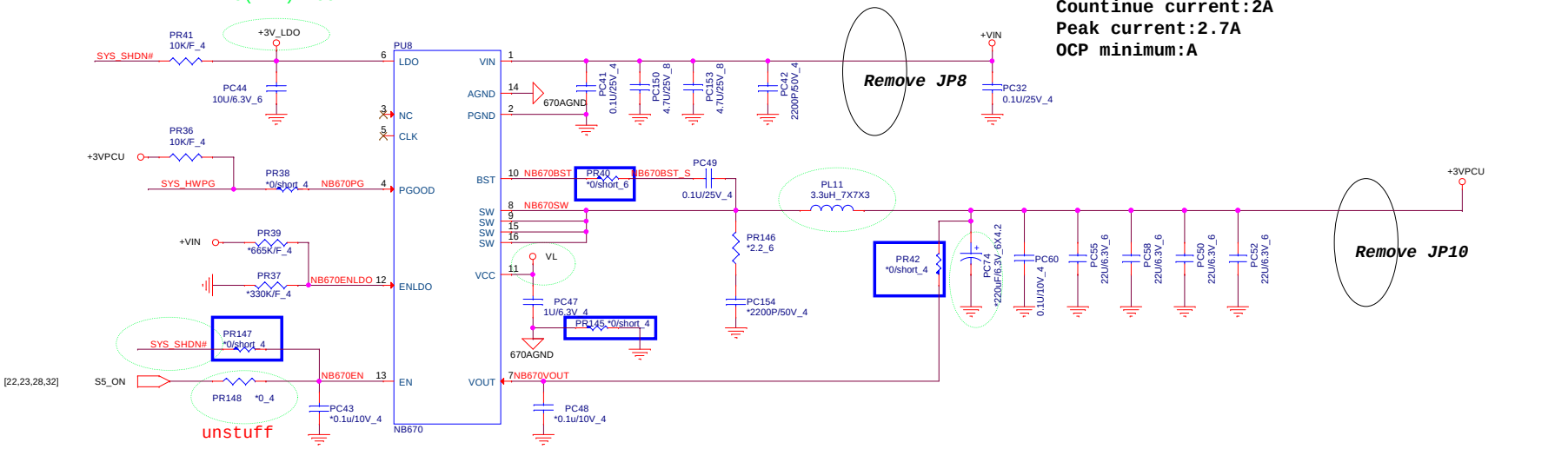
Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: Charger (OZ8690ALN)	Rev: 1A
Date: Tuesday, January 28, 2014	Sheet 25 of 33	

DC/DC +3VPCU/+5V_S5

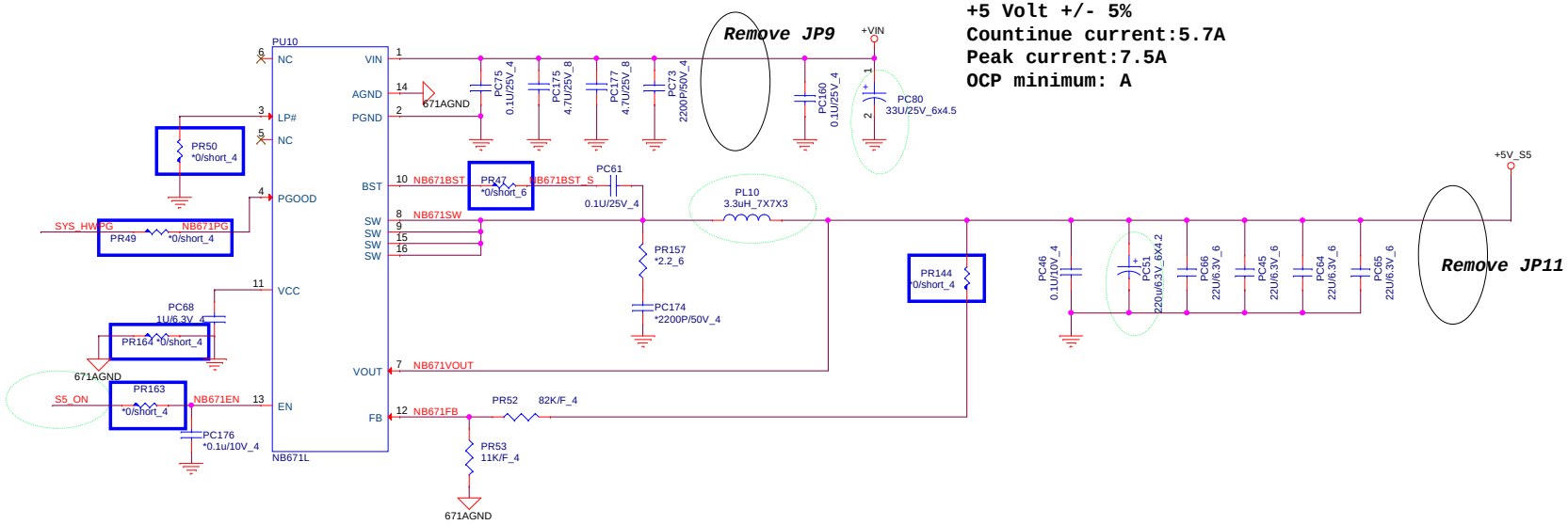
+3VPCU [6,8,15,16,19,20,23,25,27,32]
+5V_S5 [6,18,28,29,30,31,32]
SYS_SHDN# [22,27]

LDO(MAX)=100mA

+3.3 Volt +/- 5%
Countinue current:2A
Peak current:2.7A
OCP minimum:A



+5 Volt +/- 5%
Countinue current:5.7A
Peak current:7.5A
OCP minimum: A



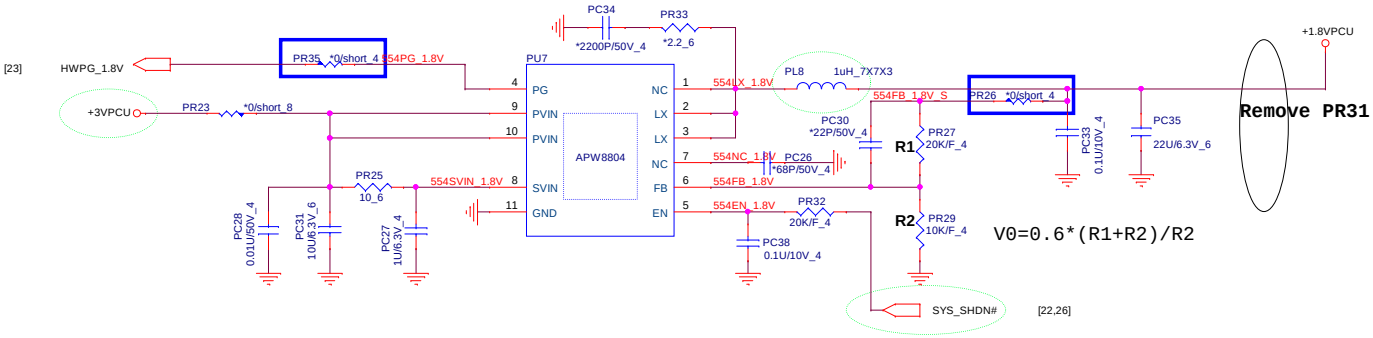
Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	3/5VS5 (NB670/NB669)	1A
Date: Tuesday, January 28, 2014	Sheet 26 of 33	

[32] +1.8VPCU

[6,8,15,16,19,20,23,25,26,32] +3VPCU

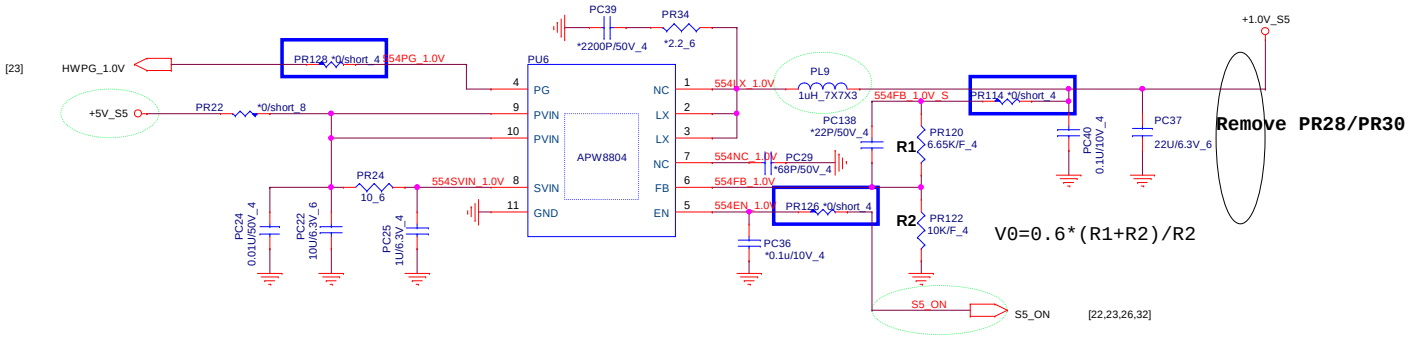
+1.8V Volt +/- 5%
Countinue current:0.08A
Peak current:0.11A
OCP minimum:A



Quanta Computer Inc. PROJECT : ZHJ			
Size	Document Number +1.8VPCU		Rev 1A
Date: Tuesday, January 28, 2014		Sheet 27 of 33	

[9,32] +1.0V_S5
[6,18,26,29,30,31,32] +5V_S5
[2,9,12,14,15,16,17,21,23,29,30,32] +3V_S5

+1.0V Volt +/- 5%
Countinue current:2.4A
Peak current:3.2A
OCP minimum:A



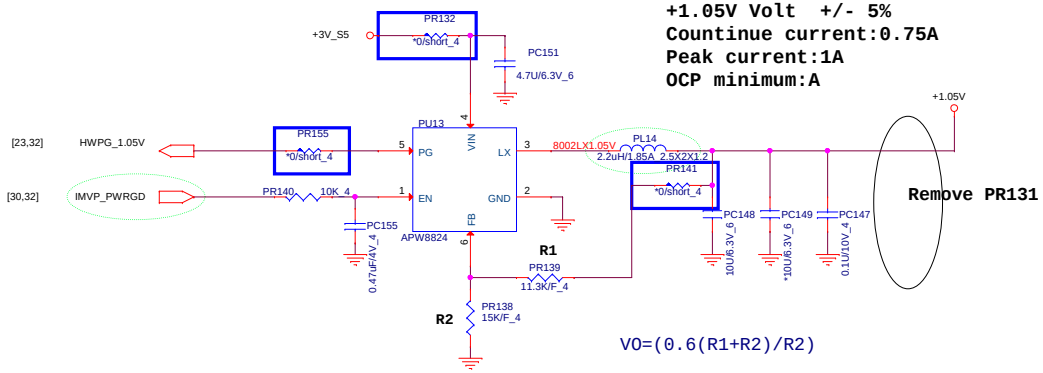
Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	+1.0V	1A
Date: Tuesday, January 28, 2014	Sheet 28 of 33	

[2,9,12,14,15,16,17,21,23,28,30,32] +3V_S5

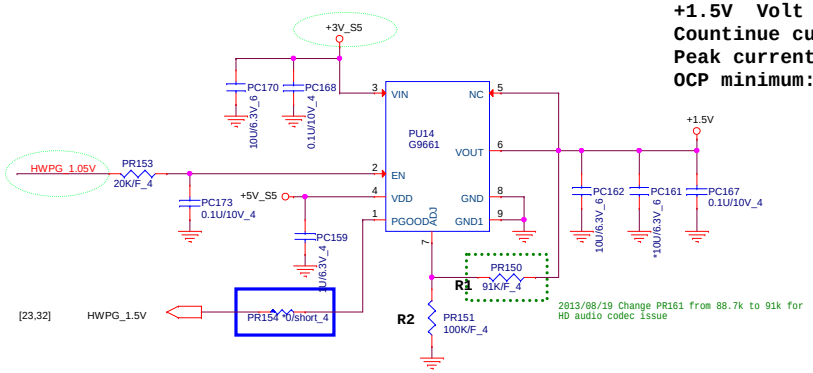
[9] +1.05V

[9,19] +1.5V



+1.05V Volt +/- 5%
Countinue current:0.75A
Peak current:1A
OCP minimum:A

VO=(0.6(R1+R2)/R2)



+1.5V Volt +/- 5%
Countinue current:0.023A
Peak current:0.03A
OCP minimum:A

VO=(0.8(R1+R2)/R2)
R2<120Kohm

Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	+1.05V/1.5V	1A
Date: Tuesday, January 28, 2014	Sheet 29 of 33	

20130617 Change +1.05V to +1.0V

Close to VR

VR_SVID_ALERT# close to CPU

VR_SVID_DATA and VR_SVID_CLK close to VR

[5,6,9,32] +1.0V
[8,9,22] +VCC_GFX
[13,22,25,26,31,32] +VIN
[6,18,26,28,29,31,32] +5V_S5

Parallel

Close to the CPU side.

PU12 ISL95833HRTZ-T

AXG

Remove JP6

DCR=4.2mOhm

+VCC_GFX
TDC : A
PEAK : 14A
OCP : A
Width : mil

GFX_CORE Load Line : -5.9mV/A for 2.xW SDP

Close to the VR side.

Close with AXG inductor

Core

Remove JP7

DCR=4.2mOhm

+VCC_CORE
TDC : A
PEAK : 12A
OCP : A
Width : mil

delete PC11

VCORE Load Line : -5.9mV/A for 2.xW SDP

Close to the VR side.

Close with phase1 inductor

Parallel

Close to the CPU side.

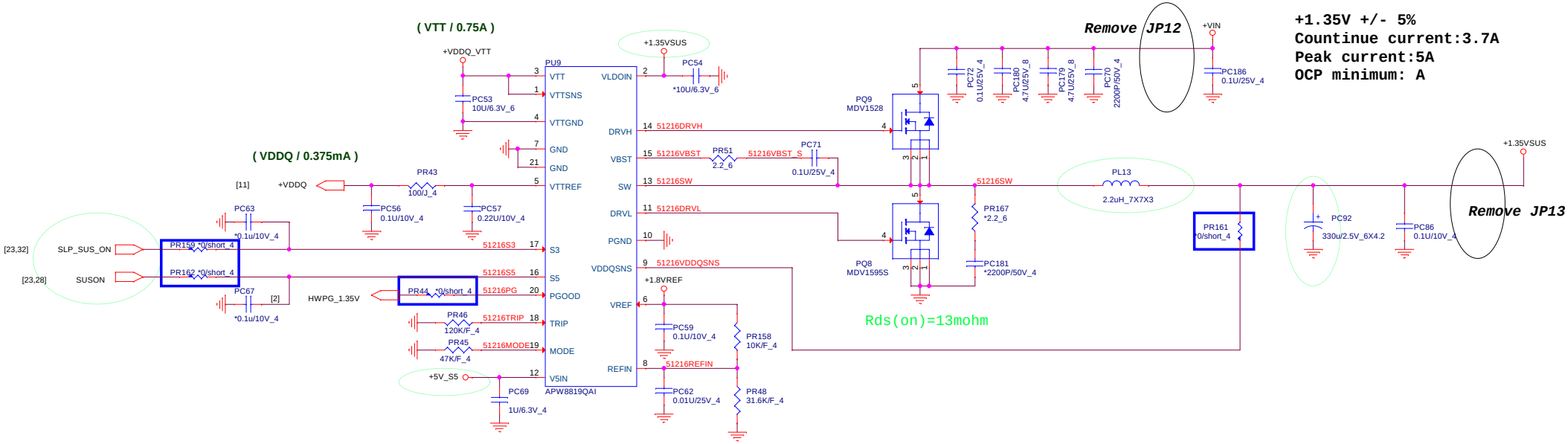
Quanta Computer Inc.
PROJECT : ZHJ

Size | Document Number: +VCC_CORE/+VGFX (ISL95833) | Rev 2A
Date: Tuesday, January 28, 2014 | Sheet 30 of 33

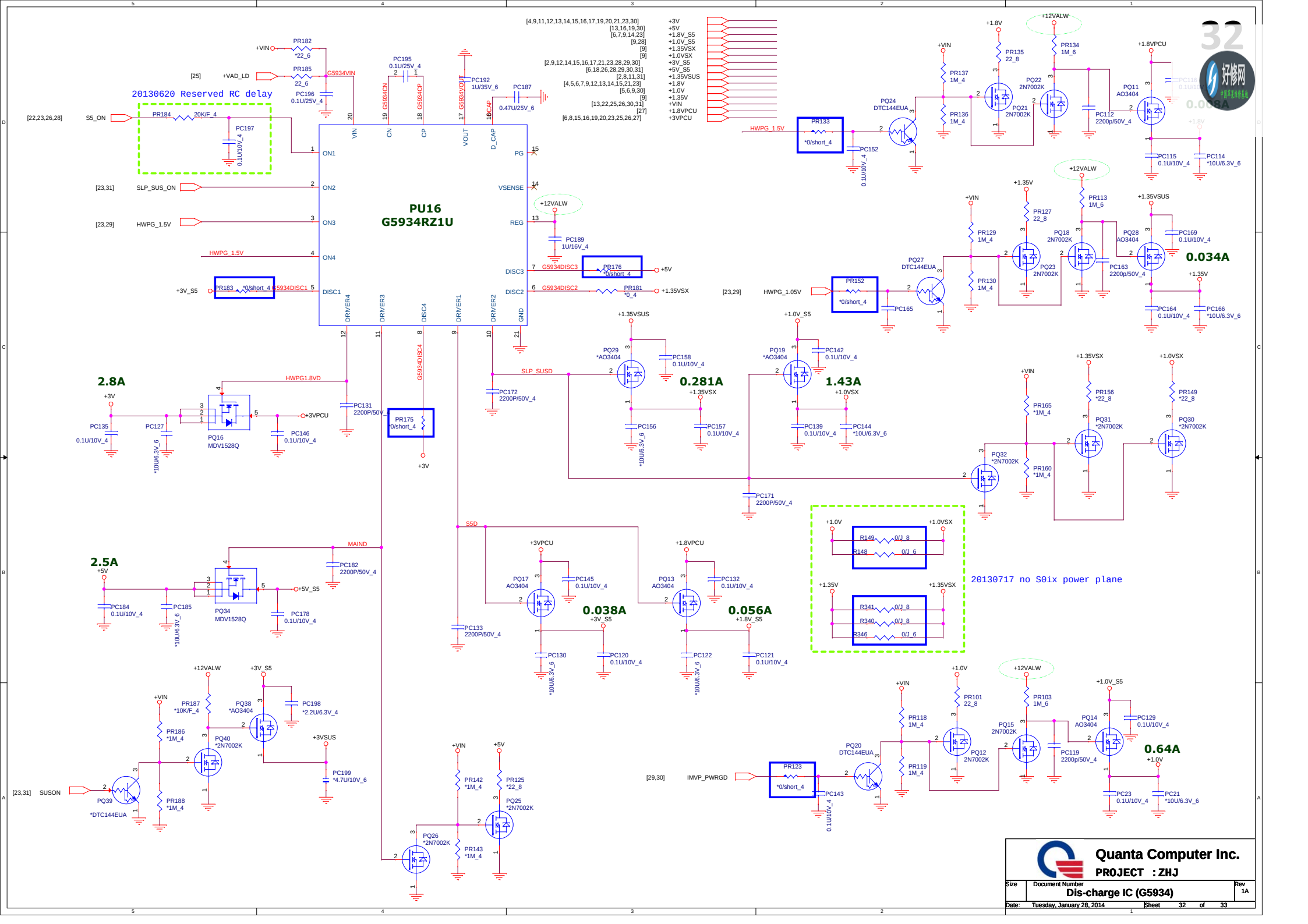
[2,8,11,32] +1.35VSUS

[11] +VDDQ_VTT

[6,18,26,28,29,30,32] +5V_S5



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: DDR3 (APW8819)	Rev: 1A
Date: Tuesday, January 28, 2014	Sheet 31 of 33	


PU16
G5934RZ1U
20130620 Reserved RC delay
20130717 no S0ix power plane
2.8A
2.5A
0.281A
1.43A
0.038A
0.056A
0.034A
0.64A
Quanta Computer Inc.
PROJECT : ZHJ
Dis-charge IC (G5934)
Tuesday, January 28, 2014
Sheet 32 of 33

B stage:

1. Page4 ,SWAP DDI0 DDI1 port
2. Page5 , Delete NGFF function , C517,C516,C272,C275,R234,R233
3. Page6 , Mount R310,R311,R353,R354 for 1.8V EC
4. Page7 , Change R118 & R119 value form *2.2K to *560K (NC)
5. Page8 , Delete C60
6. Page12 , Change CN9 (LAN) of P/N; Add R516 ; Off*R298, *Q25
7. Page13 , Add toutch sreen ON/OFF net " EMU_LID" to CN16
8. Page14 ,Change power for TP wakeup function, mount R58,Delete Q9,Q10 Add Q40 for 0C issue.
   Delete Q26,Q22,Q38; Add U25, U26, U27 C339, C338, R426; chamge R404 & R408 value to 560 Ohm ;
   mount R266; remove R256; Add R513 for TP-int.
   not mount R89,U10,mount R83 for 1.8V of EC
9. Page15 , Change power rial , change/add *R172 (0 Ohm) of value, Add U24 & R419; Delete R410,R409 short pad; remove R407, Add R411
10. Page16 , Add C340, C341 & R427 for NGFF/SSD
11. Page19 , Change CN11(Audio) of P/N & footprint ; Add D37 & C337 ; delete R34,R28,U6,D12,D13,C6,C30,C34;
    Change R27,R66 value; Add U28,R428,R511,R510,R514,R515,C342,C344,C345,C348,C349.
12. Page22 ,Remove SW7, change PR173 of value
13. Page23 , Change EC of P/N; add R420 for TP_INT to EC ; Cgange R391 value from 47K to 4.7K
    Add Q41 prevent leakage (EC internal pull high); mount R395,R370 for EC
    not mount R167,R169,R170,R168,R355,R366,U15 for 1.8V of EC
    mount C284, R165,R357,R350,R351,R356,R364 for 1.8V of EC
14. Page30 ,Rmove PC11 for RF request

C stage:

Change 0 hm to short pad : PR100,PR105,PR110,PR132,PR177,PR22,PR23,PR78,PR97,R106,R107
R107,R122,R130,R131,R134,R139,R173,R188,R189,R190,R191,R200,R207
R229,R238,R240,R244,R257,R275,R281,R282,R283,R288,R290,R294,R309
R313,R315,R316,R321,R325,R331,R332,R333,R335,R36,R361,R372,R373
R375,R379,R390,R400,R402,R427,R43

1. Page5 , Mount R286
2. Page6 , Mount R41, Delete *R64
3. Page13 , Remove R86,R87,R69,R72,D21,C75 for LDC BLON
4. Page16 , chage R371 power rail to 3VPCU, remove *R385 & add R522 ; Mount Q34,Q35,Q36, R385,R377 for LDC BLON
5. Page17 , Remove R369
6. Page19 , R66,R27 change P/N from 47 to 56 Ohm; change R37 & R33 footprint from 0402 to 0805
7. Page20 , C312 chage to 68P, Add C352, C286 68P; change R184,R185,R186,R174,R175,R179 to 91 Ohm for vendor suggestion
8. Page26 , Remove JP8,JP9,JP10,JP11
9. Page27 , Remove PR31
10. Page28 , Remove PR28,PR30
11. Page29 , Remove PR131
12. Page30 , Remove JP6,JP7
13. Page26 , Remove JP12,JP13
14. Page21 , Remove Q20

D stage:

1. Page4 ,change R31 & R300 to 200K
2. Page6 ,change CLK port0 to port2 ; change D36 footprint change P/N
3. Page13 ,Remove R111
4. Page14 ,Add *R523,*R534,*Q42 & *Q45 for +3vsus ;
   Q12 gate change to 1.8V ; Remove R153 & Q12
5. Page15 , Change R407 power reail to +3vsus; Delete R177; TPM co-layout
6. Page16 , change R192,R193 from 33 to 100 Ohm; R194,R195 from 220 to 560 Ohm; Remove R377
7. Page17 , Delete *U17,*R363,*R369,*C113, chage R154 of value
8. Page18 , Delete L6,L8,L9, R16,R15,mount L7 ; Delete 320, R324, mount L16 for EMI; Change R12,R13,R19,R20 of value from 0 to 18 Ohm
9. Page20 , not mount C111,C112,C114,C120,C121,C122 & R176,Add R360
   Reserve *R524,*R525,*Q43,*Q44,*C354 for card reader on/off; Swap CN13 Pin10 & Pin11 net name
10. Page22 , Mount C350 for EMI request
11. Page30 , Change PU12 footprin; Add *PR186,*PR187,*PR188,*PC198,*PC199,*PQ38,*PQ39,*PQ40.

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PROJECT : ZHJ		
Size	Document Number: Change note	Rev 1A
Date: Tuesday, January 28, 2014	Sheet 33 of 33	