

# EA40\_BM

## Schematics Document

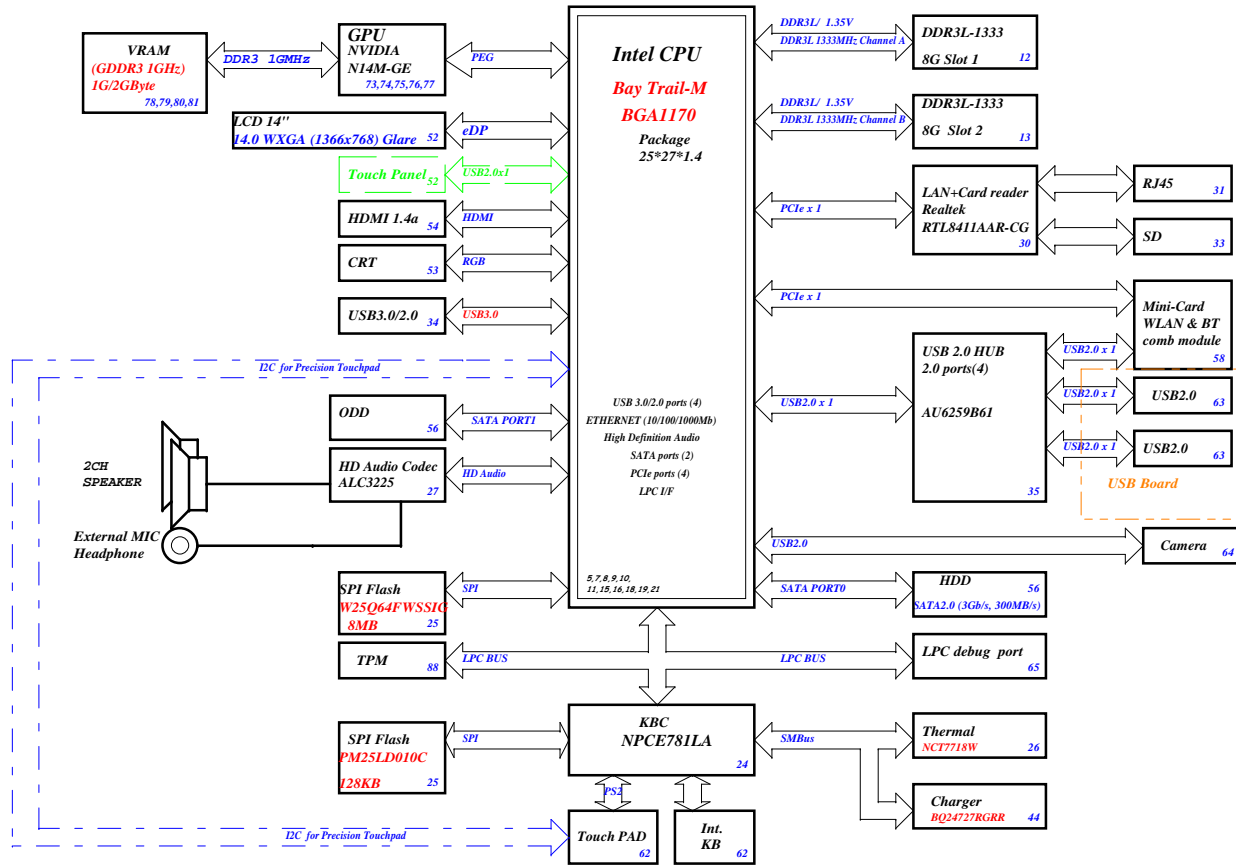
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# EA40\_BM Board Block Diagram

Project code : 91.40C01.001  
 PCB P/N : 13233  
 Revision : -1



<b>CHARGER</b>	
BQ24727	44
INPUTS	OUTPUTS
DCBATOUT	BT+
<b>SYSTEM DC/DC</b>	
TPS51225	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5
	3D3V_S5
<b>CPU DC/DC</b>	
ISL95833	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
<b>SYSTEM DC/DC</b>	
SY8208	50
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
<b>SYSTEM DC/DC</b>	
SY8208DQNC	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
<b>SYSTEM LDO</b>	
TLV70218	51
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5
	1D8V_S5
<b>SYSTEM LDO</b>	
S-1339D15	51
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5
	1D5V_S0
<b>SYSTEM LDO</b>	
TLV70012	51
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5
	1D2V_S5
<b>Step Down Regulator</b>	
SYW232	51
INPUTS	OUTPUTS
DCBATOUT	1D0V_S0_P6
	1D05V_S0
<b>GPU Core</b>	
RT8812	82
INPUTS	OUTPUTS
DCBATOUT	V6A_CORE
<b>LOAD SWITCH</b>	
TPS22966	37
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
	1D35V_S0
<b>LOAD SWITCH</b>	
TPS22965	37
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
	1D0V_S0
<b>SYSTEM DC/DC</b>	
SY8208	83
INPUTS	OUTPUTS
DCBATOUT	1D5V_V6A_S0
<b>LOAD SWITCH</b>	
TPS22966	83
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
	1D5V_V6A_S1
	3D3V_V6A_S0

<b>PCB LAYER</b>	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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File: **Block Diagram** Rev: **-1**  
 Doc: **EA40\_BM**  
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C

B

A

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5  
4 3 2 1  
**SSID = CPU**

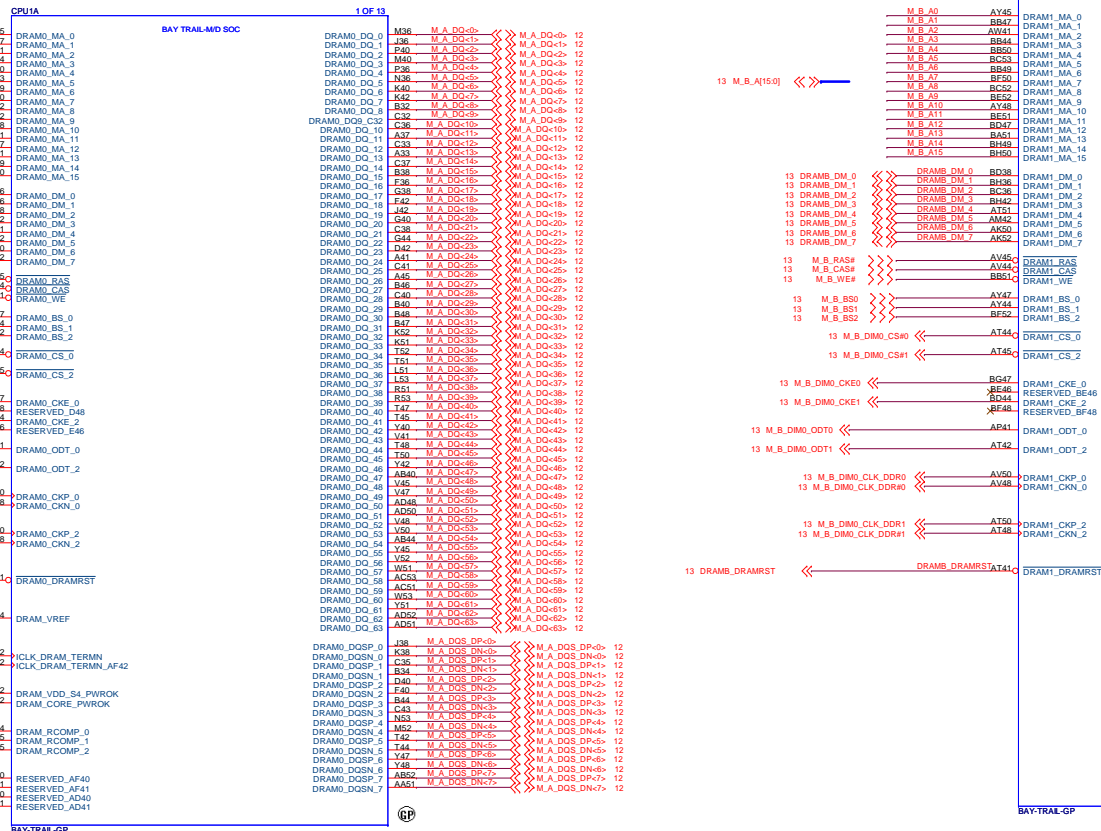
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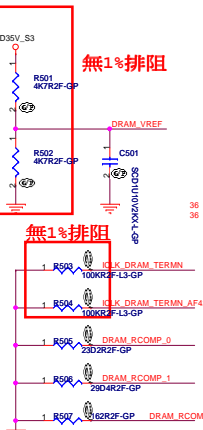
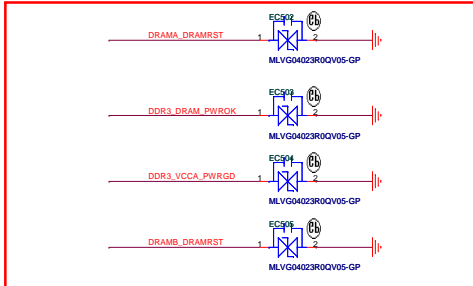
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Title			<b>CPU (Reserved)</b>		
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reserve the 0402 0.1u caps on reset for EMI.



SSID = CPU

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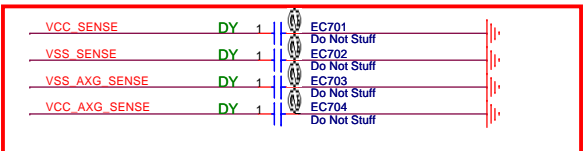
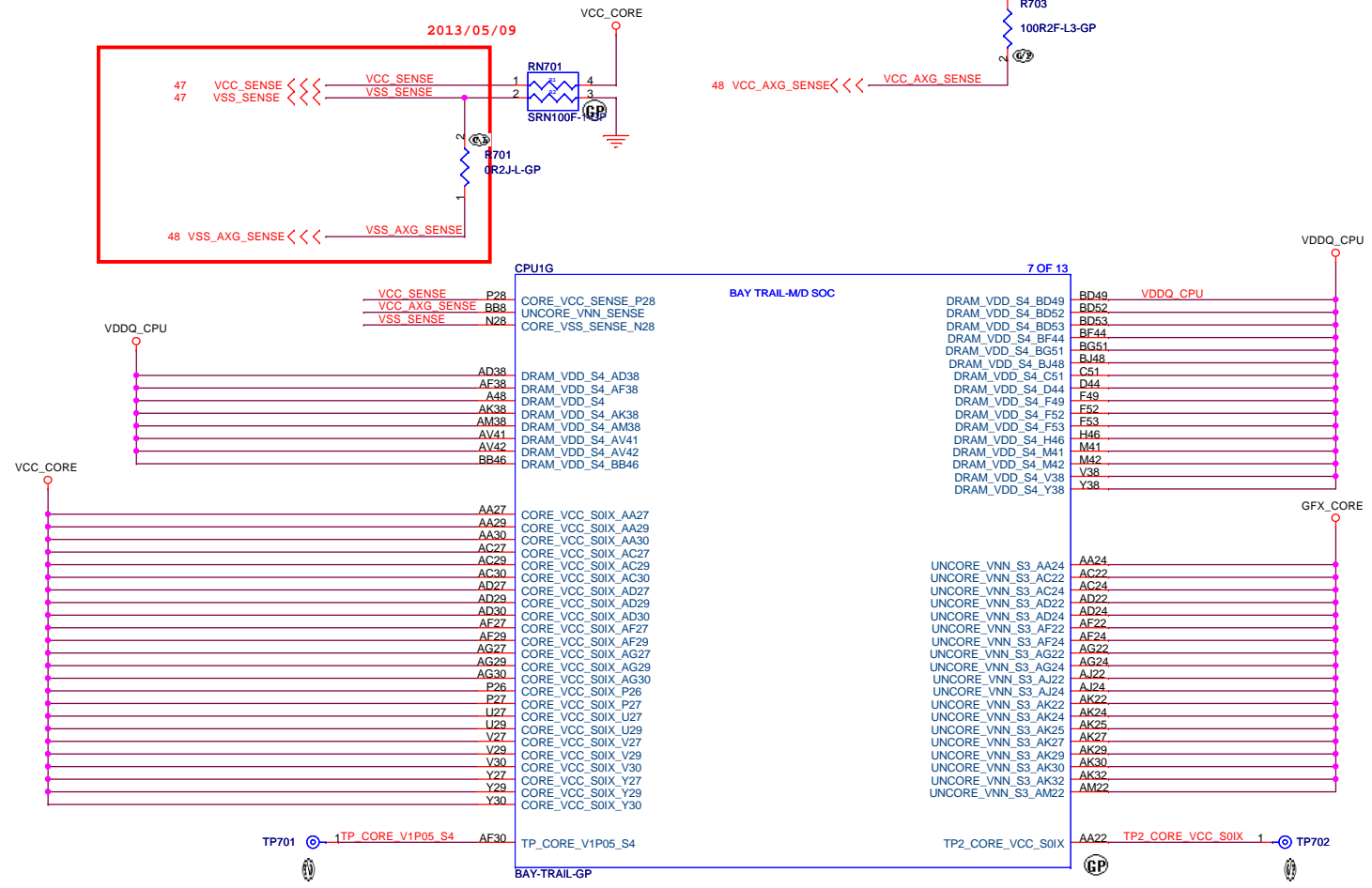
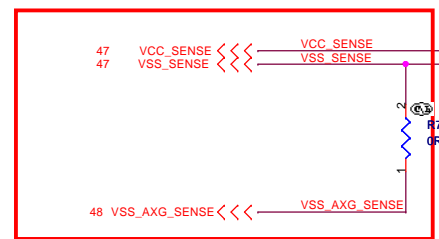
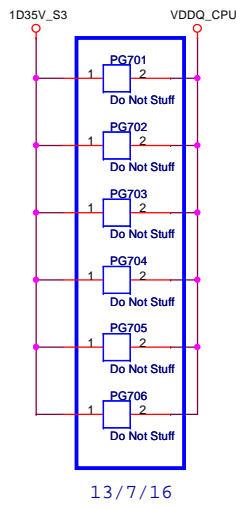
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<b>CPU (CFG)</b>		
Size	Document Number	Rev
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SSID = CPU

2013/05/09



reserve the 0402 0.1u caps on reset for EMI.

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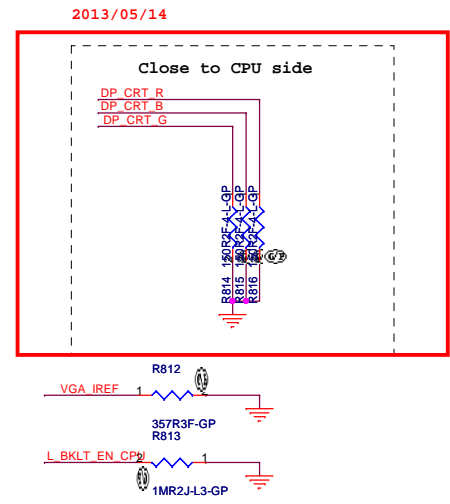
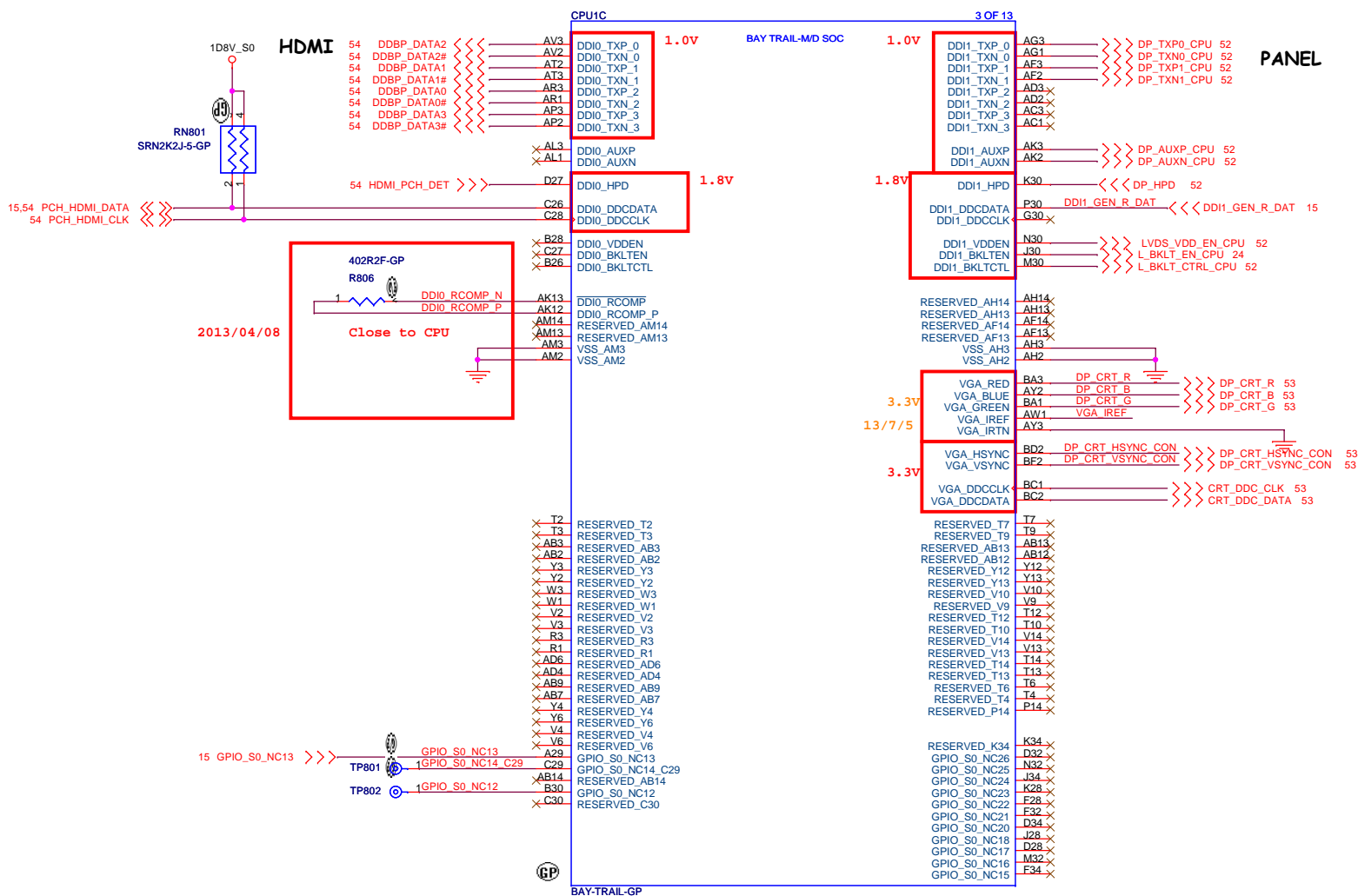
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Title CPU (VCC CORE)  
Size A3 Document Number EA40 BM Rev -1  
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SSID = CPU

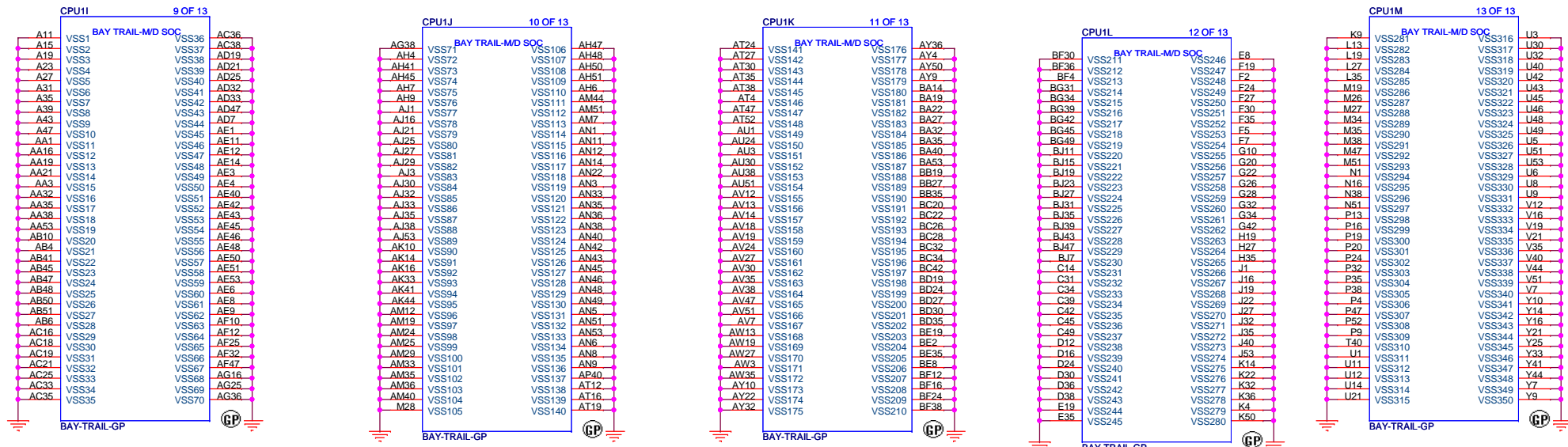


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Title	<b>CPU (DDI/EDP/GPIO)</b>	
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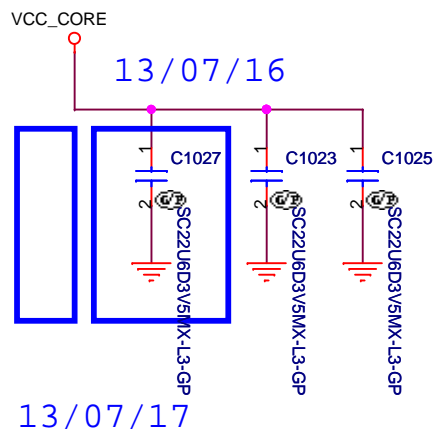
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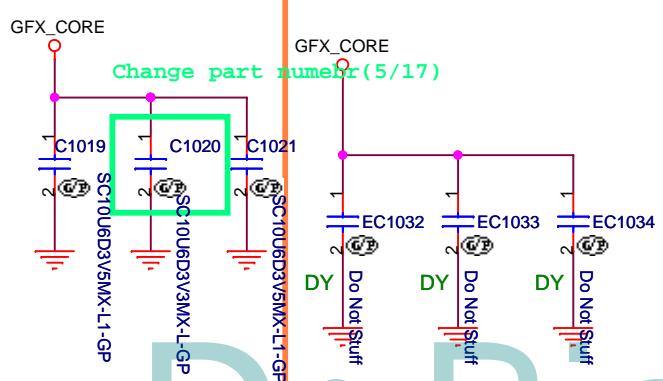
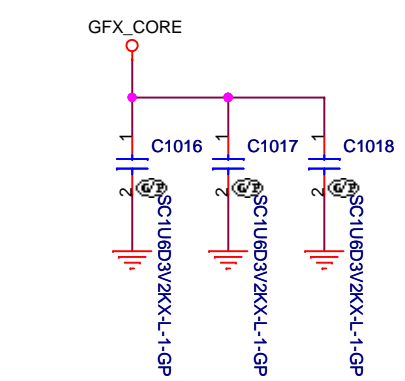
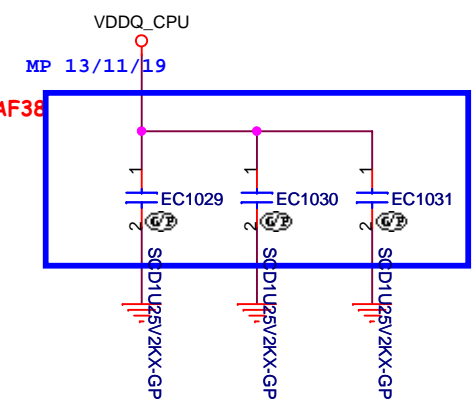
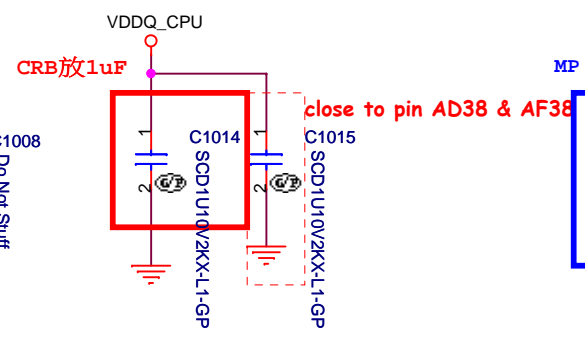
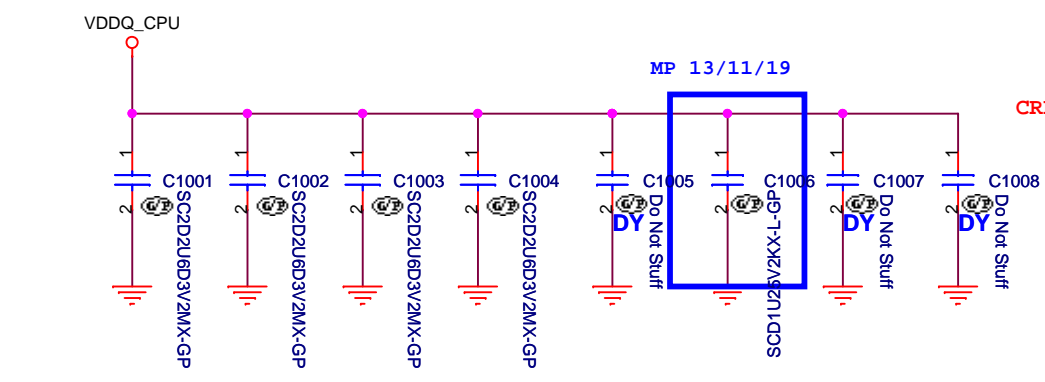
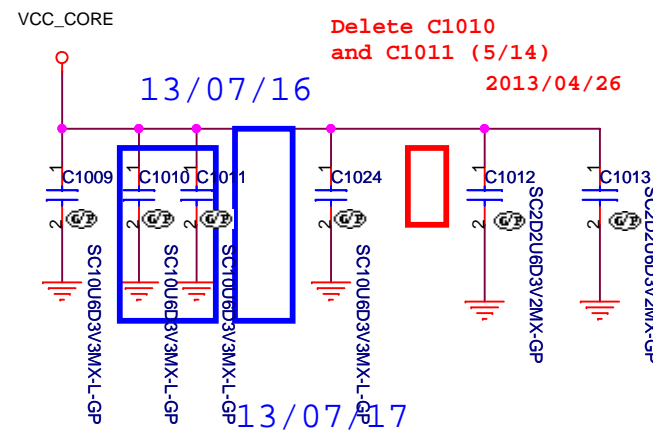
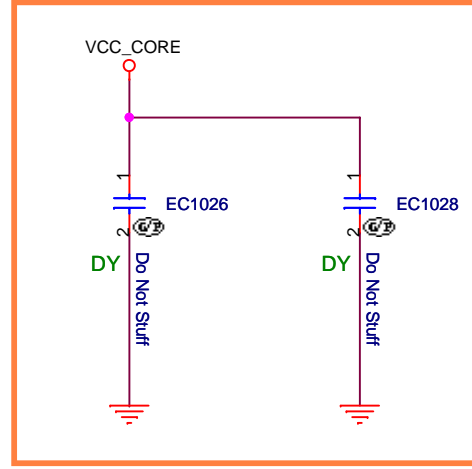
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Title		
<b>CPU (VSS)</b>		
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reserve the 0402 0.1u caps on reset for EMI(5/9).



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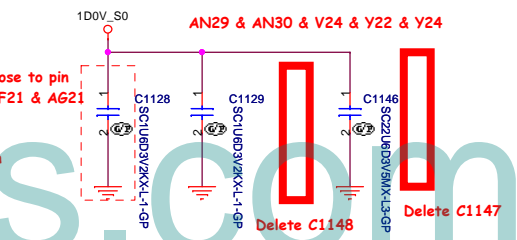
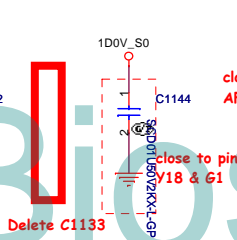
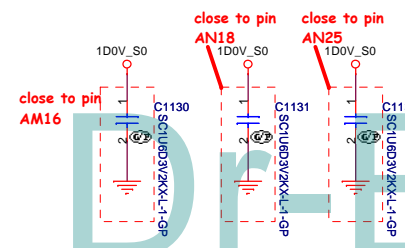
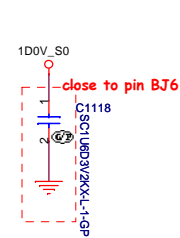
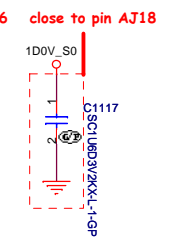
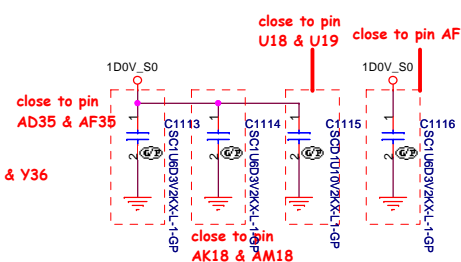
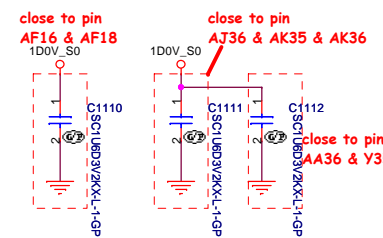
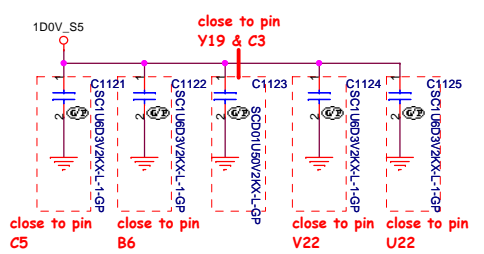
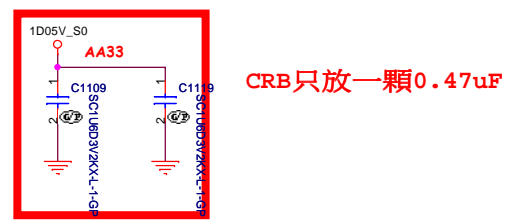
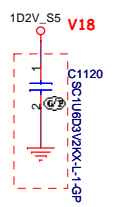
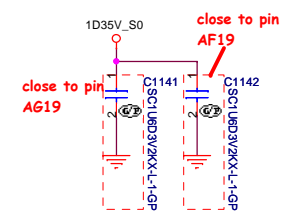
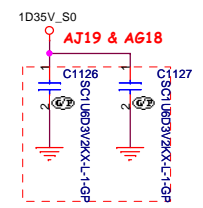
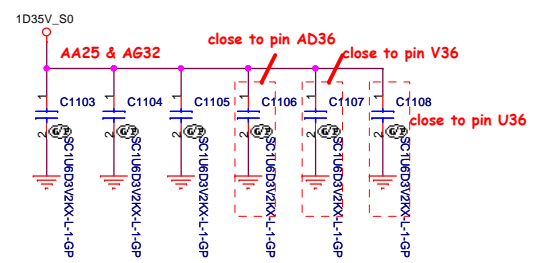
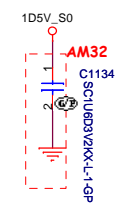
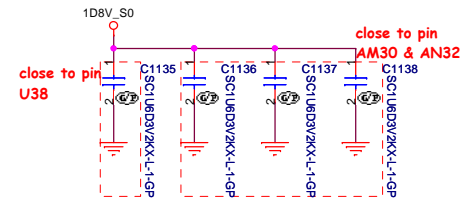
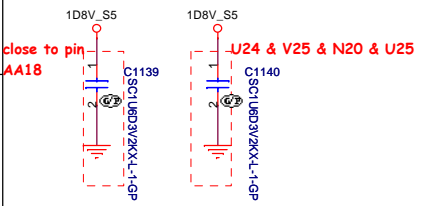
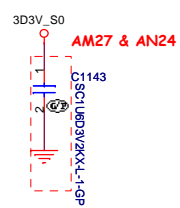
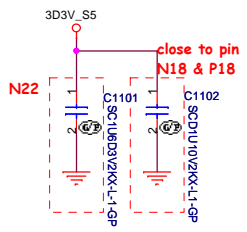
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Title		<b>CPU (Power CAP1)</b>	
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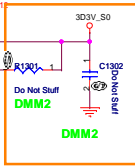
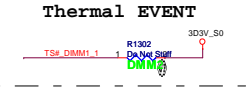
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M\_B\_A[15:0] 5

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M.B.A1	97	A1
M.B.A2	96	A2
M.B.A3	95	A3
M.B.A4	92	A4
M.B.A5	91	A5
M.B.A6	90	A6
M.B.A7	86	A7
M.B.A8	85	A8
M.B.A9	84	A9
M.B.A10	107	A10/AP
M.B.A11	84	A11
M.B.A12	83	A12
M.B.A13	80	A13
M.B.A14	80	A14
M.B.A15	78	A15
M.B.A16/BA2	78	A16/BA2
M.B.BS2	>>>	109
M.B.BS0	>>>	108
M.B.BS1	>>>	108
M.B.DQ<0>	>>>	5
M.B.DQ<1>	>>>	7
M.B.DQ<2>	>>>	15
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M.B.DQ<4>	>>>	6
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M.B.DQ<6>	>>>	18
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M.B.DQ<8>	>>>	33
M.B.DQ<9>	>>>	33
M.B.DQ<10>	>>>	35
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M.B.DQ<16>	>>>	41
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M.B.DQ<18>	>>>	53
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M.B.DQ<49>	>>>	164
M.B.DQ<50>	>>>	166
M.B.DQ<51>	>>>	174
M.B.DQ<52>	>>>	176
M.B.DQ<53>	>>>	181
M.B.DQ<54>	>>>	183
M.B.DQ<55>	>>>	191
M.B.DQ<56>	>>>	193
M.B.DQ<57>	>>>	180
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M.B.DQ<63>	>>>	82
M.B.DQ<64>	>>>	136
M.B.DQ<65>	>>>	152
M.B.DQ<66>	>>>	169
M.B.DQ<67>	>>>	186
M.B.DQS<0>	>>>	12
M.B.DQS<1>	>>>	29
M.B.DQS<2>	>>>	47
M.B.DQS<3>	>>>	64
M.B.DQS<4>	>>>	137
M.B.DQS<5>	>>>	154
M.B.DQS<6>	>>>	171
M.B.DQS<7>	>>>	188
M.B.DIMS<0>	>>>	116
M.B.DIMS<1>	>>>	120
M.B.DIMS<2>	>>>	126
M.B.DIMS<3>	>>>	1
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M.B.DIMS<6>	>>>	204

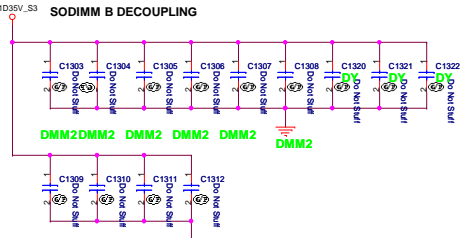
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WE#	M_B_WE# 5
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CS14	M_B_DIM0_CS#1 5
CKE0	M_B_DIM0_CKE0 5
CKE1	M_B_DIM0_CKE1 5
CK0	M_B_DIM0_CLK_DDR0 5
CK0K	M_B_DIM0_CLK_DDR#0 5
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DM1	DRAMB_DM_1 5
DM2	DRAMB_DM_2 5
DM3	DRAMB_DM_3 5
DM4	DRAMB_DM_4 5
DM5	DRAMB_DM_5 5
DM6	DRAMB_DM_6 5
DM7	DRAMB_DM_7 5
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DM19	DRAMB_DM_19 5
DM20	DRAMB_DM_20 5
DM21	DRAMB_DM_21 5
DM22	DRAMB_DM_22 5
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DM24	DRAMB_DM_24 5
DM25	DRAMB_DM_25 5
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DM40	DRAMB_DM_40 5
DM41	DRAMB_DM_41 5
DM42	DRAMB_DM_42 5
DM43	DRAMB_DM_43 5
DM44	DRAMB_DM_44 5
DM45	DRAMB_DM_45 5
DM46	DRAMB_DM_46 5
DM47	DRAMB_DM_47 5
DM48	DRAMB_DM_48 5
DM49	DRAMB_DM_49 5
DM50	DRAMB_DM_50 5
DM51	DRAMB_DM_51 5
DM52	DRAMB_DM_52 5
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DM54	DRAMB_DM_54 5
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DM56	DRAMB_DM_56 5
DM57	DRAMB_DM_57 5
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DM59	DRAMB_DM_59 5
DM60	DRAMB_DM_60 5
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DM193	DRAMB_DM_193 5
DM194	DRAMB_DM_194 5
DM195	DRAMB_DM_195 5
DM196	DRAMB_DM_196 5
DM197	DRAMB_DM_197 5
DM198	DRAMB_DM_198 5
DM199	DRAMB_DM_199 5
DM200	DRAMB_DM_200 5

Note: SO-DIMM SPD Address is 0xA4 SO-DIMM TS Address is 0x34 SO-DIMM B is placed farther from the Processor than SO-DIMMA



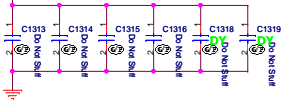
13/7/5

Layout Note: Place these Caps near SO-DIMM B.

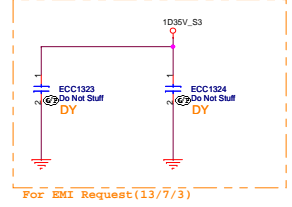


DMM2 DMM2 DMM2 DMM2

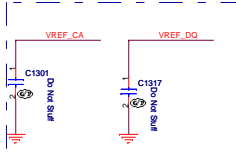
Place these caps close to VTT1 and VTT2.



DMM2 DMM2 DMM2 DMM2



For EMI Request (13/7/3)



Close RAM3 CA & DQ pin DMM2 DMM2

H=4mm DMM2

2nd = 62.10024.G21

3rd = 62.10024.M31

4th = 62.10017.X41

Do Not Stuff

DM2 change part number to 62.10024.S21(13/7/3)

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Title **Reserved**

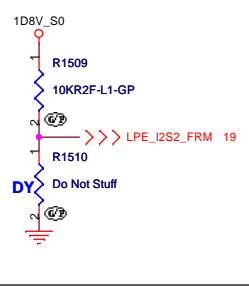
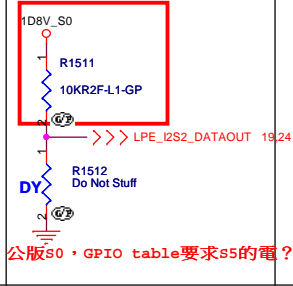
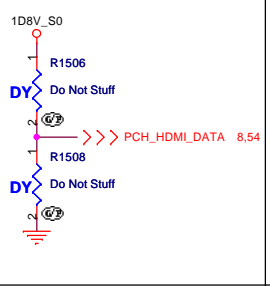
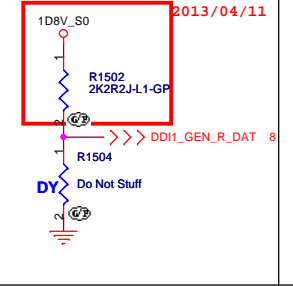
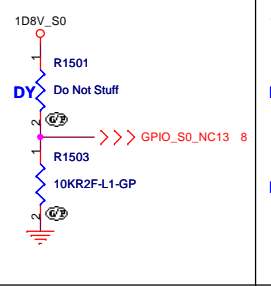
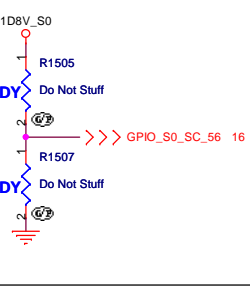
Size A4	Document Number <b>EA40 BM</b>	Rev <b>-1</b>
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Date: Tuesday, November 19, 2013 Sheet 14 of 102

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# SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap
<b>GPIO</b>	<b>GPIO_S0_SC[063]</b>	<b>GPIO_S0_SC[065]</b>	<b>DDI0_DDCDATA</b>	<b>DDI1_DDCDATA</b>	<b>MDSI_DDCDATA</b>	<b>GPIO_S0_SC [56]</b>
<b>Schematic</b>						
<b>High</b>	SPI	Normal Operation	DDI0 detected	DDI1 detected	DDI1 detected	
<b>Low</b>	LPC	Override	DDI0 not detected	DDI1 not detected	DDI1 not detected	

## 2.25 Hardware Straps

All straps are sampled on the rising edge of PMC\_CORE\_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

## 30.2 LPE\_I2S2\_DATAOUT/ GPIO\_S0\_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO\_S0\_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

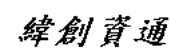
### 27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

**Note:** The Top-Swap strap is an active high signal and is multiplexed with the GPIO\_S0\_SC[56] signal.

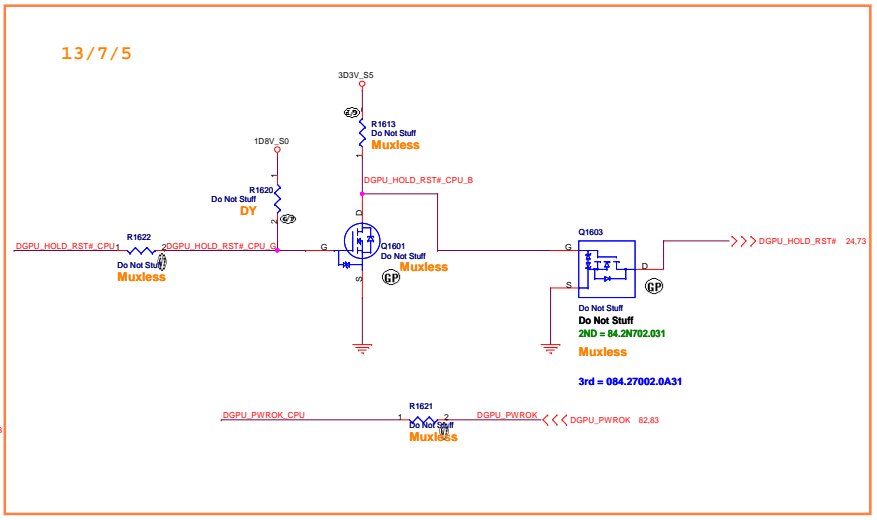
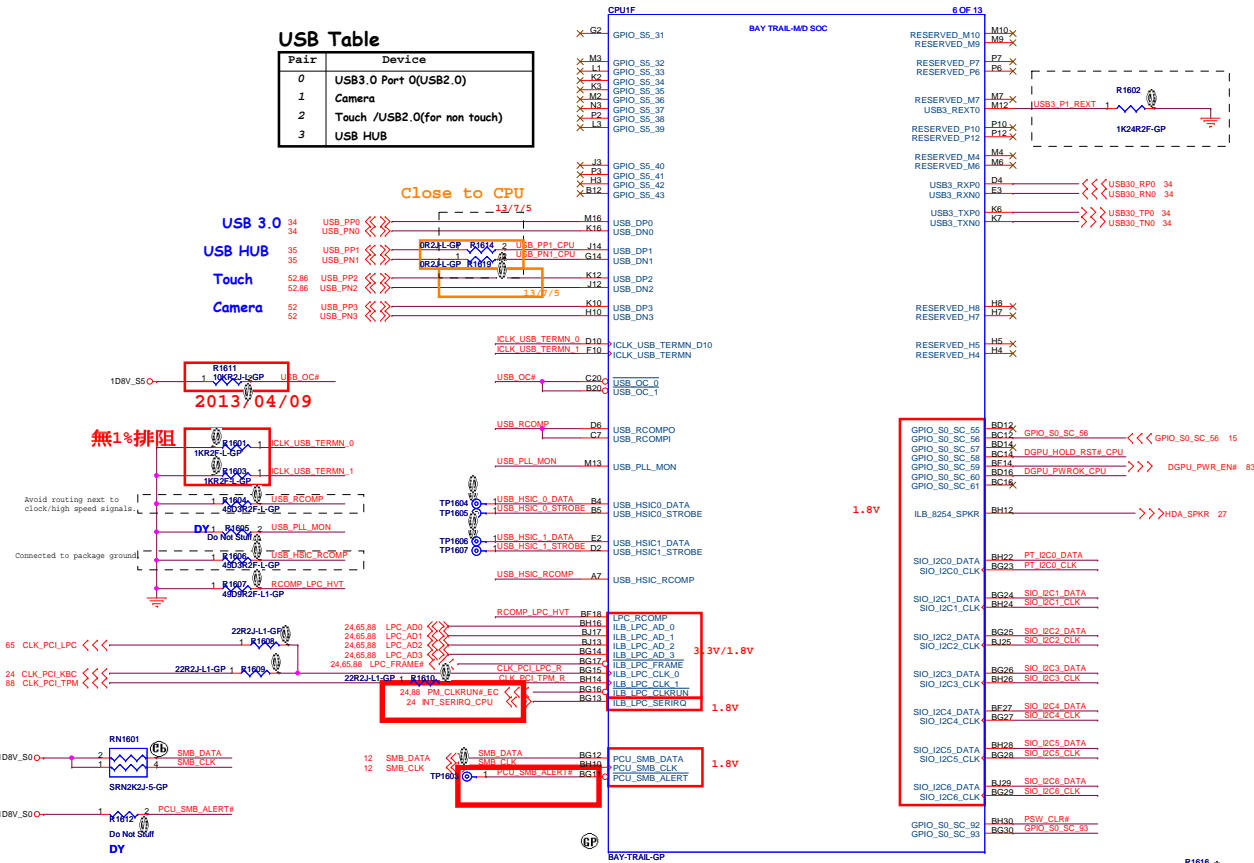
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<b>CPU(STRAP)</b>	
Size A3	Document Number
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**USB Table**

Pair	Device
0	USB3.0 Port 0(USB2.0)
1	Camera
2	Touch /USB2.0(for non touch)
3	USB HUB



2013/04/09

無1%排阻

1.8V

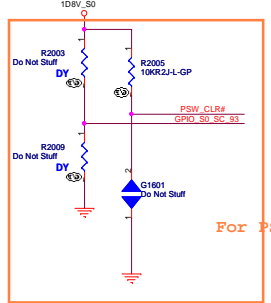
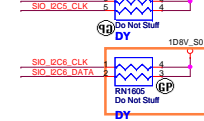
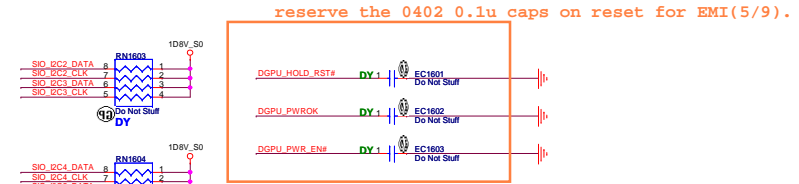
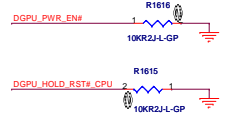
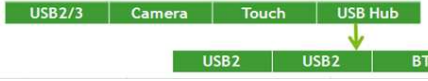
3.3V/1.8V

1.8V

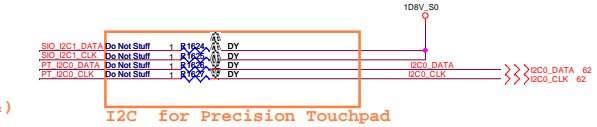
1.8V

**USB Port Routing Guide for Bay Trail-M**

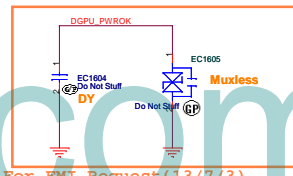
WO/ Lighting Bolt(Can support 3 USB I/O Ports)



For PSW\_CLR#(5/14)



I2C for Precision Touchpad



For EMI Request(13/7/3)

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SSID = PCH

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**CPU (DMI/FDI/PM)**

Size

A4

Document Number

**EA40 BM**

Rev

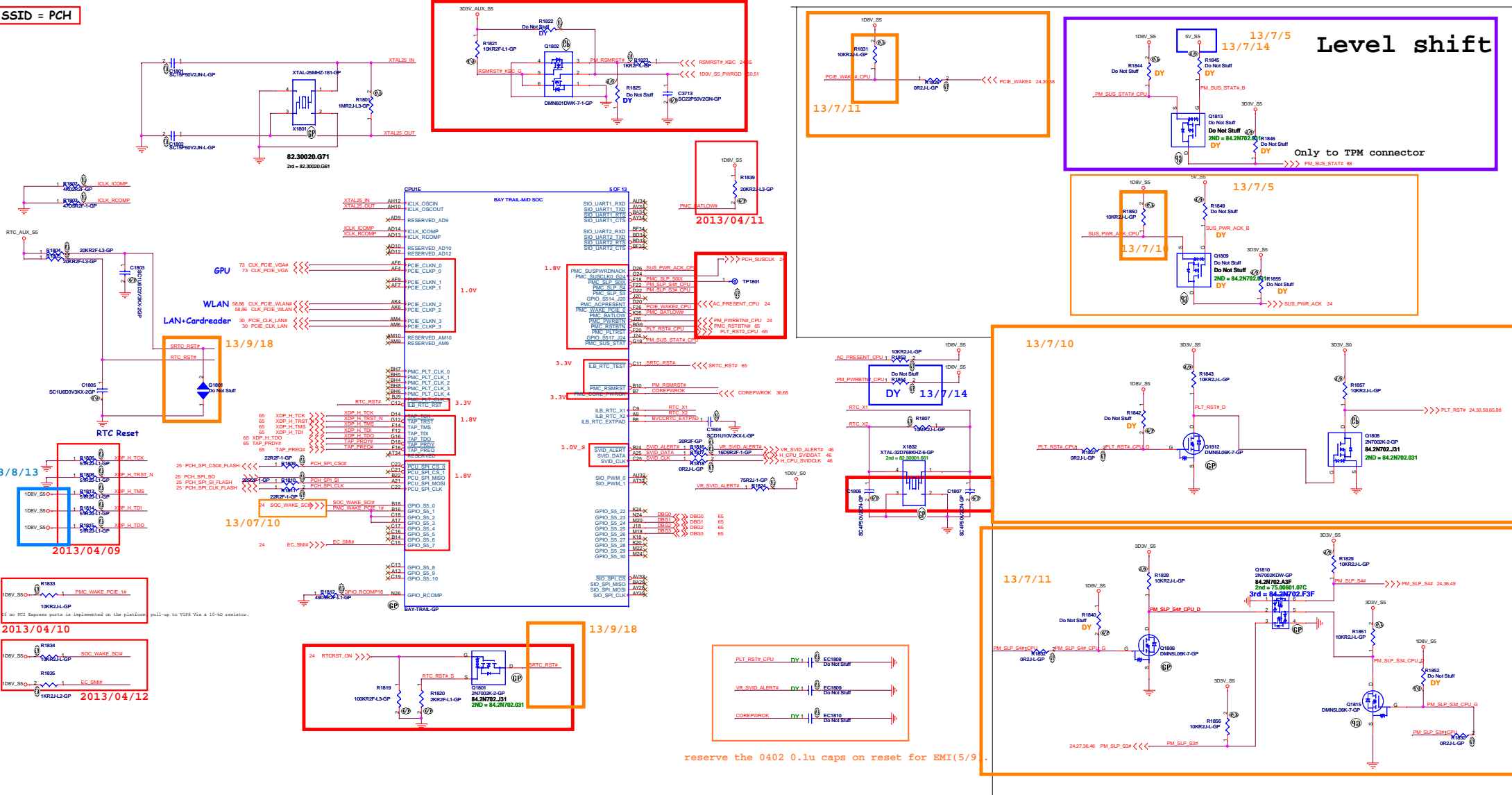
**-1**

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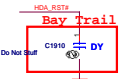
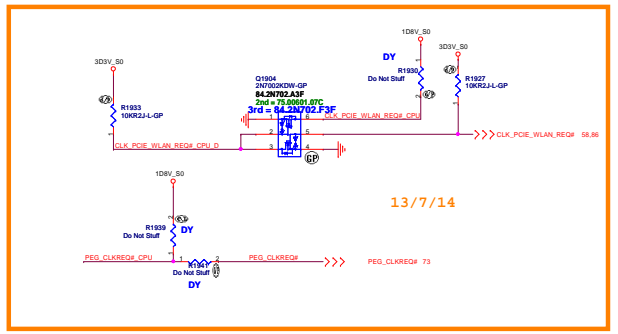
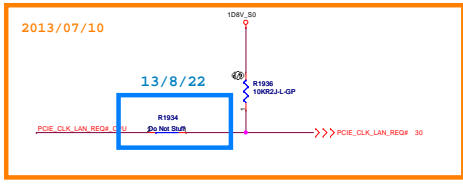
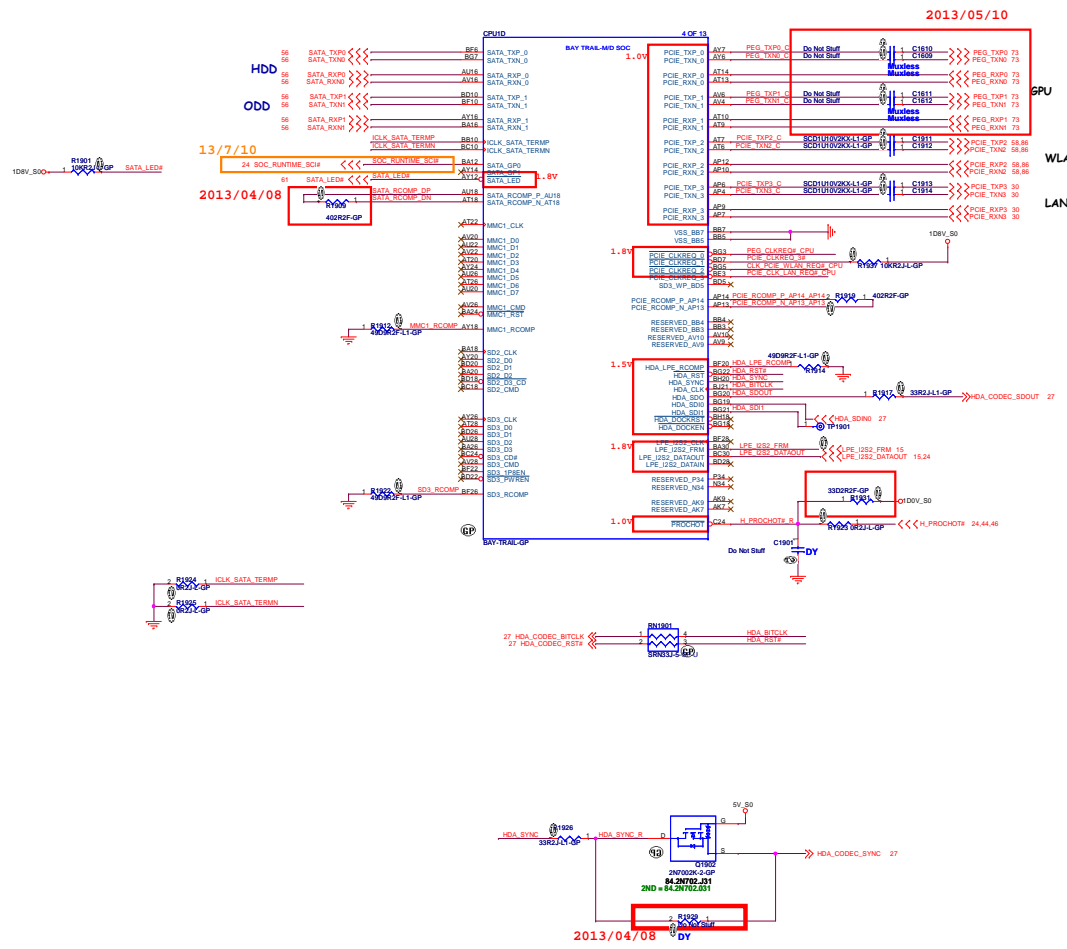
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SSID = PCH



reserve the 0402 0.1u caps on reset for EMI(5/9).

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SSID = PCH

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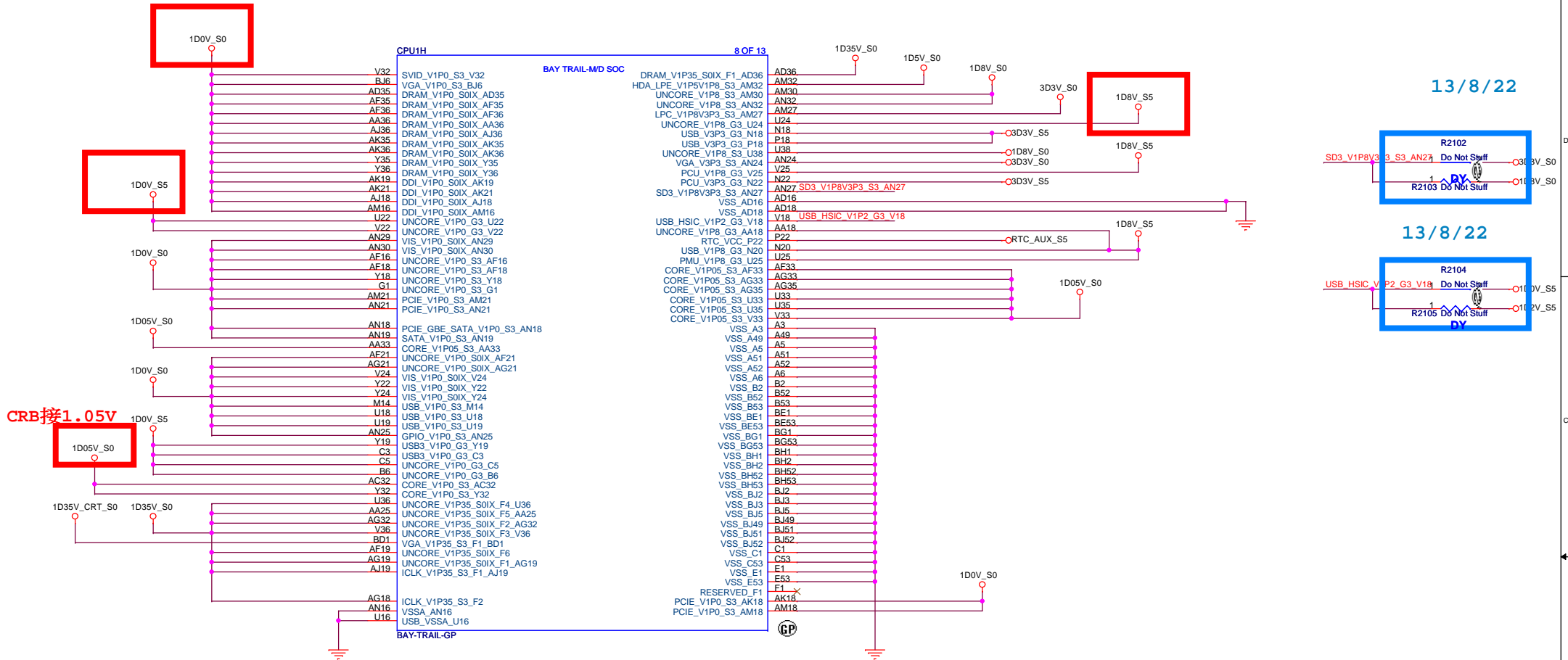
Rev

**-1**

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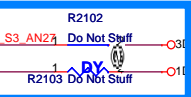
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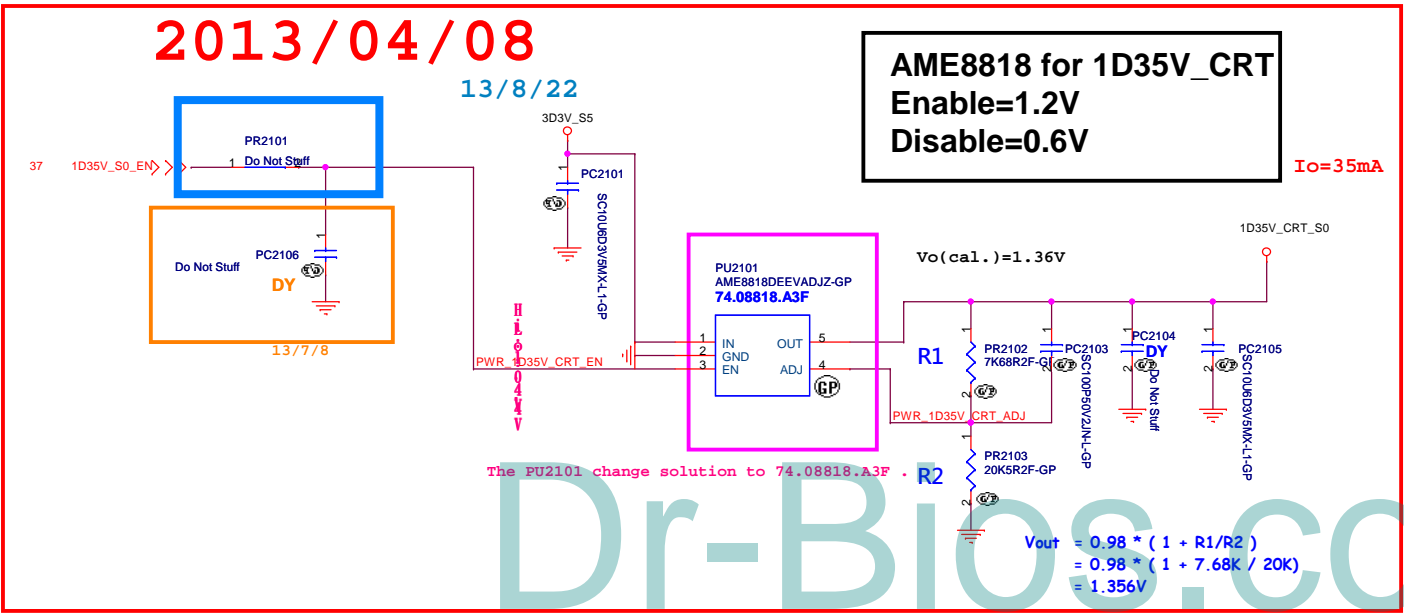
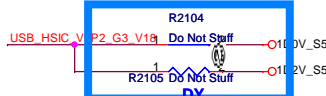


CRB接1.05V

13/8/22



13/8/22



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SSID = PCH

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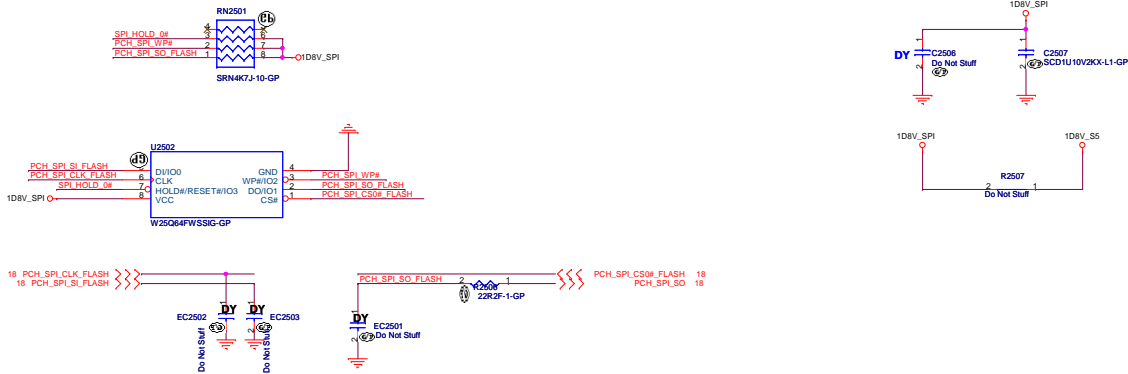
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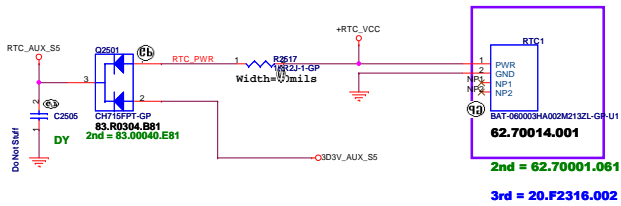
**SSID = Flash.ROM**

**SPI FLASH ROM (8M byte) for PCH**



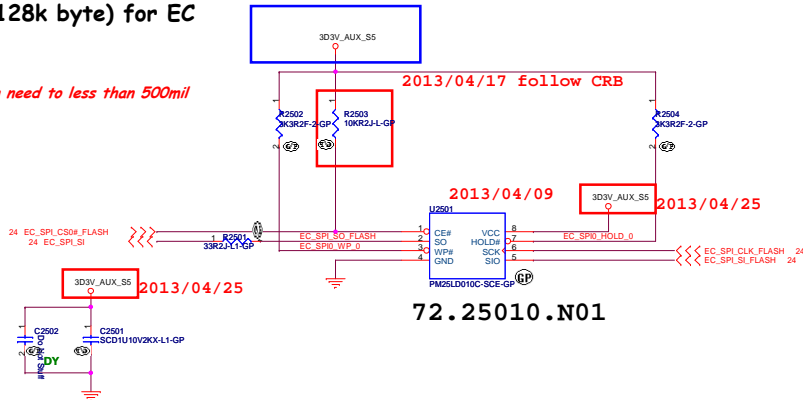
72.25Q64.S01

**SSID = RBAT**



**SPI FLASH ROM (128k byte) for EC**

*SPI ROM Equal length need to less than 500mil*



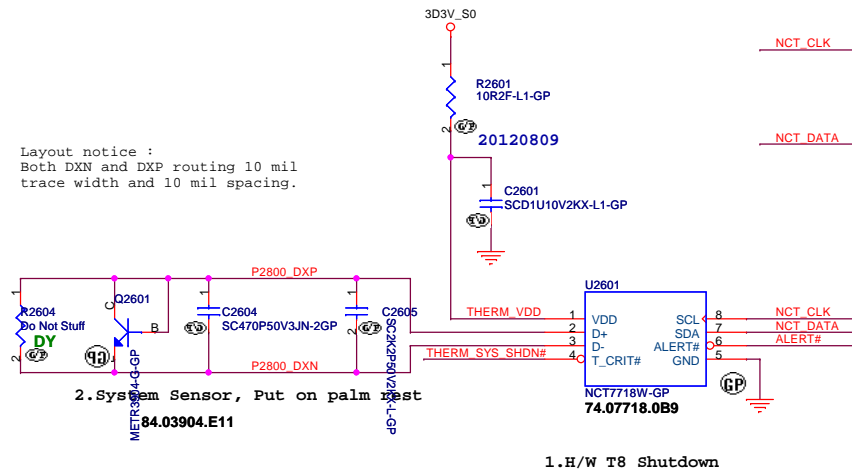
72.25010.N01

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**SSID = Thermal**

# Thermal sensor NCT 7718W

Layout notice :  
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



1.H/W T8 Shutdown

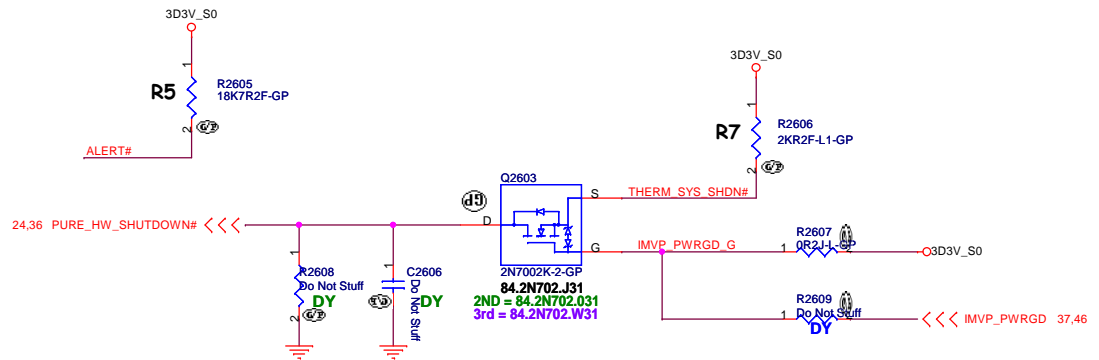
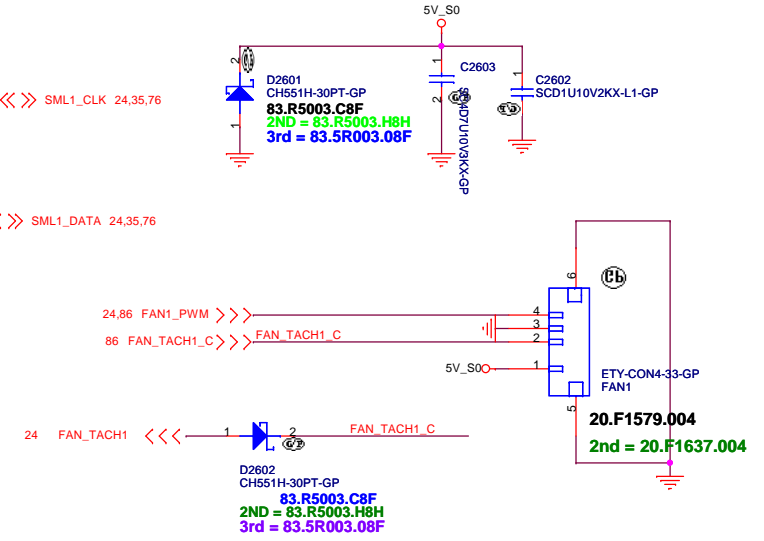
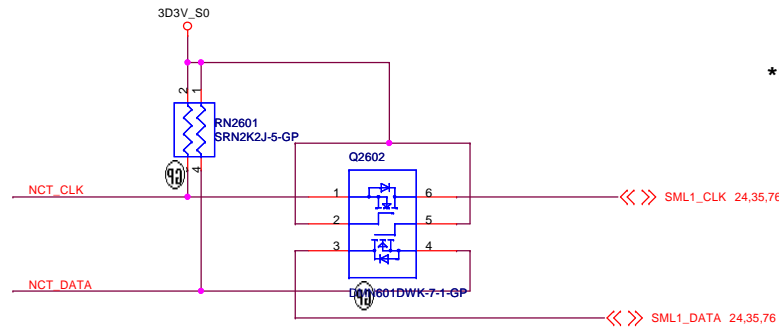
ALERT# /T CRIT#  
Pull-up Resistor

R5	77°C	87°C	97°C	107°C	117°C
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T\_CRIT temperature strapping point

T8=85 degree

\*Layout\* 15 mil



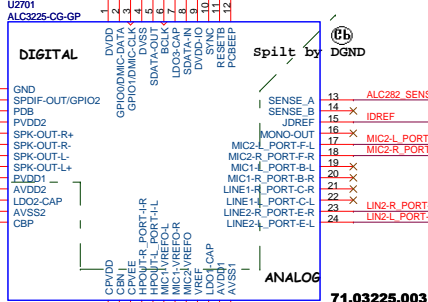
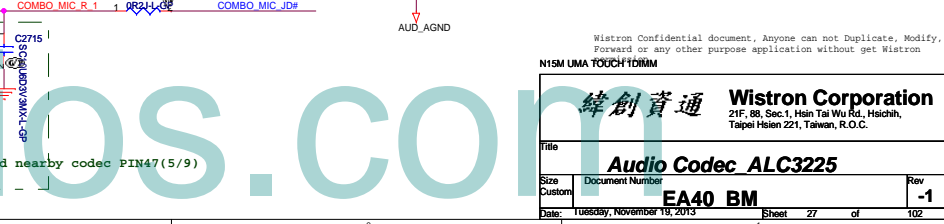
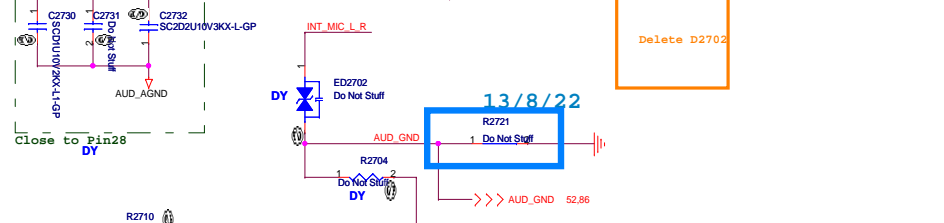
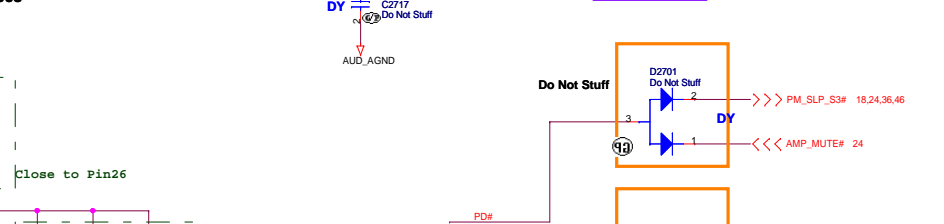
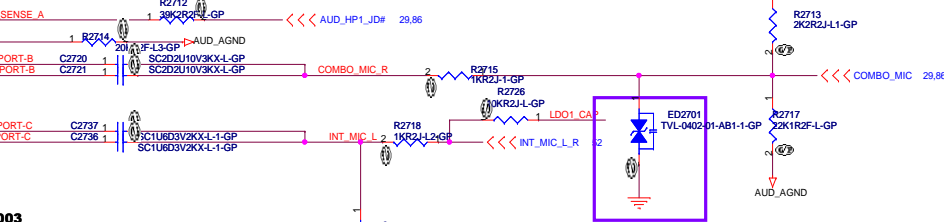
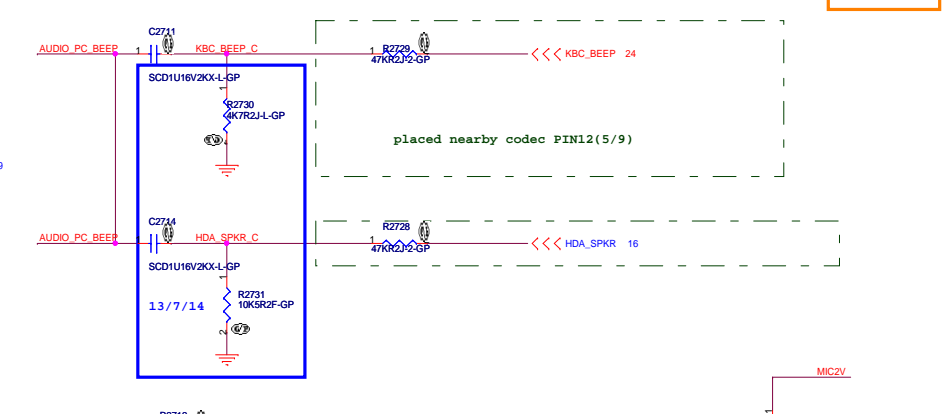
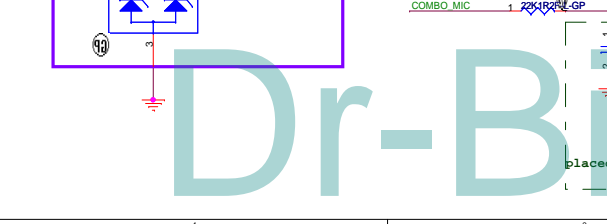
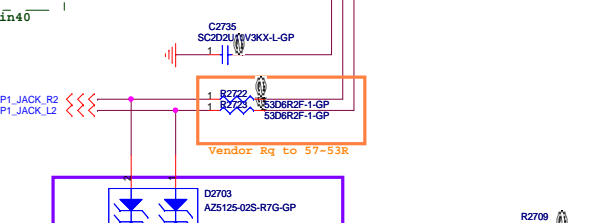
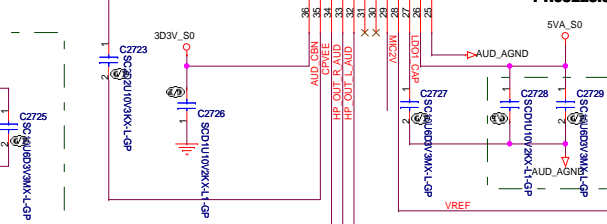
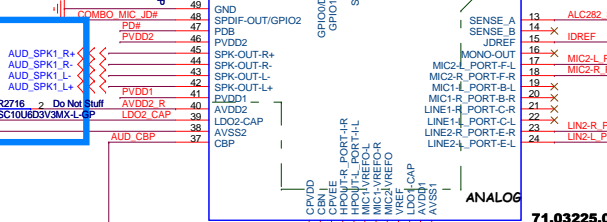
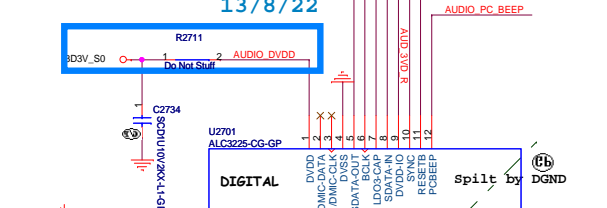
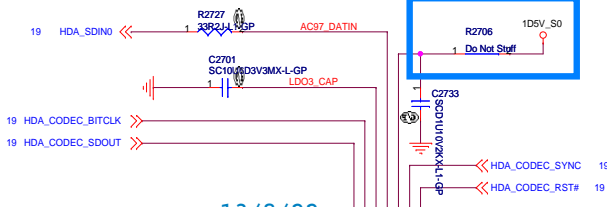
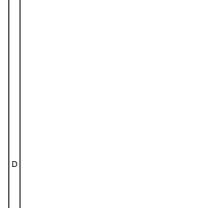
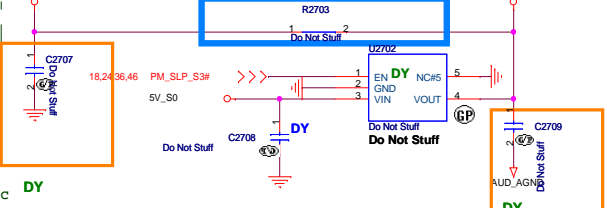
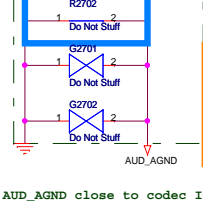
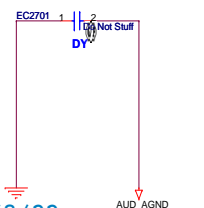
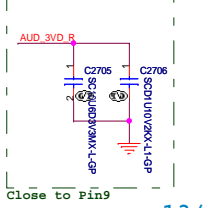
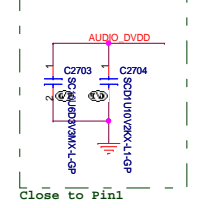
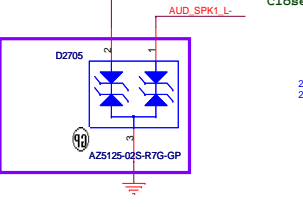
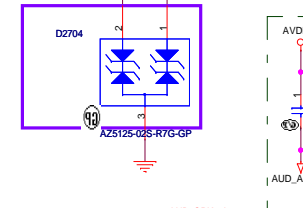
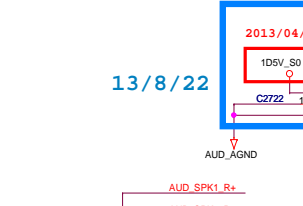
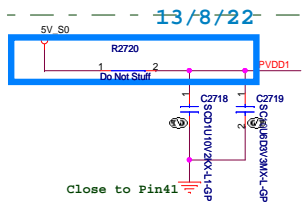
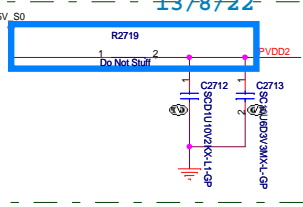
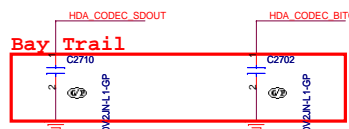
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Title	Thermal 7718/Fan Controller P2793	
Size	Document Number	Rev
A3	EA40 BM	-1
Date:	Tuesday, November 19, 2013	Sheet 26 of 102

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Title	Audio Codec ALC3225		
Size	Document Number	EA40 BM	Rev
Custom			-1
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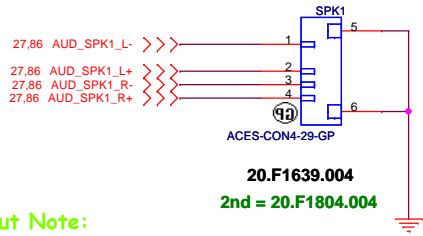
**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>Reserved</b>		
Size	Document Number	Rev
A4	<b>EA40 BM</b>	<b>-1</b>
Date:	Tuesday, November 19, 2013	Sheet 28 of 102

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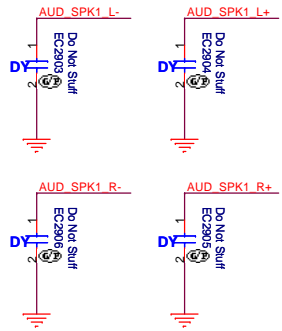
**SSID = AUDIO**

*Speaker*

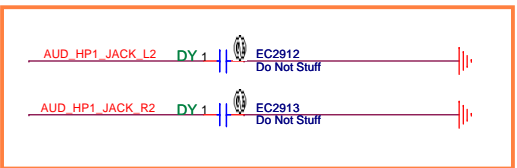
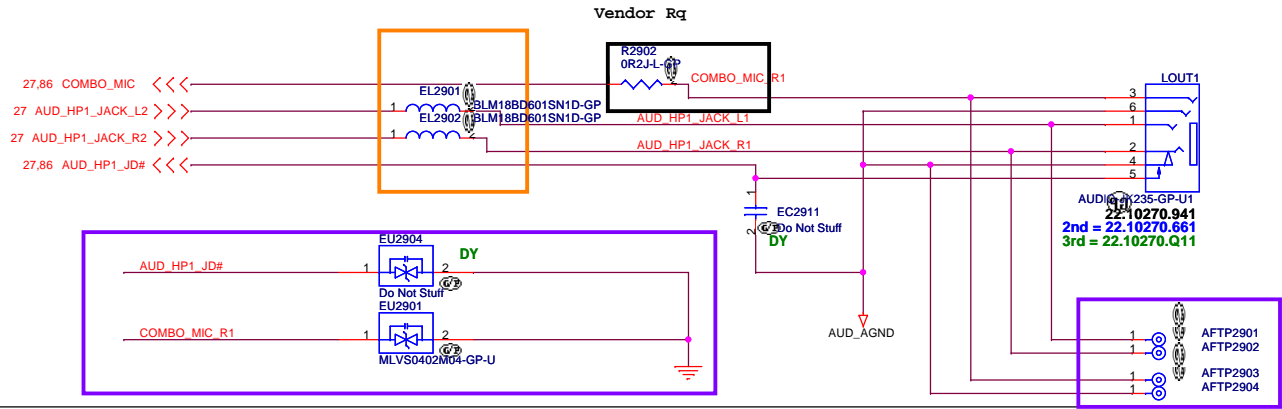


Layout Note:

Trace width=40mil



*Combo Jack*



reserve the 0402 0.1u caps on reset for EMI(5/9).

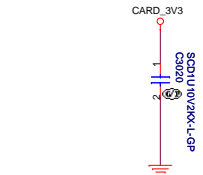
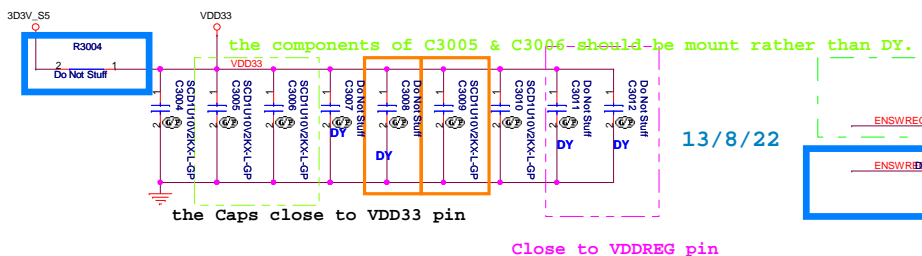
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Title	Audio Jack	
Size Custom	Document Number	Rev
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Date: Tuesday, November 19, 2013	Sheet 29 of 102	

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13/8/22

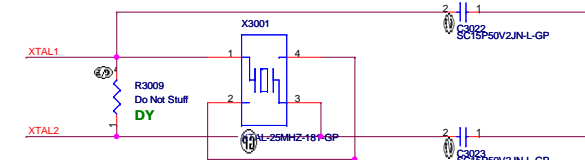
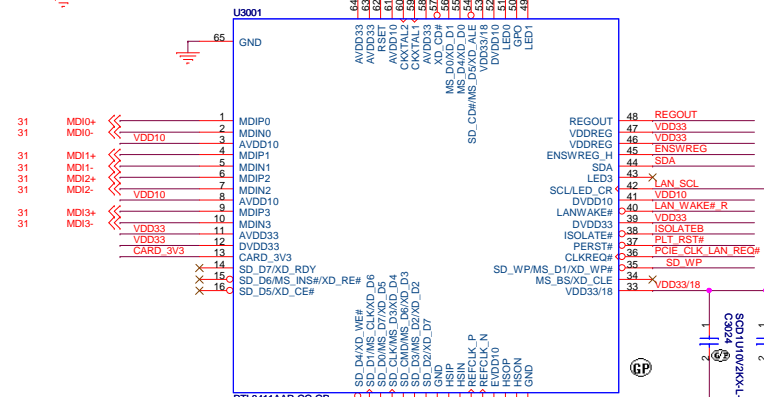
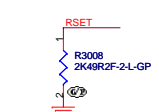
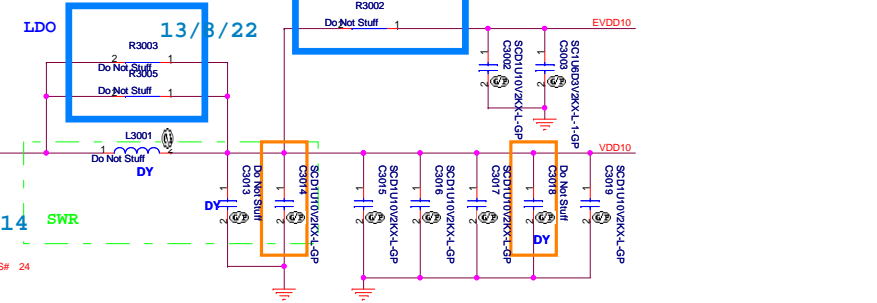
13/8/22



Close to VDDREG pin

13/8/22

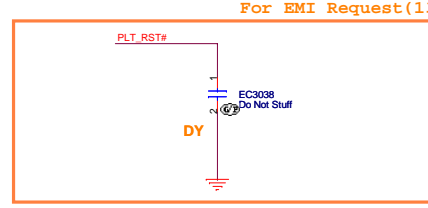
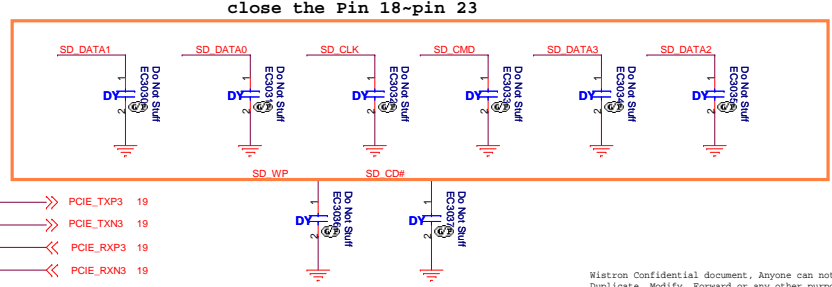
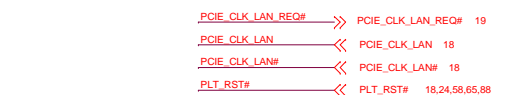
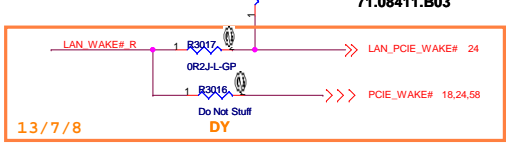
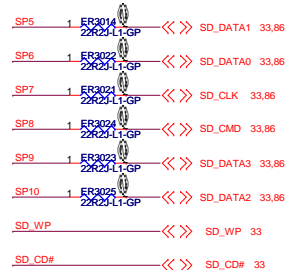
-1 13/8/14 SWR



-1 13/8/14

Add one test point of Pin42 for convenience debug. (5/8)

SP1	SP1	SD_D7	xD_RDY
SP2	SP2	SD_D6	MS_INS#
SP3	SP3	SD_D5	xD_RE#
SP4	SP4	SD_D4	xD_CE#
SP5	SP5	SD_D1	MS_CLK
SP6	SP6	SD_D0	xD_D5
SP7	SP7	SD_CLK	xD_D4
SP8	SP8	SD_CMD	xD_D3
SP9	SP9	SD_D3	MS_D2
SP10	SP10	SD_D2	xD_D7
SP11	SP11	MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1
SP13	SP13	SD_CD#	xD_ALE
SP14	SP14	MS_D4	xD_D0
SP15	SP15	MS_D0	xD_D1
SP16	SP16		xD_CD#



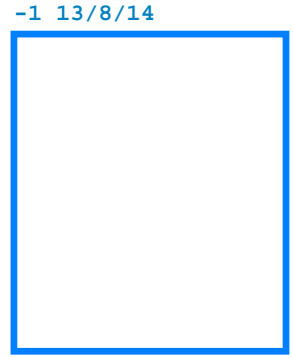
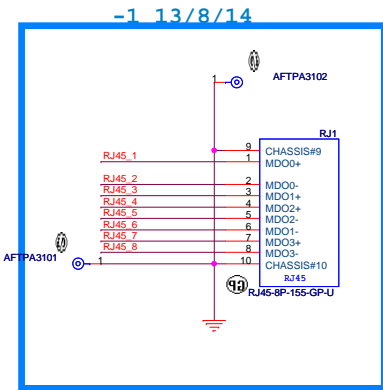
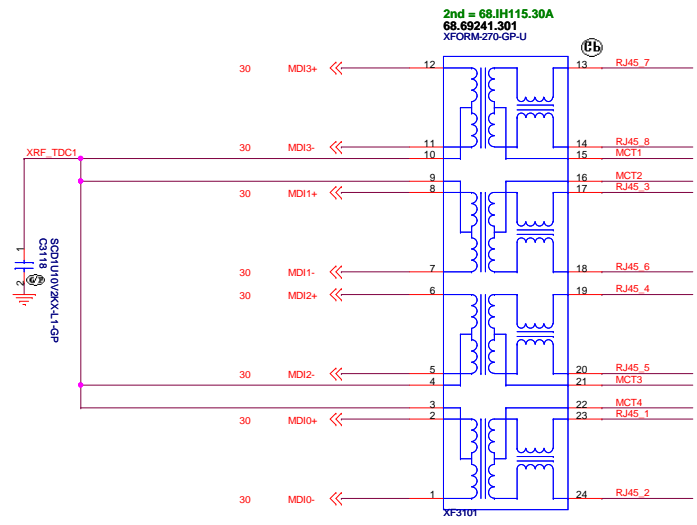
For EMI Request(13/7/3)

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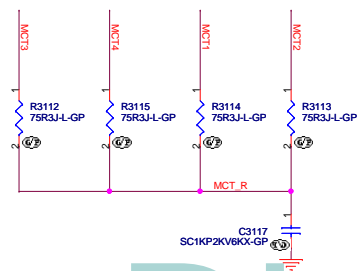
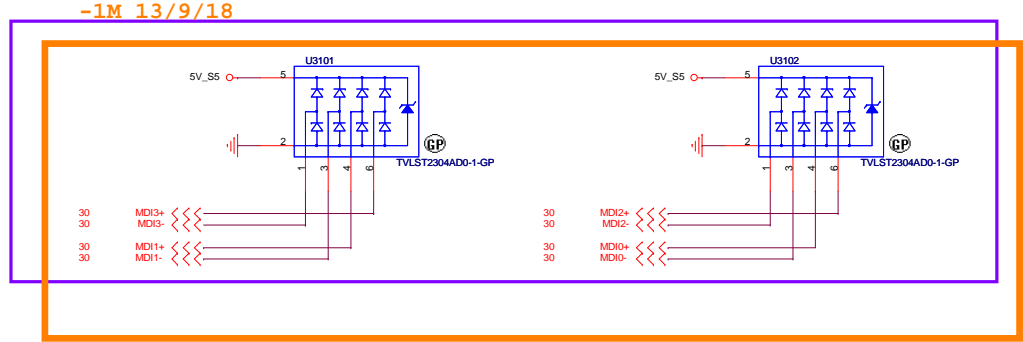
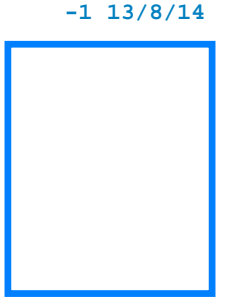
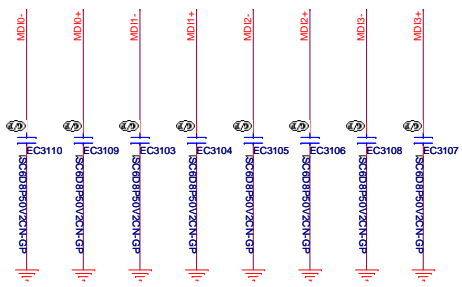
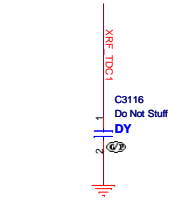
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Title	LAN(RTL8411)		
Size	Document Number		Rev
Custom	EA40 BM		-1
Date:	Thursday, November 21, 2013	Sheet 30	of 102

SSID = LAN



- 86 RJ45\_1 >>>
- 86 RJ45\_2 >>>
- 86 RJ45\_3 >>>
- 86 RJ45\_4 >>>
- 86 RJ45\_5 >>>
- 86 RJ45\_6 >>>
- 86 RJ45\_7 >>>
- 86 RJ45\_8 >>>



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<b>(LAN+VGA) CONNECTOR</b>		
Title		
Size	Document Number	Rev
Custom	<b>EA40 BM</b>	<b>-1</b>
Date:	1/05/2013, November 19, 2013	Sheet 31 of 102

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Title **RTS5170(CARD READER)**

Size A4 Document Number **EA40 BM** Rev **-1**

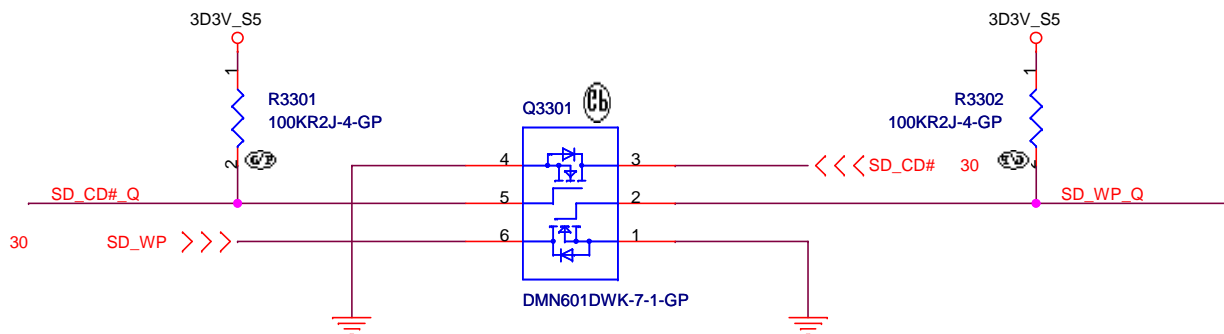
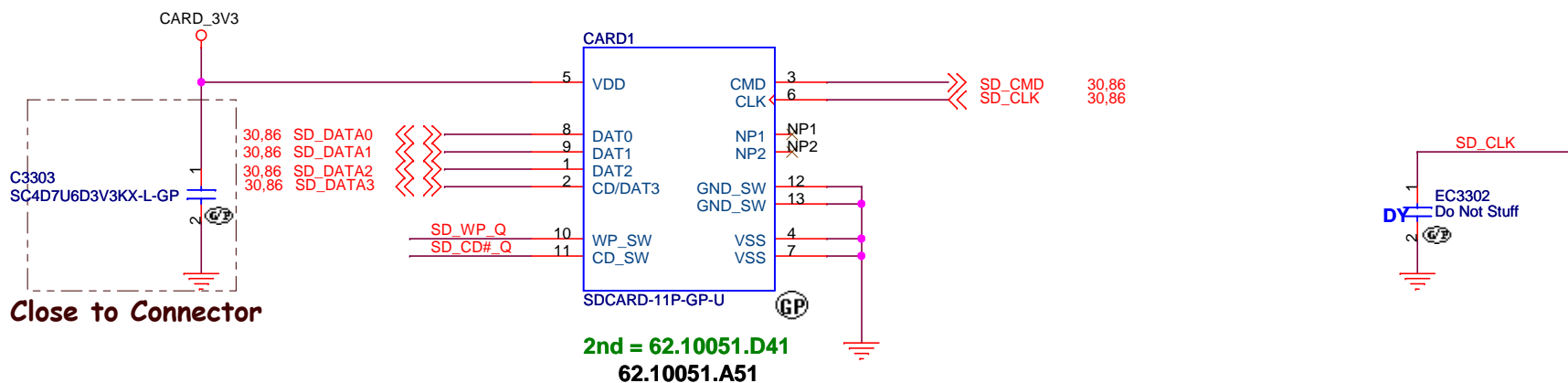
Date: Tuesday, November 19, 2013 Sheet 32 of 102

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**SSID = SDIO**

# SD//MS Card Reader



86 SD\_WP\_Q >>> \_\_\_\_\_

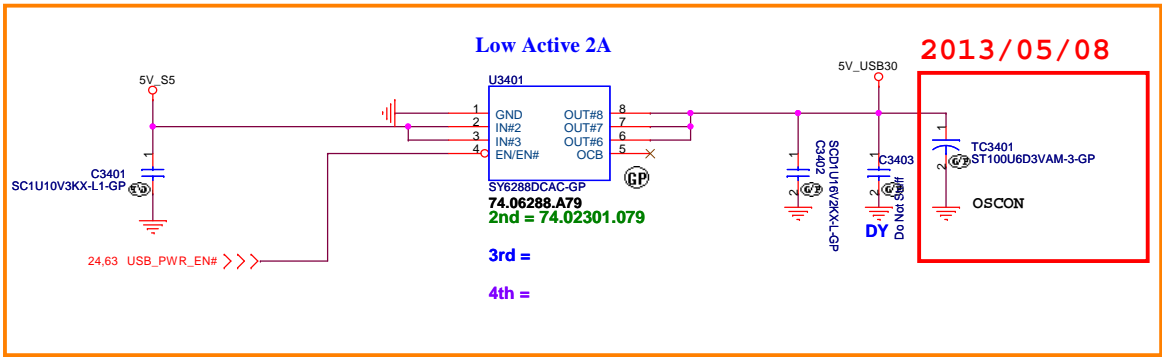
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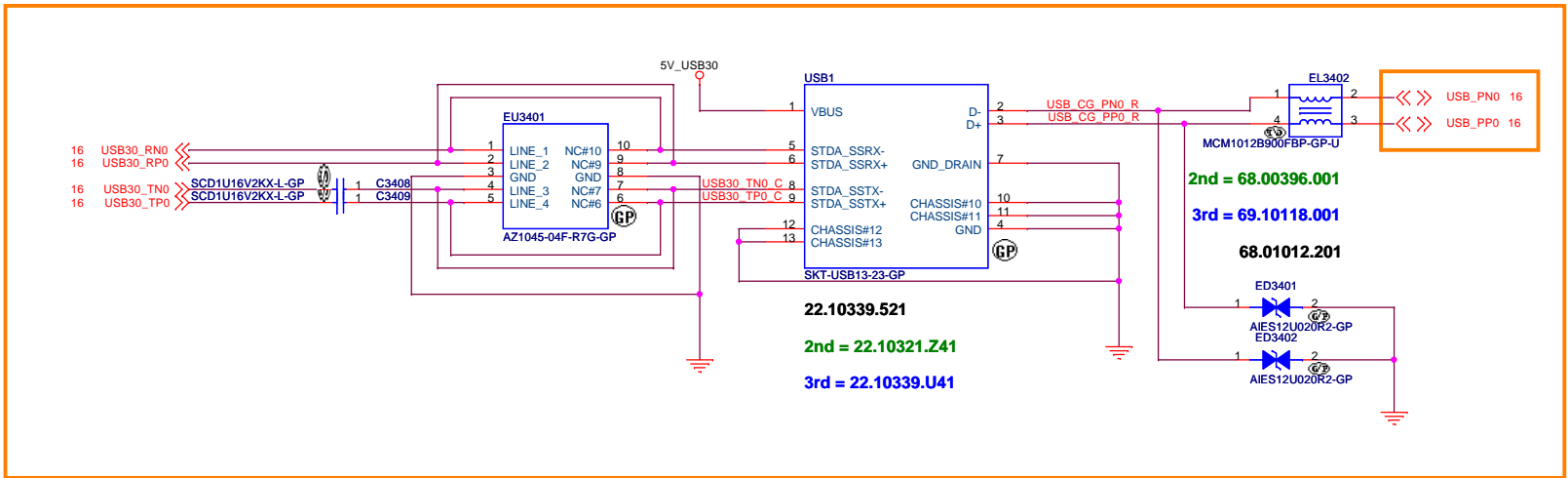
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Title <b>CARD Reader CONN</b>			
Size	Document Number	Rev	
Custom	<b>EA40 BM</b>	<b>-1</b>	
Date:	Tuesday, November 19, 2013	Sheet	33 of 102

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**USB 3.0 Connector**  
**Pin definition**

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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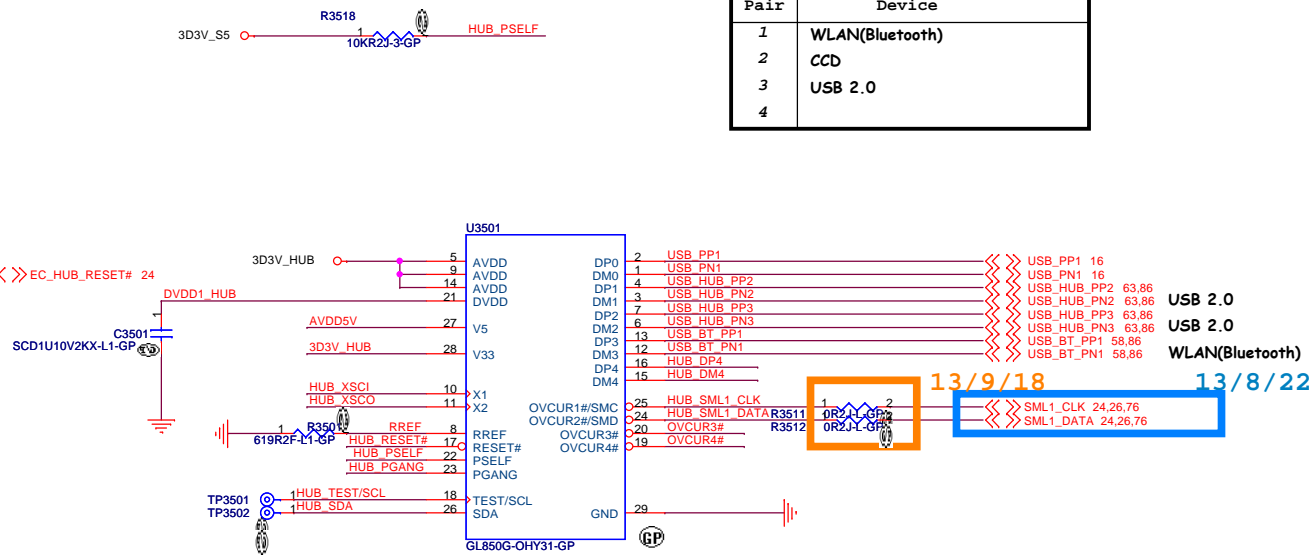
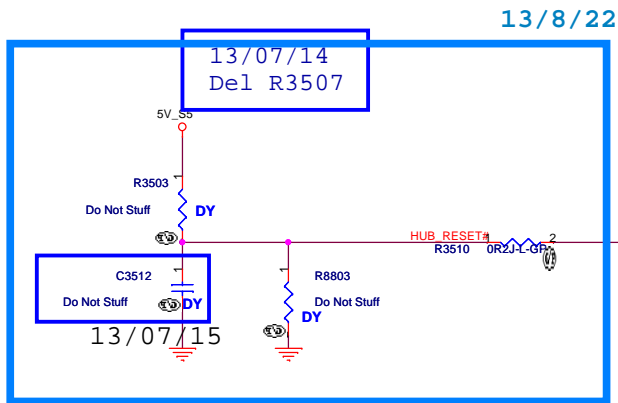
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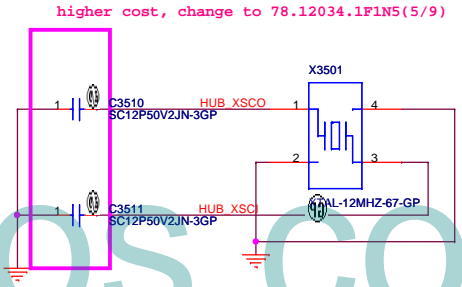
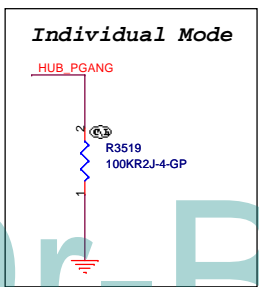
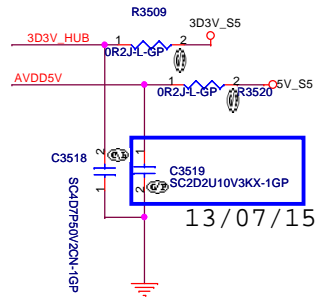
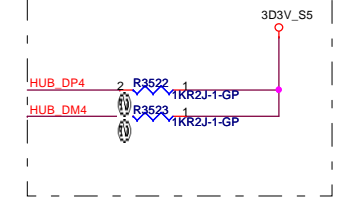
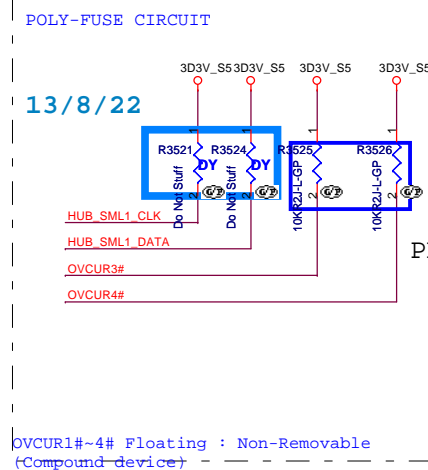
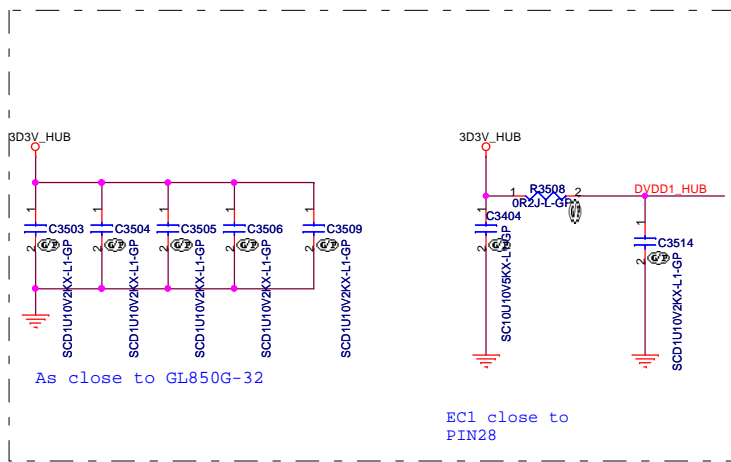
Size A3 Document Number: **EA40 BM** Rev: **-1**

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**USB Table**

Pair	Device
1	WLAN(Bluetooth)
2	CCD
3	USB 2.0
4	



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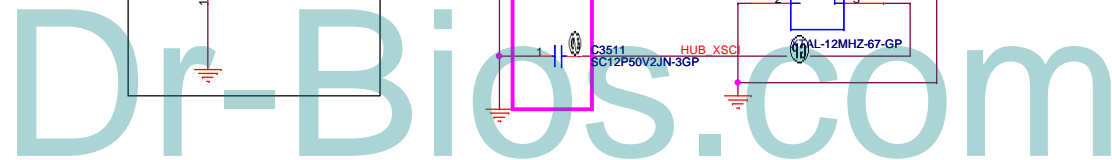
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Title: **USB HUB**

Size	Document Number	Rev
Custom	<b>EA40 BM</b>	-1

Date: Tuesday, November 19, 2013 Sheet 35 of 102



# Power Sequence

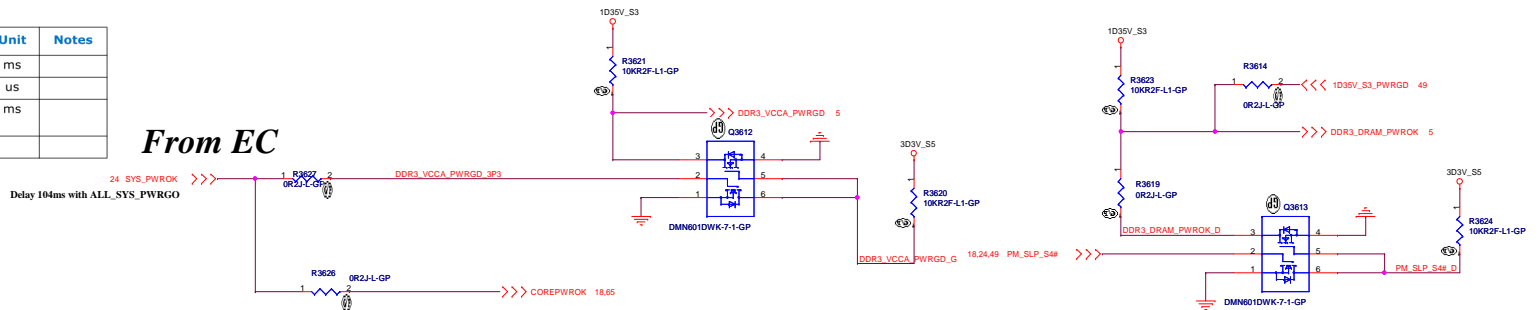
Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWRCK and PMC_CORE_PWRCK assertion	100		ms	
T3					

## DDR3\_VCCA\_PWRGD

## DDR3\_DRAM\_PWRCK

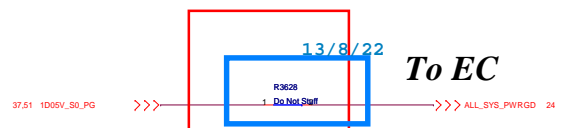
From EC



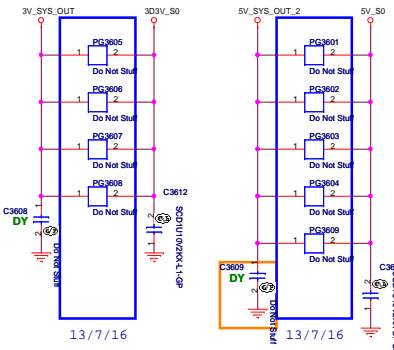
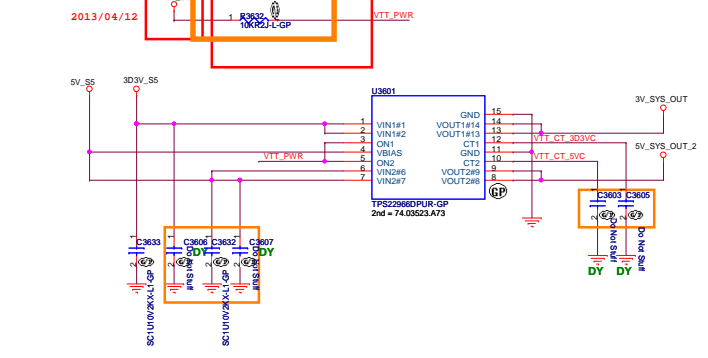
## ALL\_SYS\_PWRGD

## COREPWRCK

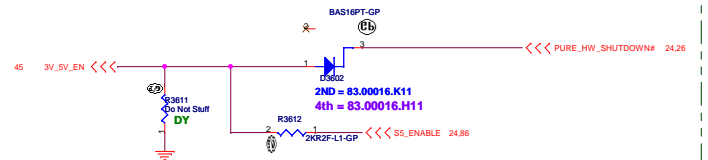
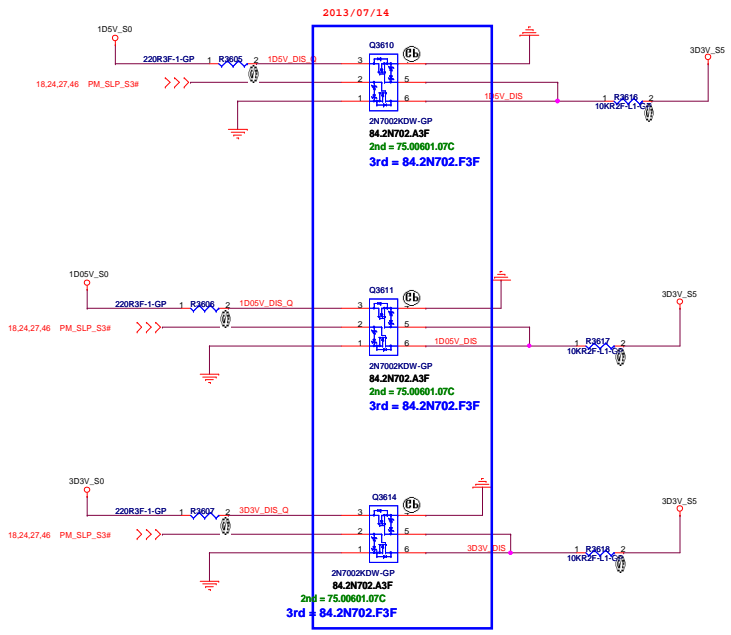
To EC



## ANNIE Run Power



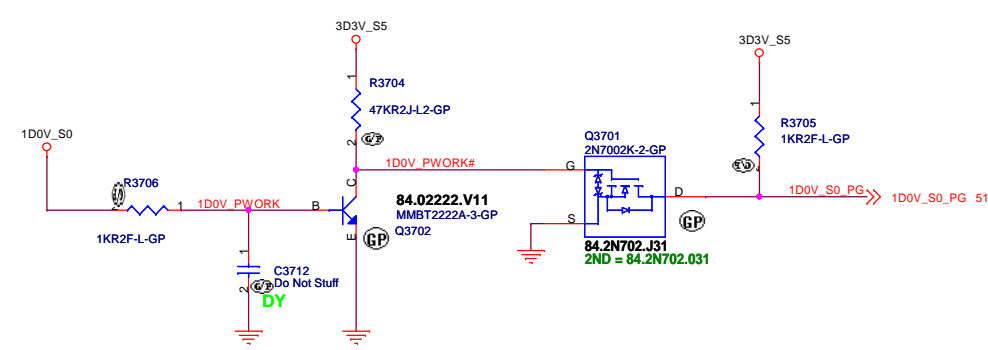
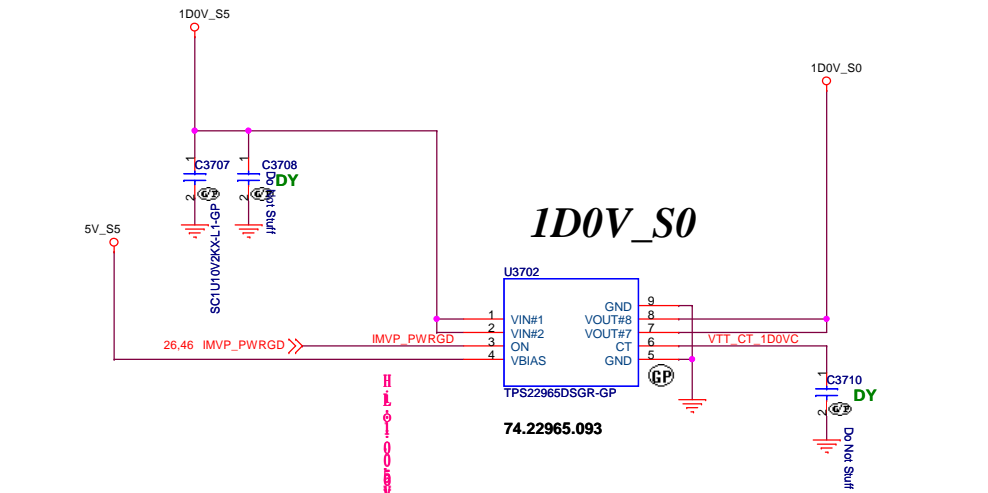
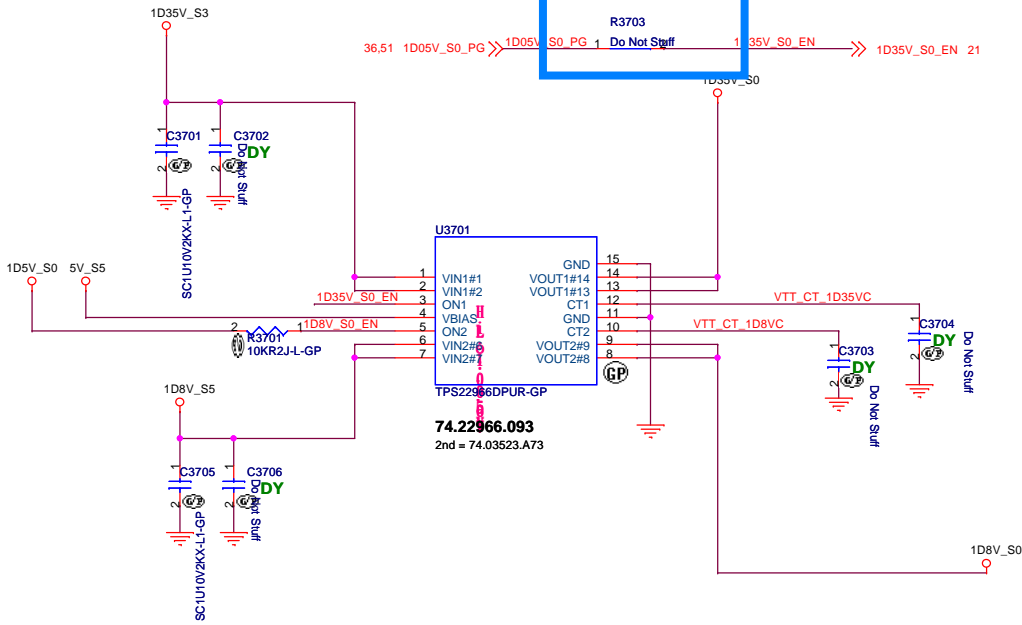
## Discharge circuit



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1D35V\_S0  
1D8V\_S0

13/8/22



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Title	ADAPTER OCP / S3 reduction	
Size	Document Number	Rev
A3	EA40 BM	-1
Date:	Tuesday, November 19, 2013	Sheet 37 of 102

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Title		<b>Reserved</b>	
Size	Document Number	Rev	
A4	<b>EA40 BM</b>	<b>-1</b>	
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Title

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Size  
A4

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**EA40 BM**

Rev  
**-1**

Date: Tuesday, November 19, 2013

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Title		<b>Reserved</b>	
Size	Document Number	Rev	
A4	<b>EA40 BM</b>	<b>-1</b>	
Date:	Tuesday, November 19, 2013	Sheet	40 of 102

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緯創資通

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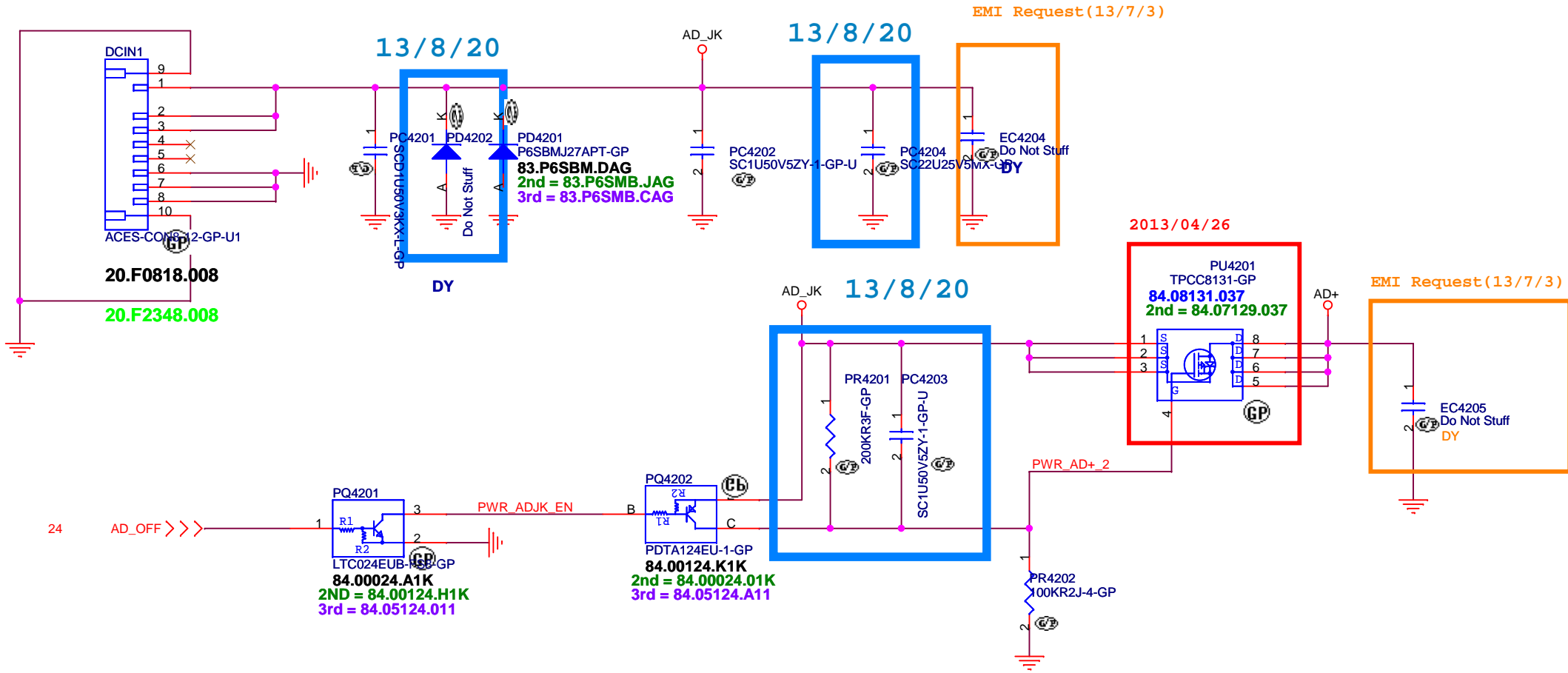
Title **Reserved**

Size A4	Document Number <b>EA40 BM</b>	Rev <b>-1</b>
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Adaptor in to generate DCBATOUT



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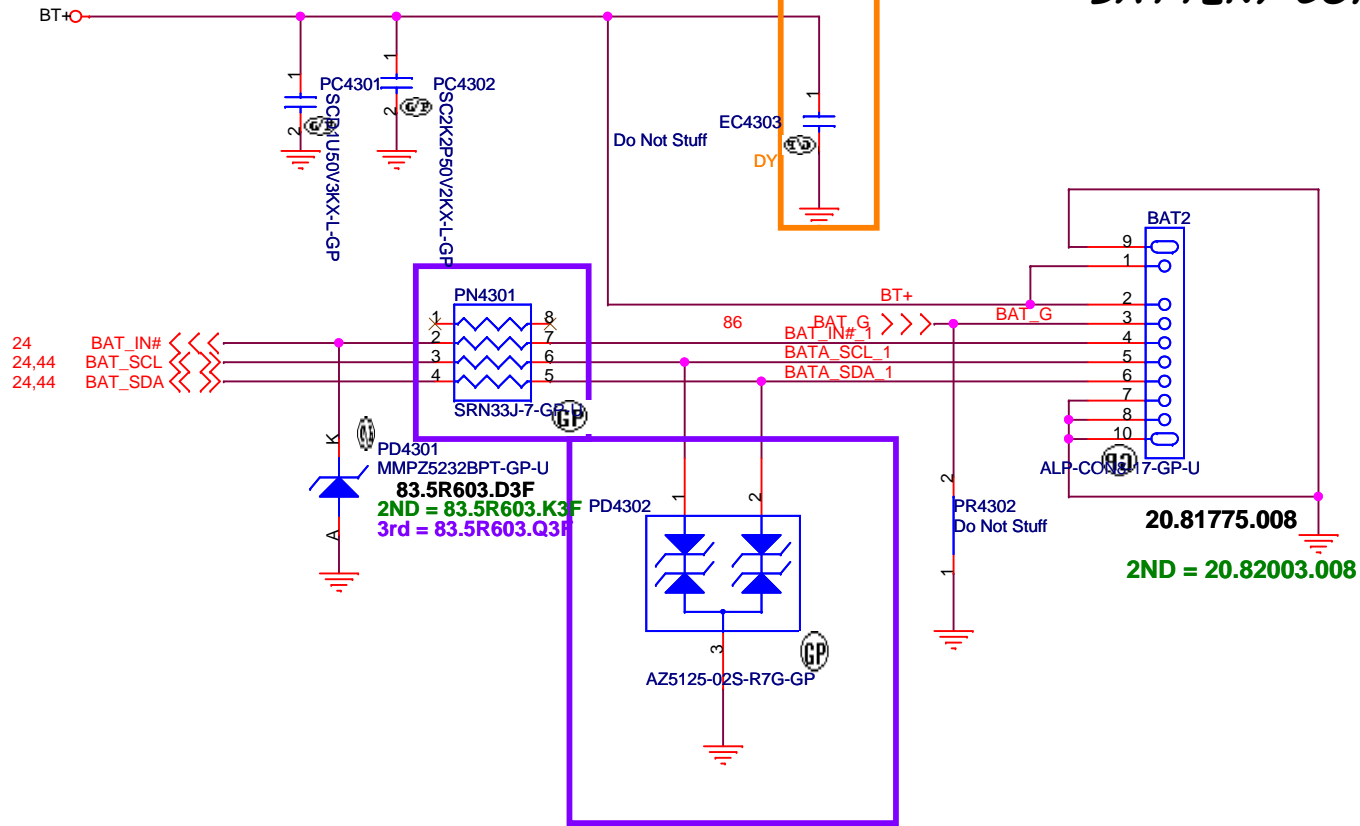
N15M UMA TOUCH 1DIMM

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>DCIN JACK</b>			
Title		EA40 BM	
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# BATTERY CONNECTOR

For EMI request



24 BAT\_IN#  
24,44 BAT\_SCL  
24,44 BAT\_SDA


86 BAT\_IN#\_1  
86 BATA\_SCL\_1  
86 BATA\_SDA\_1

86 BAT\_IN#\_1  
86 BATA\_SCL\_1  
86 BATA\_SDA\_1

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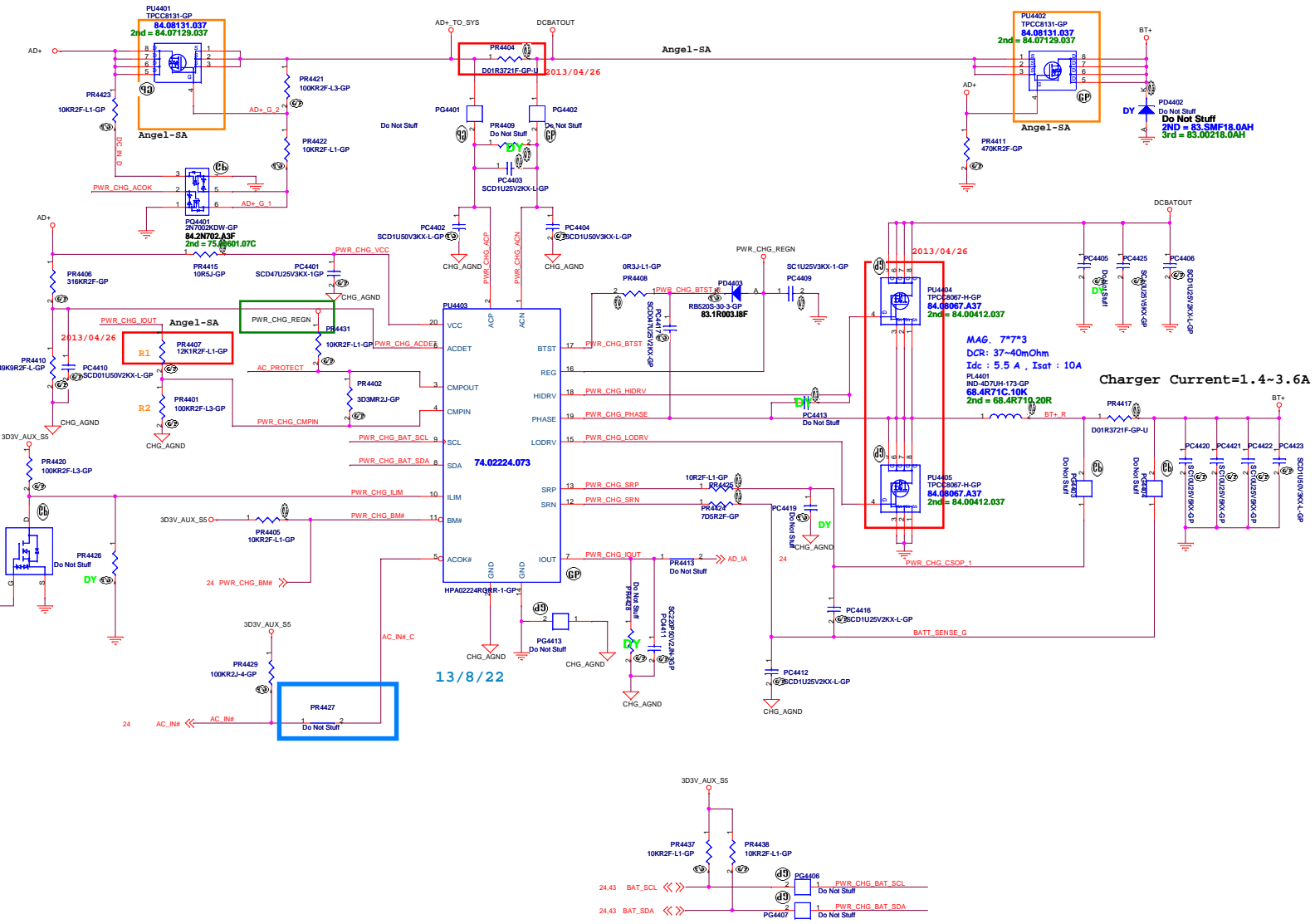
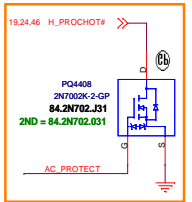
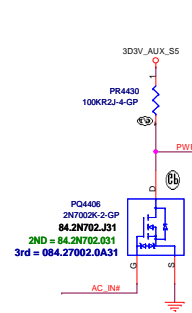
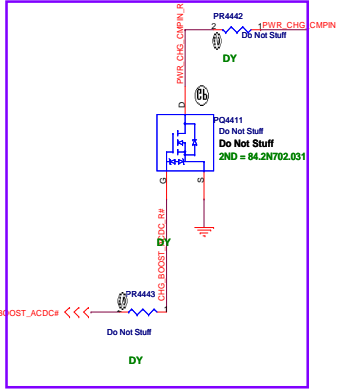
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>BATT CONN</b>			
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SSID = Charger

SSID = Charger

AD+ total power	R1	R2
65w	1.2.1K	100K

change the table



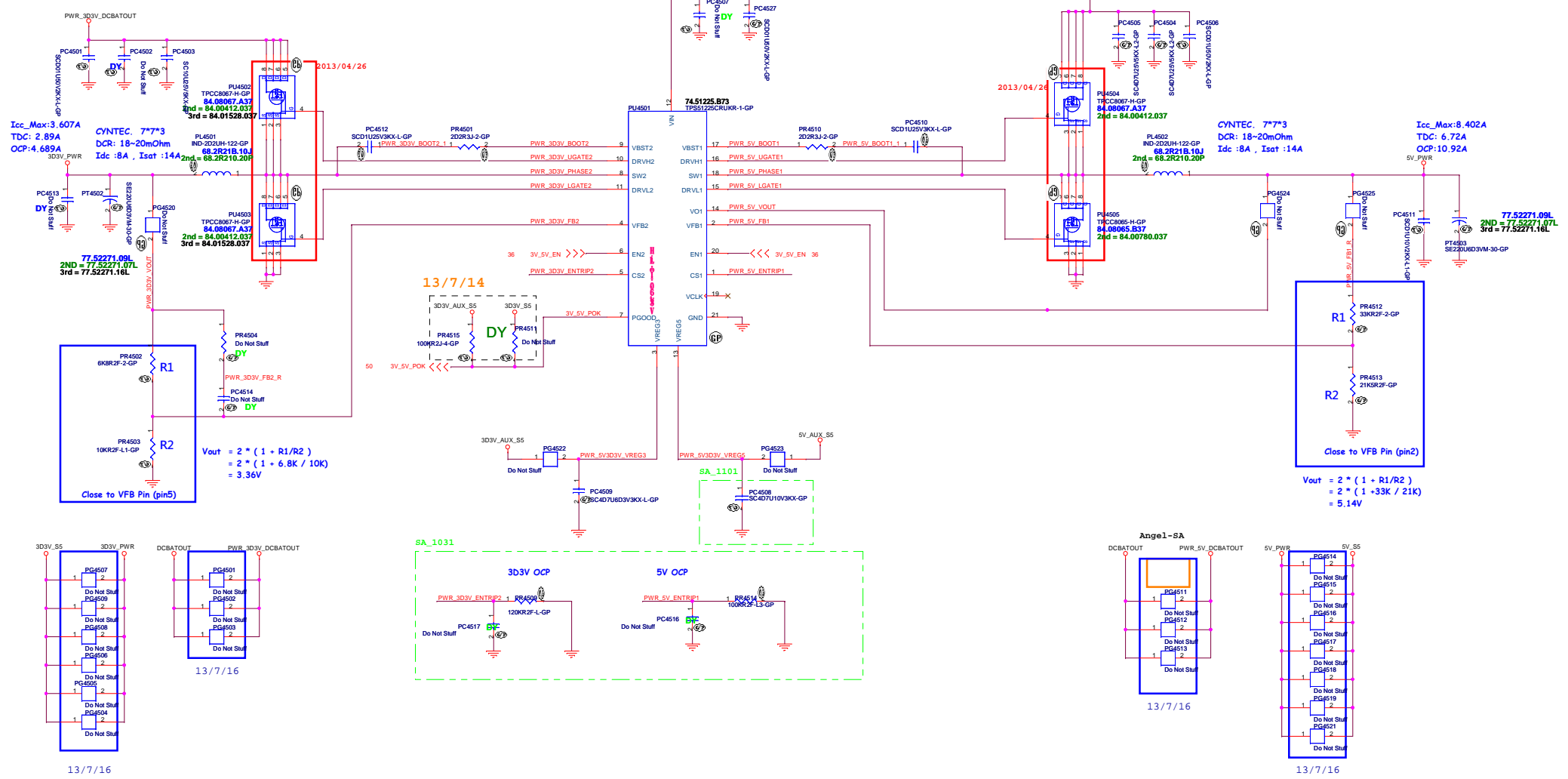
Charger Current=1.4~3.6A

MAG: 7\*7\*3  
 DCR: 37~40mOhm  
 I<sub>dc</sub>: 5.5 A, I<sub>sat</sub>: 10A

13/8/22

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**TPS51225 for 5V\_S5 and 3D3V\_S5**  
**Enable=1.6V**  
**Disable=0.3V**



Icc\_Max: 3.607A  
 TDC: 2.89A  
 OCP: 4.689A

77.52271.09L  
 2ND = 77.52271.07L  
 3rd = 77.52271.16L

$$V_{out} = 2 * (1 + R1/R2)$$

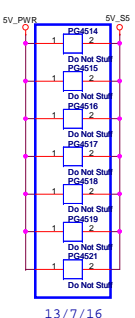
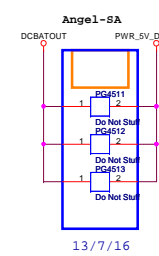
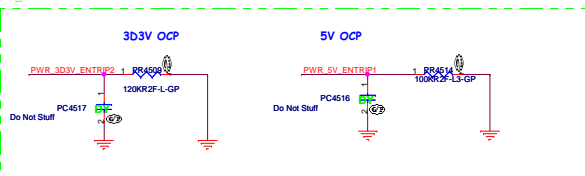
$$= 2 * (1 + 6.8K / 10K)$$

$$= 3.36V$$

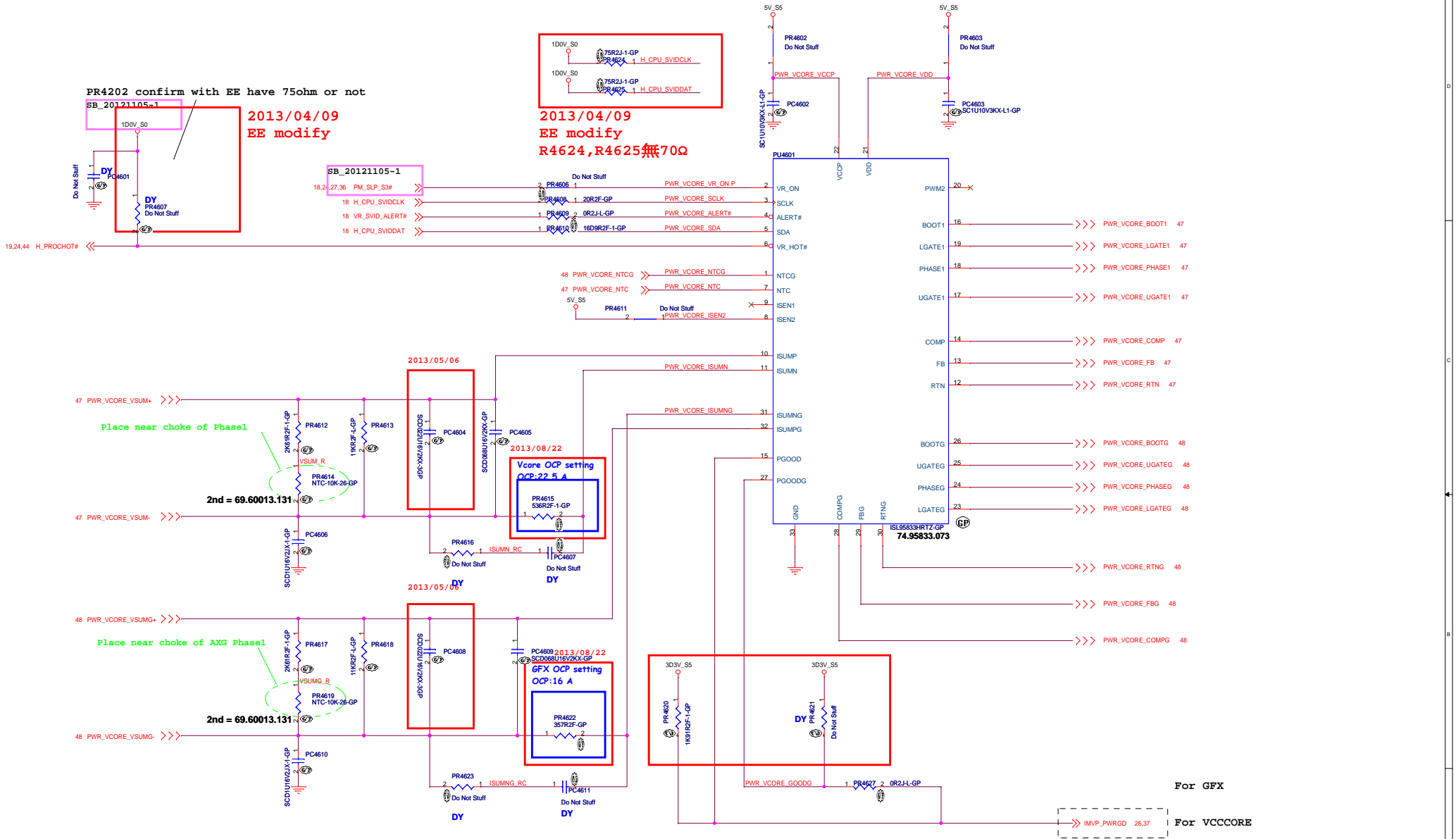
$$V_{out} = 2 * (1 + R1/R2)$$

$$= 2 * (1 + 33K / 21K)$$

$$= 5.14V$$



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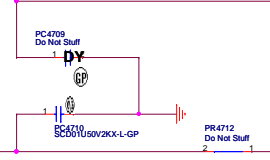
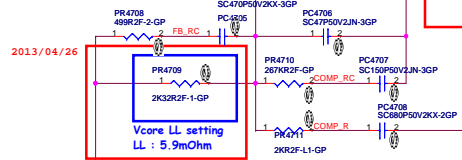
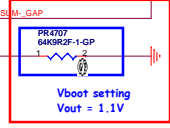
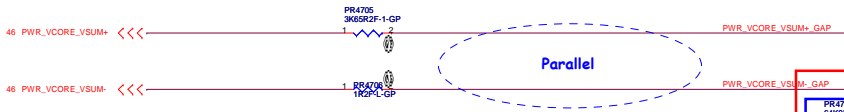
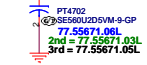
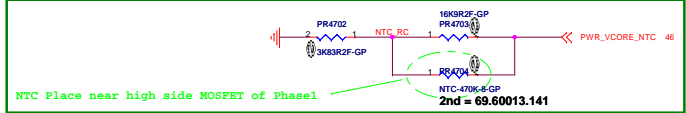
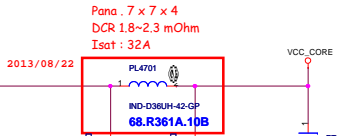
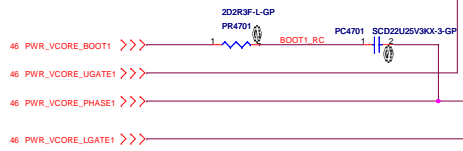
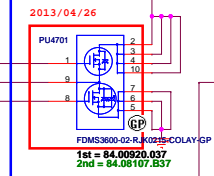


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BOM control

	Main source	2nd source
PU4701	84.03664.037 (FDMS36648)	Mount
PU4302	84.03664.037 (FDMS36648)	DY

BOM control

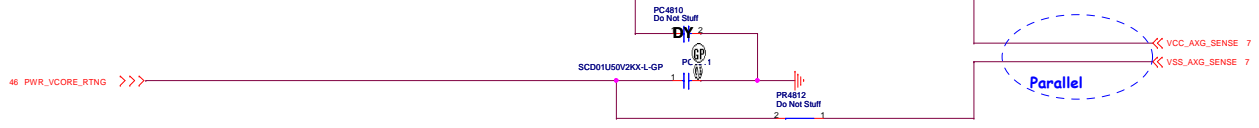
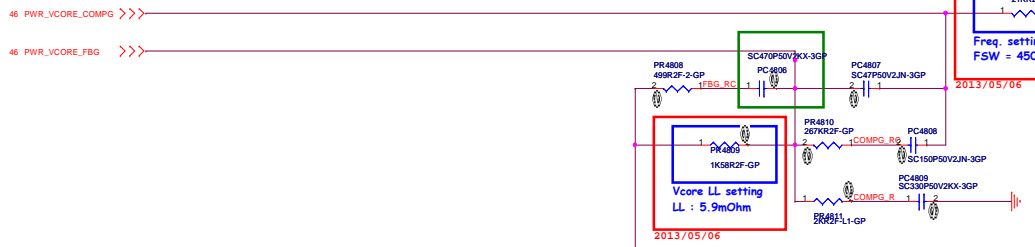
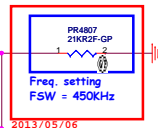
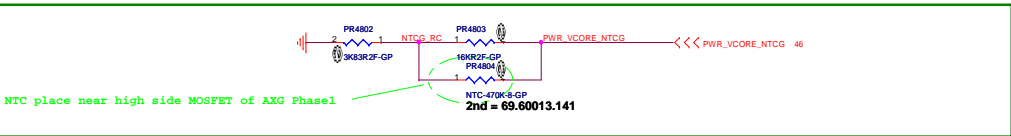
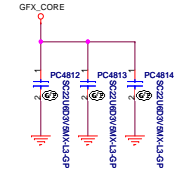
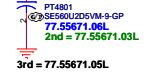
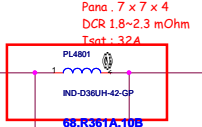
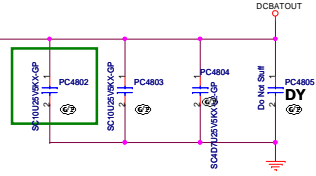
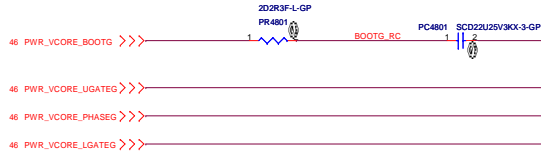
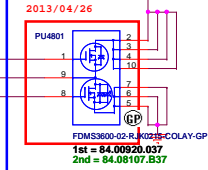


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BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S)	Mount
PU4402	84.03664.037 (FDMS3664S)	DY

BOM control

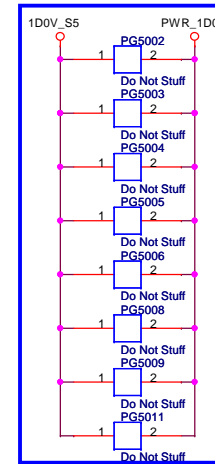
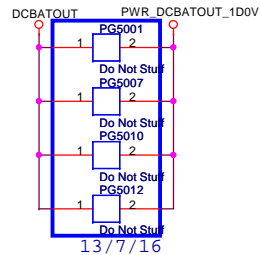


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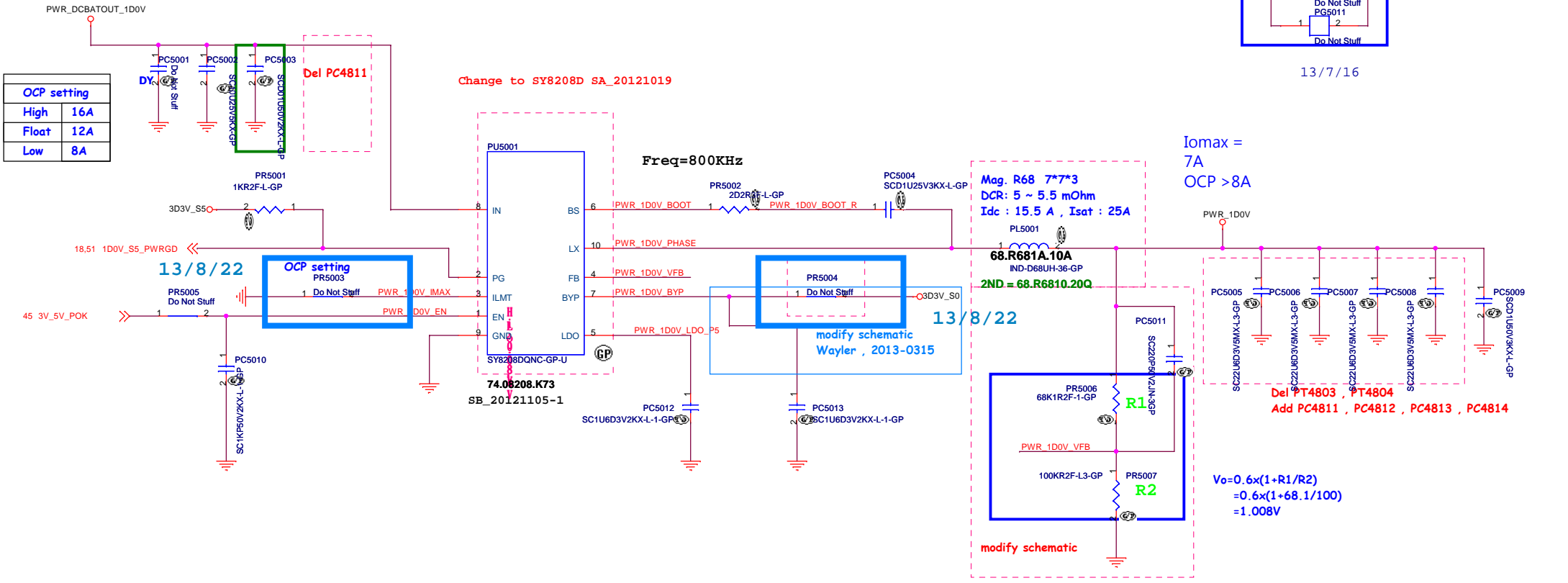




**SY8208D for 1D0V\_S5**  
**Enable=0.8V**  
**Disable=0.4V**



OCV setting	
High	16A
Float	12A
Low	8A



Iomax = 7A  
 OCP > 8A

$$V_o = 0.6 \times (1 + R1/R2)$$

$$= 0.6 \times (1 + 68.1/100)$$

$$= 1.008V$$

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Title: **DC to DC 1D05V(SY8208D)**

Size A3	Document Number <b>EA40 BM</b>	Rev <b>-1</b>
Date: Tuesday, November 19, 2013	Sheet 50 of 102	

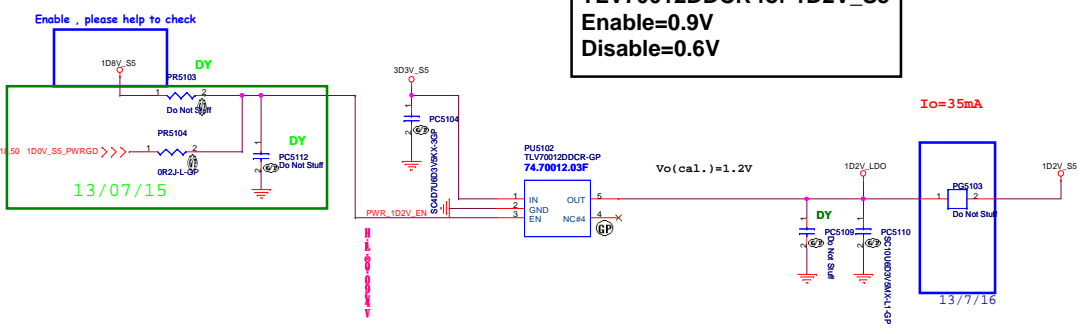
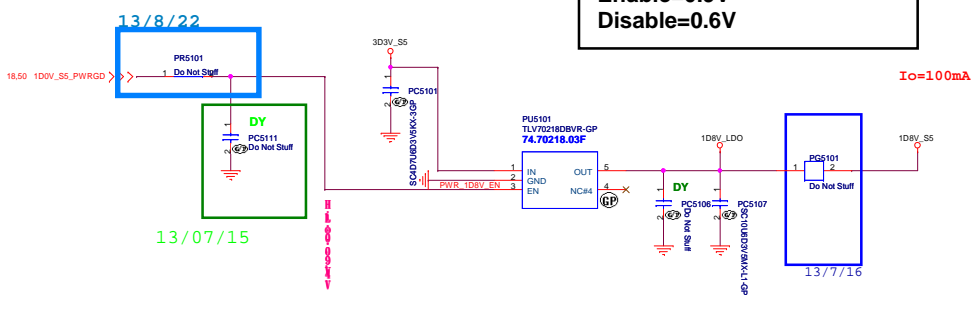
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SSID = PWR.Plane.Regulator\_1p8v

2013/04/18

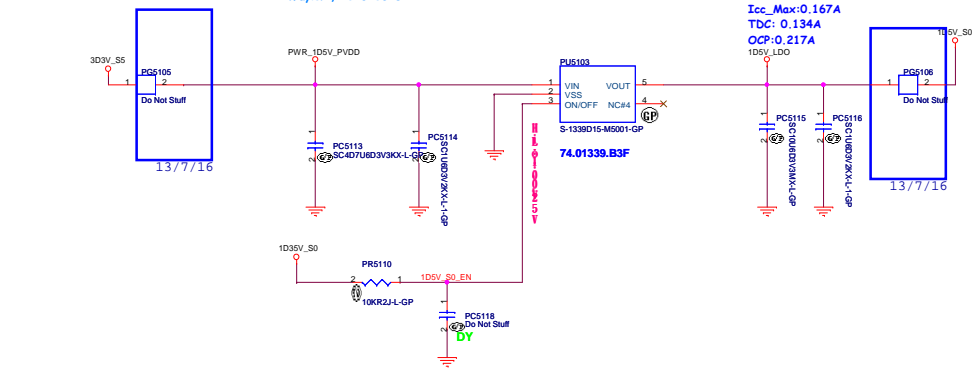
TLV70218DBVR for 1D8V\_S5  
Enable=0.9V  
Disable=0.6V

TLV70012DDCR for 1D2V\_S5  
Enable=0.9V  
Disable=0.6V



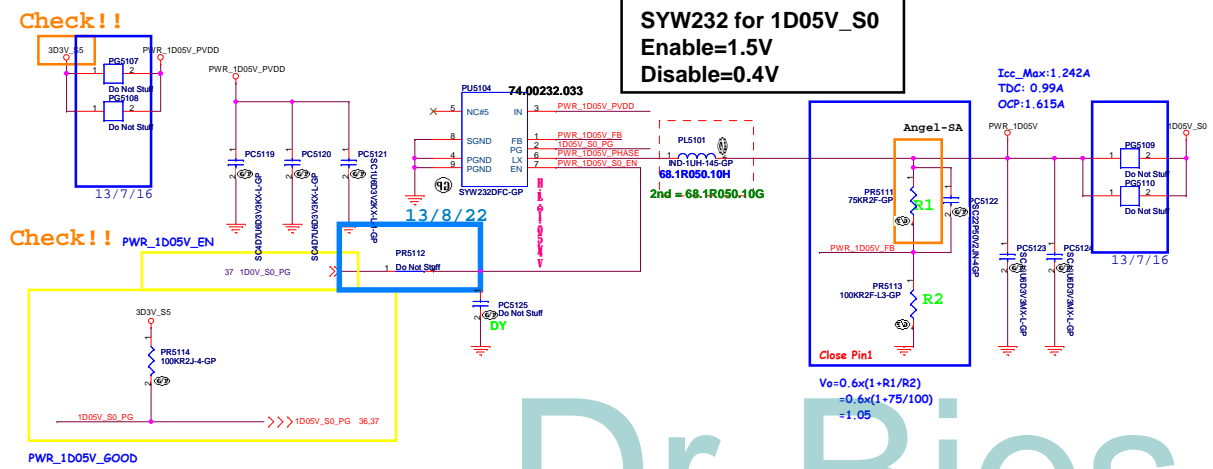
S-1339D15 for 1D5V\_S0  
Enable=1.0V  
Disable=0.25V

modify schematic  
Wayler, 2013-0315

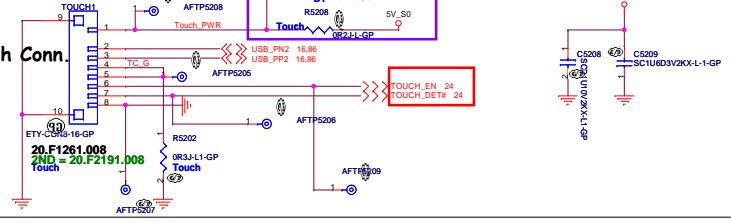
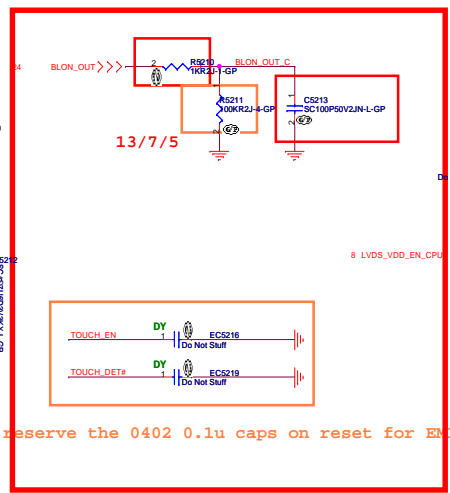
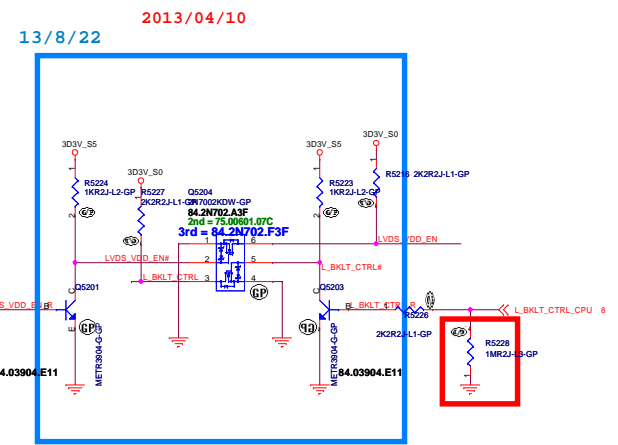
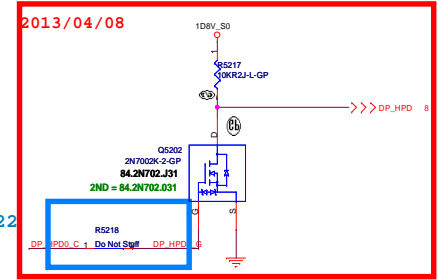
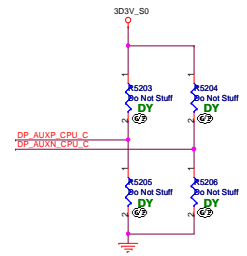
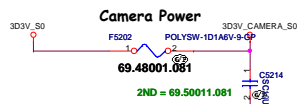
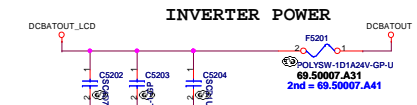
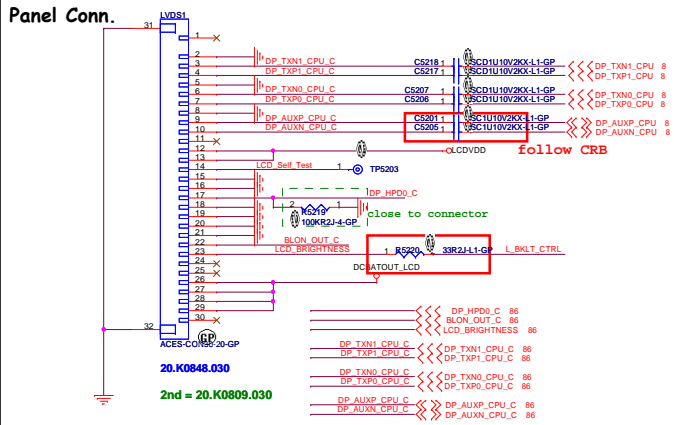


SYW232 for 1D05V\_S0  
Enable=1.5V  
Disable=0.4V

Icc\_Max: 1.242A  
TDC: 0.99A  
OCP: 1.615A



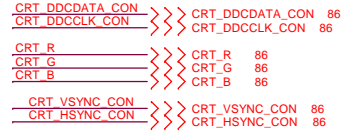
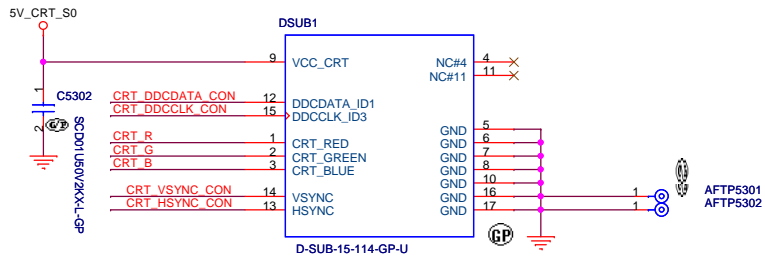
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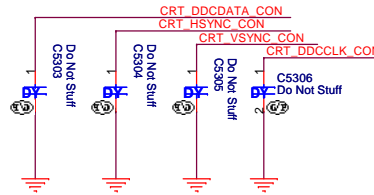
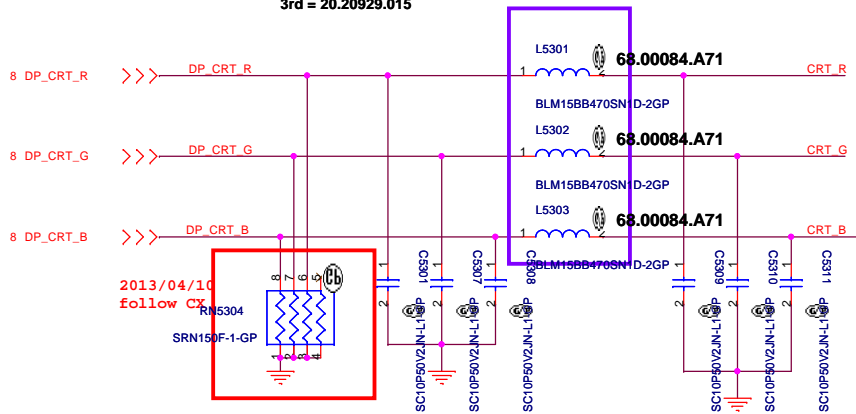
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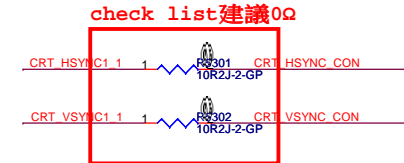
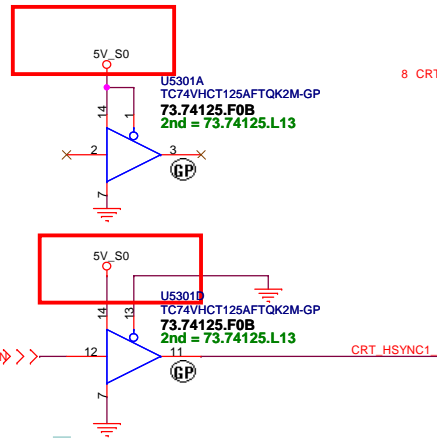
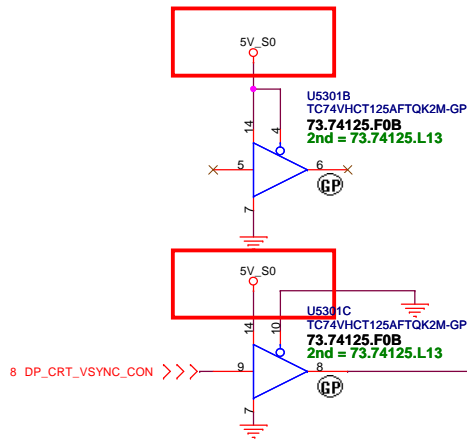
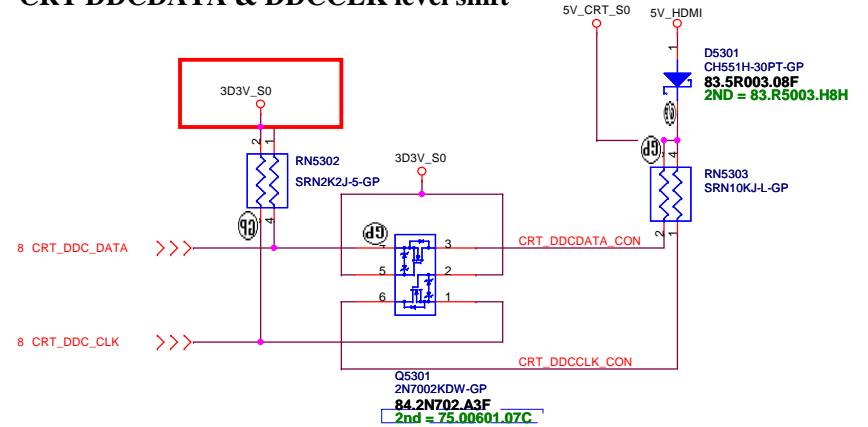
File	LCD Connector		Rev
Size	Document Number		-1
Custom	EA40 BM		
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20.21077.015  
2nd = 20.20492.015  
3rd = 20.20929.015



### CRT DDCDATA & DDCCLK level shift



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Title <b>CRT Connector</b>		
Size A3	Document Number <b>EA40 BM</b>	Rev <b>-1</b>
Date Wednesday, November 20, 2013	Sheet 53	of 102

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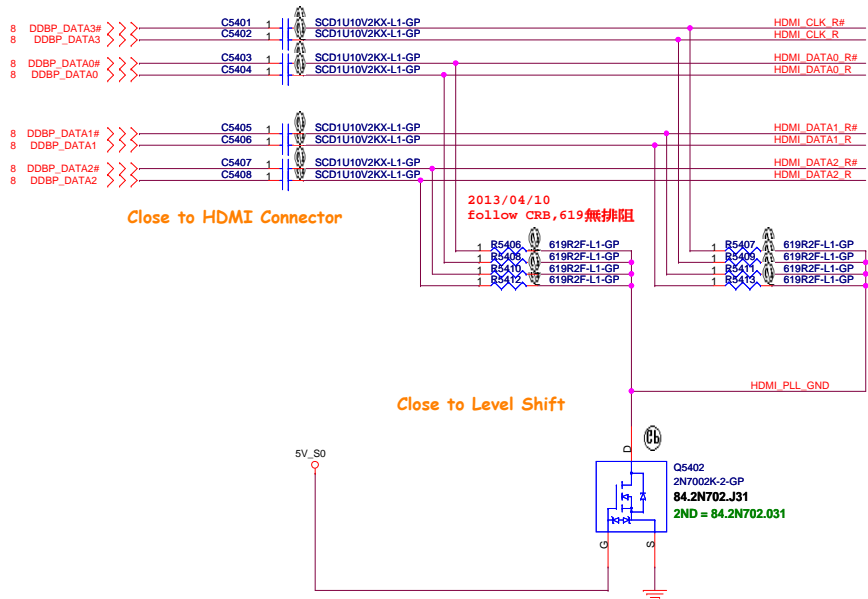
SSID = VIDEO

# HDMI Level Shifter & CONNECTOR

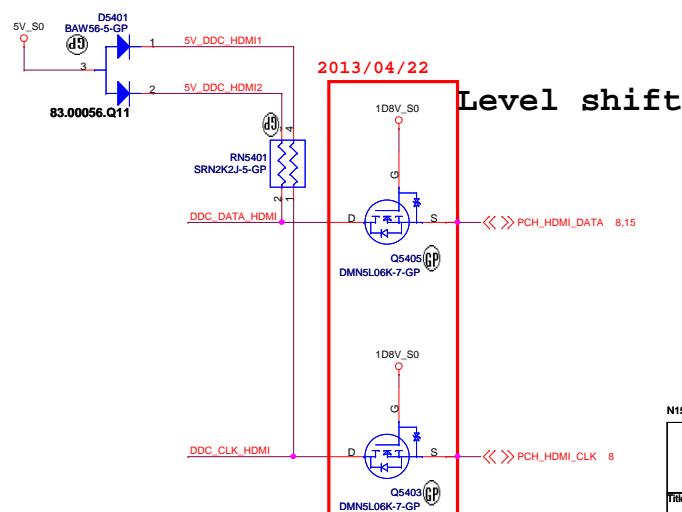
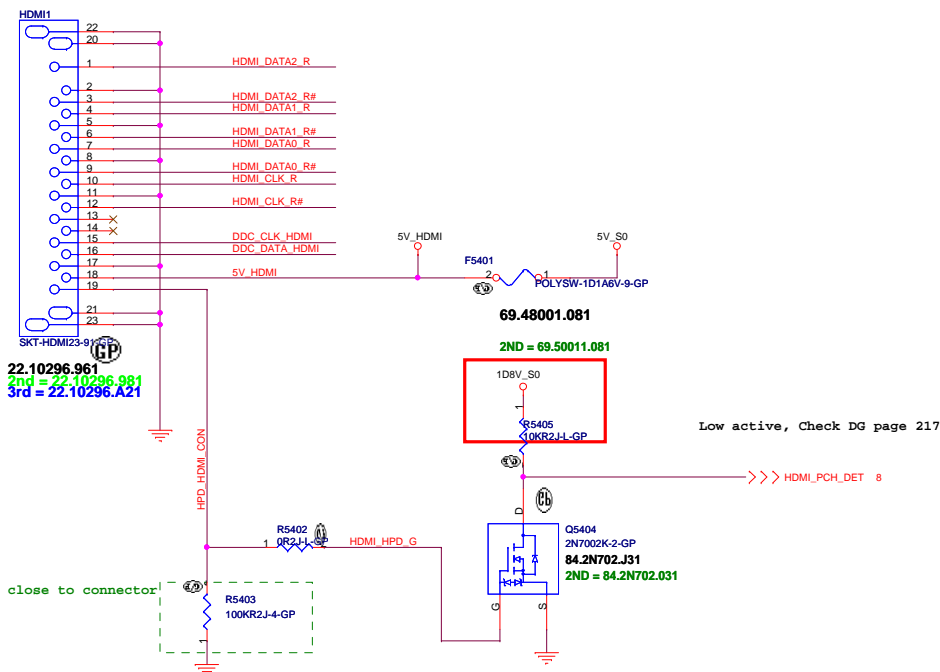
UMA\_Muxless : default setting used PS8101. if don't used PS8101 please change C5103-C5110 to 0 ohm resistor

HDMI_CLK_R#	1	R5417	150R2F-4-L-GP	HDMI_CLK_R
HDMI_DATA0_R#	1	R5414	150R2F-4-L-GP	HDMI_DATA0_R
HDMI_DATA1_R#	1	R5415	150R2F-4-L-GP	HDMI_DATA1_R
HDMI_DATA2_R#	1	R5416	150R2F-4-L-GP	HDMI_DATA2_R

Reserve 150 ohm bridge resistance on the HDMI trace as circle for EMI(5/9).



## HDMI CONN



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<b>HDMI Level Shifter/Connector</b>			
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SSID = Display Port

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Title

**Reserved**

Size

A4

Document Number

**EA40 BM**

Rev

**-1**

Date: Tuesday, November 19, 2013

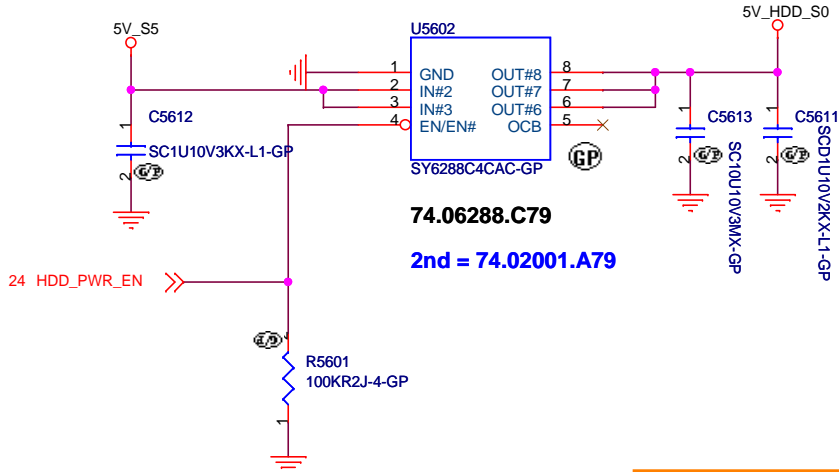
Sheet 55 of

102

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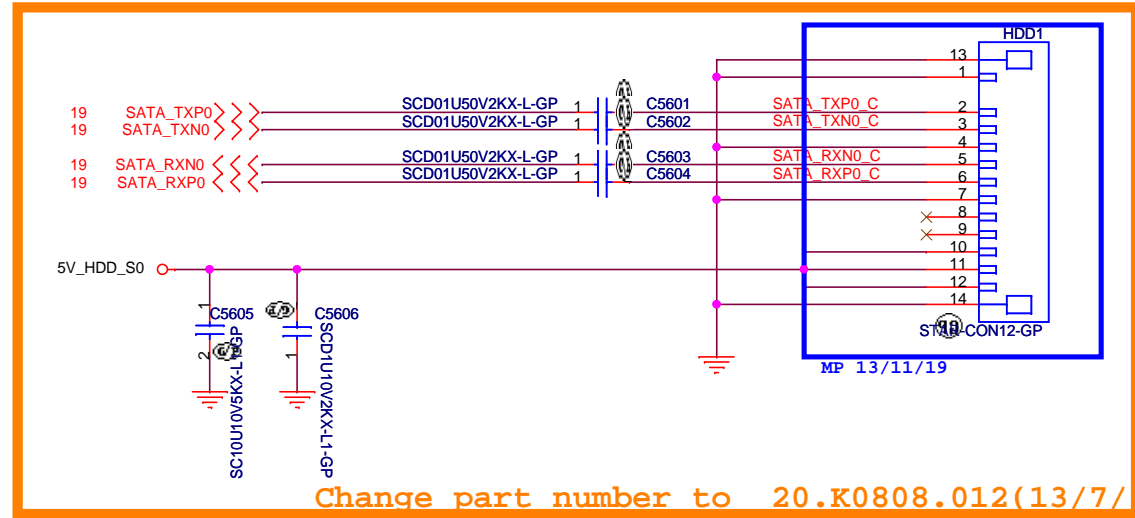
SSID = SATA

# SATA HDD Connector



74.06288.C79

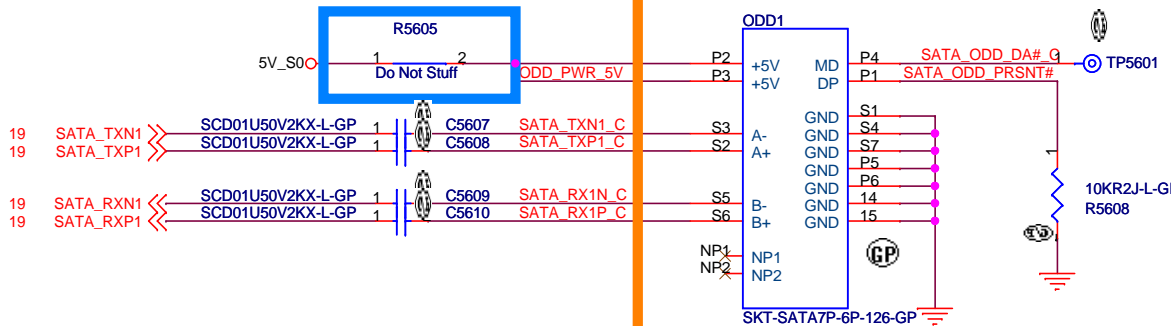
2nd = 74.02001.A79



Change part number to 20.K0808.012(13/7/8)

AC coupling caps near connector < 100 mils

## ODD Connector 13/8/22



13/07/08

22.10300.I31

2nd = 22.10300.H91

3rd = 22.10300.J41

EMI request (7/8)

Delete 12/7/14

EMI request (5/13)

Delete 12/7/14

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HDD Connector	
Size	Document Number
Custom	EA40 BM
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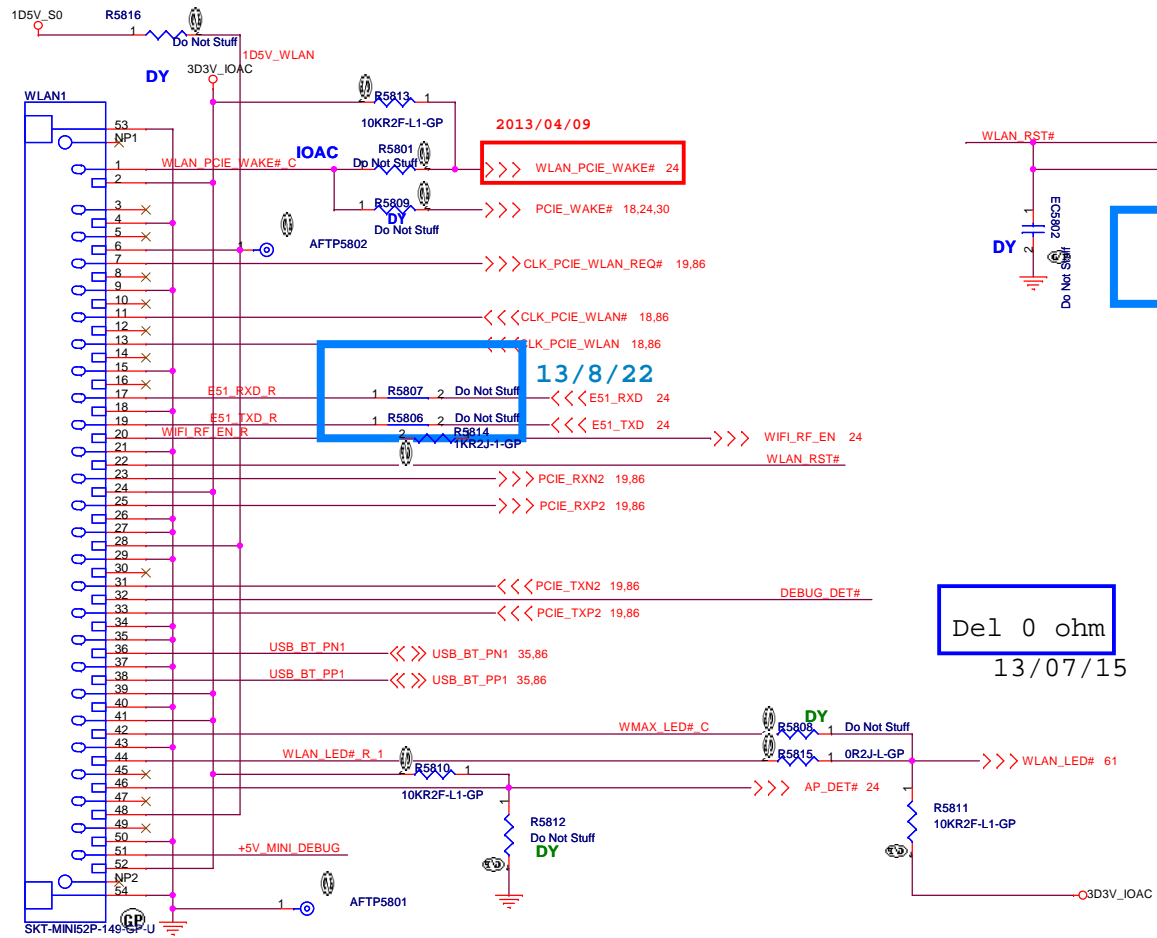
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A4	<b>EA40 BM</b>	<b>-1</b>
Date:	Tuesday, November 19, 2013	Sheet 57 of 102

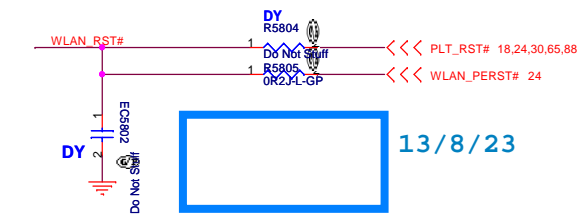
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# SSID = Wireless Mini Card Connector(802.11a/b/g/n)

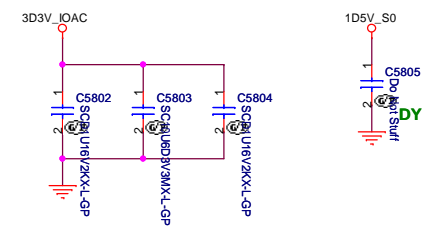
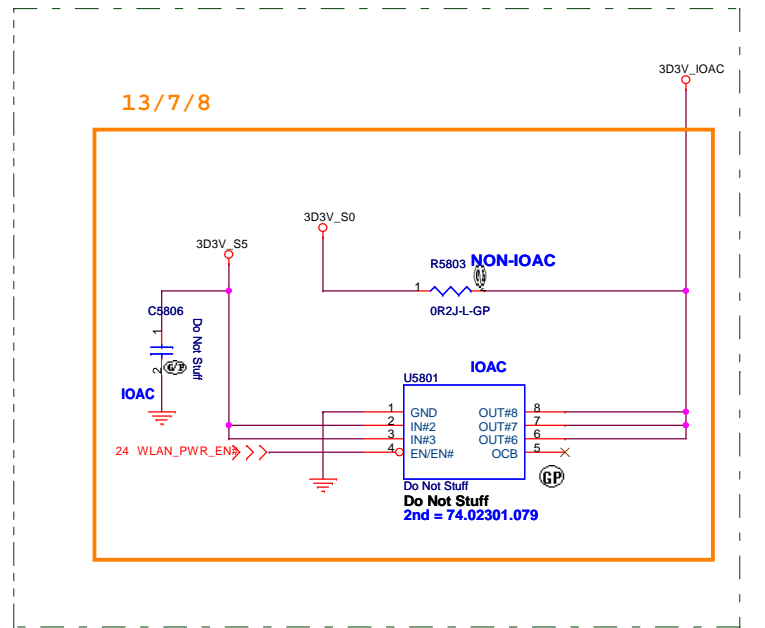
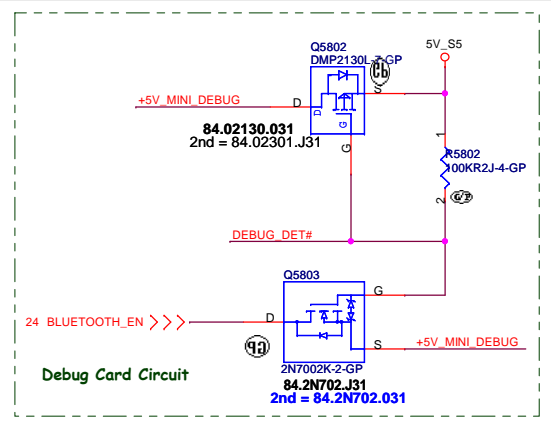
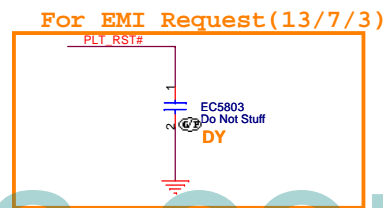
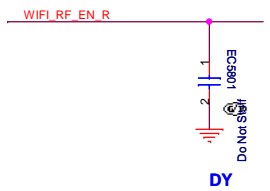


62.10043.I31  
 2nd = 62.10043.I51  
 3rd = 62.10043.K81

- WLAN\_PCIE\_WAKE# C >>> WLAN\_PCIE\_WAKE#\_C 86
- E51\_RXD\_R >>> E51\_RXD\_R 86
- E51\_TXD\_R >>> E51\_TXD\_R 86
- WLAN\_RST# >>> WLAN\_RST# 86
- DEBUG\_DET# >>> DEBUG\_DET# 86
- USB\_BT\_PN1 >>> USB\_BT\_PN1 35,86
- USB\_BT\_PP1 >>> USB\_BT\_PP1 35,86
- +5V\_MINI\_DEBUG >>> +5V\_MINI\_DEBUG 86
  
- WMAX\_LED# C >>> WMAX\_LED#\_C 86
- WLAN\_LED#\_R\_1 >>> WLAN\_LED#\_R\_1 86
  
- WIFI\_RF\_EN\_R >>> WIFI\_RF\_EN\_R 86



Del 0 ohm  
 13/07/15



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SSID = 3G

# Mini Card Connector(WWAN)

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Title			<b>WWAN CONN</b>		
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SSID = mSATA

# Mini Card Connector(mSATA)

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Size

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Document Number

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Rev

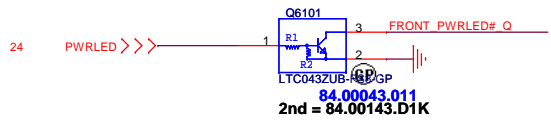
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Date: Tuesday, November 19, 2013

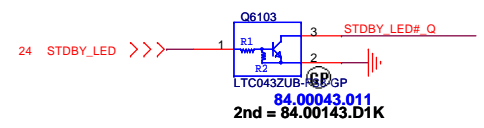
Sheet 60 of 102

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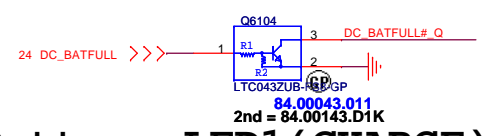
Power button LED



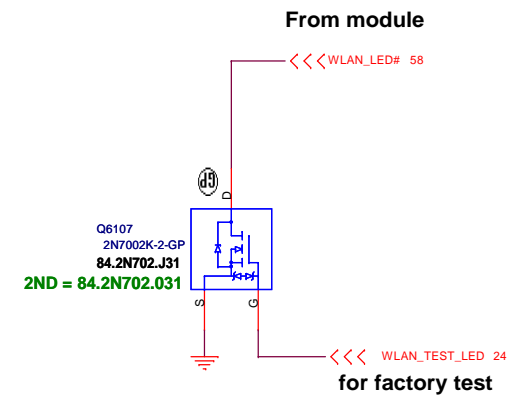
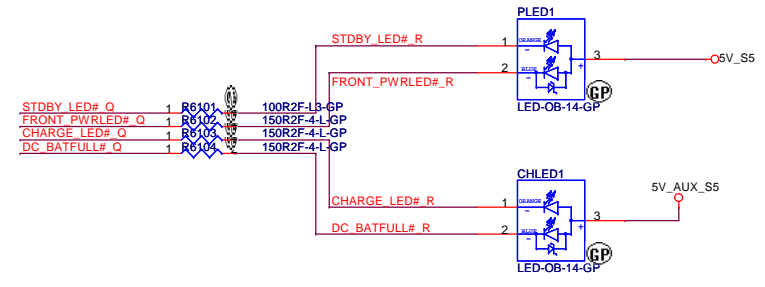
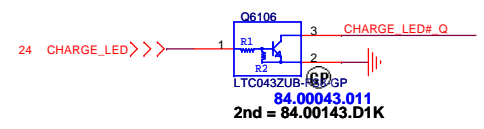
Power STDBY\_LED



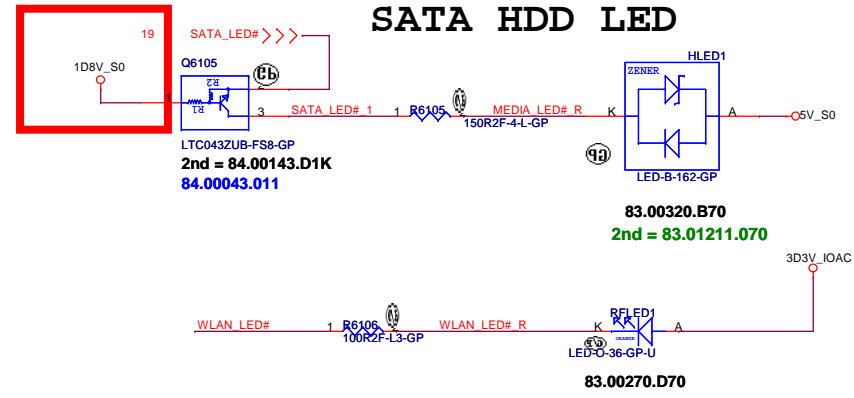
Battery LED2 (DC\_BATFULL)



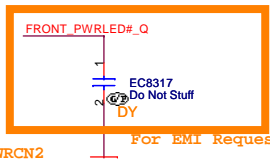
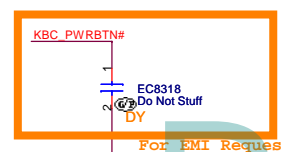
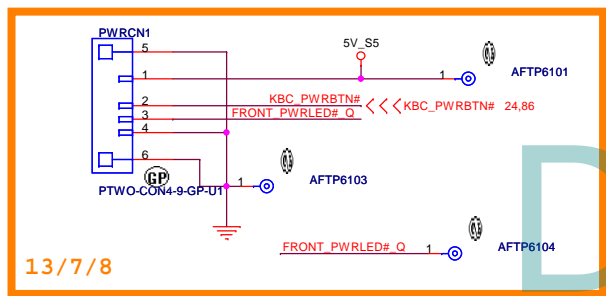
Battery LED1 (CHARGE)



SATA HDD LED



Power button BD



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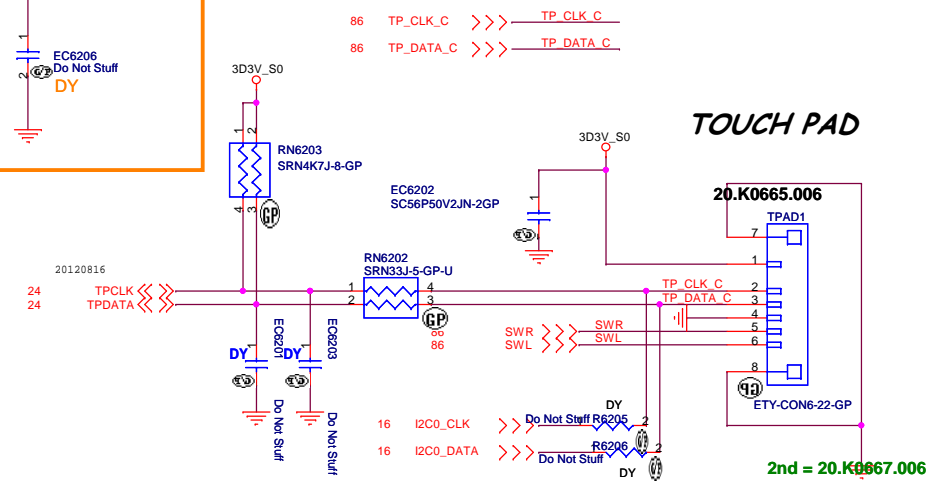
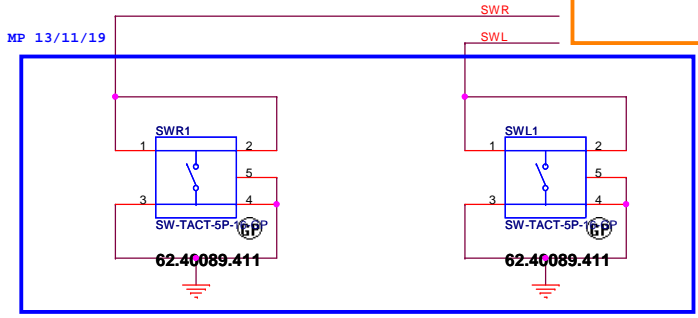
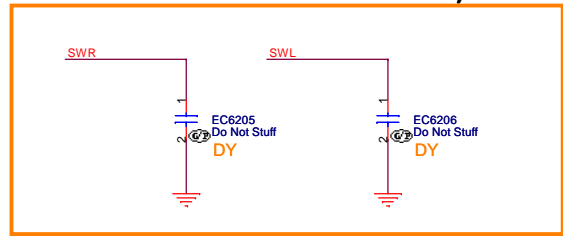
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Title <b>LED Bard/Power Button</b>		
Size A3	Document Number <b>EA40 BM</b>	Rev <b>-1</b>
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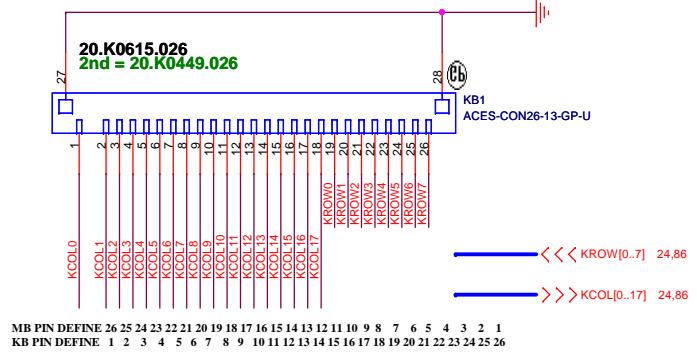
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SSID = KBC

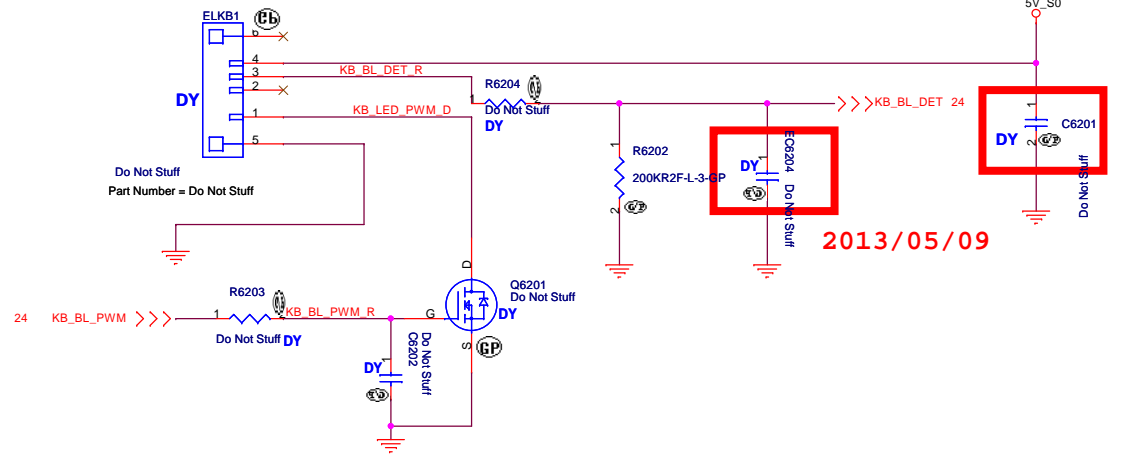
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### Internal Keyboard Connector



### KB Backlight

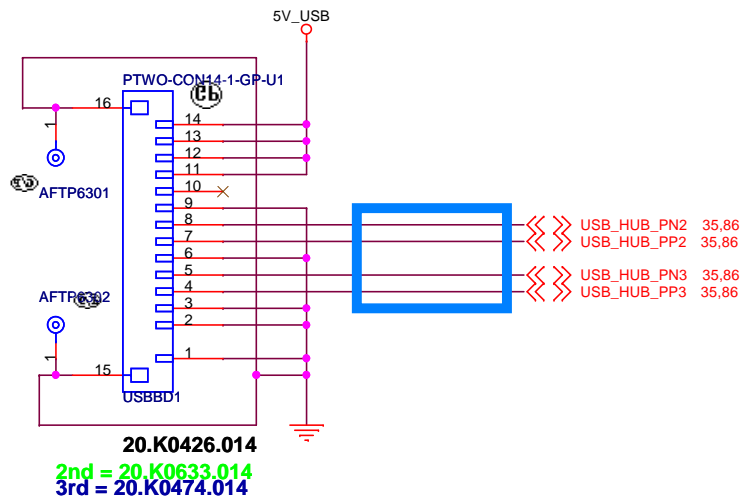
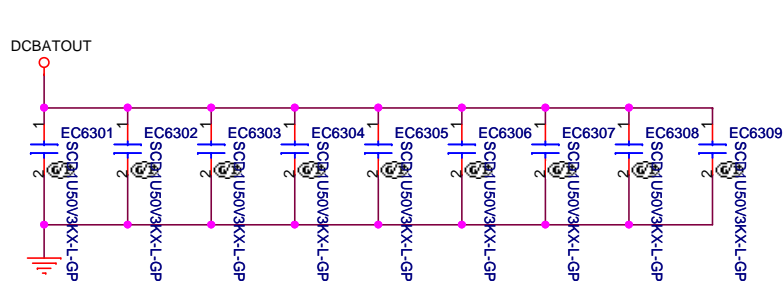


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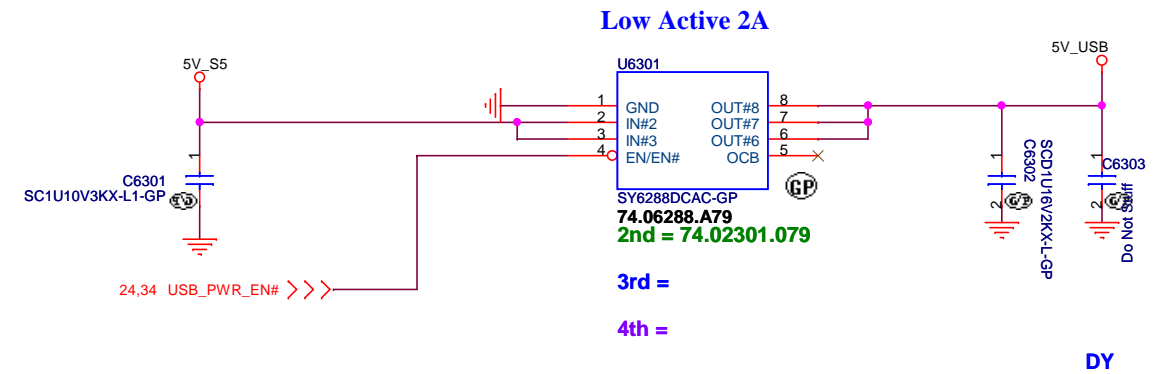
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Title		
Key Board/Touch Pad		
Size A3	Document Number	Rev
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13/8/13

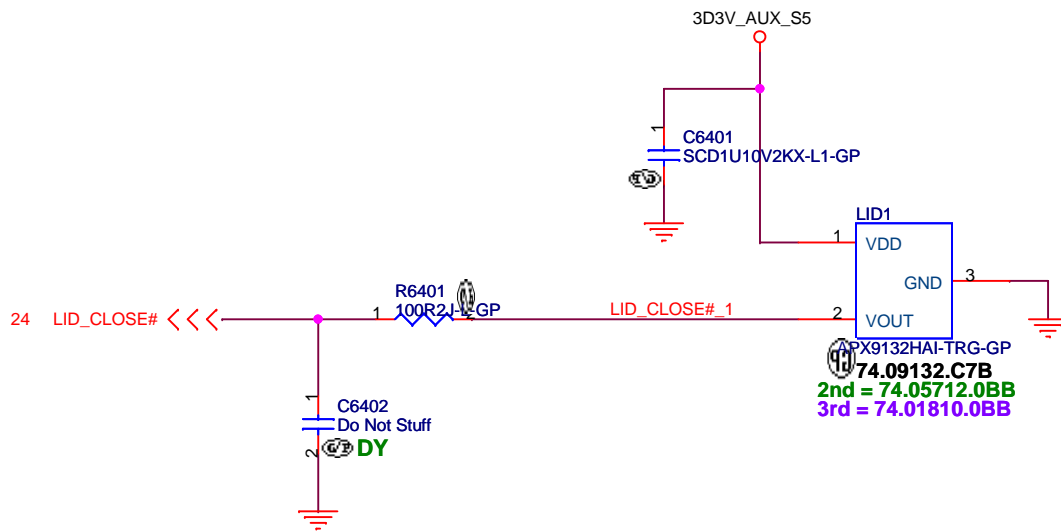


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<b>IO Board Connector</b>			
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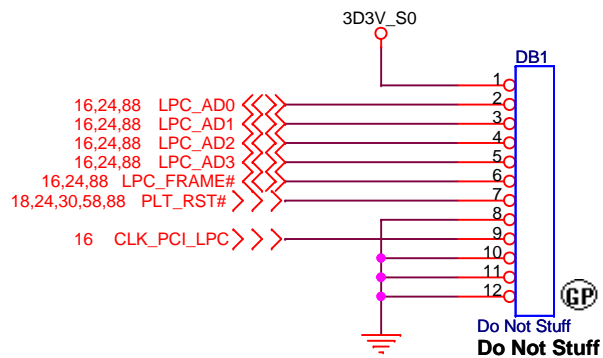
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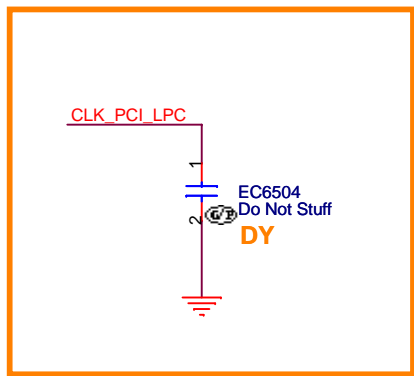
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Size	Document Number	Rev
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Date:	Tuesday, November 19, 2013	Sheet 64 of 102

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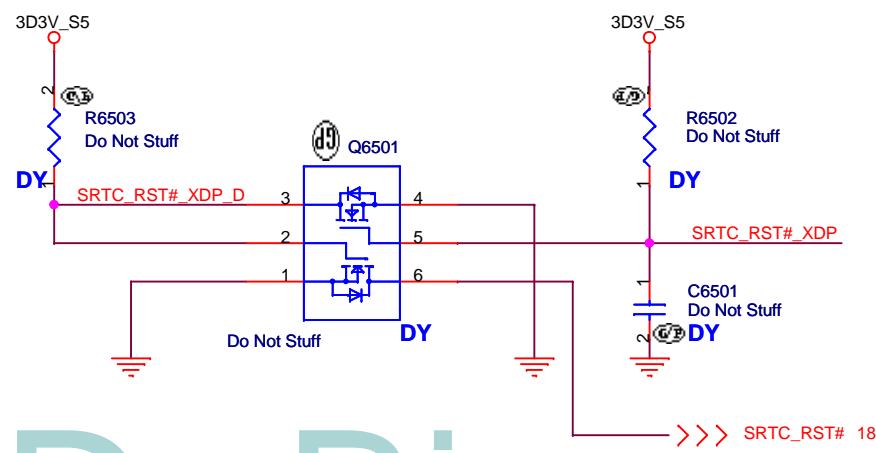
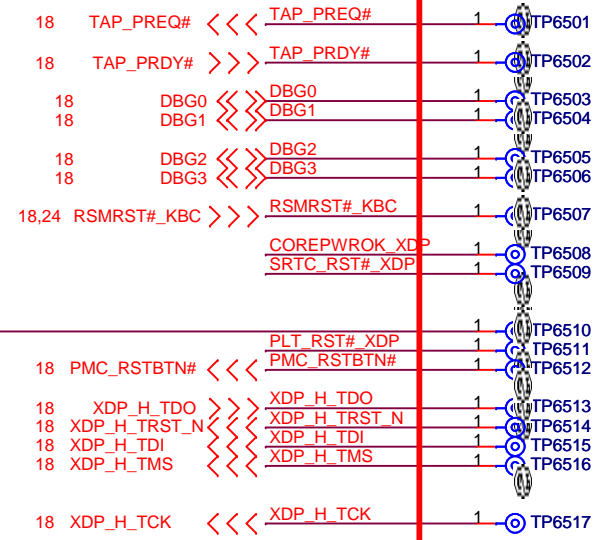
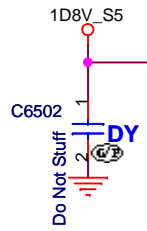
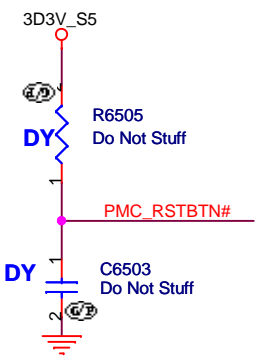
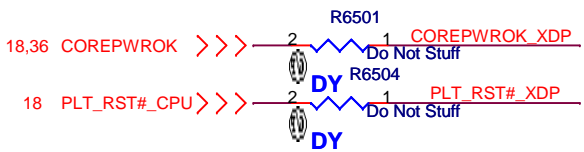




**LAB**



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# Free Fall Sensor

## Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

# Blanking

```
SDO="H"; address="3Ah"  
*SDO="L"; address="38h"
```

```
*CS="H"; mode="I2C"  
CS="L"; mode="SPI"
```

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Title

**G Sensor**

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Title		
<b>Thunderbolt (1/5)</b>		
Size	Document Number	Rev
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Title

**Thunderbolt (2/5)**

Size

A4

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Title			
<b>Thunderbolt (3/5)</b>			
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<b>Thunderbolt (4/5)</b>		
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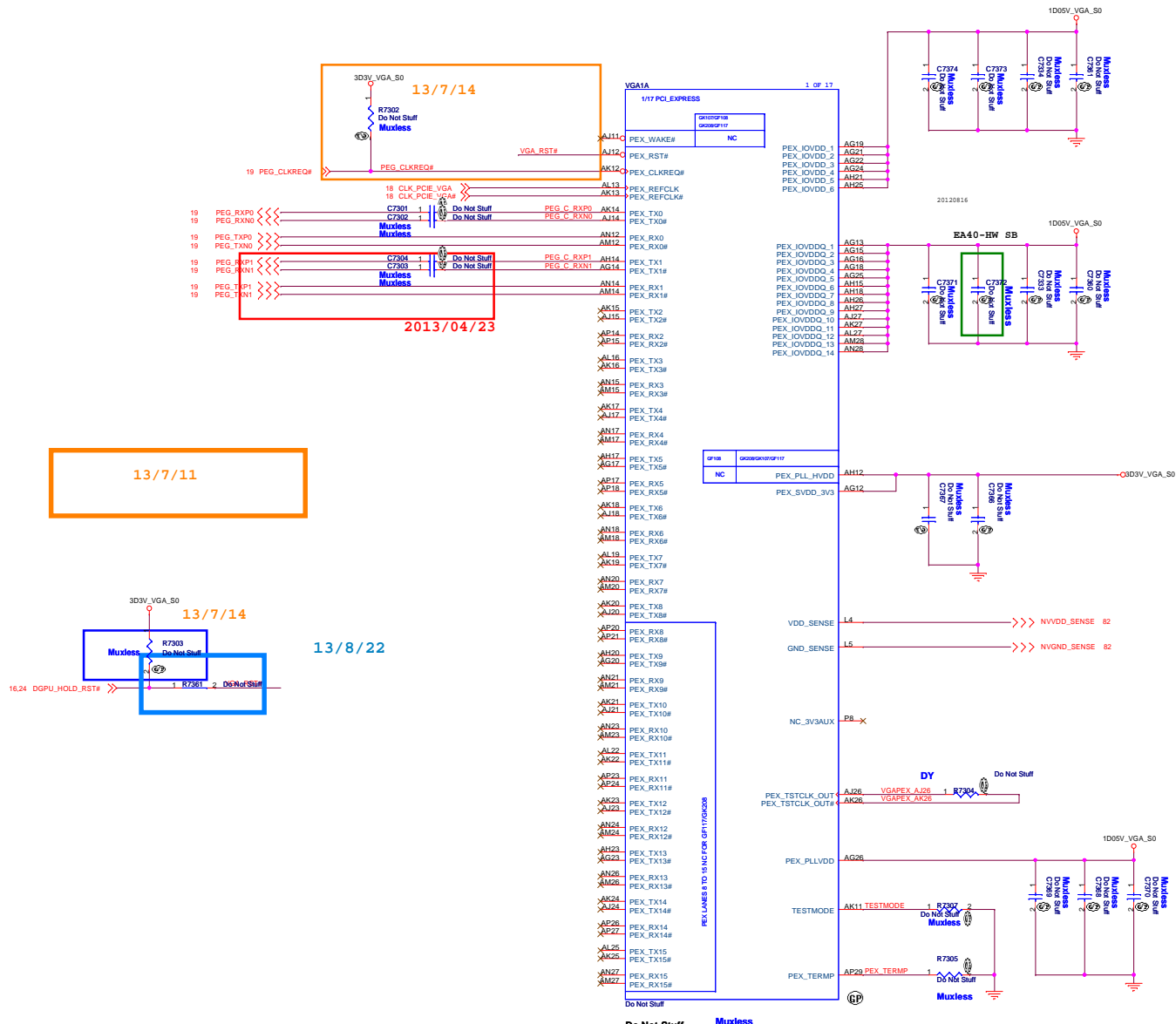
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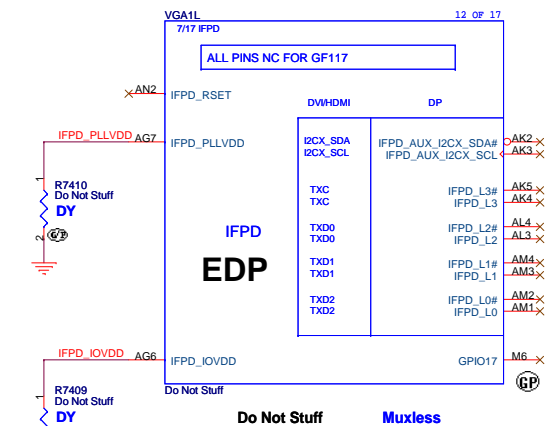
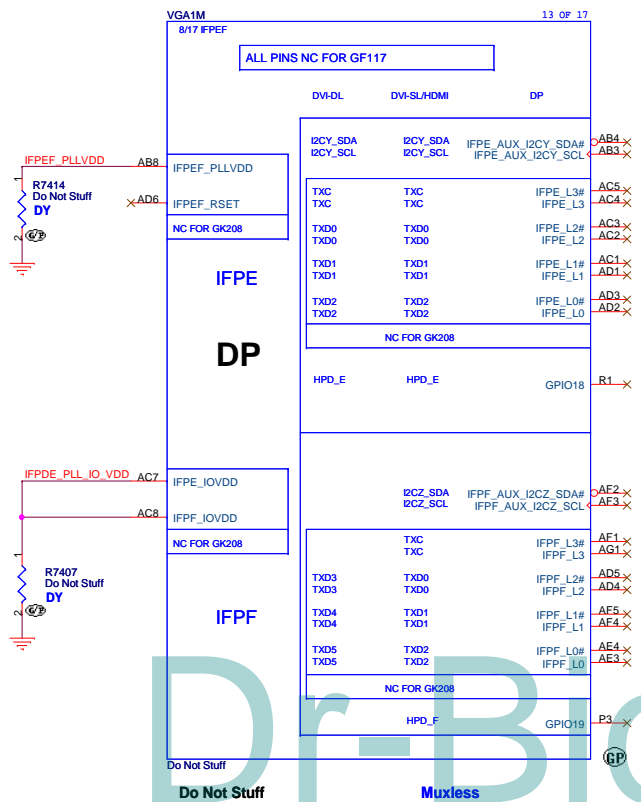
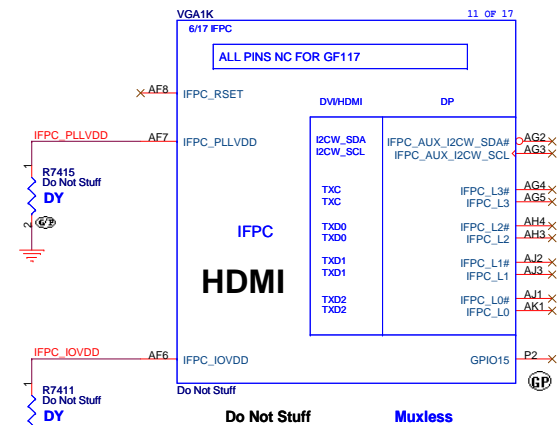
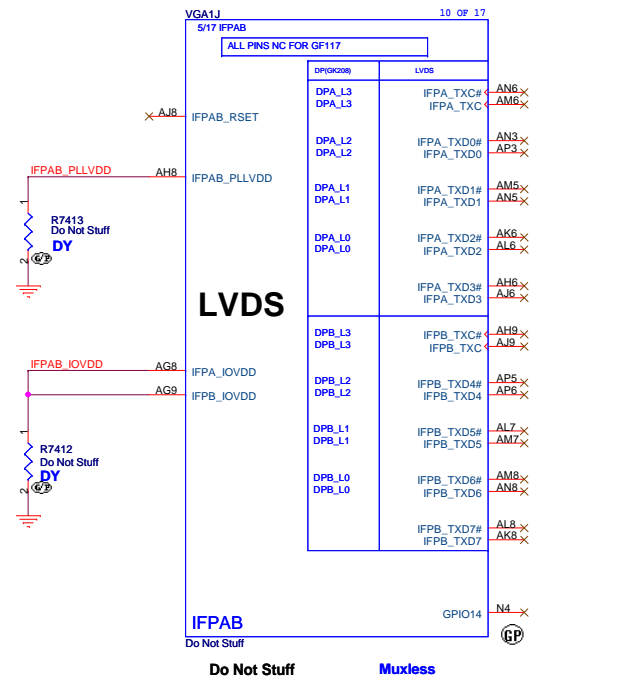
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Size	Document Number	Rev
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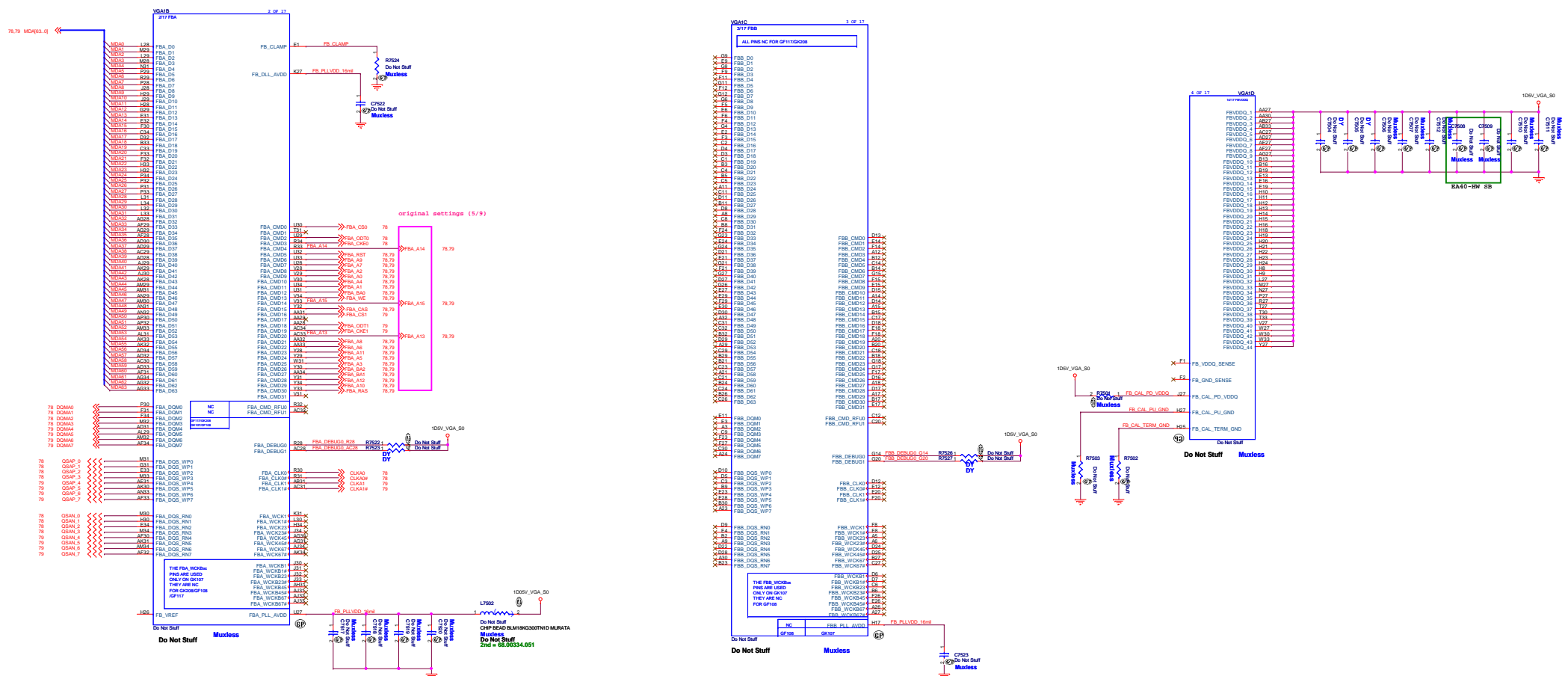
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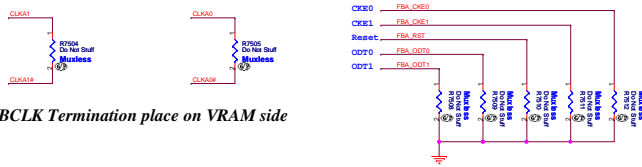
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**Group A**



**FBCLK Termination place on VRAM side**

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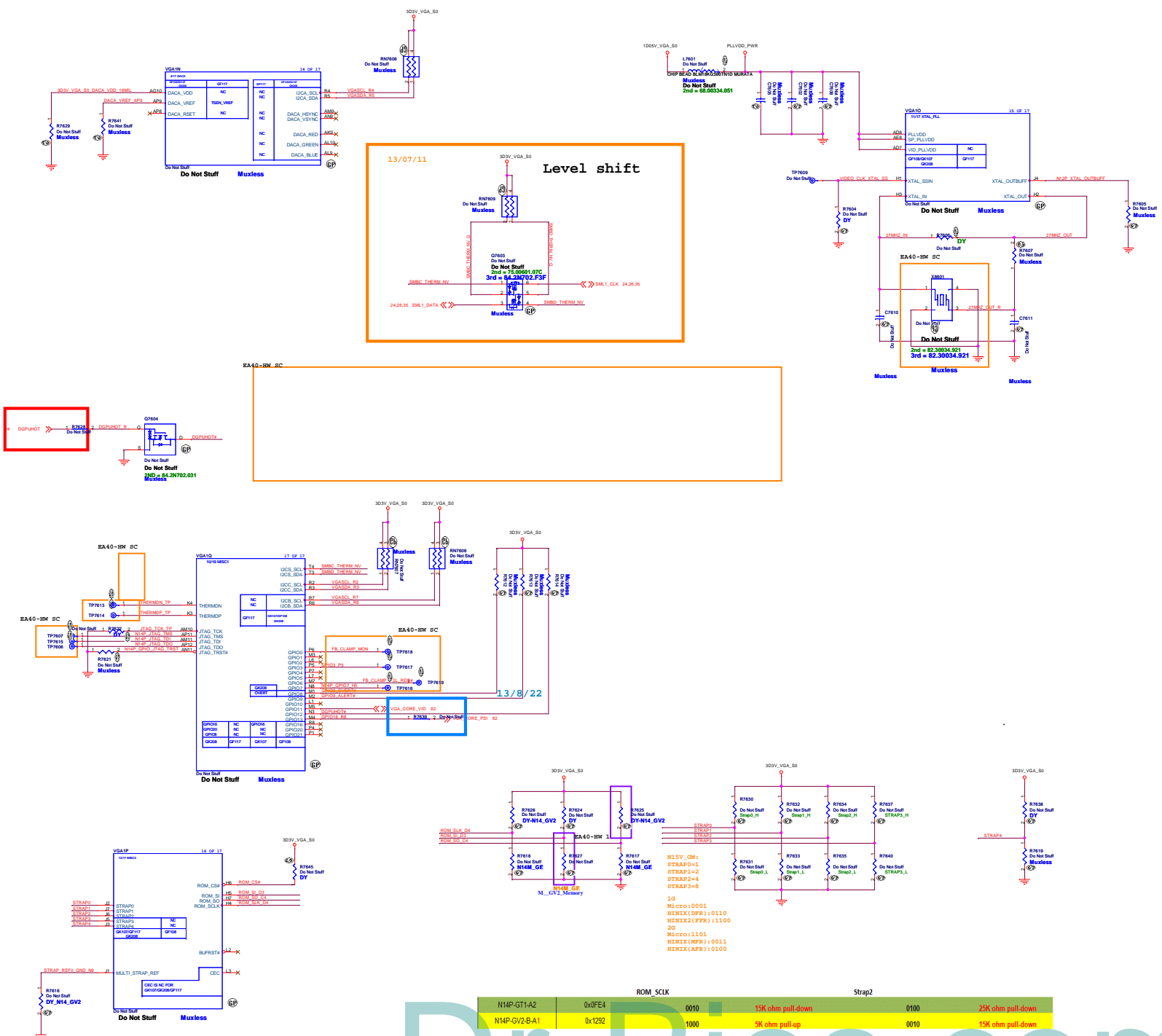


Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SD	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCI_MAX_SPEED	10k Ω	Pull-down to GND

Strap Pin Name	Logical Strapping RH3	Logical Strapping RH2	Logical Strapping RH1	Logical Strapping RH0
ROM_SCLK	PCI_DEV[0]4	SUB_VENDOR	PCI_DEV[5]	PEX_PLL_BN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SD	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 2	PCI_DEV[3]	PCI_DEV[2]	PCI_DEV[1]	PCI_DEV[0]
STRAP 3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP 4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCI_MAX_SPEED	DP_PLL_VDD33V

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/FBVDDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x8	1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
			1.5 V / 1.5 V	MT41K256M16HA-107GE	900	N/A	Production ready
	Hynix	0x3	1.5V / 1.5V	H5TQ4G3MFR-11C	900	N/A	Production ready
			0x4	H5TQ4G3AFR-11C	N/A	N/A	Qualification Candidate

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/FBVDDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x3	1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
			1.5 V / 1.5 V	MT41K128M16HA-107GE	900	N/A	Production ready
	Hynix	0x6	1.5V / 1.5V	H5TQ2G3MFR-11C	1000	N/A	Production ready
			0x7	H5TQ2G3DFR-11C	900	N/A	Production ready

Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

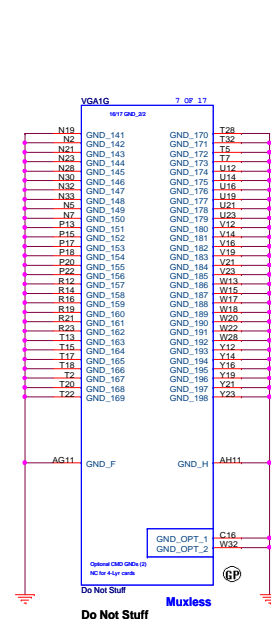
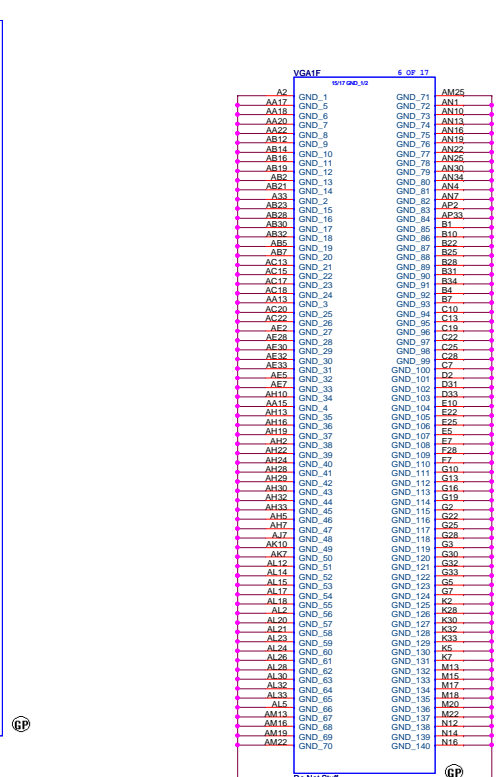
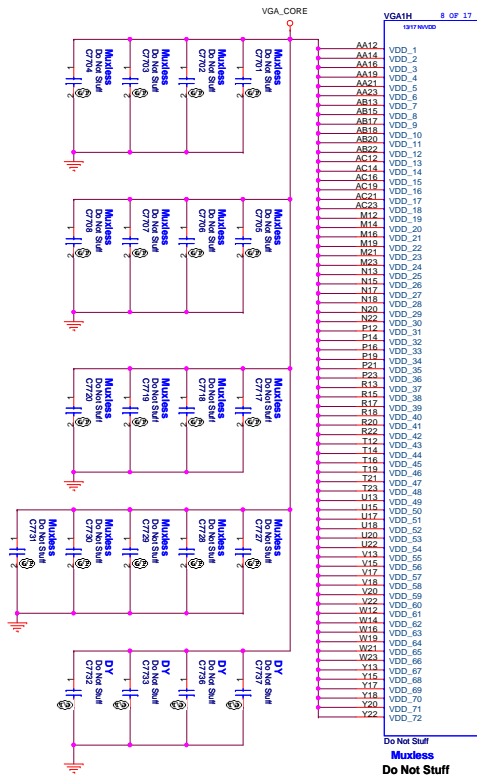
**4.99Kohm 64.49915.6DL**  
**10Kohm 64.10025.1.0L**  
**15Kohm 64.15025.6DL**  
**20Kohm 64.20025.6DL**  
**24.9Kohm 64.24925.6DL**  
**30.1Kohm 64.30125.6DL**  
**34.8Kohm 64.34825.6DL**  
**45.3Kohm 64.45325.6DL**

For 1GB VRAM (128x16\*4pes)  
 VR.02B0G.005 : VRAM HYNIX Graphic DDRIII 900 2Gb  
 H5TQ2G63DFR-11C LF+HF 128\*16 38nm Gemma die  
 KN.2GB0G.038 : VRAM HYNIX Graphic DDRIII 900 2Gb  
 H5T2G63FR-11C LF+HF 128\*16 29nm, Huma

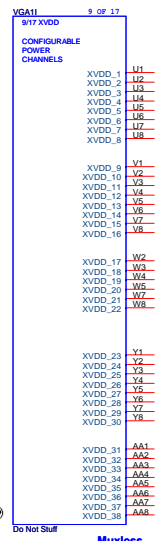
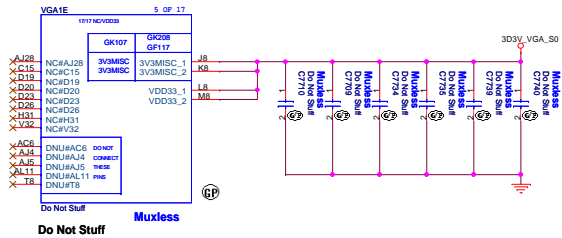
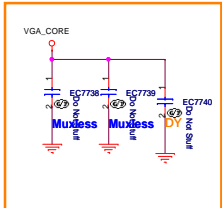
For 2GB VRAM (256x16\*4pes)  
 KN.0040G.001 : VRAM MICRON Graphic DDRIII 900 4Gb  
 MT41K256M16HA-107GE LF+HF 256\*16 30nm, V8DA  
 KN.0040G.0 : VRAM HYNIX Graphic DDRIII 900 4Gb  
 H5T4G63AFR-11C LF+HF 256\*16 29nm, Huma

ROM_SCLK	Strap2	Strap1	Strap0
N14P-GT1-A2	0x0FE4	0010	15K ohm pull-down
N14P-GV2-B-1	0x1292	1000	5K ohm pull-up

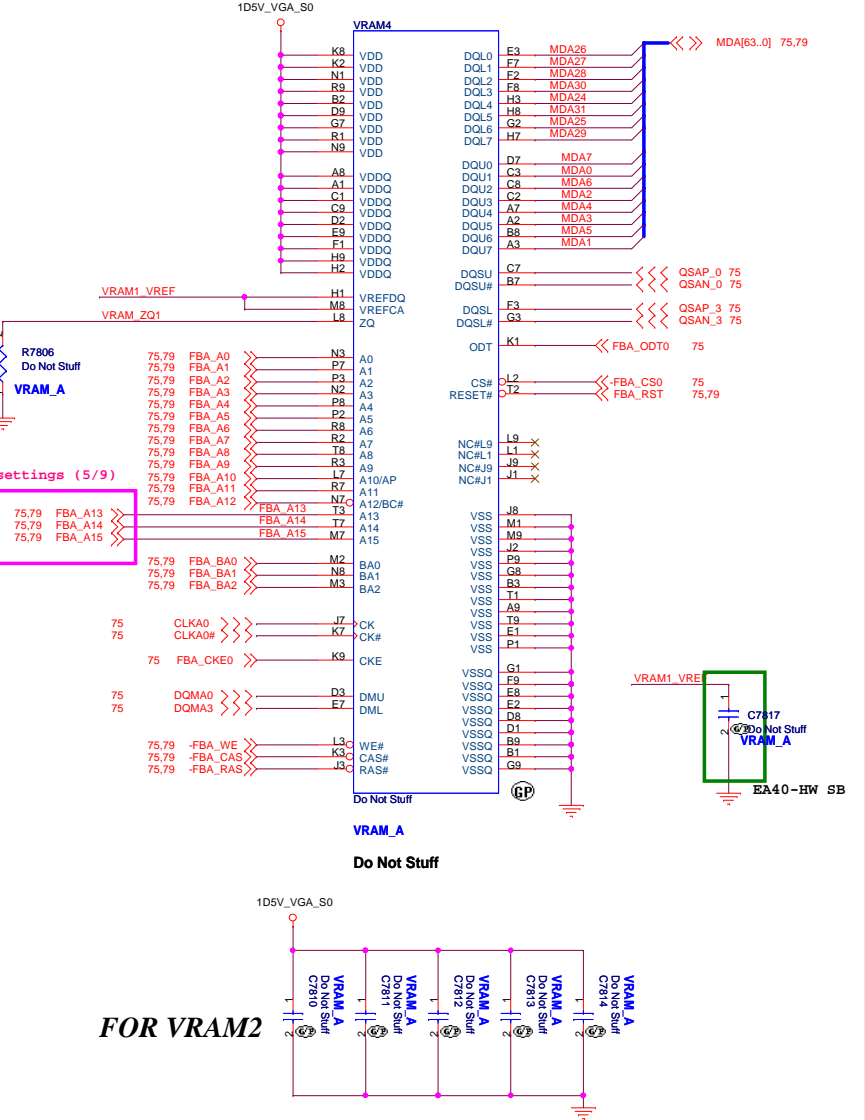
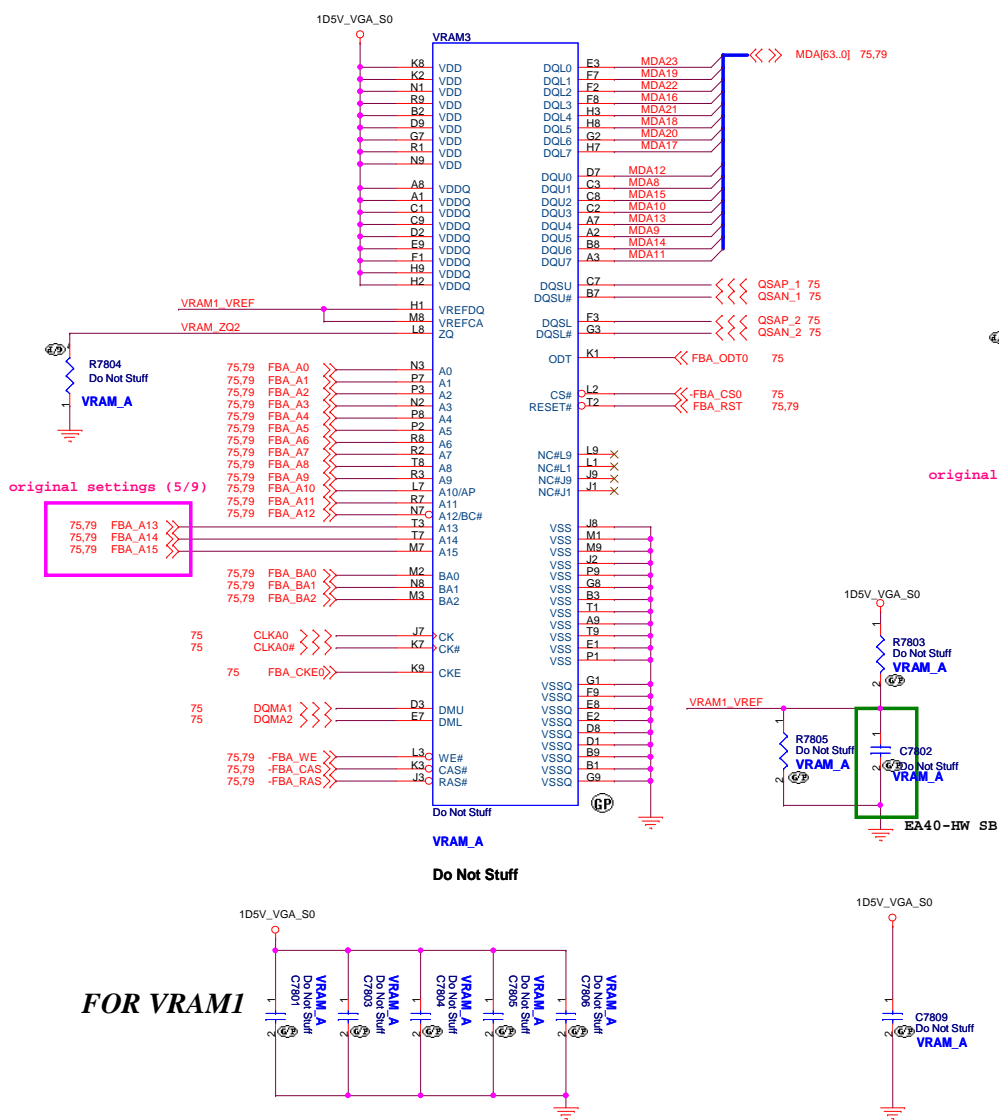




For EMI Request (13/8/23)



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FOR VRAM1

FOR VRAM2

VRAM BOM for EA40\_BM

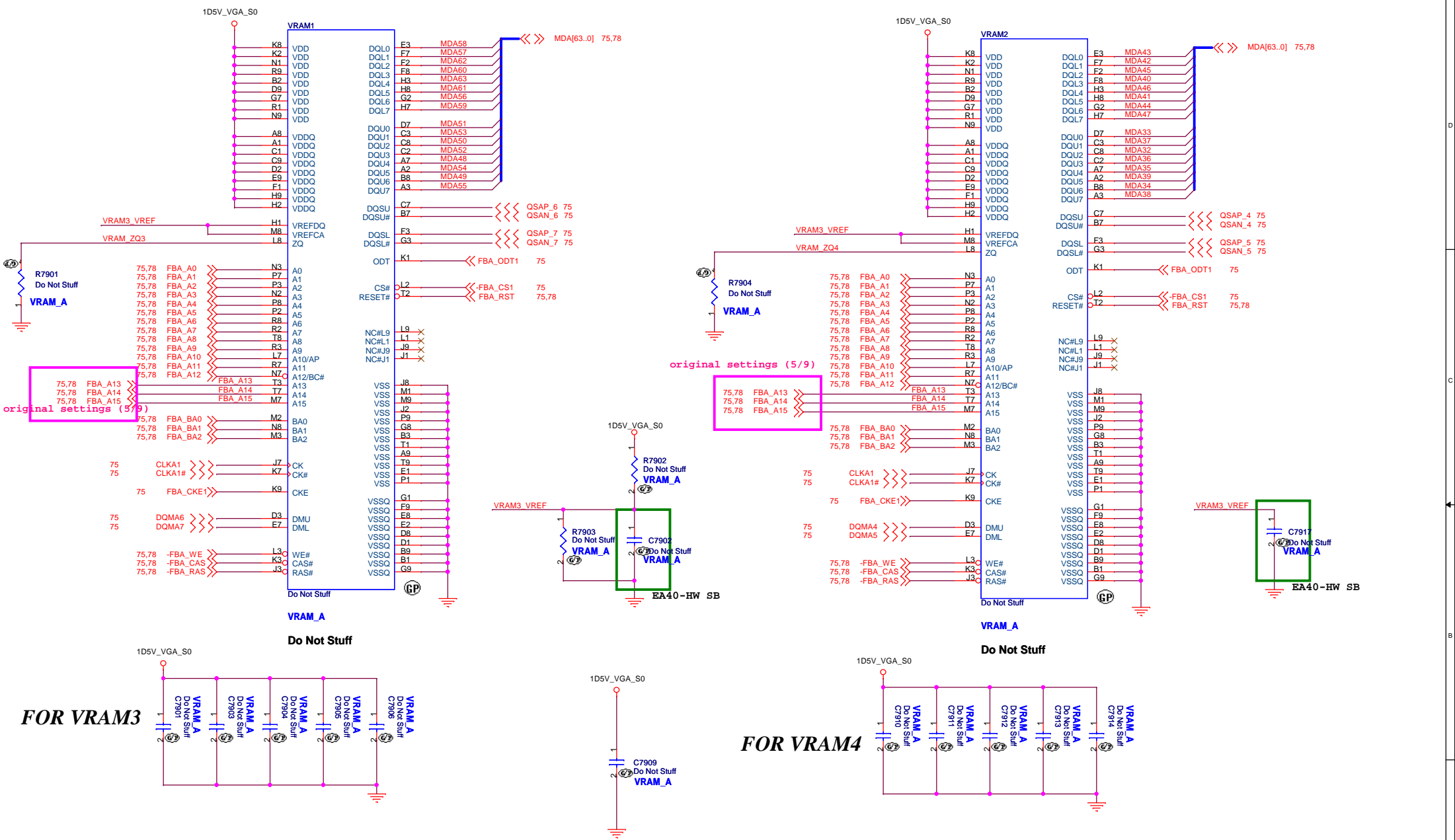
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Date: Wednesday, November 13, 2013 Sheet 78 of 102



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Size A3 Document Number: **EA40 BM** Rev: **-1**

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C

C

B

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A

A

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5

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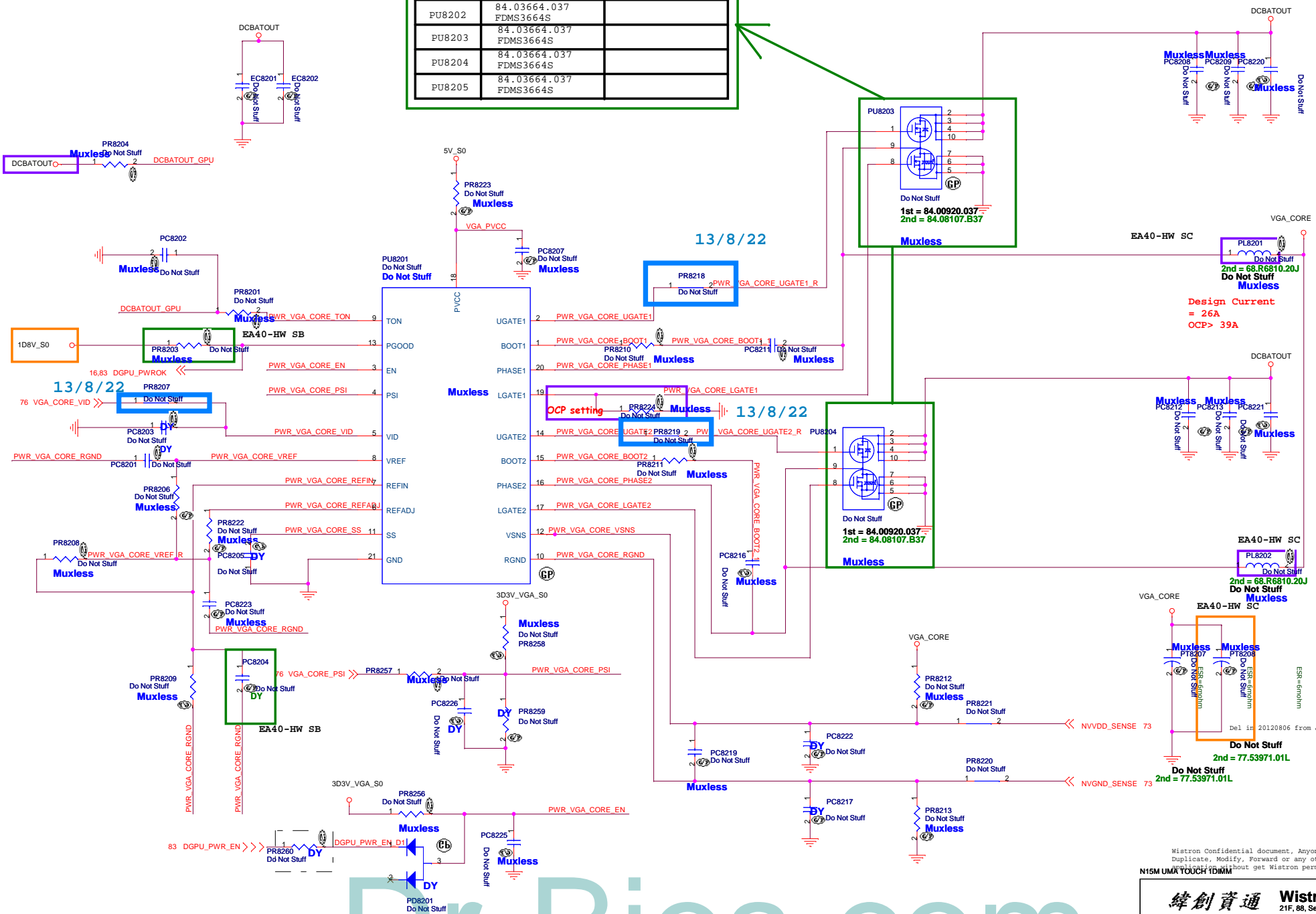
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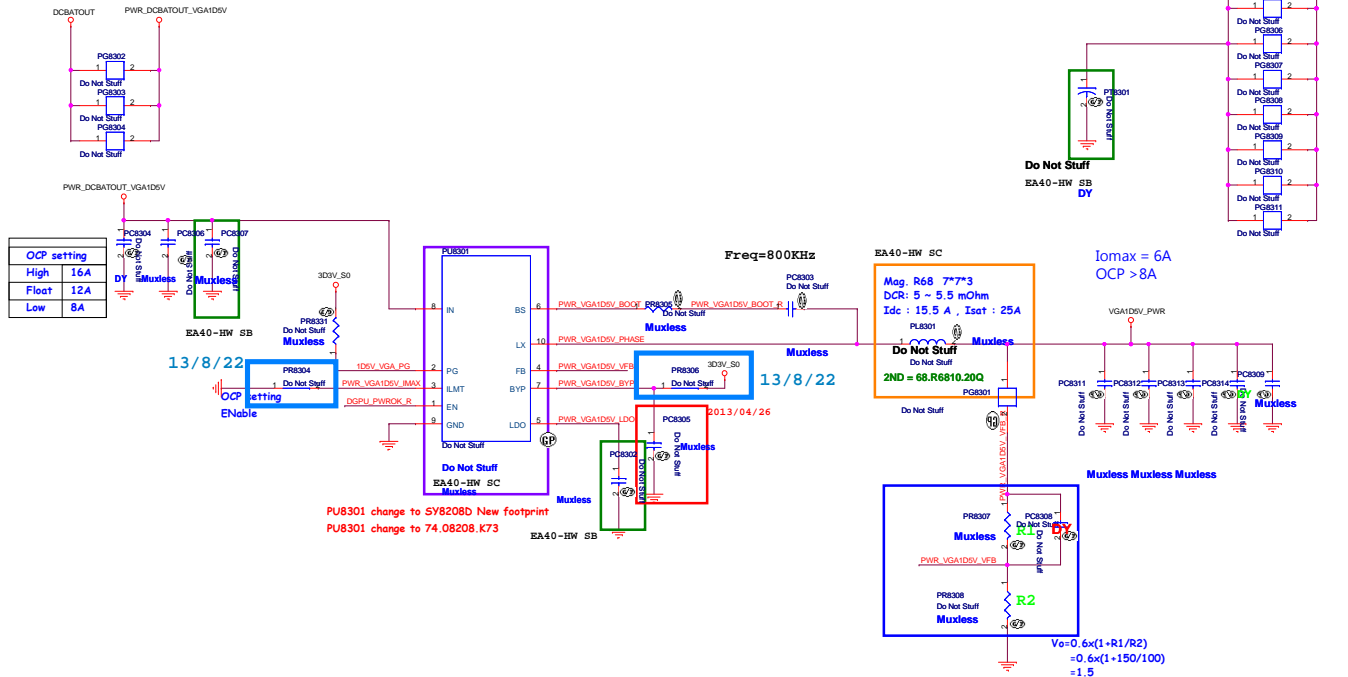


	Main source	2nd source
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PU8203	84.03664.037 FDMS3664S	
PU8204	84.03664.037 FDMS3664S	
PU8205	84.03664.037 FDMS3664S	

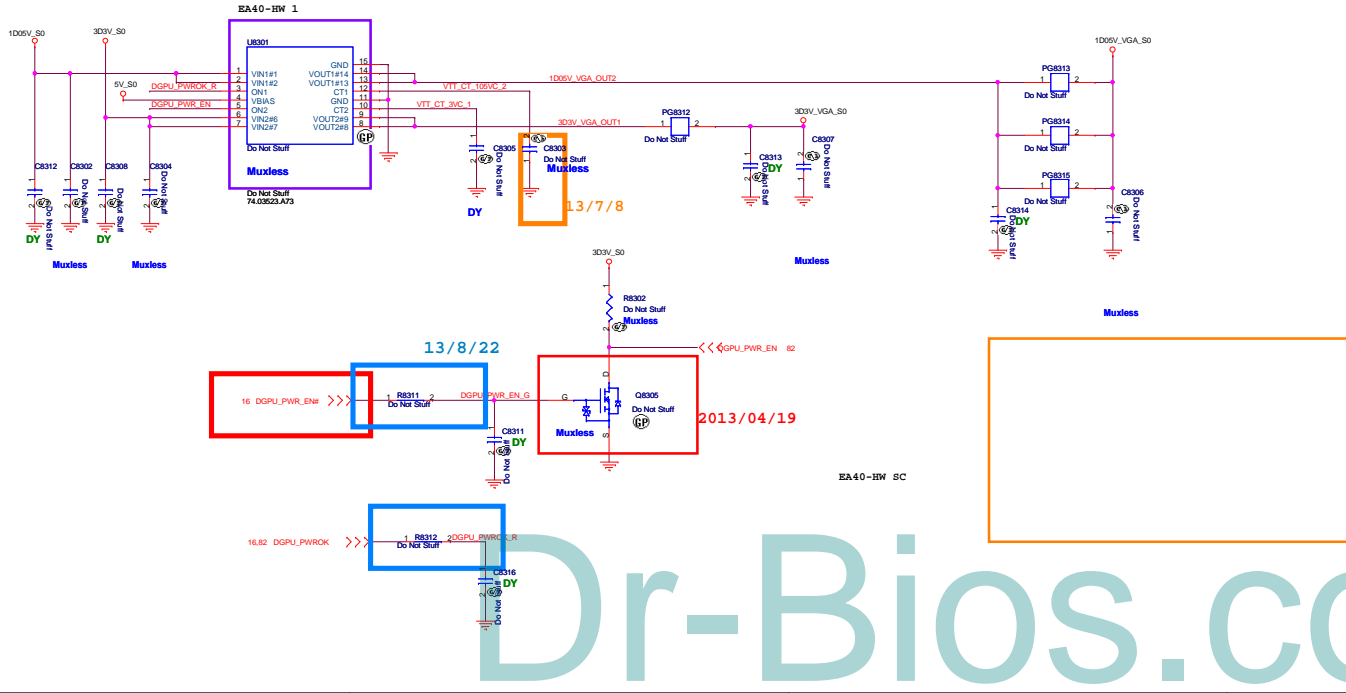


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# SY8208D for VGA\_1D5V(For VRAM GDDR3)



## 3D3V\_S0 to 3D3V\_VGA\_S0 1D05V\_VTT to 1D05V\_VGA\_S0



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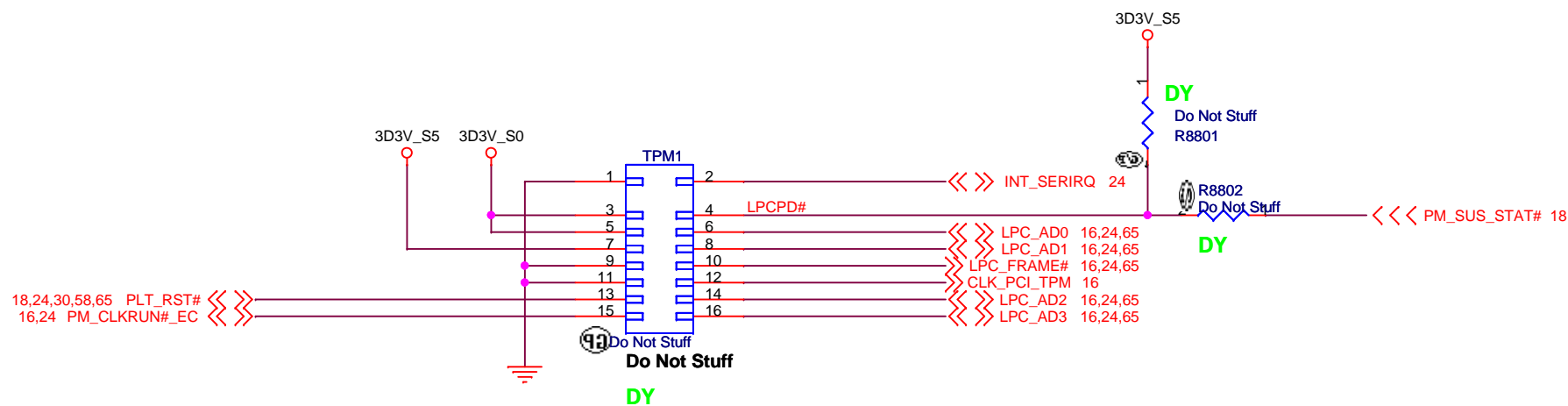
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SSID = Docking

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 <sup>1</sup>	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# <sup>1</sup>	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 <sup>1</sup>	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# <sup>1</sup>	O	System	18	HOOK7	DBR# <sup>1</sup>	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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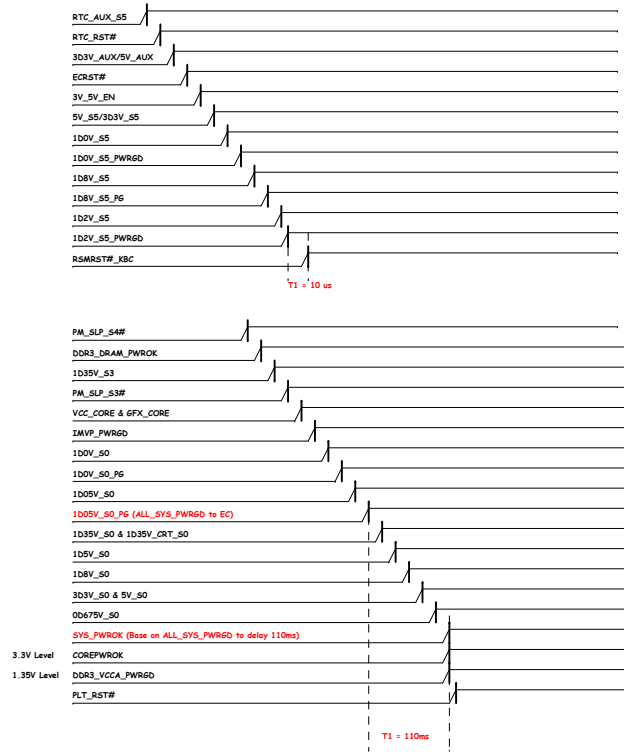
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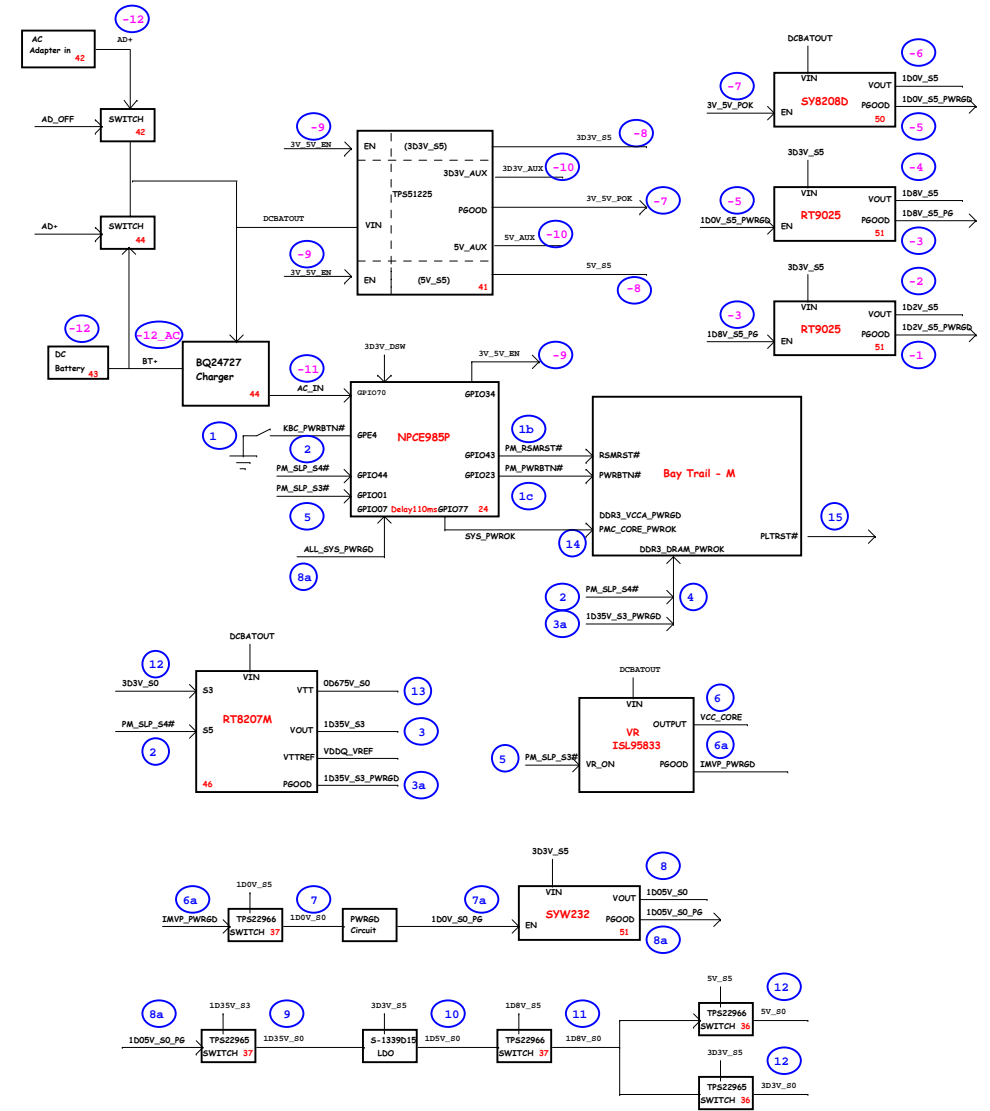
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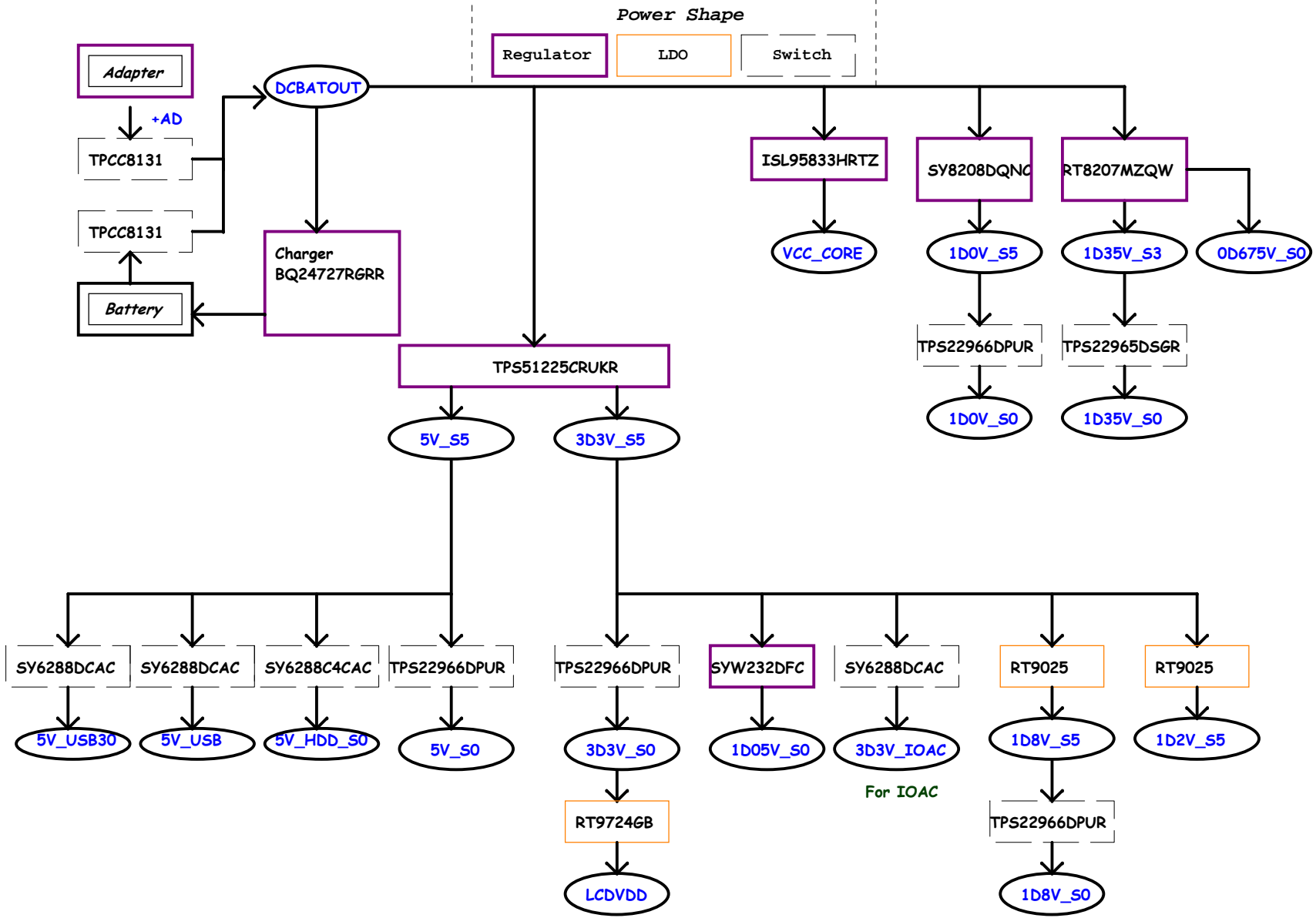
# Intel-Power Up Sequence with non-S0ix



# Bay Trail - M POWER UP SEQUENCE DIAGRAM

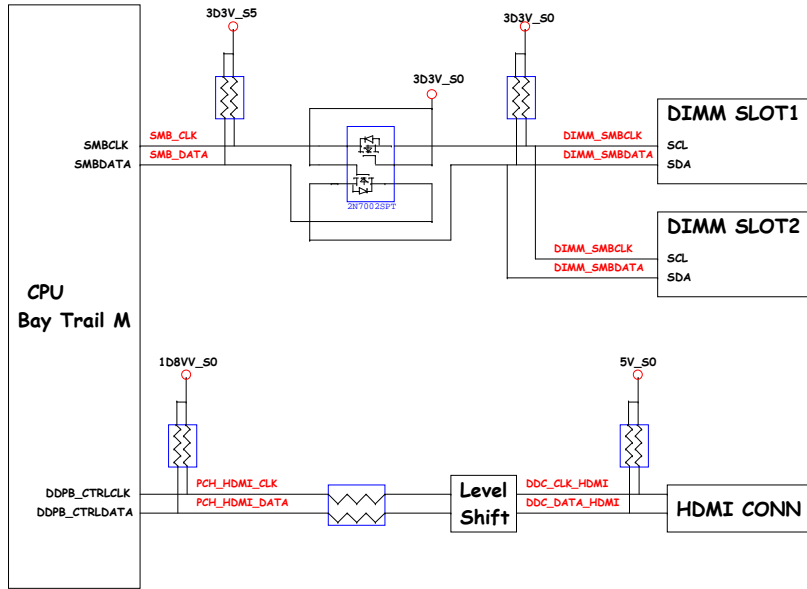


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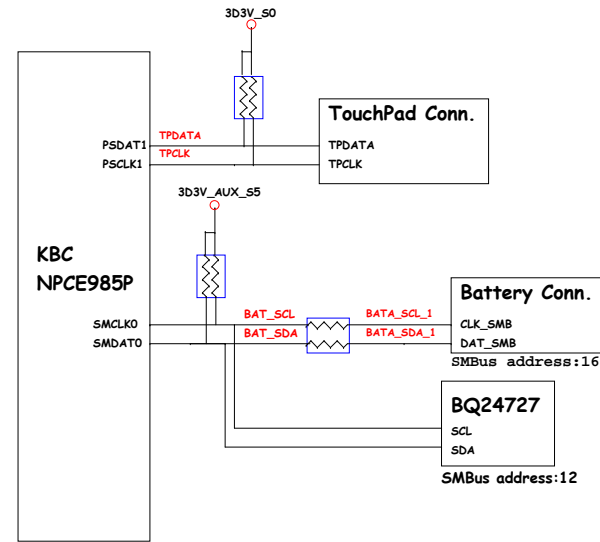


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# PCH SMBus Block Diagram



# KBC SMBus Block Diagram

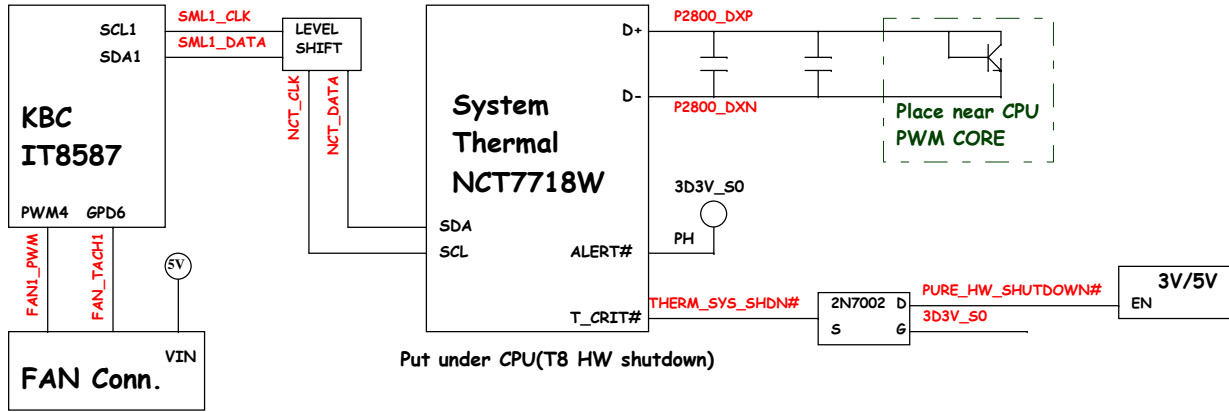


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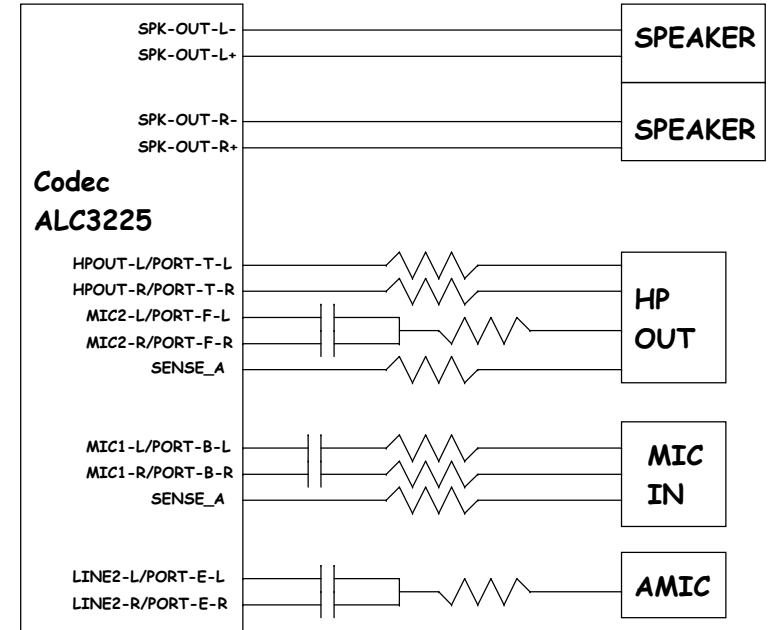
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# Thermal Block Diagram



# Audio Block Diagram



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