Compal Confidential

NAV70 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRII

2010-04-29

REV: 2.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
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Title	SCHEMATICS, MB A5651		
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Model Name : NAV70
File Name : LA-5651P

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CK505
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Speaker

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 17)

	VCC	3.3V				
	Ra	100K				
	ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max
NAV50	0	R01 (EVT)	0	0V	0V	0V
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
	2	R03 (PVT)	18K	0.436V	0.503V	0.538V
	3	R10A (MP)	33K	0.712V	0.819V	0.875V
NAV60	4	R01 (EVT)	56K	1.036V	1.185V	1.264V
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V
	7	R10A (MP)	NC	2.500V	3.3V	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
EMC1402	100_1100

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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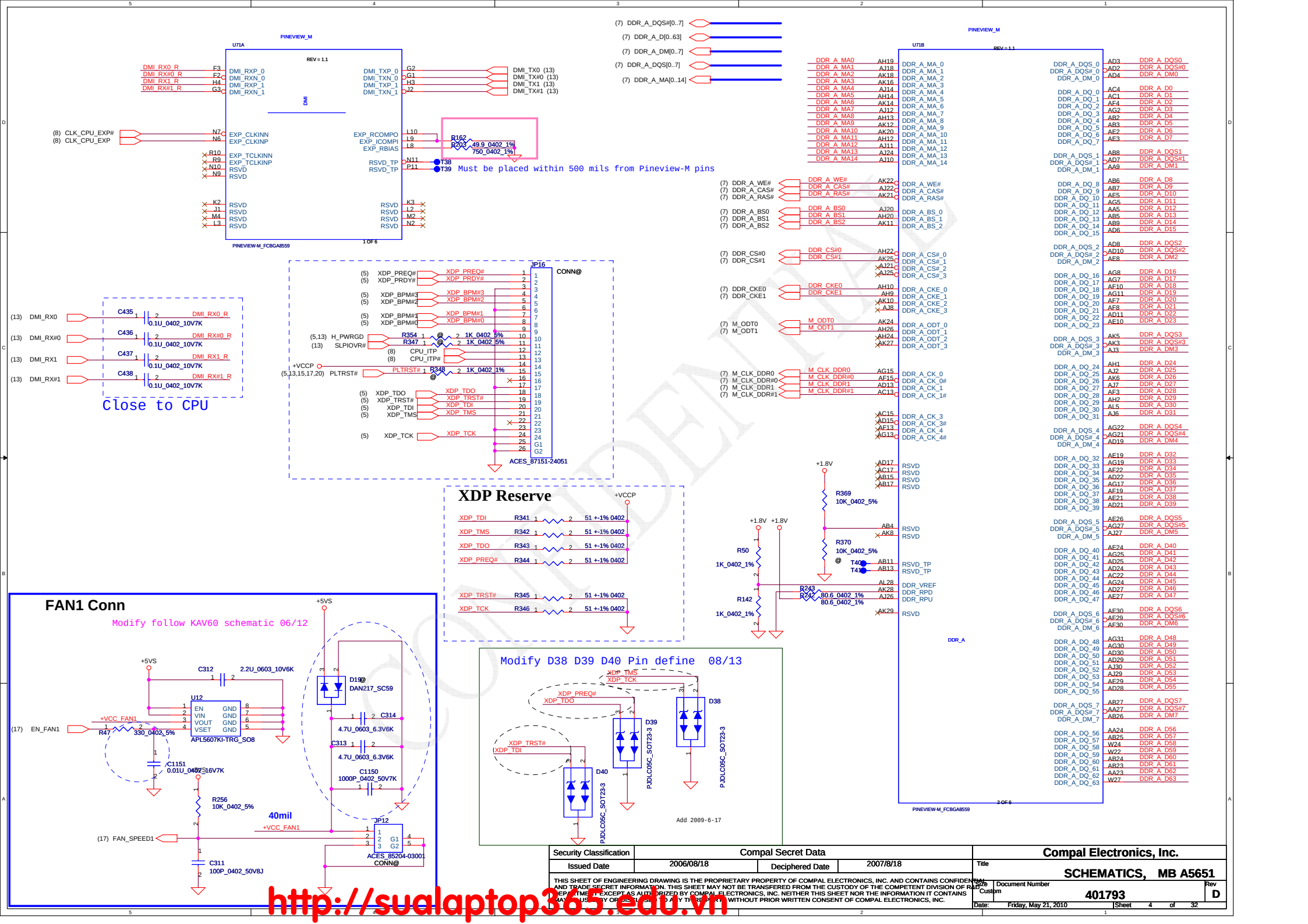
PINEVIEW_M
U71A
REV = 1.1
DMI_RX0_R
DMI_RX#0_R
DMI_RX1_R
DMI_RX#1_R
DMI_RXP_0
DMI_RXN_0
DMI_RXP_1
DMI_RXN_1
DMI_TXP_0
DMI_TXN_0
DMI_TXP_1
DMI_TXN_1
DMI_TX0 (13)
DMI_TX#0 (13)
DMI_TX1 (13)
DMI_TX#1 (13)
DMI
(8) CLK_CPU_EXP#
(8) CLK_CPU_EXP
EXP_CLKINN
EXP_CLKINP
EXP_RCOMPO
EXP_ICOMPI
EXP_RBIAS
R162
R203 49.9_0402_1%
750_0402_1%
Must be placed within 500 mils from Pineview-M pins
EXP_TCLKINN
EXP_TCLKINP
RSVD_TP
RSVD
PINEVIEW-M_FCBGA8559
1 OF 6
(7) DDR_A_DQS#[0..7]
(7) DDR_A_D[0..63]
(7) DDR_A_DM[0..7]
(7) DDR_A_DQS[0..7]
(7) DDR_A_MA[0..14]
U71B
DDR_A_MA_0
DDR_A_MA_1
DDR_A_MA_2
DDR_A_MA_3
DDR_A_MA_4
DDR_A_MA_5
DDR_A_MA_6
DDR_A_MA_7
DDR_A_MA_8
DDR_A_MA_9
DDR_A_MA_10
DDR_A_MA_11
DDR_A_MA_12
DDR_A_MA_13
DDR_A_MA_14
DDR_A_WE#
DDR_A_CAS#
DDR_A_RAS#
DDR_A_BS_0
DDR_A_BS_1
DDR_A_BS_2
DDR_A_CS#_0
DDR_A_CS#_1
DDR_A_CS#_2
DDR_A_CS#_3
DDR_A_CKE_0
DDR_A_CKE_1
DDR_A_CKE_2
DDR_A_CKE_3
DDR_A_ODT_0
DDR_A_ODT_1
DDR_A_ODT_2
DDR_A_ODT_3
DDR_A_CK_0
DDR_A_CK_0#
DDR_A_CK_1
DDR_A_CK_1#
DDR_A_CK_3
DDR_A_CK_3#
DDR_A_CK_4
DDR_A_CK_4#
DDR_A_DQS_0
DDR_A_DQS#_0
DDR_A_DM_0
DDR_A_DQ_0
DDR_A_DQ_1
DDR_A_DQ_2
DDR_A_DQ_3
DDR_A_DQ_4
DDR_A_DQ_5
DDR_A_DQ_6
DDR_A_DQ_7
DDR_A_DQS_1
DDR_A_DQS#_1
DDR_A_DM_1
DDR_A_DQ_8
DDR_A_DQ_9
DDR_A_DQ_10
DDR_A_DQ_11
DDR_A_DQ_12
DDR_A_DQ_13
DDR_A_DQ_14
DDR_A_DQ_15
DDR_A_DQS_2
DDR_A_DQS#_2
DDR_A_DM_2
DDR_A_DQ_16
DDR_A_DQ_17
DDR_A_DQ_18
DDR_A_DQ_19
DDR_A_DQ_20
DDR_A_DQ_21
DDR_A_DQ_22
DDR_A_DQ_23
DDR_A_DQS_3
DDR_A_DQS#_3
DDR_A_DM_3
DDR_A_DQ_24
DDR_A_DQ_25
DDR_A_DQ_26
DDR_A_DQ_27
DDR_A_DQ_28
DDR_A_DQ_29
DDR_A_DQ_30
DDR_A_DQ_31
DDR_A_DQS_4
DDR_A_DQS#_4
DDR_A_DM_4
DDR_A_DQ_32
DDR_A_DQ_33
DDR_A_DQ_34
DDR_A_DQ_35
DDR_A_DQ_36
DDR_A_DQ_37
DDR_A_DQ_38
DDR_A_DQ_39
DDR_A_DQS_5
DDR_A_DQS#_5
DDR_A_DM_5
DDR_A_DQ_40
DDR_A_DQ_41
DDR_A_DQ_42
DDR_A_DQ_43
DDR_A_DQ_44
DDR_A_DQ_45
DDR_A_DQ_46
DDR_A_DQ_47
DDR_A_DQS_6
DDR_A_DQS#_6
DDR_A_DM_6
DDR_A_DQ_48
DDR_A_DQ_49
DDR_A_DQ_50
DDR_A_DQ_51
DDR_A_DQ_52
DDR_A_DQ_53
DDR_A_DQ_54
DDR_A_DQ_55
DDR_A_DQS_7
DDR_A_DQS#_7
DDR_A_DM_7
DDR_A_DQ_56
DDR_A_DQ_57
DDR_A_DQ_58
DDR_A_DQ_59
DDR_A_DQ_60
DDR_A_DQ_61
DDR_A_DQ_62
DDR_A_DQ_63
DDR_A
2 OF 6
PINEVIEW-M_FCBGA8559
C435 0.1U_0402_10V7K
C436 0.1U_0402_10V7K
C437 0.1U_0402_10V7K
C438 0.1U_0402_10V7K
(13) DMI_RX0
(13) DMI_RX#0
(13) DMI_RX1
(13) DMI_RX#1
DMI_RX0_R
DMI_RX#0_R
DMI_RX1_R
DMI_RX#1_R
Close to CPU
JP16
CONN@
ACES_87151-24051
(5) XDP_PREQ#
(5) XDP_PRDY#
(5) XDP_BPM#3
(5) XDP_BPM#2
(5) XDP_BPM#1
(5) XDP_BPM#0
(5,13) H_PWRGD
(13) SLPIOVR#
R354 1K_0402_5%
R347 1K_0402_5%
(8) CPU_ITP
(8) CPU_ITP#
+VCCP
(5,13,15,17,20) PLTRST#
R348 1K_0402_1%
(5) XDP_TDO
(5) XDP_TRST#
(5) XDP_TDI
(5) XDP_TMS
(5) XDP_TCK
XDP Reserve
+VCCP
XDP_TDI R341 51 +-1% 0402
XDP_TMS R342 51 +-1% 0402
XDP_TDO R343 51 +-1% 0402
XDP_PREQ# R344 51 +-1% 0402
XDP_TRST# R345 51 +-1% 0402
XDP_TCK R346 51 +-1% 0402
+1.8V
R369 10K_0402_5%
R370 10K_0402_5%
@ T40 T41
R50 1K_0402_1%
R142 1K_0402_1%
R243 R242 80.6_0402_1%
RSVD_TP
DDR_VREF
DDR_RPD
DDR_RPU
RSVD
FAN1 Conn
Modify follow KAV60 schematic 06/12
+5VS
C312 2.2U_0603_10V6K
U12
APL5607KI-TRG_SO8
+VCC_FAN1
(17) EN_FAN1
R47 330_0402_5%
C1151 0.01U_0402_16V7K
R256 10K_0402_5%
40mil
(17) FAN_SPEED1
JP12
ACES_85204-03001
CONN@
C311 100P_0402_50V8J
D19@ DAN217_SC59
C314 4.7U_0603_6.3V6K
C313 4.7U_0603_6.3V6K
C1150 1000P_0402_50V7K
Modify D38 D39 D40 Pin define 08/13
XDP_TMS
XDP_TCK
XDP_PREQ#
XDP_TDO
XDP_TRST#
XDP_TDI
D38
D39
D40
PJDLC05C_SOT23-3
Add 2009-6-17
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Add 470PF on H_SMI# for known issue 07/08

C1171 470P_0402_50V7K

Add INVT_PWM 05/11

Del R323 05/11

Modify 08/04

Place closed to chipset

H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

CPU THERMAL SENSOR

U2 EMC1402-1-ACZL-TR MSOP 8P SENSOR
Address:100_1100

Close to Processor pin

Close to Processor pin

placed within 0.5" of processor pin.

placed within 0.5" of processor pin.

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GFX supply current: 1.38A
Sustained GFX supply current: 1.05A

DDR supply current 2.27A

DDR analog supply current: 1.32A

Display PLL SFR and CRT DAC supply current: 0.154A

GIO supply current: 0.006A

DAC, GIO, LVDS, & LGIO, DPLL, HMPLL supply current: 0.33A

Processor Core analog supply current: 0.08A

LVDS supply current: 0.06A

DMI analog supply current: 0.48A

SFR & DMIHMPLL supply current: 0.104A

PLACE IN CAVITY

2 x 330uF(9mohm/2)

Close U71.D4

Close Chipset pin

Modify to 2.2U 05/11

Follow Intel check list change to 22uF 06/06

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09/03

Change to SP07F001720 04/30

(4) DDR_A_DQS#[0..7]
(4) DDR_A_DQ[0..63]
(4) DDR_A_DM[0..7]
(4) DDR_A_DQS[0..7]
(4) DDR_A_MA[0..14]

Layout Note:
Place near JDIM1

+1.8V

C128 2.2U_0603_6.3V4Z
C129 2.2U_0603_6.3V4Z
C110 2.2U_0603_6.3V4Z
C109 2.2U_0603_6.3V4Z
C130 2.2U_0603_6.3V4Z

@ C94 220U_B2_2.5VM_R35
C106 0.1U_0402_16V4Z
C105 0.1U_0402_16V4Z
C108 0.1U_0402_16V4Z
C107 0.1U_0402_16V4Z

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS

C119 C117 C86 C121 C87 C88 C122 C115 C91 C90 C120 C118 C89 C82 C439 C440 C441 C442 C443 C444 C445 C446
0.1U_0402_16V4Z

+0.9VS

RP6: DDR_A_MA13, M_ODT0, DDR_CS#0, DDR_A_RAS# — DDR_A_BS1, DDR_A_MA0, DDR_A_MA2, DDR_A_MA4
RP5: DDR_A_BS1, DDR_A_MA0, DDR_A_MA2, DDR_A_MA4
RP2: DDR_A_BS0, DDR_A_MA10, DDR_A_MA1, DDR_A_MA3 — DDR_A_MA6, DDR_A_MA7, DDR_A_MA11, DDR_A_MA14
RP4: DDR_A_MA6, DDR_A_MA7, DDR_A_MA11, DDR_A_MA14
RP3: M_ODT1, DDR_CS#1, DDR_A_CAS#, DDR_A_WE# — DDR_A_MA5, DDR_A_MA8, DDR_A_MA9, DDR_A_MA12
RP1: DDR_A_MA5, DDR_A_MA8, DDR_A_MA9, DDR_A_MA12
47_0804_8P4R_5%

DDR_CKE1 — R63 47_0402_5%
DDR_A_BS2 — R60 47_0402_5%
DDR_CKE0 — R59 47_0402_5%

Layout Note:
Place these resistor closely DIMMA,all trace length<750 mil

Layout Note:
Place these resistor closely DIMMA,all trace length Max=1.3"

+DIMM_VREF — C111 0.1U_0402_16V4Z — C112 2.2U 6.3V M X5R 0402
+1.8V — R61 1K_0402_1% — +DIMM_VREF — R62 1K_0402_1%

Share +DIMM_VREF for
1.DDRII VREF
2.GMCH SM_VREF_0
SM_VREF_1

+3VS — C116 0.1U_0402_16V4Z — C141 0.1U_0402_16V4Z
Follow Intel Layout checklist, add C141 05/12

CONN@ JDIM1 — FOX_AS0A426-N4RN-7F

DDR_A_D0	5	DQ0	
DDR_A_D1	7	DQ1	
DDR_A_DQS#0	11	DQS0#	
DDR_A_DQS0	13	DQS0	
DDR_A_D2	17	DQ2	
DDR_A_D3	19	DQ3	
DDR_A_D8	23	DQ8	
DDR_A_D9	25	DQ9	
DDR_A_DQS#1	29	DQS1#	
DDR_A_DQS1	31	DQS1	
DDR_A_D10	35	DQ10	
DDR_A_D11	37	DQ11	
DDR_A_D16	43	DQ16	
DDR_A_D17	45	DQ17	
DDR_A_DQS#2	49	DQS2#	
DDR_A_DQS2	51	DQS2	
DDR_A_D18	55	DQ18	
DDR_A_D19	57	DQ19	
DDR_A_D24	61	DQ24	
DDR_A_D25	63	DQ25	
DDR_A_DM3	67	DM3	
DDR_A_D26	73	DQ26	
DDR_A_D27	75	DQ27	
(4) DDR_CKE0 / DDR_CKE0	79	CKE0	
(4) DDR_A_BS2 / DDR_A_BS2	87	BA2	
DDR_A_MA12	89	A12	
DDR_A_MA9	91	A9	
DDR_A_MA8	93	A8	
DDR_A_MA5	97	A5	
DDR_A_MA3	99	A3	
DDR_A_MA1	101	A1	
DDR_A_MA10	105	A10/AP	
(4) DDR_A_BS0 / DDR_A_BS0	107	BA0	
(4) DDR_A_WE# / DDR_A_WE#	109	WE#	
(4) DDR_A_CAS# / DDR_A_CAS#	113	CAS#	
(4) DDR_CS#1 / DDR_CS#1	115	NC/S1#	
(4) M_ODT1 / M_ODT1	119	NC/ODT1	
DDR_A_D32	123	DQ32	
DDR_A_D33	125	DQ33	
DDR_A_DQS#4	129	DQS4#	
DDR_A_DQS4	131	DQS4	
DDR_A_D34	135	DQ34	
DDR_A_D35	137	DQ35	
DDR_A_D40	141	DQ40	
DDR_A_D41	143	DQ41	
DDR_A_DM5	147	DM5	
DDR_A_D42	151	DQ42	
DDR_A_D43	153	DQ43	
DDR_A_D48	157	DQ48	
DDR_A_D49	159	DQ49	
DDR_A_DQS#6	167	DQS6#	
DDR_A_DQS6	169	DQS6	
DDR_A_D50	173	DQ50	
DDR_A_D51	175	DQ51	
DDR_A_D56	179	DQ56	
DDR_A_D57	181	DQ57	
DDR_A_DM7	185	DM7	
DDR_A_D58	189	DQ58	
DDR_A_D59	191	DQ59	
(8,15) CLK_SMBDATA / CLK_SMBDATA	195	SDA	
(8,15) CLK_SMBCLK / CLK_SMBCLK	197	SCL	
	199	VDDSPD	
	201	G1	

	2	VSS	
DDR_A_D4	4	DQ4	
DDR_A_D5	6	DQ5	
	8	VSS	
DDR_A_DM0	10	DM0	
	12	VSS	
DDR_A_D6	14	DQ6	
DDR_A_D7	16	DQ7	
	18	VSS	
DDR_A_D12	20	DQ12	
DDR_A_D13	22	DQ13	
DDR_A_DM1	26	DM1	
M_CLK_DDR0 (4)	30	CK0	
M_CLK_DDR#0 (4)	32	CK0#	
DDR_A_D14	36	DQ14	
DDR_A_D15	38	DQ15	
	40	VSS	
	42	VSS	
DDR_A_D20	44	DQ20	
DDR_A_D21	46	DQ21	
R64 1 — 0_0402_5% — PM_EXTTS#0 (5)	50	NC	
DDR_A_DM2	52	DM2	
DDR_A_D22	56	DQ22	
DDR_A_D23	58	DQ23	
DDR_A_D28	62	DQ28	
DDR_A_D29	64	DQ29	
DDR_A_DQS#3	68	DQS3#	
DDR_A_DQS3	70	DQS3	
DDR_A_D30	74	DQ30	
DDR_A_D31	76	DQ31	
DDR_CKE1 / DDR_CKE1 (4)	80	NC/CKE1	
	82	VDD	
	84	NC/A15	
DDR_A_MA14	86	NC/A14	
DDR_A_MA11	90	A11	
DDR_A_MA7	92	A7	
DDR_A_MA6	94	A6	
DDR_A_MA4	98	A4	
DDR_A_MA2	100	A2	
DDR_A_MA0	102	A0	
DDR_A_BS1 / DDR_A_BS1 (4)	106	BA1	
DDR_A_RAS# / DDR_A_RAS# (4)	108	RAS#	
DDR_CS#0 / DDR_CS#0 (4)	110	S0#	
M_ODT0 / M_ODT0 (4)	114	ODT0	
DDR_A_MA13	116	NC/A13	
	120	NC	
DDR_A_D36	124	DQ36	
DDR_A_D37	126	DQ37	
DDR_A_DM4	130	DM4	
DDR_A_D38	134	DQ38	
DDR_A_D39	136	DQ39	
DDR_A_D44	140	DQ44	
DDR_A_D45	142	DQ45	
DDR_A_DQS#5	146	DQS5#	
DDR_A_DQS5	148	DQS5	
DDR_A_D46	152	DQ46	
DDR_A_D47	154	DQ47	
DDR_A_D52	158	DQ52	
DDR_A_D53	160	DQ53	
M_CLK_DDR1 (4)	164	CK1	
M_CLK_DDR#1 (4)	166	CK1#	
DDR_A_DM6	170	DM6	
DDR_A_D54	174	DQ54	
DDR_A_D55	176	DQ55	
DDR_A_D60	180	DQ60	
DDR_A_D61	182	DQ61	
DDR_A_DQS#7	186	DQS7#	
DDR_A_DQS7	188	DQS7	
DDR_A_D62	192	DQ62	
DDR_A_D63	194	DQ63	
R66 1 — 10K_0402_5%	198	SA0	
R65 1 — 10K_0402_5%	200	SA1	
	202	G2	

DIMMA

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Issued Date	2006/08/18	Deciphered Date	2007/8/18

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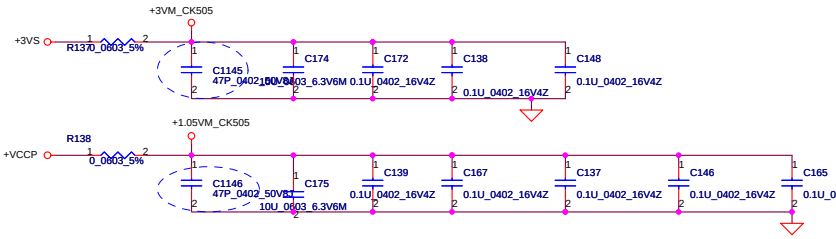
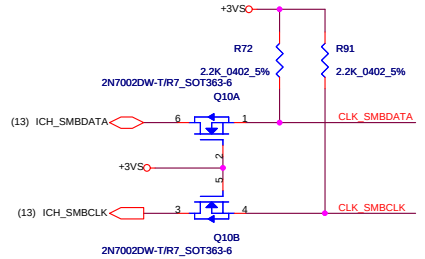
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

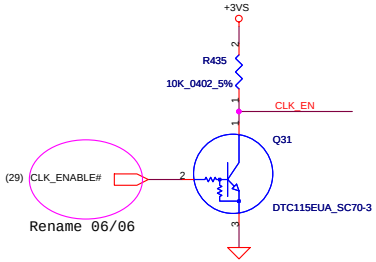
Change C174 C175 to 10U_0603 05/14



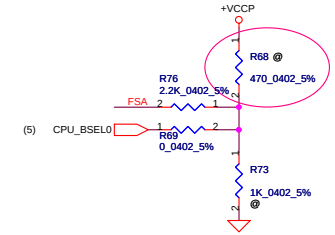


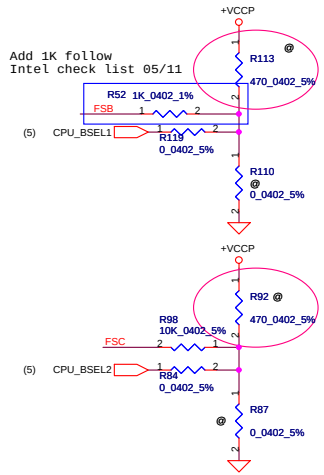
SA000020N00 (Realtek : RTM875N-397-GRT)

SA000020H10 (ICS : ICS9LPRS387BKLFT)



Rename 06/06

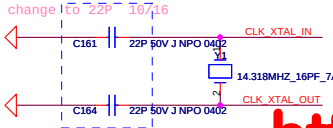




Add 1K follow
Intel check list 05/11

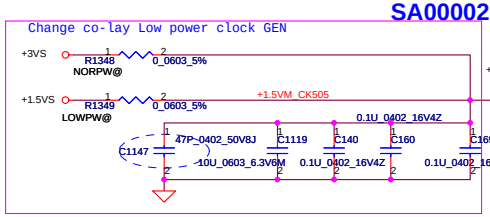
Follow Intel check list change to 27P 06/05

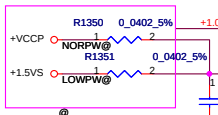
Follow Vendor check change to 22P 10/16



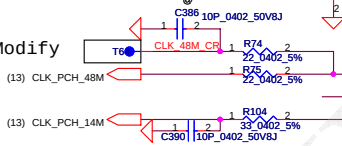
Routing the trace at least 10mil

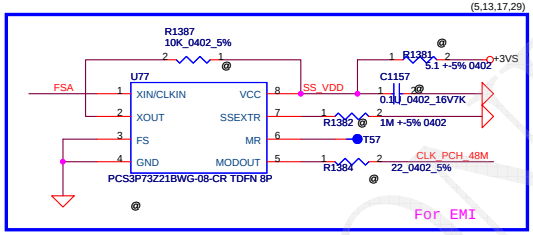
Change co-lay Low power clock GEN

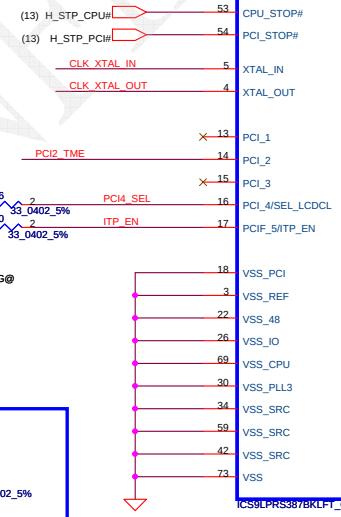




09/03 Modify



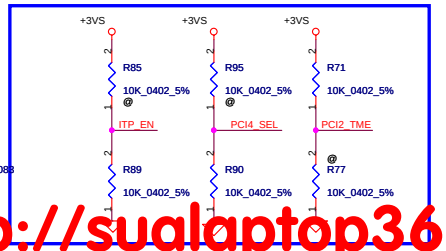




For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

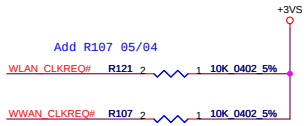
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed



SRC PORT LIST

PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN



REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	
REQ_11#	PCIE_WWAN
REQ_A#	

Security Classification	Compal Secret Data		
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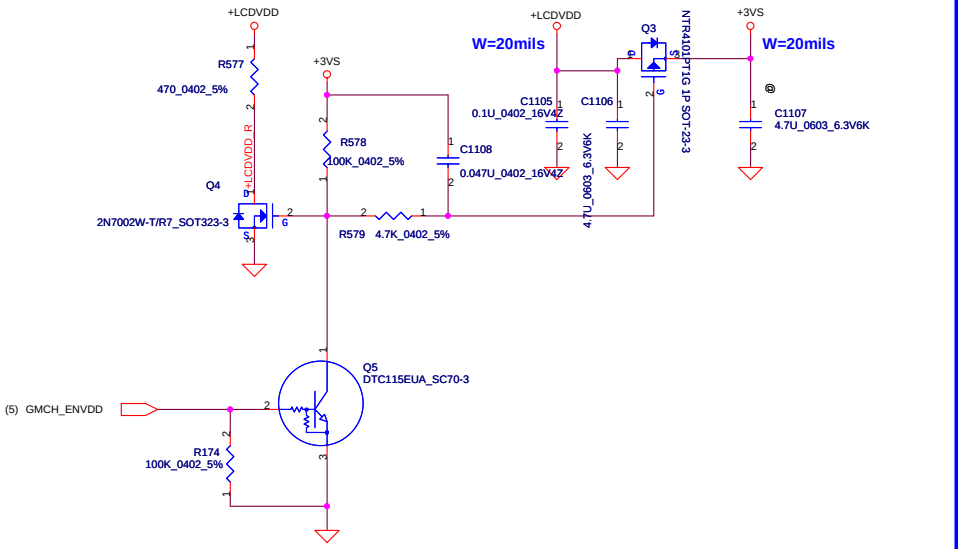
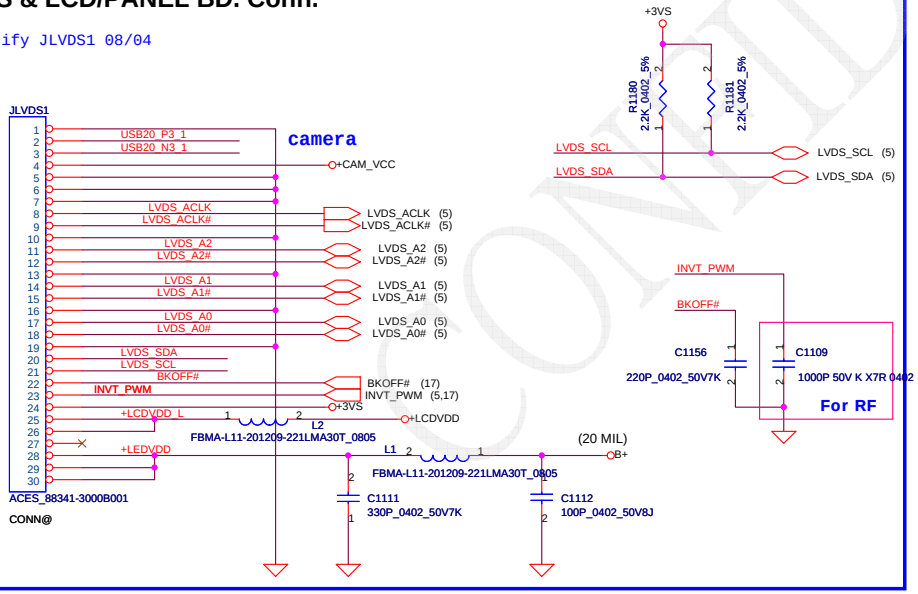
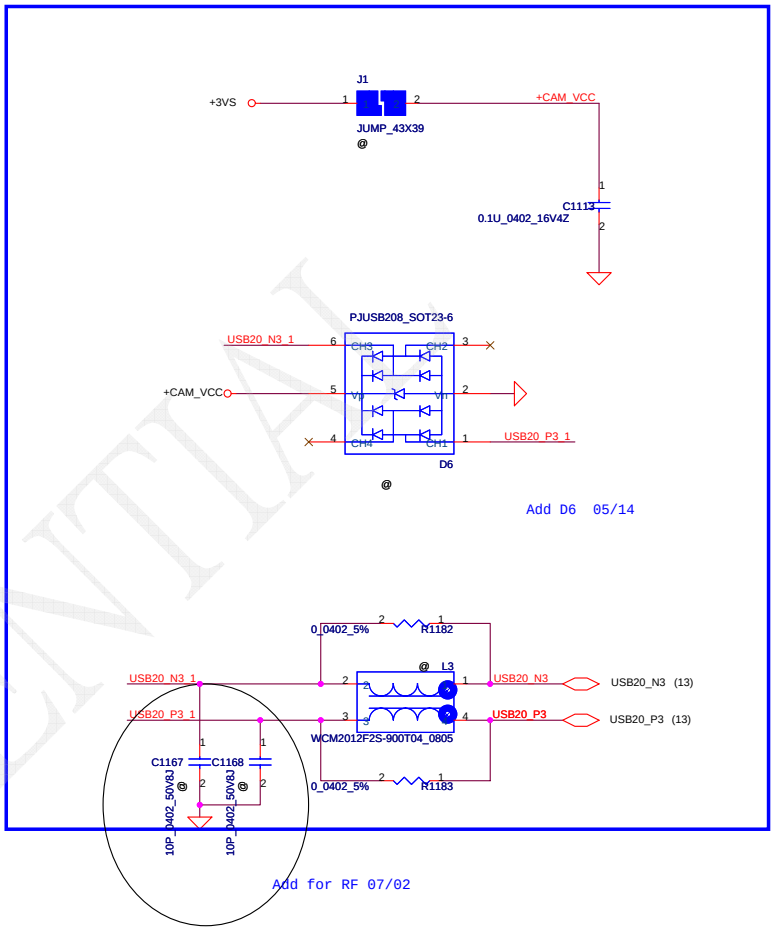
LCD POWER CIRCUIT



CMOS & LCD/PANEL BD. Conn.

Modify JLVDS1 08/04





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Close to CRT CONN for ESD.

Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615

(5) GMCH_CRT_R
(5) GMCH_CRT_G
(5) GMCH_CRT_B
(5) GMCH_CRT_HSYNC
(5) GMCH_CRT_VSYNC
(5) GMCH_CRT_DATA
(5) GMCH_CRT_CLK

R255 150_0402_1%
R253 150_0402_1%
R250 150_0402_1%

L15 BK1608LL121-T_2P
L14 BK1608LL121-T_2P
L12 BK1608LL121-T_2P

D18 PJDLC05C_SOT23-3
D17 PJDLC05C_SOT23-3

RED
GREEN
BLUE

C310 10P_0402_50V8J
C308 10P_0402_50V8J
C303 10P_0402_50V8J
C307 10P_0402_50V8J
C306 10P_0402_50V8J
C304 10P_0402_50V8J

JVGA_HS
JVGA_VS

+5VS
C301 0.1U_0402_16V4Z
R249 10_0402_5%
U11 SN74AHCT1G125DCKR_SC70-5
CRT_HSYNC_1

Place closed to chipset

C298 0.1U_0402_16V4Z
R247 10_0402_5%
U10 SN74AHCT1G125DCKR_SC70-5
CRT_VSYNC_1

Change CRT_DET# From Page 13 to Page 10 06/12

+3VS
R149 10K_0402_5%
High: CRT Plugged
(13) CRT_DET
CRT_DET
CRT_DET#
Q11 2N7002W-T/R7_SOT323-3

Add R1283 R1284
Change R247 R249 to 10 ohm
Add @ on U10 U11 C301 C298 06/08

CRT PORT

+3VS
R248 2.2K_0402_5%
R245 2.2K_0402_5%
+CRT_VCC
R246 2.2K_0402_5%
R251 2.2K_0402_5%
VGA_DDC_DAT
VGA_DDC_CLK
Q24B 2N7002DW-T/R7_SOT363-6
Q24A 2N7002DW-T/R7_SOT363-6

+5VS
D3 RB491D_SC59-3
W=40mils
+CRT_VCC
C142 0.1U_0402_16V4Z

Change JCRT1 P/N to SP010906182 06/22

JCRT1 CONN@
RED
VGA_DDC_DAT
GREEN
JVGA_HS
BLUE
JVGA_VS
VGA_DDC_CLK
SUYIN_070546FR015M21RZR

CRT_DET#
R1103 100K_0402_5%
+CRT_VCC

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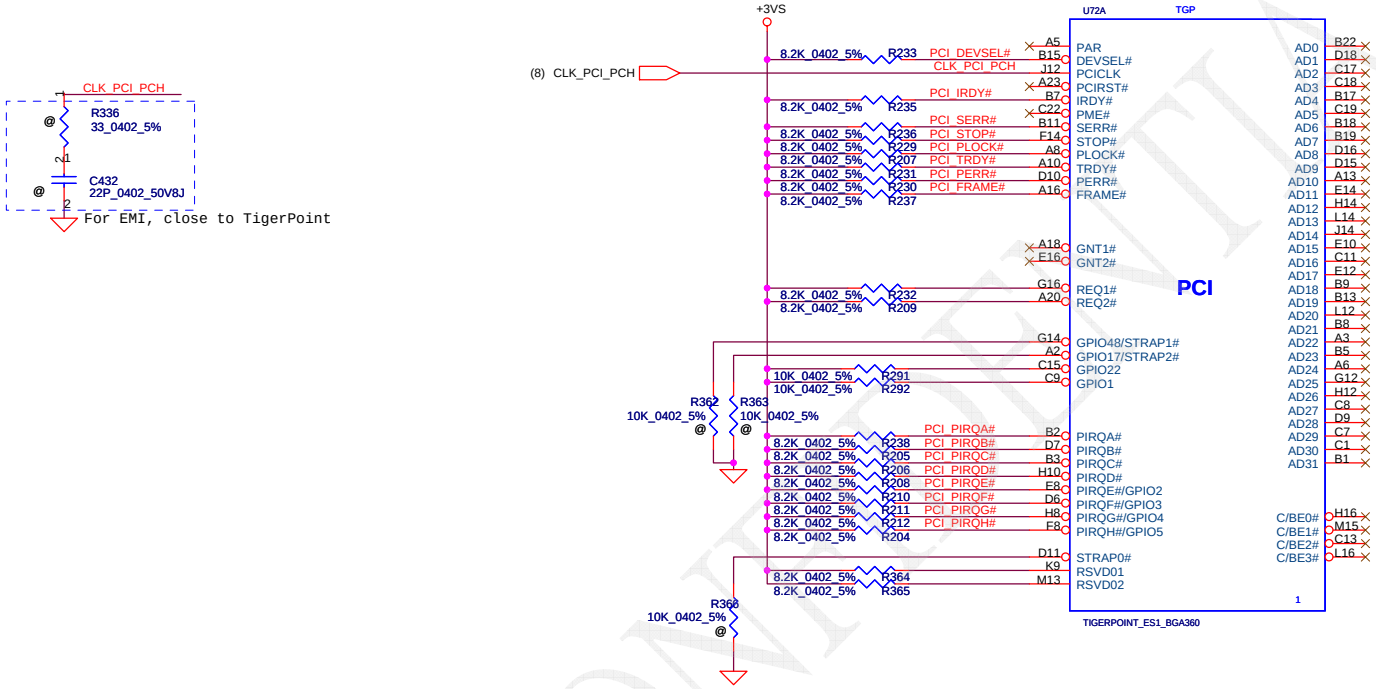

STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

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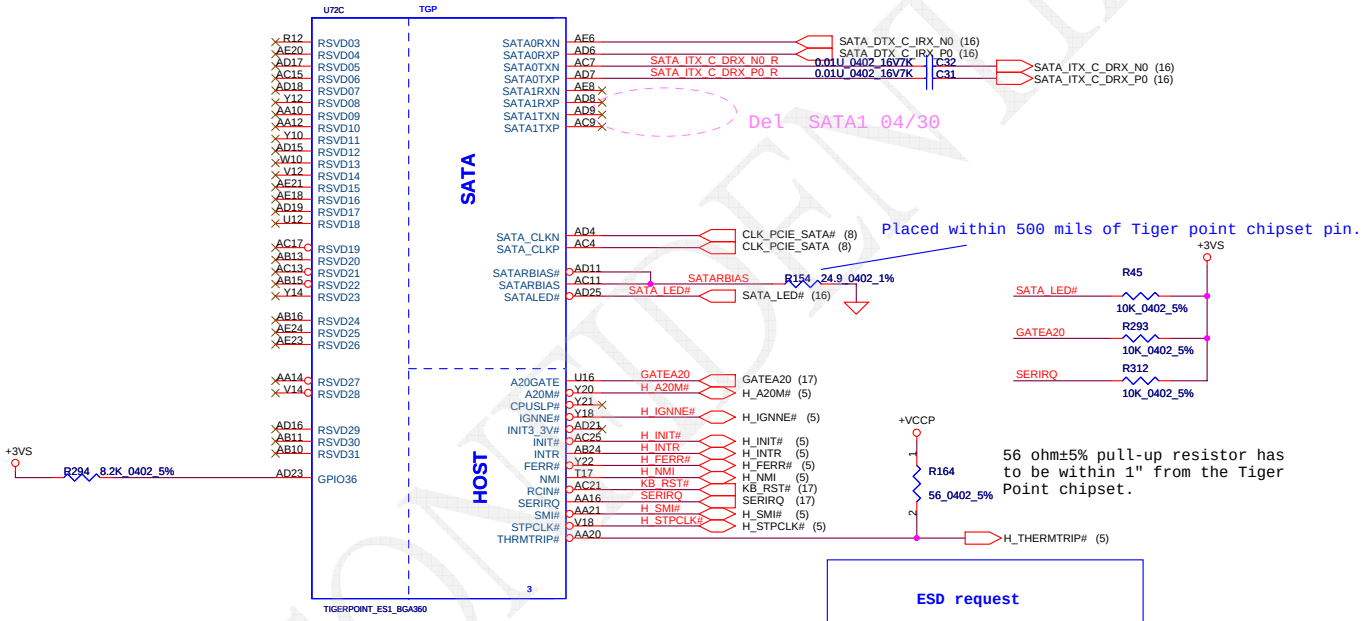

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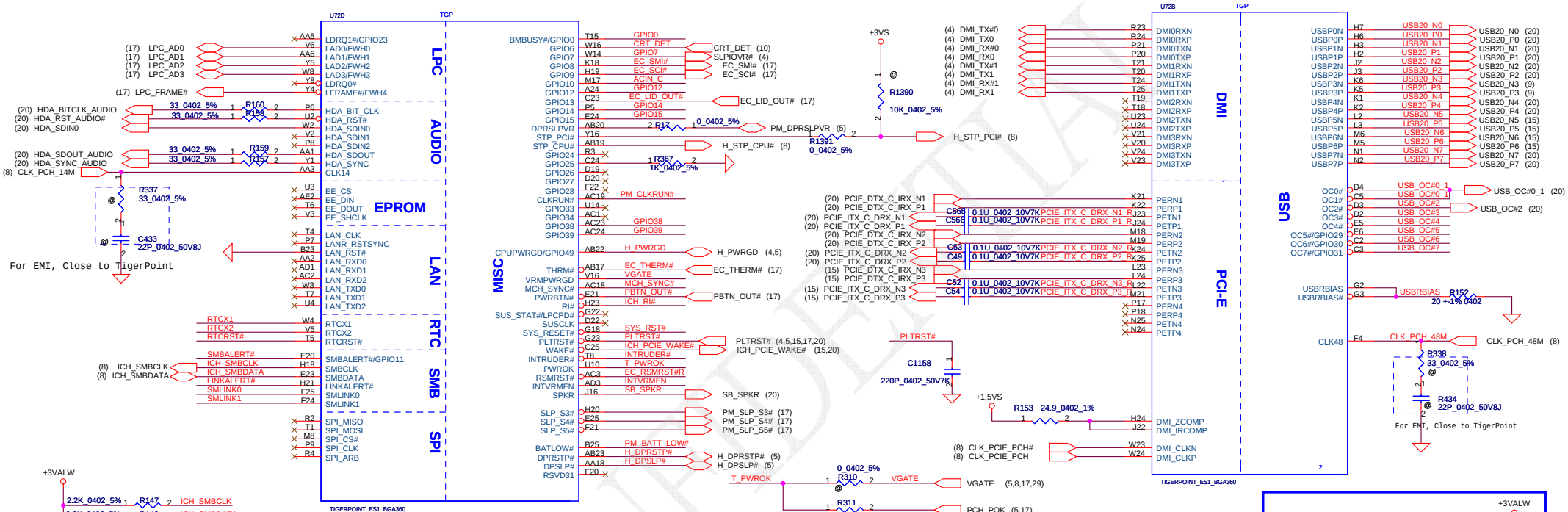
PCIE	Port List
1	LAN
2	WLAN
3	WWAN
4	

USB	Port List
0	USB Left1
1	USB Left2
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

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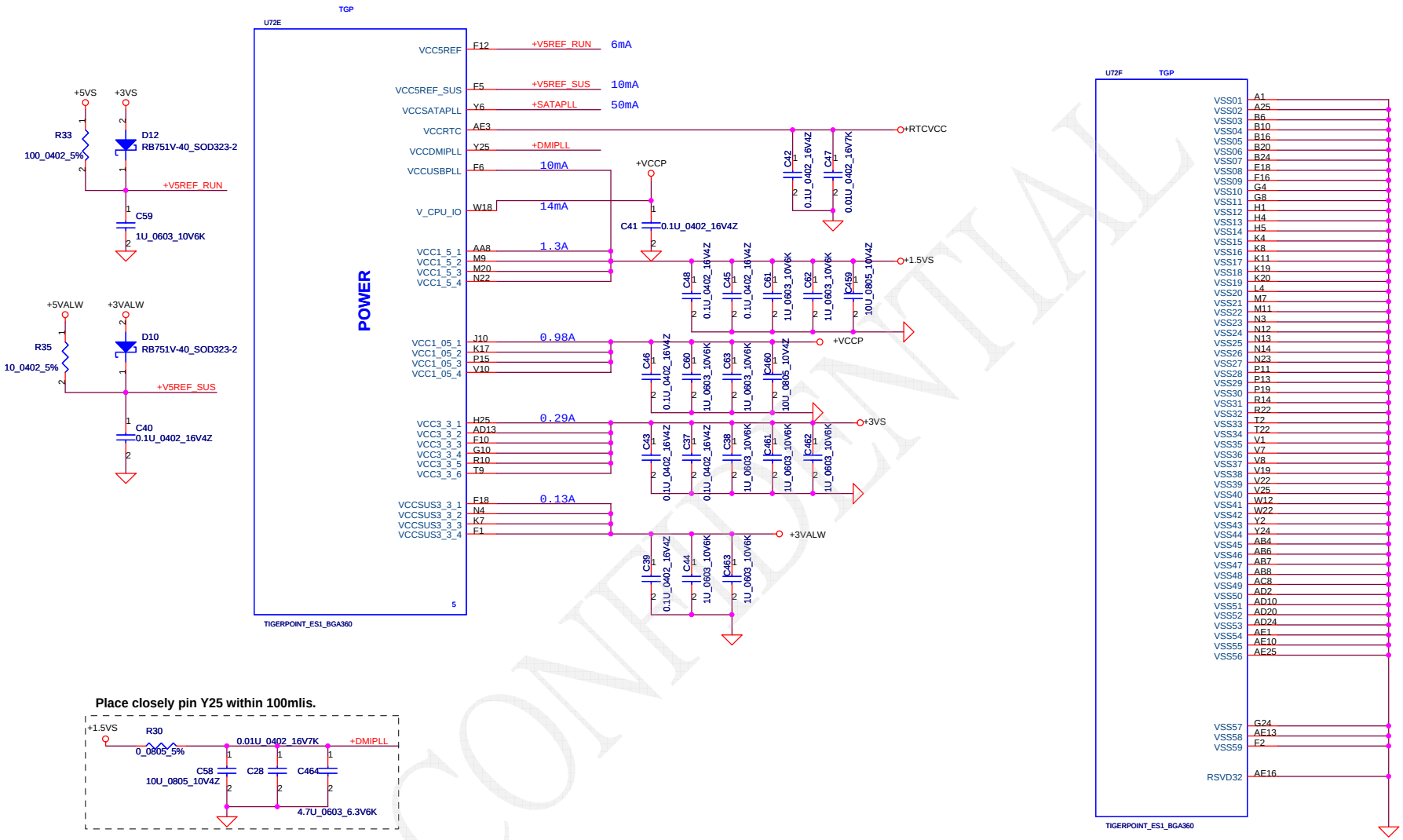

Security Classification	Compal Secret Data		
Issued Date	2009/04/15	Deciphered Date	2010/04/15

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Mini-Express Card for WWAN

Add C1163 C1164 C1165 C1166 06/23

Add C850 06/12

Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T 06/29

Change to PCIE_P3 05/13

Close to WWAN CONN

BT MODULE CONN

(9~16mA)

Reserve for SIM card does not meet rise time and pull-up is needed.

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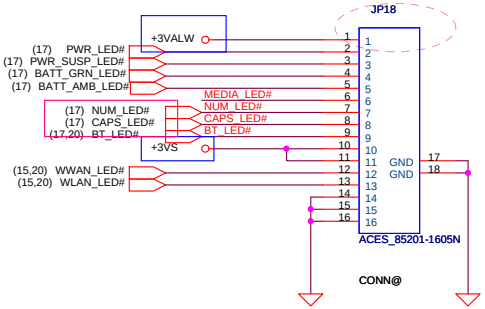
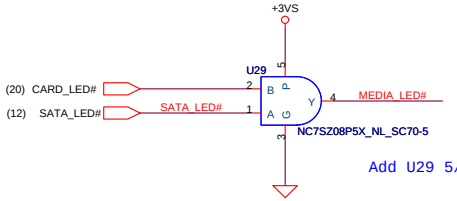
ADD LED PCB CONN 06/12

Change JP18 to NEW P/N 06/23

09/03 Change +5VALW , +5VS to +3VALW +3VS

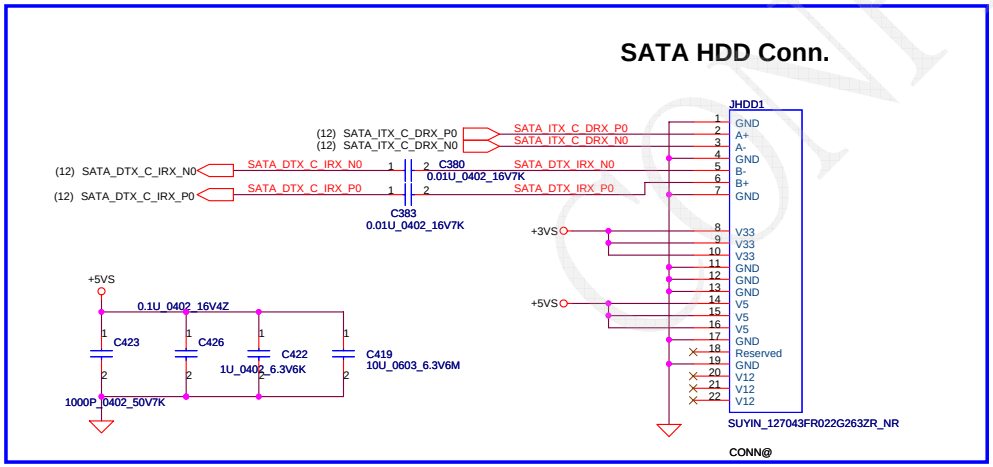
LED PCB CONN





Add U29 5/14

SATA HDD Conn.



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Change R1292 to 0 ohm for BRD ID R01 (EVT) 06/24

BOARD ID Table

	VCC	3.3V				
	Ra	100K				
	ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max
NAV50	0	R01 (EVT)	0	0V	0V	0V
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
	2	R03 (PVT)	18K	0.436V	0.503V	0.538V
	3	R10A (MP)	33K	0.712V	0.819V	0.875V
NAV60	4	R01 (EVT)	56K	1.036V	1.185V	1.264V
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V
	7	R10A (MP)	NC	2.500V	3.3V	3.3V

	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_OFF# Swap to WLAN	v	v		Low

	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#

Change INVT_PWM from Pin21 to Pin25 06/24

Change BT_ON# from Pin98 to Pin108 06/24

Add 0 ohm R1309 06/08

Del R1294 06/08

Change to R_0402 05/14

EC DEBUG PORT

8M SPI ROM

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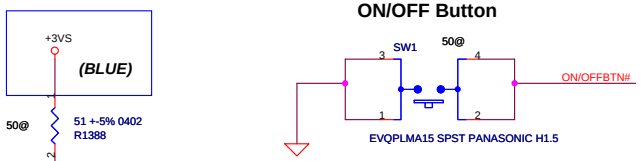
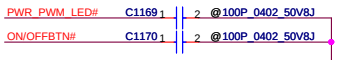
Add For NAV50 07/06

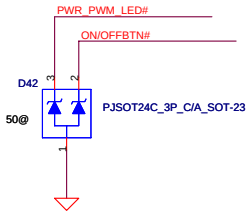
09/03 Change +5VS to +3VS

ON/OFF Button



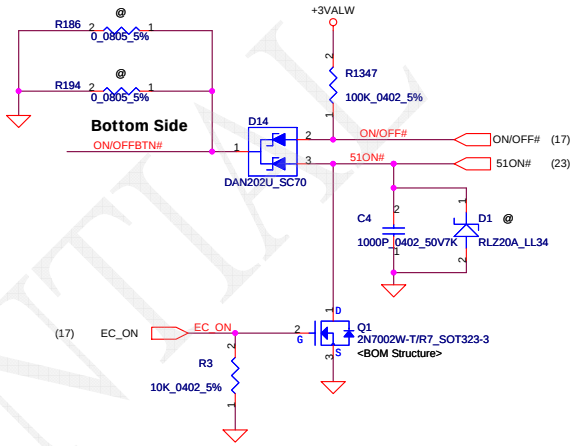
FOR EMI



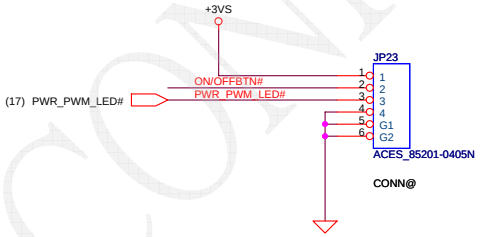


TOP Side

Bottom Side

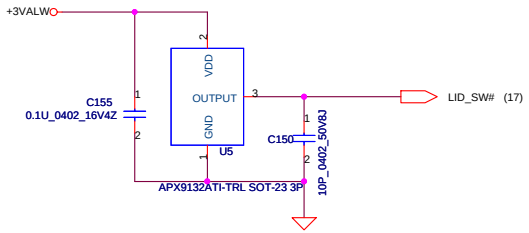


PWR/B Conn



Update PW/B Conn 0623

LID Switch



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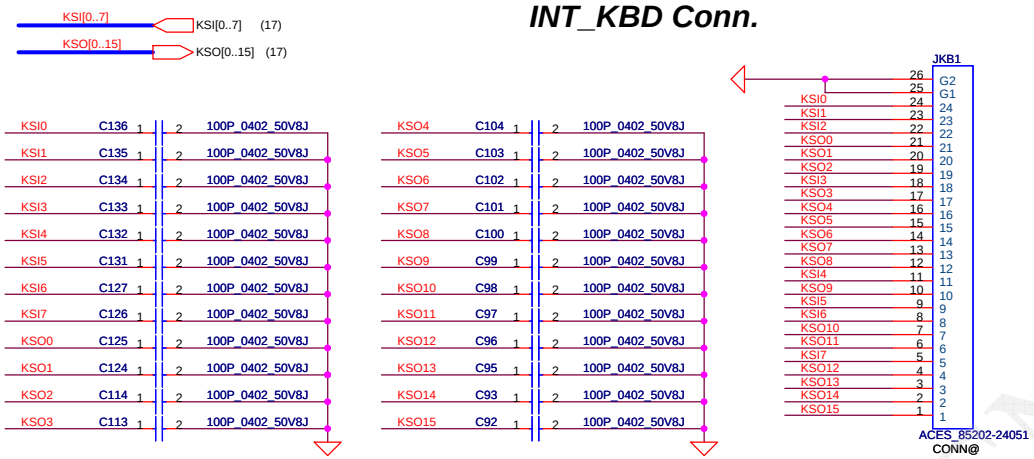
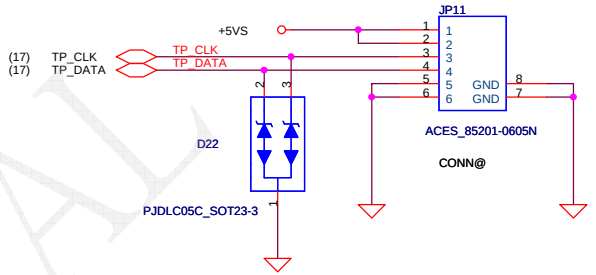
INT_KBD Conn.



To TP/B Conn.



Chage JP11 Pin define & Add D22 05/14

Update TP/B Conn 05/04

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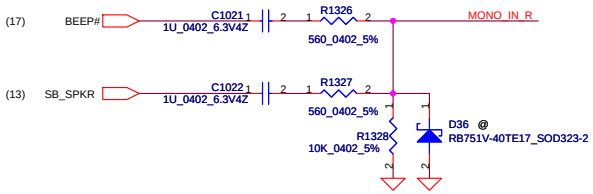
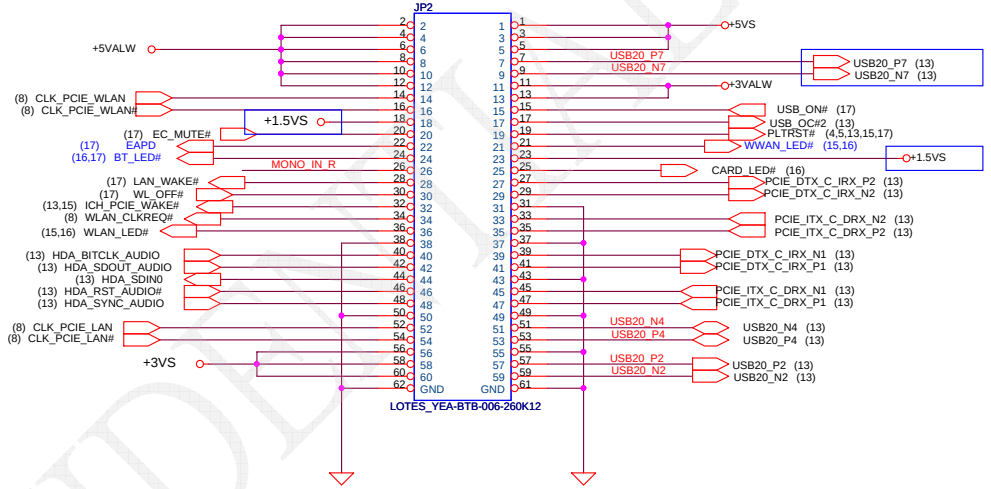
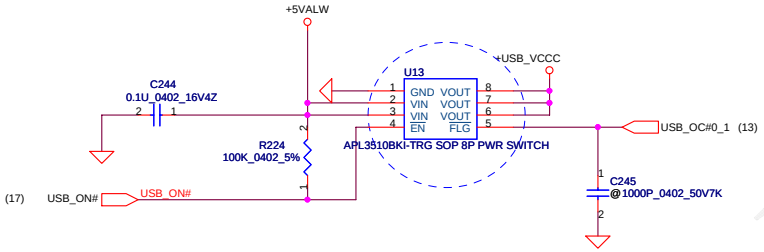
09/03 Change Pin 18, 23 to +1.5VS change Pin7 , 9 to USB20_P7 N7

I/O Board Conn.

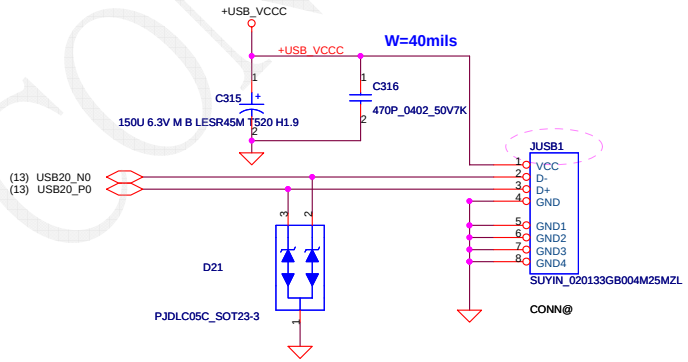




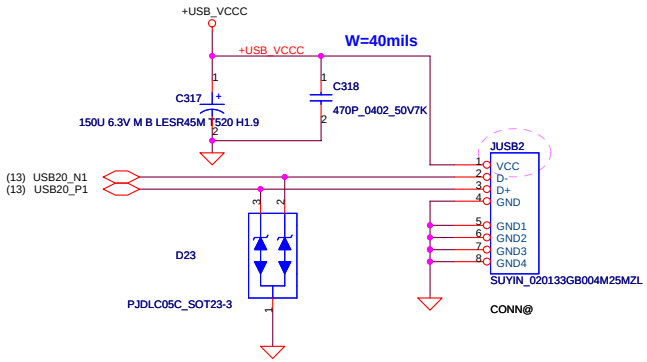


Change JUSB1 JUSB2 to NEW P/N SP010906181 06/23

USB CONN.1



USB CONN.2



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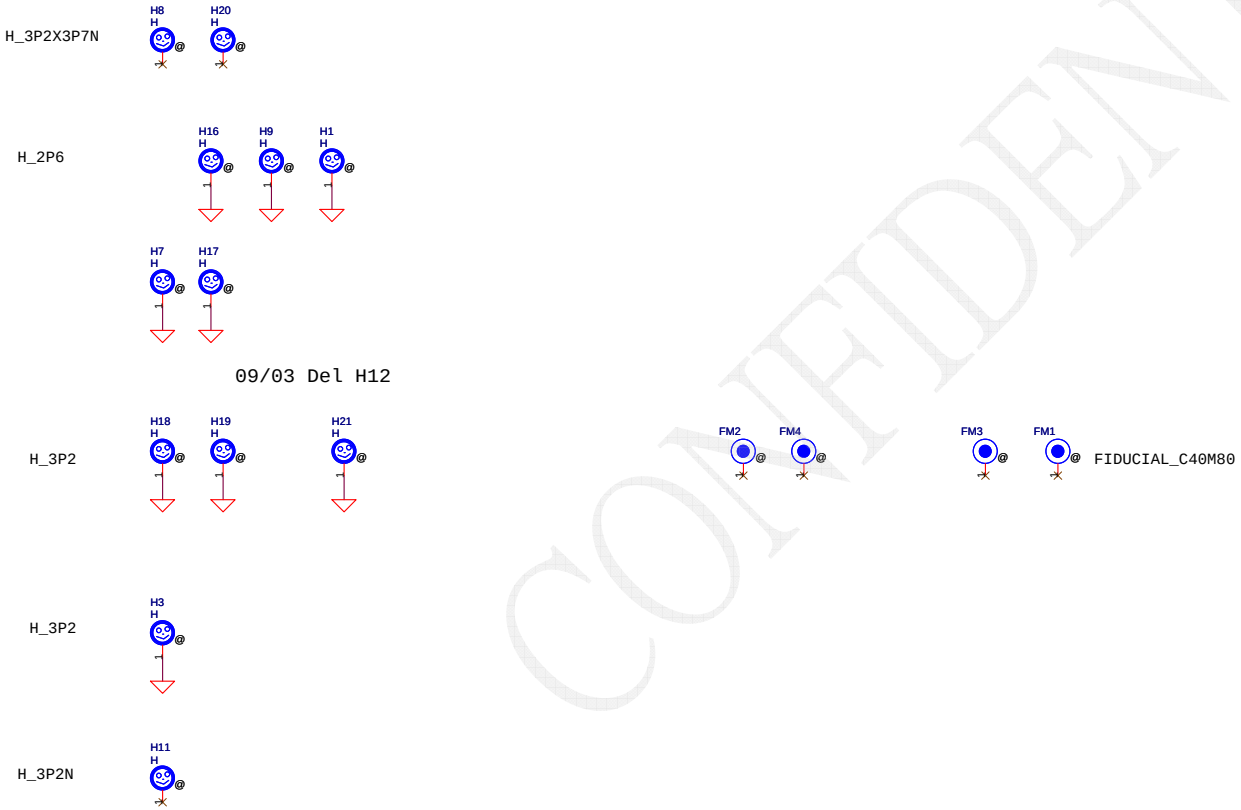
Modify Hole location by (ME Drawing 06/12) 0615



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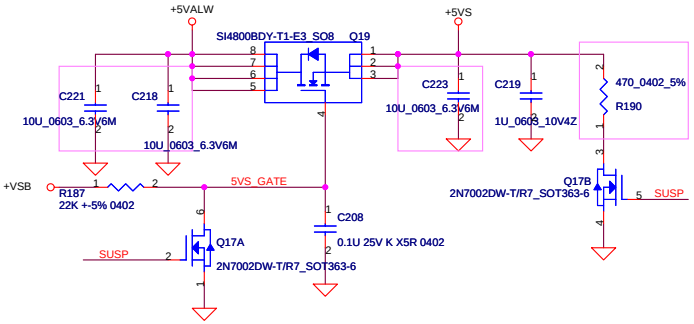
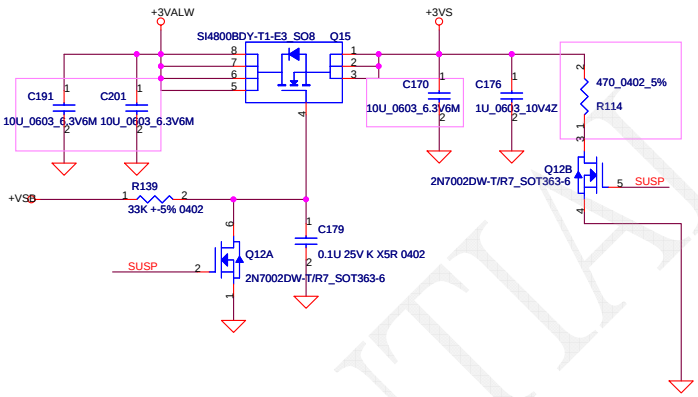
Change R51 R57 R70 R63 R317 R114 R190 to 0402 SIZE 04/30
Change C221 C218 C223 C 191 C201 C170 C392 C393 C394 to 0603 SIZE 04/30

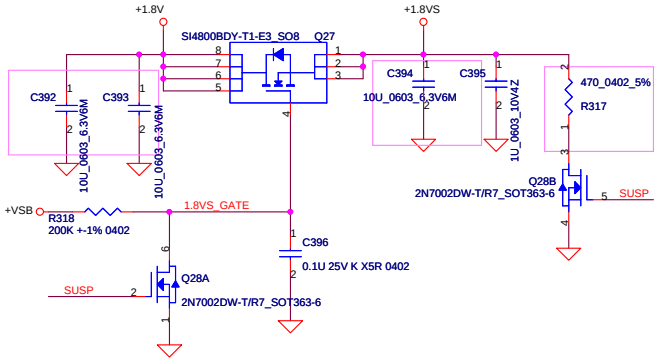
+5VALW TO +5VS

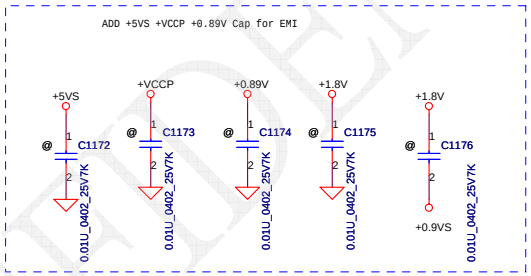


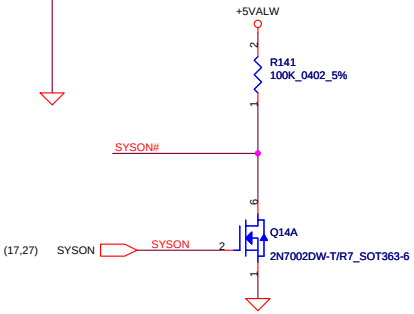
+3VALW TO +3VS

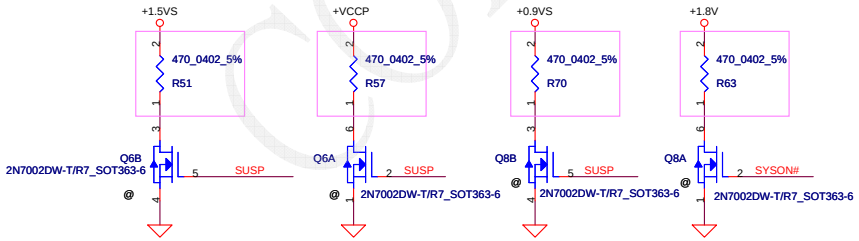


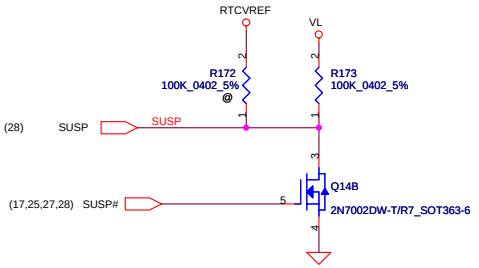
+1.8V to +1.8VS











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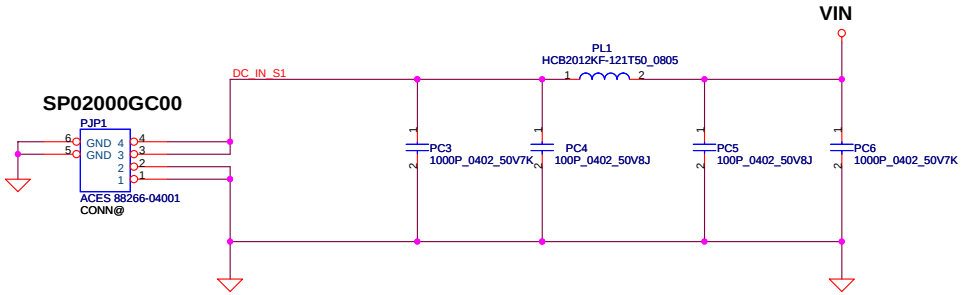
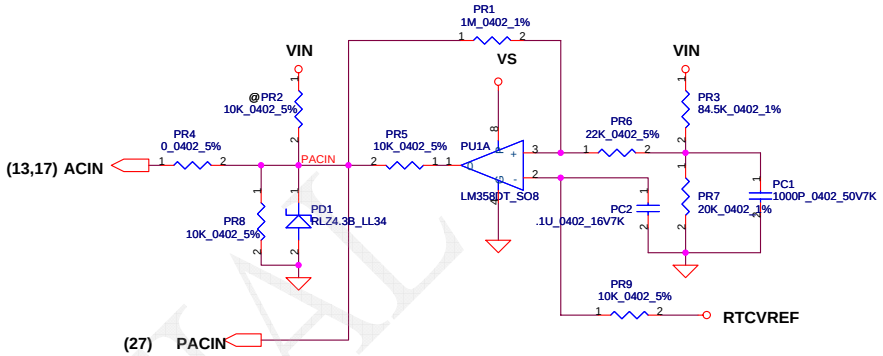
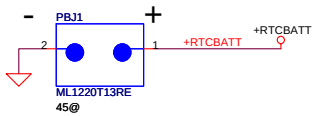
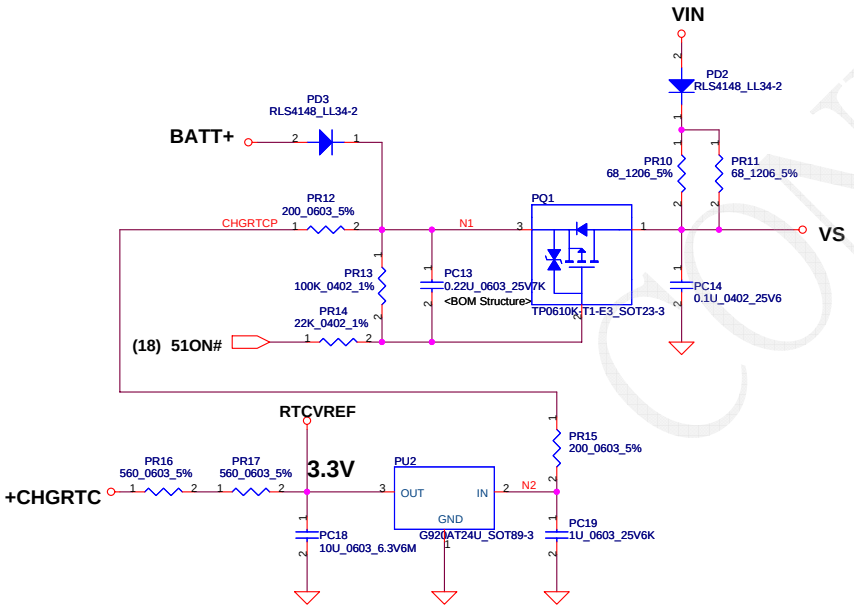


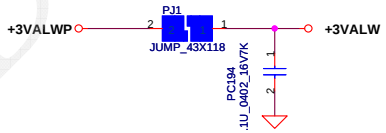


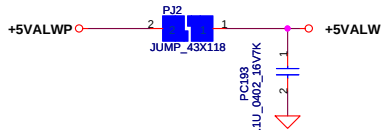


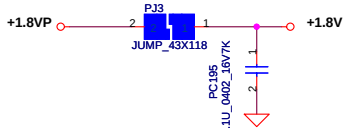
Vin Dectector

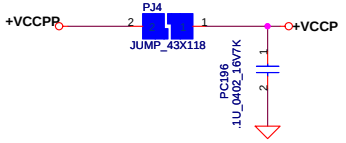
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

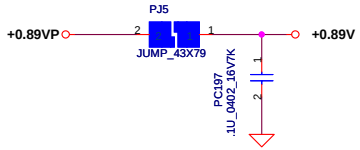












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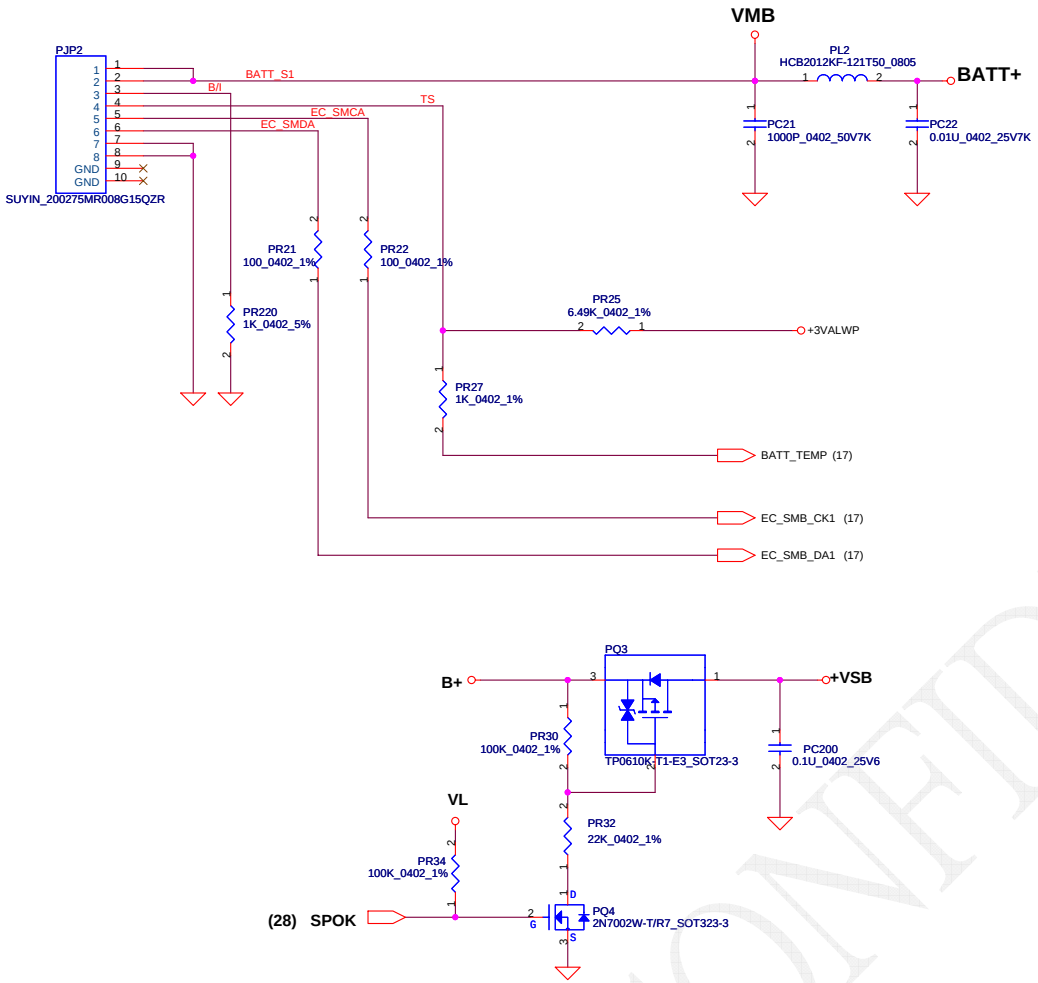
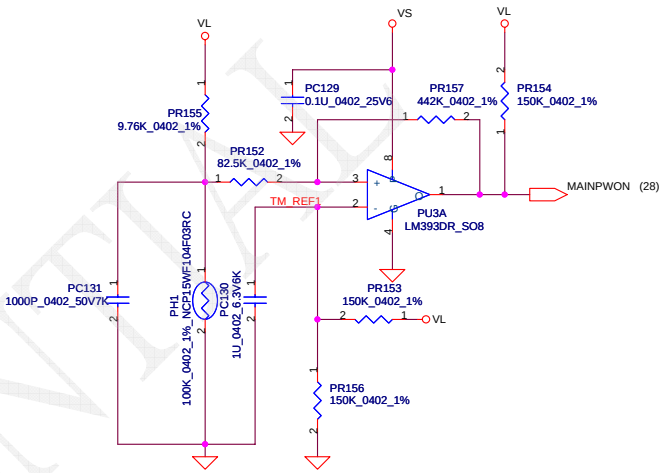
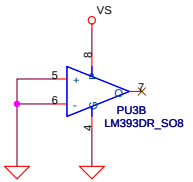


PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C





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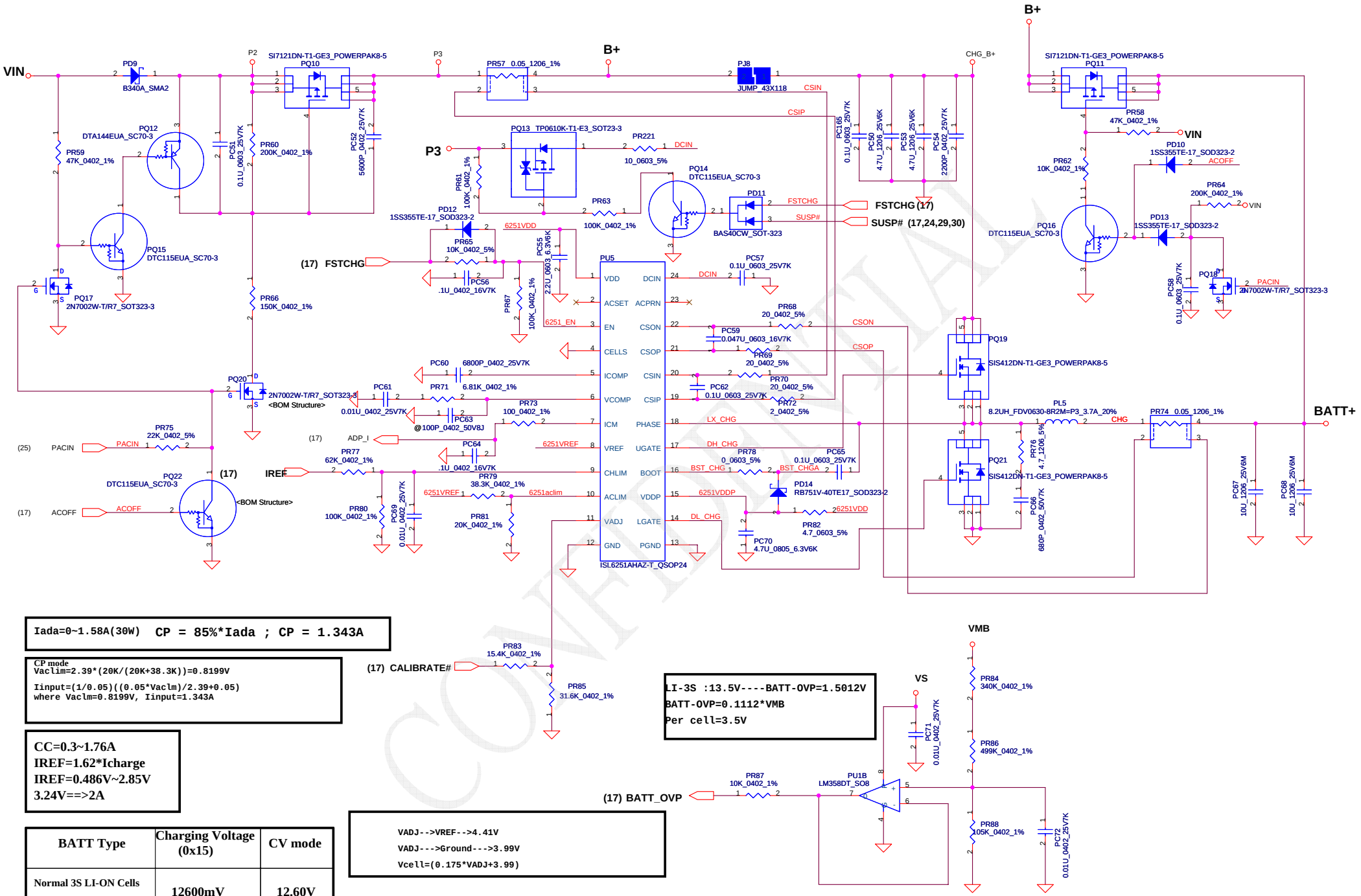

Iada=0~1.58A(30W) CP = 85%*Iada ; CP = 1.343A

CP mode
Vaclim=2.39*(20K/(20K+38.3K))=0.8199V

Iinput=(1/0.05)((0.05*Vaclm)/2.39+0.05)
where Vaclm=0.8199V, Iinput=1.343A

CC=0.3~1.76A
IREF=1.62*Icharge
IREF=0.486V~2.85V
3.24V==>2A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

VADJ-->VREF-->4.41V
VADJ--->Ground--->3.99V
Vcell=(0.175*VADJ+3.99)

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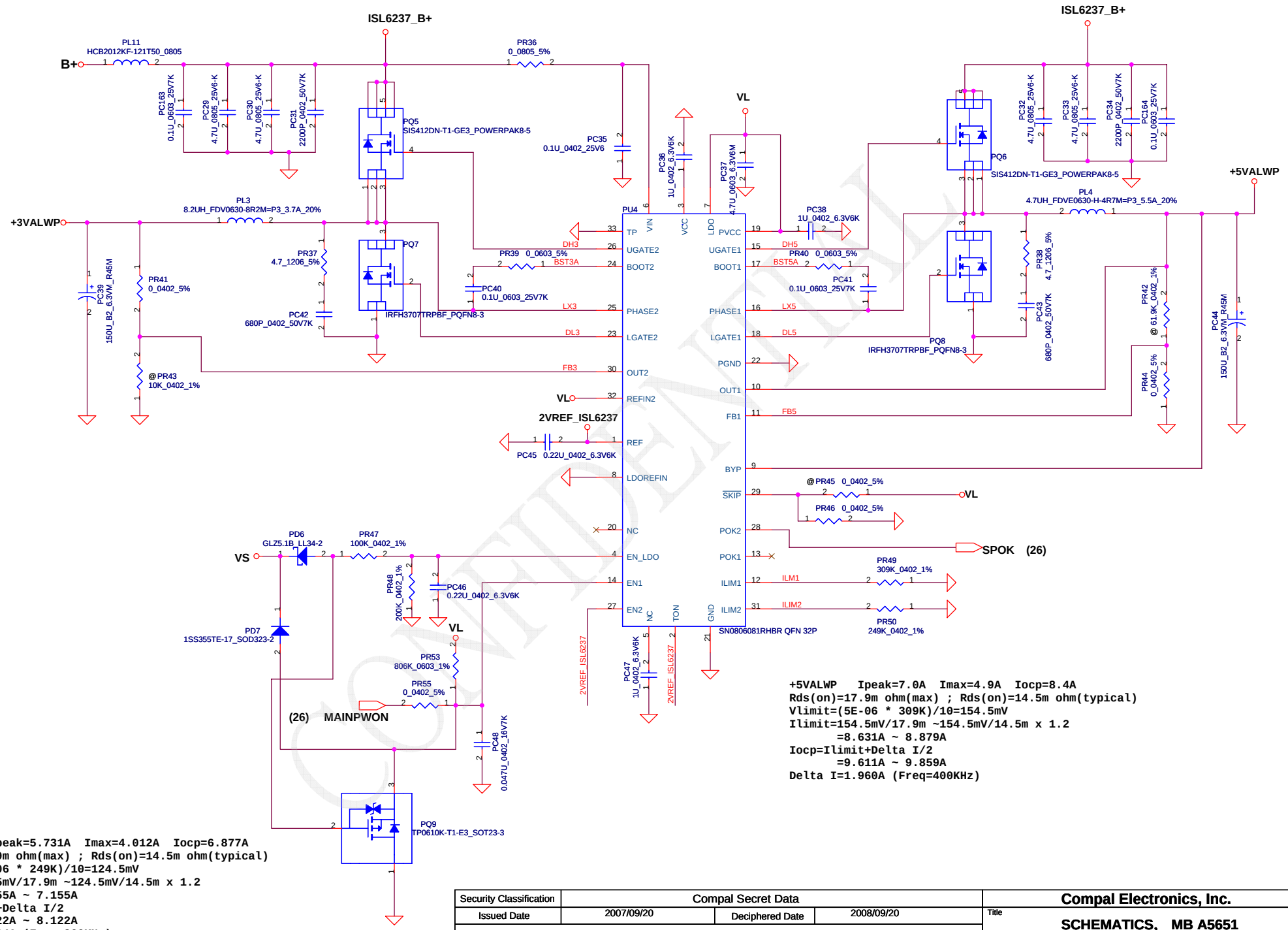

+5VALWP Ipeak=7.0A Imax=4.9A Iocp=8.4A
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vlimit=(5E-06 * 309K)/10=154.5mV
Ilimit=154.5mV/17.9m ~154.5mV/14.5m x 1.2
=8.631A ~ 8.879A
Iocp=Ilimit+Delta I/2
=9.611A ~ 8.859A
Delta I=1.960A (Freq=400KHz)

+3.3VALWP Ipeak=5.731A Imax=4.012A Iocp=6.877A
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vlimit=(5E-06 * 249K)/10=124.5mV
Ilimit=124.5mV/17.9m ~124.5mV/14.5m x 1.2
=6.955A ~ 7.155A
Iocp=Ilimit+Delta I/2
=7.922A ~ 8.122A
Delta I=1.934A (Freq=300KHz)

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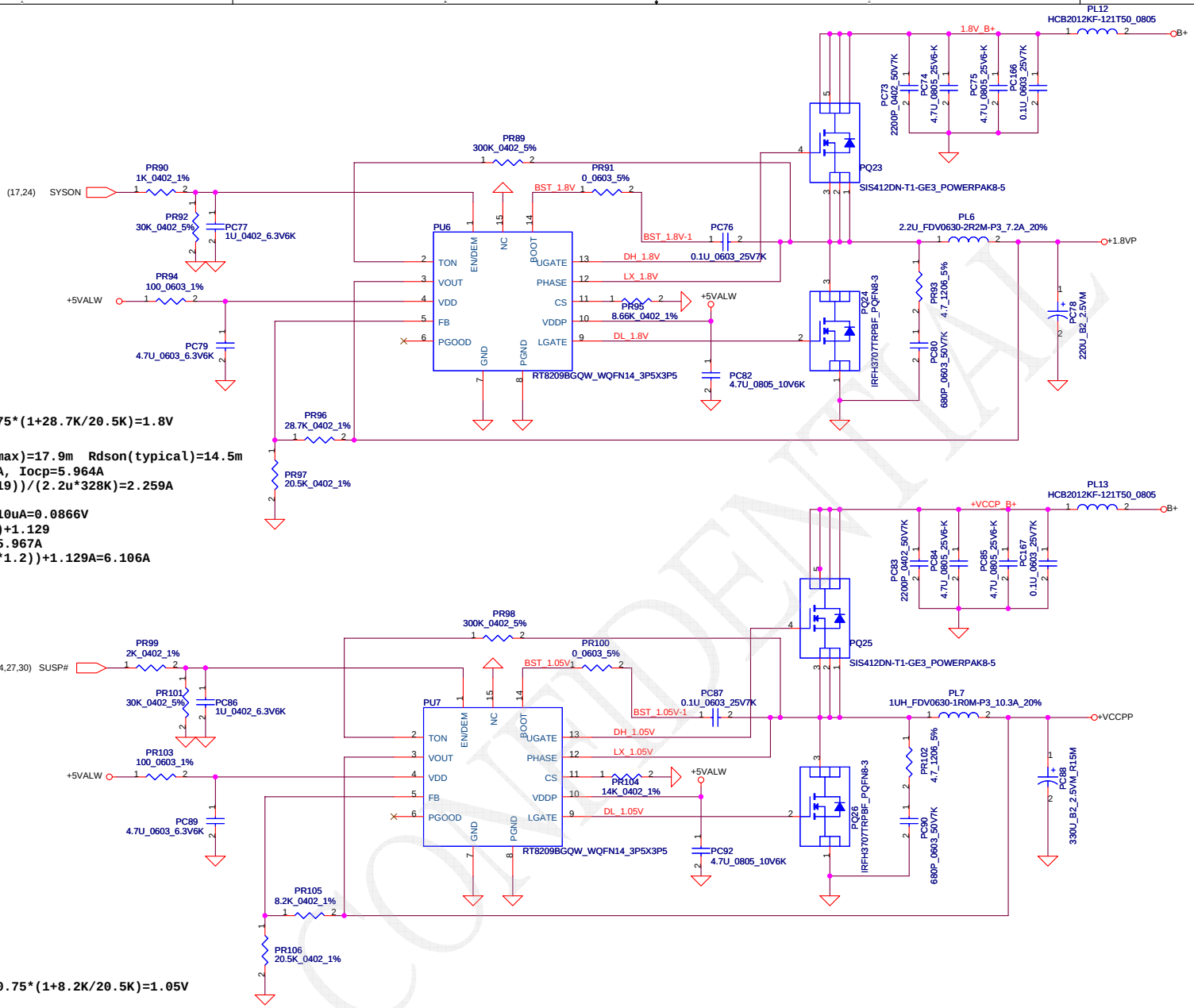

<Vo=1.8V> VFB=0.75V
Vo=VFB*(1+PR96/PR97)=0.75*(1+28.7K/20.5K)=1.8V
Fsw=328KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(typical)=14.5m
Ipeak=4.97A, Imax=3.479A, Iocp=5.964A
Delta I=((19-1.8)*(1.8/19))/(2.2u*328K)=2.259A
=>1/2DeltaI=1.129A
Vtrip=Rtrip*10uA=8.66K*10uA=0.0866V
Iocpmin=Vtrip/(Rdsonmax)+1.129
=0.0866/(0.0179)+1.129=5.967A
Iocpmax=(0.0866/(0.0145*1.2))+1.129A=6.106A
Iocp=5.967A~6.106A

<Vo=1.05V> VFB=0.75V
Vo=VFB*(1+PR105/PR106)=0.75*(1+8.2K/20.5K)=1.05V
Fsw=280KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(typical)=14.5m
Ipeak=3.124A, Imax=2.187A, Iocp=3.749A
Delta I=((19-1.05)*(1.05/19))/(1.5u*280K)=3.549A
=>1/2DeltaI=1.774A
Vtrip=Rtrip*10uA=14K*10uA=0.14V
Iocpmin=Vtrip/(Rdsonmax)+1.774
=0.14/(0.0179)+1.774=9.596A
Iocpmax=(0.14/(0.0145*1.2))+1.774A=9.820A
Iocp=9.596A~9.820A

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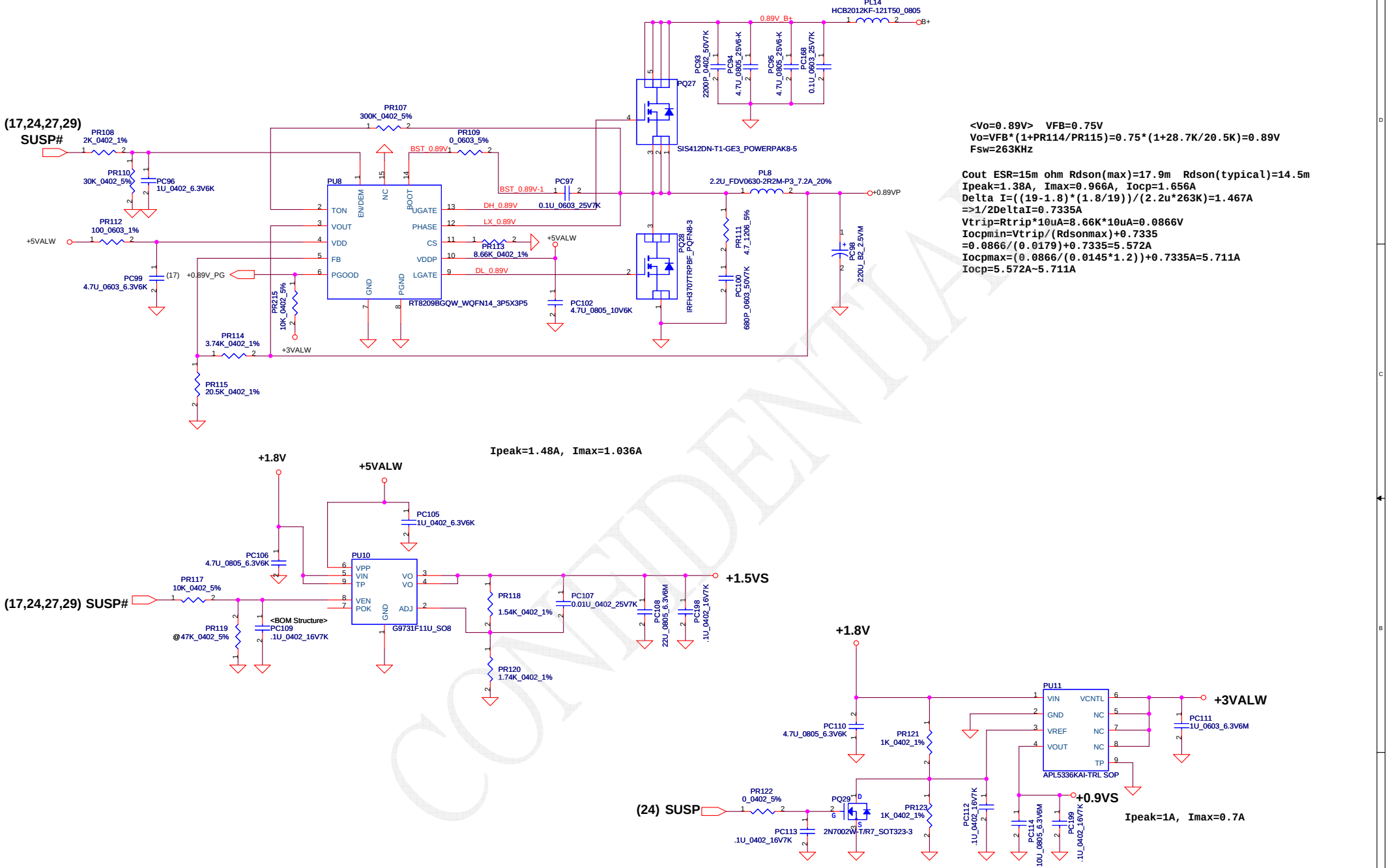

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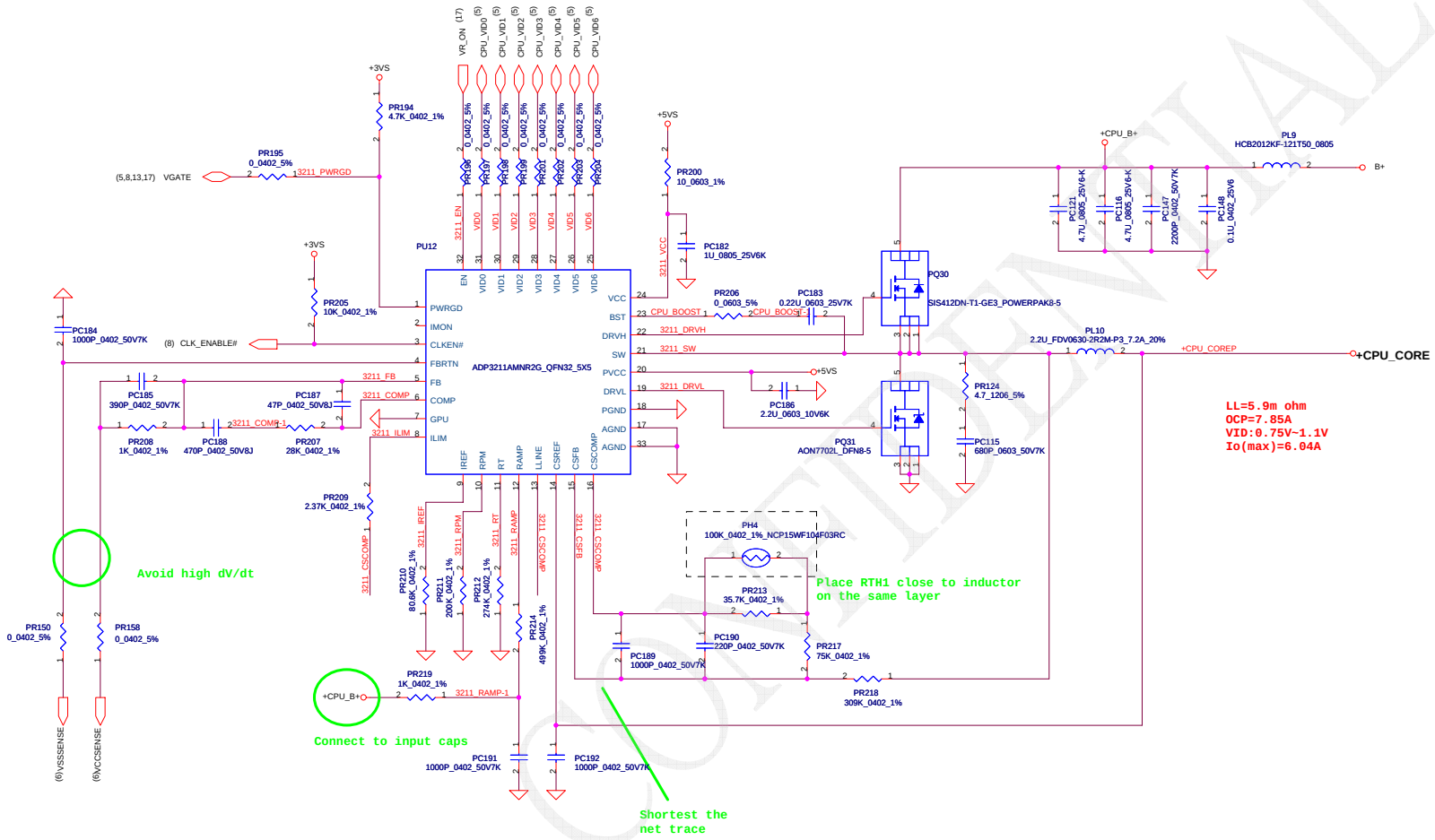

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add PC200	For design change	0.1	24		2009.5.15	EVT
2	add PC193,PC194	For design change	0.1	26		2009.5.15	EVT
3	add PC195,PC196	For design change	0.1	27		2009.5.15	EVT
4	add PC197,PC198,PC199	For design change	0.1	28		2009.5.15	EVT
5	change PL3,PL4	For design change	0.1	26	change PL3,PL4 to 4.7uH	2009.5.15	EVT
6	change PQ10,PQ11	For design change	0.1	25	change PQ10,PQ11 to P-Chanel	2009.6.5	EVT
7	add PC165	Solution for 3G noise reduce	0.1	25		2009.6.5	EVT
8	add PC163,PC164	Solution for 3G noise reduce	0.1	26		2009.6.5	EVT
9	add PC166,PC167	Solution for 3G noise reduce	0.1	27		2009.6.5	EVT
10	add PC168	Solution for 3G noise reduce	0.1	28		2009.6.5	EVT
11	delete PC103,PC1120	For design change	0.1	29		2009.6.5	
12	change PR94,PR102	For design change	0.1	27	change PR94,PR102 to 100ohm	2009.6.5	
13	change PC79,PC89	For design change	0.1	27	change PC79,PC89 to 4.7uF	2009.6.5	
14	change PR112	For design change	0.1	28	change PR112 to 100ohm	2009.6.5	
15	change PC99	For design change	0.1	28	change PC99 to 4.7uF	2009.6.5	
16	change +5VALW/+3VALW OCP	For design change	0.1	26	change PR49 to 309ohm & PR50 to 249ohm	2009.6.5	
17	add PJ1,PJ2,PJ3,PJ4,PJ5,PJ6,PJ7	For design change	0.1	25		2009.6.15	
18	add PJ9,PJ10	For design change	0.1	28		2009.6.15	
19	Change net name	For design change	0.1	25	Change net name +1.05V to +VCCP	2009.6.15	
20	Change PJP2	For design change	0.1	24	Change PJP2 to DC040903020	2009.6.15	
21	Change PBJ1	For design change	0.1	23	Change PBJ1 to SP020008Y00	2009.6.15	
22	delete PJ6,PJ7,PJ9,PJ10	For design change	0.1	28		2009.6.18	
23	Change net name	For design change	0.1	29	Change net name GND_SIGNAL to GND	2009.6.18	

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change PR194	For design change	0.1	29	change PR194 to 4.7K ohm	2009.6.30	EVT
2	add PR221	For design change	0.1	25		2009.6.30	EVT
3	Change PR4	For design change	0.1	23	change PR4 to 0 ohm	2009.7.2	EVT
4	Change PJP3 to PBJ1	For design change	0.1	23	change SP020008Y00 to SP093MX000	2009.8.4	EVT
5	Change PH1 & PH4	For design change	0.1	24	change SL210031F00 to SL200000V00	2009.8.12	EVT
6	Change PL10	For design change	0.1	29	change SH000006I80 to SH000000700	2009.8.12	EVT
7	Change PR99 & PR108	Modify power sequence	0.1	27	change SD028000080(0 ohm) to SD034200280(20K ohm)	2009.8.12	EVT
8	Change PR90	Modify power sequence	0.1	27	change SD028000080(0 ohm) to SD034100280(10K ohm)	2009.8.12	EVT
9	Change PR83	Modify ISL6251 Charger KV	0.1	25	change SD034182280(18.2 ohm) to SD034154280(15.4K ohm)	2009.8.24	EVT
10	Change PR117	Modify power sequence	0.1	28	change SD028000080(0 ohm) to SD034100280(10K ohm)	2009.8.24	EVT
11	Change PR99 & PR108	Modify power sequence	0.1	27	change SD034200280(20K ohm) to SD034200180(2K ohm)	2009.8.24	EVT
12	Change PR90	Modify power sequence	0.1	27	change SD034100280(10K ohm) to SD034100180 (1K ohm)	2009.8.24	EVT
13	Change PC77 & PC86 & PC96	Modify power sequence	0.1	27	Change PC77 & PC86 & PC96 to pop change SE076104KM8(0.1uf) to SE000000K80 (1uf)	2009.8.24	EVT
14	Change PC109	Change part number	0.1	27	change SE076104KM8(0.1uf) to SE076104K80(0.1uf)	2009.8.24	EVT
15	Change PL3.PL4	To slove high frequency noise	0.1	26	change SH00000BU00(4.7uH) to SH00000BS00(8.2uH)	2009.8.27	EVT
16	Change PL9	For design change	0.1	29	change SM01000BY00 to SM01000C000	2009.9.4	DVT
17	Change PL4	To improve +5VALWP efficiency	0.1	26	change SH00000BS00(8.2uH) to SH00000F900(4.7uH)	2009.9.10	DVT
18	Change PR209	Modify CPU CORE OCP	0.1	29	change SD028180180(1.8K ohm) to SD034237180 (2.37K ohm)	2009.9.30	PVT
19							
20							
21							
22							
23							

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<2009/4/28>
Update new power schematic,
release first version NAV50 schematic

<2009/04/29>
. Add R1182 R1183 L3 on page 9
. Change J3 to R1184 on page 13

<2009/04/30>
. Change JDIM1 to SP07F001720 on page 7
. Del SATA1 Port on page 12
. Change R51 R57 R70 R63 R317 R314 R190 to 0402 Size on page 21
<2009/05/04>
. Add WWAN_CLKREQ# and R107 pull-high to +3VS on page 8
. Add CRT_DET# on page 10
. Add CRT_DET# circuit on page 13
. Add 3 LEDS on page 16
. Add BT/BTN Board CONN. on page 16
. Update TP/B CONN. to SP01000LB00 on page 19

<2009/05/11>
. Add INVT_PWM on Page 5
. Del R323 on page 5
. C74 change to 2.2U_0603 on page 6
. C267 change to 22U on page 6
. C391 change to 0.1U on page 6
. Del C67 C35 C33 C36 on page 6
. Del +LGI_VID and U71.A21 direct connect to +VCCP on page 6
. Follow Intel checklist, add R52 on FSB on page 8
. Add D5 D7 D8 on page 4
. Add R174 on page 9
. Add PCI_RST# on page 11
. Add C1115 C1114 C1116 C1117 C1118 on page 15

<2009/05/12>
. Follow Intel Layout Checklist, Add C141 on VDDSPD on page 7
. Modify SRC CLK PORT LIST on page 8
. Del CLKREQ_LAN# on page 8
. Change PCIE Port list on page 13
. Change USB Port list on page 13
. Add W/L 3G SW on page 16
. Del R103 on page 18

<2009/05/13>
. Change JMINI1 to PCIE Port 3 on page 15
<2009/05/14>
. Page8 Change C174 C175 to 10U_0603

<2009/05/14>
. Update New Power schematic
. Del R376 R377 on page 8
. Del D5 D7 D8 on page 4
. Change JLVDS1 to SP010006810 on page 9
. Add D6 for EMI on page 9
. Change C1106 to C_0603 type on page 9
. Change USB_OC# on page 13
. Add USB Port2 on page 20
. Change JP11 Pin define & Add D22 on page 19
. Change C512 to 1u_0402 on page 15
. Add U29 (MEDIA_LED#)) on page 16

<2009/05/19>
.Update new clock GEN co-lay schematic on page 8

<2009/06/05>
.Update new clock GEN co-lay schematic on page 8
.Follow Intel check list change C161 C165 to 27P on page 8
.Follow Intel check list change C56 to 22uF on page 6

<2009/06/08>
.Update New Power schematic 06/06 version
Page 13- a.Del R203 (pull-up GPIO6 Resister)
b.Change R1184 NU
Page 17- a. Add VGATE
b. Del R1294
c. Change D30 NU
d. Change R1295 to 0 ohm
e. Add R1309 0 ohm on EC_RSMRST#
f. Pull-up LAN_WAKE# +3VALW
g. ICH_POK change to PCH_POK
h. Pull-up KB_RST# to +3VS
Page 10- a. Add R1283 R1284 ,Change R247 R249 to 10 ohm
b. Add @ on U10 U11 C301 C298
c. Del C302 C300 R1281 R1287

<2009/06/10>
. Page 7- Add C116 @
. Page 22- Modify USB_OC#1_2 to USB_OC#2
. Page 17- Modify PLTRST# to PCI_RST#
. Page 17- Add @ on R1311

<2009/06/12>
. Page4 Add C314 C313 C1150 D19 on +VCC_FAN1
. Page8 Add C1145 C1146 C1147
. Page10 Move CRT_DET# from Page13 to Page10
. Page13 Add +RTCVCC circuit

<2009/06/15>
. Update New Power schematic (change PBJ1 to PJP3)
. Page 10 modify C310 C308 C303 C307 C306 C304 Bom Structure
. Page 22 Modify Hole location by (ME drawing 06/12)

<2009/06/16>
. Page7 Modify DDR Command Control Pin pull-high Resister location
. Page9 Change R577 to 0402 type

<2009/06/17>
. Update New Power schematic 06/17
. Page9 modify LVDS Conn. Pin define
. Page9 Del C1110
. Page4 Add EMI solution D38 D39 D40

<2009/06/18>
. Update New Power schematic 06/18
. Page8 modify U4 Pin define and Q31
. Page13 Add R1376, R1377
. Page15 Modify C403
. Page23 Modify H11

<2009/06/19>
. Page4 Add new signal CPU_ITP , CPU_ITP#
. Page5 ADD R1378
. Page6 ADD C1152,C1153,C1154 C1160,C1161,C1162
. Page7 DDR_A_D8與DDR_A_D9互換
. Page8 ADD R1379,R1380,U77,R1381,C1157,R1382,R1383,R1384,C1157
, Page8 DEL C390
. Page9 ADD C1156
. Page11 DEL R1322, R1154
. Page13 DEL U77, ADD C1158
. Page17 ADD C1159

<2009/06/22>
. Page22 change IO Conn. pin34 from 48M to USB_ON#
. Page10 change JCRT1 P/N to SP010906182
<2009/06/23>
. Page15 Add C1163 C1164 C1165 C1166
. Page18 change PWR/B Conn. P/N to SP01000H300
. Page22 change JUSB1 JUSB2 P/N

<2009/06/24>
. Page8 Change C1350 C1351 to 0402 type
. Page10 Add R1385 R1386 on JVGA_HS JVGA_VS

<2009/06/25>
. Page22 move some parts to I/O Board , Add the MONO_IN_R on M/B
.

<2009/06/29>
. Page16 Change JP24 to ACES_88266_05001
. Page15 Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T

<2009/06/30>
. Page18 Change PWR_LED# to PWR_PWM_LED#
. Page17 Add PWR LED DETECT PIN on Pin97

<2009/07/02>
. Update New Power schematic 07/02
. Page9 Add C1167 C1168 for RF request.
. Page13 Change R223 to 100K
. Page16 change JP24 to ACES_85201-0505N
. Page17 Del R1387 R1388 on EC Pin97
. Page17 Add New Board ID to separate NAV50 NAV60
. Page17 Change 展頻IC to SA00003J400 (New)
. Page18 Add D41 for ESD

<2009/07/03>
. Page18 Add D41.2 to PWR_PWM_LED#
. Page8 Change co-lay net name to +1.5VM_CK505
. Page20 Change JP2 Pin42 to +5VS

<2009/07/06>
. Page18 Add pwr switch for NAV50

<2009/07/08>
. Page5 Add 470pf on H_SMI# for known issue.

<DVT START>

<2009/08/04>
. Page5 CLK_CPU_HPLCLK CLK_CPU_HPLCLK# exchange
. Page9 Change JLVDS1 to P/N ACES 88341-3001 30P
. Page17 del PM_1.8V(U6.82) ,Del R1310 R1311
. Page18 Del D41

<2009/09/03>
. Page7 Change C112 to 0402 type
. Page8 Add T6 on CLK_48M_CR
. Page16 Modify JP18 Pin define change +5VALW +5VS to +3VALW +3VS
. Page20 Change Pin 18, 23 to +1.5VS change Pin7 , 9 to USB20_P7 N7
. Page21 Del H12

<2009/09/08>
Update Power schematic 0904
. Page18 Change R1388 to 100 ohm 0402
. Page18 Change LED1 to SC591NB5A00

<2009/09/10>
Update Power schematic 0910
. Page22 unmount Q6 Q8

<2009/10/07>
. Page4 U71 Change to SA00003M800
. Page6 R26 Change to SHI00009C00
. Page13 R152 Change to SD034200A80
. Page18 R1388 Change to SD028510A80

<2010/04/29>
update new bom

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