

PCB DAZ0I200101

MB DA60000KP10
 USB IO/B DA60000KQ10
 HDD/B DA400011R10
 LED/B DA400011T10
 TP/B DA400013910

Compal Confidential

P1VE6 LA7071P Schematics Document

AMD Ontario Processor with DDRIII + Hudson M1

11.6" M/B

2011-03-17

Rev : 1.0

Dr-Bios.com

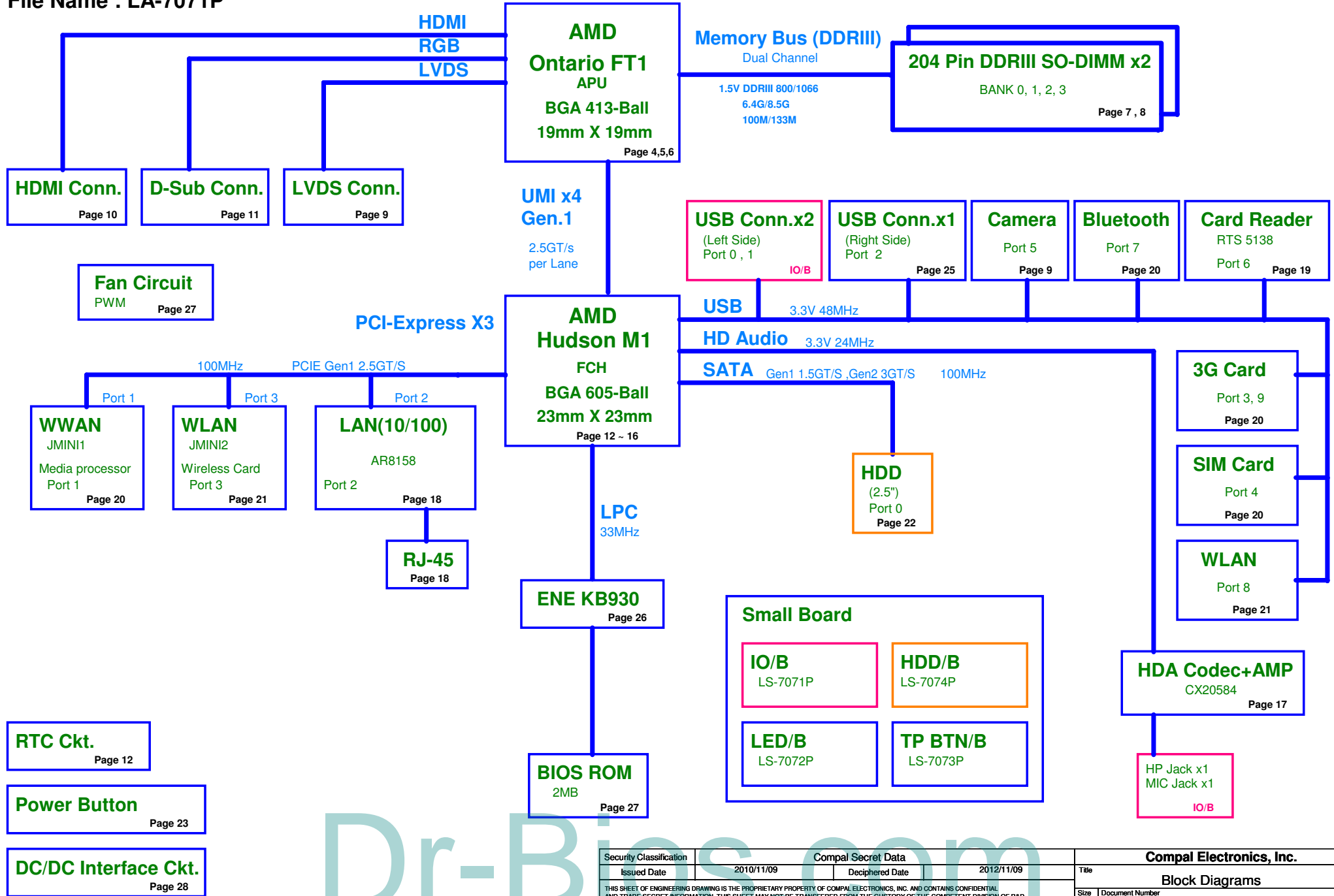
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Model Name : P1VE6

File Name : LA-7071P

Brazos Platform



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	16H	SB-TSI	1001-100xb	98H

SM Bus Controller 0

(FCH_SMB1 - FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90

BOM Structure

HDMI@ : HDMI function
 BT@ : BT function
 CONN@ : Conneters
 45@ : 45 Level
 3G@ : 3G function
 N3G@ : None 3G function
 CMBS@ : Combo Jack POPO noise Solution
 NCMS@ : None Combo Jack POPO noise Solution

FCH Hudson-M1 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Left conn
Port1	Left conn
Port2	Right conn
Port3	WWAN
Port4	SIM
Port5	USB Camera
Port6	CardReader
Port7	BT
Port8	WiMax
Port9	WWAN
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List

	PCIE0	
APU	PCIE1	NC
	PCIE2	
	PCIE3	
FCH	PCIE0	NC
	PCIE1	WWAN
	PCIE2	LAN
	PCIE3	WLAN

FCH Hudson-M1 SATA Port List

SATA0	HDD
SATA1	NC
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Board ID / SKU ID Table for AD channel

Vcc	+3VALW				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	PCB Revision
0	0	0 V	0 V	0 V	0.1
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

SMBUS Control Table

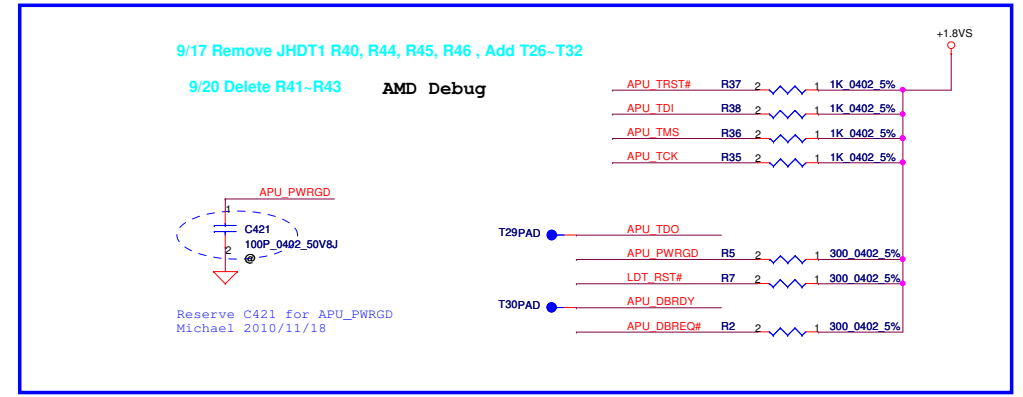
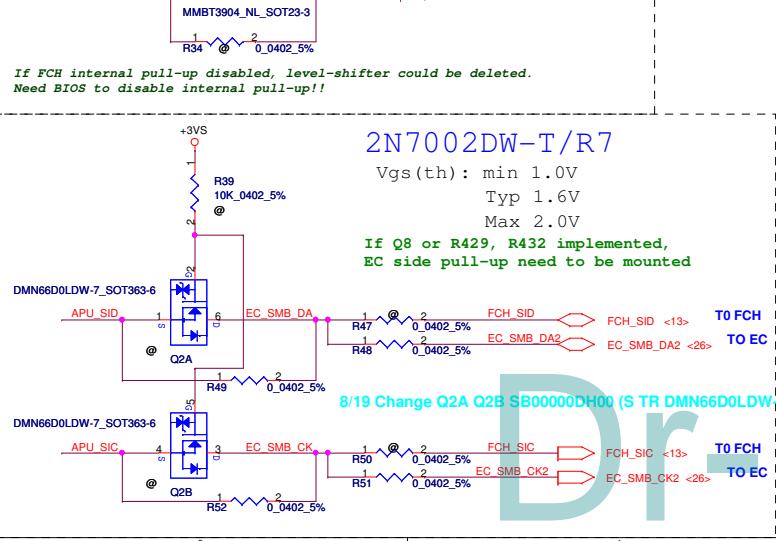
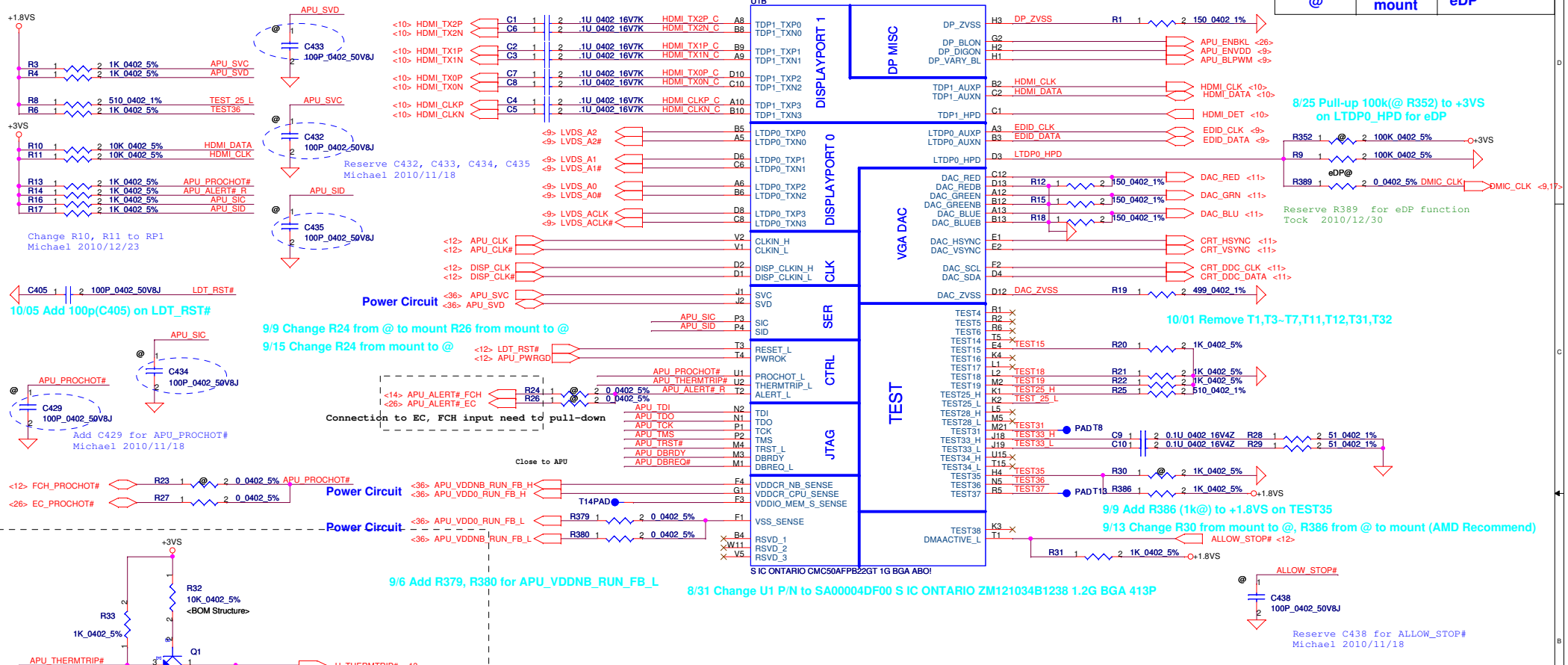
	Source	BATT	DIMM	MINI Card	LCD DDC ROM	HDMI DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB930	V					
EC_SMB_CK2 EC_SMB_DA2	KB930						V
HDMI_DATA HDMI_CLK	APU FT1					V	
EDID_DATA EDID_CLK	APU FT1				V		
FCH_SMDAT0 FCH_SMCLK0	FCH M1		V	V			

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APU C50 P/N change to SA00004KD50
Tock 2010/12/30

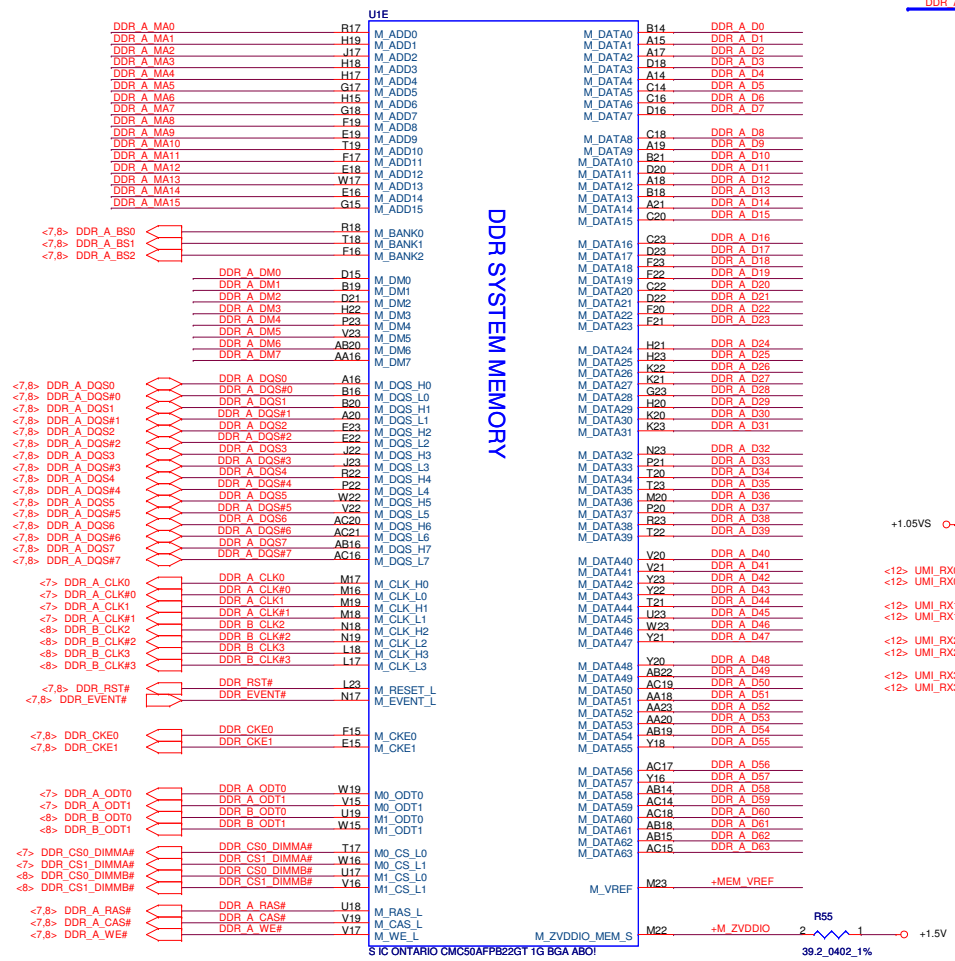
R9	R352	Display
mount	@	LVDS
@	mount	eDP

SA00004KD50



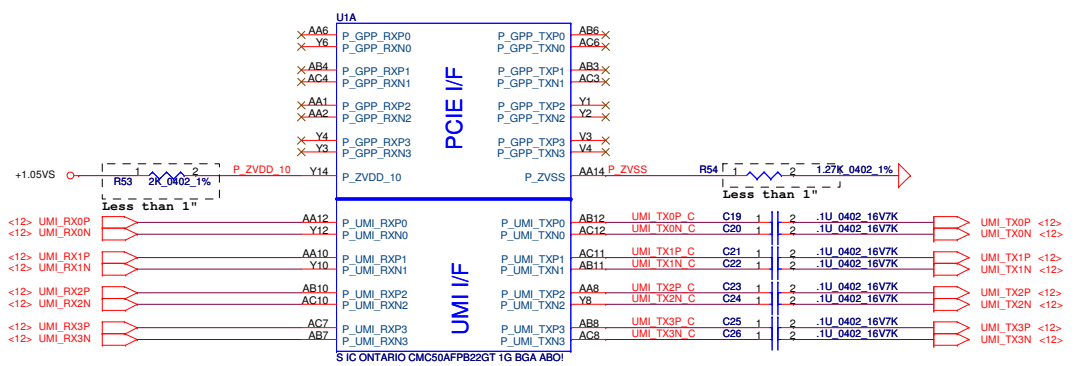
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DDR A D[0..63] <7,8>
 DDR A MA[0..15] <7,8>
 DDR A DM[0..7] <7,8>

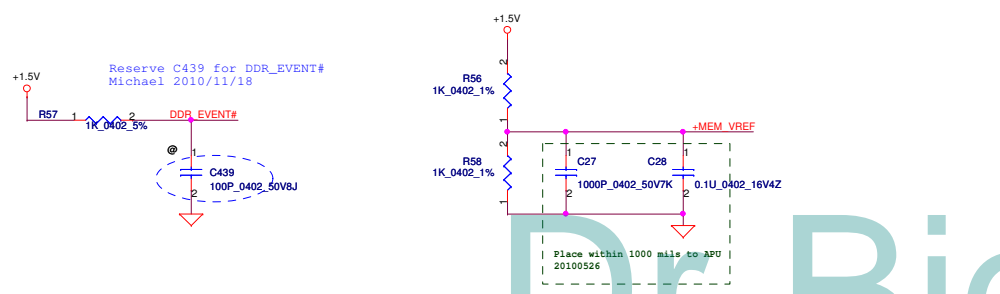


DDR SYSTEM MEMORY

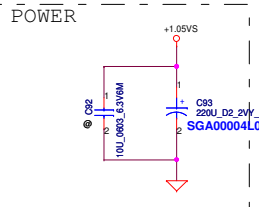
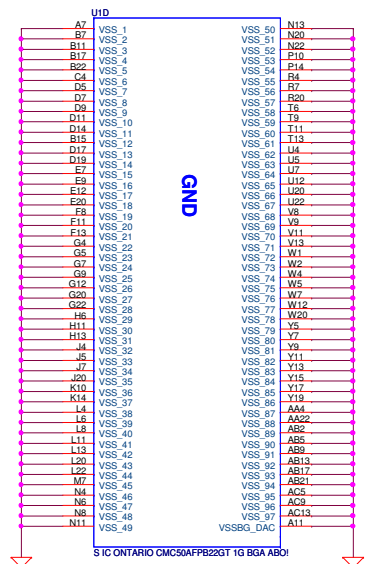
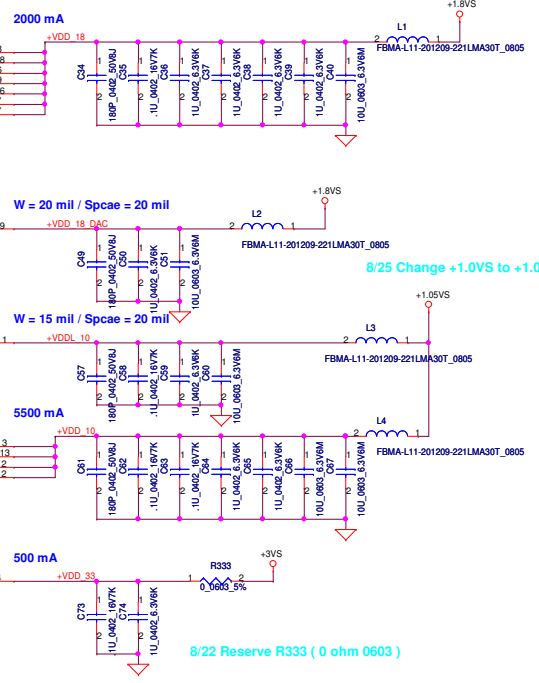
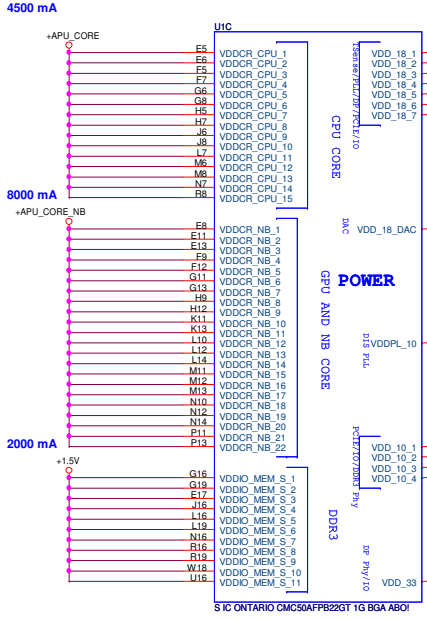
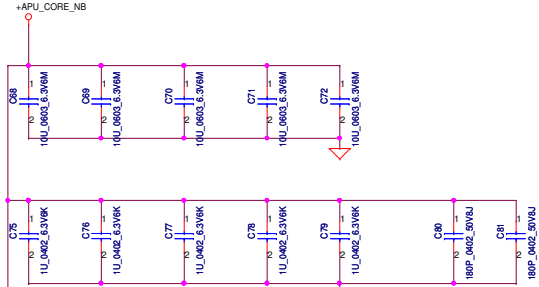
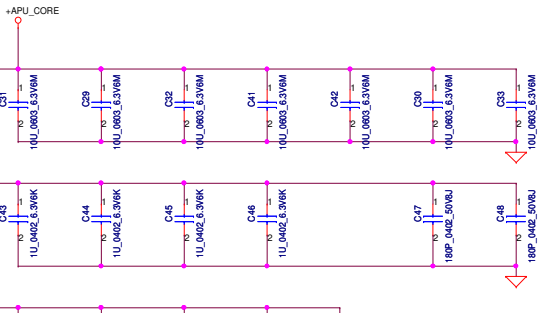
8/22 Delete C11~C18 (No VGA)
 9/6 Change PCI-E from FCH to APU
 9/6 Update PCI-E port List
 9/15 Change PCI-E from APU to FCH



9/11 Delete DDR Signal link to JDIMM2

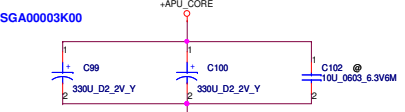


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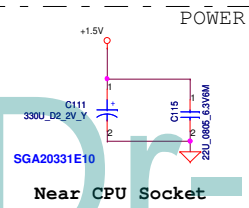


9/20 Change C93 to SGA00004L00

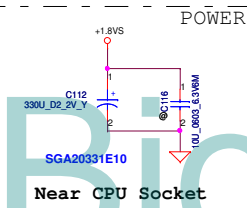
9/15 Change C99,C100 to 470U(SGA00003K00)



SGA00003K00

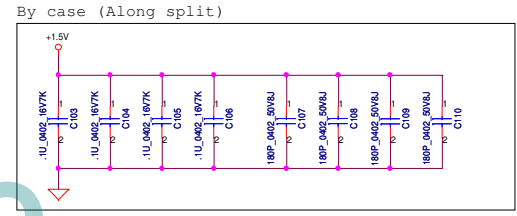


SGA20331E10



SGA20331E10

8/22 Change C111~C113 from E-Cap to Poly-Cap (SGA20331E10)
8/25 Change C111 from poly-cap to E-cap (SF000002200)
9/11 Change C111 to SGA20331E10

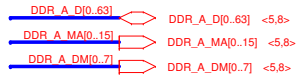
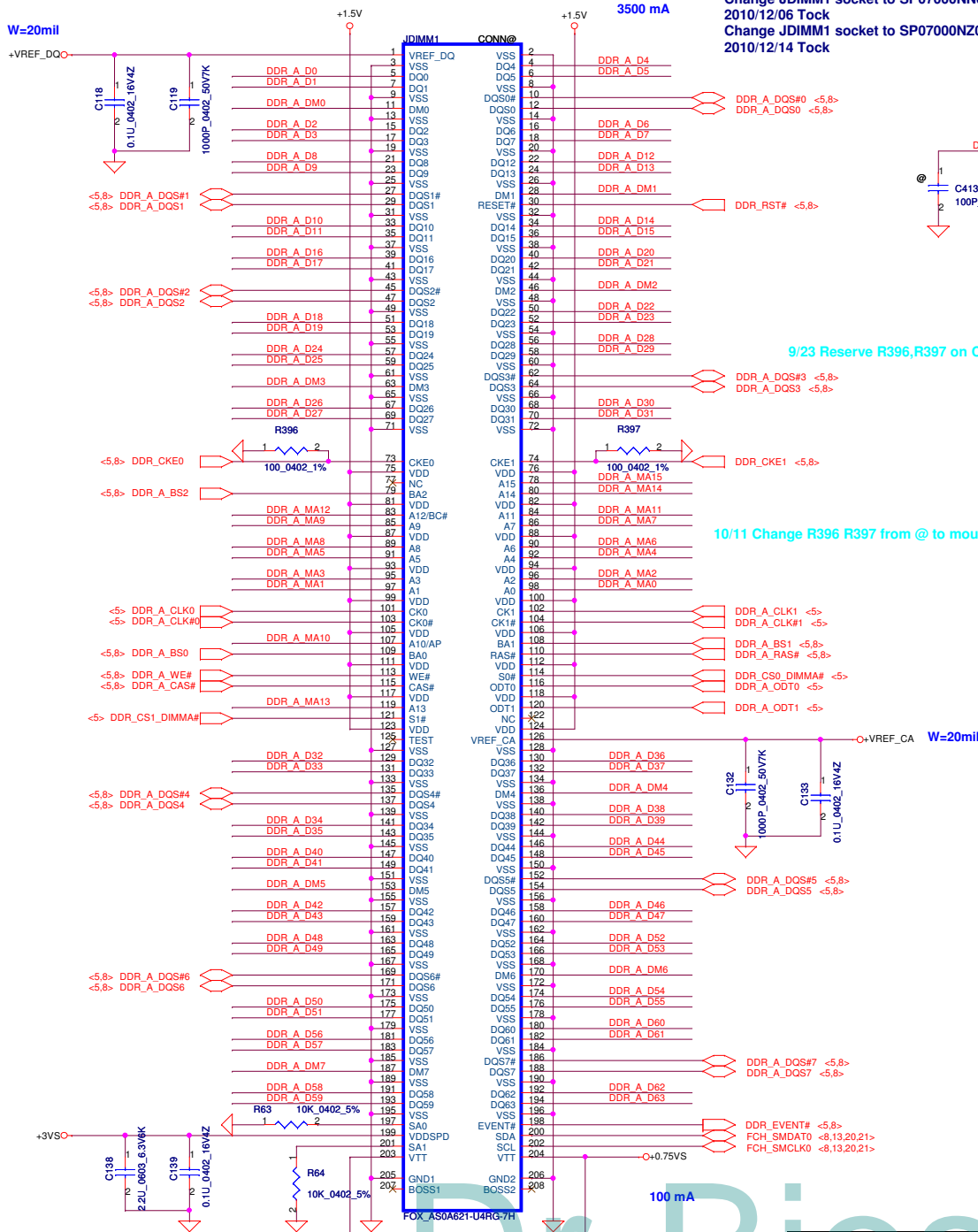


By case (Along split)

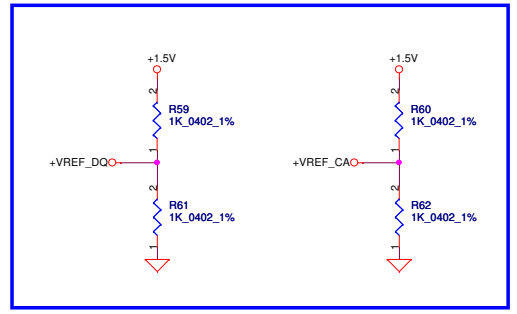
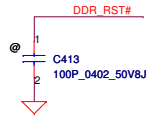
change C99,C100 from 470U to 330U , 2011/01/28 Tock
change C99,C100 footprint from C_D2 to C_X for placement

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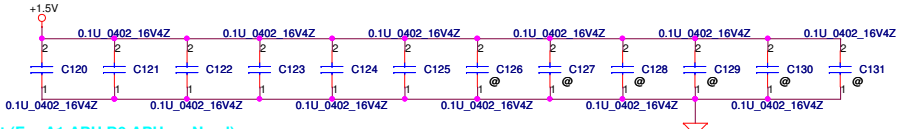
Change JDIMM1 socket to SP07000N00
2010/12/06 Tock
Change JDIMM1 socket to SP07000N200
2010/12/14 Tock



Reserve C413 for DDR_RST#
Michael 2010/11/18

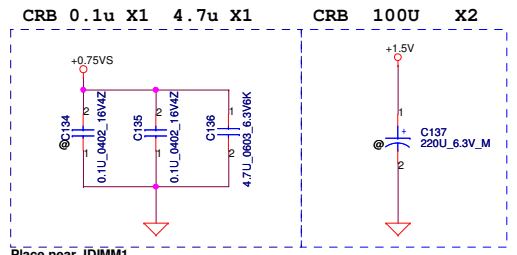


9/23 Reserve R396, R397 on CKE0 & CKE1 (S3 hang Issue)



10/11 Change R396 R397 from @ to mount (For A1 APU, B0 APU no Need)

9/11 Change C137 to SGA00004L00



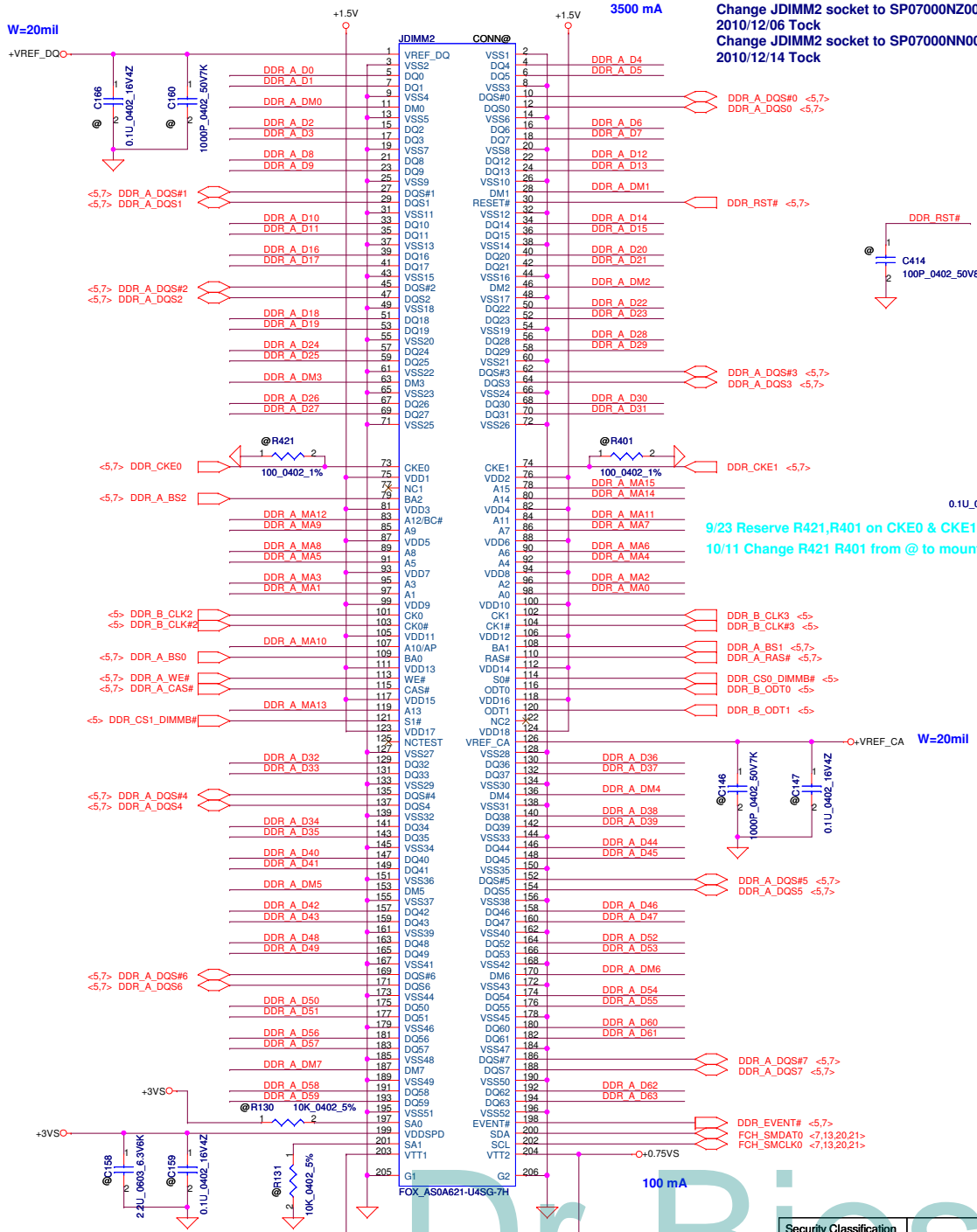
SGA00004L00
change C137 to SF000002Y00
2010/12/14 Tock

8/25 Change C137 from poly-cap to E-cap (SF000002Y00)
8/25 Reserve C381 E-cap (SF000002Y00) on +1.5V

9/11 Remove C381

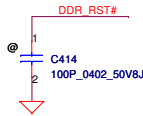
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				DDR3 SODIMM-I Socket	
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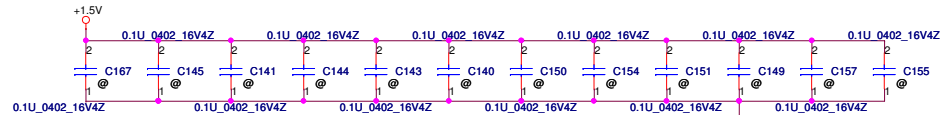


Change JDIMM2 socket to SP07000NZ00 for reverse
 2010/12/06 Tock
 Change JDIMM2 socket to SP07000NN00
 2010/12/14 Tock

DDR_A D[0..63] <-5,7>
 DDR_A MA[0..15] <-5,7>
 DDR_A DM[0..7] <-5,7>

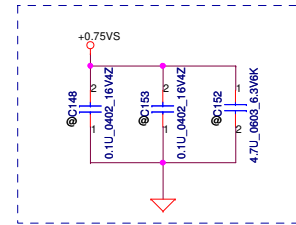


Reserve C414 for DDR_RST#
 Michael 2010/11/18



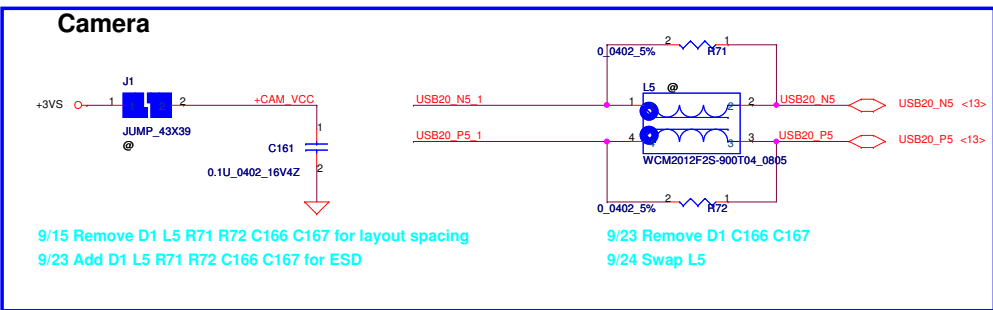
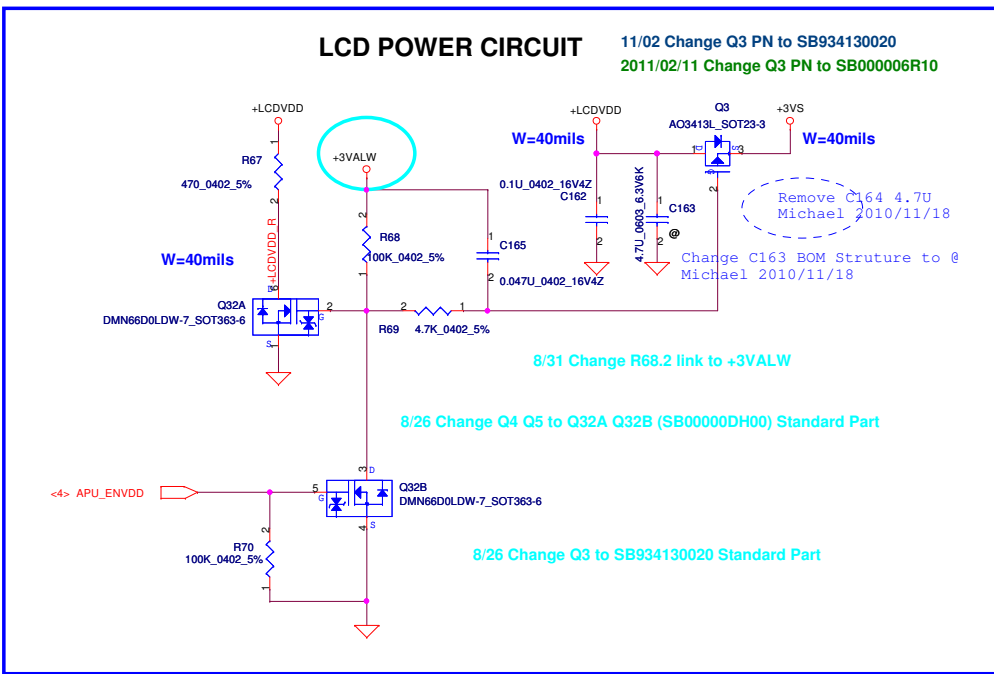
9/23 Reserve R421, R401 on CKE0 & CKE1(S3 hang Issue)
 10/11 Change R421 R401 from @ to mount (For A1 APU, B0 APU no Need)

CRB 0.1u X1 4.7u X1



Place near JDIMM2

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9/9 Reserve 100k PD to GND on INVT_PWM 9/17 Change R387 from @ to induct

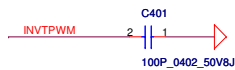
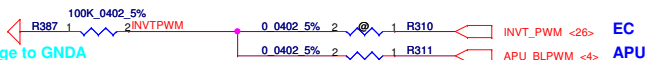
CMOS & LCD/PANEL BD. Conn.

DMIC

Add R344 0 ohm for +3VS_MIC
Michael 2010/11/18

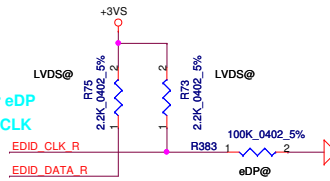
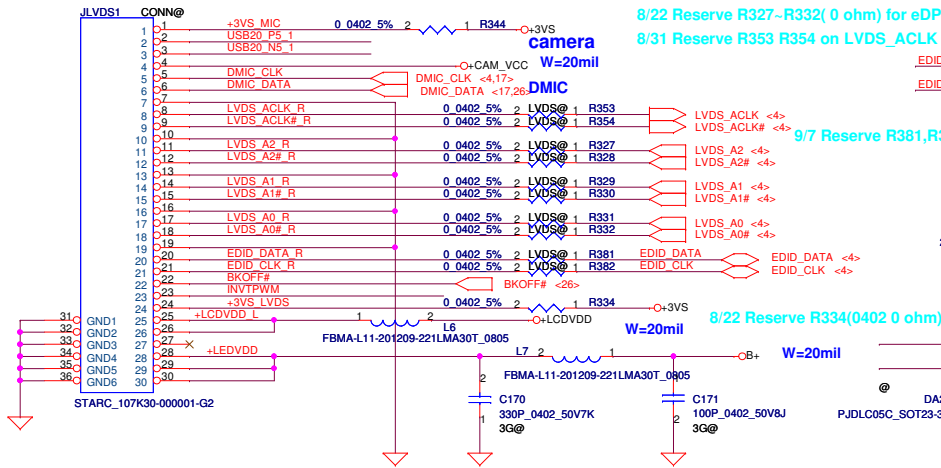
Connect DMIC_CLK,
DMIC_DATA
to JLVDS1 pin 5 and 6
Michael 2010/11/18

8/25 JLVDS1.5 change to INT_MIC0 JLVDS1.6 change to GNDA
8/31 Update JLVDS1 Pin definition Delete R74 R76
9/13 Update LVDS Pin definition, Add R74,R76
9/13 Add Net Name +3VS_DMIC 10/01 Remove R74,R76



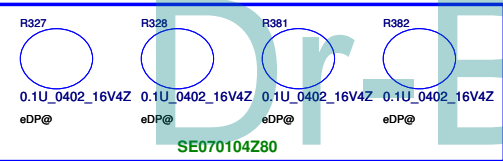
10/04 Add 100p(C401) on INVT_PWM

10/04 Change C401 on INVT_PWM

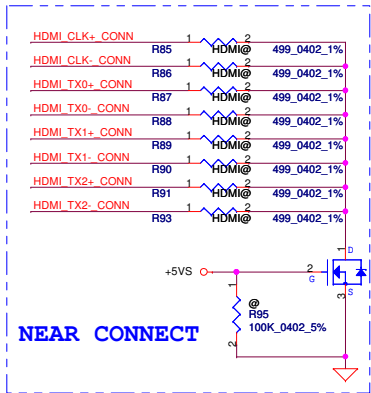
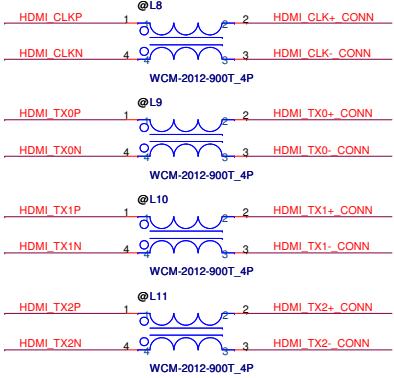
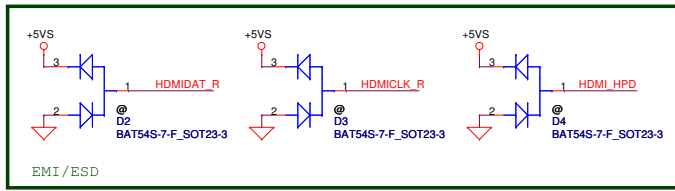
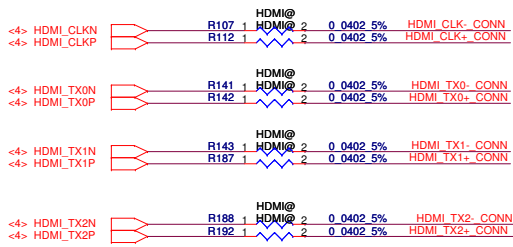


Display	LVDS	eDP
R327	0 ohm	0.1uF
R328	0 ohm	0.1uF
R381	0 ohm	0.1uF
R382	0 ohm	0.1uF
R383	@	100k ohm
R73	2.2k ohm	@
R75	2.2k ohm	100k ohm

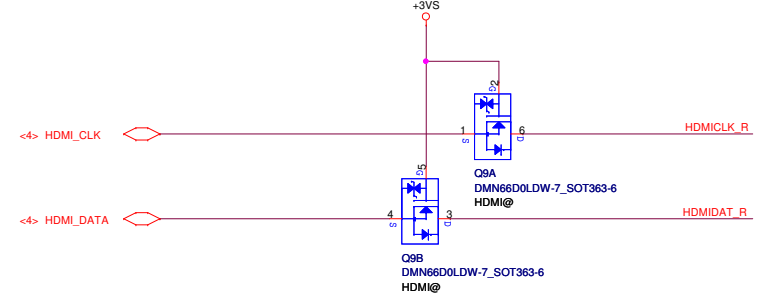
change JLVDS1 to SP010011S00
2010/12/14 Tock



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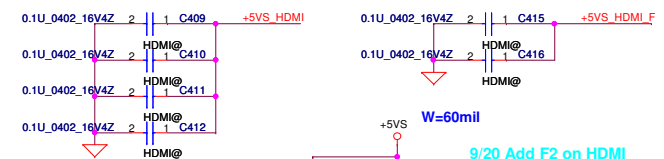


8/26 Change Q7 to SB000009610 Standard Part



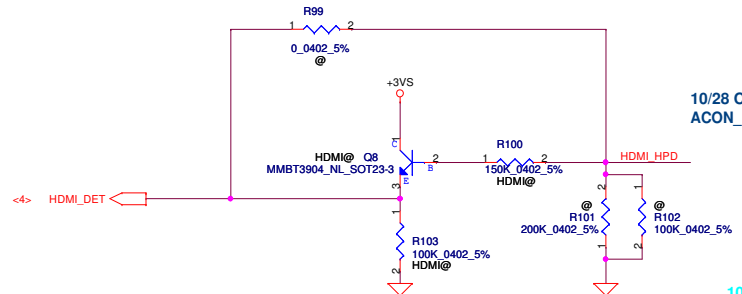
8/19 Change Q9A Q9B to SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6)

10/29 Add C409~C412(0.1U) on +5VS_HDMI
10/29 Add C415~C416(0.1U) on +5VS_HDMI_F



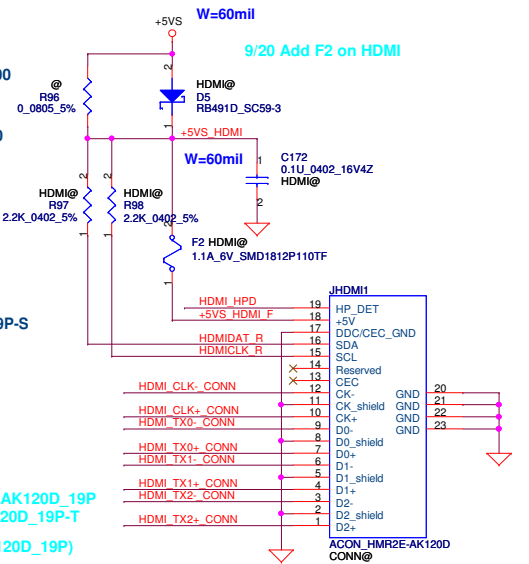
10/27 Change D5 P/N from SC1B491D000 to SCS00003H00
10/27 Change F2 P/N from SP04301P120 to SP040001B00

9/20 Change R99 from HDMI@ to @
9/20 Change Q8,R100 from @ to HDMI@

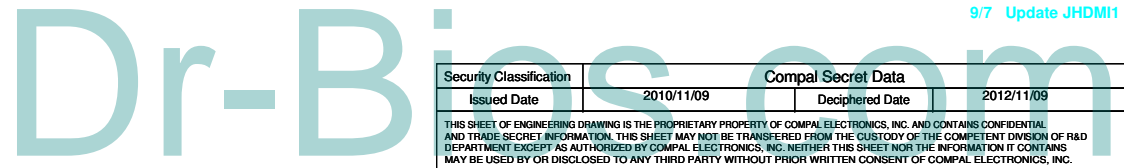


10/28 Change JHDMI1 footprint from ACON_HMR2E-AK120D_19P-T to ACON_HMR2E-AK120D_19P-S

10/07 Update JHDMI1 footprint from ACON_HMR2E-AK120D_19P to ACON_HMR2E-AK120D_19P-T
11/16 Update JHDMI1 Symbol (ACON_HMR2E-AK120D_19P)



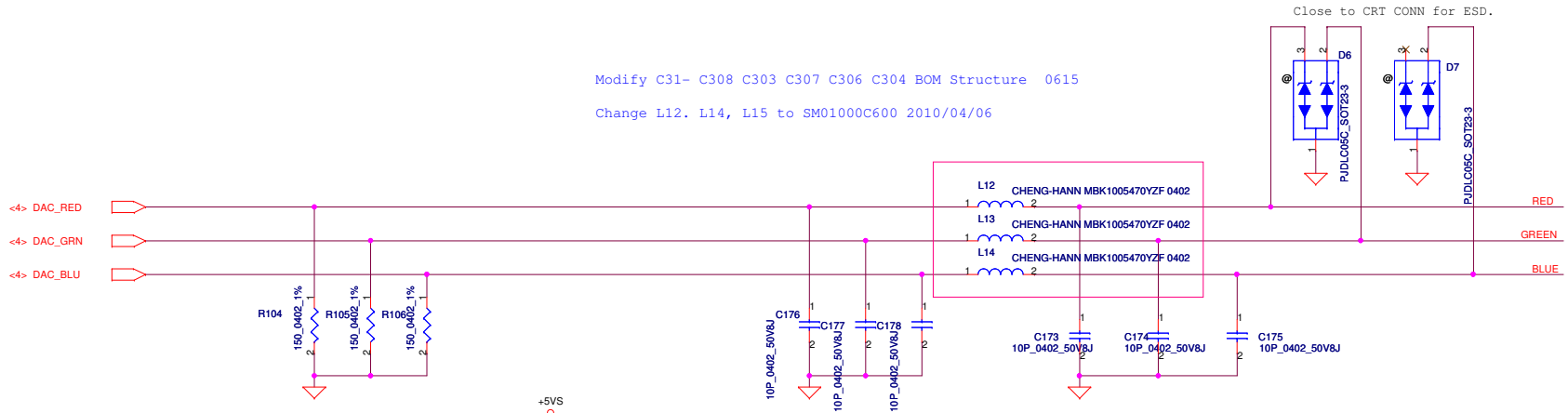
8/23 Update JHDMI1 Symbol (SUYIN_100042GR019S268ZR_19P-T)
9/7 Update JHDMI1 Symbol (ACON_HMR2E-AK120D_19P)



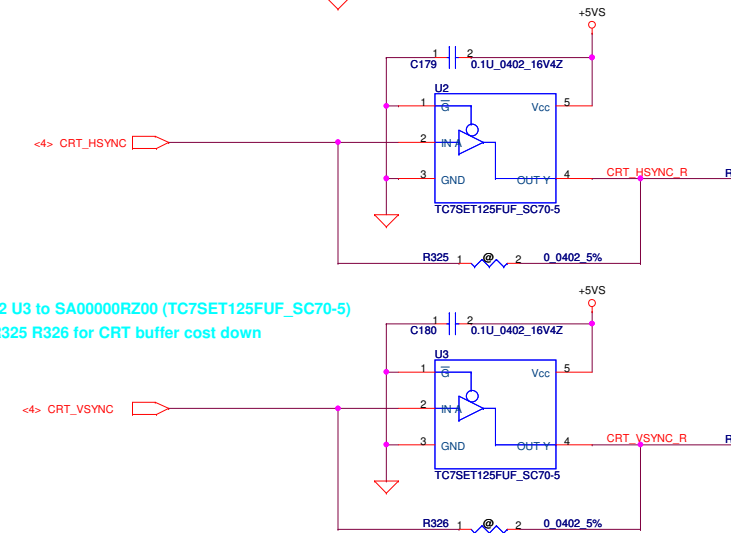
Security Classification		Compal Secret Data		Title	
Issued Date	2010/11/09	Deciphered Date	2012/11/09	HDMI Connector	
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				Custom	P1VE6 Schematics
				Date:	Thursday, March 17, 2011
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Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615
 Change L12, L14, L15 to SM01000C600 2010/04/06

Close to CRT CONN for ESD.



8/21 Change U2 U3 to SA00000RZ00 (TC7SET125FUF_SC70-5)
 8/21 Reserve R325 R326 for CRT buffer cost down

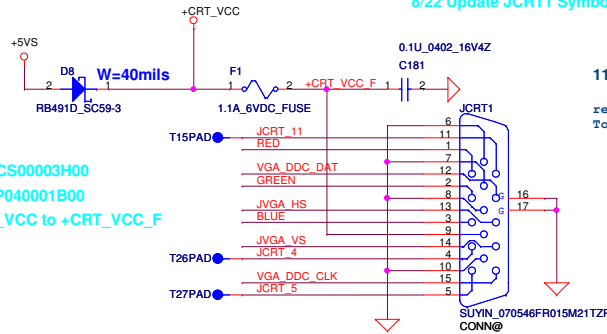


Delete Q10, R107
 for CRT Hot Plug detect Circuit
 2010/12/15 Tock

8/31 Delete Net Name: CRT_HSYNC_1, CRT_VSYNC_1
 9/3 Add R375 R376 for CRT

CRT PORT

8/26 Change Q10 to SB000009610 Standard Part
 8/22 Update JCRT1 Symbol from database (SUYN_070546FR015M21TZR_15P)

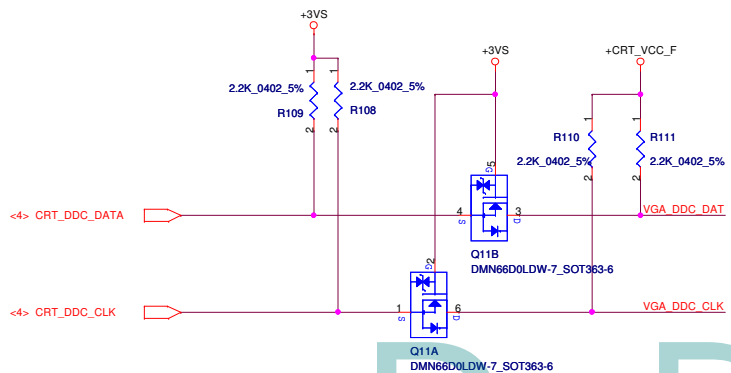


11/01 Add Net CRT4, CRT11 on JCRT.4, JCRT.11
 remove CRT11, CRT4
 Tock 2010/11/26

8/26 Update D8 P/N to SCS00003H00
 8/26 Update F1 P/N to SP040001B00
 10/4 Change from +CRT_VCC to +CRT_VCC_F

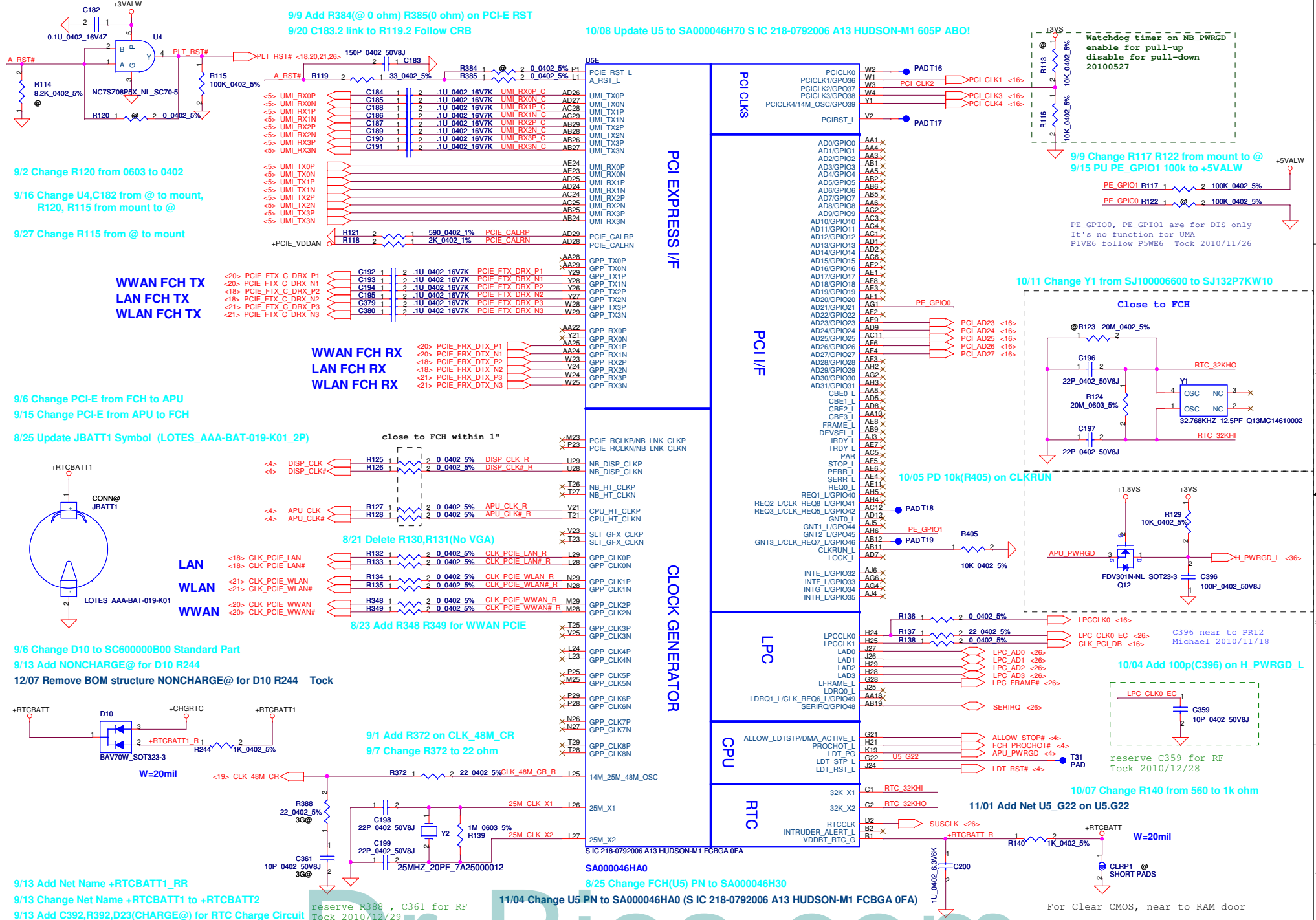
Add JCRT_4, JCRT_5, JCRT_11
 2011/01/28 Tock

Delete R112 and net CRT_DET#
 for CRT Hot Plug detect Circuit
 2010/12/15 Tock



8/19 Change Q11A Q11B to SB00000DH00 (S TR DMN66D0LDW-7.2N SOT363-6)

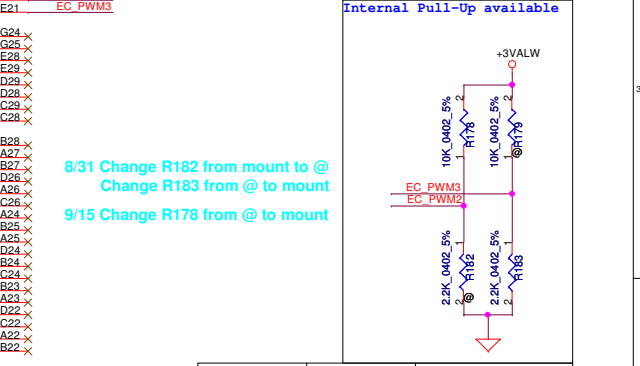
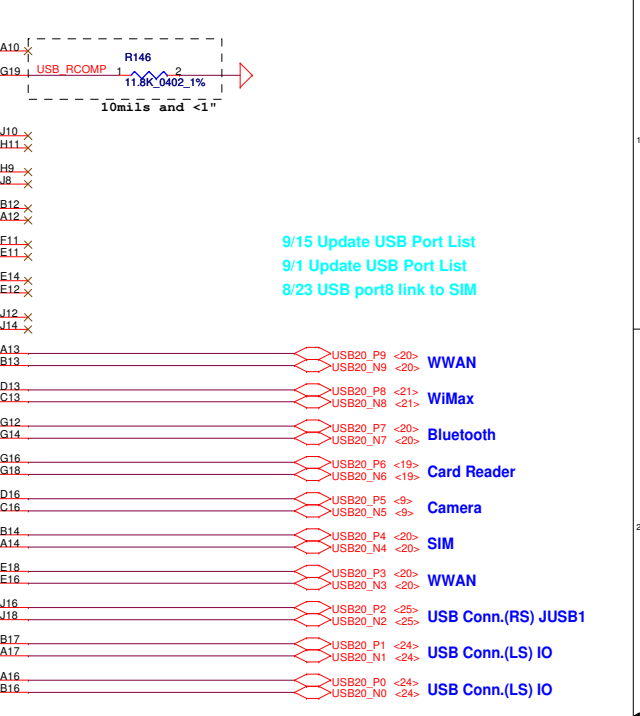
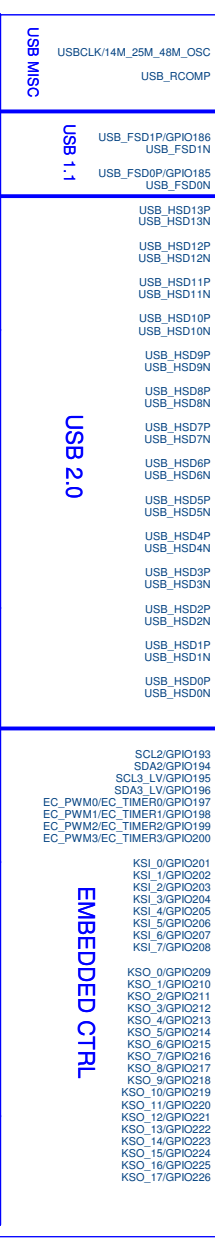
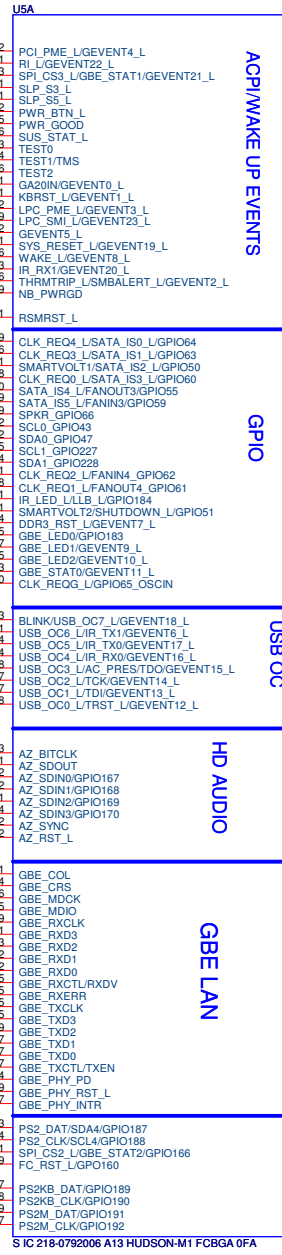
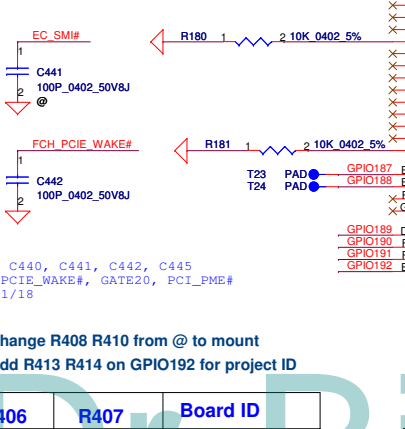
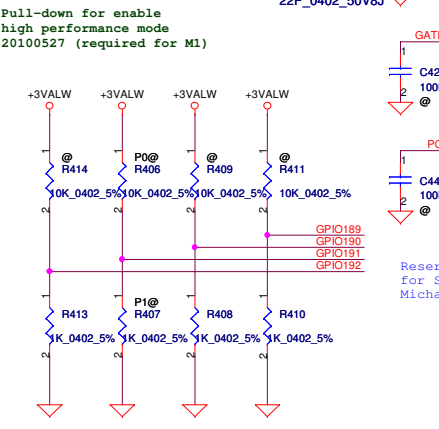
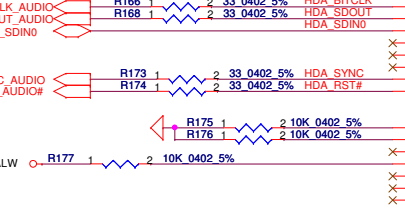
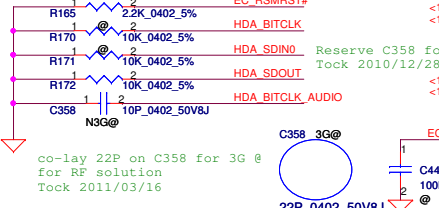
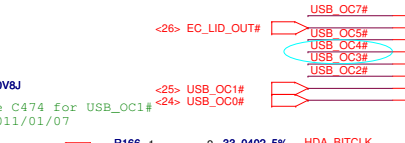
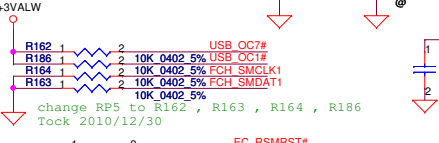
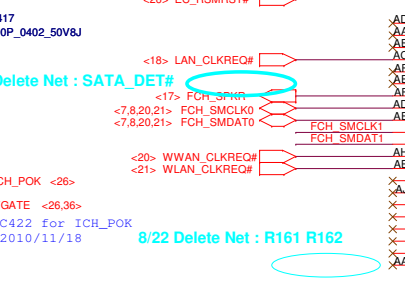
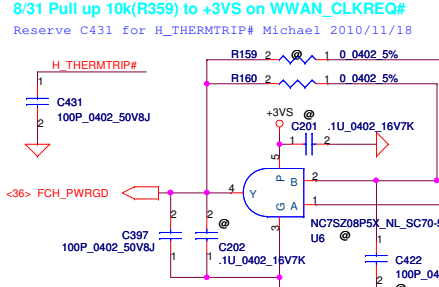
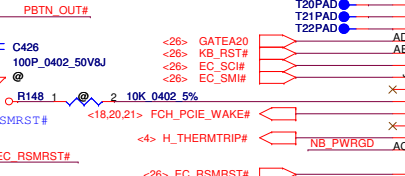
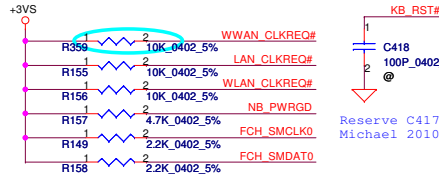
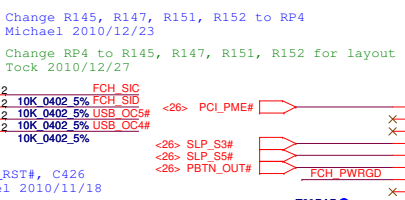
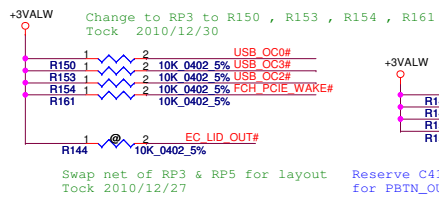
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/09	Deciphered Date	2012/11/09	Title	
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Compal Electronics, Inc.		
FCH PCIE/PCI/ACPI/LPC/RTC		
Title	Document Number	Rev
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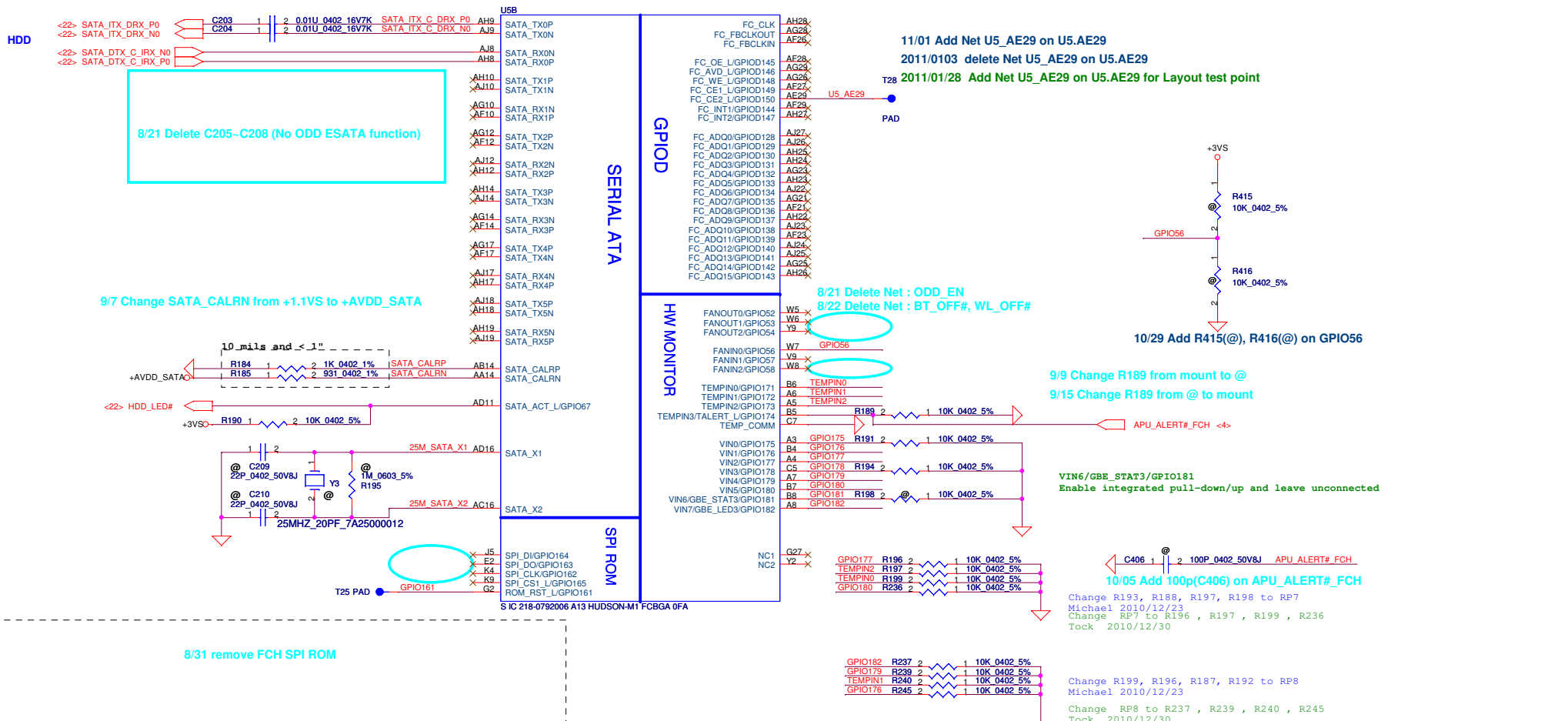
EC_PWM3	EC_PWM2	ROM TYPE
NC	L	SPI ROM
NC	NC	Reserved
L	L	Reserved
L	H	LPC ROM

R406	R407	Board ID
mount	@	P1VE6
@	mount	P1VS6

Security Classification	Compal Secret Data
Issued Date	Deciphered Date
2010/11/09	2012/11/09

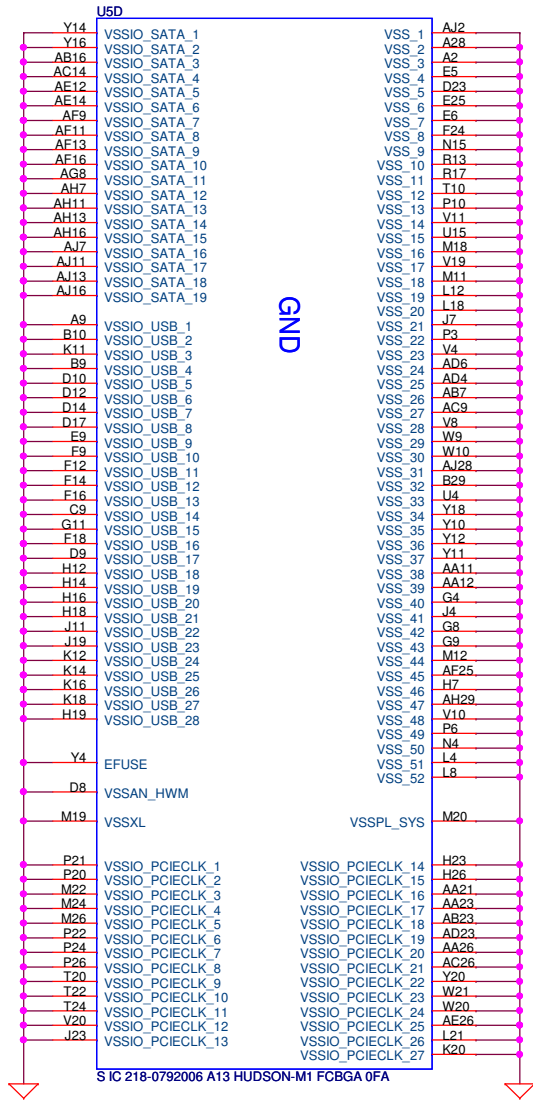
Compal Electronics, Inc.		
FCH HDA/USB/ACPI		
Title	Document Number	Rev
	P1VE6 Schematics	1.0
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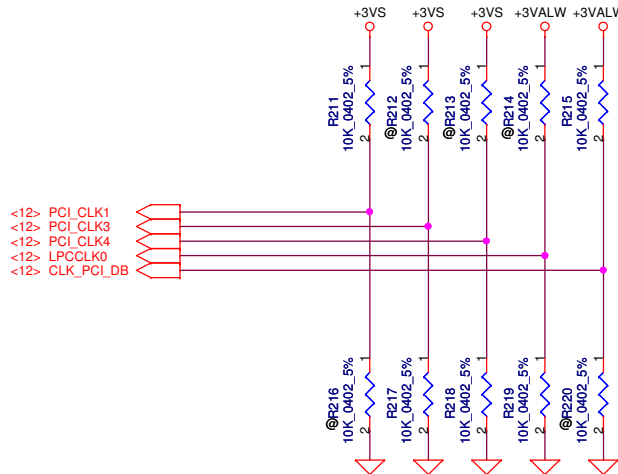
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/09	Deciphered Date	2012/11/09	FCH-SATA/SPI	
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REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	CLK_PCI_DB				
PULL HIGH	ALLOW PCIE GEN2 *	USE DEBUG STRAP	Reserved	internal EC ENABLE	Internal CLKGEN Mode *				
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP *	CLKGEN Mode Internal *	internal EC DISABLE *	External CLKGEN Mode				



9/13 Change R211 from mount to @, R216 from @ to mount
9/13 Change R211 from @ to mount, R216 from mount to @

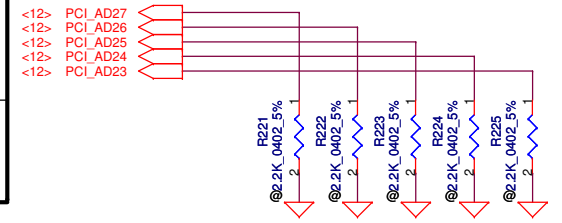
DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

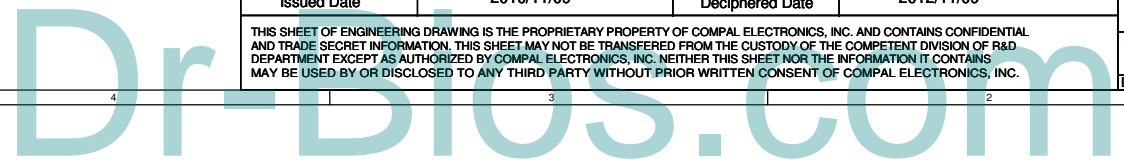
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK *	ILA AUTORUN Disabled *	Selects FC PLL *	Disable I2C ROM *	Required Setting *
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

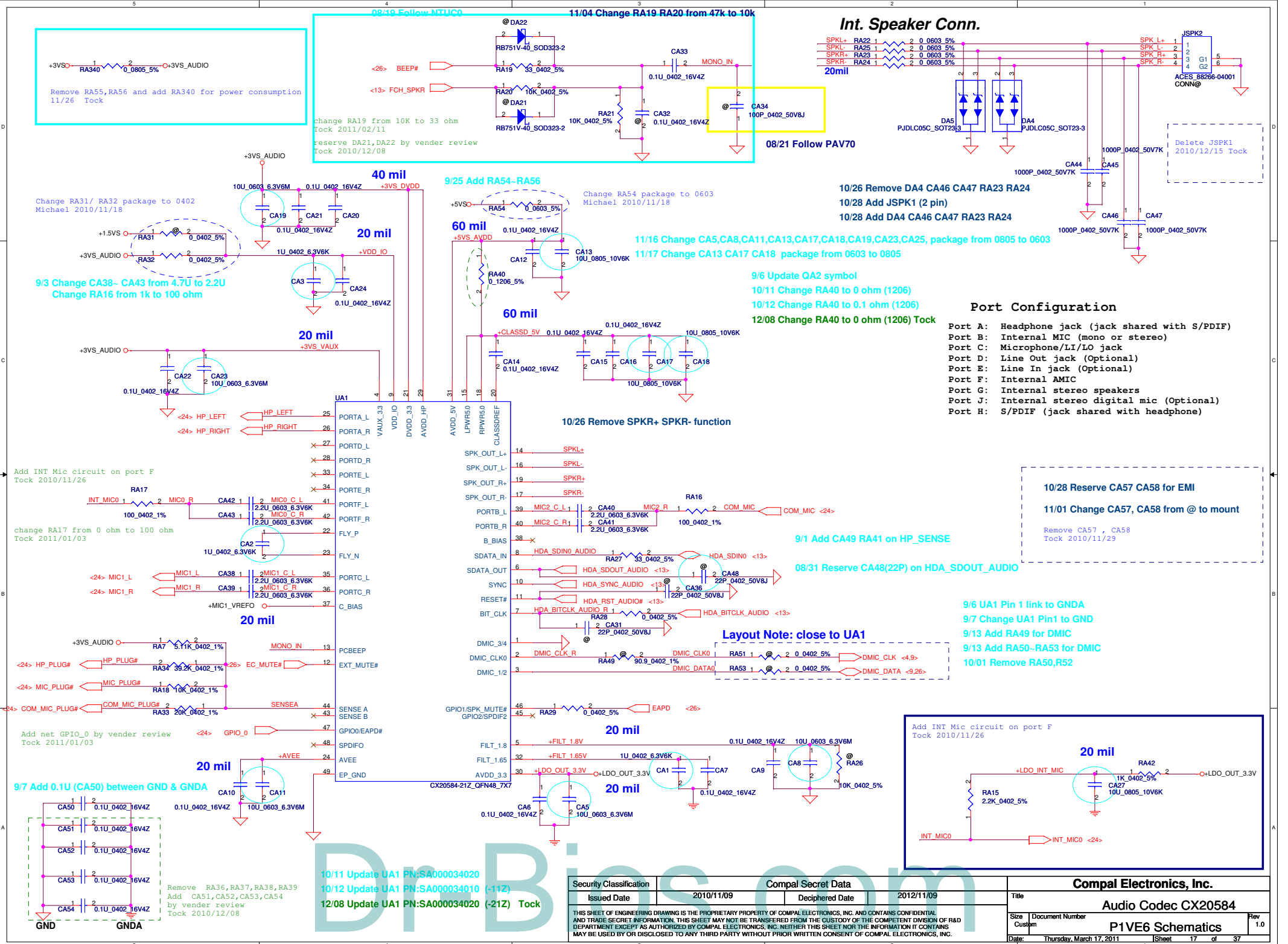
Check AD29,AD28 strap function

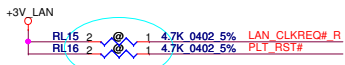
check default



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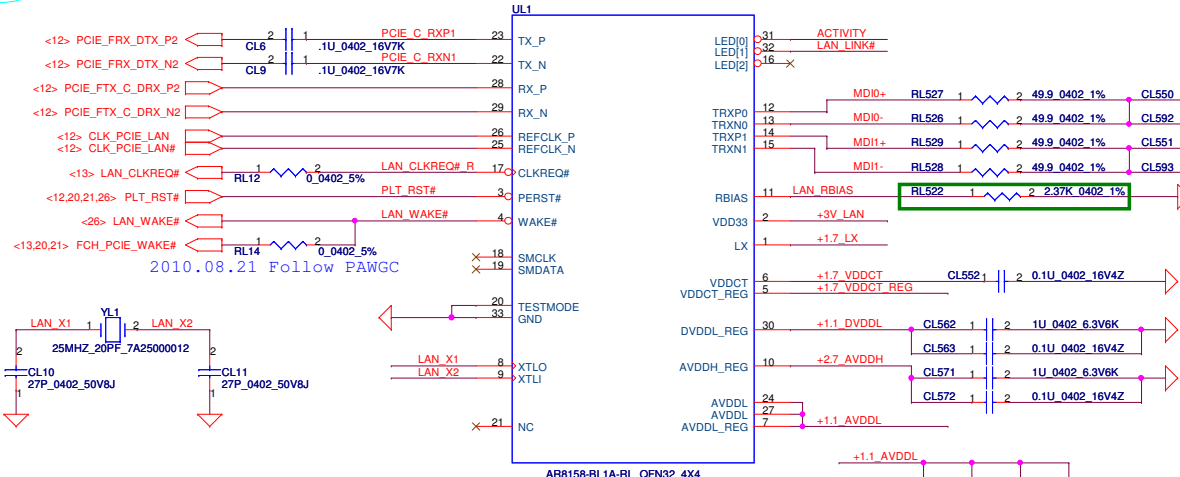






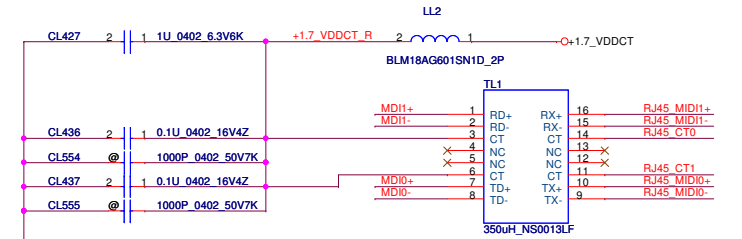
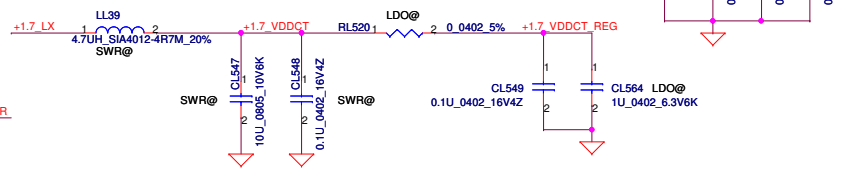
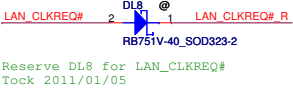
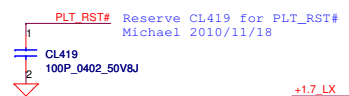
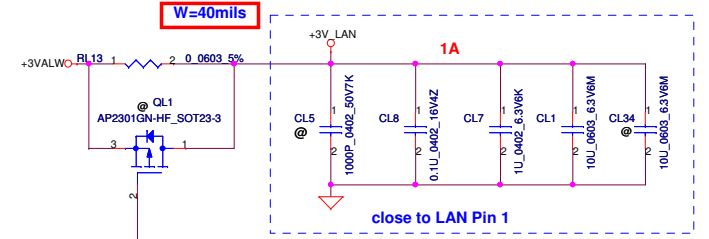
Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H

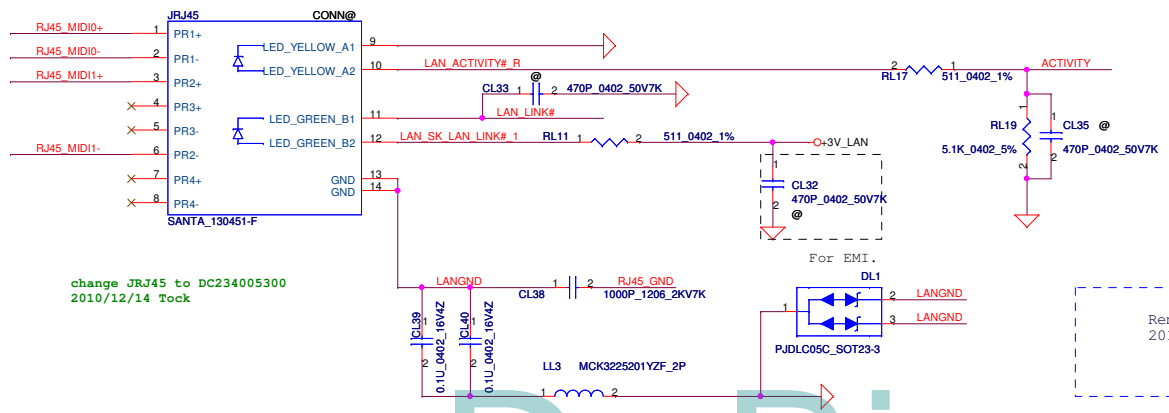


2010.08.21 Follow PAWGC

W=40mils



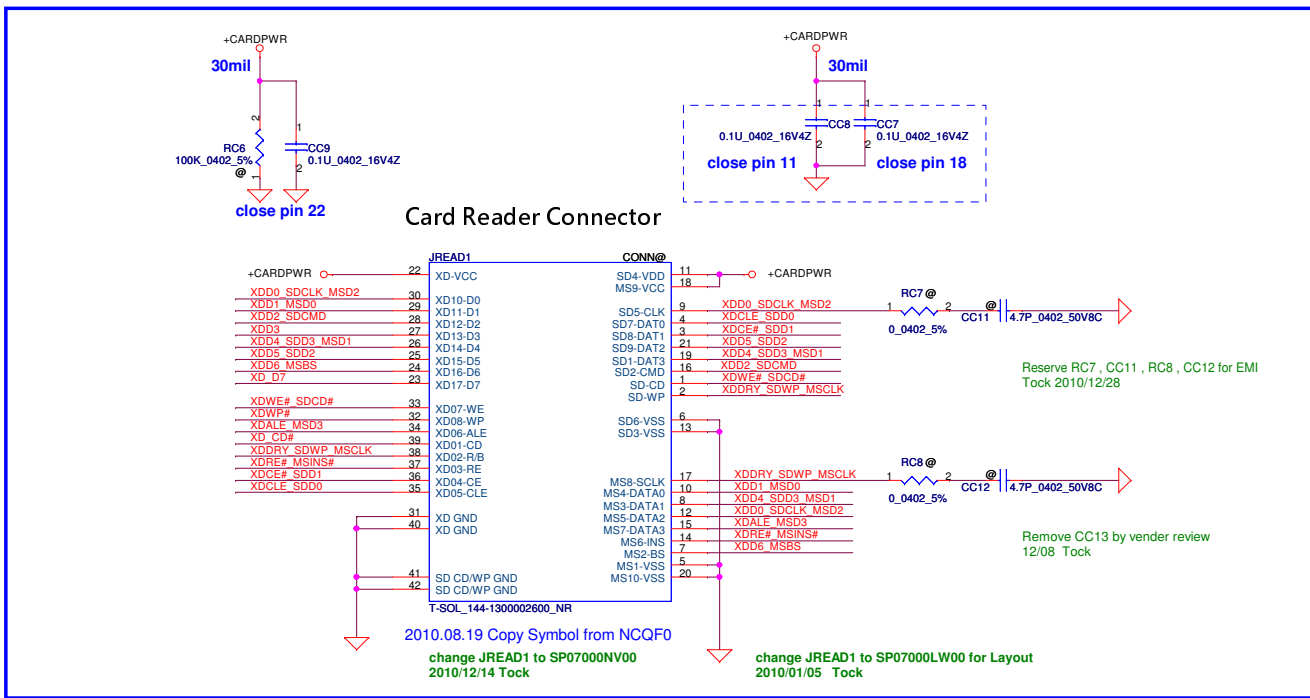
change T1 to SP050005900 <MHPC> but use BOTH_GST5009-LF_24P footprint 2010/12/14 Tock
change TL1 PN to SP050006E00 2011/02/11 Tock



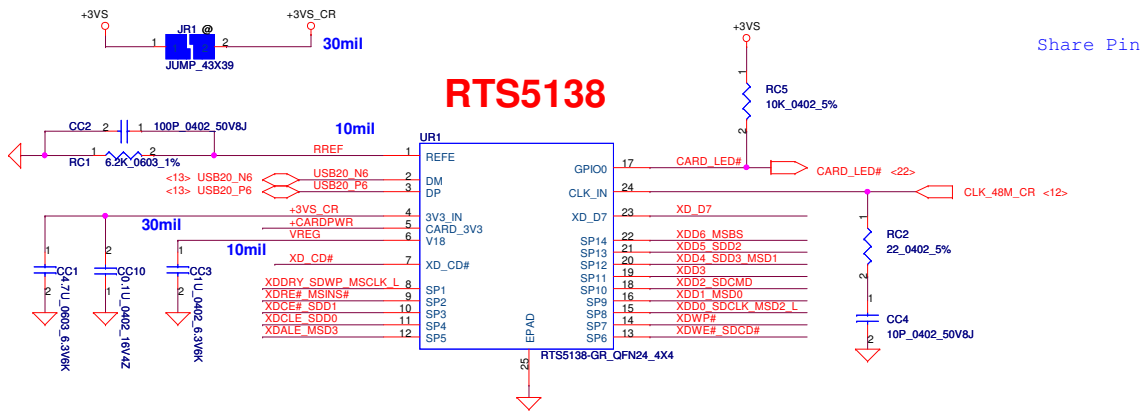
change JRJ45 to DC234005300 2010/12/14 Tock

Remove DL2-DL13 2010/12/06 Tock

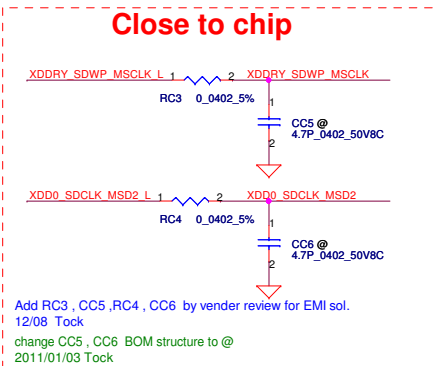
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/09	Deciphered Date	2012/11/09	Title	LAN AR8158
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2010.11.02 Del LED circuit



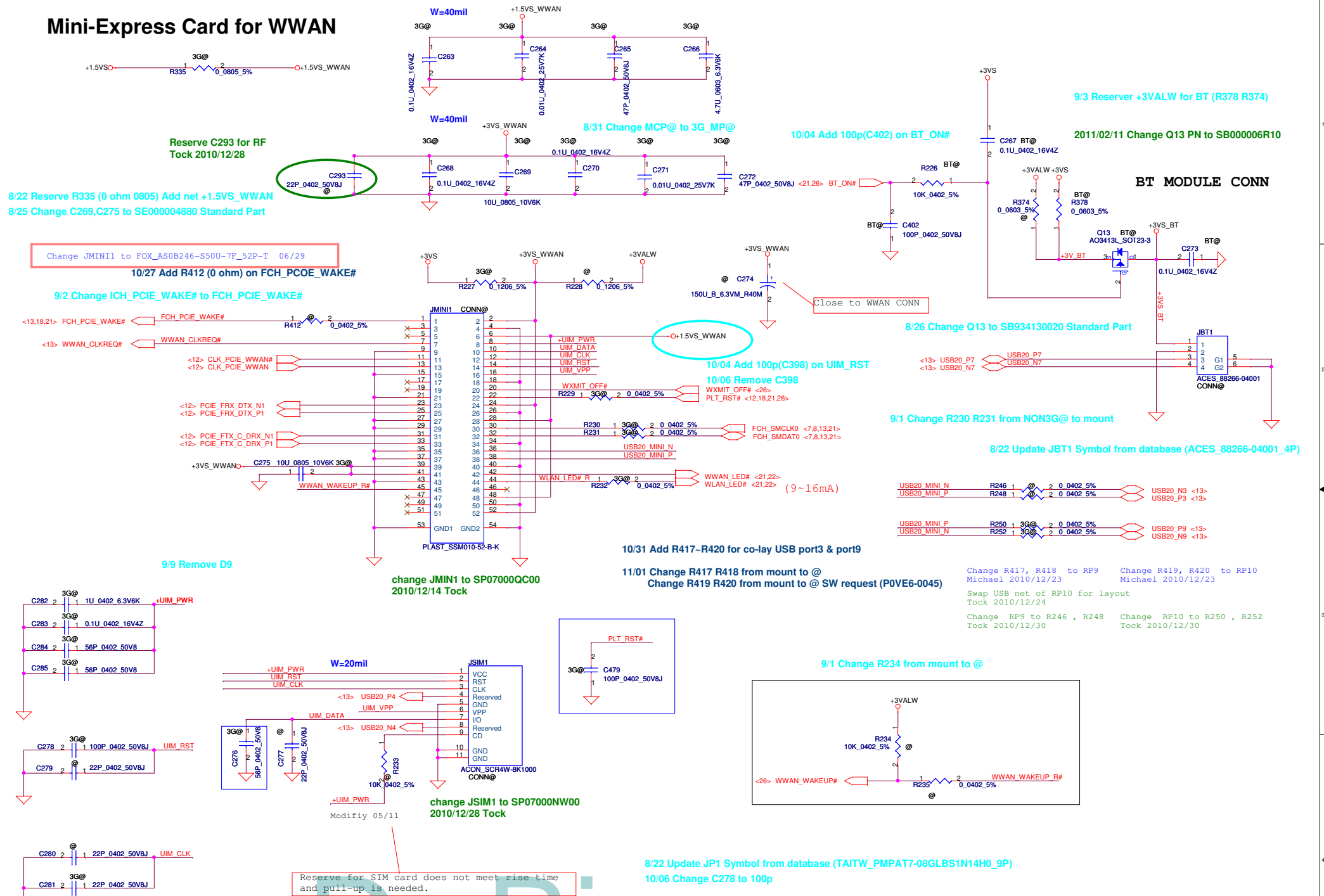
	XD	SD	MS
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE		MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP		
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1		MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3		
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS
	XD_D7		



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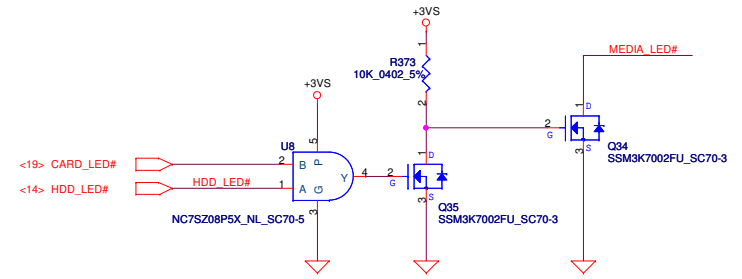
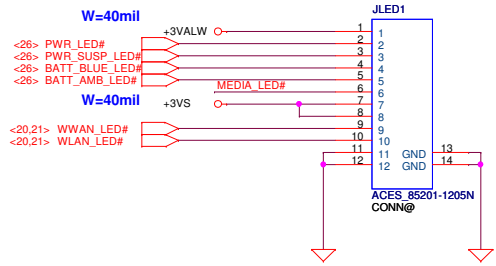
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/09	Deciphered Date	2012/11/09	Title
				CARD READER RTS5138
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				Document Number P1VE6 Schematics
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Mini-Express Card for WWAN



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				Mini-Card/BT CONN	
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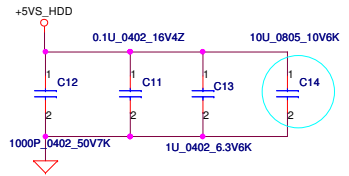
LED PCB CONN



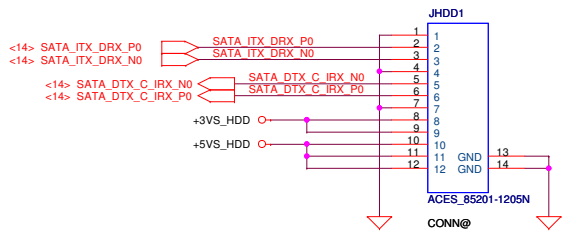
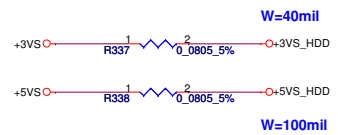
- 8/22 Update JP2 Symbol from database (ACES_85201-1605N_16P)
- 8/24 Update JLED1 Symbol from database (ACES_85201-1205N_12P) & Update pin definition
- 9/1 Add LED Circuit (LED2-4(SC597UDB000)LED5(SC5191NB000), R360-R369, Q33)
- 9/1 Change All LED power to 5V
- 9/9 Change LED2-4 footprint to LED_HT-297DQ-GQ_4P
- 9/11 Remove LED portion

9/1 Add R373, Q34, Q35 for MEDIA_LED#

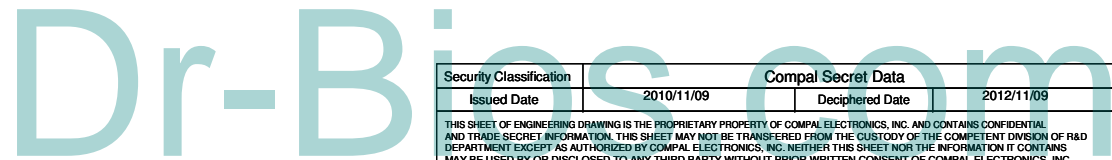
Add C11~C14 from HDD board
2011/01/07 Tock



SATA HDD Conn.



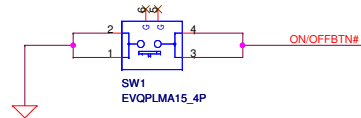
- 8/22 Change C298 from 10U 6.3V to 10U 10V
- 8/22 Reserve R337 R338 Add net +3VS_HDD,+5VS_HDD
- 9/1 Change Q33 to SB000009610(SSM3K7002FU_SC70-3)
- change JHDD1 to SP01000E400 , delete C293 ~ C298
- 2010/12/14 Tock
- Modify JHDD1 pin define
- 2010/12/15 Tock



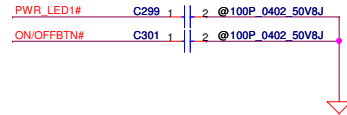
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Issued Date	2010/11/09	Deciphered Date	2012/11/09	Title	
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updated SW1 symbol for SN100002K00
2010/12/06 Tock

ON/OFF Button



FOR EMI

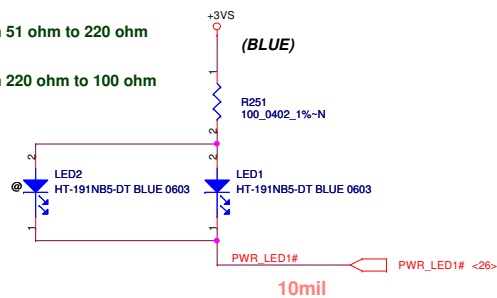


9/6 Change D13 from mount to @
10/05 Remove D13

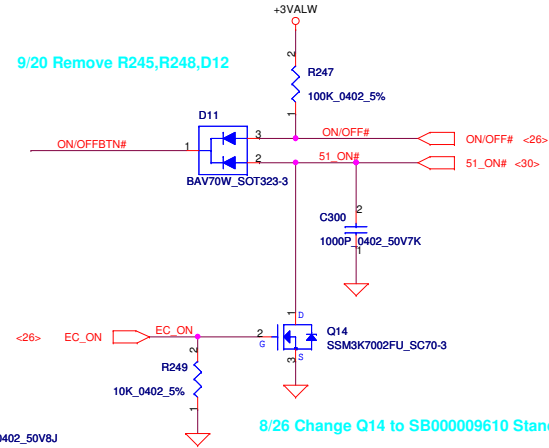
9/1 Remove LED2 LED3 circuit, Change 70@ to mount

9/20 Add LED2 LED3 Circuit
9/21 Remove LED2 LED3 Circuit

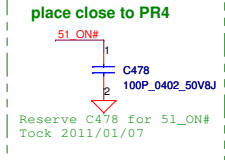
change R251 from 51 ohm to 220 ohm
2011/03/07 Tock
change R251 from 220 ohm to 100 ohm
2011/03/16 Tock



8/26 Change D11 to SC60000B00 Standard Part



9/20 Remove R245,R248,D12

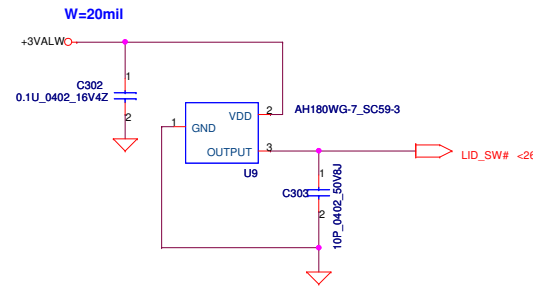


EC_ON
C473
100P_0402_50V8J
Reserve C473 for EC_ON
Tock 2011/01/07

8/26 Change Q14 to SB000009610 Standard Part

9/24 Change U9 to SA00001TC00

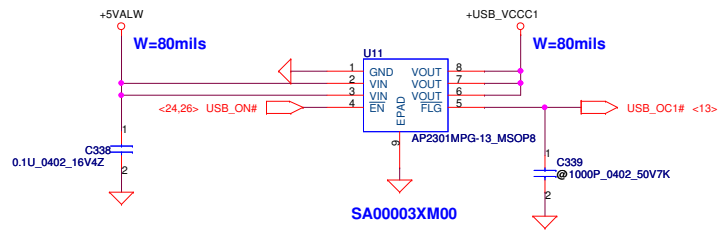
LID Switch



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11/17 Move Left Side USB CONN. Circuit to IO board

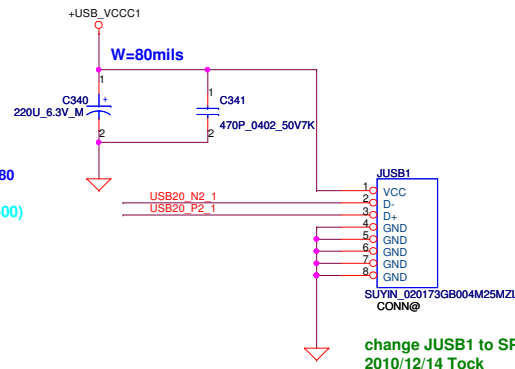


delete D17 for DFB issue
2011/02/25 Tock

8/25 Change C340 from poly-cap to E-cap (SF000001500)

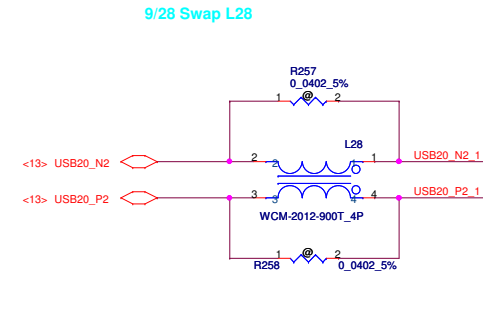
SGA00002N80

Change C340 to SF000001500
2010/12/14 Tock



change JUSB1 to SP060004B00
2010/12/14 Tock

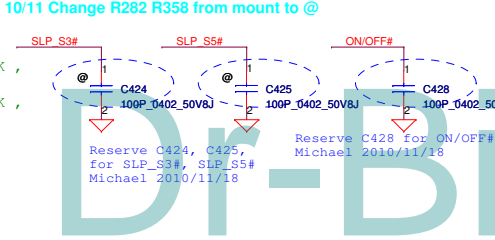
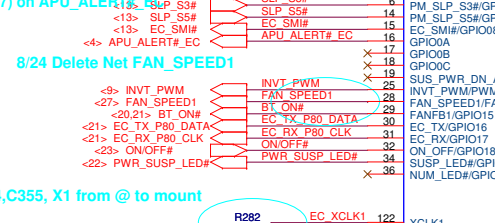
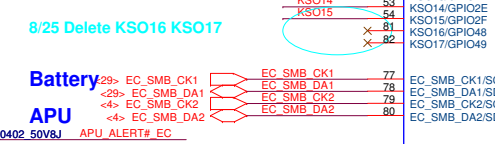
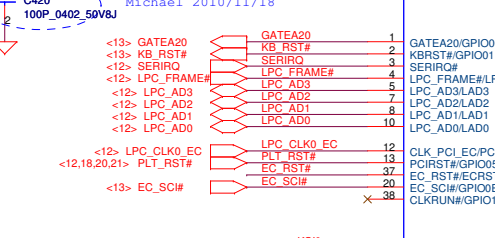
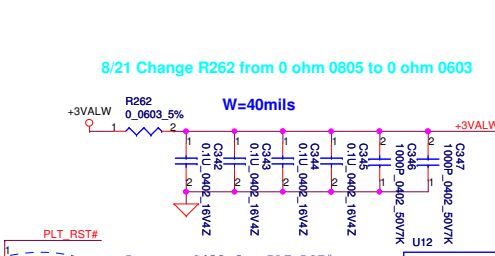
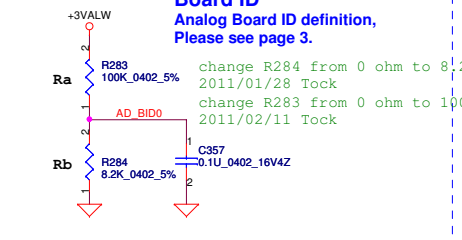
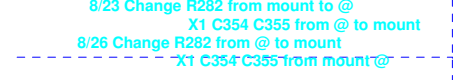
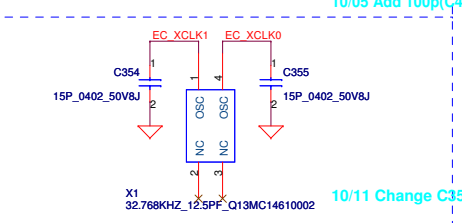
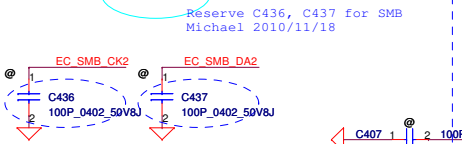
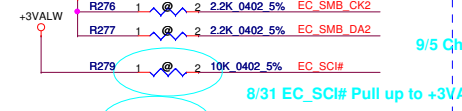
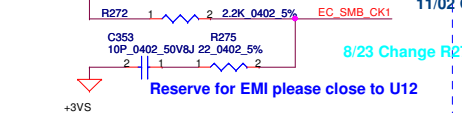
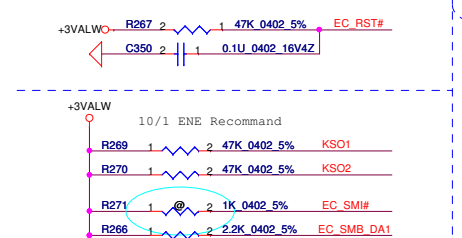
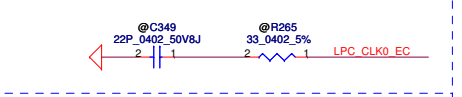
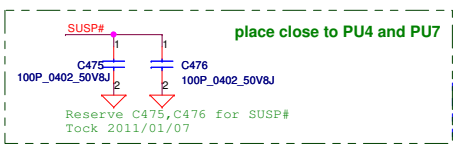
Right Side USB CONN.



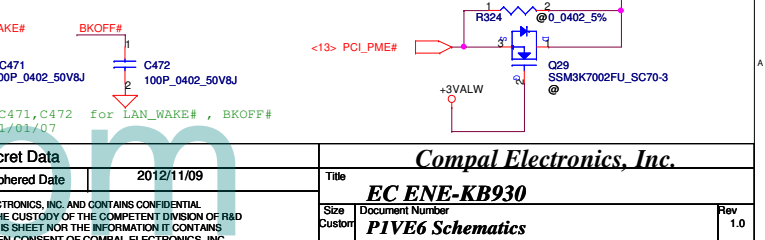
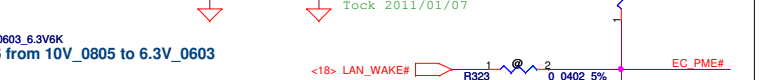
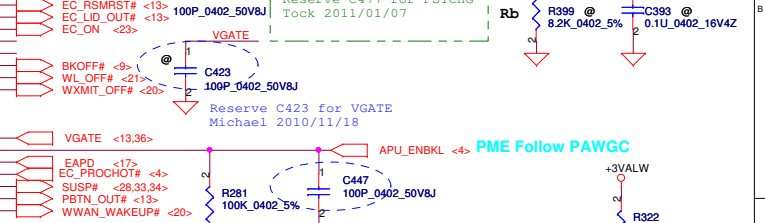
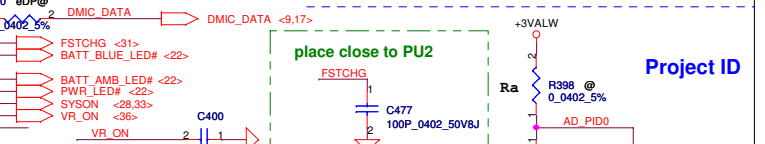
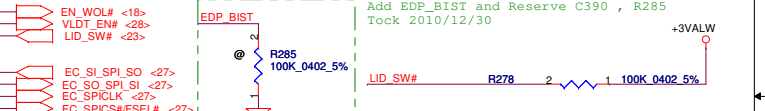
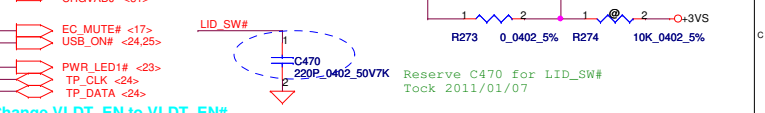
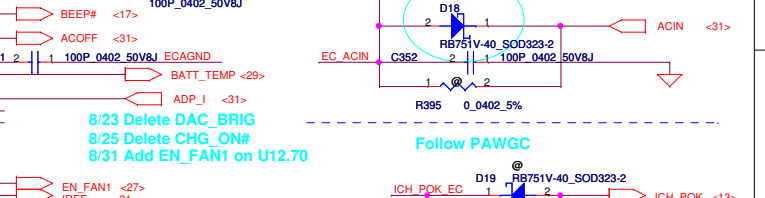
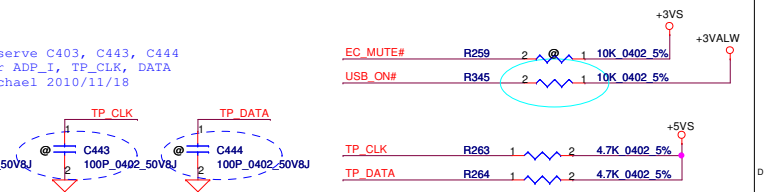
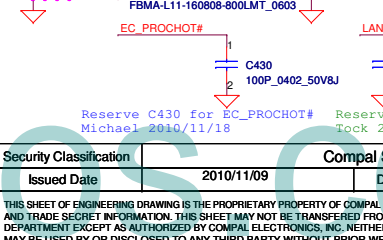
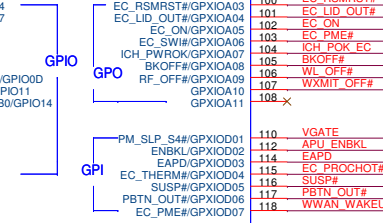
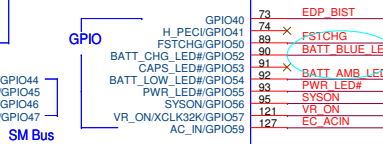
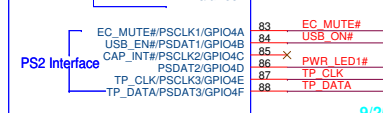
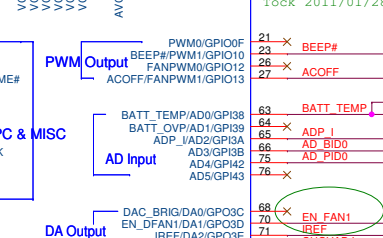
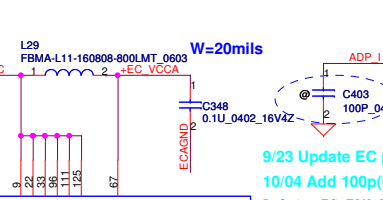
9/28 Swap L28

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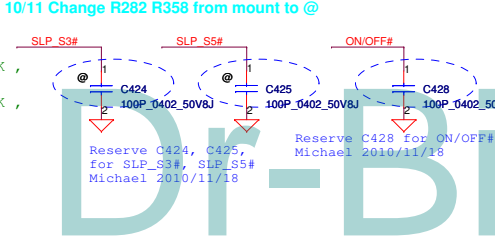
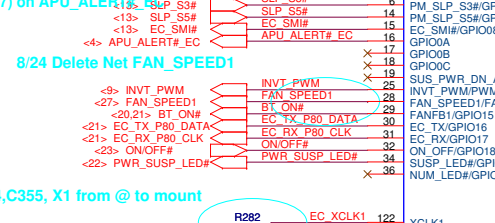
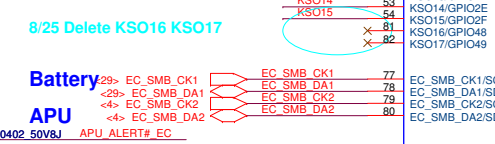
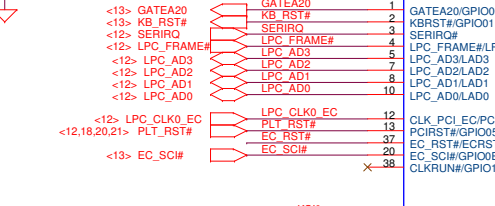
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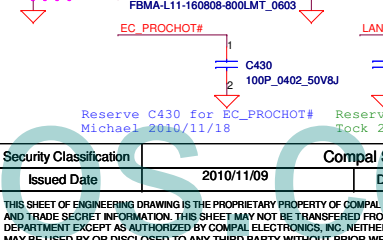
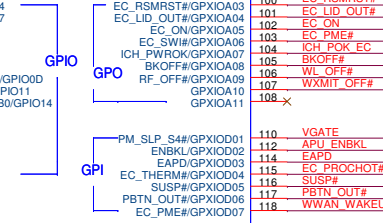
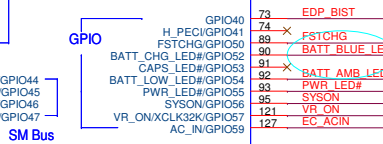
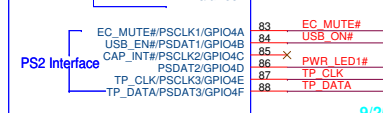
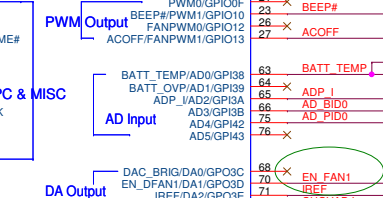
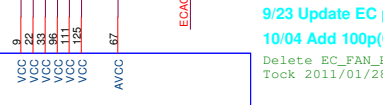
8/23 Pull up 10k (R345) to +3VALW on USB_ON#
8/31 Change EC_MUTE# Pull-up to +3VS(@)



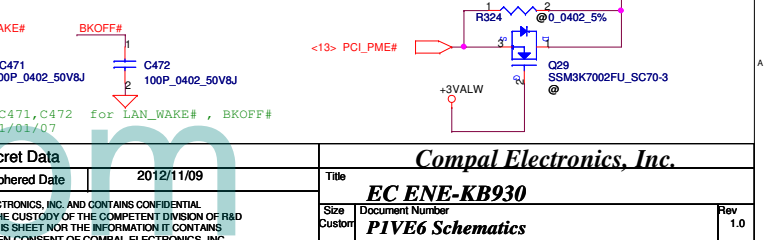
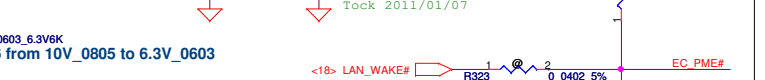
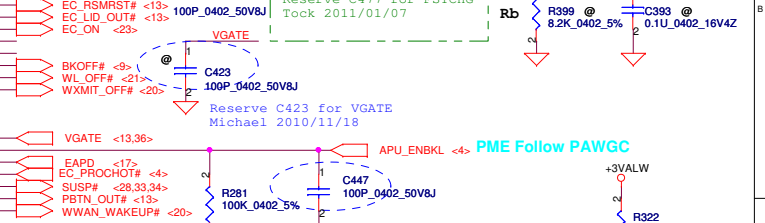
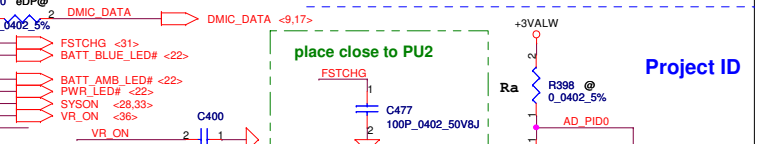
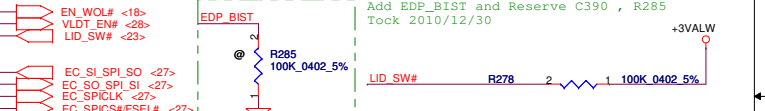
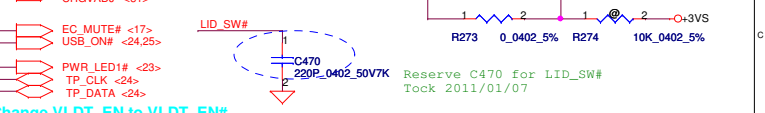
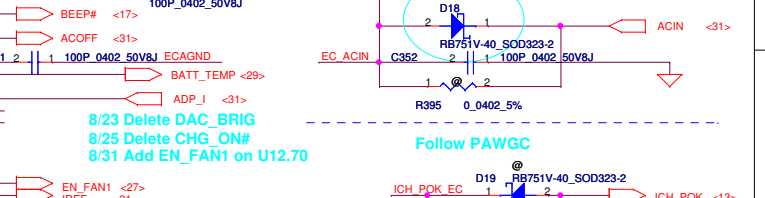
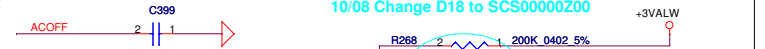
8/21 Change R262 from 0 ohm 0805 to 0 ohm 0603
W=40mils



Reserve C403, C443, C444 for ADP_I, TP_CLK, DATA
Michael 2010/11/18



9/23 Update EC pin definition follow P5WE6
10/04 Add 100p(C399) on ACOFF
Delete EC_FAN_PWM
Tock 2011/01/28



Reserve C420 for PLT_RST#
Michael 2010/11/18

11/02 Change C353 to 10p R275 to 22 ohm

8/23 Change R271 R279 from mount to @

9/5 Change R276 R277 from mount to @

8/31 EC_SCI# Pull up to +3VALW
8/23 Delete R280
Reserve C436, C437 for SMB
Michael 2010/11/18

8/25 Delete KSO16 KSO17

10/05 Add 100p(C407) on APU_ALERT#_EC

8/24 Delete Net FAN_SPEED1

10/11 Change R282 R358 from mount to @

8/23 Delete DAC_BRIG
8/25 Delete CHG_ON#
8/31 Add En FAN# on U12.70

9/25 Change VLDT_EN to VLDT_EN#

9/27 Change C356 from 10V_0805 to 6.3V_0603

10/27 Change C356 from 10V_0805 to 6.3V_0603

8/26 Change D18 to SCS00002G00 Standard Part
9/23 Reserve R395 on ACIN
10/08 Change D18 to SCS00000Z00

Follow PAWGC

Add EDP_BIST and Reserve C390, R285
Tock 2010/12/30

Reserve C477 for FSCHG
Tock 2011/01/07

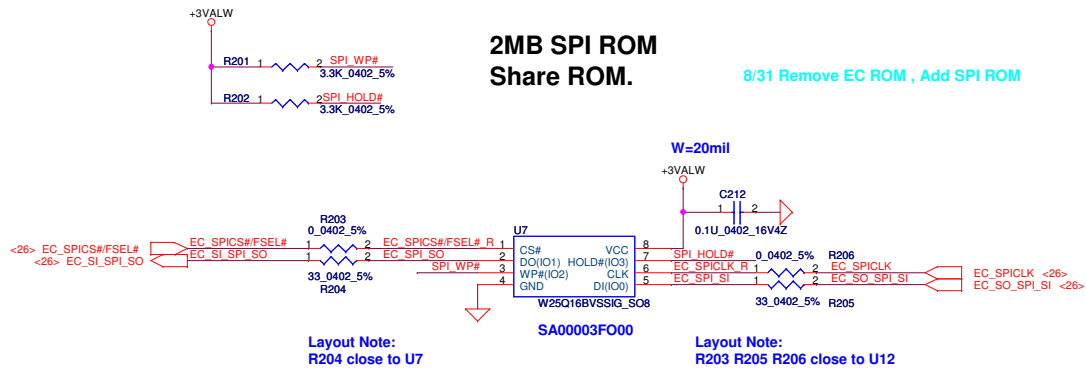
Reserve C423 for VGATE
Michael 2010/11/18

Reserve C423 for VGATE
Michael 2010/11/18

Reserve C423 for VGATE
Michael 2010/11/18

Reserve C423 for VGATE
Michael 2010/11/18

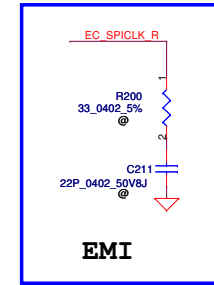
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2MB SPI ROM Share ROM.

8/31 Remove EC ROM , Add SPI ROM

9/2 Change EC_SPICLK to EC_SPICLK_R



Layout Note:
R204 close to U7

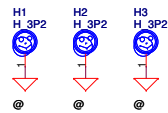
SA00003FO00

Layout Note:
R203 R205 R206 close to U12

Delete U17,C382,C386,R355,D20,C383,C384,C385 for Fan control IC circuit 2010/12/15 Tock

Add U17,C382,C386,R355,D20,C383,C384,C385 for Fan control IC circuit 2011/01/19 Tock

3P2 x 3 (APU)



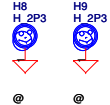
9/15 Update the Screw Hole
9/20 Add H20 (H_3P4X3P2N)
10/07 Change H13 from GND to LANGND
10/07 Change H13 from LANGND to GND

3P0N x 1



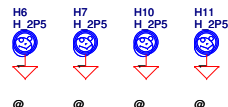
Update the Screw Hole
2010/12/16 Tock

2P3 x 2

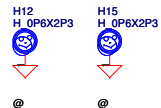


Update the Screw Hole
2010/12/22 Tock

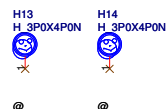
2P5 x 4



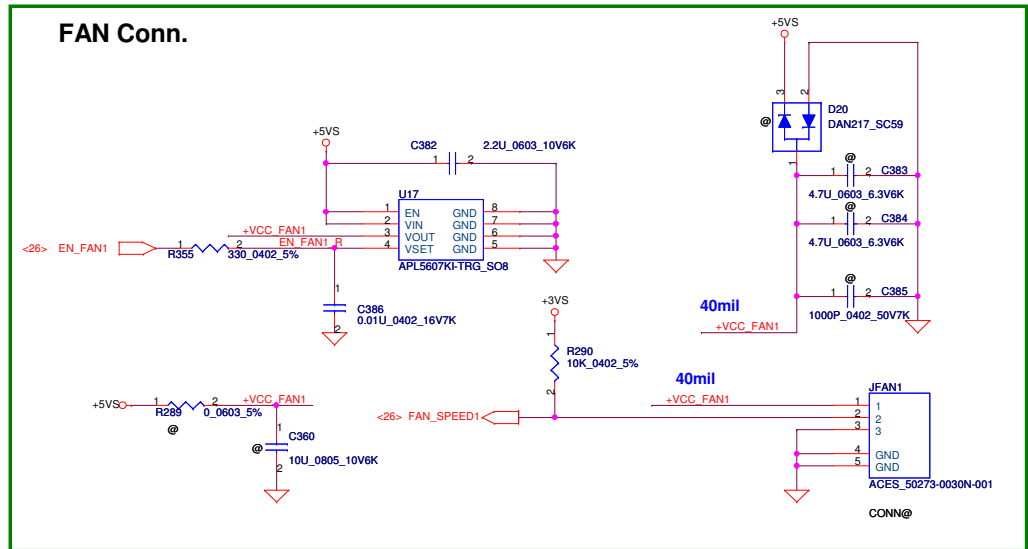
0P6X2P3 x 2



3P0X4P0N x 2



FAN Conn.

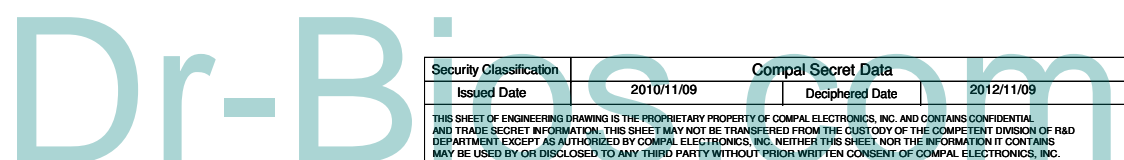


8/24 Update JFAN1 Symbol from database (ACES_85205-03001_3P) & Update pin definition
8/24 Delete R290

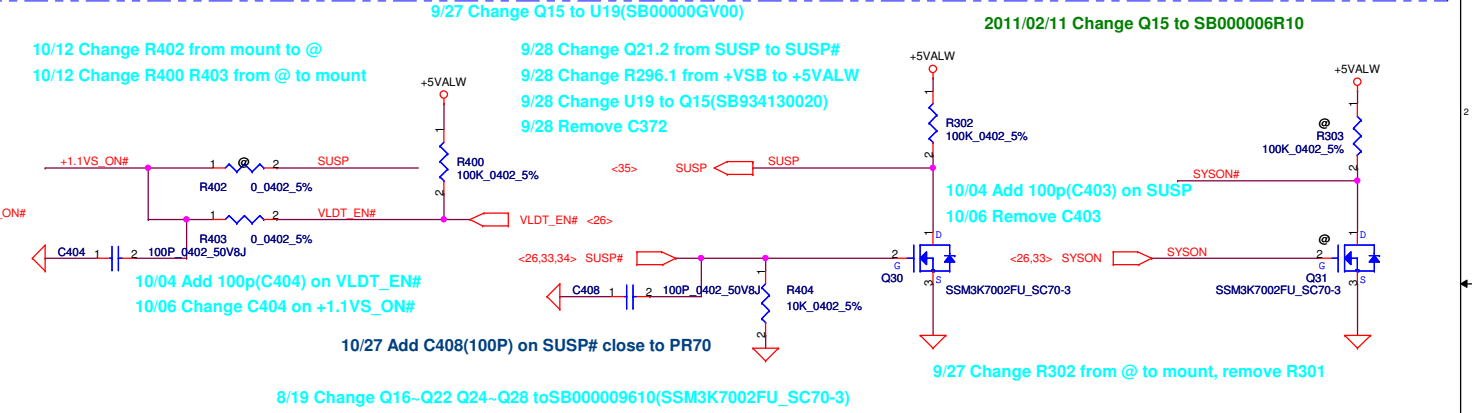
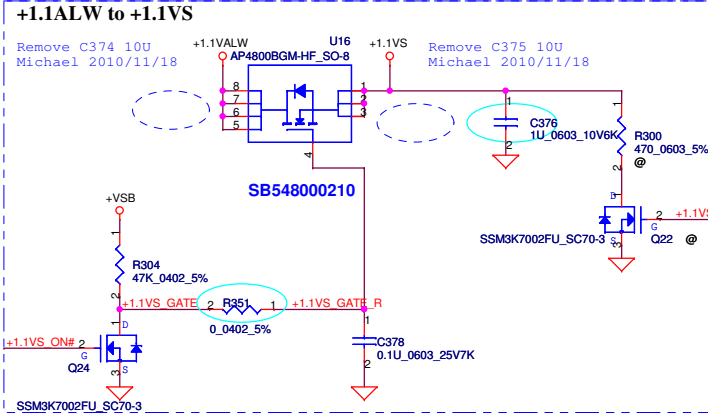
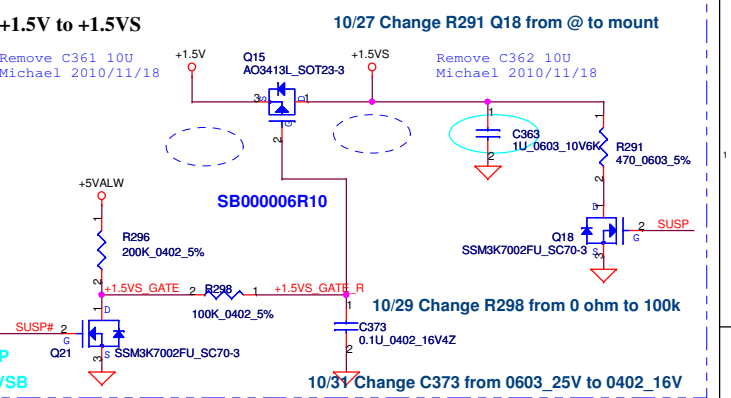
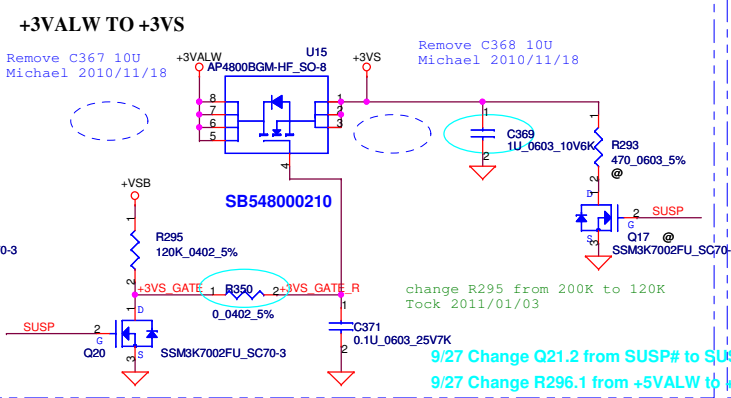
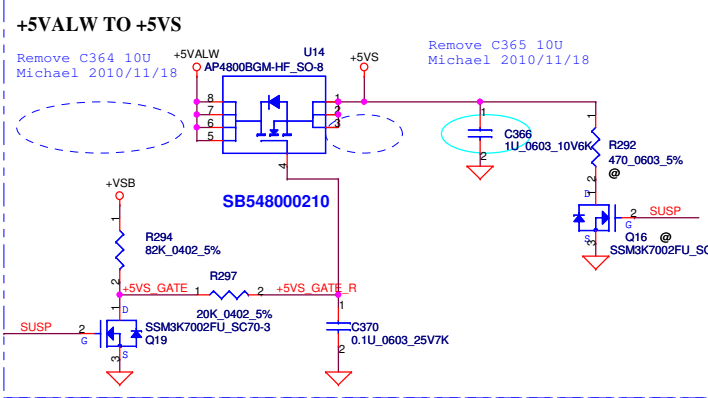
8/25 Update JFAN1 Symbol from database (ACES_85205-04001_4P) & Update pin definition
8/25 Add R290 10k pull-up tp +3VS

8/31 Reserve U17,C382-C386, R355-R357, D20 (Fan Drive Circuit)

change JFAN1 footprint from ACES_85205-04001_4P to ACES_50273-0030N-001_3P , 2011/01/28 Tock ,
delete EC_FAN_PWM and R356,R357 , 2011/01/28 Tock ,



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Size	B	Document Number	P1VE6 Schematics		Rev
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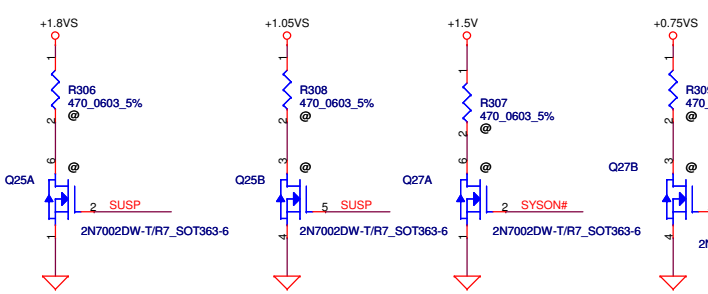


Change Q25 package to SOT363-6 Remove Q26 Michael 2010/11/18
Change Q27 package to SOT363-6 Remove Q28 Michael 2010/11/18

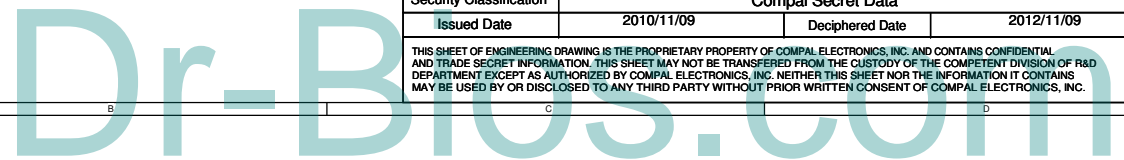
10/12 Change R294 to 100k
10/12 Change R295, R296 to 200k
10/12 Change R304 to 47k
10/12 Change R294 to 82k
10/12 Change R297 to 20k

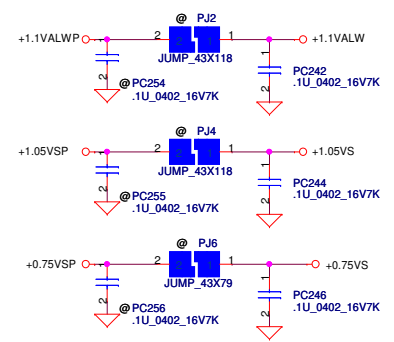
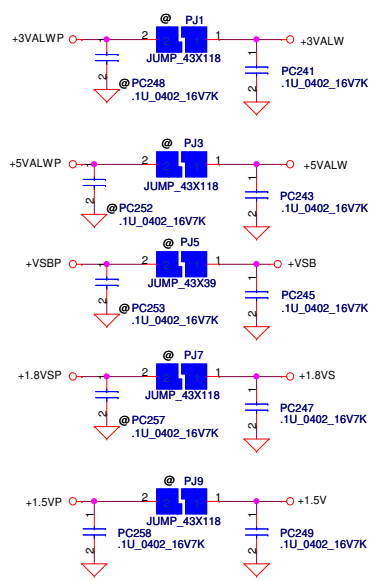
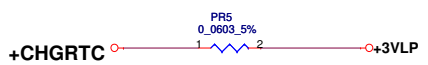
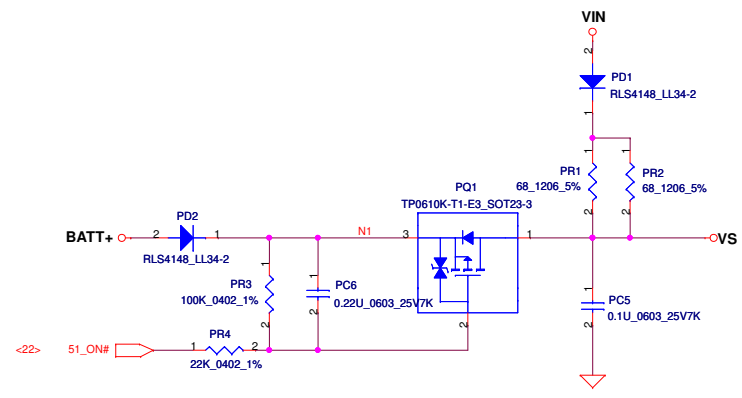
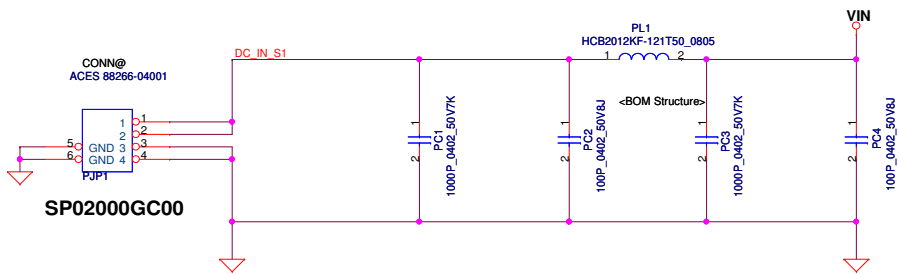
8/19 Change Q16-Q22 Q24-Q28 to SB000009610(SSM3K7002FU_SC70-3)
8/19 Change Q29 Q30 to Q23A Q23B (SB00000DH00 S TR DMN66D0LDW-7 2N SOT363-6)
8/21 Change U14-U16 to SB548000310 (SI4800BDY-T1-E3_SO8)
8/23 Remove R305 R299 Add R350 R351 for Sequence
8/24 Change Q23A Q23B to Q30 Q31(@) (SB000009610 SSM3K7002FU_SC70-3)
8/25 Change C363,C366,C369,C376 to SE080105K80 Standard Part
8/25 Change C361,C362,C364,C365,C367,C368,C374,C375 to SE000004880 Standard Part
8/26 Change U14, U15, U16 to SB00000GV00 Standard Part
9/3 Delete C377(DIS@)
9/23 Reserve R400-403, Q36 for VLDT_EN
9/25 Remove R401 Q36 on VLDT_EN
9/25 Add 10k(R404) PD on SUSP#

10/31 Change C361 C362 from mount to @



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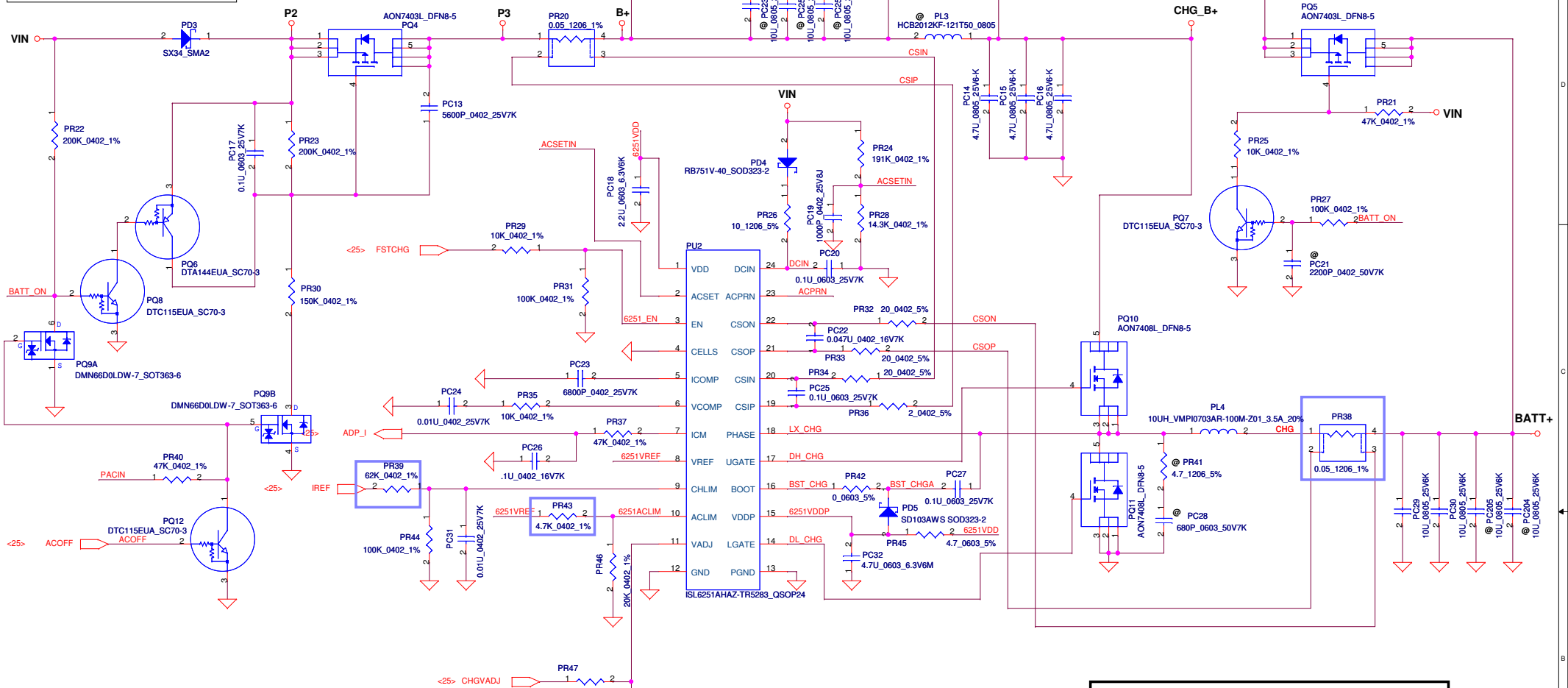
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Iada=0~2.105A (40W/19V=2.105A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 1.789A



BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

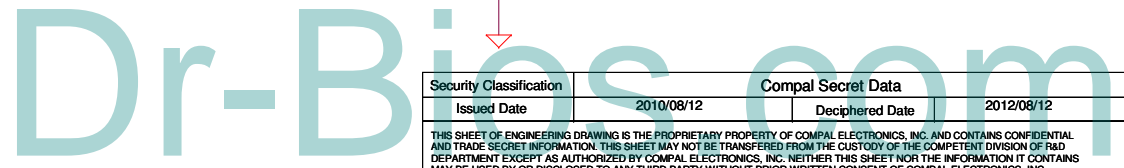
CC=0.25~3.52A
IREF=0.7224*Icharge
IREF=0.43V~3.24V

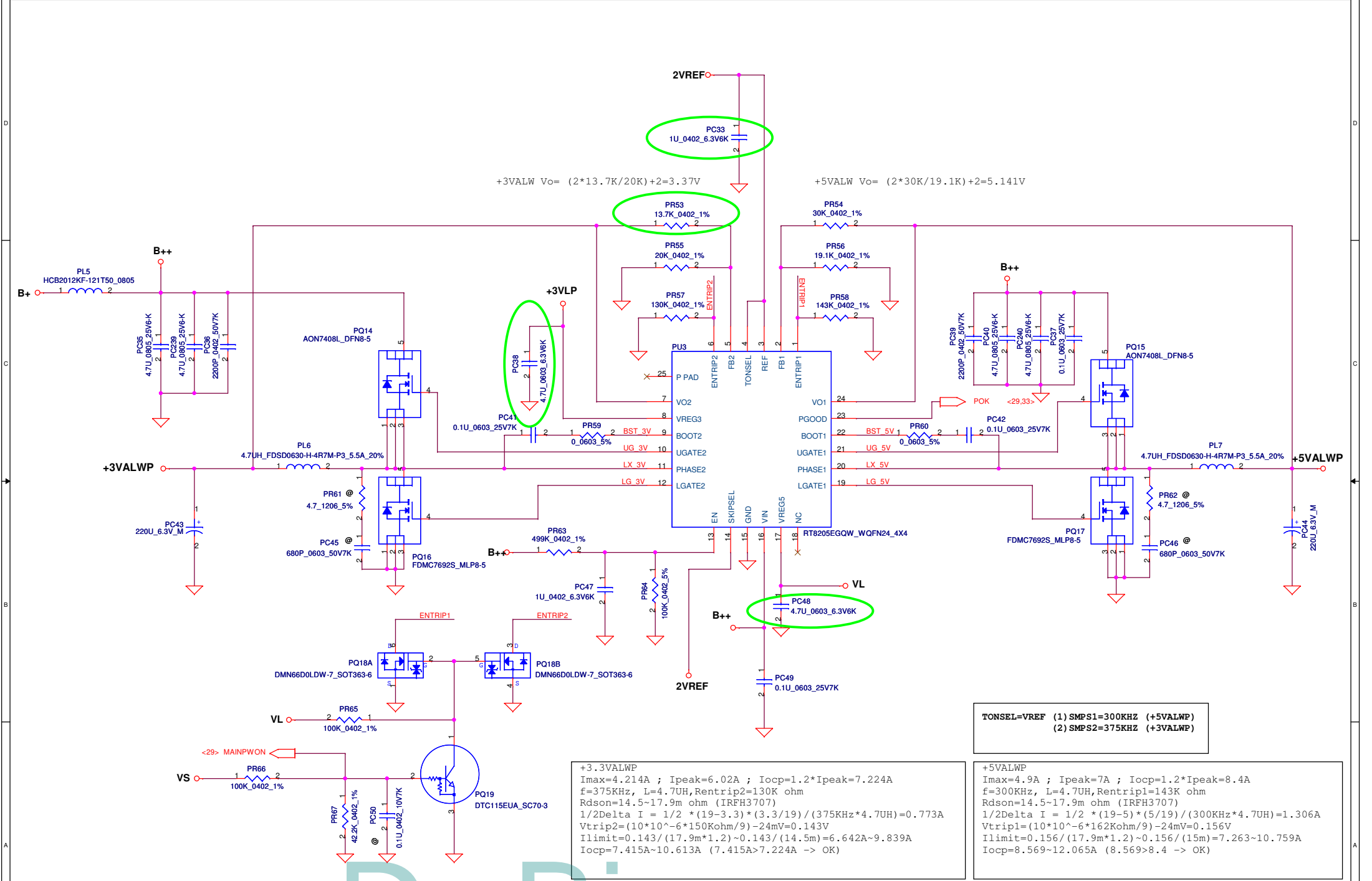
Vth, rise (typical) = ((191K/14.3K)+1)*1.26 = 18.089V
 Vth, fall (typical) = ((191K/14.3K)+1)*1.26 - 3.4uA*191K = 17.44V

Ki
 Vchlim=Iref*(PR39/(PR39+PR44))
 Iref=(100K/(80.6K+100K))
 =Iref*0.617
 Icharge=(165mV/PR38)*(Vchlim/3.3V)
 =(165mV/50m)*(1/3.3V)*Iref*0.617
 =0.617*Iref
 Iref=1.62*Icharge =>Ki=1.62

Kv
 Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
 R=514K/31.6K/(15.4K+3K)=11.372K
 r=514K/514K/31.6K=28.14K
 Vcell=0.175*Vadj+3.99v
 4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
 Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r+514K))
 1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
 1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
 A=Vref*(R/(R+514K))=0.052
 Kv=9.451

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+3VALW Vo= (2*13.7K/20K)+2=3.37V

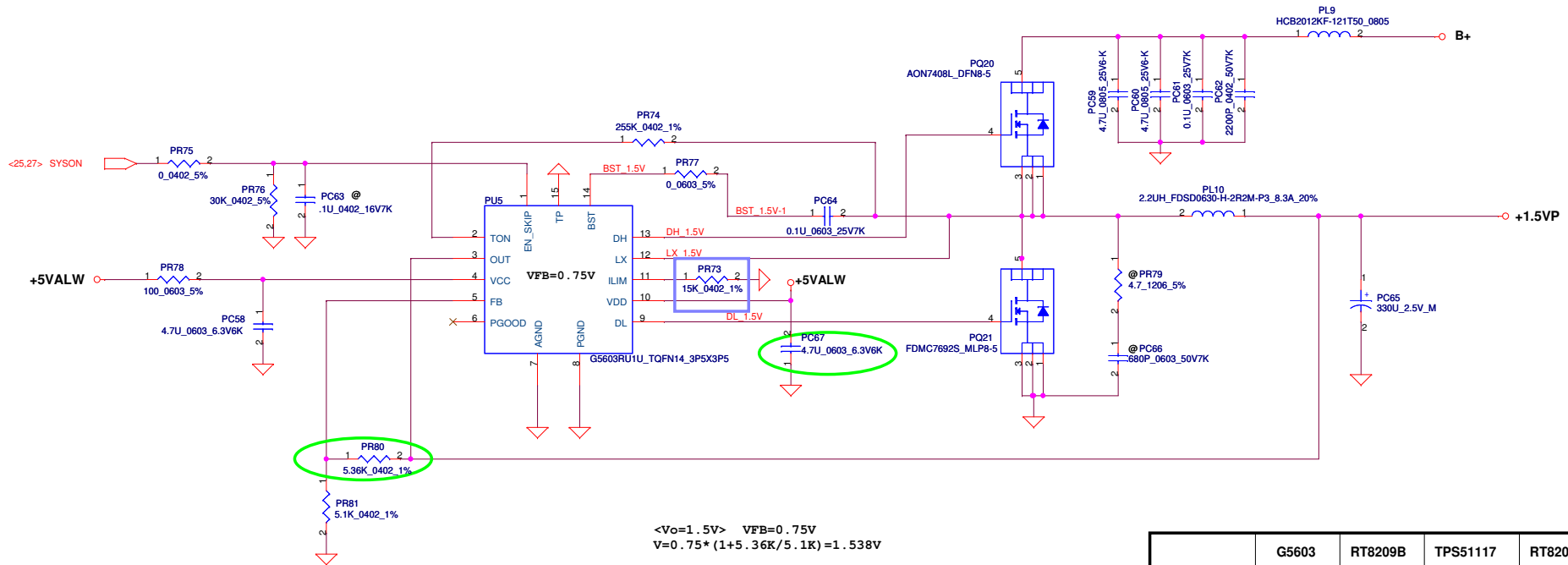
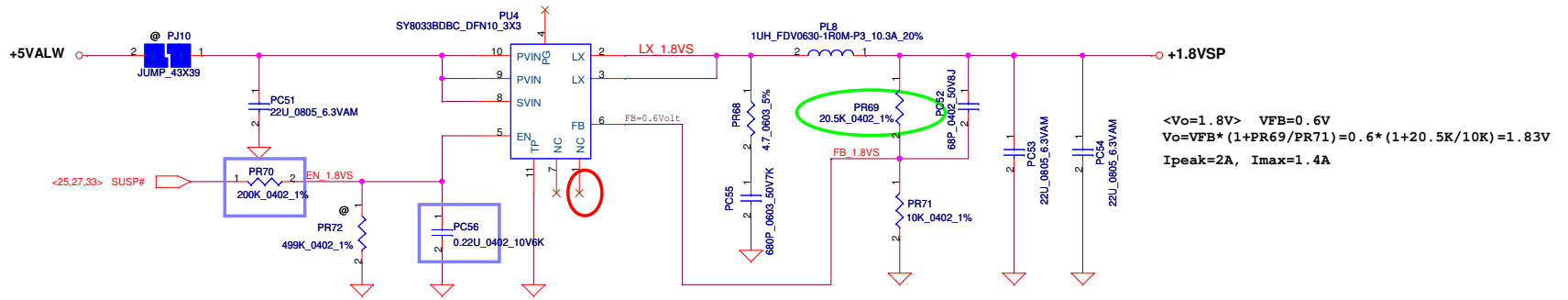
+5VALW Vo= (2*30K/19.1K)+2=5.141V

TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=375KHZ (+3VALWP)

+3.3VALWP
 I_{max}=4.214A ; I_{peak}=6.02A ; I_{ocp}=1.2*I_{peak}=7.224A
 f=375KHz, L=4.7UH, R_{entrip2}=130K ohm
 R_{dson}=14.5~17.9m ohm (IRFH3707)
 1/2Delta I = 1/2 *(19-3.3) *(3.3/19) / (375KHz*4.7UH)=0.773A
 V_{trip2}=(10*10⁻⁶*150Kohm/9)-24mV=0.143V
 I_{limit}=0.143/(17.9m*1.2)-0.143/(14.5m)=6.642A~9.839A
 I_{ocp}=7.415A~10.613A (7.415A>7.224A -> OK)

+5VALWP
 I_{max}=4.9A ; I_{peak}=7A ; I_{ocp}=1.2*I_{peak}=8.4A
 f=300KHz, L=4.7UH, R_{entrip1}=143K ohm
 R_{dson}=14.5~17.9m ohm (IRFH3707)
 1/2Delta I = 1/2 *(19-5) *(5/19) / (300KHz*4.7UH)=1.306A
 V_{trip1}=(10*10⁻⁶*162Kohm/9)-24mV=0.156V
 I_{limit}=0.156/(17.9m*1.2)-0.156/(15m)=7.263~10.759A
 I_{ocp}=8.569~12.065A (8.569>8.4 -> OK)

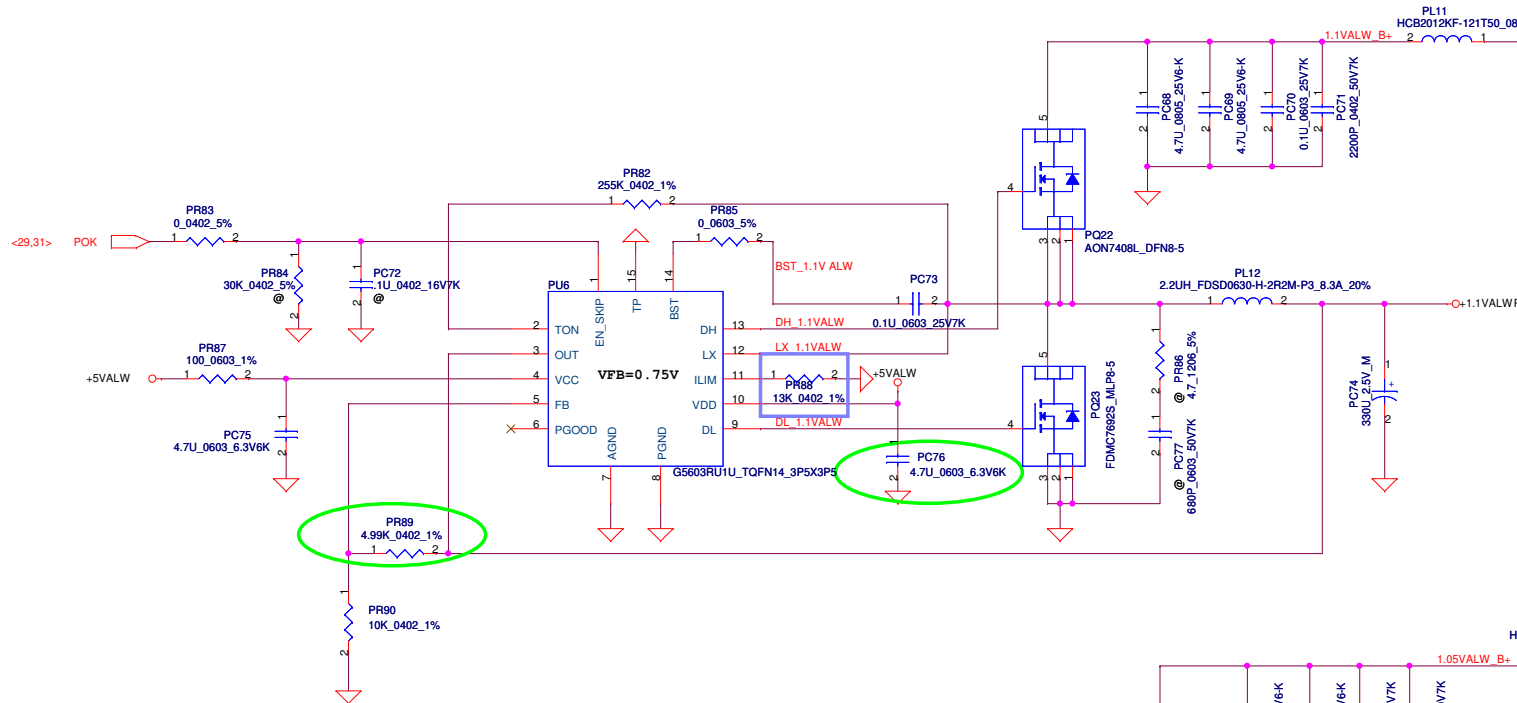
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Cout ESR=25m ohm
 Rdson (max)=17.9 mohm Rdson (typ)=14.5 mohm. (IRFH3707)
 Ipeak=6.5A, Imax=4.55A, Iocp > 7.8A

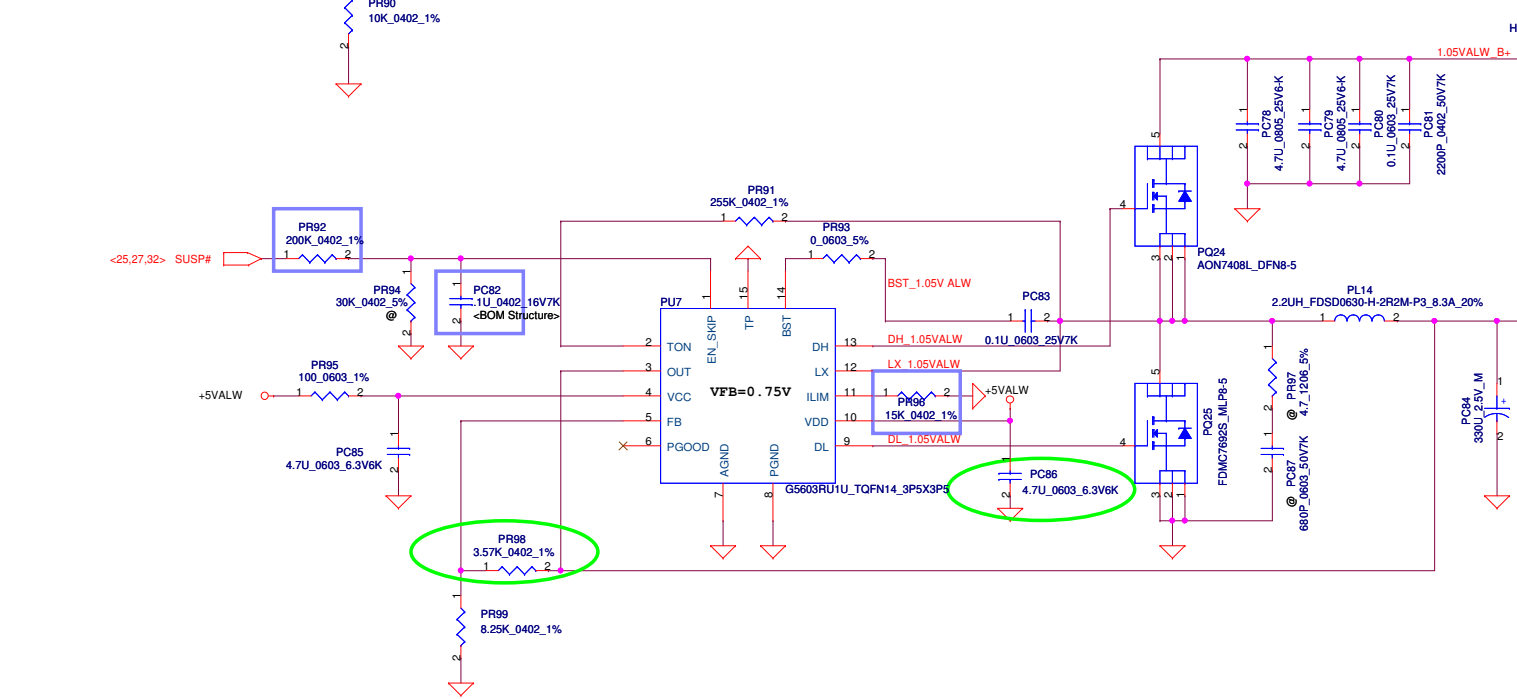
	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.821A	7.235A	8.000A	8.178A

	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV



$\langle V_o=1.1V \rangle$ $V_{FB}=0.75V$
 $V=0.75 * (1+4.99K/10K)=1.124V$
 Cout ESR=25m ohm
 $R_{dson(max)}=17.9$ mohm $R_{dson(typ)}=14.5$ mohm. (IRFH3707)
 $I_{peak}=4.02A$, $I_{max}=2.814A$, $I_{ocp} > 4.824A$

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	5.799A	6.183A	6.845A	6.976A

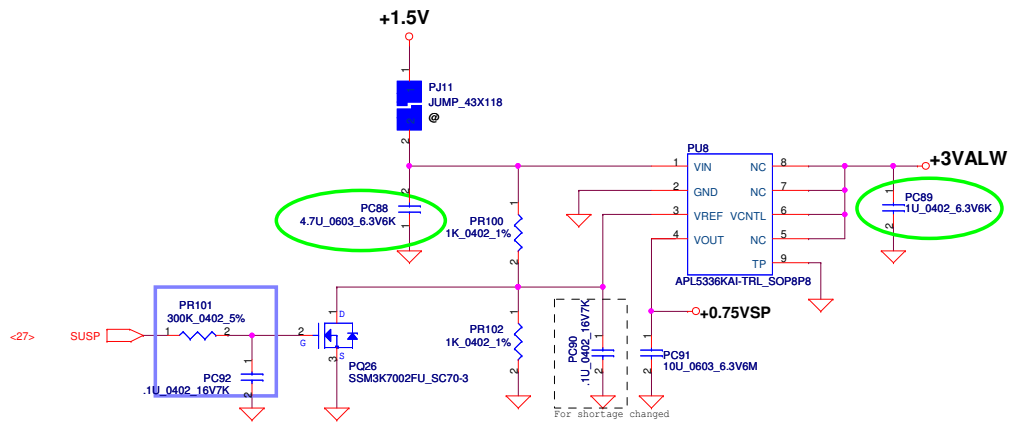


$\langle V_o=1.05V \rangle$ $V_{FB}=0.75V$
 $V=0.75 * (1+3.57K/8.25K)=1.074V$
 Cout ESR=25m ohm
 $R_{dson(max)}=17.9$ mohm $R_{dson(typ)}=14.5$ mohm. (IRFH3707)
 $I_{peak}=5.5A$, $I_{max}=3.85A$, $I_{ocp} > 6.6A$

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.524A	7.003A	7.768A	7.881A

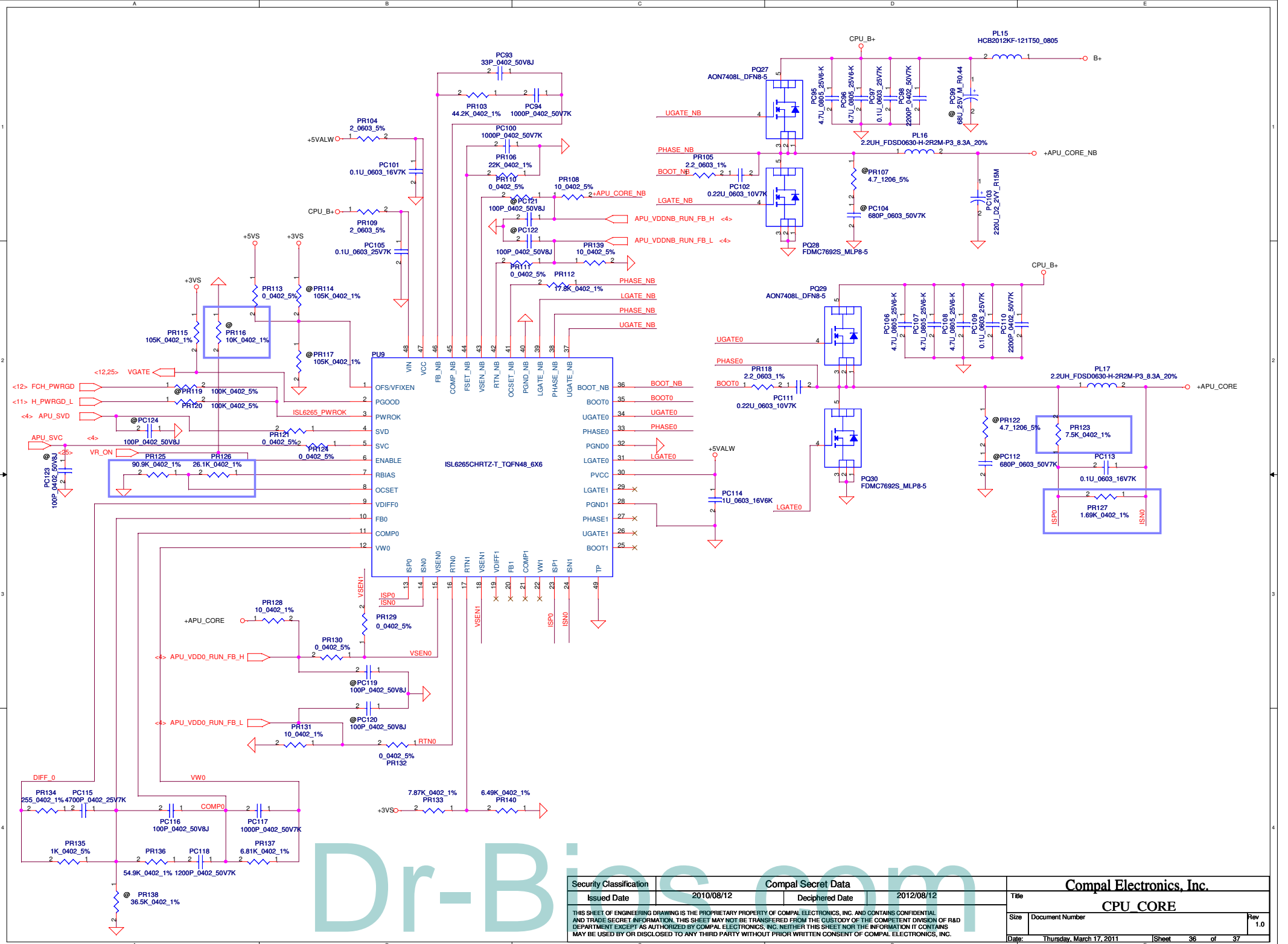
	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

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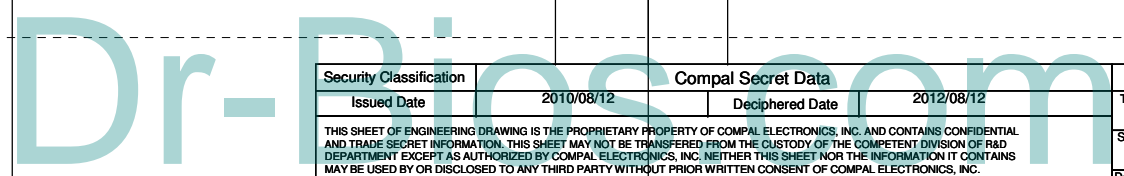
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify DCIN/VIN DECTOR power sequence	1	30	Add PC248 for +3VALWP PC252 for +5VALWP PC253 for +VSBP PC254 for +1.1VALWP PC255 for +1.05VSP PC256 for +0.75VSP PC257 for +1.8VSP	20101228	EVT
2		Modify charger power sequence	1	31	delete PC234	20101228	EVT
3		Modify 3VALWP/5VALWP power sequence	1	32	delete PC34	20101228	EVT
4		Modify charger power sequence	1	31	Chang PD5 from SCS00000200 (RB751V-40_SOD323-2 to SCS00005I00 (SD103AWS SOD323-2)	20110104	EVT
5		Modify charger power sequence	1	31	Chang PD3 from SCS00001180 (B340A SMA) to SCS00000W00 (SX34_SMA2) Chang PQ4&PQ5 from SB00000KI00 (SI7121DN-T1-GE3 1P POWERPAK1212-8) to SB00000KZ00 (AON7403L_DFN8-5)	20110106	EVT
6		Modify 3VALWP/5VALWP power sequence	1	32	Chang PL6 & PL7 from SH00000F900 (4.7UH_FDVE0630-H-4R7M= P3_5.5A_20%) to SH00000MB00 (4.7UH_FDS0630-H-4R7M-P3_5.5A_20%)	20110110	EVT
7		Modify 1.8VSP/1.5VP power sequence	1	33	Chang PL10 from SH00000F800 (2.2UH_FDVE0630-H-2R2M= P3_8.3A_20%) to SH00000M700 (2.2UH_FDS0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
8		Modify 1.1VALWP/1.05VSP power sequence	1	34	Chang PL12 & PL14 from SH00000F800 (2.2UH_FDVE0630-H-2R2M= P3_8.3A_20%) to SH00000M700 (2.2UH_FDS0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
9		Modify CPU_CORE power sequence	1	36	Chang PL16 & PL17 from SH00000F800 (2.2UH_FDVE0630-H-2R2M= P3_8.3A_20%) to SH00000M700 (2.2UH_FDS0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
10		Modify CPU_CORE power sequence	1	36	Chang PR17 from SD034750180 (1.75k_0402_1%) to SD034750180 (1.75k_0402_1%) Chang PR123 from SD000002680 (6.98k_0402_1%) to SD034750180 (7.5k_0402_1%) Chang PR127 from SD034187180 (1.87k_0402_1%) to SD00000J800 (1.69k_0402_1%)	20110110	EVT
11		Modify 1.8VSP/1.5VP power sequence	2	33	add PC258 to +1.5V output capacitor (co-lay higt from 4.5 to 2.5) for thermal issue	20110208	DVT
12		Modify 1.1VALWP/1.05VSP power sequence	2	34	add PC259 to +1.1VALWP output capacitor (co-lay higt from 4.5 to 2.5) for thermal issue	20110208	DVT
13		Modify 1.8VSP/1.5VP power sequence	3	33	delete co-lay PC258 for +1.5V output capacitor	20110225	PVT
14		Modify 1.1VALWP/1.05VSP power sequence	3	34	delete co-lay PC259 for +1.1VALW output capacitor	20110225	PVT
15		Modify charger power sequence	3	31	delete co-lay PJ32 modify P04 P05 footprint from AON7403L_DFN8-5 to SIS412DN-T1-GE3_POWERPAK8-5	20110226	PVT
16		Modify charger power sequence	3	31	change charger IC from G5209 to ISL6251 change output choke from 8.2u to 10u	20110226	PVT
17		Modify DCIN/VIN DECTOR power sequence	3	30	Add PC258 for +1.5V jump by RF test	2010302	PVT
18							
19							
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				PIR (PWR)			
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