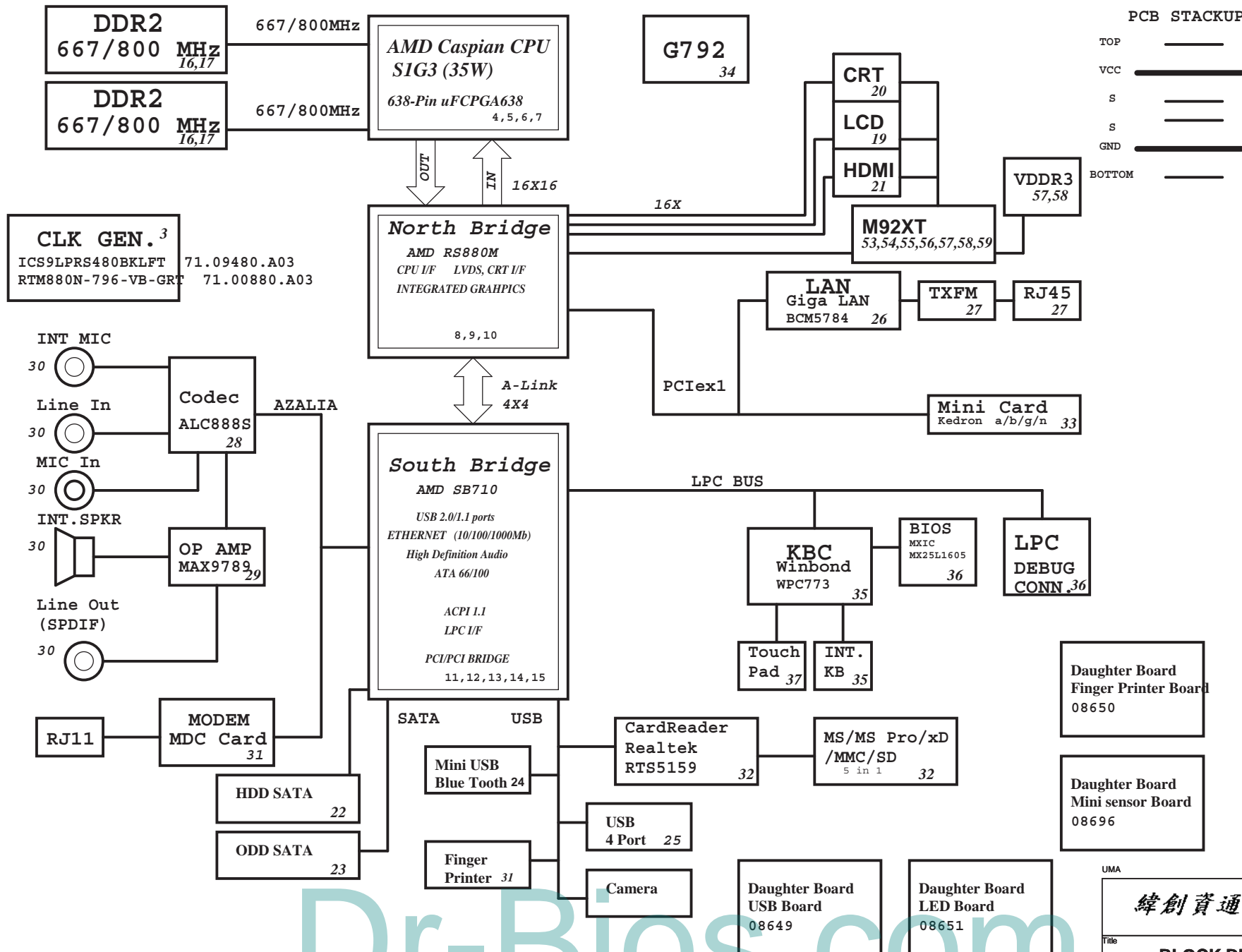


# JV71-TR Block Diagram

Project code: 91.4FP01.001  
 PCB P/N : 48.4FP02.0SB  
 REVISION : 09243-SB



PCB STACKUP

TOP	_____
VCC	_____
S	_____
S	_____
GND	_____
BOTTOM	_____

SYSTEM DC/DC RT8205A 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (6A)
	3D3V_S5 (6A)

SYSTEM DC/DC TPS51124 47	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0 (7.5A)
	1D2V_S0 (4A)

SYSTEM DC/DC RT8209B 48	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 (11A)

RT9025 49	
5V_S5	1D1V_M92

RT9161 49	
3D3V_S0	2D5V_S0 (200mA)

G957 49	
3D3V_S0	1D5V_S0 (1A)

G9161 49	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
	UP+5V 5V 100mA

CPU DC/DC ISL6265HR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A
	VCC_CORE_S0_1 0~1.55V 18A
	VDDNB 0~1.55V 18A

UMA

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

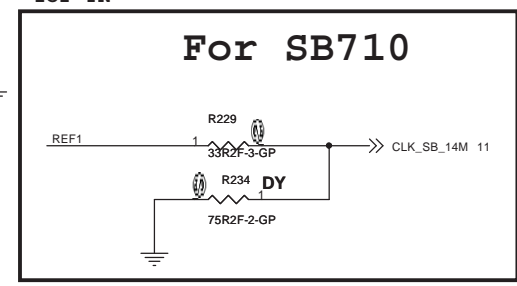
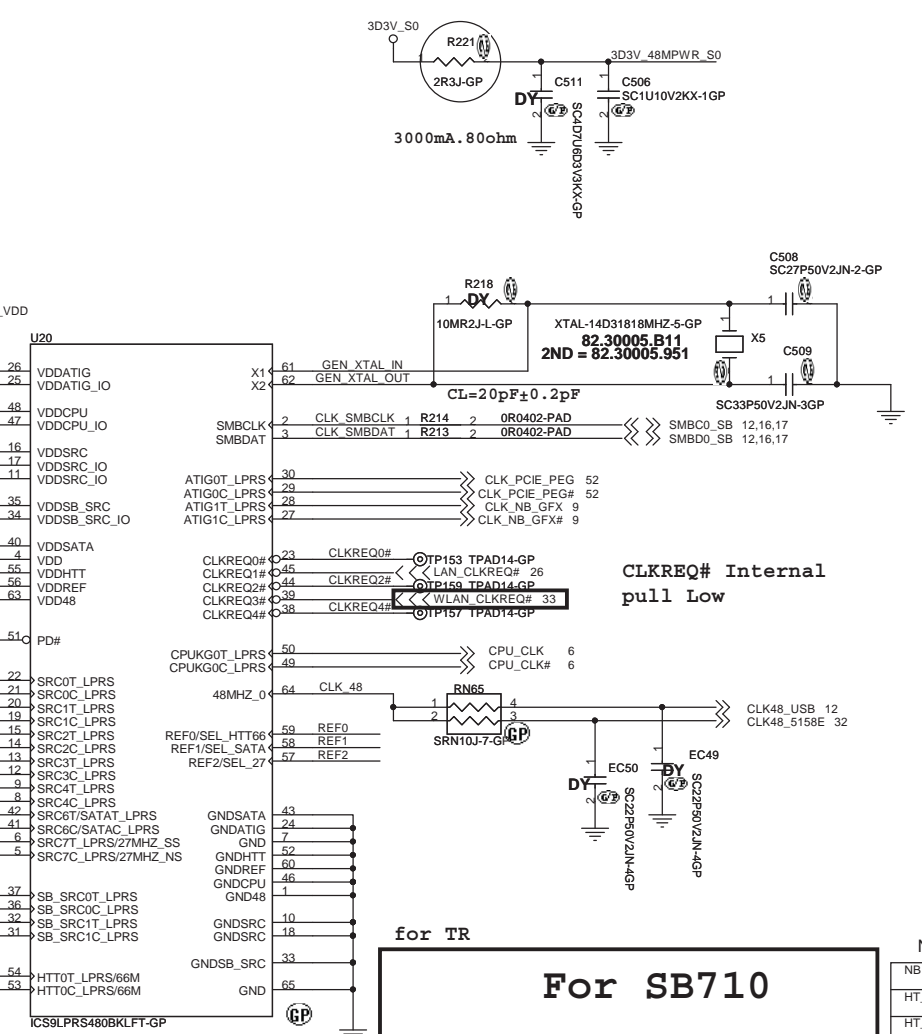
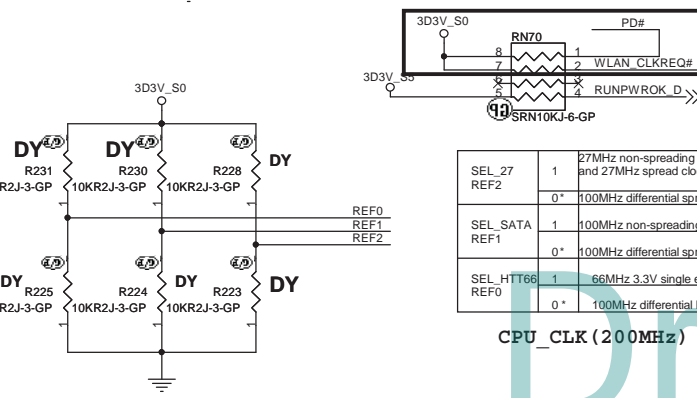
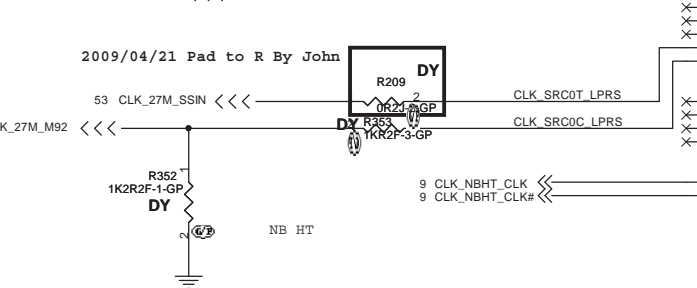
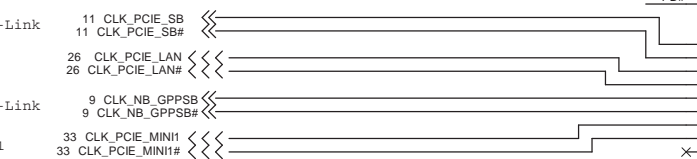
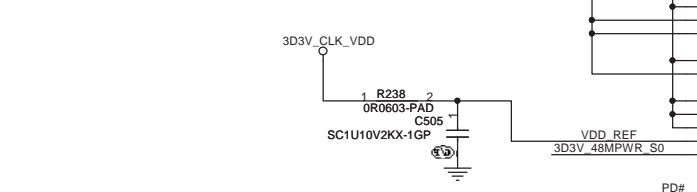
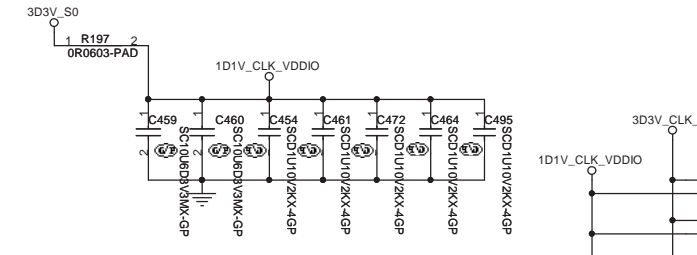
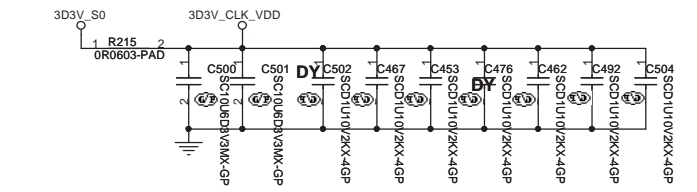
Size: A3	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet: 1	of: 61

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Title			
<b>USB/PCIE Routing</b>			
Size	Document Number	Rev	
A3	<b>JV71-TR</b>	SA	
Date: Monday, July 06, 2009	Sheet 2	of 61	



Due to PLL issue on current clock chip, the Sblink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

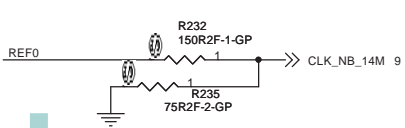
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

### NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

\* RS780 can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.

SEL_27	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
REF2	0*	100MHz differential spreading SRC clock
SEL_SATA	1	100MHz non-spreading differential SATA clock
REF1	0*	100MHz differential spreading SRC clock
SEL_HTT66	1	66MHz 3.3V single ended HTT clock
REF0	0*	100MHz differential HTT clock



OSC 14M NB  
RS780M 1.1V 158R/90.9R

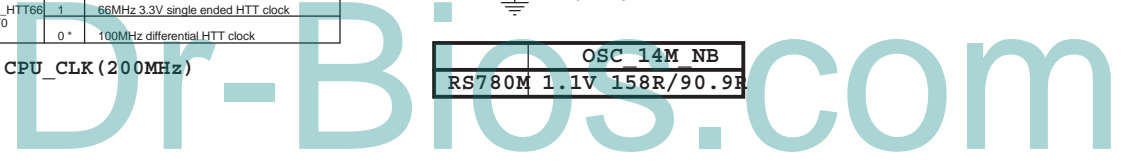
UMA

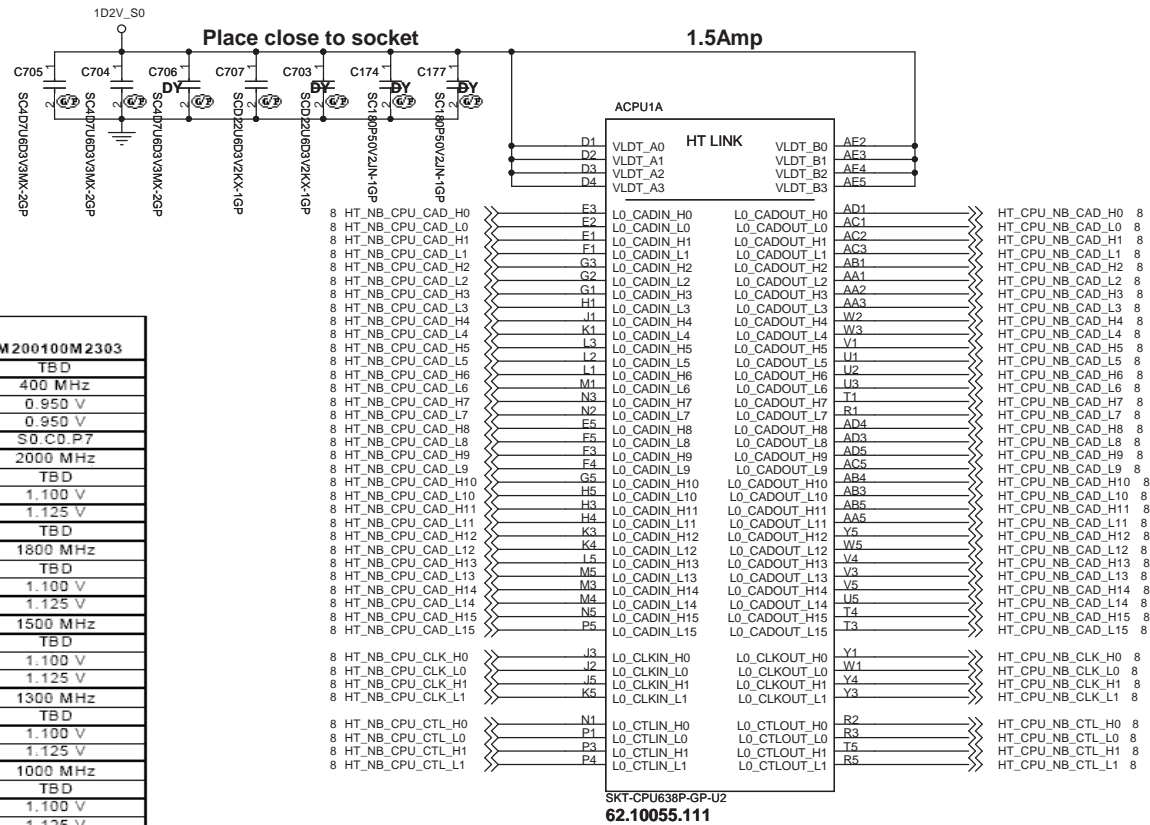
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CLKGEN ICS9LPRS480**

Size: A3 Document Number: **JV71-TR** Rev: SB

Date: Monday, July 06, 2009 Sheet 3 of 61





State	Specification	Notes	ZM200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

SKT-BGA638H176

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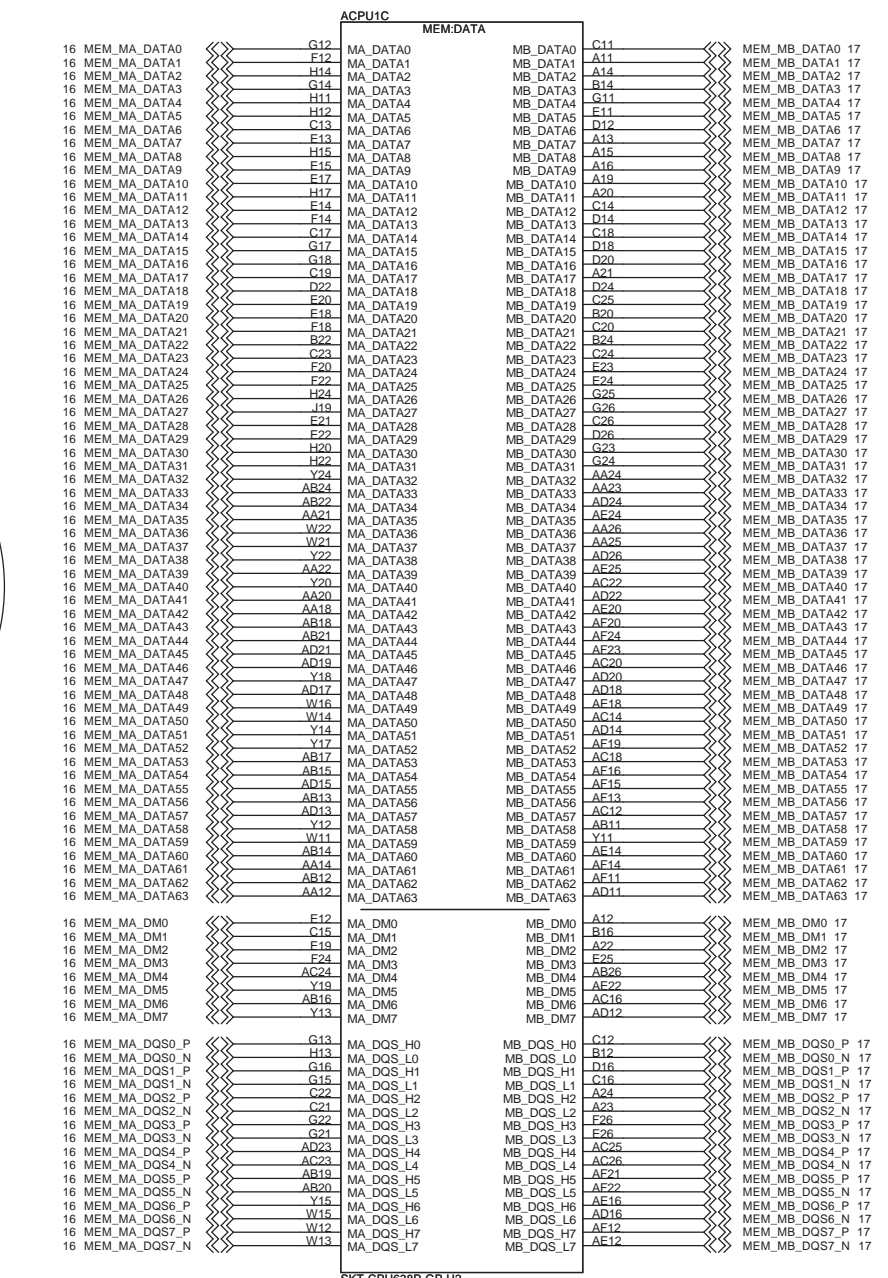
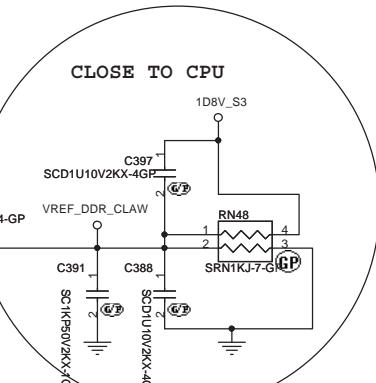
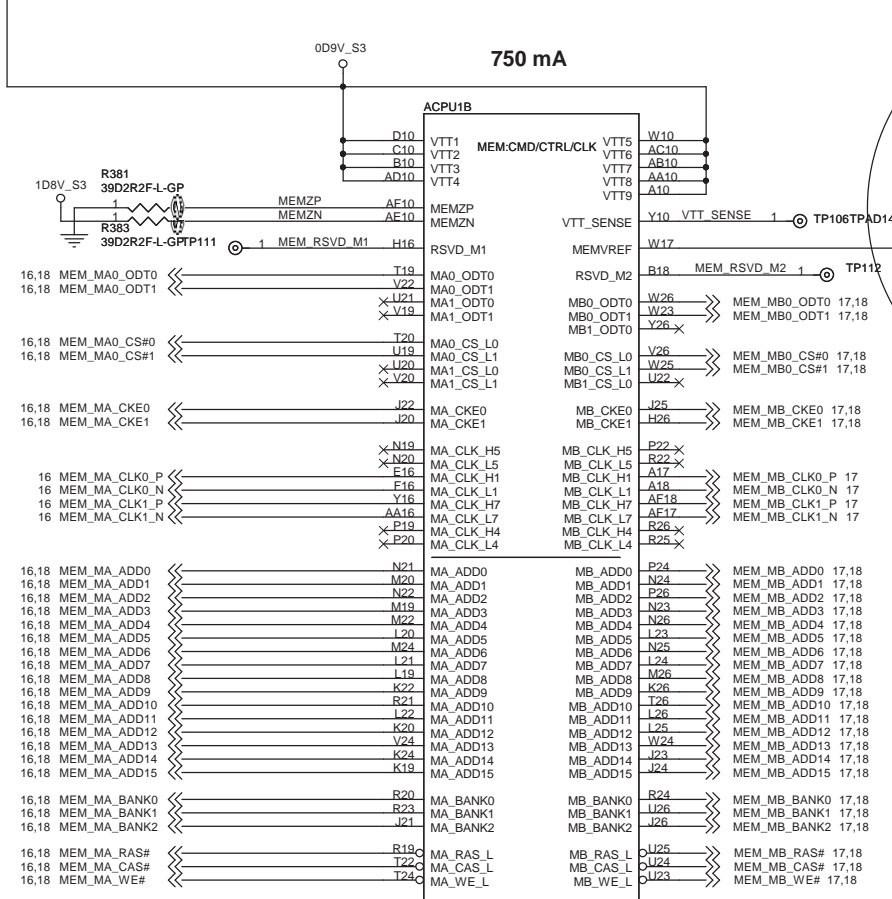
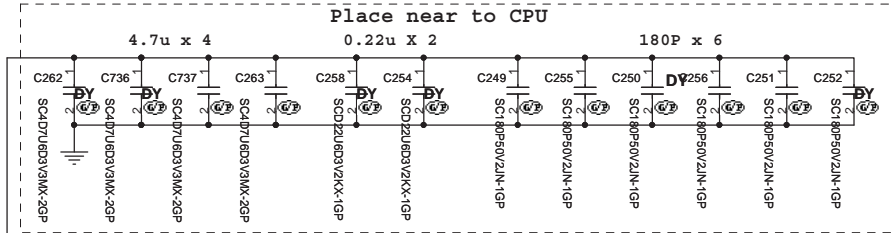
UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU HT LINK I/F (1/4)**

Size: **A3** Document Number: **JV71-TR** Rev: **SA**

Date: Monday, July 06, 2009 Sheet 4 of 61



SKT-CPU638P-GP-U2  
62.10055.111

SKT-CPU638P-GP-U2  
62.10055.111



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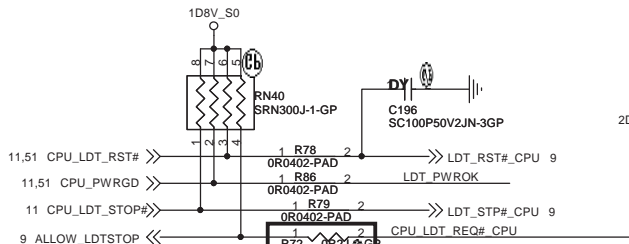
緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU DDR (2/4)

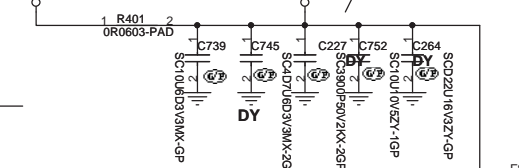
Size: A3 Document Number: JV71-TR Rev: SA

Date: Monday, July 06, 2009 Sheet: 5 of 61

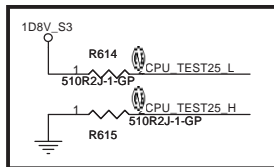
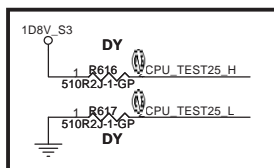
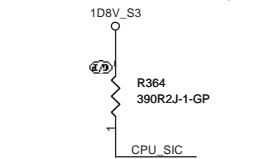
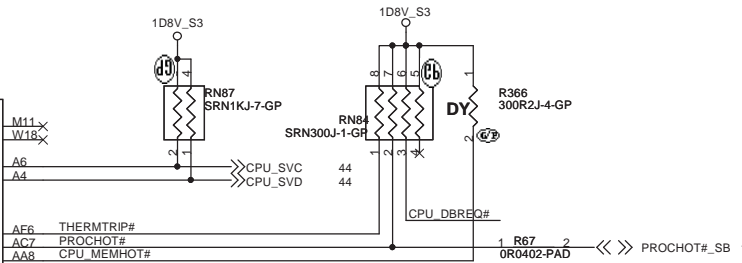
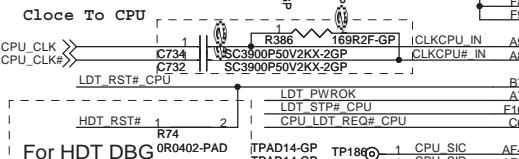
The Processor has reached a preset maximum operating temperature. 100°C  
I=Active HTC  
O=FAN



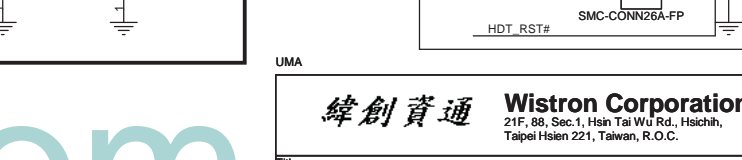
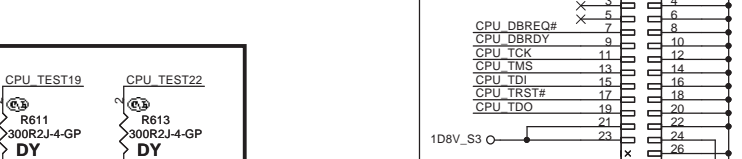
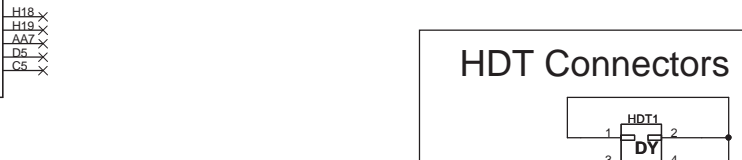
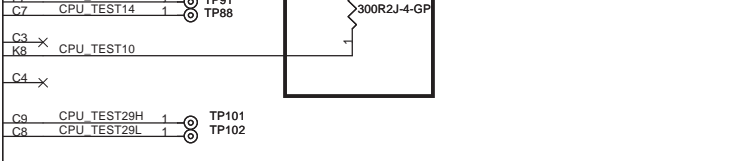
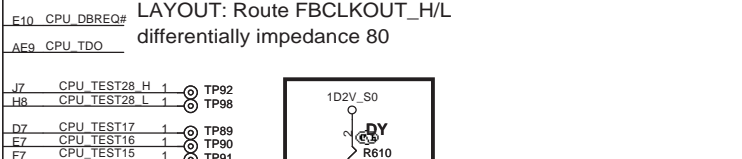
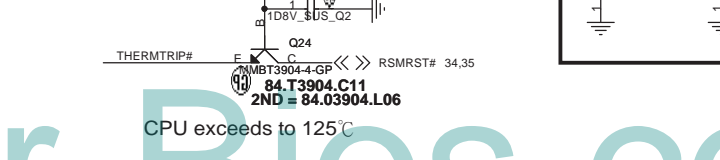
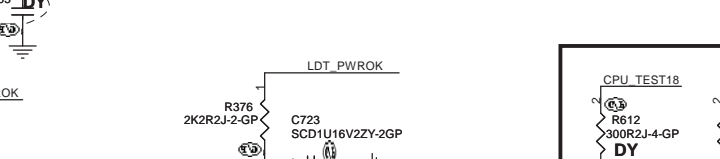
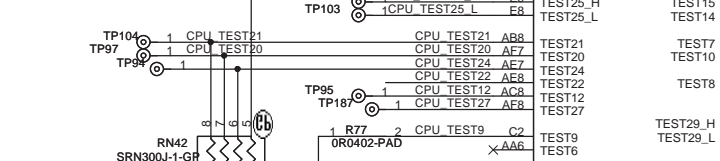
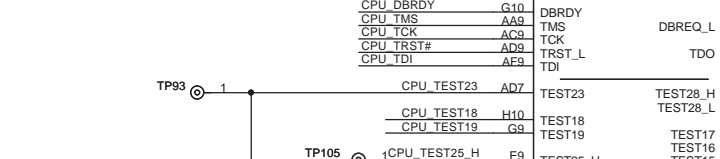
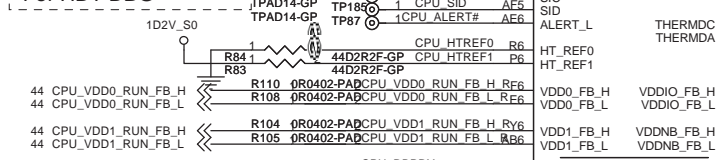
IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491  
LYAOUT:ROUTE VDDA TRACE APPROX.  
50mils WIDE(USE 2X25 ml TRACES TO  
EXIT BALL FIELD) AND 500 mils LONG.



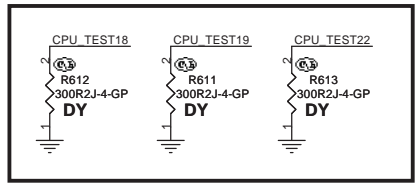
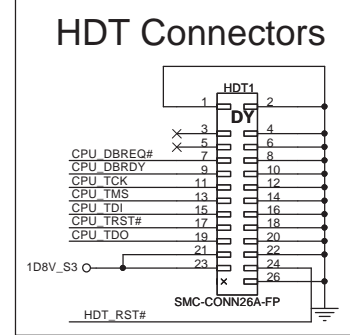
ACPU1D



for TR



LAYOUT: Route FBCLKOUT\_H/L  
differentially impedance 80



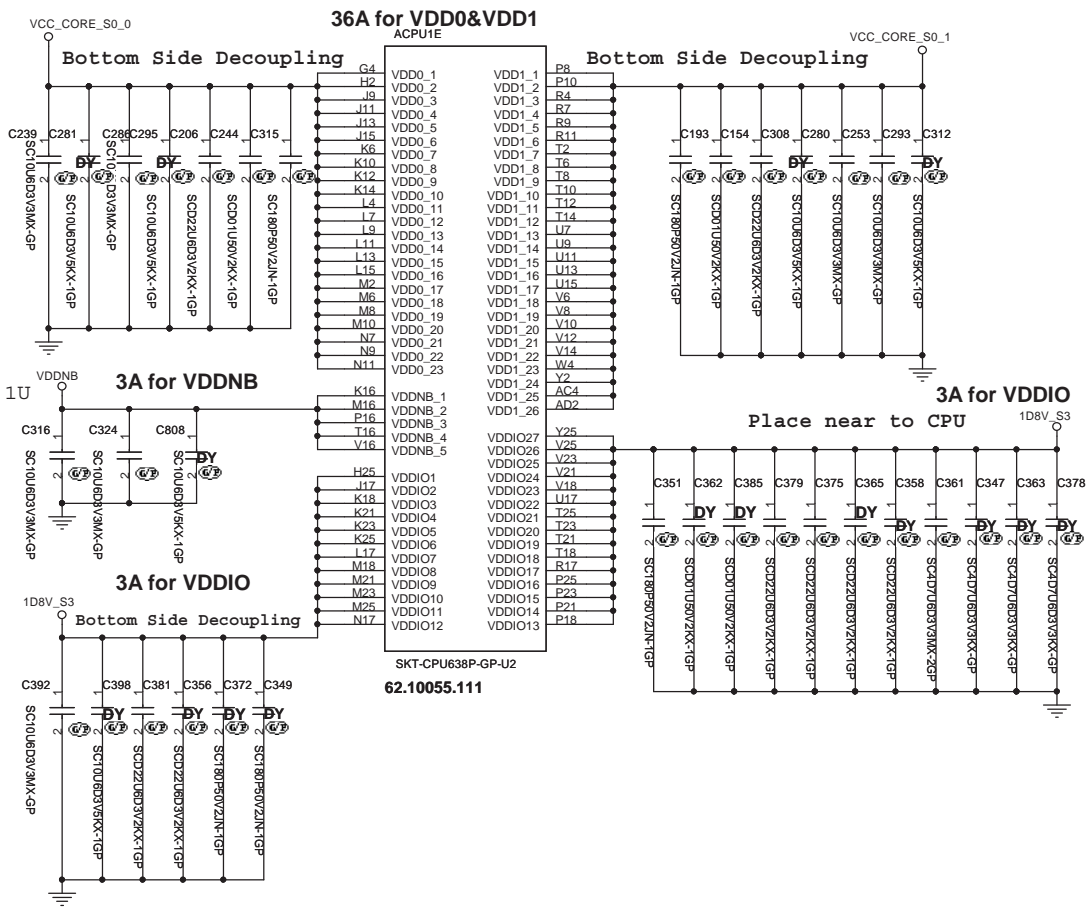
CPU exceeds to 125°C

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU_Control&Debug_(3/4)	
Size A3	Document Number JV71-TR
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ACPU1F		
AA4	VSS1	VSS66
AA11	VSS2	VSS67
AA13	VSS3	VSS68
AA15	VSS4	VSS69
AA17	VSS5	VSS70
AA19	VSS6	VSS71
AB2	VSS7	VSS72
AB7	VSS8	VSS73
AB9	VSS9	VSS74
AB23	VSS10	VSS75
AB25	VSS11	VSS76
AC11	VSS12	VSS77
AC13	VSS13	VSS78
AC15	VSS14	VSS79
AC17	VSS15	VSS80
AC19	VSS16	VSS81
AC21	VSS17	VSS82
AD6	VSS18	VSS83
AD8	VSS19	VSS84
AD25	VSS20	VSS85
AE11	VSS21	VSS86
AE13	VSS22	VSS87
AE15	VSS23	VSS88
AE17	VSS24	VSS89
AE19	VSS25	VSS90
AE21	VSS26	VSS91
AE23	VSS27	VSS92
B4	VSS28	VSS93
B6	VSS29	VSS94
B8	VSS30	VSS95
B9	VSS31	VSS96
B11	VSS32	VSS97
B12	VSS33	VSS98
B15	VSS34	VSS99
B17	VSS35	VSS100
B19	VSS36	VSS101
B21	VSS37	VSS102
B23	VSS38	VSS103
B25	VSS39	VSS104
D6	VSS40	VSS105
D8	VSS41	VSS106
D9	VSS42	VSS107
D11	VSS43	VSS108
D13	VSS44	VSS109
D15	VSS45	VSS110
D17	VSS46	VSS111
D19	VSS47	VSS112
D21	VSS48	VSS113
D23	VSS49	VSS114
D25	VSS50	VSS115
F4	VSS51	VSS116
F2	VSS52	VSS117
F11	VSS53	VSS118
F13	VSS54	VSS119
F15	VSS55	VSS120
F17	VSS56	VSS121
F19	VSS57	VSS122
F21	VSS58	VSS123
F23	VSS59	VSS124
F25	VSS60	VSS125
H7	VSS61	VSS126
H9	VSS62	VSS127
H21	VSS63	VSS128
H23	VSS64	VSS129
J4	VSS65	VSS129

SKT-CPU638P-GP-U2  
62.10055.111



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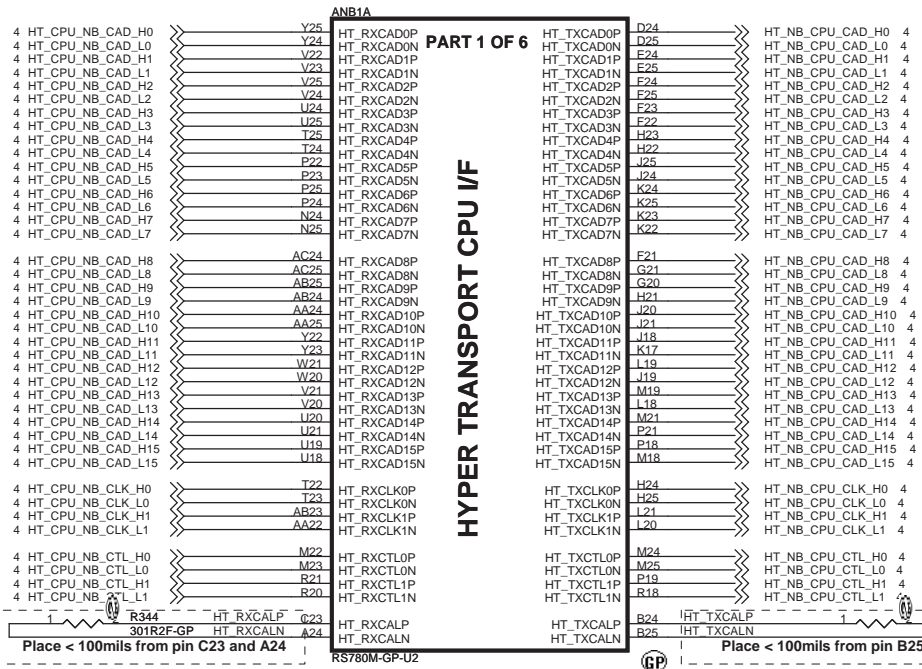
UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU\_Power\_(4/4)**

Size: A3 Document Number: **JV71-TR** Rev: SA

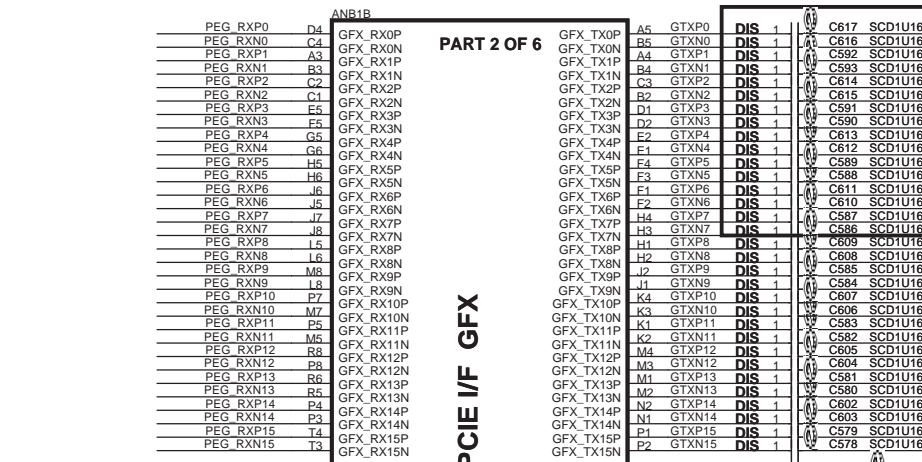
Date: Monday, July 06, 2009 Sheet 7 of 61



**RS780 SYMBOL**

Placement: close RS780

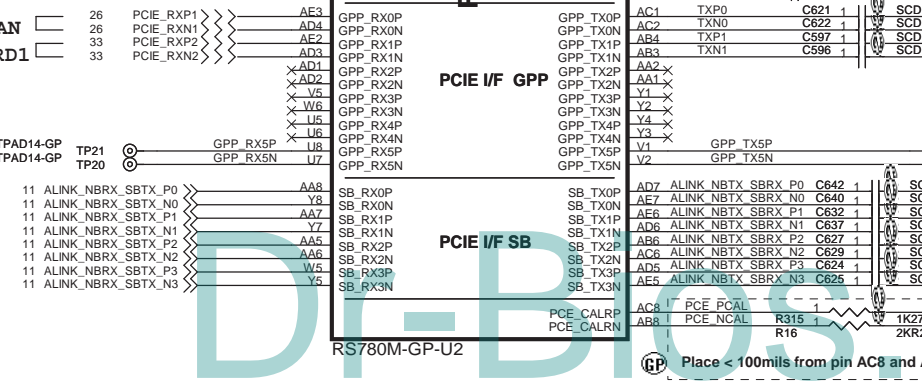
Placement: close RS780



**RS780M Display Port Support (muxed on GFX)**

DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1

GTXP0	LIMA	C30	1	SCD1U16V2KX-3GP	HDMI DATA2+	2
GTXP0	LIMA	C29	1	SCD1U16V2KX-3GP	HDMI DATA2-	2
GTXP1	LIMA	C27	1	SCD1U16V2KX-3GP	HDMI DATA1+	2
GTXP1	LIMA	C26	1	SCD1U16V2KX-3GP	HDMI DATA1-	2
GTXP2	LIMA	C25	1	SCD1U16V2KX-3GP	HDMI DATA0+	2
GTXP2	LIMA	C22	1	SCD1U16V2KX-3GP	HDMI DATA0-	2
GTXP3	LIMA	C21	1	SCD1U16V2KX-3GP	HDMI_CLK+	2
GTXN3	LIMA	C19	1	SCD1U16V2KX-3GP	HDMI_CLK-	2



**LAN**

**MINICARD1**

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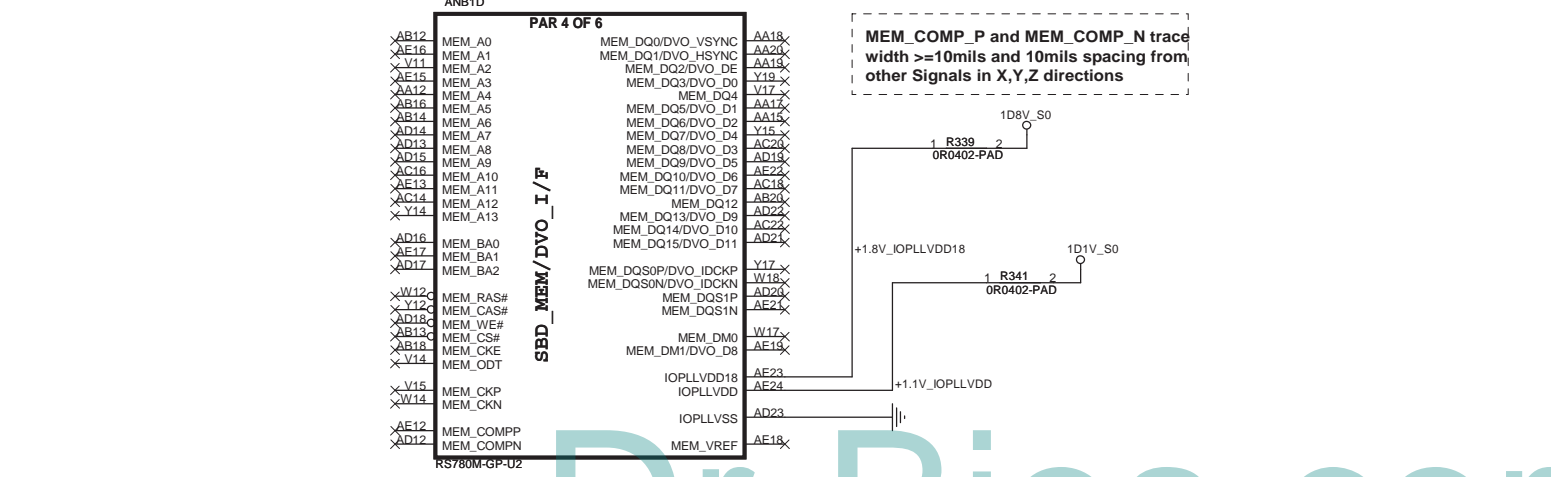
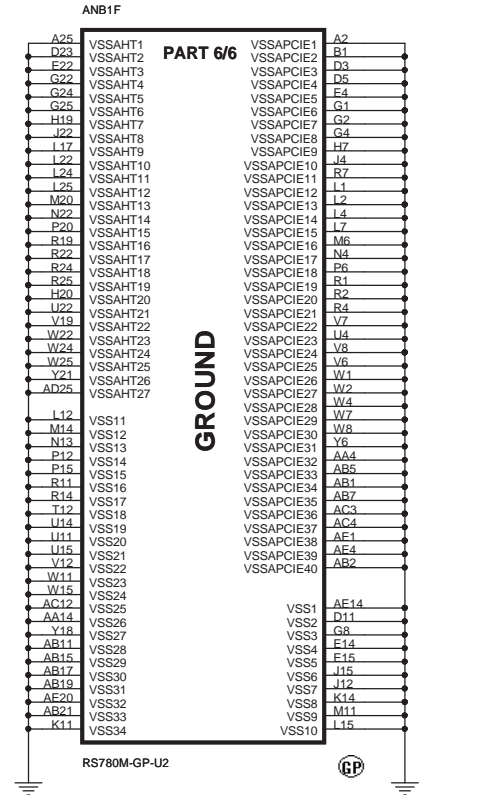
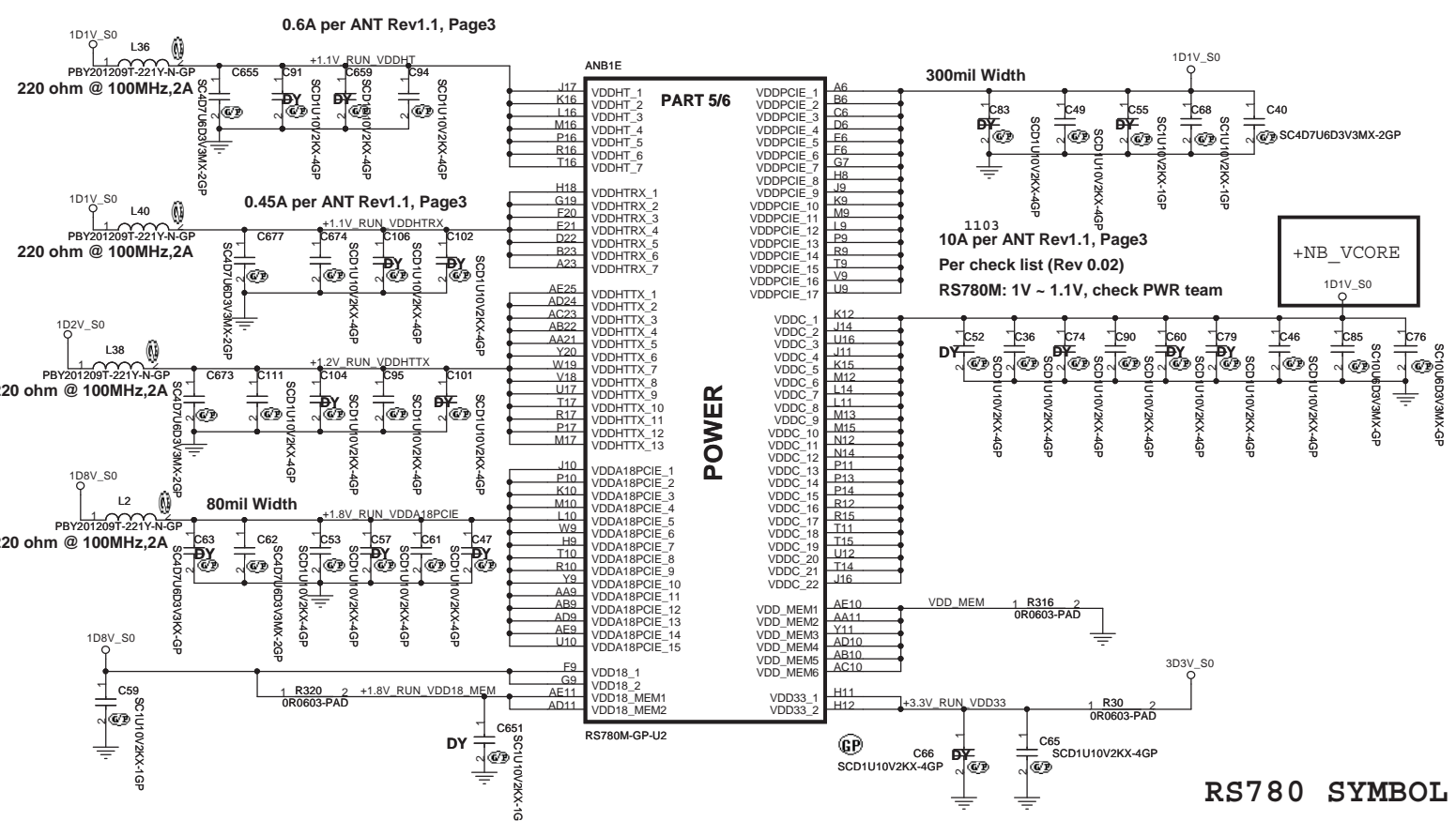
**ATI-RS880M\_HT LINK&PCIe(1/3)**

Size A3 Document Number **JV71-TR** Rev SA

Date: Monday, July 06, 2009 Sheet 8 of 61







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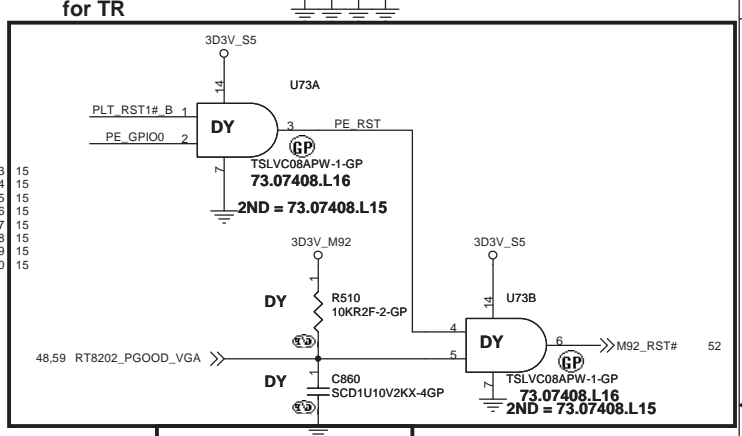
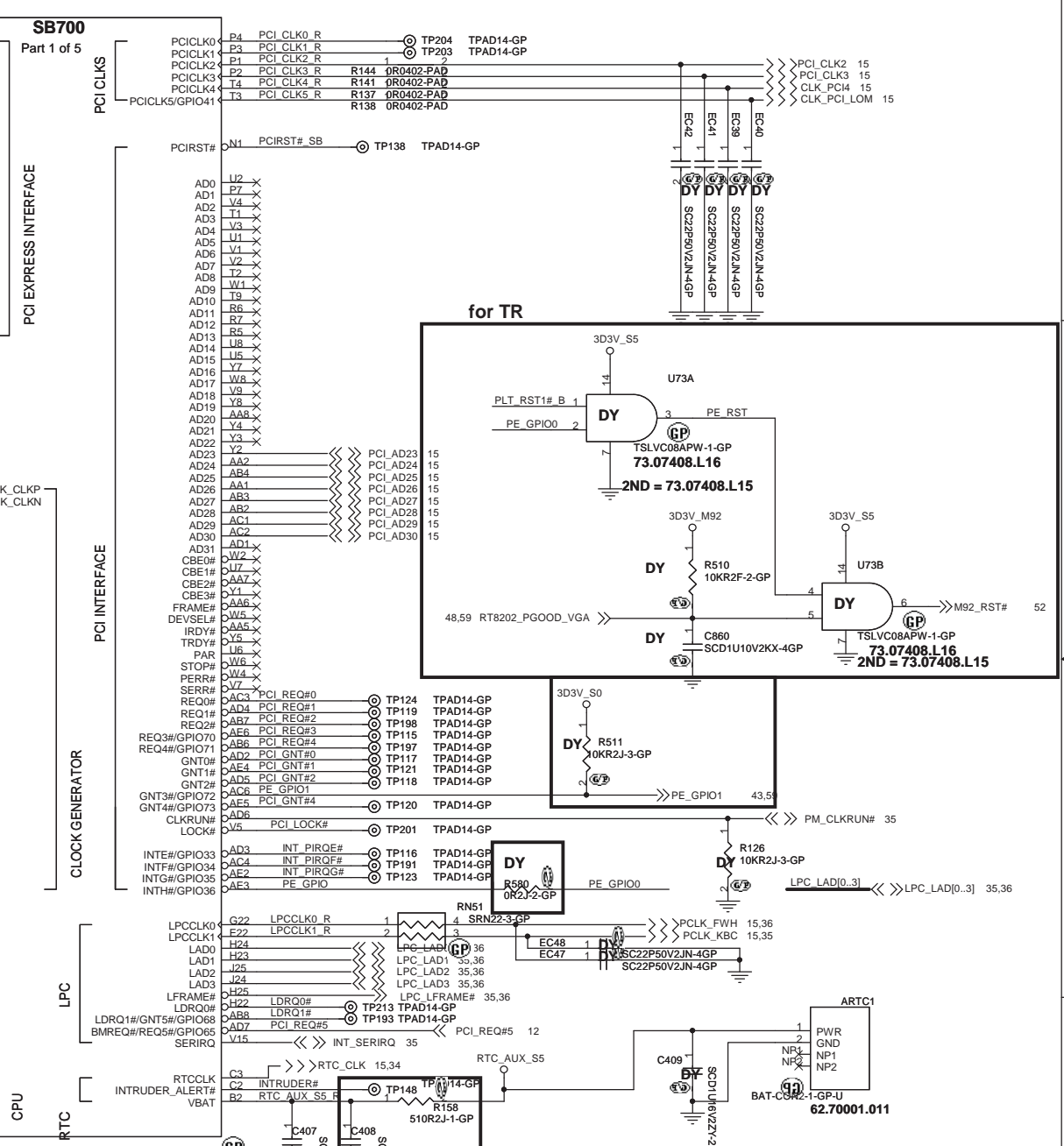
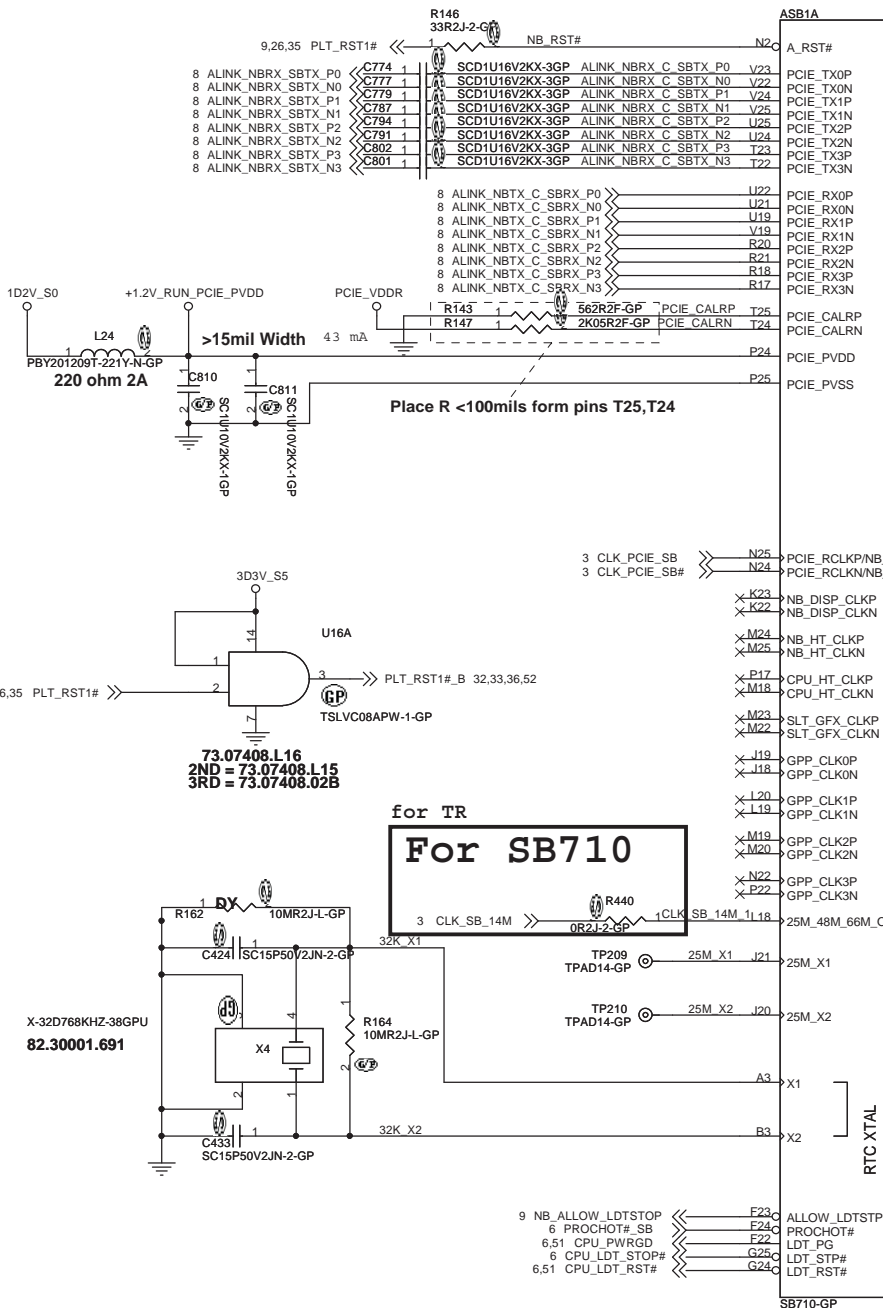
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**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

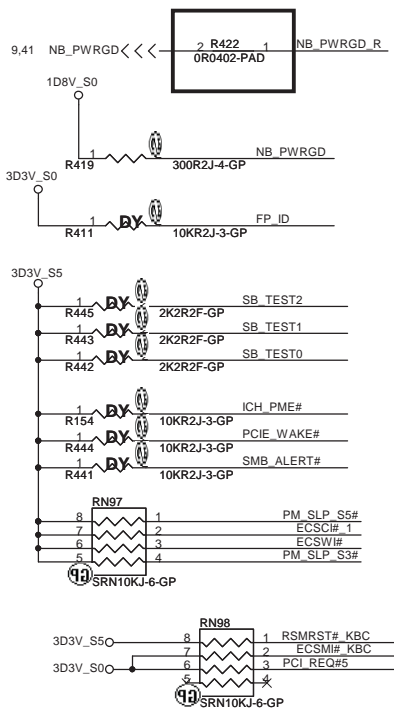
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Size: A3 Document Number: **JV71-TR** Rev: SA

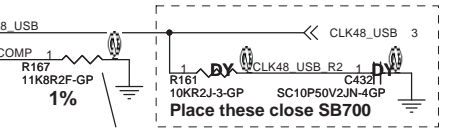
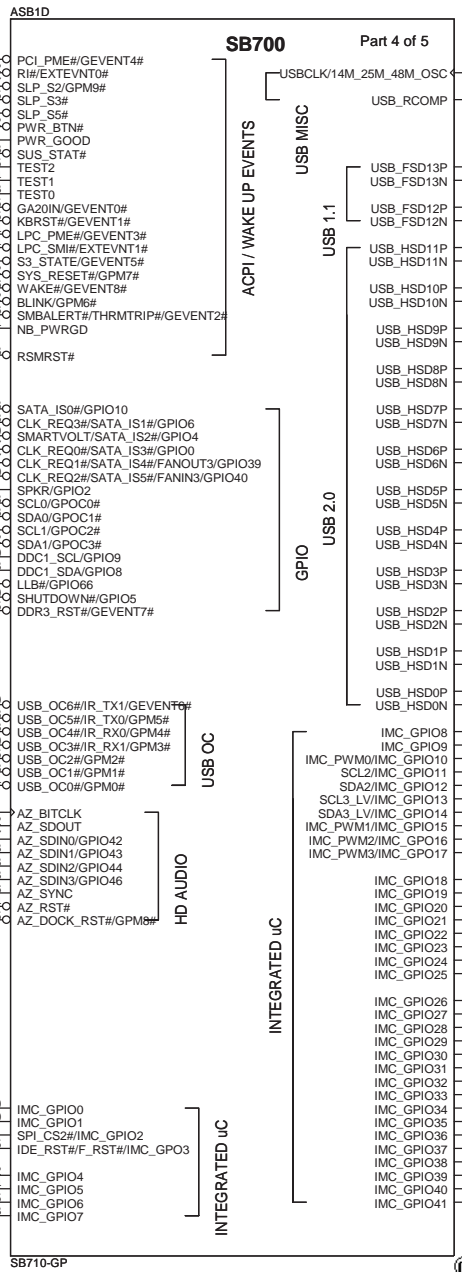
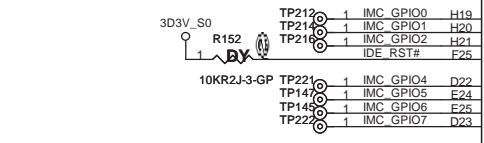
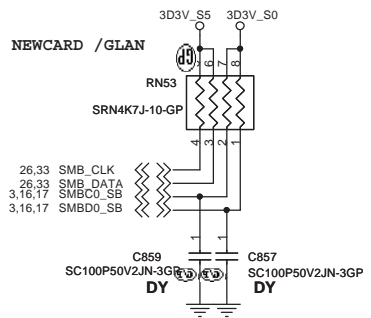
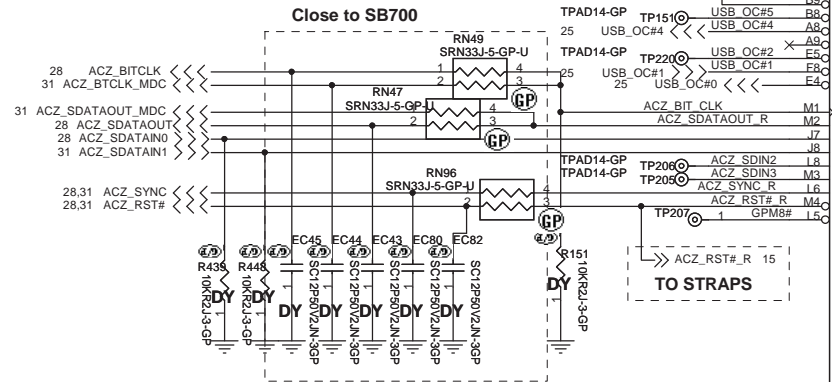
Date: Monday, July 06, 2009 Sheet 10 of 61



**Reserve for DY**  
EMI  
0408



**Close to SB700**



Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.

USB	
Pair	Device
11	CardReader
10	WEBCAM
9	NC
8	USB2
7	USBCN1
6	USB1
5	Bluetooth
4	NC
3	Fringier print
2	NC
1	MINIC1
0	USB3

OCP1#  
OCP0#

Strap Pin / define to use LPC or SPI ROM

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UMA

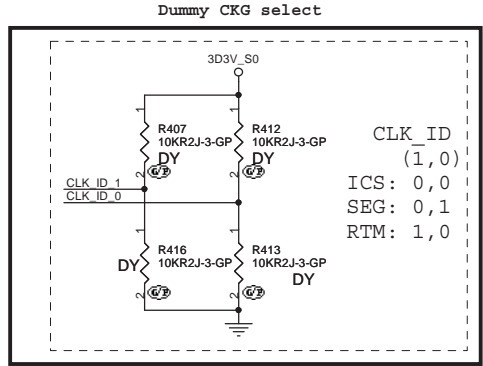
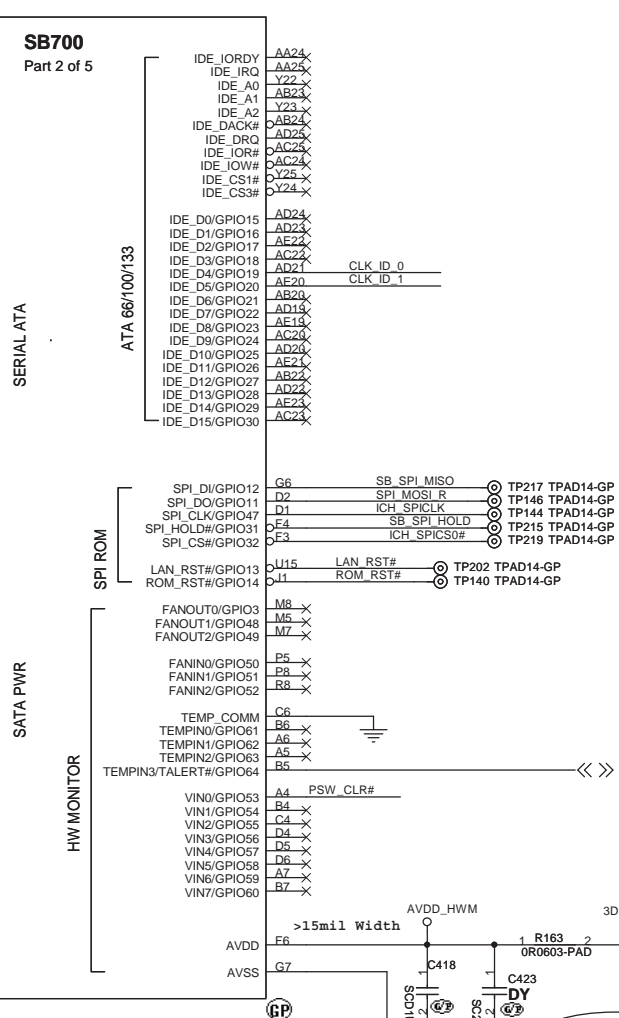
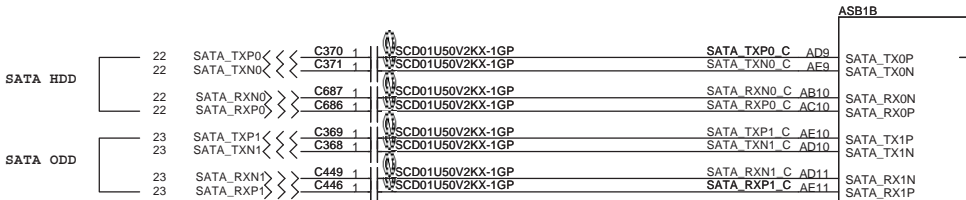
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

File: **ATI-SB710 USB&GPIO (2/5)**

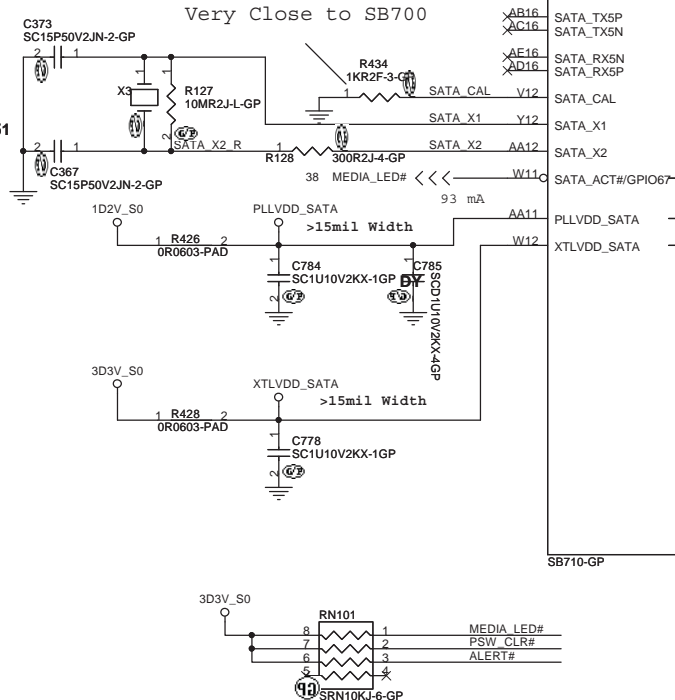
Size: A3 Document Number: **JV71-TR** Rev: SA

Date: Monday, July 06, 2009 Sheet 12 of 61

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700



2009/04/09 ALL DY



Layout connect to Cap then GND

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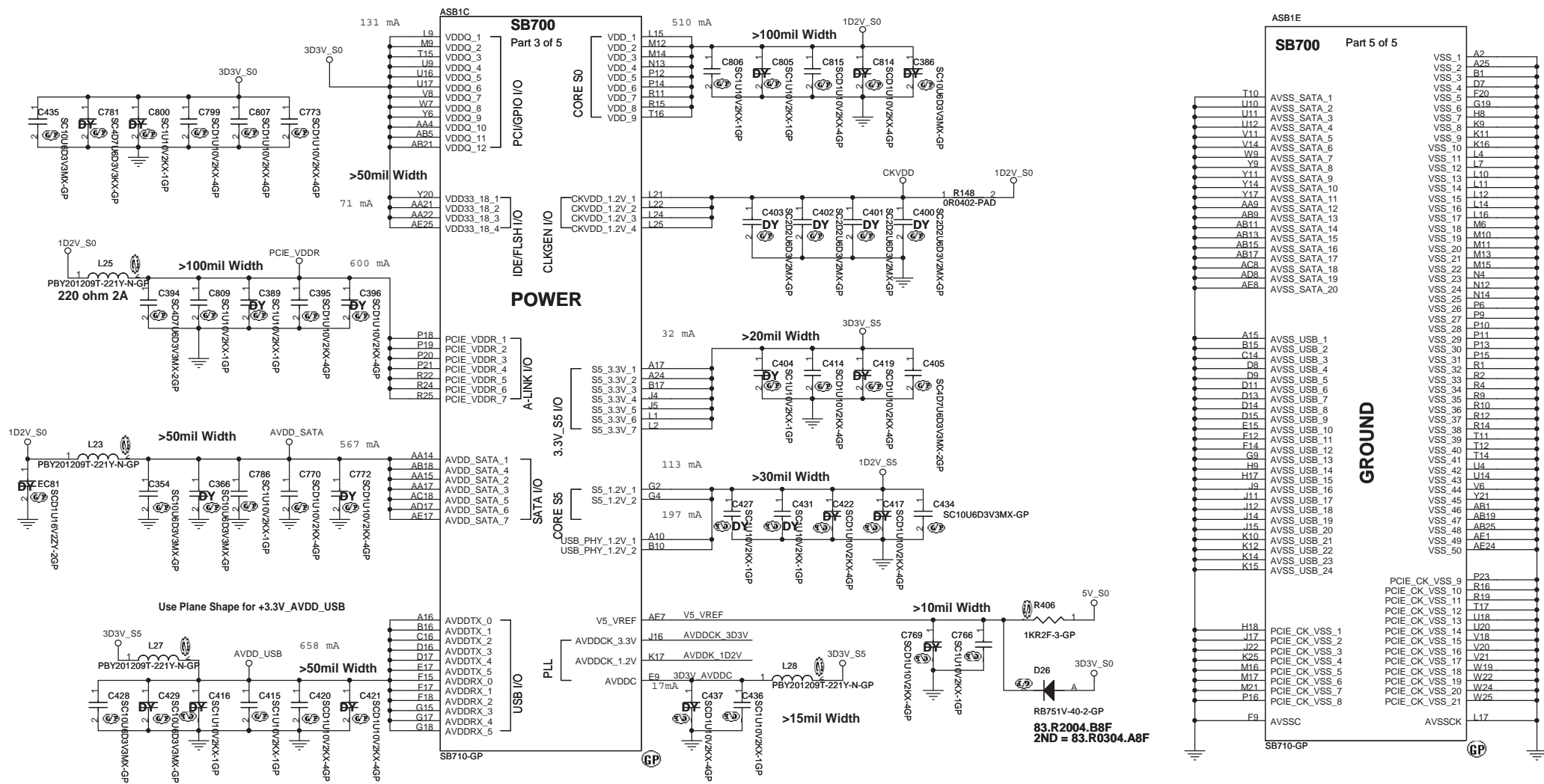
UMA

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-SB710 SATA-IDE (3/5)**

Size: A3 Document Number: **JV71-TR** Rev: **SB**

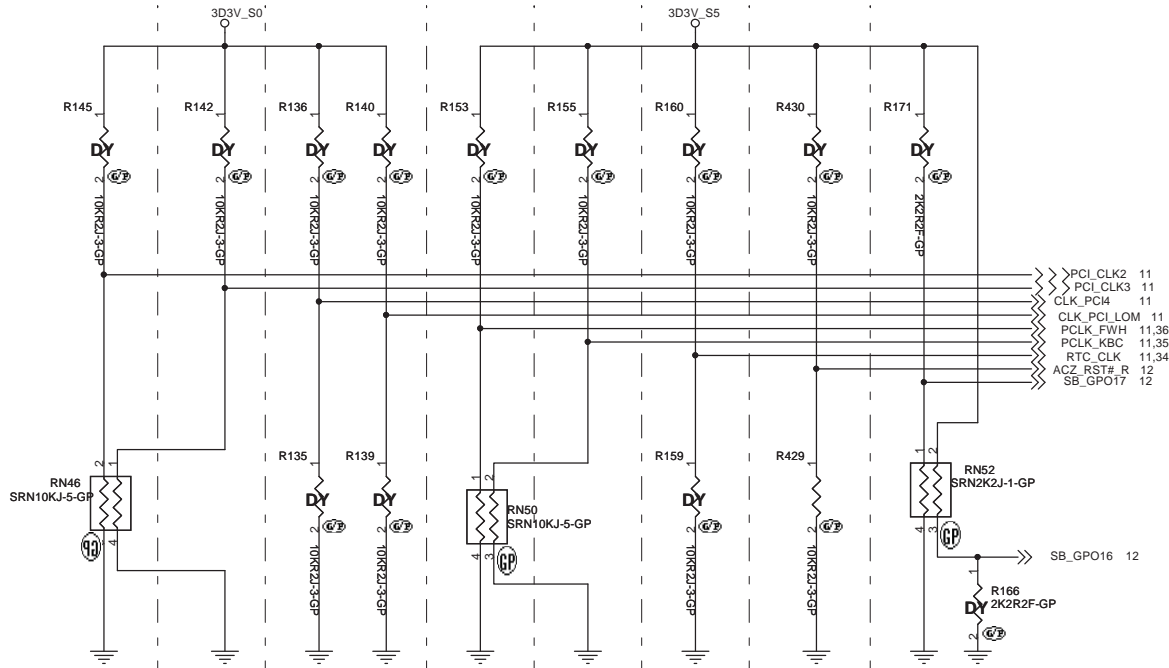
Date: Monday, July 06, 2009 Sheet 13 of 61



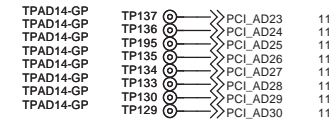
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
<b>ATI-SB710 POWER&amp;GND (4/5)</b>			
Title		Rev	
<b>JV71-TR</b>		<b>SB</b>	
Size	Document Number		
<b>A3</b>			
Date	Monday, July 06, 2009	Sheet	14 of 61

## REQUIRED STRAPS REQUIRED SYSTEM STRAPS



## DEBUG STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
<b>PULL HIGH</b>	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM
<b>PULL LOW</b>	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM DEFAULT L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

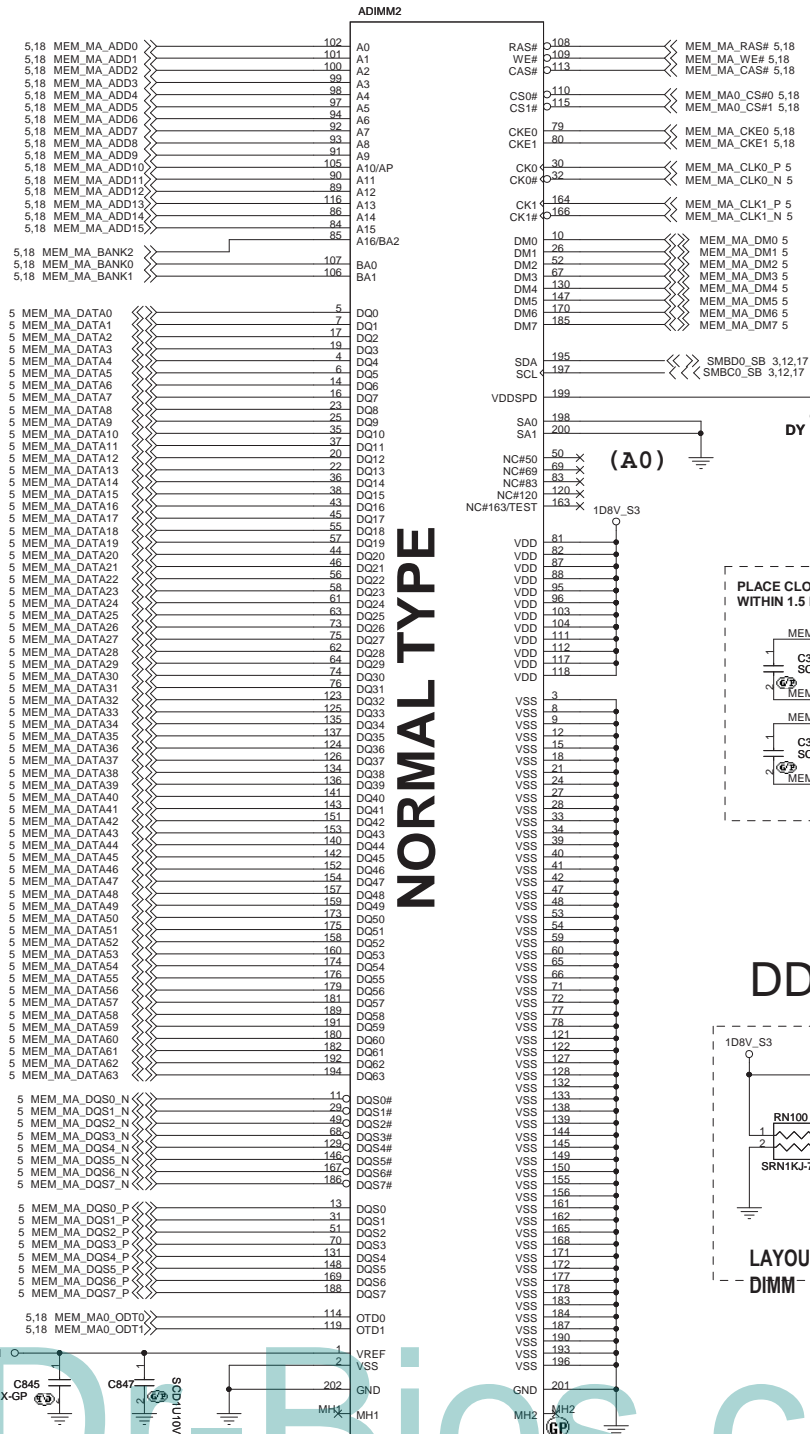
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
<b>PULL HIGH</b>	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI\_AD[30:23]

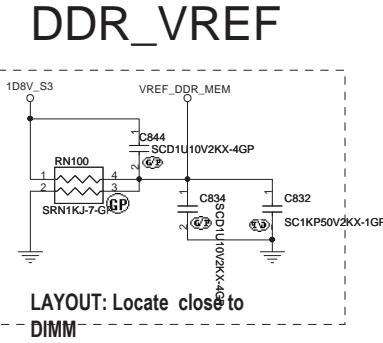
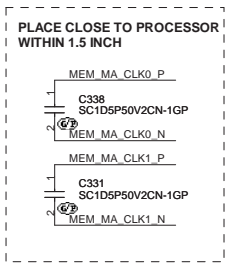
# Dr-Bios.com

UMA

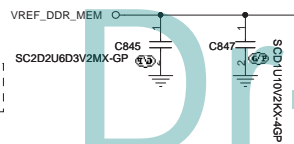
<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: <b>ATI-SB710 STRAPPING (5/5)</b>	
Size: <b>A3</b>	Document Number: <b>JV71-TR</b>
Date: <b>Monday, July 06, 2009</b>	Rev: <b>SA</b>
Sheet 15 of 61	



**NORMAL TYPE**



Place C2.2uF and 0.1uF < 500mils from DDR connector



SKT-SODIMM20020U4GP  
**62.10017.661**  
 2ND = 62.10017.A41  
 3RD = 62.10017.G81

LOW 5.2 mm

UMA

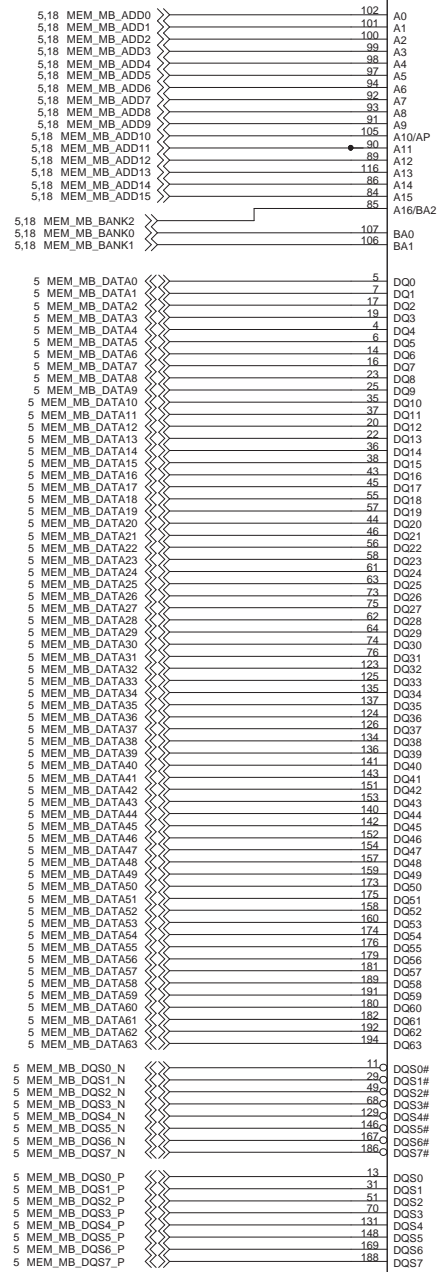
**緯創資通** Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR SO-DIMM SKT\_1**

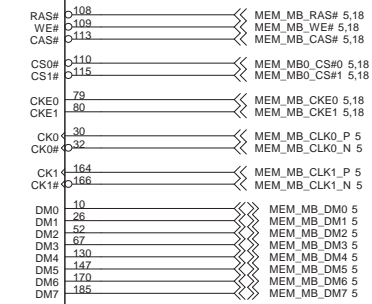
Size: Custom Document Number: **JV71-TR** Rev: **SB**

Date: Monday, July 06, 2009 Sheet 16 of 61

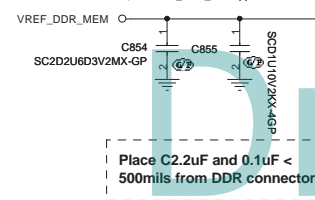
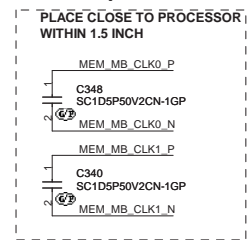




NORMAL TYPE



(A2)



SKT-SODIMM200-37GP  
 62-10017.E21  
 2ND = 62-10017.A51  
 3RD = 62-10017.G71

HI 9.2mm

UMA

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 21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

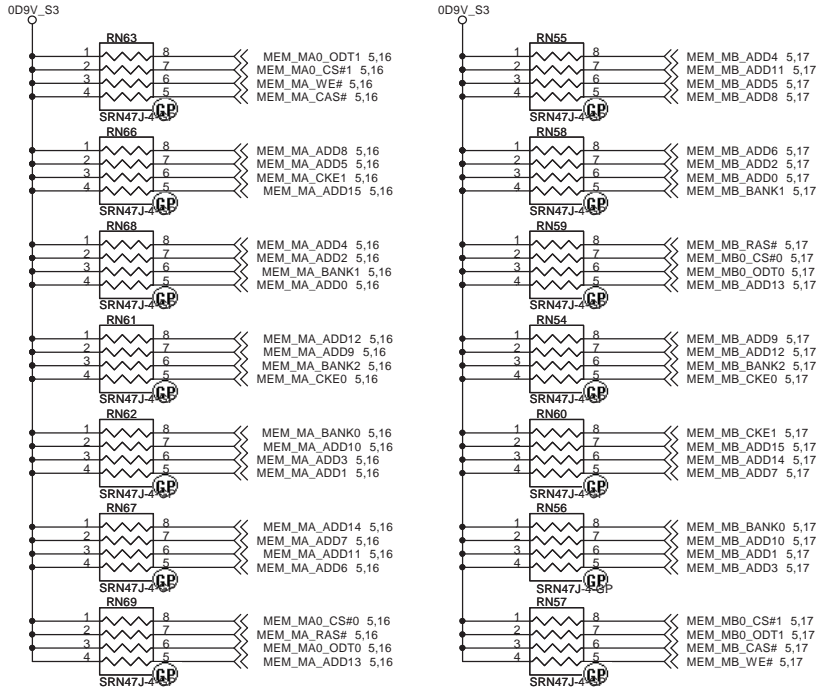
Title: **DDR SO-DIMM SKT 2**

Size: Custom Document Number: **JV71-TR** Rev: **SB**

Date: Monday, July 06, 2009 Sheet 17 of 61

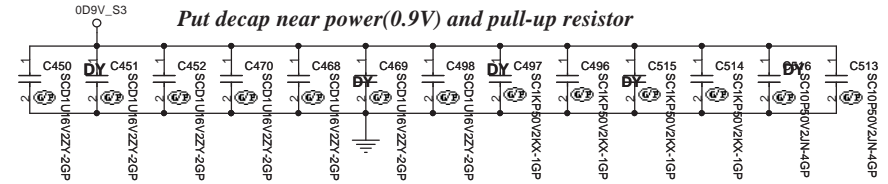
# PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

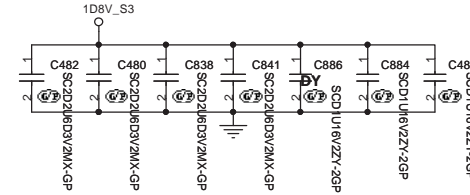


Do not share the Term resistor between the DDR address and Control Signals.

# Decoupling Capacitor

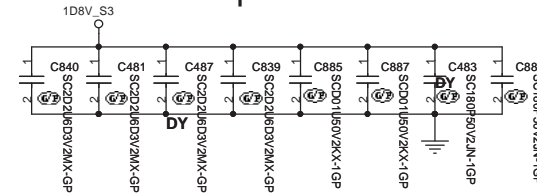


## Place these Caps near DM1



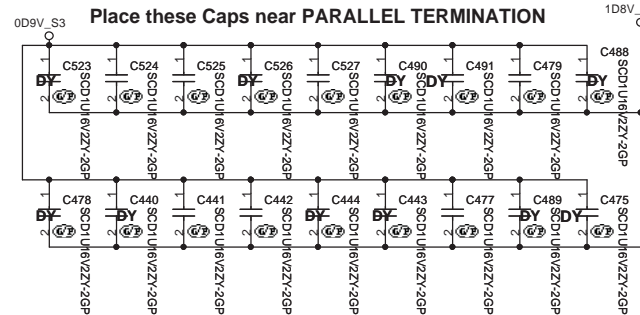
Layout Note:  
Place one cap close to every 2 pullup resistors terminated to 0D9V\_S3

## Place these Caps near DM2



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to 0D9V\_S3

## Place these Caps near PARALLEL TERMINATION



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UMA

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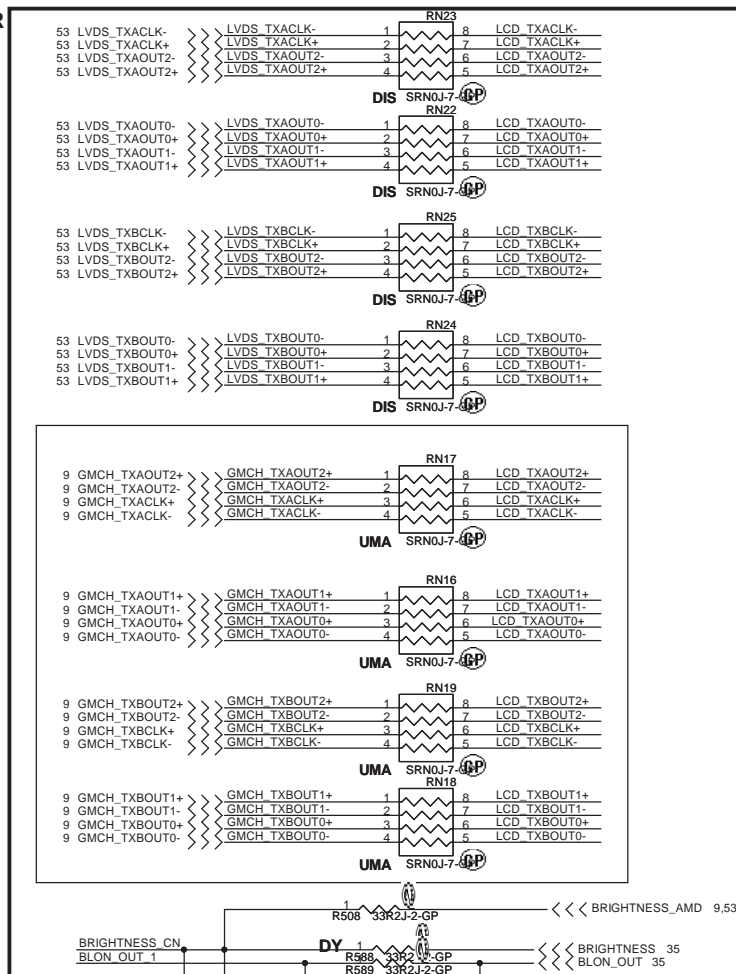
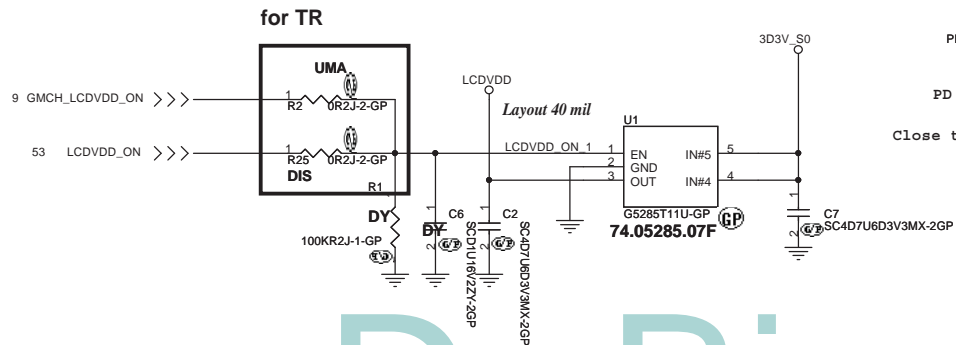
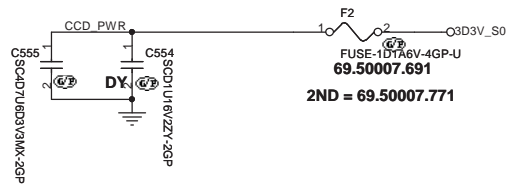
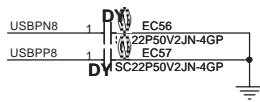
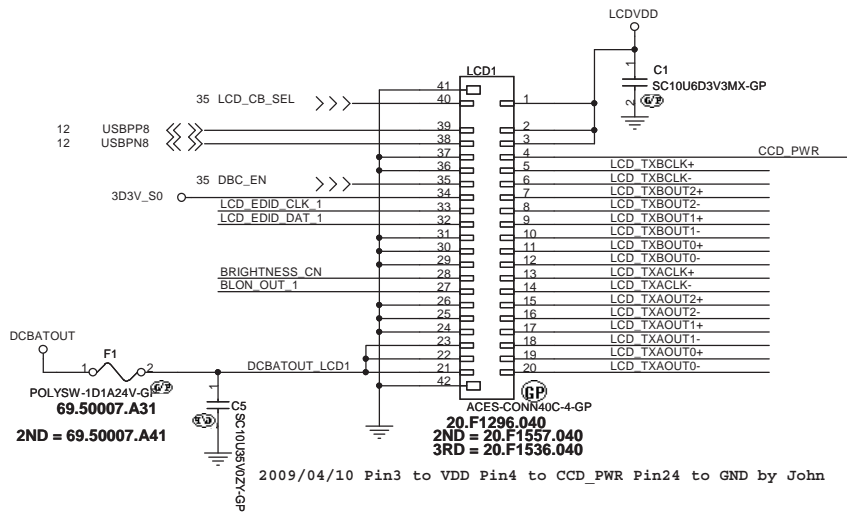
Title: **DDR DAMPING & TERMINATION**

Size A3 Document Number **JV71-TR** Rev **SB**

Date: Monday, July 06, 2009 Sheet 18 of 61

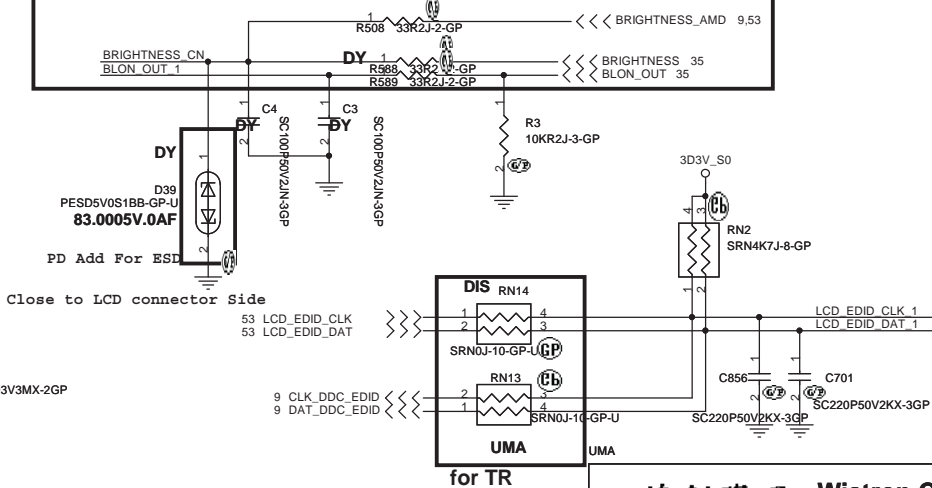
# LCD/INVERTER/CCD CONN

for TR



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

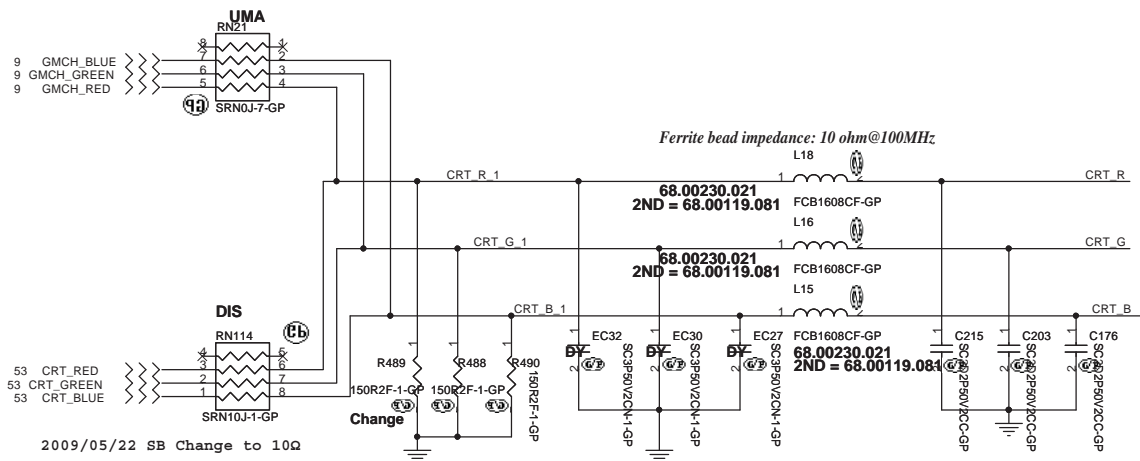
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



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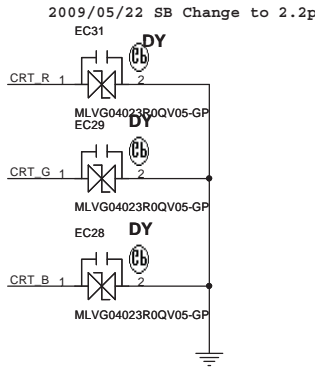
緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title <b>LCD CONN</b>		
Size A3	Document Number <b>JV71-TR</b>	Rev <b>-1</b>
Date Monday, July 06, 2009	Sheet 19	of 61



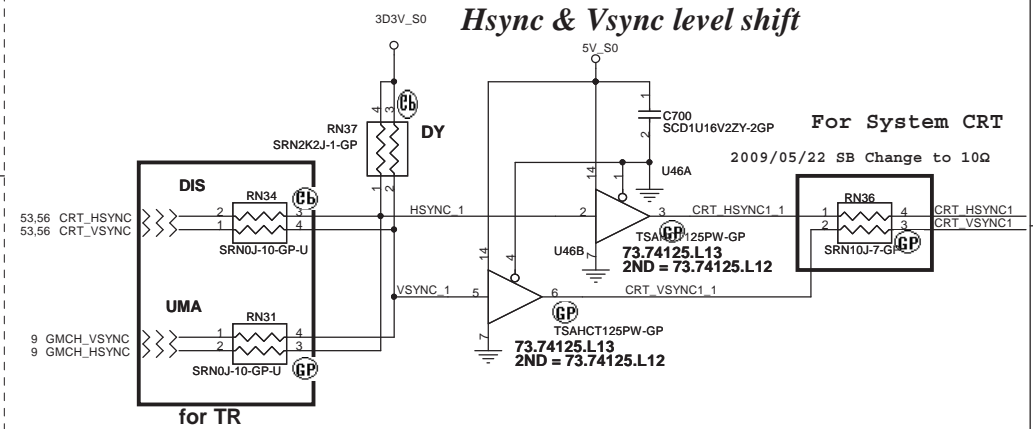
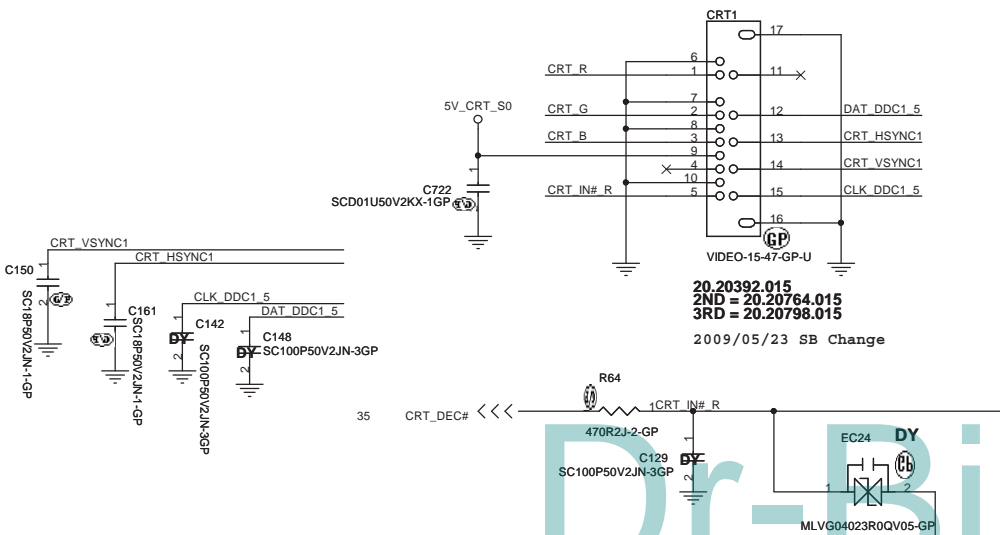
R489 PU & TR-DIS-->150R  
TR-UMA & TR-MUX-->140R

Layout Note:  
Place these resistors  
close to the CRT-out  
connector

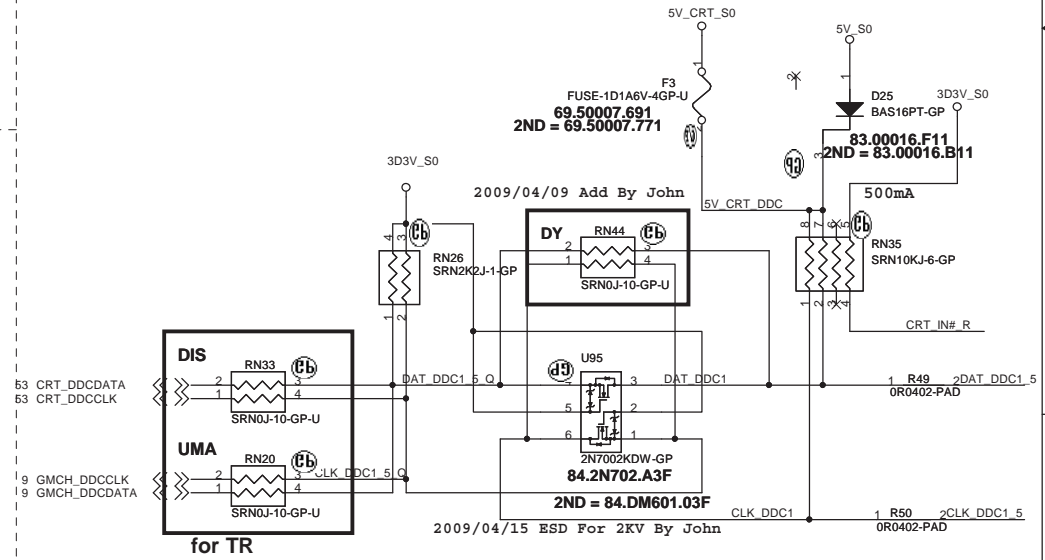


Layout Note:  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

## CRT I/F & CONNECTOR



## DDC\_CLK & DATA level shift



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

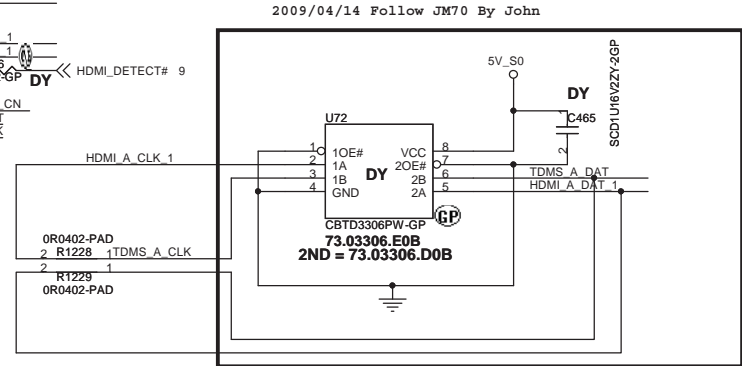
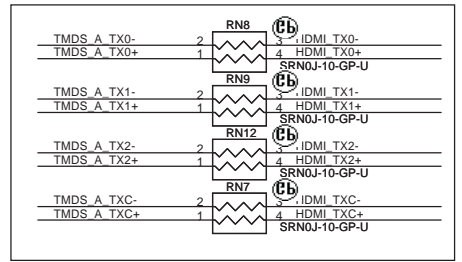
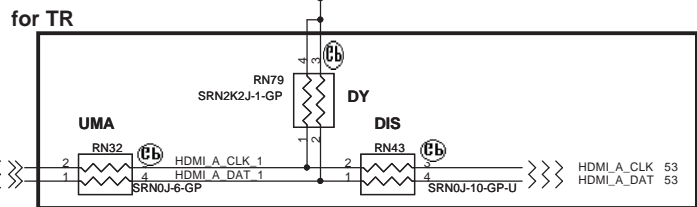
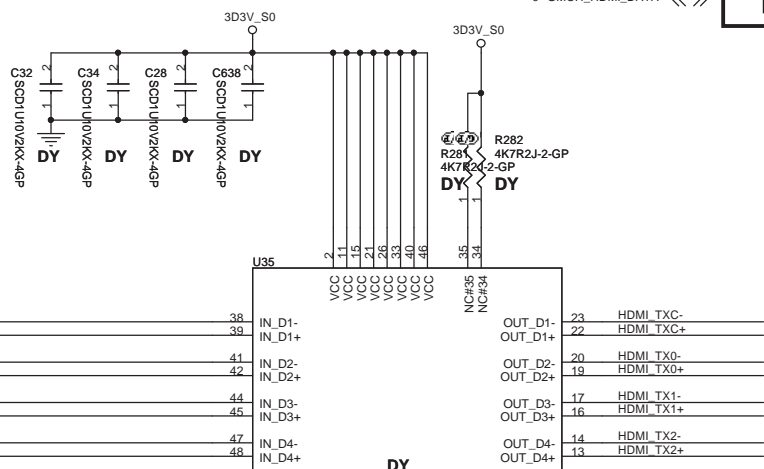
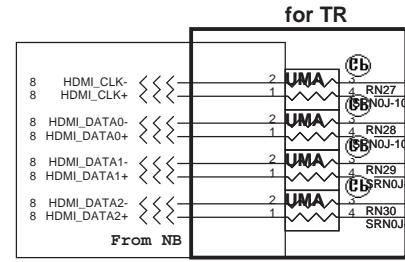
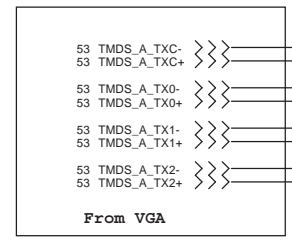
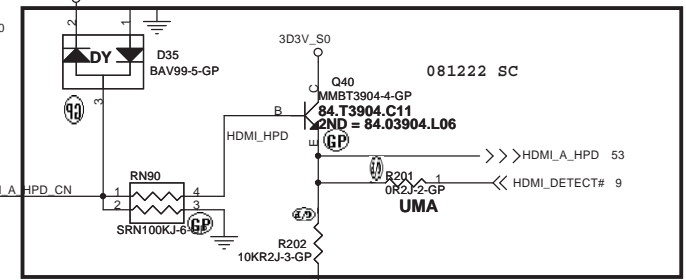
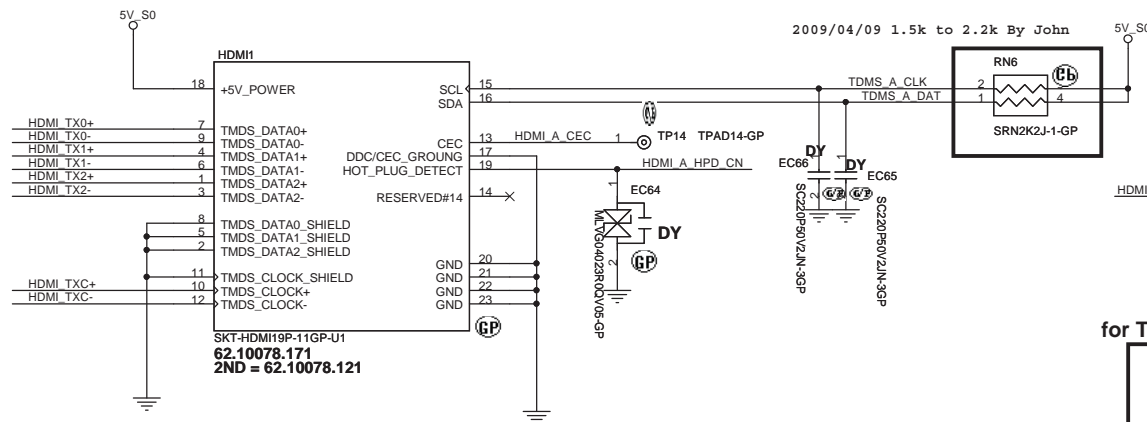
Title  
**CRT Connector**

Size Document Number  
**JV71-TR**

Date: Monday, July 06, 2009 Sheet 20 of 61

Rev  
**SB**





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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Connector

Size: Document Number

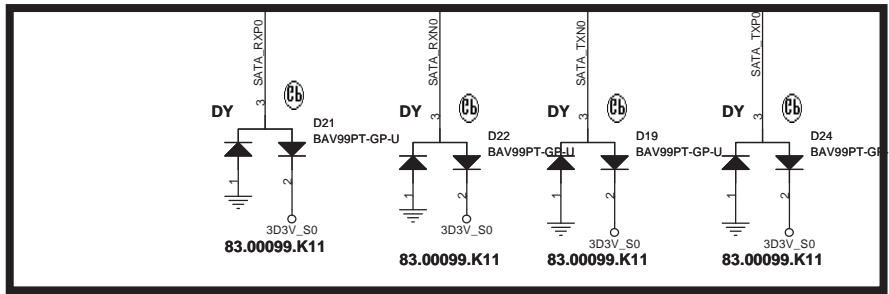
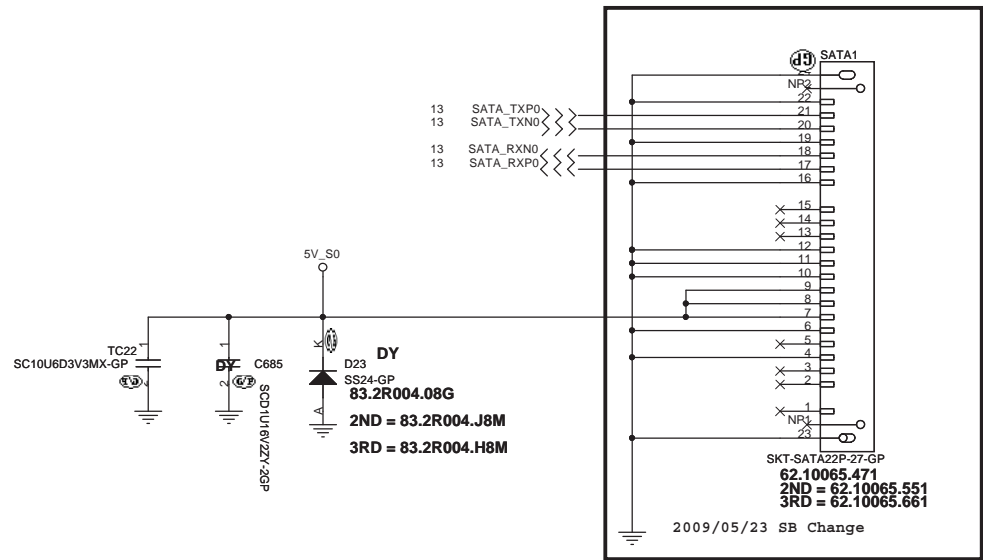
Date: Monday, July 06, 2009

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Rev: SB

JV71-TR

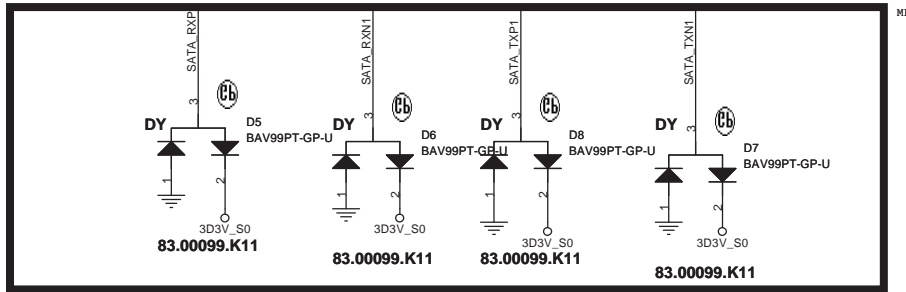
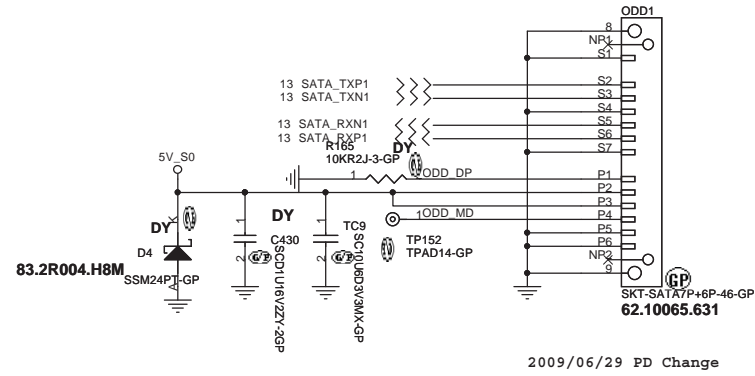
# SATA Connector



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UMA		<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		HDD	
Size	Document Number	Rev	
	JV71-TR	SB	
Date: Monday, July 06, 2009	Sheet 22	of 61	

# SATA ODD Connector



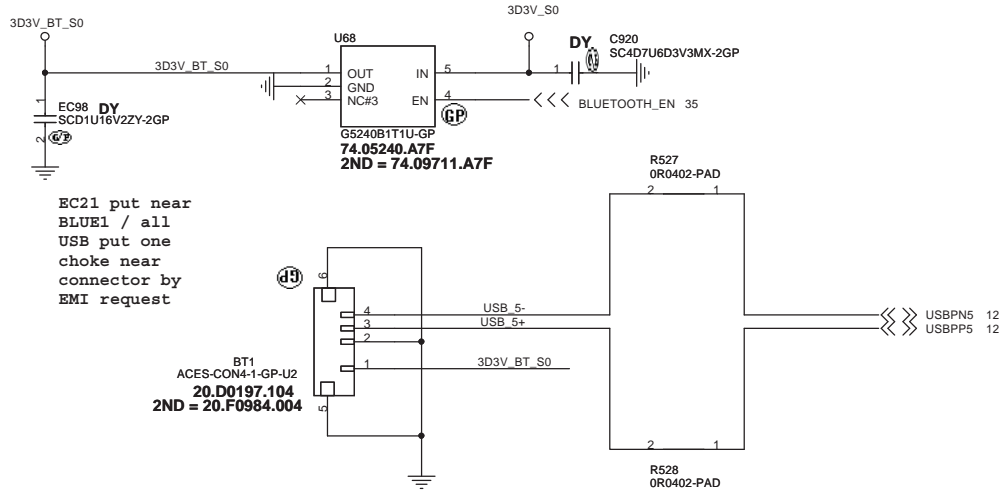
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UMA

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>ODD</b>	
Size	Document Number <b>JV71-TR</b>
Date: Monday, July 06, 2009	Rev <b>SB</b>
Sheet 23 of 61	

# BLUETOOTH MODULE

1.5A / High Active Voltage 2V

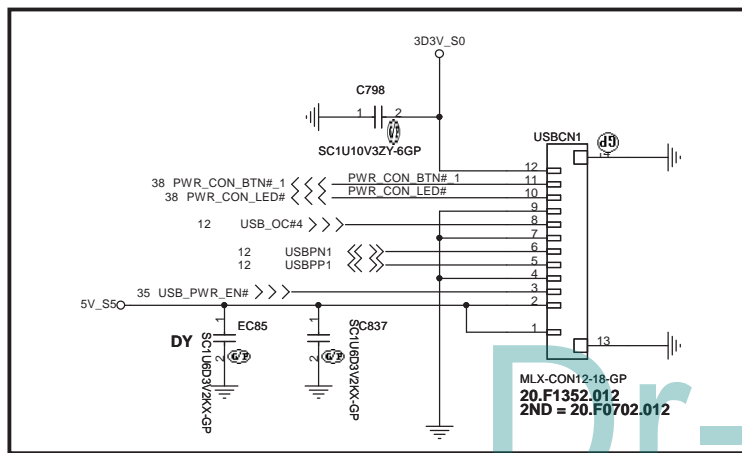
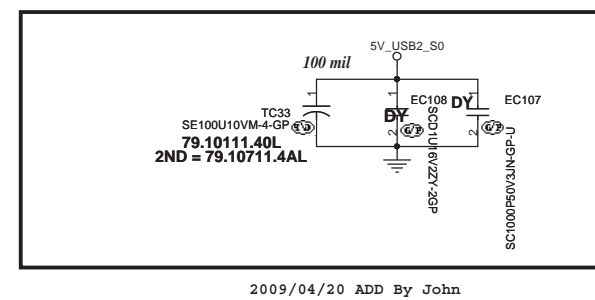
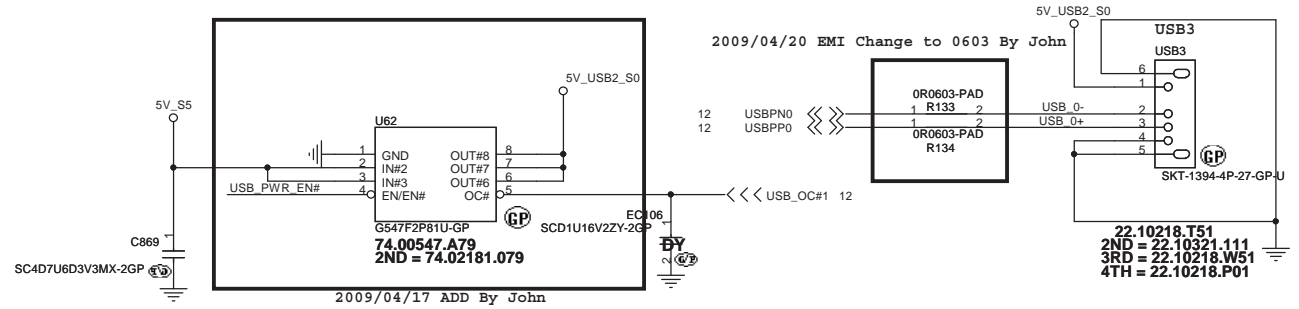
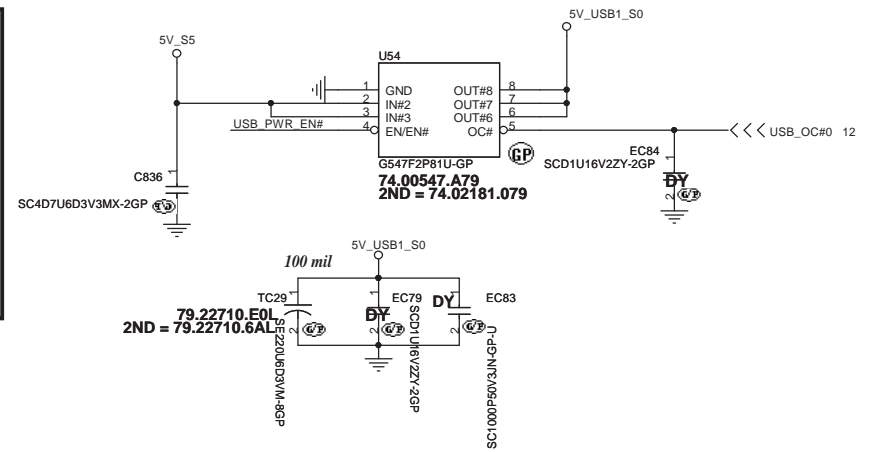
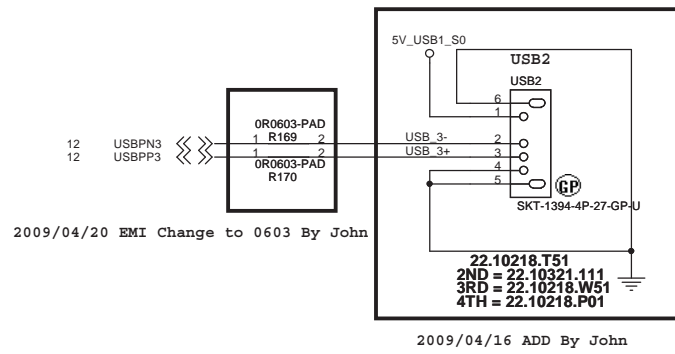
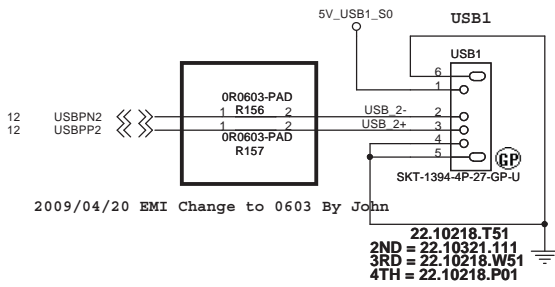


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UMA

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>BLUETOOTH</b>			
Size	Document Number		Rev
	<b>JV71-TR</b>		<b>SA</b>
Date: Monday, July 06, 2009	Sheet	24 of	61





- USB\_OC#4 1 173 AFTE14P-GP
- USBPN1 1 174 AFTE14P-GP
- USBPP1 1 176 AFTE14P-GP
- USB\_PWR\_EN# 1 178 AFTE14P-GP
- 5V\_S5 1 179 AFTE14P-GP

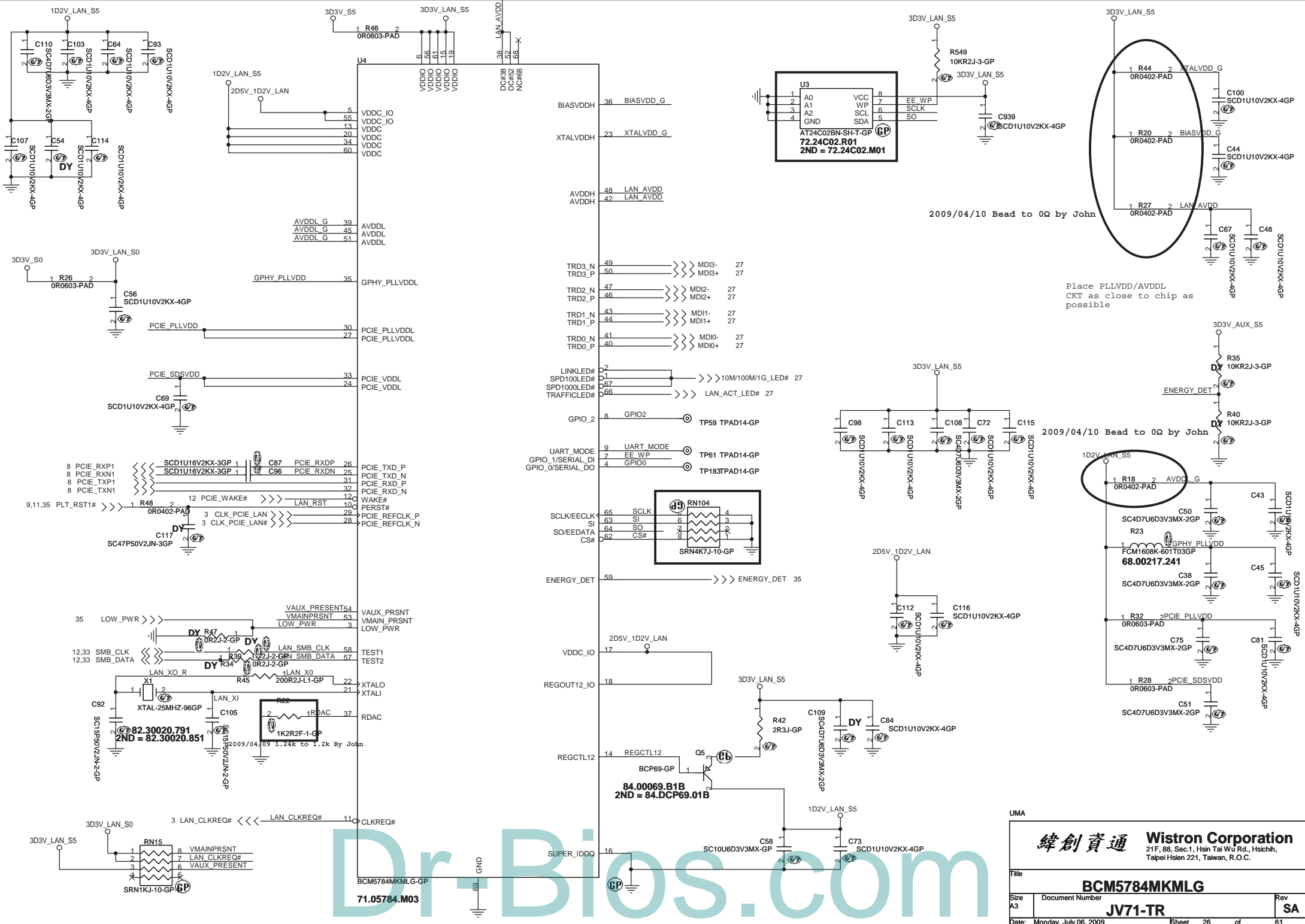
UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB**

Size: Document Number **JV71-TR** Rev: **SA**

Date: Monday, July 06, 2009 Sheet 25 of 61



2009/04/10 Bead to 0Ω by John

Place PLLVDD/AVDDL CKT as close to chip as possible

2009/04/10 Bead to 0Ω by John

2009/04/09 1.24K to 1.2k By John

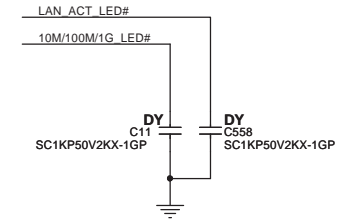
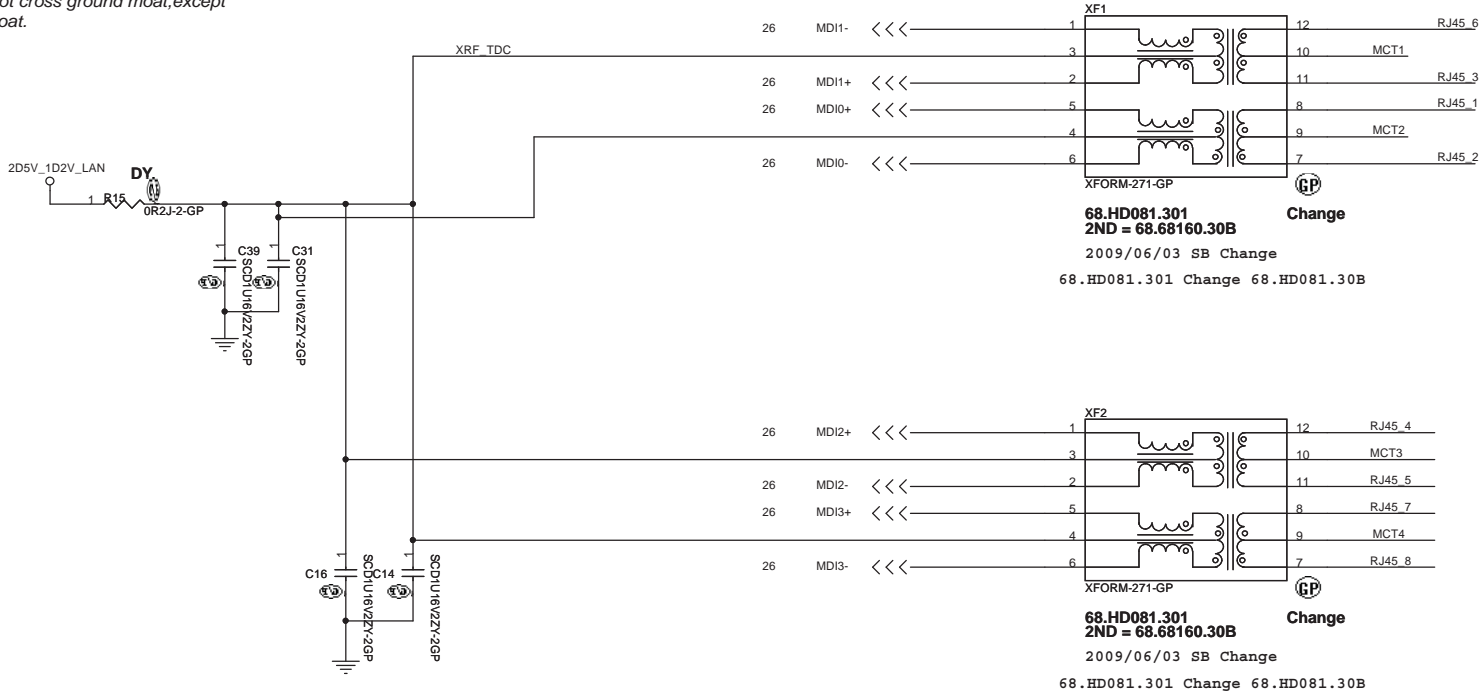
Dr-Bios.com

<p><b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.</p>		
<p>Title: <b>BCM5784MKMLG</b></p>		
Size A3	Document Number	Rev SA
<p><b>JV71-TR</b></p>		Sheet 26 of 61
Date: Monday, July 06, 2009		

# LAN Connector

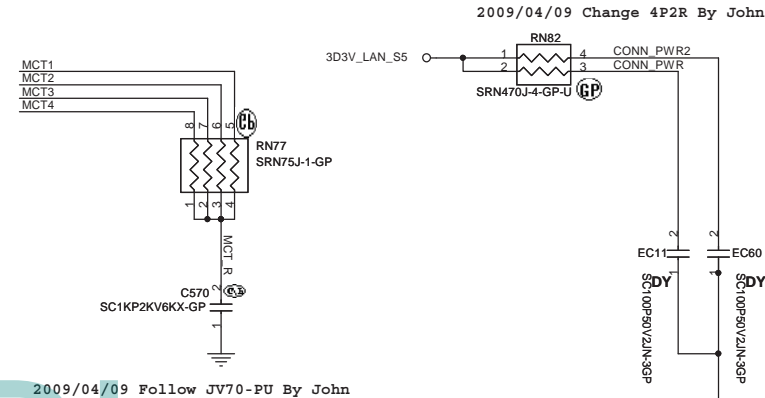
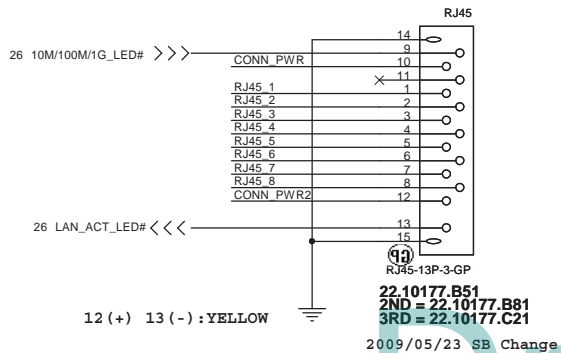
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

## GIGA Lan Transformer



10 (+) 9 (-) : GREEN  
 10 (+) 11 (-) : ORANGE

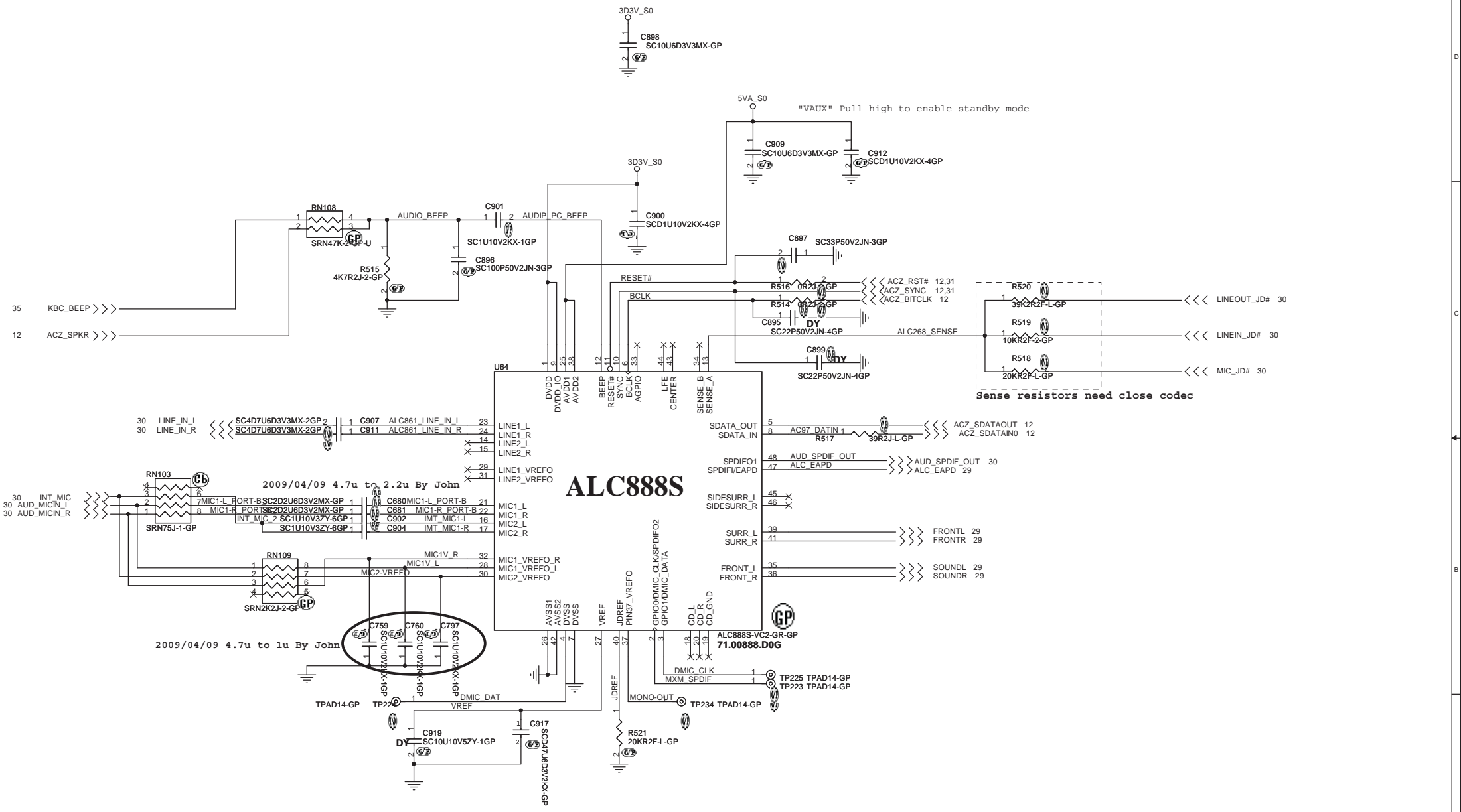
# LAN Connector



DOC\_TIP,DOC\_RING,TIP,RING:  
 W/S : 10/100 @ Surface layers  
 10/20 @ Inner layers

UMA	
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Title	
<b>LAN CONN</b>	
Size	Document Number
A3	<b>JV71-TR</b>
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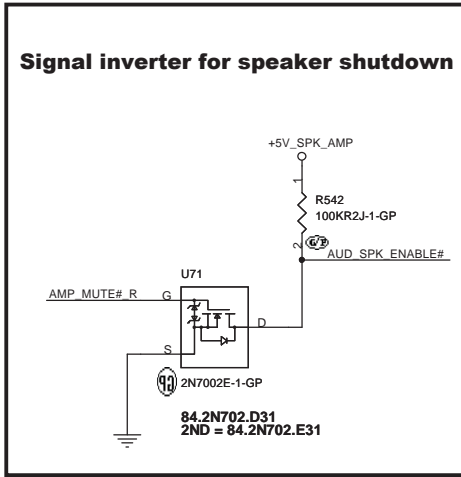
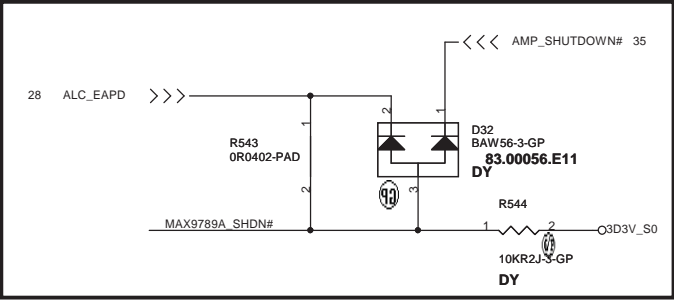
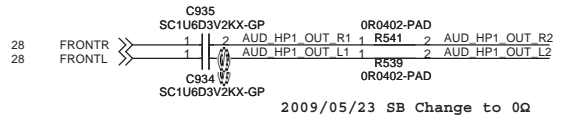
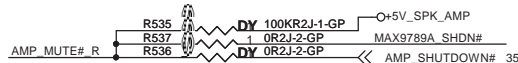
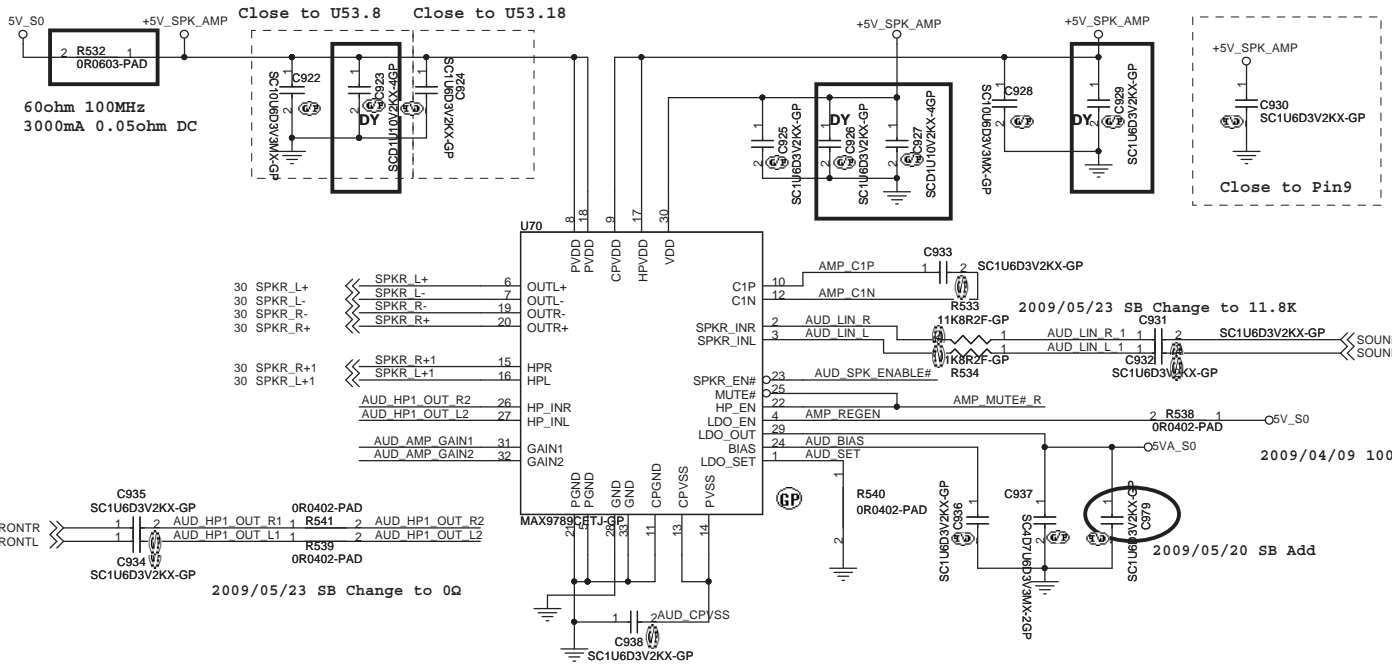
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title Azalia codec ALC888</b>	
Size A3	Document Number <b>JV71-TR</b>
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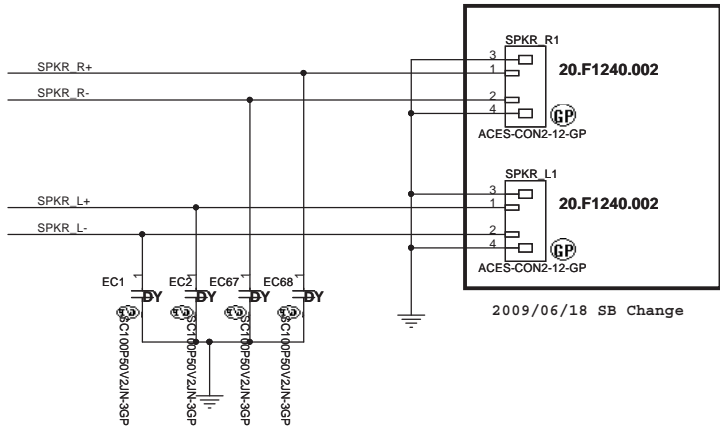
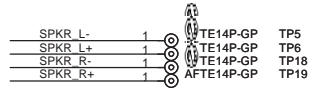
### GAIN SETTING

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

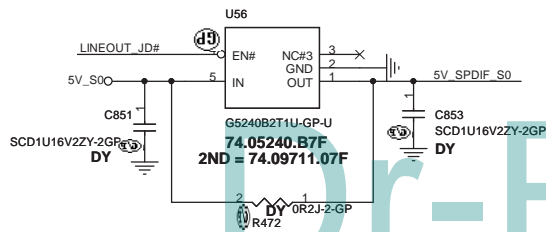
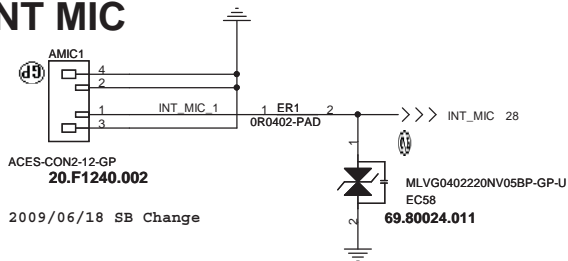
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# Internal Speaker

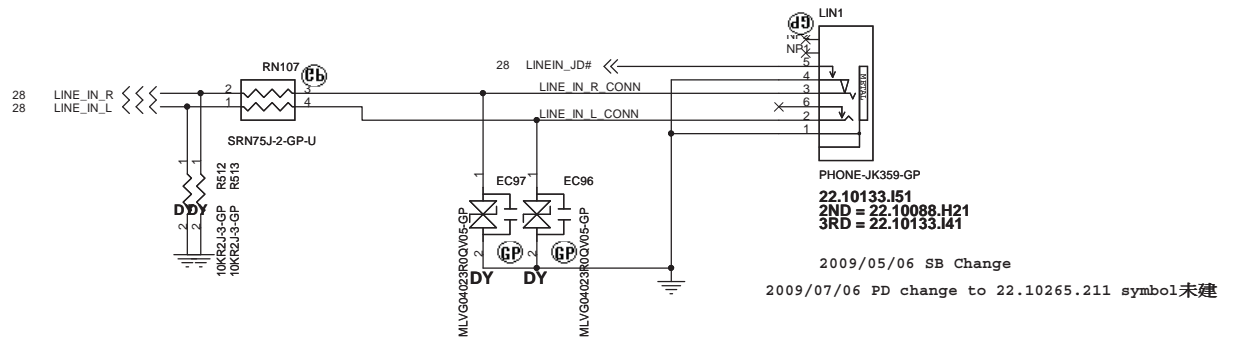
29 SPKR\_L- <<<<< SPKR\_L-  
 29 SPKR\_L+ <<<<< SPKR\_L+  
 29 SPKR\_R- <<<<< SPKR\_R-  
 29 SPKR\_R+ <<<<< SPKR\_R+



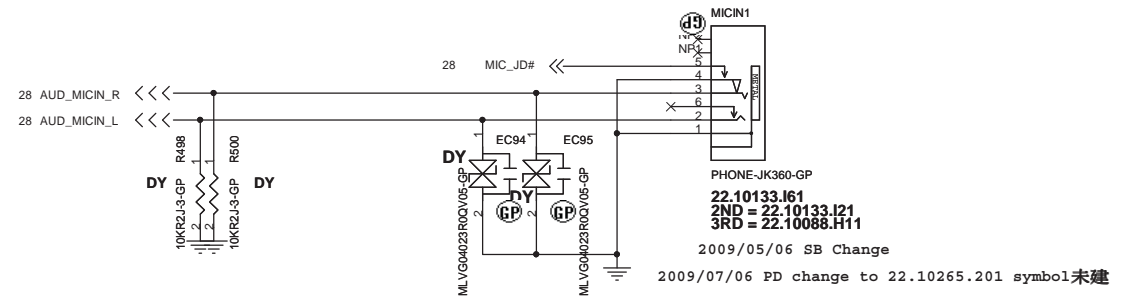
# INT MIC



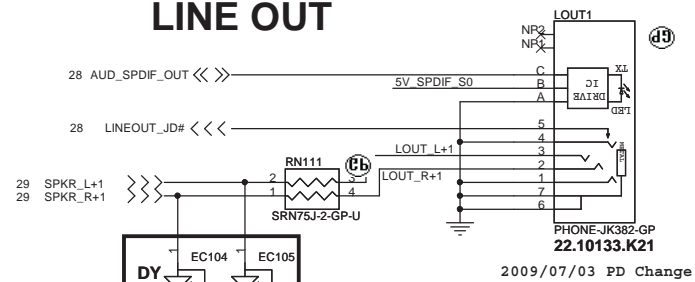
# LINE IN



# MIC IN



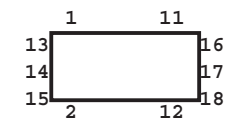
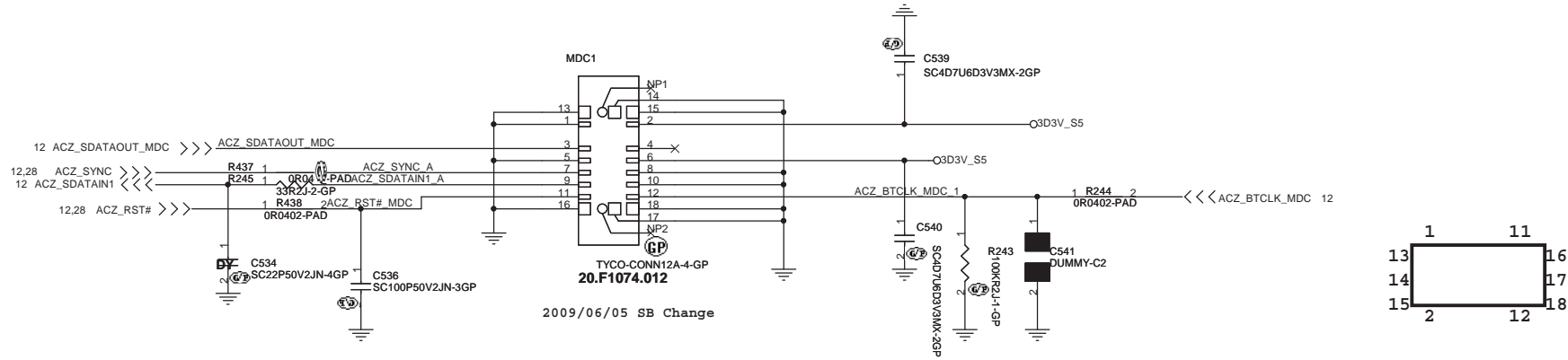
# LINE OUT



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<b>AUDIO JACK</b>	
<b>JV71-TR</b>	
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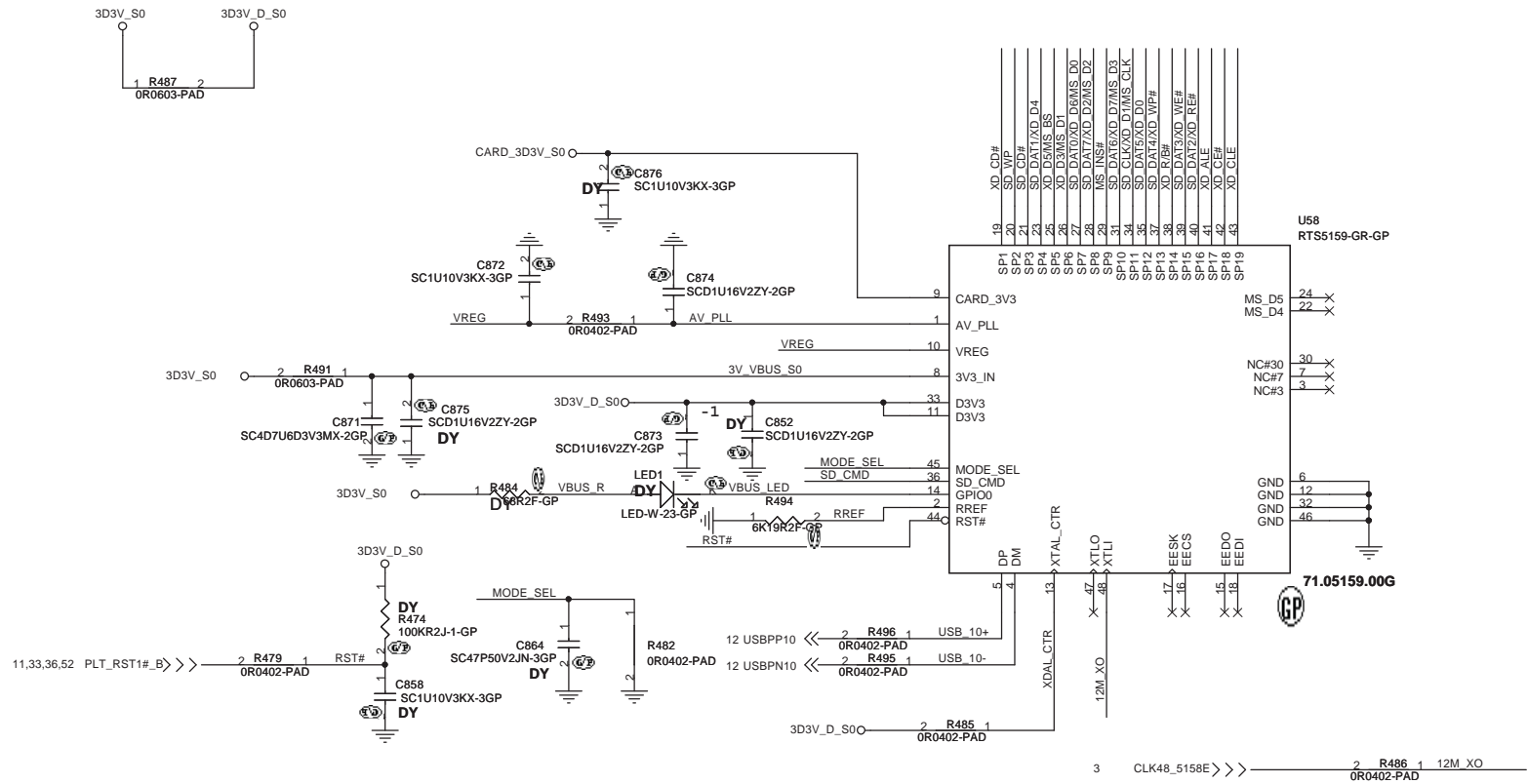
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# MDC 1.5 CONN

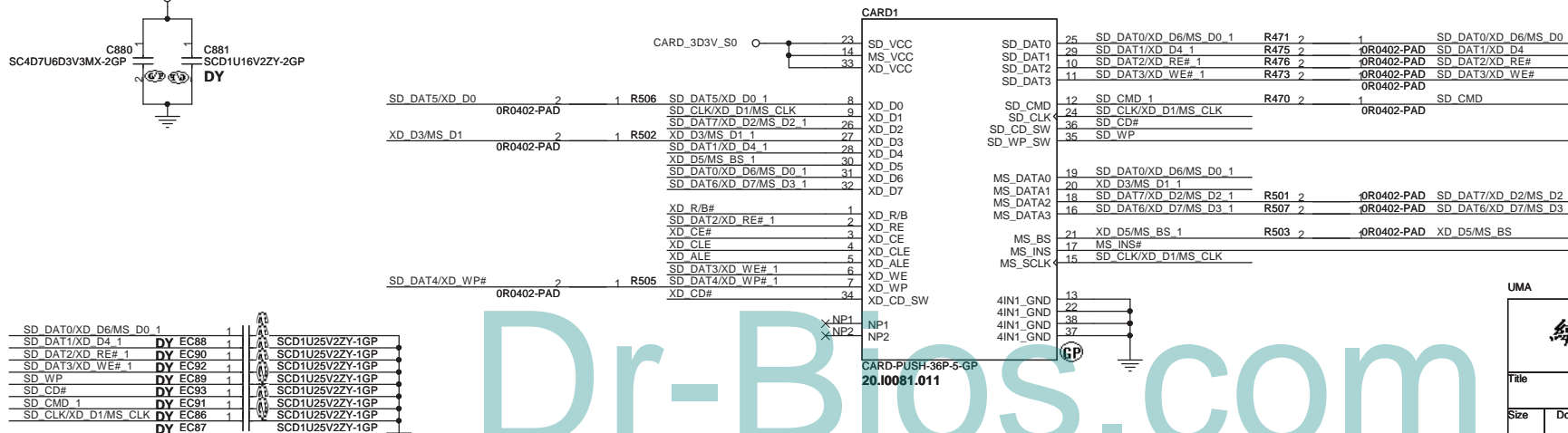
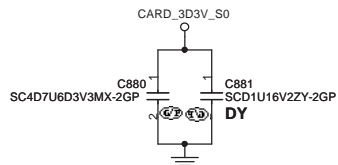


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Title		<b>MDC</b>	
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### 5 IN 1 CARD-READER (SD/MMC/MS/MS PRO/XD)



SD DAT0/XD D6/MS D0 1	1		
SD DAT1/XD D4 1	DY EC88	1	SCD1U25V2ZY-1GP
SD DAT2/XD RE# 1	DY EC90	1	SCD1U25V2ZY-1GP
SD DAT3/XD WE# 1	DY EC92	1	SCD1U25V2ZY-1GP
SD WP	DY EC89	1	SCD1U25V2ZY-1GP
SD CD#	DY EC93	1	SCD1U25V2ZY-1GP
SD CMD 1	DY EC91	1	SCD1U25V2ZY-1GP
SD CLK/XD D1/MS CLK	DY EC86	1	SCD1U25V2ZY-1GP
	DY EC87	1	SCD1U25V2ZY-1GP

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Taipei Hsien 221, Taiwan, R.O.C.

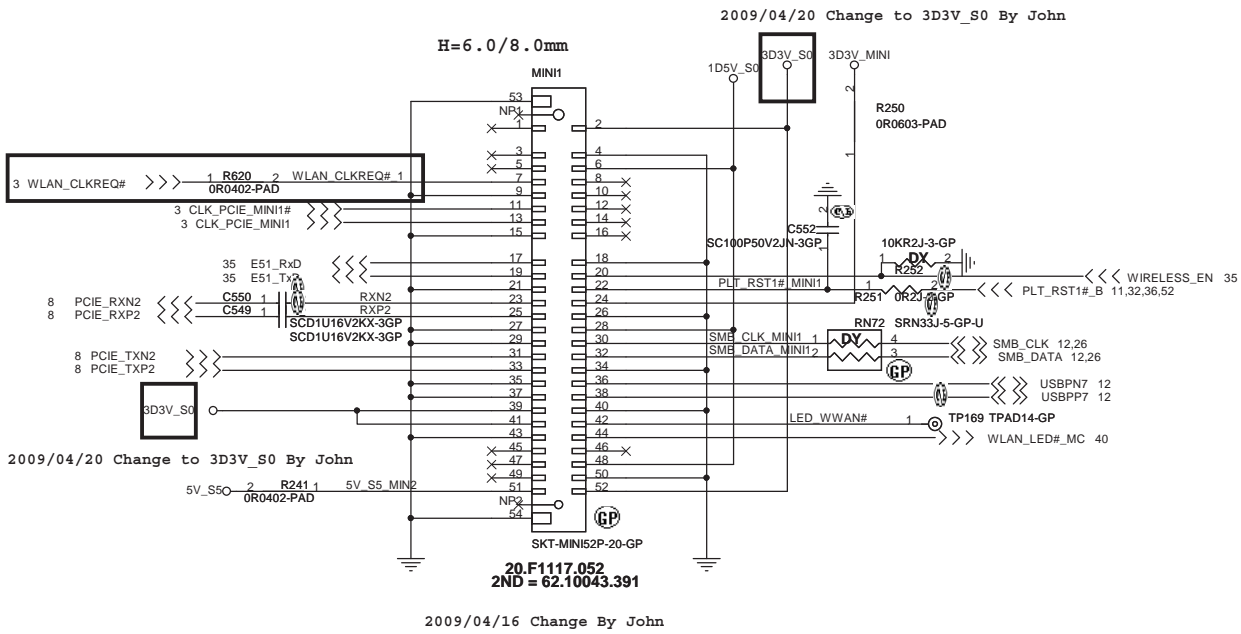
Title: **CARDREADER- RTS5159**

Size: Document Number: **JV71-TR** Rev: **SB**

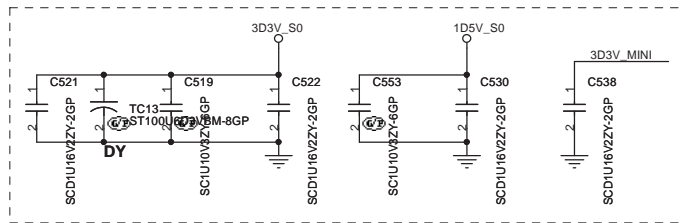
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# Mini Card Connector(WLAN)

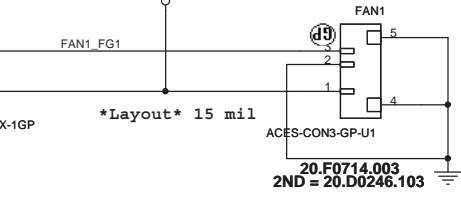
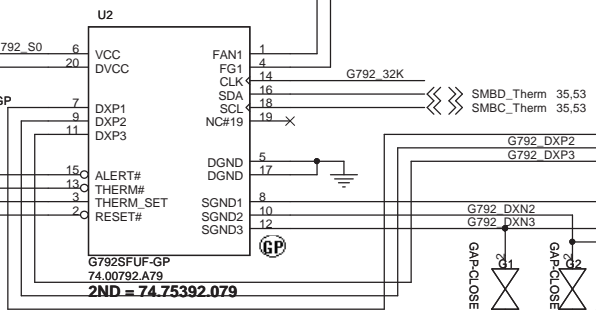
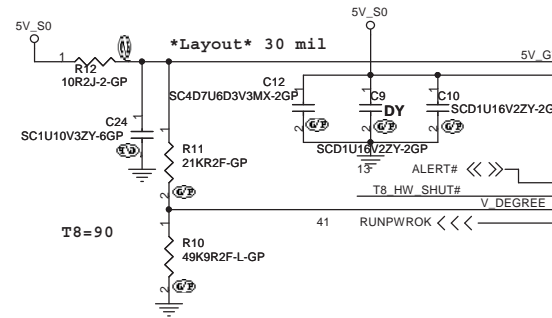
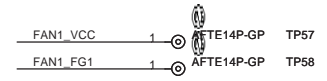
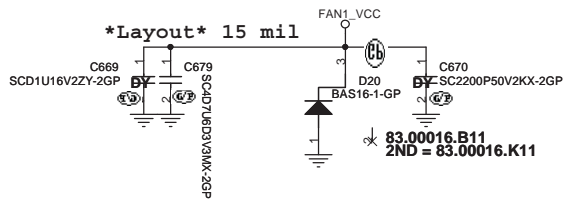


Place near MINI1

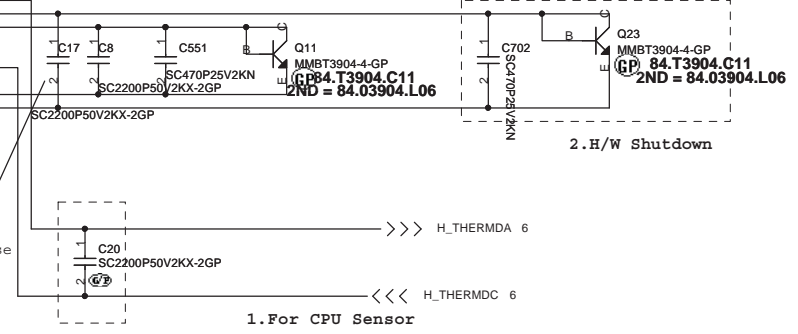


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Title		
<b>MINI CARD</b>		
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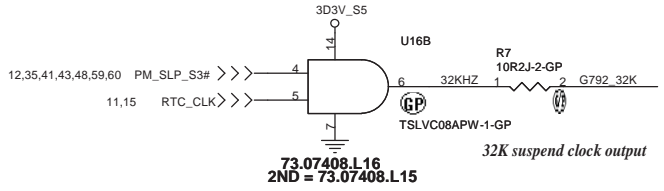


3.System Sensor, Put Plamrest.



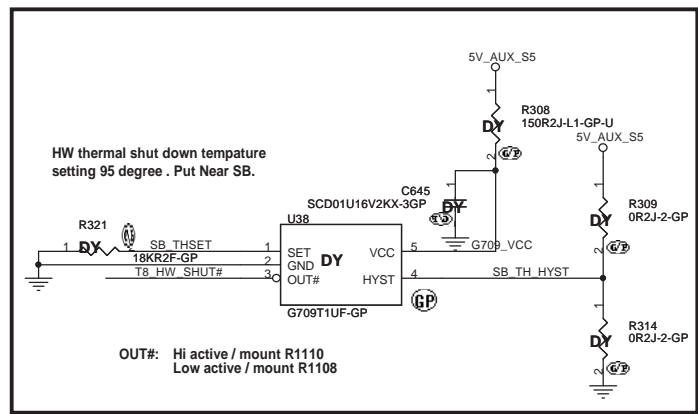
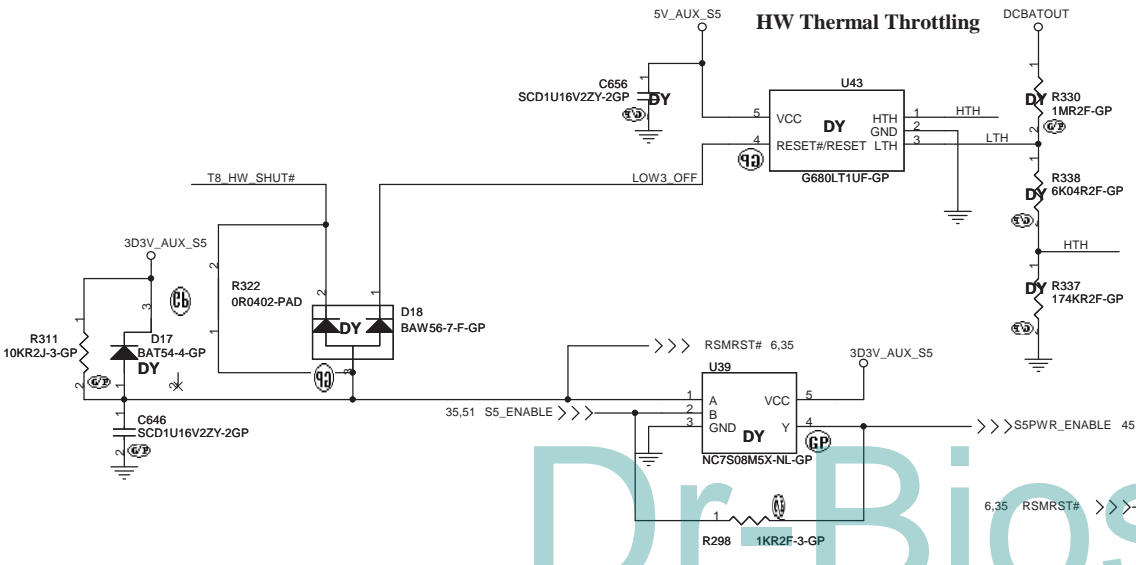
DXP1:108 Degree  
DXP2:H/W Setting  
DXP3:88 Degree

Place near chip as close as possible



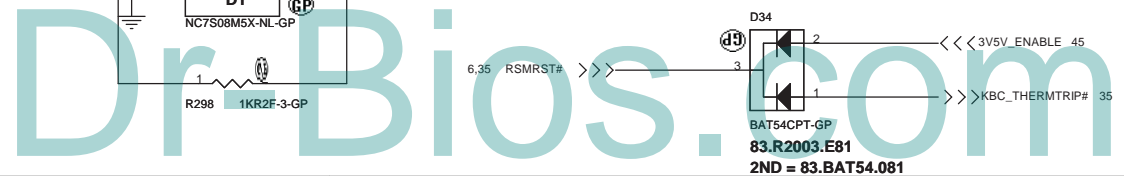
**BL3#**

**HW Thermal Throttling**

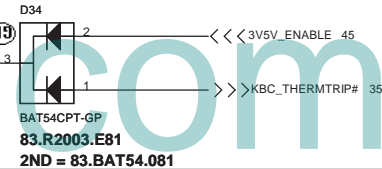


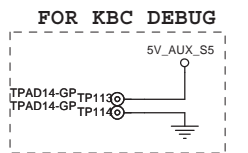
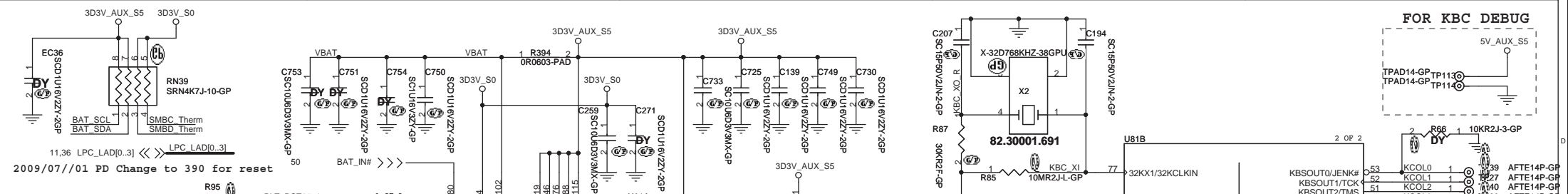
HW thermal shut down temperature setting 95 degree . Put Near SB.

OUT#: Hi active / mount R1110  
Low active / mount R1108

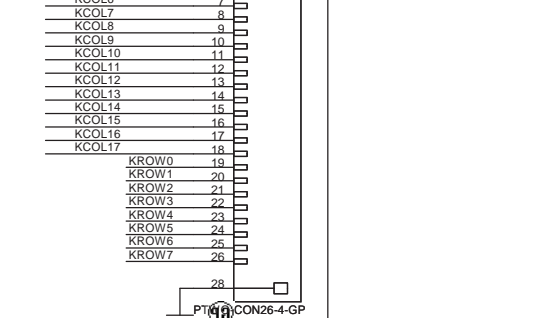
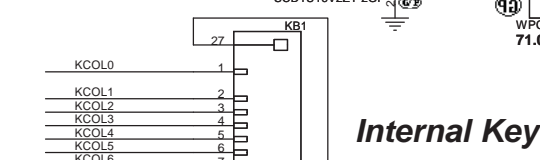
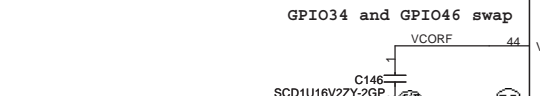
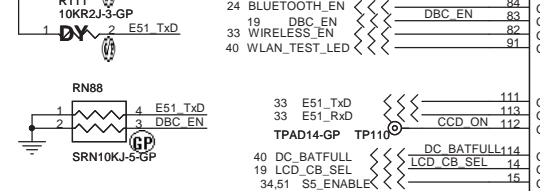
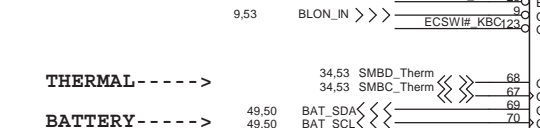
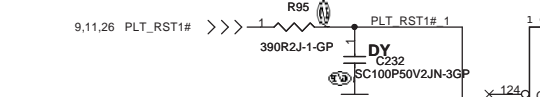


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<b>G792</b>		
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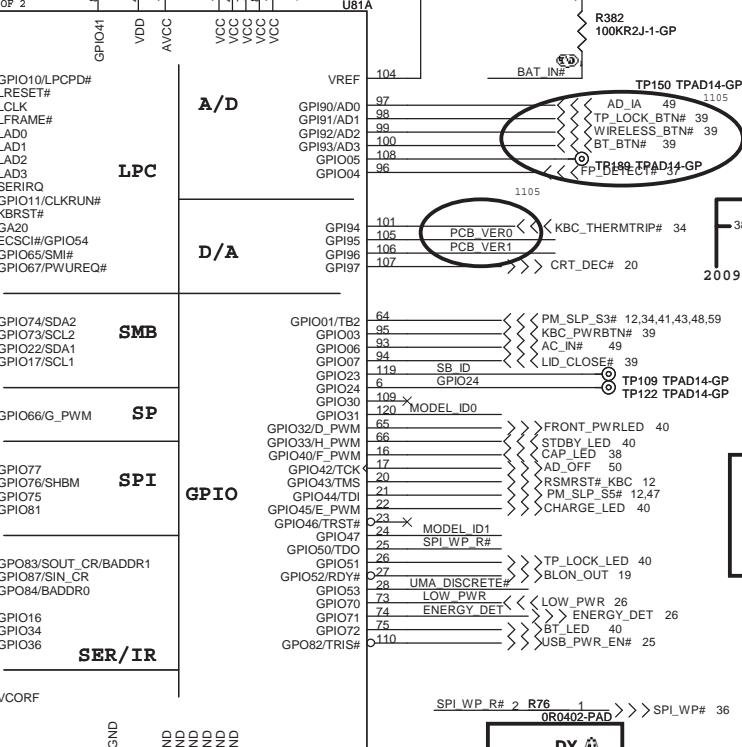




11.36 LPC\_LAD[0..3] <<< LPC\_LAD[0..3]  
2009/07//01 PD Change to 390 for reset  
9.11,26 PLT\_RST1# >>> 1 R95 PLT\_RST1# 1

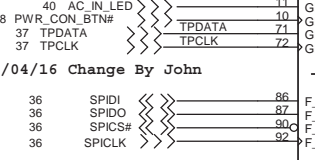
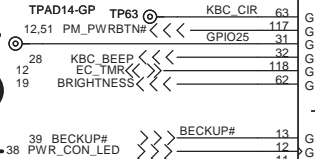
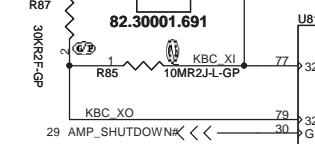


20\_K0382.026  
2ND = 20\_K0320.026

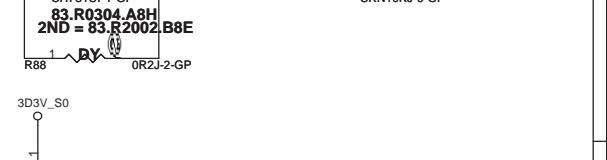
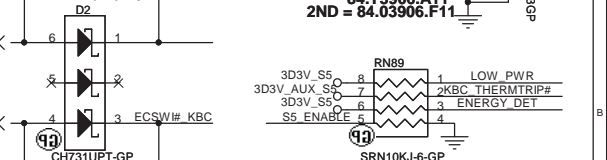
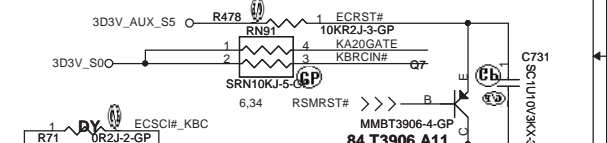
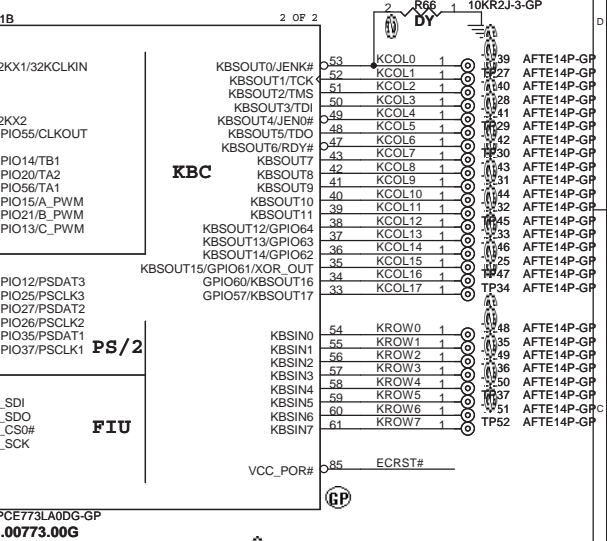
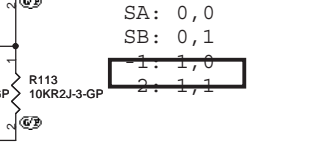
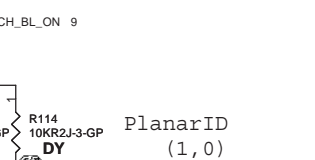
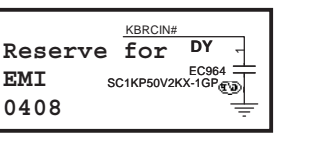


### Internal Keyboard Connector

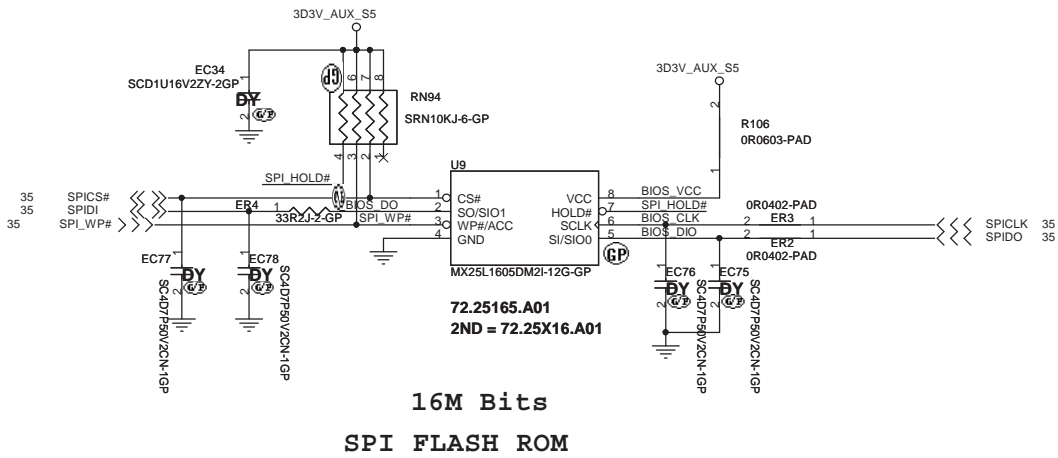
2009/04/20 ADD By John



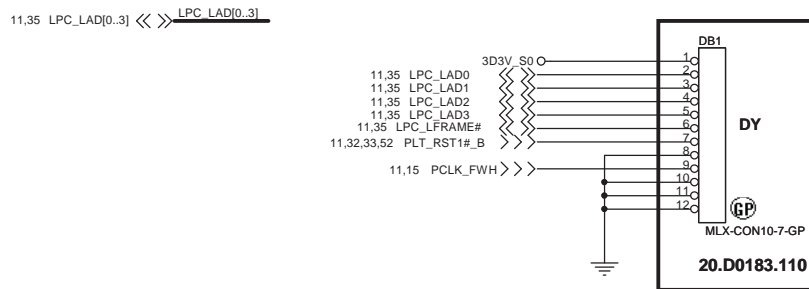
2009/04/16 Change By John



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KBC WPC773  
JV71-TR  
Date: Monday, July 06, 2009



GOLDEN FINGER FOR DEBUG BOARD

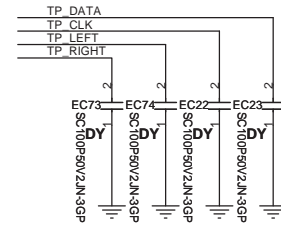
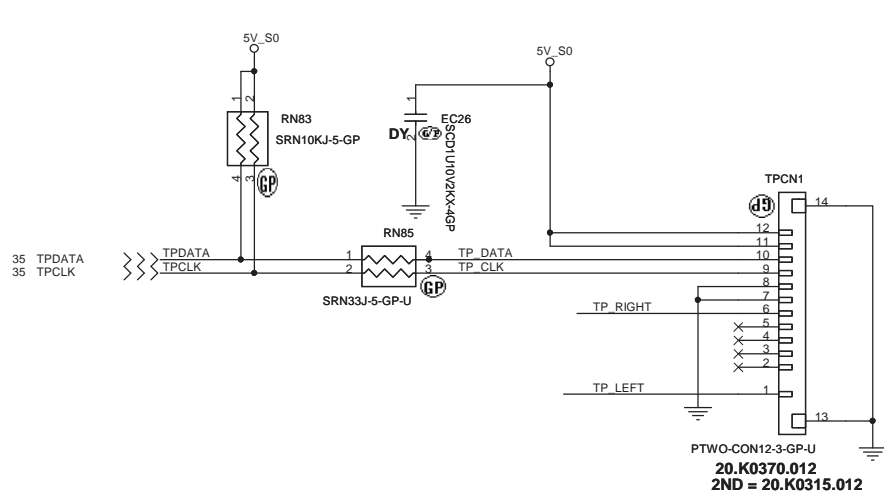


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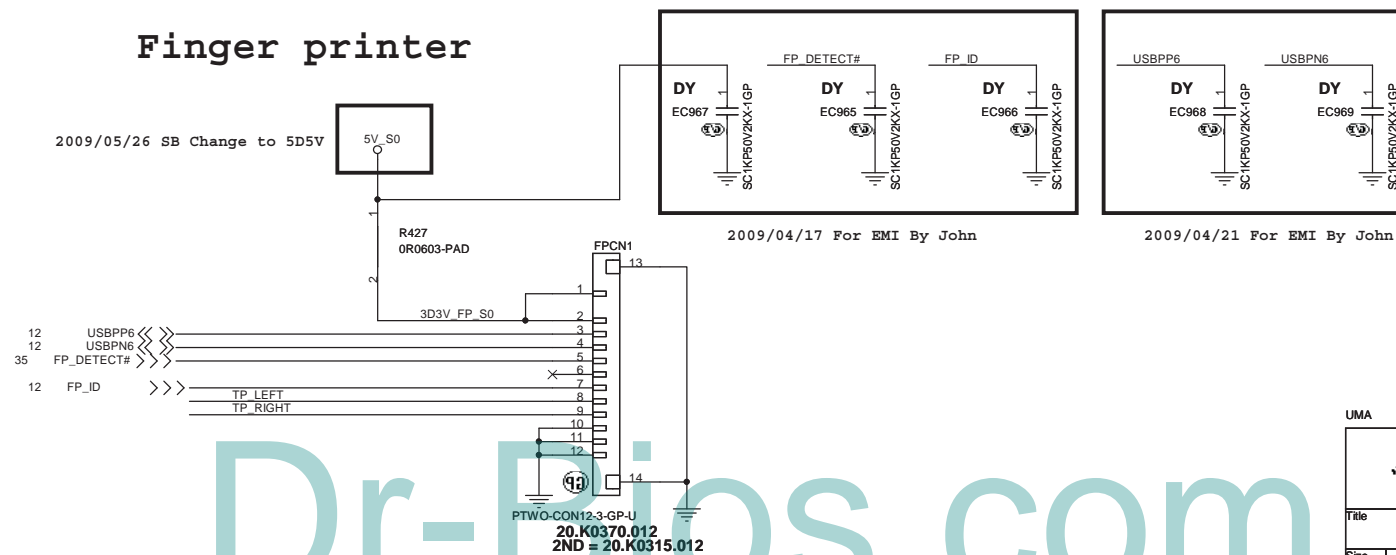
UMA

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Title			
<b>BIOS</b>			
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# TOUCH PAD



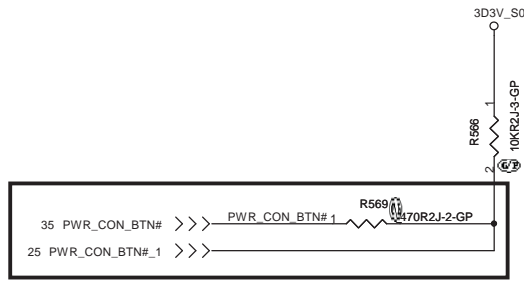
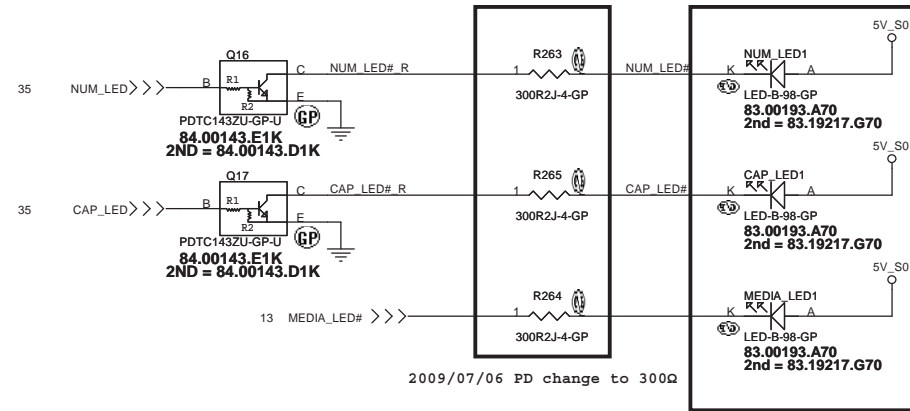
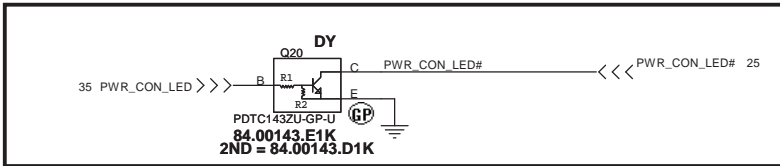
# Finger printer



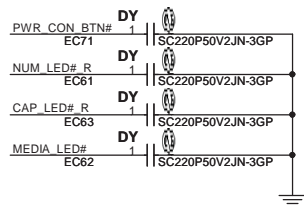
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Title		
<b>Touch PAD/Finger printer</b>		
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2009/04/16 Change By John



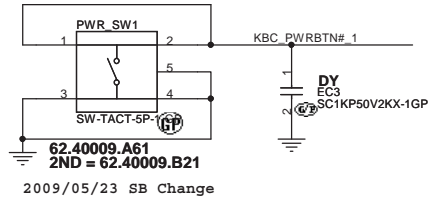
2009/04/16 Change By John



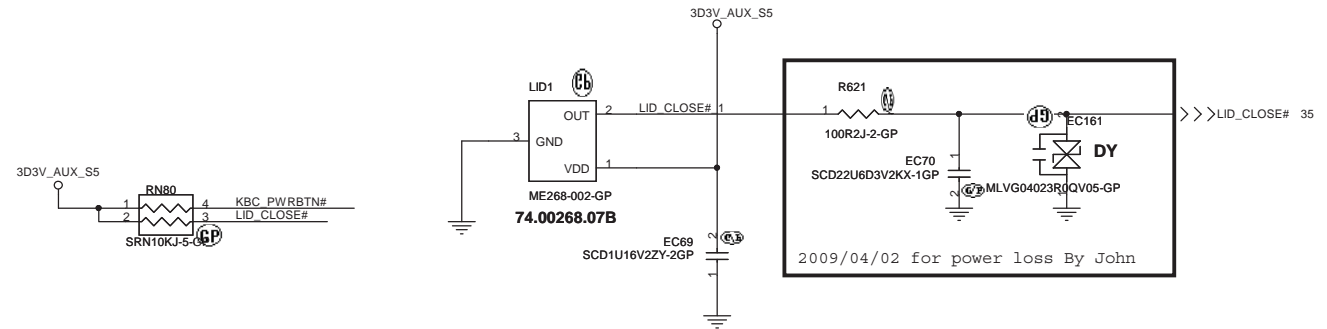
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<b>LAUNCH BOARD</b>	
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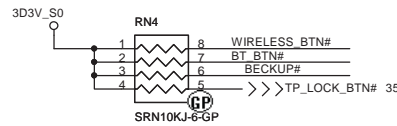
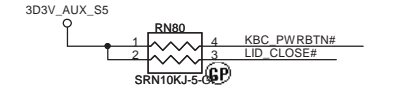
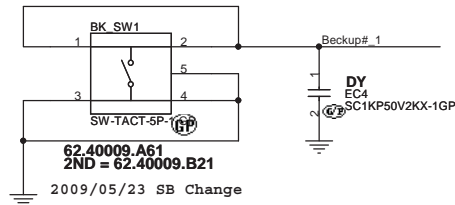
### Power Button



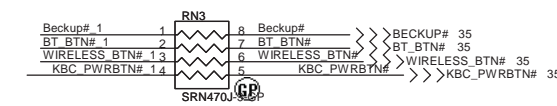
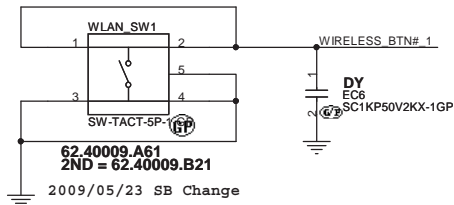
### Cover Up Switch



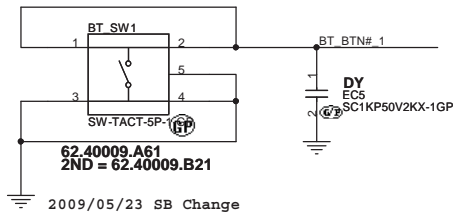
### Beckup Button



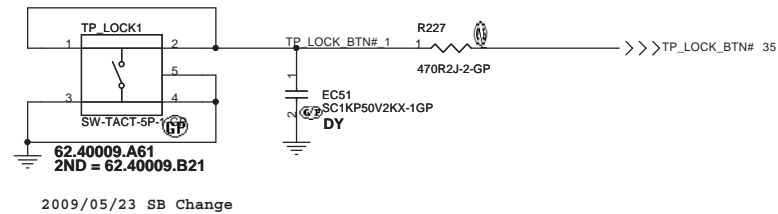
### WIRELESS Button



### BT/3G Button

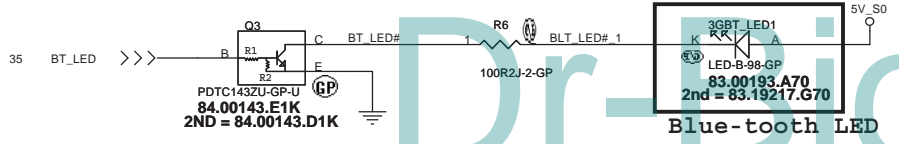
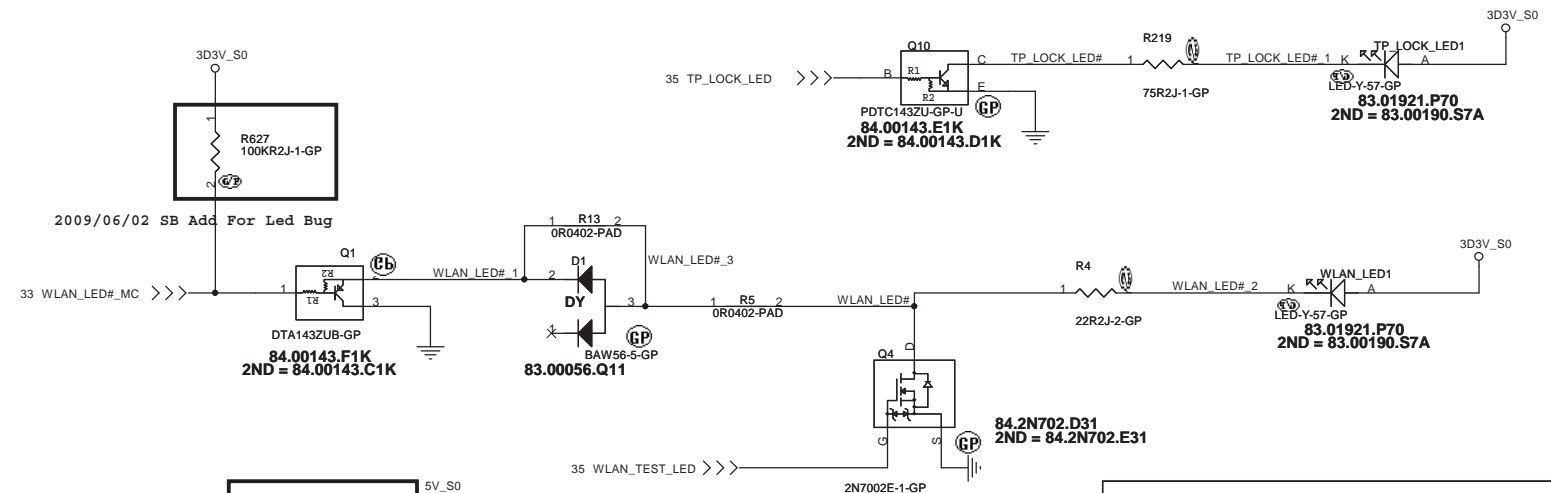
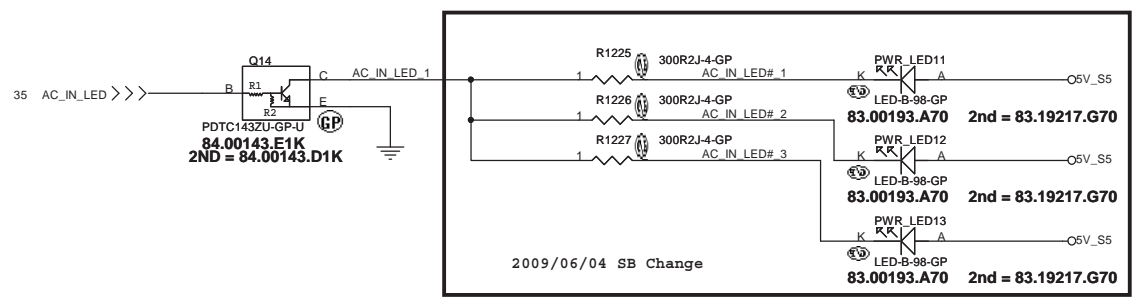
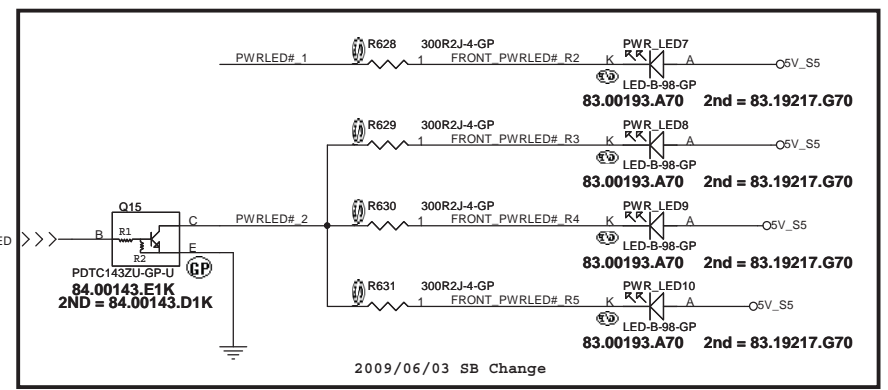
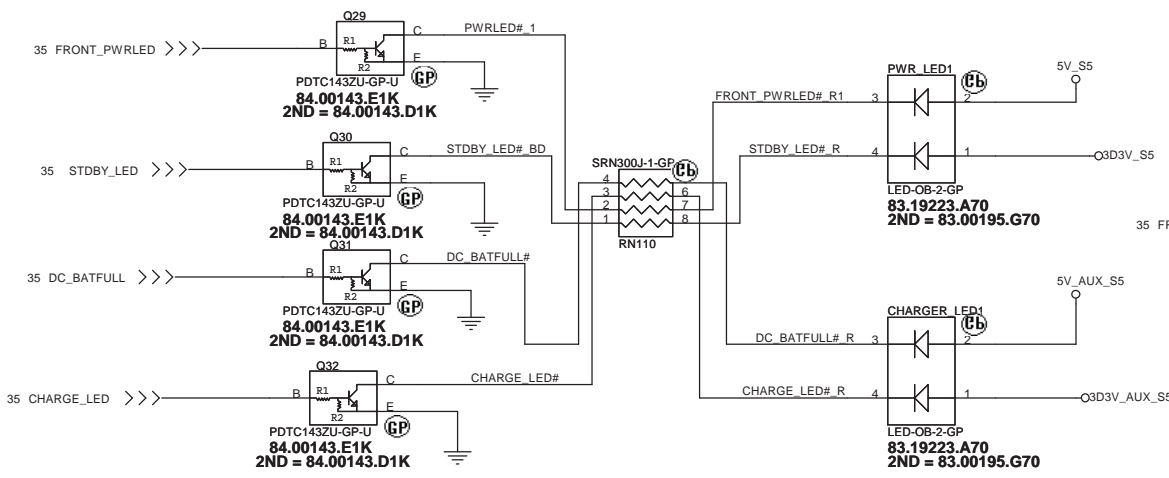


### T/P lock Button



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<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	<b>SWITCH</b>
Size	Document Number
A3	<b>JV71-TR</b>
Date: Monday, July 06, 2009	Sheet 39 of 61
Rev	<b>SA</b>



**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

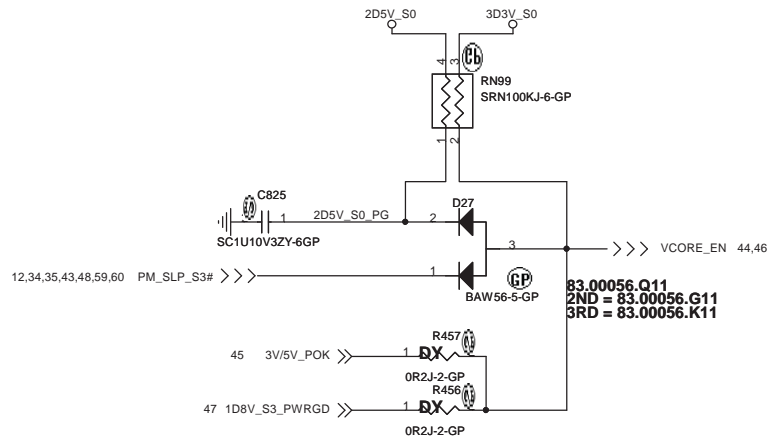
Title: **LED**

Size: A3 Document Number: **JV71-TR** Rev: **SB**

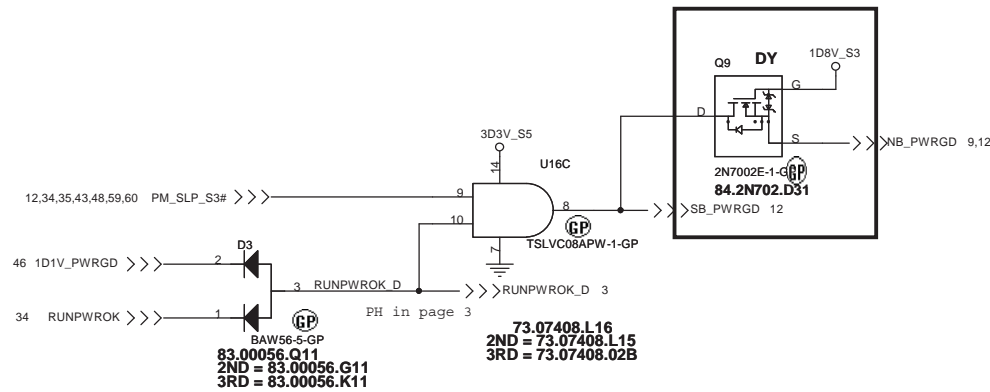
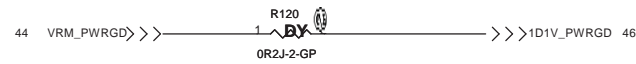
Date: Wednesday, July 08, 2009 Sheet: 40 of 61

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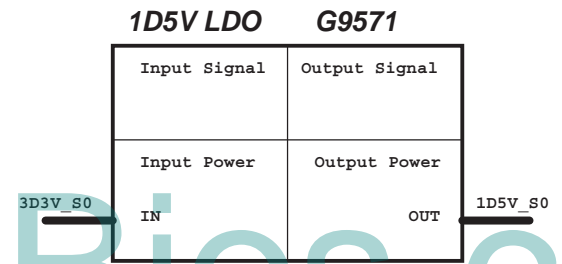
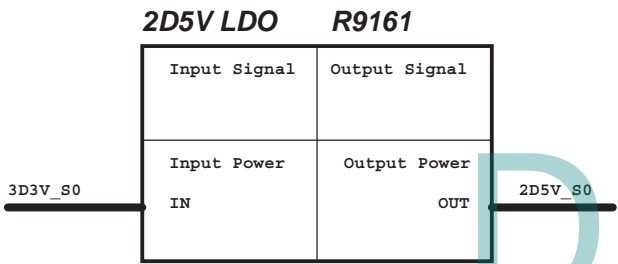
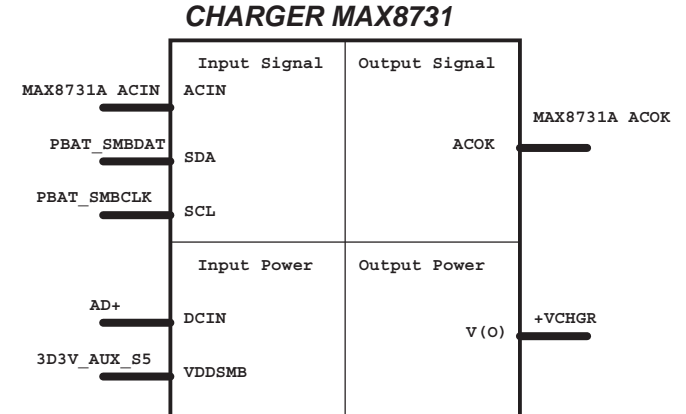
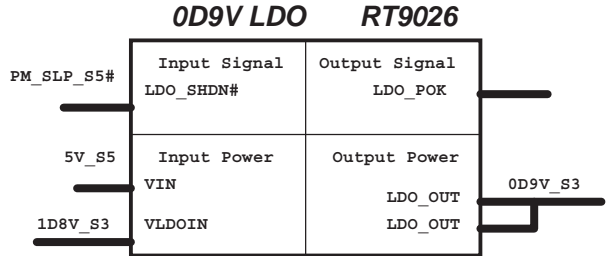
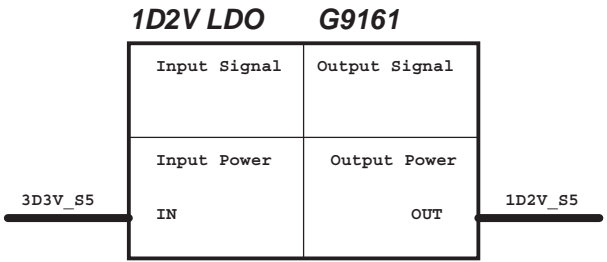
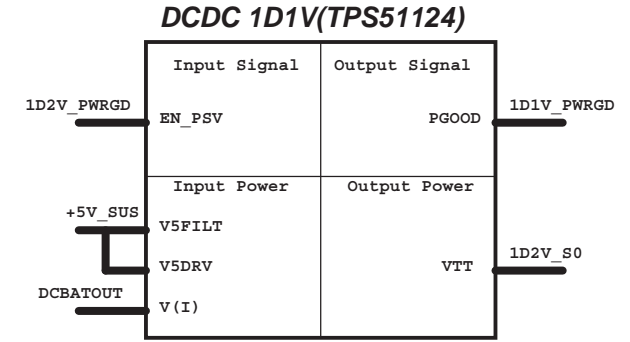
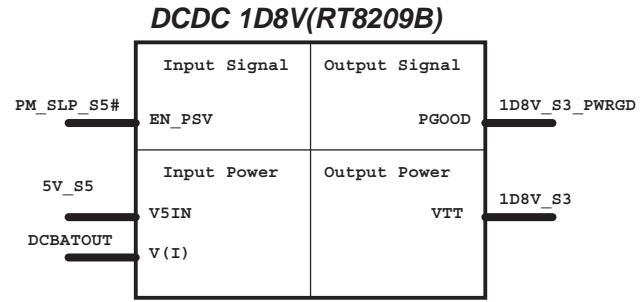
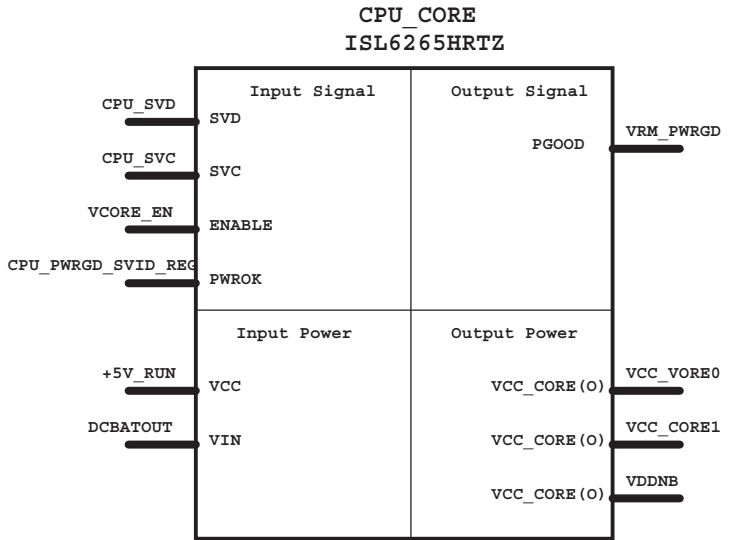
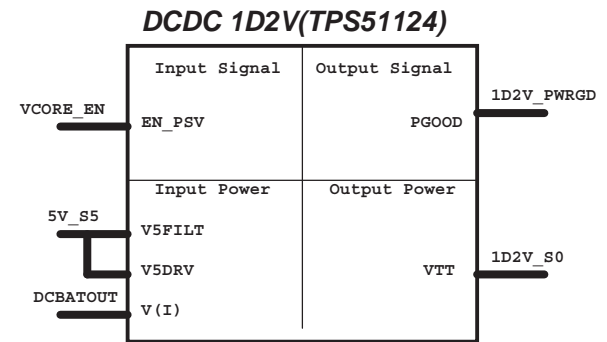
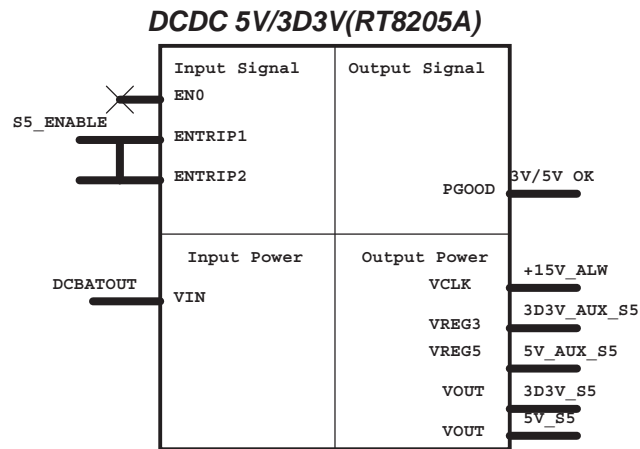
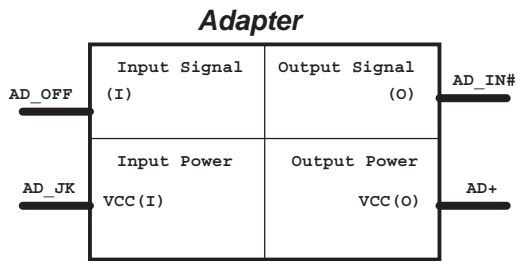
P/H @ 1D8V\_S3 PAGE



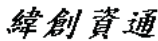
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<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title <b>POWER ON LOGIC</b></p>	
<p>Size A3</p>	<p>Document Number <b>JV71-TR</b></p>
<p>Date: Monday, July 06, 2009</p>	<p>Rev SA</p>
<p>Sheet 41 of 61</p>	<p>1</p>

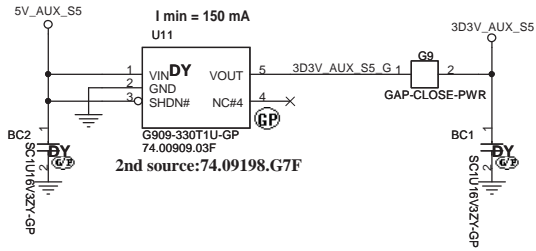


UMA

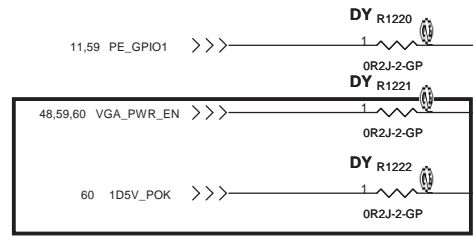
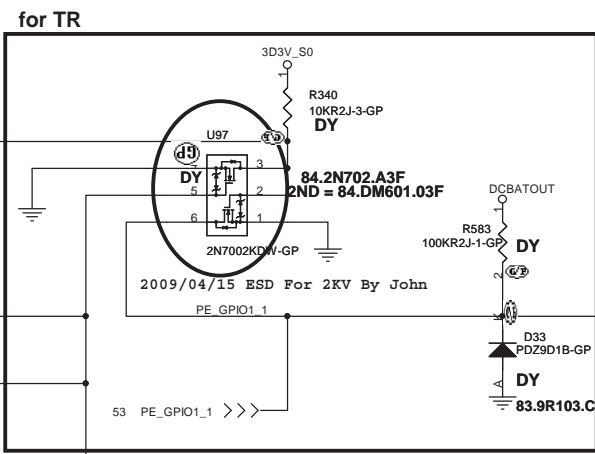
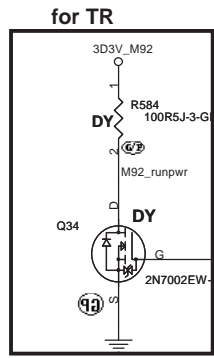
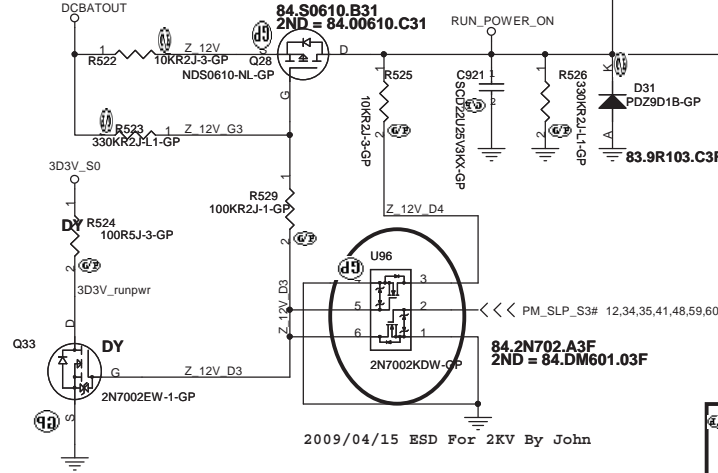
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Power Block Diagram</b>	
Size <b>A3</b>	Document Number <b>JV71-TR</b>
Date: <b>Monday, July 06, 2009</b>	Rev <b>SA</b>
Sheet <b>42</b>	of <b>61</b>

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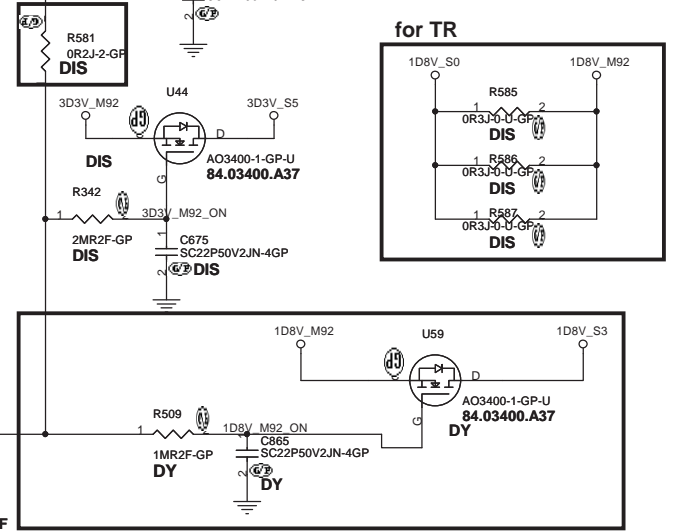
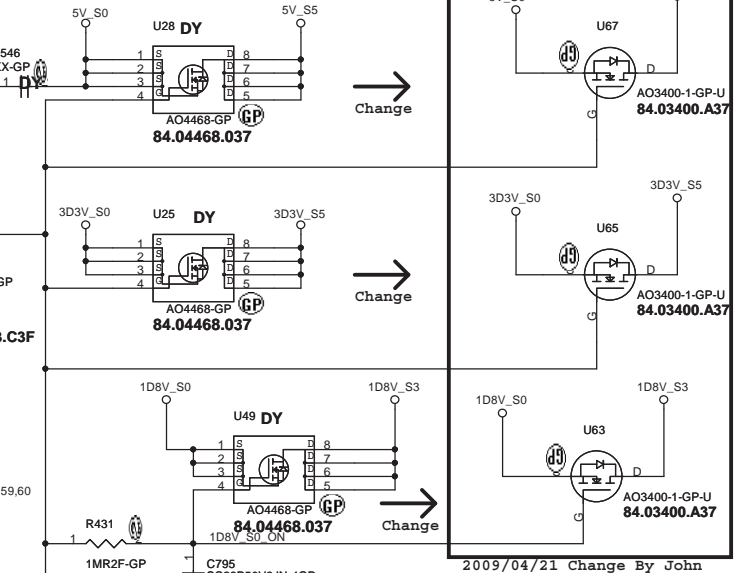
# Aux Power 3D3V\_AUX\_S5



# Run Power



2009/04/21 ADD By John



R509, R342--10MΩ  
 C865--22pF  
 C795--1000pF  
 For VGA sequence issue

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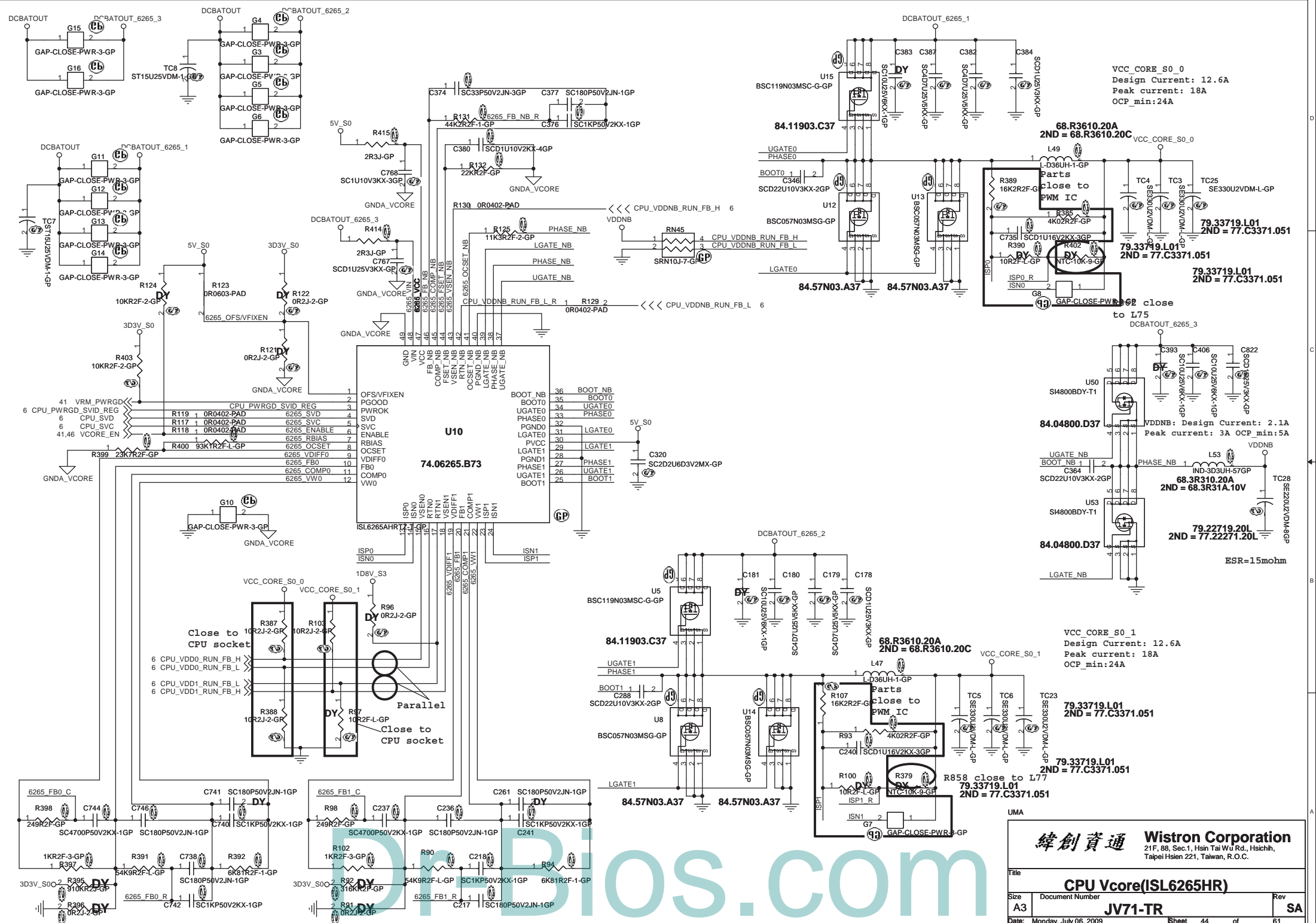
UMA

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Title: **RUN AND AUX POWER**

Size: A3 Document Number: **JV71-TR** Rev: SA

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VCC\_CORE\_S0\_0  
 Design Current: 12.6A  
 Peak current: 18A  
 OCP\_min:24A

VCC\_CORE\_S0\_0  
 2ND = 68.R3610.20C

79.33719.L01  
 2ND = 77.C3371.051

79.33719.L01  
 2ND = 77.C3371.051

VDDNB: Design Current: 2.1A  
 Peak current: 3A OCP\_min:5A

68.3R310.20A  
 2ND = 68.3R31A.10V

79.22719.20L  
 2ND = 77.22271.20L

ESR=15mohm

VCC\_CORE\_S0\_1  
 Design Current: 12.6A  
 Peak current: 18A  
 OCP\_min:24A

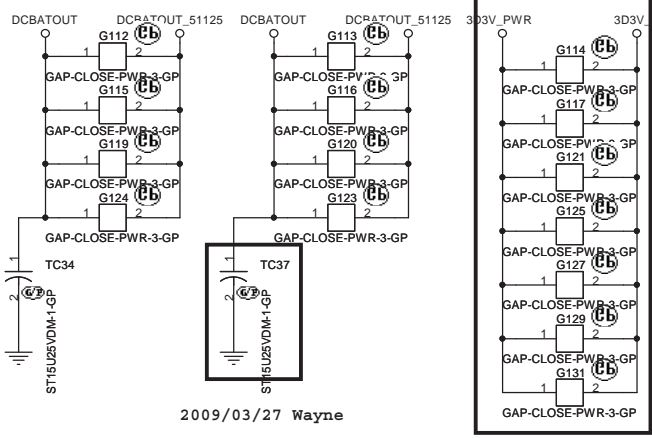
79.33719.L01  
 2ND = 77.C3371.051

79.33719.L01  
 2ND = 77.C3371.051

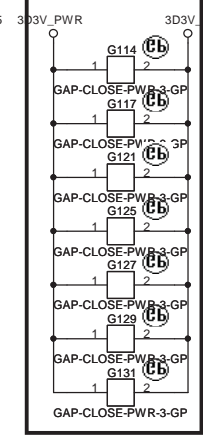
79.33719.L01  
 2ND = 77.C3371.051

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

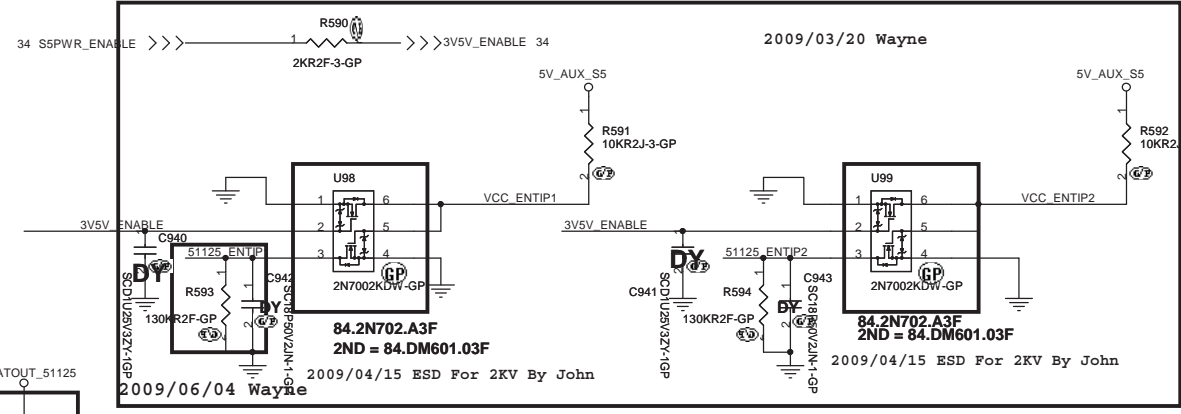
Title			CPU Vcore (ISL6265HR)		
Size	Document Number				Rev
A3	JV71-TR				SA
Date:	Monday, July 06, 2009		Sheet	44	of 61



2009/03/27 Wayne



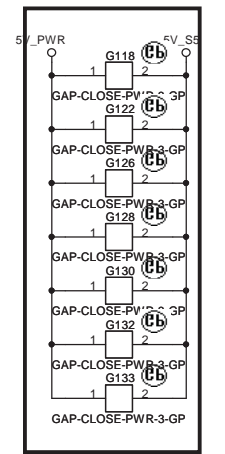
2009/03/11 Wayne



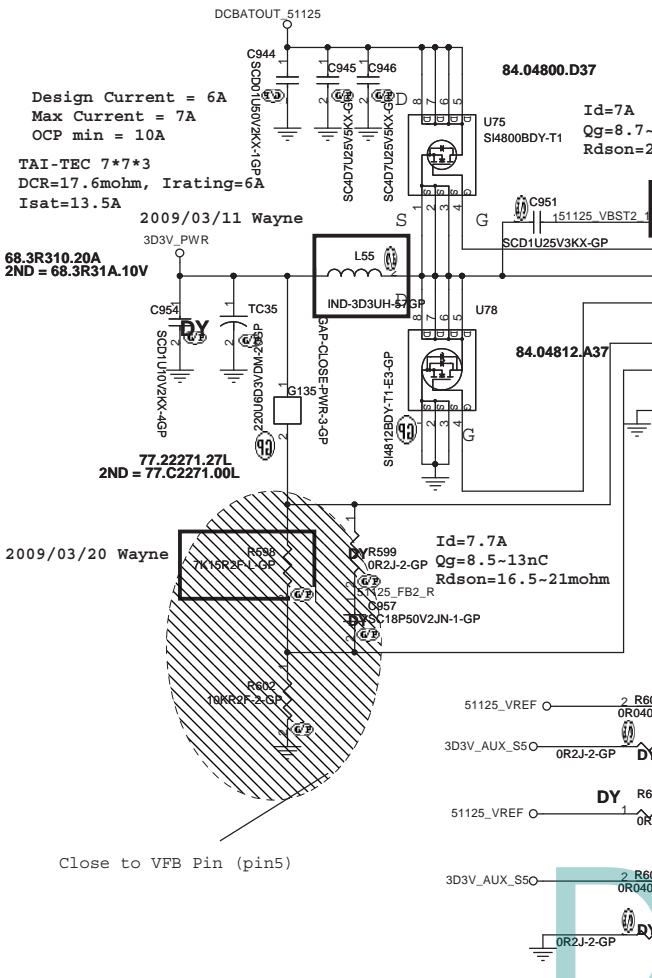
2009/06/04 Wayne

2009/04/15 ESD For 2KV By John

2009/04/15 ESD For 2KV By John



2009/03/11 Wayne



Design Current = 6A  
Max Current = 7A  
OCP min = 10A  
TAI-TEC 7\*7\*3  
DCR=17.6mohm, Irating=6A  
Isat=13.5A

84.04800.D37

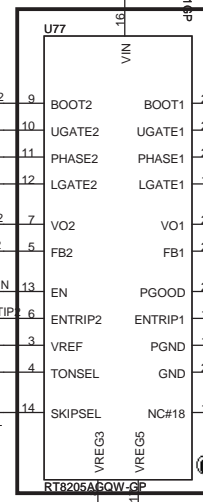
2009/03/20 Wayne

Id=7A  
Qg=8.7-13nC  
Rdson=23-30mohm

84.04800.D37

TAI-TEC 7\*7\*3  
DCR=17.6mohm, Irating=6A  
Isat=13.5A

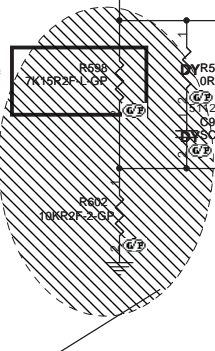
Design Current = 6A  
Max Current = 7A  
OCP min = 10A



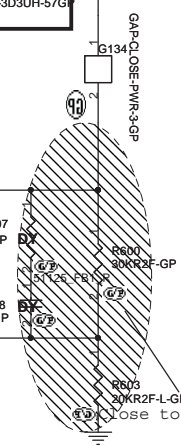
2009/03/20 Wayne

68.3R310.20A  
2ND = 68.3R31A.10V

2009/03/11 Wayne



Close to VFB Pin (pin5)



Close to VFB Pin (pin2)

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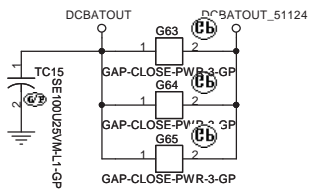
UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

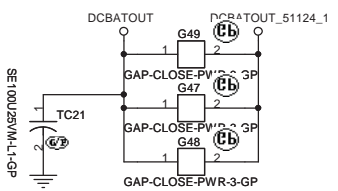
Title: **DCDC 5V/3D3V (RT8205A)**

Size: A3 Document Number: **JV71-TR** Rev: SA

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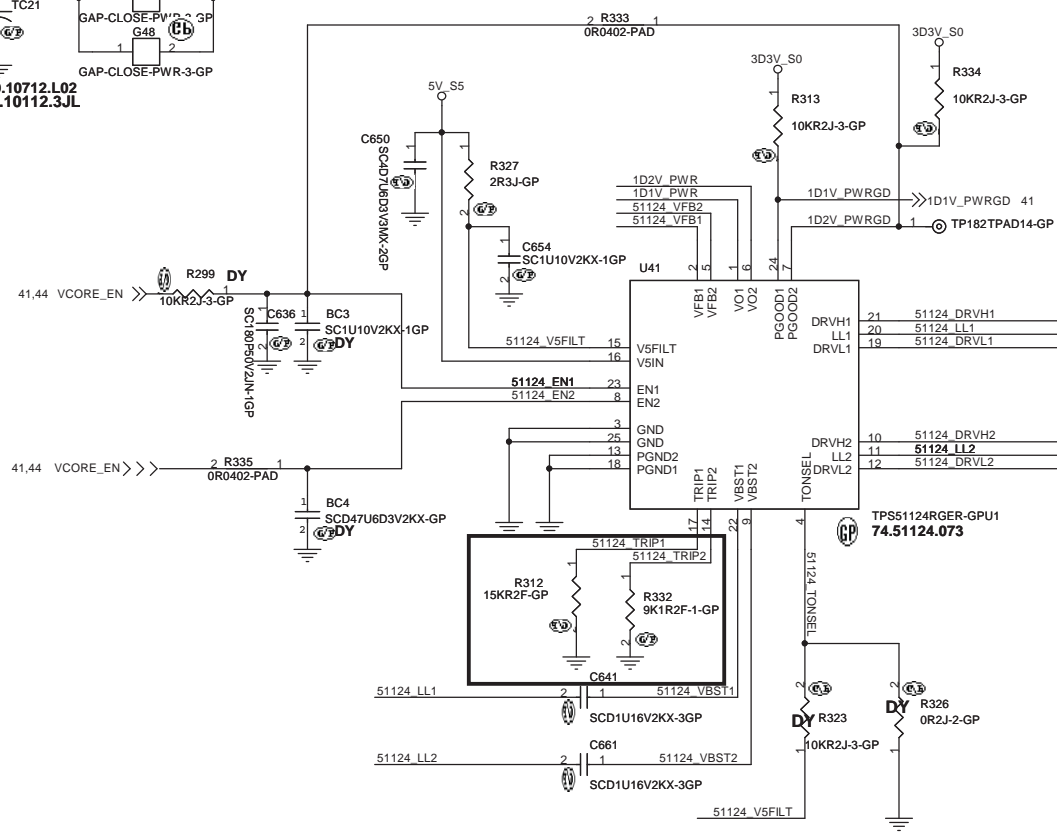
79.10712.L02  
2ND = 79.10112.3JL



79.10712.L02  
2ND = 79.10112.3JL

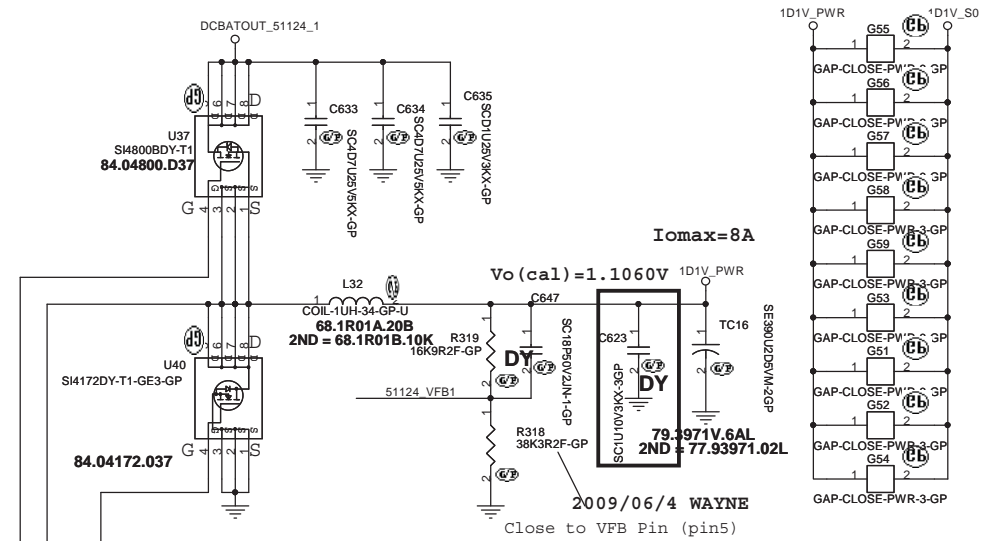
$$V_{trip} (mV) = R_{trip} (Kohm) * 10 (uA)$$

$$I_{ocp} = (V_{trip} / R_{dson}) + ((1 / (2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$



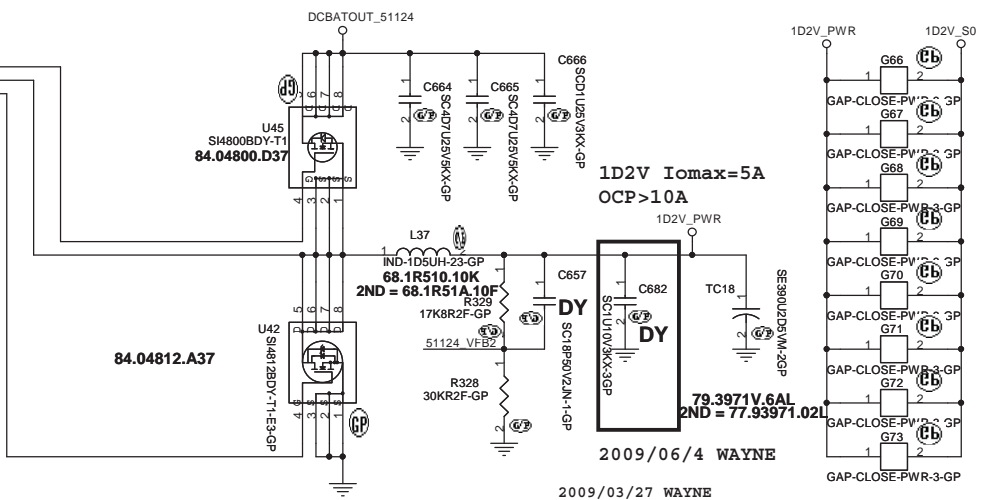
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1 + R2) / R2$  --> PWM mode  
 $V_{out} = 0.764V * (R1 + R2) / R2$  --> Skip Mode



2009/06/4 WAYNE  
Close to VFB Pin (pin5)

2009/03/27 WAYNE  
C623 change to 1u10v for ESL



2009/06/4 WAYNE  
2009/03/27 WAYNE  
C682 change to 1u10v for ESL

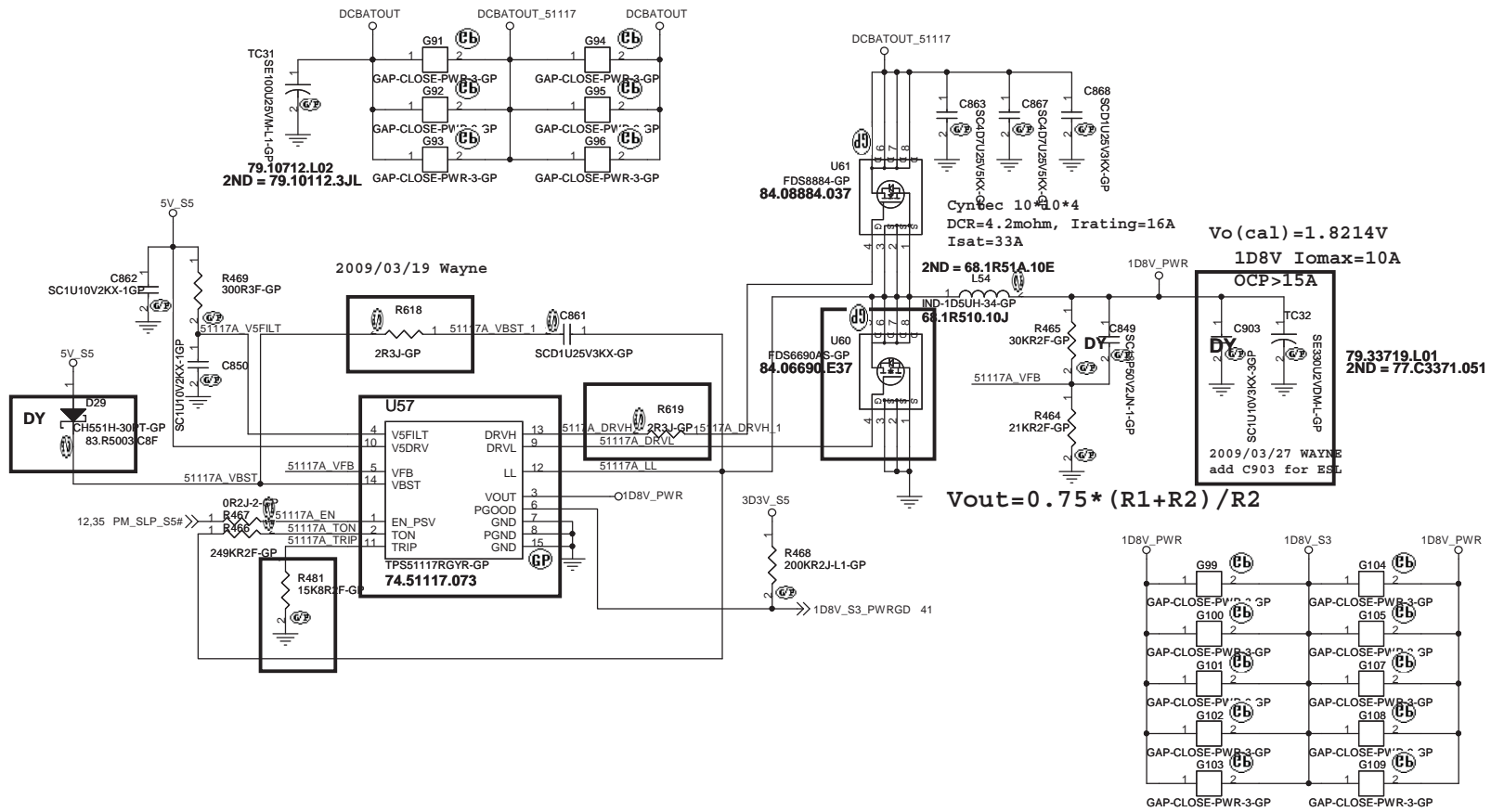
UMA

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51124 1D1V 1D2V**

Size: A3	Document Number: <b>JV71-TR</b>	Rev: SA
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79.10712.L02  
2ND = 79.10112.3JL

84.08884.037

CynSec 10#10\*4  
DCR=4.2mohm, Irating=16A  
Isat=33A

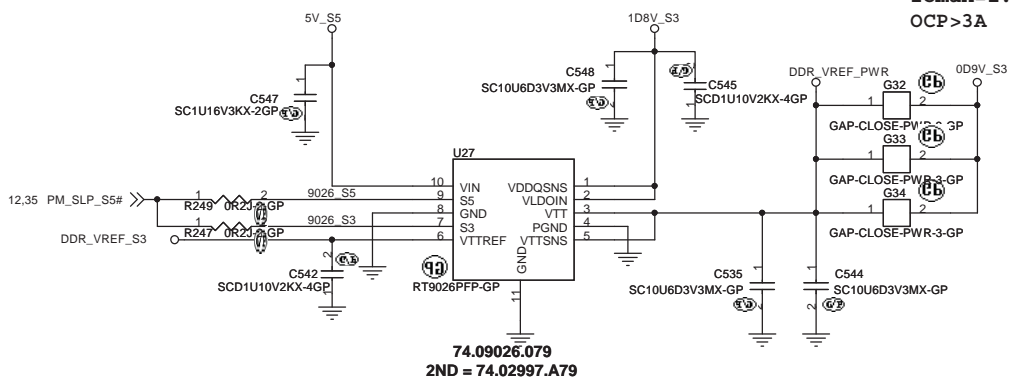
Vo(cal)=1.8214V  
1D8V Iomax=10A

79.33719.L01  
2ND = 77.C3371.051

$$V_{out} = 0.75 * (R1 + R2) / R2$$

DDR\_0.9V

Iomax=1.5A  
OCP>3A



74.09026.079  
2ND = 74.02997.A79

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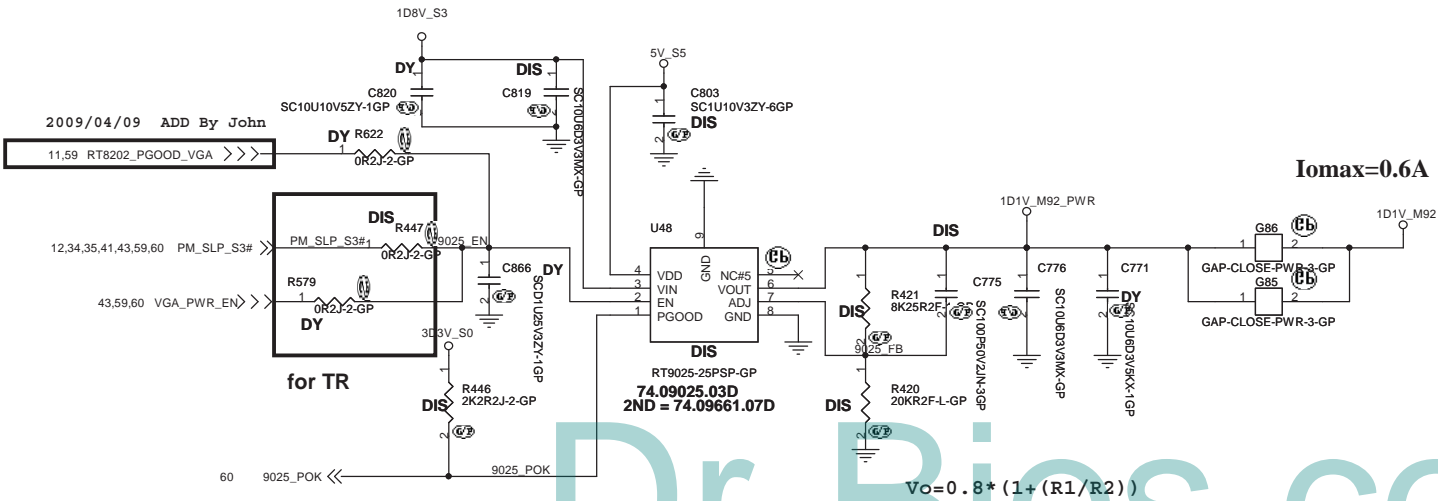
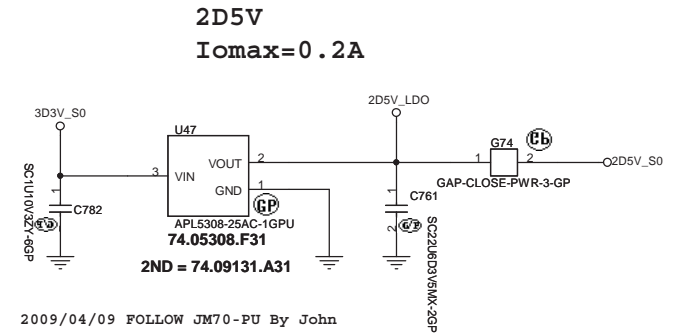
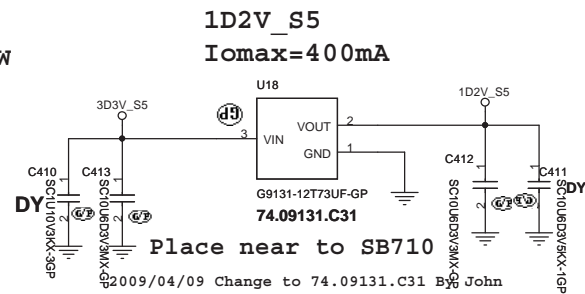
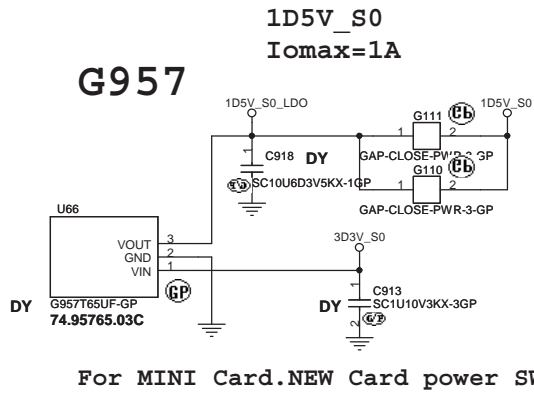
UMA

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCDC 1D8V APW7141/LDO 0D9V**

Size: A3 Document Number: **JV71-TR** Rev: SA

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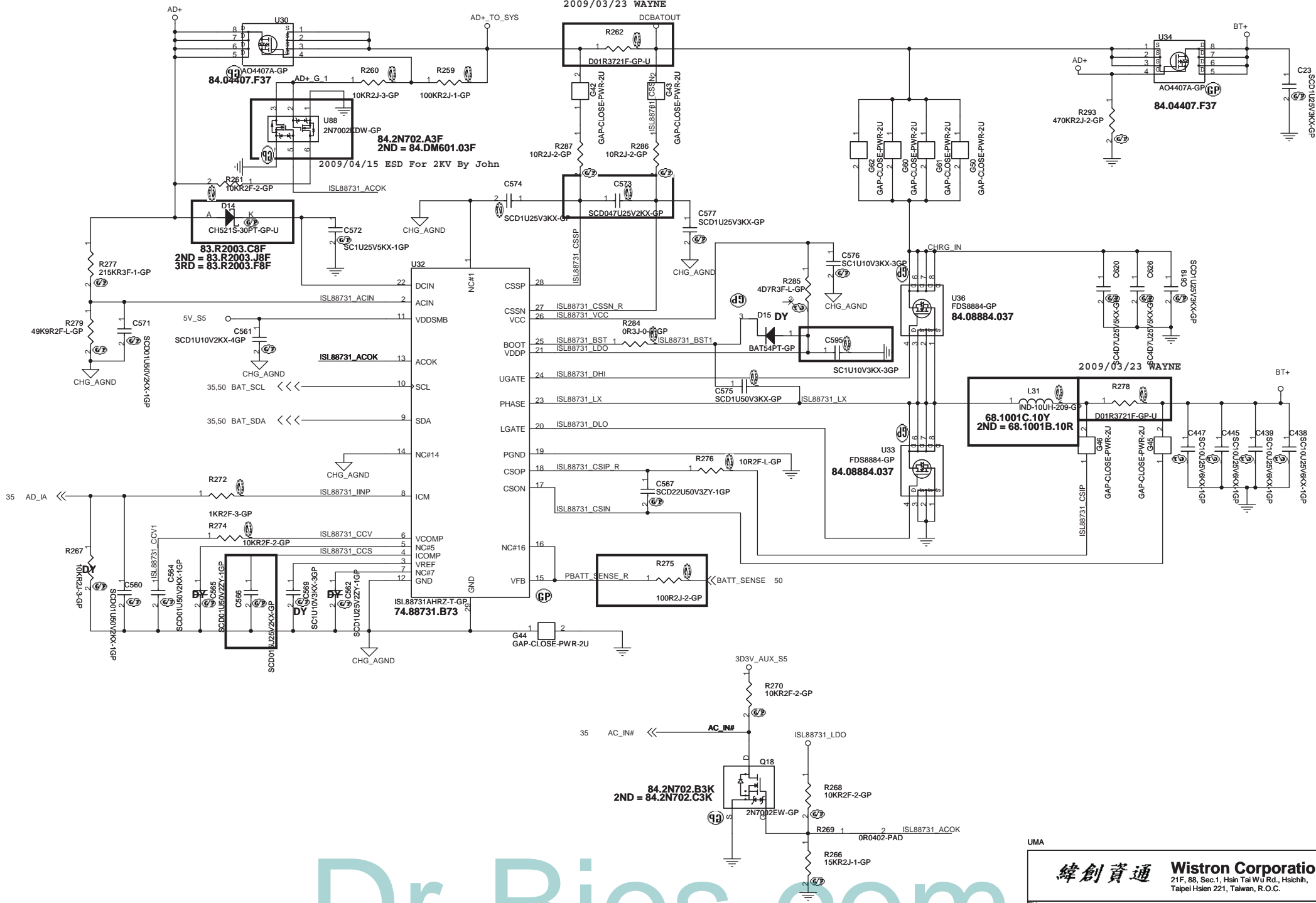


UMA		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LDO 2D5V/1D5V/1D2V S5/1D1V M92		
Size	Document Number	Rev	
A3	JV71-TR	SA	
Date:	Monday, July 06, 2009	Sheet	48 of 61

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2009/03/23 WAYNE



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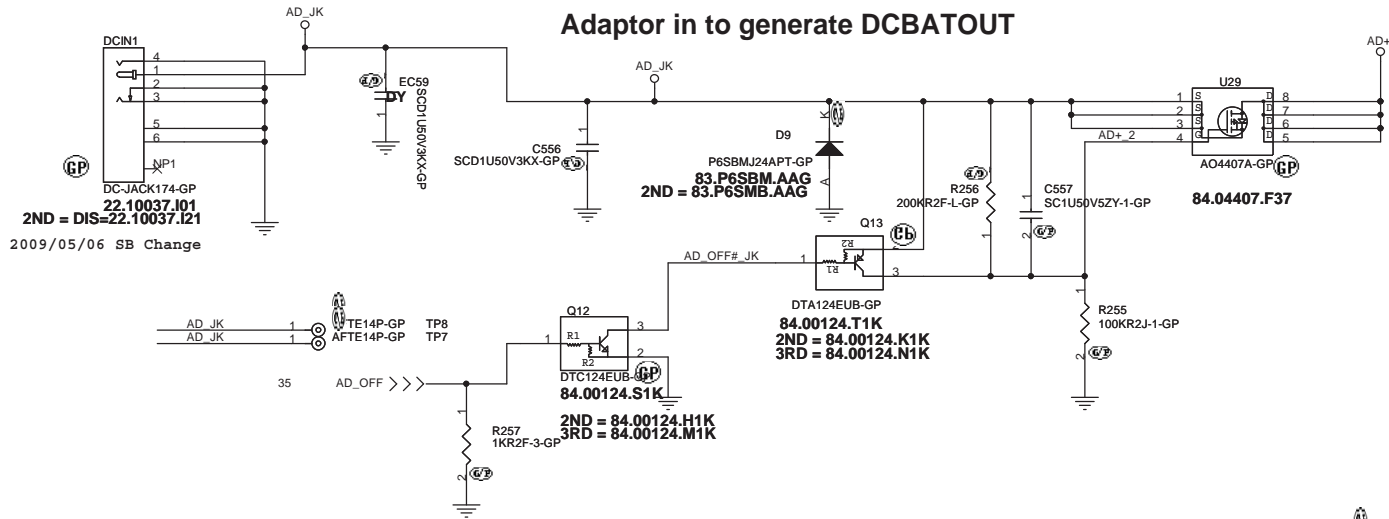
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL88731A Charger**

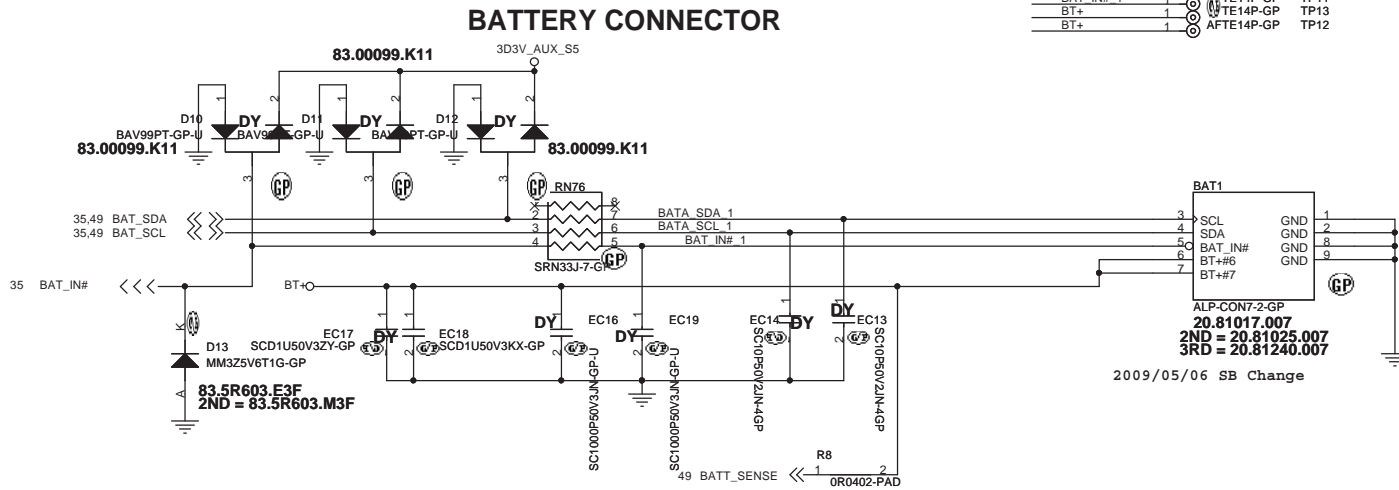
Size A3 Document Number **JV71-TR** Rev SA

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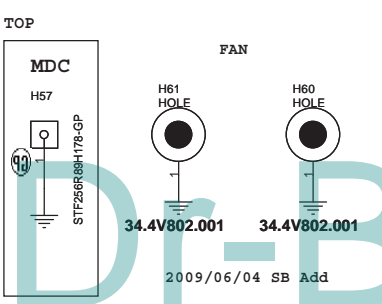
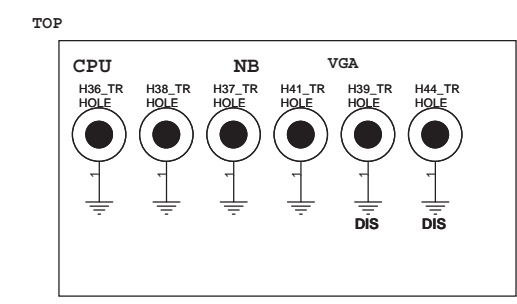
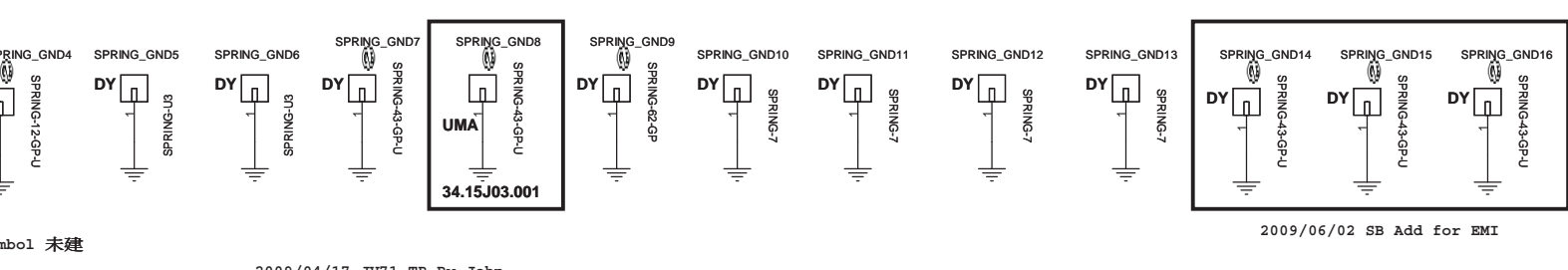
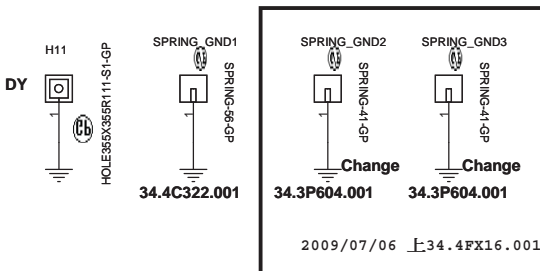
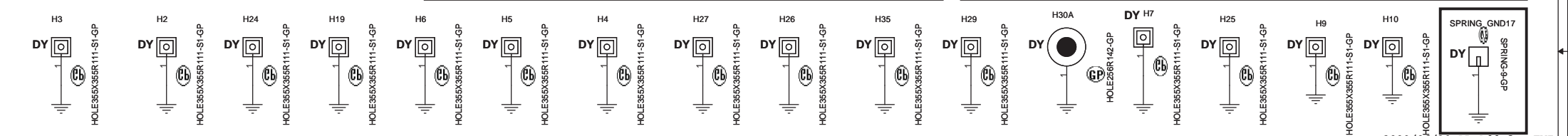
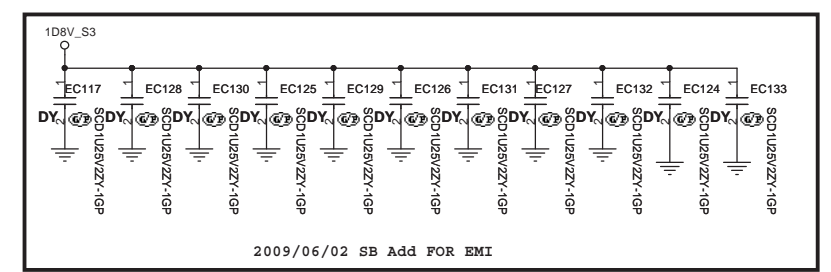
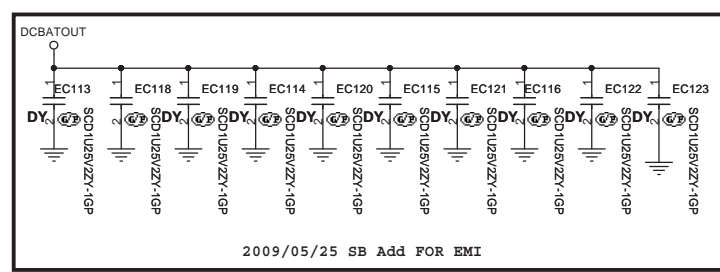
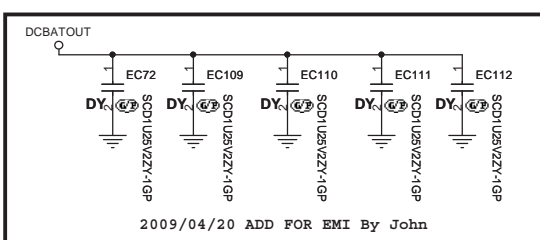
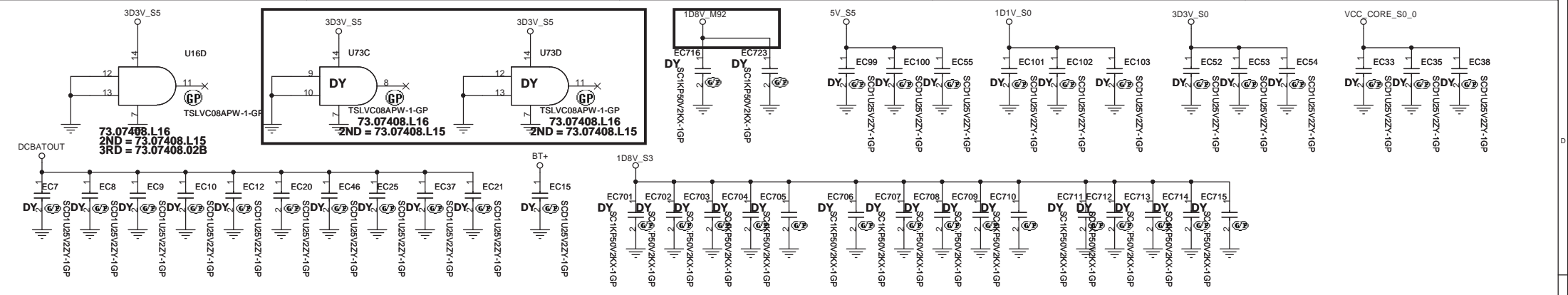


BATA_SDA_1	1	TE14P-GP	TP9
BATA_SCL_1	1	TE14P-GP	TP10
BAT_IN#_1	1	TE14P-GP	TP11
BT+	1	TE14P-GP	TP13
BT+	1	AFTE14P-GP	TP12



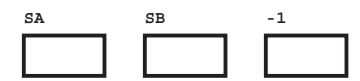
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<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>AD/BATT CONN</b>	
Size	Document Number <b>JV71-TR</b> Rev <b>SB</b>
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**Check test point**

3D3V_S0	TP233	TPAD14-GP
3D3V_AUX_S5	TP232	TPAD14-GP
3D3V_S5	TP231	TPAD14-GP
5V_S5	TP230	TPAD14-GP
12.35 PM_PWRBTN#	TP229	TPAD14-GP
6.11 CPU_PWRGD	TP228	TPAD14-GP
34.35 SS_ENABLE	TP227	TPAD14-GP
6.11 CPU_LDT_RST#	TP226	TPAD14-GP



Test Point放在Dimm Door打開可量測處

UMA

緯創資通 Wistron Corporation

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Title: EMI/Spring/Boss

Size: Document Number JV71-TR Rev SB

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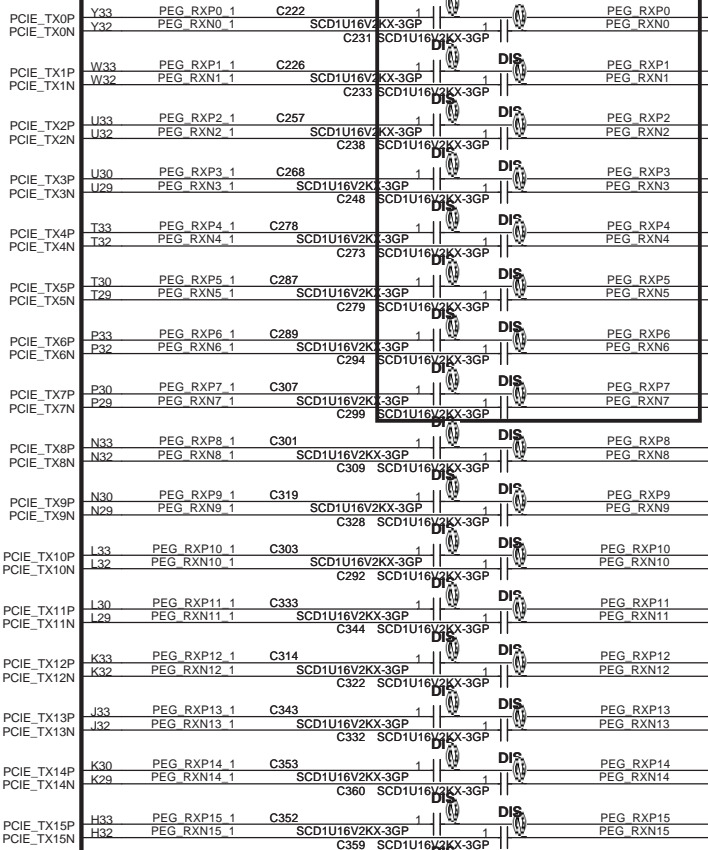
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AVGA1A 1 OF 8

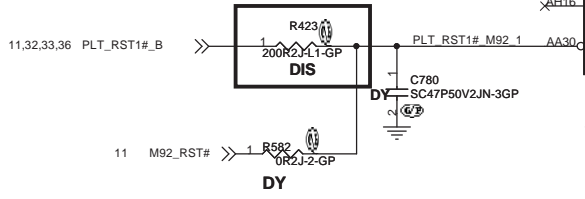
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PEG_TXP2	W38	PCI_E_RX2P
PEG_TXN2	V37	PCI_E_RX2N
PEG_TXP3	V35	PCI_E_RX3P
PEG_TXN3	U36	PCI_E_RX3N
PEG_TXP4	U38	PCI_E_RX4P
PEG_TXN4	T37	PCI_E_RX4N
PEG_TXP5	T35	PCI_E_RX5P
PEG_TXN5	R36	PCI_E_RX5N
PEG_TXP6	R38	PCI_E_RX6P
PEG_TXN6	P37	PCI_E_RX6N
PEG_TXP7	P35	PCI_E_RX7P
PEG_TXN7	N36	PCI_E_RX7N
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PEG_TXN8	M37	PCI_E_RX8N
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PEG_TXN9	L36	PCI_E_RX9N
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PEG_TXP11	K35	PCI_E_RX11P
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PEG_TXP12	J38	PCI_E_RX12P
PEG_TXN12	H37	PCI_E_RX12N
PEG_TXP13	H35	PCI_E_RX13P
PEG_TXN13	G36	PCI_E_RX13N
PEG_TXP14	G38	PCI_E_RX14P
PEG_TXN14	F37	PCI_E_RX14N
PEG_TXP15	F35	PCI_E_RX15P
PEG_TXN15	E36	PCI_E_RX15N

PCI EXPRESS INTERFACE



3 CLK\_PCIE\_PEG << AB35  
 3 CLK\_PCIE\_PEG# << AA36

2009/07/01 PD Change to 200 for reset

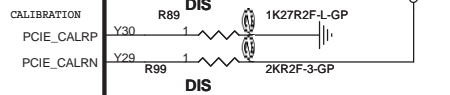


CLOCK  
 PCI\_E\_REFCLKP  
 PCI\_E\_REFCLKN

NC#AJ21  
 NC#AK21  
 NC\_PWRGOOD

PERST#  
 M92-M2-GP  
 DIS

71.M92M2.M01 Change to 71.M92M2.M02



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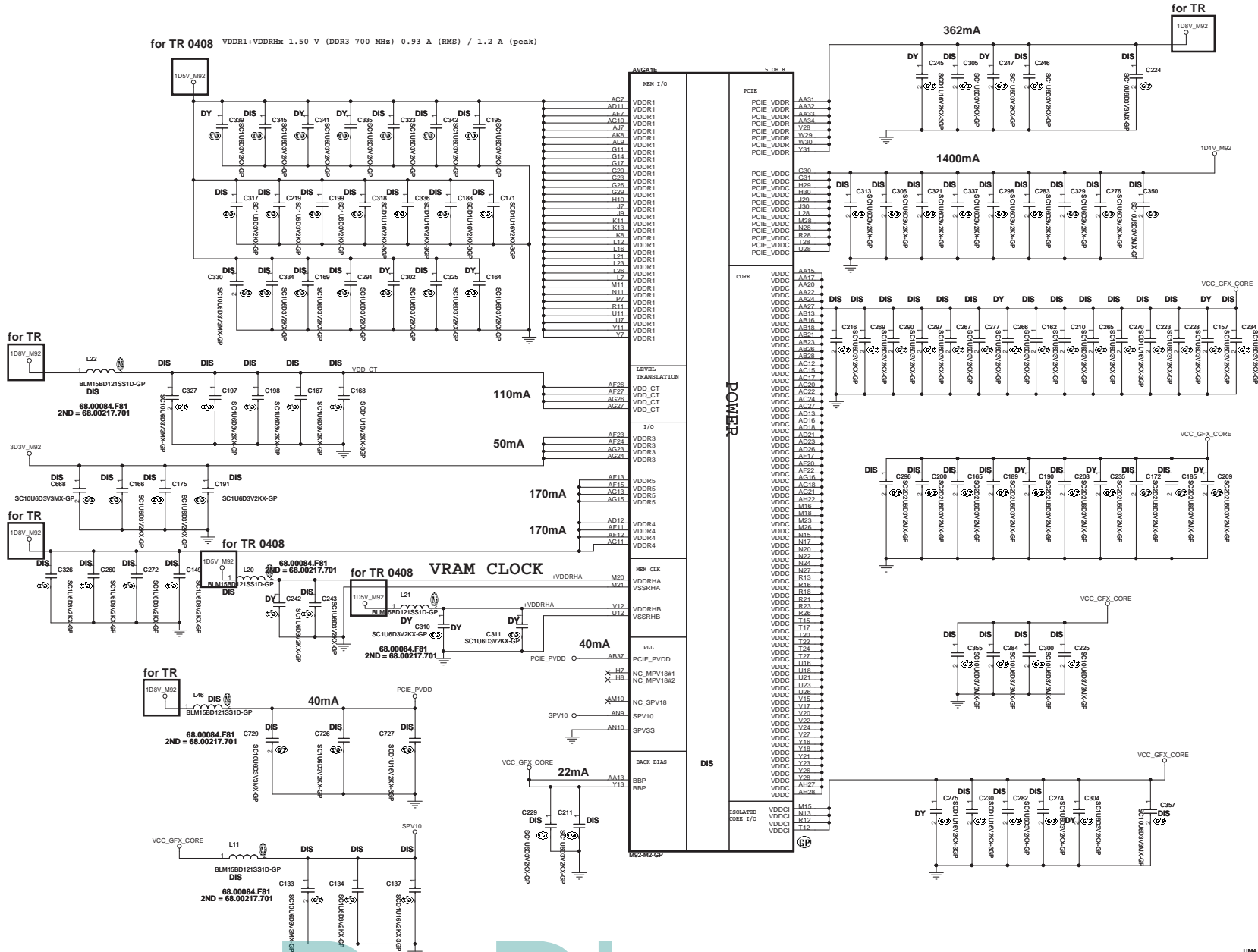
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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

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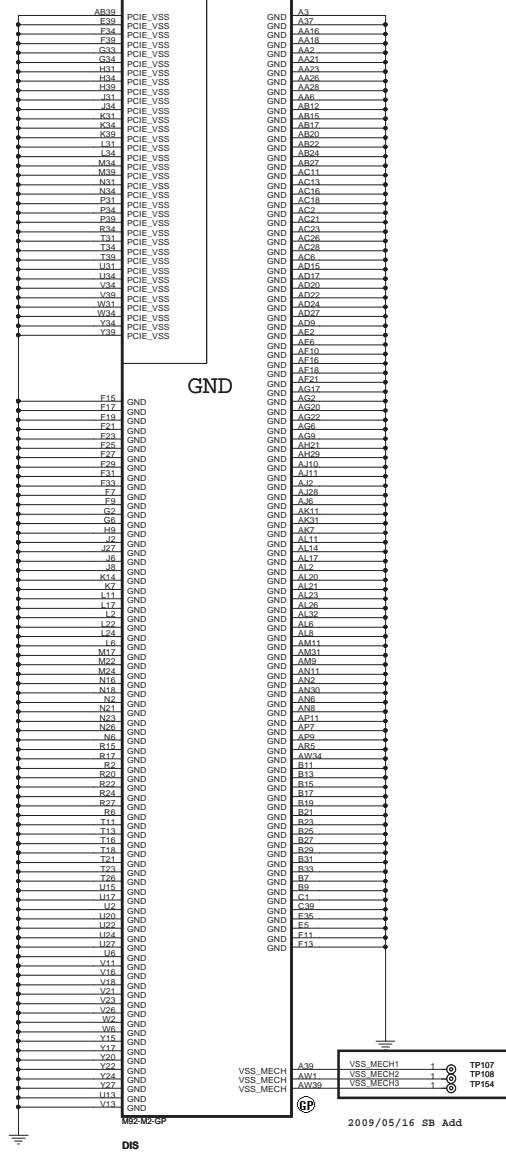
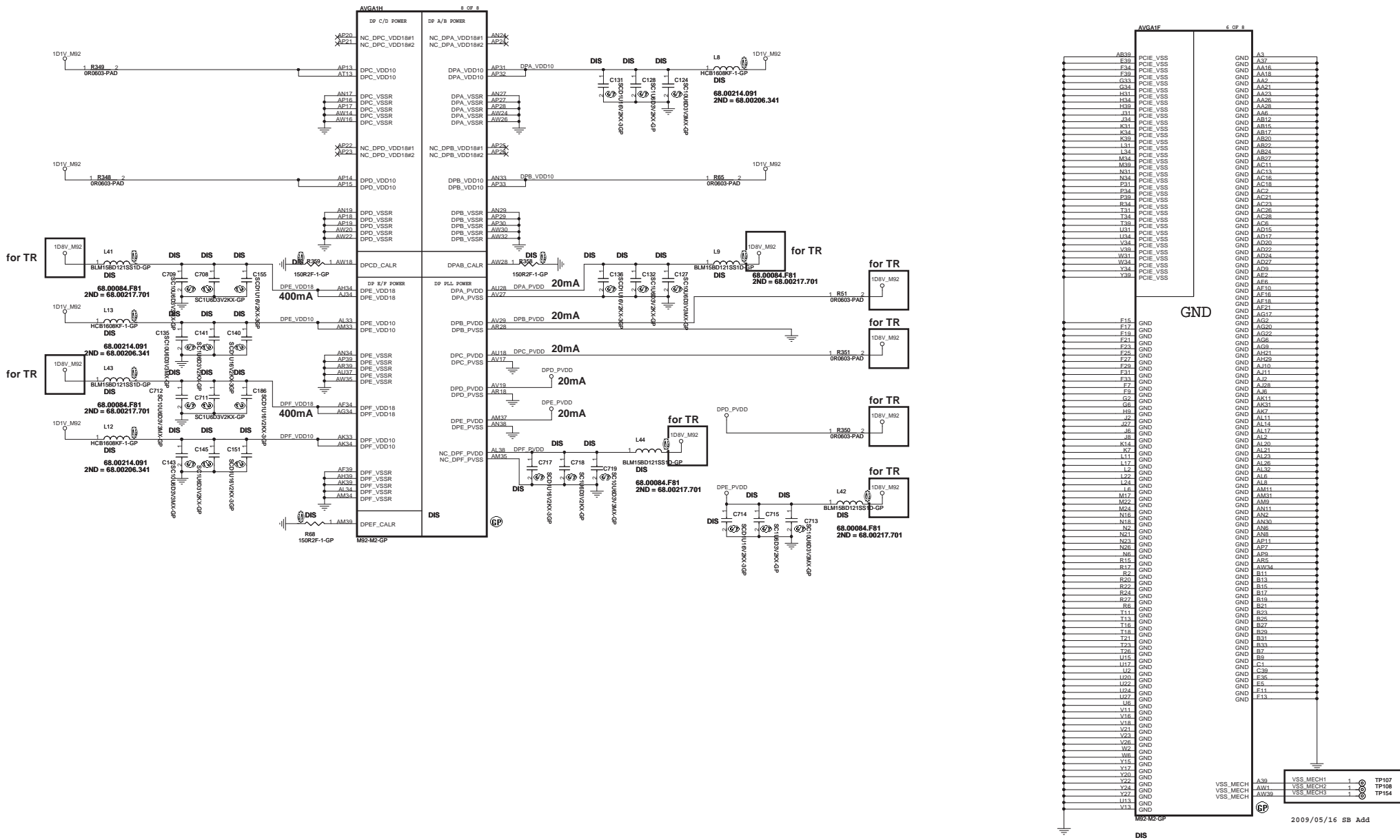
Size A3 Document Number **JV71-TR** Rev **SB**

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File: **DP POWER\_GND**

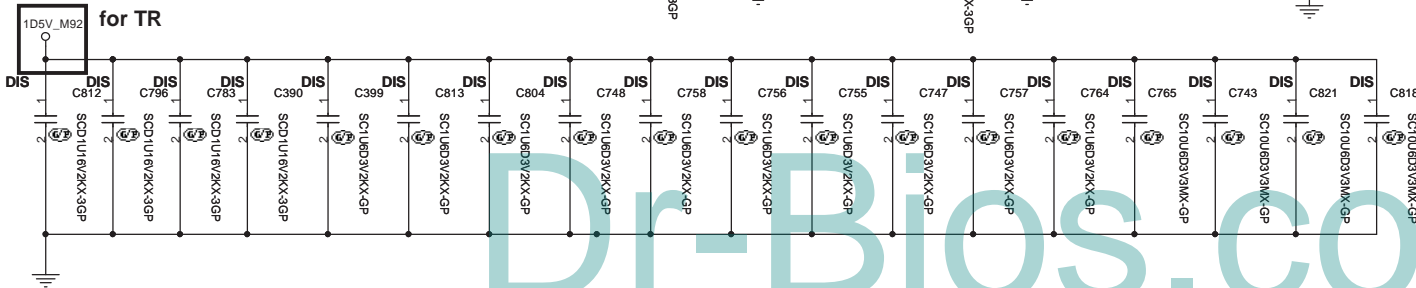
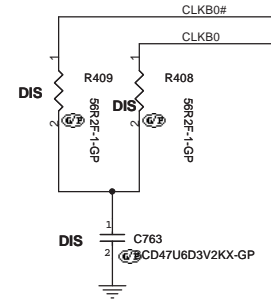
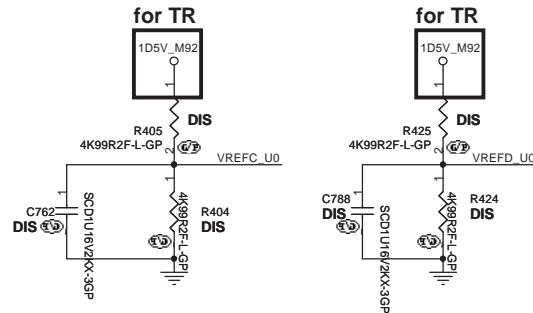
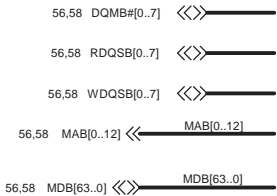
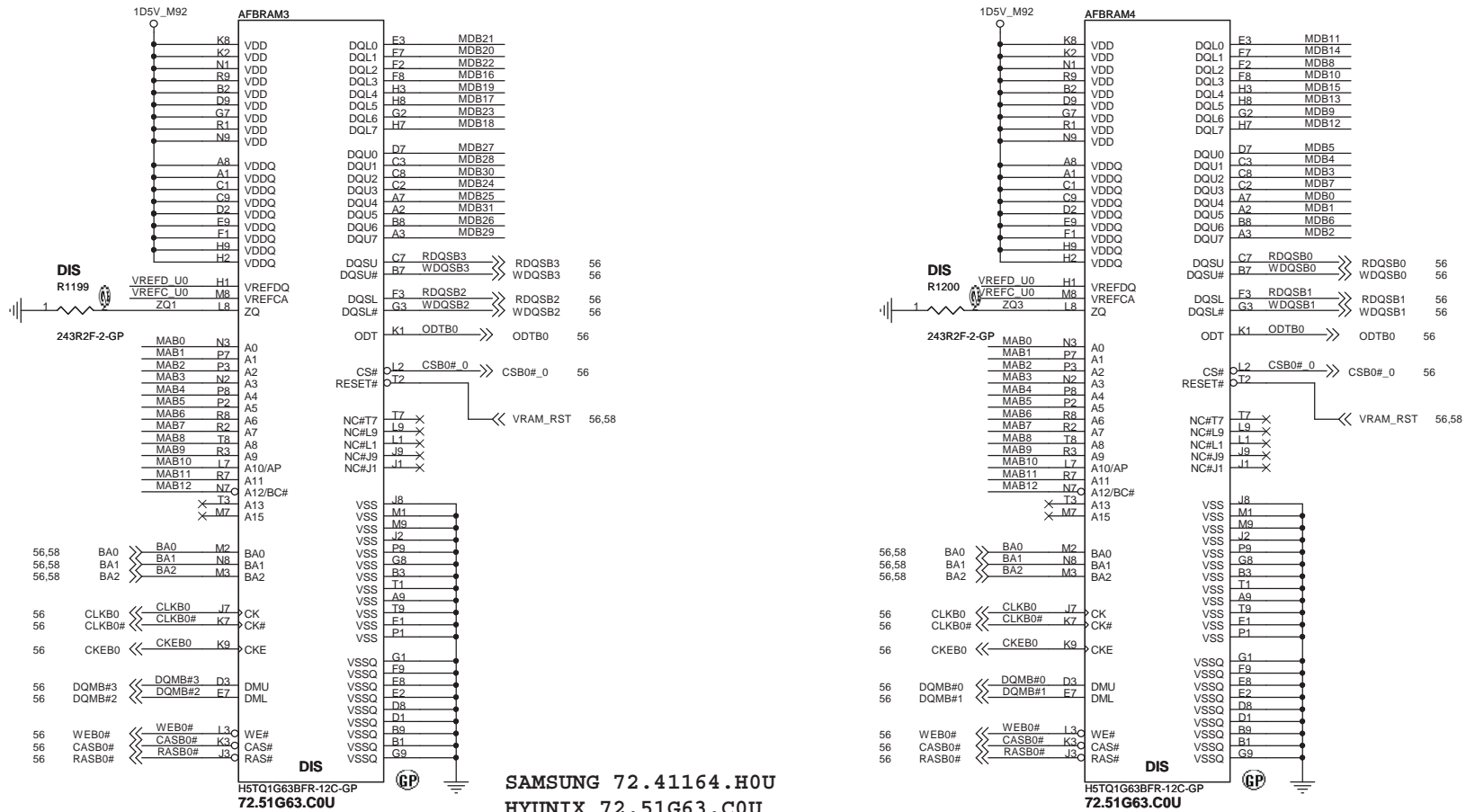
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# DDR3



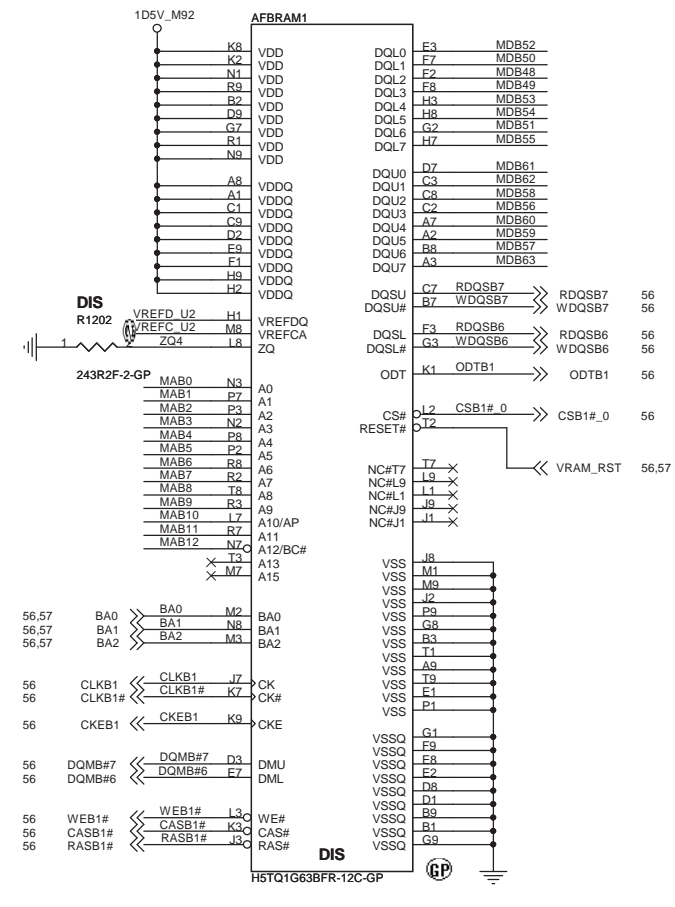
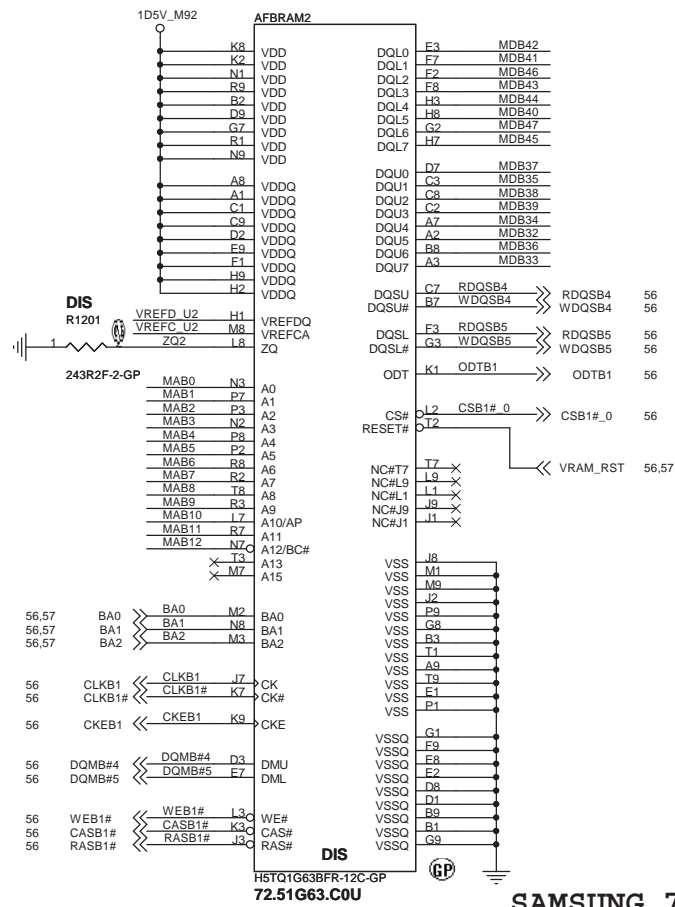
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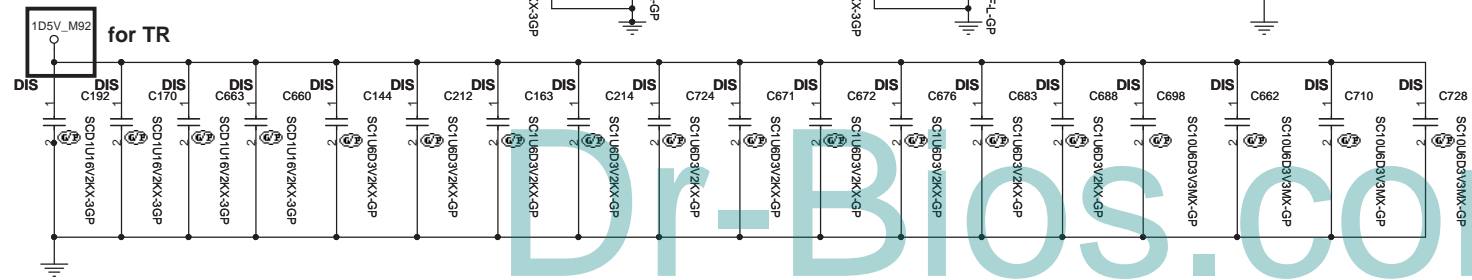
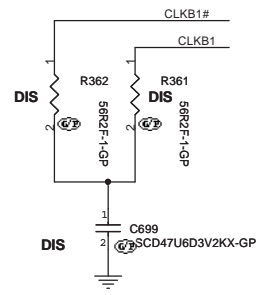
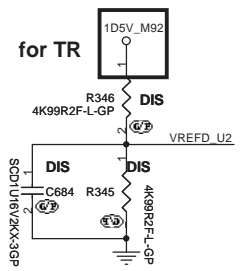
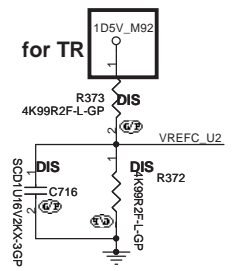
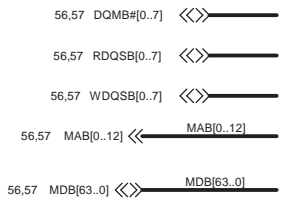
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HYUNIX 72.51G63.C0U



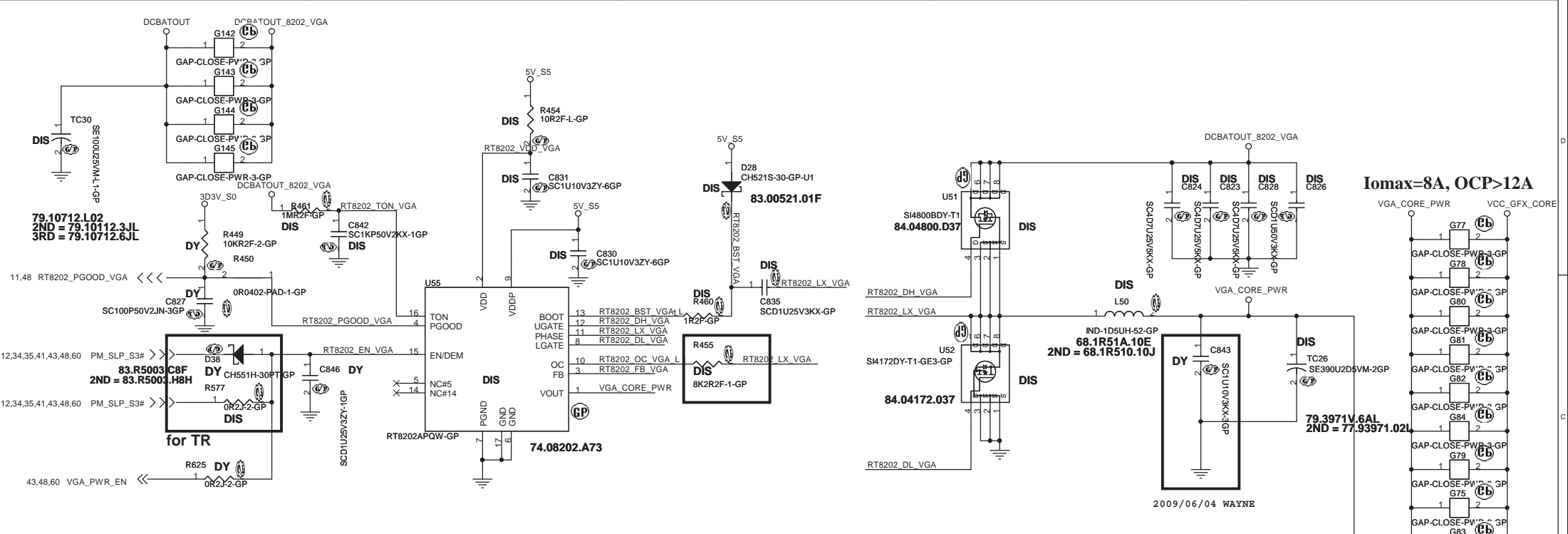
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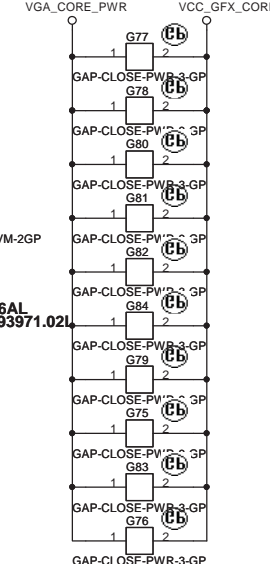
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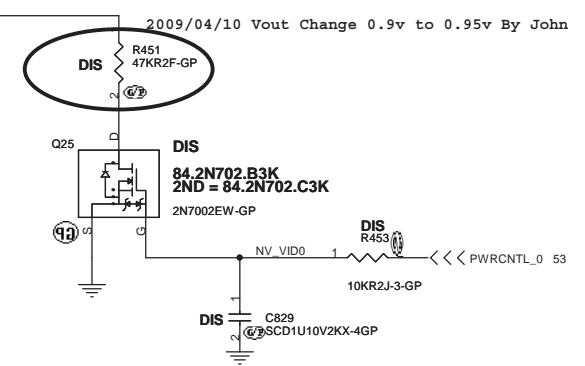
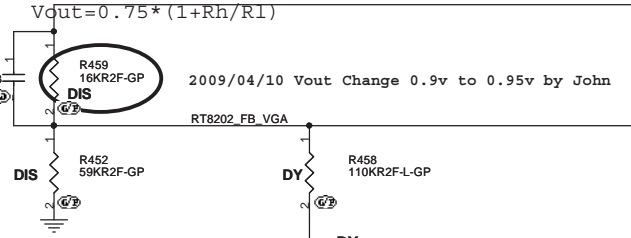
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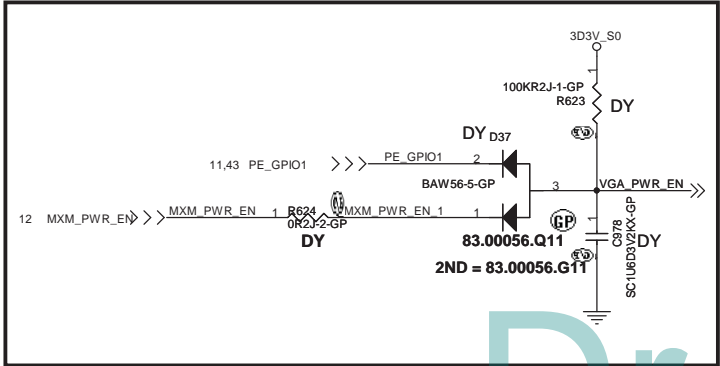
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2009/06/04 WAYNE

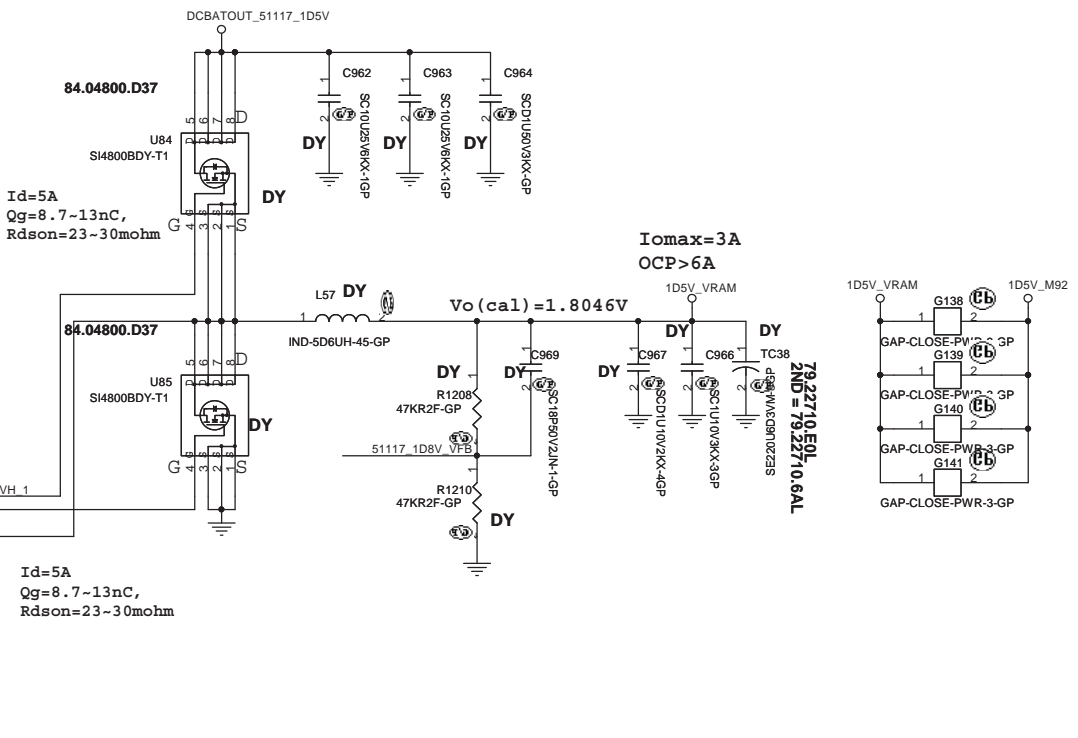
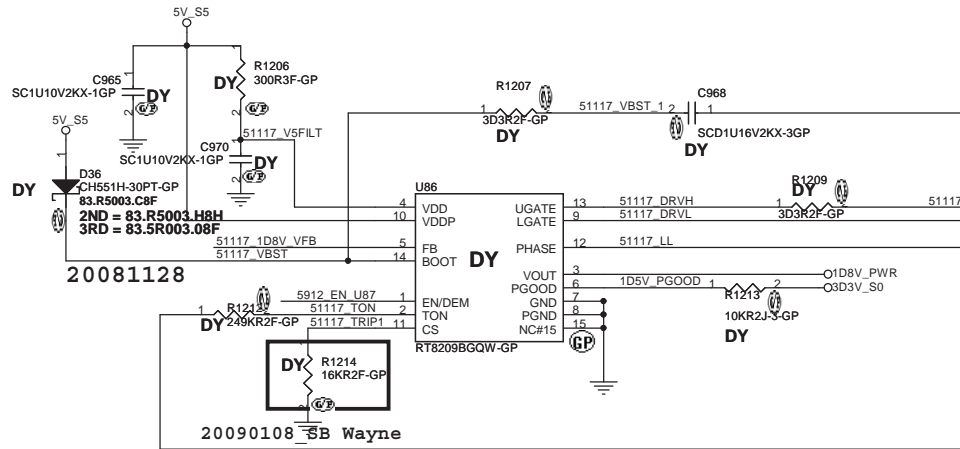
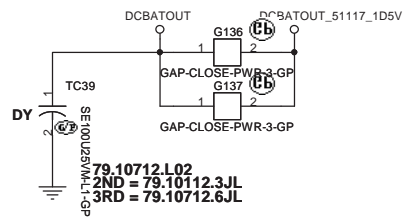


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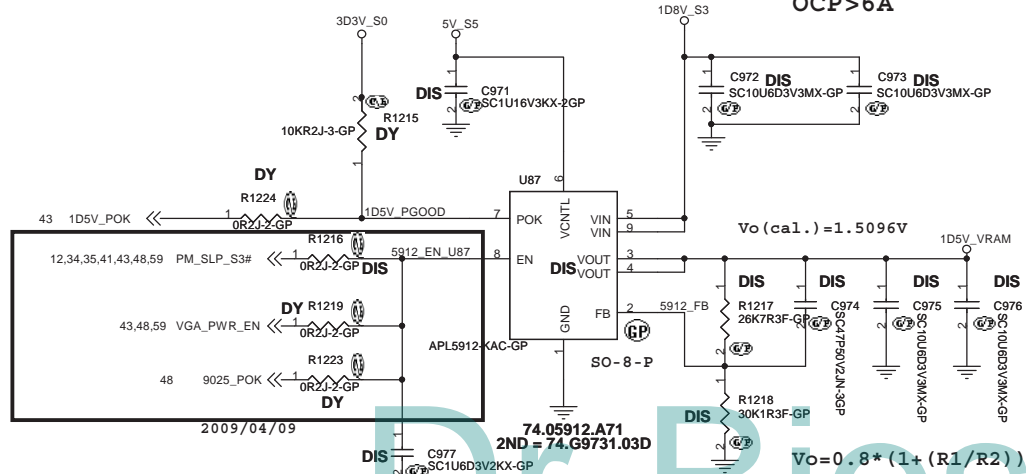


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Title: <b>RT8202A VGA CORE</b>	
Size: A3	Document Number: <b>JV71-TR</b>
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Taipei Hsien 221, Taiwan, R.O.C.

Title <b>RT8209B/APL5912_1D5V_VRAM</b>		
Size A3	Document Number <b>JV71-TR</b>	Rev <b>SA</b>
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