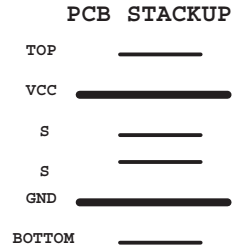
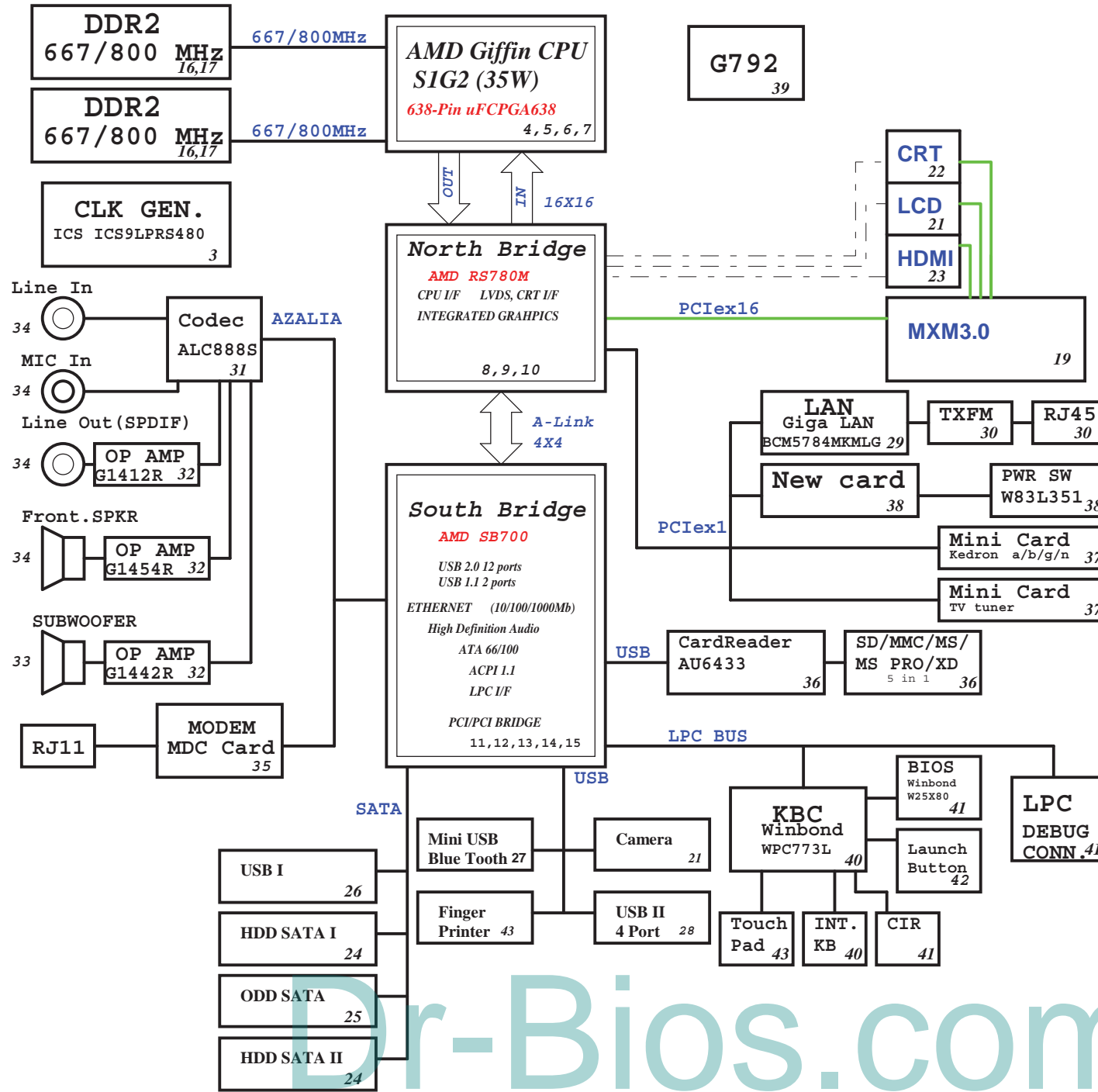


JM70-PU (AS 17") Block Diagram

Project code: 91.4CE01.001
 PCB P/N : 48.4CE01.0SC
 REVISION : 08255-SC



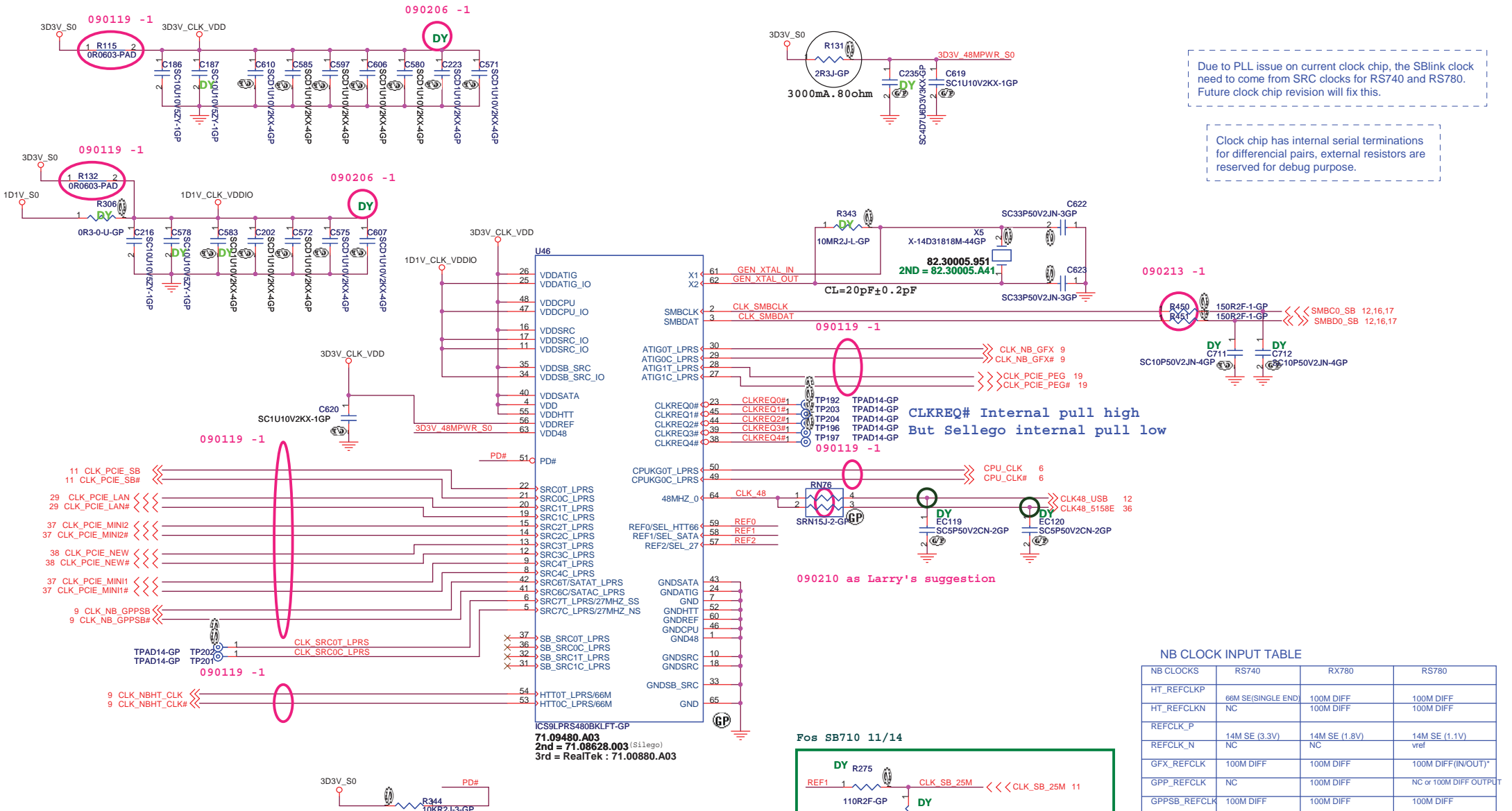
SYSTEM DC/DC TPS51125 49	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (7A)
	3D3V_S5 (7A)
SYSTEM DC/DC TPS51124 50	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0 (8A)
	1D2V_S0 (5A)
SYSTEM DC/DC TPS51117 52	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 (10A)
RT9026PFP 51	
1D8V_S3	DDR_VREF_S3
	0D9V_S3 (1A)
RT9166 51	
3D3V_S0	2D5V_S0 (300mA)
G957 51	
3D3V_S0	1D5V_S0 (1A)
G9161 (UMA) 51	
3D3V_S5	1D2V_S5 (400mA)
G9131 (DIS) 51	
3D3V_S5	1D2V_S5 (300mA)
CHARGER MAX8731A 53	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR
	1.8V 6.0A
	UP+5V
	5V 100mA
CPU DC/DC ISL6265HR 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0
	0~1.55V 18A
	VCC_CORE_S0_1
	0~1.55V 18A
	VDDNB
	0~1.55V 18A

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Title	
HISTORY	
Size	Document Number
A3	JM70-PU
Date: Monday, March 02, 2009	Sheet 2 of 56
	Rev -2



Due to PLL issue on current clock chip, the SBLink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

CLKREQ# Internal pull high
But Sellego internal pull low

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0*	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0*	100MHz differential HTT clock

CPU_CLK (200MHz)

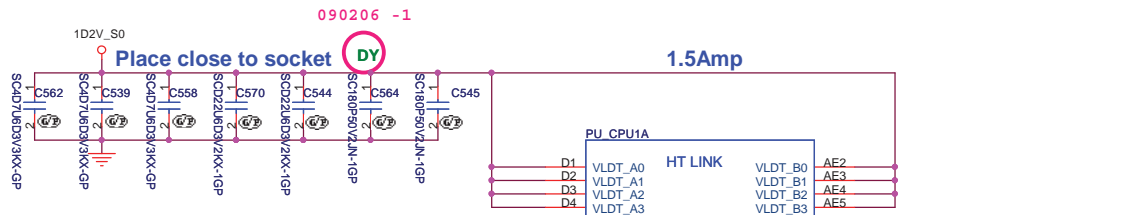


OSC 14M NB
RS780M 1.1V 158R/90.9R

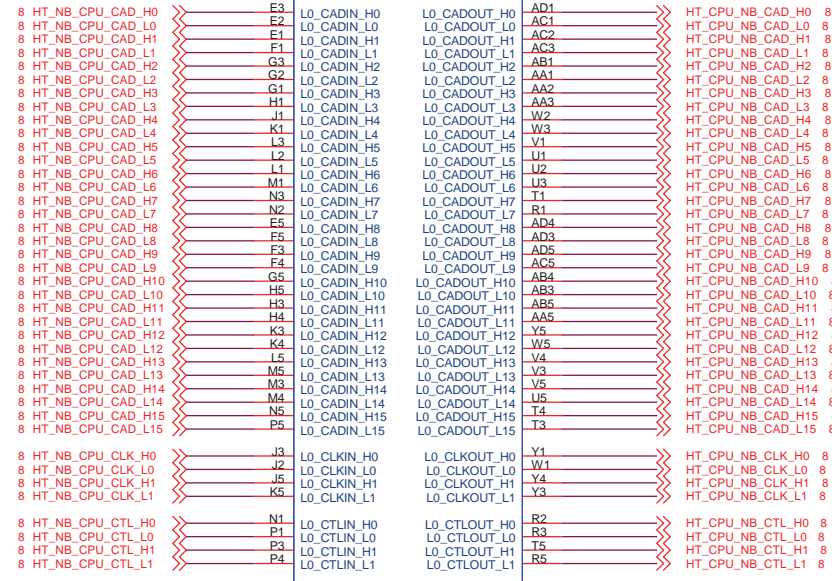
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Title	CLKGEN_ICS9LPRS480	
Size	Document Number	Rev
A3	JM70-PU	-2
Date:	Friday, March 06, 2009	Sheet 3 of 56



State	Specification	Notes	ZM200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V



62-10055-111
ZND = 62.10055.251
090109 SC
SKT-BGA638H176

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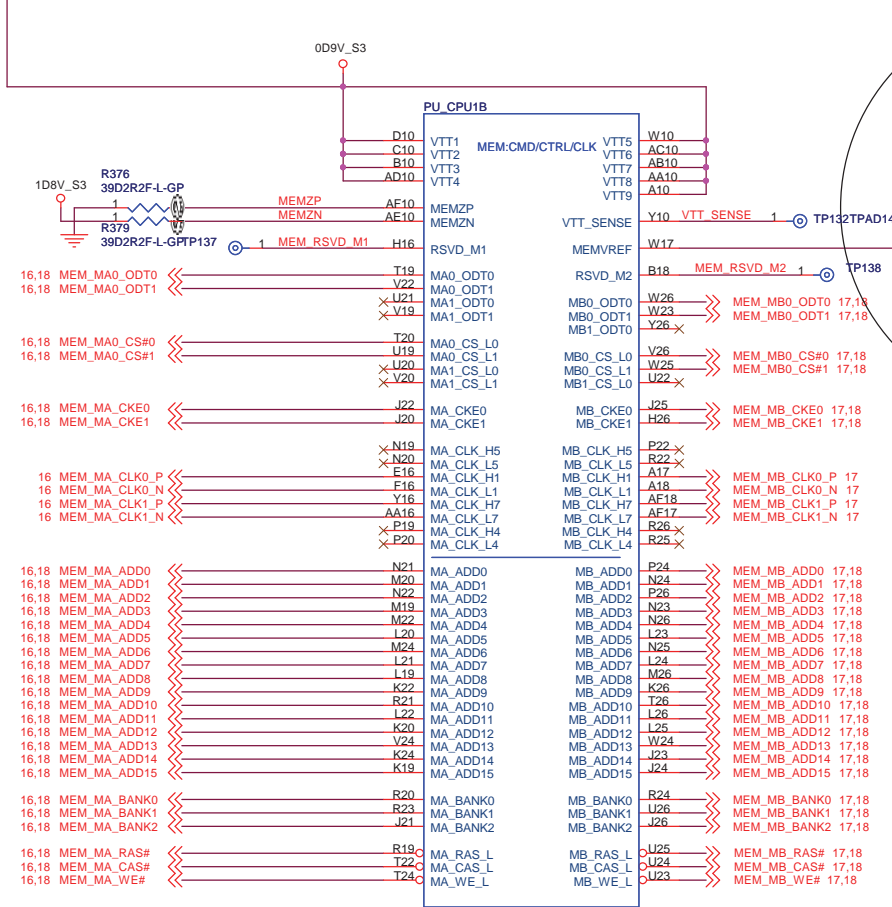
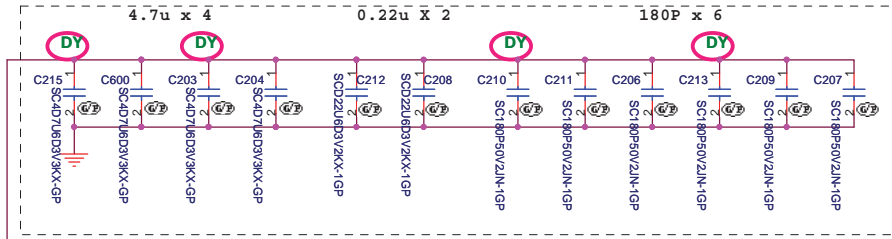
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Size: **A3** Document Number: **JM70-PU** Rev: **-2**

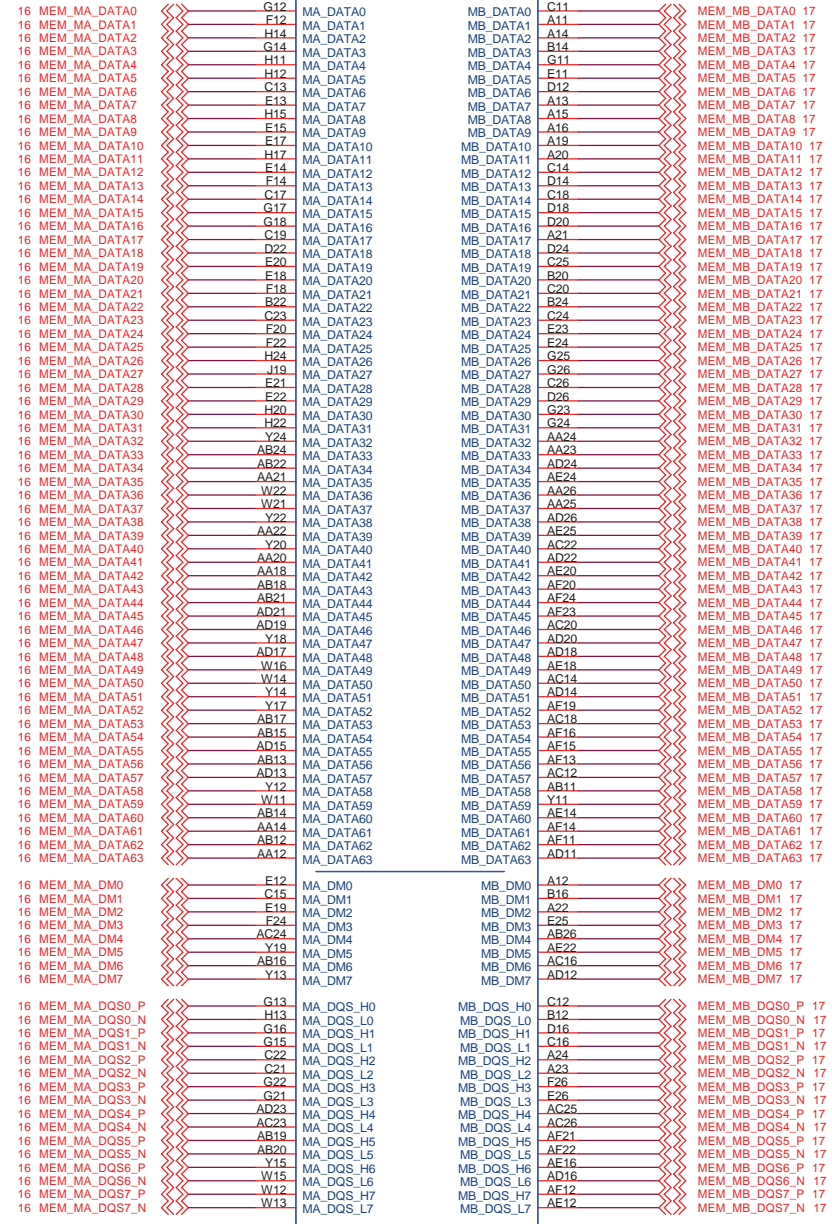
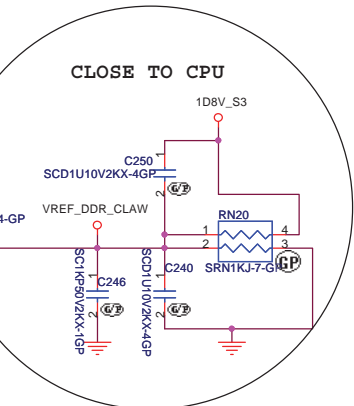
Date: Friday, March 06, 2009 Sheet 4 of 56

090206 -1

Place near to CPU



CLOSE TO CPU



62-10055-111
2ND = 62.10055-251

62.10055.111
2ND = 62.10055.251

090109 SC

090109 SC

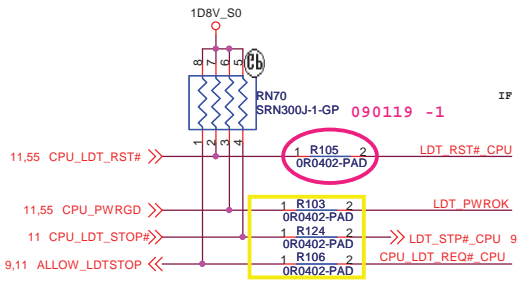
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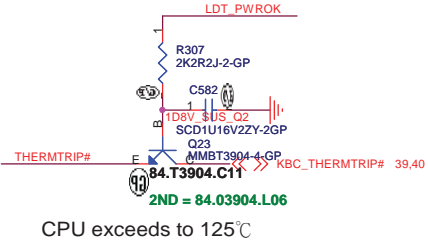
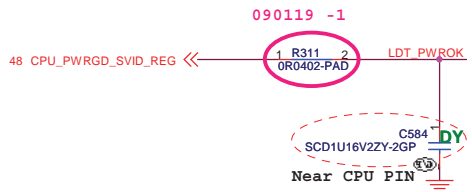
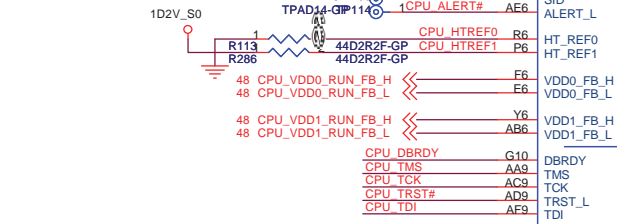
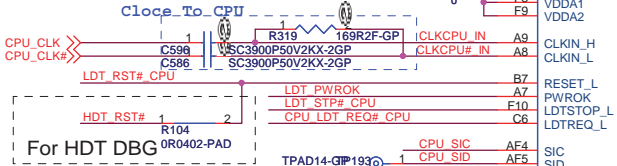
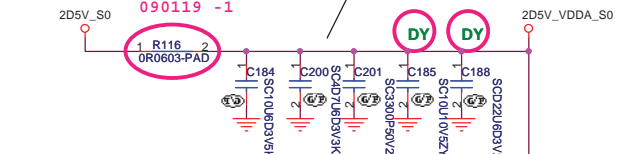
Title			CPU_DDR (2/4)		
Size	Document Number		Rev		
A3	JM70-PU		-2		
Date:	Friday, March 06, 2009	Sheet	5	of	56

LYAOUT:ROUTE VDDA TRACE APPROX.
40 mils WIDE
(USE 2X25 mil TRACES TO EXIT BALL FIELD)
& 500 mils LONG.

The Processor has reached a preset maximum operating temperature. 100°C
I=Active HTC
O=FAN

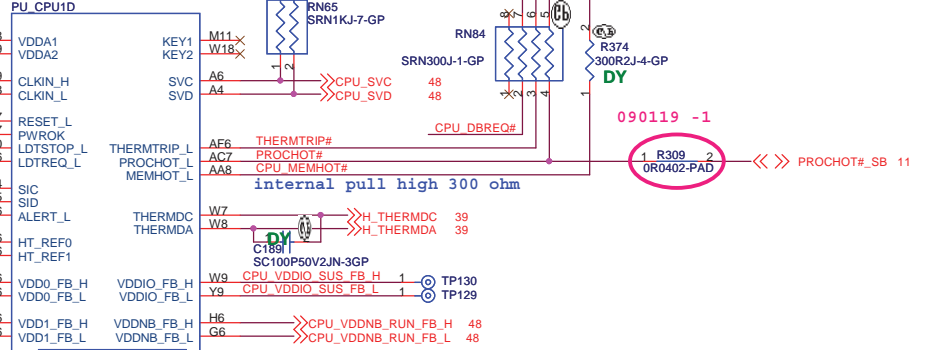
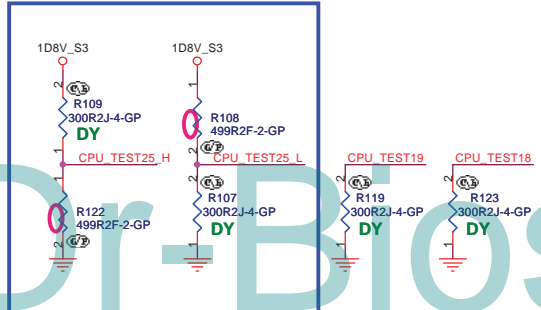


IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491



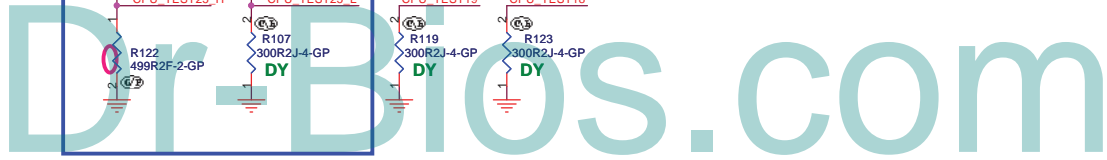
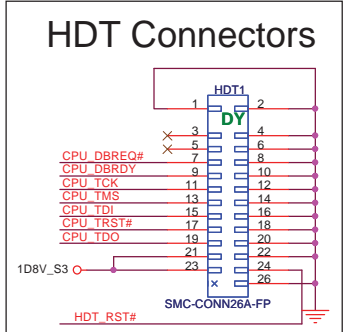
081223 SC

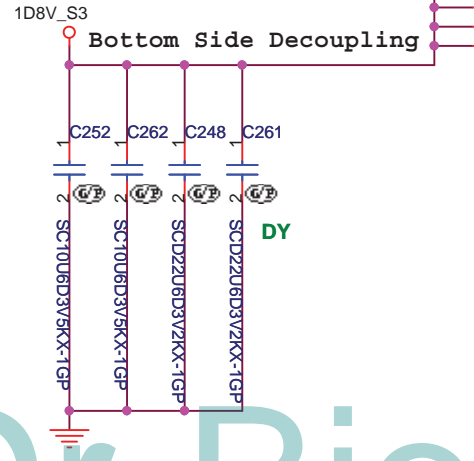
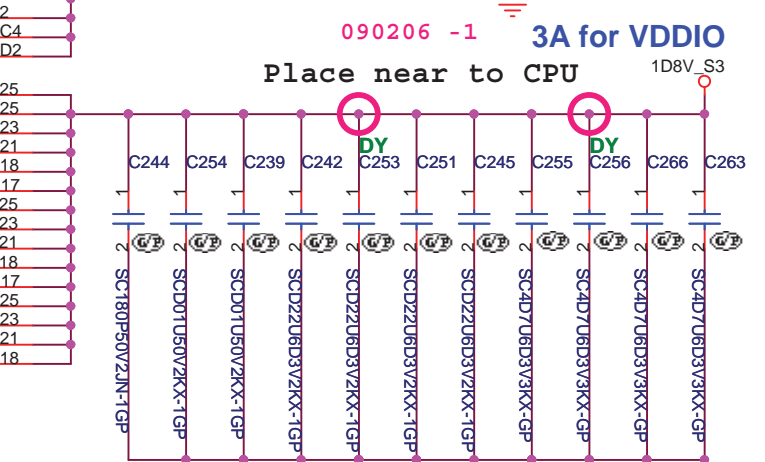
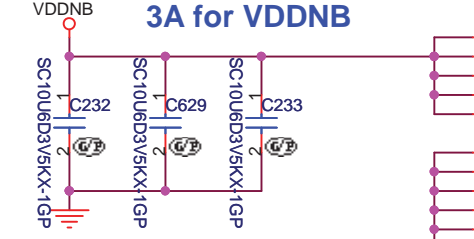
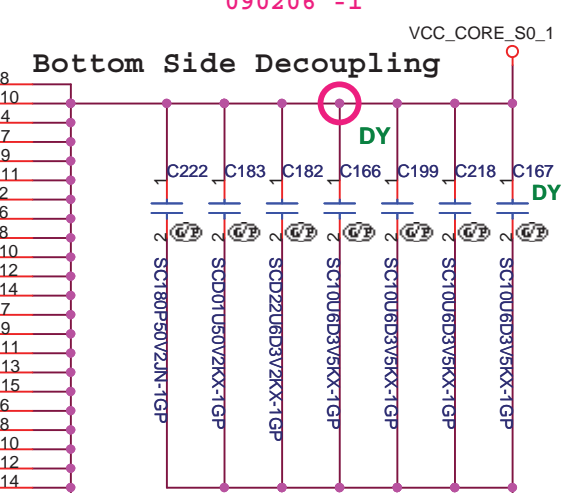
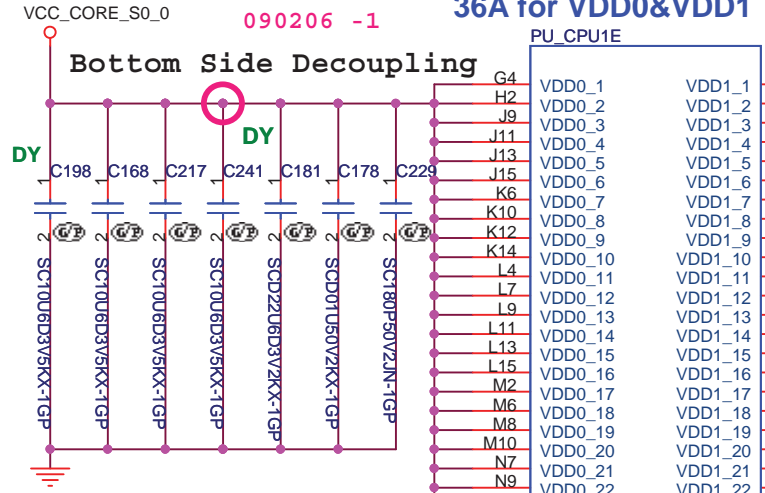
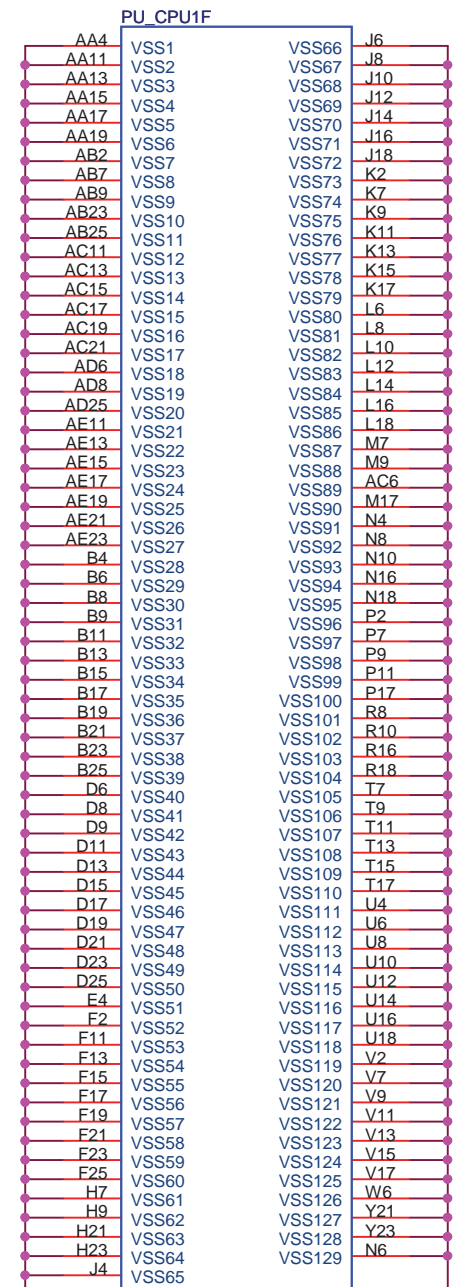
090113 -1



LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

62 10055 111
ZIND = 62.10055.251





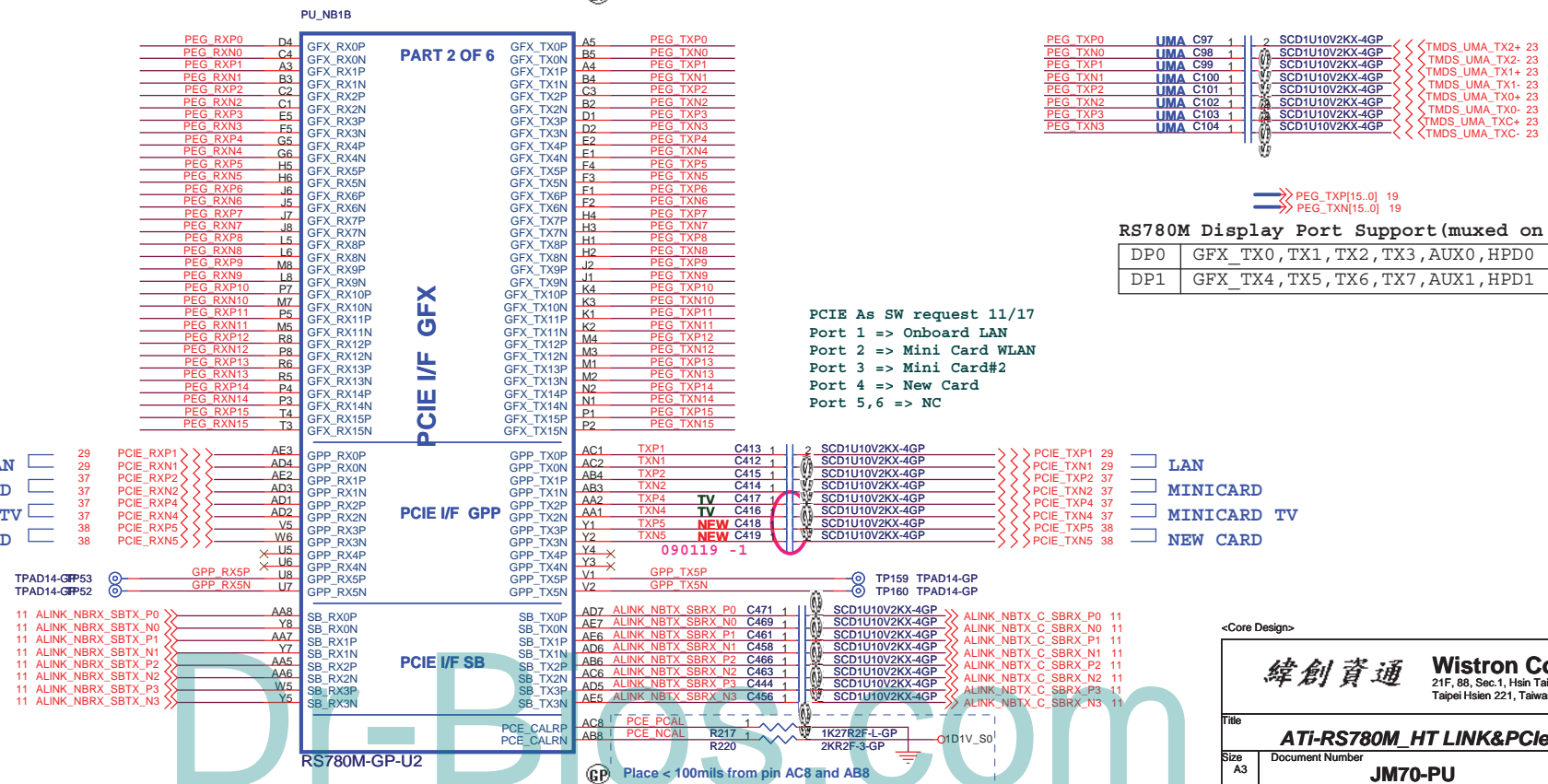
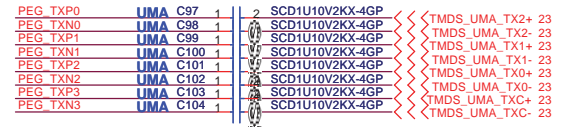
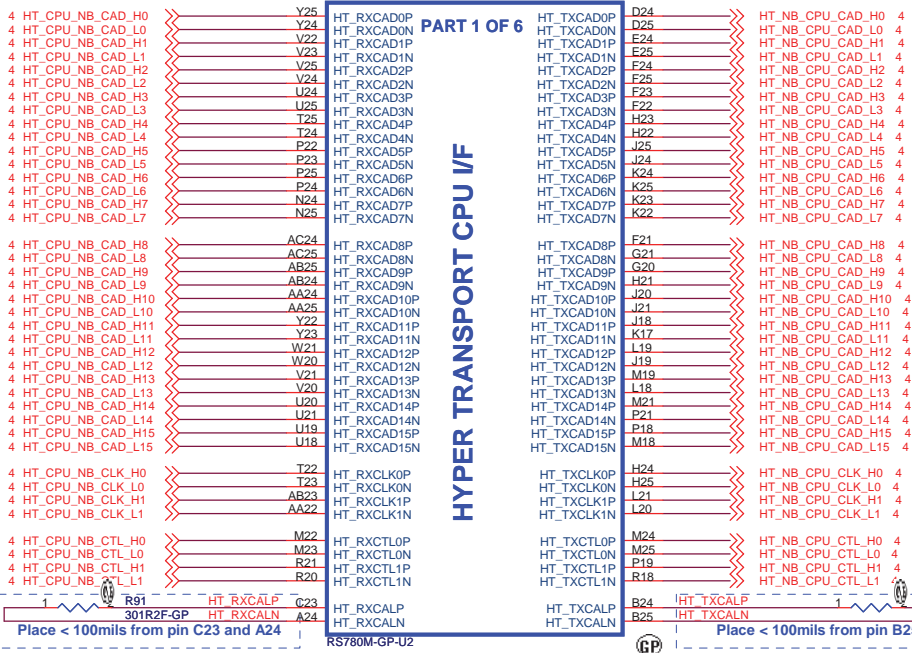
62.10055.111
2ND = 62.10055.251
090109 SC

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Title		CPU_Power_(4/4)	
Size	A4	Document Number	JM70-PU
Date:	Monday, March 02, 2009	Sheet	7 of 56

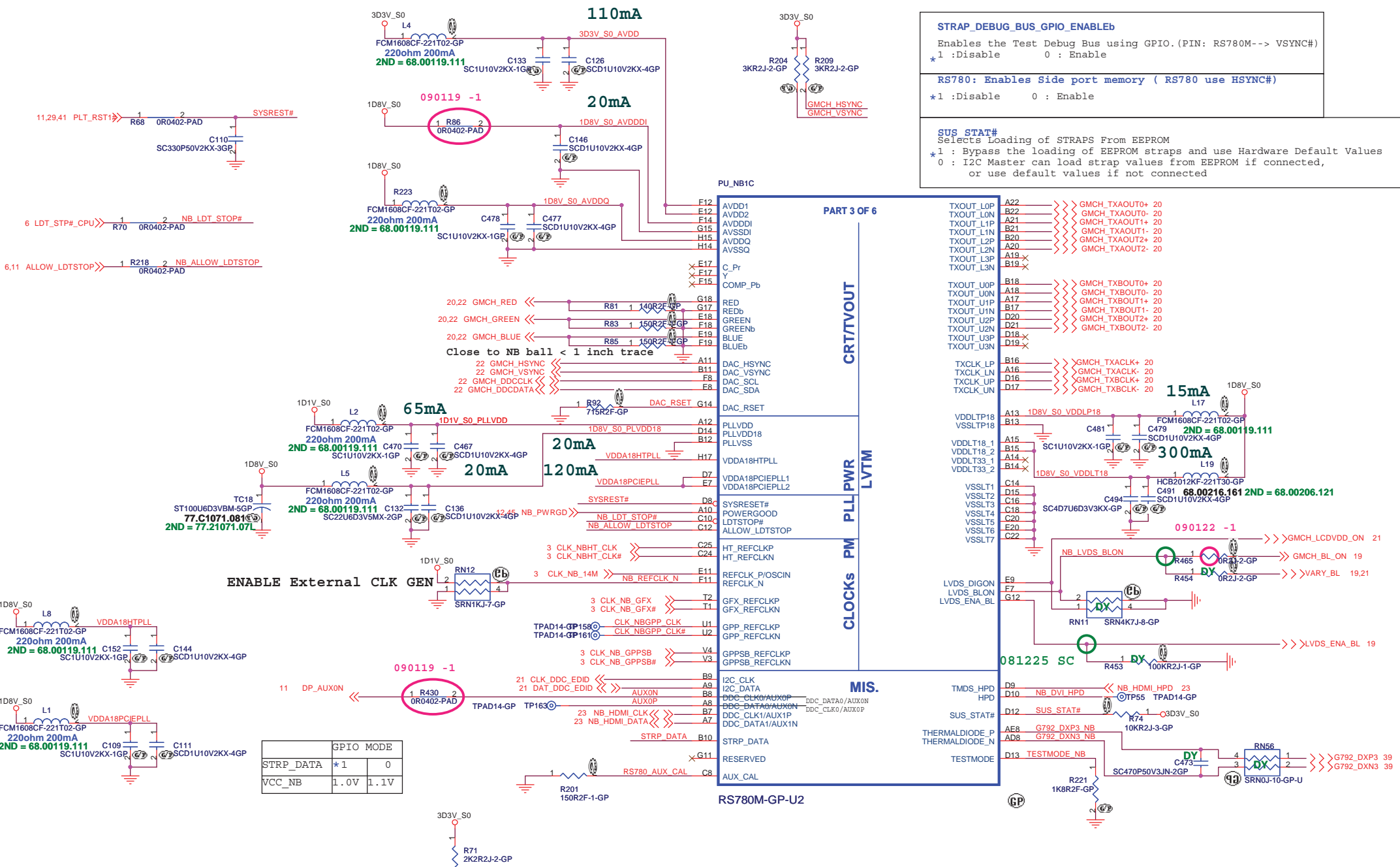


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File: **ATI-RS780M_HT LINK&PCIE(1/3)**

Size: A3 Document Number: **JM70-PU** Rev: -2

Date: Friday, March 06, 2009 Sheet 8 of 56

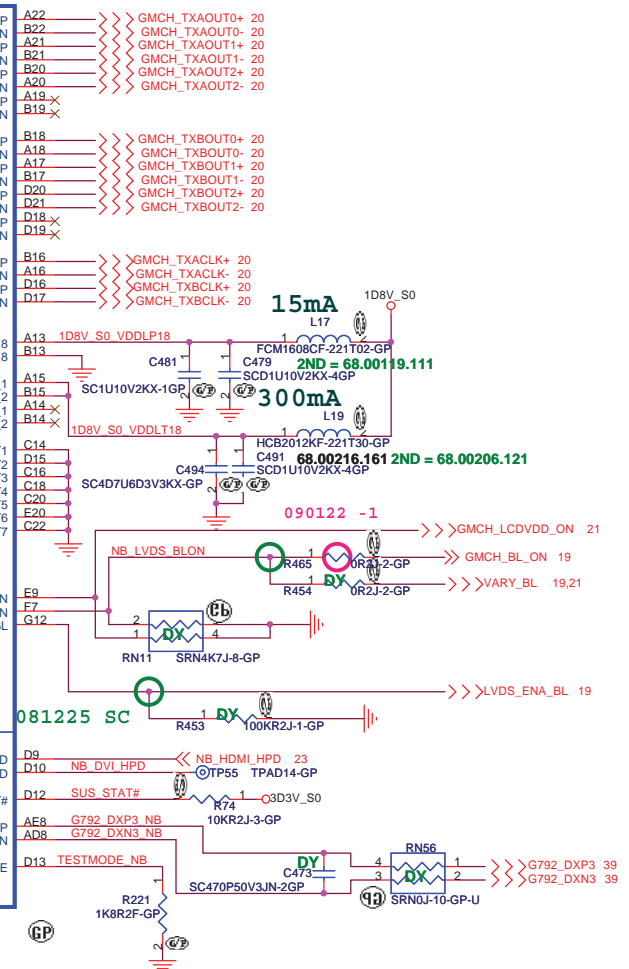


STRAP_DEBUG_BUS_GPIO_ENABLE#
 Enables the Test Debug Bus using GPIO. (PIN: RS780M--> VSYNC#)
 * 1 : Disable 0 : Enable

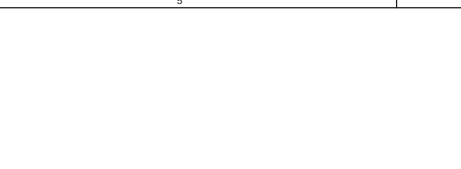
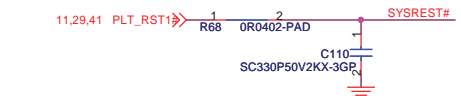
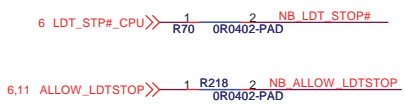
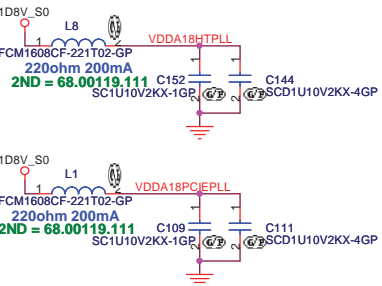
RS780: Enables Side port memory (RS780 use HSYNC#)
 * 1 : Disable 0 : Enable

SUS_STAT#
 Selects Loading of STRAPS from EEPROM
 * 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

	GPIO MODE	
STRP_DATA	*1	0
VCC_NB	1.0V	1.1V



ENABLE External CLK GEN

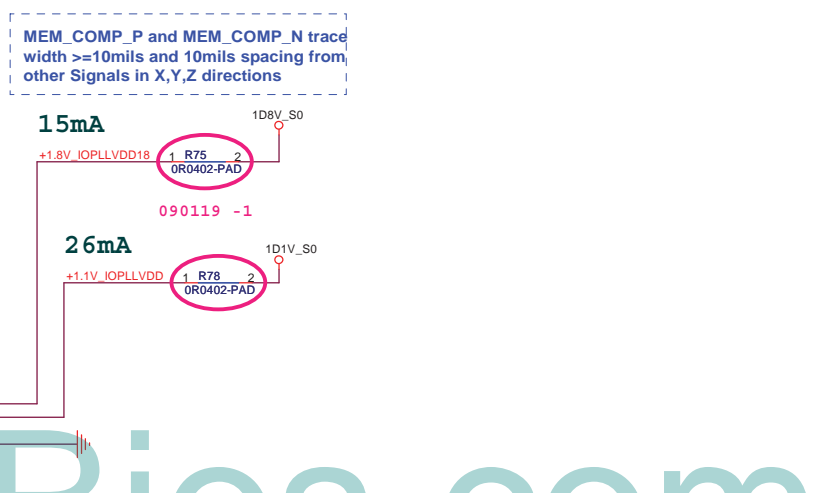
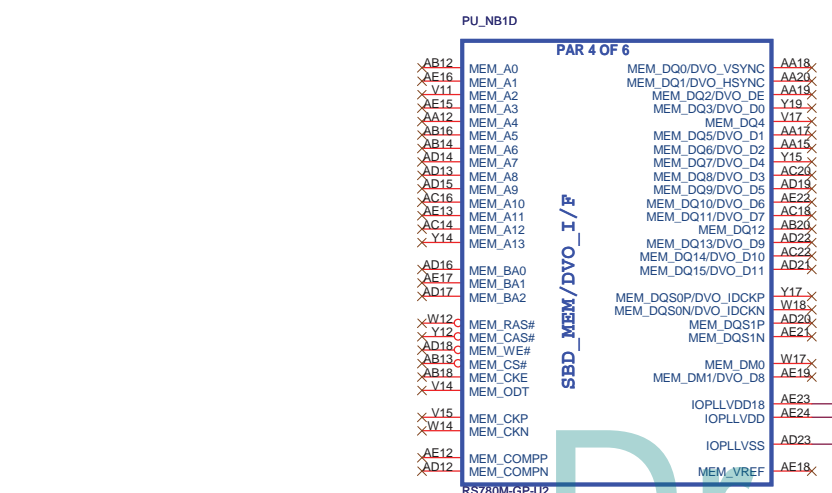
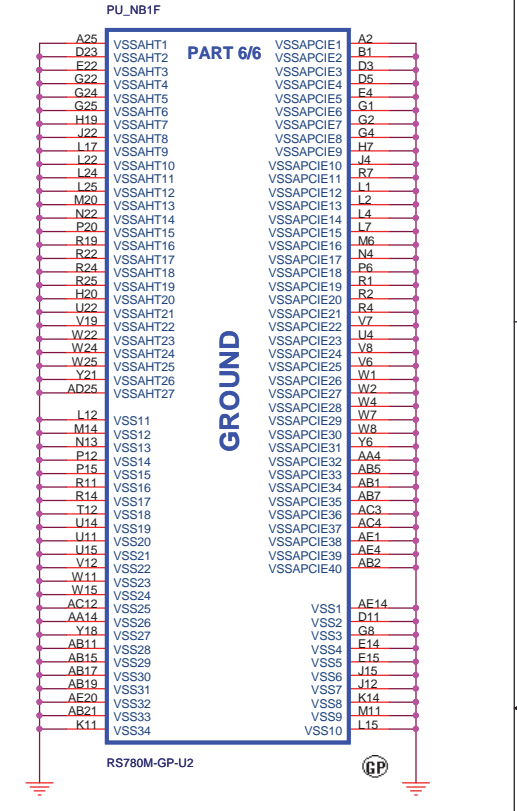
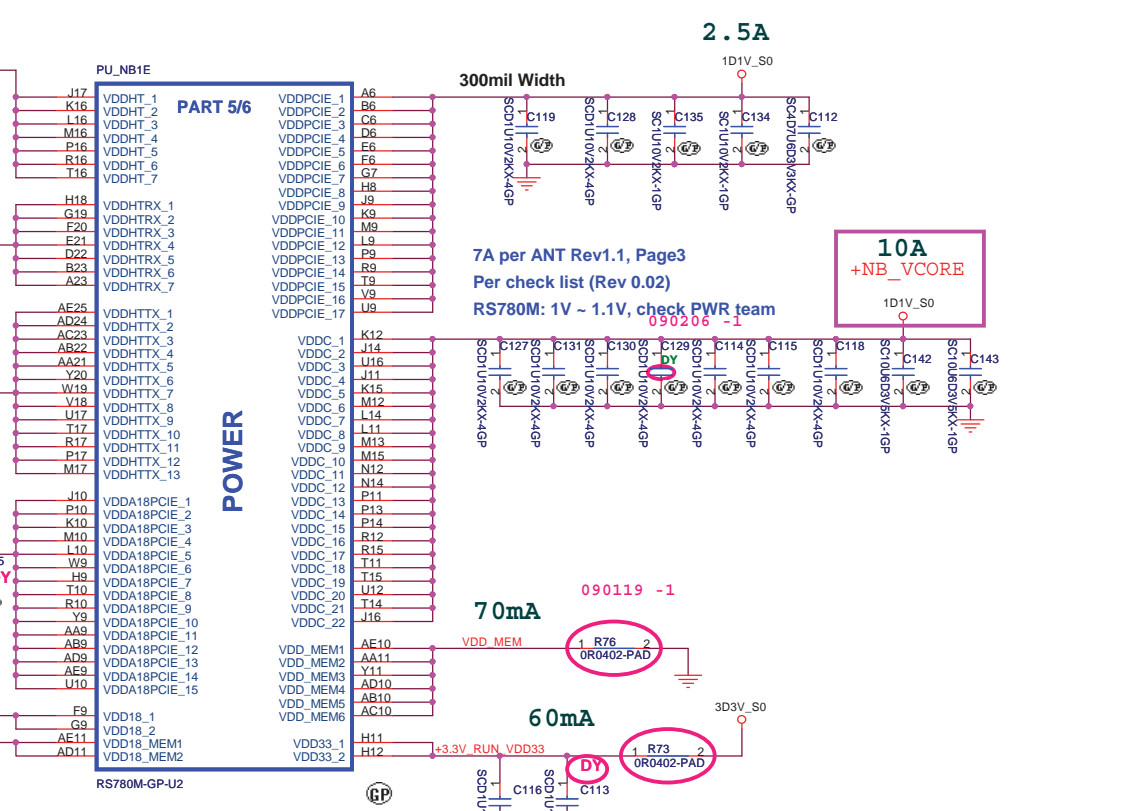
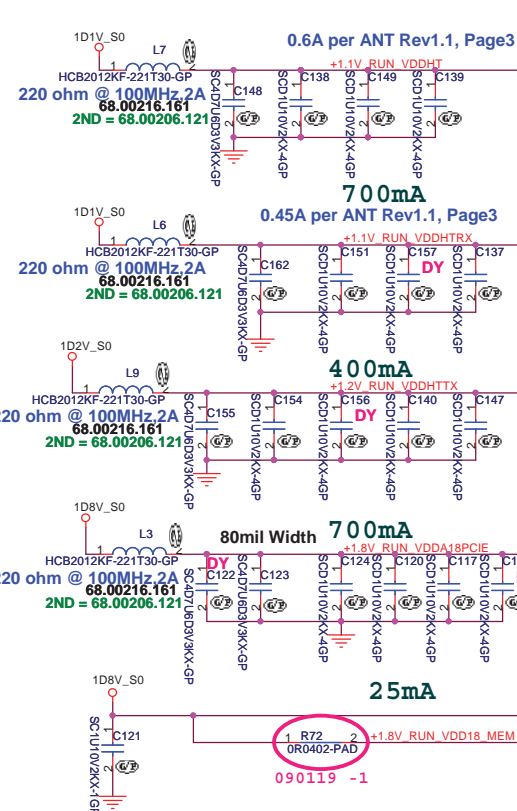


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Title: **ATI-RS780M_LVDS&CRT_(2/4)**

Size A3	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 9 of 56	



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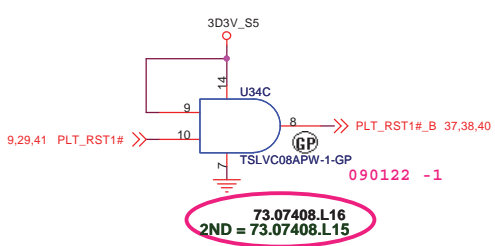
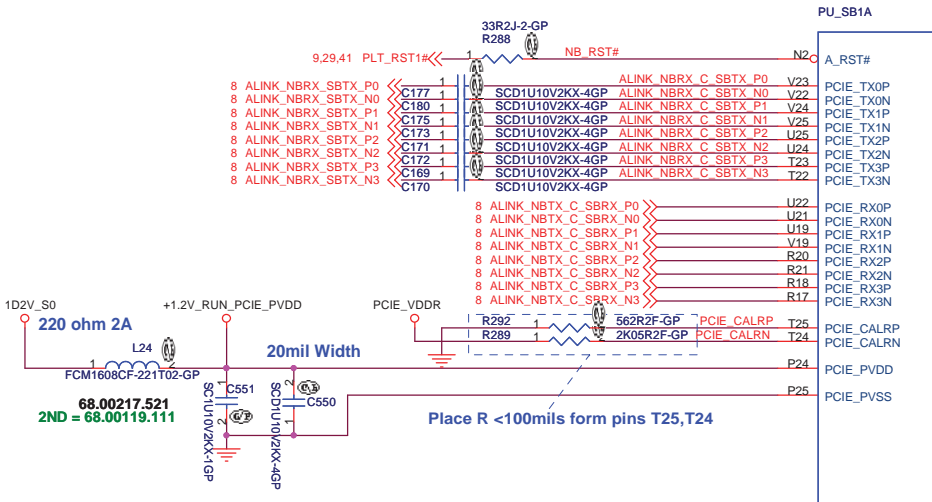
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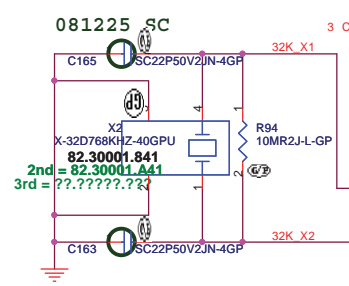
Title: **ATI-RS780M_Side Port&PWR&GND(3/3)**

Size: A3 Document Number: **JM70-PU** Rev: -2

Date: Monday, March 02, 2009 Sheet 10 of 56

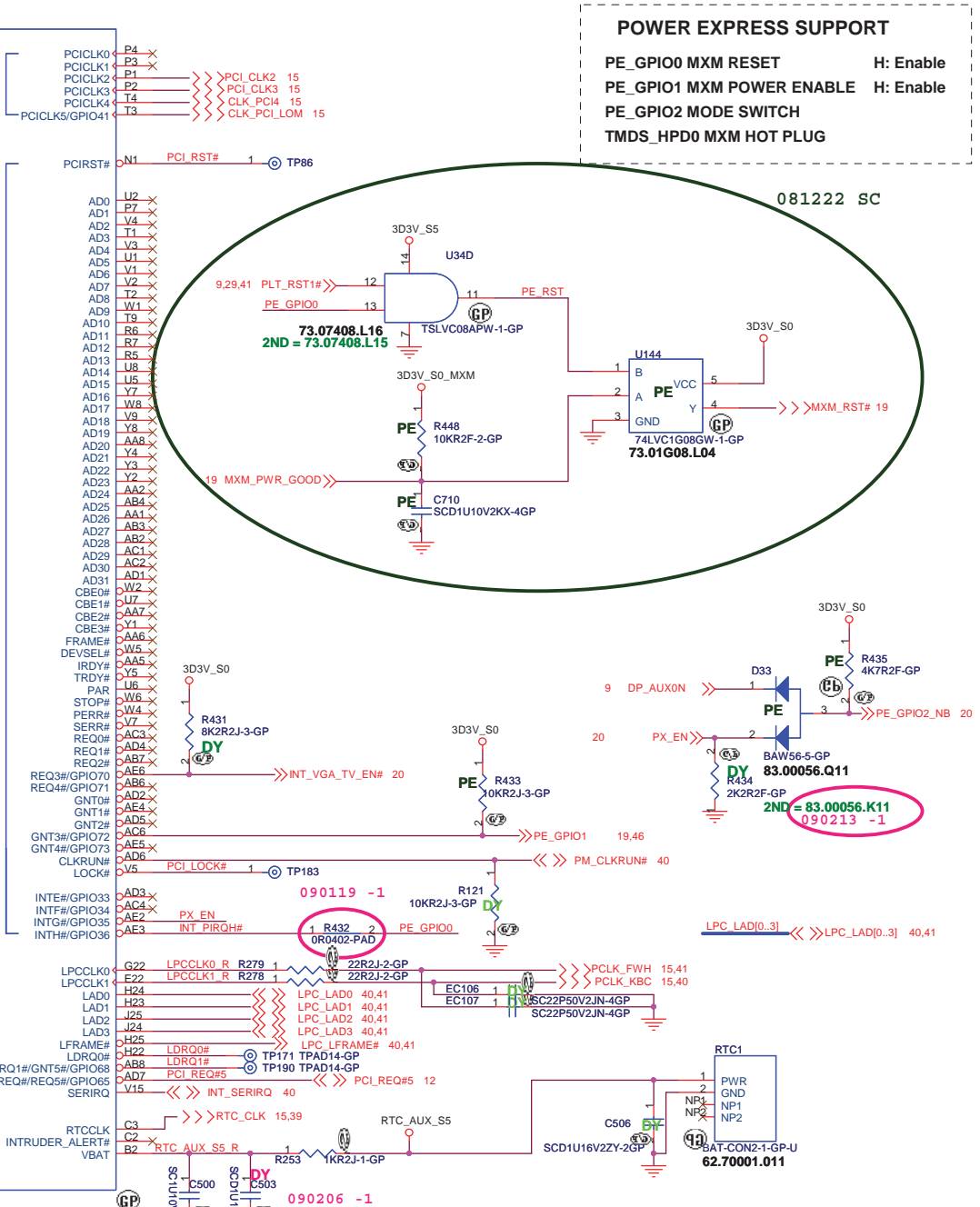


Fos SB710 11/14

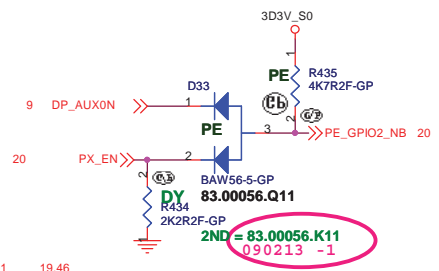
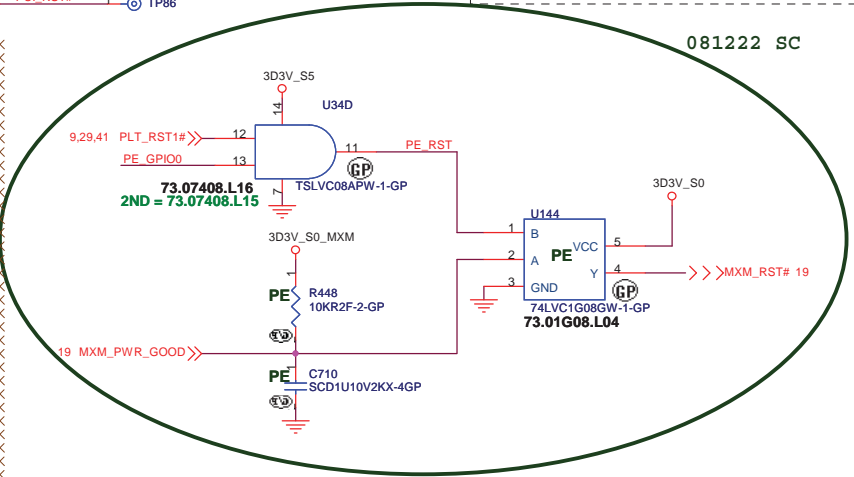


- 6.9 ALLOW_LDTSTOP << F23 ALLOW_LDTSTP
- 6 PROCHOT#_SB << F24 PROCHOT#
- 6.55 CPU_PWRGD << F22 LDT_PG
- 6 CPU_LDT_STOP# << G25 LDT_STP#
- 6.55 CPU_LDT_RST# << G24 LDT_RST#

PU_SB1A
SB700 Part 1 of 5
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC
CPU



POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMD5_HPDD0 MXM HOT PLUG



<Core Design>

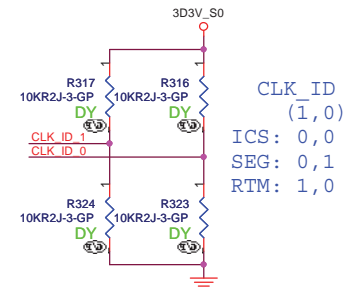
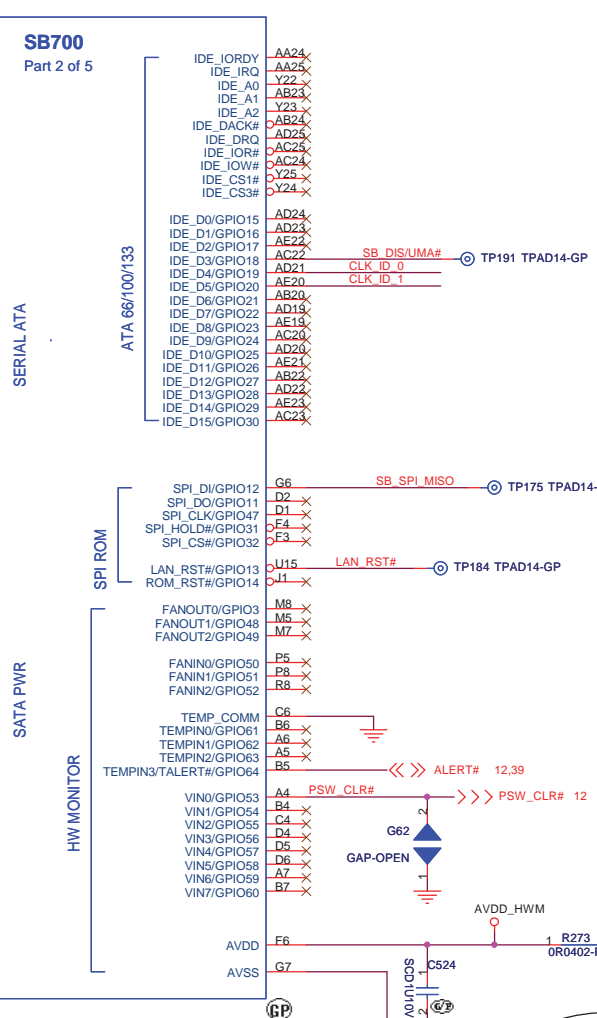
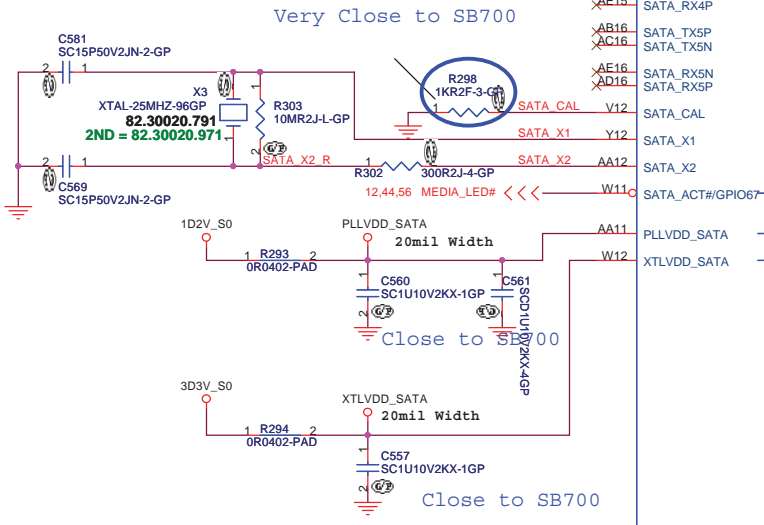
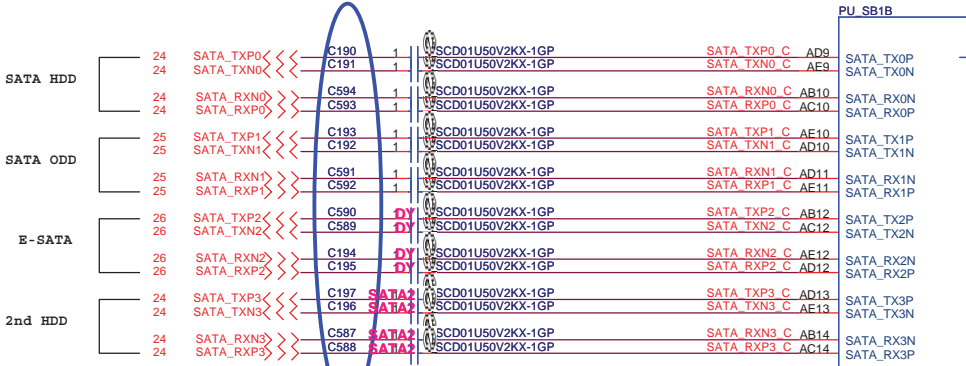
緯創資通 Wistron Corporation
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Title: **ATI-SB700_PCIE&PCI (1/5)**

Size A3	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 11	of 56

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PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700



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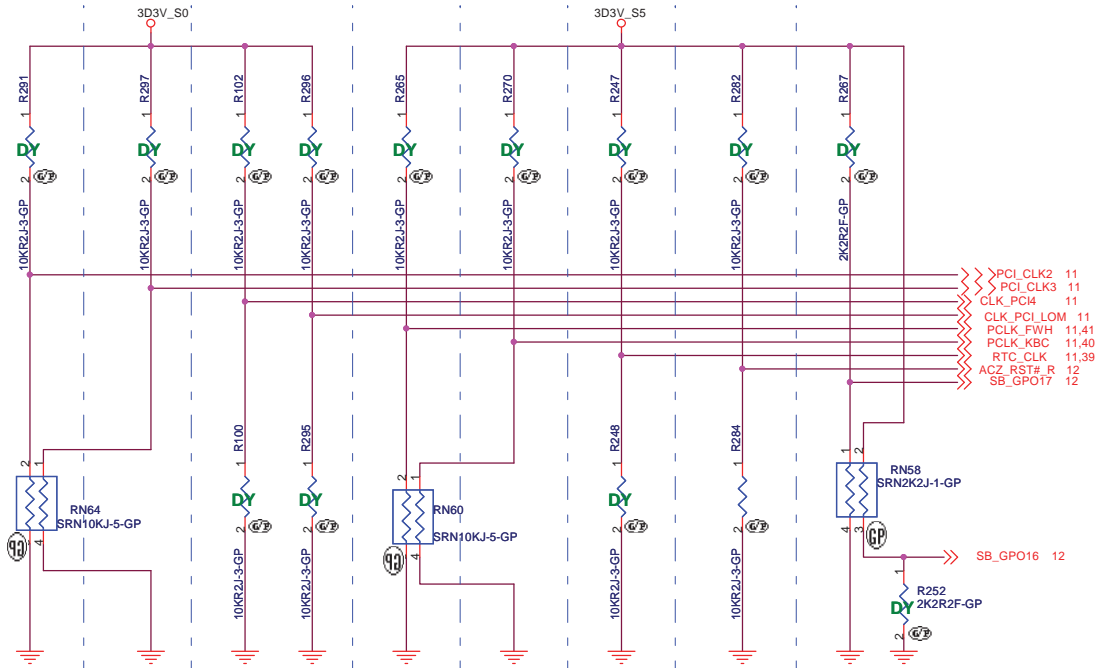
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB700 SATA-IDE (3/5)**

Size: **A3** Document Number: **JM70-PU** Rev: **-2**

Date: **Friday, March 06, 2009** Sheet: **13** of **56**

REQUIRED STRAPS REQUIRED SYSTEM STRAPS



DEBUG STRAPS

	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	Reserved

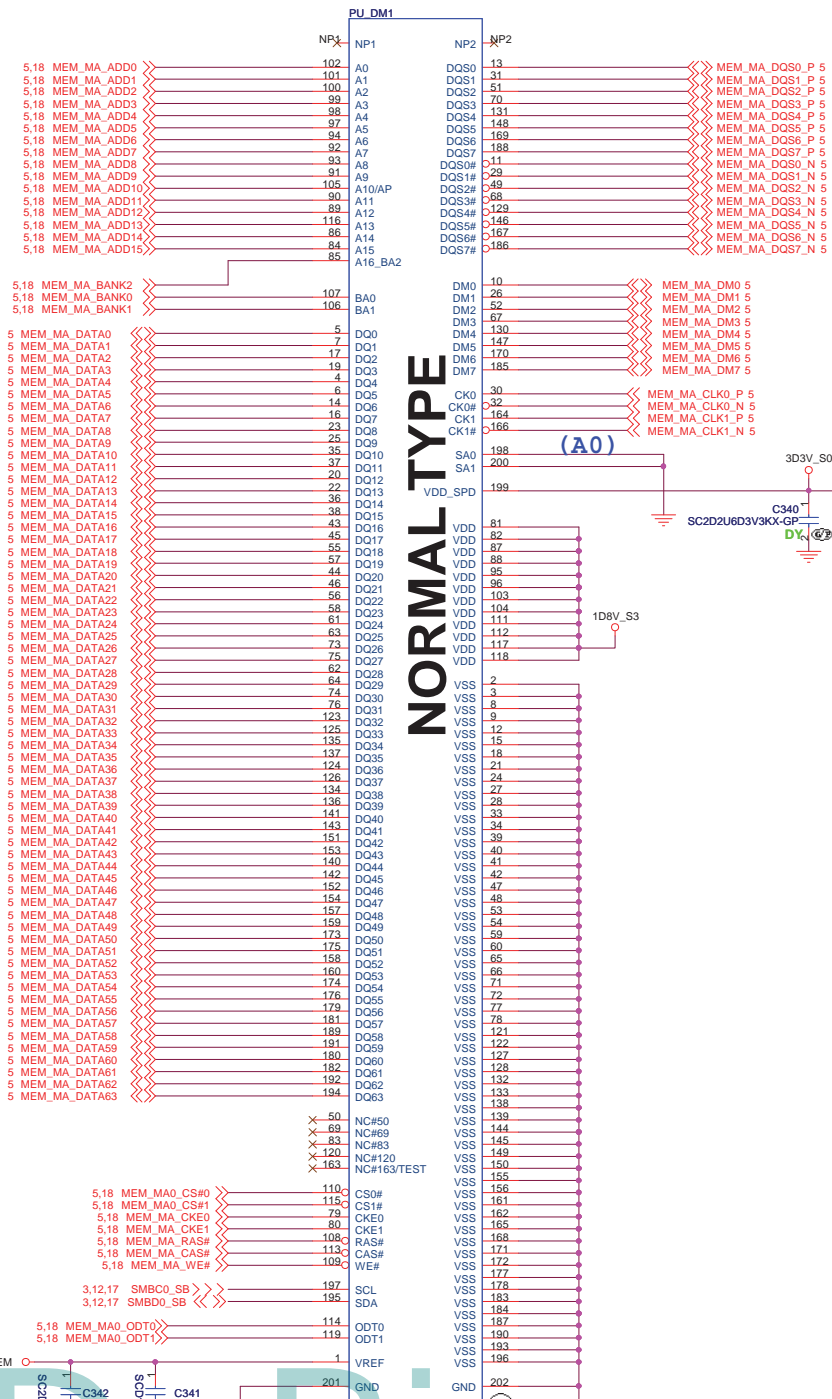
Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

Dr-Bios.com

<Core Design>

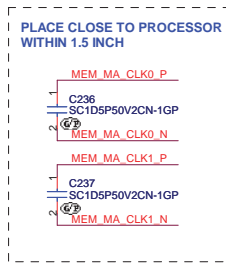
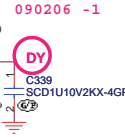
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title ATI-SB700 STRAPPING (5/5)		
Size A3	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 15 of 56	

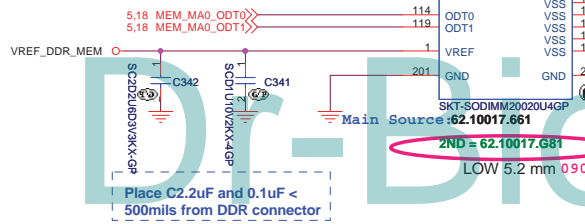
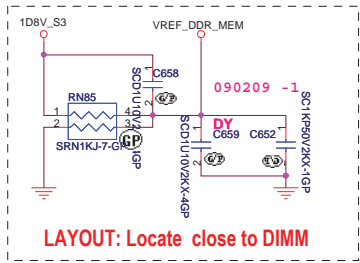


NORMAL TYPE

(A0)



DDR_VREF



<Core Design>

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Title: **DDR_SO-DIMM SKT_1**

Size: Custom Document Number: **JM70-PU** Rev: -2

Date: Friday, March 06, 2009 Sheet: 16 of 56

5,18 MEM_MB_ADD0 102 A0
 5,18 MEM_MB_ADD1 101 A1
 5,18 MEM_MB_ADD2 100 A2
 5,18 MEM_MB_ADD3 98 A3
 5,18 MEM_MB_ADD4 99 A4
 5,18 MEM_MB_ADD5 97 A5
 5,18 MEM_MB_ADD6 94 A6
 5,18 MEM_MB_ADD7 93 A7
 5,18 MEM_MB_ADD8 92 A8
 5,18 MEM_MB_ADD9 91 A9
 5,18 MEM_MB_ADD10 105 A10/AP
 5,18 MEM_MB_ADD11 90 A11
 5,18 MEM_MB_ADD12 89 A12
 5,18 MEM_MB_ADD13 116 A13
 5,18 MEM_MB_ADD14 84 A14
 5,18 MEM_MB_ADD15 85 A15
 5,18 MEM_MB_BANK2 107 A16/BA2
 5,18 MEM_MB_BANK0 107 BA0
 5,18 MEM_MB_BANK1 106 BA1

5 MEM_MB_DATA0 7 DO0
 5 MEM_MB_DATA1 17 DO1
 5 MEM_MB_DATA2 19 DO2
 5 MEM_MB_DATA3 4 DO3
 5 MEM_MB_DATA4 4 DO4
 5 MEM_MB_DATA5 6 DO5
 5 MEM_MB_DATA6 14 DO6
 5 MEM_MB_DATA7 16 DO7
 5 MEM_MB_DATA8 23 DO8
 5 MEM_MB_DATA9 25 DO9
 5 MEM_MB_DATA10 35 DO10
 5 MEM_MB_DATA11 37 DO11
 5 MEM_MB_DATA12 20 DO12
 5 MEM_MB_DATA13 22 DO13
 5 MEM_MB_DATA14 36 DO14
 5 MEM_MB_DATA15 38 DO15
 5 MEM_MB_DATA16 43 DO16
 5 MEM_MB_DATA17 45 DO17
 5 MEM_MB_DATA18 55 DO18
 5 MEM_MB_DATA19 44 DO19
 5 MEM_MB_DATA20 44 DO20
 5 MEM_MB_DATA21 46 DO21
 5 MEM_MB_DATA22 58 DO22
 5 MEM_MB_DATA23 61 DO23
 5 MEM_MB_DATA24 58 DO24
 5 MEM_MB_DATA25 63 DO25
 5 MEM_MB_DATA26 73 DO26
 5 MEM_MB_DATA27 62 DO27
 5 MEM_MB_DATA28 75 DO28
 5 MEM_MB_DATA29 64 DO29
 5 MEM_MB_DATA30 74 DO30
 5 MEM_MB_DATA31 76 DO31
 5 MEM_MB_DATA32 123 DO32
 5 MEM_MB_DATA33 125 DO33
 5 MEM_MB_DATA34 135 DO34
 5 MEM_MB_DATA35 137 DO35
 5 MEM_MB_DATA36 124 DO36
 5 MEM_MB_DATA37 126 DO37
 5 MEM_MB_DATA38 134 DO38
 5 MEM_MB_DATA39 136 DO39
 5 MEM_MB_DATA40 141 DO40
 5 MEM_MB_DATA41 143 DO41
 5 MEM_MB_DATA42 151 DO42
 5 MEM_MB_DATA43 153 DO43
 5 MEM_MB_DATA44 140 DO44
 5 MEM_MB_DATA45 142 DO45
 5 MEM_MB_DATA46 152 DO46
 5 MEM_MB_DATA47 154 DO47
 5 MEM_MB_DATA48 157 DO48
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 5 MEM_MB_DATA60 180 DO60
 5 MEM_MB_DATA61 182 DO61
 5 MEM_MB_DATA62 192 DO62
 5 MEM_MB_DATA63 194 DO63

5 MEM_MB_DQS0_N 111 DOS0#
 5 MEM_MB_DQS1_N 29 DOS1#
 5 MEM_MB_DQS2_N 49 DOS2#
 5 MEM_MB_DQS3_N 68 DOS3#
 5 MEM_MB_DQS4_N 129 DOS4#
 5 MEM_MB_DQS5_N 146 DOS5#
 5 MEM_MB_DQS6_N 167 DOS6#
 5 MEM_MB_DQS7_N 186 DOS7#

5 MEM_MB_DQS0_P 13 DOS0
 5 MEM_MB_DQS1_P 31 DOS1
 5 MEM_MB_DQS2_P 51 DOS2
 5 MEM_MB_DQS3_P 70 DOS3
 5 MEM_MB_DQS4_P 131 DOS4
 5 MEM_MB_DQS5_P 148 DOS5
 5 MEM_MB_DQS6_P 169 DOS6
 5 MEM_MB_DQS7_P 188 DOS7

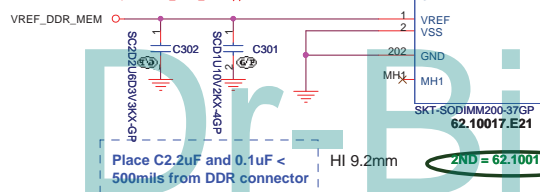
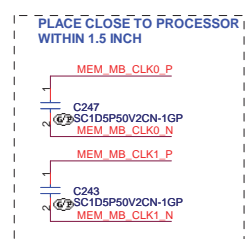
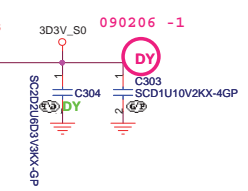
5,18 MEM_MB0_ODT0 114 OTD0
 5,18 MEM_MB0_ODT1 119 OTD1

PU DM2

NORMAL TYPE

RAS# 108
 WE# 109
 CAS# 113
 CS0# 110
 CS1# 115
 CK0 79
 CK1# 164
 DM0 10
 DM1 26
 DM2 52
 DM3 130
 DM4 147
 DM5 170
 DM6 185
 SDA 195
 SCL 197
 VDDSPD 199
 SA0 198
 SA1 200
 NC#50 50
 NC#69 69
 NC#83 83
 NC#120 120
 NC#163 163
 VDD 81
 VDD 82
 VDD 87
 VDD 88
 VDD 95
 VDD 103
 VDD 104
 VDD 111
 VDD 112
 VDD 117
 VDD 118
 VSS 3
 VSS 8
 VSS 9
 VSS 12
 VSS 15
 VSS 18
 VSS 21
 VSS 24
 VSS 27
 VSS 28
 VSS 33
 VSS 34
 VSS 38
 VSS 40
 VSS 41
 VSS 42
 VSS 47
 VSS 48
 VSS 53
 VSS 59
 VSS 60
 VSS 65
 VSS 66
 VSS 71
 VSS 72
 VSS 77
 VSS 78
 VSS 121
 VSS 122
 VSS 127
 VSS 128
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 VSS 161
 VSS 162
 VSS 165
 VSS 168
 VSS 171
 VSS 172
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 VSS 178
 VSS 183
 VSS 184
 VSS 187
 VSS 190
 VSS 193
 VSS 196
 GND 201
 MH2 202

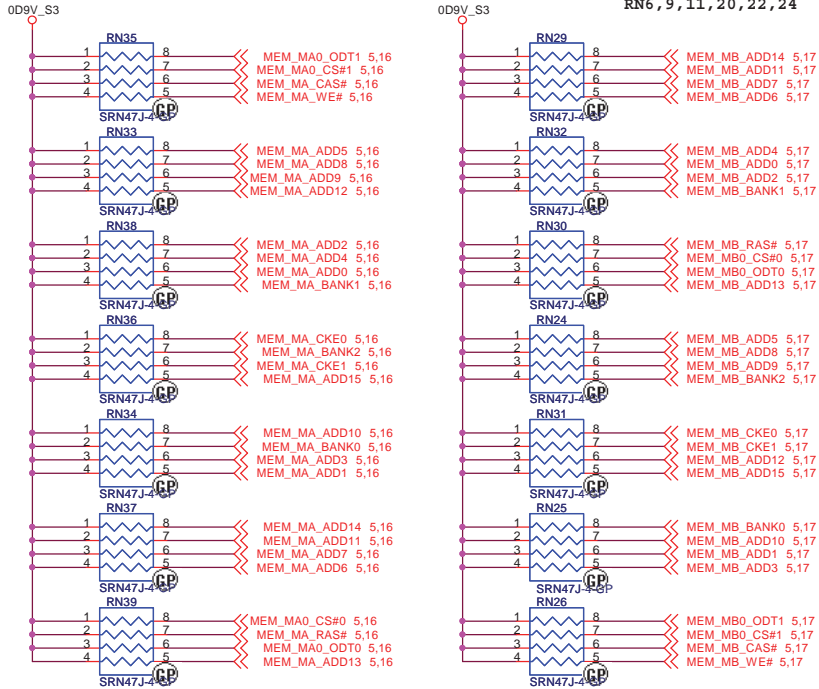
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 MEM_MB_WE# 5,18
 MEM_MB_CAS# 5,18
 MEM_MB_CS0# 5,18
 MEM_MB_CS1# 5,18
 MEM_MB_CKE0 5,18
 MEM_MB_CKE1 5,18
 MEM_MB_CLK0_P 5
 MEM_MB_CLK0_N 5
 MEM_MB_CLK1_P 5
 MEM_MB_CLK1_N 5
 MEM_MB_DM0 5
 MEM_MB_DM1 5
 MEM_MB_DM2 5
 MEM_MB_DM3 5
 MEM_MB_DM4 5
 MEM_MB_DM5 5
 MEM_MB_DM6 5
 MEM_MB_DM7 5
 SMBD0_SB 3,12,16
 SMBD0_SB 3,12,16
 DIMM2_SA1
 10KR2J-3-GP
 1D8V_S3



PARALLEL TERMINATION

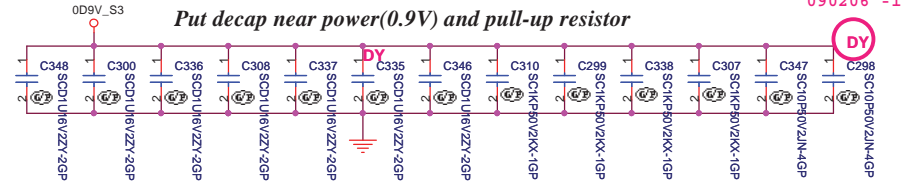
Put decap near power(0.9V) and pull-up resistor

Net swap 11/14
RN6, 9, 11, 20, 22, 24

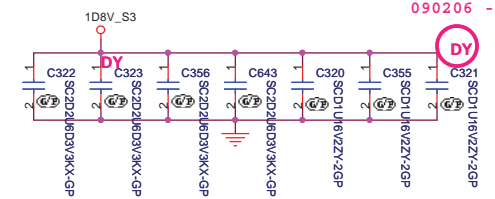


Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

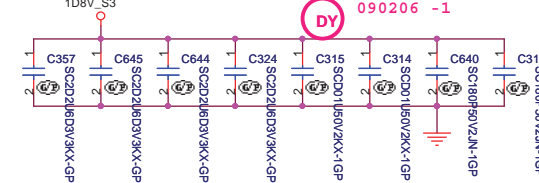


Place these Caps near DM1

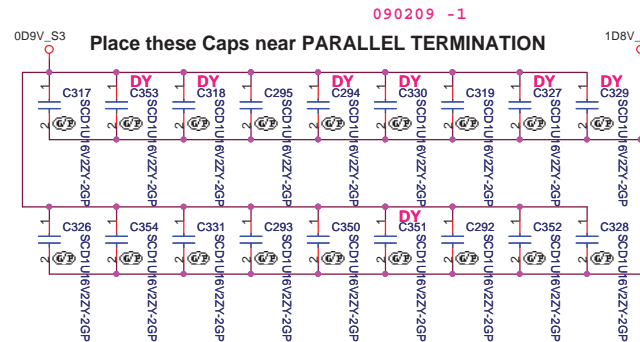


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2

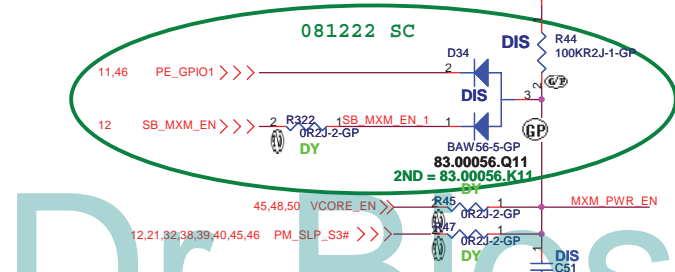
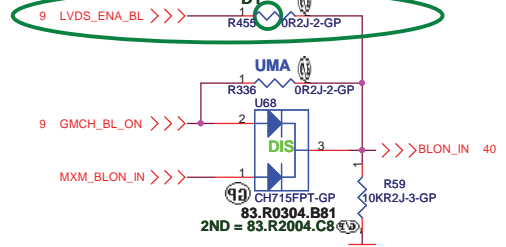
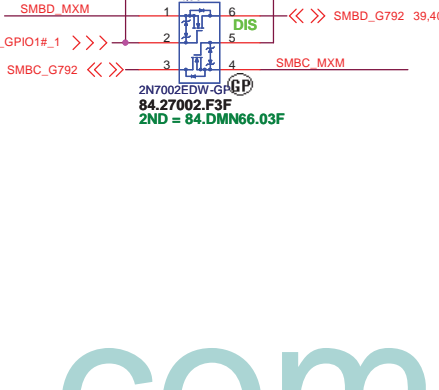
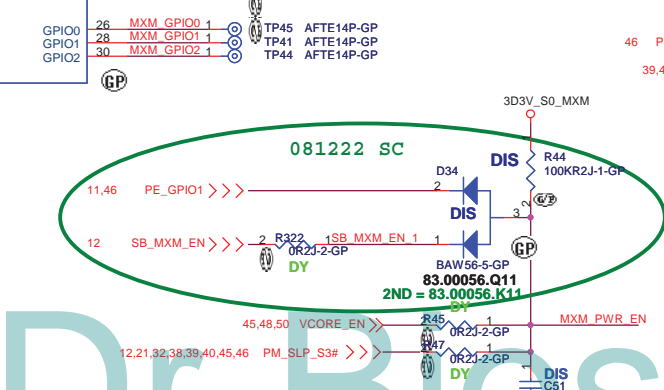
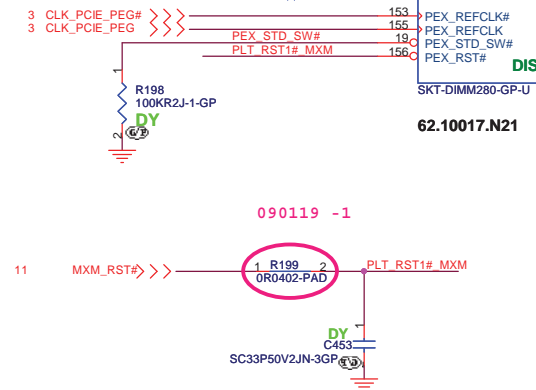
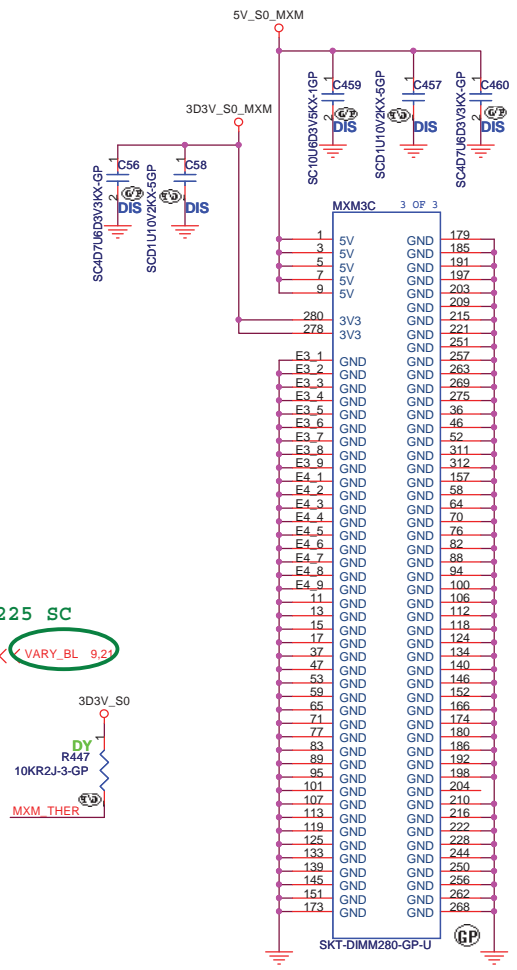
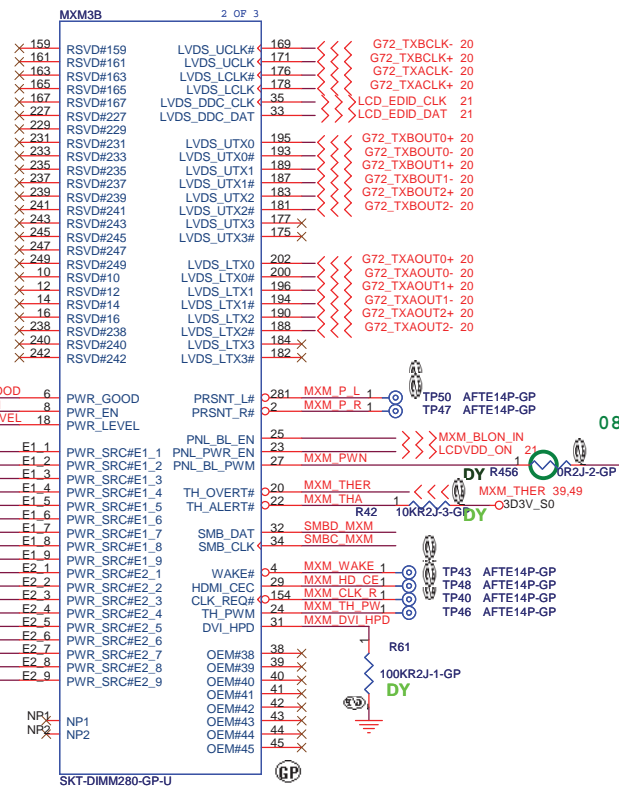


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3



- 8 PEG_TXP[15..0] <<>
- 8 PEG_TXN[15..0] <<>
- 8 PEG_RXP[15..0] <<>
- 8 PEG_RXN[15..0] <<>

MXM3A 1 OF 3		MXM3B 2 OF 3		MXM3C 3 OF 3	
PEG_RXP0	SCD1U10V2KX-5GP C442	DIS GRXP0	149	PEX_RX0	DP_A_AUX# 277
PEG_RXN0	SCD1U10V2KX-5GP C441	DIS GRXN0	147	PEX_RX0#	DP_A_AUX 279
PEG_RXP1	SCD1U10V2KX-5GP C440	DIS GRXP1	141	PEX_RX1	DP_A_HPD 276
PEG_RXN1	SCD1U10V2KX-5GP C439	DIS GRXN1	141	PEX_RX1#	
PEG_RXP2	SCD1U10V2KX-5GP C438	DIS GRXP2	137	PEX_RX2	DP_A_L0# 253
PEG_RXN2	SCD1U10V2KX-5GP C437	DIS GRXN2	135	PEX_RX2#	DP_B_L0# 255
PEG_RXP3	SCD1U10V2KX-5GP C436	DIS GRXP3	123	PEX_RX3	DP_A_L1# 259
PEG_RXN3	SCD1U10V2KX-5GP C435	DIS GRXN3	121	PEX_RX3#	DP_B_L1# 261
PEG_RXP4	SCD1U10V2KX-5GP C446	DIS GRXP4	117	PEX_RX4	DP_A_L2# 265
PEG_RXN4	SCD1U10V2KX-5GP C445	DIS GRXN4	115	PEX_RX4#	DP_B_L2# 267
PEG_RXP5	SCD1U10V2KX-5GP C434	DIS GRXP5	111	PEX_RX5	DP_A_L3# 271
PEG_RXN5	SCD1U10V2KX-5GP C433	DIS GRXN5	109	PEX_RX5#	DP_B_L3# 273
PEG_RXP6	SCD1U10V2KX-5GP C452	DIS GRXP6	105	PEX_RX6	DP_A_L3 273
PEG_RXN6	SCD1U10V2KX-5GP C451	DIS GRXN6	103	PEX_RX6#	
PEG_RXP7	SCD1U10V2KX-5GP C432	DIS GRXP7	97	PEX_RX7	DP_B_AUX# 270
PEG_RXN7	SCD1U10V2KX-5GP C431	DIS GRXN7	97	PEX_RX7#	DP_B_AUX 274
PEG_RXP8	SCD1U10V2KX-5GP C455	DIS GRXP8	93	PEX_RX8	DP_B_HPD 274
PEG_RXN8	SCD1U10V2KX-5GP C454	DIS GRXN8	91	PEX_RX8#	
PEG_RXP9	SCD1U10V2KX-5GP C430	DIS GRXP9	87	PEX_RX9	DP_B_L0# 246
PEG_RXN9	SCD1U10V2KX-5GP C429	DIS GRXN9	85	PEX_RX9#	DP_B_L0 247
PEG_RXP10	SCD1U10V2KX-5GP C428	DIS GRXP10	81	PEX_RX10	DP_B_L1# 252
PEG_RXN10	SCD1U10V2KX-5GP C427	DIS GRXN10	79	PEX_RX10#	DP_B_L1 254
PEG_RXP11	SCD1U10V2KX-5GP C450	DIS GRXP11	75	PEX_RX11	DP_B_L2# 260
PEG_RXN11	SCD1U10V2KX-5GP C449	DIS GRXN11	73	PEX_RX11#	DP_B_L2 262
PEG_RXP12	SCD1U10V2KX-5GP C426	DIS GRXP12	69	PEX_RX12	DP_B_L3# 264
PEG_RXN12	SCD1U10V2KX-5GP C425	DIS GRXN12	67	PEX_RX12#	DP_B_L3 266
PEG_RXP13	SCD1U10V2KX-5GP C424	DIS GRXP13	63	PEX_RX13	
PEG_RXN13	SCD1U10V2KX-5GP C423	DIS GRXN13	61	PEX_RX13#	
PEG_RXP14	SCD1U10V2KX-5GP C448	DIS GRXP14	57	PEX_RX14	DP_C_AUX# 223
PEG_RXN14	SCD1U10V2KX-5GP C447	DIS GRXN14	55	PEX_RX14#	DP_C_AUX 225
PEG_RXP15	SCD1U10V2KX-5GP C422	DIS GRXP15	51	PEX_RX15	DP_C_HPD 234
PEG_RXN15	SCD1U10V2KX-5GP C421	DIS GRXN15	49	PEX_RX15#	
PEG_TXP0	SCD1U10V2KX-5GP C73	DIS GTXP0	150	PEX_TX0	DP_C_L0# 201
PEG_TXN0	SCD1U10V2KX-5GP C74	DIS GTXN0	148	PEX_TX0#	DP_C_L0 202
PEG_TXP1	SCD1U10V2KX-5GP C75	DIS GTXP1	144	PEX_TX1	DP_C_L1# 205
PEG_TXN1	SCD1U10V2KX-5GP C76	DIS GTXN1	142	PEX_TX1#	DP_C_L1 207
PEG_TXP2	SCD1U10V2KX-5GP C88	DIS GTXP2	138	PEX_TX2	DP_C_L2# 211
PEG_TXN2	SCD1U10V2KX-5GP C89	DIS GTXN2	136	PEX_TX2#	DP_C_L2 213
PEG_TXP3	SCD1U10V2KX-5GP C90	DIS GTXP3	122	PEX_TX3	DP_C_L3# 217
PEG_TXN3	SCD1U10V2KX-5GP C91	DIS GTXN3	120	PEX_TX3#	DP_C_L3 219
PEG_TXP4	SCD1U10V2KX-5GP C77	DIS GTXP4	116	PEX_TX4	
PEG_TXN4	SCD1U10V2KX-5GP C78	DIS GTXN4	114	PEX_TX4#	
PEG_TXP5	SCD1U10V2KX-5GP C80	DIS GTXP5	110	PEX_TX5	DP_D_AUX# 230
PEG_TXN5	SCD1U10V2KX-5GP C80	DIS GTXN5	108	PEX_TX5#	DP_D_AUX 232
PEG_TXP6	SCD1U10V2KX-5GP C81	DIS GTXP6	104	PEX_TX6	DP_D_HPD 236
PEG_TXN6	SCD1U10V2KX-5GP C82	DIS GTXN6	102	PEX_TX6#	
PEG_TXP7	SCD1U10V2KX-5GP C83	DIS GTXP7	98	PEX_TX7	DP_D_L0# 206
PEG_TXN7	SCD1U10V2KX-5GP C84	DIS GTXN7	96	PEX_TX7#	DP_D_L0 208
PEG_TXP8	SCD1U10V2KX-5GP C85	DIS GTXP8	92	PEX_TX8	DP_D_L1# 212
PEG_TXN8	SCD1U10V2KX-5GP C86	DIS GTXN8	90	PEX_TX8#	DP_D_L1 214
PEG_TXP9	SCD1U10V2KX-5GP C92	DIS GTXP9	86	PEX_TX9	DP_D_L2# 218
PEG_TXN9	SCD1U10V2KX-5GP C93	DIS GTXN9	84	PEX_TX9#	DP_D_L2 220
PEG_TXP10	SCD1U10V2KX-5GP C61	DIS GTXP10	80	PEX_TX10	DP_D_L3# 224
PEG_TXN10	SCD1U10V2KX-5GP C62	DIS GTXN10	78	PEX_TX10#	DP_D_L3 226
PEG_TXP11	SCD1U10V2KX-5GP C65	DIS GTXP11	74	PEX_TX11	
PEG_TXN11	SCD1U10V2KX-5GP C66	DIS GTXN11	72	PEX_TX11#	
PEG_TXP12	SCD1U10V2KX-5GP C63	DIS GTXP12	68	PEX_TX12	VGA_DISABLE# 21
PEG_TXN12	SCD1U10V2KX-5GP C64	DIS GTXN12	66	PEX_TX12#	VGA_DDC_DAT 158
PEG_TXP13	SCD1U10V2KX-5GP C67	DIS GTXP13	62	PEX_TX13	VGA_DDC_CLK 160
PEG_TXN13	SCD1U10V2KX-5GP C68	DIS GTXN13	60	PEX_TX13#	VGA_VSYNC 162
PEG_TXP14	SCD1U10V2KX-5GP C69	DIS GTXP14	58	PEX_TX13#	VGA_HSYNC 164
PEG_TXN14	SCD1U10V2KX-5GP C70	DIS GTXN14	54	PEX_TX14	VGA_RED 168
PEG_TXP15	SCD1U10V2KX-5GP C71	DIS GTXP15	50	PEX_TX14#	VGA_GREEN 170
PEG_TXN15	SCD1U10V2KX-5GP C72	DIS GTXN15	48	PEX_TX15#	VGA_BLUE 172



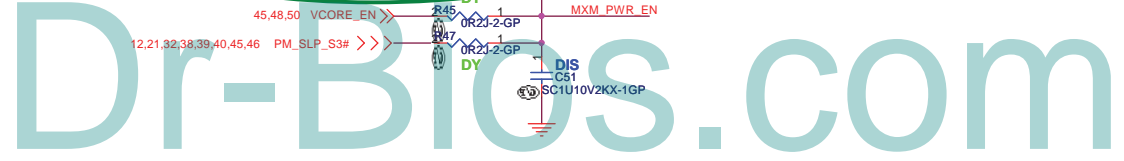
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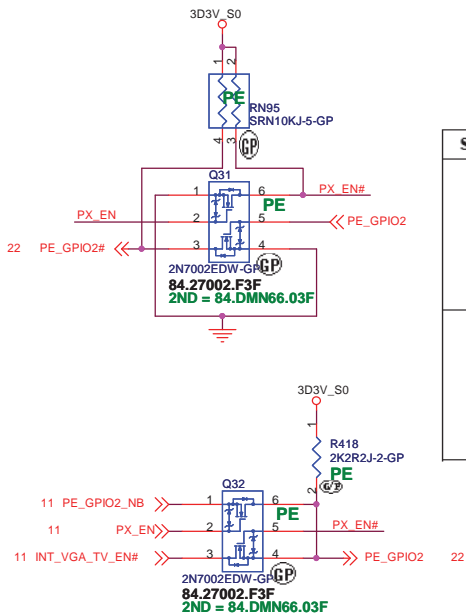
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

File: **Graphic MXM 3.0 CONN**

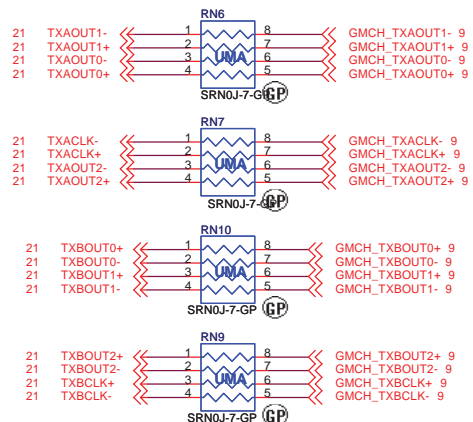
Size: A3 Document Number: **JM70-PU** Rev: -2

Date: Friday, March 06, 2009 Sheet 19 of 56

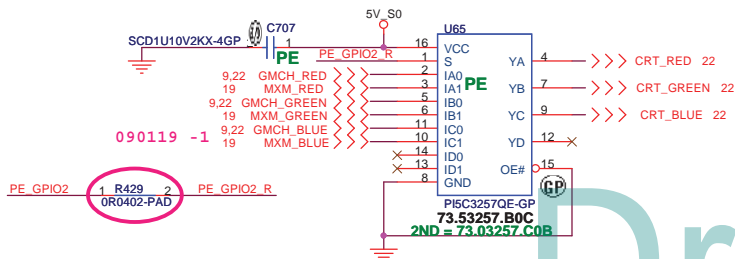




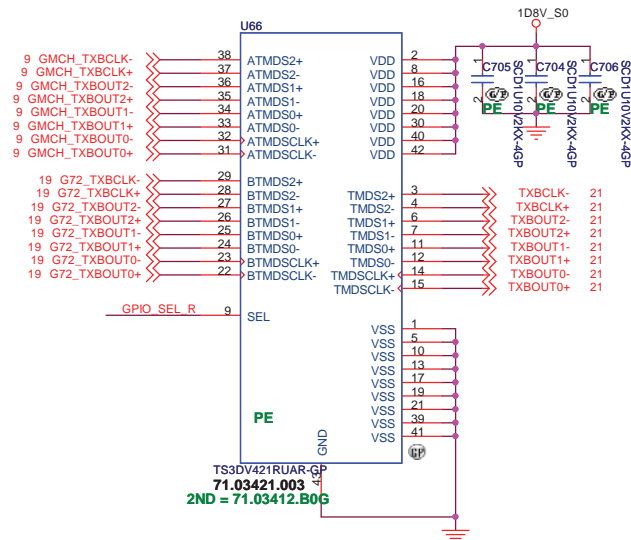
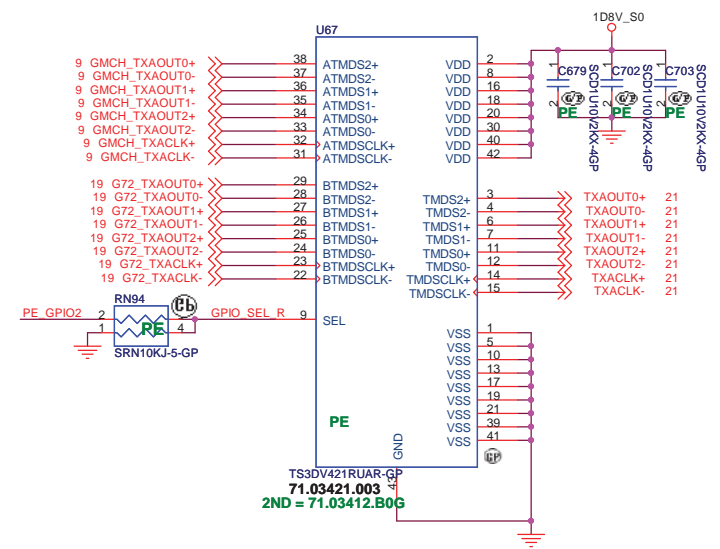
FUNCTION TABLE		
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-



\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



DISPLAY SUPPORT TABLE				
	PX_EN	PE_GPIO2_NB	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	0	X	0	IGP(LVDS,VGA,HDMI,DP)
MXM only mode	0	X	1	MXM(LVDS,VGA,HDMI,DP)
Power Express mode	1	0/1	X	*MXM(VGA,HDMI,DP); MXM/IGP(LVDS)
IGP + MXM	0	X	0	IGP(LVDS,VGA,HDMI)



<Core Design>

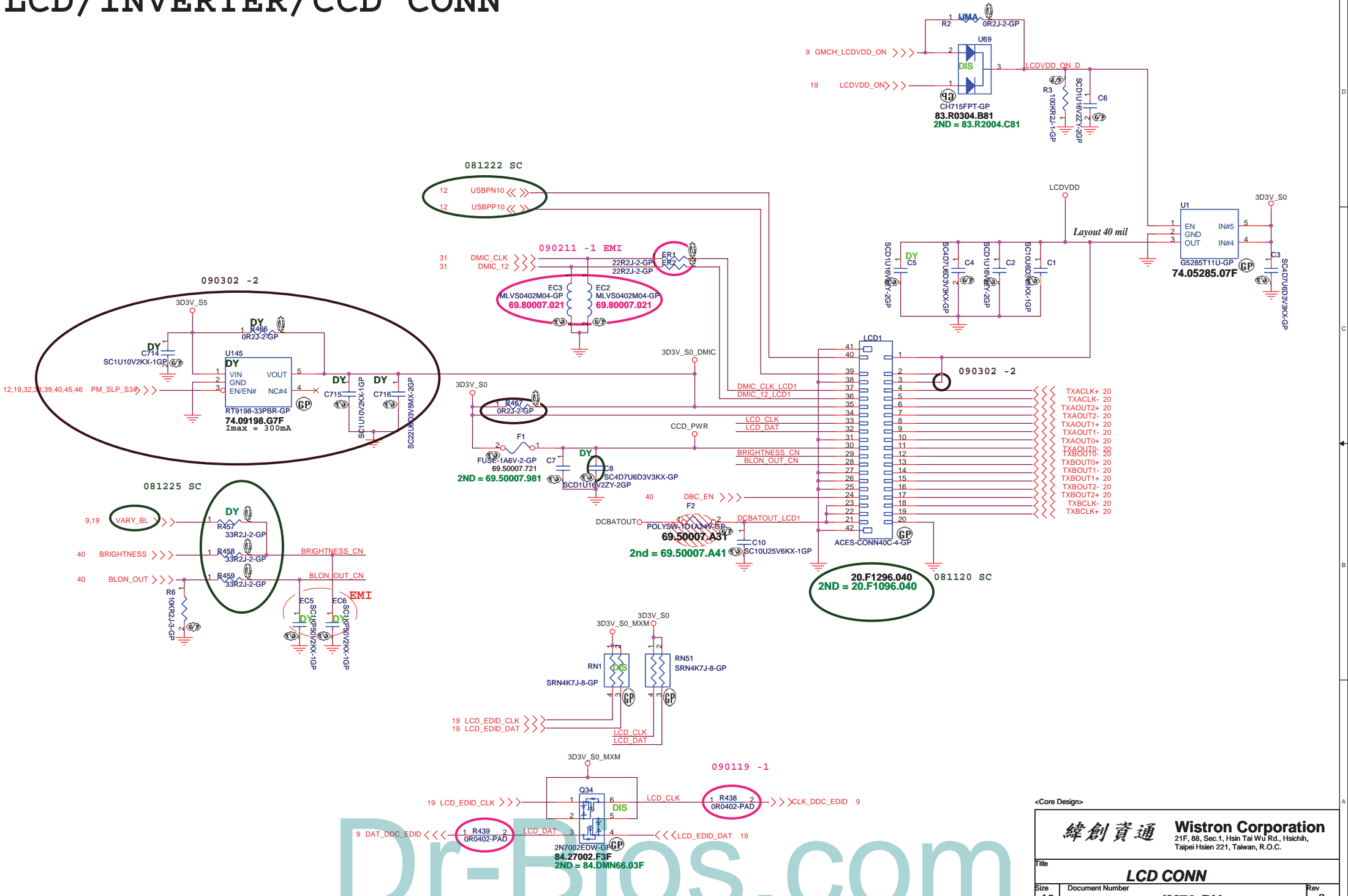
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **SWITCH**

Size: Document Number: **JM70-PU** Rev: -2

Date: Friday, March 06, 2009 Sheet 20 of 56

LCD/INVERTER/CCD CONN



<Core Design>

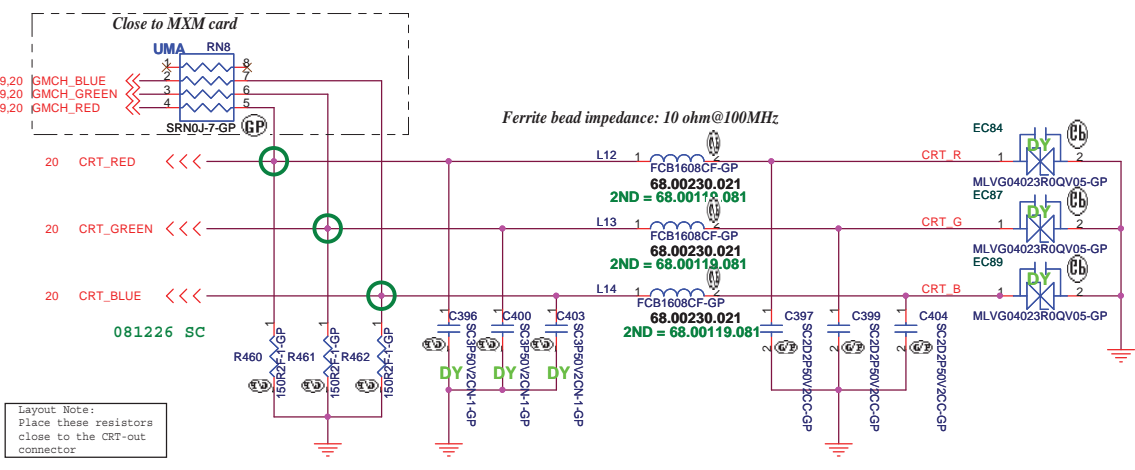
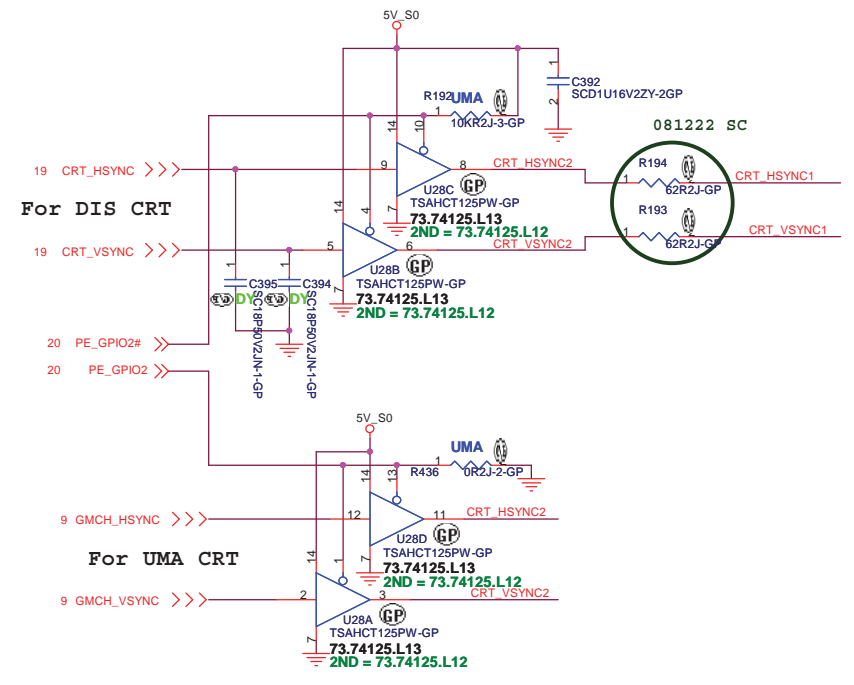
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN**

Size: A3	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 21 of 56	

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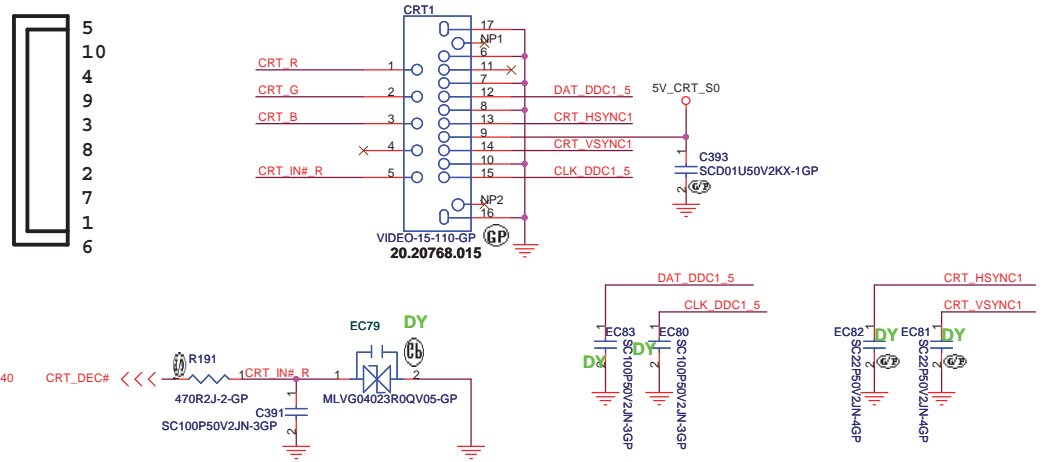
Hsync & Vsync level shift



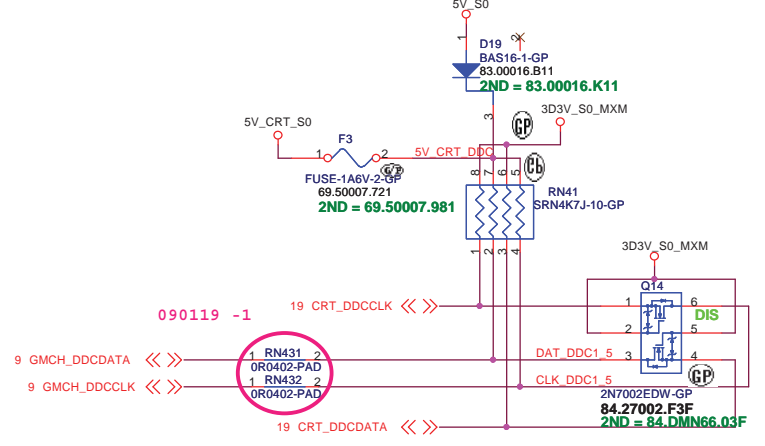
Layout Note:
Place these resistors close to the CRT-out connector

Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



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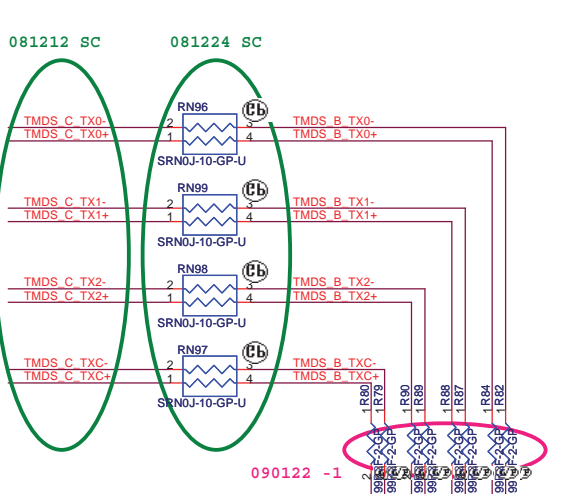
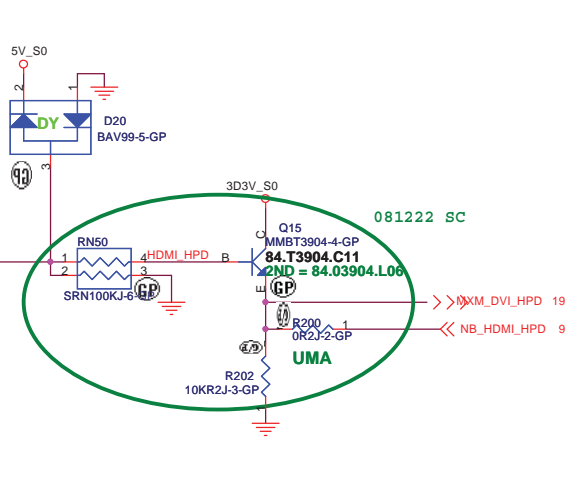
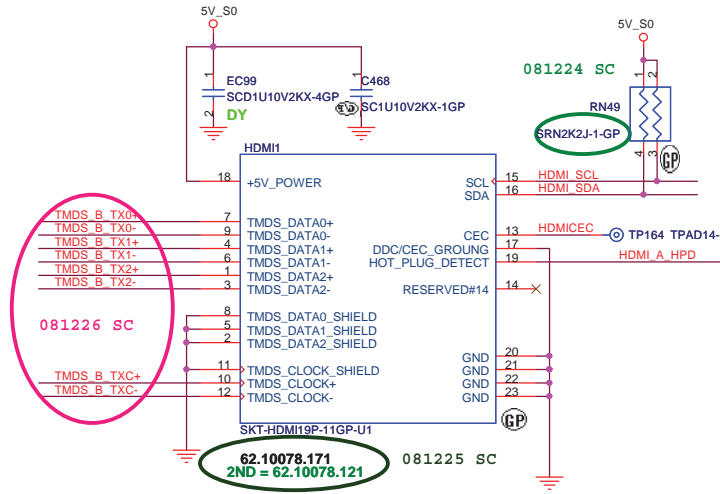
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

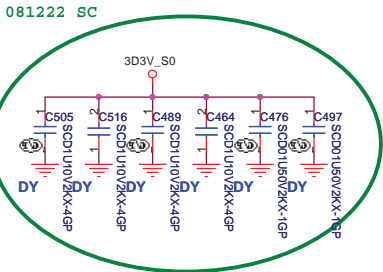
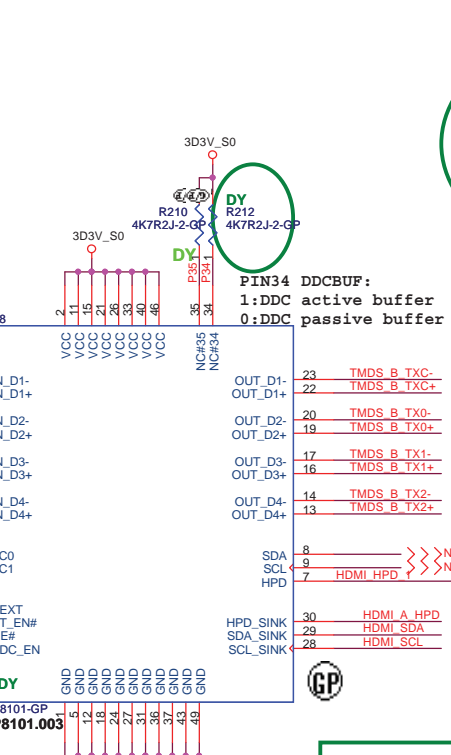
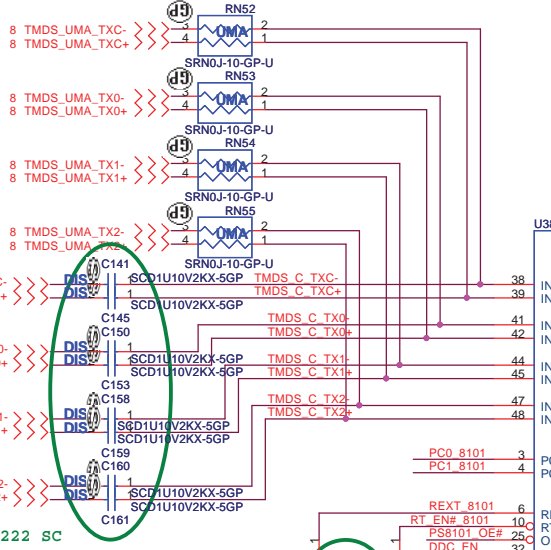
Title: **CRT Connector**

Size: Document Number **JM70-PU** Rev: **-2**

Date: Friday, March 06, 2009 Sheet 22 of 56

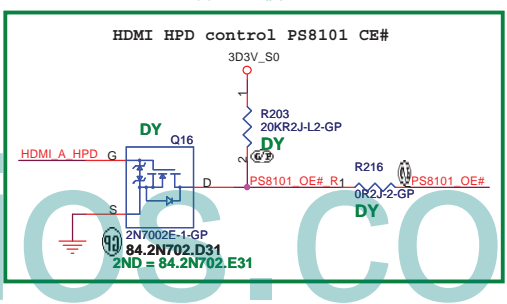
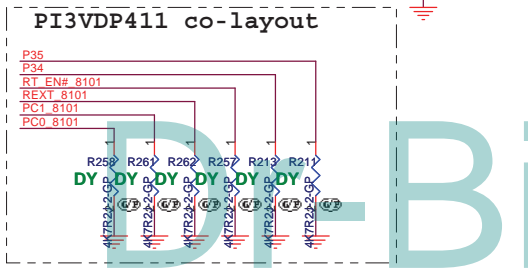
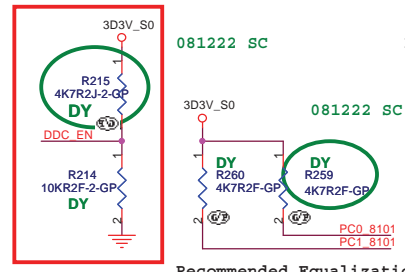
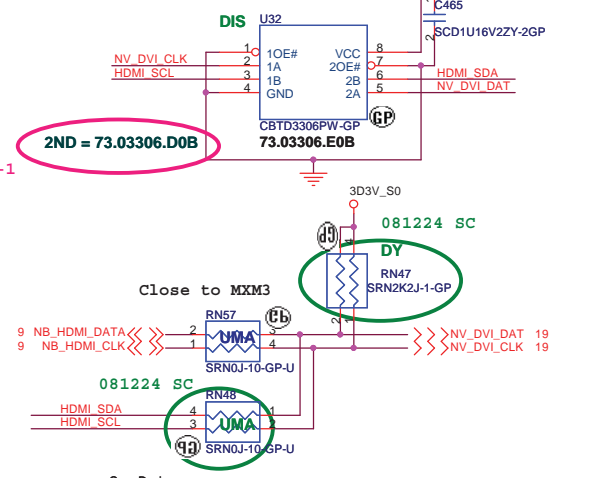


Place Near MXM3 Connector



HDMI SM BUS LEVEL shifter

Close HDMI1



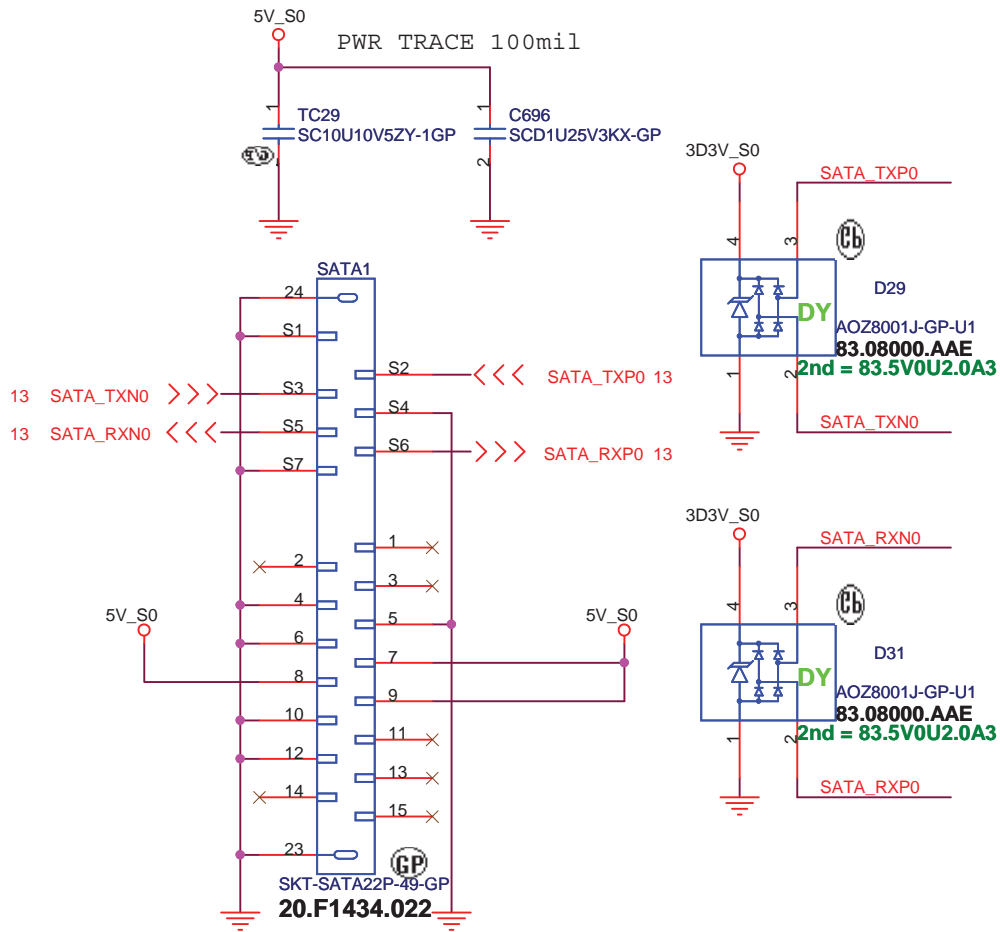
Recommended Equalization:
[PCL, PC0]=01, 4dB

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

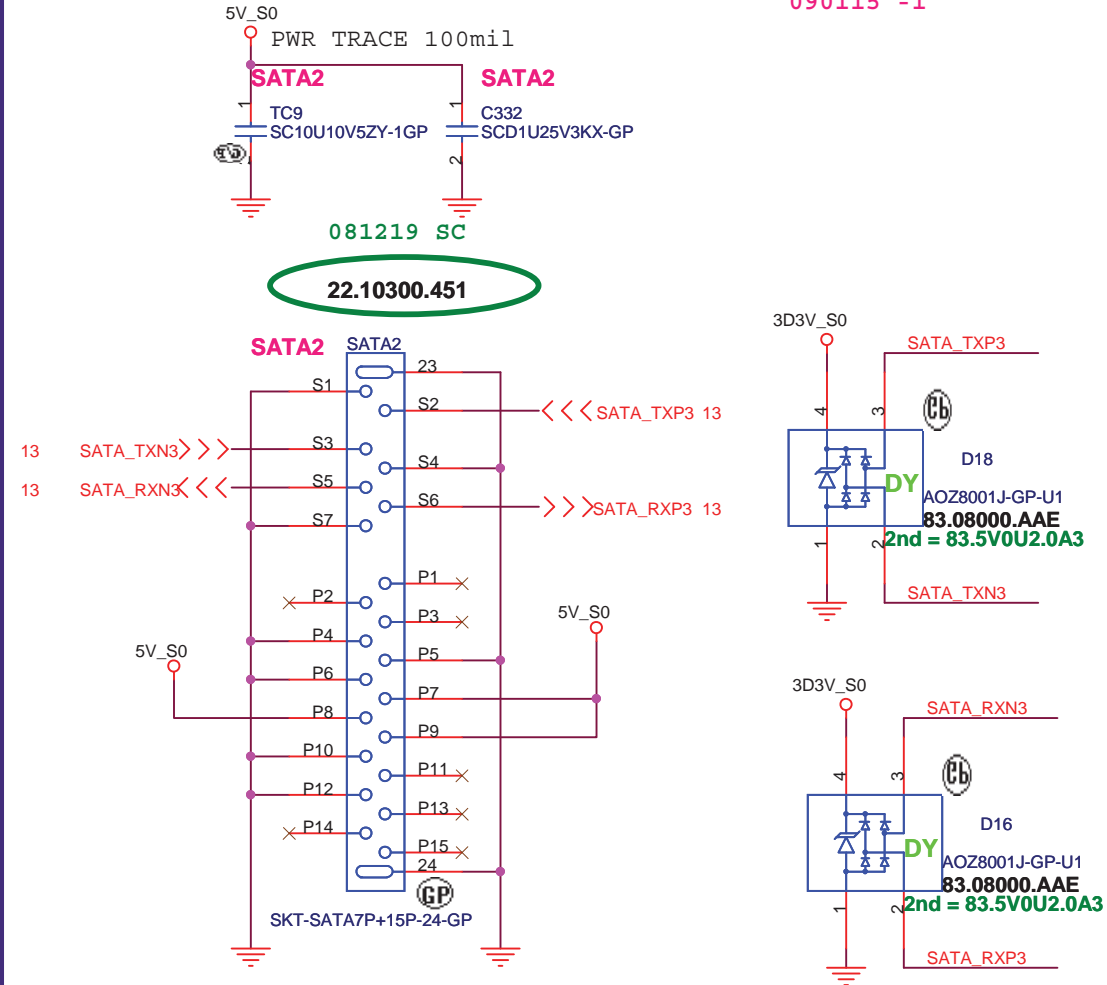
Title	HDMI CONNECTOR		
Size	Document Number	JM70-PU	Rev -2
Date: Friday, March 06, 2009		Sheet 23	of 56

SATA HDD Connector



2ND SATA HDD Connector

090115 -1



<Core Design>

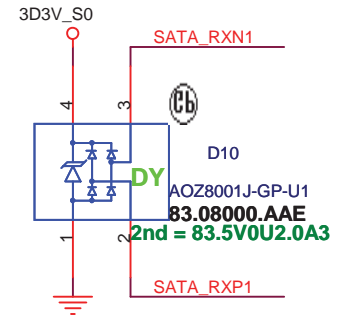
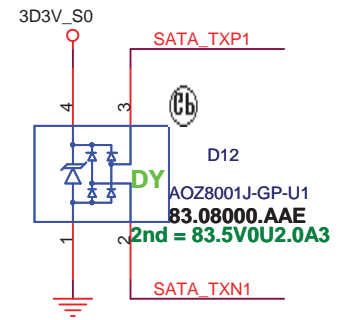
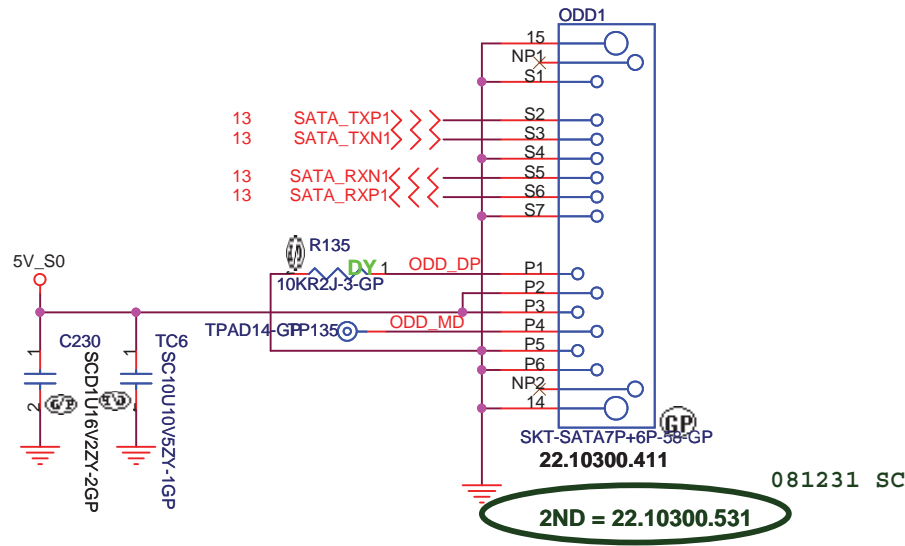
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title HDD		
Size A4	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 24 of	56

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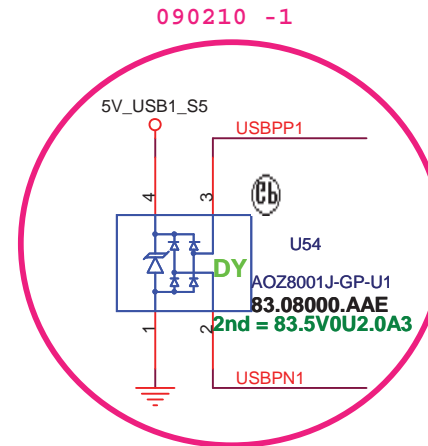
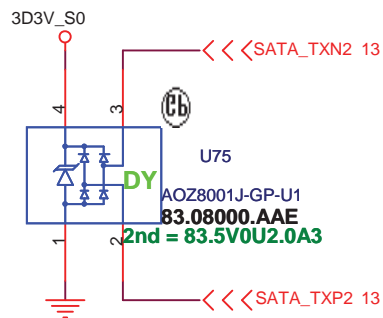
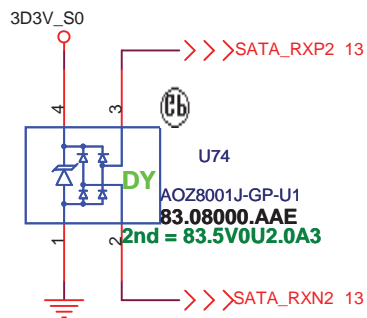
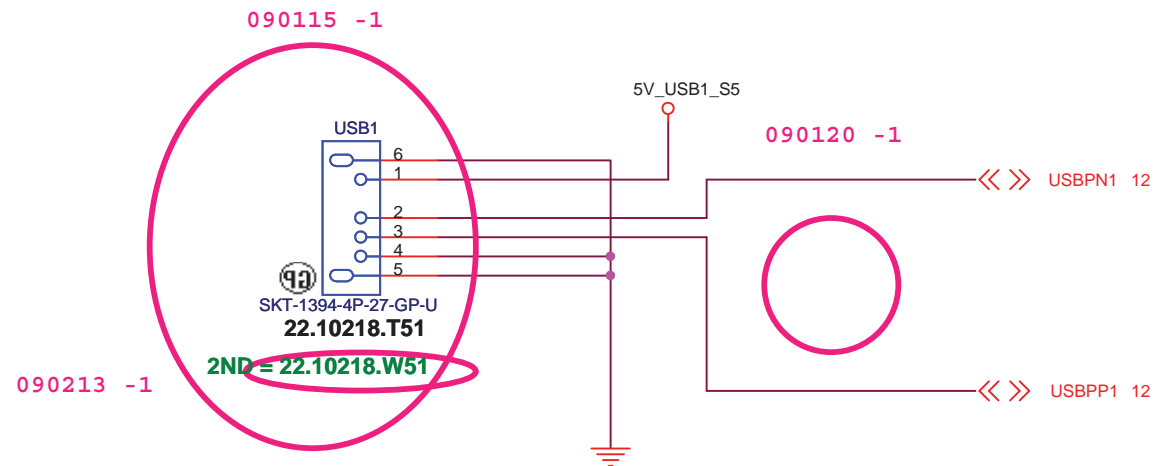
ODD Connector



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<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
CDROM	
Size	Document Number
A4	JM70-PU
Date:	Rev
Friday, March 06, 2009	-2
Sheet 25 of 56	

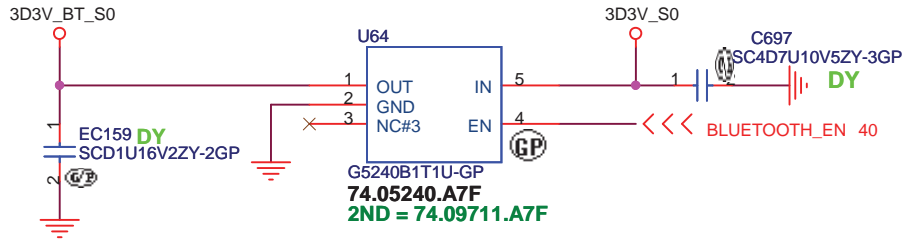


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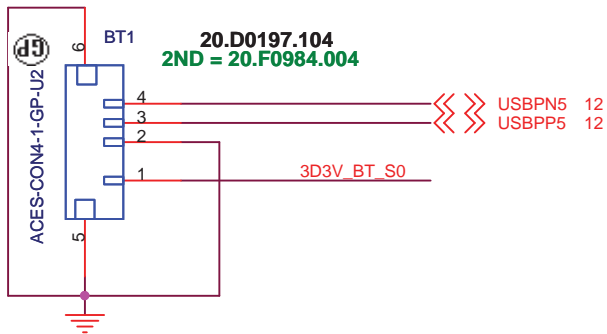
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		USB1	
Size	Document Number	Rev	
A4	JM70-PU	-2	
Date:	Friday, March 06, 2009	Sheet	26 of 56

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BLUETOOTH MODULE



EC40 put near BLUE1 / all USB put one choke near connector by EMI request

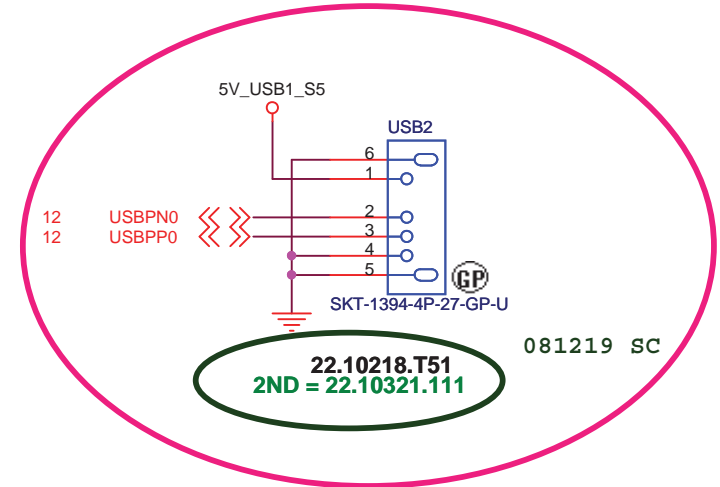
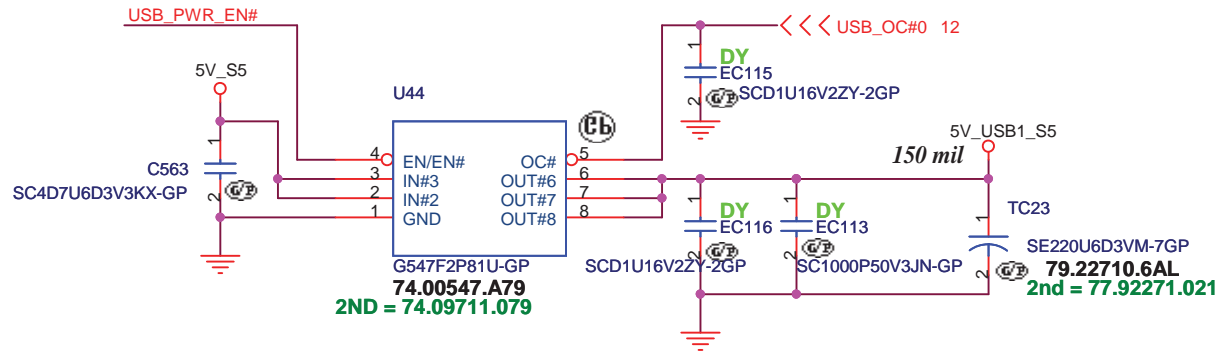


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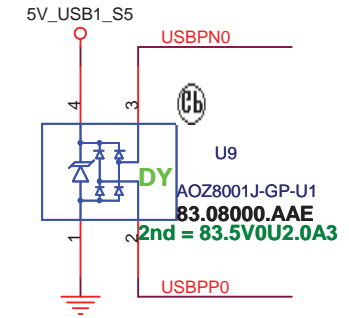
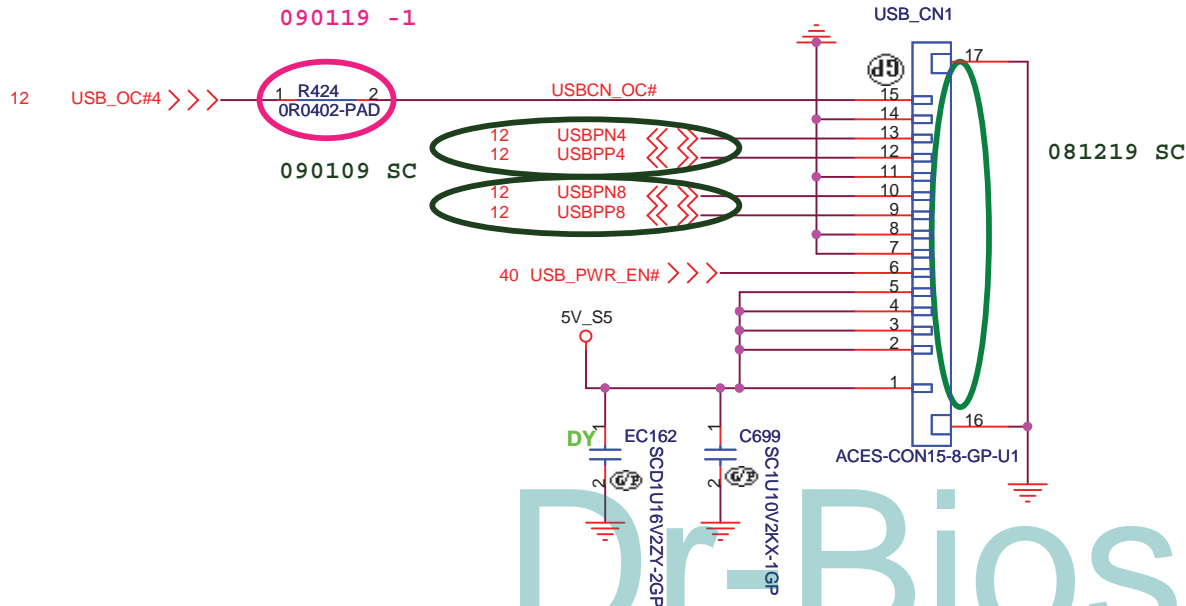
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
BLUETOOTH	
Size	Document Number
A4	JM70-PU
Date:	Rev
Friday, March 06, 2009	-2
Sheet 27 of 56	

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090115 -1



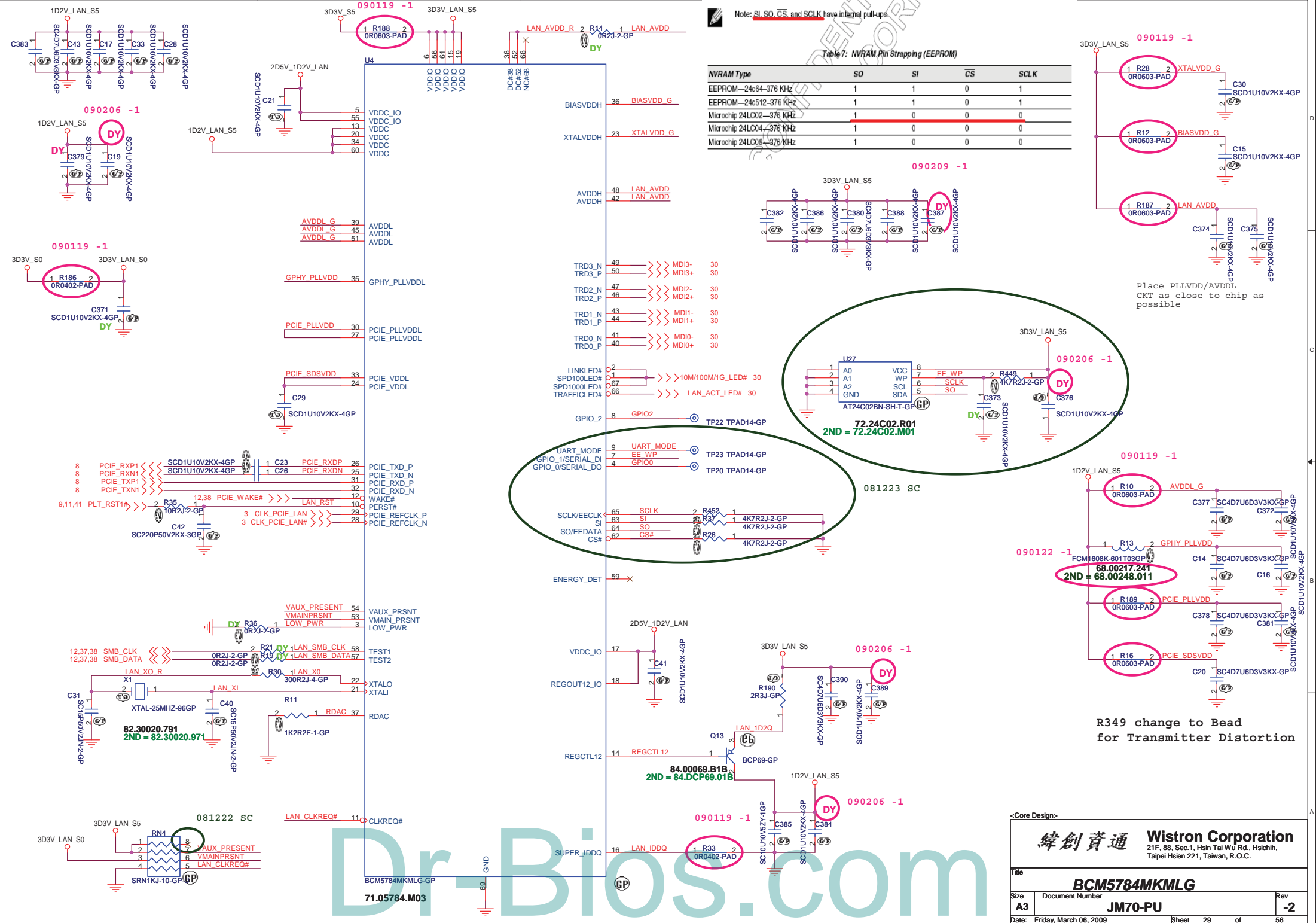
20.F1290.015
2ND = 21.D0214.115



<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB2			
Title	Document Number		Rev
A4	JM70-PU		-2
Date:	Friday, March 06, 2009	Sheet	28 of 56

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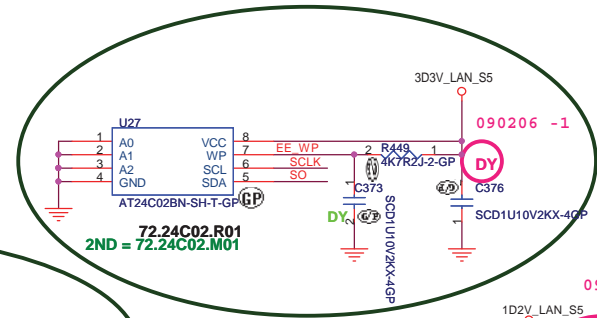
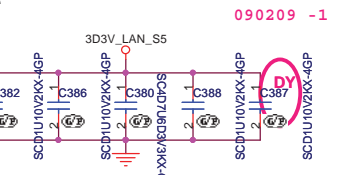


Note: SI, SO, CS, and SCLK have internal pull-ups.

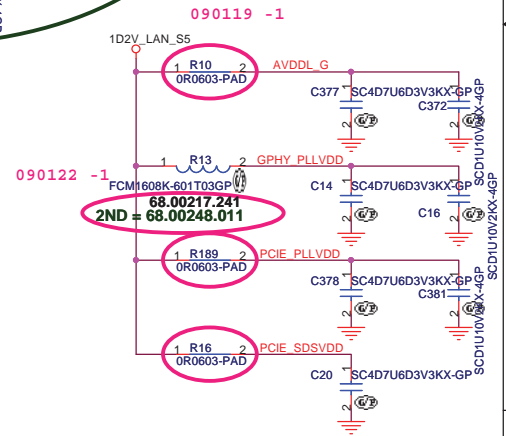
Table 7: NVRAM Pin Strapping (EEPROM)

NVRAM Type	SO	SI	CS	SCLK
EEPROM—24c64—376 KHz	1	1	0	1
EEPROM—24c512—376 KHz	1	1	0	1
Microchip 24LC02—376 KHz	1	0	0	0
Microchip 24LC04—376 KHz	1	0	0	0
Microchip 24LC08—376 KHz	1	0	0	0

Place PLLVDD/AVDDL CKT as close to chip as possible



081223 SC



R349 change to Bead for Transmitter Distortion

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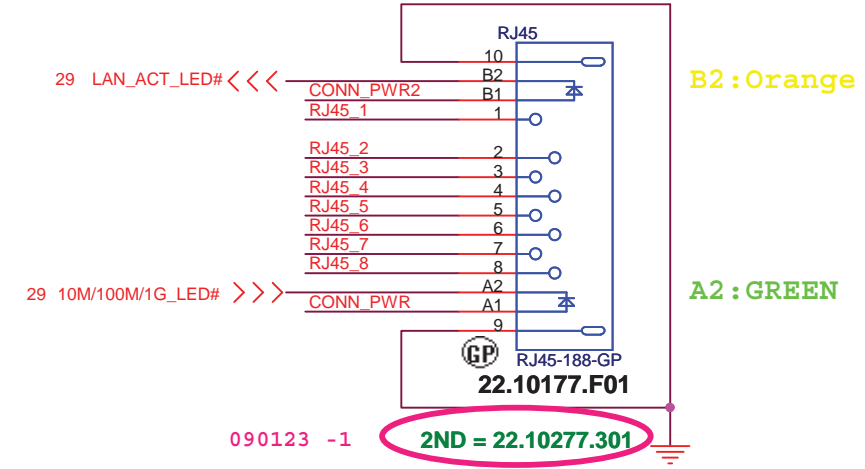
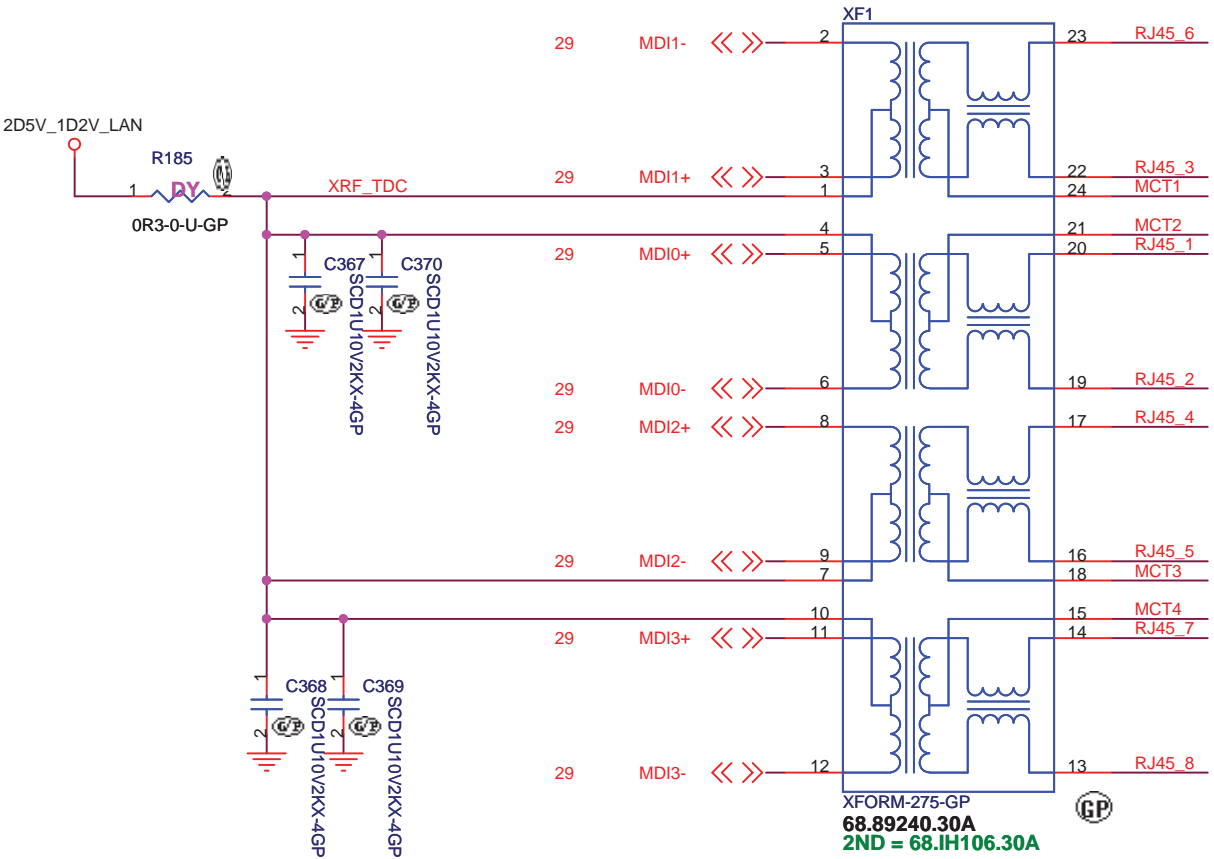
File: **BCM5784MKMLG**

Size: **A3** Document Number: **JM70-PU** Rev: **-2**

Date: Friday, March 06, 2009 Sheet 29 of 56

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LAN Connector



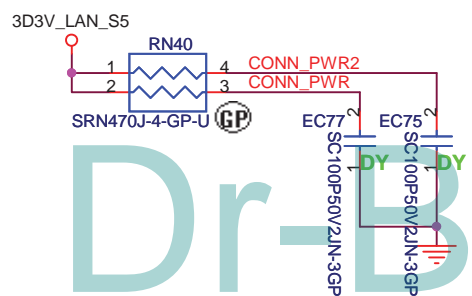
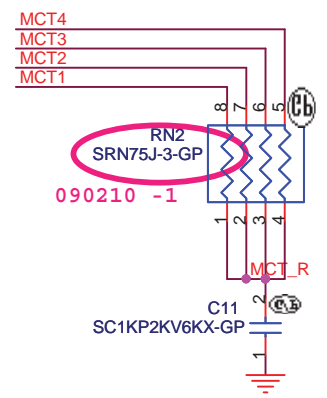
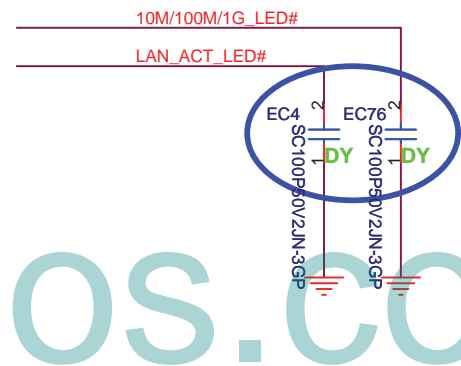
LAN Link: Green(A2), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

Soucrer want to add 3rd source 11/10
68.05009.301 GST5009-R LF
Angela Chi 0955-314886

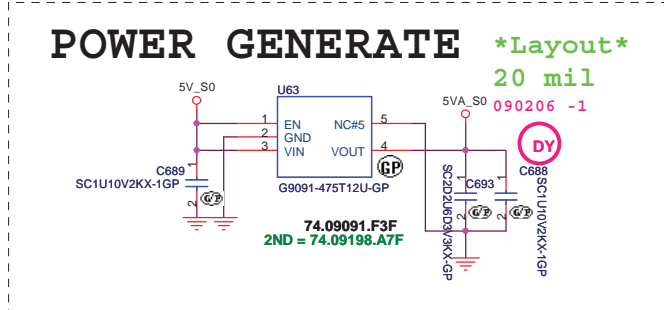
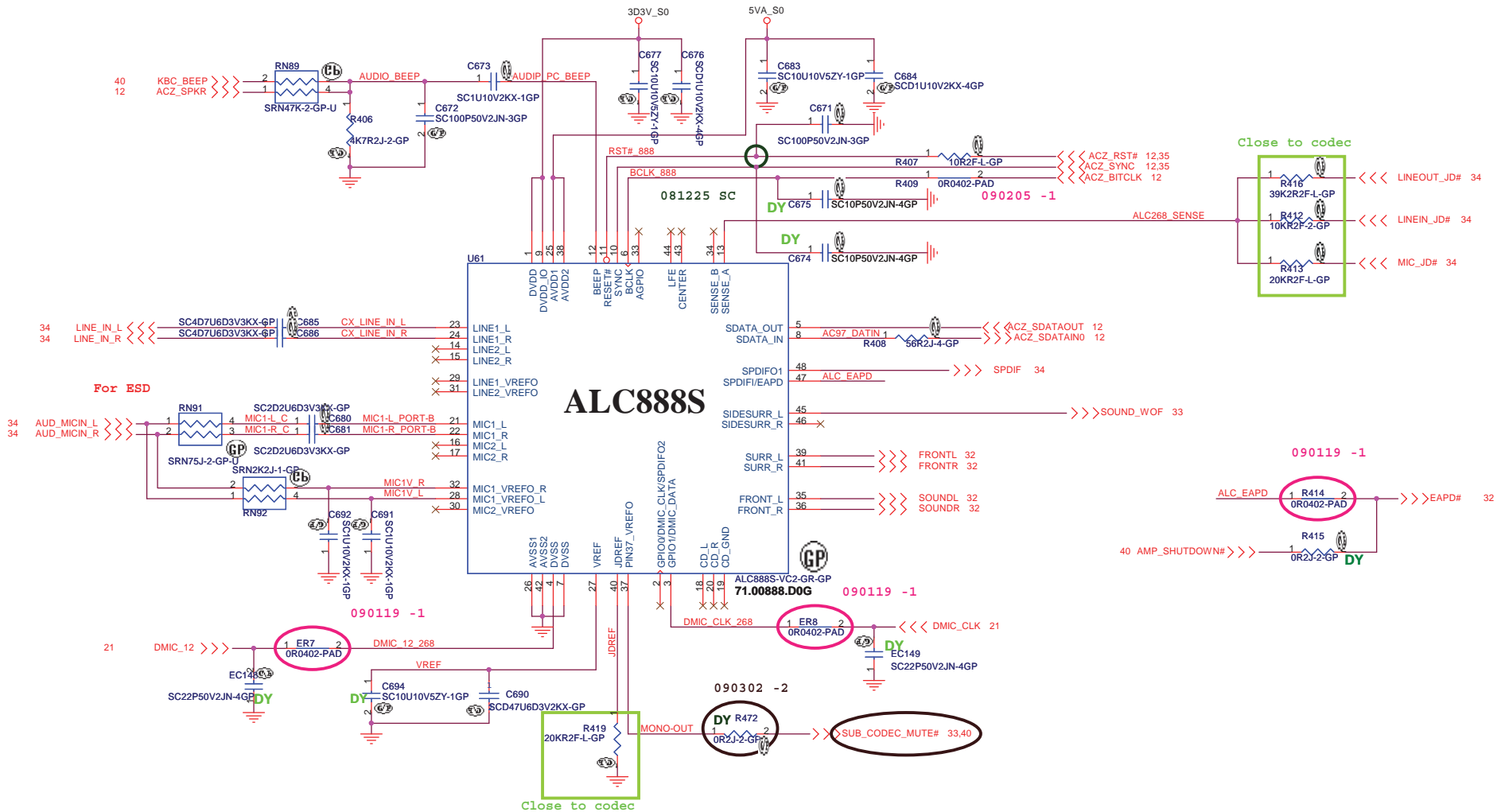
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

For EMI Near LAN1 CONN



<p><Core Design></p> <p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title LAN CONN</p>		
Size A4	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 30 of 56	

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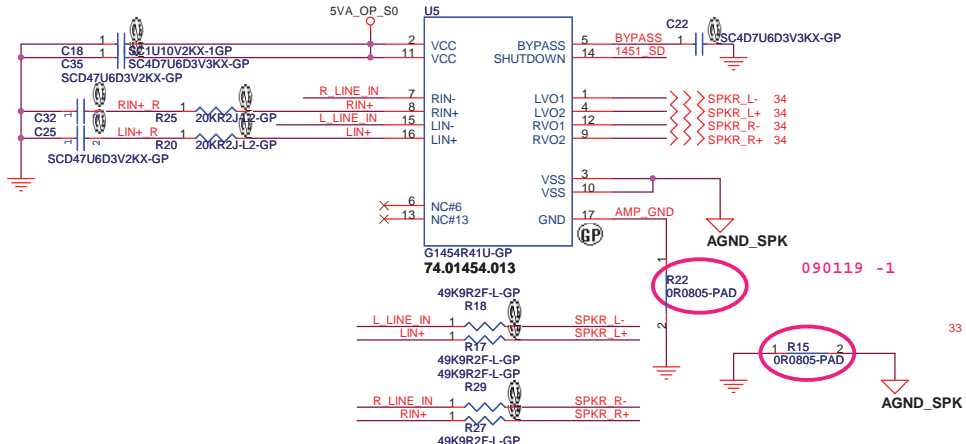
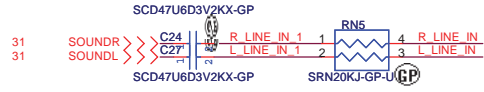
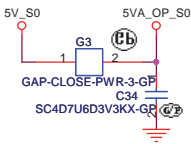


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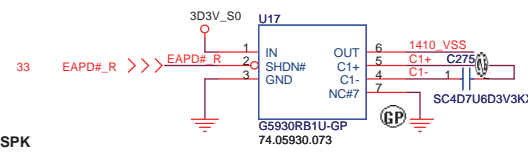
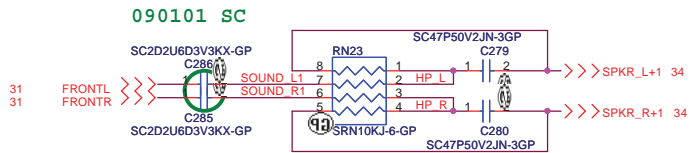
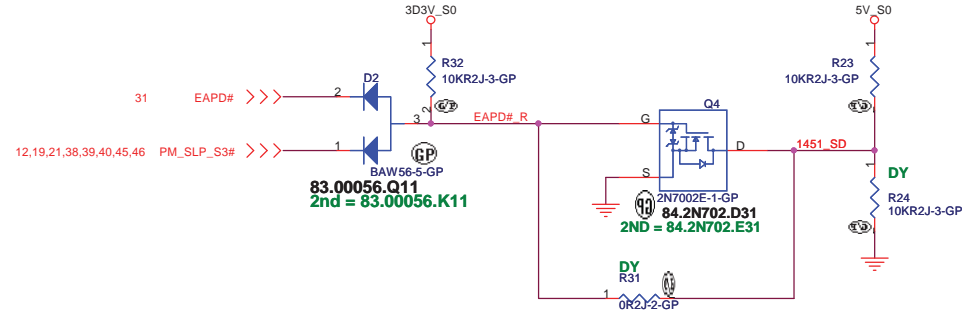
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緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Azalia codec ALC268	
Size A3	Document Number JM70-PU
Date: Friday, March 06, 2009	Rev -2
Sheet 31	of 56

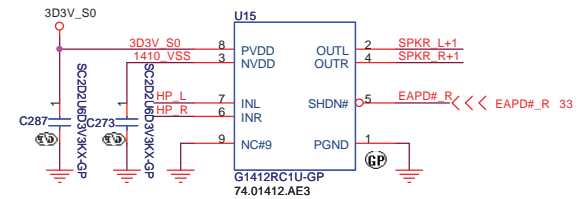
AUDIO OP AMPLIFIER



Gain= Rf/Ri=49.9K/20K=2.495V/V
 f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
 If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V
 V(rms)=2.828V
 Power= 2.828^2/4=1.999W



Gain= Rf/Ri=20K/18K=0.9V/V
 f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
 If VIN= 1.54V Gain=0.9V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
 Power= ?



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<Core Design>

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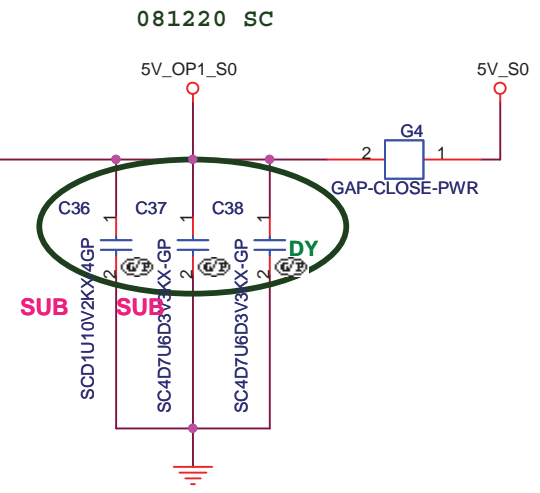
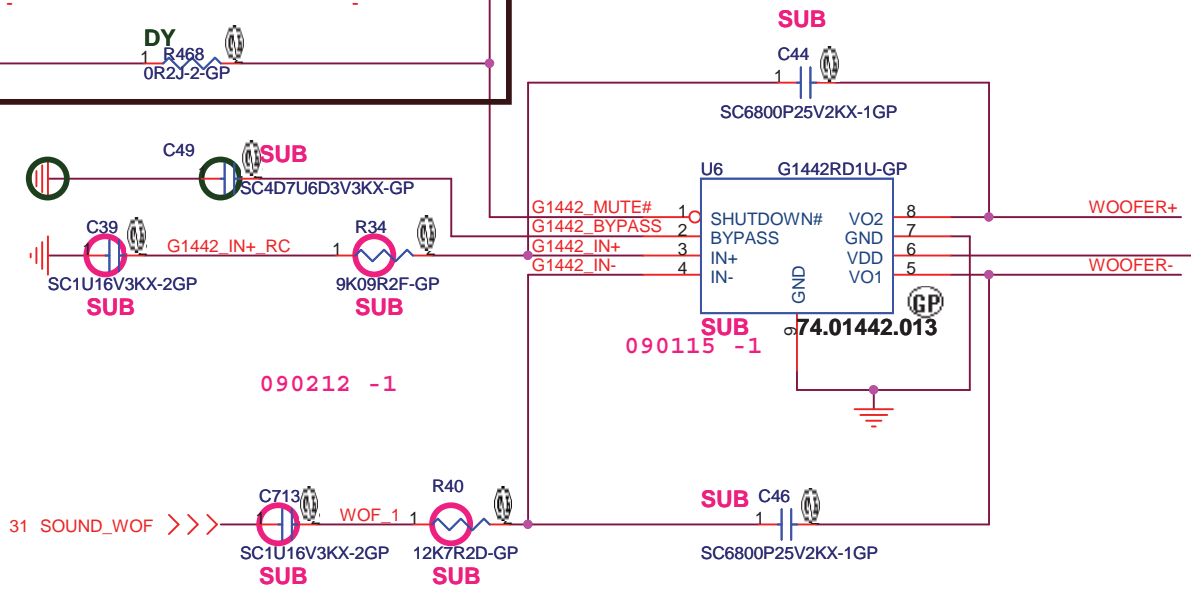
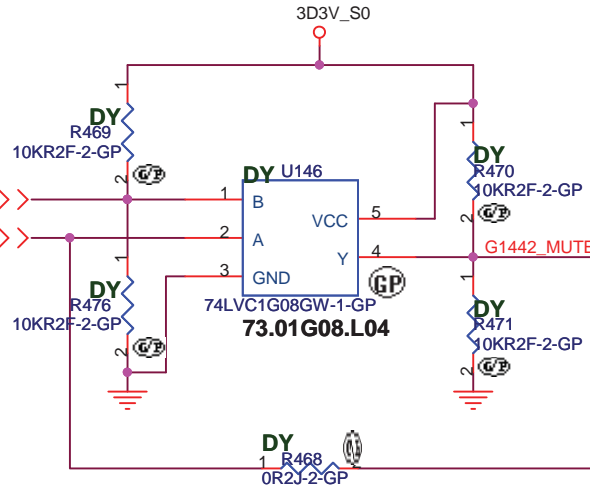
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Size: **A3** Document Number: **JM70-PU** Rev: **-2**

Date: **Friday, March 06, 2009** Sheet: **32** of **56**

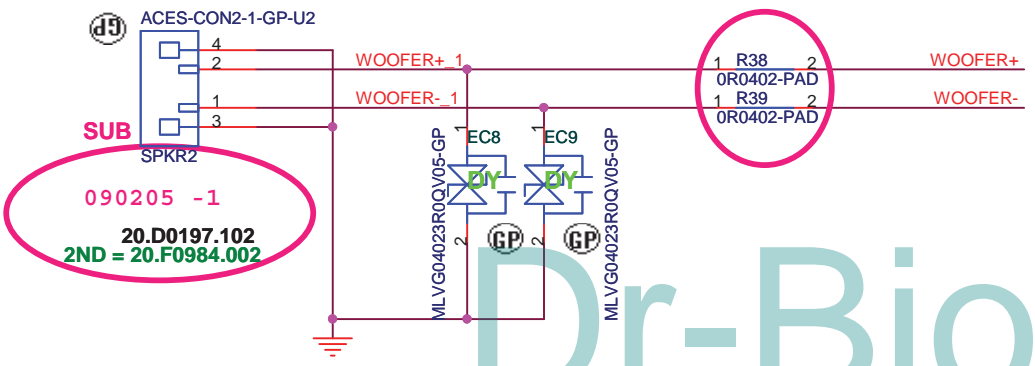
090305 -2

31, 30 SUB_CODEC_MUTE# >>>
32 EAPD#_R >>>



SUBWOOFER CONN.

090119 -1

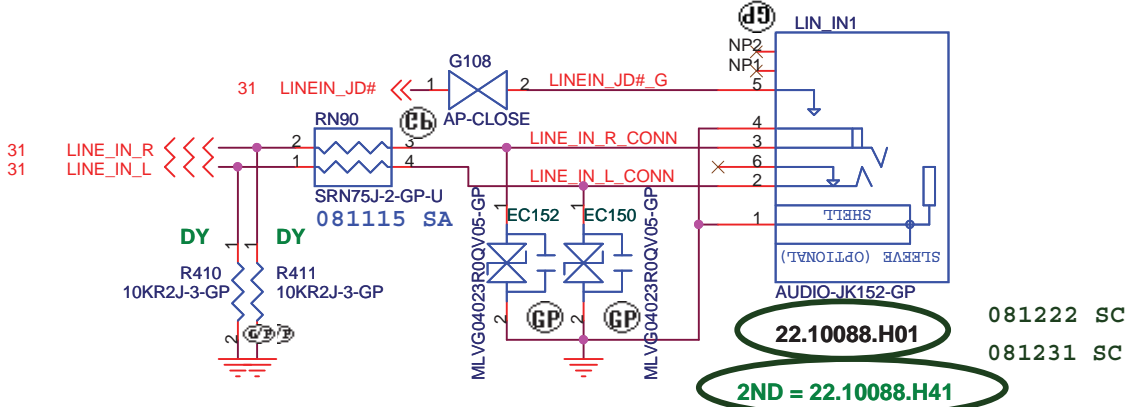


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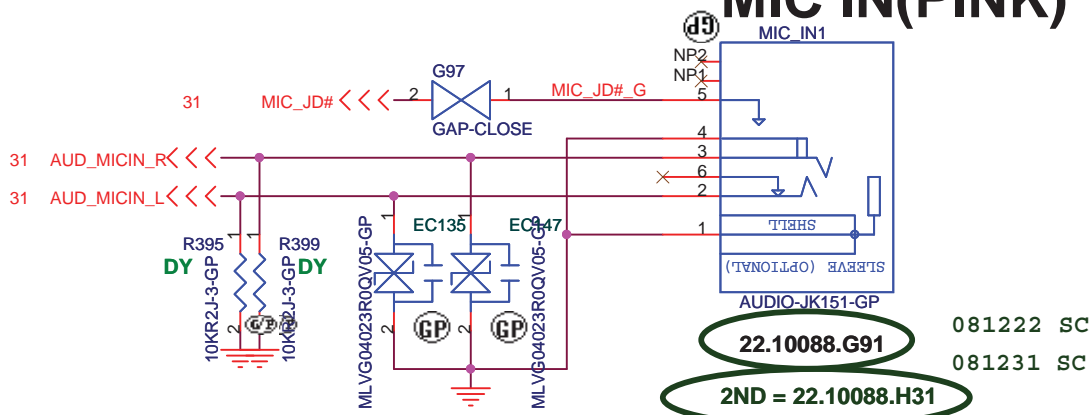
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio AMP for Subwoofer			
Size A4	Document Number	JM70-PU	
Date: Friday, March 06, 2009	Sheet 33	of	Rev -2

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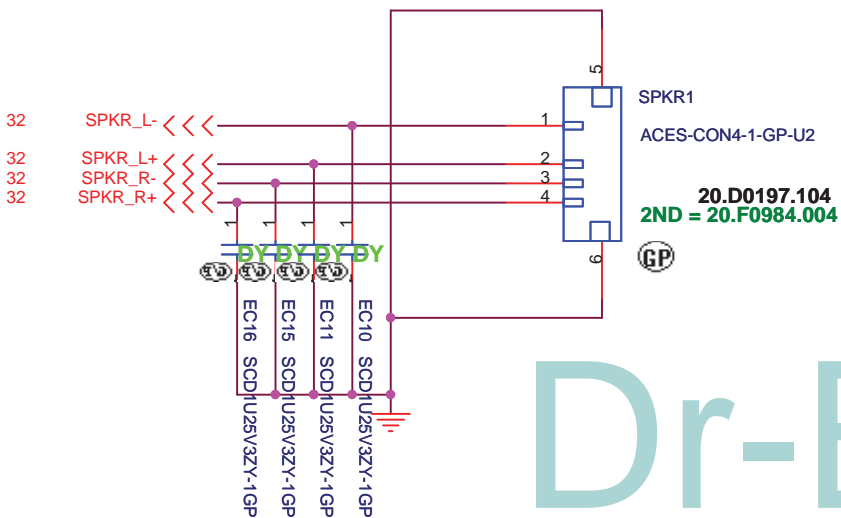
LINE IN(BLUE)



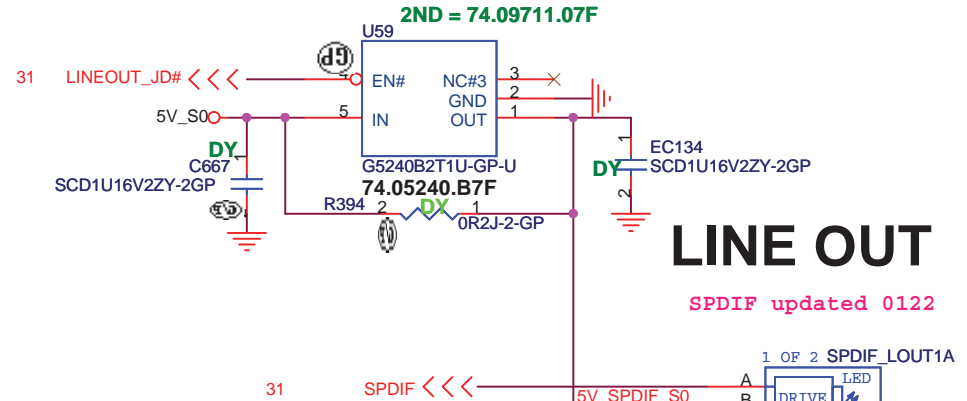
MIC IN(PINK)



REAR Speaker



2ND = 74.09711.07F



LINE OUT

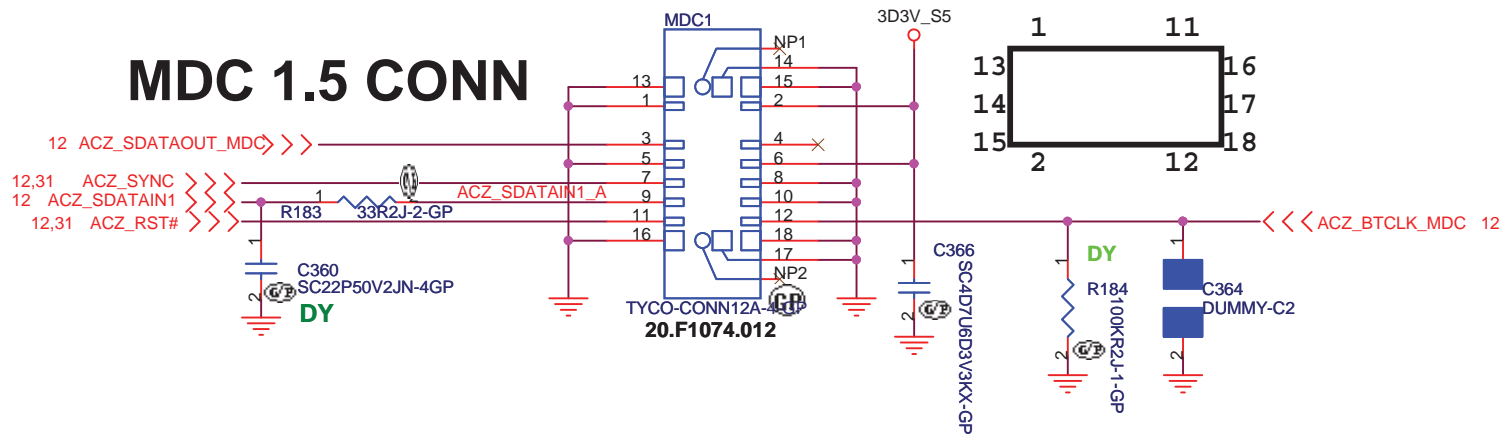
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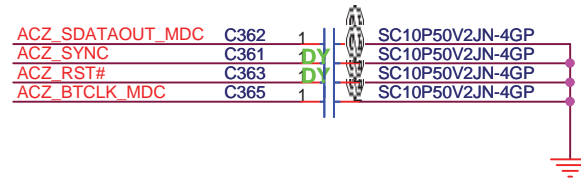
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Title AUDIO JACK			
Size A4	Document Number JM70-PU		Rev -2
Date: Friday, March 06, 2009	Sheet 34 of		56

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MDC 1.5 CONN



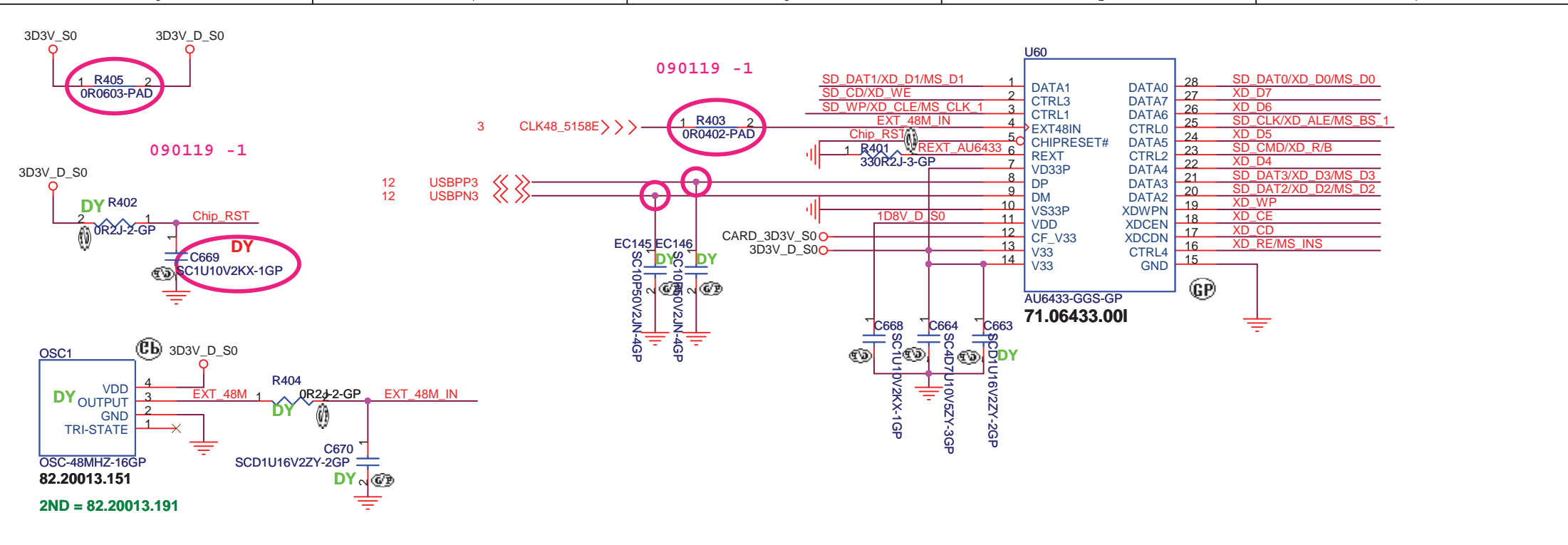
090211 -1 EMI
Stuff C362,C365 (10P)



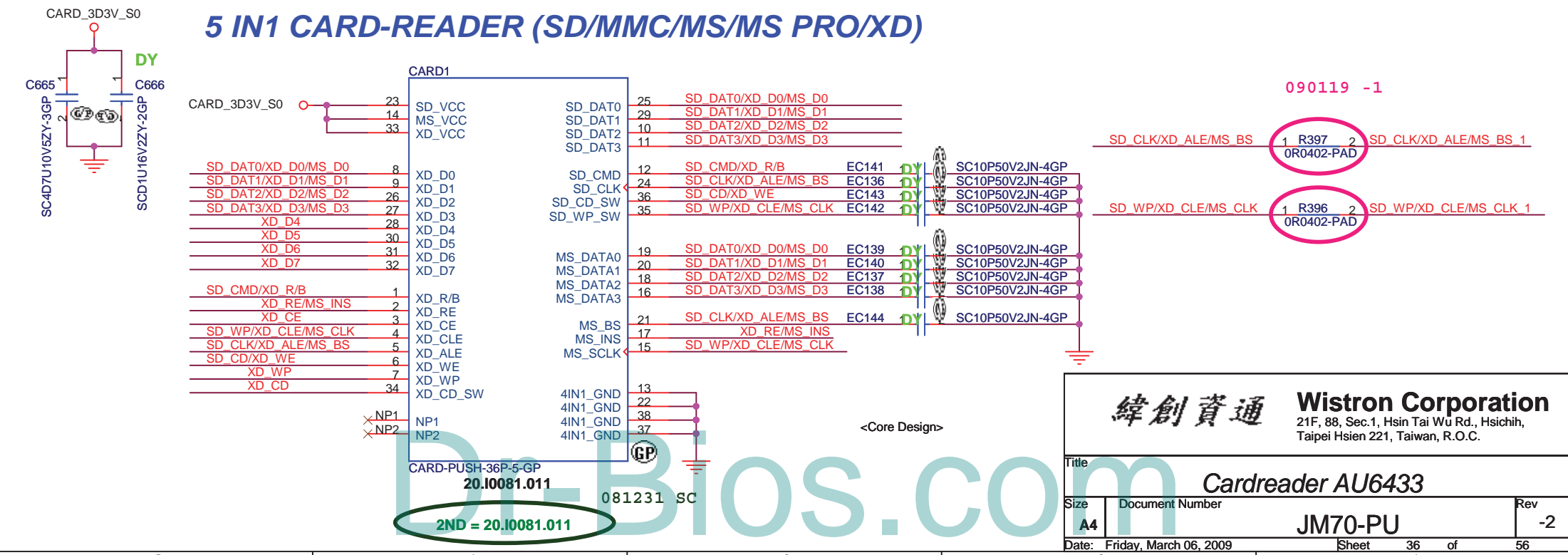
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 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
MDC	
Size	Document Number
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5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



緯創資通 Wistron Corporation
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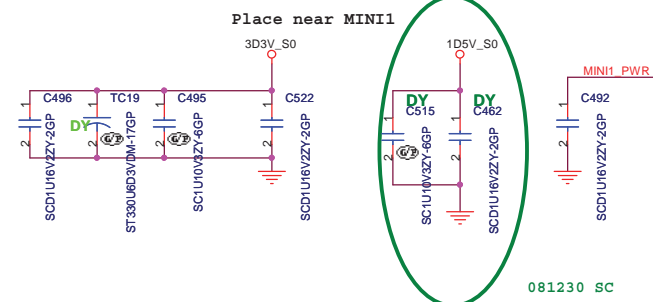
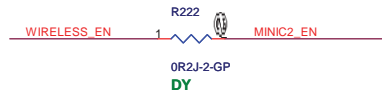
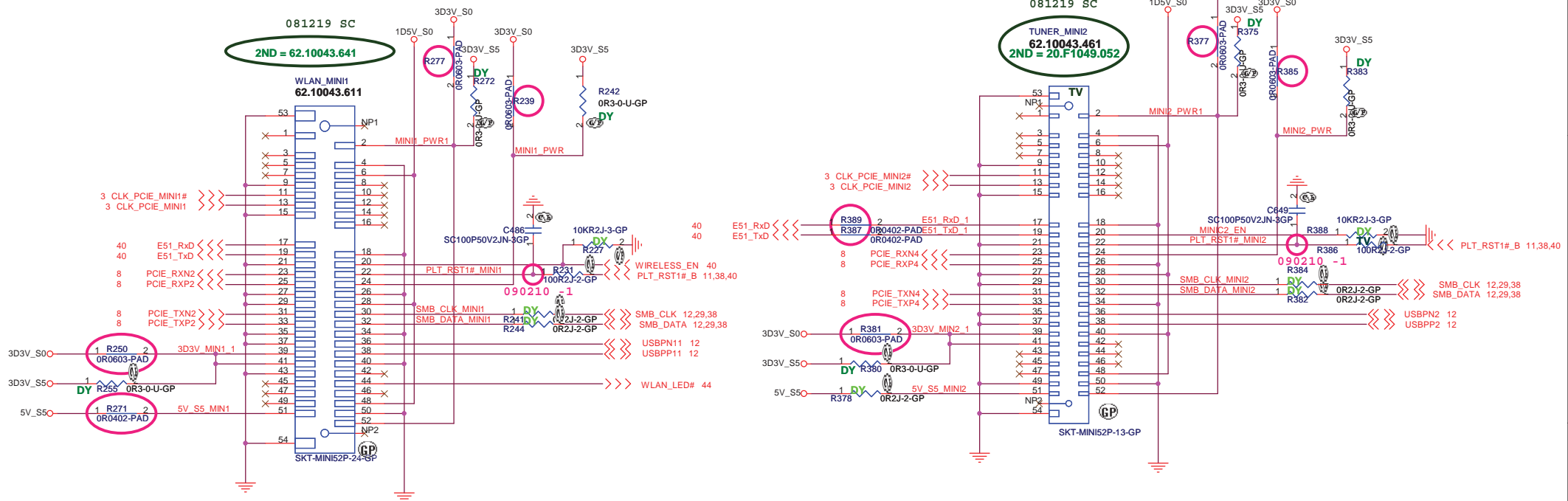
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Size	Document Number		Rev		
A4	JM70-PU				-2
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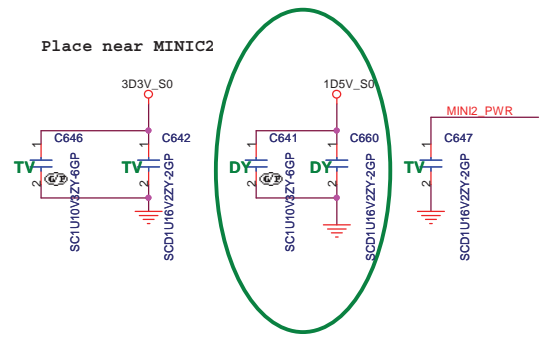
2ND = 20.10081.011

Mini2 Card Connector(TV tuner)

Mini1 Card Connector(WLAN) Support debug-card 090119 -1



081230 SC



081230 SC

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<Core Design>

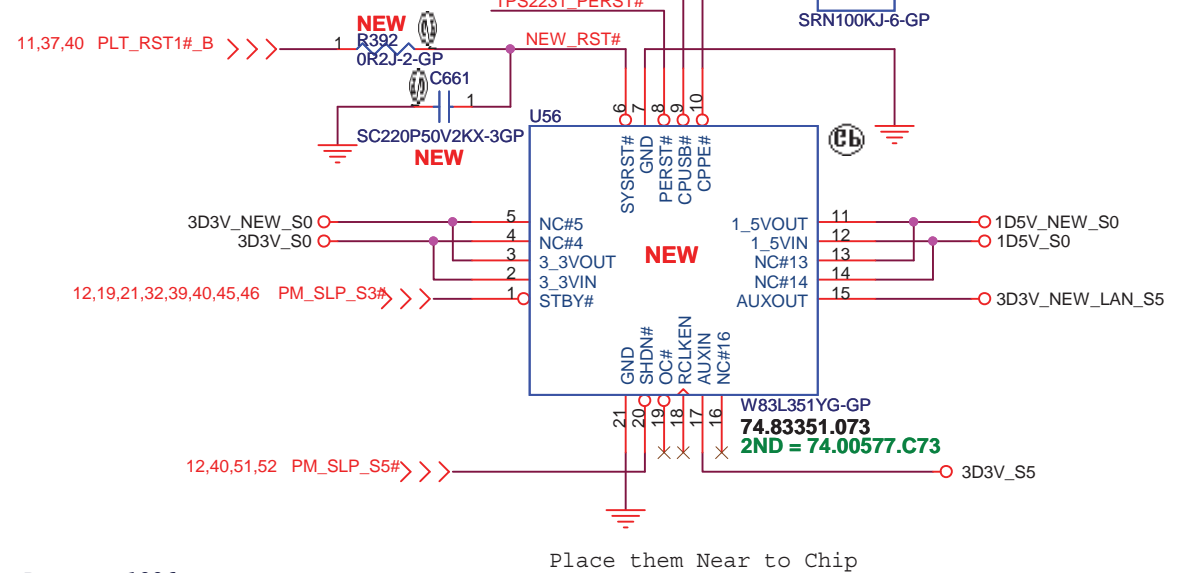
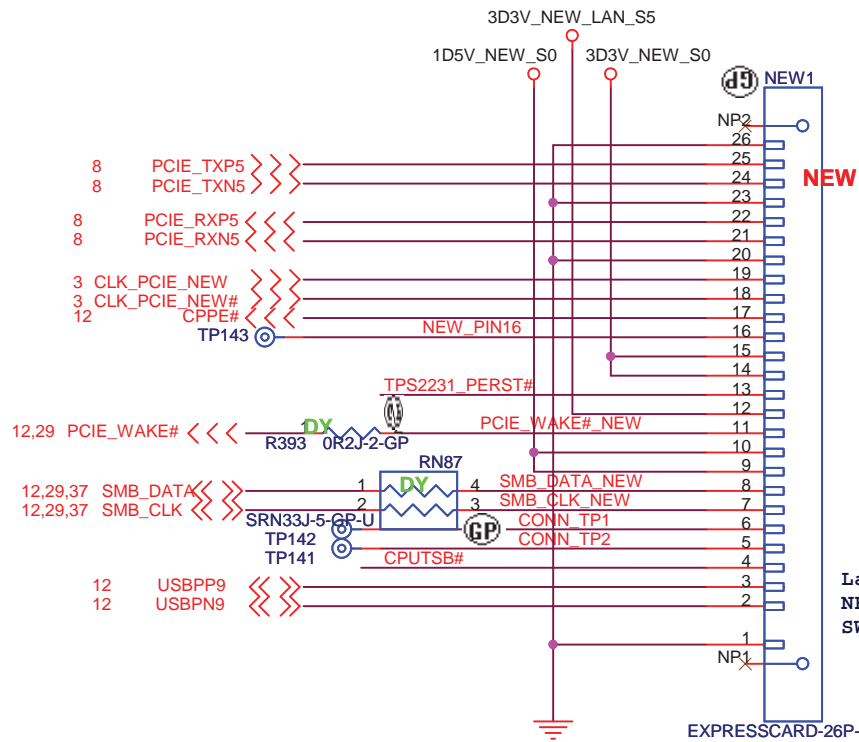
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Mini Card**

Size: A3	Document Number: JM70-PU	Rev: -2
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NEWCARD Connector

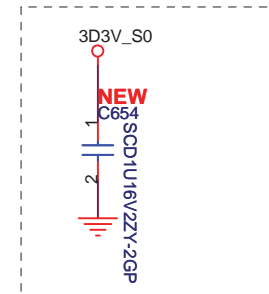
ENG stage without NEW card function 12/22



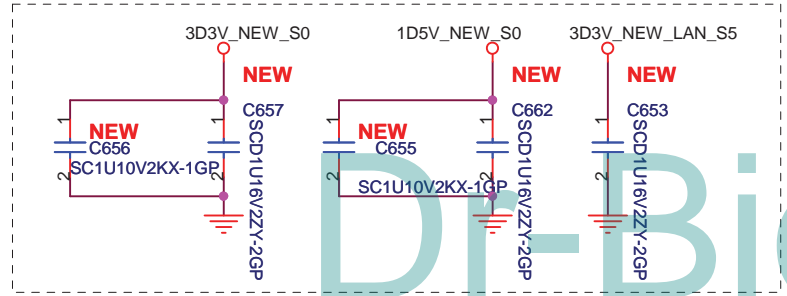
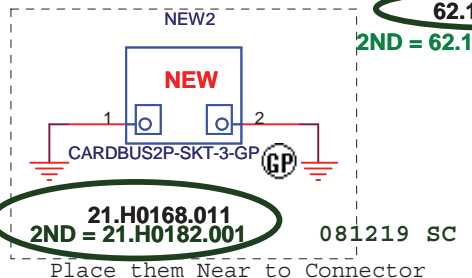
Layout Request 1226
NEW1 & NEW2
SWAP 1st & 2nd

74.00577.C73
new card power switch
GMT cost down solution

Place them Near to Chip



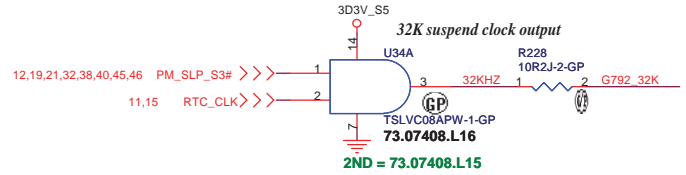
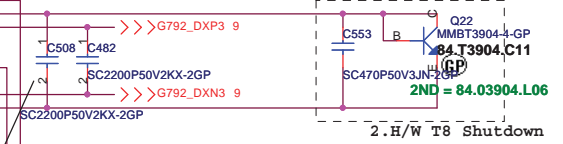
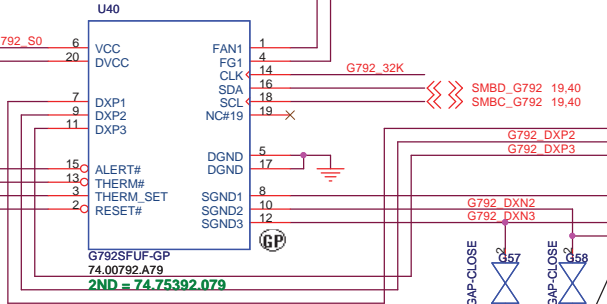
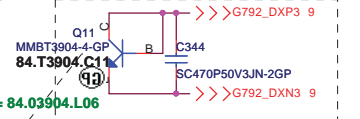
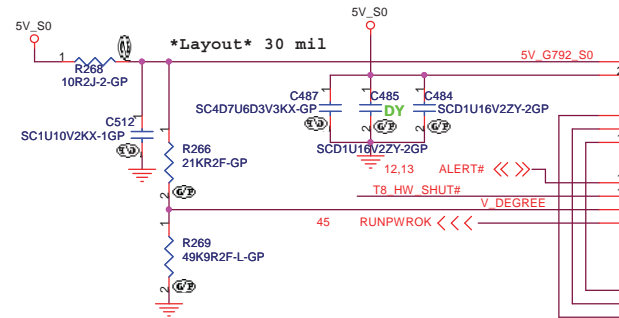
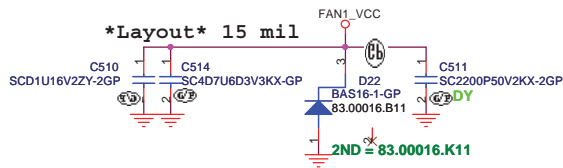
TOP VIEW



<Core Design>

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Title NEW CARD		
Size A4	Document Number JM70-PU	Rev -2
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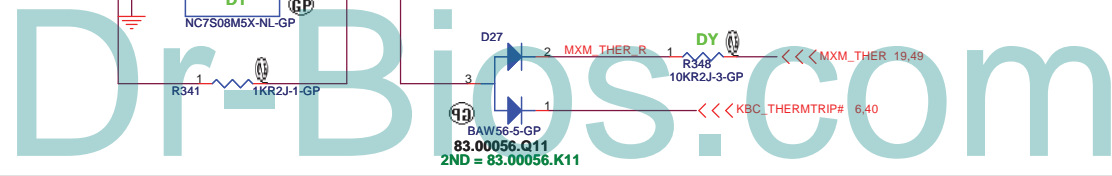
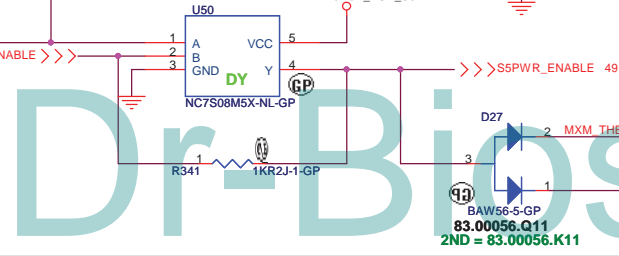
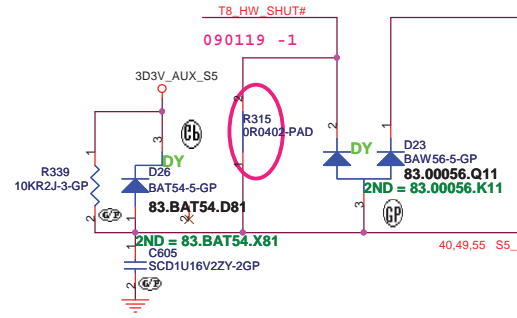
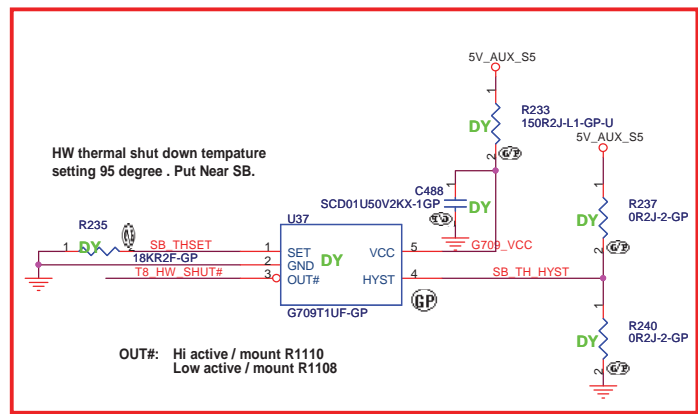
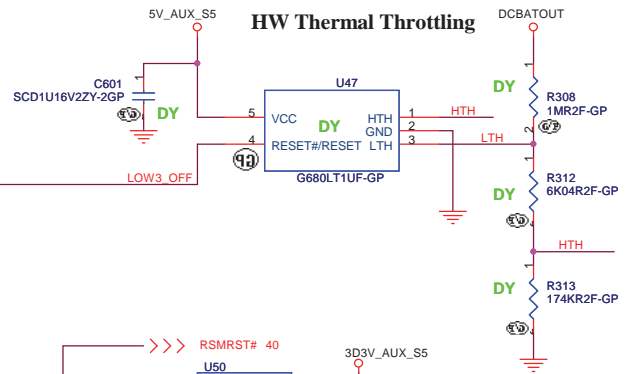


DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close as possible

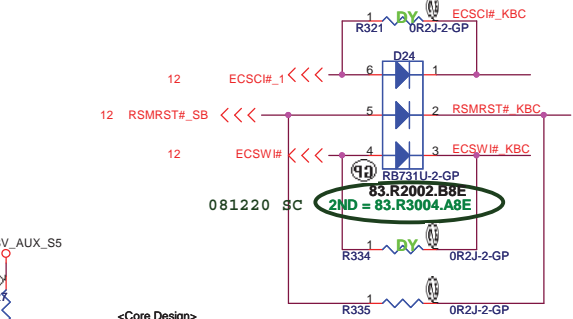
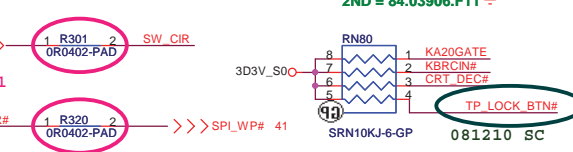
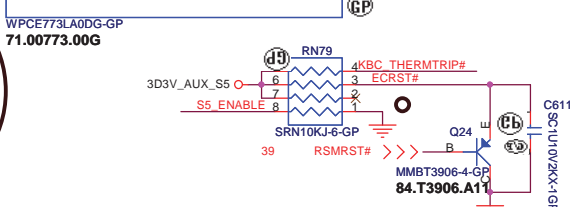
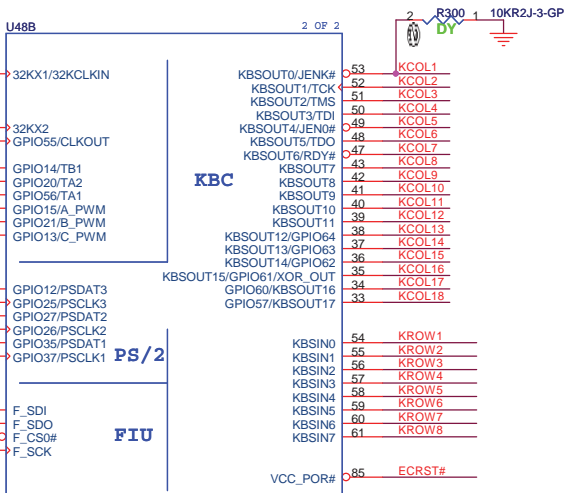
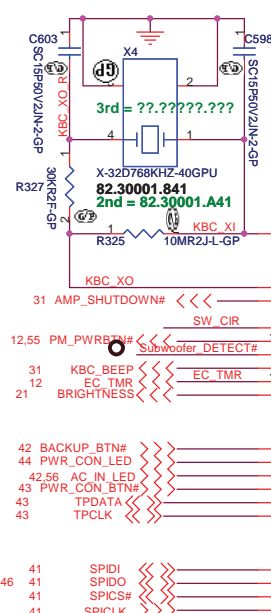
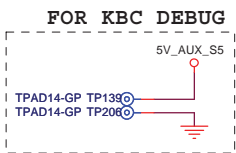
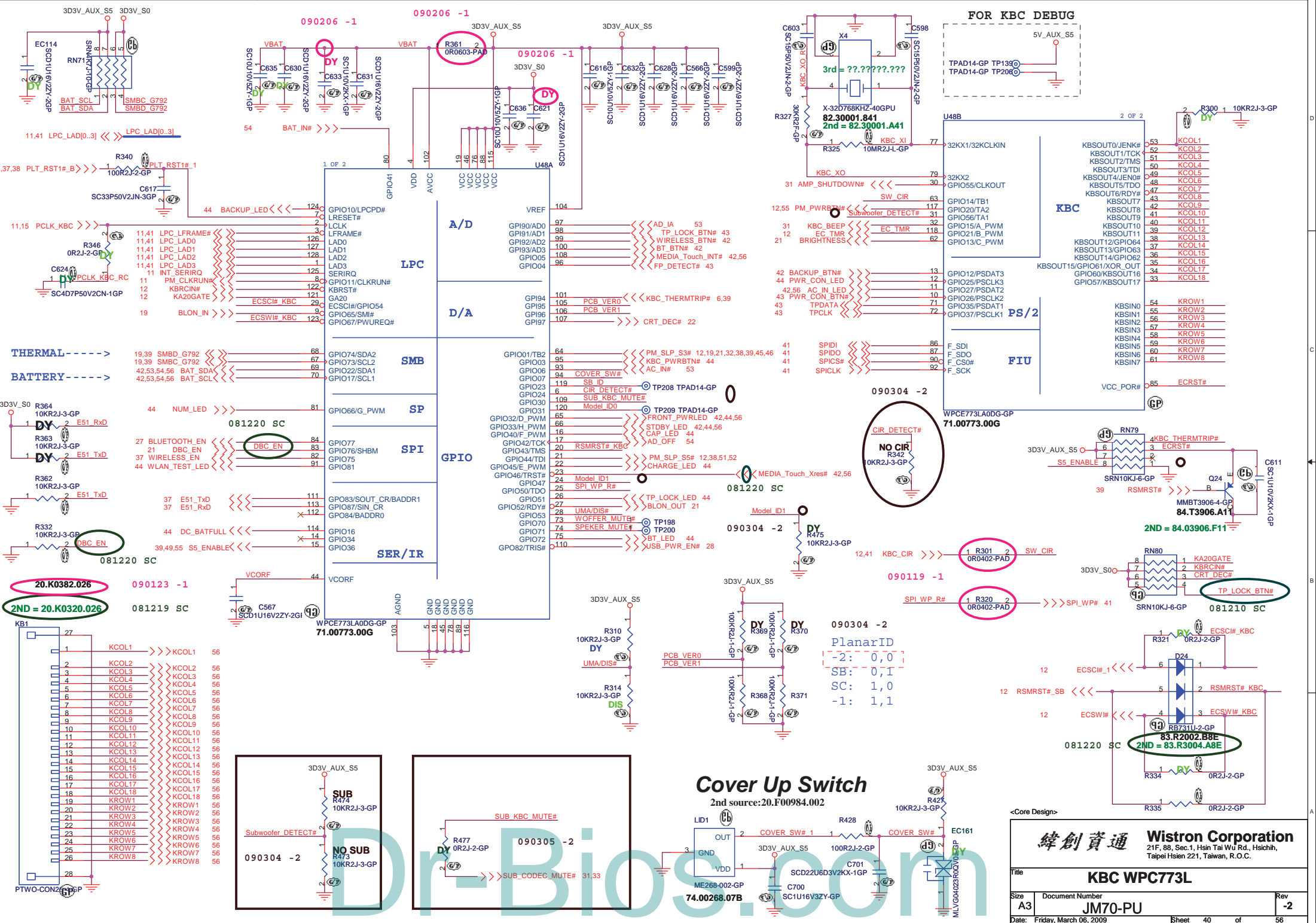
BL3#

HW Thermal Throttling



<Core Design>

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G792			
Title	Document Number	Rev	
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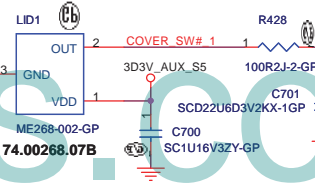


Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

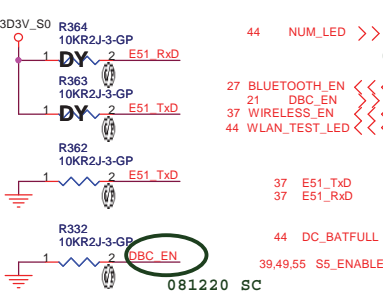
KBC WPC773L

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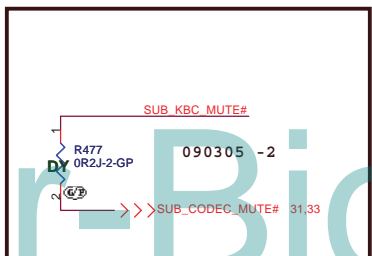
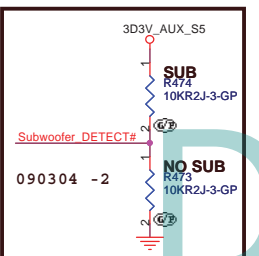
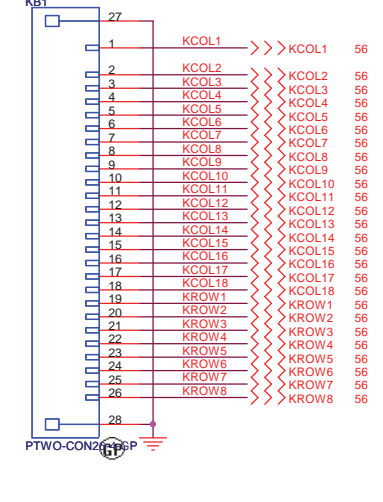
Cover Up Switch
2nd source: 20.F00984.002



THERMAL----->>>>
BATTERY----->>>>

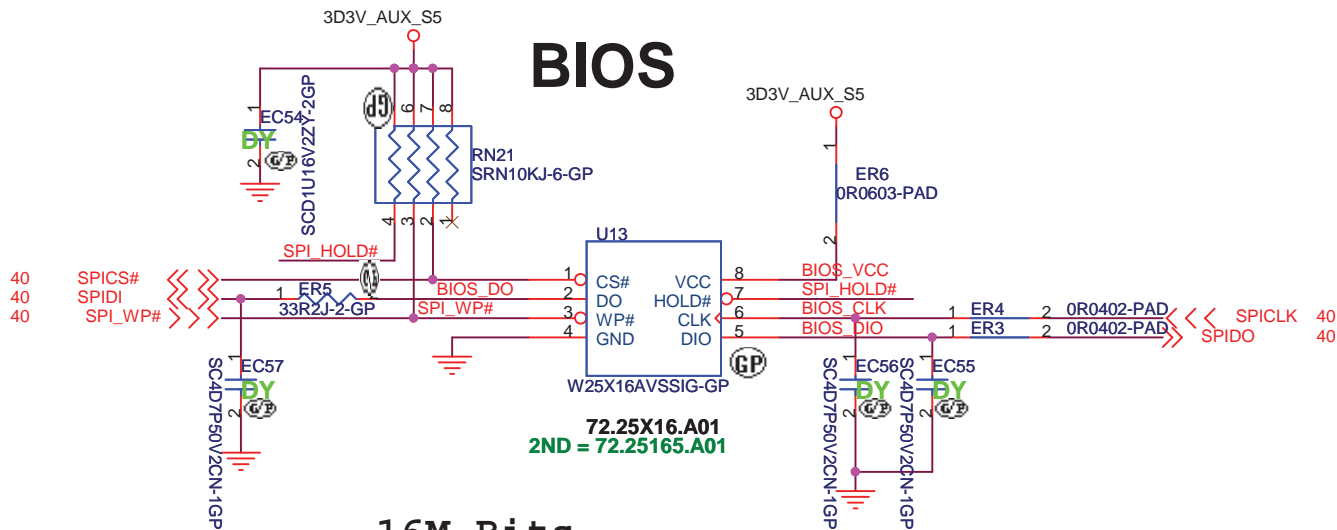


20.K0382.026 090123 -1
2ND = 20.K0320.026 081219 SC



74.00268.07B

BIOS

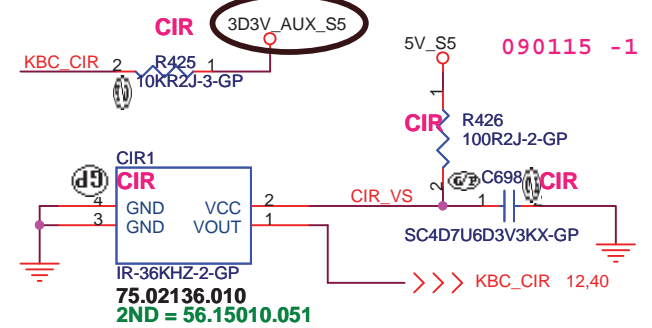


**16M Bits
SPI FLASH ROM**

**72.25X16.A01
2ND = 72.25165.A01**

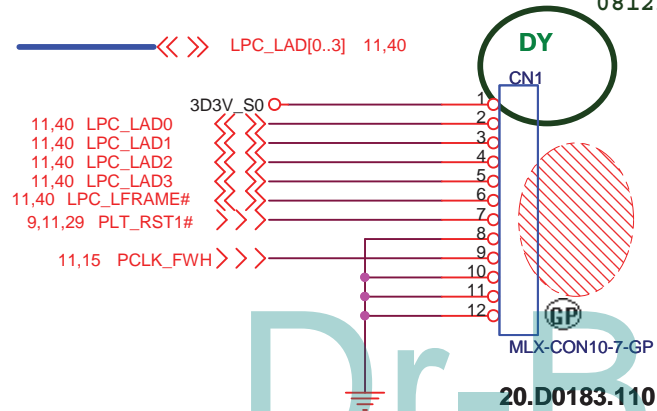
CIR Module

090304 -2



GOLDEN FINGER FOR DEBUG BOARD

081225 SC

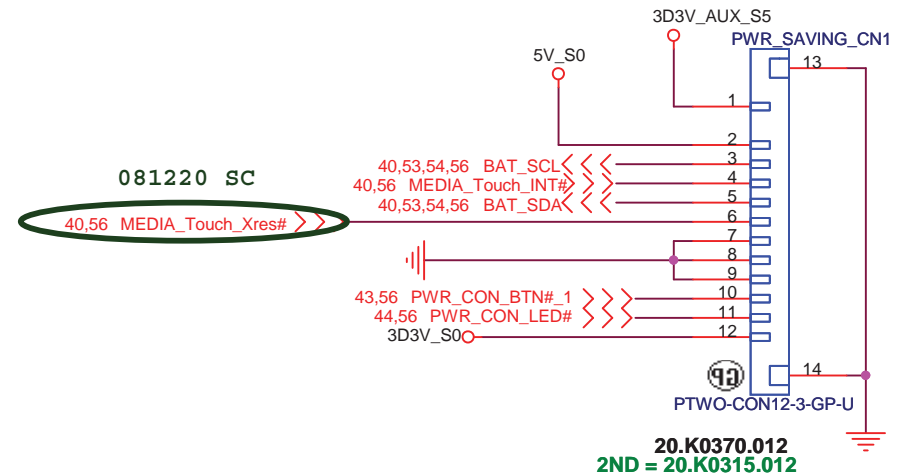
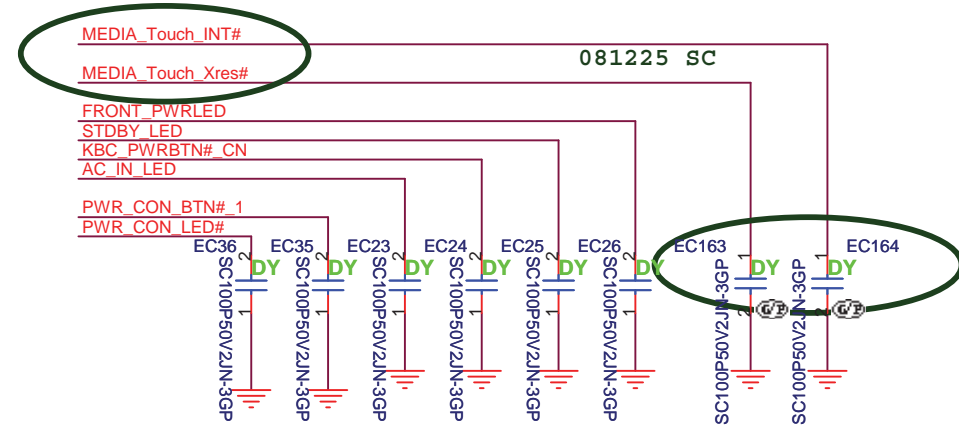
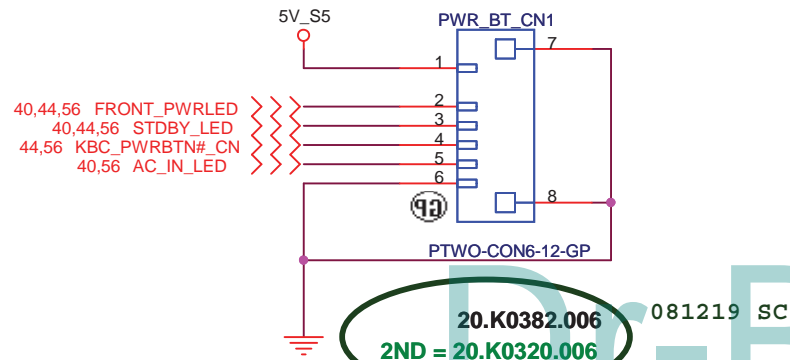
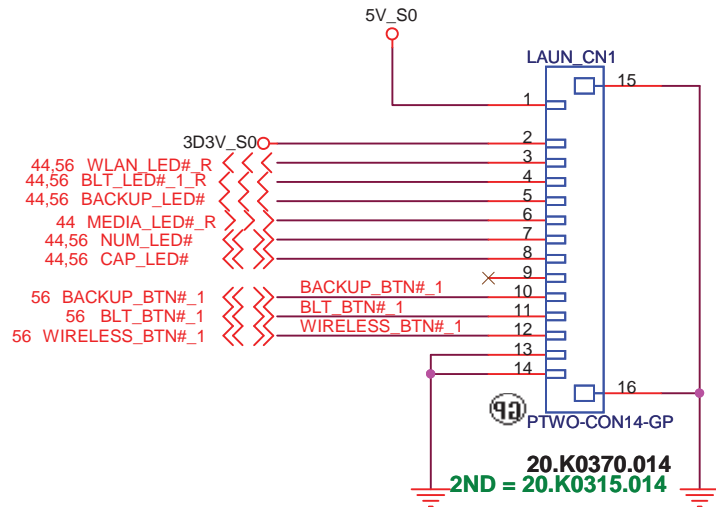
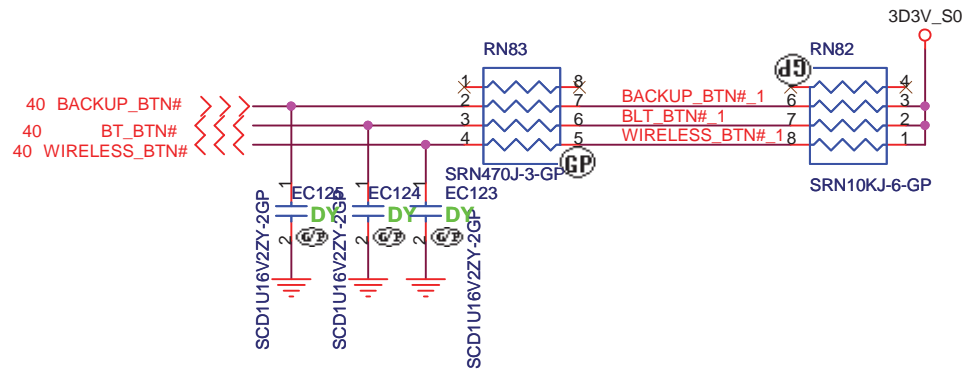


<Core Design>

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BIOS & CIR			
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LAUNCH



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LAUNCH & LID

Size
A4

Document Number

JM70-PU

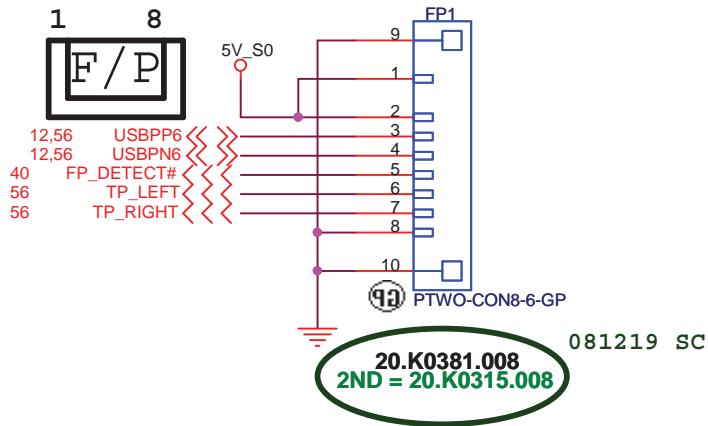
Rev
-2

Date: Friday, March 06, 2009

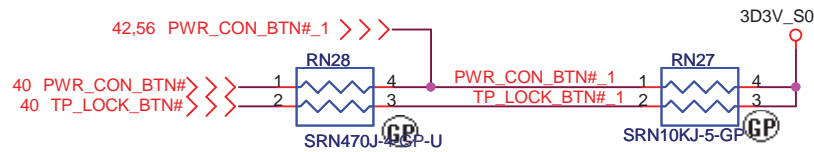
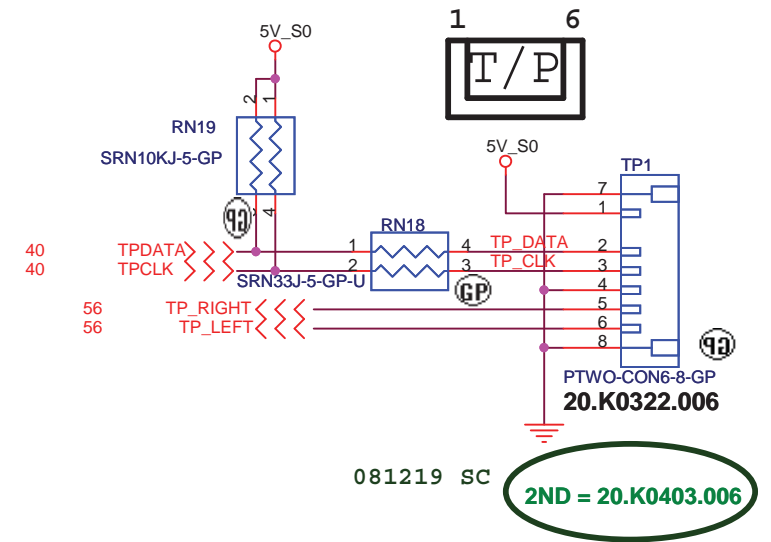
Sheet 42 of 56

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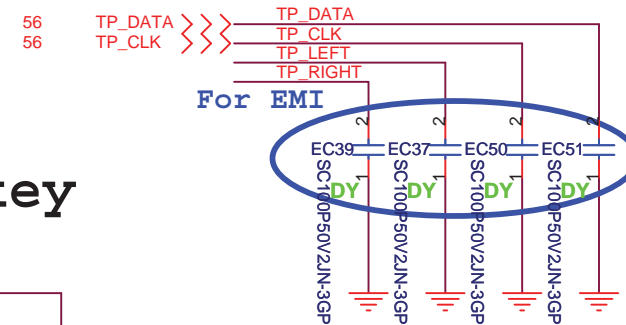
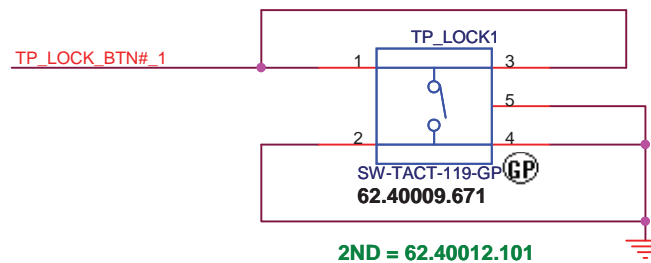
Finger printer



TOUCH PAD



TP_LOCK key

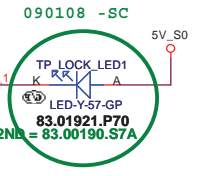
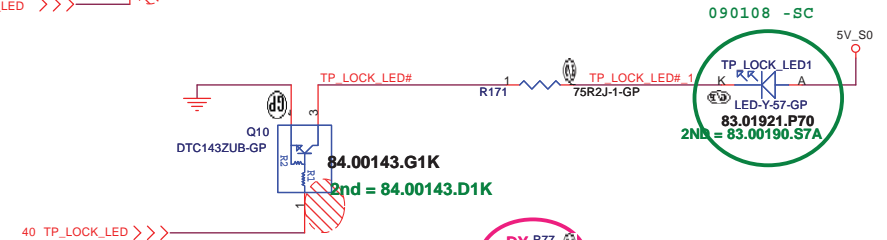
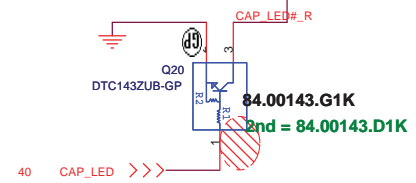
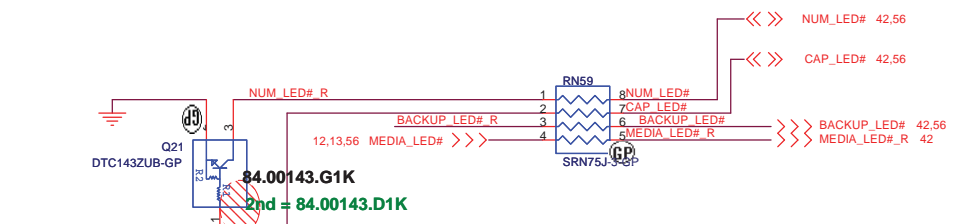
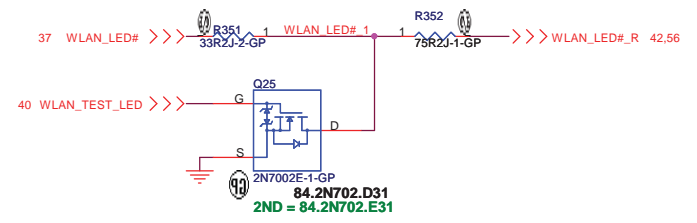
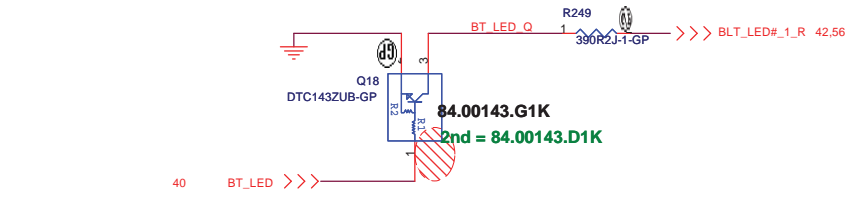
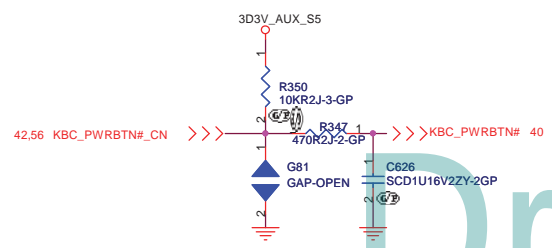
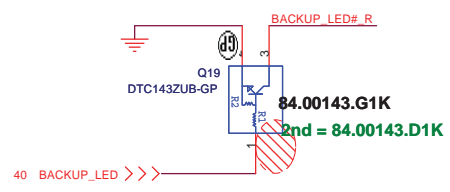
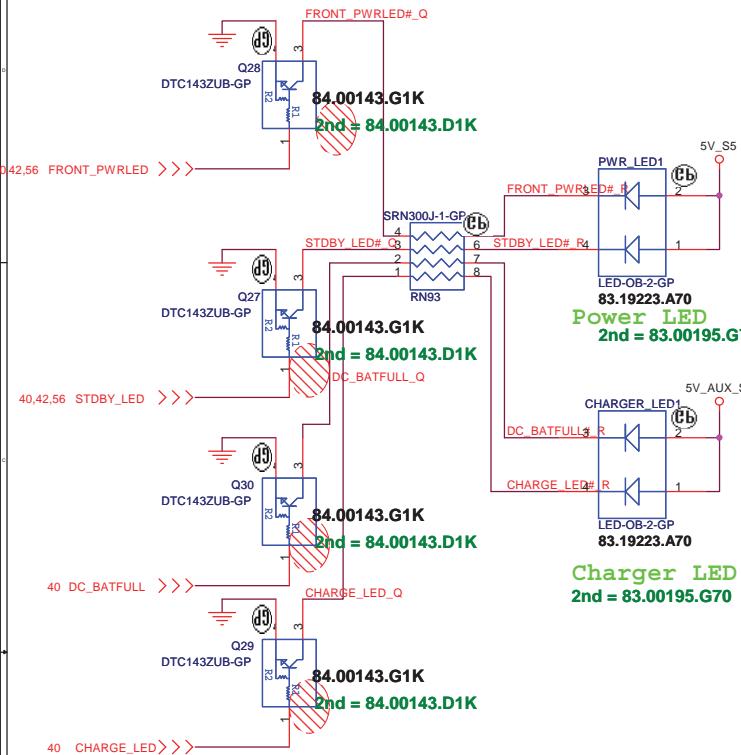


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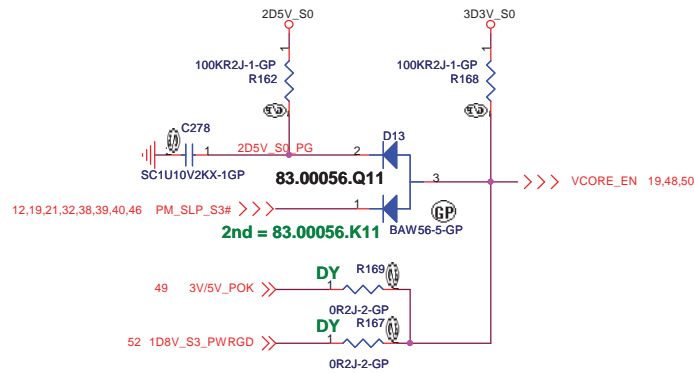
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Finger Printer			
Size	Document Number		Rev
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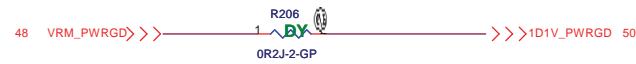
LED



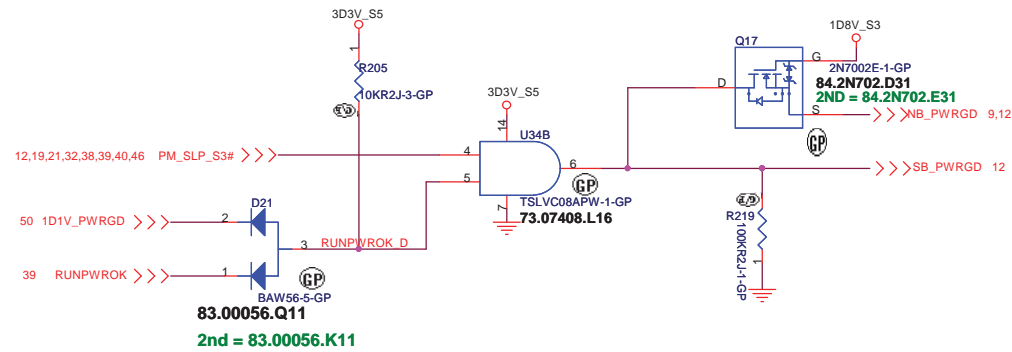
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P/H @ 1D8V_S3 PAGE



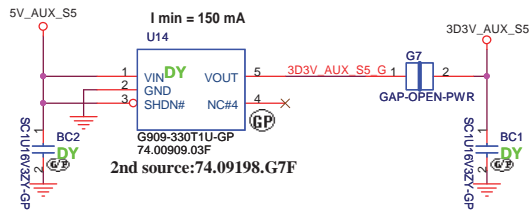
Reference schematic recommend



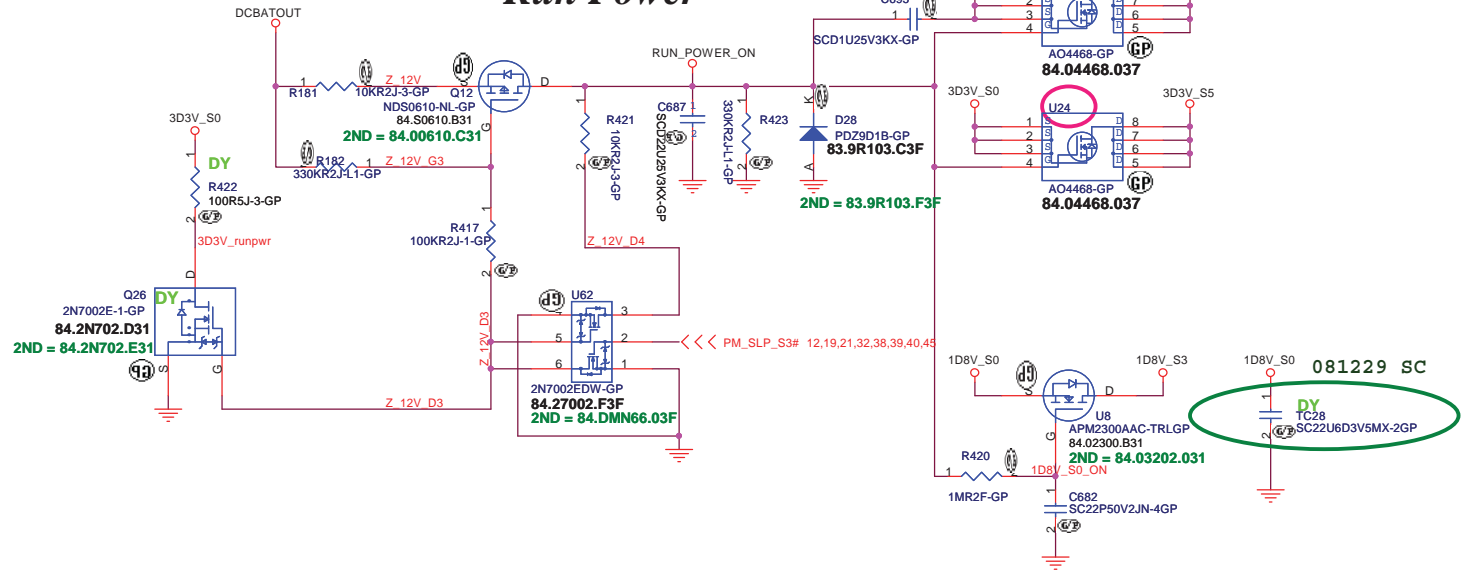
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<Core Design>		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.		
Title POWER ON LOGIC		
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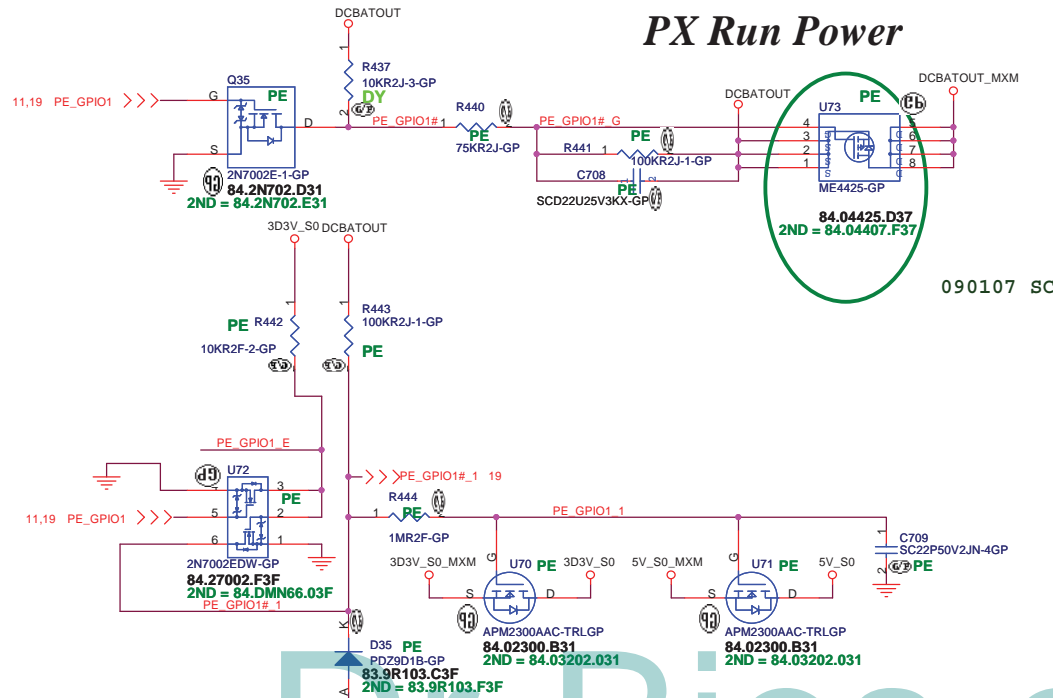
Aux Power 3D3V_AUX_S5



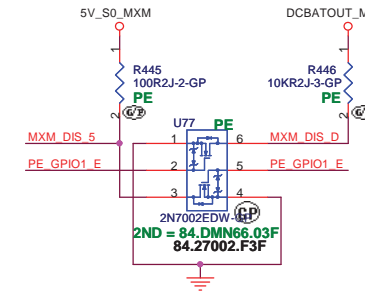
Run Power



PX Run Power

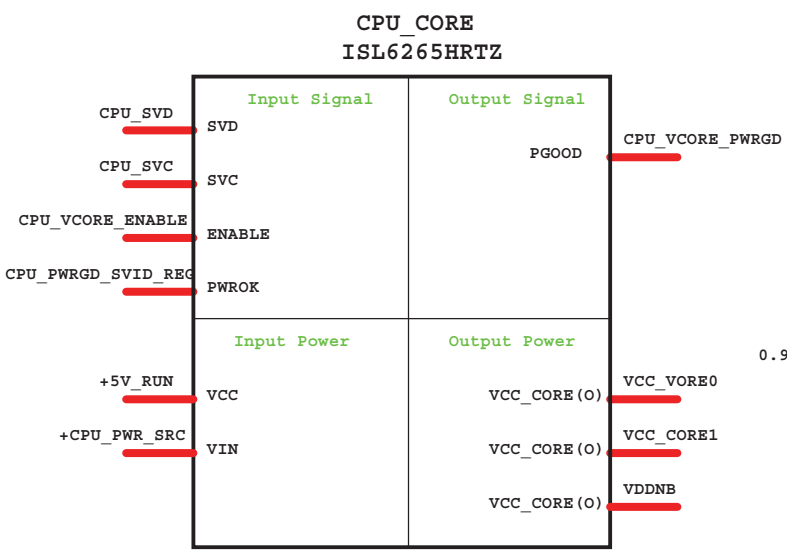
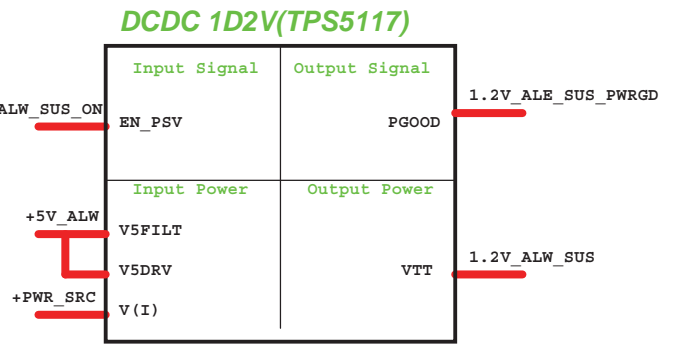
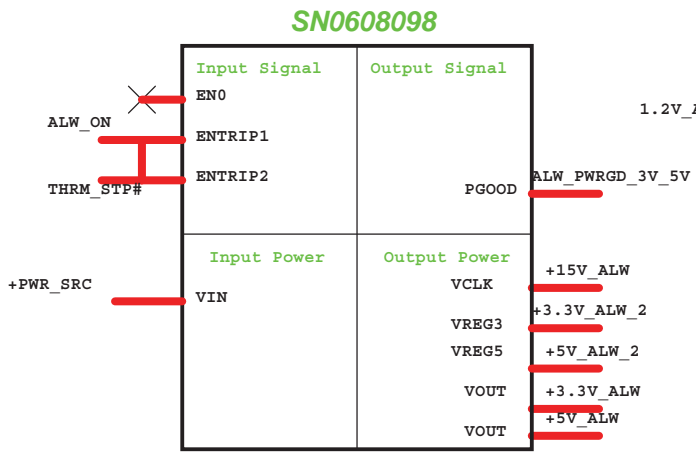
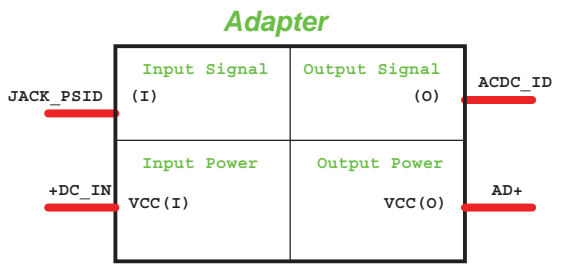


PX Run Power Discharge circuit

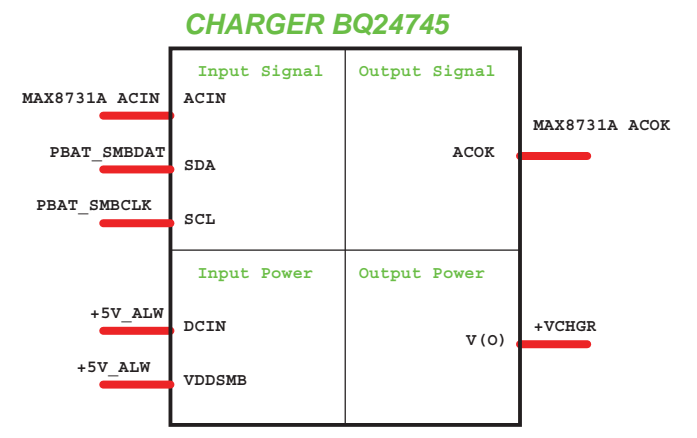
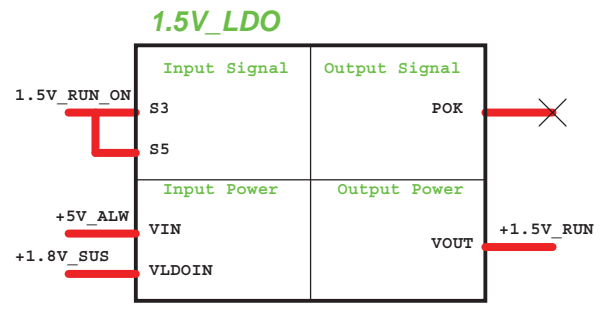
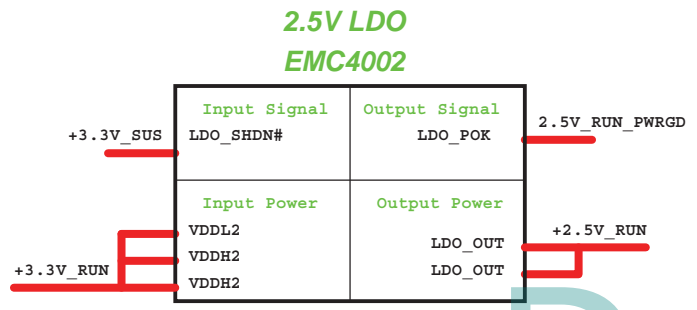
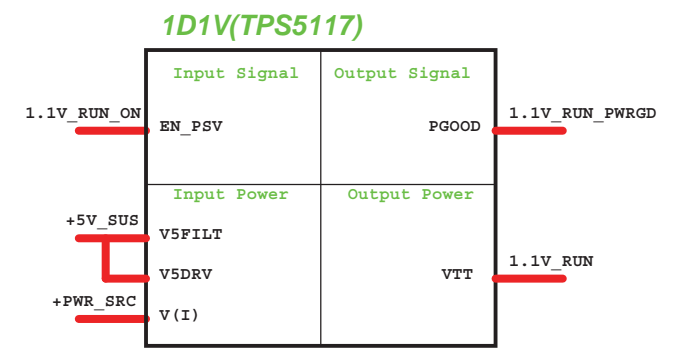
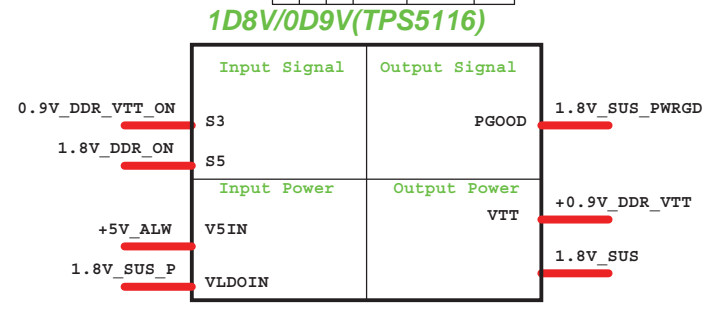


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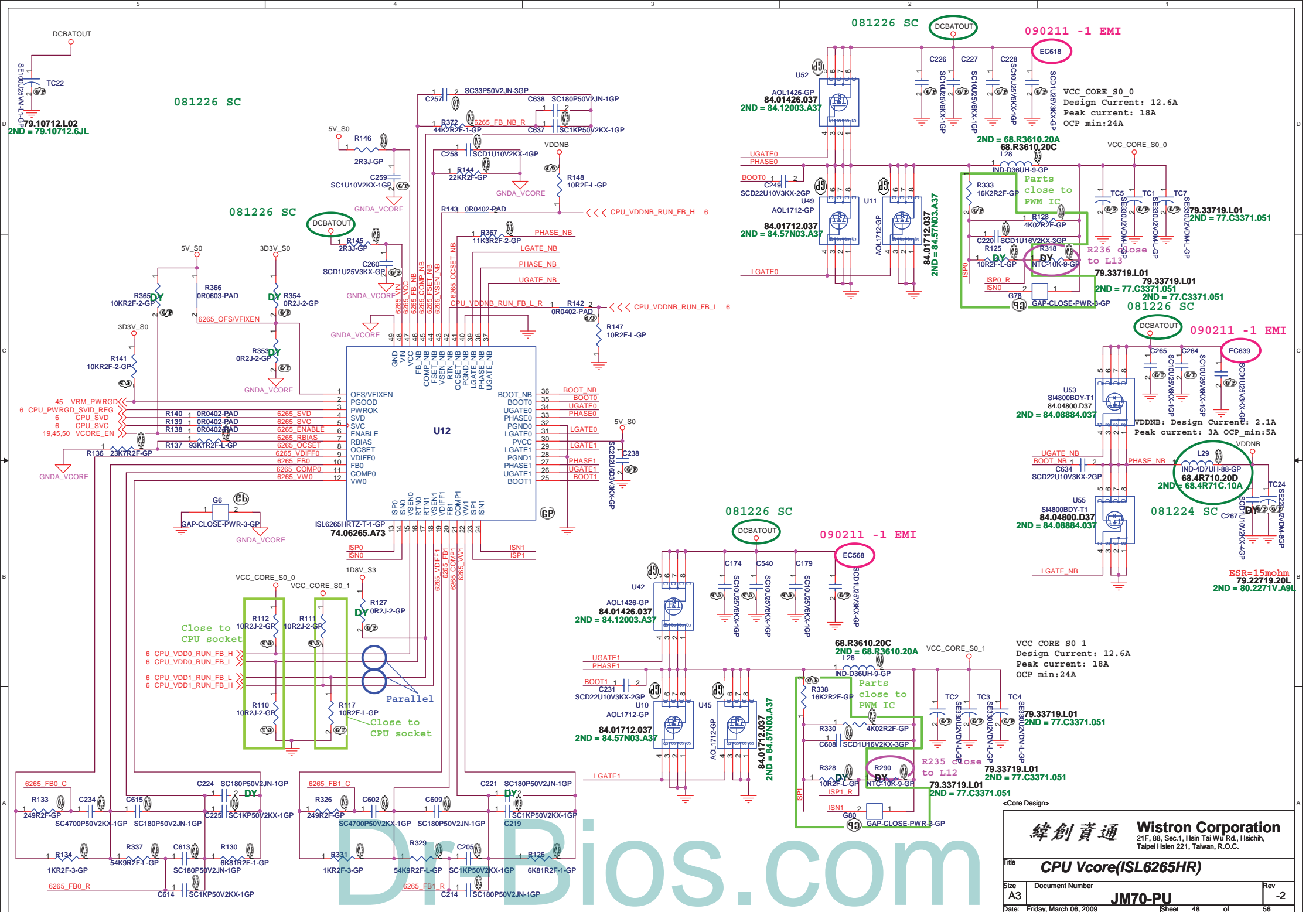
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緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.		
Title RUN POWER and 3D3V_AUX_S5		
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	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	1	1	1
S3					
S4	0	0	0	0	0
S5					



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79.10712.L02
2ND = 79.10712.GJL

081226 SC

081226 SC

081226 SC

090211 -1 EMI

AOL1426-GP
84.01426.037
2ND = 84.12003.A37

2ND = 68.R3610.20A
68.R3610.20C

AOL1712-GP
84.01712.037
2ND = 84.57N03.A37

84.01712.037
2ND = 84.57N03.A37

79.33719.L01
2ND = 77.C3371.051

090211 -1 EMI

S4800BDY-T1
84.04800.D37
2ND = 84.08884.037

IND-4D7UH-88-GP
68.4R71C.10A
2ND = 68.4R71C.10A

081226 SC

090211 -1 EMI

AOL1426-GP
84.01426.037
2ND = 84.12003.A37

68.R3610.20C
2ND = 68.R3610.20A

AOL1712-GP
84.01712.037
2ND = 84.57N03.A37

84.01712.037
2ND = 84.57N03.A37

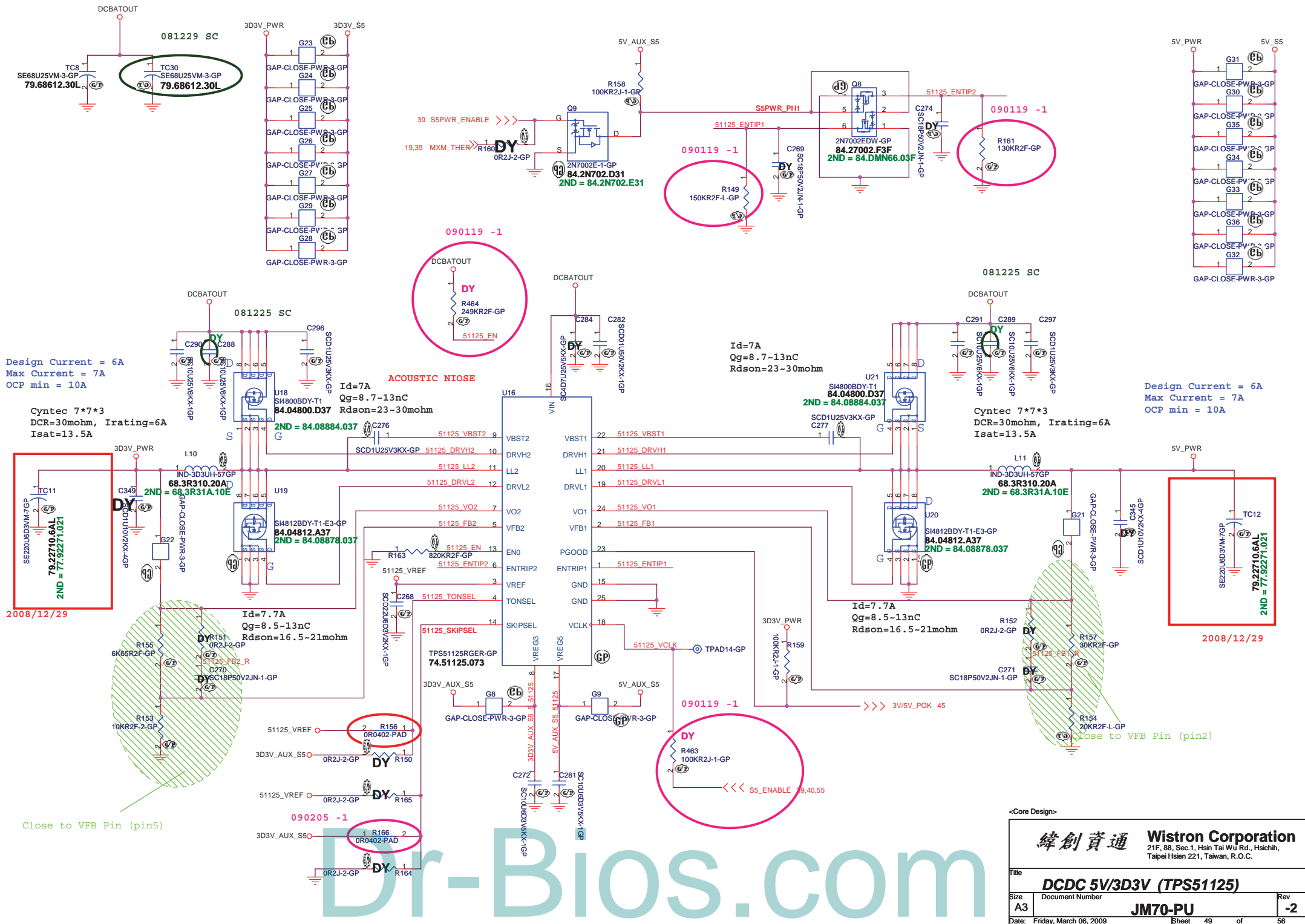
79.33719.L01
2ND = 77.C3371.051

79.33719.L01
2ND = 77.C3371.051

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU Vcore(ISL6265HR)	
Size	Document Number	Rev
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Design Current = 6A
 Max Current = 7A
 OCP min = 10A

Cyntec 7*7*3
 DCR=30mohm, Irating=6A
 Isat=13.5A

ACOUSTIC NIOSE
 Id=7A
 Qg=8.7-13nC
 Rdson=23-30mohm

Id=7A
 Qg=8.7-13nC
 Rdson=23-30mohm

Cyntec 7*7*3
 DCR=30mohm, Irating=6A
 Isat=13.5A

2008/12/29

2008/12/29

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

090205 -1

090119 -1

090205 -1

090205 -1

090205 -1

090205 -1

090205 -1

090205 -1

090205 -1

090205 -1

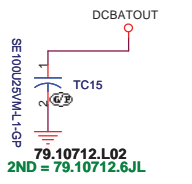
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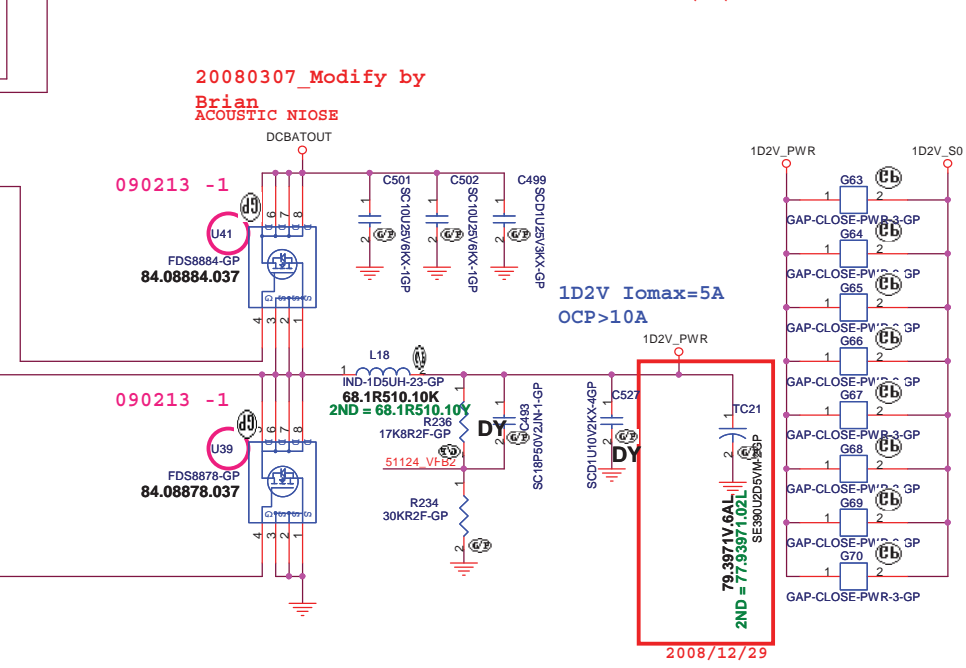
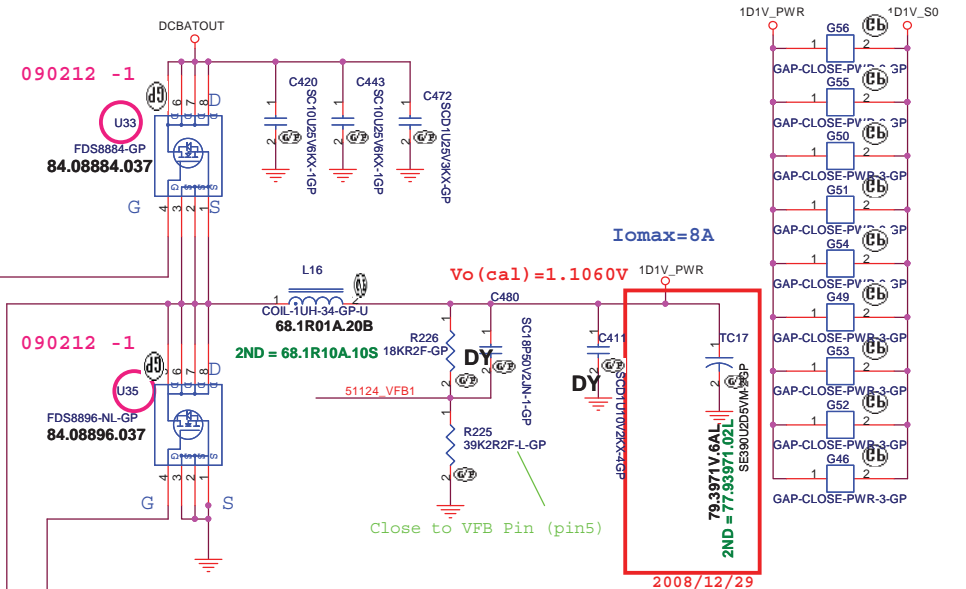
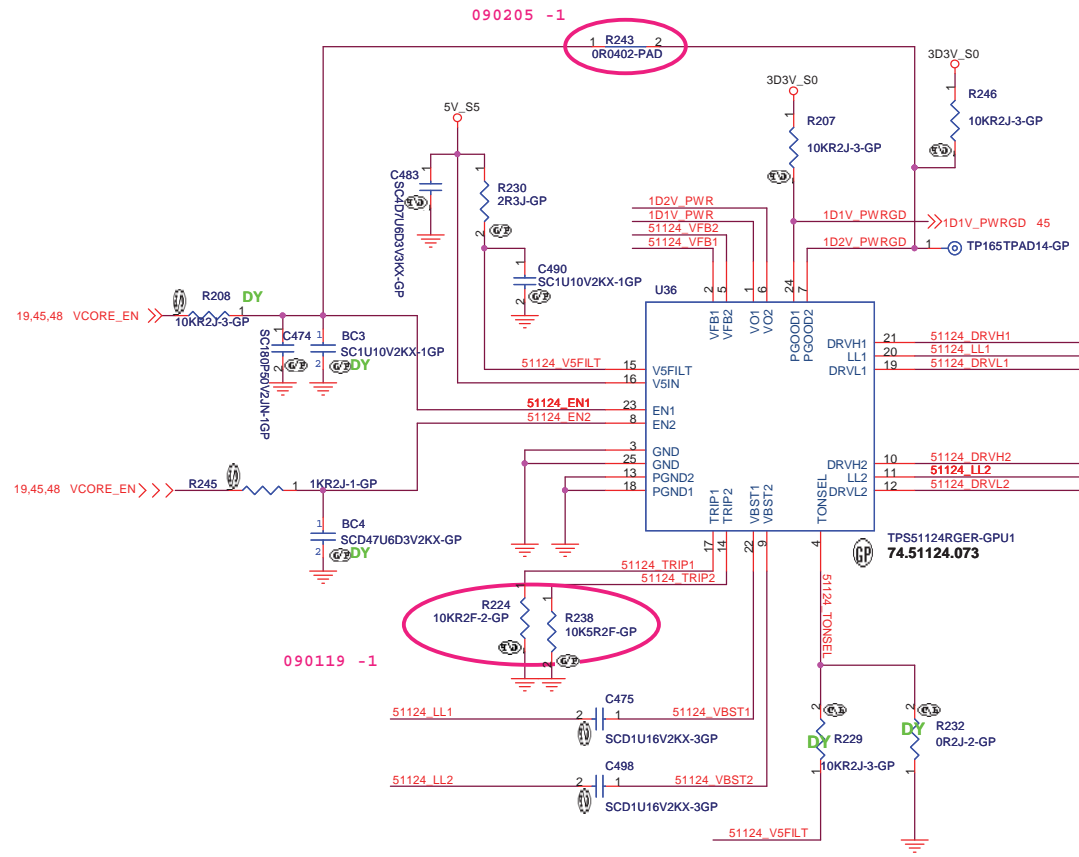
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 Taipei Hsien 221, Taiwan, R.O.C.

Title	DCDC 5V/3D3V (TPS51125)	
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$V_{trip} (mV) = R_{trip} (Kohm) * 10 (uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*E)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2) / R2$ --> Skip Mode



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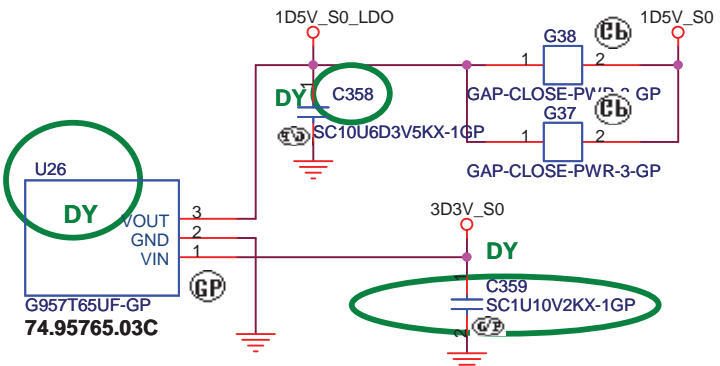
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Size: A3 Document Number: **JM70-PU** Rev: **-2**

Date: Friday, March 06, 2009 Sheet 50 of 56

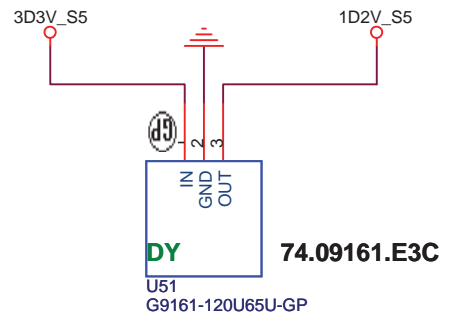
G957

1D5V_S0 Iomax=1A

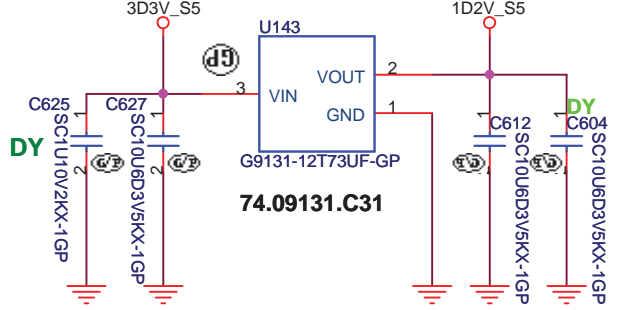


081230 SC

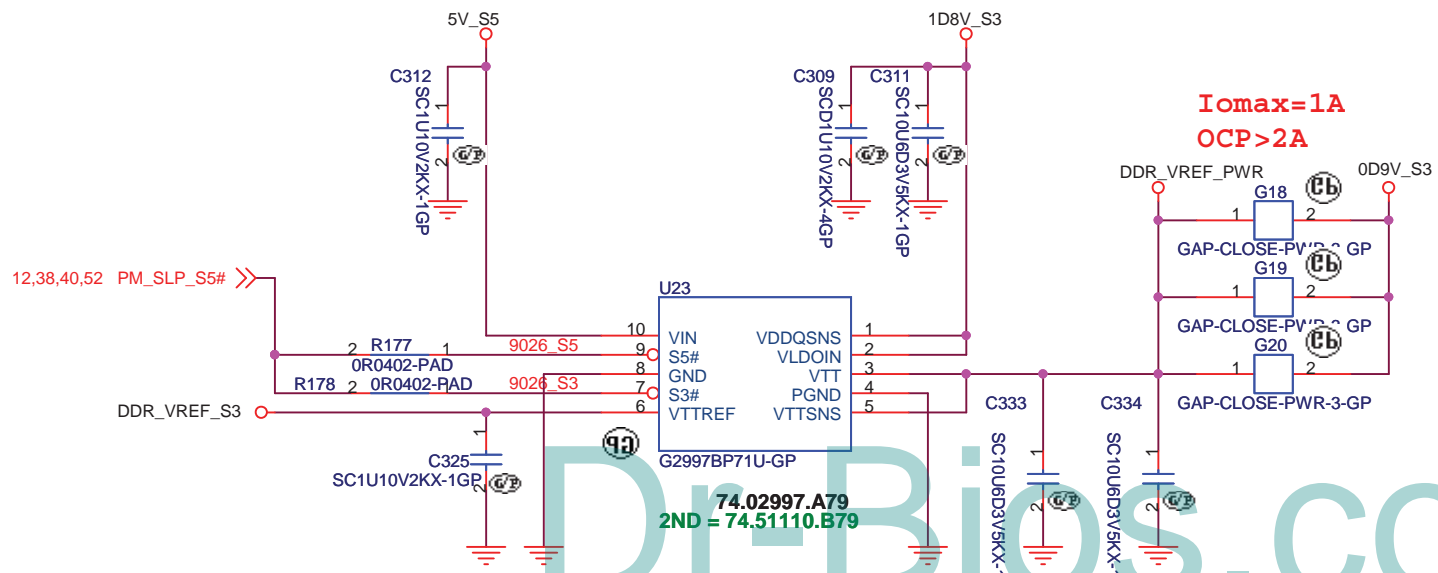
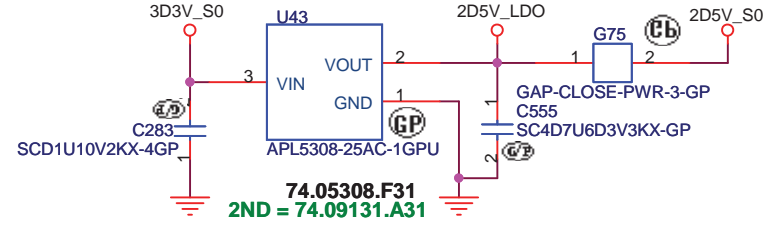
1D2V_S5 Iomax=400mA



Place near to SB700



2D5V_S0 Iomax=0.3A 2D5V/300mA

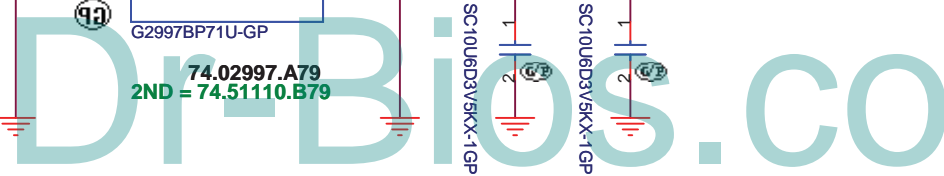


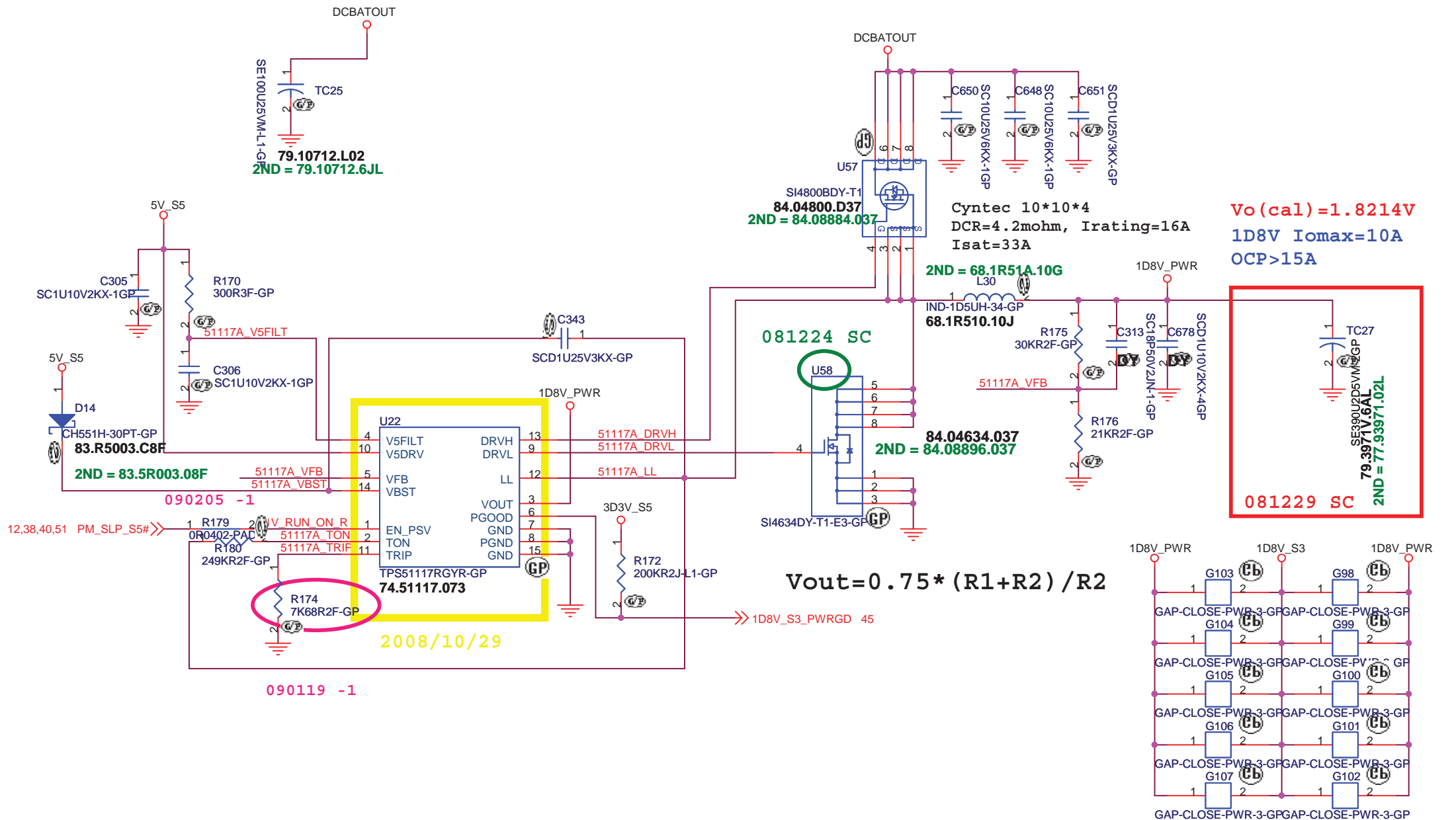
Iomax=1A
OCP>2A

<Core Design>

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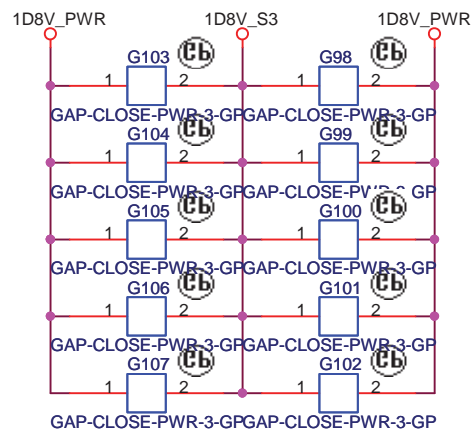
Title			
0D9V&2D5V&1D25V&1D5V			
Size	Document Number		Rev
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Vo(cal) = 1.8214V
1D8V Iomax=10A
OCP>15A

$$V_{out} = 0.75 * (R1 + R2) / R2$$

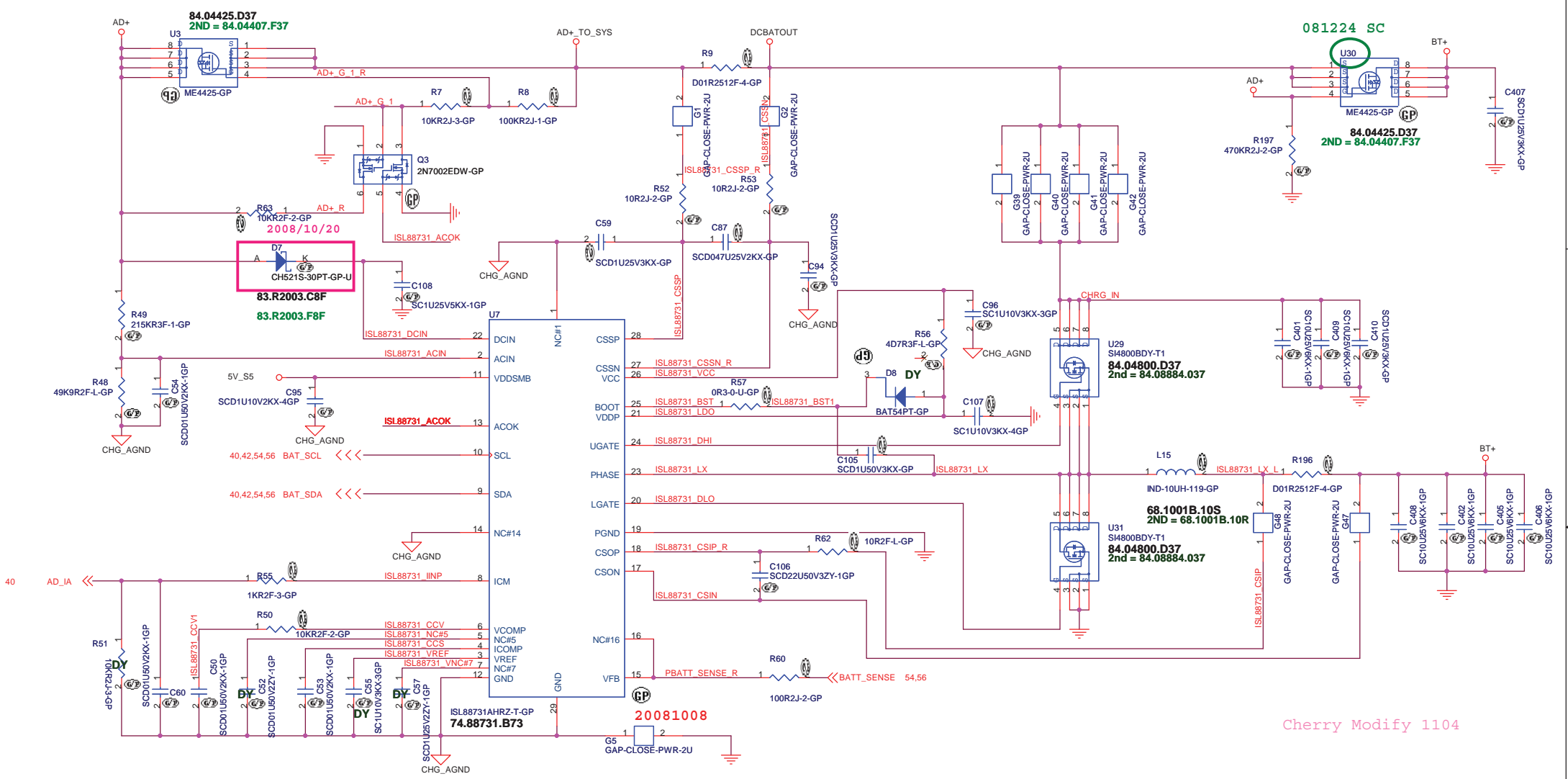


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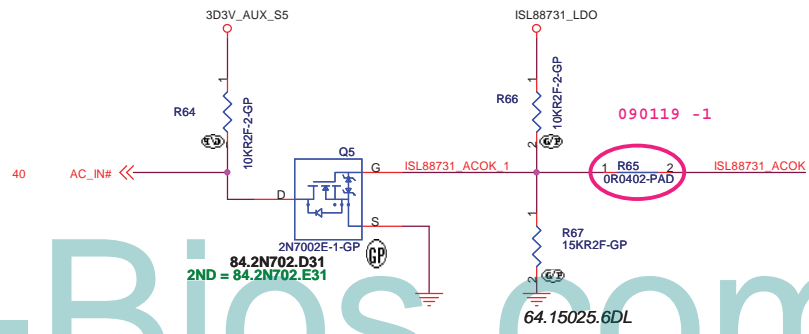
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Title		1D8V(TPS5117)	
Size	Document Number	Rev	
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Cherry Modify 1104



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Title: **ISL88731A Charger**

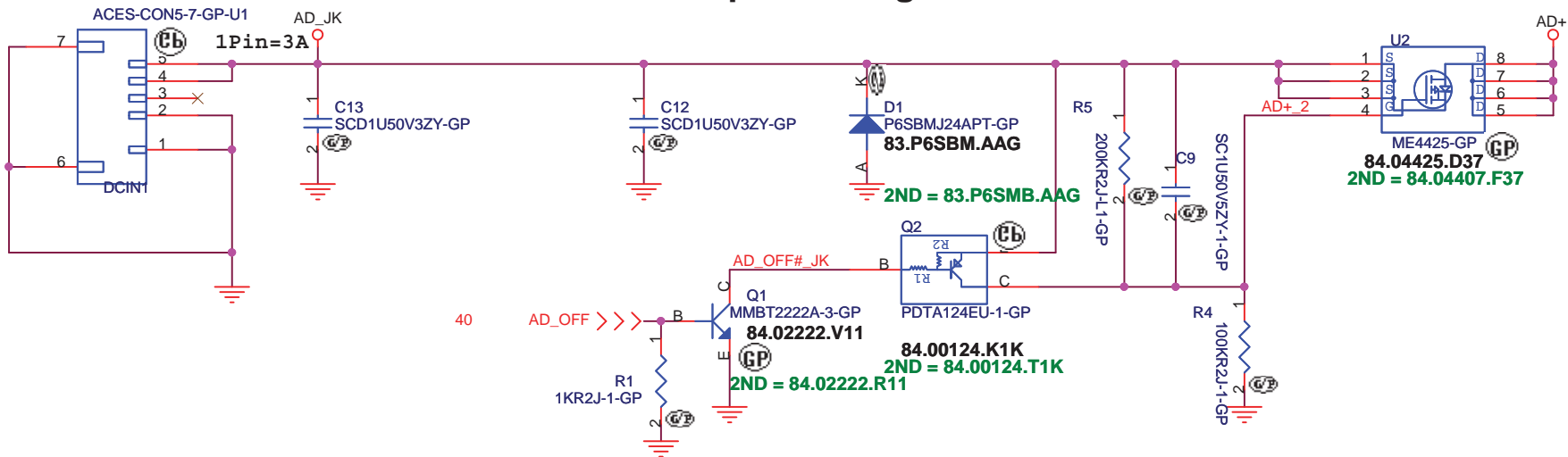
Size A3 Document Number: **JM70-PU** Rev: **-2**

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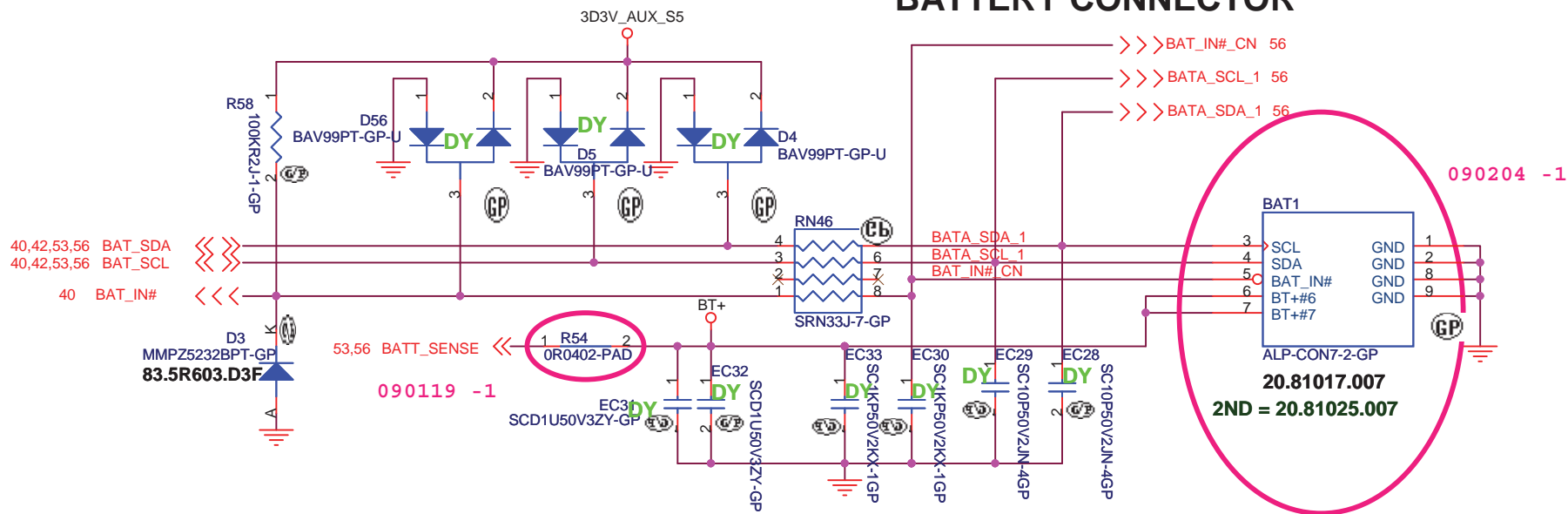
20.F1002.005

2ND = 20.F1170.005

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

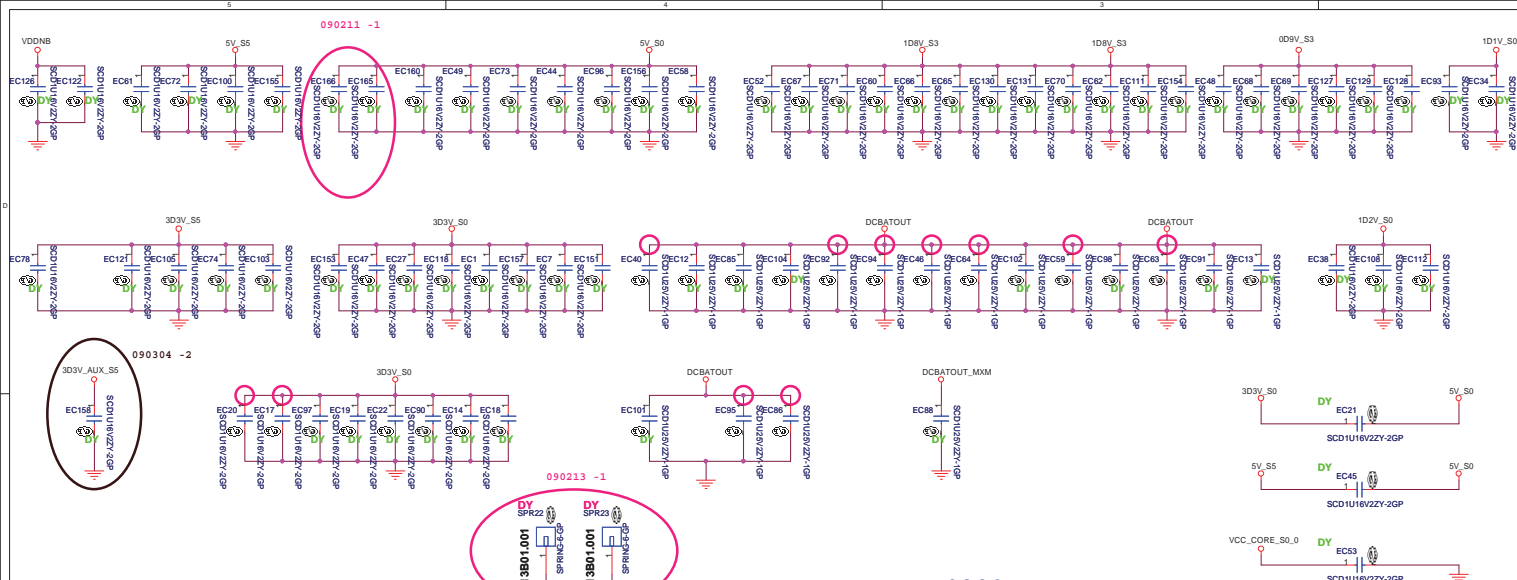
緯創資通

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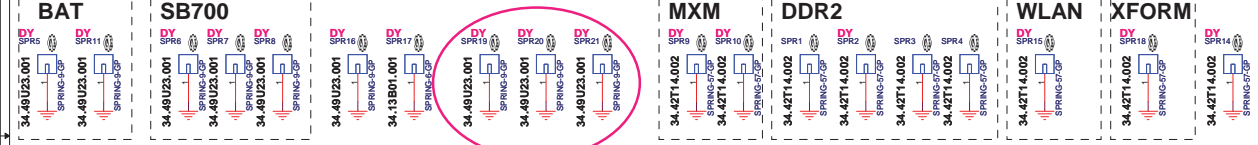
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Size	Document Number		Rev		
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SPRING ON TOP ~ 0209
 34.49U23.001 + 34.13B01.001

SPRING ON BOTTOM ~ 0209
 34.42T14.002



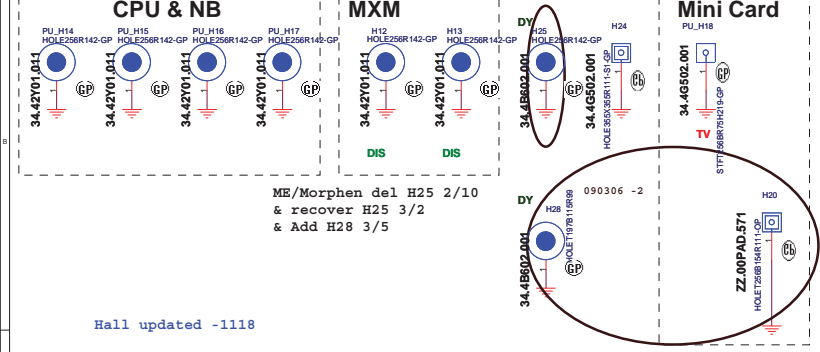
Check test point

- 3D3V_S0 ○ TP213 TPAD14-GP
- 3D3V_AUX_S5 ○ TP215 TPAD14-GP
- 3D3V_S5 ○ TP212 TPAD14-GP
- 5V_S5 ○ TP211 TPAD14-GP
- 12.40_PML_PWRBTN <<< TP176 TPAD14-GP
- 6.11_CPU_PWRGD <<< TP189 TPAD14-GP
- 39.40_49_SS_ENABLE <<< TP207 TPAD14-GP
- 6.11_CPU_LDT_RST# <<< TP195 TPAD14-GP

Test Point放在Dimm Door打開可量測處

STAND OFF ON BOTTOM ~ 0210

STAND OFF ON TOP ~ 0209

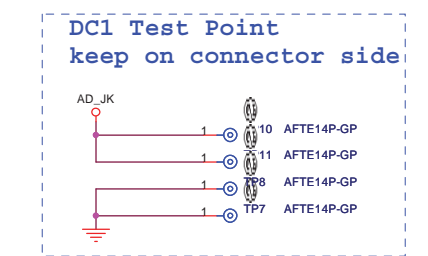
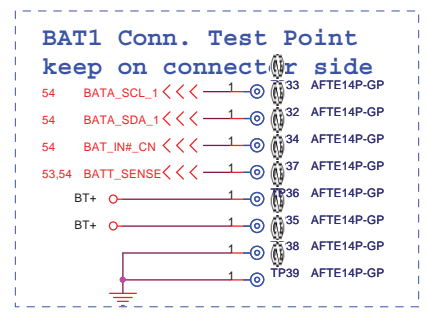
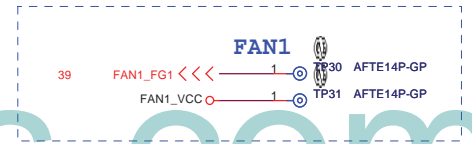
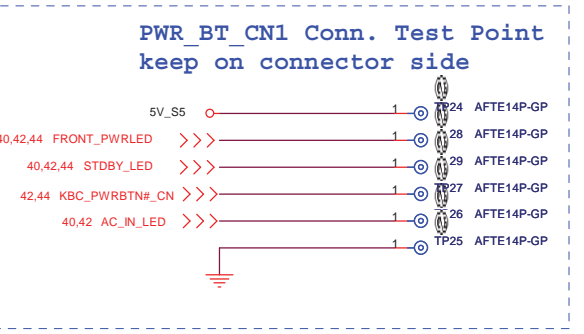
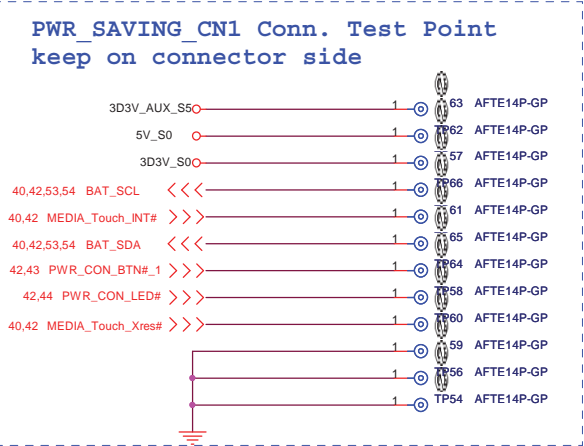
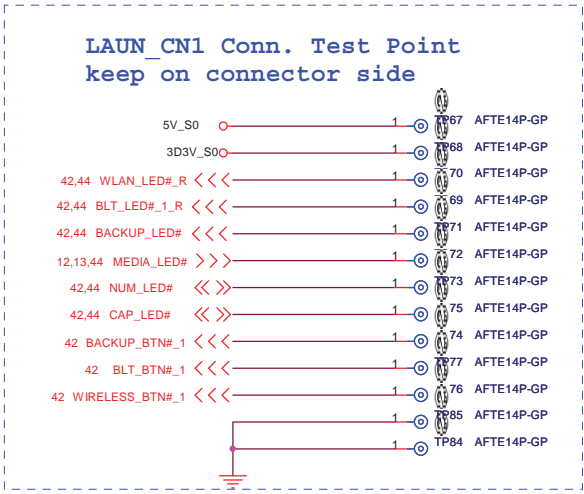
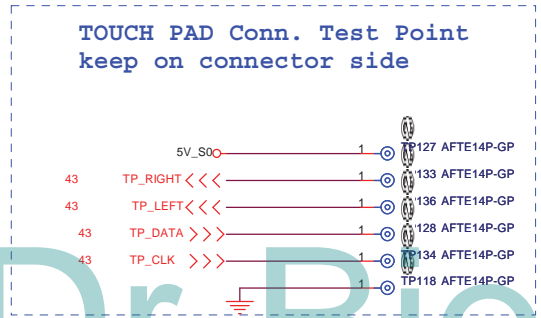
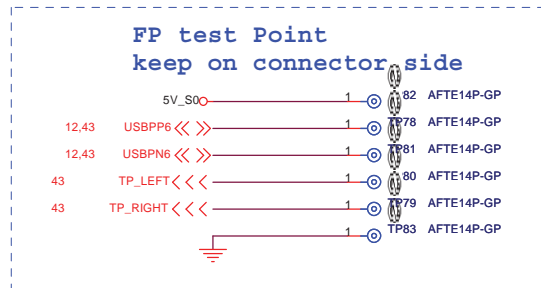
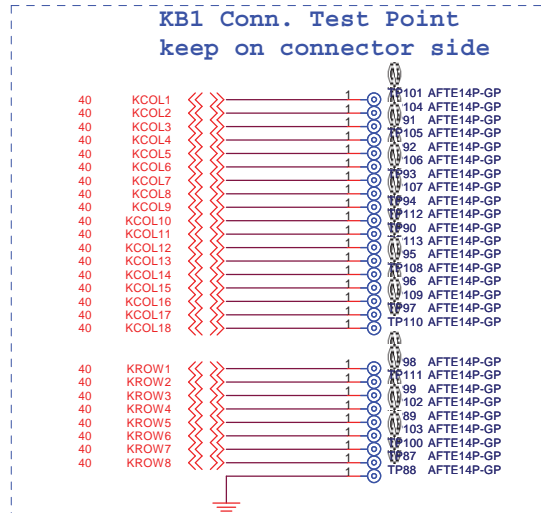


ME/Morphen del H25 2/10
 R recover H25 3/2
 R Add H28 3/5

ME/Morphen del H26, H27 1/8

Hall updated -1118

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