ZZZ1	PJP1	ZZZ2	ZZZ3	ZZZ4	ZZZ5	ZZZ6	ZZZ7
PCB DAZ@	45@DCIN	LA-5981P DA2@	LS-5981P DA2@	LS-5982P DA2@	LS-5983P DA2@	LS-5984P DA2@	LS-5986P DA2@

Compal Confidential

NCQF0 M/B Schematics Document

Intel Arrandale/Clarksfield Processor with DDRIII + Ibex Peak-M

2010-04-18

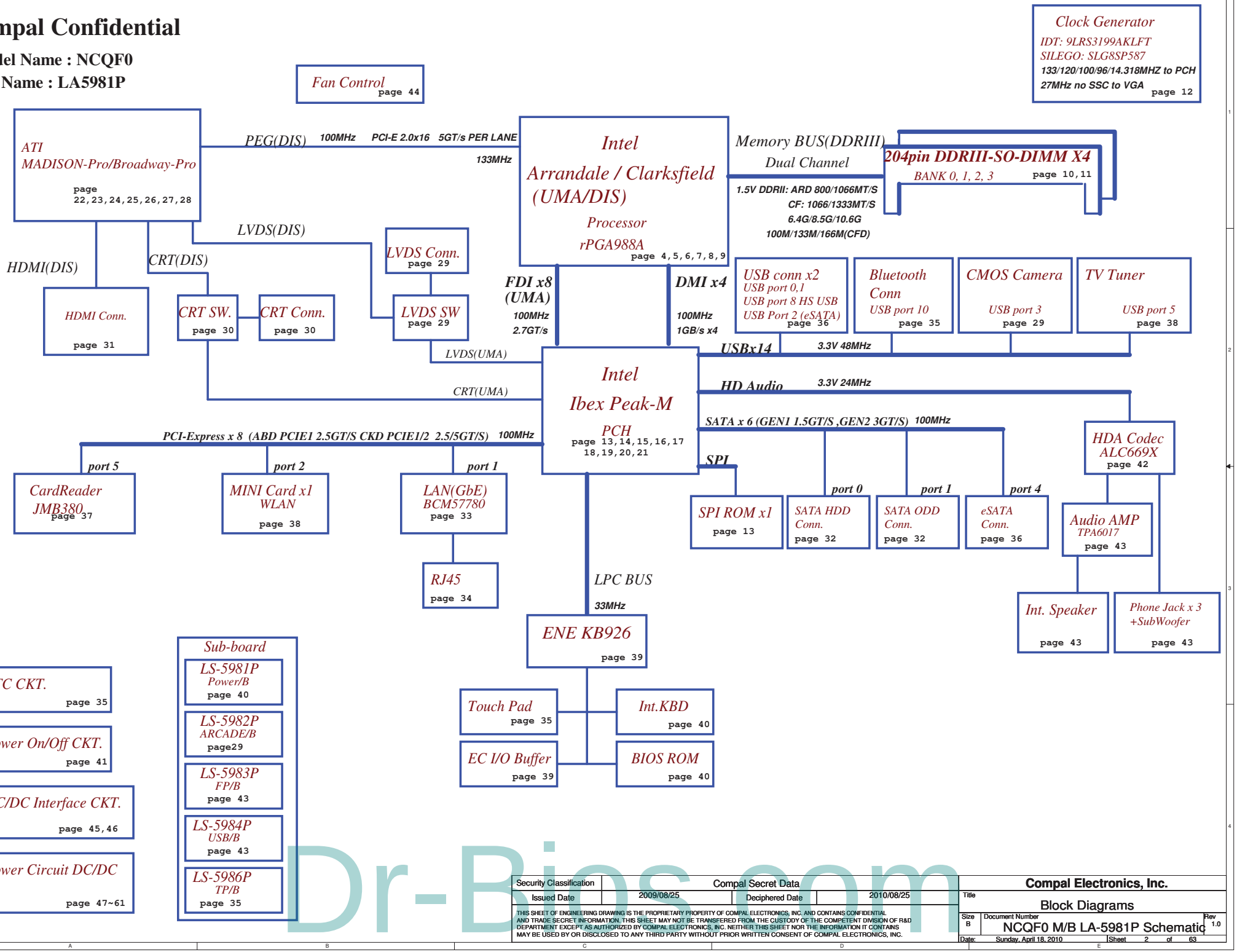
REV:1.A

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic	Rev: 1.0
Date: Sunday, April 18, 2010	Sheet 1 of 63	

Compal Confidential

Model Name : NCQF0
File Name : LA5981P



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.		
Title	Block Diagrams	
Size B	Document Number NCQF0 M/B LA-5981P Schematic	Rev 1.0
Date: Sunday, April 18, 2010	Sheet 2 of 63	

Voltage Rails

Power Plane	Description	S1	S3	S5	DGPU (UMA)	DGPU (DIS)
VIN	Adapter power supply (19V)	N/A	N/A	N/A		
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A		
+CPU_CORE	Core voltage for CPU	ON	ON	OFF		
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF		
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF		
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF		
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF		
+1.5VS	1.5V switched power rail	ON	OFF	OFF		
+1.8VS	1.8V switched power rail	ON	OFF	OFF		
+3VALW	3.3V always on power rail	ON	ON	ON*		
+3V	3.3V power rail for PCH	ON	ON	ON		
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*		
+3VS	3.3V switched power rail	ON	OFF	OFF		
+5VALW	5V always on power rail	ON	ON	ON*		
+5VS	5V switched power rail	ON	OFF	OFF		
+5V	5V power rail for PCH	ON	ON	ON		
+VSB	VSB always on power rail	ON	ON	ON*		
+RTCVCC	RTC power	ON	ON	ON		
+5VSDGPU	5V power rail for GPU				OFF	ON
+1.5VSDGPU	1.5V power rail for VRAM				OFF	ON
+1.8VSDGPU	1.8V switched power rail for GPU				OFF	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
DIS Only	DIS@
DGPU	VGA@
Broadway	WAY@
Madison	MAD@
Park	PAR@
Switchable Graphics	SG@

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

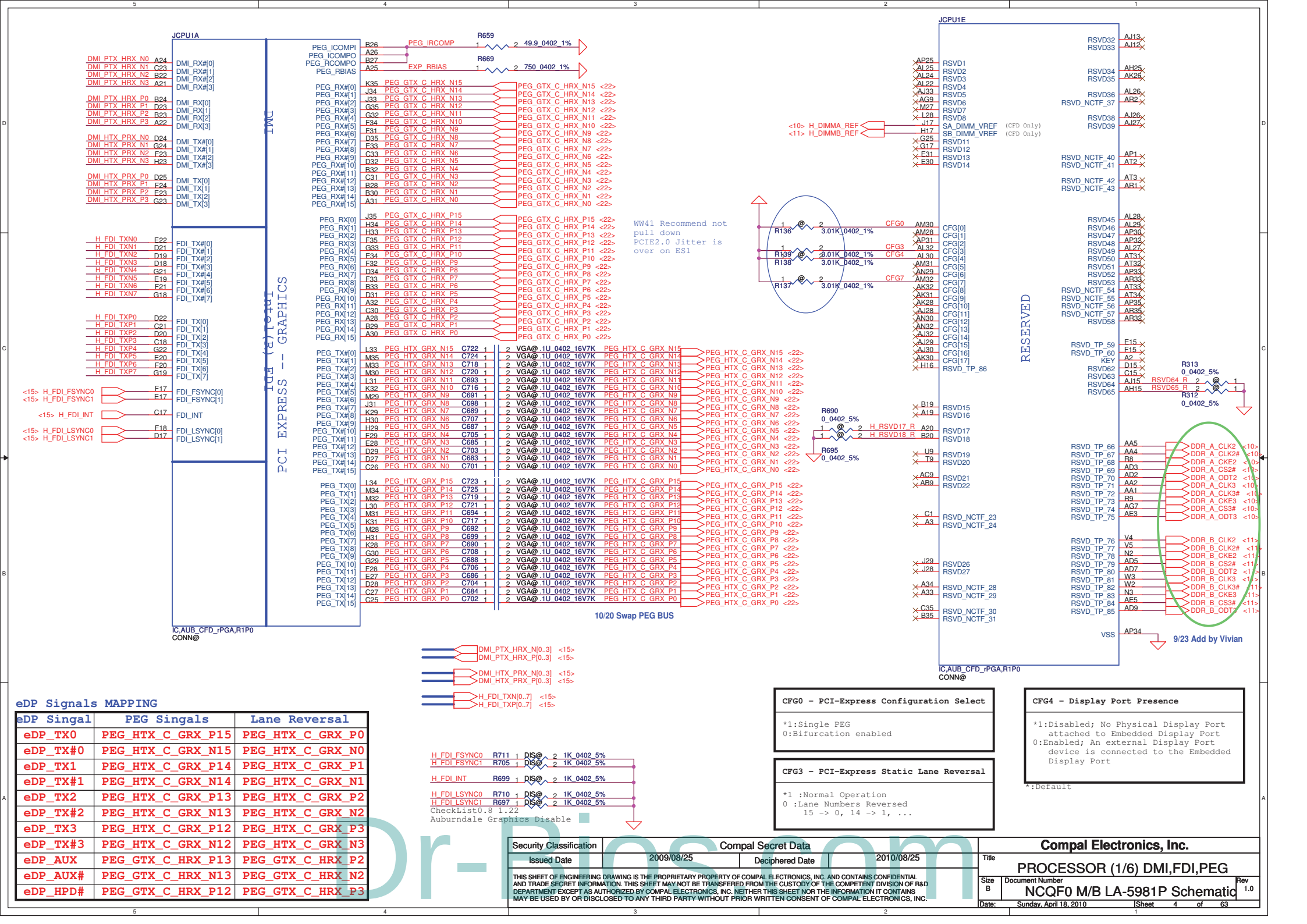
Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727	0101 1100b
ISL90728	0111 1100b

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB/B
	UHCI1	2	eSATA USB
		3	CMOS Camera
	UHCI2	4	Mini Card 1
		5	Mini Card 2
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Conn.
		9	
	UHCI5	10	Blue Tooth
		11	Finger Print
	UHCI6	12	
		13	

BOM Config
Switchable Graphics (PARK) SKU: SG@/VGA@/PAR@
Switchable Graphics (MADISON) SKU: SG@/VGA@/MAD@
DIS ONLY (BROADWAY): DIS@/VGA@/WAY@

Compal Electronics, Inc.
Title: Notes List
Size: B
Document Number: NCQF0 M/B LA-5981P Schematic
Rev: 1.0
Date: Sunday, April 18, 2010
Sheet 3 of 63



eDP Signals MAPPING

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

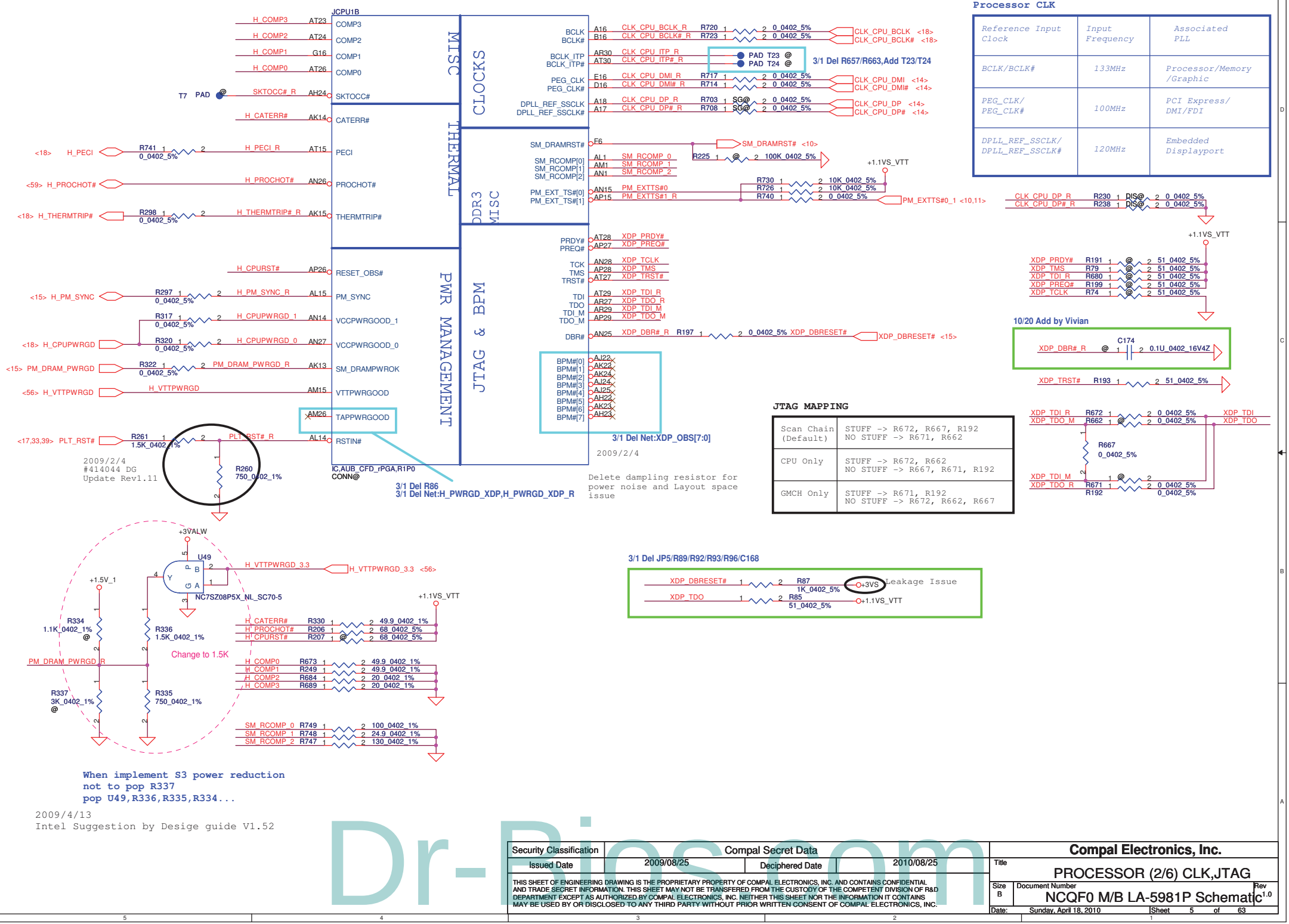
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PROCESSOR (1/6) DMI,FDI,PEG

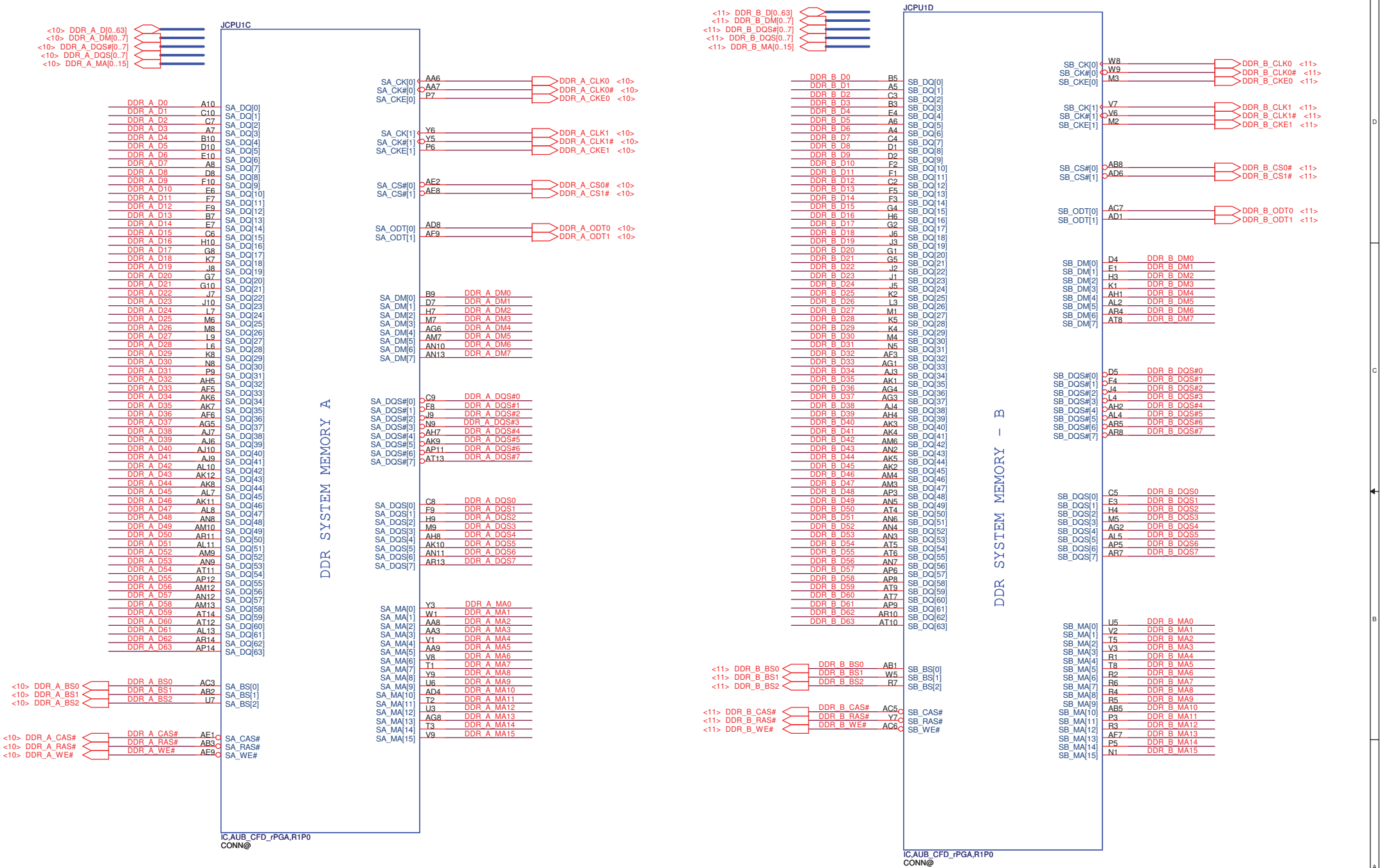
Size	Document Number	Rev
B	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 | Sheet 4 of 63



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	PROCESSOR (2/6) CLK,JTAG		
Size B	Document Number NCQF0 M/B LA-5981P Schematic	Rev 1.0	
Date: Sunday, April 18, 2010	Sheet 5 of 63		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date	2010/08/25
Title	PROCESSOR (3/6) DDRIII		
Size B	Document Number NCQF0 M/B LA-5981P Schematic		Rev 1.0
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JCPU1F

WW15 MOW
Peak 21A
Continuous 18A

48A

+CPU_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

1.1V RAIL POWER

CPU CORE SUPPLY

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

+1.1VS_VTT

10U_0805_6.3V6M

C412 C386 C381 C411 C408 C392 C368

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

22U_0805_6.3V6M

C413 C414

330U_D2E_2VM_R6M

C800 C799 C802

11/13 Change symbol of C799/C800/C802 from SGA00002380 to SGA00002U00(Due to EOL)

+CPU_CORE

C330 C344 C365 C384 C398 C349 C333 C364 C399

(Place these capacitors between inductor and socket on Bottom)

C401 C397 C335 C402 C385 C334 C400

(Place these capacitors under CPU socket, top layer)

C774 C772 C773 C771 C770 C769

(Place these capacitors on CPU cavity, Bottom Layer)

C787 C792 C791 C790 C789 C788

(Place these capacitors on CPU cavity, Bottom Layer)

CSC (Current Sense Configuration) 8/25

CPU_VID0	R605 / R616	1K_0402_1%
CPU_VID1	R606 / R617	1K_0402_1%
CPU_VID2	R607 / R618	1K_0402_1%
CPU_VID3	R608 / R619	1K_0402_1%
CPU_VID4	R259 / R263	1K_0402_1%
CPU_VID5	R609 / R620	1K_0402_1%
CPU_VID6	R610 / R621	1K_0402_1%
H_DPRSLPVR	R611 / R622	1K_0402_1%
H_PSI#	R612 / R623	1K_0402_1%

POWER

CPU VIDS

PSI# AN33 H_PSI# <59>

VID[0] AK35 CPU_VID0 <59>
VID[1] AK33 CPU_VID1 <59>
VID[2] AK34 CPU_VID2 <59>
VID[3] AL35 CPU_VID3 <59>
VID[4] AL33 CPU_VID4 <59>
VID[5] AM33 CPU_VID5 <59>
VID[6] AM35 CPU_VID6 <59>
PROC_DPRSLPVR AM34 H_DPRSLPVR <59>

VTT_SELECT G15 H_VTTVID1 H_VTTVID1 <56>

H_VTTVID1 = low, 1.1V
H_VTTVID1 = high, 1.05V

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

SENSE LINES

ISENSE AN35 IMVP_IMON <59>

VCC_SENSE AJ34 VCCSENSE_CPU R615 0_0402_5%
VSS_SENSE AJ35 VSSSENSE_CPU R614 0_0402_5%

R604 100_0402_1% +CPU_CORE
VCCSENSE <59>
VSSSENSE <59>
R603 100_0402_1%

VTT_SENSE B15 VTT_SENSE <56>
VSS_SENSE_VTT A15 VSS_SENSE_VTT
R727 0_0402_5%

Note:CRB has the VTT_SENSE connected through a "no-stuff" 0- series resistor and VSS_SENSE_VTT floating.

+CPU_CORE

4 x 330uF(6m ohm@100kHz)

C232 C186 C711 C221 C259 C196

330U_D2E_2VM_R6M

TOP side (under inductor)

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X330uF	6m ohm/4	2X330uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

IC,AUB_CFD_rPGA,R1P0
CONN@

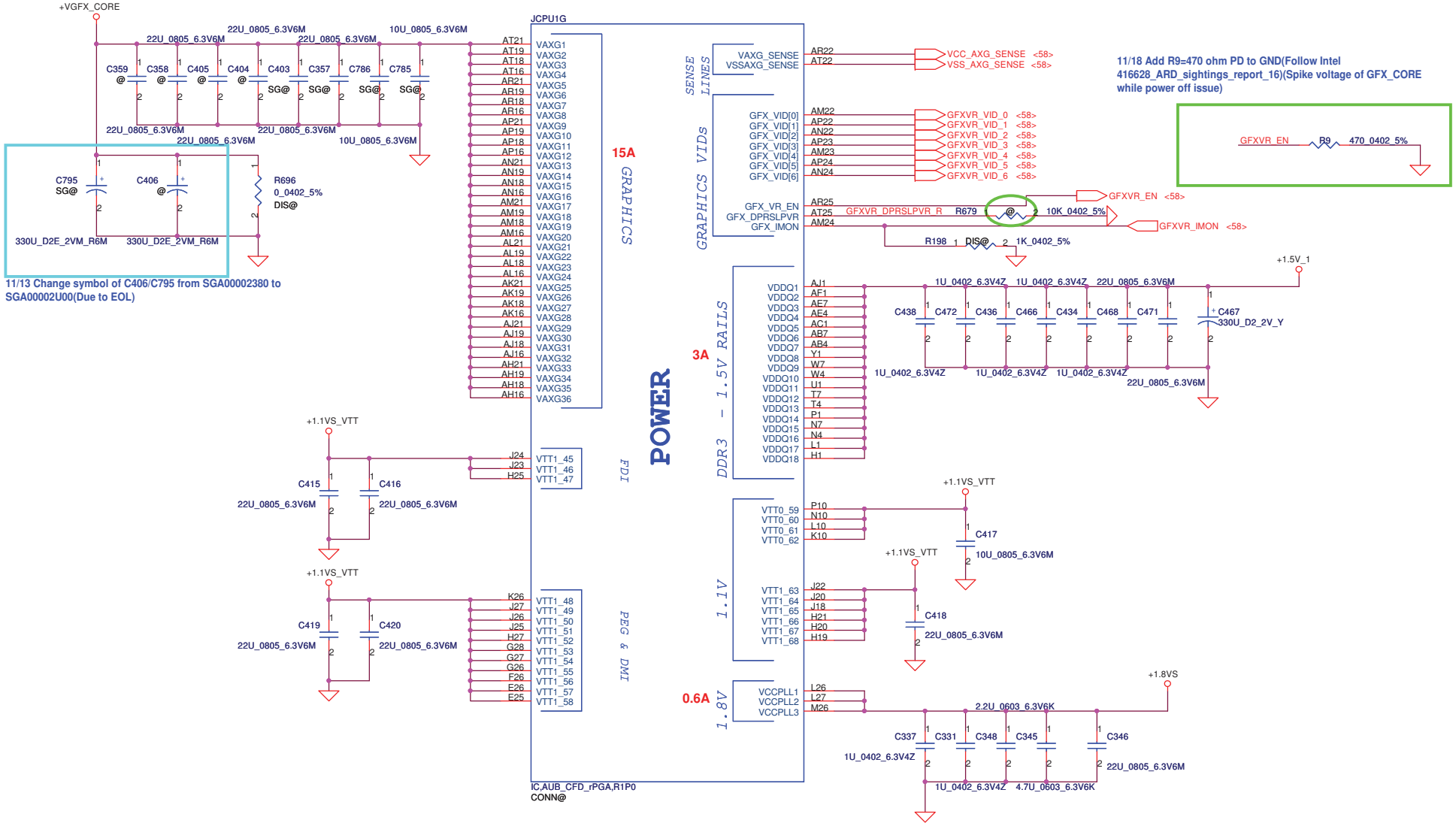
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

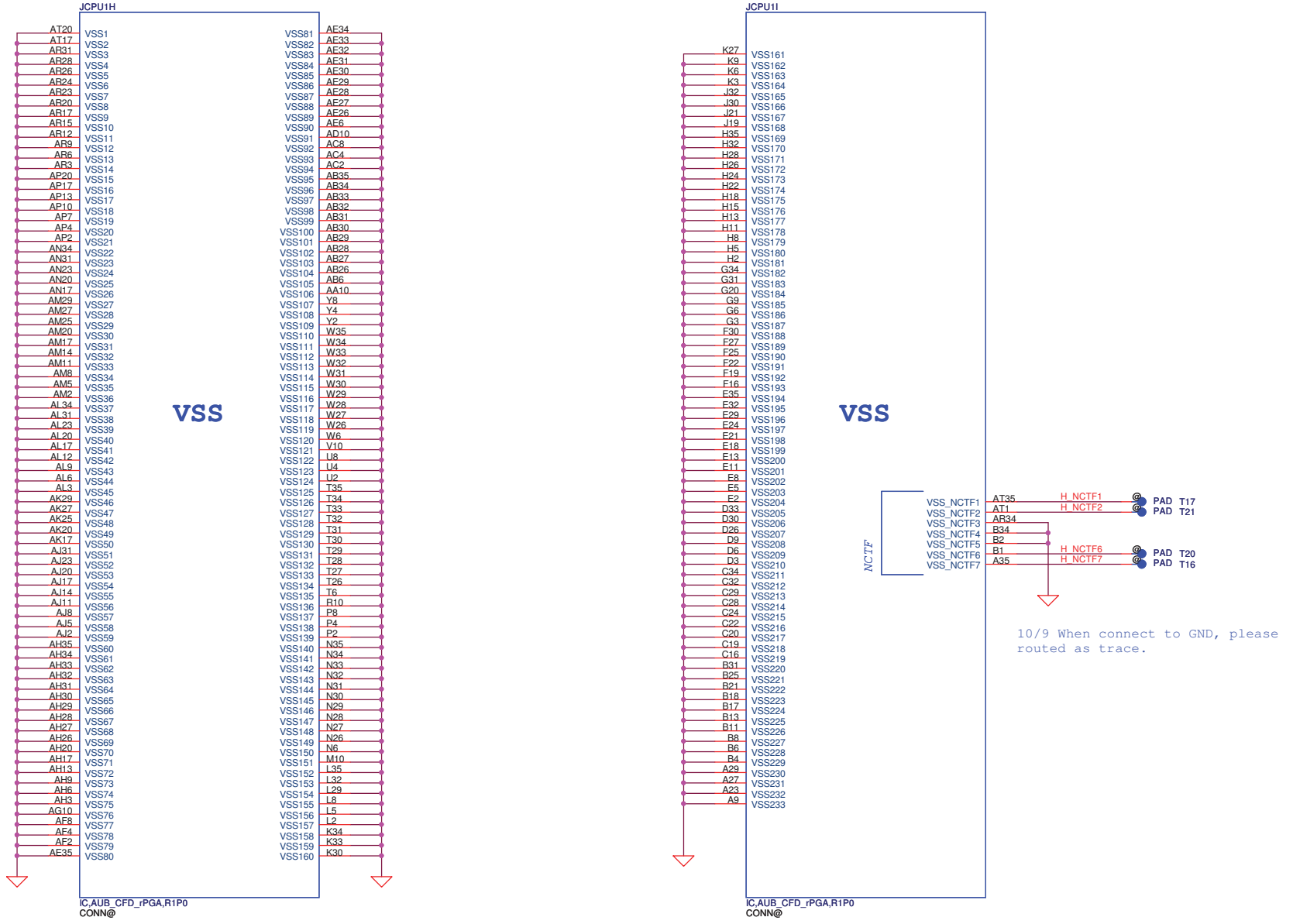
Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 7 of 63

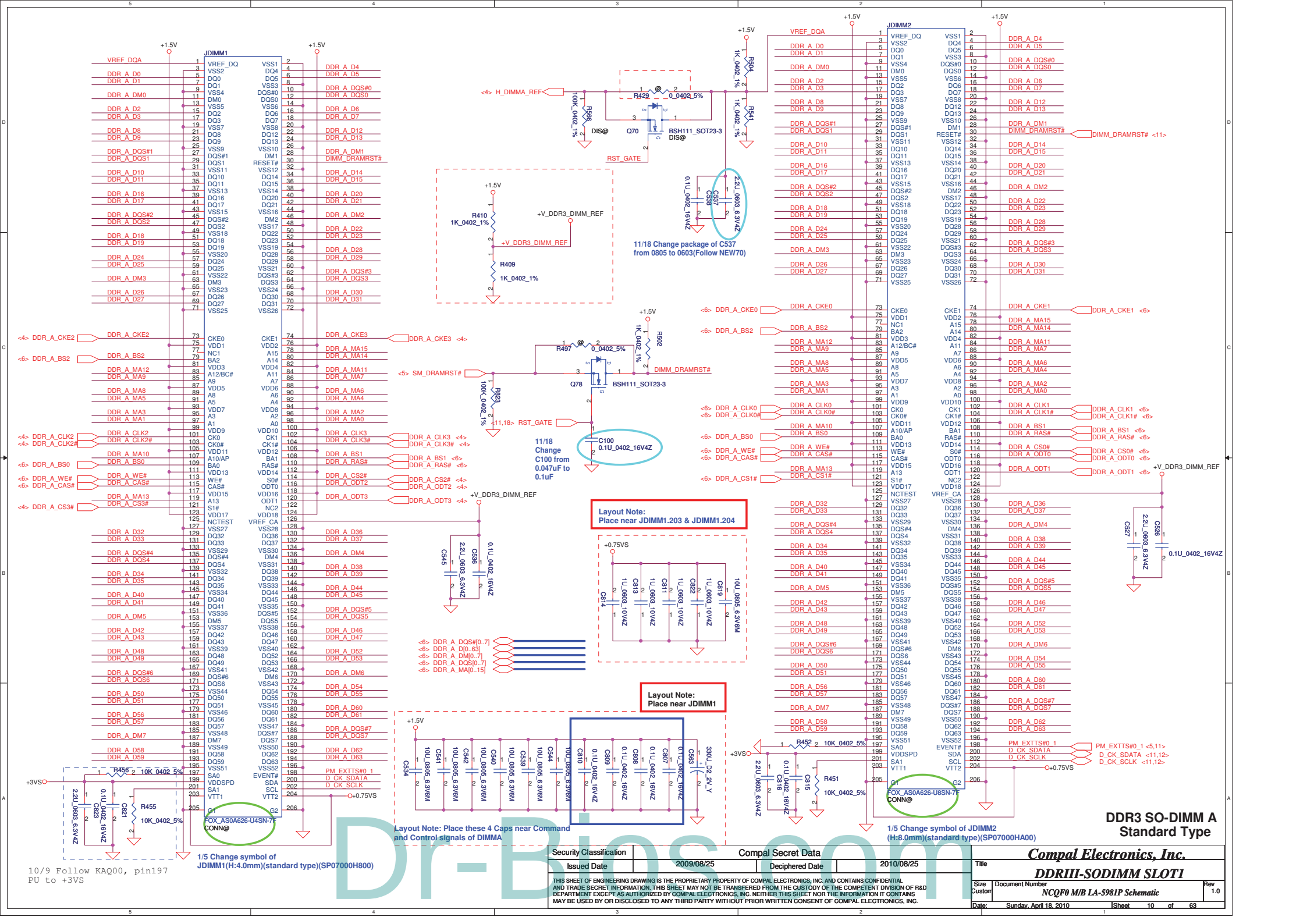


Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.	
Title	PROCESSOR (5/6) PWR
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic
Rev	1.0
Date: Sunday, April 18, 2010	Sheet 8 of 63



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date	2010/08/25
Title	PROCESSOR (6/6) VSS		
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 0
Date: Sunday, April 18, 2010	Sheet 9 of 63		



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: DDRIII-SODIMM SLOT1			
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 1.0
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2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

JDIMM4

JDIMM3

Layout Note:
Place near JDIMM2.203 & JDIMM2.204

Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

11/18 Change package of C553 from 0805 to 0603(Follow NEW70)

11/09 Change symbol of JDIMM4 by Vivian(H:8.0mm)(Reverse type)(SP07000M300)

11/09 Change symbol of JDIMM3 by Vivian(H:4.0mm)(Reverse type)(SP07000J500)

10/9 Follow KAQ00, pin197 PU to +3VS

DDR3 SO-DIMM B Reverse Type

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Title	Compal Electronics, Inc.		
	DDRIII-SODIMM SLOT2		
Size	Document Number		Rev
	NCQF0 M/B LA-5981P Schematic		1.0
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10/9 Change L34 part number
from SM010014520 to SM01000AX00

10/9 Change L39 part number
from SM010014520 to SM01000AX00

10/9 Change L37 part number
from SM010014520 to SM01000AX00

Clock Generator

Integrated 33ohm Resistor

10/19 Add

Integrated 33ohm Resistor

U35

9LVS3199AKLFT_32P

12/11 Change PN of U35 to SA00003HR00

LOW Power:
Realtek: RTM890N-631-VB-GRT, SA00003HQ10
*IDT: ICS9LVS3199AKLFT, SA00003HR00

Integrated 33ohm Resistor

10/27 Place C497/C485/C488 on pin1/pin17/pin24 side(U35)

Silego Have Internal Pull-Up

IDT Have Internal Pull-Down

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

9/10 Change symbol of
Q31/Q32 to SC70-3

9/10 Change symbol of
Q29 to SC70-3

9/23 Change C495 to 22pF

update PCB footprint

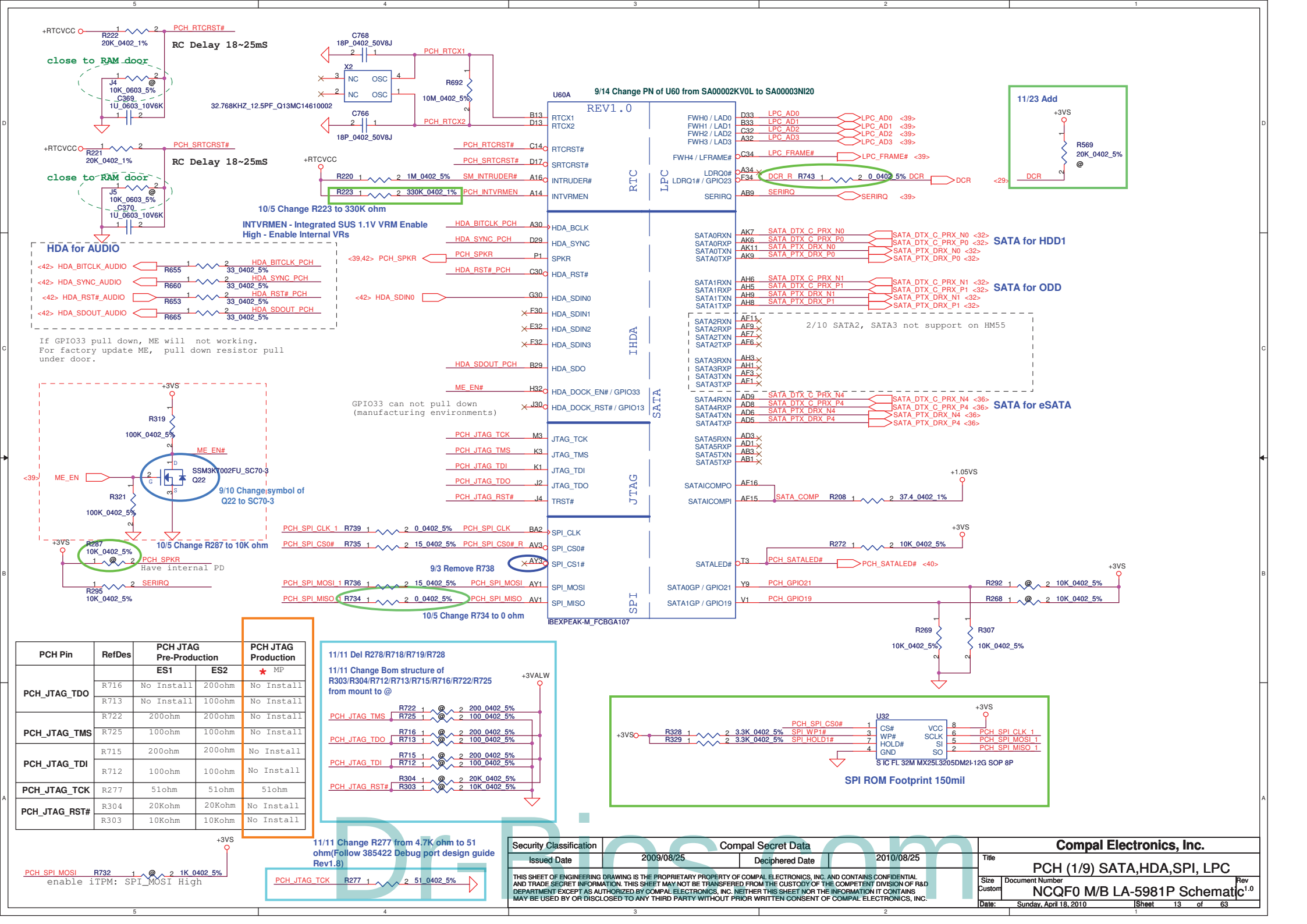
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

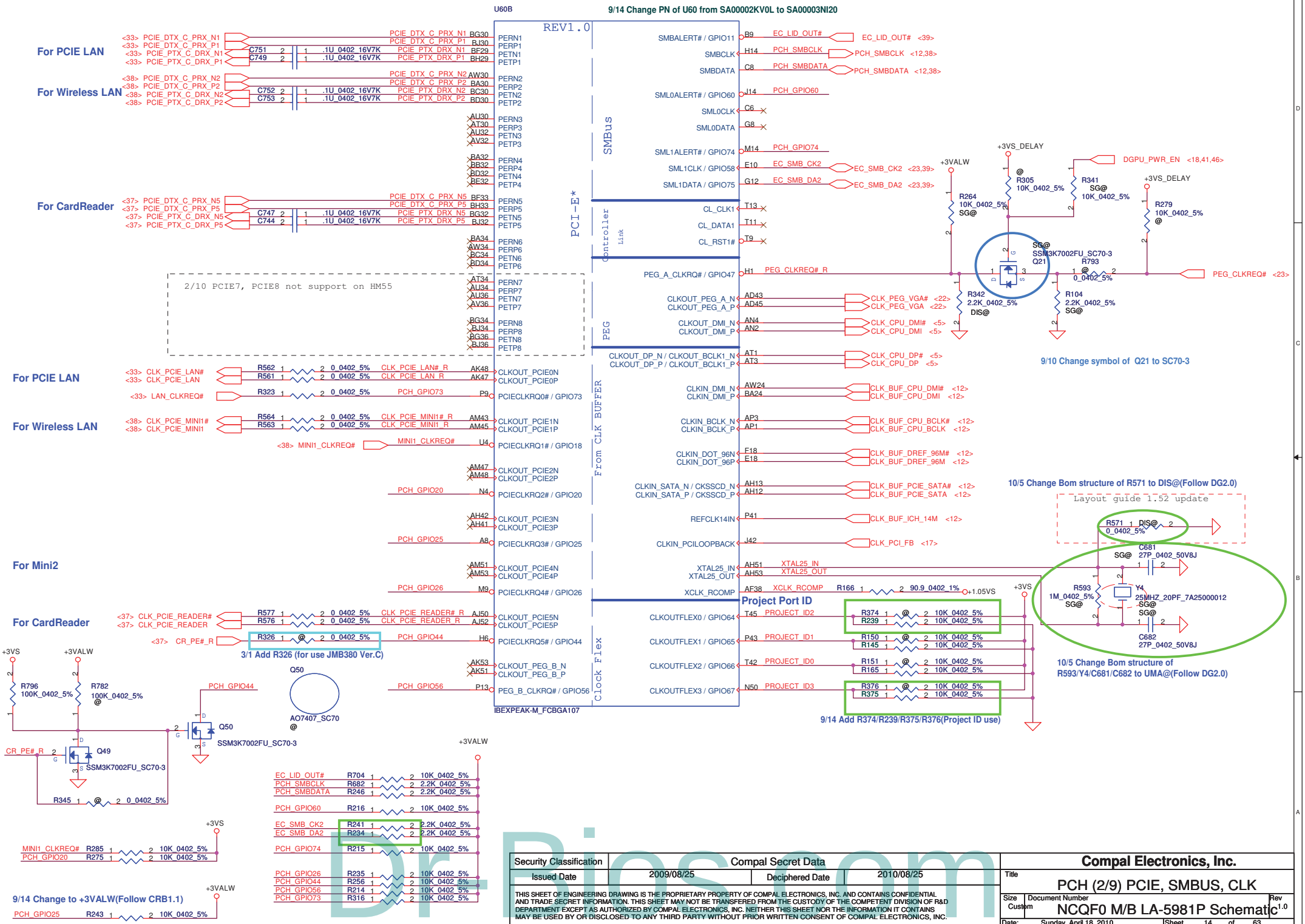
Date: Sunday, April 18, 2010 | Sheet 12 of 63



PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	* MP
PCH_JTAG_TDO	R716	No Install	200ohm	No Install
	R713	No Install	100ohm	No Install
PCH_JTAG_TMS	R722	200ohm	200ohm	No Install
	R725	100ohm	100ohm	No Install
PCH_JTAG_TDI	R715	200ohm	200ohm	No Install
	R712	100ohm	100ohm	No Install
PCH_JTAG_TCK	R277	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R304	20Kohm	20Kohm	No Install
	R303	10Kohm	10Kohm	No Install

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Title	PCH (1/9) SATA,HDA,SPI, LPC		
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 1.0
Date: Sunday, April 18, 2010	Sheet 13 of 63		



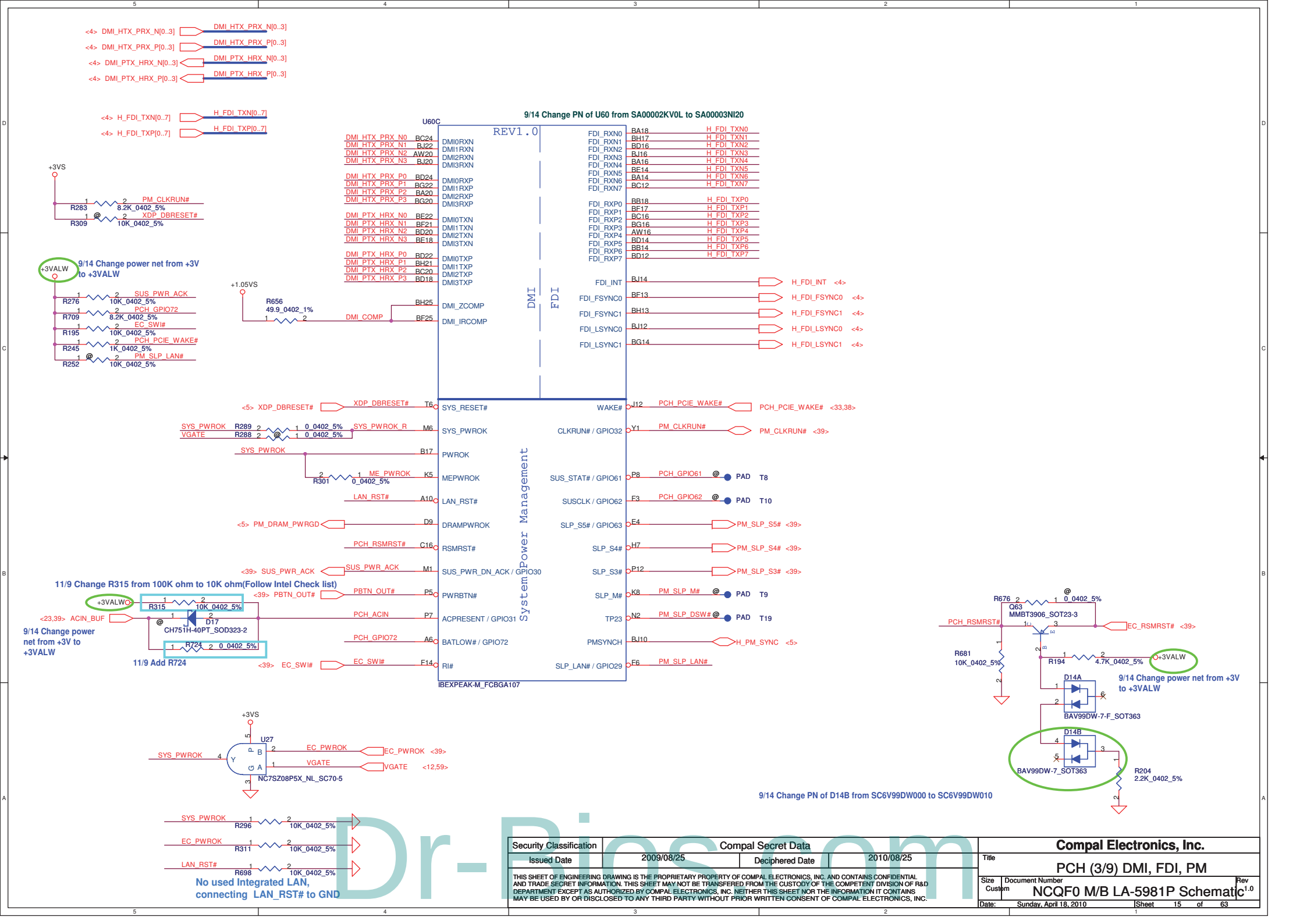
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

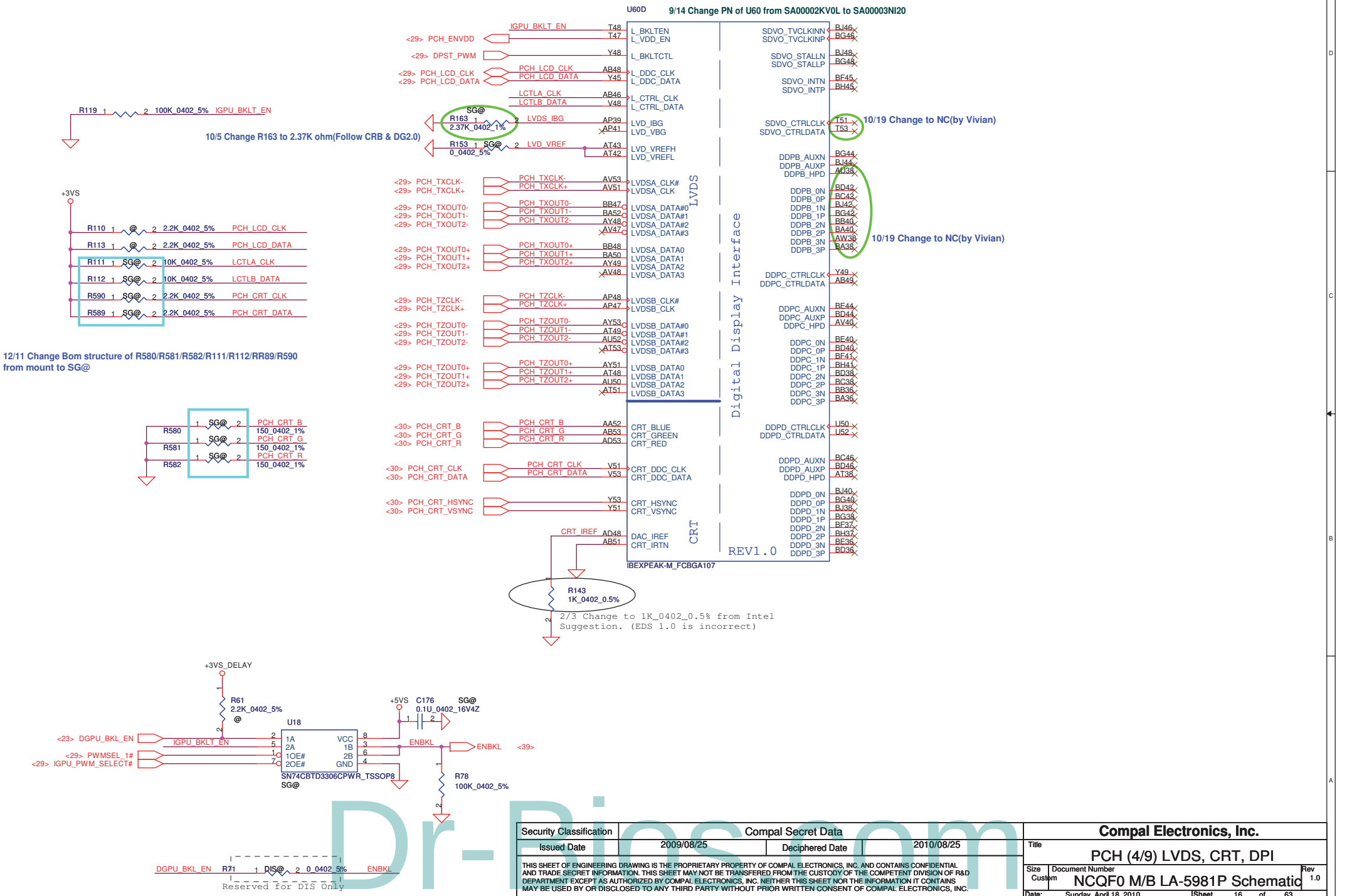
Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 14 of 63



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	PCH (3/9) DMI, FDI, PM		
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 1.0
Date: Sunday, April 18, 2010	Sheet 15 of 63		



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	PCH (4/9) LVDS, CRT, DPI		
Size	Document Number		Rev
Custom	NCQF0 M/B LA-5981P Schematic		1.0
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9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

11/13 Add RP1~RP5

RP1: DGPU_SELECT#, PCI_PIRQD#, PCI_STOP#, PCI_IRDY# — 8.2K_1206_8P4R_5%

RP2: PCI_PERR#, PCI_DEVSEL#, PCI_PLOCK#, PCI_SERR# — 8.2K_1206_8P4R_5%

RP3: PCI_REQ3#, PCI_PIRQF#, PCI_PIRQB#, PCI_REQ0# — 8.2K_1206_8P4R_5%

RP4: PCI_PIRQH#, PCI_TRDY#, PCI_FRAME#, PCI_REQ1# — 8.2K_1206_8P4R_5%

RP5: PCI_PIRQE#, PCI_PIRQA#, PCI_PIRQC#, PCI_PIRQG# — 8.2K_1206_8P4R_5%

U60E REV1.0

PCI: AD0–AD31, C/BE0#–C/BE3#, PIRQA#–PIRQD#, REQ0#, REQ1# / GPIO50, REQ2# / GPIO52, REQ3# / GPIO54, GNT0#, GNT1# / GPIO51, GNT2# / GPIO53, GNT3# / GPIO55, PIRQE# / GPIO2, PIRQF# / GPIO3, PIRQG# / GPIO4, PIRQH# / GPIO5, PCIRST#, SERR#, PERR#, IRDY#, PAR, DEVSEL#, FRAME#, PLOCK#, STOP#, TRDY#, PME#, PLTRST#, CLKOUT_PCI0–CLKOUT_PCI4

NVRAM: NV_CE#0–NV_CE#3, NV_DQS0, NV_DQS1, NV_DQ0 / NV_IO0 – NV_DQ15 / NV_IO15, NV_ALE, NV_CLE, NV_RCOMP, NV_RB#, NV_WR#0_RE#, NV_WR#1_RE#, NV_WE#_CK0, NV_WE#_CK1 — 9/4 NC

USB: USBP0N/P – USBP12N/P13P, USBRBIAS#, USBRBIAS, OC0# / GPIO59 – OC7# / GPIO14

IBEXPEAK-M_FCBGA107

USB Conn.(HS) JUSB1 — USB/B — eSATA USB Conn. — CMOS Camera (LVDS) — Mini Card(WLAN) — Mini Card(Mini2) — EHCI 1

USB Conn.(HS) JUSB2 — Bluetooth — Fingerprint — EHCI 2

<29,30> DGPU_SELECT#

<29> DGPU_PWMSEL#

<5,33,39> PLT_RST#

<39> CLK_PCI_LPC — R588 1 2 22_0402_5% — CLK_PCI_LPC_R

<14> CLK_PCI_FB — R141 1 2 22_0402_5% — CLK_PCI_FB_R

2008/1/6 2009MOW01 change to 22 ohm

R188 22.6_0402_1%

(For USB Port0)
(For USB Port1)
(For eSATA USB Port)

(For USB Port8)

OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

+VCCQ_NAND

NV_ALE R721 1 @ 2 1K_0402_5%
NV_CLE R240 1 @ 2 1K_0402_5%

U30 NC7SZ08P5X_NL_SC70-5: PLT_RST# → PLT_RST_BUF# <37,38>; R338 100K_0402_5%

U29 NC7SZ08P5X_NL_SC70-5 VGA@: <18> DGPU_HOLD_RST#; R765 0_0402_5% DIS@; PLT_RST_BUF# → PLTRST_VGA# <22>; R340 100_0402_5% VGA@; R339 100K_0402_5% VGA@

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
* 1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

PCI_GNT0# R123 1 @ 2 1K_0402_5% Have internal PU

PCI_GNT1# R149 1 @ 2 1K_0402_5% Have internal PU

PCI_GNT3# R585 1 @ 2 1K_0402_5% Have internal PU

11/18 Del RP13
11/18 Add R168/R172/R174/R176(For Layout request)

USB_OC#3_R R168 1 2 10K_0402_5%
USB_OC#5_R R172 1 2 10K_0402_5%
USB_OC#7_R R174 1 2 10K_0402_5%
USB_OC#6_R R176 1 2 10K_0402_5%
→ +3VALW

10/27 Change power net from +3V to +3VALW

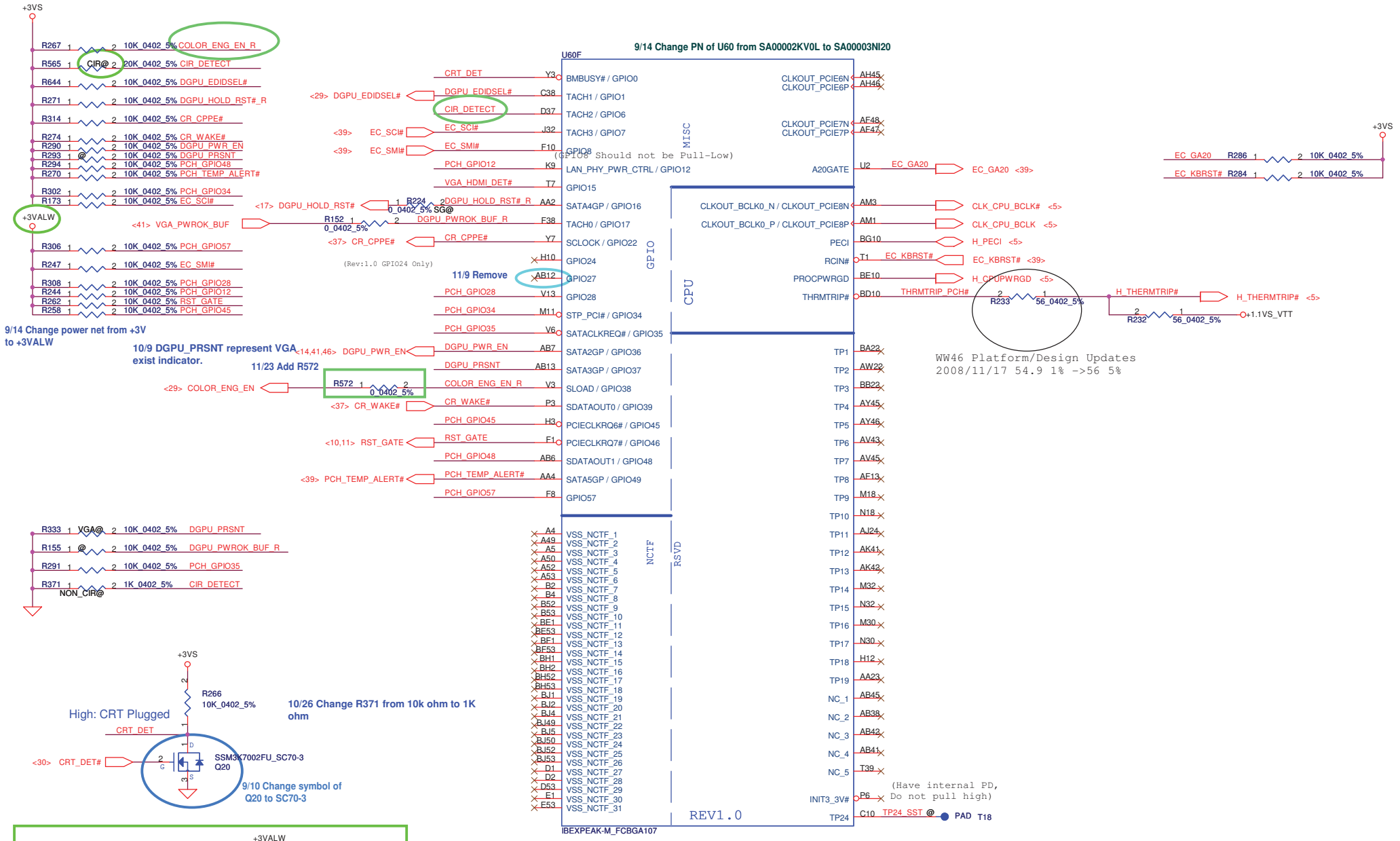
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 17 of 63



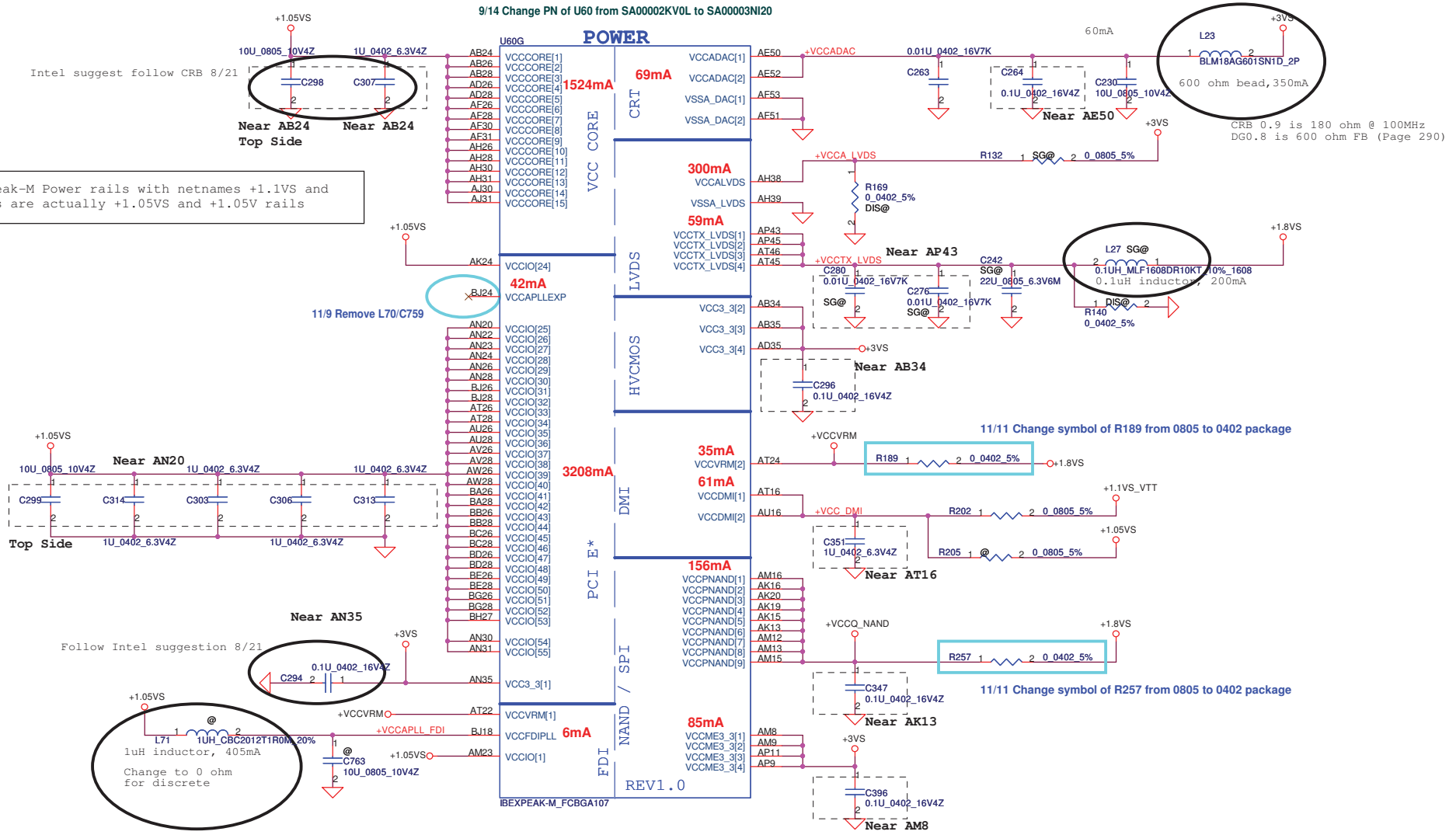
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

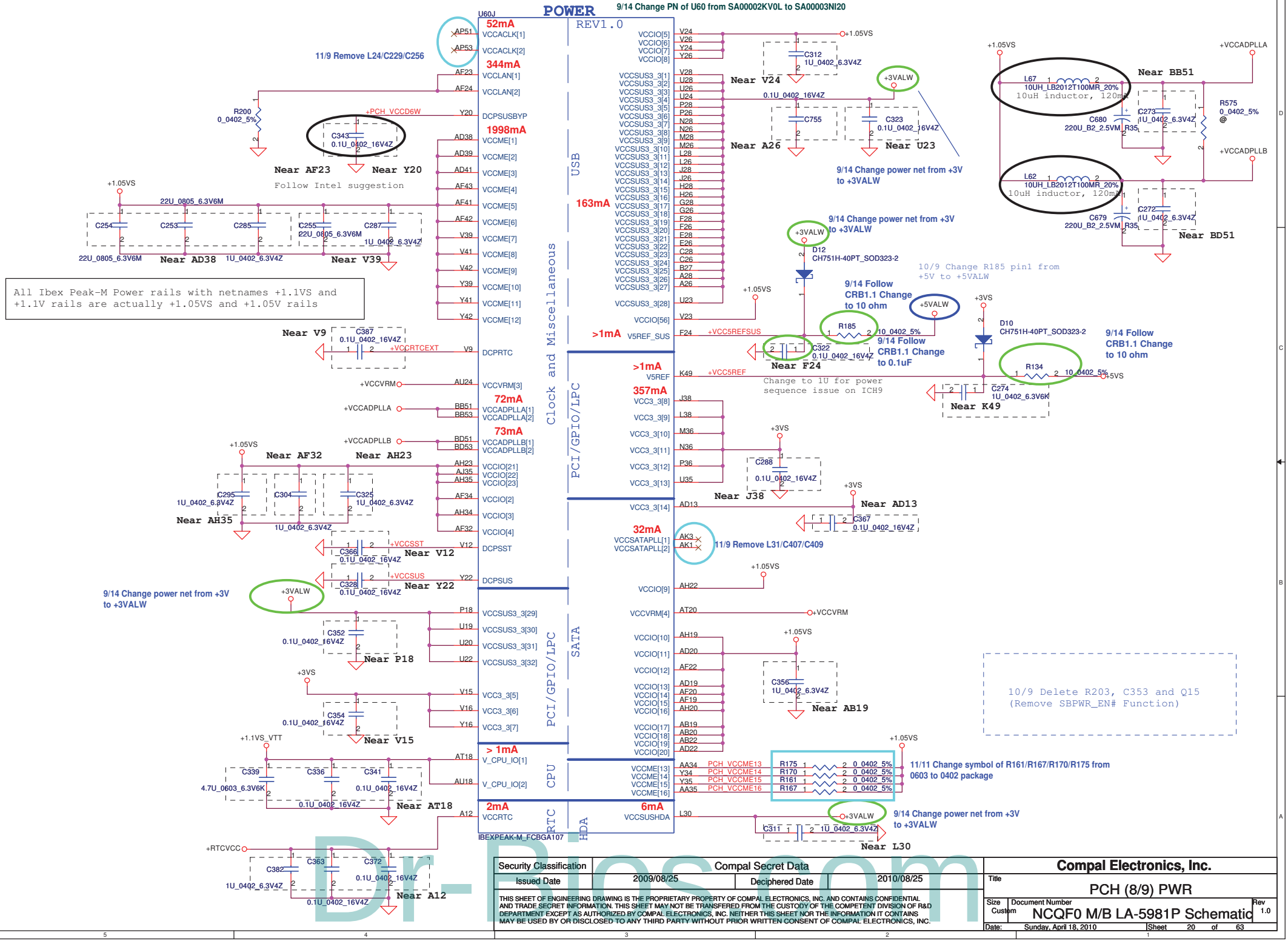
Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 | Sheet 18 of 63



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	PCH (7/9) PWR		
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic	Rev: 1.0	
Date: Sunday, April 18, 2010	Sheet 19 of 63		



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 | Sheet 20 of 63

U60I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE46	VSS[203]	VSS[303]	U30
BE48	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BE6	VSS[206]	VSS[306]	U34
BE8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D51	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
E48	VSS[237]	VSS[337]	Y32
E6	VSS[238]	VSS[338]	Y38
E8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	P49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G32	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AD47
G44	VSS[250]	VSS[350]	Y47
G52	VSS[251]	VSS[351]	AT12
AF39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK39
H38	VSS[257]	VSS[366]	AV14
H42	VSS[258]		

REV1.0

IBEXPEAK-M_FCBGA107

9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

U60H

AB16	VSS[0]	
AA19	VSS[1]	AK30
AA20	VSS[2]	AK31
AA22	VSS[3]	AK32
AM19	VSS[4]	AK34
AA24	VSS[5]	AK35
AA26	VSS[6]	AK38
AA28	VSS[7]	AK43
AA30	VSS[8]	AK46
AA31	VSS[9]	AK49
AA32	VSS[10]	AK5
AB11	VSS[11]	AK8
AB15	VSS[12]	AL2
AB23	VSS[13]	AL52
AB30	VSS[14]	AM11
AB31	VSS[15]	BB44
AB32	VSS[16]	AD24
AB39	VSS[17]	AM20
AB43	VSS[18]	AM22
AB47	VSS[19]	AM24
AB5	VSS[20]	AM26
AB8	VSS[21]	AM28
AC2	VSS[22]	BA42
AC52	VSS[23]	AM30
AD11	VSS[24]	AM31
AD12	VSS[25]	AM32
AD16	VSS[26]	AM34
AD23	VSS[27]	AM35
AD30	VSS[28]	AM38
AD31	VSS[29]	AM39
AD32	VSS[30]	AM42
AD34	VSS[31]	AU20
AU22	VSS[32]	AM46
AD42	VSS[33]	AV22
AD46	VSS[34]	AM49
AD49	VSS[35]	AM7
AD7	VSS[36]	AA50
AE2	VSS[37]	BB10
AE4	VSS[38]	AN32
AF12	VSS[39]	AN50
Y13	VSS[40]	AN52
AH49	VSS[41]	AP12
AU4	VSS[42]	AP42
AF35	VSS[43]	AP46
AP13	VSS[44]	AP49
AN34	VSS[45]	AP5
AF45	VSS[46]	AP8
AF46	VSS[47]	AR2
AF49	VSS[48]	AR52
AF5	VSS[49]	AT11
AF8	VSS[50]	BA12
AG2	VSS[51]	AH48
AG52	VSS[52]	AT32
AH11	VSS[53]	AT36
AH15	VSS[54]	AT41
AH16	VSS[55]	AT47
AH24	VSS[56]	AT7
AH32	VSS[57]	AV12
AV18	VSS[58]	AV16
AH43	VSS[59]	AV20
AH47	VSS[60]	AV24
AH7	VSS[61]	AV30
AJ19	VSS[62]	AV34
AJ2	VSS[63]	AV38
AJ20	VSS[64]	AV42
AJ22	VSS[65]	AV46
AJ23	VSS[66]	AV49
AJ26	VSS[67]	AV5
AJ28	VSS[68]	AV8
AJ32	VSS[69]	AW14
AJ34	VSS[70]	AW18
AT5	VSS[71]	AW2
AJ4	VSS[72]	BF9
AK12	VSS[73]	AW32
AM41	VSS[74]	AW36
AN19	VSS[75]	AW40
AK26	VSS[76]	AW52
AK22	VSS[77]	AY11
AK23	VSS[78]	AY43
AK28	VSS[79]	AY47
		VSS[158]

REV1.0

IBEXPEAK-M_FCBGA107

9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

1. dGPU Power On at Post

(1) Check DGPU_PRSNT (GPIO37) is low

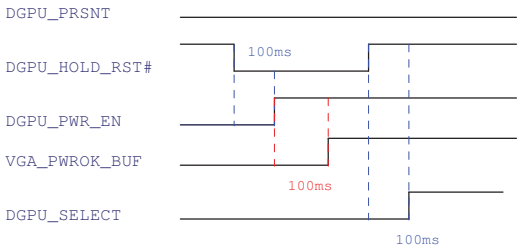
(2) Hold DGPU_HOLD_RST# (GPIO16) low, and wait for 100ms

(3) Set DGPU_PWR_EN (GPIO36) high, and wait for 100ms

(4) If, after 100 ms, VGA_PWROK_BUF (GPIO17) is not asserted high, then it is a fatal error

(5) Set DGPU_HOLD_RST# pin high and wait 100ms

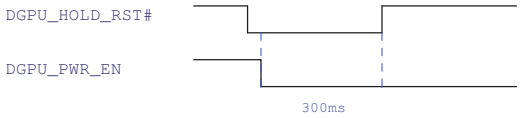
(6) DGPU_SELECT is high



2. dGPU Power On at Runtime

(1) 3 interposer
- Ⅰ. DGPU_HOLD_RST# held low
- Ⅱ. DGPU_PWR_EN held high to turn on DGPU
- Ⅲ. Delay 300ms

(2) DGPU_HOLD_RST# held high



3. dGPU Power OFF at Runtime

(1) Set DGPU_HOLD_RST# low

(2) Set DGPU_PWR_EN low

DGPU_PWR_EN:
-Driven by BIOS to turn on/off discrete graphic power.

VGA_PWROK_BUF:
-Driven by dGPU VR to indicate the power status to PCH.
-Used to enable clocks to dGPU.

DGPU_HOLD_RST#:
-Discrete Graphic Enable signal. Controlled by BIOS and driven by PCH GPIO.
-Used to gate with Platform Reset to enable the Reset for DGPU.

DGPU_SELECT:
-Select line for MUX to control the Display from iGPU or dGPU
-Needs to be controlled by BIOS.

DGPU_PWM_SELECT#
-Select line for MUX to control Backlight Inverter from iGPU or dGPU.

EDID_SELECT#
-Select line for MUX to control EDID from iGPU or dGPU.

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	PCH (9/9) VSS & PCH XDP Port		
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 1.0
Date: Sunday, April 18, 2010	Sheet 21 of 63		

10/14 Add By Vivian

U54 — 216-0769010 BROADWAY WAY@

U54 — 216-0774007 PARK PAR@

U54A

PCI EXPRESS INTERFACE

<4> PEG_HTX_C_GRX_P0	PEG_HTX_C_GRX_P0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_GTX_HRX_P0	C66	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_P0 <4>
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<4> PEG_HTX_C_GRX_N10	PEG_HTX_C_GRX_N10	K37	PCIE_RX10N	PCIE_TX10N	L32	PEG_GTX_HRX_N10	C63	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_N10 <4>
<4> PEG_HTX_C_GRX_P11	PEG_HTX_C_GRX_P11	K35	PCIE_RX11P	PCIE_TX11P	L30	PEG_GTX_HRX_P11	C90	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_P11 <4>
<4> PEG_HTX_C_GRX_N11	PEG_HTX_C_GRX_N11	J36	PCIE_RX11N	PCIE_TX11N	L29	PEG_GTX_HRX_N11	C91	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_N11 <4>
<4> PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P12	J38	PCIE_RX12P	PCIE_TX12P	K33	PEG_GTX_HRX_P12	C92	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_P12 <4>
<4> PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N12	H37	PCIE_RX12N	PCIE_TX12N	K32	PEG_GTX_HRX_N12	C93	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_N12 <4>
<4> PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P13	H35	PCIE_RX13P	PCIE_TX13P	J33	PEG_GTX_HRX_P13	C45	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_P13 <4>
<4> PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N13	G36	PCIE_RX13N	PCIE_TX13N	J32	PEG_GTX_HRX_N13	C46	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_N13 <4>
<4> PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P14	G38	PCIE_RX14P	PCIE_TX14P	K30	PEG_GTX_HRX_P14	C80	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_P14 <4>
<4> PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N14	F37	PCIE_RX14N	PCIE_TX14N	K29	PEG_GTX_HRX_N14	C81	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_N14 <4>
<4> PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P15	F35	PCIE_RX15P	PCIE_TX15P	H33	PEG_GTX_HRX_P15	C64	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_P15 <4>
<4> PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N15	E37	PCIE_RX15N	PCIE_TX15N	H32	PEG_GTX_HRX_N15	C65	VGA@ .1U_0402_16V7K	PEG_GTX_C_HRX_N15 <4>

CLOCK

<14> CLK_PEG_VGA	CLK_PEG_VGA	AB35	PCIE_REFCLKP
<14> CLK_PEG_VGA#	CLK_PEG_VGA#	AA36	PCIE_REFCLKN

	AJ21		NC#1
	AK21		NC#2
<41,57> VGA_PWROK	VGA_PWROK	AH16	PWRGOOD
<17> PLTRST_VGA#	PLTRST_VGA#	AA30	PERSTB

CALIBRATION

PCIE_CALRP	Y30	PCIE_CALRP	R75 VGA@	1.27K_0402_1%
PCIE_CALRN	Y29	PCIE_CALRN	R82 VGA@	2K_0402_1%

VGA_PWROK — R517 @ 0_0402_5% — VGA_PWROK_R

VGA_PWROK_R — R766 10K_0402_1% VGA@

216-0772000 MADISON

MAD@

10/6 Change symbol of U54 to Madison-M2

M96 P/N : SA00002UQ50 (S IC 216-0729042-00 A13 M96 FCBGA962 0FA)

+1.0VSDGPU

9/14 Change poewr net to +1.0VSDGPU

ENVDD — R88 10K_0402_5% VGA@

VGA_PNL_PWM — R84 10K_0402_5% VGA@

add for DPST support.

U54G

LVDS CONTROL

VARY_BL	AK27	VGA_PNL_PWM	VGA_PNL_PWM <29>
DIGON	AJ27	ENVDD	ENVDD <29>

TXCLK_UP_DPF3P	AK35	VGA_TZCLK+	VGA_TZCLK+ <29>
TXCLK_UN_DPF3N	AL36	VGA_TZCLK-	VGA_TZCLK- <29>
TXOUT_U0P_DPF2P	AJ38	VGA_TZOUT0+	VGA_TZOUT0+ <29>
TXOUT_U0N_DPF2N	AK37	VGA_TZOUT0-	VGA_TZOUT0- <29>
TXOUT_U1P_DPF1P	AH35	VGA_TZOUT1+	VGA_TZOUT1+ <29>
TXOUT_U1N_DPF1N	AJ36	VGA_TZOUT1-	VGA_TZOUT1- <29>
TXOUT_U2P_DPF0P	AG38	VGA_TZOUT2+	VGA_TZOUT2+ <29>
TXOUT_U2N_DPF0N	AH37	VGA_TZOUT2-	VGA_TZOUT2- <29>
TXOUT_U3P	AF35	T12	
TXOUT_U3N	AG36	T13	

LVTMDP

@ @

TXCLK_LP_DPE3P	AP34	VGA_TXCLK+	VGA_TXCLK+ <29>
TXCLK_LN_DPE3N	AR34	VGA_TXCLK-	VGA_TXCLK- <29>
TXOUT_L0P_DPE2P	AW37	VGA_TXOUT0+	VGA_TXOUT0+ <29>
TXOUT_L0N_DPE2N	AU35	VGA_TXOUT0-	VGA_TXOUT0- <29>
TXOUT_L1P_DPE1P	AR37	VGA_TXOUT1+	VGA_TXOUT1+ <29>
TXOUT_L1N_DPE1N	AU39	VGA_TXOUT1-	VGA_TXOUT1- <29>
TXOUT_L2P_DPE0P	AP35	VGA_TXOUT2+	VGA_TXOUT2+ <29>
TXOUT_L2N_DPE0N	AR35	VGA_TXOUT2-	VGA_TXOUT2- <29>
TXOUT_L3P	AN36	T15	
TXOUT_L3N	AP37	T14	

@ @

216-0772000 MADISON

10/6 Change symbol of U54 to Madison-M2

MAD@

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Mannhatton_ PCIE / LVDS

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 22 of 63

Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
CONFIG[1] CONFIG[2] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
SMS_EN_HARD	H2SYNC	Can be unconnected if not used.	0
VIP_DEVICE _STRAP_DIS	V2SYNC	Can be unconnected if not used.	0

Madison Pro

Location / VRAM	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
ATI(8pcs)1GB	O	1	O	O
* Samsung(8pcs) 1GB	O	1	O	1
Hynix(8pcs) 1GB	O	1	1	O
Samsung(8pcs) 128*16	1	1	O	1
Hynix(8pcs) 128*16	1	1	1	O

Broadway Pro

Location / VRAM	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
ATI(8pcs)1GB	O	1	O	O
Samsung(8pcs) 1GB	O	1	O	1
* Hynix(8pcs) 1GB	O	1	1	O
Samsung(8pcs) 128*16	1	1	O	1
Hynix(8pcs) 128*16	1	1	1	O

External VGA Thermal Sensor

PWR Sequence

+3VS_DELAY
VGA_CORE (VDDC)
+1.8VS

M96 only

CRT

HDMI

FLASH ROM

U22 AT25F512B-SSH-T_SOP8

+3VS_DELAY

100mA

70mA

45mA

50mA

130mA

1.5mA

75mA

125mA

5mA

9/14 Change part of C72 to 10uF(ATI suggest)

9/14 Modify PWR Seq

8/25 ATI suggest

8/25 Modify by Vivian

10/19 Add by Vivian

9/14 Change poewr net to +1.0VSDGPU

9/21 Add R378 PU to +3VS_DELAY(Slove system boot up hangs issue)

9/21 Add R666 PD to GND(Slove system boot up hangs issue)

12/7 Add C567=@100pF(Avoid noise)

Do not PU R177 for GPIO22 if not implement external flash ROM

11/2 Add R648

10/5 Add

9/10 Change symbol of Q76 to SC70-3

1/14 Change PN of Q9 from SB00000AR00 to SB00000D900(material issue)

3/2 Change Bom structure of C120 to mount,Change value of R525 to 24k ohm(1%)

Use boradway GPU, R28 change to 0 Ohm(SD028000080)

10/27 Add R670/R678/R685/R691
10/27 Place R670 Close to U22,R678/R685/R691 close to U54

1/6 Change PN of U22 from SA00001O100 to SA00003NH00

10/6 Change symbol of U54 to Madison-M2

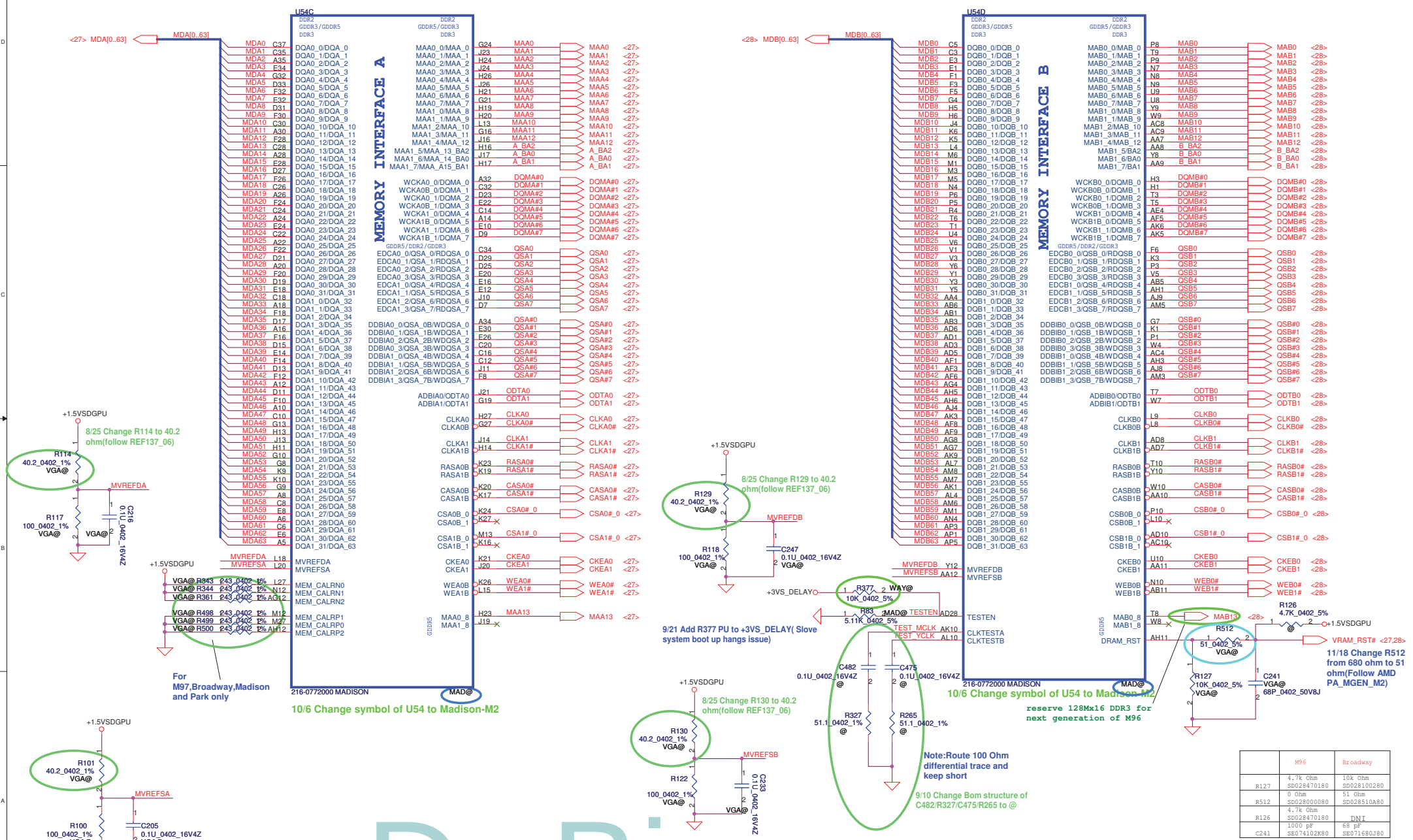
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Mannhatton_Strape/DP/HDMI//CRT

Size: C | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 23 of 63



	M96	Broadway
R127	4.7k Ohm SD028470180	10k Ohm SD028100280
R512	0 Ohm SD028000080	51 Ohm SD028510A80
R126	4.7k Ohm SD028470180	DNI
C241	1000 pF SE074102K80	68 pF SE071680J80

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.	
Title	Mannhatton_ Memory
Size / Document Number	Custom / NCQF0 M/B LA-5981P Schematic
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Date:	Sunday, April 18, 2010
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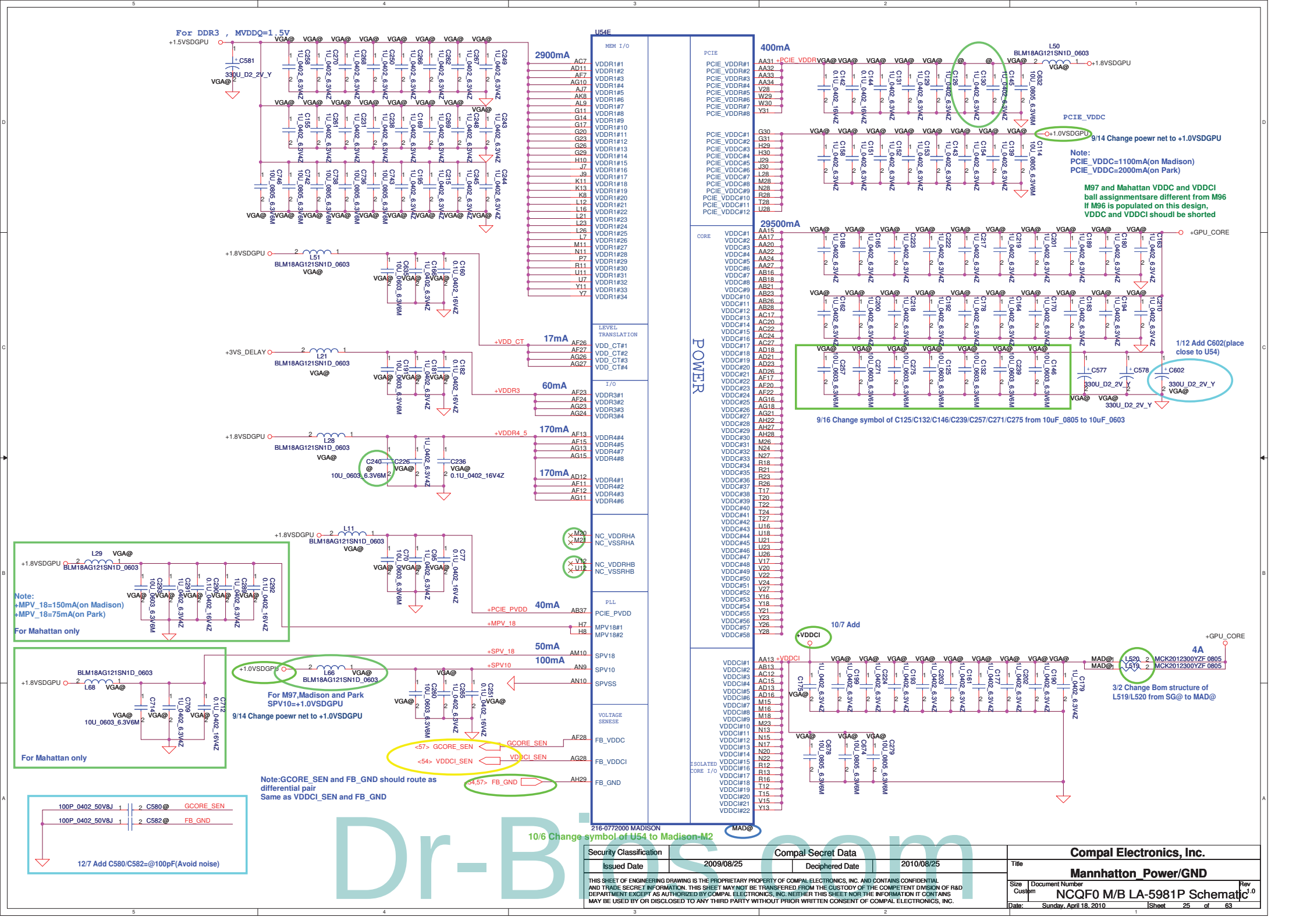

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **Mannhatton_Power/GND**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

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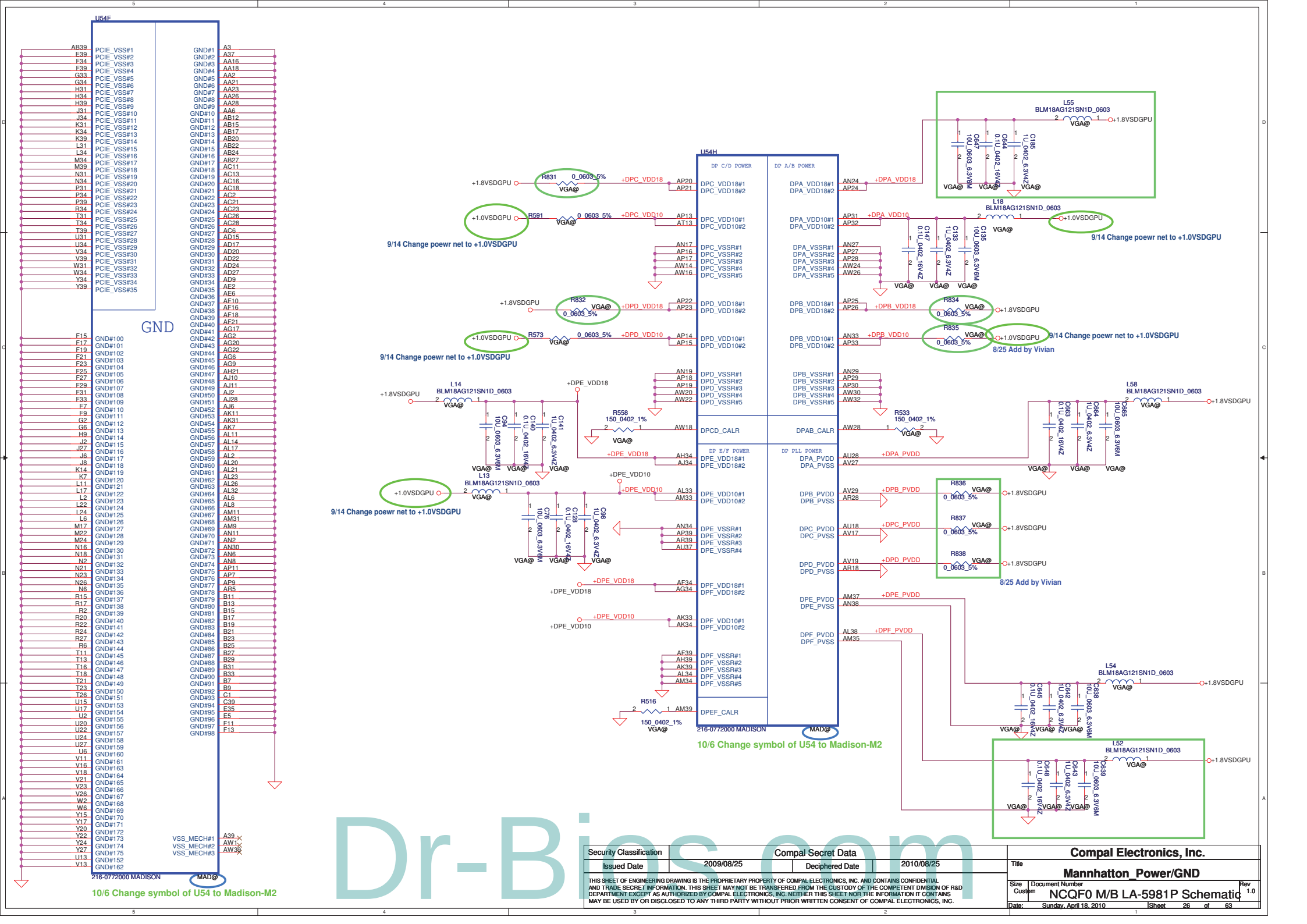

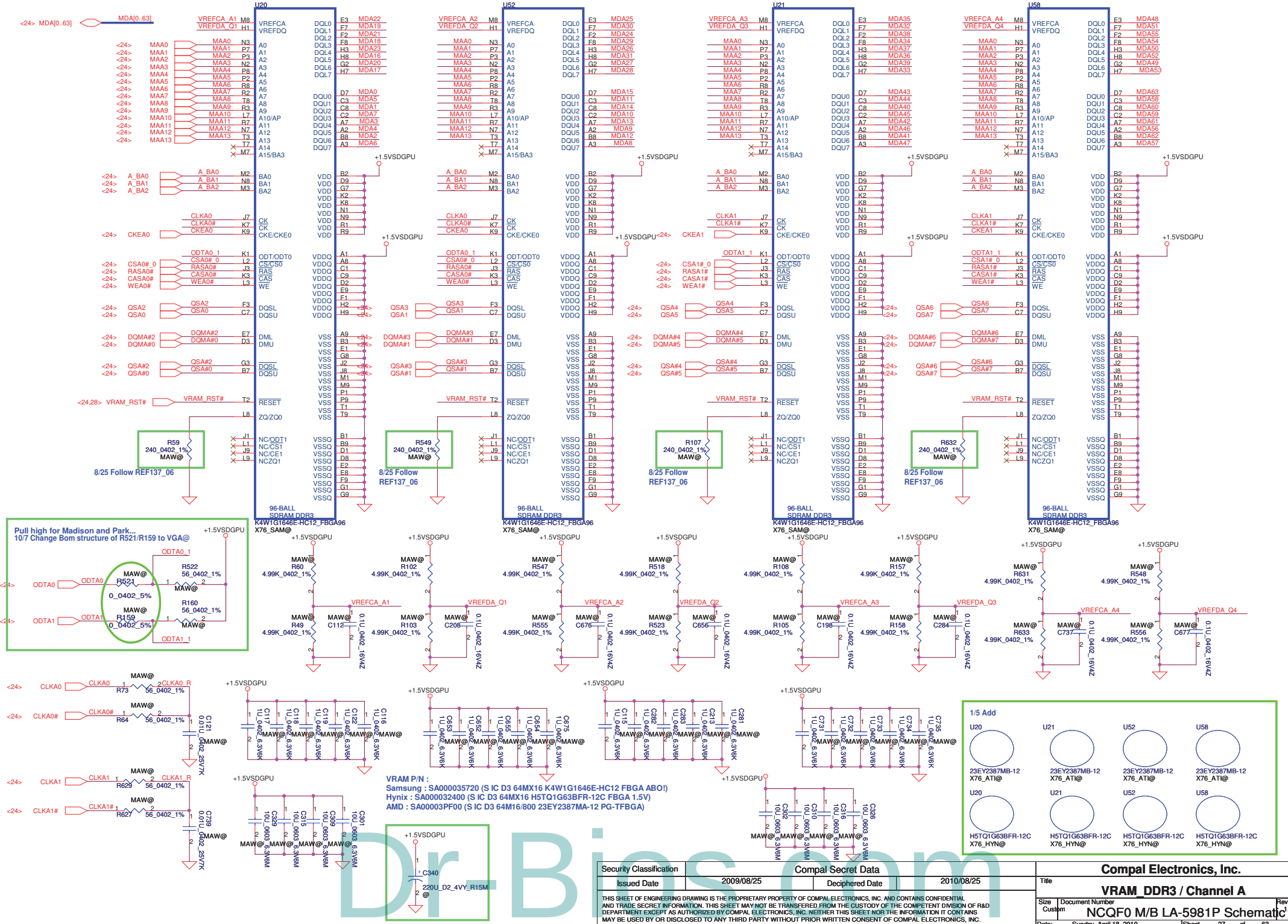

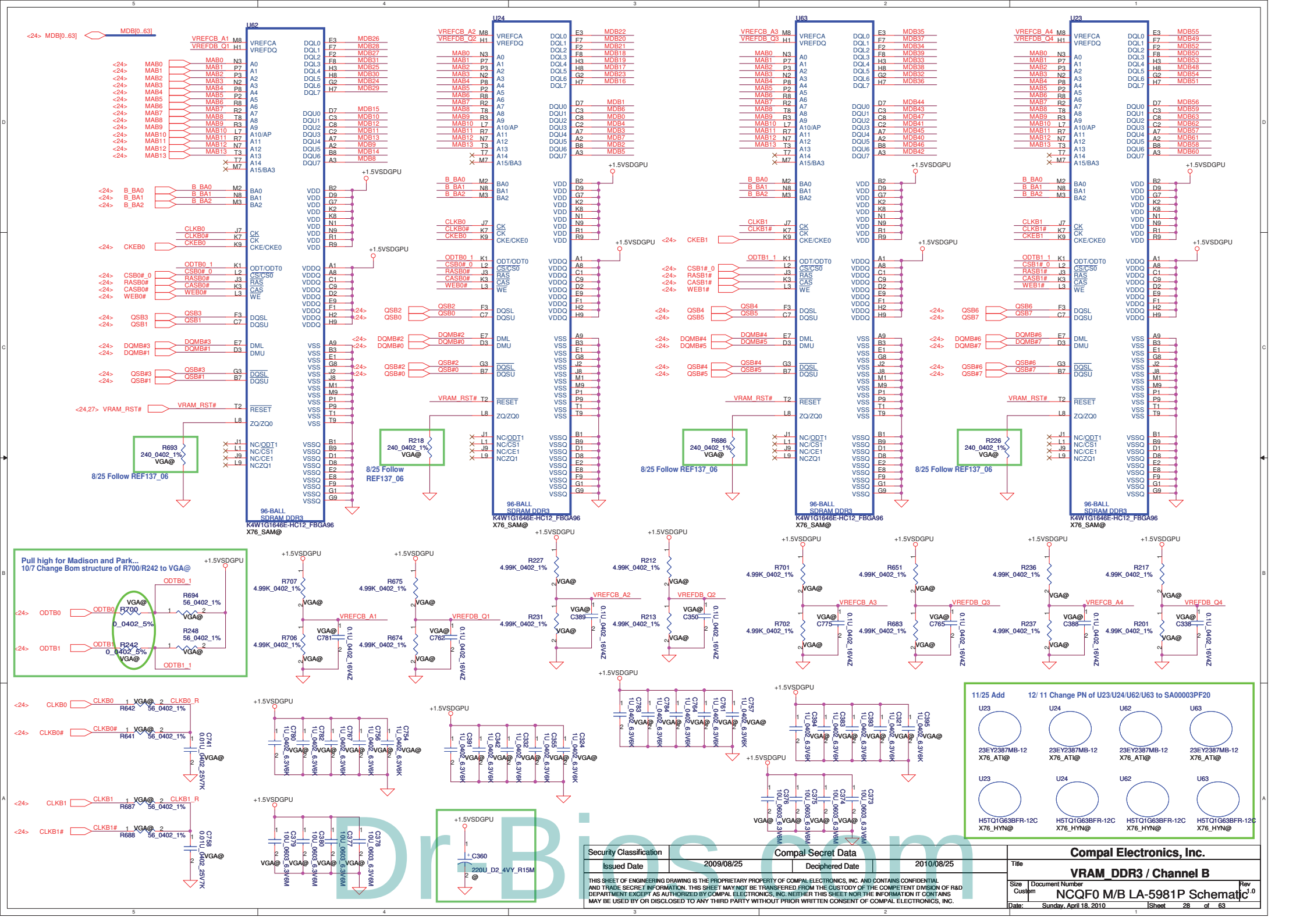
U62
U24
U63
U23
96-BALL SDRAM DDR3
K4W1G1646E-HC12_FBGA96
X76_SAM@
+1.5VSDGPU
MDB[0..63]
8/25 Follow REF137_06
Pull high for Madison and Park...
10/7 Change Bom structure of R700/R242 to VGA@
11/25 Add
12/ 11 Change PN of U23/U24/U62/U63 to SA00003PF20
23EY2387MB-12 X76_ATI@
H5TQ1G63BFR-12C X76_HYN@
Security Classification
Compal Secret Data
Issued Date
2009/08/25
Deciphered Date
2010/08/25
Compal Electronics, Inc.
VRAM_DDR3 / Channel B
NCQF0 M/B LA-5981P Schematic
Rev 1.0
Sunday, April 18, 2010
Sheet 28 of 63

LCD POWER CIRCUIT

1/14 Change PN of Q6 from SB00000AR00 to SB00000D900(material issue)

9/14 Change power net from +3V to +3VALW

W=60mils

4/17 Add D22

Reserved for DIS Only

GPU Support DPST for DIS Only

4/16 Add

4/16 Add R46

SG For LVDS

SEL=LOW, B1
SEL=High, B2

9/1 Del D5/R22(BKOFF# not need to pull high)

LED PANEL Conn.

W=40mils

10/14 Change R16/R17 to 2.2K ohm

1/14 Change PN of Q80 from SB00000AR00 to SB00000D900(material issue)

11/11 Change R65/R91 to 2.2K ohm

1/14 Change PN of Q81 from SB00000AR00 to SB00000D900(material issue)

DIS ONLY

9/1 Add L7(EMI Suggest)

9/14 Add R777(by Vivian)

9/16 Add D25(by Vivian)

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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CRT Connector

10/14 Change PN of L40/L43/L48 to SM01000AX00

L48 MBK1608221YZF_2P @
L43 MBK1608221YZF_2P @
L40 MBK1608221YZF_2P @

W=40mils
+5VS
+R_CRT_VCC
+CRT_VCC
D2 RB491D_SC59-3
F1 1.1A_6V_SMD1812P110TF
W=40mils
C17 0.1U_0402_16V4Z

10/14 Change to 0 ohm for DIS

CRT_R L48 0_0603_5% CRT_R_1 L49 FCM2012CF-800T06_2P CRT_R_2
CRT_G L43 0_0603_5% CRT_G_1 L44 FCM2012CF-800T06_2P CRT_G_2
CRT_B L40 0_0603_5% CRT_B_1 L41 FCM2012CF-800T06_2P CRT_B_2

R508 150_0402_1%
R503 150_0402_1%
R501 150_0402_1%
C631 12P_0402_50V8J
C623 12P_0402_50V8J
C611 12P_0402_50V8J
Change to 15pF for DIS
C630 @ 22P_0402_50V8J
C615 @ 22P_0402_50V8J
C610 @ 22P_0402_50V8J
C50 15P_0402_50V8J
C41 15P_0402_50V8J
C24 15P_0402_50V8J
Change to 12pf for DIS

JCRT1
RGND
ID0
Red
GGND
SDA
Green
BGND
Hsync
Blue
+5V
Vsync
res
SGND
SCL
GND
GND
GND
SUYIN_070546FR015S263ZR @

C18 100P_0402_50V8J
CRT_DET# <18>
DSUB_12
DSUB_15
R13 100K_0402_5%
C37 10P_0402_50V8J
C19 10P_0402_50V8J
C40 68P_0402_50V8J
C14 68P_0402_50V8J
+CRT_VCC

11/13 Change symbol of JCRT1 from DC060003O00 to DC060003N00

9/14 Change description and value of L2/L3.

L3 BLM18AG121SN1D_0603
L2 BLM18AG121SN1D_0603
CRT_HSYNC_2
CRT_VSYNC_2

C49 0.1U_0402_16V4Z
+CRT_VCC
R21 10K_0402_5%
U12
CRT_HSYNC
CRT_HSYNC_1
74AHCT1G125GW_SOT353-5

C29 0.1U_0402_16V4Z
+CRT_VCC
U4
CRT_VSYNC
CRT_VSYNC_1
74AHCT1G125GW_SOT353-5

+3VS
C113 0.1U_0402_16V4Z SG@
C173 0.1U_0402_16V4Z SG@
C172 0.1U_0402_16V4Z SG@
C171 0.1U_0402_16V4Z SG@

U17 SG@
+3VS
VDD VDD VDD VDD VDD
0B1 1B1 2B1 3B1 4B1 5B1 6B1
2B2 1B2 2B2 3B2 4B2 5B2 6B2
GND GND GND GND GND GPAD
A0 A1 A2 A3 A4 SEL1 A5 A6 SEL2
CRT_R CRT_G CRT_B CRT_HSYNC CRT_VSYNC
DGPU_SELECT# DGPU_SELECT# <17,29>
DSUB_12_R DSUB_15_R
10/14 Change net name
DGPU_EDIDSEL_R# DGPU_EDIDSEL_R# <29>

<23> VGA_CRT_R VGA_CRT_R
<23> VGA_CRT_G VGA_CRT_G
<23> VGA_CRT_B VGA_CRT_B
<23> VGA_CRT_HSYNC VGA_CRT_HSYNC
<23> VGA_CRT_VSYNC VGA_CRT_VSYNC
<23> VGA_DDC_DATA VGA_DDC_DATA
<23> VGA_DDC_CLK VGA_DDC_CLK

<16> PCH_CRT_R PCH_CRT_R
<16> PCH_CRT_G PCH_CRT_G
<16> PCH_CRT_B PCH_CRT_B
<16> PCH_CRT_HSYNC PCH_CRT_HSYNC
<16> PCH_CRT_VSYNC PCH_CRT_VSYNC
<16> PCH_CRT_DATA PCH_CRT_DATA
<16> PCH_CRT_CLK PCH_CRT_CLK

PI3V712-AZLEX_TQFN32_6X3~D

L	B1	DIS
H	B2	UMA

9/10 Change U17 from SA000026Y00 to SA00003B300
Michael

VGA DDC PU 4.7K on Page 23
Reserved for DIS only

10/14 Add R55/R56= 0 ohm
VGA_DDC_DATA R55 DIS@ DSUB_12_R 0_0402_5%
VGA_DDC_CLK R56 DIS@ DSUB_15_R 0_0402_5%
+3VS
+CRT_VCC
R15 2.2K_0402_5%
R14 2.2K_0402_5%
Q84A DMN66D0LDW-7 2N_SOT363-6 VGA@
Q84B DMN66D0LDW-7 2N_SOT363-6 VGA@
DSUB_12
DSUB_15

4/2 Change PN of Q84 from SB00000D900 to SB00000DH00(ESD issue)

Reserved for DIS only

VGA_CRT_G VGA_CRT_R RP11 DIS@ 0_0404_4P2R_5% CRT_G CRT_R
VGA_CRT_HSYNC VGA_CRT_B RP12 DIS@ 0_0404_4P2R_5% CRT_HSYNC CRT_B
VGA_CRT_VSYNC R53 DIS@ 0_0402_5% CRT_VSYNC

9/14 Change to RP for layout request
Michael

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2009/08/25

Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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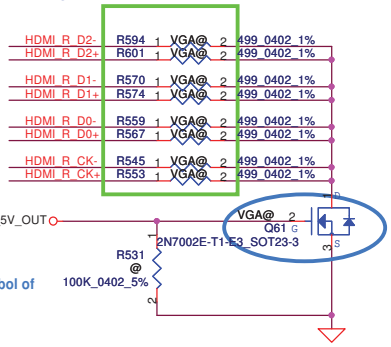
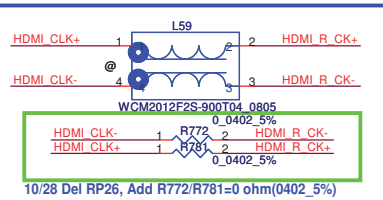
Place closed to JHDMI1

9/14 Change Bom structure from DIS @ to VGA@

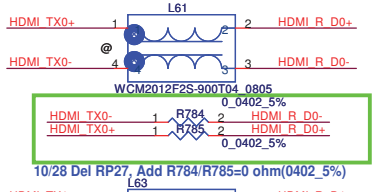


9/23 Change symbol of Q61 to SOT23-3

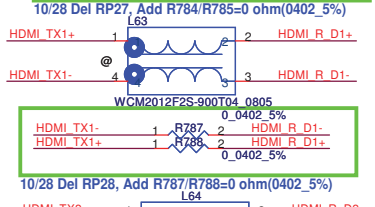
4/2 Change PN of Q61 from SB570020110 to SB000008J10



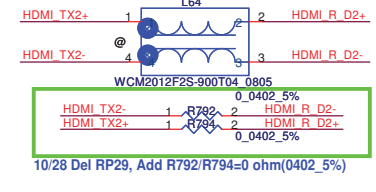
10/28 Del RP26, Add R772/R781=0 ohm(0402_5%)



10/28 Del RP27, Add R784/R785=0 ohm(0402_5%)



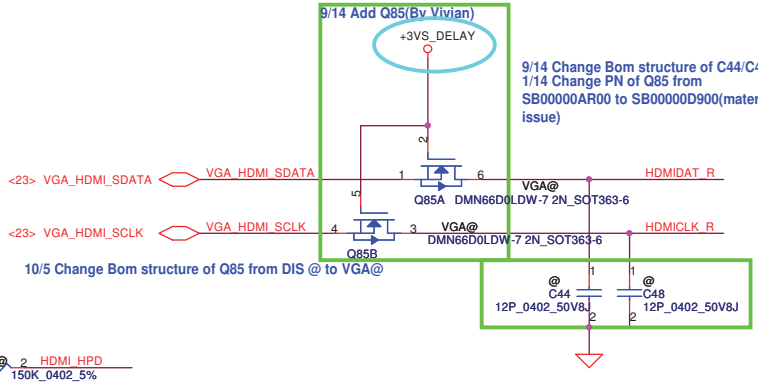
10/28 Del RP28, Add R787/R788=0 ohm(0402_5%)



10/28 Del RP29, Add R792/R794=0 ohm(0402_5%)

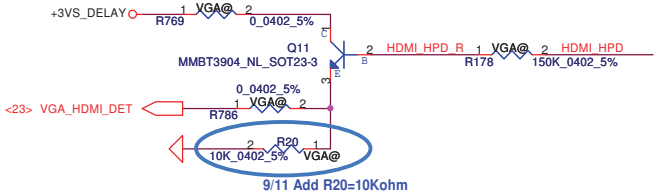
0914 Change to RP
Michael

9/14 Add Q85(By Vivian)

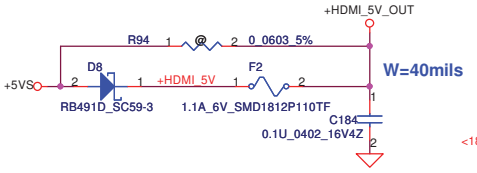


9/14 Change Bom structure of C44/C48 from DIS @ to @
1/14 Change PN of Q85 from SB00000AR00 to SB00000D900(material issue)

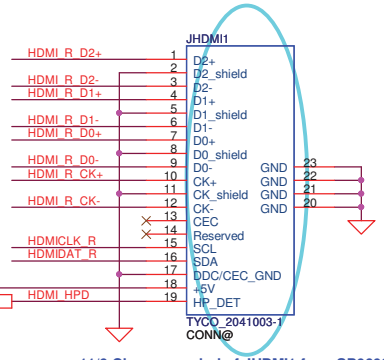
10/5 Change Bom structure of Q85 from DIS @ to VGA@



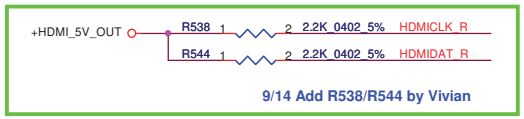
9/11 Add R20=10Kohm



W=40mils



11/9 Change symbol of JHDMI1 from SP060003Z00 to DC232000A00



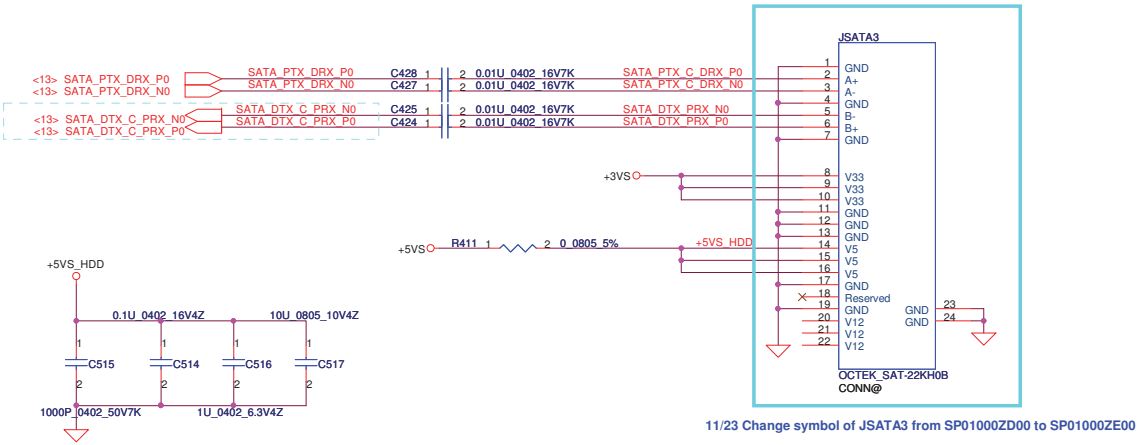
9/14 Add R538/R544 by Vivian

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	HDMI Level Shife & Conn		
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 1.0
Date: Sunday, April 18, 2010	Sheet 31 of 63		

HDD

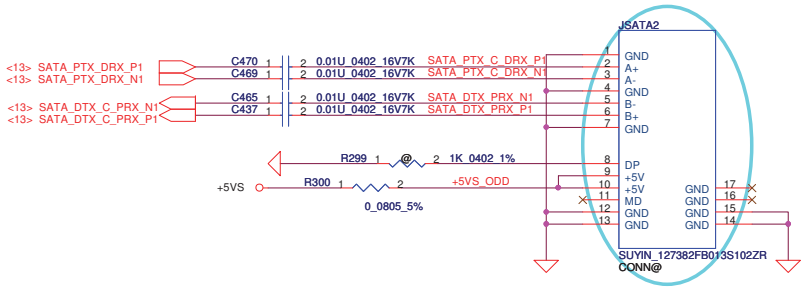
SATA HDD Conn.



11/23 Change symbol of JSATA3 from SP01000ZD00 to SP01000ZE00

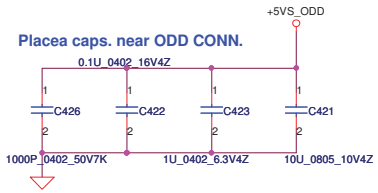
ODD

SATA ODD Conn.



12/1 Change symbol of JSATA2 to SUYIN_127382FB013S102ZR_13P(SP01000QJ00)

Placea caps. near ODD CONN.



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	HDD & ODD Connector		
Size B	Document Number NCQF0 M/B LA-5981P Schematic		Rev 1.0
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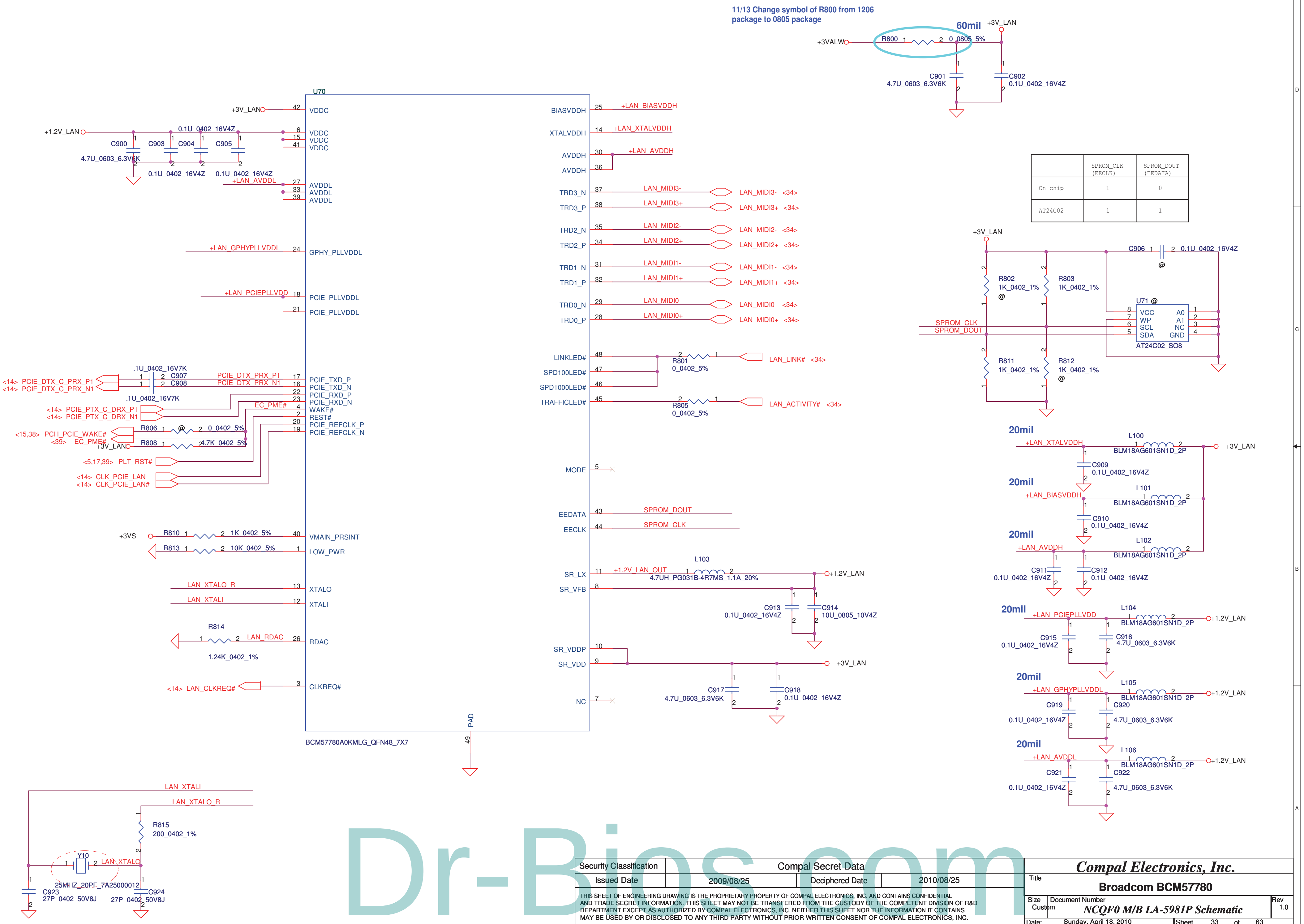


	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

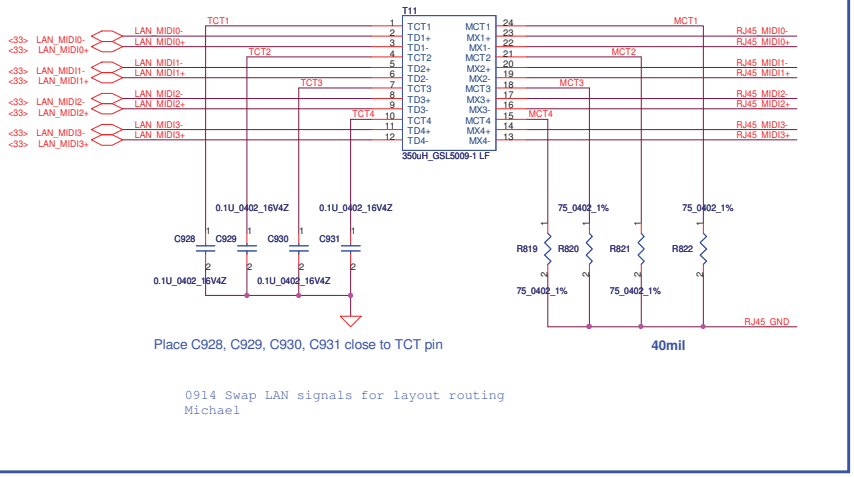
Compal Electronics, Inc.

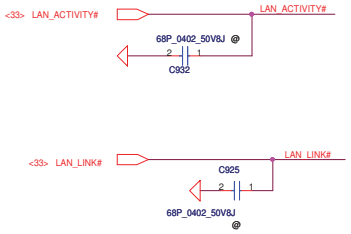
Title: **Broadcom BCM57780**

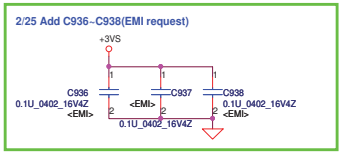
Size: Custom | Document Number: *NCQF0 M/B LA-5981P Schematic* | Rev 1.0

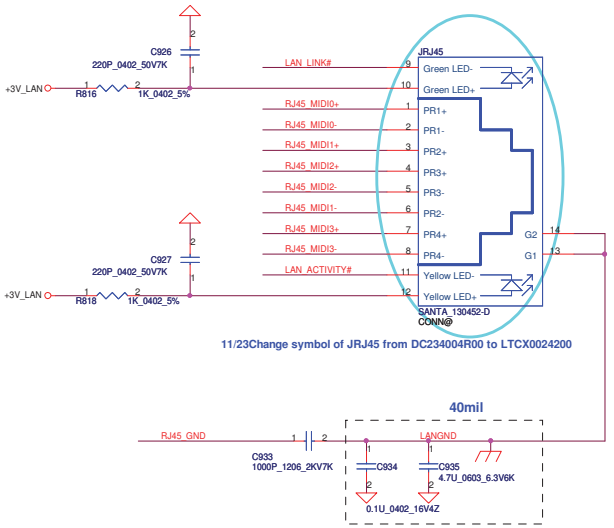
Date: Sunday, April 18, 2010 |

LAN Connector









Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	LAN Magnetic & RJ45		
Size	Document Number	NCQF0 M/B LA-5981P Schematic	Rev 1.0
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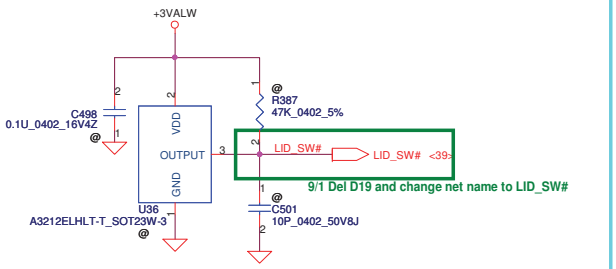
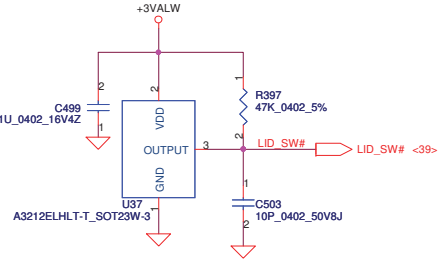
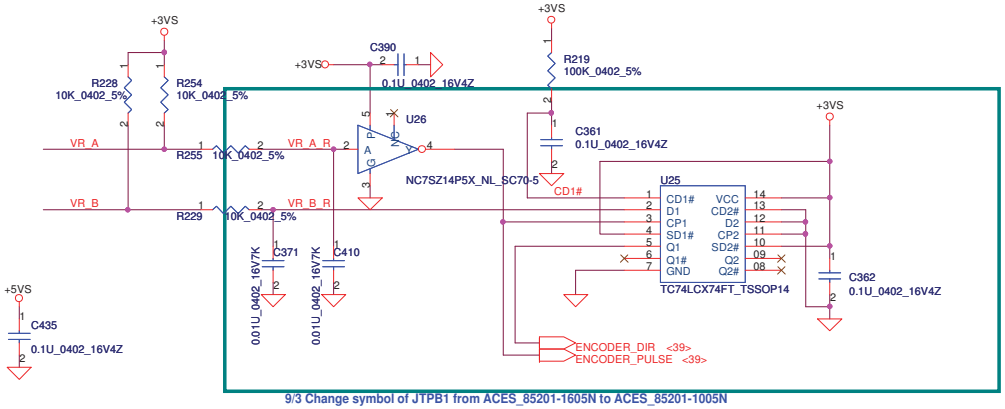
Lid Switch

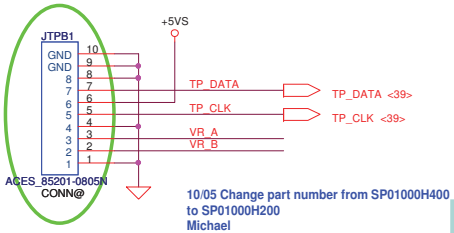
(Hall Effect Switch)

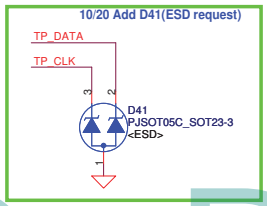




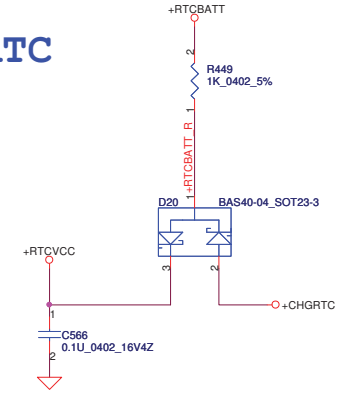
Touch Pad



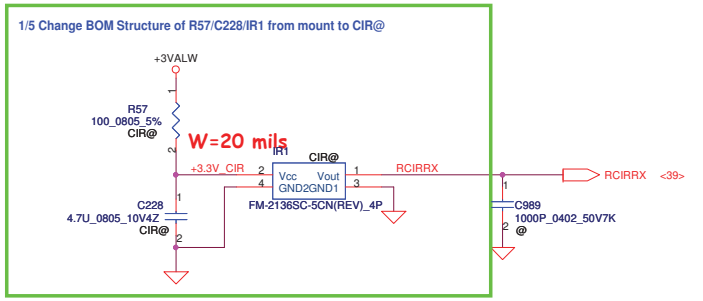




RTC



CIR



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	LID/RTC/CIR		
Size	Document Number	NCQF0 M/B LA-5981P Schematic	Rev 1.0
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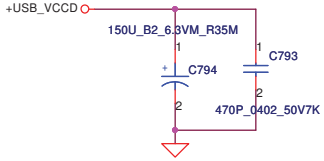
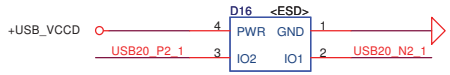
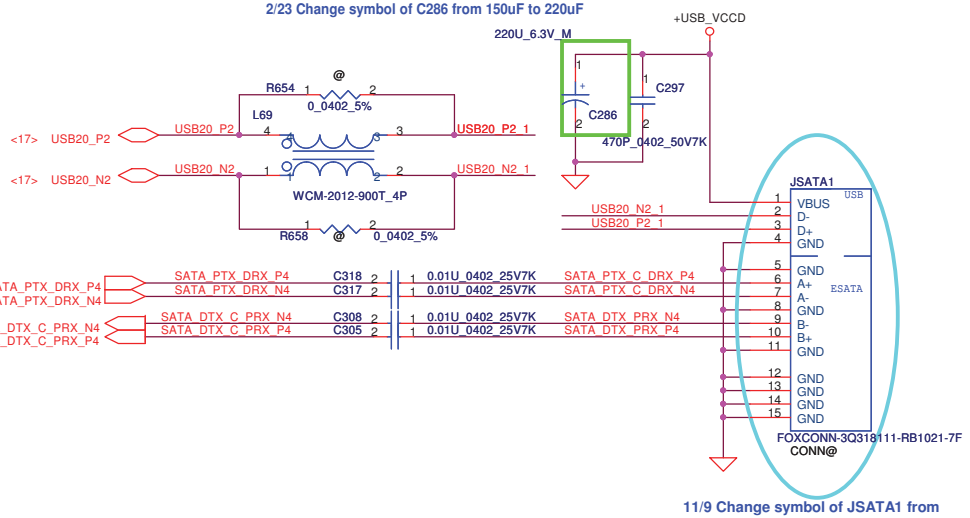
eSATA



10/28 Add symbol of D16 of SC300000P00

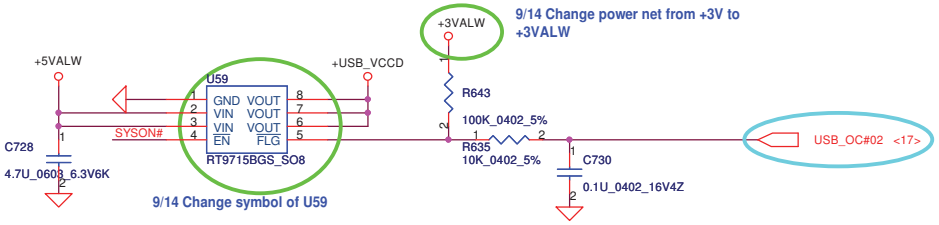


2/23 Change symbol of C286 from 150uF to 220uF



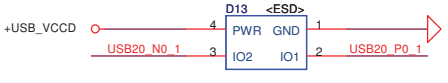
11/9 Change symbol of JSATA1 from DC230711060 to DC233004B00

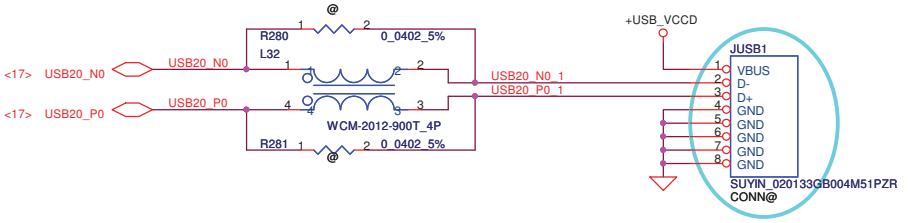
9/14 Change power net from +3V to +3VALW



9/14 Change symbol of U59

10/28 Change symbol of D13 from SC300000O00 to SC300000P00

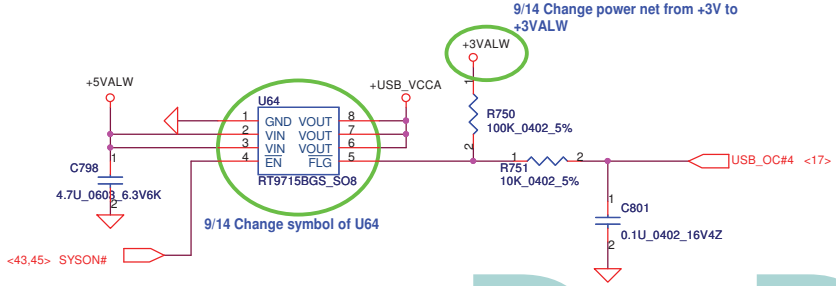




11/9 Change symbol of JUSB1 from SP01000F100 to SP060004200

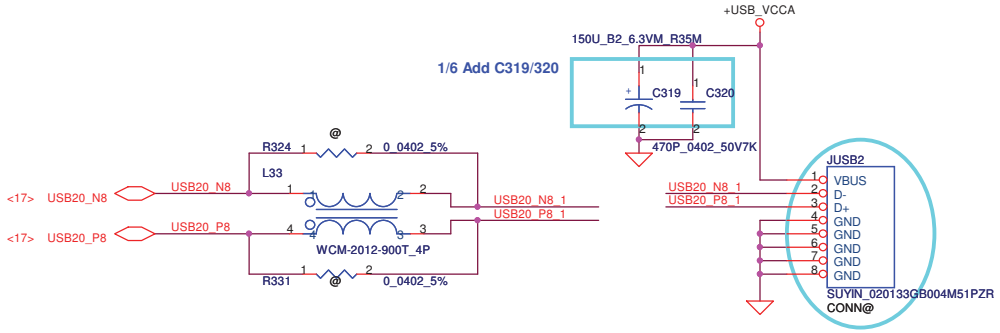
HS USB Port

9/14 Change power net from +3V to +3VALW



9/14 Change symbol of U64

1/6 Add C319/320



11/9 Change symbol of JUSB2 from SP01000B000 to SP060004200

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: USB / eSATA			
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 1.0
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SD,MMC,MS, xD muti-function pin define

MDIO PIN Name	SD/MMC PIN Name	MS Card PIN Name	xD Card PIN Name
MDIO00	SD7-DAT0	MS4-DATA0	XD10-D0
MDIO01	SD8-DAT1	MS3-DATA1	XD11-D1
MDIO02	SD9-DAT2	MS5-DATA2	XD12-D2
MDIO03	SD1-DAT3	MS7-DATA3	XD13-D3
MDIO04	SD2-CMD	MS2-BS	XD07-WE
MDIO05	SD5-CLK	MS8-SCLK	XD04-CE
MDIO06	SD-WP		XD08-WP
MDIO07			XD05-CLE
MDIO08			XD14-D4
MDIO09			XD15-D5
MDIO10			XD16-D6
MDIO11			XD17-D7
MDIO12			XD03-RE
MDIO13			XD02-R/B
MDIO14			XD06-ALE
CR1_LEDN			
CR1_PCTLN			
CR1_CD0N	SD-CD		XD01-CD
CR1_CD1N		MS6-INS	XD01-CD

NOTE

12/2 JMB380B--Mount D7/R24/R30,R849 use 8.2K ohm
12/2 JMB380C--Del D7/R24/R30,mount R853;R849 use 12K ohm

12/2 Add C104(Follow Spec)

12/2 Place C73/C68/C104 close to pin5 of U2

3/2 Change R849 to 12K ohm

3/2 Add R718/C168 for RESET

12/2 Add R853= 0 ohm(co-layout JMB380 revisonC)

12/2 Add R95(Place R95 close to pin24 of U2)

3/3 Change PN of U2 from SA000023A10 to SA000023A20(JMB380 Ver.B to Ver.C)

10/15 Change symbol of J1394A from SUYIN_020115FR004S550ZL_4P-T to SUYIN_020115FB004S512ZL_4P by Vivian

5 IN 1 CardRead

Memory Card Power

Close to Chip

9/1 1394 Differential Pairs=110 ohm

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Card Reader JMB380

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

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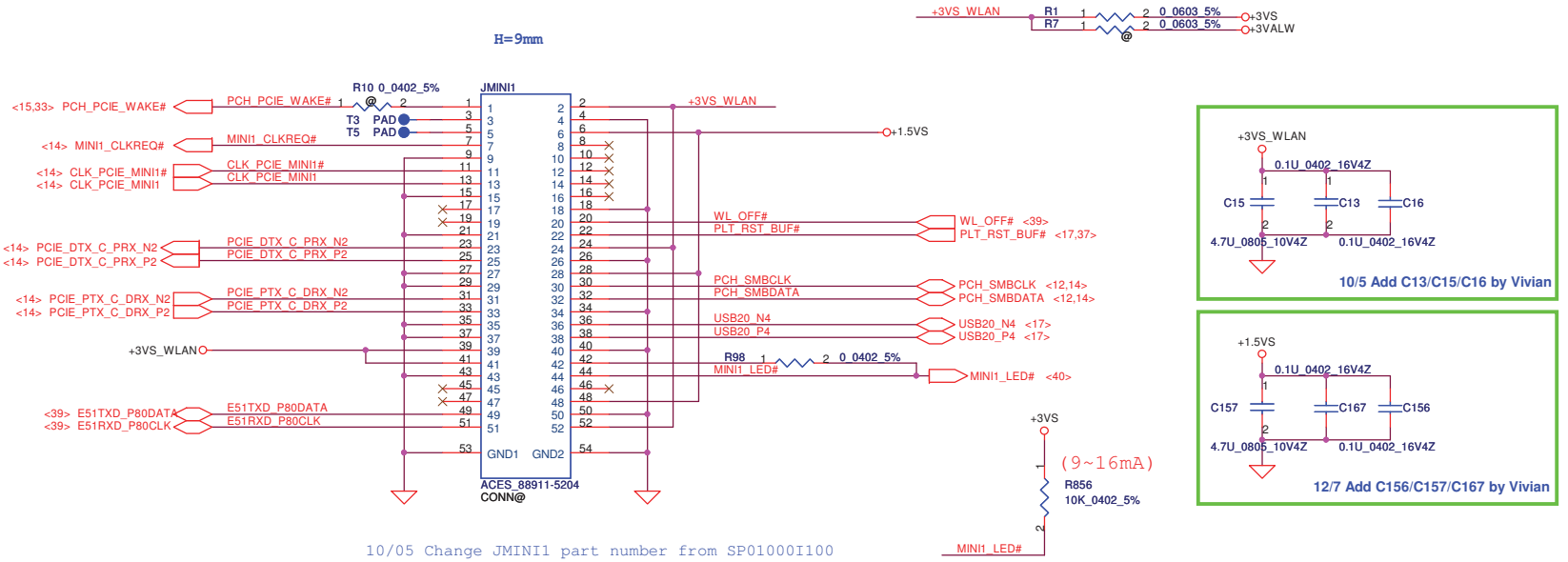
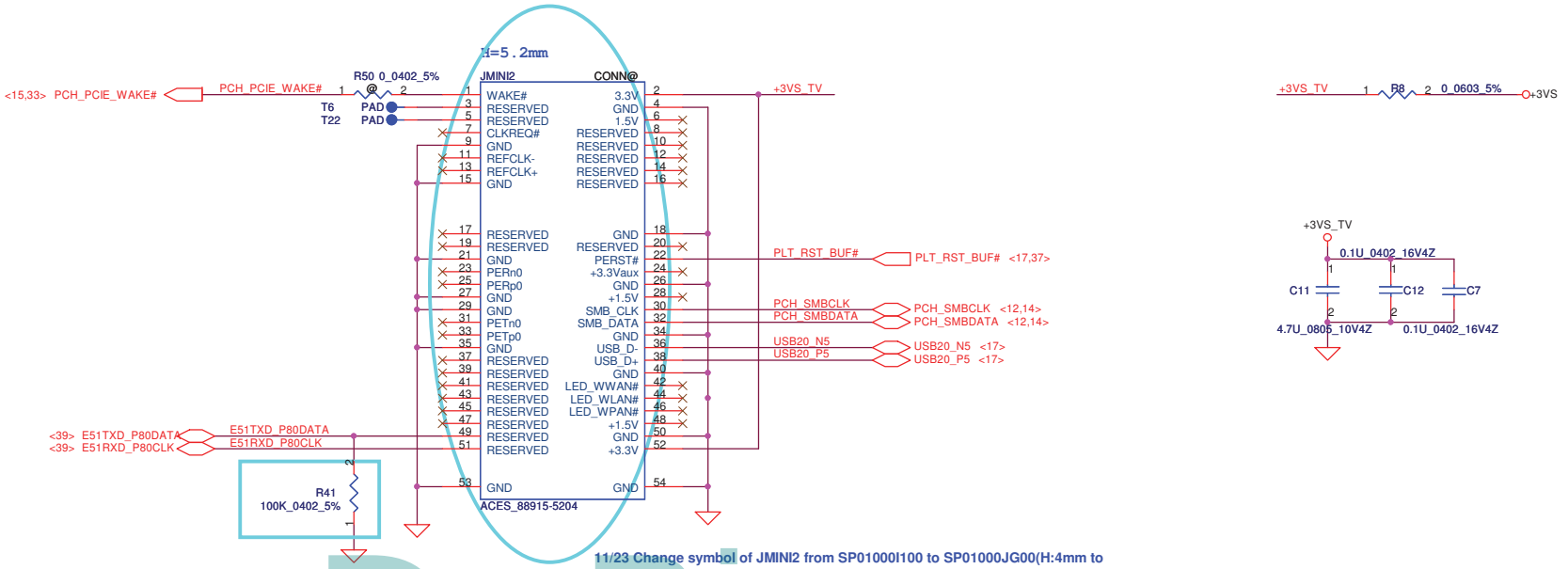
WLAN



10/05 Change JMINI1 part number from SP01000I100
to SP01000FP00
Michael

MINI



11/23 Change symbol of JMINI2 from SP01000I100 to SP01000JG00(H:4mm to H:5.2mm)

11/9 Change symbol of R41 from SD028100280 to SD028100380(10k ohm to 100k ohm)

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: WLAN&MINI			
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 1.0
Date: Sunday, April 18, 2010		Sheet 38 of 63	

For EC Tools

9/14 Change description and value of L36.

L36 BLM18AG121SN1D_0603

+3VALW_EC

+EC_VCCA

R354 0_0805_5%

C486 C524 C511 C525 C531 C530 1000P_0402_50V7K

0.1U_0402_16V4Z 0.1U_0402_16V4Z 0.1U_0402_16V4Z 0.1U_0402_16V4Z 1000P_0402_50V7K

C483 0.1U_0402_16V4Z

ECAGND

KSI[0..7] KSI[0..7] <40>

KSO[0..17] KSO[0..17] <40>

JP10 ACES_85205-0400 CONN@

E51RXD_P80CLK E51TXD_P80DATA

E51RXD_P80CLK <38> E51TXD_P80DATA <38>

9/14 Add By Vivian(EMI suggest)

C535 0.1U_0402_16V4Z @ EC_KBRST# <EMI>

U38

VCC VCC VCC VCC VCC VCC AVCC

12/11 Change PN of U38 from SA00001J580 to SA00001J5A0(Rev:D3 to E0)

12/ 11 Change R365 from 100K to 0 ohm(Follow EC request)

Ra R364 100K_0402_5% @

Rb R365 0_0402_5%

C484 0.1U_0402_16V4Z

AD_BID0

C533 @22P_0402_50V8J

R415 @33_0402_5%

<17> CLK_PCI_LPC

R408 47K_0402_5%

C520 0.1U_0402_16V4Z

R273 @ 0_0402_5%

11/11 Add R273=@ 0 ohm(Follow NAU00)

GA20/GPIO00 KBRST#/GPIO01 SERIRQ# LFRAME# LAD3 LAD2 LAD1 LAD0 PCICLK PCIRST#/GPIO05 ECRST# SCI#/GPIO0E CLKRUN#/GPIO1D

LPC & MISC

EC_GA20 EC_KBRST# SERIRQ LPC_FRAME# LPC_AD3 LPC_AD2 LPC_AD1 LPC_AD0 PLT_RST# EC_RST# EC_SCI# PM_CLKRUN#_R

INVT_PWM/PWM1/GPIO0F BEEP#/PWM2/GPIO10 FANPWM1/GPIO12 ACOFF/FANPWM2/GPIO13

PWM Output

BEEP# FAN_PWM ACOFF

ACOFF <49,50> ECAGND

C494 0.01U_0402_16V7K

BATT_TEMP_AD0/GPIO38 BATT_OVP/AD1/GPIO39 ADP_I/AD2/GPIO3A AD3/GPIO3B AD4/GPIO42 SELIO2#/AD5/GPIO43

AD Input

BATT_TEMP BATT_OVP ADP_I AD_BID0 ENCODER_DIR

BATT_TEMP <48>

BATT_OVP <50> ADP_I <50>

ENCODER_DIR <35>

9/1 Change net to ENCODER_DIR

DAC_BRIG/DA0/GPIO3C EN_DFAN1/DA1/GPIO3D IREF/DA2/GPIO3E DA3/GPIO3F

DA Output

RF_DISABLE# IREF CALIBRATE#

RF_DISABLE# <43> IREF <50> CALIBRATE# <50>

+5VS

TP_CLK 4.7K_0402_5% R356

TP_DATA 4.7K_0402_5% R355

+3VALW

10/1 EC Recommand

3S/4S# R385 100K_0402_5%

65W/90W# R386 100K_0402_5%

+3VALW

EC_SMB_CK1 R360 2.2K_0402_5%

EC_SMB_DA1 R359 2.2K_0402_5%

LID_SW# R396 100K_0402_5%

KSO1 R407 47K_0402_5%

KSO2 R405 47K_0402_5%

EC_PME# R398 @ 10K_0402_5%

10/1 ENE Recommand

KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7 KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16 KSO17

KSI0/GPIO30 KSI1/GPIO31 KSI2/GPIO32 KSI3/GPIO33 KSI4/GPIO34 KSI5/GPIO35 KSI6/GPIO36 KSI7/GPIO37 KSO0/GPIO20 KSO1/GPIO21 KSO2/GPIO22 KSO3/GPIO23 KSO4/GPIO24 KSO5/GPIO25 KSO6/GPIO26 KSO7/GPIO27 KSO8/GPIO28 KSO9/GPIO29 KSO10/GPIO2A KSO11/GPIO2B KSO12/GPIO2C KSO13/GPIO2D KSO14/GPIO2E KSO15/GPIO2F KSO16/GPIO48 KSO17/GPIO49

Int. K/B Matrix

PSCLK1/GPIO4A PSDAT1/GPIO4B PSCLK2/GPIO4C PSDAT2/GPIO4D TP_CLK/PSCLK3/GPIO4E TP_DATA/PSDAT3/GPIO4F

PS2 Interface

EC_MUTE# PCH_SPKR PWR_SAVE_LED# FP_LED# TP_CLK TP_DATA

EC_MUTE# <43> PCH_SPKR <13,42> PWR_SAVE_LED# <29> FP_LED# <43> TP_CLK <35> TP_DATA <35>

SDICS#/GPXOA00 SDICLK/GPXOA01 SDIDO/GPXOA02 SDIDI/GPXID0

SPI Device Interface

3S/4S# 65W/90W# ME_EN LID_SW#

3S/4S# <50> 65W/90W# <50> ME_EN <13> LID_SW# <35>

SPIDI/RD# SPIDO/WR# SPICLK/GPIO58 SPICS#

SPI Flash ROM

EC_SI_SPI_SO EC_SO_SPI_SI_R EC_SPICLK_R EC_SPICS#/FSEL#

EC_SI_SPI_SO <40>

EC_SO_SPI_SI <40> EC_SPICLK <40> EC_SPICS#/FSEL# <40>

R363 10K_0402_5%

D18 CH751H-40PT_SOD323-2

<35> RCIRRX EC_RCIRRX

Analog Board ID definition, Please see page 3.

+3VS

PCH_TEMP_ALERT# R362 2.2K_0402_5%

ENCODER_PULSE R419 10K_0402_5%

POWER_SMART# R421 10K_0402_5%

BACKUP_KEY# R422 10K_0402_5%

BKOFF# R428 10K_0402_5%

WLAN_SW# R431 10K_0402_5%

2/25 Change Bom structure of R421/R422/R431 from mount to @

RF_DISABLE# R459 10K_0402_5%

11/9 Add R459

2/25 Add R430/R442/R446

POWER_SMART# R430 10K_0402_5%

BACKUP_KEY# R442 10K_0402_5%

WLAN_SW# R446 10K_0402_5%

EC_SMB_CK1 EC_SMB_DA1 EC_SMB_CK2 EC_SMB_DA2

SCL1/GPIO44 SDA1/GPIO45 SCL2/GPIO46 SDA2/GPIO47

SM Bus

<48> EC_SMB_CK1 <48> EC_SMB_DA1 <14,23> EC_SMB_CK2 <14,23> EC_SMB_DA2

PM_SLP_S3# PM_SLP_S5# EC_SMI# PCH_TEMP_ALERT# POWER_SMART# BACKUP_KEY# SUS_PWR_ACK INVT_PWM FAN_SPEED1 BT_ON# E51TXD_P80DATA E51RXD_P80CLK ON/OFF PWR_SUSP_LED# NUM_LED#

PM_SLP_S3#/GPIO04 PM_SLP_S5#/GPIO07 EC_SMI#/GPIO08 LID_SW#/GPIO0A SUSP#/GPIO0B PBTN_OUT#/GPIO0C EC_PME#/GPIO0D EC_THERM#/GPIO11 FAN_SPEED1/FANFB1/GPIO14 FANFB2/GPIO15 EC_TX/GPIO16 EC_RX/GPIO17 ON_OFF/GPIO18 PWR_LED#/GPIO19 NUMLED#/GPIO1A

GPIO

<15> PM_SLP_S3# <15> PM_SLP_S5# <18> EC_SMI# <18> PCH_TEMP_ALERT# <29> POWER_SMART# <15> SUS_PWR_ACK <29> INVT_PWM <44> FAN_SPEED1 <43> BT_ON# <41> ON/OFF <40> PWR_SUSP_LED# <40> NUM_LED#

EC_RSMRST#/GPXO03 EC_LID_OUT#/GPXO04 EC_ON/GPXO05 EC_SWI#/GPXO06 ICH_PWROK/GPXO07 BKOFF#/GPXO08 WL_OFF#/GPXO09 GPXO10 GPXO11

GPO

EC_RSMRST# EC_LID_OUT# EC_ON EC_SWI# EC_PWROK BKOFF# WL_OFF# BACKUP_LED# WLAN_SW#

EC_RSMRST# <15> EC_LID_OUT# <14> EC_ON <41> EC_SWI# <15> EC_PWROK <15> BKOFF# <29> WL_OFF# <38> BACKUP_LED# <40>

PM_SLP_S4#/GPXID1 ENBKL/GPXID2 GPXID3 GPXID4 GPXID5 GPXID6 GPXID7

GPI

PM_SLP_S4# ENBKL EAPD ARCADE_BTN# SUSP# PBTN_OUT# EC_PME#

PM_SLP_S4# <15> ENBKL <16> EAPD <42> ARCADE_BTN# <29> SUSP# <41,45,50> PBTN_OUT# <15> EC_PME# <33>

1/14 Change value of C518/C519 from 15pF to 18pF

C518 18P_0402_50V8J C519 18P_0402_50V8J

EC_CRY1 EC_CRY2

32.768KHZ_12.5PF_Q13MC14610002 X1

OSC OSC NC NC

BATT_TEMP C493 100P_0402_50V8J

BATT_OVP C489 100P_0402_50V8J

ACIN C528 100P_0402_50V8J

SUSP# @C548 100P_0402_50V8J

EC_SMB_CK1 @C550 100P_0402_50V8J

EC_SMB_DA1 @C562 100P_0402_50V8J

ADP_I @C595 100P_0402_50V8J

ACOFF @C596 100P_0402_50V8J

IREF @C597 100P_0402_50V8J

CALIBRATE# @C598 100P_0402_50V8J

FSTCHG @C599 100P_0402_50V8J

3S/4S# @C600 100P_0402_50V8J

65W/90W# @C601 100P_0402_50V8J

SW2 WLAN_SW# NTC317-AB1G-C220C_2P

SW3 BACKUP_KEY# NTC317-AB1G-C220C_2P

4/15 Change PN of SW2/SW3 from SN100001C00 to SN100003R00

4/1 Change footprint of SW2/SW3 from SW_SKRELGE010_2P to SW_NTC317-AB1G-C220C_2P

EC_CRY1 EC_CRY2

XCLK1 XCLK0

V18R

C523 4.7U_0603_6.3V6K

12/8 Add C548/C550/C562/C595~C601=@ 100pF(Avoid switching noise)

GND GND GND GND GND

AGND

KB926QFE0_LQFP128_14X14

20mil

L35 ECAGND BLM18AG121SN1D_0603

9/14 Change description and value of L35.

+3VALW

U28 NC7SZ08P5X_NL_SC70-5

<15,23> ACIN_BUF ACIN

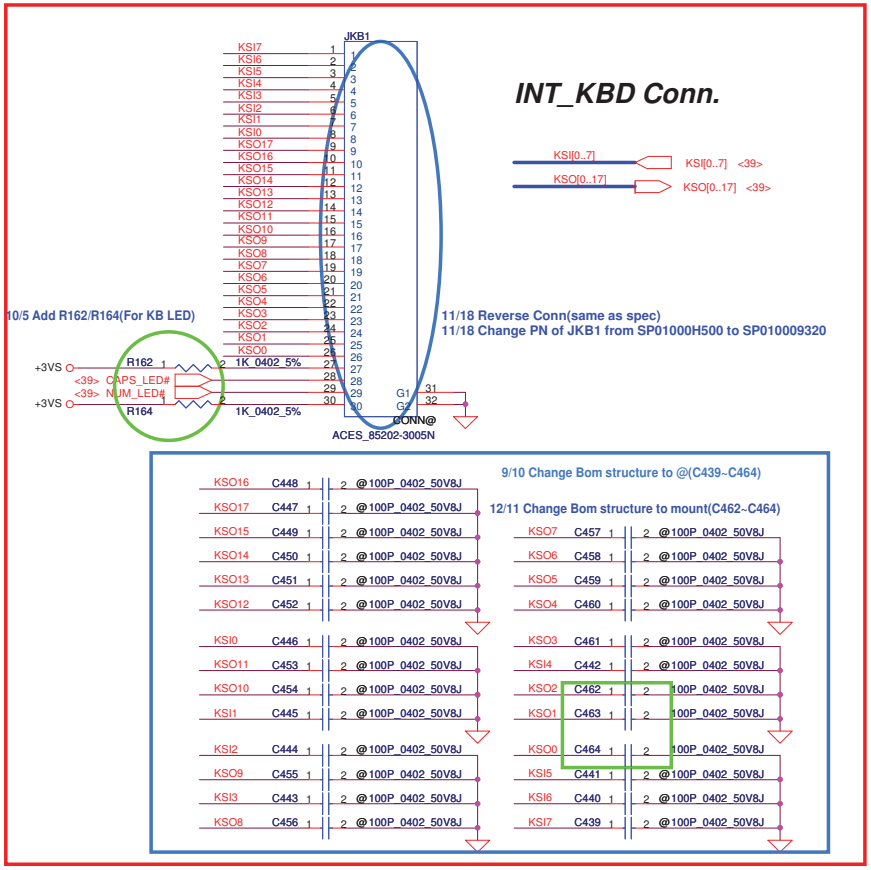
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

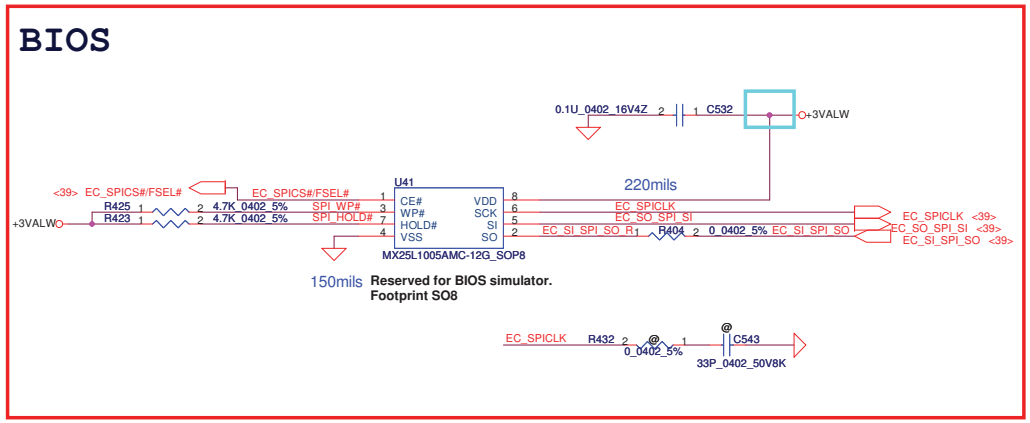
Compal Electronics, Inc.

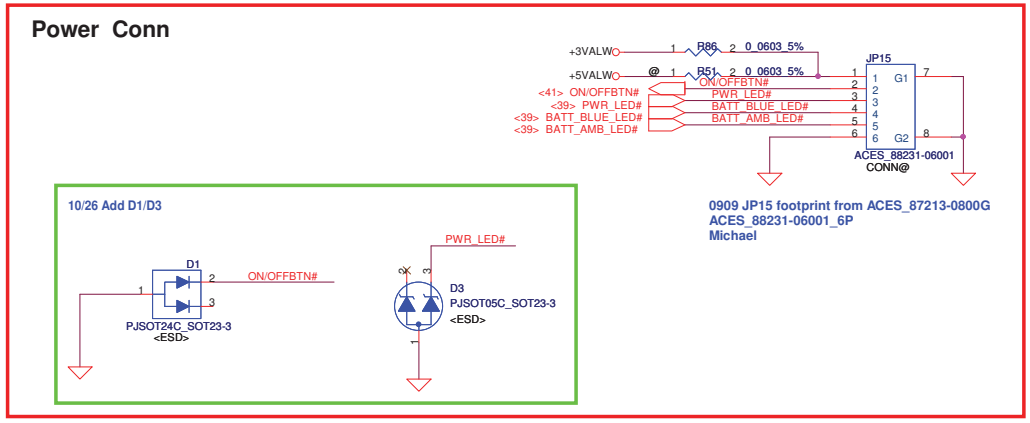
Title: EC ENE KB926

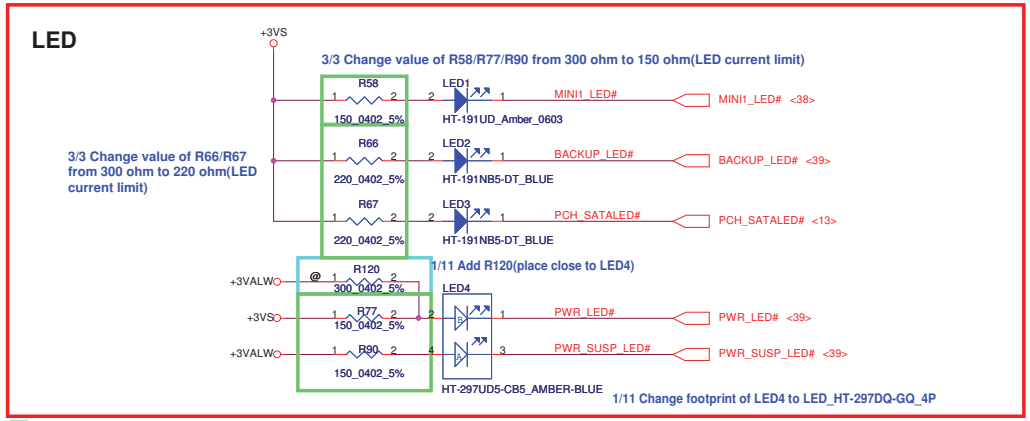
Size	Document Number	Rev
B	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 Sheet 39 of 63



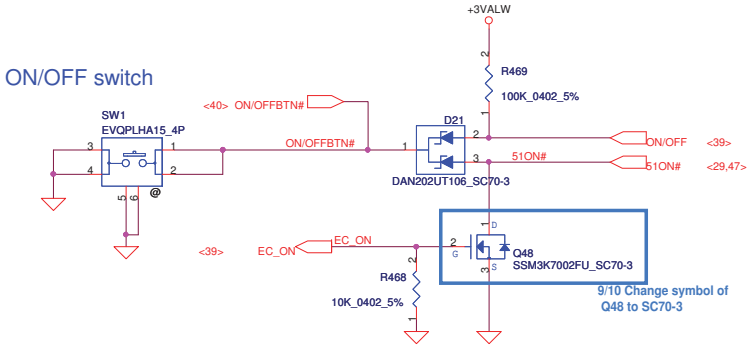


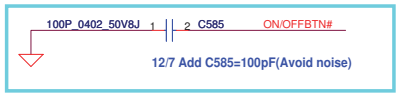




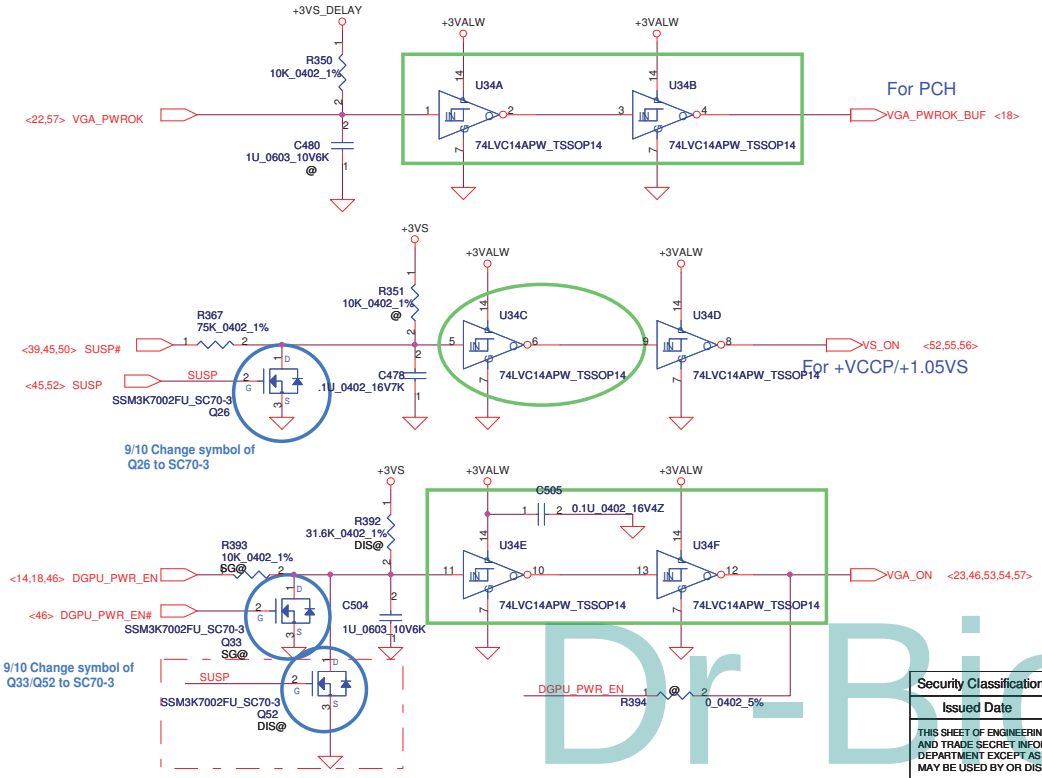
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date	2010/08/25
Title	BIOS, I/O Port & K/B Connector		
Size B	Document Number NCQF0 M/B LA-5981P Schematic		Rev 1.0
Date: Sunday, April 18, 2010		Sheet 40 of 63	

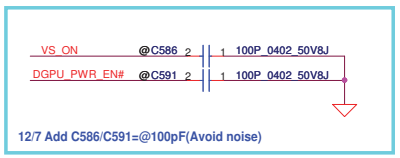
Power Button





Power ON Circuit





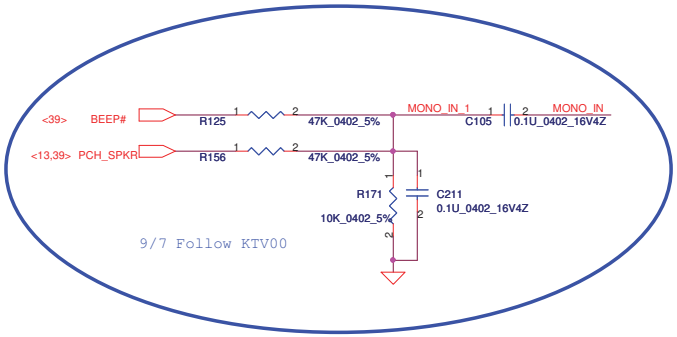
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

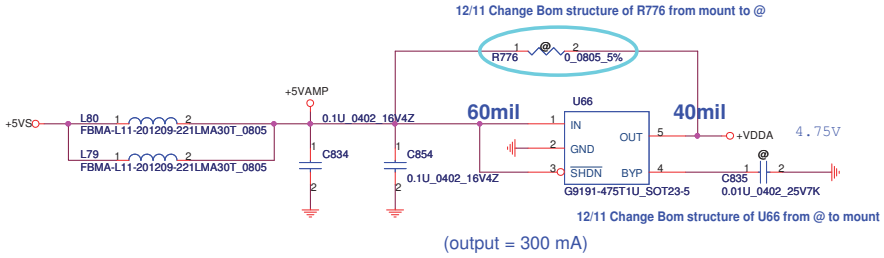
Compal Electronics, Inc.

Title: Power OK/PBN/TP Lock/LED

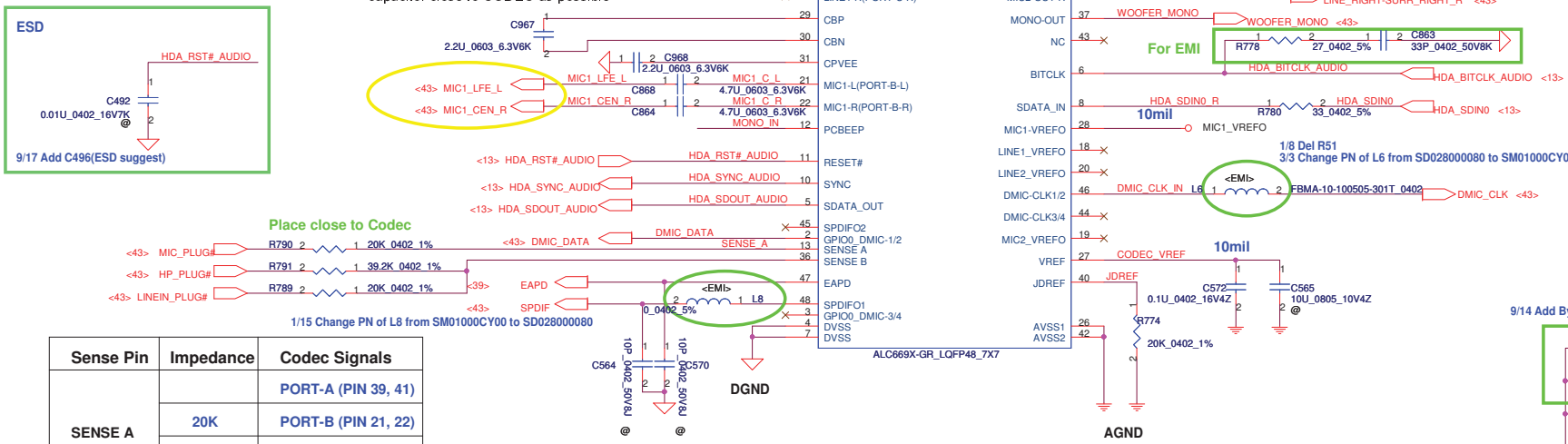
Size: B | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 1.0

Date: Sunday, April 18, 2010 | Sheet 41 of 63





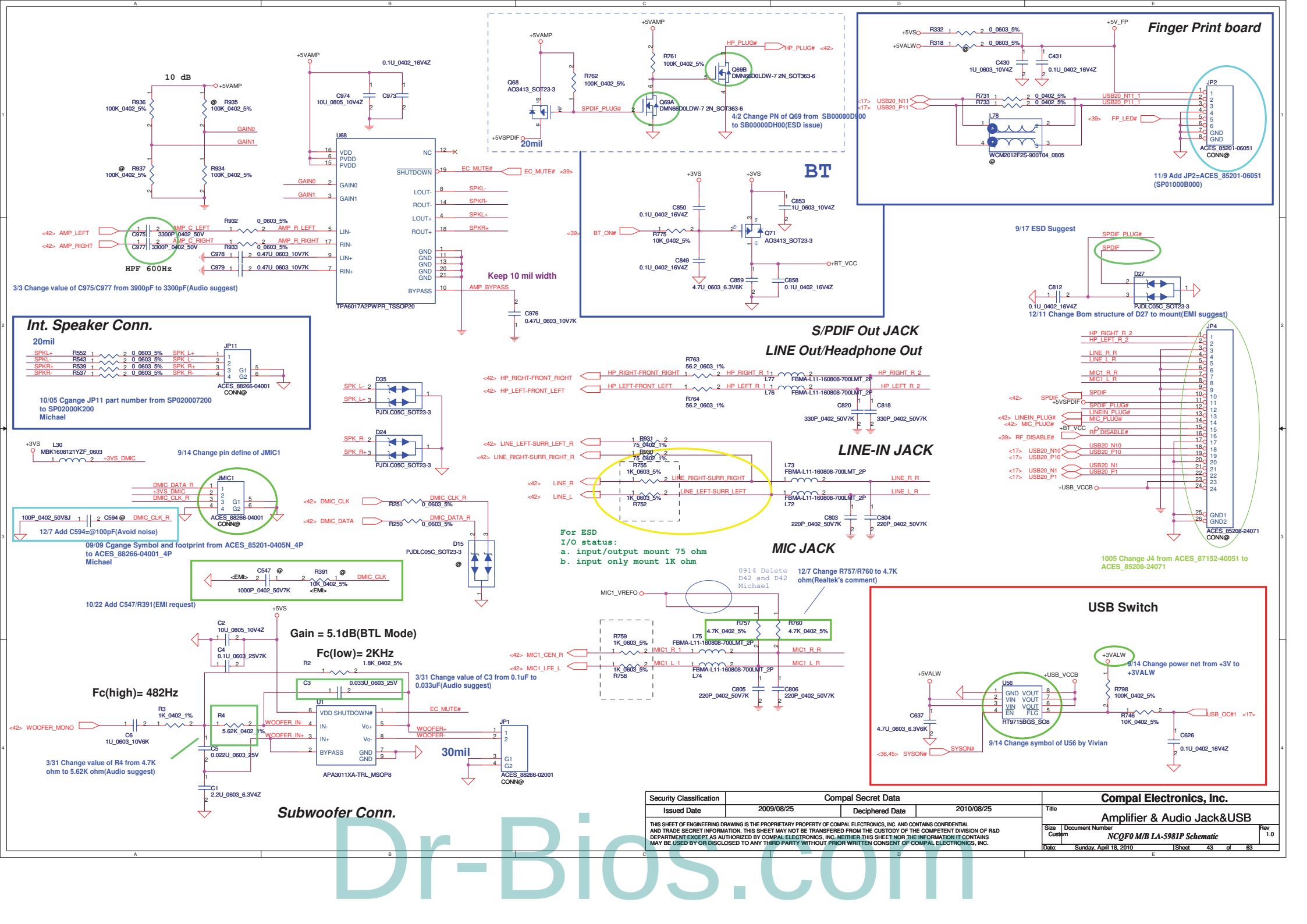
HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A		PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
		PORT-C (PIN 23, 24)
SENSE B	39.2K	PORT-E (PIN 32, 34)
	20K	PORT-F (PIN 33, 35)
		PORT-H (PIN 37)

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	HD Audio Codec ALC669X		
Size B	Document Number NCQF0 M/B LA-5981P Schematic		Rev 1.0
Date: Sunday, April 18, 2010		Sheet 42 of 63	



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

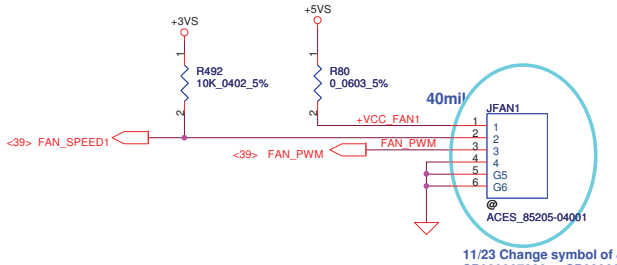
Compal Electronics, Inc.

Title: Amplifier & Audio Jack&USB

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 | Sheet 43 of 63

FAN1 Conn



11/23 Change symbol of JFAN1 from SP020007200 to SP020008X00

Screw

H1 H_3P0 @
H2 H_3P0 @
H3 H_3P0 @
H4 H_3P0 @
H5 H_3P0 @
H6 H_3P0 @
H7 H_3P0 @
H8 H_3P0 @
H9 H_3P0 @
H10 H_3P0 @
H11 H_3P2 @
H12 H_3P2 @
H19 H_3P2 @
H15 H_3P8 @
H16 H_3P8 @
H17 H_3P8 @
H18 H_3P8 @
H13 H_3P8 @
H14 H_3P8 @
H23 H_2P3X0P6 @
H24 H_2P3X0P6 @

NON-PDH

2/25 Change footprint of H22

H21 H_5P0X3P0N @
H20 H_6P0X3P0N @
H22 H_2P8N @

FD3 @ FIDUCIAL_C40M80
FD1 @ FIDUCIAL_C40M80
FD4 @ FIDUCIAL_C40M80
FD2 @ FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	FAN & Screw Hole		
Size B	Document Number NCQF0 M/B LA-5981P Schematic		Rev 1.0
Date: Sunday, April 18, 2010	Sheet 44 of 63		

+5VALW TO +5VS

For EMI Require 1/21
Put near Right side of DIMM

+5VALW
+5VS
U44
SI4800BDY-T1-E3_SO8
C555 1U_0603_10V4Z
R443 470_0603_5%
0.1U_0402_16V4Z
C556
9/1 Del C574/C562/567
+VSB
R444 200K_0402_5%
5VS_GATE
DMN66D0LDW-7 2N_SOT363-6
Q42B
SUSP
C561 0.1U_0603_25V7K
Q42A
DMN66D0LDW-7 2N_SOT363-6
4/2 Change PN of Q42 from SB00000D900 to SB00000DH00(ESD issue)

+3VALW TO +3VS

+3VALW
+3VS
U42
SI4800BDY-T1-E3_SO8
C549 1U_0603_10V4Z
R440 470_0603_5%
9/1 Del C547/C548/C545
+VSB
R447 200K_0402_5%
3VS_GATE
DMN66D0LDW-7 2N_SOT363-6
Q43B
SUSP
C560 0.1U_0603_25V7K
Q43A
DMN66D0LDW-7 2N_SOT363-6
12/7 Add C579
C579 100P_0402_50V8J @
4/2 Change PN of Q43 from SB00000D900 to SB00000DH00(ESD issue)

+1.5V to +1.5VS

Optional, if +1.5VS can combine with +1.5V_1

+1.5V
+1.5VS
U43
SI4800BDY-T1-E3_SO8
J3
JUMP_43X118@
+1.5V_1
C557 1U_0603_10V4Z
R441 470_0603_5%
9/1 Del C550/C558/C559
+VSB
R436 510K_0402_5%
1.5VS_GATE
DMN66D0LDW-7 2N_SOT363-6
Q41B
SUSP
C546 0.1U_0603_25V7K
R435 @ 510K_0402_5%
Q41A
DMN66D0LDW-7 2N_SOT363-6
4/2 Change PN of Q41 from SB00000D900 to SB00000DH00(ESD issue)
<39,47> ACIN
@ SSM3K7002FU_SC70-3 Q39
9/10 Change symbol of Q39 to SC70-3

11/26 Change R448 from 470 ohm to 22 ohm

+0.75VS
+1.05VS
+1.1VS_VTT
+1.8VS
+1.5V
R448 22_0603_5%
R661 470_0603_5% @
R729 470_0603_5% @
R424 470_0603_5% @
R437 470_0603_5% @
SSM3K7002FU_SC70-3 Q44
SSM3K7002FU_SC70-3 Q64 @
SSM3K7002FU_SC70-3 Q66 @
SSM3K7002FU_SC70-3 Q37 @
SSM3K7002FU_SC70-3 Q38 @
SUSP
SYSON#
9/10 Change symbol of Q37/Q38/Q44/Q64/Q66 to SC70-3
11/13 Change Bom structure of R424/R448/R661/R729/Q37/Q44/Q64/Q66 from mount to @

10/9 Delete R428, R431 and Q36
(Remove SBPWR_EN# Function)

+5VALW
R439 100K_0402_5%
<36,43> SYSON#
SYSON#
<39,55> SYSON
SYSON
R434 100K_0402_5%
Q40A DMN66D0LDW-7 2N_SOT363-6
4/2 Change PN of Q40 from SB00000D900 to SB00000DH00(ESD issue)

+5VALW
R433 100K_0402_5%
<41,52> SUSP
SUSP
<39,41,50> SUSP#
Q40B DMN66D0LDW-7 2N_SOT363-6
R438 10K_0402_5%
4/2 Change PN of Q40 from SB00000D900 to SB00000DH00(ESD issue)

For Calpella CPU S3 DRAM Power

(1.5V_CPU VDDQ)

+1.5V
+1.5V_1
C969 0.1U_0402_16V4Z
C970 0.1U_0402_16V4Z
C971 0.1U_0402_16V4Z
C972 0.1U_0402_16V4Z
U48
SI4856ADY_SO8
250mil(6A)
C592 0.1U_0402_16V4Z
R495 470_0603_5%
12/7 Add R325=20K ohm(For Capella S3 resume become shutdown issue
R496 100K_0402_1%
1.5V_1_GATE
R325 20K_0402_5%
+VSB
SUSP
SSM3K7002FU_SC70-3 Q79
C593 0.1U_0603_25V7K
9/10 Change symbol of Q79 to SC70-3
SSM3K7002FU_SC70-3 Q55
9/10 Change symbol of Q55 to SC70-3

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

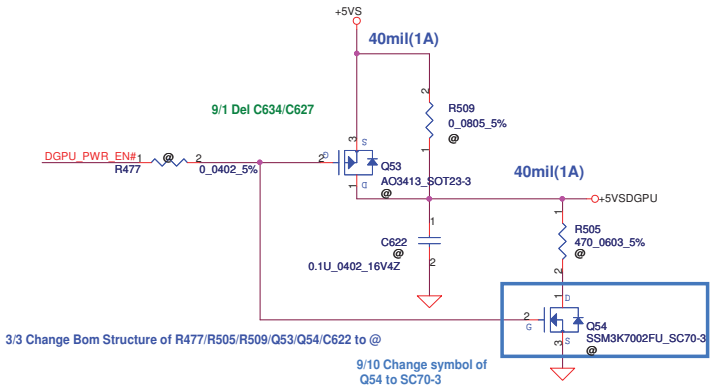
Compal Electronics, Inc.

Title: DC Interface

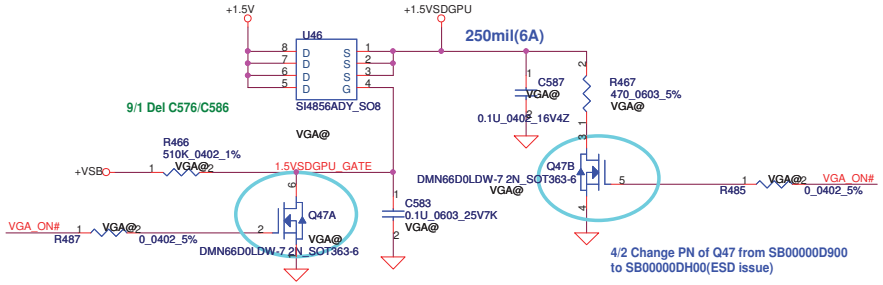
Size	Document Number	Rev
B	NCQF0 M/B LA-5981P Schematic	1.0

Date: Sunday, April 18, 2010 Sheet 45 of 63

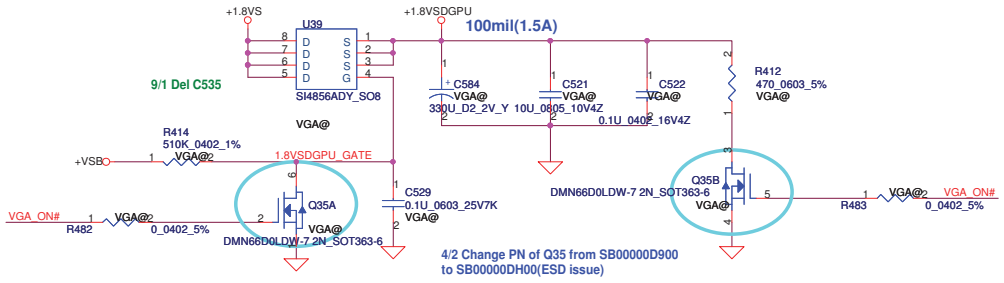
+5VS to +5VSDGPU

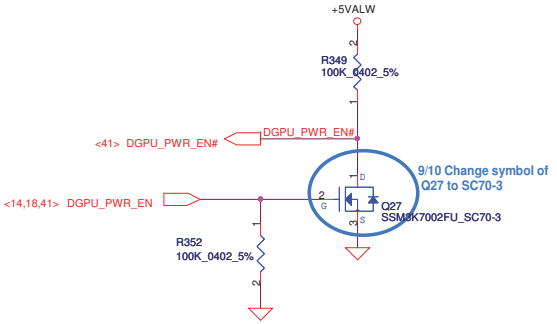


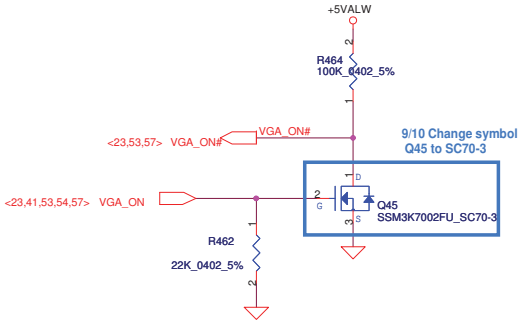
+1.5V to +1.5VSDGPU Transfer



+1.8VS to +1.8VSDGPU Transfer



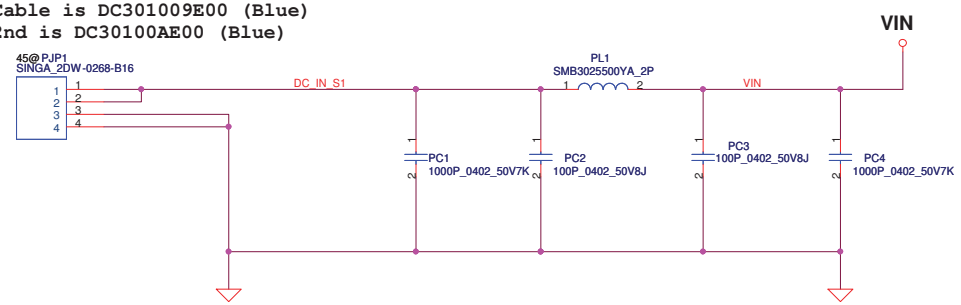


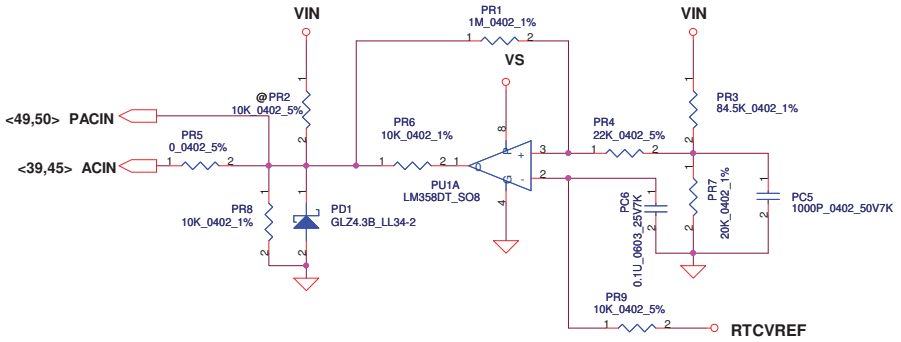


Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	VGA DC Interface		
Size B	Document Number NCQF0 M/B LA-5981P Schematic		Rev 1.0
Date: Sunday, April 18, 2010	Sheet 46 of 63		

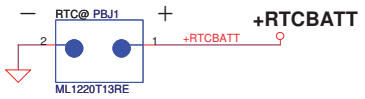
On board conn is DC301001Y00
Cable is DC301009E00 (Blue)
2nd is DC30100AE00 (Blue)

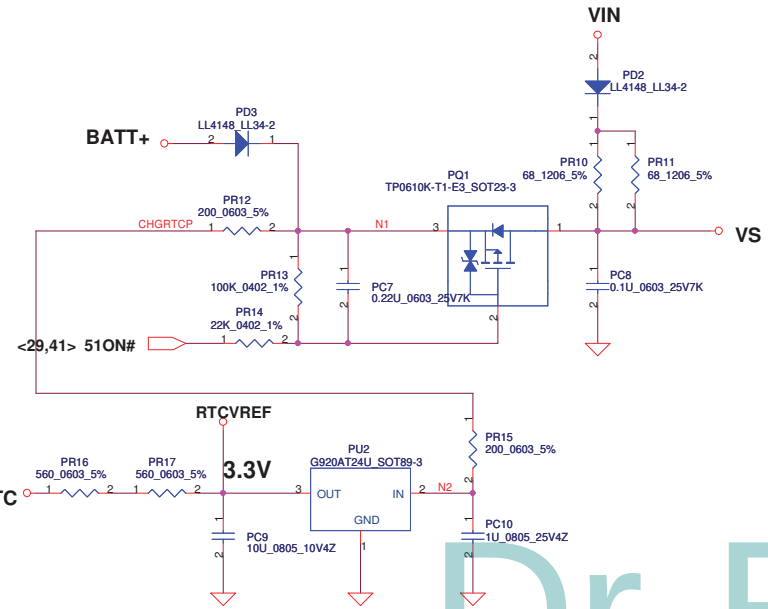


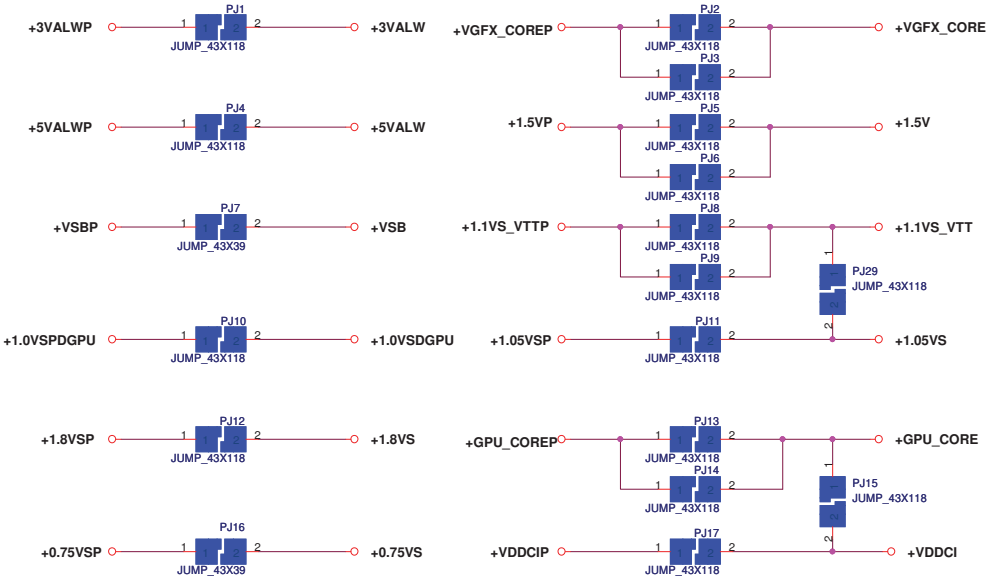


Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V







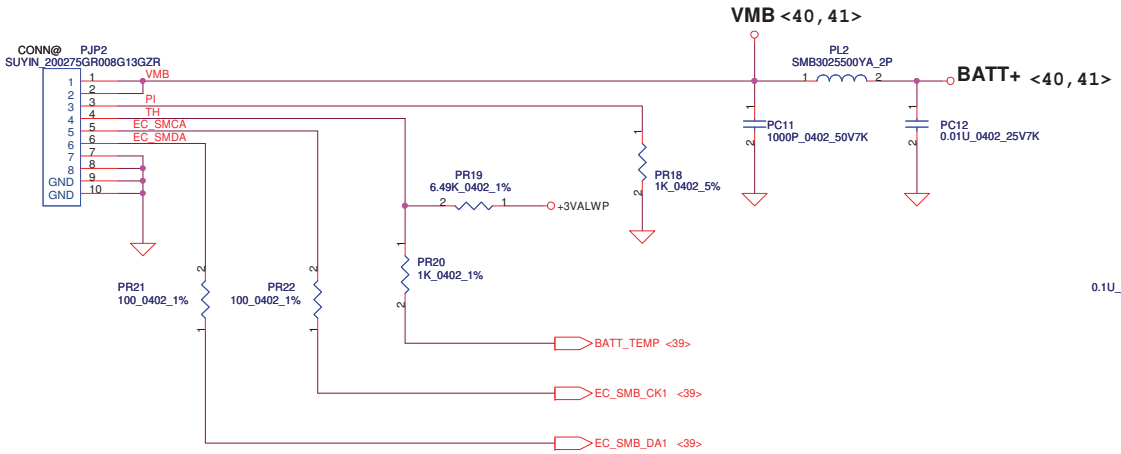
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 | Sheet 47 of 62



Reference only!! Not SPEC

PH1 under CPU botten side :

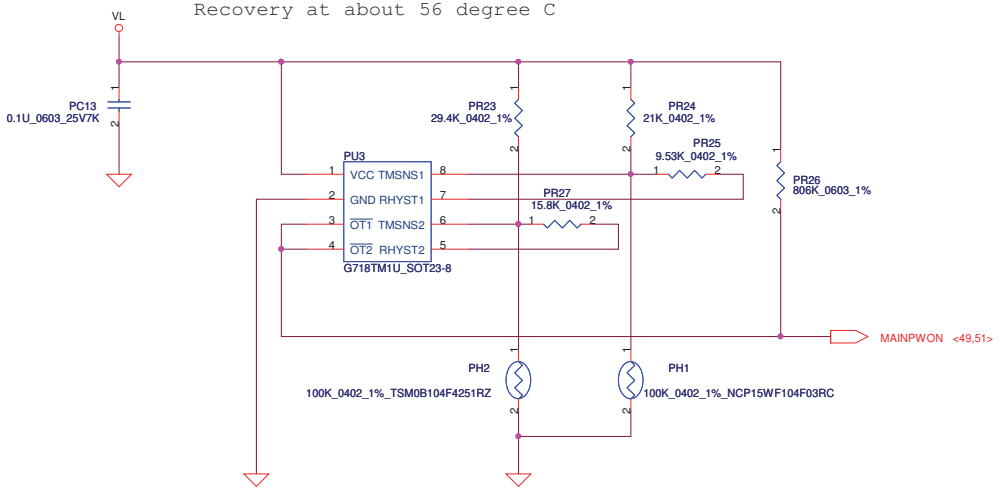
CPU thermal protection at about 92 degree C

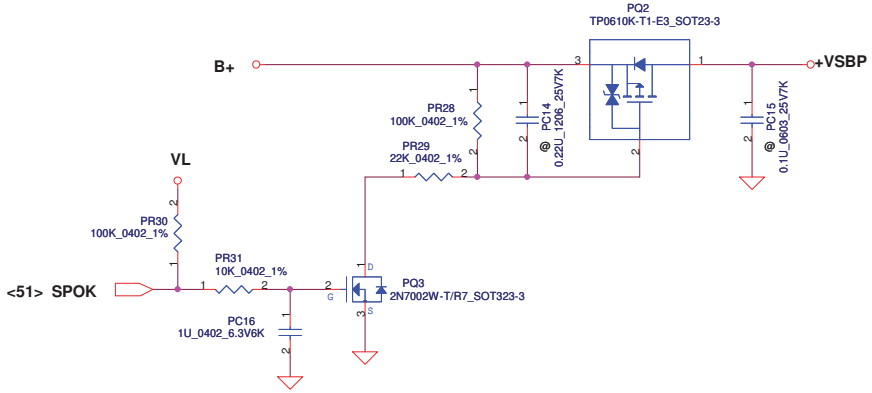
Recovery at about 56 degree C

PH2 under FAN down side :

CPU thermal protection at about 82 degree C

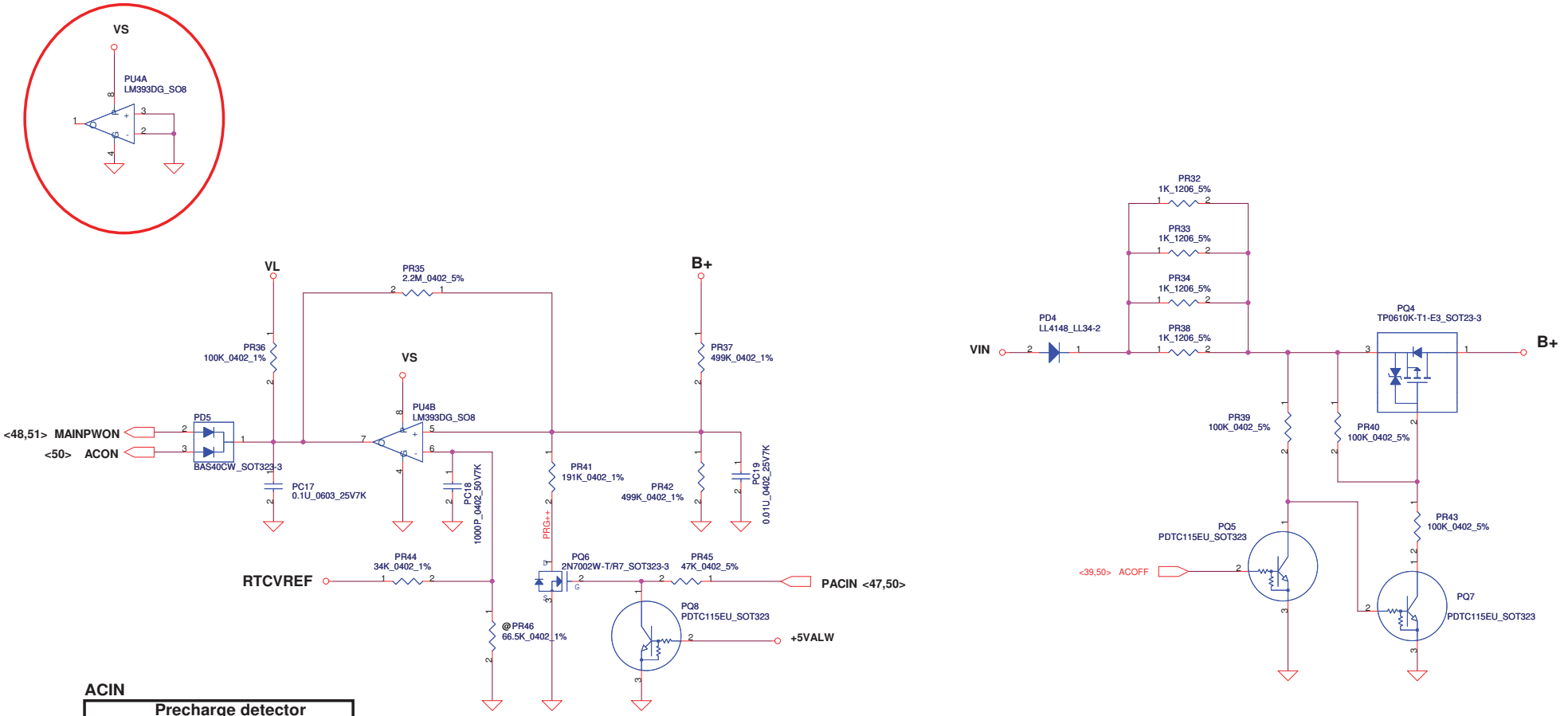
Recovery at about 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	BATTERY CONN / OTP		
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 0.1
Date: Sunday, April 18, 2010		Sheet 48 of 62	



ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **PRECHARGE**

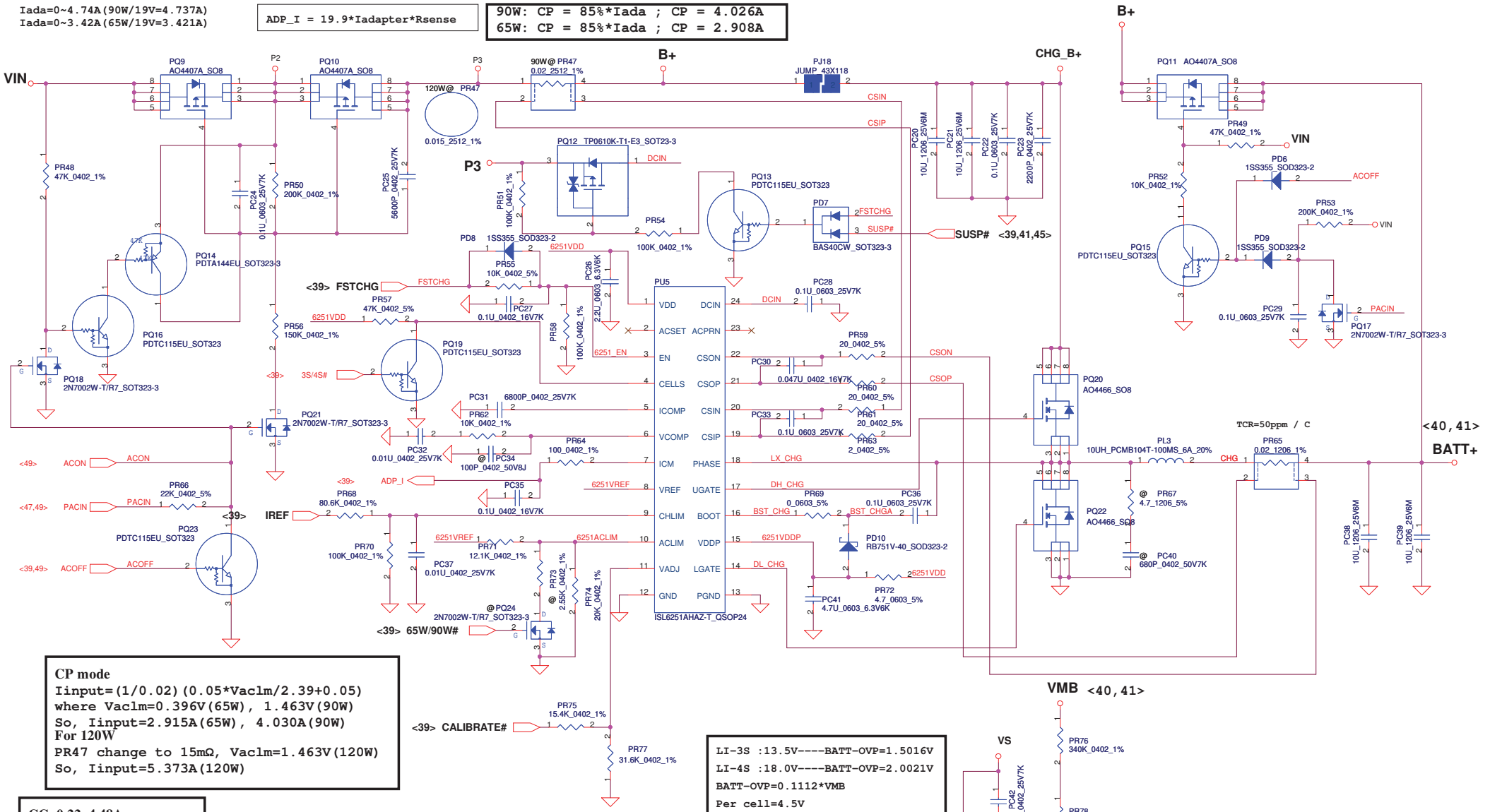
Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 | Sheet 49 of 62

Iada=0~4.74A(90W/19V=4.737A)
Iada=0~3.42A(65W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

90W: CP = 85%*Iada ; CP = 4.026A
65W: CP = 85%*Iada ; CP = 2.908A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=0.396V(65W), 1.463V(90W)
So, Iinput=2.915A(65W), 4.030A(90W)
For 120W
PR47 change to 15mΩ, Vaclm=1.463V(120W)
So, Iinput=5.373A(120W)

CC=0.22~4.48A
Iref=0.7297*Ichanrge
=>Ki=0.7297
IREF=0.159V~3.269V

LI-3S :13.5V----BATT-OVP=1.5016V
LI-4S :18.0V----BATT-OVP=2.0021V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

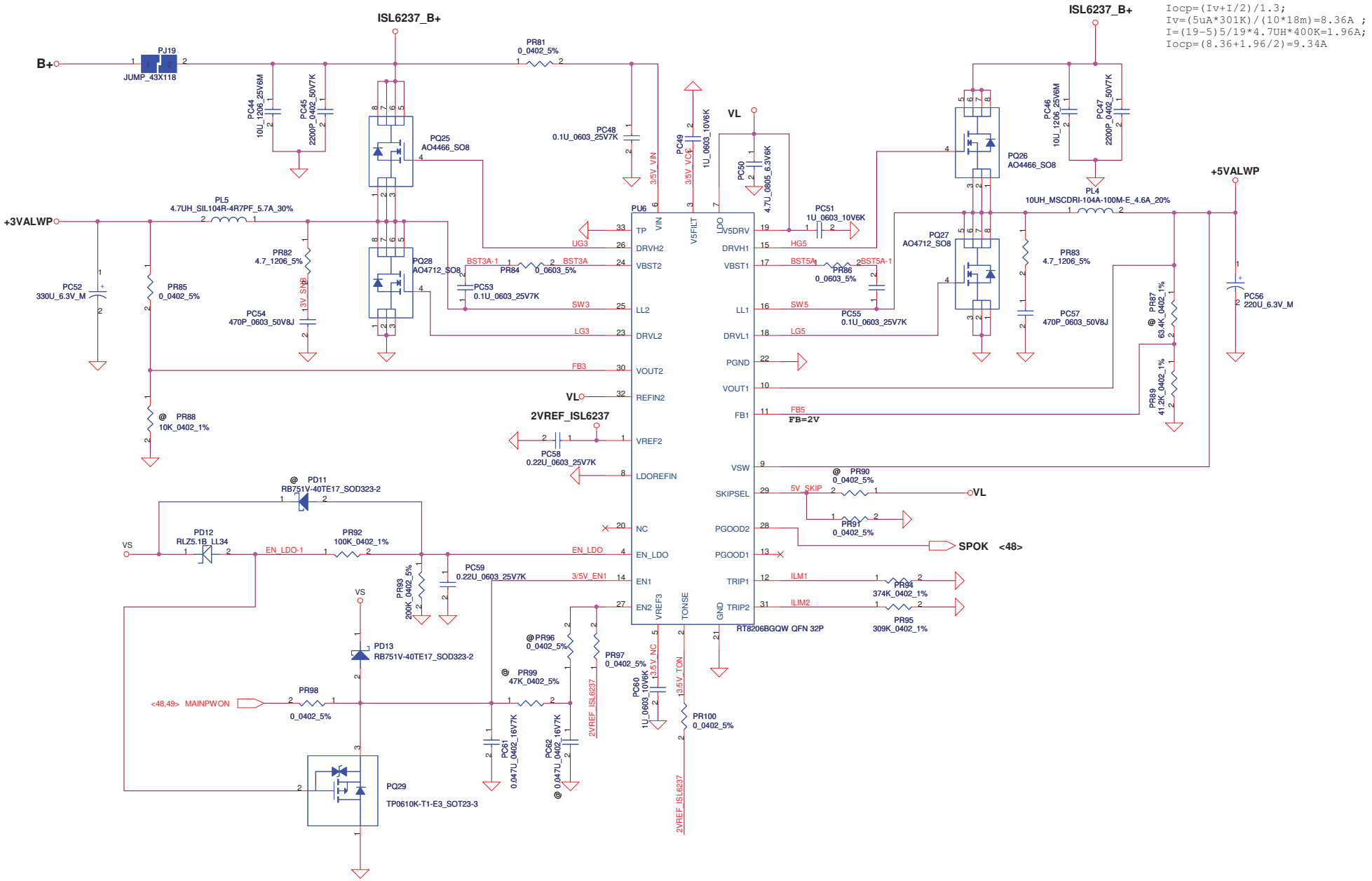
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: CHARGER

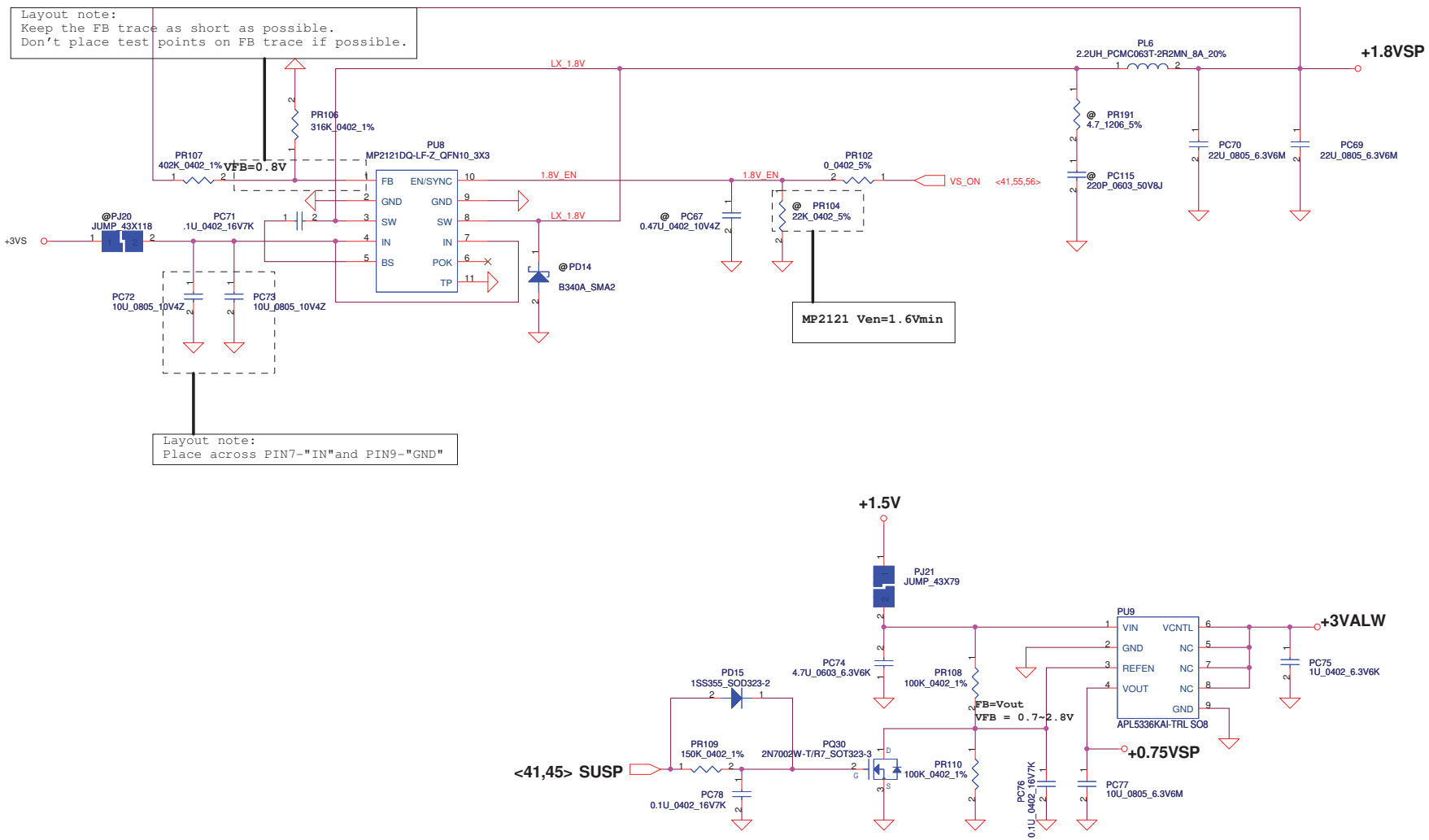
Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 0.1

Date: Sunday, April 18, 2010 | Sheet 50 of 62



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.		
Title	3VALW/5VALW	
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic	Rev: 0.1
Date: Sunday, April 18, 2010	Sheet 51 of 62	



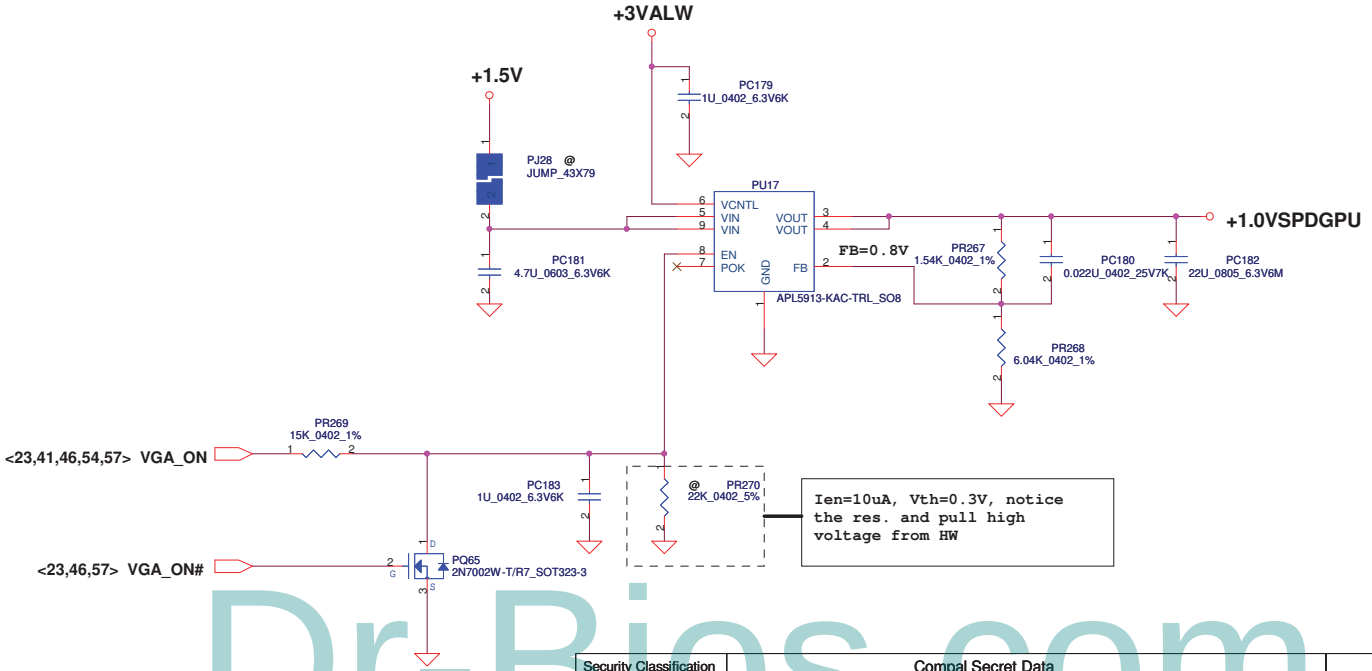
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **+1.8VSP/+0.75VSP**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 | Sheet 52 of 62



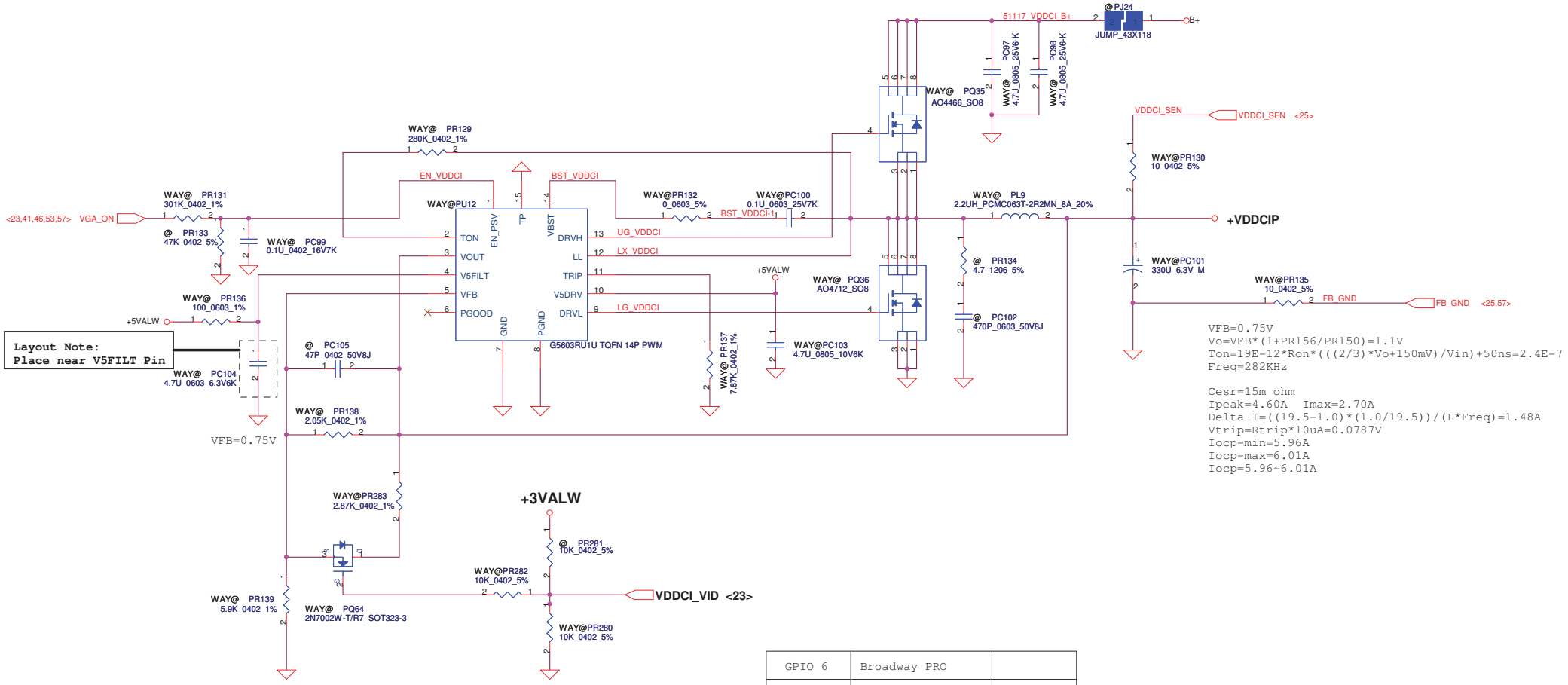
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **+1.0VSDGPU**

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 | Sheet 53 of 62



VFB=0.75V
Vo=VFB*(1+PR156/PR150)=1.1V
Ton=19E-12*Ron*(((2/3)*Vo+150mV)/Vin)+50ns=2.4E-7
Freq=282KHz

Cesr=15m ohm
Ipeak=4.60A Imax=2.70A
Delta I=((19.5-1.0)*(1.0/19.5))/(L*Freq)=1.48A
Vtrip=Rtrip*10uA=0.0787V
Iocp-min=5.96A
Iocp-max=6.01A
Iocp=5.96~6.01A

GPIO 6	Broadway PRO	
VDDCI_VID	VDDCI Voltage Level	Comment
0	1.00 V	Default
1	0.90 V	

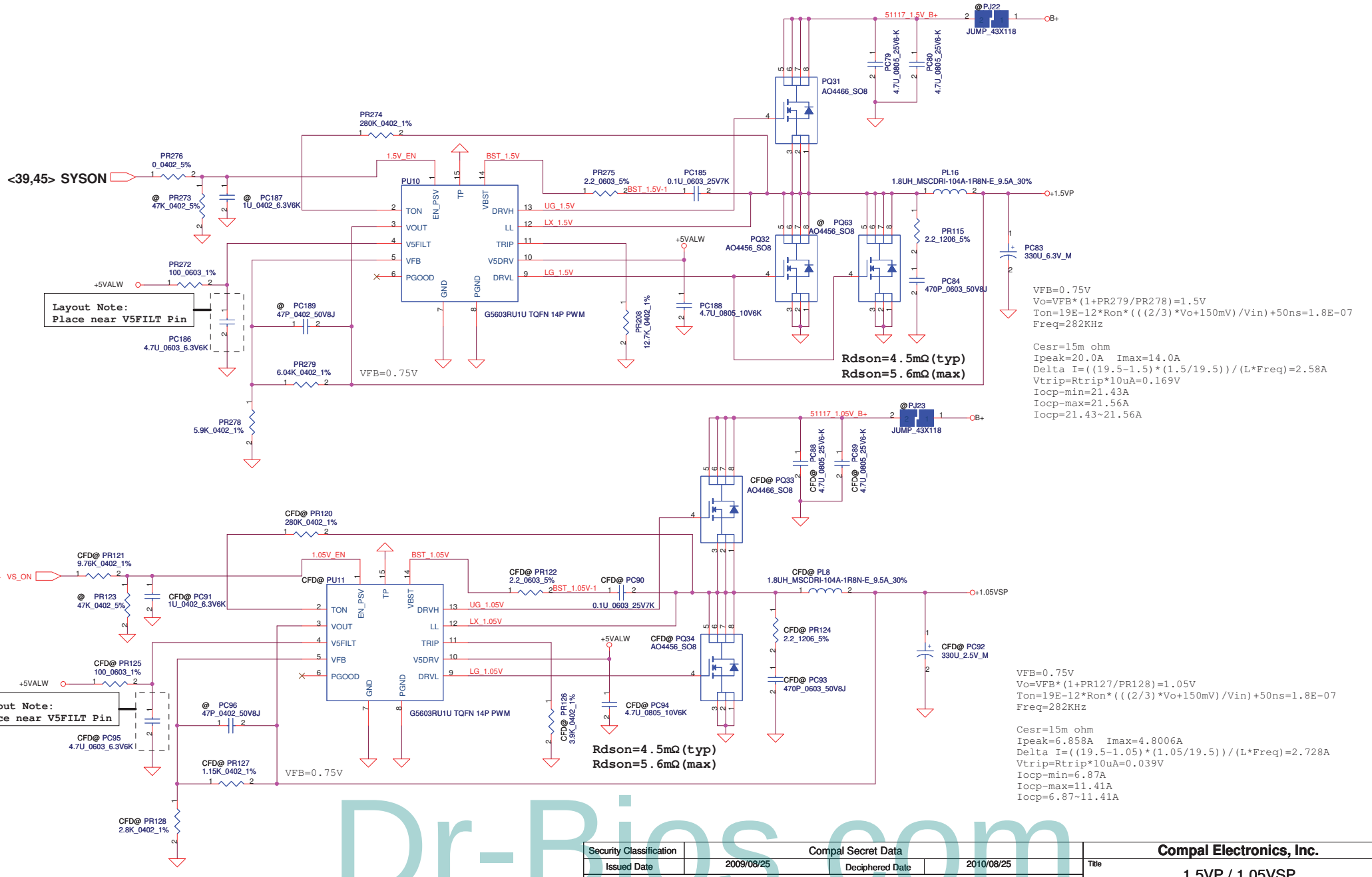
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: VDDCIP

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 | Sheet 54 of 62



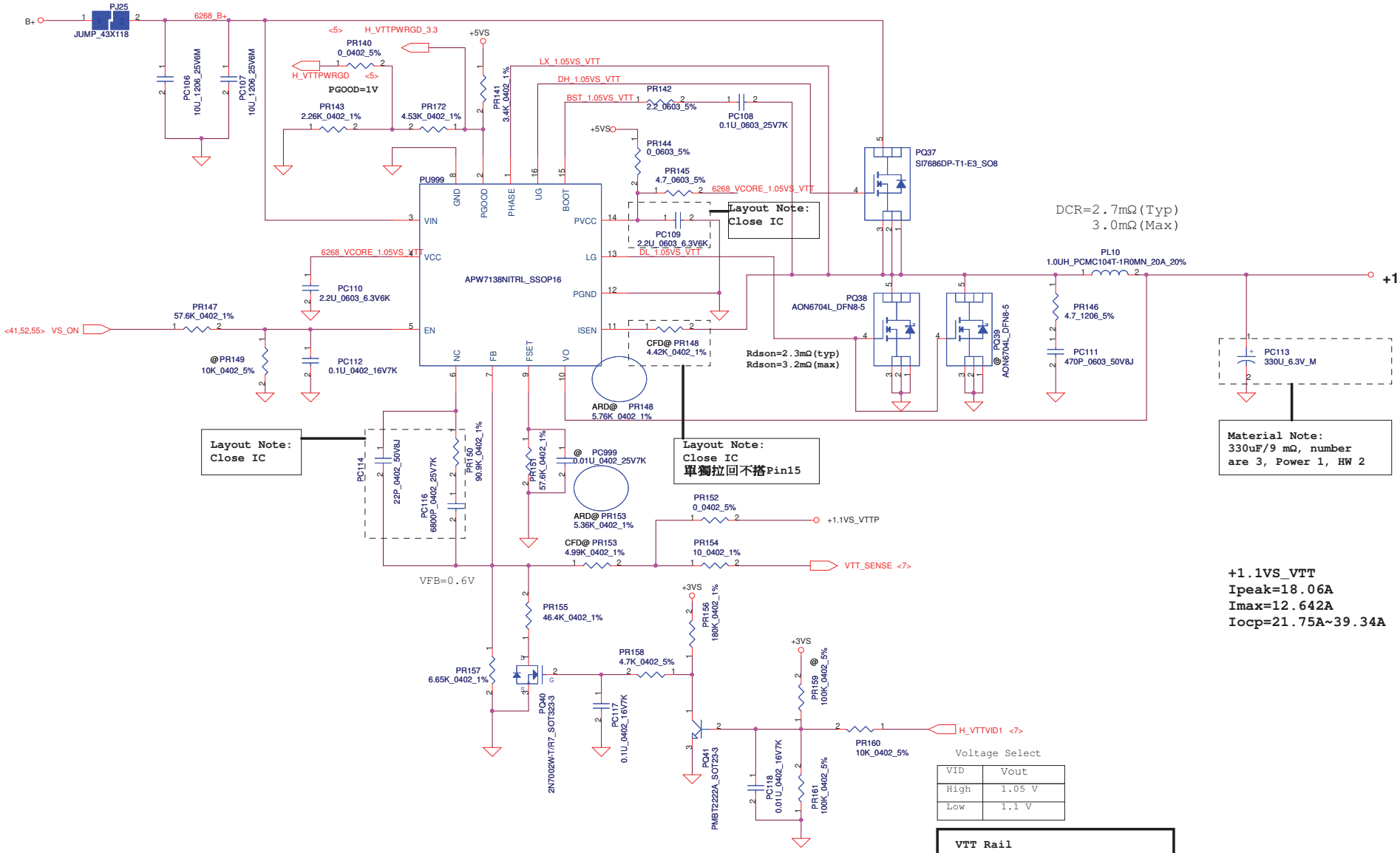
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: 1.5VP / 1.05VSP

Size	Document Number	Rev
Custom	NCQF0 M/B LA-5981P Schematic	0.1

Date: Sunday, April 18, 2010 | Sheet 55 of 62



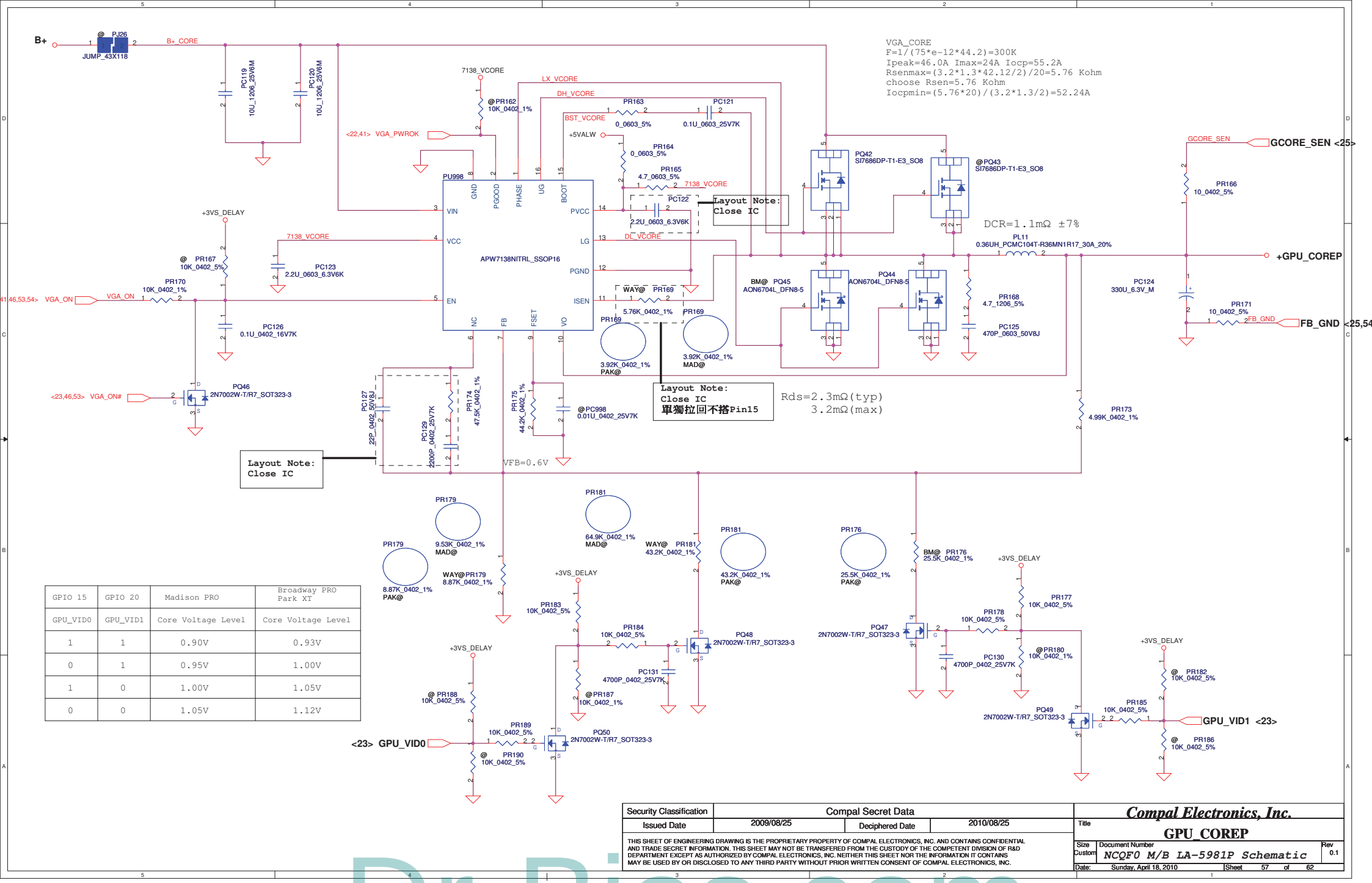
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: +1.1VS_VTTP

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 0.1

Date: Sunday, April 18, 2010 | Sheet 56 of 62



VGA_CORE
F=1/(75*e-12*44.2)=300K
Ipeak=46.0A Imax=24A Iocp=55.2A
Rsenmax=(3.2*1.3*42.12/2)/20=5.76 Kohm
choose Rsen=5.76 Kohm
Iocpmin=(5.76*20)/(3.2*1.3/2)=52.24A

GPIO 15	GPIO 20	Madison PRO	Broadway PRO Park XT
GPU_VID0	GPU_VID1	Core Voltage Level	Core Voltage Level
1	1	0.90V	0.93V
0	1	0.95V	1.00V
1	0	1.00V	1.05V
0	0	1.05V	1.12V

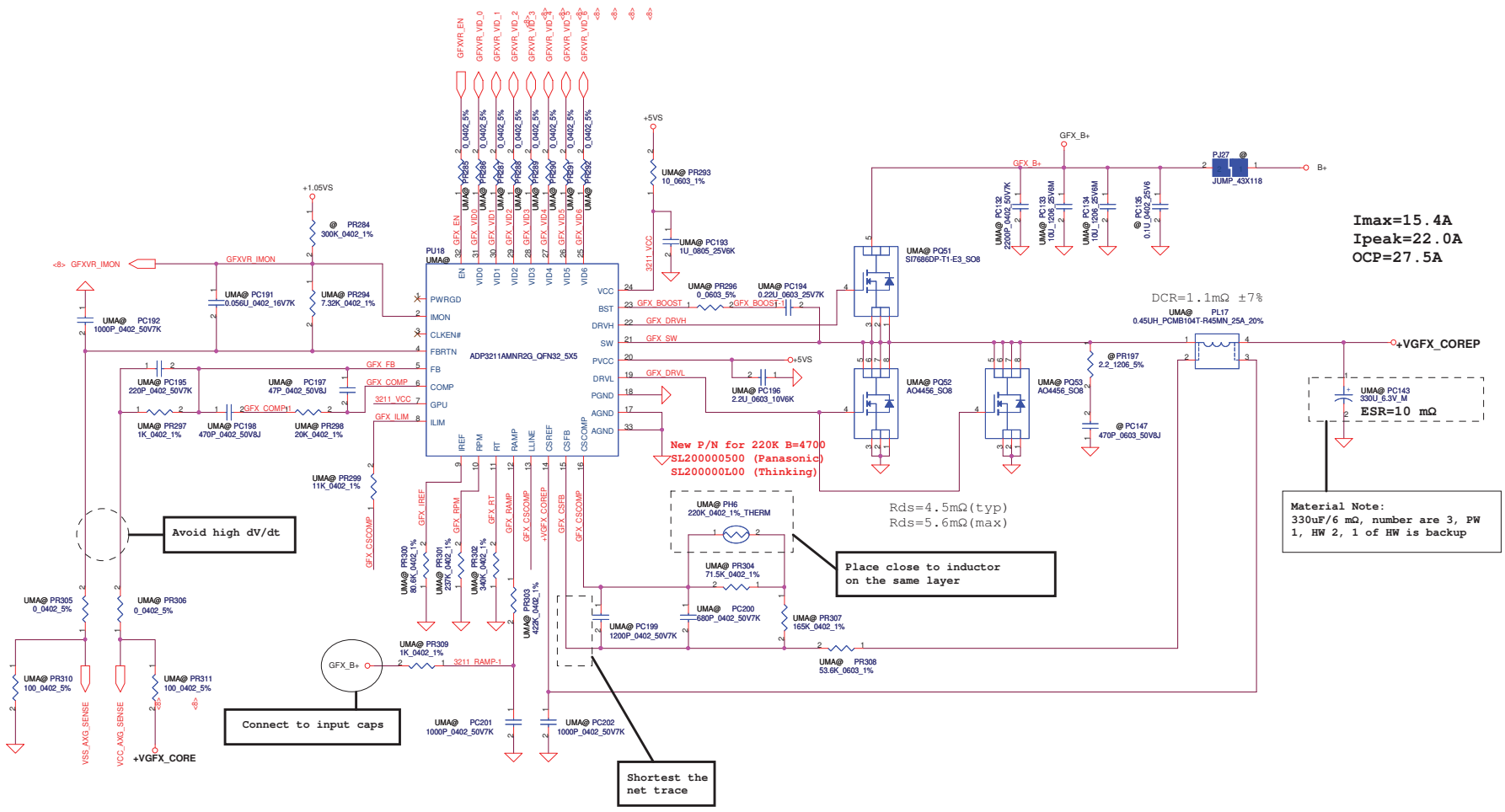
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: GPU_COREP

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 0.1

Date: Sunday, April 18, 2010 | Sheet 57 of 62



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.			
Title	+GFX_COREP		
Size C	Document Number NCQF0 M/B LA-5981P Schematic		Rev 0.1
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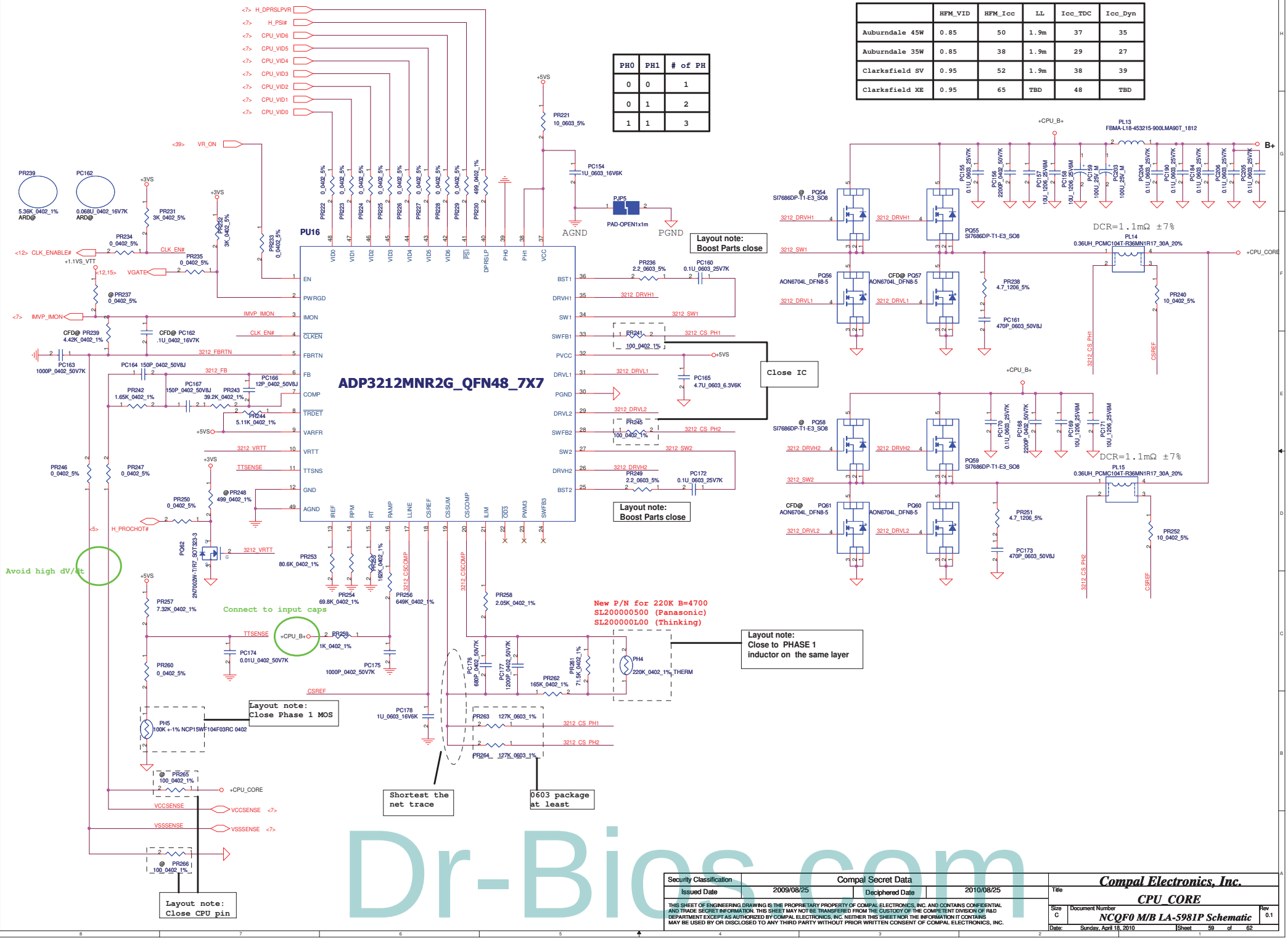
	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	0.85	50	1.9m	37	35
Auburndale 35W	0.85	38	1.9m	29	27
Clarksfield SV	0.95	52	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

PH0	PH1	# of PH
0	0	1
0	1	2
1	1	3



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: CPU_CORE			
Size: C	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 0.1
Date: Sunday, April 18, 2010		Sheet 59 of 62	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify chager circuit	Design change	0.1	48	Change BQ24751 to ISL6251	2009 10/07	EVT
2	During shutdown, GFX has a pulse	Make GFX_EN pull down quickly	0.1	58	~~Add PD15 to connect GFX_EN and VS_ON~~	~~2009~~ 11/02	EVT
3	Park XT SPEC change	More display performance	0.1	57	Change PR176 from 31.6KΩ to 43.2KΩ(SD034432280) Change PR179 from 9.53KΩ to 8.87KΩ(SD034887180) Change PR181 from 64.9KΩ to 25.5KΩ(SD034255280)	2009 11/05	EVT
4	ME height not enough	Prevent EL-cap. to knock the door	0.1	51	Change PC56 from 330uF 6L to 220uF 4.5L(SF000002Y00)	2009 11/11	EVT
5	Cost review	Cost down	0.1	57	Change PC124 from 6mΩ to 10mΩ(SF000002O00)	2009 11/11	EVT
6		Tune OCP	0.1	58	Change PR294 from 6.98KΩ to 7.15KΩ(SD034715180) Change PR299 from 10.7KΩ to 11KΩ(SD034110280)	2009 11/11	EVT
7		Tune OCP & Imon	0.1	59	Change PR239 from 499KΩ to 4.53KΩ(SD034453180) Change PC162 from 0.082uF to 0.1uF(SE076104KM8) Change PR258 from 1.91KΩ to 2.05KΩ(SD034205180) ~~Change PR261 from 73.2KΩ to 71.5KΩ(SD034715280)~~ Change PR263, PR264 from 120KΩ to 127KΩ(SD014127380) Change PR258 from 1.91KΩ to 2.05KΩ(SD034205180)	2009 11/11	EVT
8							
9	Not enough space	Not enough space	0.1	52	Change PL6 from 10x10 to 7x7(SH000006I80)	2009 11/12	EVT
10	HW Jason request	Add new VGA voltage table	0.1	57	Add PR176,PR179,PR181 virtual parts	2009 11/19	EVT
11	Design review	1.5V change APW7138 to TPS51117	0.1	55		2009 11/19	EVT
12	Design review	Provide GFX output a reference	0.1	58	Add PR310,PR311	2009 12/03	EVT
13	S3 resume shutdown	Make sure 0.75V high later than 1.5V and low earlier than 1.5V	0.1	52	Add PD15	2009 12/08	EVT
14	Design review	1.5V tune output voltage	0.2	55	Change PR278 from 59KΩ to 124KΩ(SD034124380) Change PR279 from 24KΩ to 124KΩ(SD034124380) Change PR208 from 9.09KΩ to 16.9KΩ(SD034169280)	2009 12/15	DVT
15	Power OFF sequence	+1.0vsdgpu need power down within 20ms	0.2	53	Add PQ65	2010 01/05	DVT
16	HW request raise 1% voltage	1.5V tune output voltage	0.2	55	Change PR279 from 124KΩ to 127KΩ(SD034127380)	2010 01/07	DVT
17	OTP activity	Have a pull high	0.2	48	Enable PR23	2010 01/07	DVT
18	EMI solution	Add bypass cap from B+ to Gnd	0.2	59	Add PC184,PC190,PC204,PC205,PC206	2010 01/08	DVT
19	GFX character	Improve Imon, Loadline	0.2	58	Change PR294 from 7.15KΩ to 7.32KΩ(SD034732180) Change PR308 from 43.2KΩ to 53.6KΩ(SD034536380)	2010 01/08	DVT
20	CPU character	Improve Imon, Loadline, Transient	0.2	59	Change PR239 from 4.53KΩ to 4.42KΩ(SD000004J80) Change PC176 from 390pF to 680pF(SE074681K80)	2010 01/08	DVT
21	Costdown	Change pack from 1206 to 0805	0.2		Change PC79,PC80,PC88,PC89,PC97,PC98 from 1206 to 0805(SE000006R80)	2010 01/08	DVT
22	Tune sequence	GPU_core need ramp up before VDDCIP	0.2	54	Change PR131 from 10KΩ to 57.6KΩ(SD034576280)	2010 01/08	DVT
23	Run 3D Mark hang	Improve GPU character	0.2	57	Change PL11 from 0.56uH to 0.36uH(SH000005680) Change PR169 from 2.43KΩ to 3.92KΩ(SD034392180) Change PR176 from 31.6KΩ to 25.5KΩ(SD034255280) ~~Change PR181 from 68.1KΩ to 64.9KΩ(SD034649280)~~ Change PR137 from 6.65KΩ to 7.87KΩ(SD034787180)	2010 01/13	DVT

Delete 2009 11/05

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	PIR (PWR)		
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic		Rev: 0.1
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	01/05	P.40	PWR_LED# connect from +3VALW to +3VS; PWR_SUSP_LED# conector from +3VS to +3VALW	
	01/05	P.10	JDIMM1 and JDIMM2 location swap	
	01/05	P.47~60	upgrade PWR schematic	
	01/06	P.31	Change net name of Q85.pin2/5 from +3VS to +3VS_DELAY	
	01/06	P.35	Add one Lid Switch schematic for reserve	
	01/08	P.47~60	upgrade PWR schematic	
	01/08	P.42	Add two of 300 ohm bead for DMIC_CLK and SPDIF signal(L6/L8)	
	01/11	P.47~60	upgrade PWR schematic	
	01/11	P.40	Reserve R120=300 ohm pull-high to +3VALW	
	01/11	P.18	Change net name of Q23.pin2 from VGA_HDMI_DET to HDMI_HPD	
	01/12	P.25	Add C602=330uF to decrease ripple of +GPU_CORE	
	02/25	P.23	Change net connection(from R45.2 to Q7.1)	
	02/25	P.29	Add R37=SG@ 0 ohm connect between DPST_PWM_1 and INVTPWM	
	02/25	P.34	Add C936~C938=mount 0.1uF for slove EMI issue	
	02/25	P.39	Add R430/R442/R446=mount 10k ohm pull-high to +3VALW	
	02/25	P.39	Change Bom structure of R421/R422/R431 from mount to reserve	
	02/25	P.47~63	upgrade PWR schematic	
	03/01	P.5	Del XDP schematic(JP5/R89/R92/R93/R96/C168/R86/R657/R663)	
	03/01	P.14	Add R326/R345/R782/R796(for use JMB380 Ver.C)	
	03/01	P.14	Add Q49/Q50(for use JMB380 Ver.C)	
	03/01	P.47~63	upgrade PWR schematic	
	03/02	P.37	Add R718/C168 (for reset)	
	03/31	P.23	Add Update VRAM Table	
	03/31	P.43	Change value of R4 from 4.7K ohm to 5.62K ohm	
	03/31	P.43	Change value of C3 from 0.1uF to 0.033uF	
	03/31	P.36	Change Bom structure of R654/R658/R280/R281/R324/R331 from mount to @	
	03/31	P.36	Change Bom structure of L32/L33/L69 from @ to mount	
	03/31	P.36	Change symbol and PN of L32/L33/L39 from SM070001310 to SM070000K00	
	03/31	P.24	Change Bom structure of R83 from SG@ to MAD@	
	04/01	P.39	Change footprint of SW2/SW3 from SW_SKRELGE010_2P to SW_NTC317-AB1G-C220C_2P	
	04/02	P.23	Change PN of Q9 from SB00000D900 to SB00000DH00	
	04/02	P.29	Change PN of Q6/Q80/Q81 from SB00000D900 to SB00000DH00	
	04/02	P.30	Change PN of Q84 from SB00000D900 to SB00000DH00	
	04/02	P.31	Change PN of Q85 from SB00000D900 to SB00000DH00	
	04/02	P.31	Change PN of Q61 from SB570020110 to SB000008J10	
	04/02	P.43	Change PN of Q69 from SB00000D900 to SB00000DH00	
	04/02	P.45	Change PN of Q40/Q41/Q42/Q43 from SB00000D900 to SB00000DH00	
	04/02	P.46	Change PN of Q35/Q47 from SB00000D900 to SB00000DH00	
	04/15	P.39	Change PN of SW2/SW3 from SN100001C00 to SN100003R00	
	04/15	P.41	Change Bom structure of SW1 from mount to @	
	04/18	P.29	Add LVDS schematic(U13/U31/C204/C187=@)	
	04/18	P.40	Add R51=@ 0 ohm	
	04/18	P.47~63	upgrade PWR schematic	

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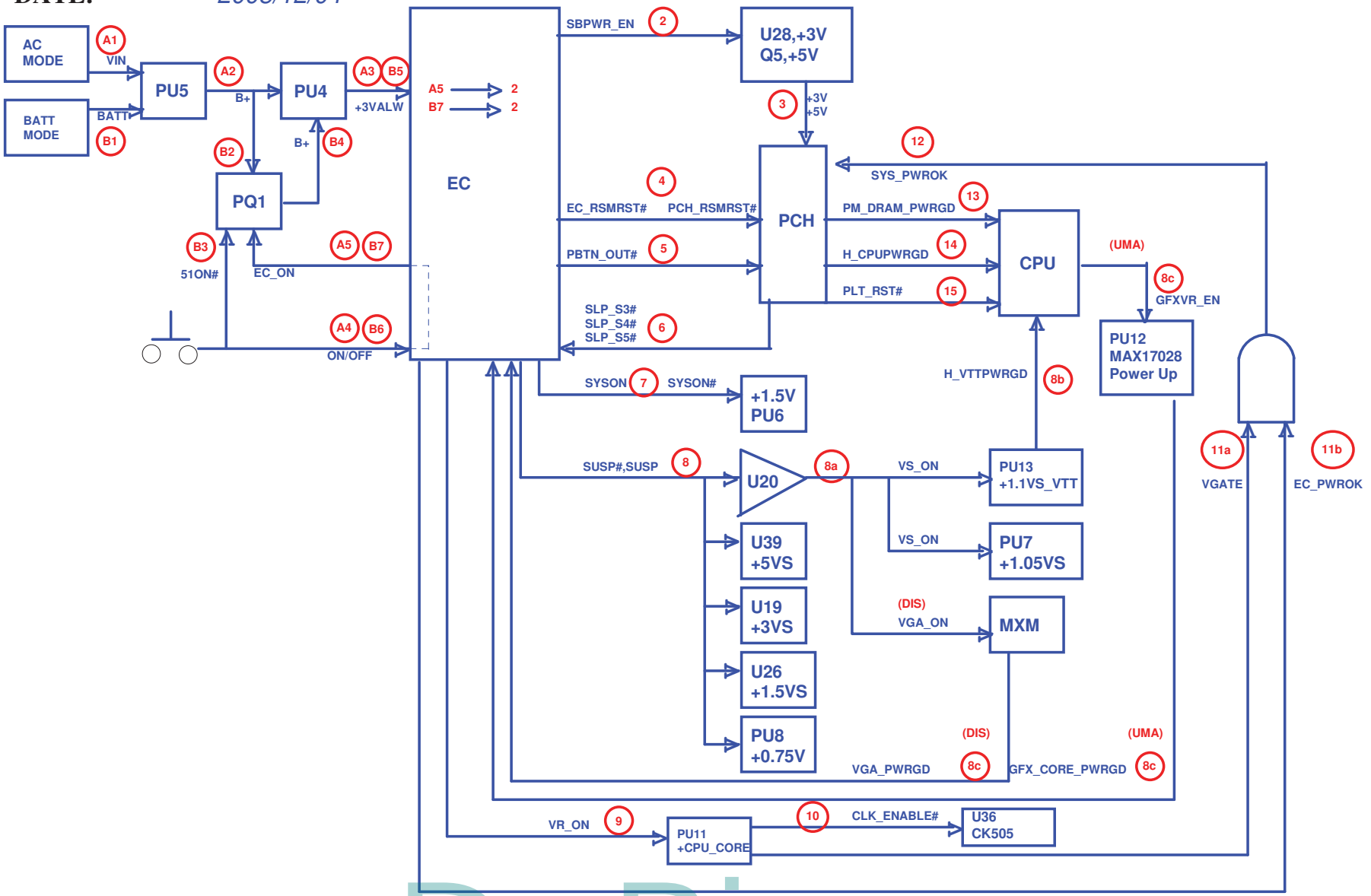
Compal Electronics, Inc.		
Title	HW PIR	
Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic	Rev: 1.0
Date: Sunday, April 18, 2010	Sheet 61 of 63	

COMPAL CONFIDENTIAL

MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Power Sequence Block Diagram

Size: Custom | Document Number: NCQF0 M/B LA-5981P Schematic | Rev: 0.1

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	EMI request	Cut-in snubber and couple cap on B+	0.2		Enable 3V/5V/1.5V/1.05V/VTT/GPU snubber	2010 01/13	DVT
25	Buyer request	Costdown	0.2		Change PU10,PU11,PU12 from TPS51117 to G5603(SA00003HM00)	2010 01/14	DVT
26	HW/Ivan request	Raise voltage 2%(Arrendale only)	0.3	56	Change PR153 from 4.99KΩ to 5.36KΩ(SD034536180)	2010 02/11	PVT
27	The same setting for 2nd source	Fix 5V for all IC	0.3	51	Disable PR87	2010 02/23	PVT
28	GPU output cap add 330uF for hang issue	Tune VDDCIP sequence and Power common design	0.3	54	Change PR131 from 57.6KΩ to 301KΩ(SD034301380) Net +5VALW instead of +5VSDGPU	2010 02/23	PVT
29	EMI request	Cut-in snubber and boost res.	0.3		Change PR122,PR142,PR236,PR249,PR275 from 0Ω to 2.2Ω(SD013220B80) Add PR238,PR251 to 4.7Ω Add PC161,PC173 to 470pF	2010 02/25	PVT
30	65/90# only low signal	Fix adapter mode	0.4	50	Disable PR73, PQ24	2010 03/23	Pre-MP
8	Protect logic deformation	Add PH2 function	0.4	48	Change PR23 from 0Ω to 29.4Ω(SD034294280) Add PR27, PH2	2010 03/23	Pre-MP
9	Improve anti-noise	Reduce voltage divider	0.4	54	Change PR138 from 43K to 2.05K(SD034205180) Change PR139 from 124K to 5.9K(SD034590180) Change PR283 from 60.4K to 2.87K(SD034287180)	2010 03/26	Pre-MP
10	Improve anti-noise	Reduce voltage divider	0.4	55	~~Change PR278 from 124K to 5.9K(SD034590180)~~ Change PR279 from 127K to 6.04K(SD034604180) Change PR127 from 24K to 1.15K(SD034115180) ~~Change PR128 from 59K to 2.8K(SD034280180)~~	2010 03/26	Pre-MP
11							
12	Cut-in 120W adapter	Tune a CP setting for 120W adapter	0.4	50	Change PR47 from 0.02 to 0.015(SD000001E00)	2010 03/26	Pre-MP
13	Modify VGA voltage table	Rise Broadway voltage to the same to Park	0.4	57	Change PR179 from 9.53 to 8.87 Change PR181 from 64.9 to 43.2	2010 04/16	Pre-MP
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/25	Deciphered Date	2010/08/25
		Title	PIR (PWR)
		Size: Custom	Document Number: NCQF0 M/B LA-5981P Schematic
		Rev	0.1
		Date: Sunday, April 18, 2010	Sheet 63 of 63