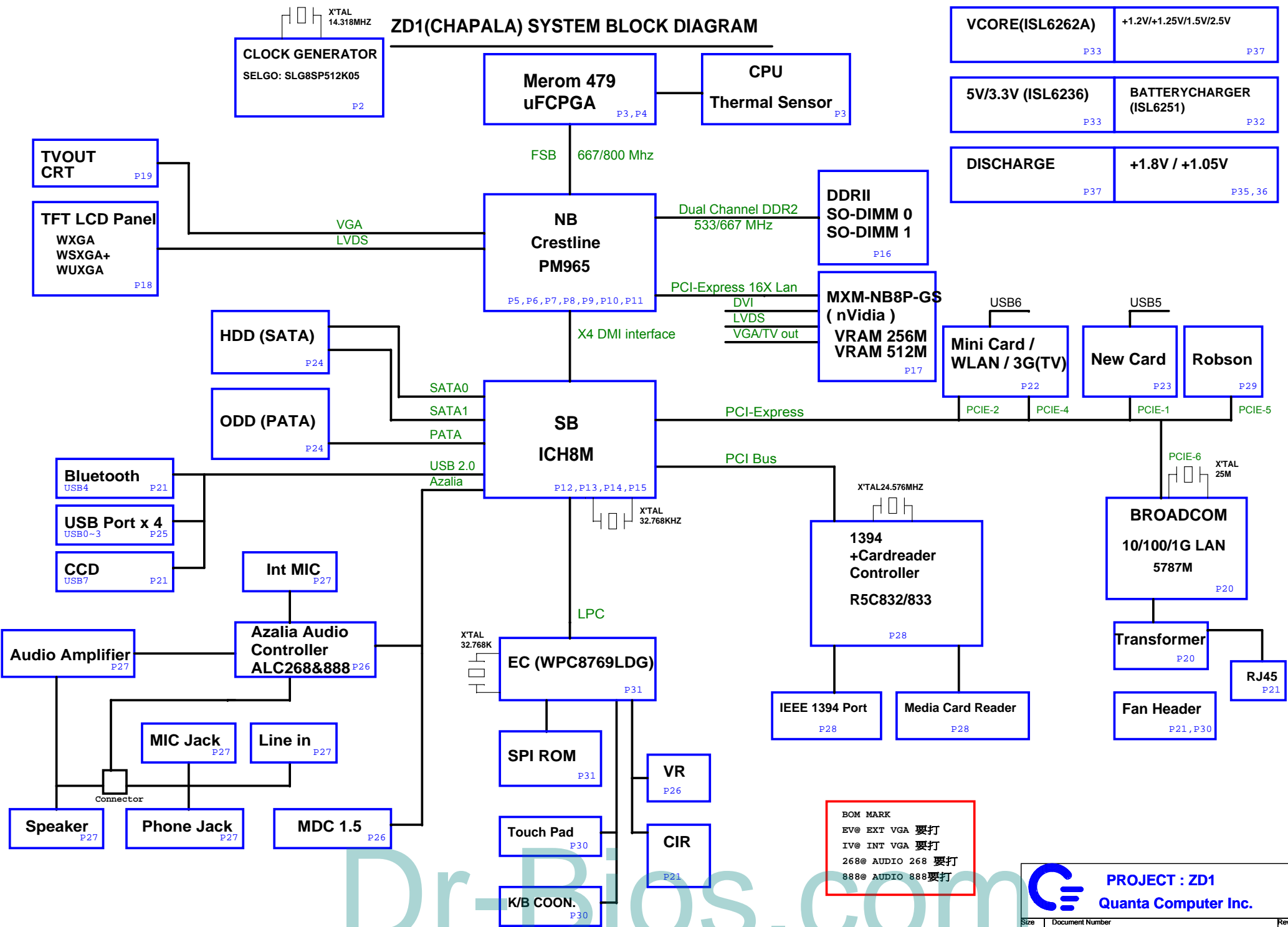


ZD1(CHAPALA) SYSTEM BLOCK DIAGRAM

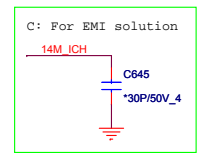
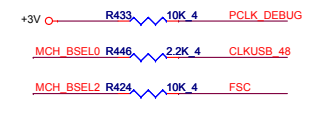
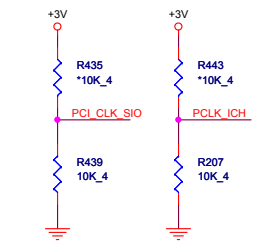
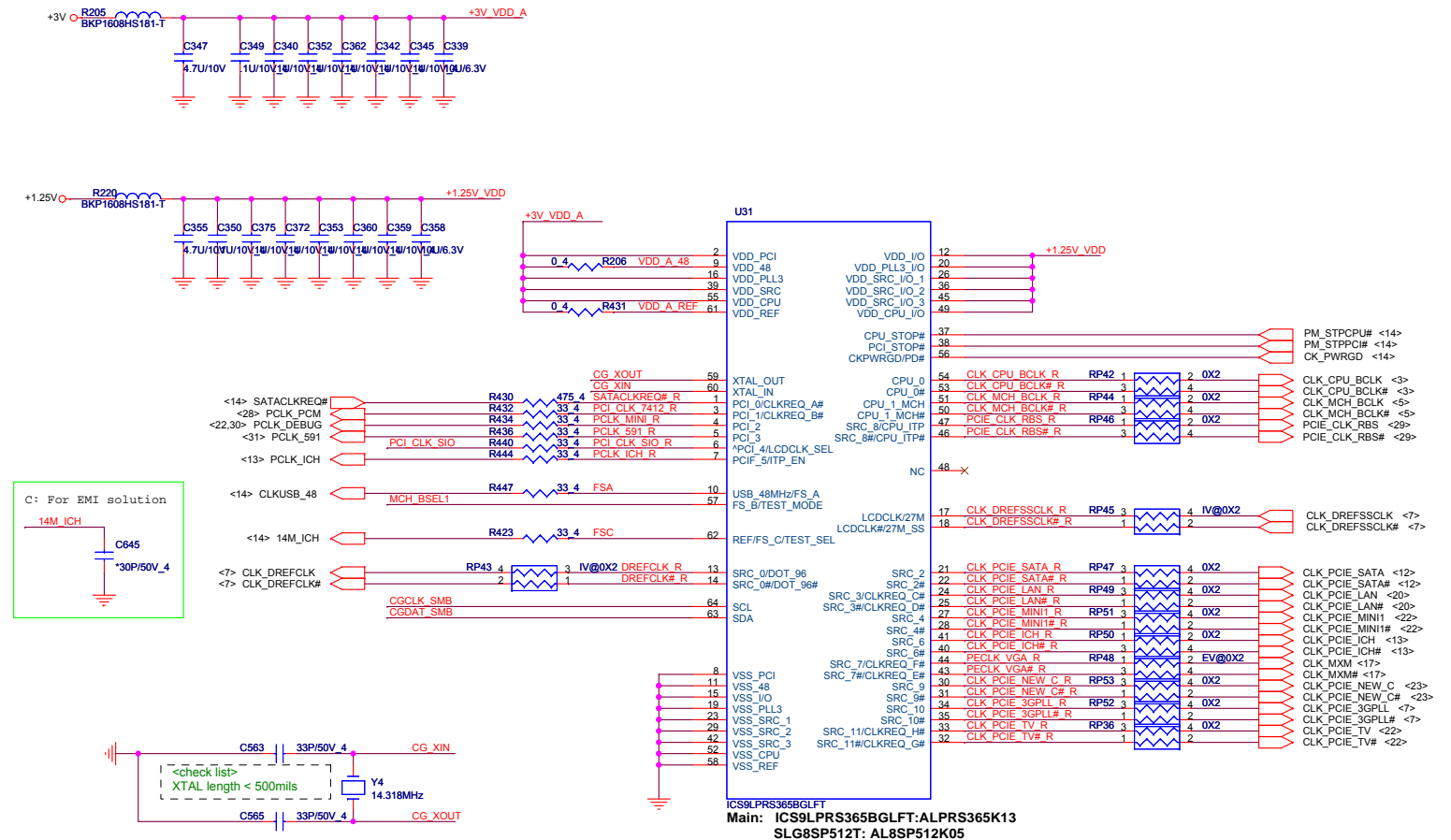


VCORE(ISL6262A) P33	+1.2V/+1.25V/1.5V/2.5V P37
5V/3.3V (ISL6236) P33	BATTERYCHARGER (ISL6251) P32
DISCHARGE P37	+1.8V / +1.05V P35, 36

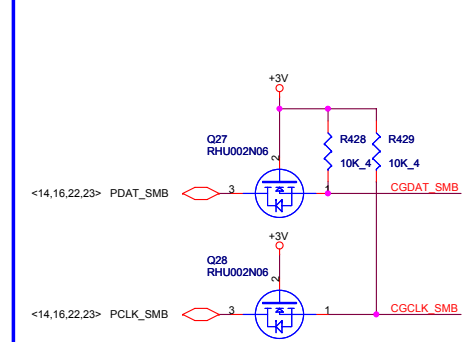
BOM MARK
 EV@ EXT VGA 要打
 IV@ INT VGA 要打
 268@ AUDIO 268 要打
 888@ AUDIO 888 要打

Clock Generator

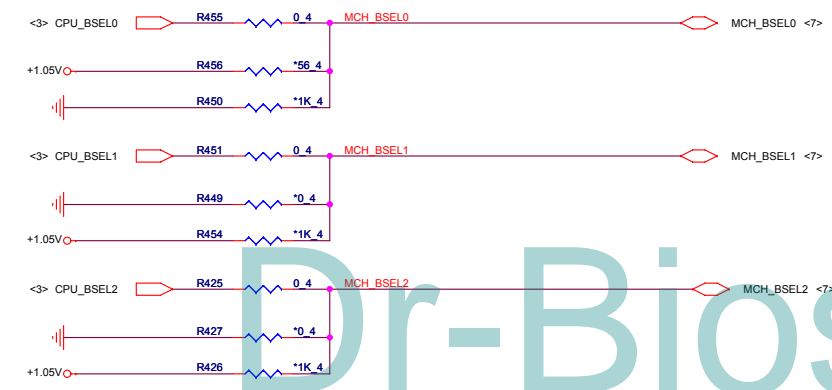
Change list:
 B-test
 1.Change U31 P/N to ALPRS365K13 (ICS)



Clock Gen I2C



CPU Clock select

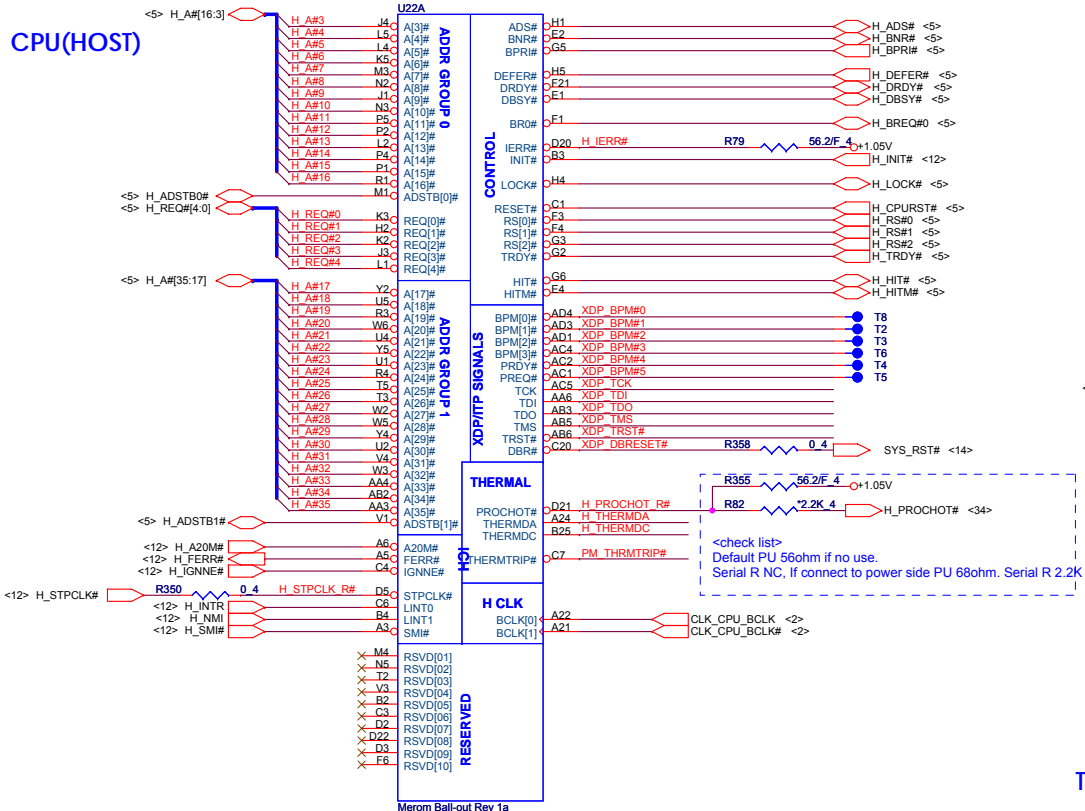


BSEL Frequency Select Table

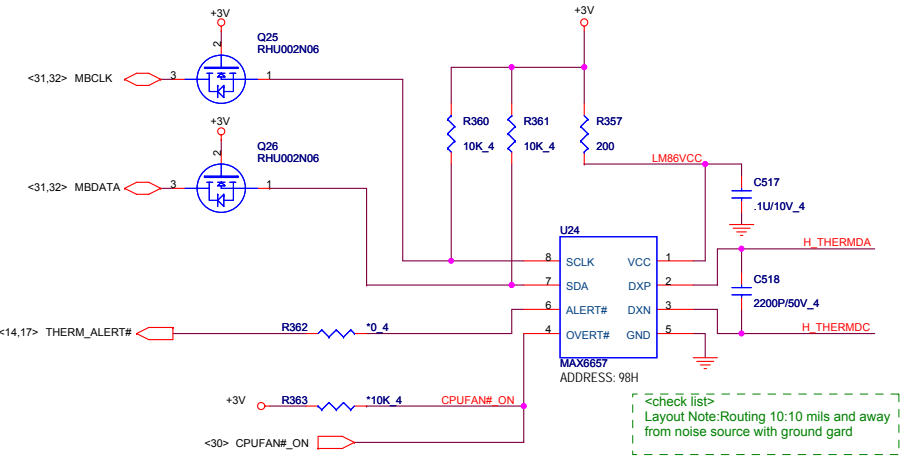
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	1.33Mhz
0	1	1	1.66Mhz
0	1	0	2.00Mhz
1	1	0	4.00Mhz
1	1	1	Reserved
1	0	1	1.00Mhz
1	0	0	3.33Mhz

PROJECT : ZD1
Quanta Computer Inc.

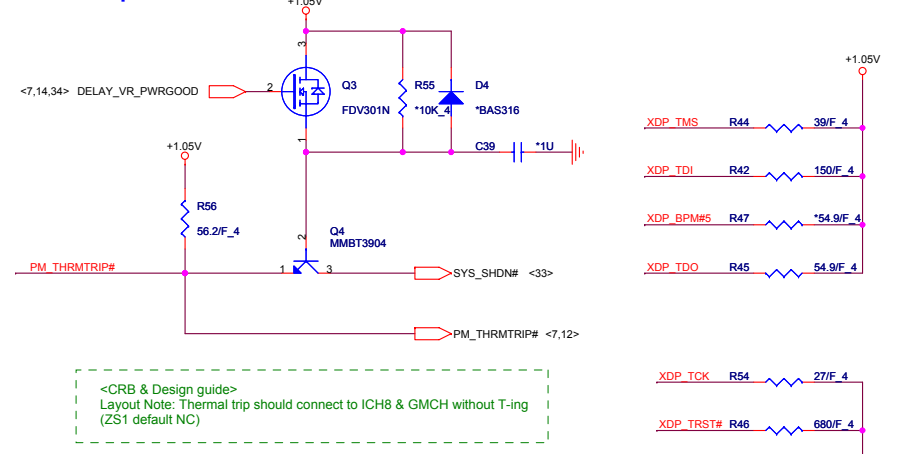
CPU(HOST)



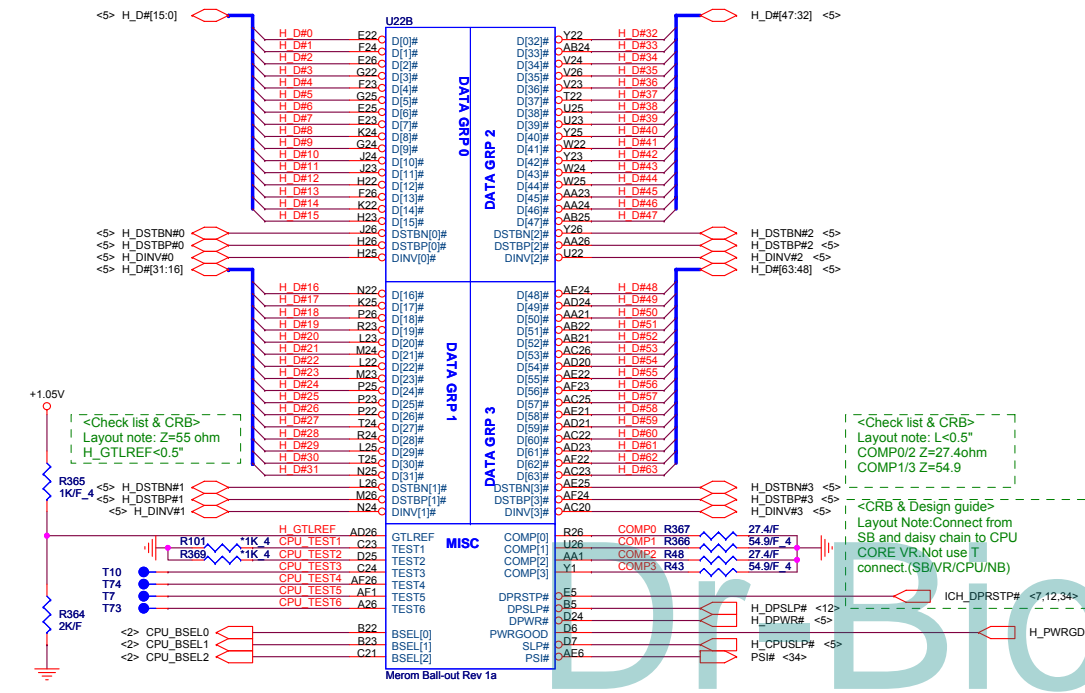
CPU Thermal monitor



Thermal Trip

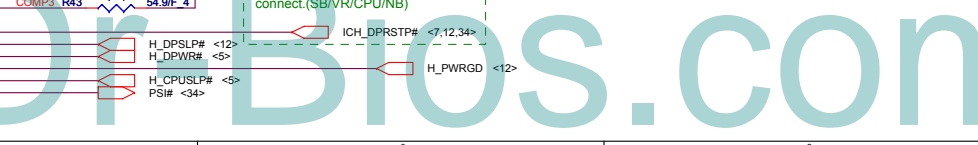


PU/PD (ITP700)



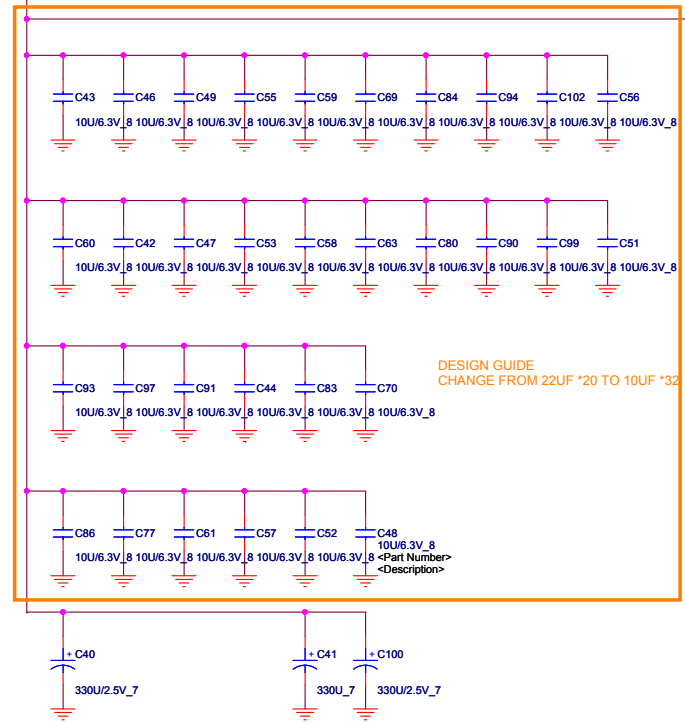
PROJECT : ZD1
Quanta Computer Inc.

Size Document Number
CPU(1 of 2)/FAN/Thermal
Date: Monday, May 07, 2007 Sheet 3 of 38



CPU(Power)

VCC_CORE

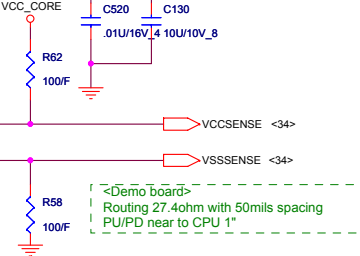
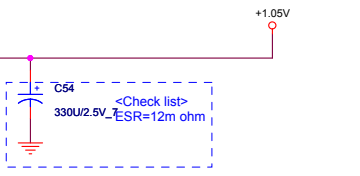
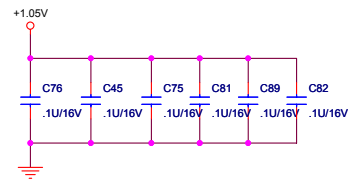


<Check list>
Option1:330U*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U*20(ESR=3mohm typ/20 , ESL=0.6nH/20)
Option2:330U*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

U22C		
A7	VCC[001]	VCC[068]
A9	VCC[002]	VCC[069]
A10	VCC[003]	VCC[070]
A12	VCC[004]	VCC[071]
A15	VCC[005]	VCC[072]
A16	VCC[006]	VCC[073]
A17	VCC[007]	VCC[074]
A18	VCC[008]	VCC[075]
A20	VCC[009]	VCC[076]
B7	VCC[010]	VCC[077]
B9	VCC[011]	VCC[078]
B10	VCC[012]	VCC[079]
B12	VCC[013]	VCC[080]
B14	VCC[014]	VCC[081]
B15	VCC[015]	VCC[082]
B17	VCC[016]	VCC[083]
B18	VCC[017]	VCC[084]
B20	VCC[018]	VCC[085]
C9	VCC[019]	VCC[086]
C10	VCC[020]	VCC[087]
C12	VCC[021]	VCC[088]
C13	VCC[022]	VCC[089]
C15	VCC[023]	VCC[090]
C17	VCC[024]	VCC[091]
C18	VCC[025]	VCC[092]
D9	VCC[026]	VCC[093]
D10	VCC[027]	VCC[094]
D12	VCC[028]	VCC[095]
D14	VCC[029]	VCC[096]
D15	VCC[030]	VCC[097]
D17	VCC[031]	VCC[098]
D18	VCC[032]	VCC[099]
E7	VCC[033]	VCC[100]
E9	VCC[034]	VCC[101]
E10	VCC[035]	VCC[102]
E12	VCC[036]	VCC[103]
E13	VCC[037]	VCC[104]
E15	VCC[038]	VCC[105]
E17	VCC[039]	VCC[106]
E18	VCC[040]	VCC[107]
E20	VCC[041]	VCC[108]
F7	VCC[042]	VCC[109]
F9	VCC[043]	VCC[110]
F10	VCC[044]	VCC[111]
F12	VCC[045]	VCC[112]
F14	VCC[046]	VCC[113]
F15	VCC[047]	VCC[114]
F18	VCC[048]	VCC[115]
F20	VCC[049]	VCC[116]
AA7	VCC[050]	VCC[117]
AA9	VCC[051]	VCC[118]
AA10	VCC[052]	VCC[119]
AA12	VCC[053]	VCC[120]
AA13	VCC[054]	VCC[121]
AA15	VCC[055]	VCC[122]
AA17	VCC[056]	VCC[123]
AA18	VCC[057]	VCC[124]
AA20	VCC[058]	VCC[125]
AB9	VCC[059]	VCC[126]
AC10	VCC[060]	VCC[127]
AB10	VCC[061]	VCC[128]
AB12	VCC[062]	VCC[129]
AB14	VCC[063]	VCC[130]
AB15	VCC[064]	VCC[131]
AB17	VCC[065]	VCC[132]
AB18	VCC[066]	VCC[133]
AB18	VCC[067]	VCC[134]

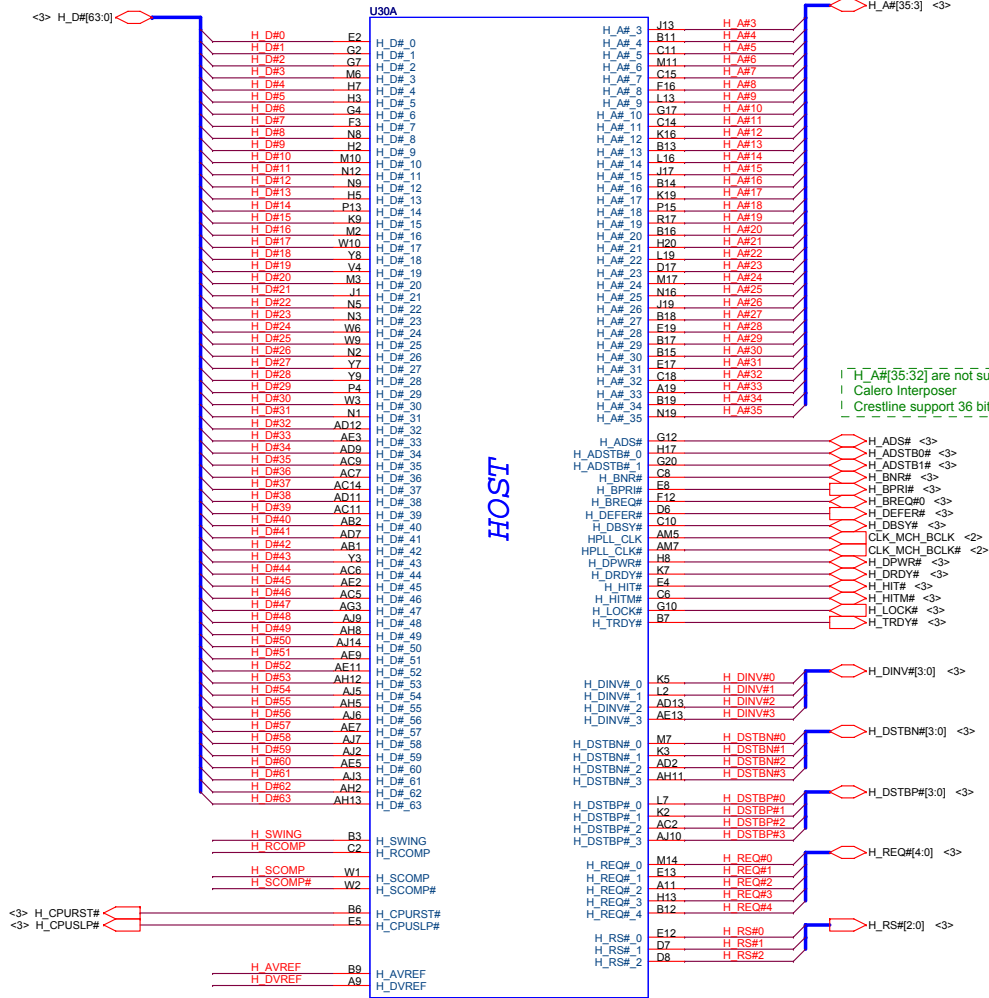
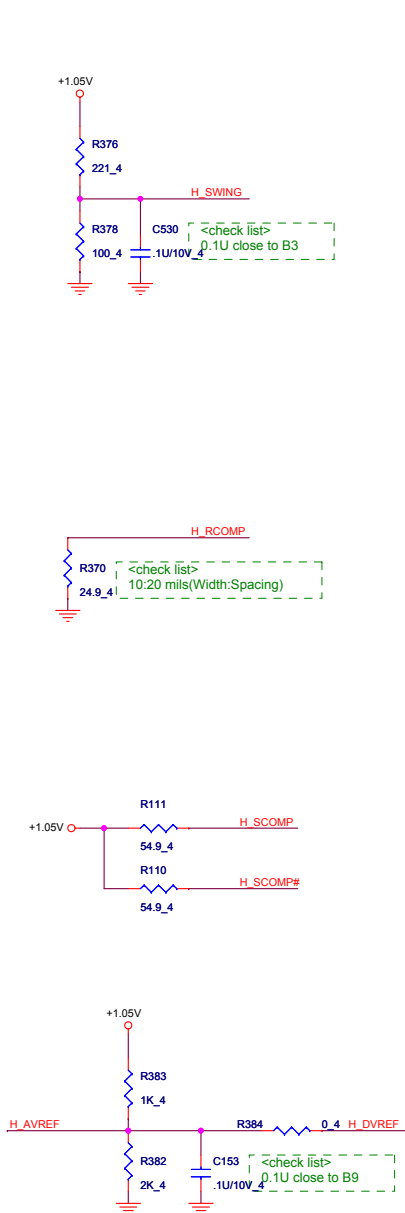
Merom Ball-out Rev 1a

<REV.NO. 0.5/REF.NO.19343>
Ivccp Max 52A
Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)
Ivcca Max 130mA

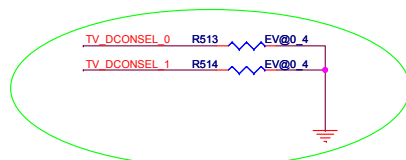
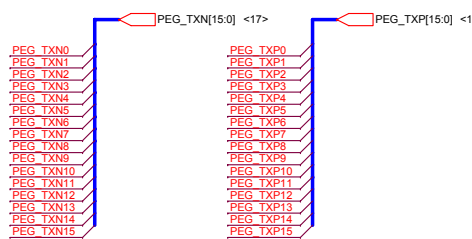
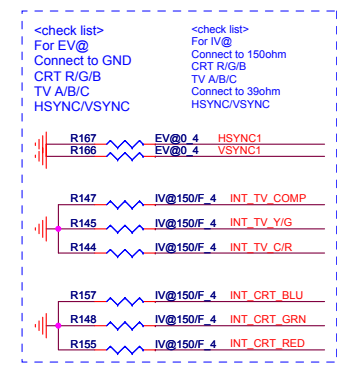
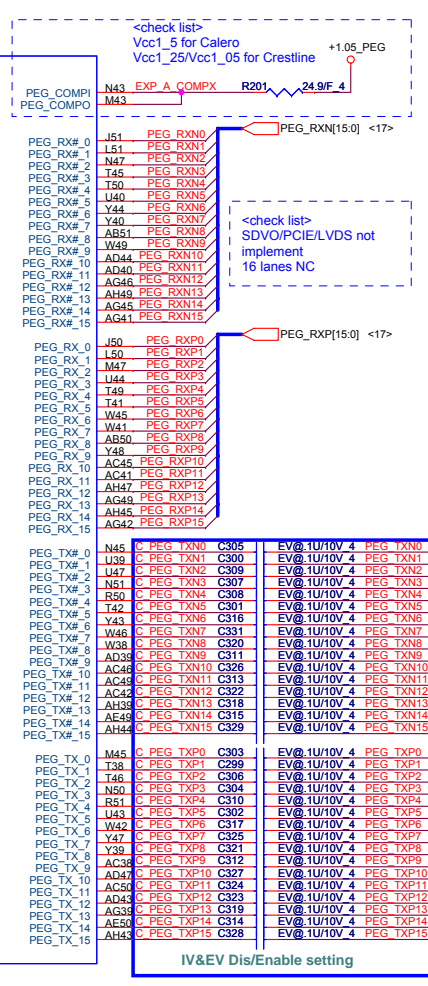
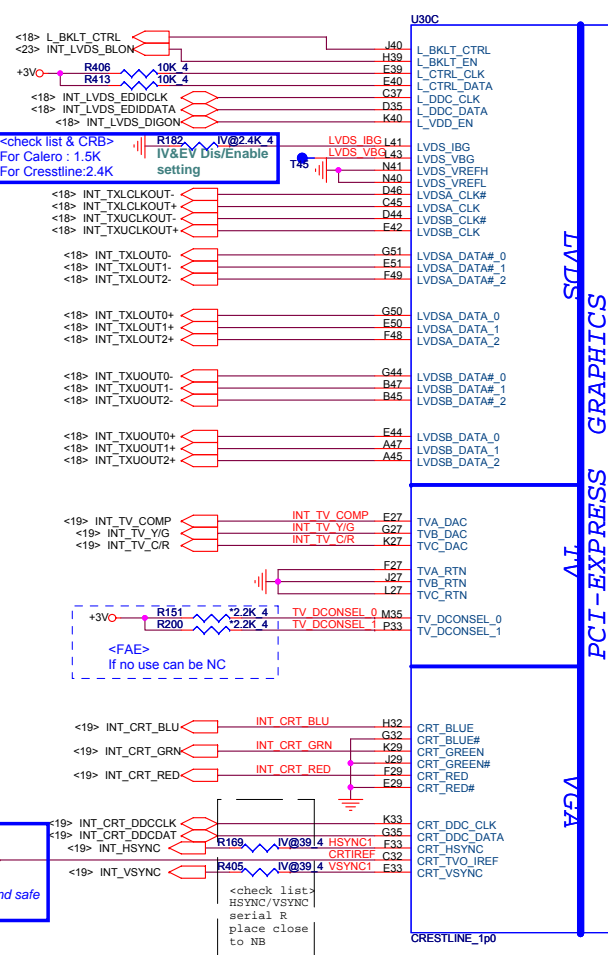


U22D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AF2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B24	VSS[015]	VSS[096]
C2	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C16	VSS[020]	VSS[101]
C19	VSS[021]	VSS[102]
C22	VSS[022]	VSS[103]
C25	VSS[023]	VSS[104]
D1	VSS[024]	VSS[105]
D11	VSS[025]	VSS[106]
D13	VSS[026]	VSS[107]
D16	VSS[027]	VSS[108]
D19	VSS[028]	VSS[109]
D23	VSS[029]	VSS[110]
D26	VSS[030]	VSS[111]
E3	VSS[031]	VSS[112]
E6	VSS[032]	VSS[113]
E8	VSS[033]	VSS[114]
E11	VSS[034]	VSS[115]
E16	VSS[035]	VSS[116]
E19	VSS[036]	VSS[117]
E21	VSS[037]	VSS[118]
E24	VSS[038]	VSS[119]
F5	VSS[039]	VSS[120]
F8	VSS[040]	VSS[121]
F11	VSS[041]	VSS[122]
F13	VSS[042]	VSS[123]
F16	VSS[043]	VSS[124]
F19	VSS[044]	VSS[125]
F25	VSS[045]	VSS[126]
G2	VSS[046]	VSS[127]
G26	VSS[047]	VSS[128]
H3	VSS[048]	VSS[129]
H6	VSS[049]	VSS[130]
H21	VSS[050]	VSS[131]
H24	VSS[051]	VSS[132]
J5	VSS[052]	VSS[133]
J22	VSS[053]	VSS[134]
K4	VSS[054]	VSS[135]
K11	VSS[055]	VSS[136]
K23	VSS[056]	VSS[137]
K26	VSS[057]	VSS[138]
L3	VSS[058]	VSS[139]
L6	VSS[059]	VSS[140]
L21	VSS[060]	VSS[141]
L24	VSS[061]	VSS[142]
M2	VSS[062]	VSS[143]
M5	VSS[063]	VSS[144]
M22	VSS[064]	VSS[145]
M25	VSS[065]	VSS[146]
N1	VSS[066]	VSS[147]
N4	VSS[067]	VSS[148]
N23	VSS[068]	VSS[149]
N26	VSS[069]	VSS[150]
P3	VSS[070]	VSS[151]
	VSS[071]	VSS[152]
	VSS[072]	VSS[153]
	VSS[073]	VSS[154]
	VSS[074]	VSS[155]
	VSS[075]	VSS[156]
	VSS[076]	VSS[157]
	VSS[077]	VSS[158]
	VSS[078]	VSS[159]
	VSS[079]	VSS[160]
	VSS[080]	VSS[161]
	VSS[081]	VSS[162]
	VSS[082]	VSS[163]

Merom Ball-out Rev 1a



H_A# [35:32] are not supported in Calero Interposer
 Crestline support 36 bit address



INTEL FAE request PD.

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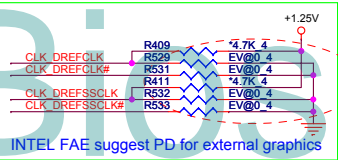
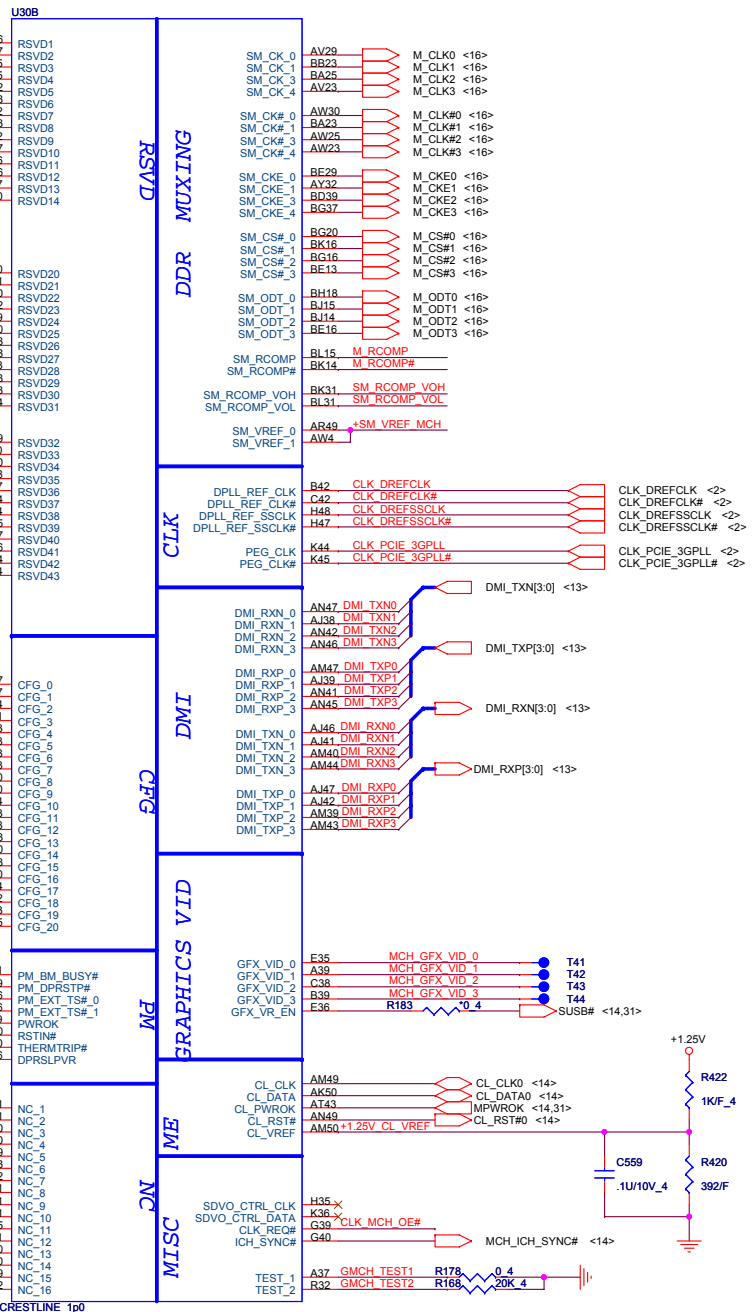
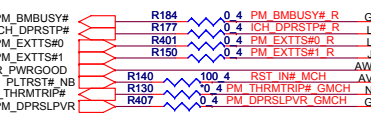
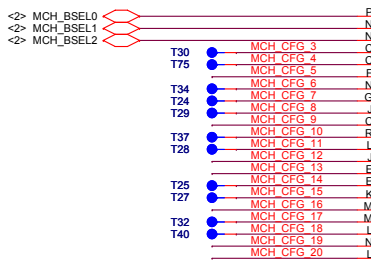
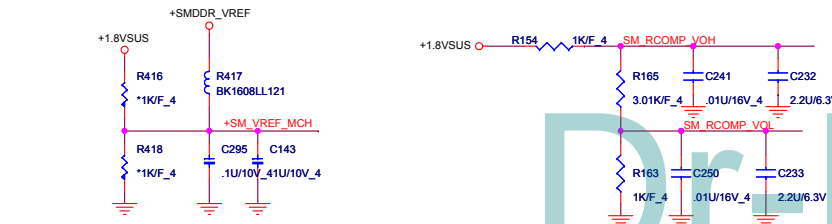
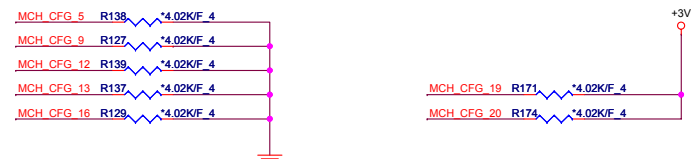
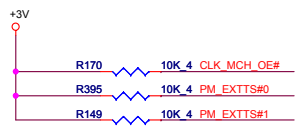
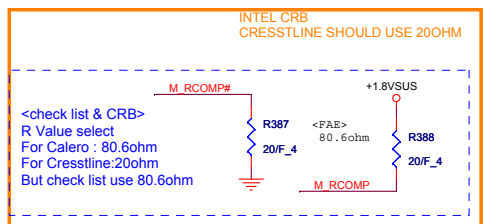
PROJECT : ZD1
 Quanta Computer Inc.

Size Document Number
 GMCH GRAPHICS(277)
 Date: Monday, May 07, 2007 Sheet 6 of 38 Rev E

Strapping table

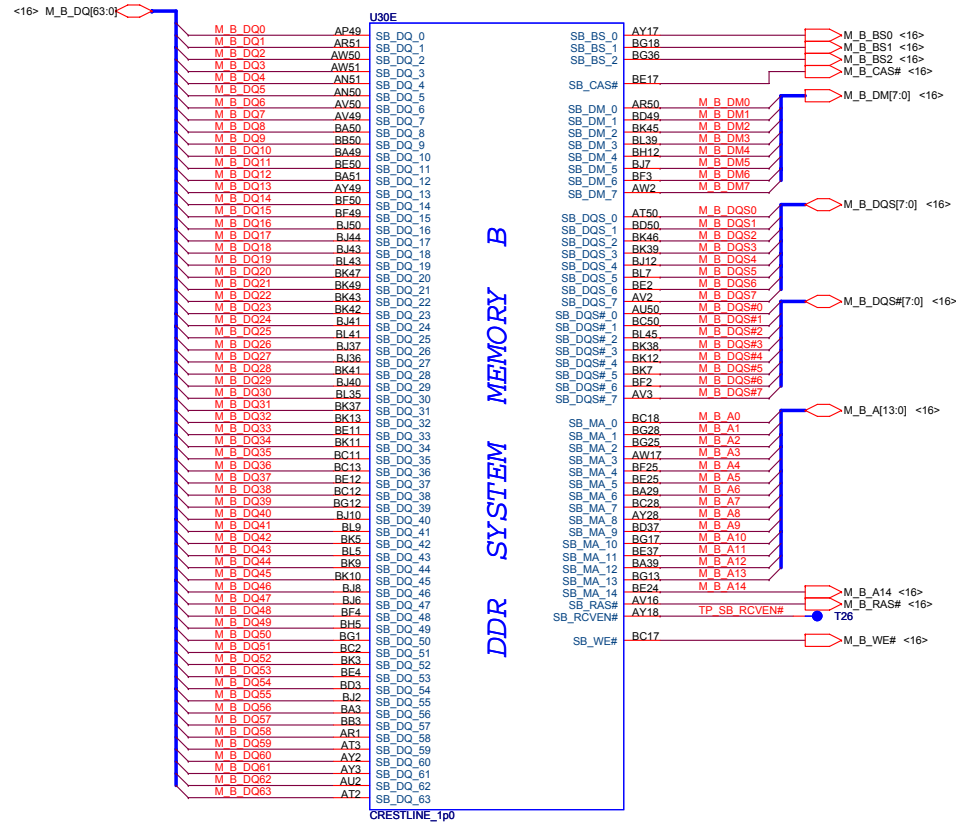
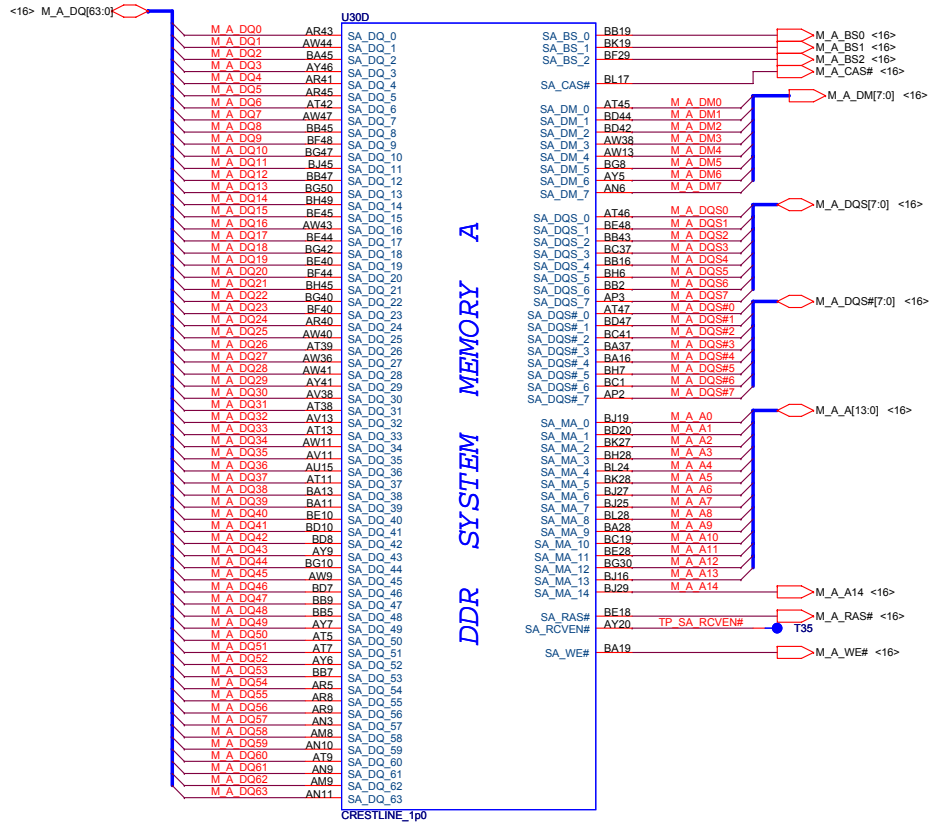
All strap are sampled with respect to the leading edge of the GMCH power ok signal
 CFG[17:3] have internal pull-up
 CFG[18:19] have internal pull-down
 Any CFG signal strapping option not list below should be left NC pin

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CEG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Mobile CPU (Default) 1 = Reserved Lanes
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reserved Lanes 1 = Normal operation (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ ALLZ/ Clock Un gating	00 = Clock gating disable 01 = ALL-Z Mode Enable 10 = XOR Mode Enable 11 = Normal C operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation 1 = Reverse Lanes (Default)
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIe x1 is operation (Default) 1 = SDVO and PCIe x1 are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card Present

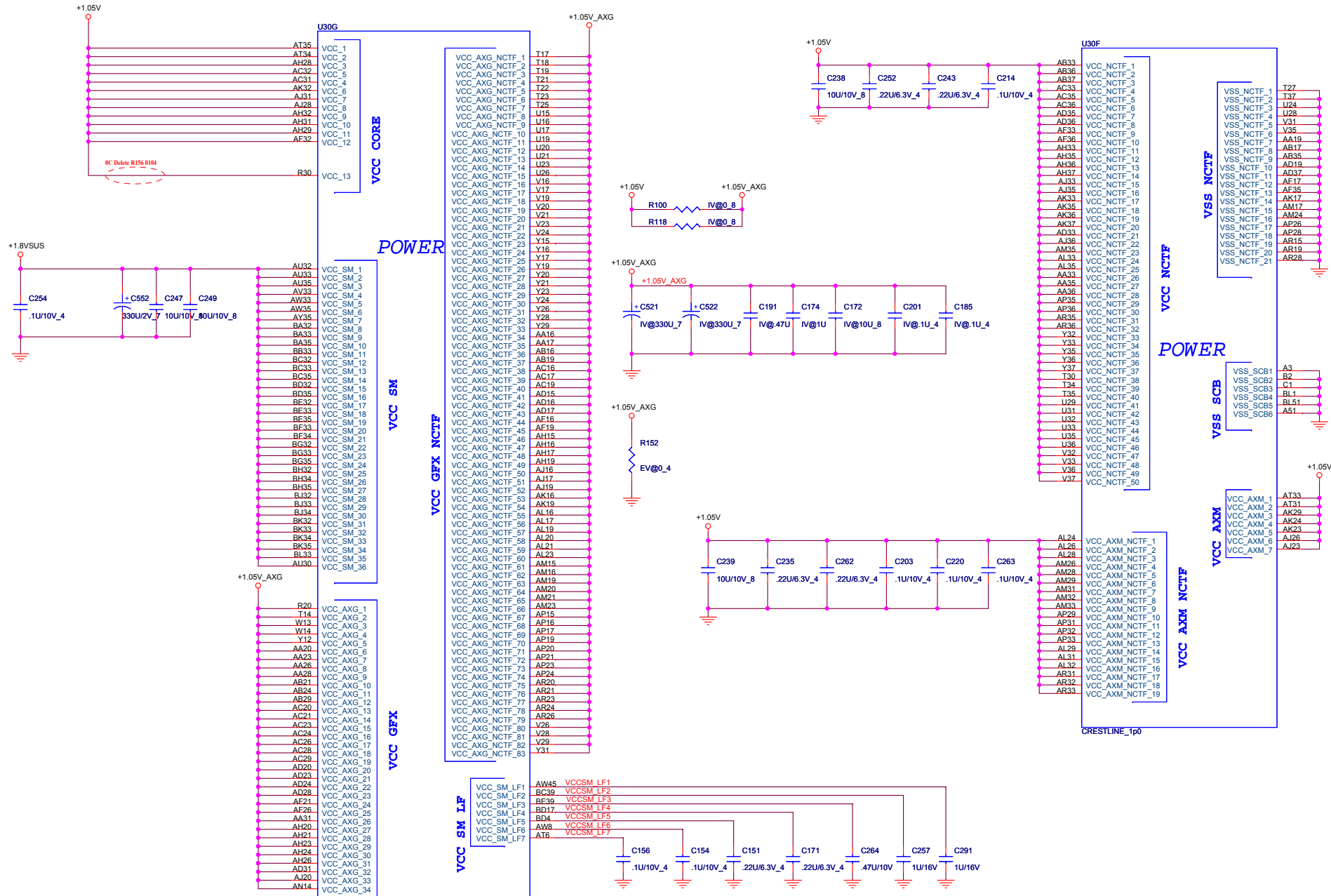


PROJECT : ZD1
 Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (STRAPPING/OTHER 3/7)	E
Date:	Monday, May 07, 2007	Sheet 7 of 38



NB(Power-1)



CRESTLINE_1p0

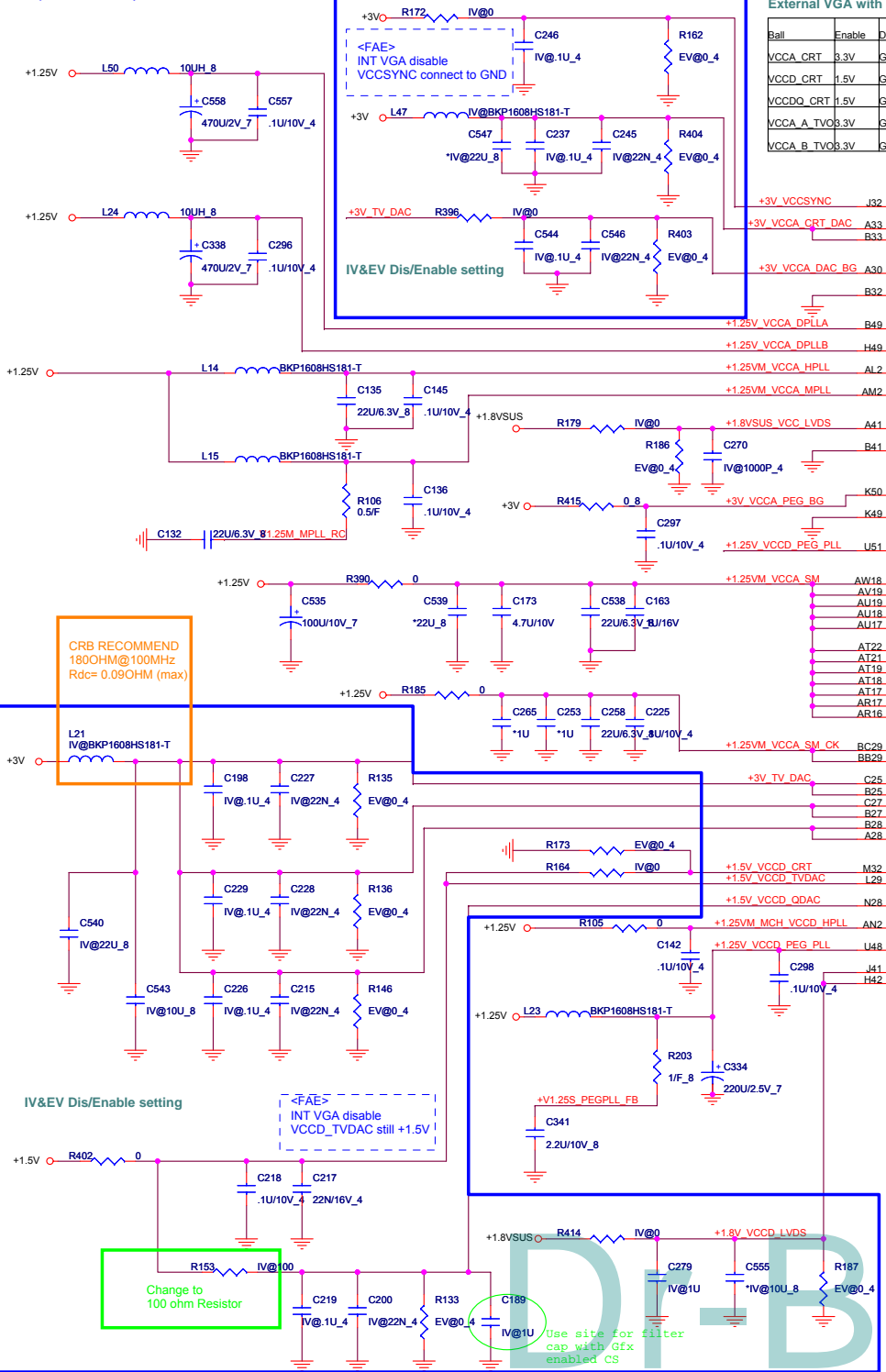
CRESTLINE_1p0



PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-1(5/7)	E
Date:	Wednesday, April 25, 2007	Sheet 9 of 38

NB(Power-2)



CRT/TV Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

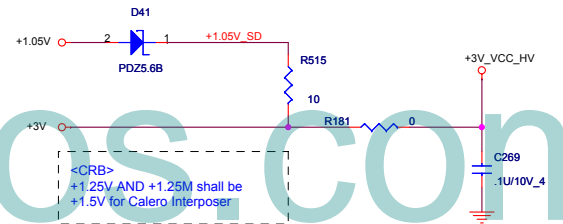
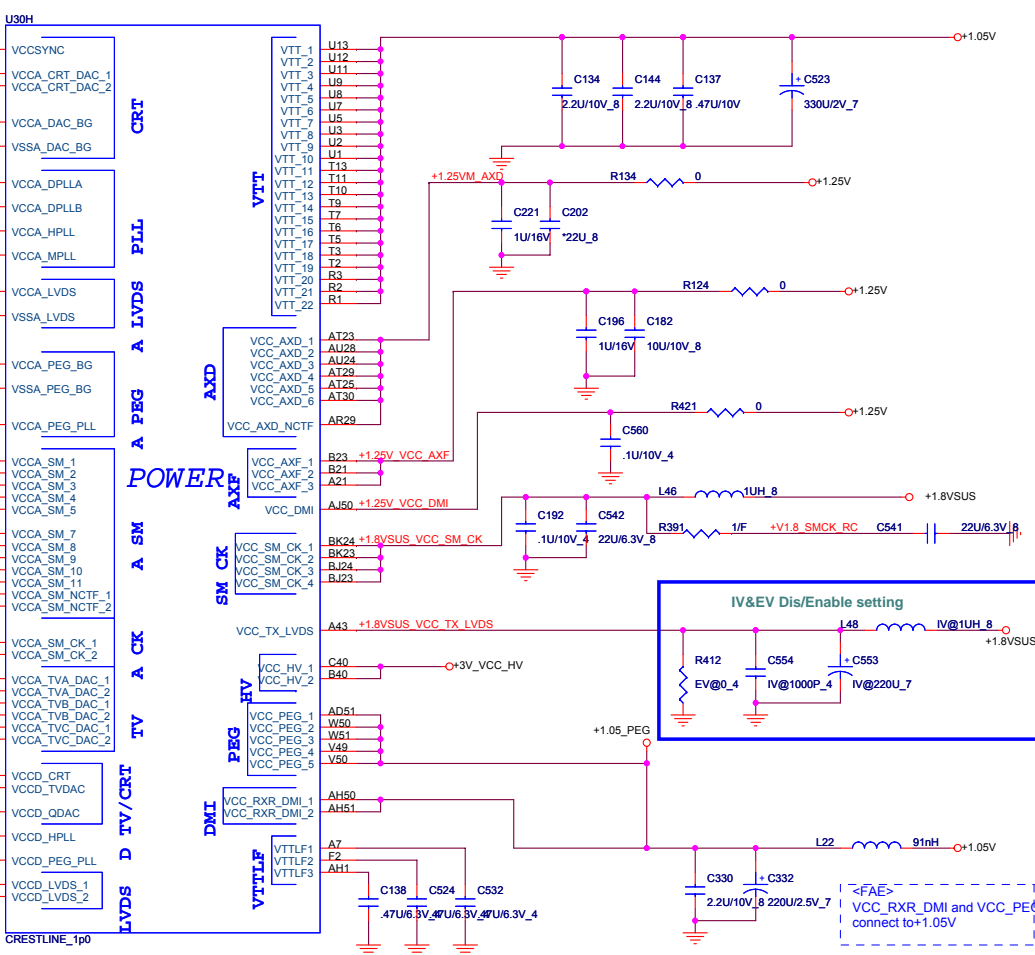
Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TV0	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TV0	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

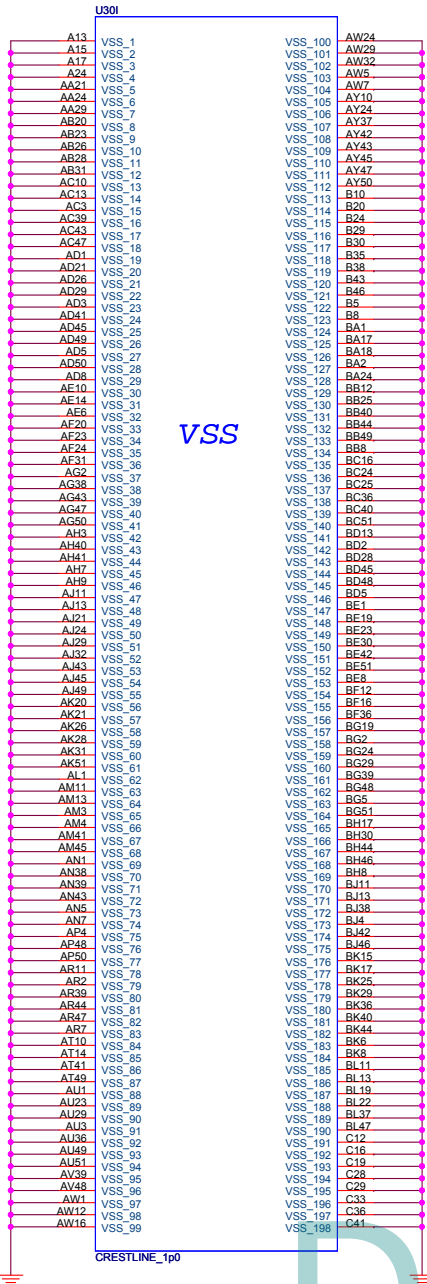
Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCXTX_LVDS	GND	GND	1.8V

EXTERNAL INTERNAL

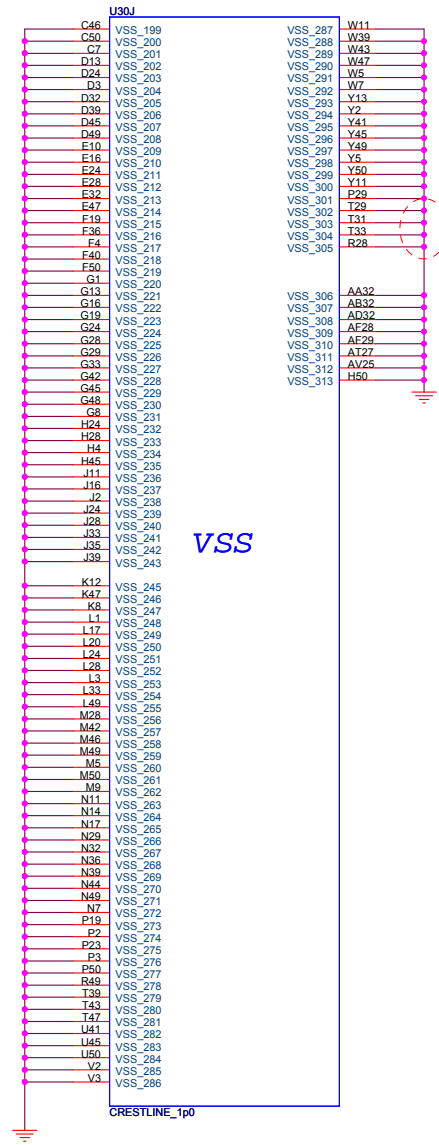


PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-2(6/7)	E
Date:	Wednesday, April 25, 2007	Sheet 10 of 38



VSS



VSS

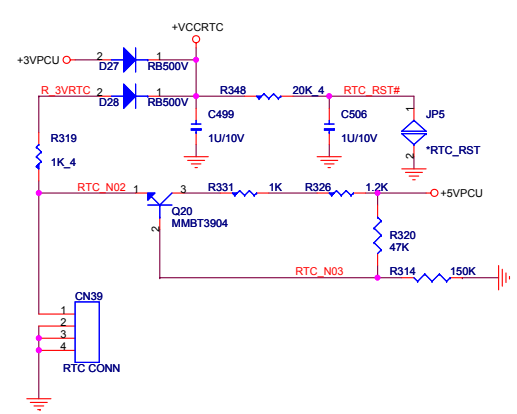
OC Data: R142,R197,R198,R143 0104



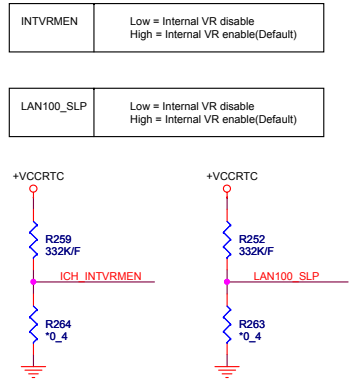
PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-3(7/7)	E
Date:	Wednesday, April 25, 2007	Sheet 11 of 38

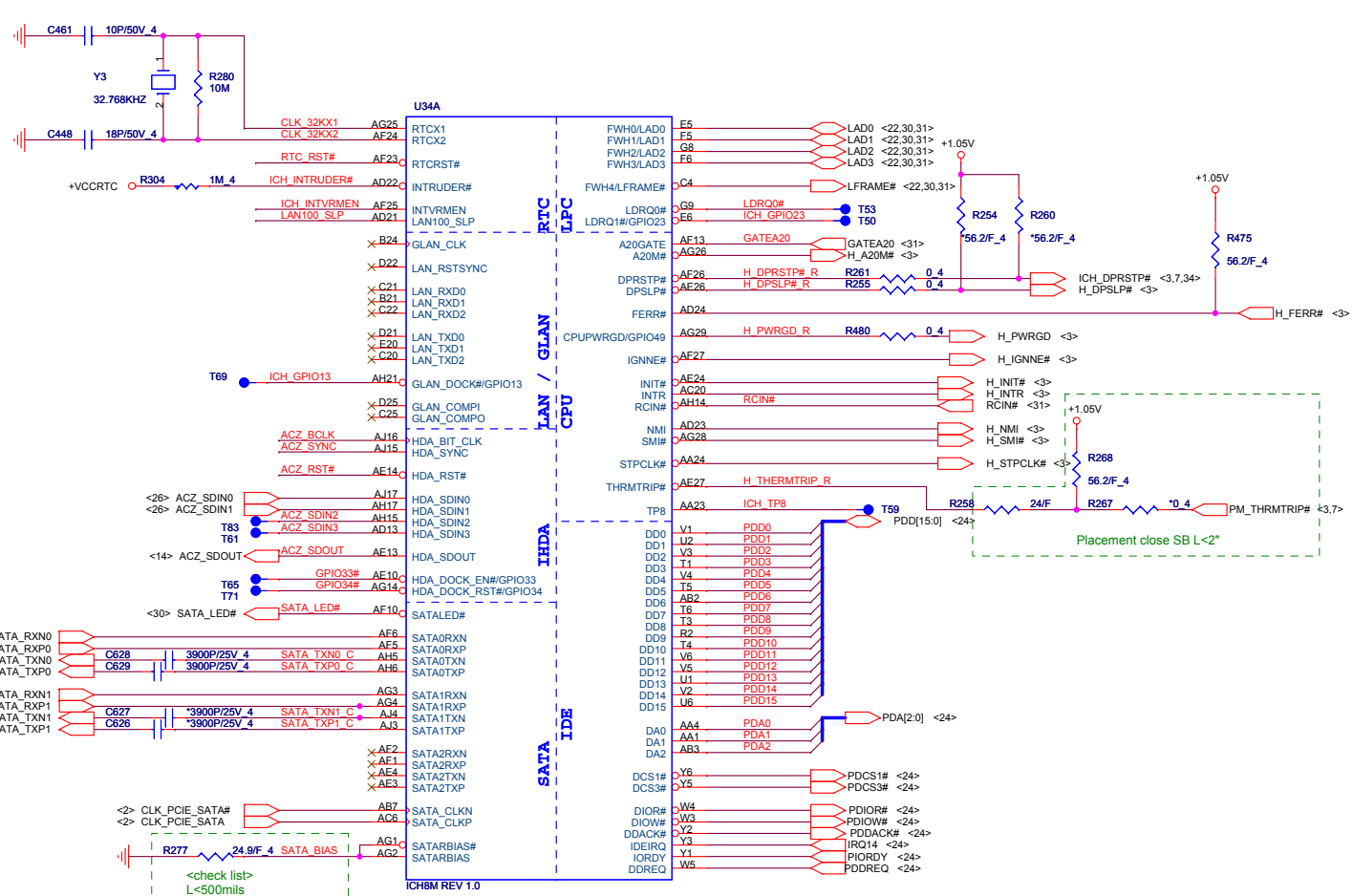
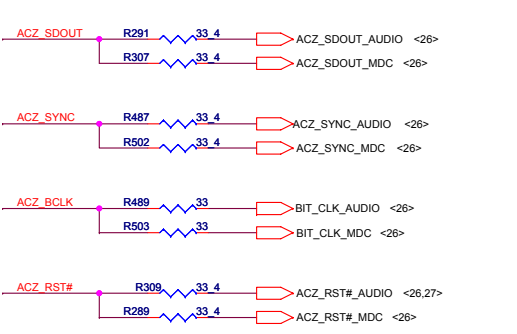
RTC



SB Strap



HDA



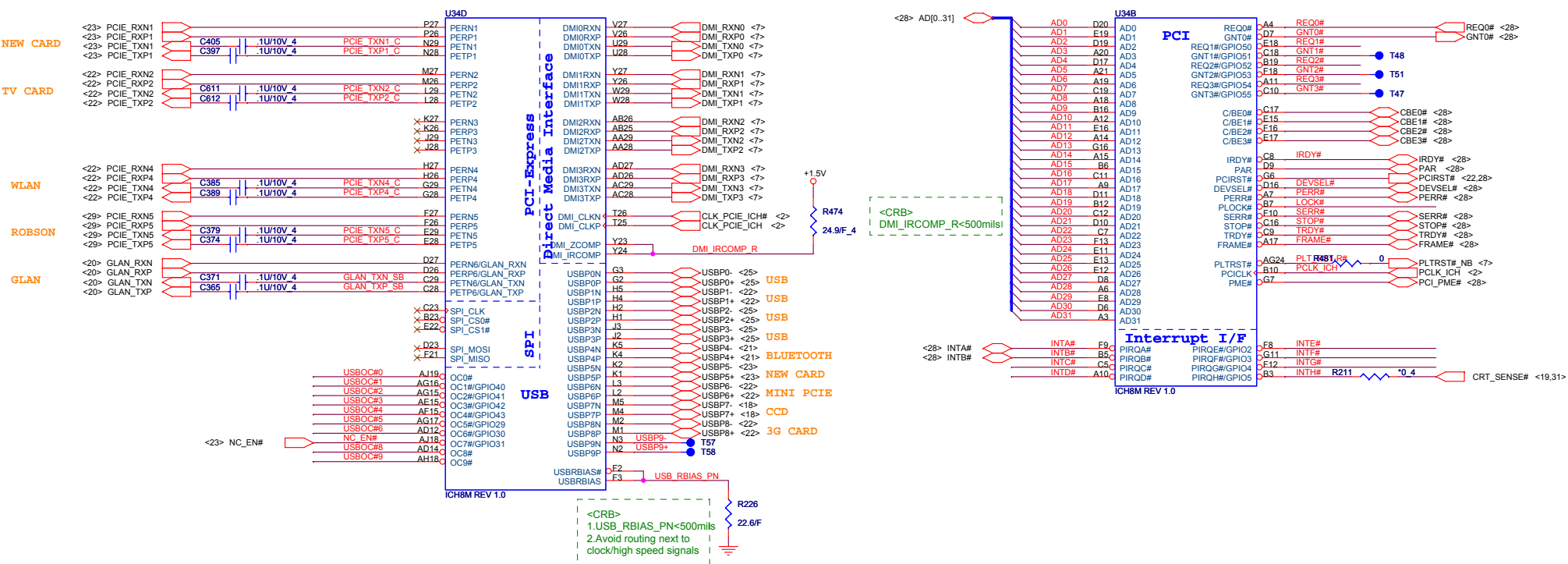
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PROJECT : ZD1
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Size	Document Number	Rev
	ICH8M HOST(1/4)	E
Date:	Monday, May 07, 2007	Sheet 12 of 38

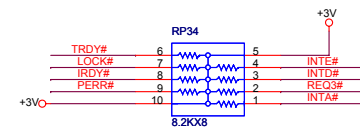
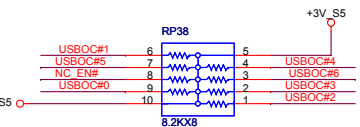
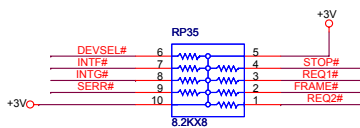
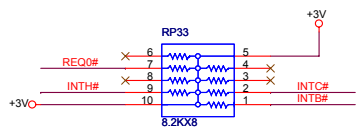
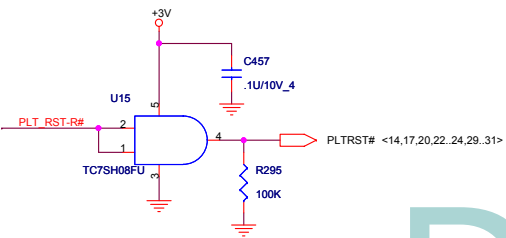
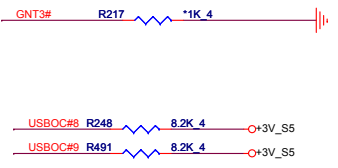
SB-PCIE/USB/DMI

SB-PCI



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default
-----------	---



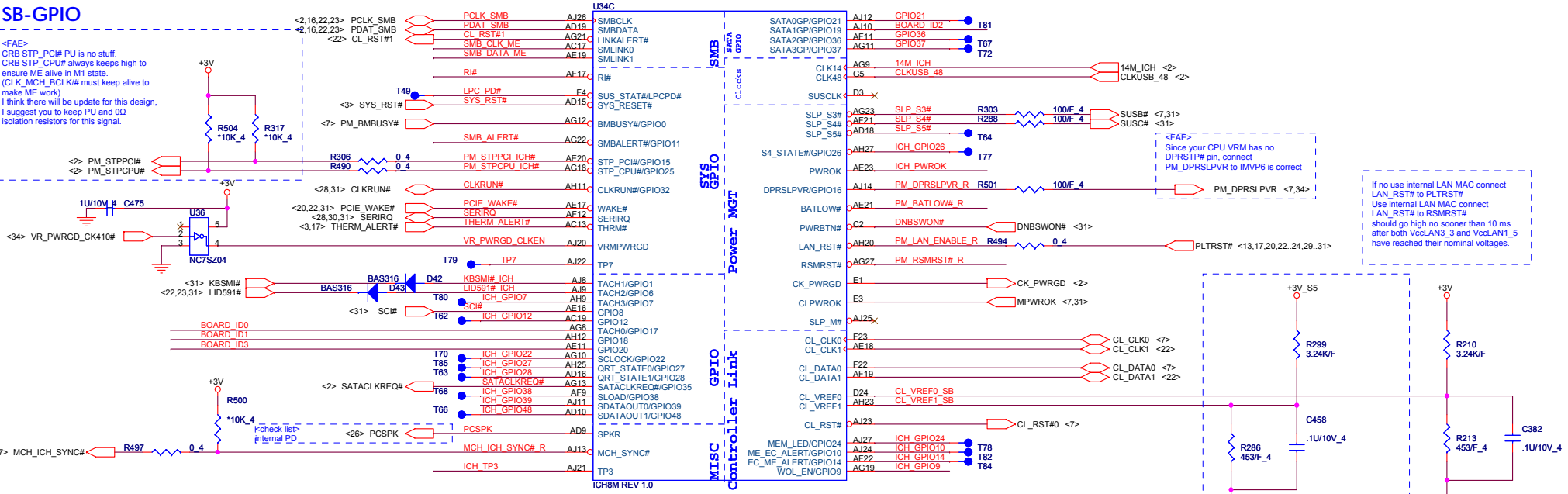
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PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M PCIE/PC/USB(2/4)	E
Date:	Monday, May 07, 2007	Sheet 13 of 38

SB-GPIO

<FAE>
 CRB STP_CPU# PU is no stuff.
 CRB STP_CPU# always keeps high to ensure ME alive in M1 state.
 (CLK_MCH_BCLK# must keep alive to make ME work)
 I think there will be update for this design.
 I suggest you to keep PU and 0Ω isolation resistors for this signal.



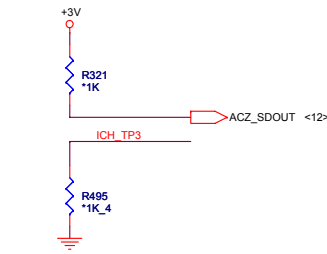
<FAE>
 Since your CPU VRM has no DPRSLP# pin, connect PM_DPRSLPVR to IMVP6 is correct

If no use internal LAN MAC connect LAN_RST# to PLTRST#
 Use internal LAN MAC connect LAN_RST# to RSMRST# should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

Controller Link 1 VREF for IAMT support only

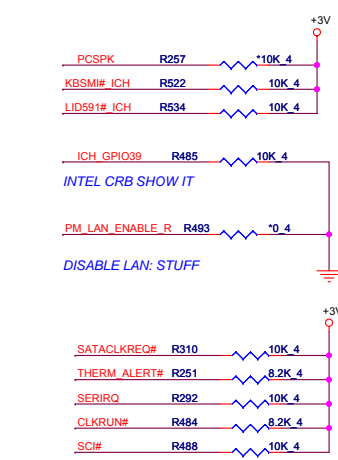
XOR Chain Entrance Strap

ICH_RSVD0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

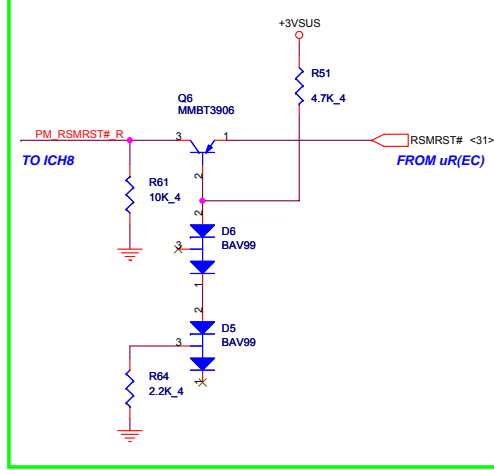


No Reboot strap

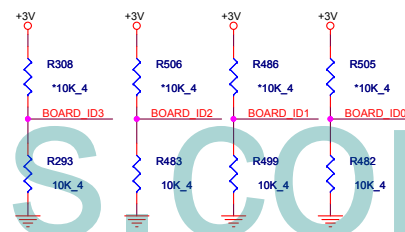
HDA_SPKR	Low = Default High = No Reboot
----------	-----------------------------------

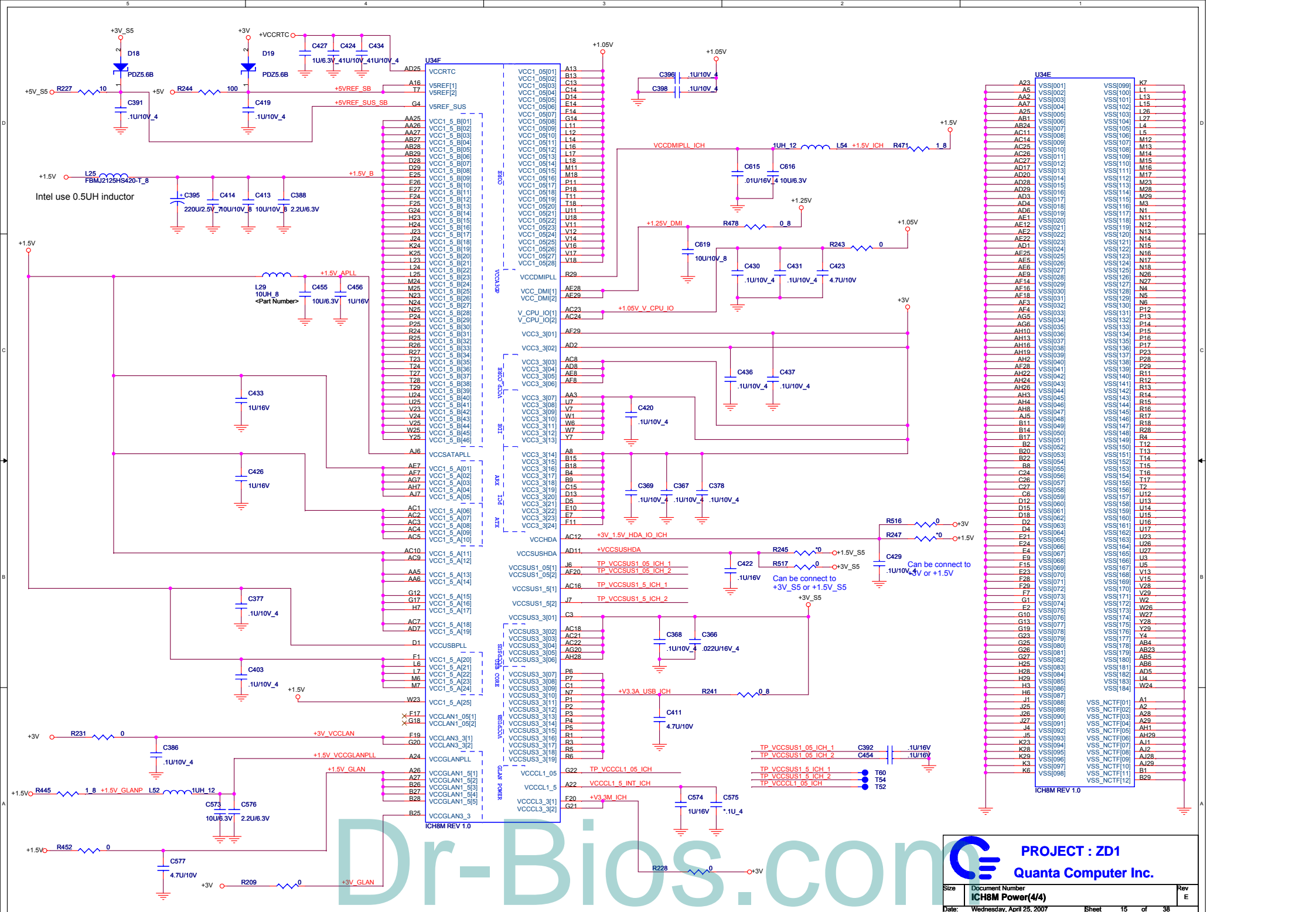


INTEL FAE (08/17)
 Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)



Board ID	ID3	ID2	ID1	ID0
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

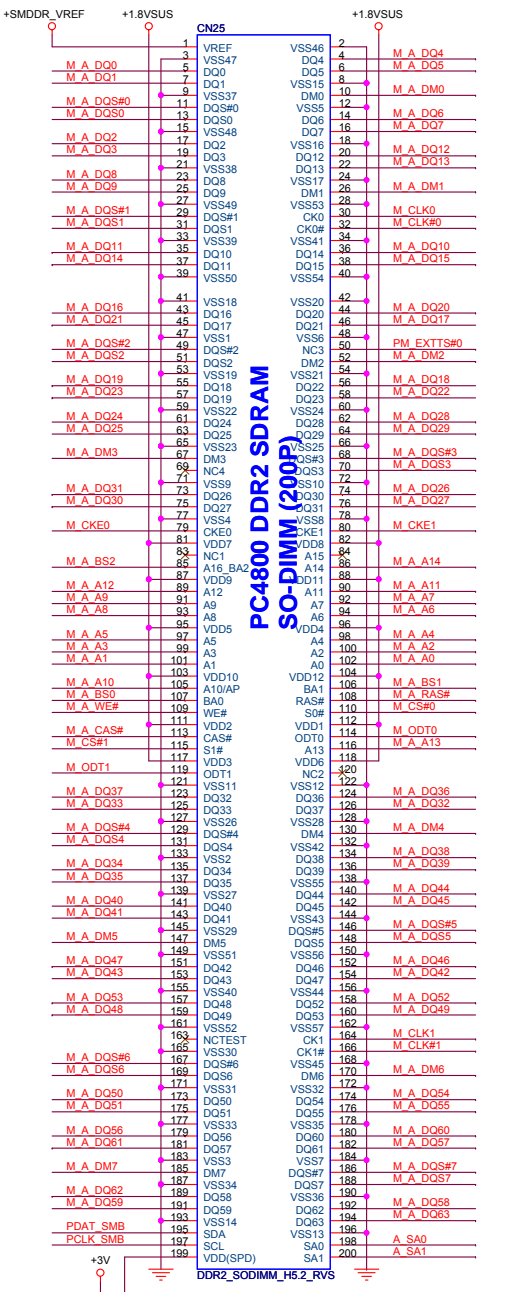




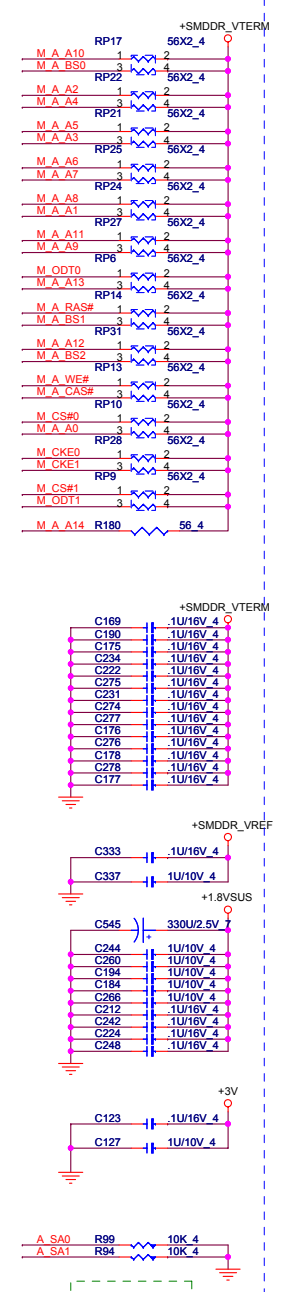
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PROJECT : ZD1
Quanta Computer Inc.

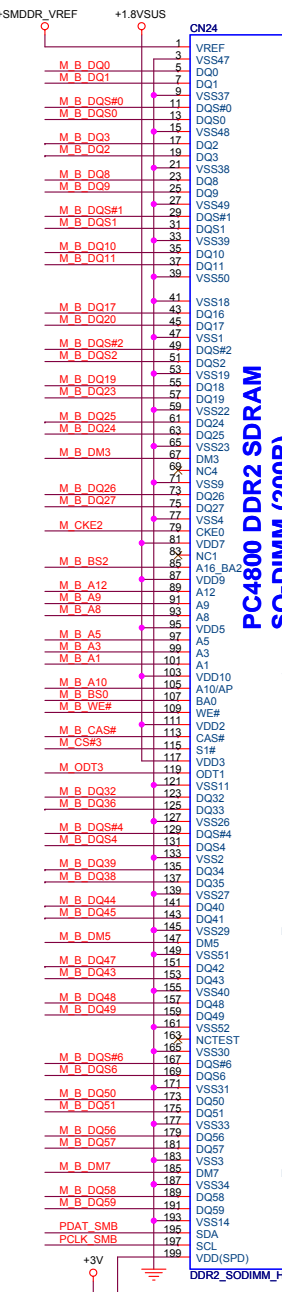
Size	Document Number	Rev
	ICH8M Power(4/4)	E
Date:	Wednesday, April 25, 2007	Sheet 15 of 38



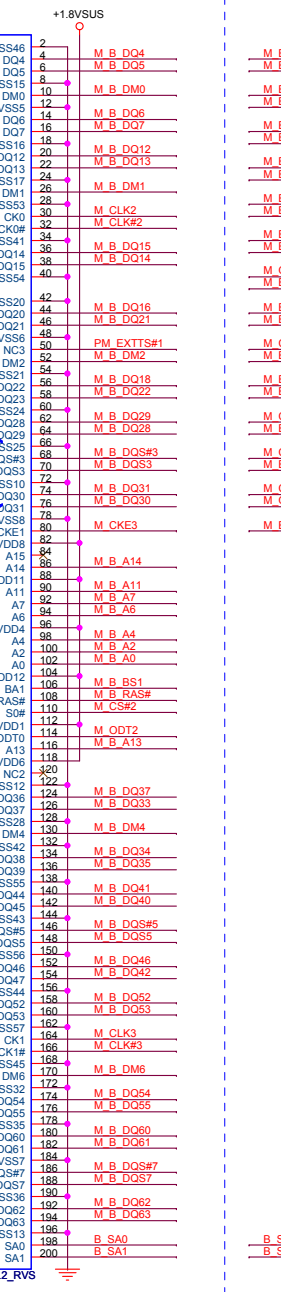
SO-DIMM0 SMbus address A0



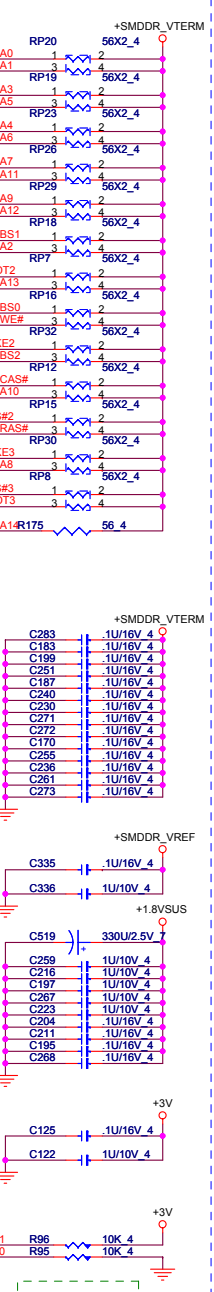
SO-DIMM1 SMbus address A2



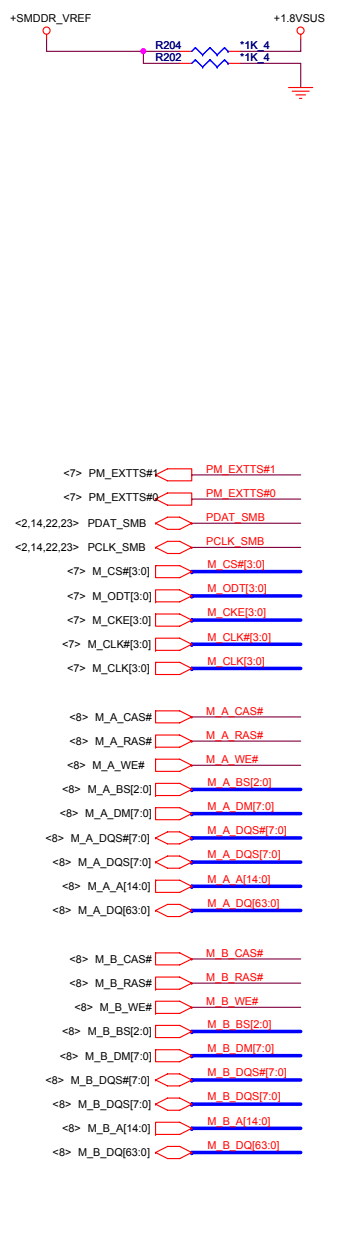
SO-DIMM1 SMbus address A2

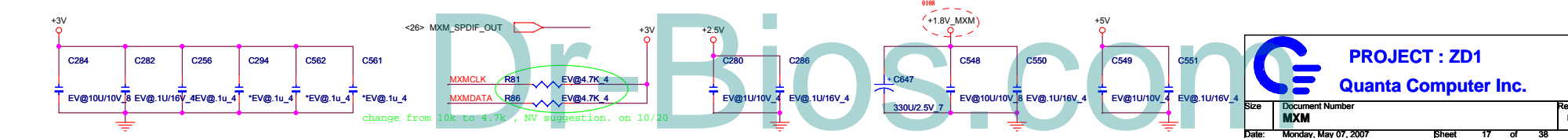
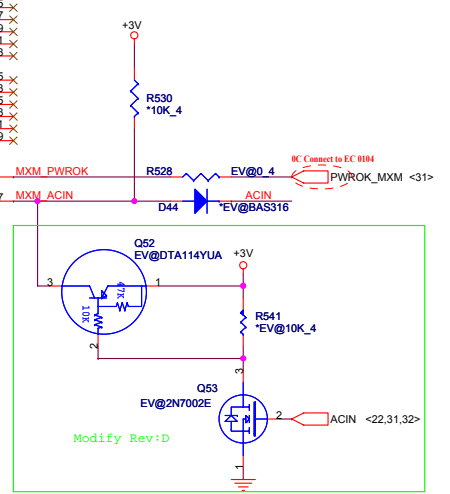
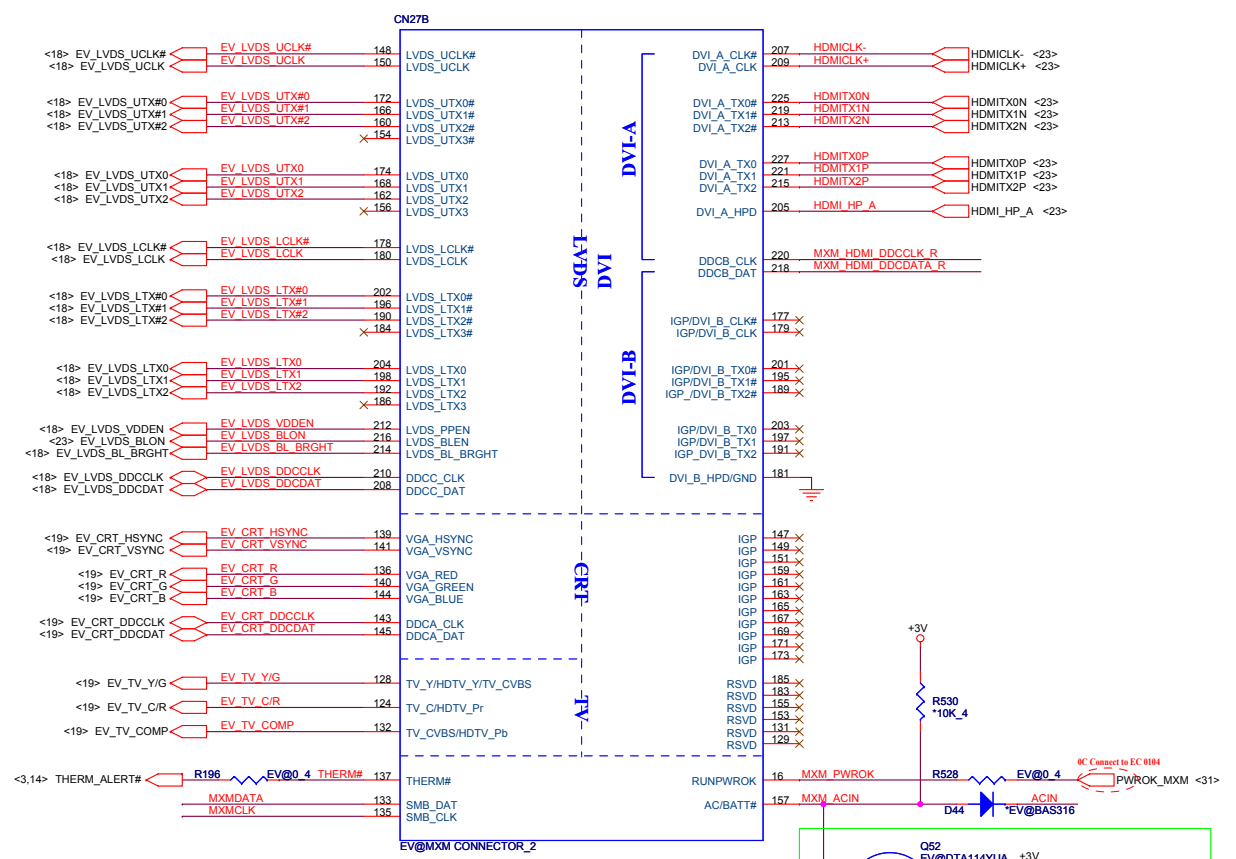
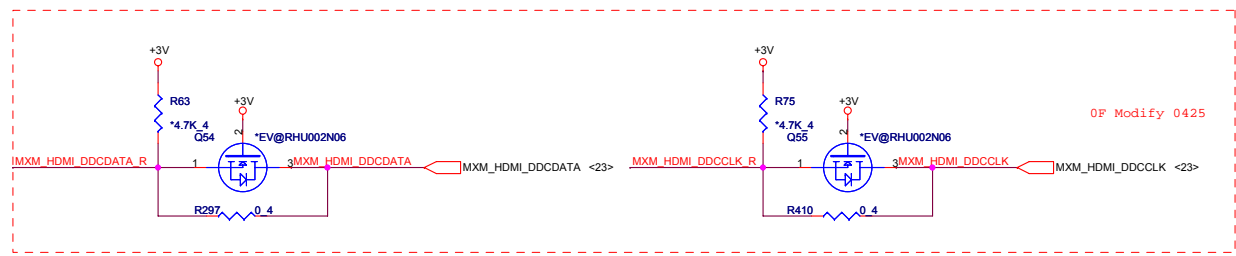
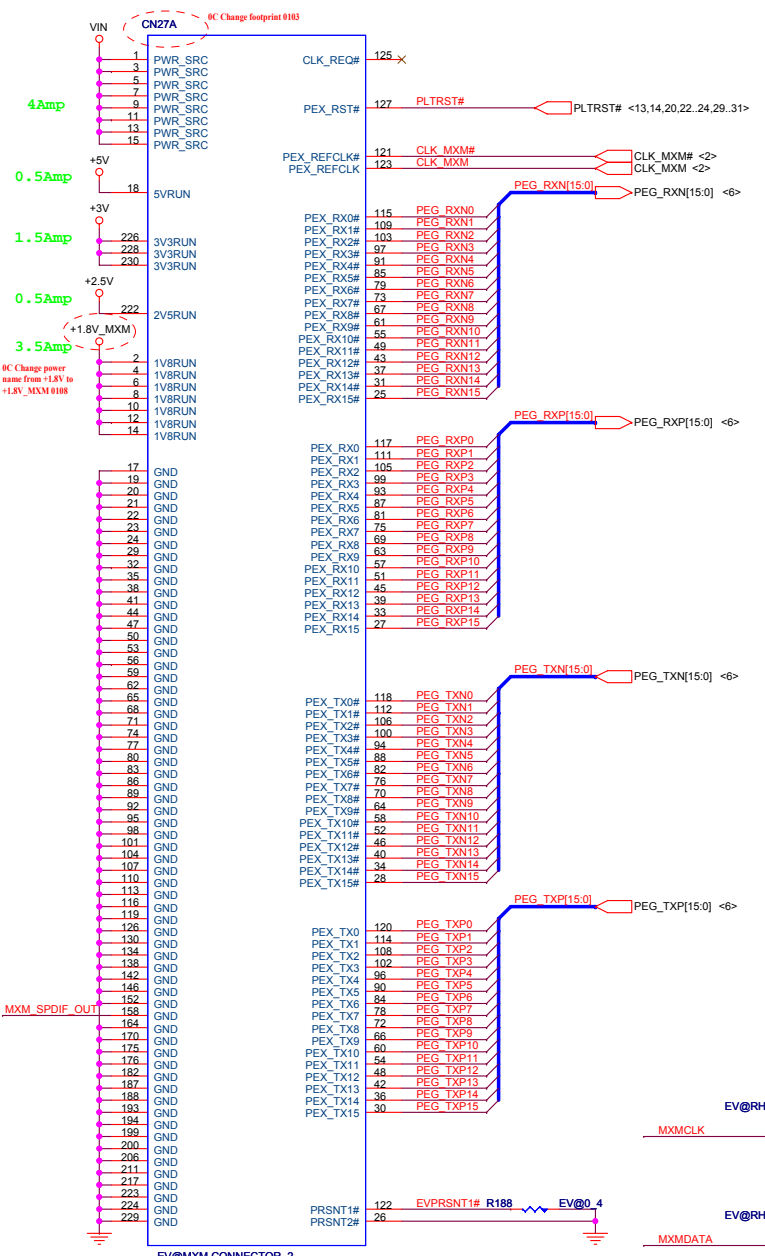


SO-DIMM1 SMbus address A1



SO-DIMM1 SMbus address A1

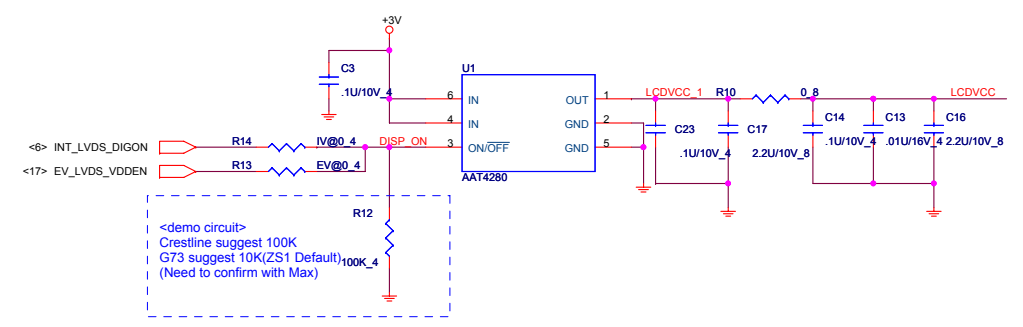
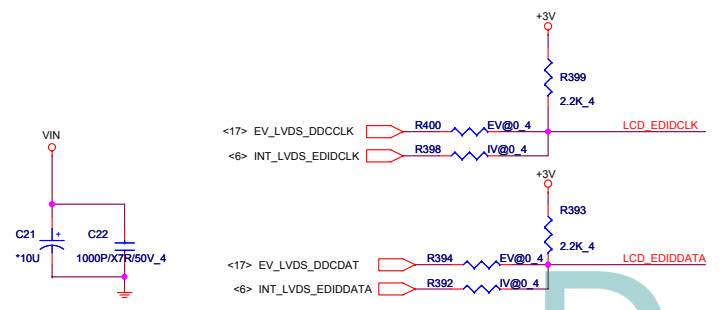
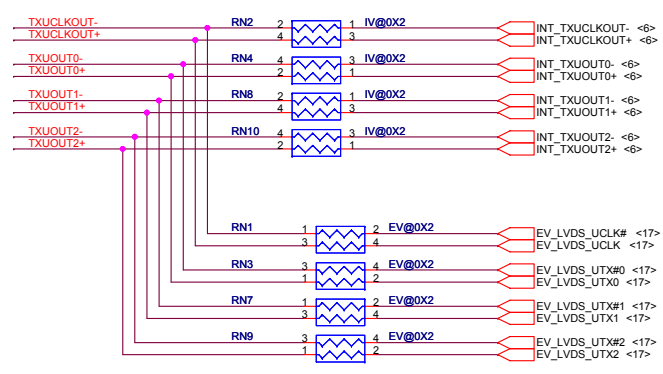
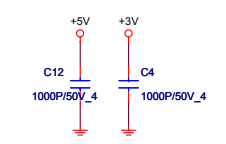
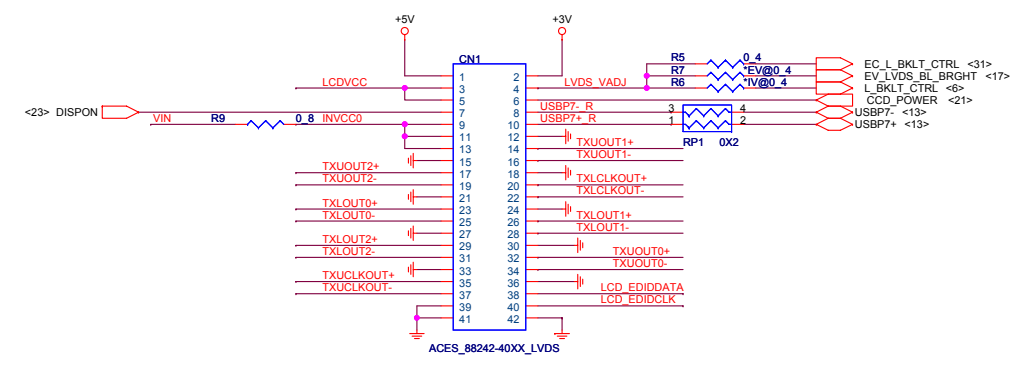
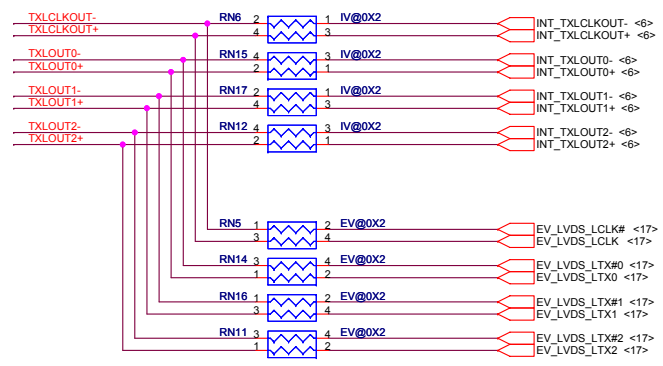




PROJECT : ZD1
Quanta Computer Inc.

Size: Document Number
MXM

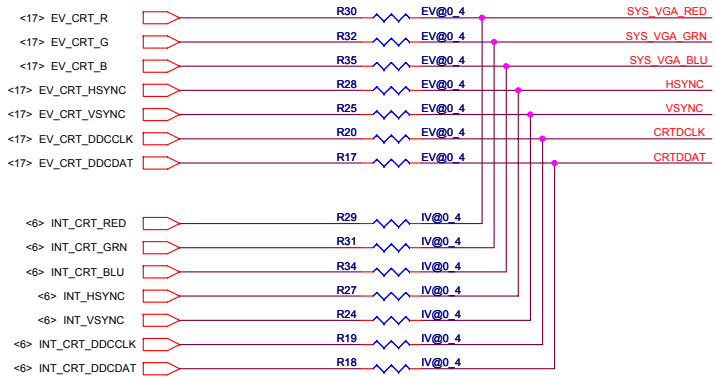
Date: Monday, May 07, 2007 Sheet 17 of 38 Rev E



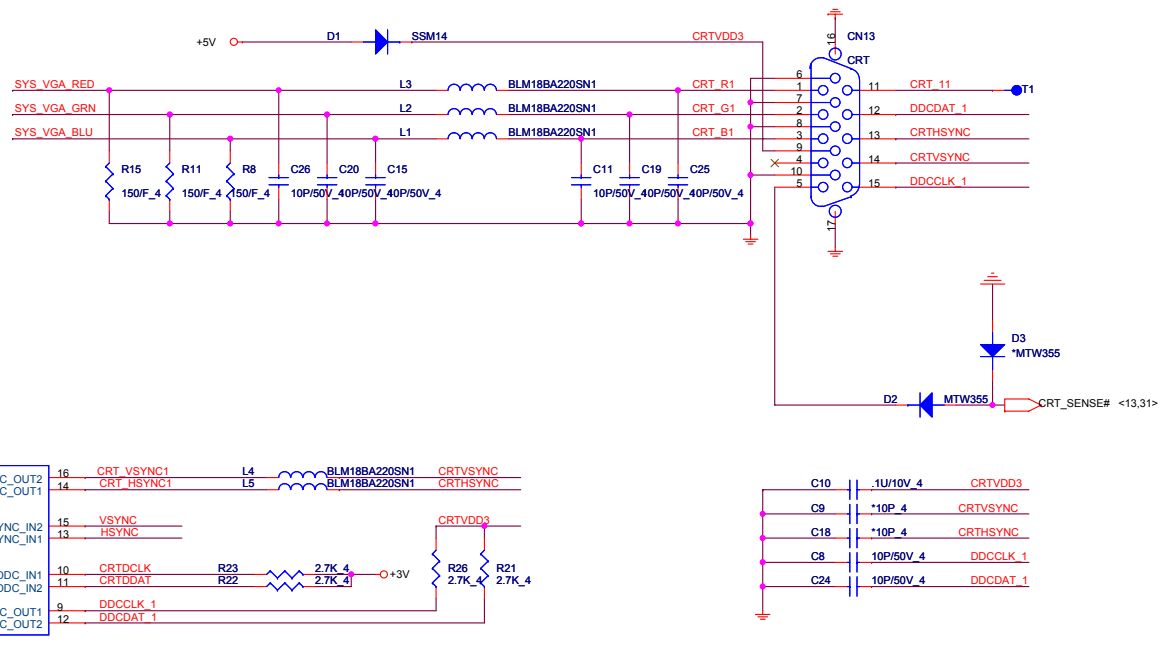
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PROJECT : ZD1
Quanta Computer Inc.
 Size Document Number
LVDS
 Date: Monday, May 07, 2007 Sheet 18 of 38 Rev E

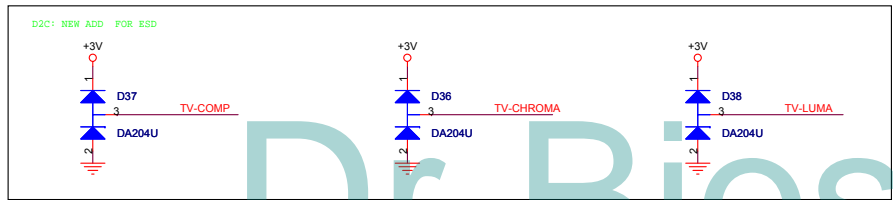
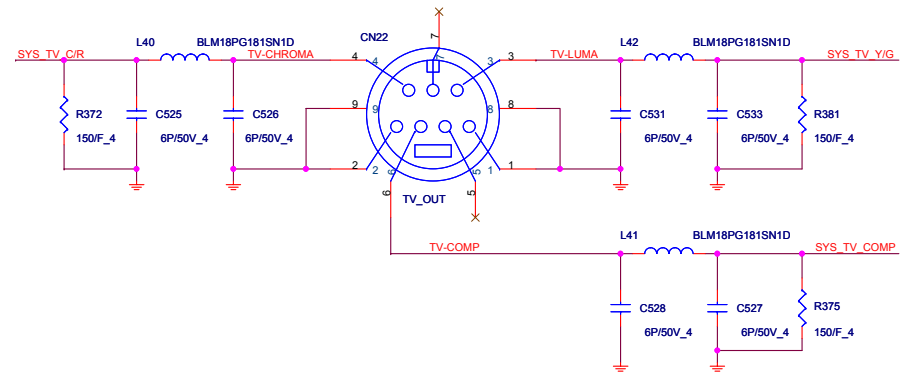
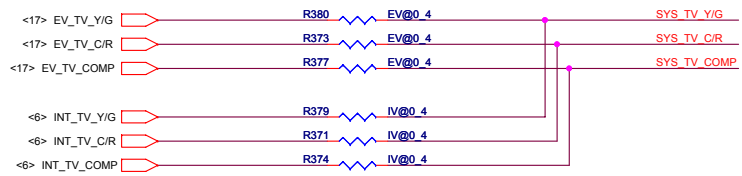
CRT Select



CRT CONNECTOR AND ESD

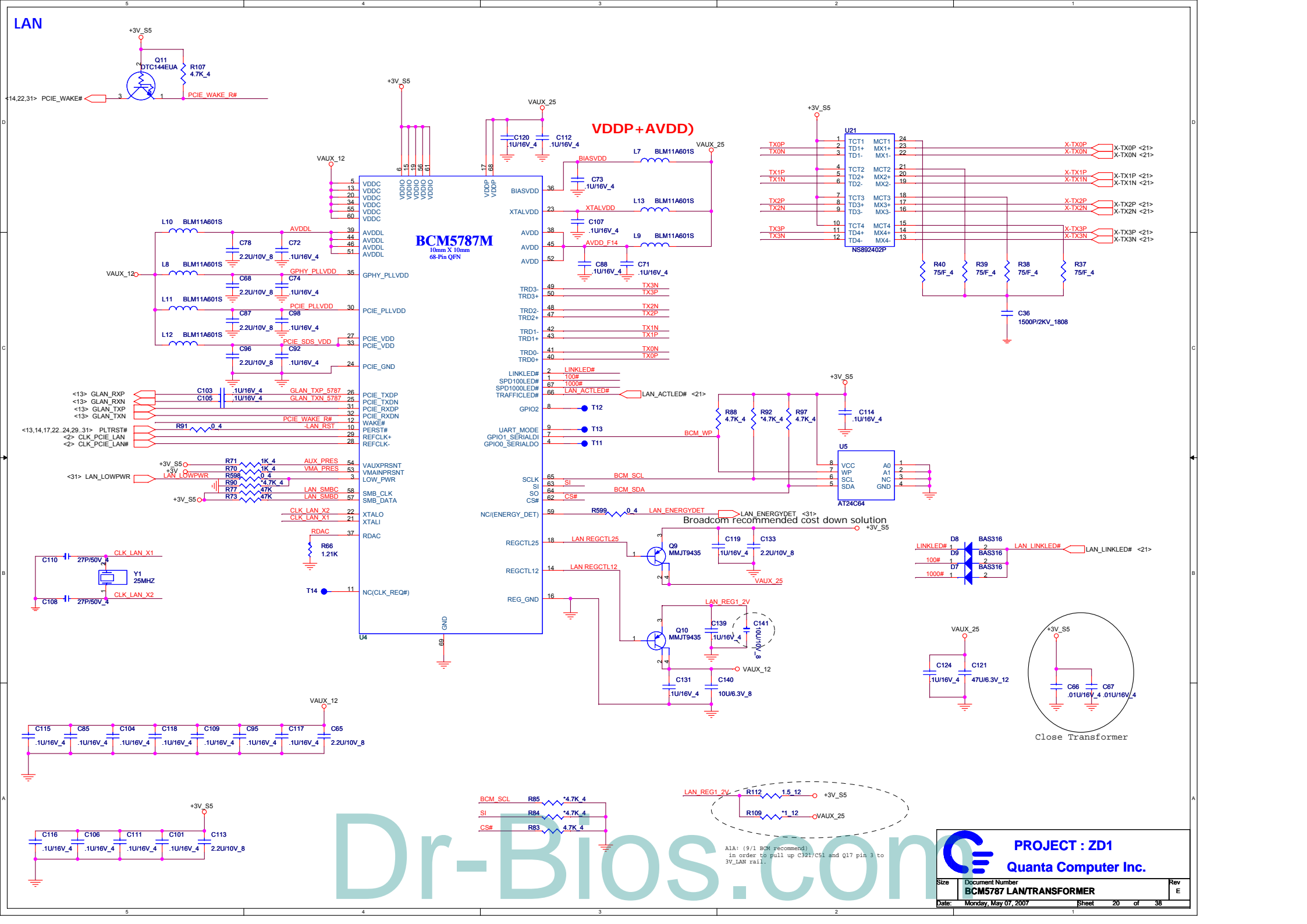


TV Out (SVHS) MiniDIN 7-pin

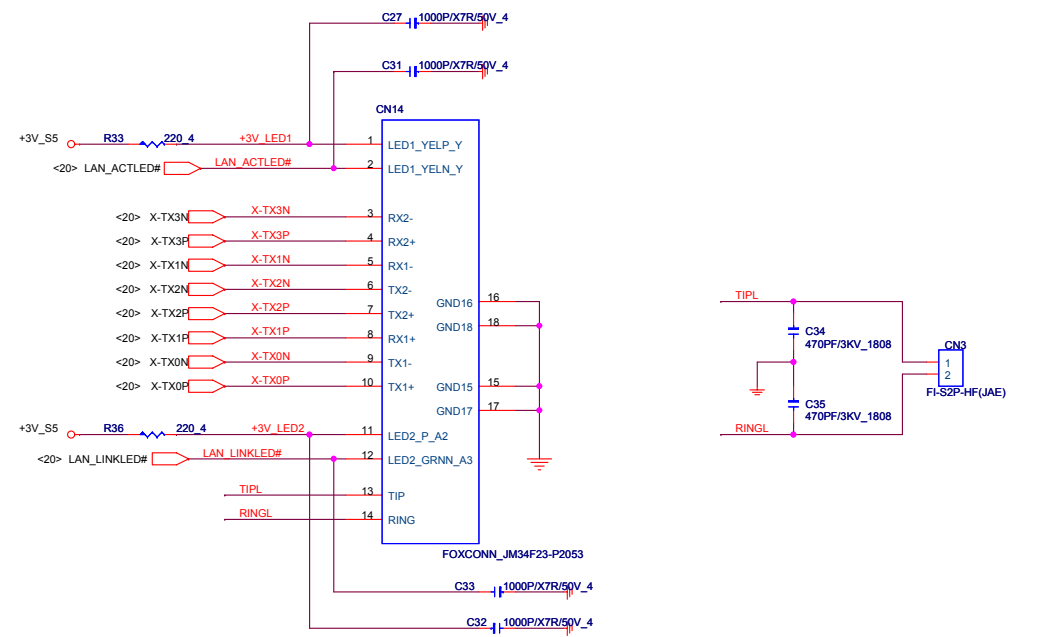


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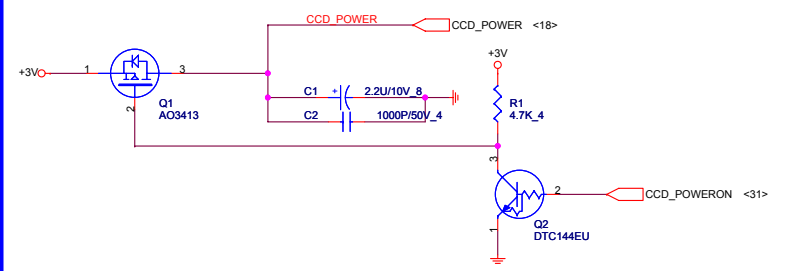
PROJECT : ZD1
Quanta Computer Inc.
 Size: Document Number
CRT/VOUT
 Date: Monday, May 07, 2007 Sheet 19 of 38 Rev E



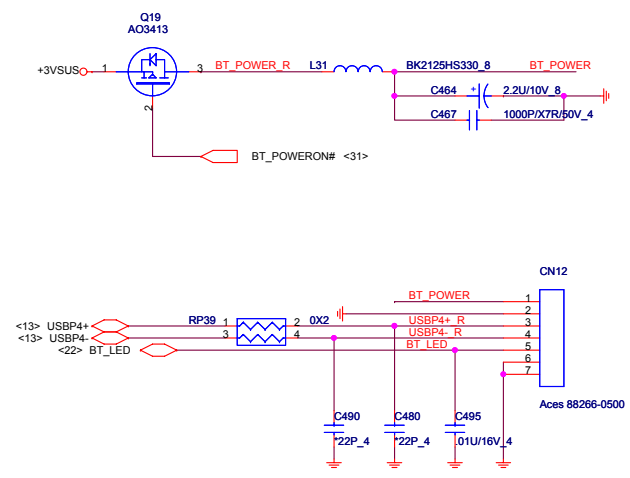
RJ45-11



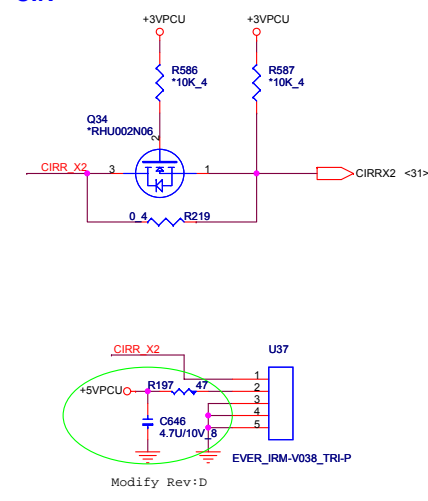
CAMERA MODULE CONNECTOR



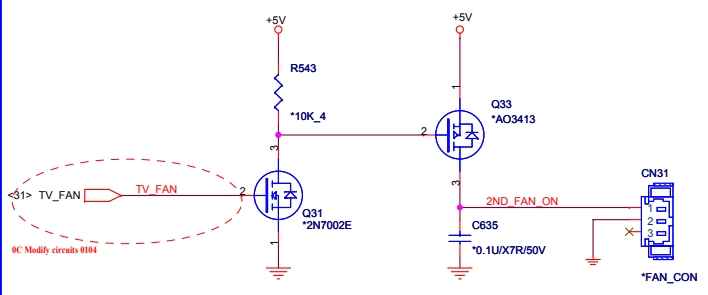
BLUETOOTH MODULE CONNECTOR



CIR



2nd FAN

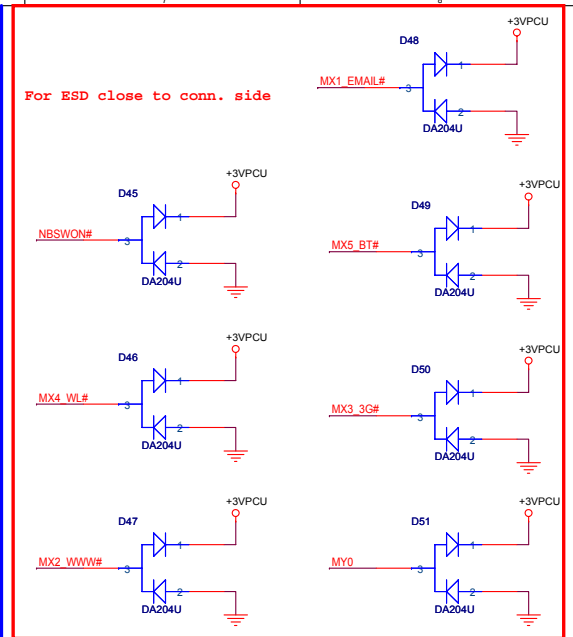
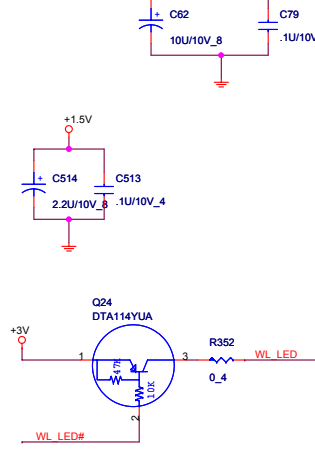
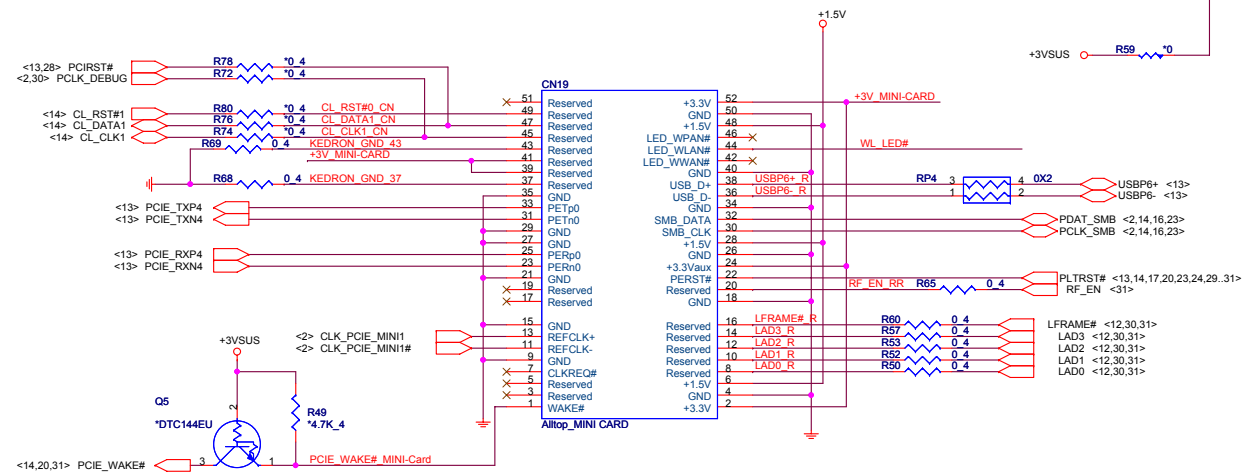


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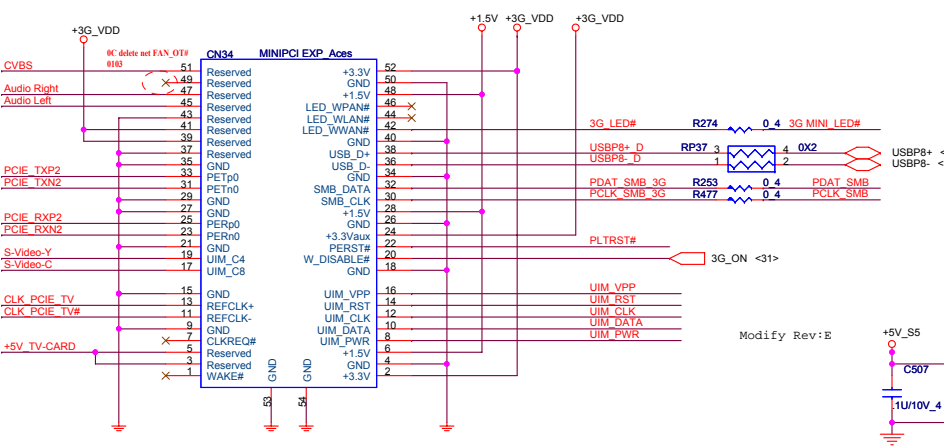
PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	BT/CCD/RJ45-11/CIR/2nd FAN	E
Date:	Monday, May 07, 2007	Sheet 21 of 38

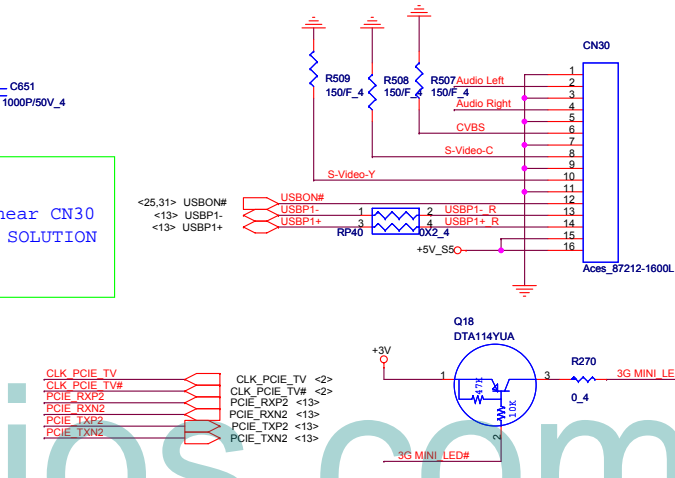
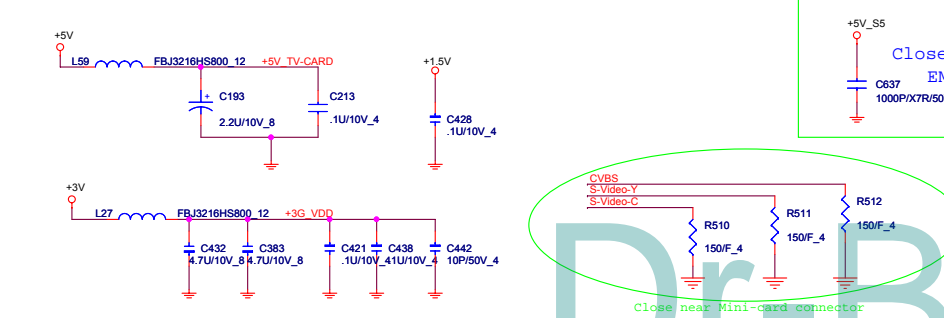
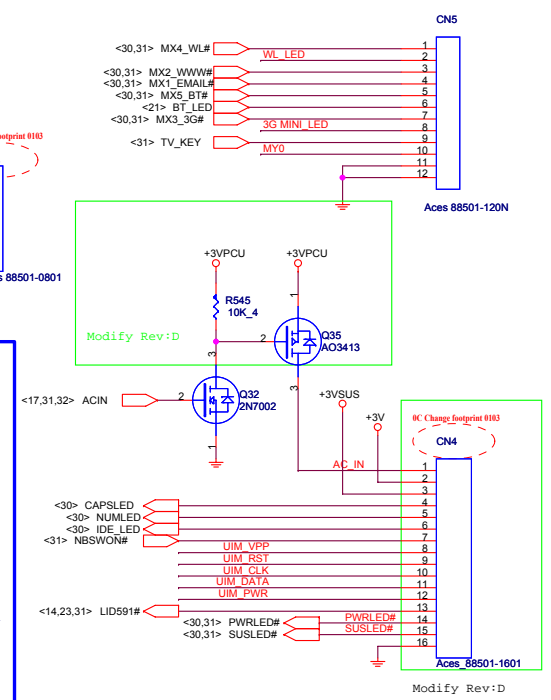
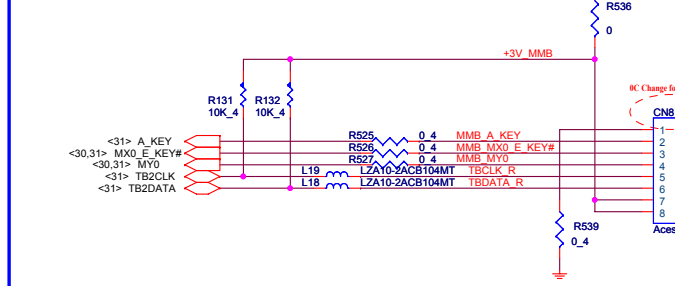
MINI-Card



3G/TV MINI CARD



Media Key

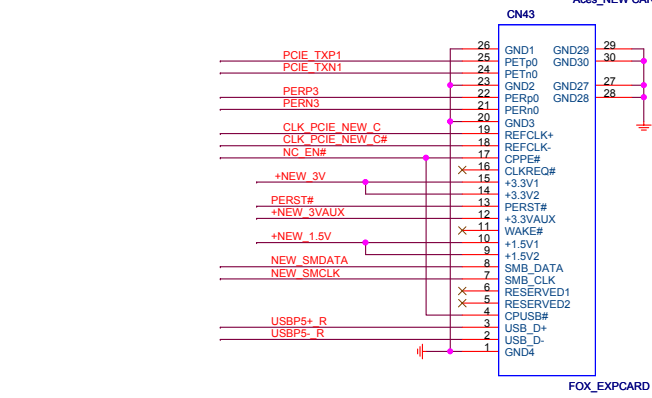
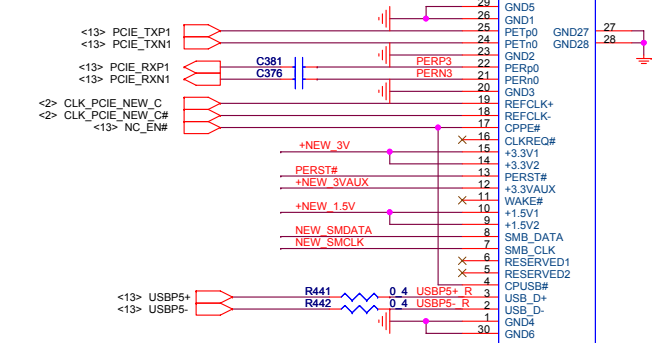


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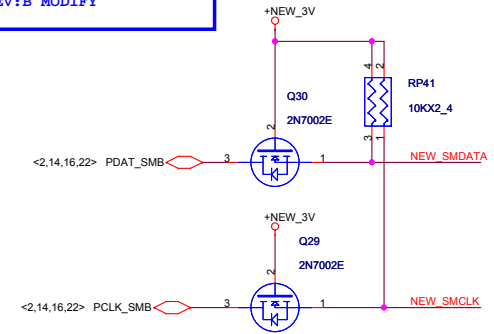
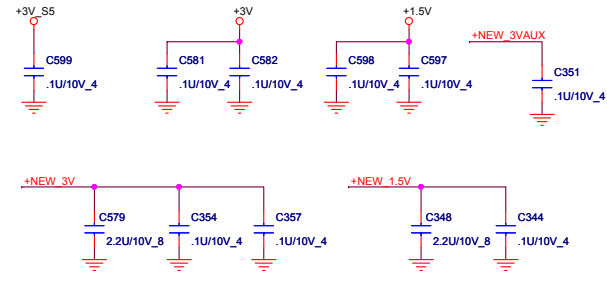
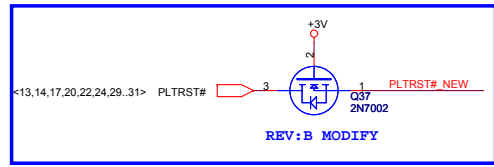
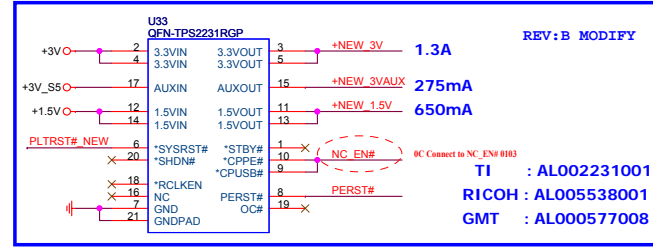
PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
Date: Monday, May 07, 2007	MINI PCI-E card/3G/TV/Media Key	E
Sheet	22	of 38

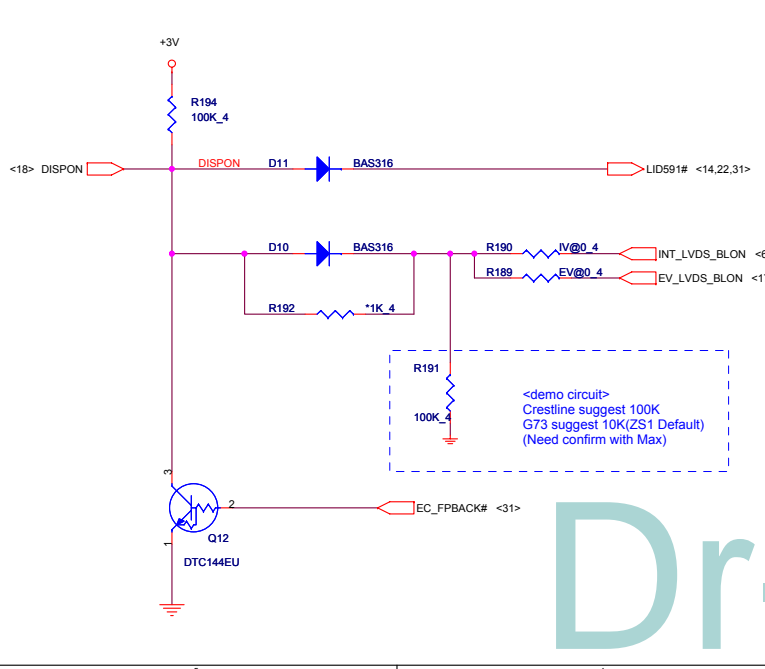
New card



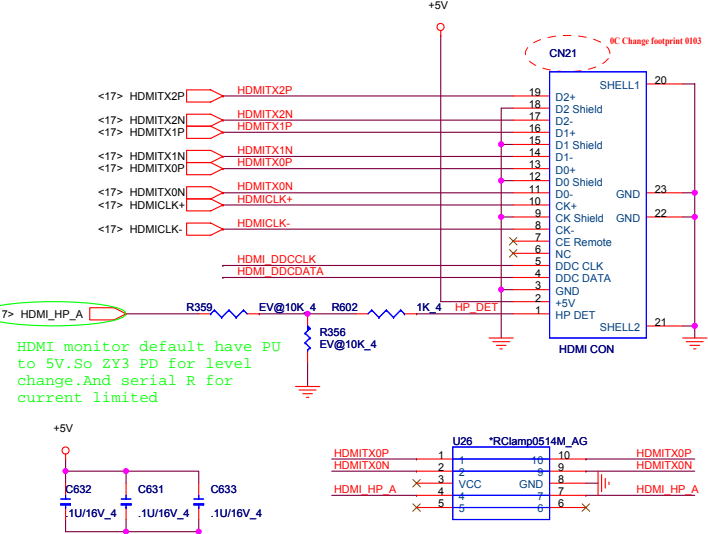
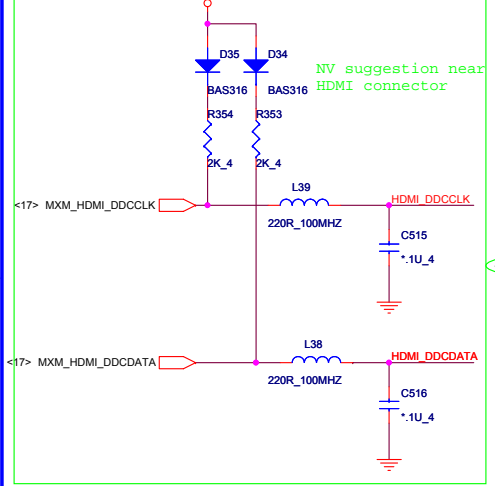
NEW CARD'S POWER SWITCH



LID SWITCH



HDMI

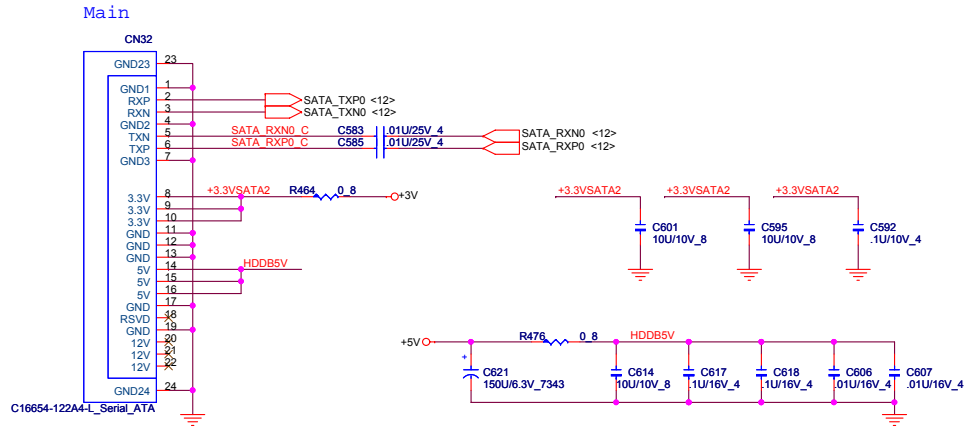
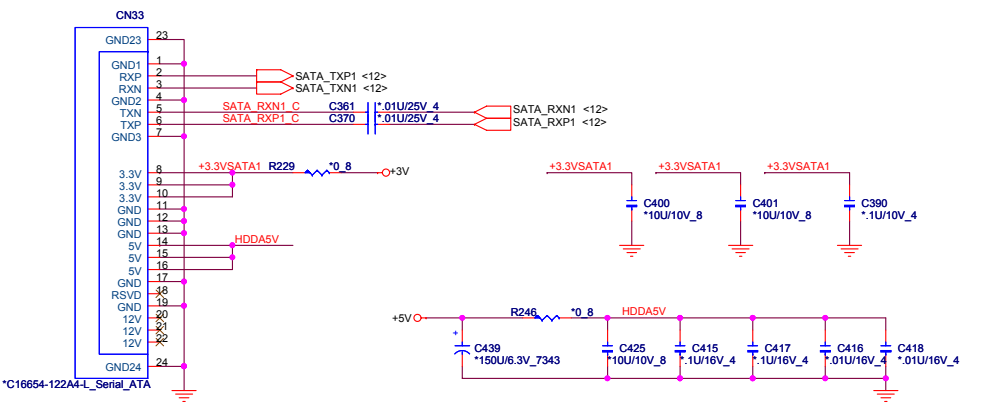


HDMI TX2P	1	10	HDMI TX2N	10	HDMI CLK+	1	10	HDMI CLK-	10
HDMI TX2N	2	9	HDMI TX1P	9	HDMI CLK-	2	9	HDMI CLK+	9
HDMI TX1P	3	8	HDMI TX1N	8	HDMI DDCCLK	3	8	HDMI DDCDATA	8
HDMI TX1N	4	7	HDMI TX2P	7	HDMI DDCDATA	4	7	HDMI DDCCLK	7
	5	6		6		5	6		6

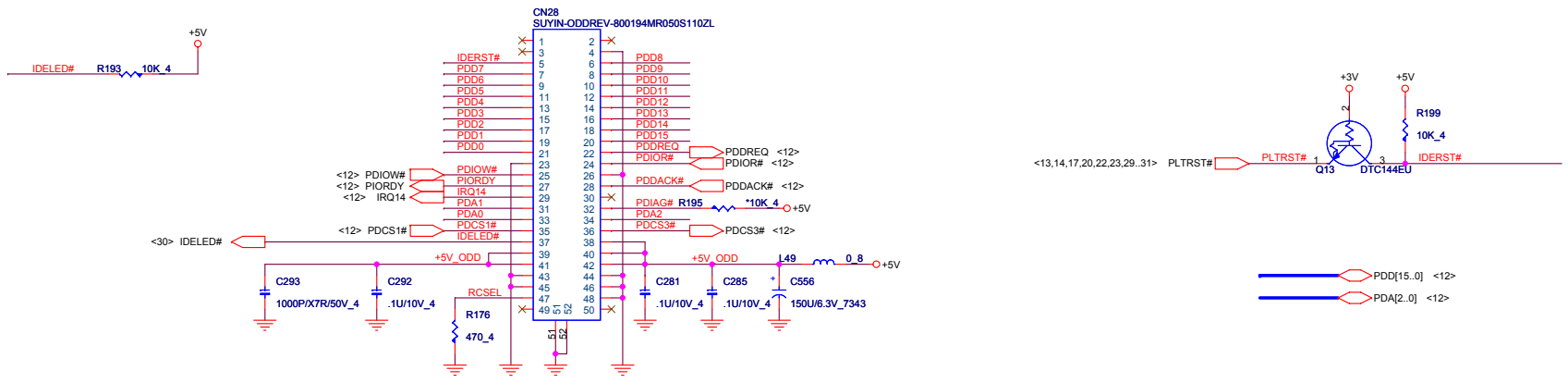
PROJECT : ZD1
Quanta Computer Inc.
 Size Document Number
NEW CARD/HDMI/LID
 Date: Monday, May 07, 2007 Sheet 23 of 38 Rev E

SATA HDD1

SATA HDD2



ODD (PATA)

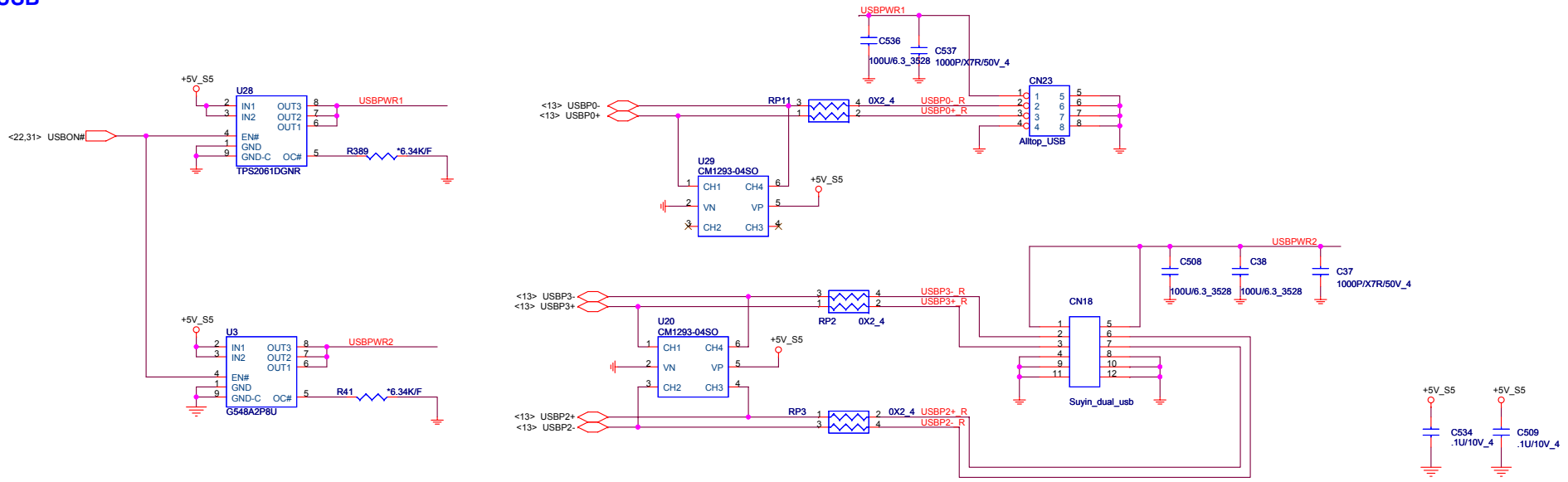


Dr-Bios.com

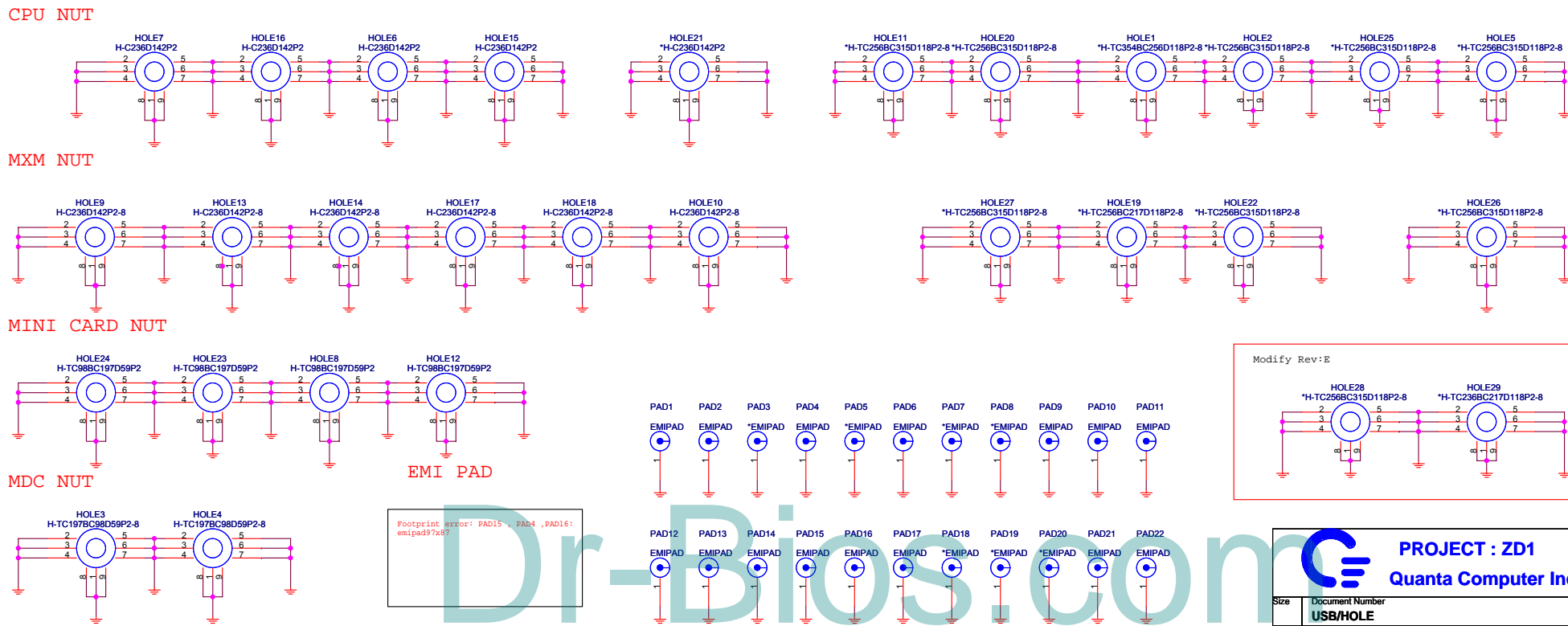
PROJECT : ZD1
 Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD & PATA-ODD	E
Date:	Monday, May 07, 2007	Sheet 24 of 38

USB



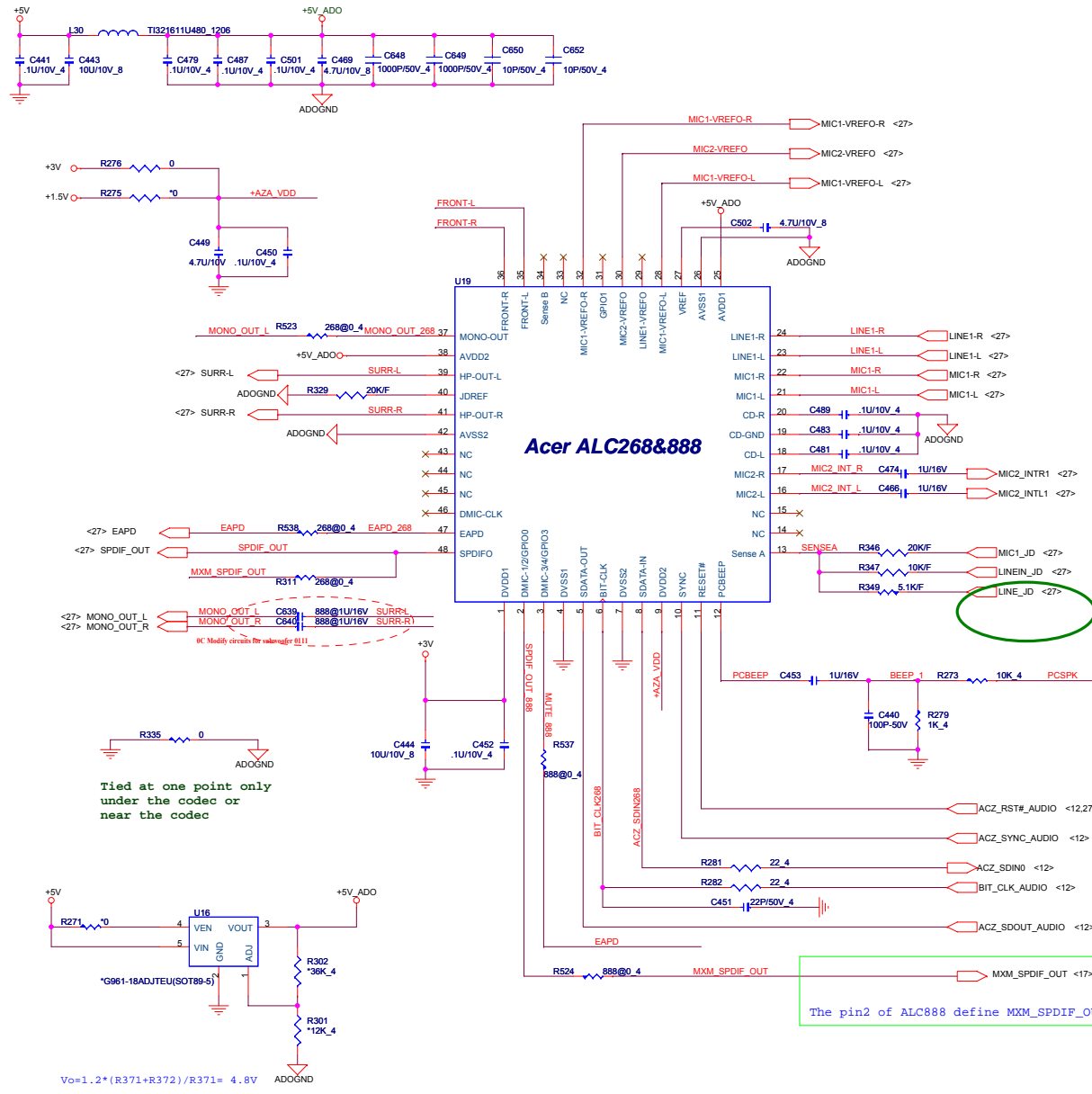
HOLES



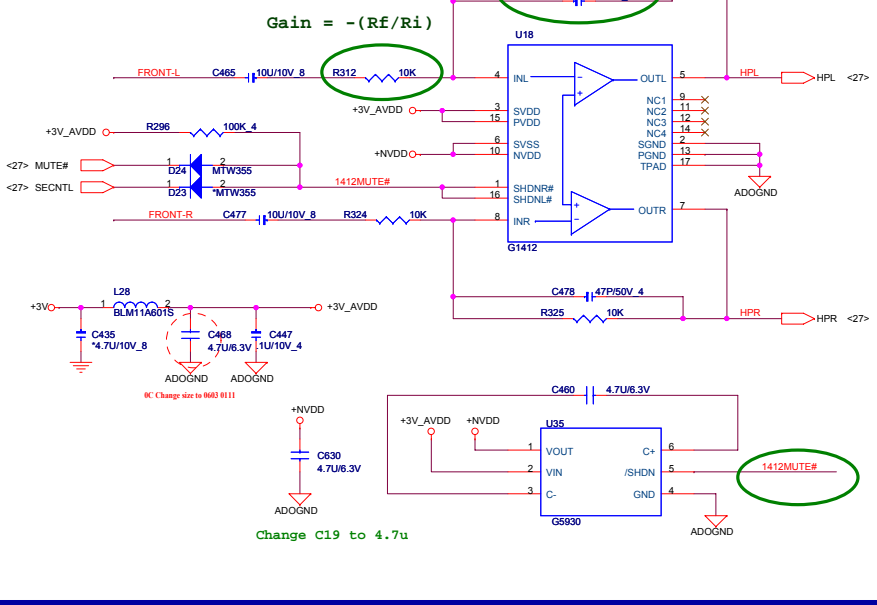
PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	USB/HOLE	E
Date:	Monday, May 07, 2007	Sheet 25 of 38

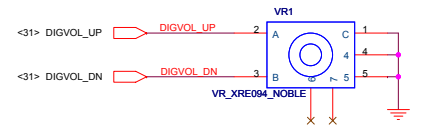
CODEC (ALC268)



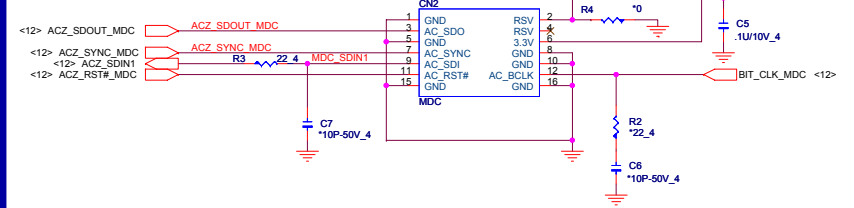
LINE OUT Amplifier



VR



MDC



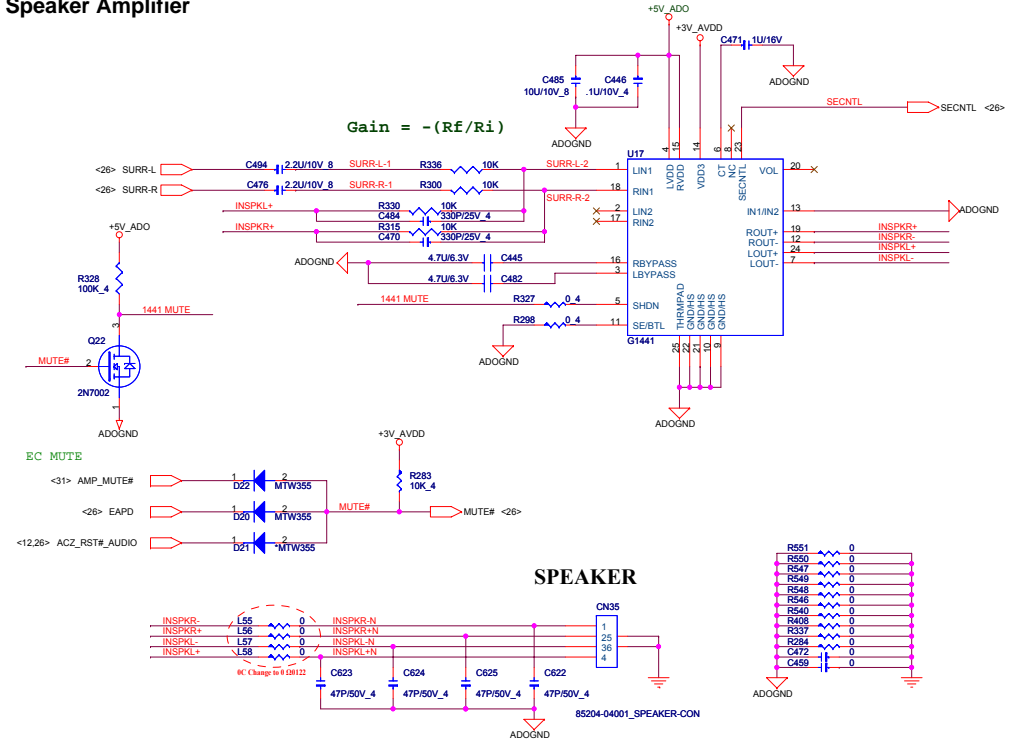
The pin2 of ALC888 define MXM_SPDIF_OUT

Tied at one point only under the codec or near the codec

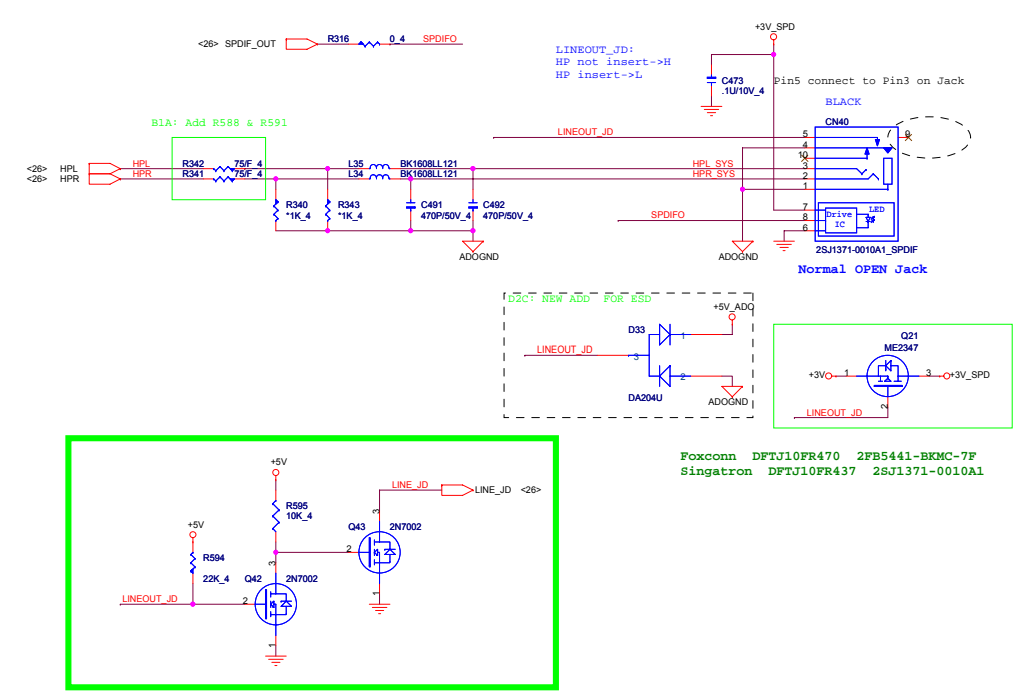
PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	REALTEK ALC268&888/MDC/VR	E
Date:	Monday, May 07, 2007	Sheet 26 of 38

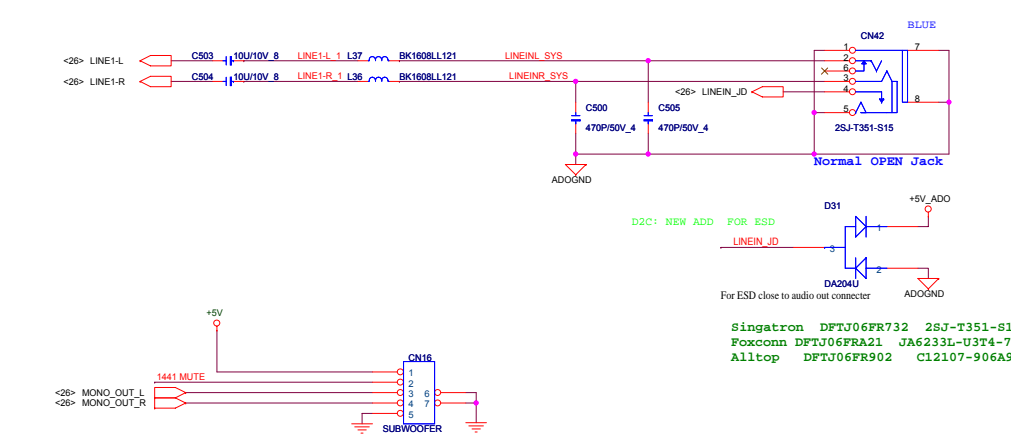
Speaker Amplifier



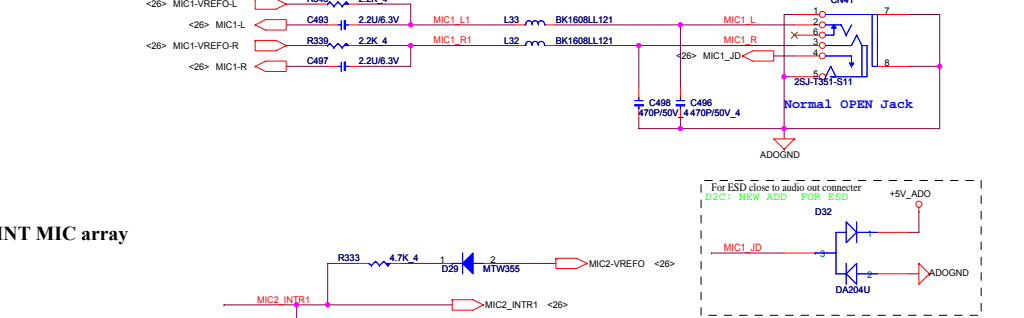
SYSTEM LINE OUT/SPDIF



SYSTEM LINE IN/SUBWOOFER

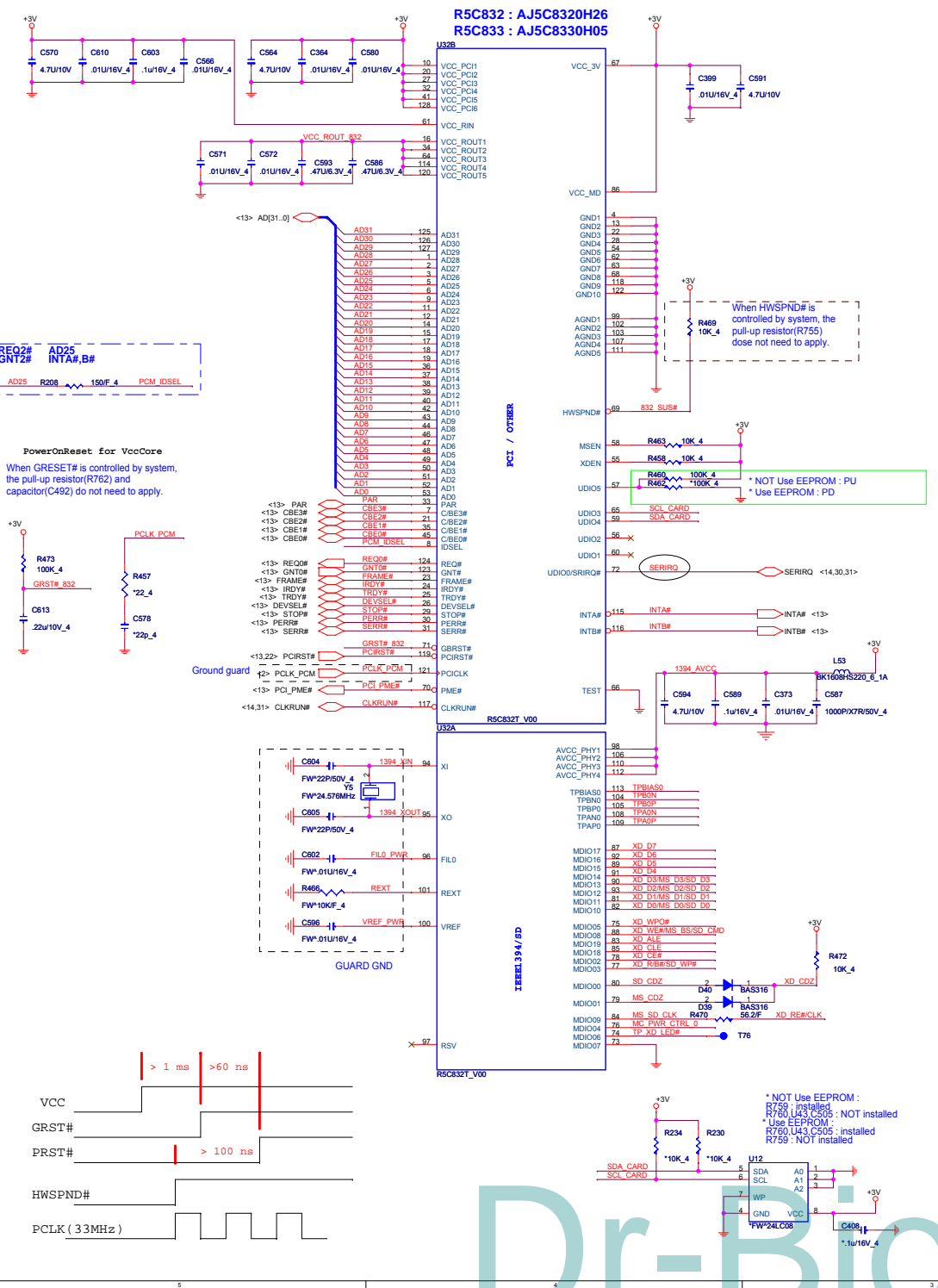


MIC

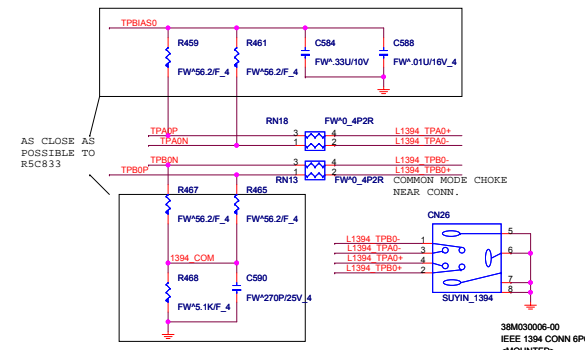


INT MIC array



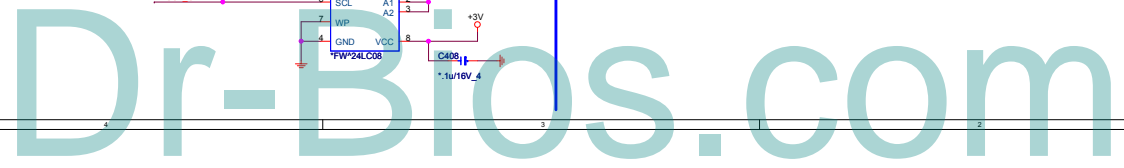
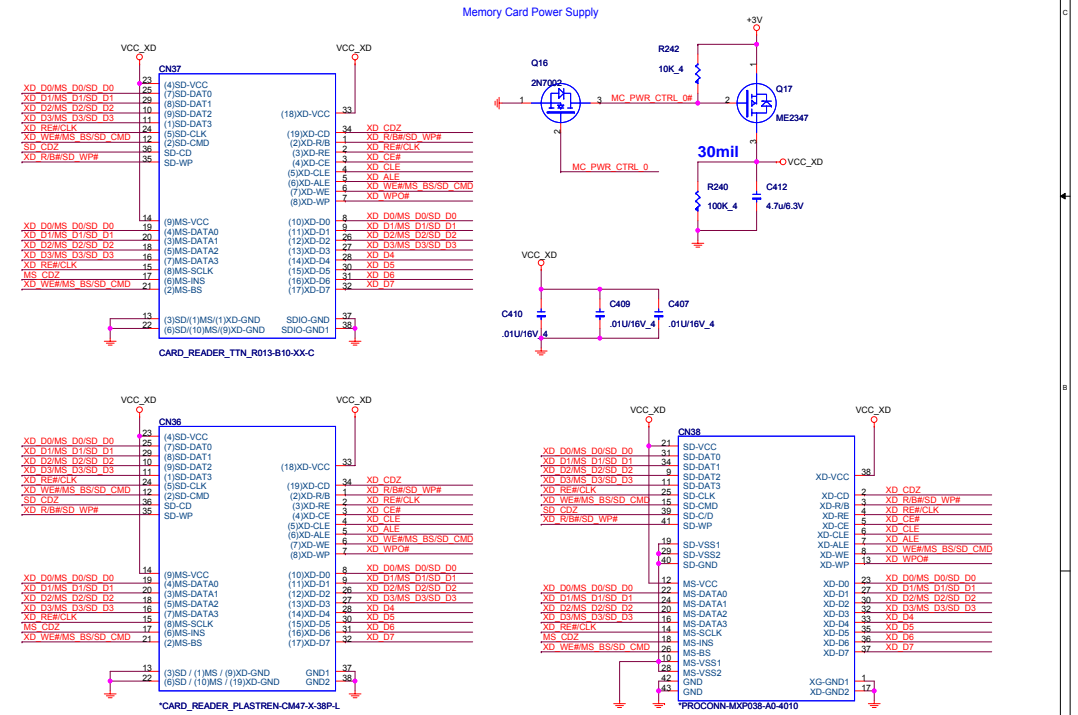


1394

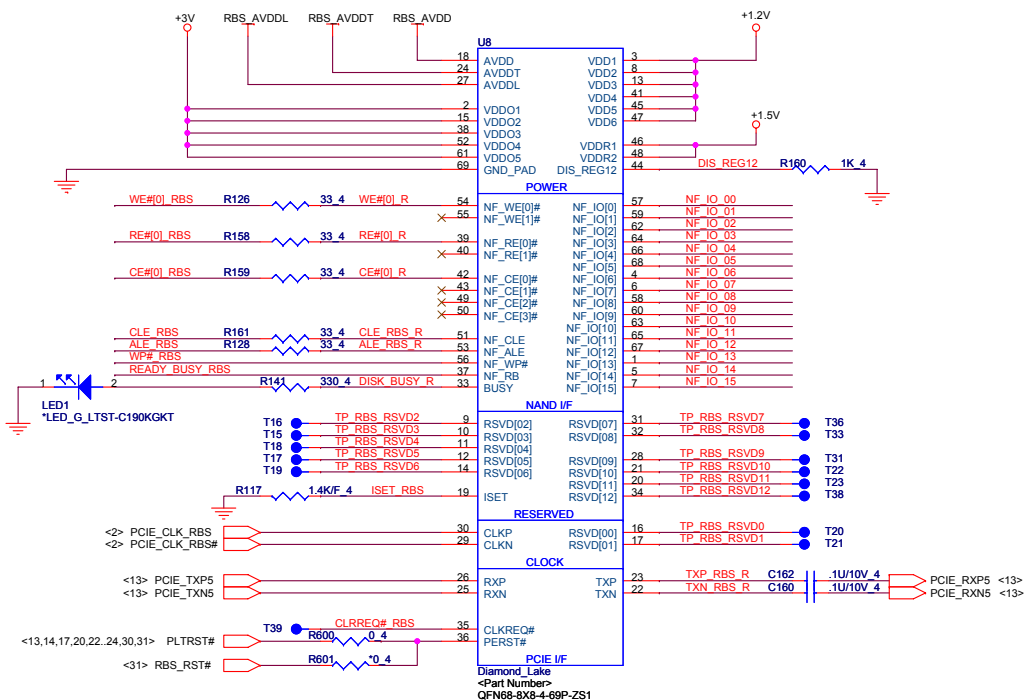


38M0006-00
 IEEE 1394 CONN 6POLE P/A 78756-1 DIP AMP
 <MOUNTED>

5 IN 1 CARD READER



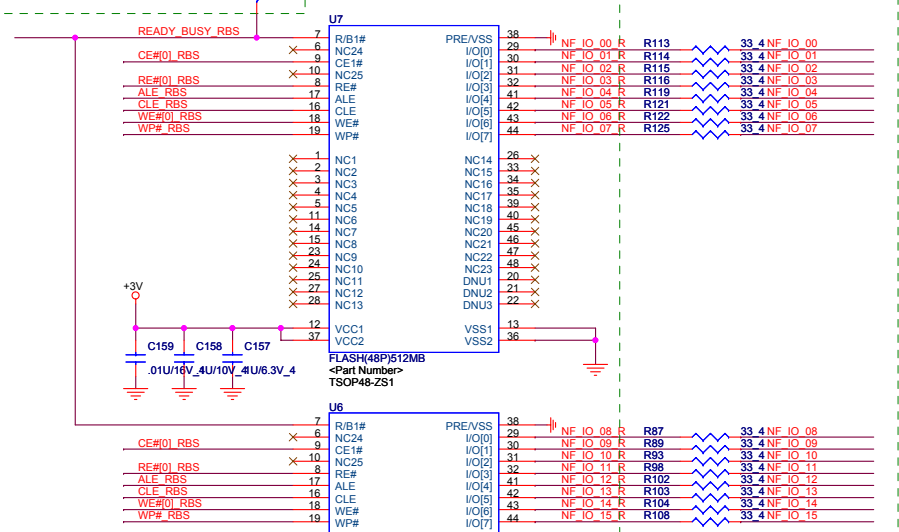
DIAMOND-LAKE ASIC



INTEL NAND FLASH

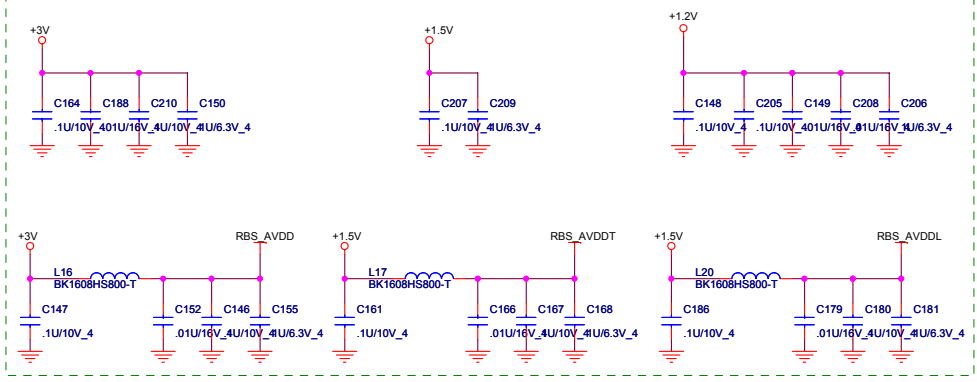
PLACE CLOSE TO NAND FLASH

PLACEMENT NOTE:
PLACE TERMINATION RESISTORS AT 10% TO 25% DISTANCE FROM NAND FLASH.



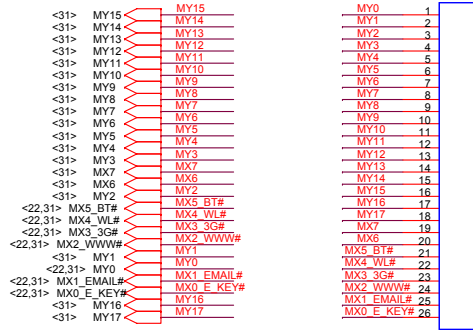
PLACE AS CLOSE AS POSSIBLE TO DIAMOND-LAKE ASIC.

STUFF: INDICATES A 2KB VIRTUAL PAGE => 256MB
DESTUFF: INDICATES A 4KB VIRTUAL PAGE => 512MB & 1024MB



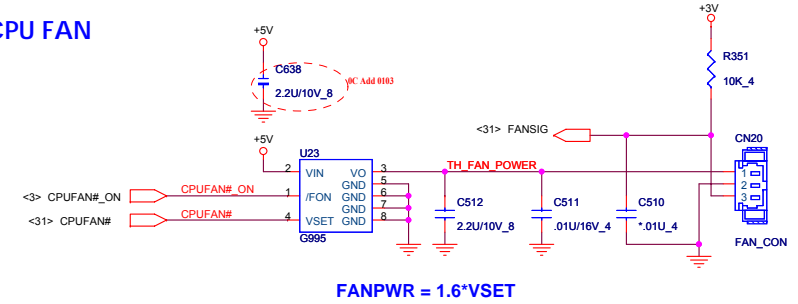
LAYOUT NOTE:
ANY VIA ADDED BENEATH THE NAND FLASH NEEDS TO HAVE A SOLDERMASK ON IT.

INT K/B

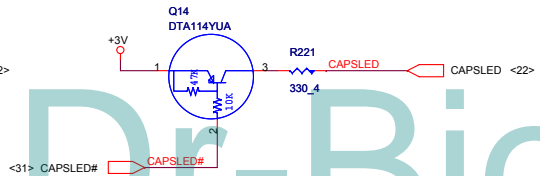
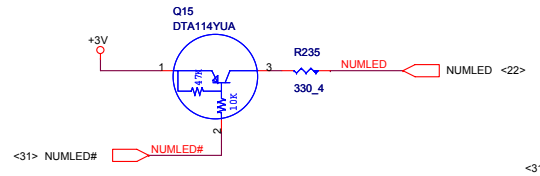
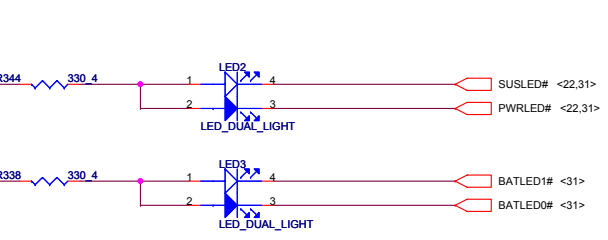
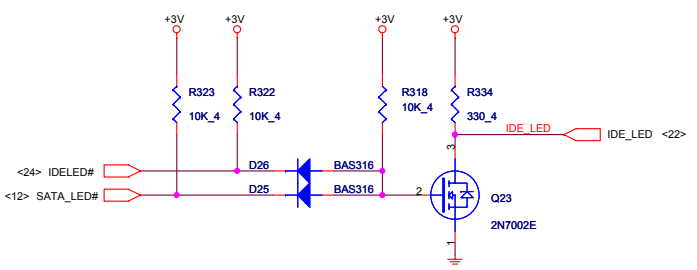


Acex 88502-2641

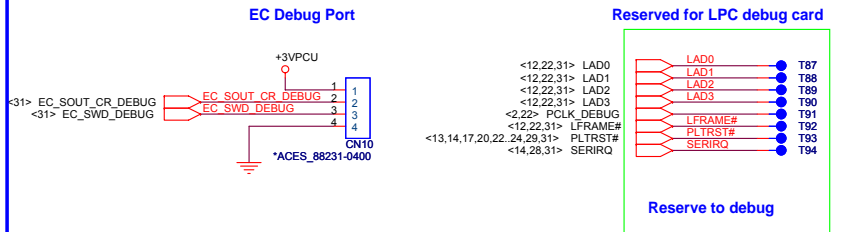
CPU FAN



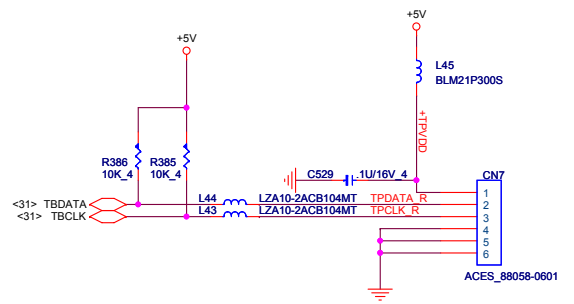
LED



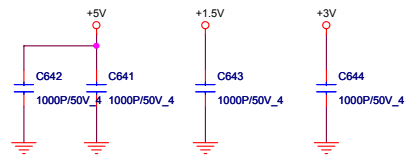
DEBUG PORT



T/P



EMI solution

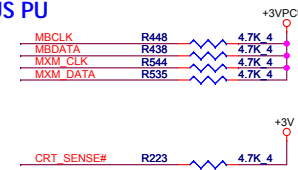


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PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	FAN,LED,KB,DEBUG PORT,TP	E
Date:	Monday, May 07, 2007	Sheet 30 of 38

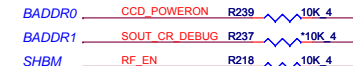
SM BUS PU



I/O ADDRESS SETTING

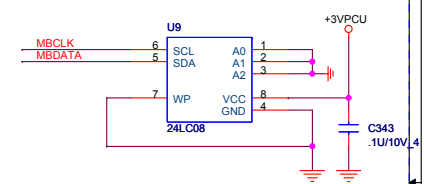
I/O Address	
BADDR1-0	Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHBM=0: Enable shared memory with host BIOS

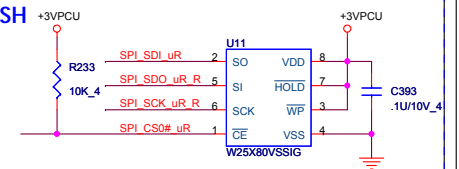


1/13 Confirm by vendor mail :
Disabled (*) if using FWH device on LPC.
Enabled (0) if using SPI flash for both system BIOS and EC firmware

ACER ID



SPI FLASH

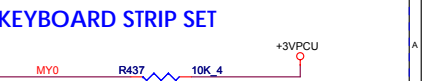


1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

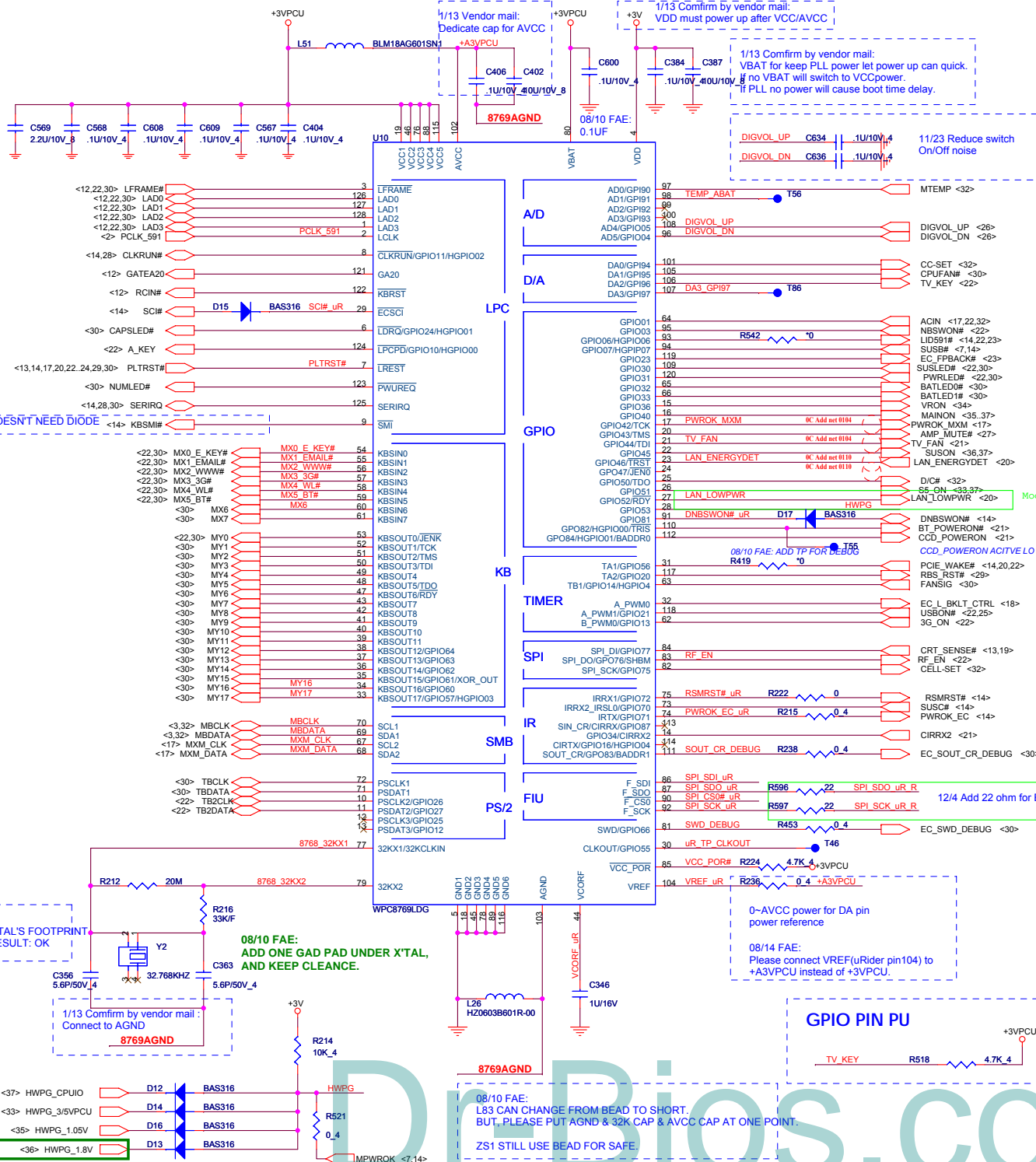
BUTTON ON KEYBOARD MATRIX



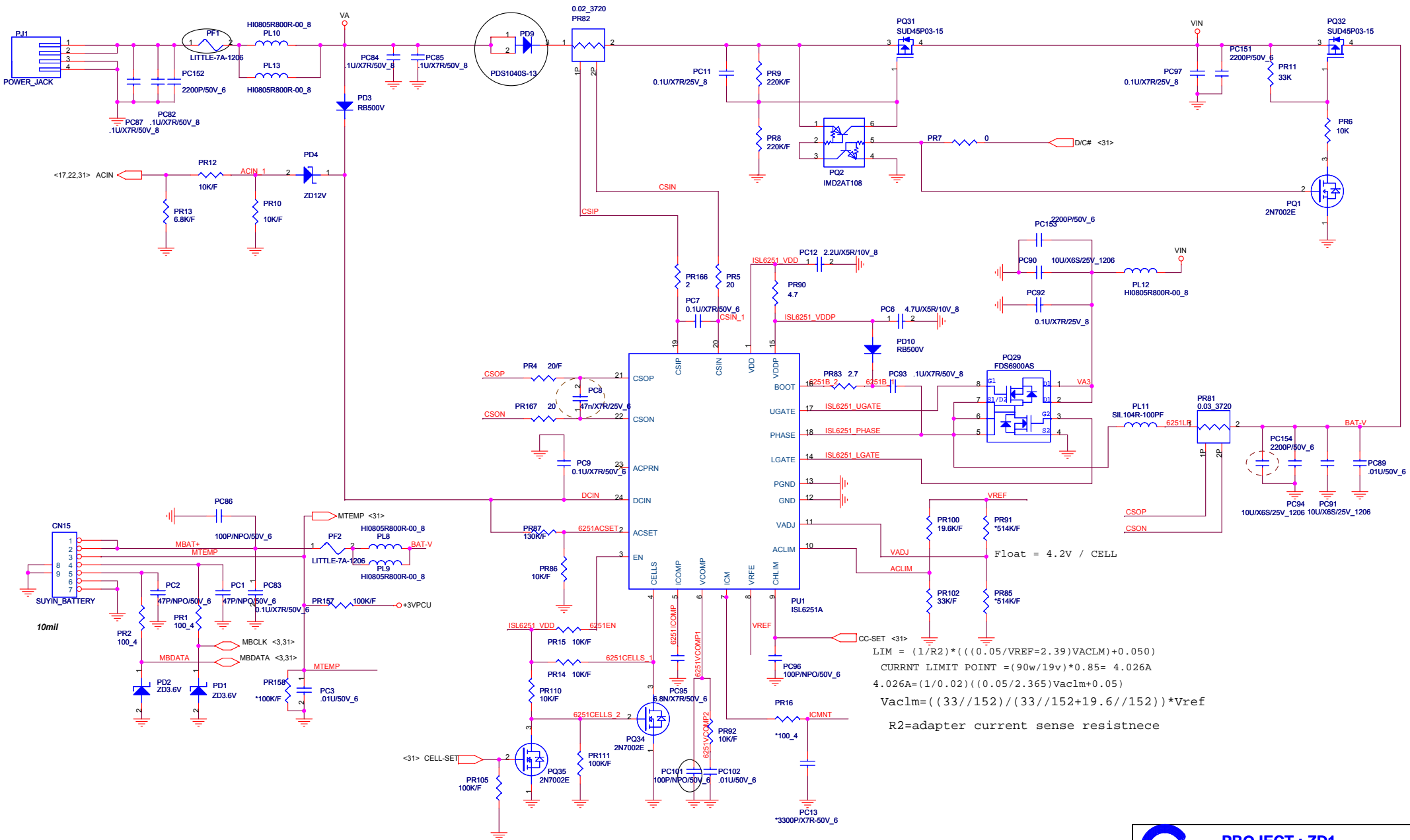
INTERNAL KEYBOARD STRIP SET



PROJECT : ZD1
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08/10 FAE:
L83 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.



CELL-SET = Hi -----> Cells = VDD ----->4S
 CELL-SET = Low -----> Cells = GND ----->3S

$$LIM = (1/R2) * (((0.05/VREF=2.39)VACLM)+0.050)$$

$$CURRENT LIMIT POINT = (90w/19v) * 0.85 = 4.026A$$

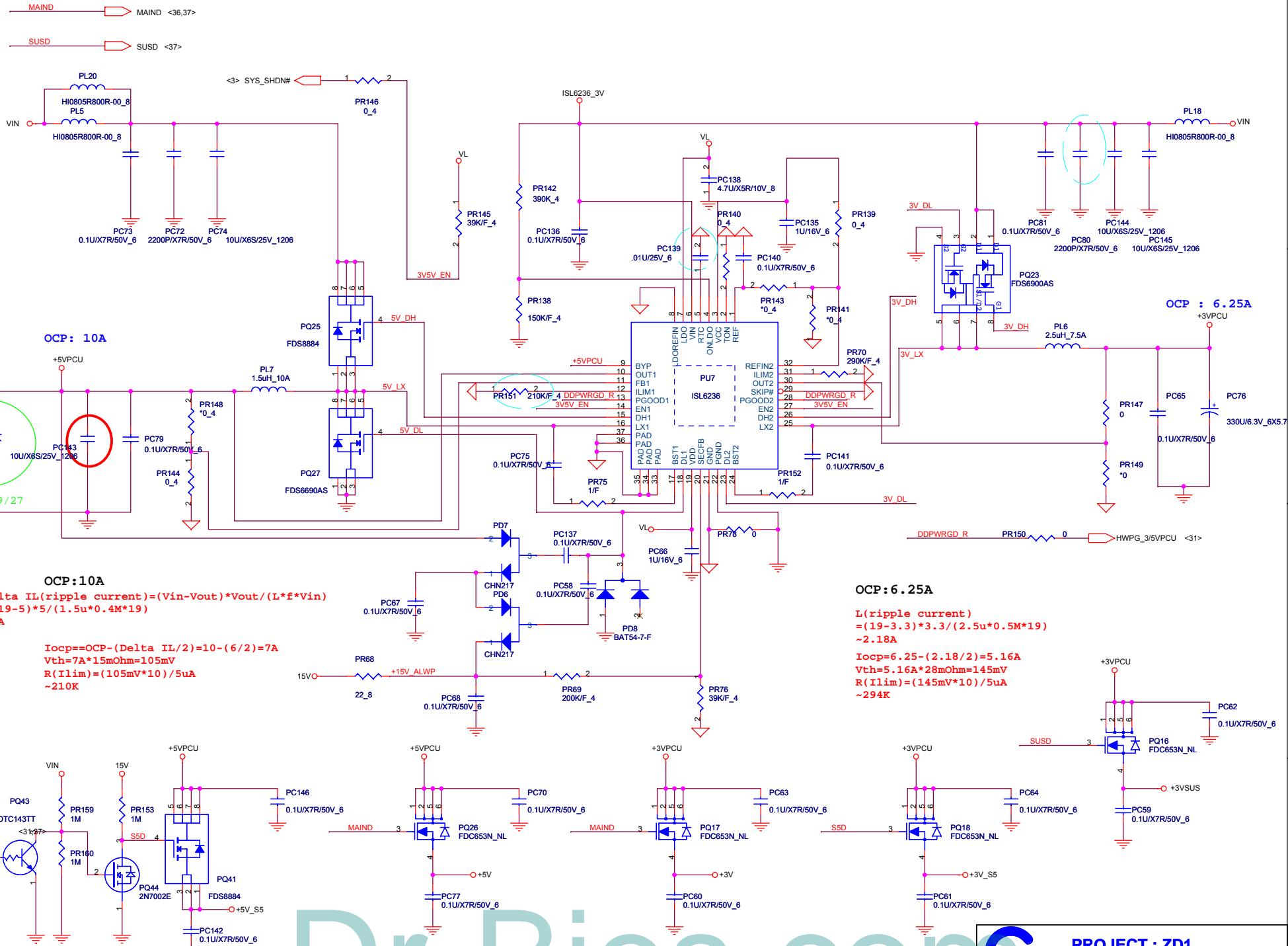
$$4.026A = (1/0.02) * ((0.05/2.365)VAclm+0.05)$$

$$VAclm = ((33//152) / (33//152+19.6//152)) * Vref$$

R2=adapter current sense resistnece

PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ISL6251 CHARGER	C
Date:	Monday, May 07, 2007	Sheet 32 of 38



OCP: 10A

OCP: 10A

$$\Delta IL(\text{ripple current}) = (V_{in} - V_{out}) * V_{out} / (L * f * V_{in})$$

$$= (19 - 5) * 5 / (1.5 \mu * 0.4 \text{M} * 19)$$

$$\sim 6A$$

$$I_{ocp} = OCP - (\Delta IL / 2) = 10 - (6 / 2) = 7A$$

$$V_{th} = 7A * 15 \text{m}\Omega = 105 \text{mV}$$

$$R(I_{lim}) = (105 \text{mV} * 10) / 5 \mu A$$

$$\sim 210K$$

OCP: 6.25A

$$L(\text{ripple current}) = (19 - 3.3) * 3.3 / (2.5 \mu * 0.5 \text{M} * 19)$$

$$\sim 2.18A$$

$$I_{ocp} = 6.25 - (2.18 / 2) = 5.16A$$

$$V_{th} = 5.16A * 28 \text{m}\Omega = 145 \text{mV}$$

$$R(I_{lim}) = (145 \text{mV} * 10) / 5 \mu A$$

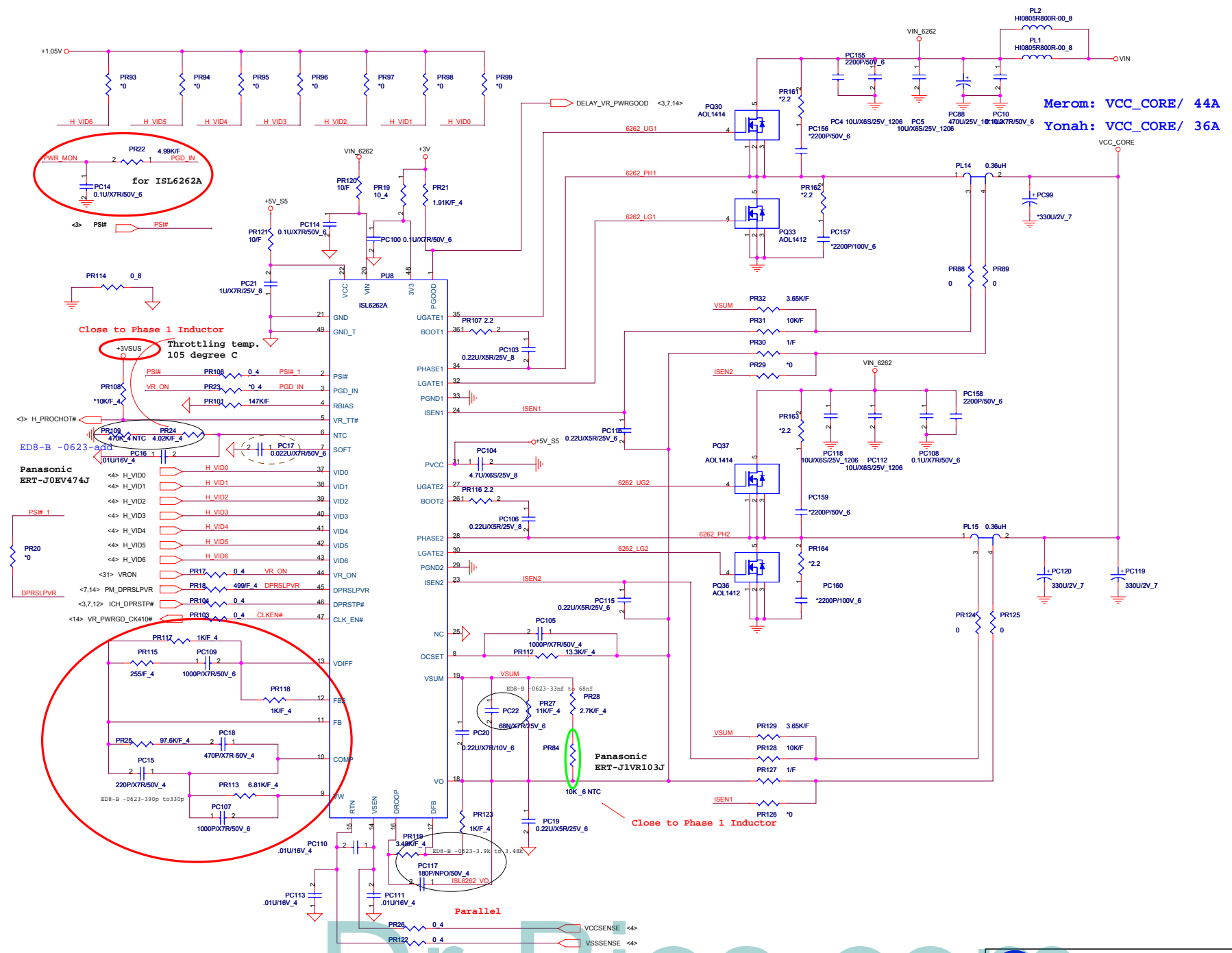
$$\sim 294K$$

modify 0103 2007

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PROJECT : ZD1
Quanta Computer Inc.

Size Custom	Document Number	Rev B
ISL6251 CHARGER		
Date: Monday, May 07, 2007	Sheet	33 of 38



Merom: VCC_CORE/ 44A
 Yonah: VCC_CORE/ 36A

for ISL6262A
 PC14 0.1U/X7R/50V_6

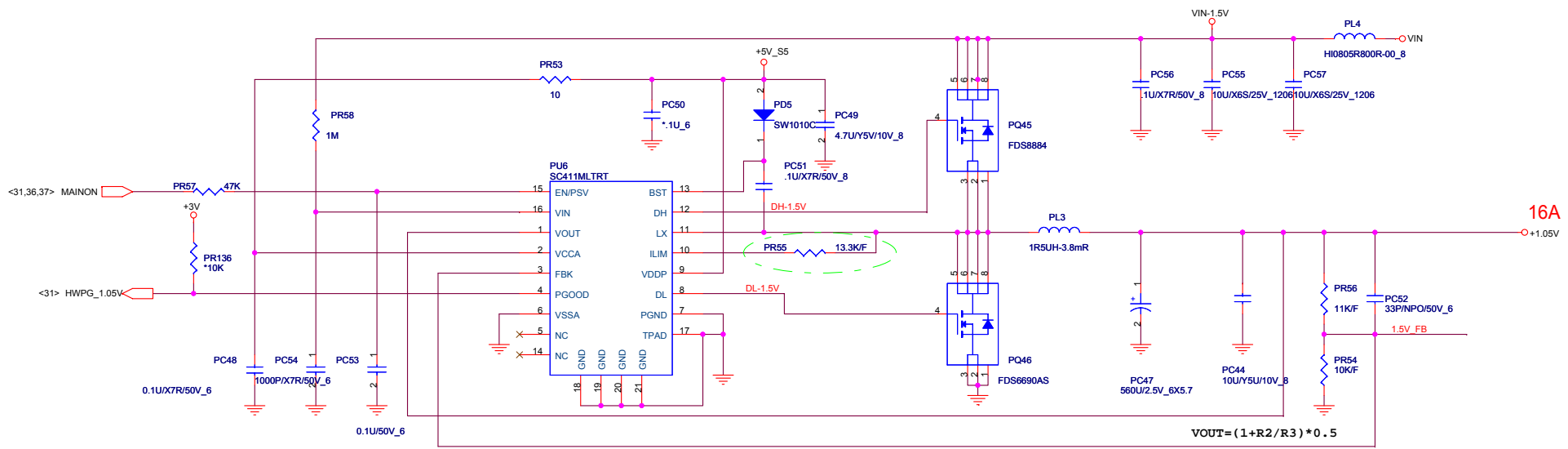
Close to Phase 1 Inductor
 Throttling temp. 105 degree C

Close to Phase 1 Inductor

Parallel

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PROJECT : ZD1
 Quanta Computer Inc.
 CPU CORE(ISL6262)
 Date: Monday, May 07, 2007 Sheet 34 of 38



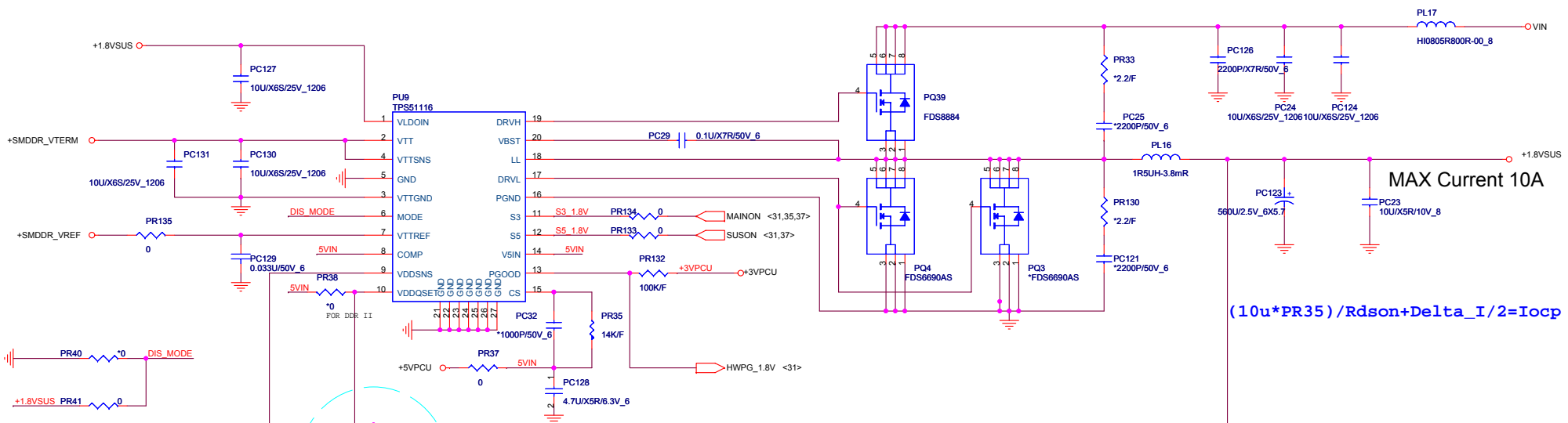
$R_{dson} * I_{ocp} = PR55 * 10u$ $R_{dson} = 15m \text{ ohm}$

$V_{OUT} = (1 + R2/R3) * 0.5$

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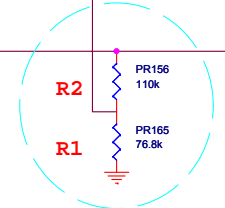
PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	VTT +1.05V	C
Date:	Monday, May 07, 2007	Sheet 35 of 38



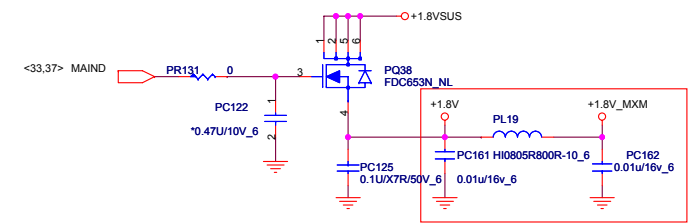
MAX Current 10A

$(10u \cdot PR35) / R_{dson} + \Delta I / 2 = I_{ocp}$



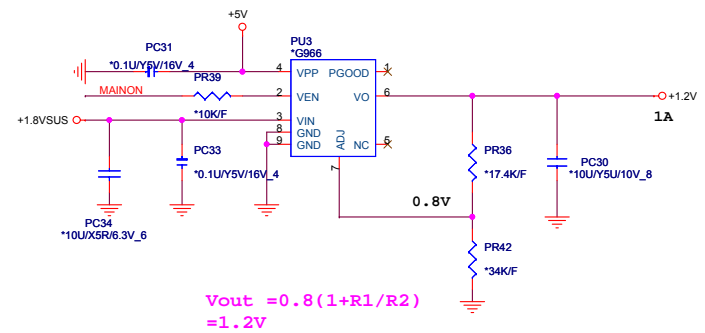
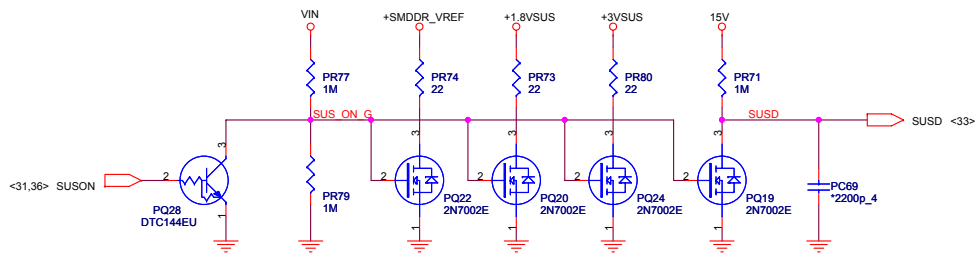
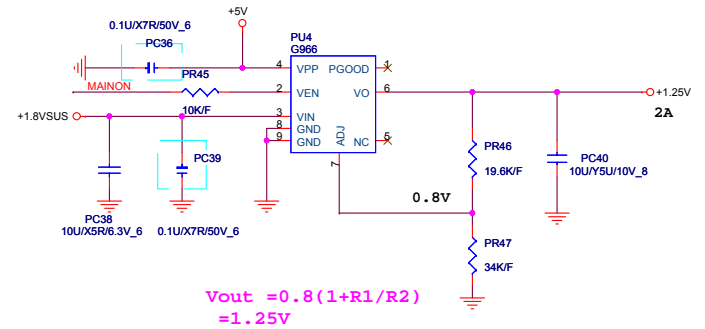
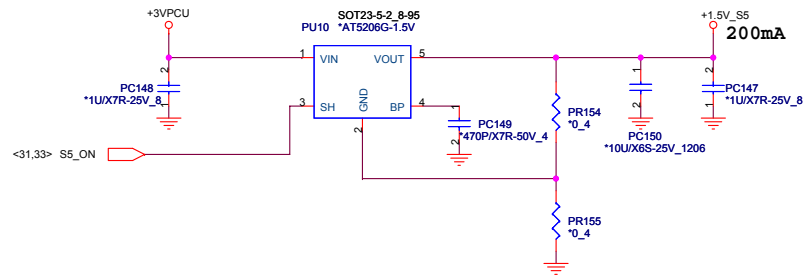
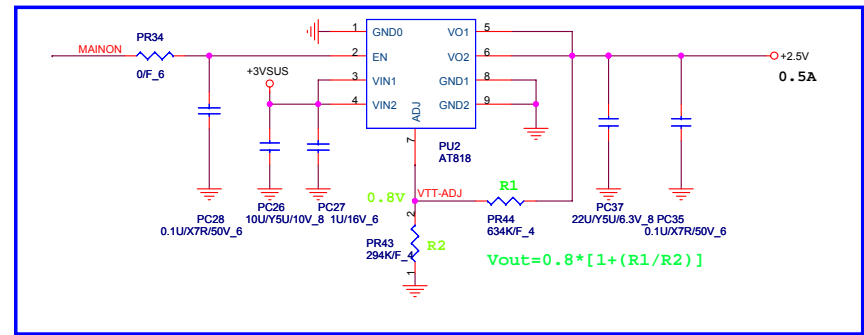
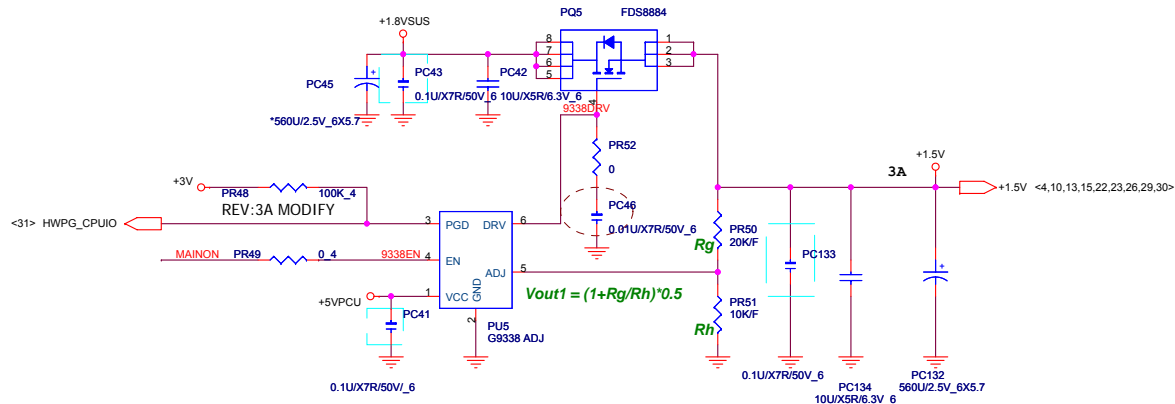
$R1 = (100 \cdot V_{out} - R2) / K$

if tune V_{out} PR38 un-mount, PR156 PR165 mount

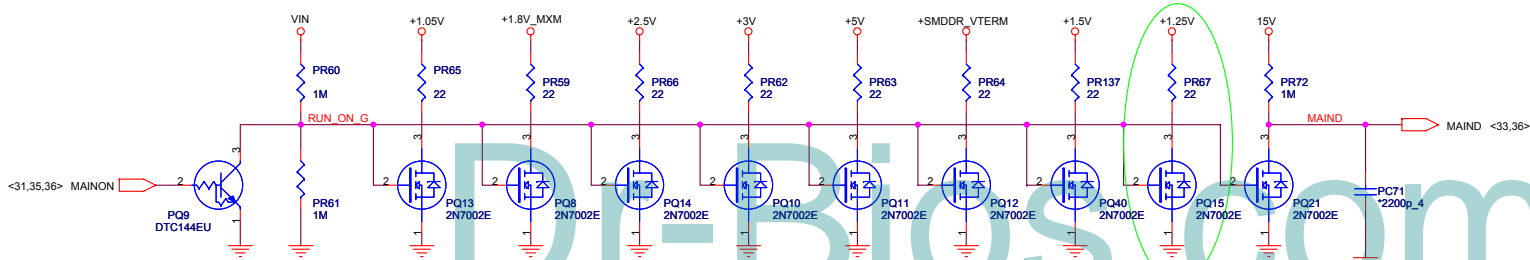


MAX Current 3.5A


PC161, PL19 & PC162 near CN27



Add by power on 10/19



Model	REV	CHANGE LIST	MODEL	ZY3	
				FROM	To
ZD1 MB	1A	FIRST RELEASED: E200610-3793 (PCB: DA0ZD1MB6A0)	X	1A	
	2A	<p>Page10 : Depop R153 & pop L23 for system can not boot</p> <p>Page14 : U36 package didn't math footprint, change P/N.</p> <p>Page26 : Remove R275, install R276; remove R4, install R16; Change R245, R247 power source from +1.5V_S5/+1.5V to +3V_S5/+3V , Follow customer request modem change support to +3VSUS.</p> <p>Page22 : MMB(CN8) PIN define error.</p> <p>Page22 : TV card change support to +1.5V.</p> <p>Page18 : Install R5, depop R7,: Follow customer request use EC to control backlight ON/OFF function.</p> <p>Page14 : GPIO10: Reserve PU, 10K +> It is GPO and OD; GPIO14: Reserve PD, 10K => It is GPI as AC present and active high;</p> <p>Page6 : TV_DCONSEL[0:1], UMA =>NC, External VGA tie to GND.</p> <p>Page31 : 2nd FAN change design</p> <p>Page23 : New card power SW (location: U33) change same as Z01</p> <p>Page31 : add 2 capacity 0.1uF(C634,C636) in DIGVOL_UP / DIGVOL_DN pins</p> <p>Page26 : Co-layout ALC268 and 888S</p> <p>Page28 : SD card can not be detected , U32(ES2) sample will fix this issue.</p> <p>Page28 : MMC card can not be detected , U32(ES2) sample will fix this issue.</p> <p>Page14 : The CLPWROK pin of ICH8 connect with HWFG signal</p> <p>Page22 : change CN7 pin definition for T/P no function.</p> <p>Page24 : change CN8 pin definition MMB no function.</p> <p>Page14 : The signal of KBSMI#_ICH add diode , and it PU to +3V_S5 The signal of LID591#_ICH add diode , and it PU to +3V_S5 for ICH8 electric leakage issue.</p> <p>Page26 : Change subwoofer from 4pin to 5pin connector.</p>	X	1A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
			1A	2A	
1A			2A		
2B	<p>Page 2 : Add C645 for EMI solution</p> <p>Page31 : Follow customer request 2nd FAN is controlled by EC</p> <p>Page19 : Floating CN13.16 & CN13.17 ,CN14.15 & CN14.16 for ESD test</p> <p>Page07 : DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK and DPLL_REF_SSCLK#. To GND</p> <p>Page36 : Add PI filter to reduce the power ripple of +1.8V.</p> <p>Page16 : Modify SMBus address A2 , The signal of B_SAL need to PU and B_SA0 need to PD</p> <p>Page26 : add 2 capacity 1uF(C639,C640) for subwoofer</p> <p>Page30 : add capacity 2.2uF(C638)</p>	1A	2A		
		1A	2A		
		1A	2A		
		1A	2A		
		1A	2A		
		1A	2A		
		2A	2B		
		2A	2B		
		2A	2B		
		2A	2B		
2C	<p>Page17 : Adding (Q52 & R541 & Q53) extra circuitry to prevent power leakage from system into MXM</p> <p>Page21 : Change power of CIR from +3VPCU and +5VPCU.</p> <p>Page31 : AEC pin24 is multi function pin, when EC power up, pin17 will change to JTAG/TCK function not GPIO. So,need to change from pin24 (GPIO47) to pin27 (GPIO52).</p> <p>Page22: Power/B connector add two LED control signal and change to 16 pin from 14-pin for meet ACER LED spec .</p> <p>Page22: Q35 change to AO3413 form DTAL14 for increase LED driving power.</p> <p>Page23: BL_ON pull up resistor from 10kohm to 100Kohm(R194).+3V pull up will cause power on leakage on BL_ON signal due to our VGA have 10kohm pull low.</p>	2A	2B		
		2A	2B		
		2A	2B		
		2B	3A		
		2B	3A		
		2B	3A		
		2B	3A		
		2B	3A		
		2B	3A		
		2B	3A		
2D	<p>Page19 : Connect CRT of CN13.16 & 17 to GND for ESD</p> <p>Page17 : Add capacity 330uF(C647) & Remove R541</p> <p>Page22 & 25: Combine USB/B (CN17) and TV/B(CN30) connector, Connector change to 16 pin. and +5_S5 from 1pin to 2pin.</p> <p>Page25 : Connect HOLE 28 & 29 to GND for ESD</p> <p>Page32-37 : Update power circuit</p> <p>Page37 : Remove 1.2V circuit</p> <p>Page26 : Add 1000pF and 10pF total 4 PCS Location: C648 , C649, C650, C652 (between +5V_ADOand AGND).</p> <p>Page22 : CN8.8 remove +5V & R540 & connect to +3V (K)</p> <p>Page27 : Modify and ADD. AGND bridge (R337,R284,C459 and C472 = 0 Ohm).</p> <p>Page34 : Remove PR16L, PR163, PC156, PC159</p> <p>Page22 : Add D45-D51 for ESD</p> <p>Page28 : Change CN36.37 & 38 ,CN37.37 & 38 ,CN38.42 & 43 from ADOGND and GND.</p>				
3A	<p>Page32 : PD9 Change footprint</p> <p>Page25 : Add EMI Spring</p> <p>Page27 : Add GND & AGND bridge (R546,R540,R408)</p> <p>Page22 : Modify pin define (TV/B(CN30) connector)</p>				
F	<p>Page23 & 17 : HDMI circuits modify: Add level-shifter for MXM_HDMI_DDCCLK and MXM_HDMI_DDCDATA.(Location: Q54 ,Q55 , R75, R63, R297, R410 & R602) .</p>				

 PROJECT : ZD1
Quanta Computer Inc.

Size: Document Number: Rev: 1A
Change list

Date: Monday, May 07, 2007 Sheet: 38 of 38

DOC NO.	PROJECT MODEL : ZD1	APPROVED BY:	DATE: 2007/ 2/15
	PART NUMBER:	DRAWING BY:	REVISION: 3A

