Huron Block Diagram

Project code: 91.4V301.001
PCB P/N : 07205
REVISION : SD

CLK GEN.
IDTCV125PAG 71.00125.A0W
RTM865T-433 71.00865.B0W
3

Mobile CPU
Yonah 478
Celeron M
62.10079.001 4, 5

FSB 400/533/667MHz

G792 20

TV Out 14
CRT 14
LCD 13
DVI 42

DDR2 533/667 MHz 13,14
533/667MHz

DDR2 533/667 MHz 13,14
533/667MHz

Calistoga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CALIS.00U 6,7,8,9,10

VGA Borad 26

DMI 100MHz

Line In
MIC In 29
INT.MIC
INT.SPKR 29
Line Out (SPDIF)
SUBWF 29

Codec ALC268 28
AZALIA

OP AMP G1431Q 29
OP AMP G1412 29
OP AMP G1442 29

ICH7M
4 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
2 SATA
1 PATA 66/100
8 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
71.ICH7M.00U 15,16,17,18

PCI BUS

OZ129 1394 CardReader 24
1394 CONN 25

Cardreader BD
PCB P/N:07517
MS/MS Pro/xD/ MMC/SD 5 in 1
MODEM Card 25
RJ11

AZALIA

PCI Express

Giga LAN 22
BCM5787MKMLG
TXFM 23
RJ45 23

New card 27
P2231NFC1 28

Mini Card
Kedron a/b/g/n 27

LPC BUS

KBC
Winbond
WPC8768L 30
SPI I/F
BIOS
W25X80-VSS 32

Touch Pad 31
INT. KB 31

USB

MINI USB
BlueTooth 22

HDD 20
SATA

CDROM 20
PATA

USB BD
PCB : 07521 21
USB
2 Port 21
CAMERA 13

MEDIA BD
56.41004.031 31
PWM BD
PCB : 07520 31
LAUNCH BD
PCB : 07519 31
e-Key BD
PCB : 07518 31

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC
TPS51120 37

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC
TPS51124 38

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D05V_S0

TPS51100 40

1D8V_S3	DDR_VREF

APL5308 40

3D3V_S0	2D5V_S0

APL5912 39

1D8V_S3	1D5V_S0

Intersil CHARGER
MAX8731 41

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
ISL6262 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A

Volvi

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: HURON | Rev: SD
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ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

RTM865T-433 100Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	0.8% Down
0	0	0	1	1.0% Down
0	0	1	0	1.25% Down
0	0	1	1	1.50% Down
0	1	0	0	1.75% Down
0	1	0	1	2.0% Down
0	1	1	0	2.5% Down
0	1	1	1	3.0% Down
1	0	0	0	+-0.3% Center
1	0	0	1	+-0.4% Center
1	0	1	0	+-0.5% Center
1	0	1	1	+-0.6% Center
1	1	0	0	+-0.8% Center
1	1	0	1	+-1.0% Center
1	1	1	0	+-1.25% Center
1	1	1	1	+-1.5% Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
OZ129TZ	AD22	A→G	REQ0# ->REQ0#

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

<Core Design>

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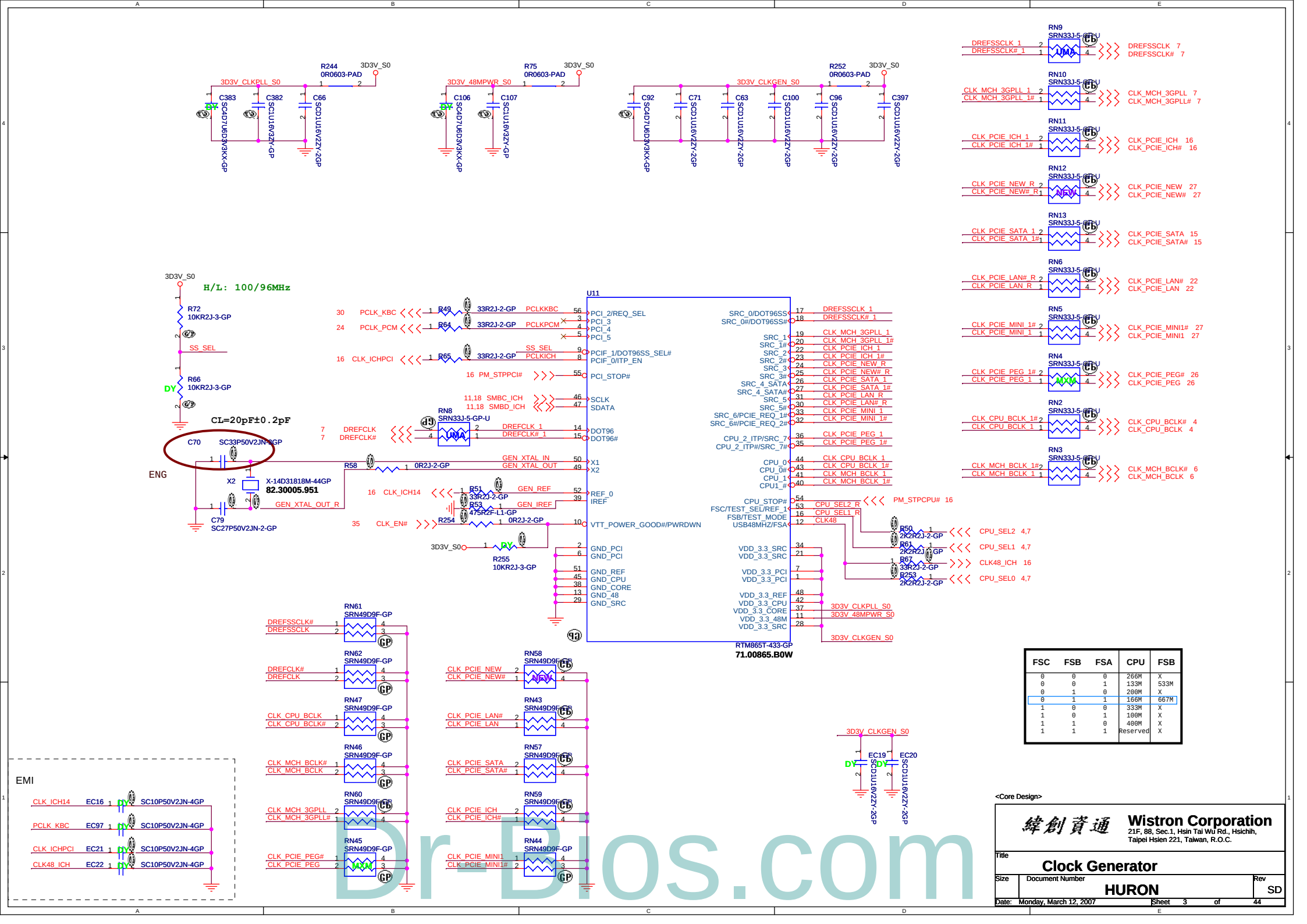
Title: Reference

Size | Document Number: HURON | Rev: SD

Date: Monday, March 12, 2007 | Sheet 2 of 44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R244 0R0603-PAD
3D3V_S0
C383 SC4D7U6D3V3KX-GP
C382 SC1U16V3ZY-GP
C66 SCD1U16V2ZY-2GP
3D3V_48MPWR_S0
R75 0R0603-PAD
C106 SC4D7U6D3V3KX-GP
C107 SC1U16V3ZY-GP
3D3V_CLKGEN_S0
R252 0R0603-PAD
C92 SC4D7U6D3V3KX-GP
C71 SCD1U16V2ZY-2GP
C63 SCD1U16V2ZY-2GP
C100 SCD1U16V2ZY-2GP
C96 SCD1U16V2ZY-2GP
C397 SCD1U16V2ZY-2GP
RN9 SRN33J-5-GP-U
DREFSSCLK_1
DREFSSCLK# 1
DREFSSCLK 7
DREFSSCLK# 7
RN10 SRN33J-5-GP-U
CLK_MCH_3GPLL_1
CLK_MCH_3GPLL_1#
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
RN11 SRN33J-5-GP-U
CLK_PCIE_ICH_1
CLK_PCIE_ICH_1#
CLK_PCIE_ICH 16
CLK_PCIE_ICH# 16
RN12 SRN33J-5-GP-U
CLK_PCIE_NEW_R
CLK_PCIE_NEW#_R
CLK_PCIE_NEW 27
CLK_PCIE_NEW# 27
RN13 SRN33J-5-GP-U
CLK_PCIE_SATA_1
CLK_PCIE_SATA_1#
CLK_PCIE_SATA 15
CLK_PCIE_SATA# 15
RN6 SRN33J-5-GP-U
CLK_PCIE_LAN#_R
CLK_PCIE_LAN_R
CLK_PCIE_LAN# 22
CLK_PCIE_LAN 22
RN5 SRN33J-5-GP-U
CLK_PCIE_MINI_1#
CLK_PCIE_MINI_1
CLK_PCIE_MINI1# 27
CLK_PCIE_MINI1 27
RN4 SRN33J-5-GP-U
CLK_PCIE_PEG_1#
CLK_PCIE_PEG_1
CLK_PCIE_PEG# 26
CLK_PCIE_PEG 26
RN2 SRN33J-5-GP-U
CLK_CPU_BCLK_1#
CLK_CPU_BCLK_1
CLK_CPU_BCLK# 4
CLK_CPU_BCLK 4
RN3 SRN33J-5-GP-U
CLK_MCH_BCLK_1#
CLK_MCH_BCLK_1
CLK_MCH_BCLK# 6
CLK_MCH_BCLK 6
3D3V_S0
H/L: 100/96MHz
R72 10KR2J-3-GP
SS_SEL
R66 10KR2J-3-GP
CL=20pF±0.2pF
C70 SC33P50V2JN-4GP
ENG
X2 X-14D31818M-44GP
82.30005.951
C79 SC27P50V2JN-2-GP
R58 0R2J-2-GP
GEN_XTAL_OUT_R
U11
PCLK_KBC
PCLK_PCM
CLK_ICHPCI
R49 33R2J-2-GP PCLKKBC
R64 33R2J-2-GP PCLKPCM
R65 33R2J-2-GP PCLKICH
SS_SEL
PM_STPPCI#
PCI_STOP#
SMBC_ICH
SMBD_ICH
SCLK
SDATA
RN8 SRN33J-5-GP-U
DREFCLK
DREFCLK#
DREFCLK_1
DREFCLK#_1
DOT96
DOT96#
GEN_XTAL_IN
GEN_XTAL_OUT
X1
X2
CLK_ICH14
R51 33R2J-2-GP
R53 475R2F-L1-GP
GEN_REF
GEN_IREF
REF_0
IREF
CLK_EN#
R254 0R2J-2-GP
VTT_POWER_GOOD#/PWRDWN
3D3V_S0
R255 10KR2J-3-GP
GND_PCI
GND_REF
GND_CPU
GND_CORE
GND_48
GND_SRC
PCI_2/REQ_SEL
PCI_3
PCI_4
PCI_5
PCIF_1/DOT96SS_SEL#
PCIF_0/ITP_EN
SRC_0/DOT96SS
SRC_0#/DOT96SS#
SRC_1
SRC_1#
SRC_2
SRC_2#
SRC_3
SRC_3#
SRC_4_SATA
SRC_4_SATA#
SRC_5
SRC_5#
SRC_6/PCIE_REQ_1#
SRC_6#/PCIE_REQ_2#
CPU_2_ITP/SRC_7
CPU_2_ITP#/SRC_7#
CPU_0
CPU_0#
CPU_1
CPU1_#
CPU_STOP#
FSC/TEST_SEL/REF_1
FSB/TEST_MODE
USB48MHZ/FSA
VDD_3.3_SRC
VDD_3.3_PCI
VDD_3.3_REF
VDD_3.3_CPU
VDD_3.3_CORE
VDD_3.3_48M
VDD_3.3_SRC
RTM865T-433-GP
71.00865.B0W
DREFSSCLK_1
DREFSSCLK#_1
CLK_MCH_3GPLL_1
CLK_MCH_3GPLL_1#
CLK_PCIE_ICH_1
CLK_PCIE_ICH_1#
CLK_PCIE_NEW_R
CLK_PCIE_NEW#_R
CLK_PCIE_SATA_1
CLK_PCIE_SATA_1#
CLK_PCIE_LAN_R
CLK_PCIE_MINI_1
CLK_PCIE_MINI_1#
CLK_PCIE_PEG_1
CLK_PCIE_PEG_1#
CLK_CPU_BCLK_1
CLK_CPU_BCLK_1#
CLK_MCH_BCLK_1
CLK_MCH_BCLK_1#
CPU_SEL2_R
CPU_SEL1_R
CLK48
PM_STPCPU# 16
R50 2K2R2J-2-GP
R61 2K2R2J-2-GP
R67 33R2J-2-GP
R253 2K2R2J-2-GP
CPU_SEL2 4,7
CPU_SEL1 4,7
CLK48_ICH 16
CPU_SEL0 4,7
3D3V_CLKPLL_S0
3D3V_48MPWR_S0
3D3V_CLKGEN_S0
RN61 SRN49D9F-GP
DREFSSCLK#
DREFSSCLK
RN62 SRN49D9F-GP
DREFCLK#
DREFCLK
RN47 SRN49D9F-GP
CLK_CPU_BCLK
CLK_CPU_BCLK#
RN46 SRN49D9F-GP
CLK_MCH_BCLK#
CLK_MCH_BCLK
RN60 SRN49D9F-GP
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
RN45 SRN49D9F-GP
CLK_PCIE_PEG#
CLK_PCIE_PEG
RN58 SRN49D9F-GP
CLK_PCIE_NEW
CLK_PCIE_NEW#
RN43 SRN49D9F-GP
CLK_PCIE_LAN#
CLK_PCIE_LAN
RN57 SRN49D9F-GP
CLK_PCIE_SATA
CLK_PCIE_SATA#
RN59 SRN49D9F-GP
CLK_PCIE_ICH
CLK_PCIE_ICH#
RN44 SRN49D9F-GP
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
EMI
CLK_ICH14 EC16 SC10P50V2JN-4GP
PCLK_KBC EC97 SC10P50V2JN-4GP
CLK_ICHPCI EC21 SC10P50V2JN-4GP
CLK48_ICH EC22 SC10P50V2JN-4GP
3D3V_CLKGEN_S0
EC19 SCD1U16V2ZY-2GP
EC20 SCD1U16V2ZY-2GP
FSC FSB FSA CPU FSB
0 0 0 266M X
0 0 1 133M 533M
0 1 0 200M X
0 1 1 166M 667M
1 0 0 333M X
1 0 1 100M X
1 1 0 400M X
1 1 1 Reserved X
<Core Design>
緯創資通
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Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator
Size
Document Number
HURON
Rev
SD
Date: Monday, March 12, 2007
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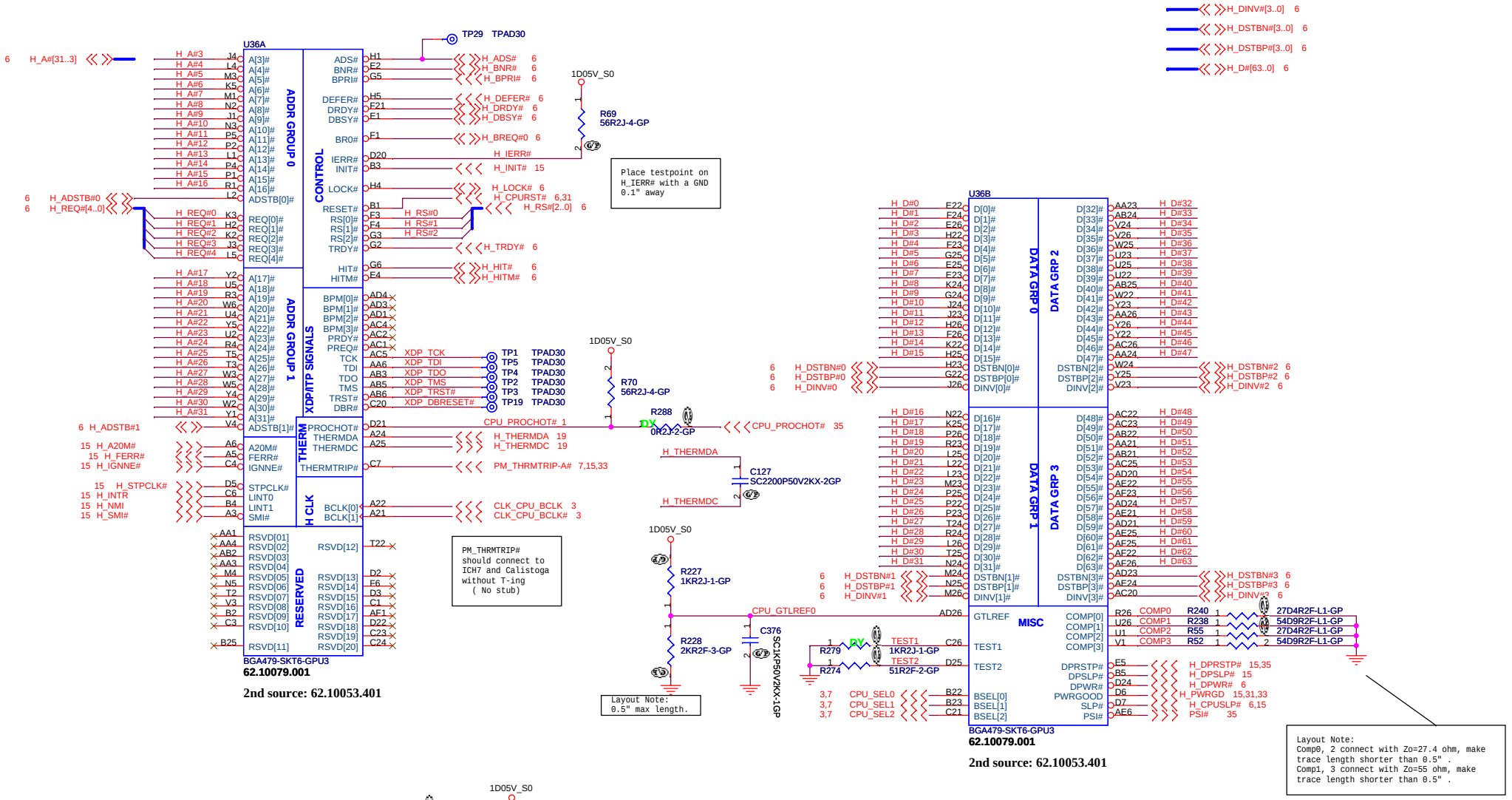

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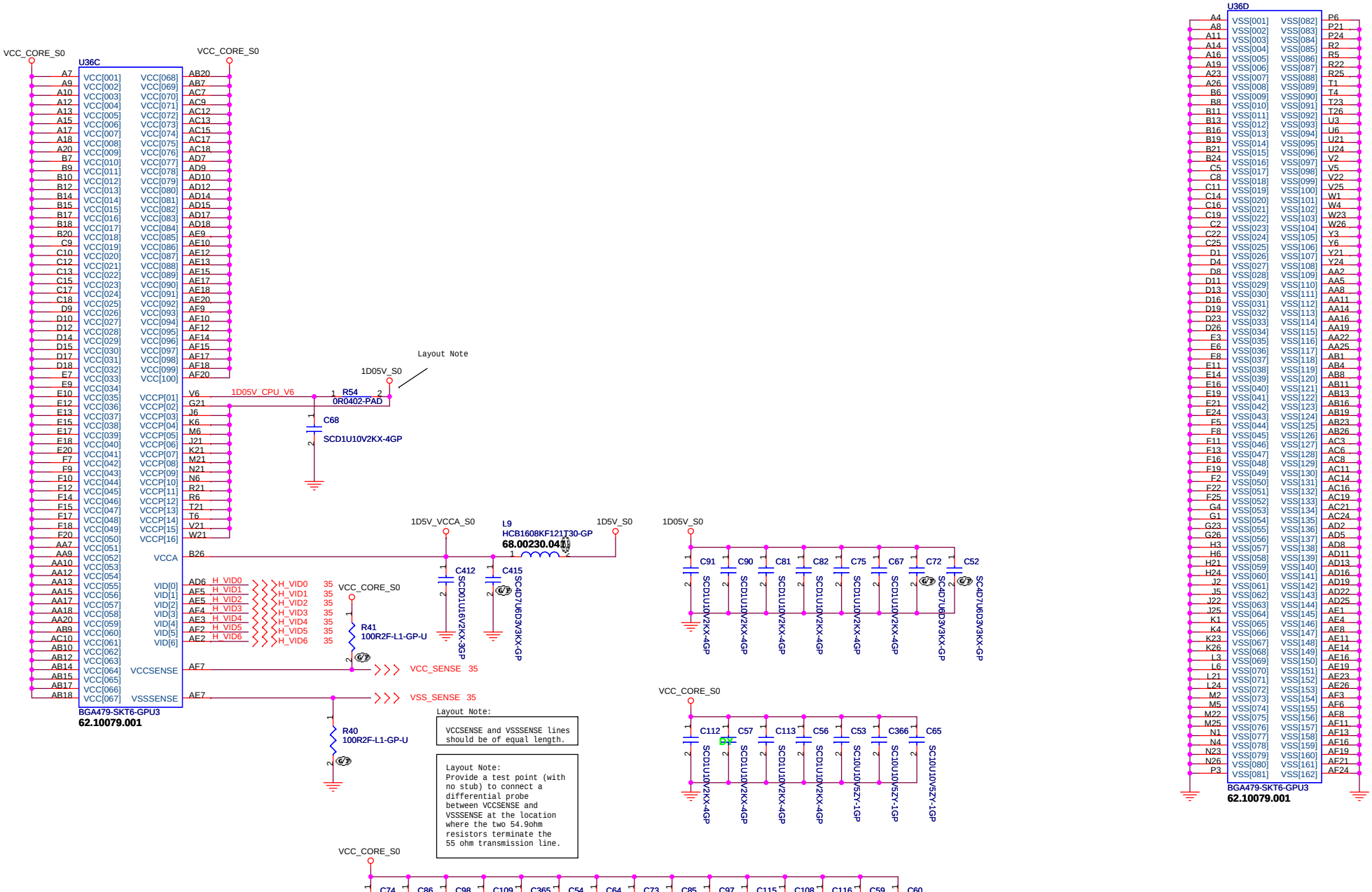

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Size	Document Number: HURON	Rev: SD
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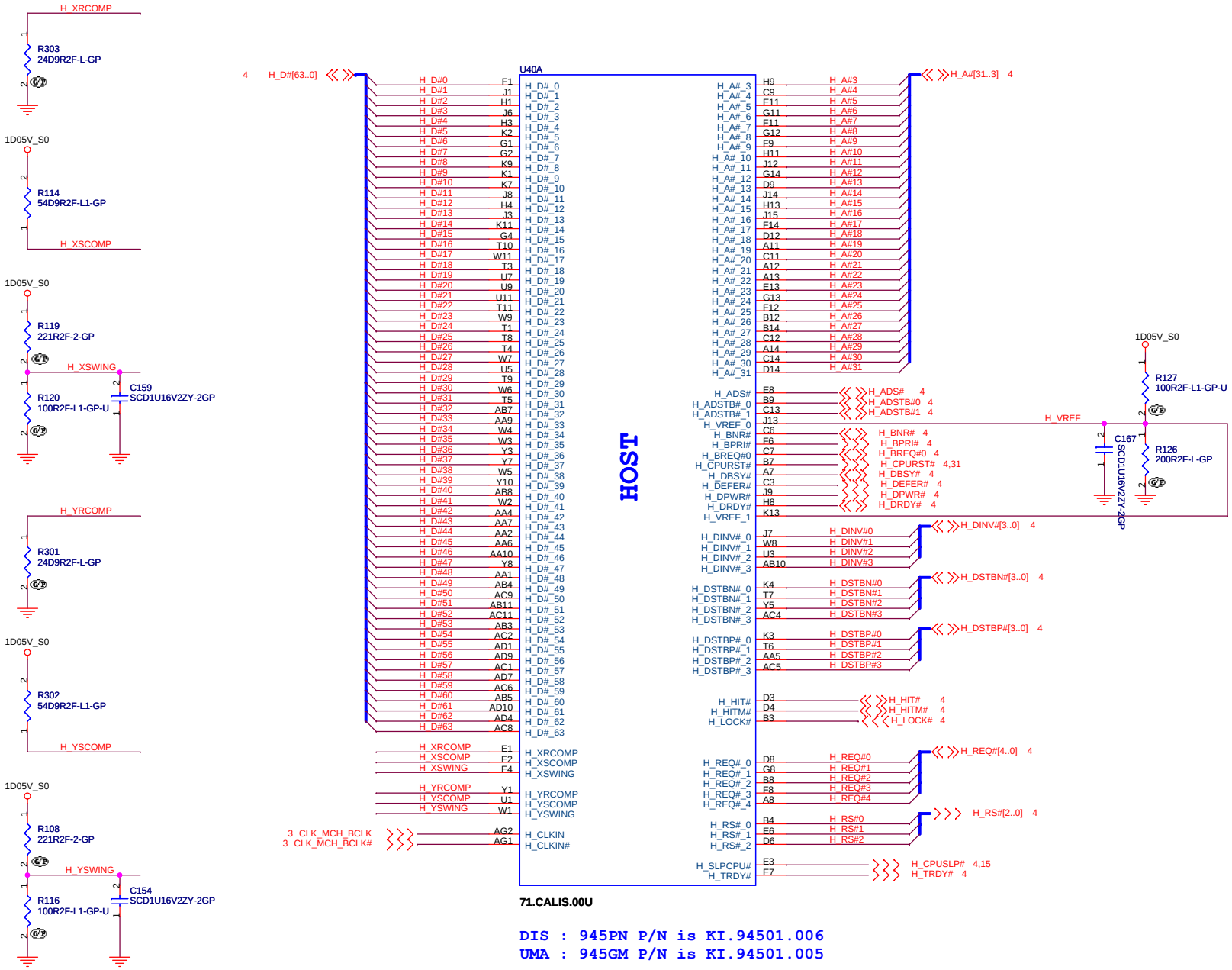

71.CALIS.00U

DIS : 945PN P/N is KI.94501.006
UMA : 945GM P/N is KI.94501.005

Place them near to the chip (< 0.5")

<Core Design>

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Title: GMCH (1 of 5)

Size | Document Number: HURON | Rev: SD

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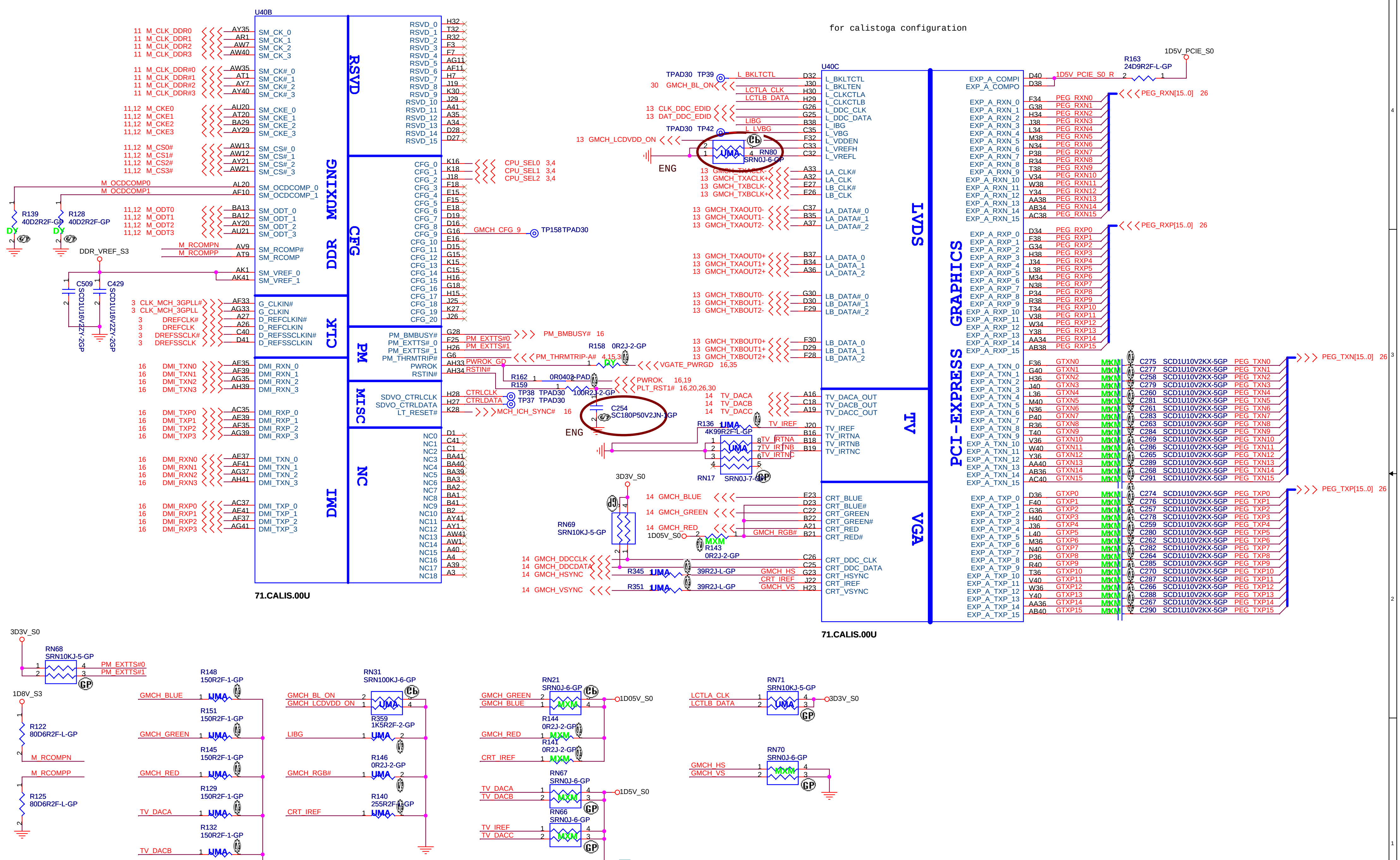

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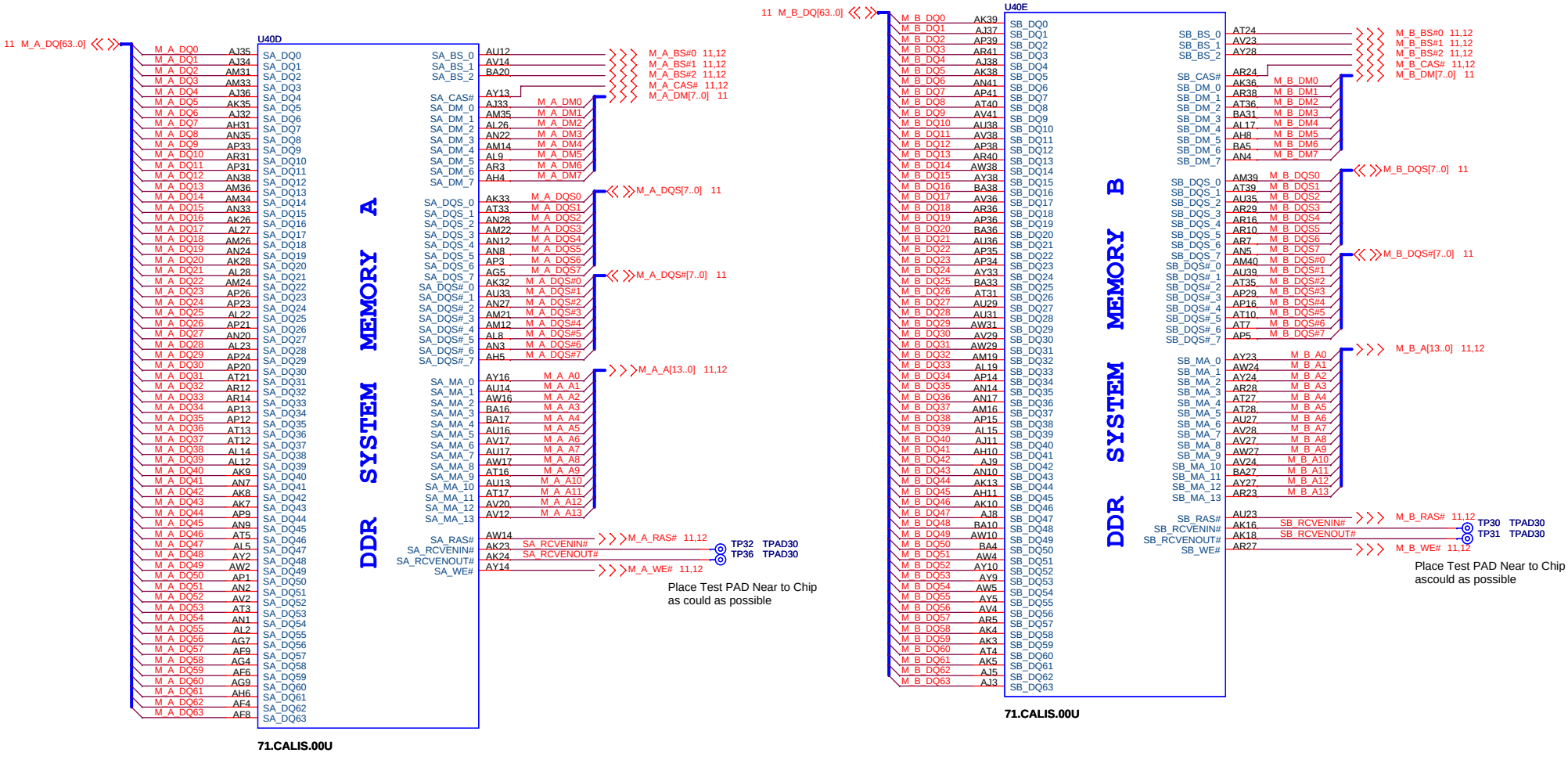
Date: Thursday, March 15, 2007	Sheet 7 of 44	



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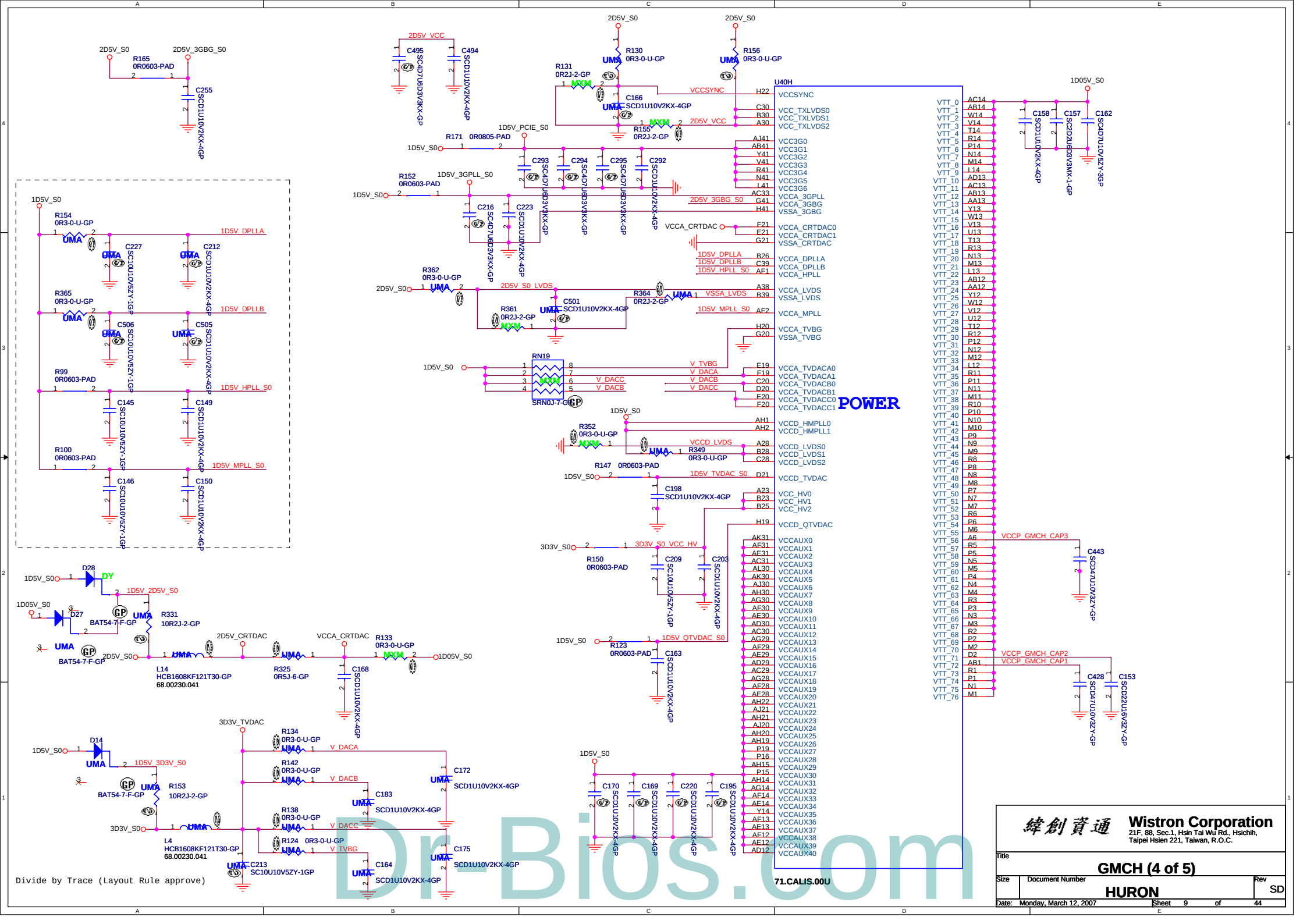
Title: **GMCH (3 of 5)**

Size | Document Number: **HURON** | Rev: SD

Date: Monday, March 12, 2007 | Sheet 8 of 44


POWER
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VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
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VTT_3
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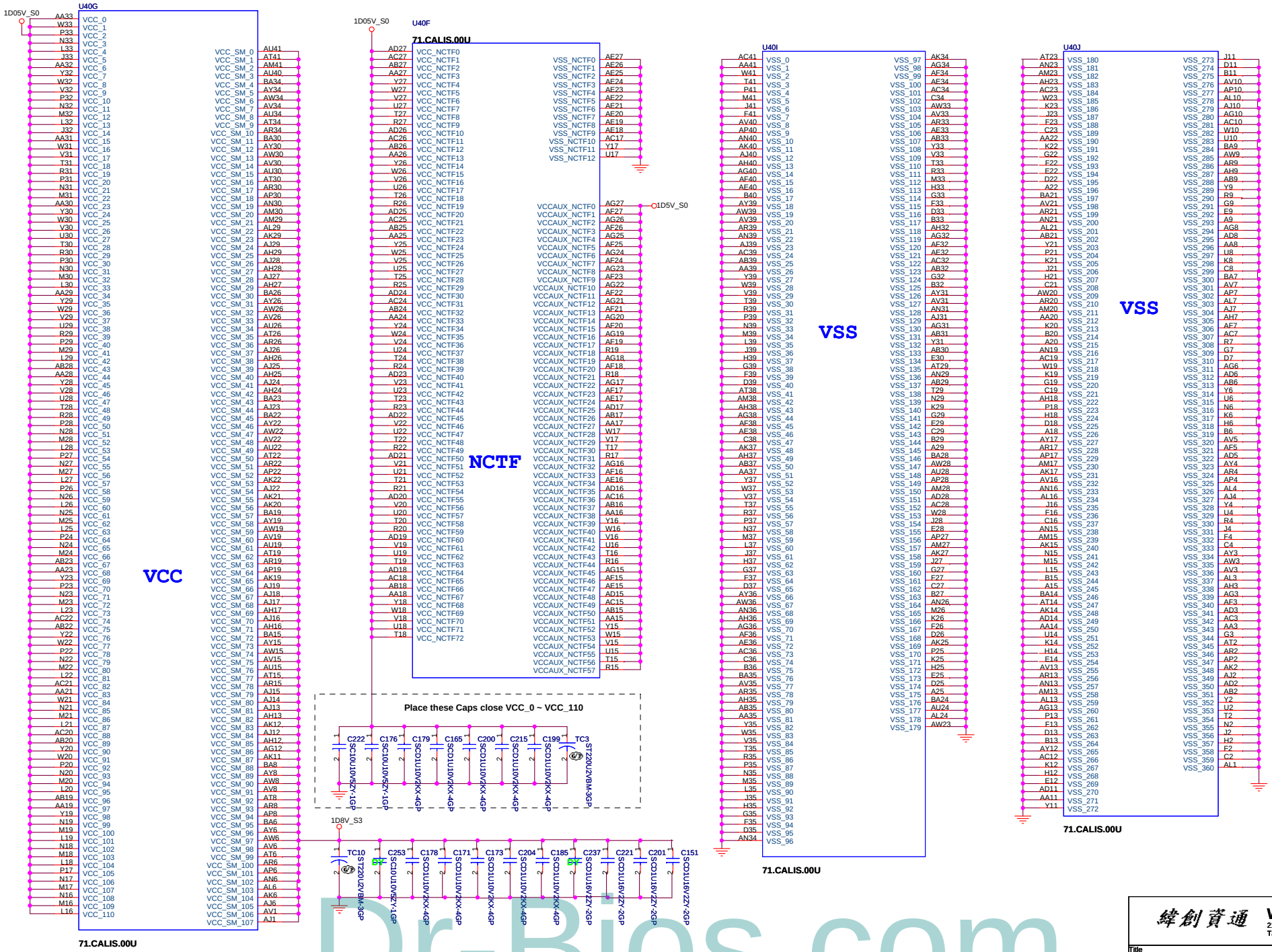
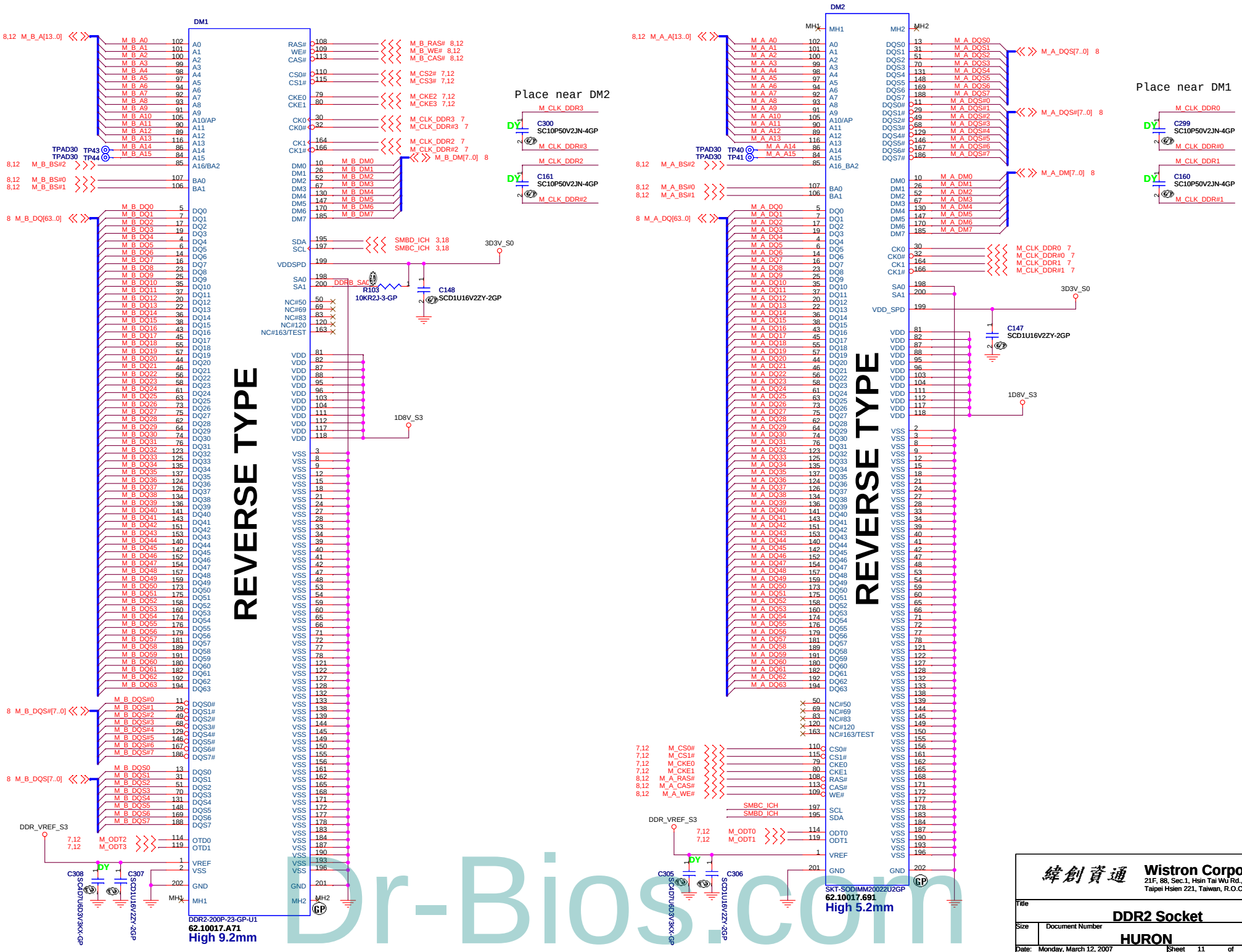
VTT_70
VTT_71
VTT_72
VTT_73
VTT_74
VTT_75
VTT_76
71.CALIS.00U
2D5V_S0
2D5V_3GBG_S0
2D5V_VCC
1D5V_S0
1D5V_PCIE_S0
1D5V_3GPLL_S0
2D5V_S0_LVDS
1D5V_DPLLA
1D5V_DPLLB
1D5V_HPLL_S0
1D5V_MPLL_S0
1D5V_TVDAC_S0
1D5V_QTVDAC_S0
3D3V_S0_VCC_HV
VCCP_GMCH_CAP3
VCCP_GMCH_CAP2
VCCP_GMCH_CAP1
1D05V_S0
3D3V_S0
3D3V_TVDAC
2D5V_CRTDAC
VCCA_CRTDAC
V_TVBG
V_DACA
V_DACB
V_DACC
1D5V_2D5V_S0
1D5V_3D3V_S0
VCCSYNC
2D5V_3GBG_S0
VSSA_LVDS
VCCD_LVDS
Divide by Trace (Layout Rule approve)
Dr-Bios.com
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (4 of 5)
Size
Document Number
HURON
Rev
SD
Date: Monday, March 12, 2007
Sheet 9 of 44



Company	Wistron Corporation
Address	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GMCH (5 of 5)
Size	
Document Number	HURON
Rev	SD
Date	Monday, March 12, 2007
Sheet	10 of 44



Company	緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR2 Socket
Size	Document Number: HURON
Rev	SD
Date	Monday, March 12, 2007
Sheet	11 of 44

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN34 SRN56J-5-GP
M_A_A12 → M_CKE0 7,11
M_A_BS#2 8,11

RN30 SRN56J-5-GP
M_B_A9
M_B_A8
M_B_A3
M_B_A5

RN35 SRN56J-5-GP
M_CKE2 7,11
M_B_BS#2 8,11
M_B_A12

RN26 SRN56J-5-GP
M_B_A10
M_B_BS#0 8,11
M_B_A0

RN24 SRN56J-5-GP
M_B_A13
M_ODT2 7,11
M_ODT3 7,11
M_B_RAS# 8,11

RN28 SRN56J-5-GP
M_B_BS#1 8,11
M_B_A2
M_B_A1
M_B_A4

RN33 SRN56J-5-GP
M_B_A6
M_B_A7
M_B_A11
M_CKE3 7,11

RN22 SRN56J-5-GP
M_B_CAS# 8,11
M_CS3# 7,11
M_B_WE# 8,11
M_CS2# 7,11

RN23 SRN56J-5-GP
M_A_A13
M_ODT0 7,11
M_CS0# 7,11
M_A_RAS# 8,11

RN27 SRN56J-5-GP
M_A_BS#1 8,11
M_A_A0
M_A_A2
M_A_A4

RN20 SRN56J-5-GP
M_A_CAS# 8,11
M_CS1# 7,11
M_ODT1 7,11

RN29 SRN56J-5-GP
M_A_A9
M_A_A8
M_A_A5
M_A_A1

RN32 SRN56J-5-GP
M_A_A6
M_A_A7
M_A_A11
M_CKE1 7,11

RN25 SRN56J-5-GP
M_A_A3
M_A_A10
M_A_WE# 8,11
M_A_BS#0 8,11

M_A_A[13..0] → M_A_A[13..0] 8,11
M_B_A[13..0] → M_B_A[13..0] 8,11

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C190 C174 C243 C235 C214 C191 C236 C238 C188 C245 C205 — SCD1U16V2ZY-2GP (DY)
C233 C226 C249 C244 C187 C232 C234 C206 C182 C218 C197 — SCD1U16V2ZY-2GP (DY)

Place these Caps near DM1

1D8V_S3

C177 C207 C242 C239 C180 — SC2D2U6D3V3MX-1-GP
C189 C219 C194 C228 — SCD1U16V2ZY-2GP (DY)

Place these Caps near DM2

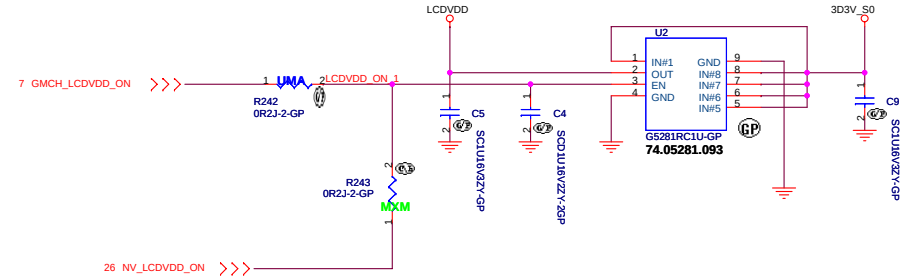
1D8V_S3

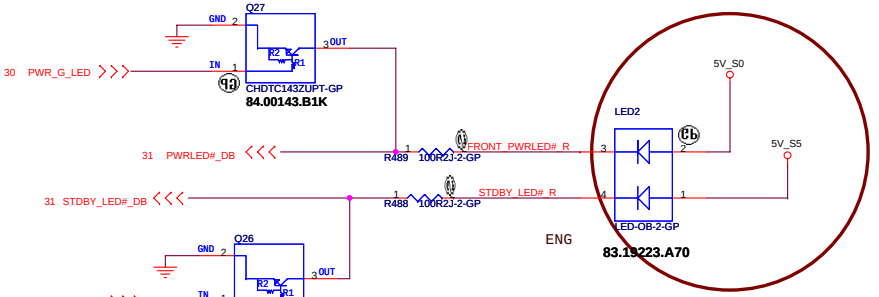
C181 C184 C241 C240 C250 — SC2D2U6D3V3MX-1-GP
C231 C217 C208 C192 — SCD1U16V2ZY-2GP (DY)

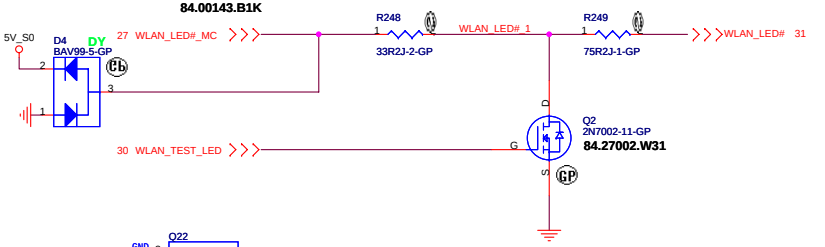
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

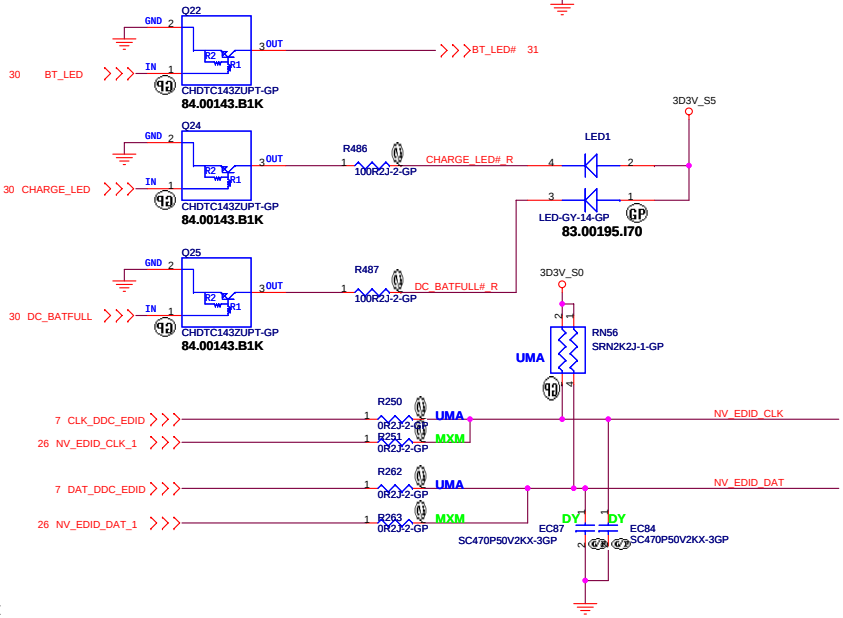
Title: DDR2 Termination Resistor
Size | Document Number: HURON | Rev: SD
Date: Monday, March 12, 2007 | Sheet 12 of 44

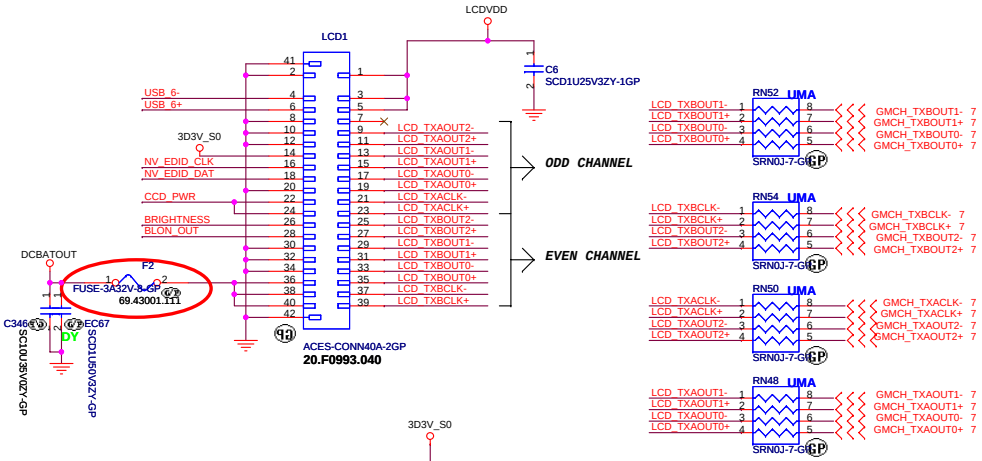
LCD/INVERTER CONN

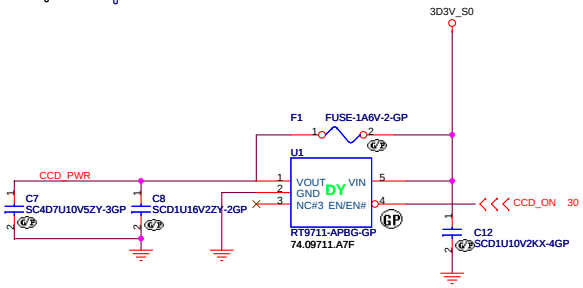


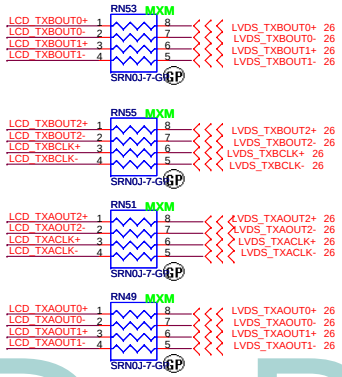


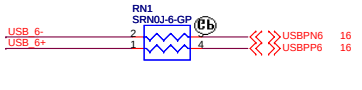


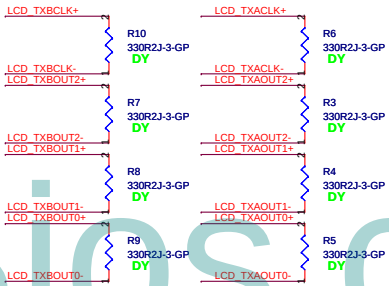












<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED

Size | Document Number: HURON | Rev: SD

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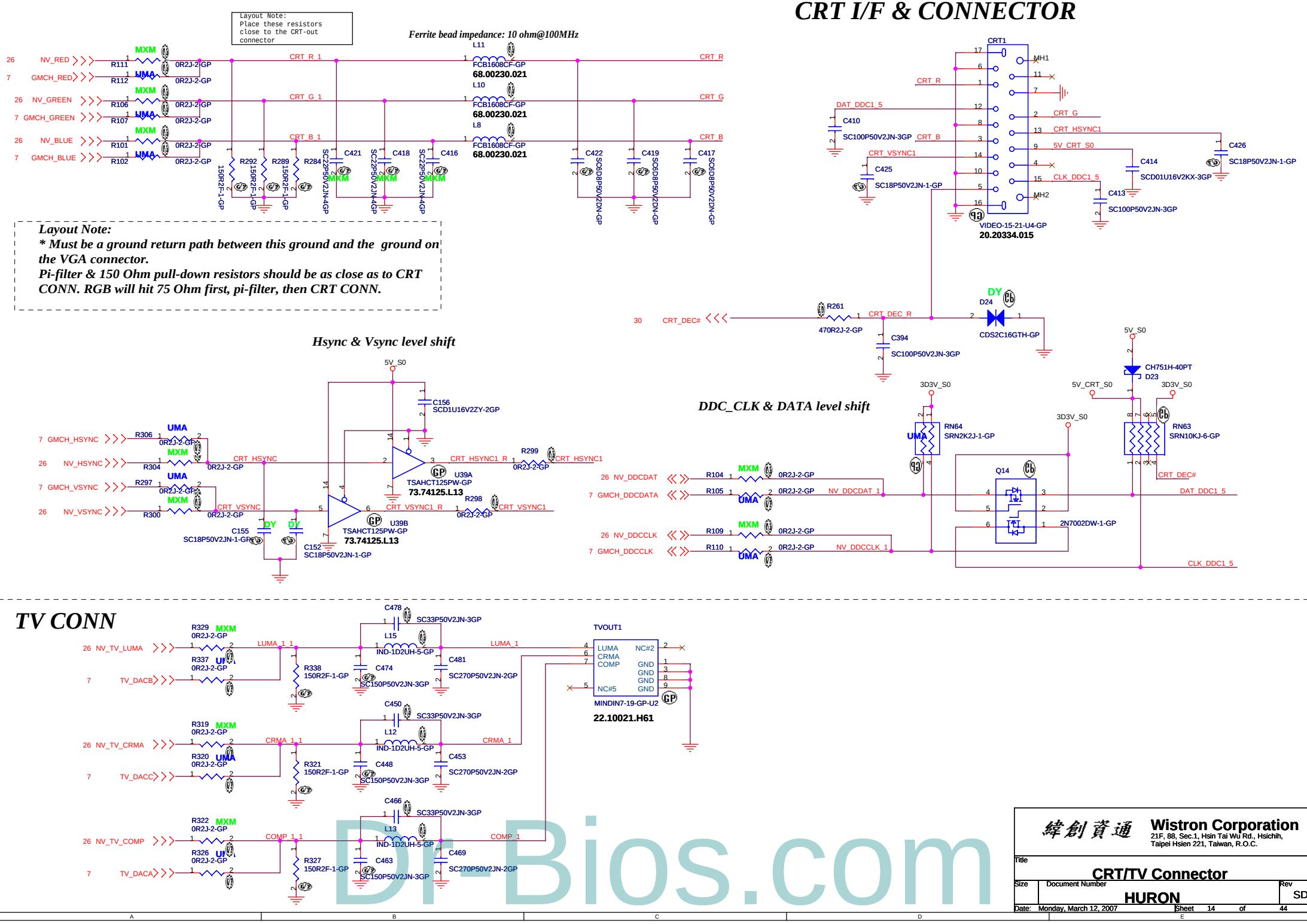
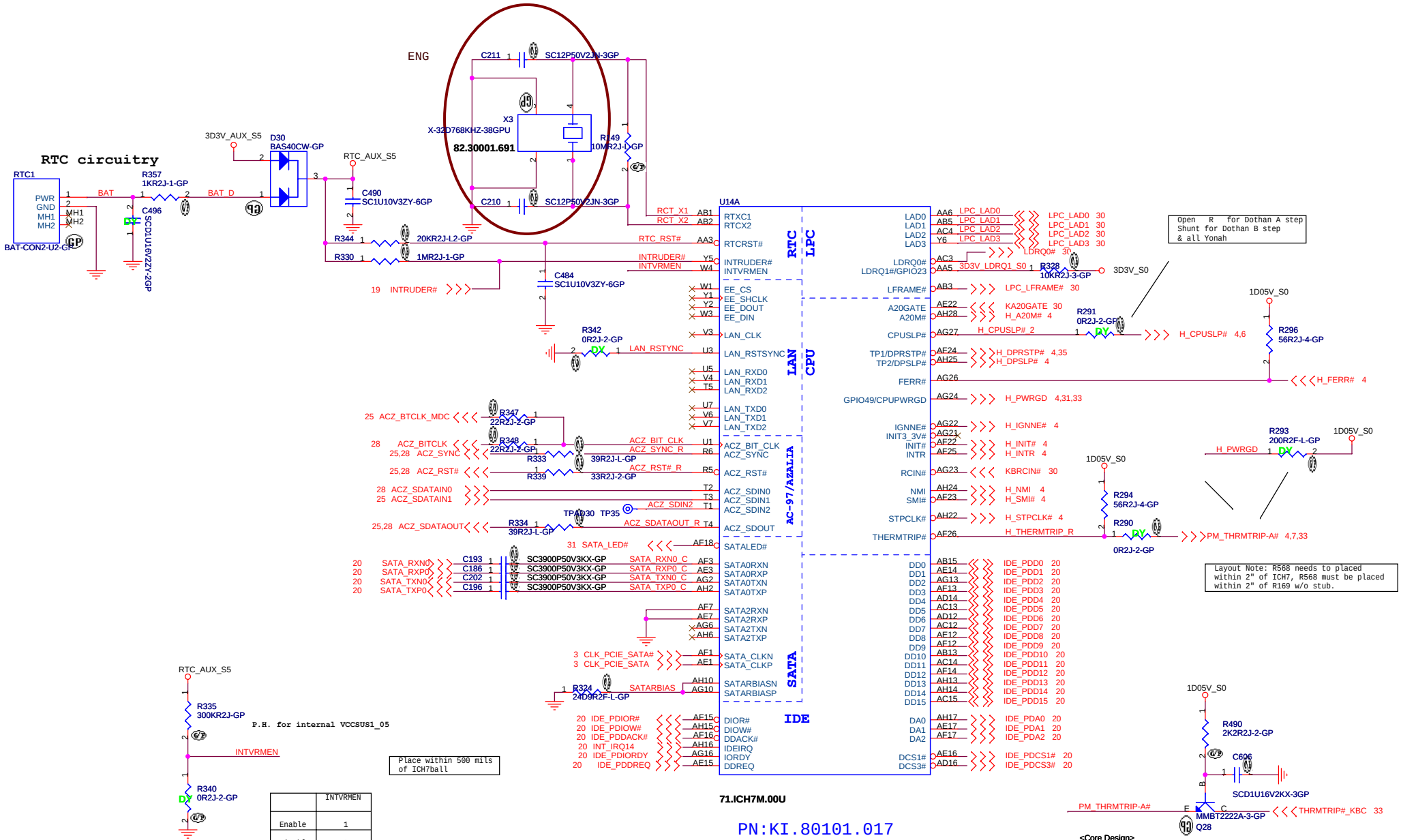
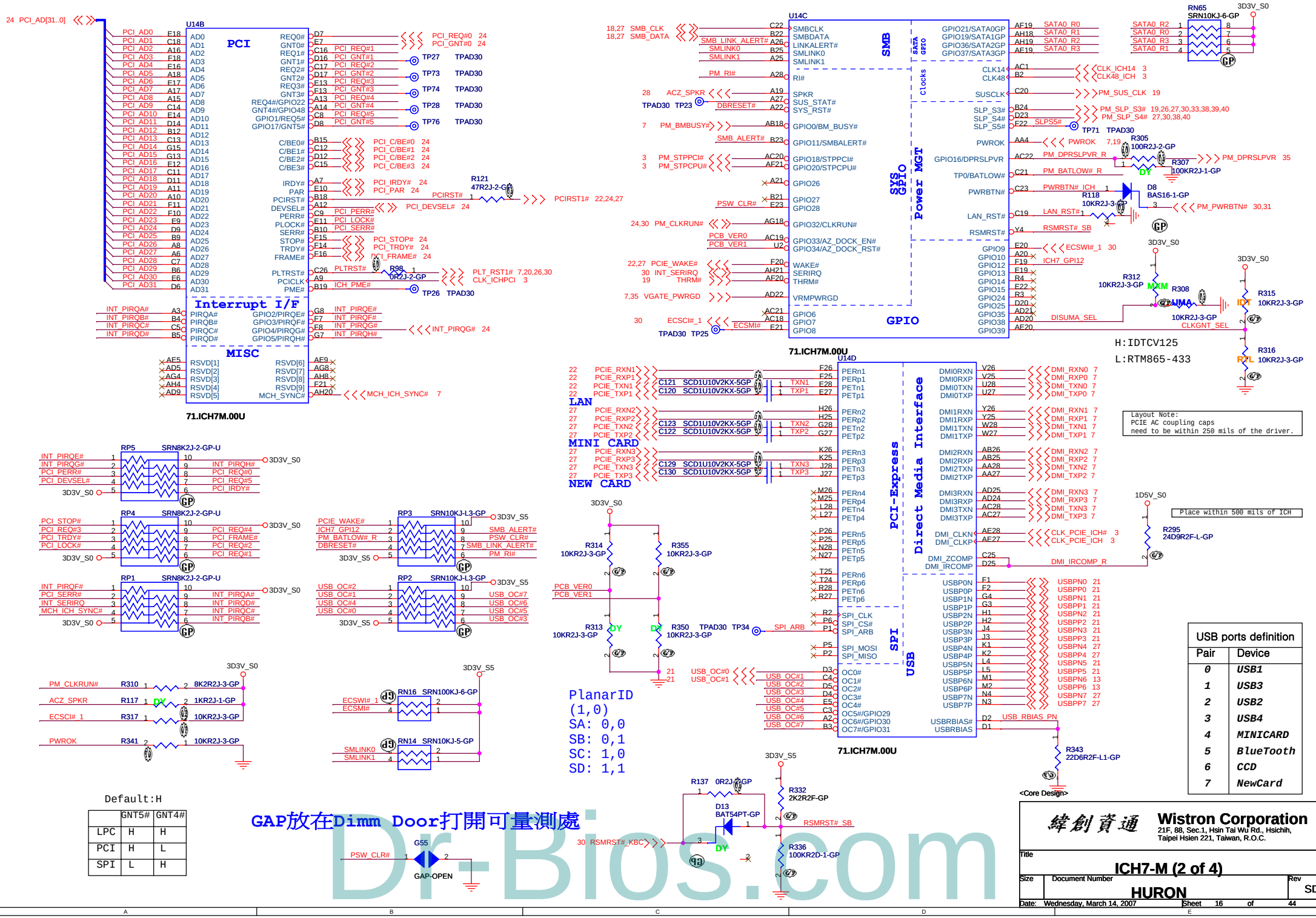
CRT I/F & CONNECTOR



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT/TV Connector	
Size	Document Number: HURON	Rev: SD
Date: Monday, March 12, 2007	Sheet 14 of 44	


RTC circuitry
ENG
X3
X-32D768KHZ-38GPU
82.30001.691
C211 SC12P50V2JN-3GP
C210 SC12P50V2JN-3GP
R149 10MR2J-L-GP
RTC1
BAT-CON2-U2-GP
R357 1KR2J-1-GP
C496 SCD1U16V2ZY-2GP
D30 BAS40CW-GP
3D3V_AUX_S5
RTC_AUX_S5
C490 SC1U10V3ZY-6GP
R344 20KR2J-L2-GP
R330 1MR2J-1-GP
C484 SC1U10V3ZY-6GP
R342 0R2J-2-GP
U14A
RTC
LPC
LAN
CPU
AC-97/AZALIA
IDE
SATA
RTCRST#
INTRUDER#
INTVRMEN
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
Open R for Dothan A step
Shunt for Dothan B step
& all Yonah
R328 10KR2J-3-GP
R291 0R2J-2-GP
R296 56R2J-4-GP
R293 200R2F-L-GP
R294 56R2J-4-GP
R290 0R2J-2-GP
Layout Note: R568 needs to placed within 2" of ICH7, R568 must be placed within 2" of R169 w/o stub.
R335 300KR2J-GP
P.H. for internal VCCSUS1_05
R340 0R2J-2-GP
INTVRMEN
Enable 1
Disable 0
Place within 500 mils of ICH7ball
R324 24D9R2F-L-GP
R490 2K2R2J-2-GP
C606 SCD1U16V2KX-3GP
MMBT2222A-3-GP Q28
Placement Note:
Diatance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.
71.ICH7M.00U
PN:KI.80101.017
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (1 of 4)
Size
Document Number
HURON
Rev
SD
Date: Monday, March 12, 2007
Sheet 15 of 44


U14B
PCI
Interrupt I/F
MISC
71.ICH7M.00U
U14C
SMB
SYS MGT
Power MGT
GPIO
71.ICH7M.00U
U14D
LAN
MINI CARD
NEW CARD
PCI-Express
Direct Media Interface
SPI
USB
71.ICH7M.00U
H:IDTCV125
L:RTM865-433
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 1,0
SD: 1,1
USB ports definition
Pair | Device
0 USB1
1 USB3
2 USB2
3 USB4
4 MINICARD
5 BlueTooth
6 CCD
7 NewCard
Default:H
GNT5# GNT4#
LPC H H
PCI H L
SPI L H
GAP放在Dimm Door打開可量測處
GAP-OPEN
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size
Document Number
HURON
Rev
SD
Date: Wednesday, March 14, 2007
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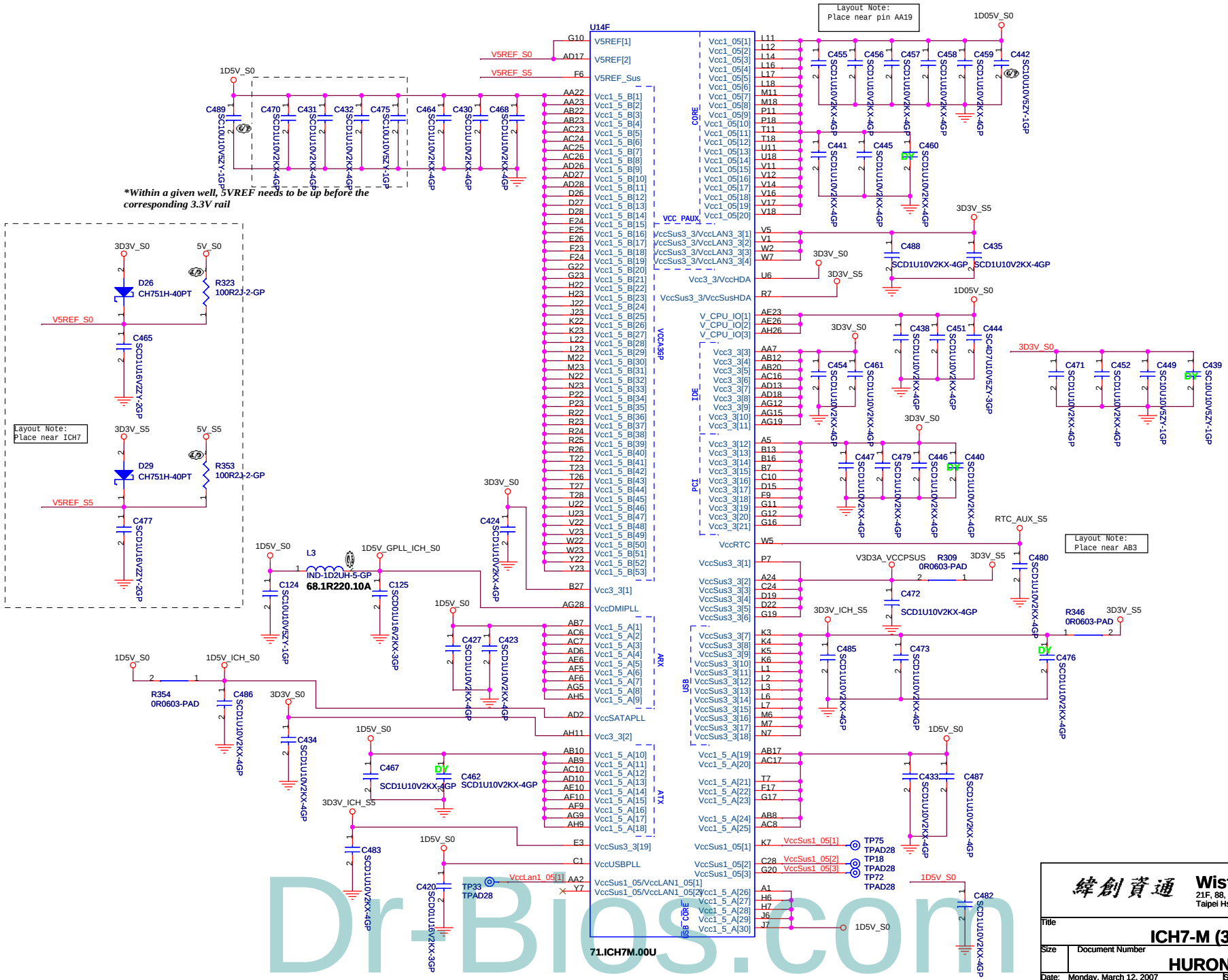
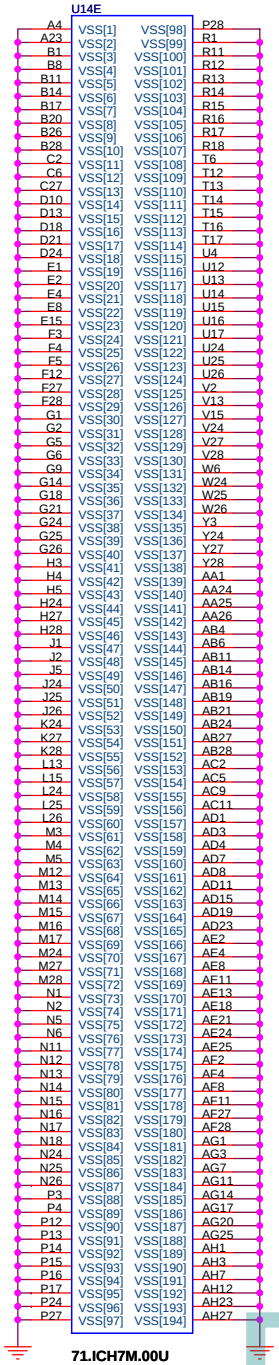
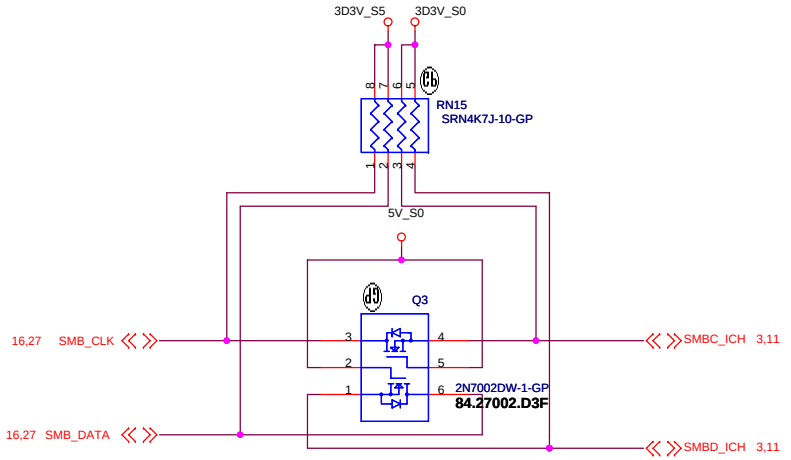


緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ICH7-M (3 of 4)**
Size	Document Number: **HURON**
Rev	SD
Date: Monday, March 12, 2007	Sheet 17 of 44





Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

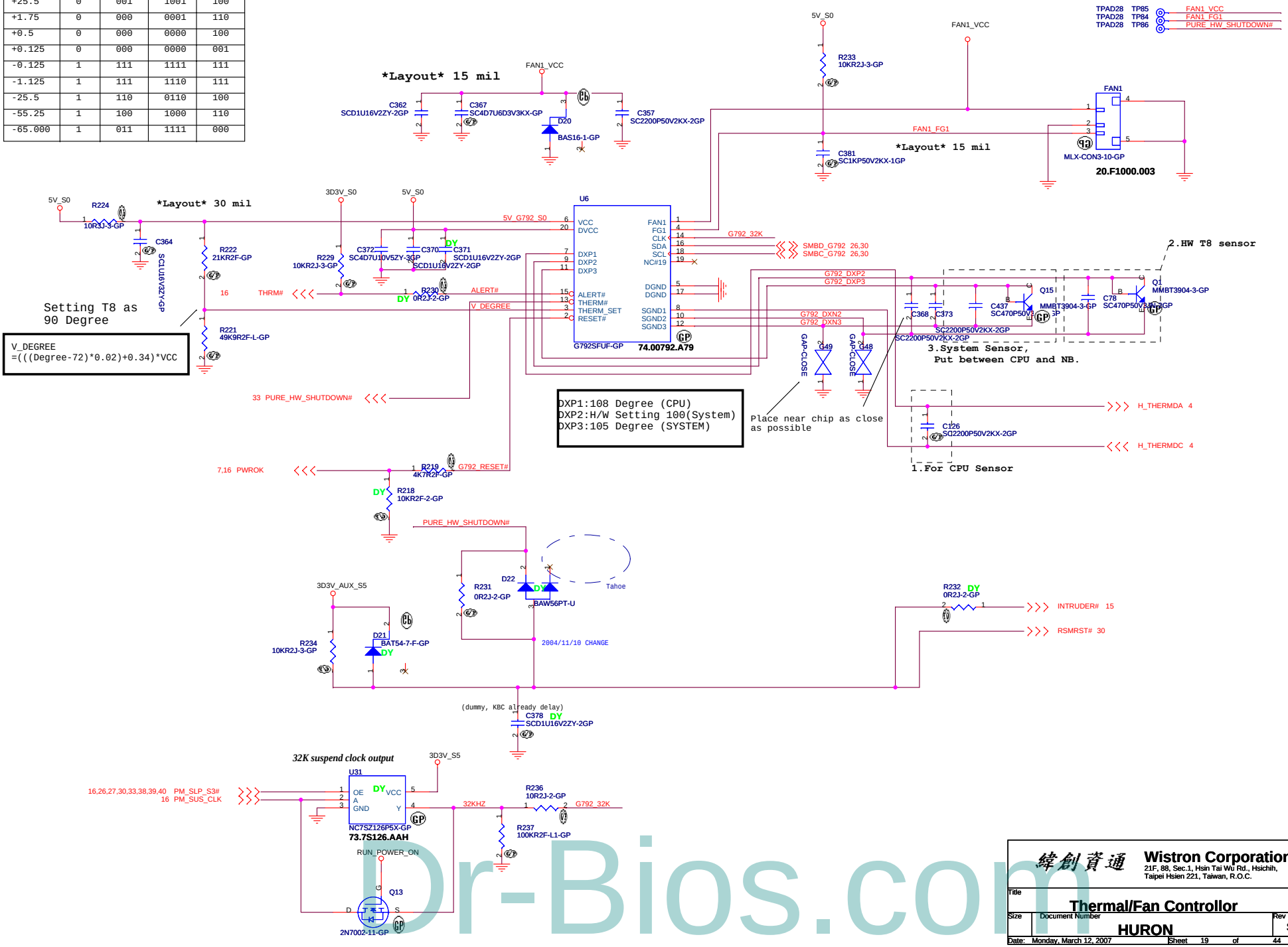
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH7-M (4 of 4)**

Size | Document Number: **HURON** | Rev: SD

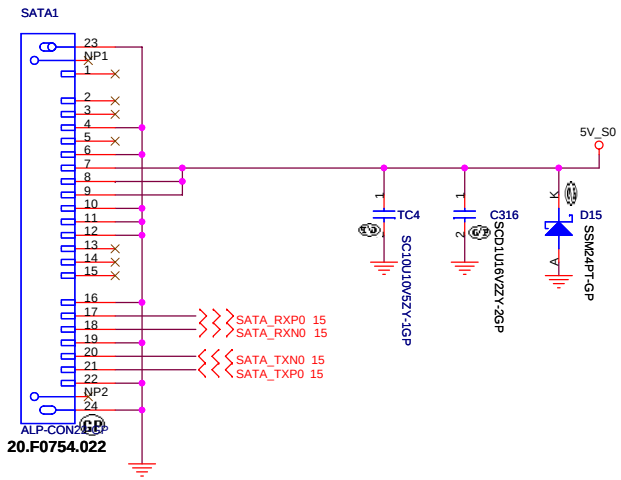
Date: Monday, March 12, 2007 | Sheet 18 of 44

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

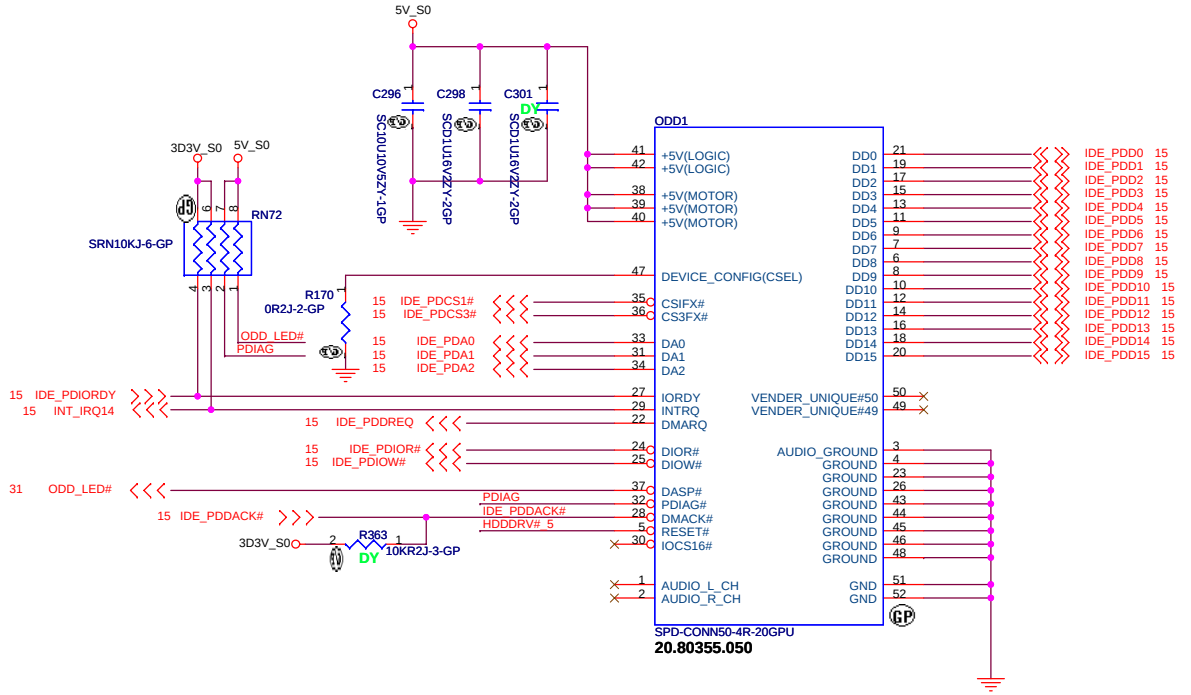


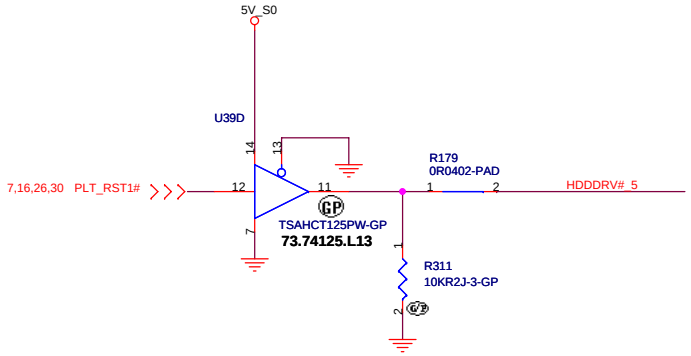
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Thermal/Fan Controllor		
Size	Document Number: HURON	Rev: SD
Date: Monday, March 12, 2007	Sheet 19 of 44	

SATA HD Connector



ODD Connector





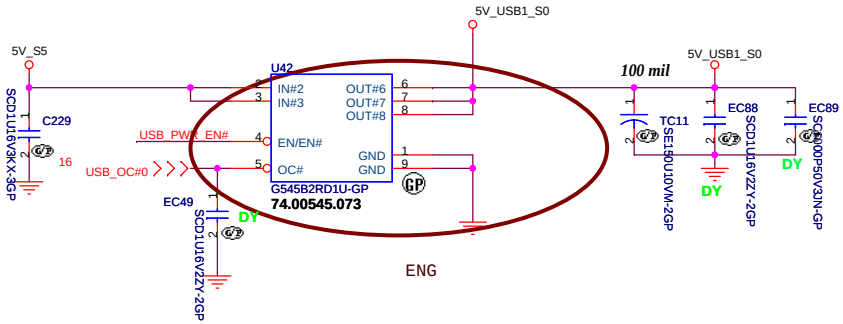
<Core Design>

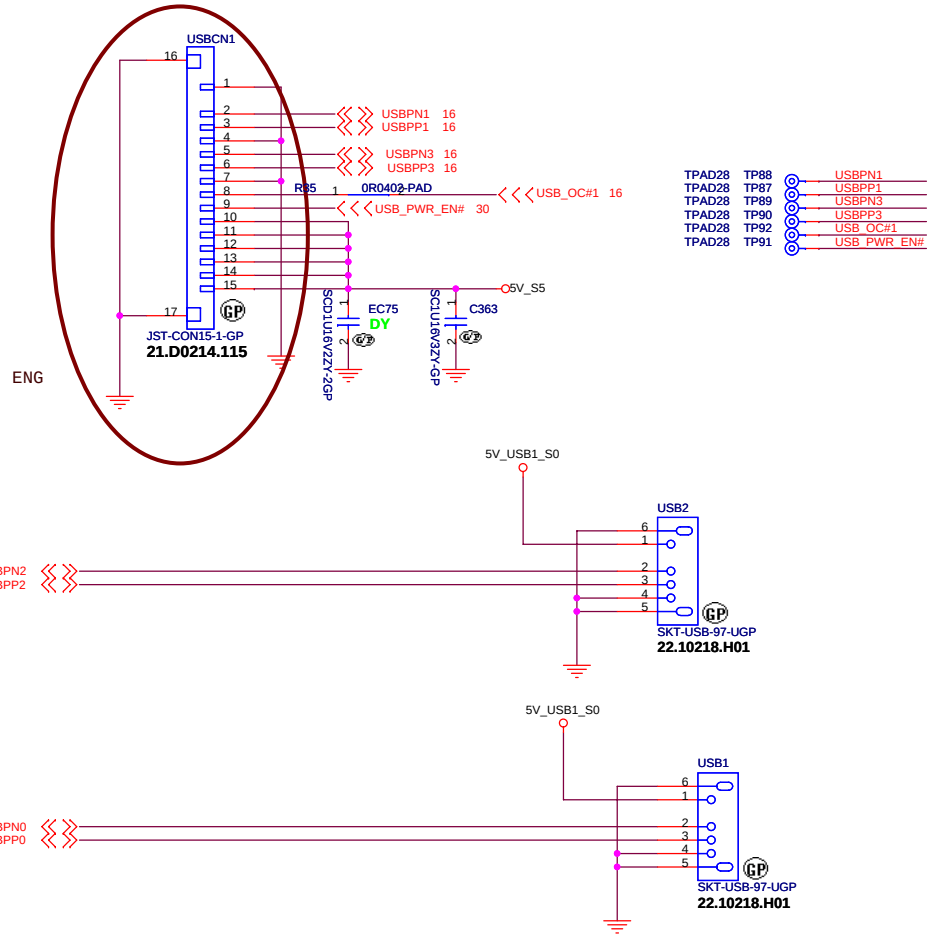
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD and CDROM

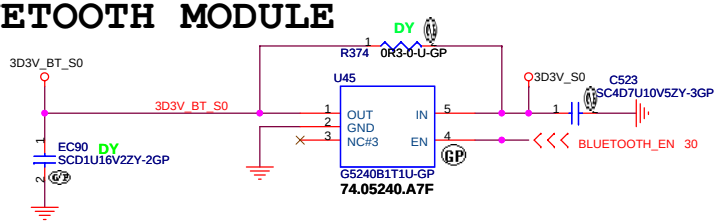
Size	Document Number	Rev
	HURON	SD

Date: Monday, March 12, 2007 Sheet 20 of 44

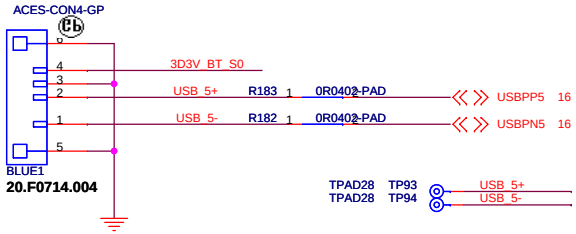




BLUETOOTH MODULE



EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



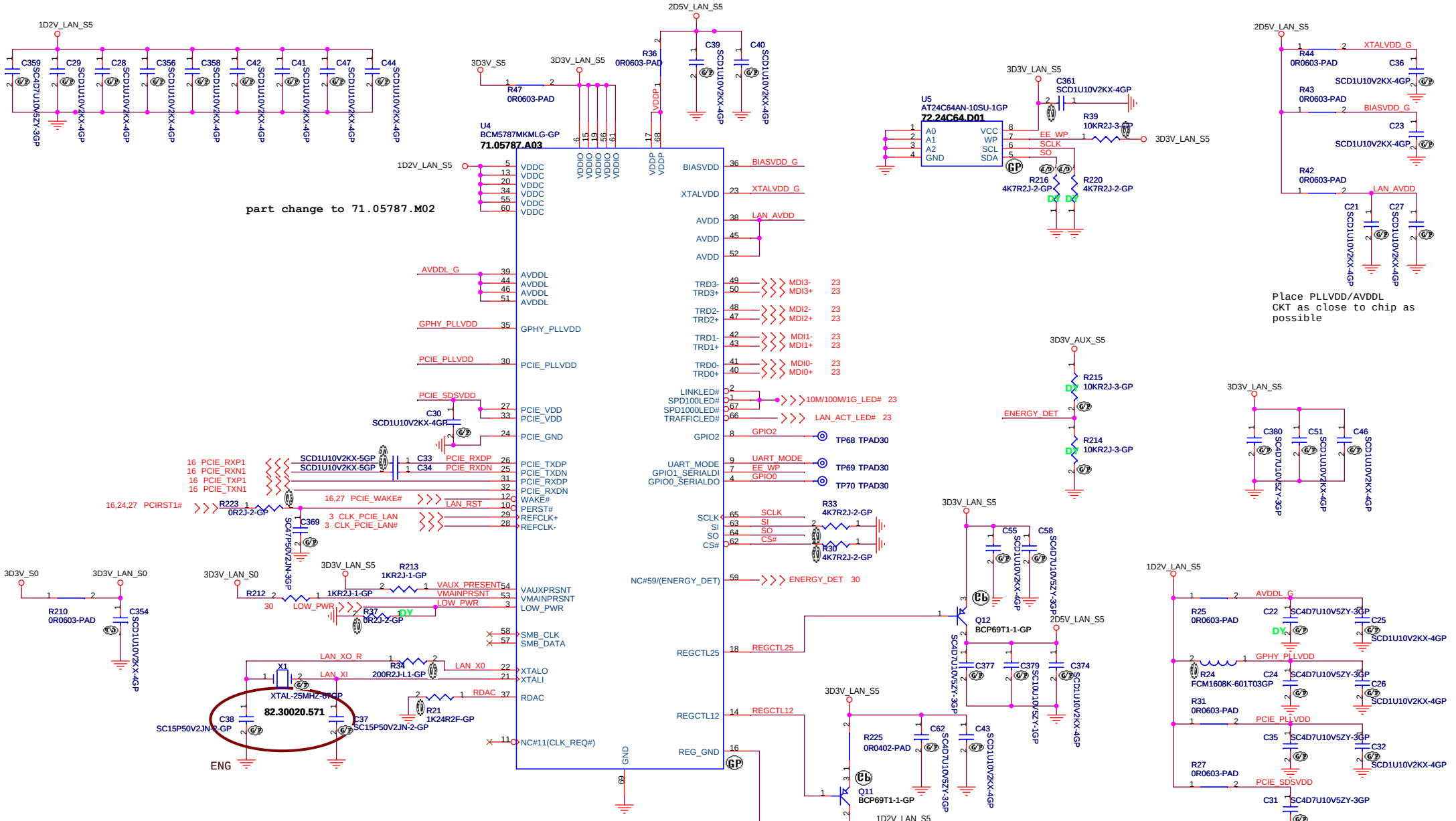
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB / BLUETOOTH

Size | Document Number: HURON | Rev: SD

Date: Tuesday, March 13, 2007 | Sheet 21 of 44



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

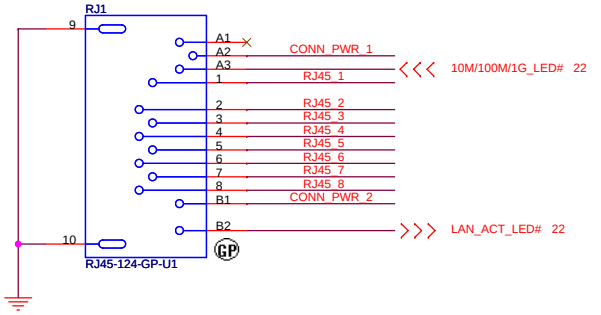
Title: LAN BCM5787

Size: A3 | Document Number: HURON | Rev: SD

Date: Monday, March 19, 2007 | Sheet 22 of 44

LAN Connector

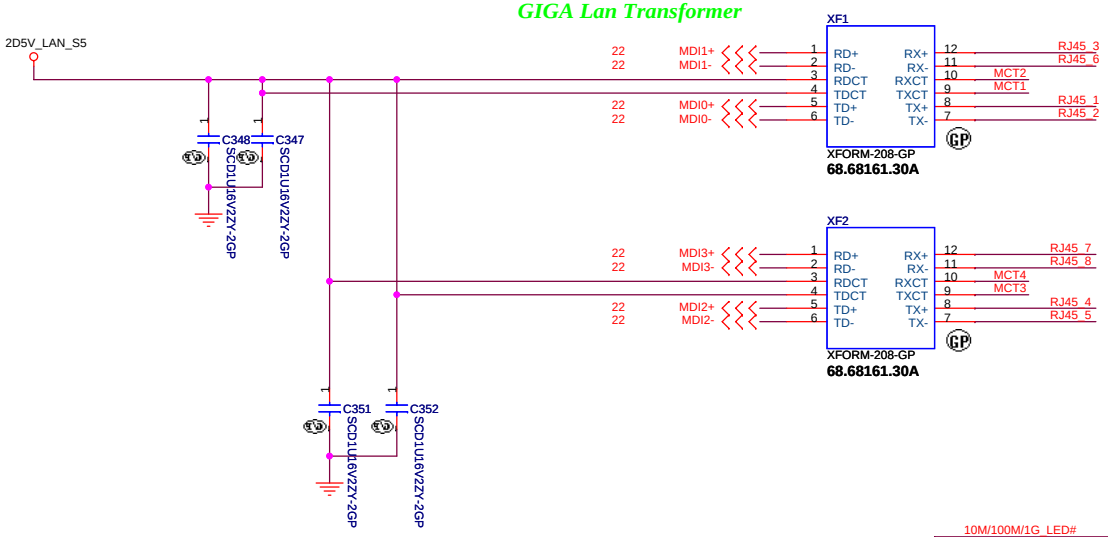
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

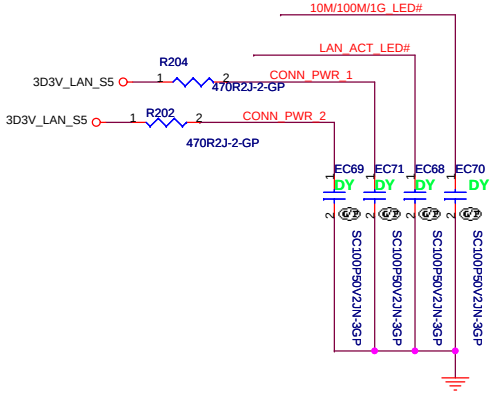


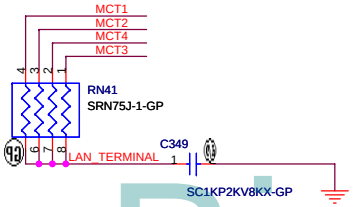
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

GIGA Lan Transformer







1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Core Design>

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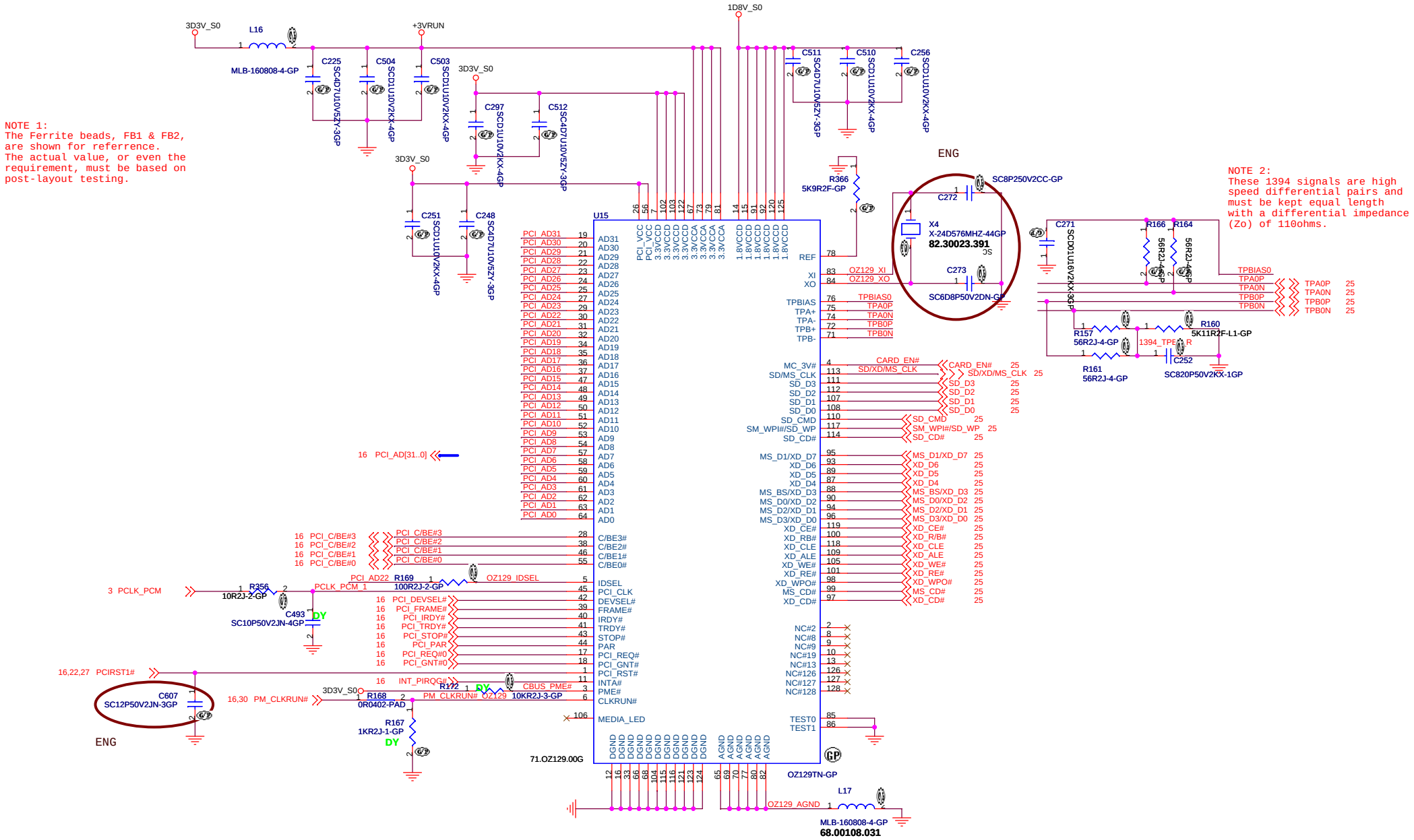
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 | Document Number: HURON | Rev: SD
Date: Monday, March 19, 2007 | Sheet 23 of 44



<Core Design>
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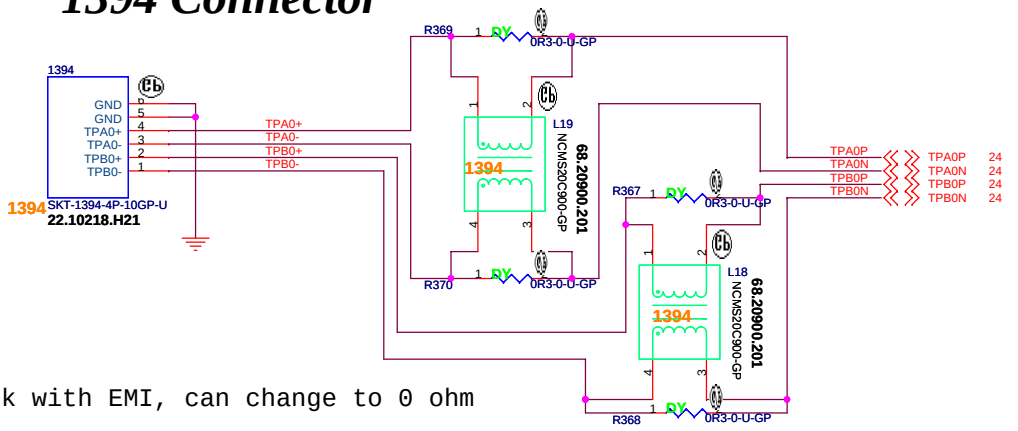
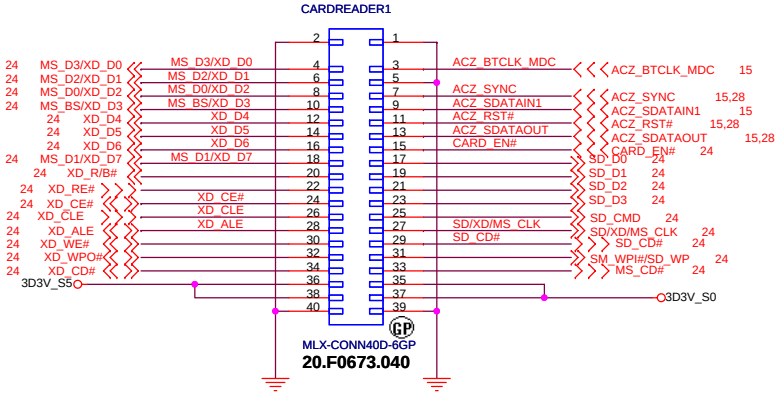
Taipei Hsien 221, Taiwan, R.O.C.

Title: OZ129T
Size: Document Number: HURON
Rev: SD
Date: Monday, March 19, 2007 Sheet 24 of 44

1394 Connector



check with EMI, can change to 0 ohm



CONN on Bottom side

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**1394 / CARD READER BD**
Size	Document Number: **HURON** — Rev: SD
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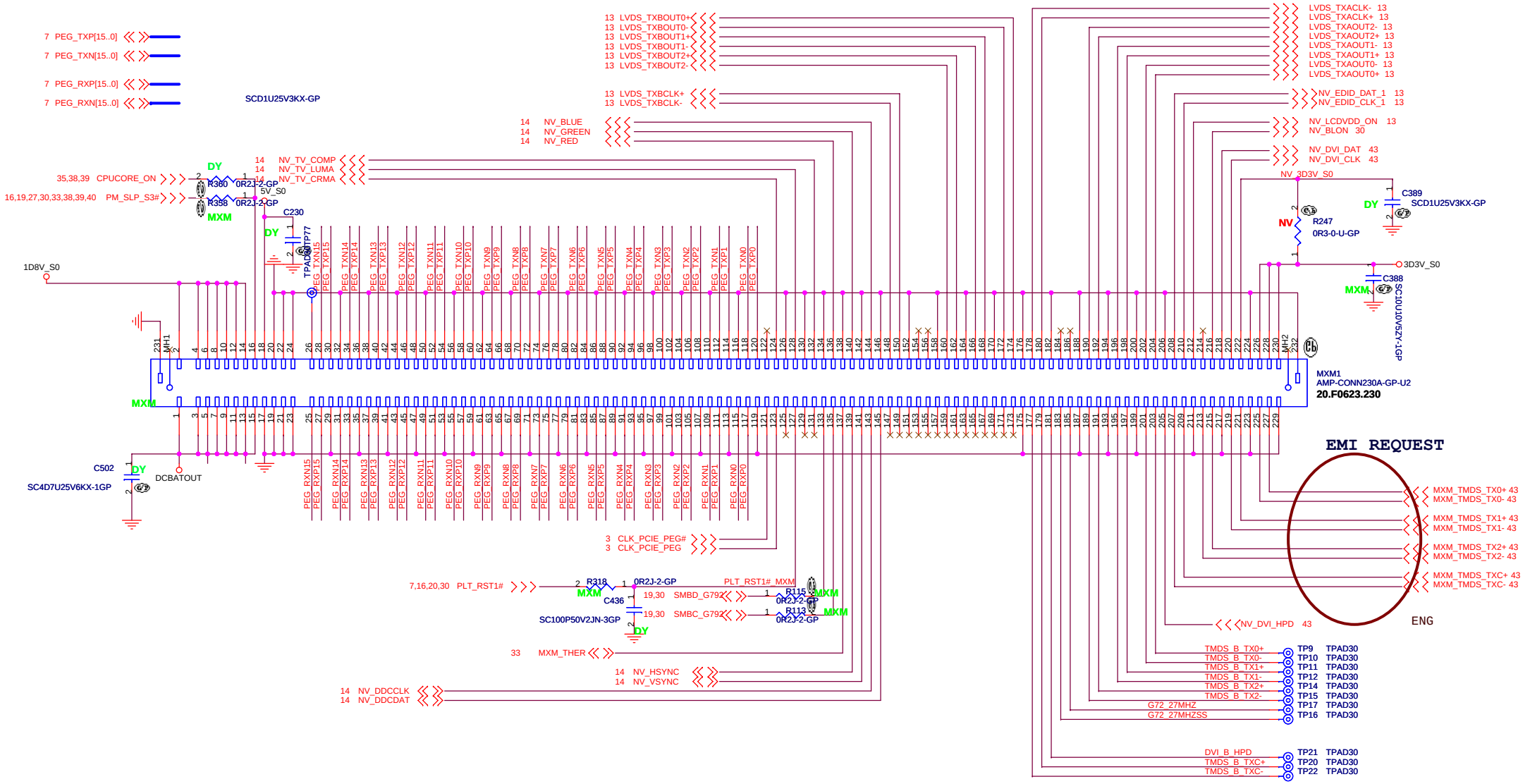
NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Graphic MXM CONN

Size: A3 | Document Number: HURON | Rev: SD

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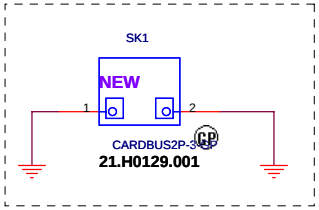
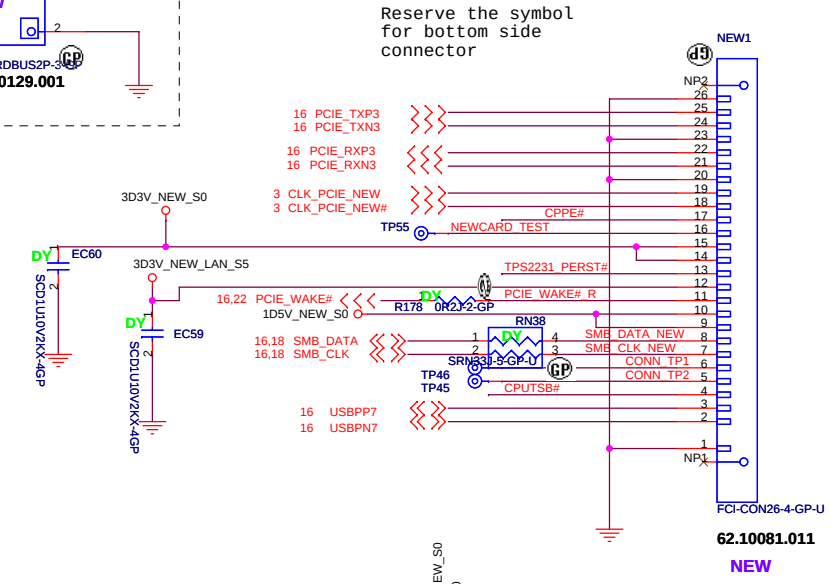
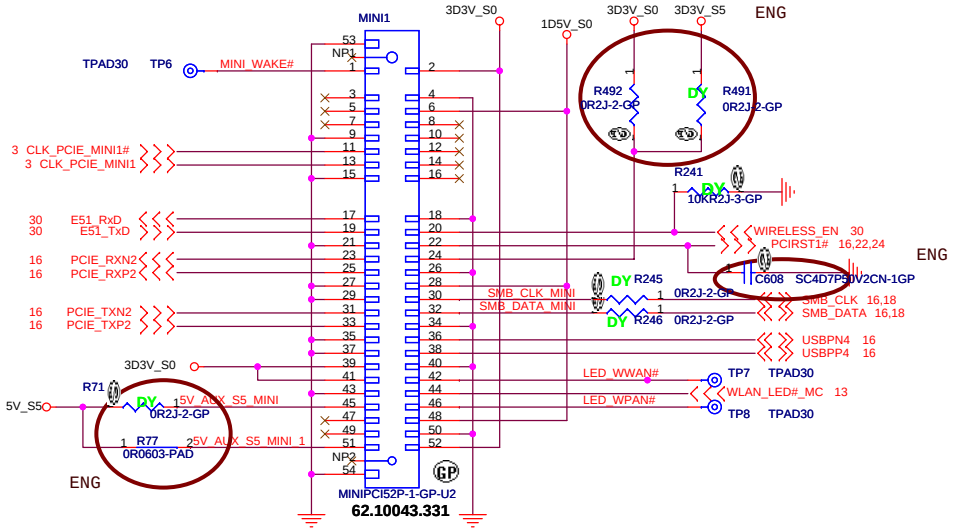
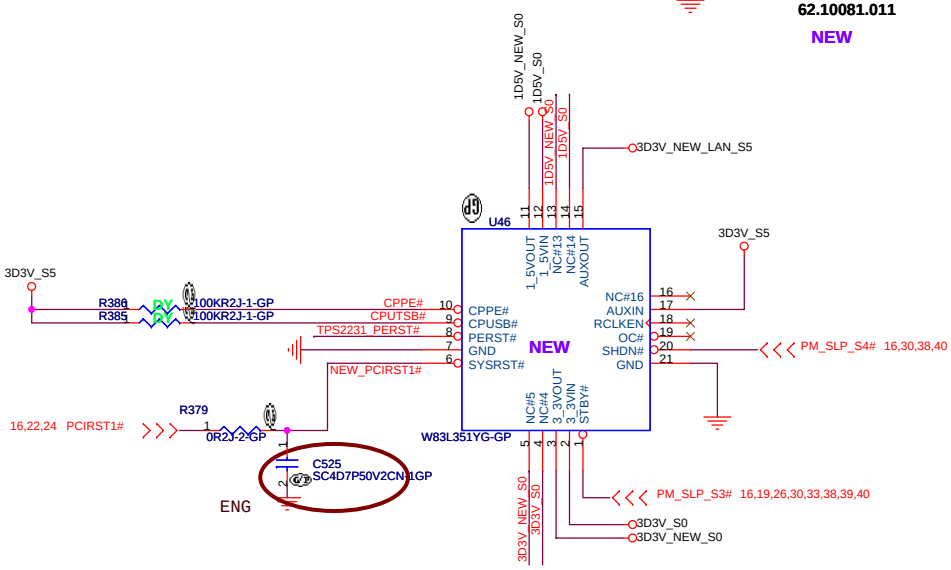
NEWCARD Connector

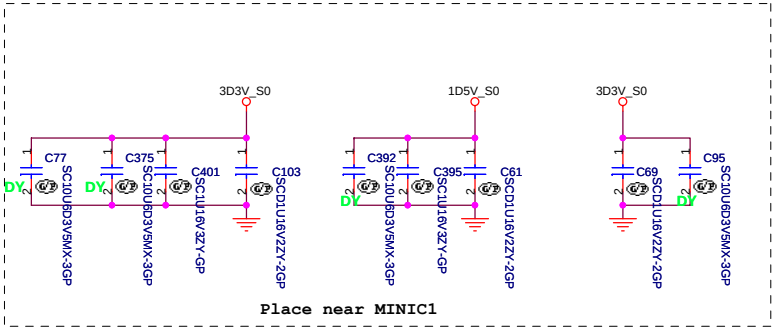


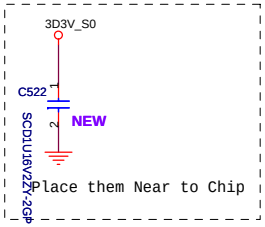


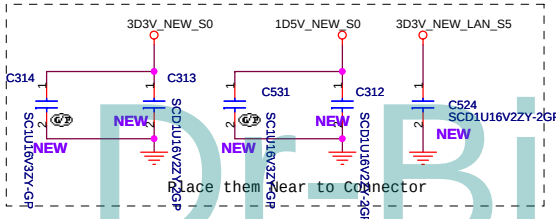
Mini Card Connector











<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / NEW CARD

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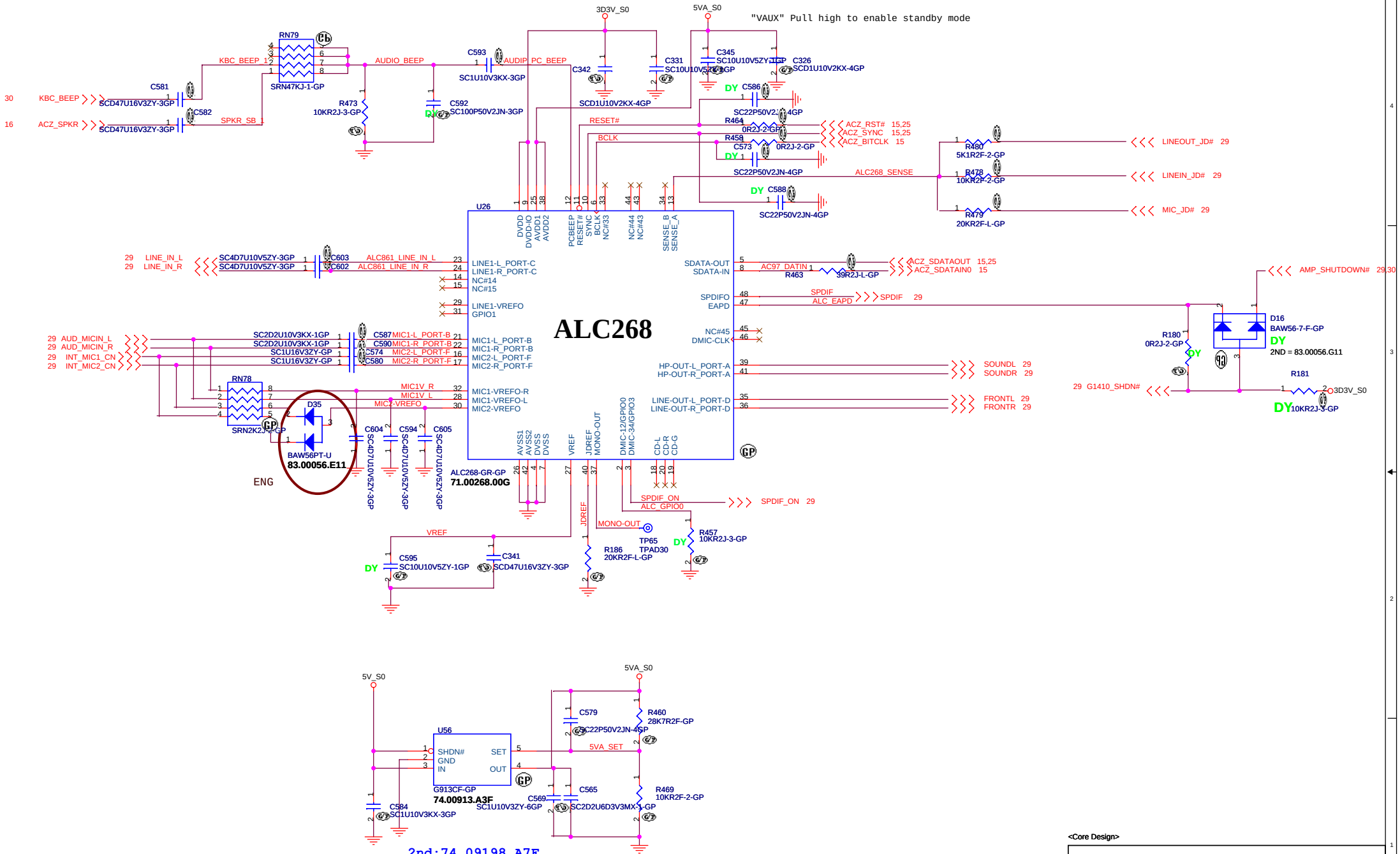

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: AZALIA CODEC - ALC268

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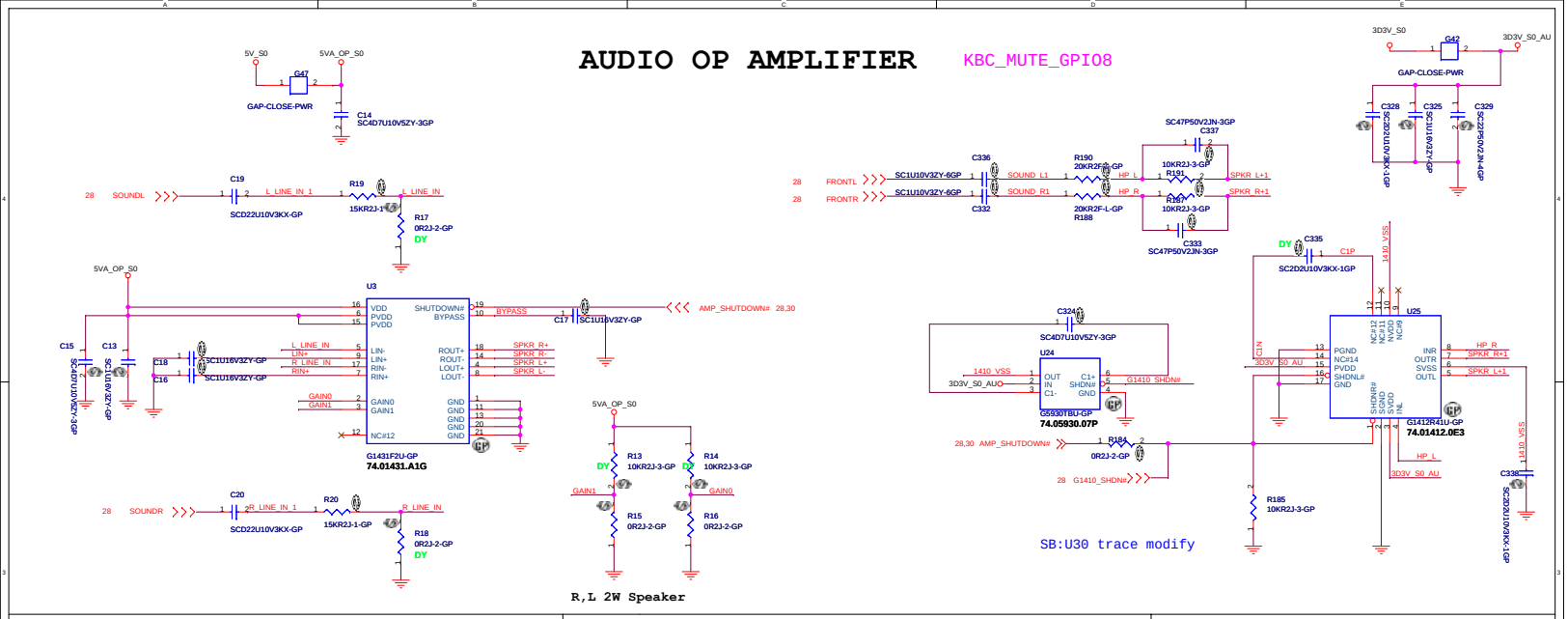
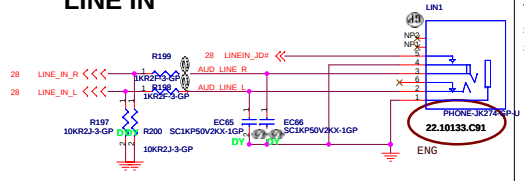
AUDIO OP AMPLIFIER

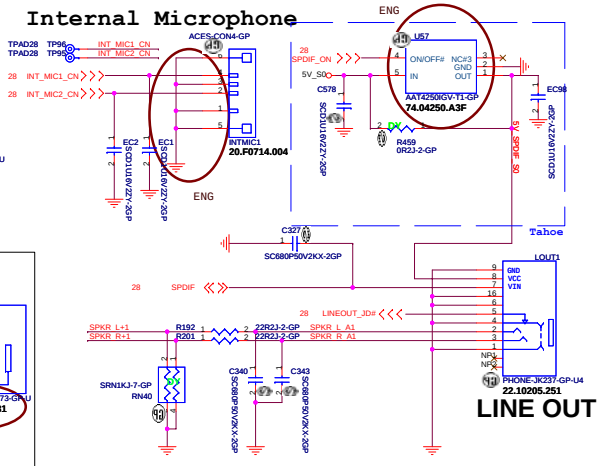
KBC_MUTE_GPIO8



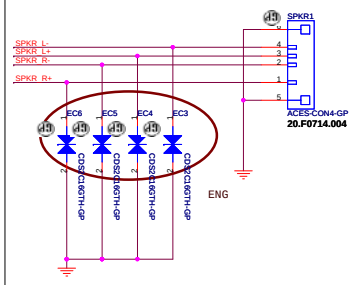
LINE IN



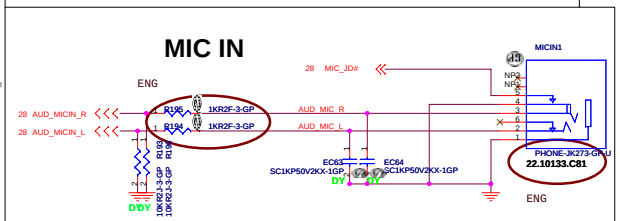
Internal Microphone



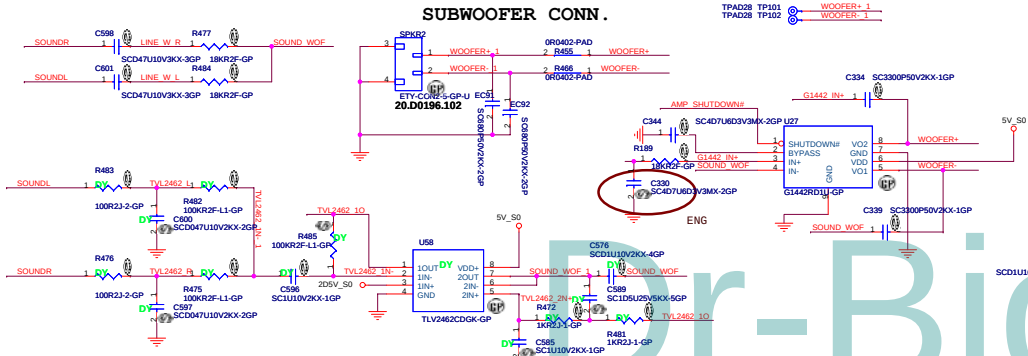
Internal Speaker



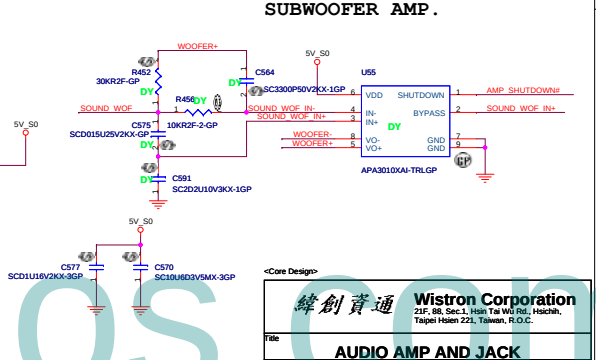
MIC IN



SUBWOOFER CONN.



SUBWOOFER AMP.



<Core Design>
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Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO AMP AND JACK
Size
Document Number
HURON
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SD
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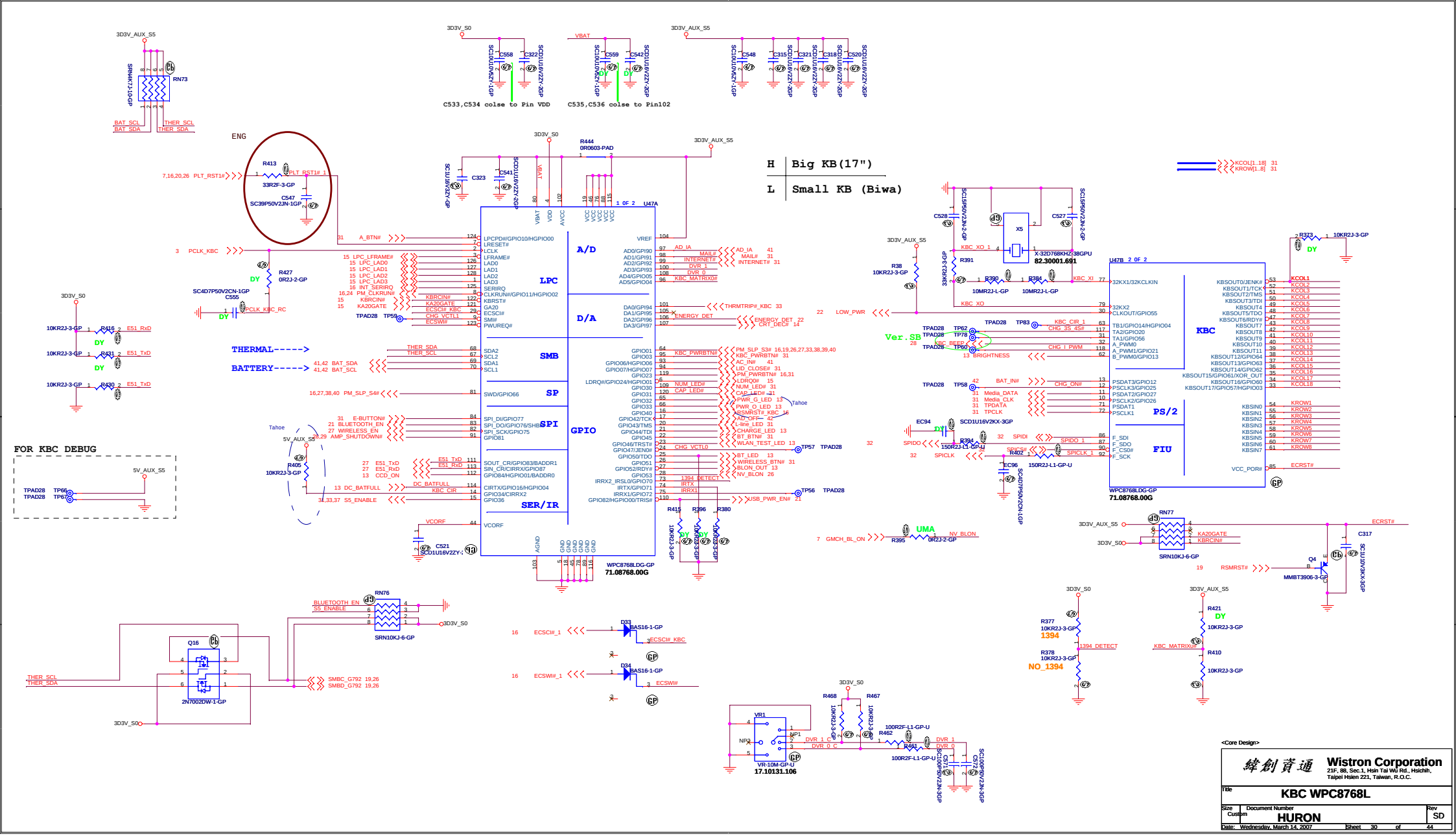
H | Big KB(17")
L | Small KB (Biwa)
ENG
FOR KBC DEBUG
C533,C534 colse to Pin VDD
C535,C536 colse to Pin102
THERMAL----->
BATTERY----->
Tahoe
UMA
Ver.SB
WPC8768LDG-GP
71.08768.00G
82.30001.691
17.10131.106
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
HURON
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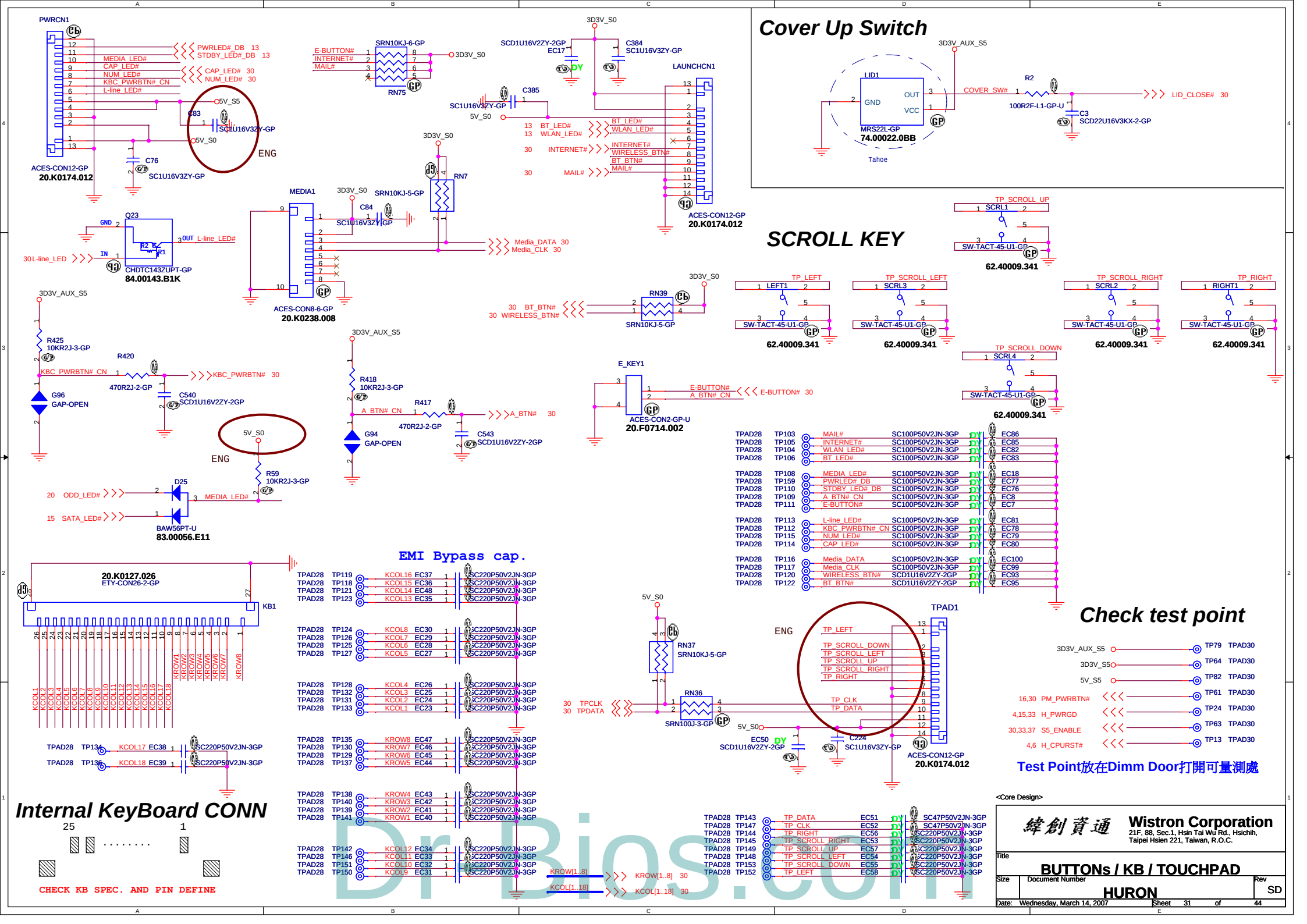
Cover Up Switch
SCROLL KEY
EMI Bypass cap.
Check test point
Internal KeyBoard CONN
Test Point放在Dimm Door打開可量測處
CHECK KB SPEC. AND PIN DEFINE
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Taipei Hsien 221, Taiwan, R.O.C.
BUTTONs / KB / TOUCHPAD
HURON
Date: Wednesday, March 14, 2007
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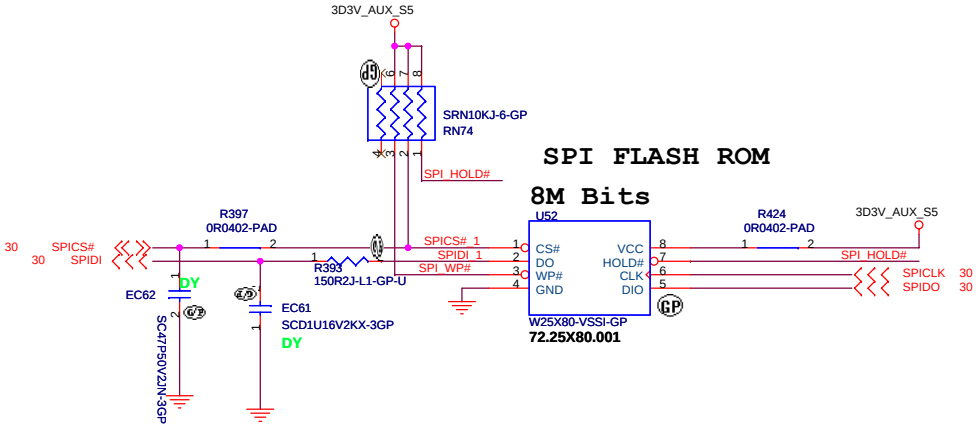
Dr.Bios.com



<Core Design>

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Title: BIOS

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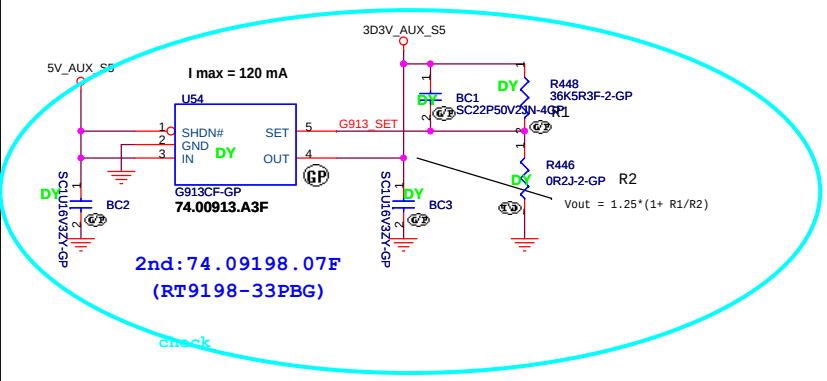
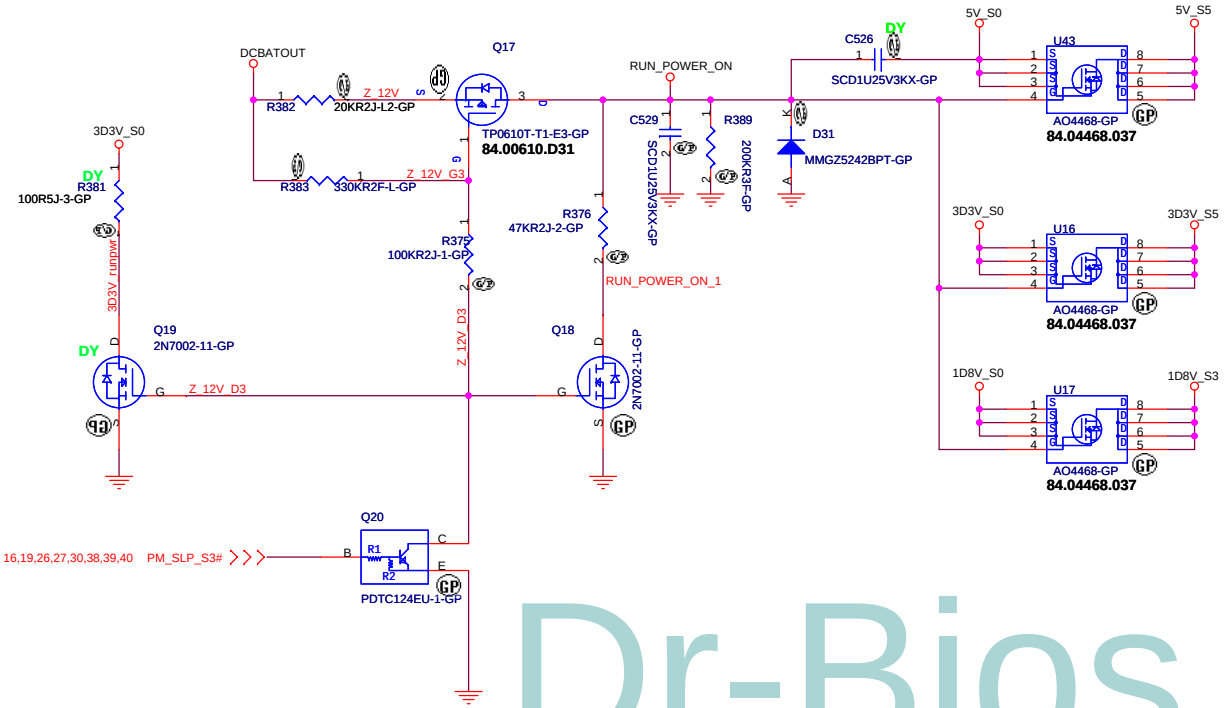
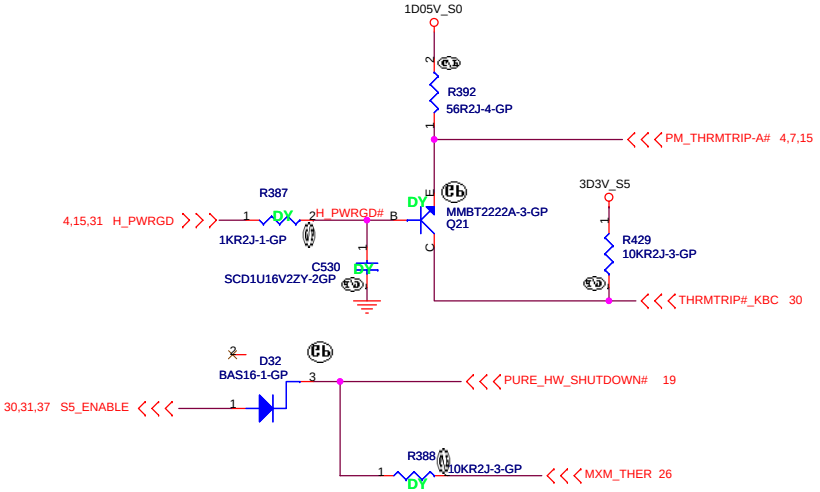
Aux Power 3D3V_AUX_S5



Run Power





<Core Design>

緯創資通 Wistron Corporation
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Title: RUN POWER

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	HURON	SD

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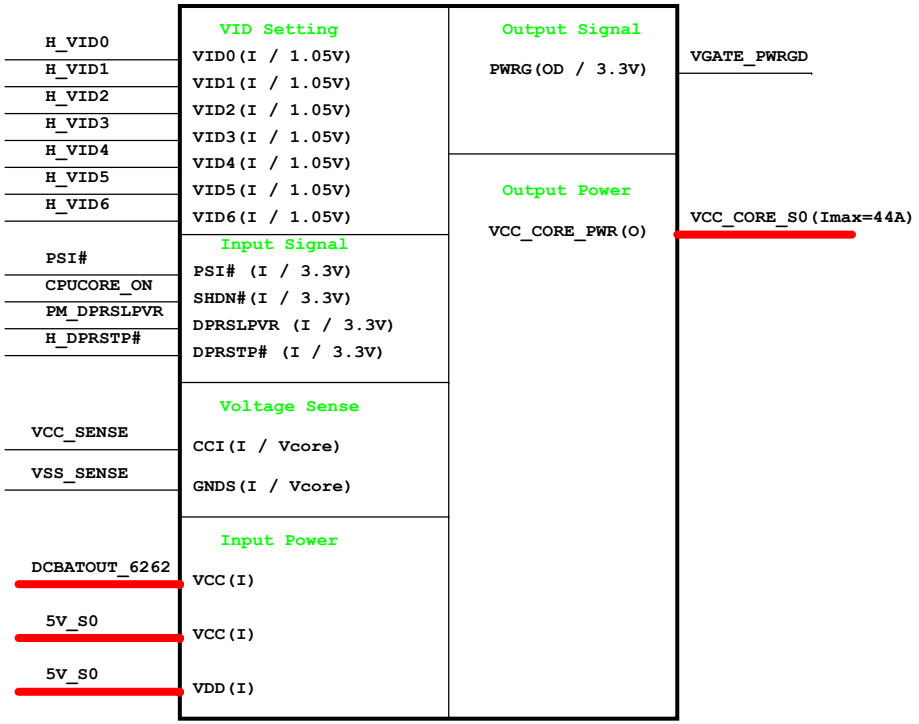
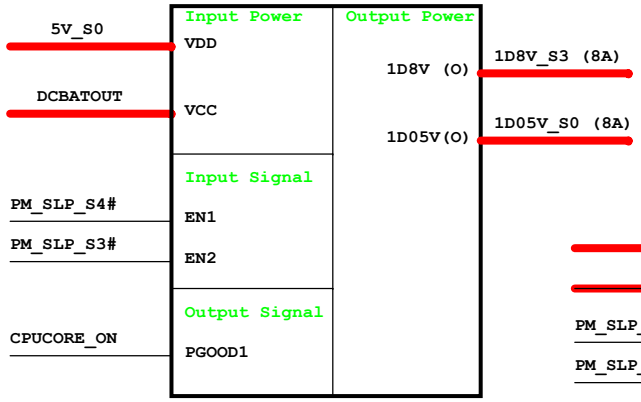
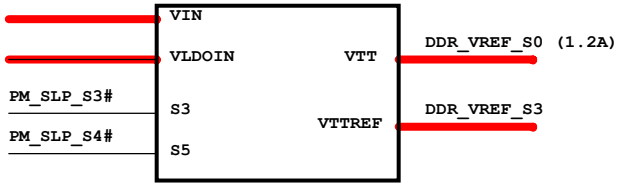
CPU_CORE
ISL6262



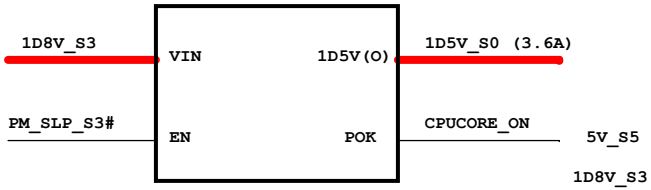
TPS51124
1D8V_S3 / 1D05V_S0



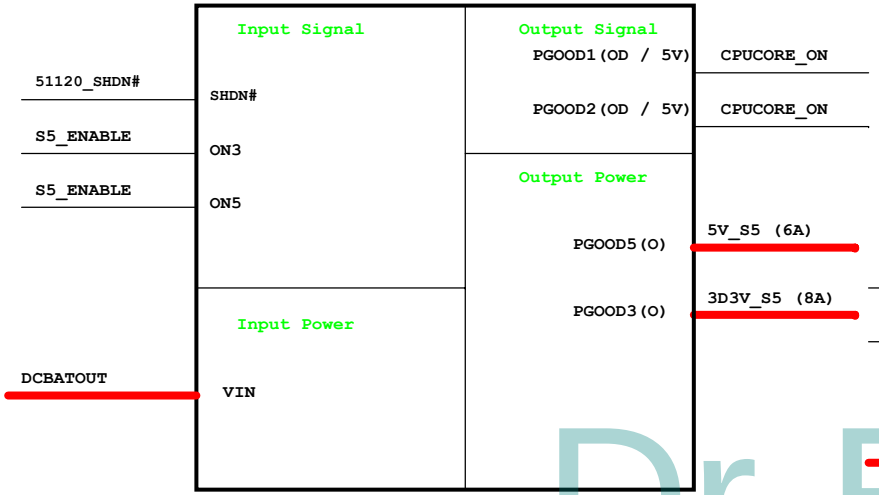
TPS51100
DDR_VREF_S0



APl5912
1D5V_S0

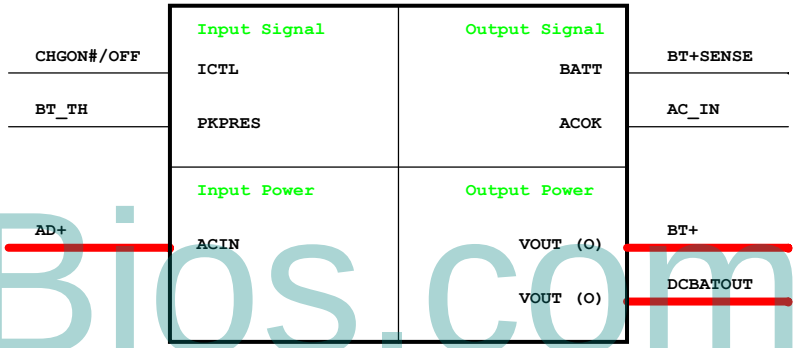


TPS51120
5V_S5 / 3D3V_S5



APL5308
2D5V_S0

Charger MAX8731A



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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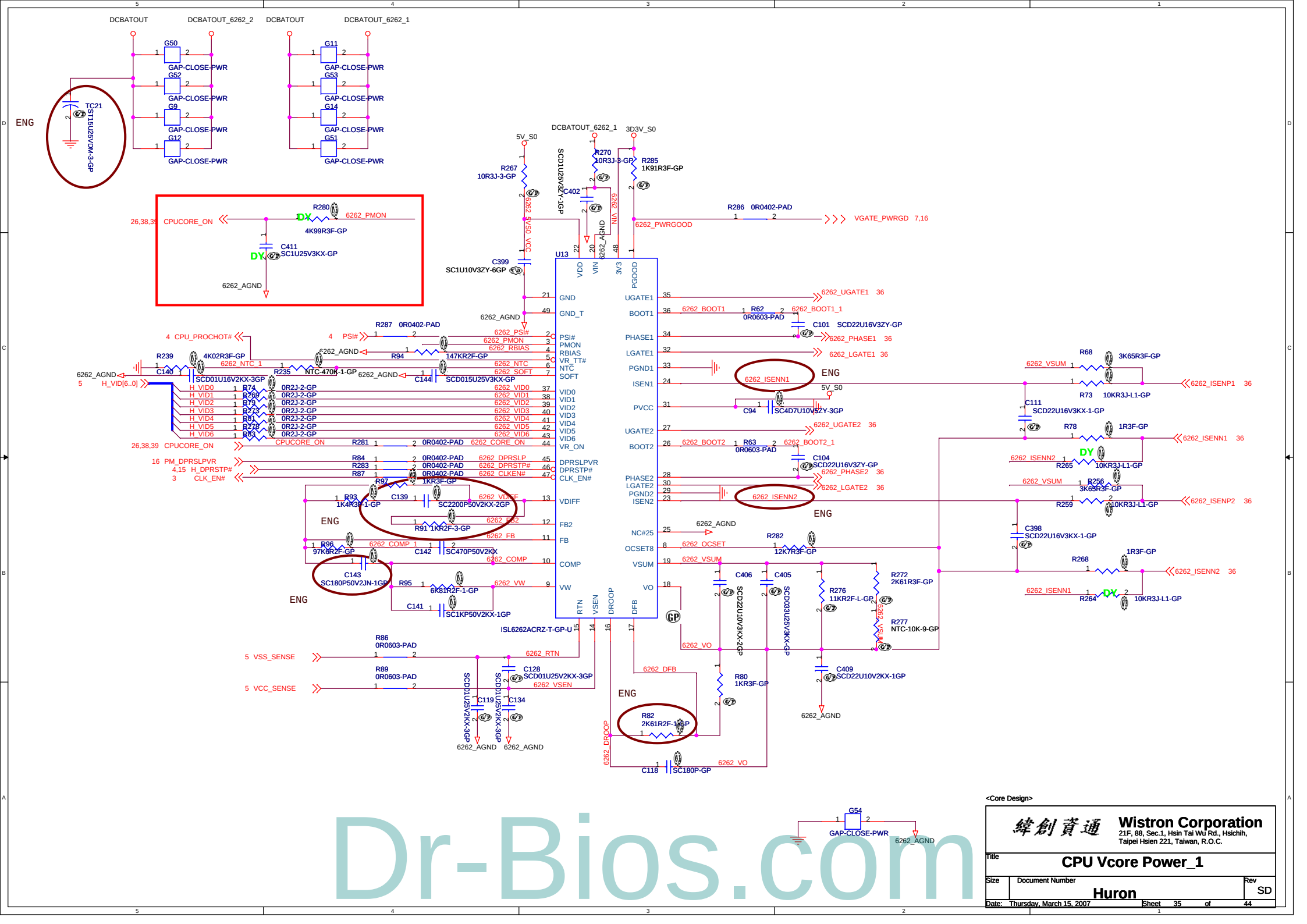
DCBATOUT
DCBATOUT_6262_2
DCBATOUT
DCBATOUT_6262_1
ENG
TC21
ST15U25VDM-3-GP
G50
G52
G9
G12
G11
G53
G14
G51
GAP-CLOSE-PWR
R280
4K99R3F-GP
C411
SC1U25V3KX-GP
CPUCORE_ON
6262_PMON
6262_AGND
5V_S0
3D3V_S0
R267
10R3J-3-GP
R270
10R3J-3-GP
R285
1K91R3F-GP
C402
SCD1U25V2KX-1-GP
R286
0R0402-PAD
VGATE_PWRGD 7,16
6262_PWRGOOD
C399
SC1U10V3ZY-6GP
U13
VDD
VIN
3V3
PGOOD
GND
GND_T
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
DPRSTP#
CLK_EN#
VDIFF
FB2
FB
COMP
VW
RTN
VSEN
DROOP
DFB
UGATE1
BOOT1
PHASE1
LGATE1
PGND1
ISEN1
PVCC
UGATE2
BOOT2
PHASE2
LGATE2
PGND2
ISEN2
NC#25
OCSET8
VSUM
VO
ISL6262ACRZ-T-GP-U
6262_UGATE1
6262_BOOT1
6262_PHASE1
6262_LGATE1
6262_ISENN1
6262_UGATE2
6262_BOOT2
6262_PHASE2
6262_LGATE2
6262_ISENN2
6262_OCSET
6262_VSUM
6262_VO
6262_DFB
6262_DROOP
6262_RTN
6262_VSEN
6262_VDIFF
6262_FB2
6262_FB
6262_COMP
6262_VW
6262_PSI#
6262_RBIAS
6262_NTC
6262_SOFT
6262_VID0
6262_VID1
6262_VID2
6262_VID3
6262_VID4
6262_VID5
6262_VID6
6262_CORE_ON
6262_DPRSLP
6262_DPRSTP#
6262_CLKEN#
6262_VIN
6262_SVSO_VCC
CPU_PROCHOT#
PSI#
H_VID[6..0]
PM_DPRSLPVR
H_DPRSTP#
CLK_EN#
6262_NTC_1
NTC-470K-1-GP
147KR2F-GP
4K02R3F-GP
SCD01U16V2KX-3GP
SCD015U25V3KX-GP
0R2J-2-GP
1KR3F-GP
SC2200P50V2KX-2GP
1K43R3-1-GP
1KR2F-3-GP
97K6R2F-GP
SC470P50V2KX
SC180P50V2JN-1GP
6K81R2F-1-GP
SC1KP50V2KX-1GP
R82
2K61R2F-1-GP
SC180P-GP
R62
0R0603-PAD
C101
SCD22U16V3ZY-GP
C94
SC4D7U10V3ZY-3GP
R63
C104
SCD22U16V3ZY-GP
R282
12K7R3F-GP
C406
C405
SCD22U10V3KX-2GP
SCD033U25V3KX-GP
R272
2K61R3F-GP
R276
11KR2F-L-GP
R277
NTC-10K-9-GP
R80
1KR3F-GP
C409
SCD22U10V2KX-1GP
R86
0R0603-PAD
R89
0R0603-PAD
C128
SCD01U25V2KX-3GP
C119
C134
VSS_SENSE
VCC_SENSE
R68
3K65R3F-GP
R73
10KR3J-L1-GP
C111
SCD22U16V3KX-1-GP
R78
1R3F-GP
R265
10KR3J-L1-GP
R256
3K65R3F-GP
R259
10KR3J-L1-GP
C398
SCD22U16V3KX-1-GP
R268
1R3F-GP
R264
10KR3J-L1-GP
6262_ISENP1
6262_ISENP2
6262_ISENN1
6262_ISENN2
G54
GAP-CLOSE-PWR
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Vcore Power_1
Size
Document Number
Huron
Rev
SD
Date: Thursday, March 15, 2007
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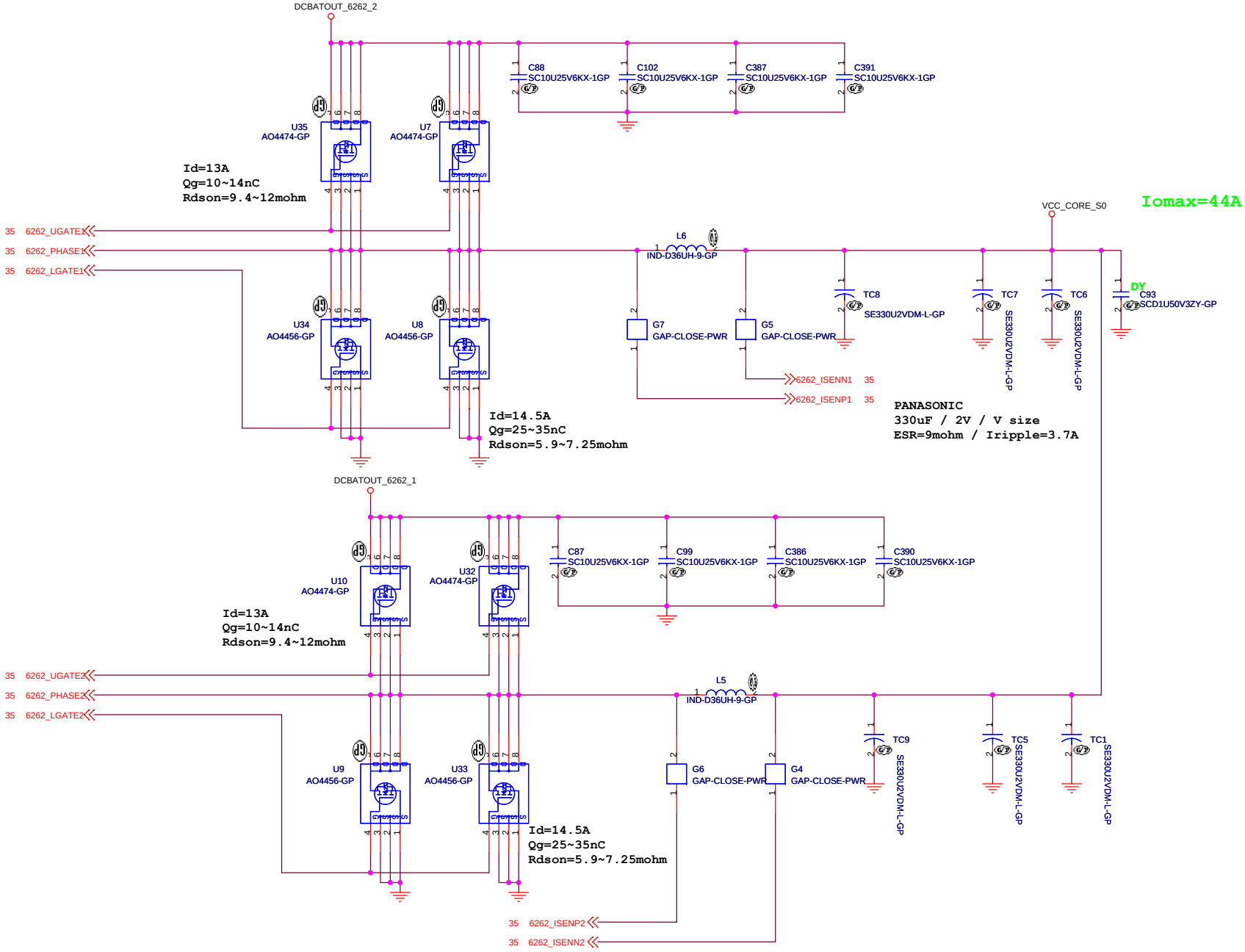

<Core Design>

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Title: CPU Vcore Power_2

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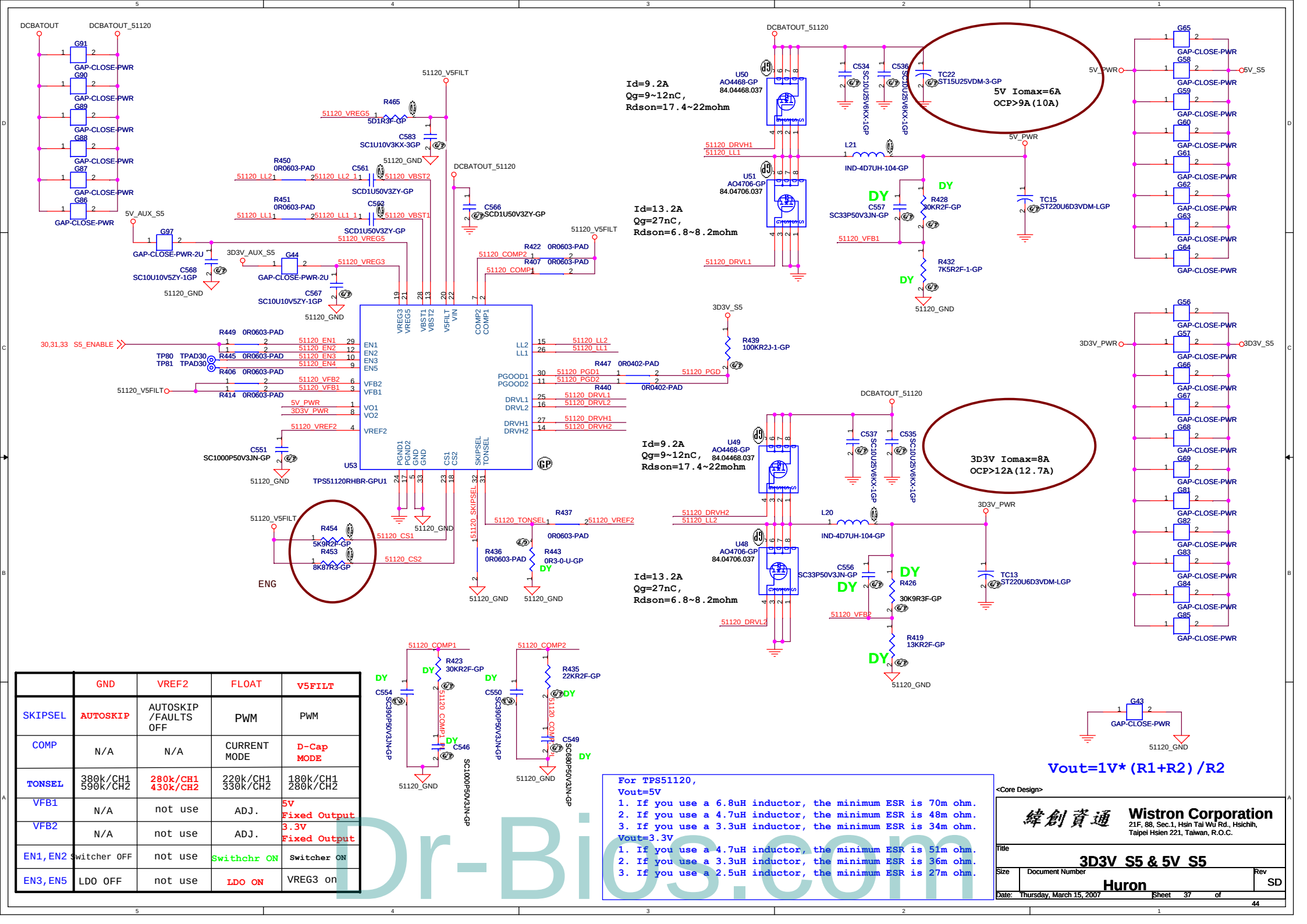

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

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Title: 3D3V_S5 & 5V_S5

Size | Document Number: Huron | Rev: SD

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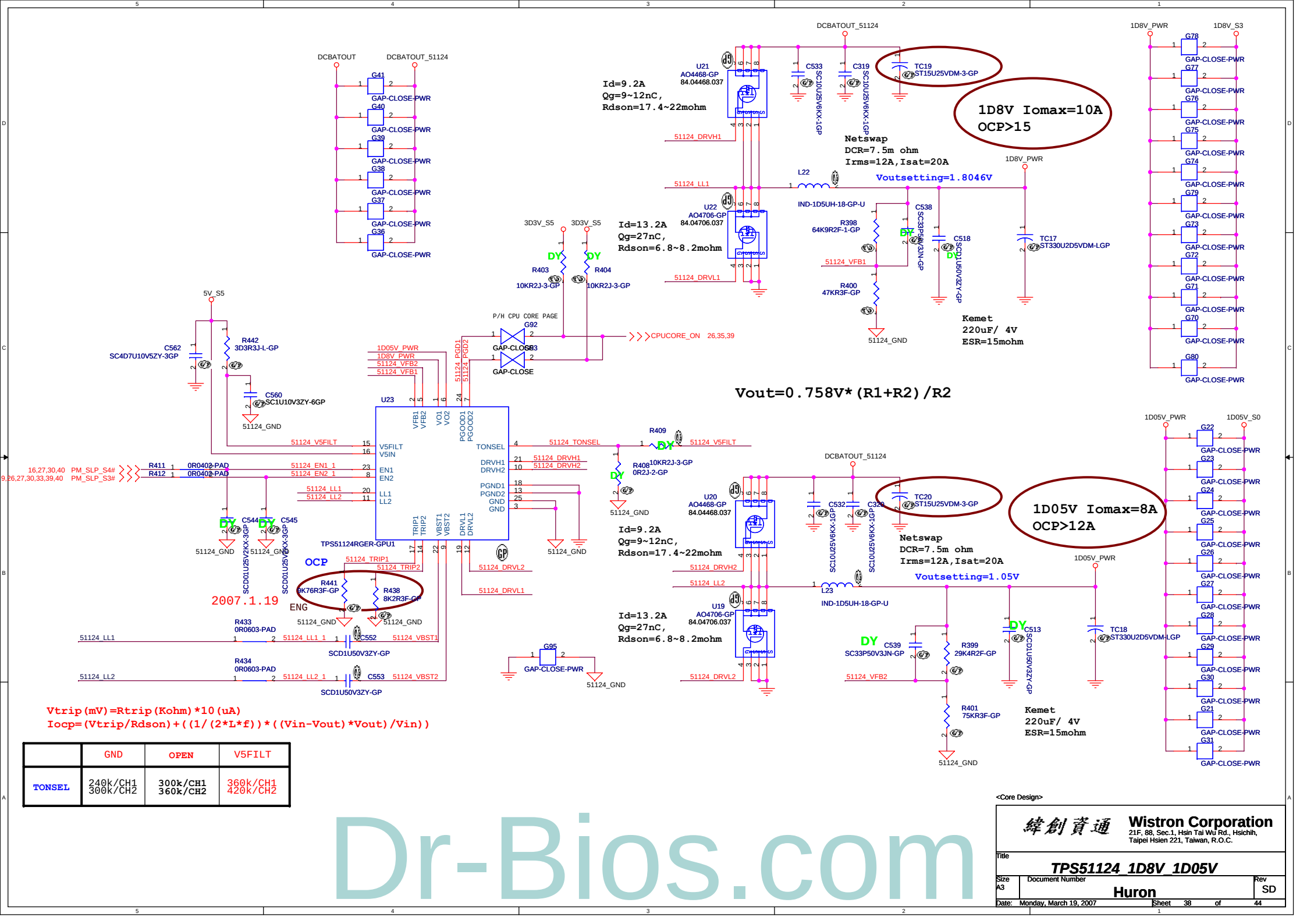
<Core Design>



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

<Core Design>

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Title: TPS51124_1D8V_1D05V

Size: A3 | Document Number: Huron | Rev: SD

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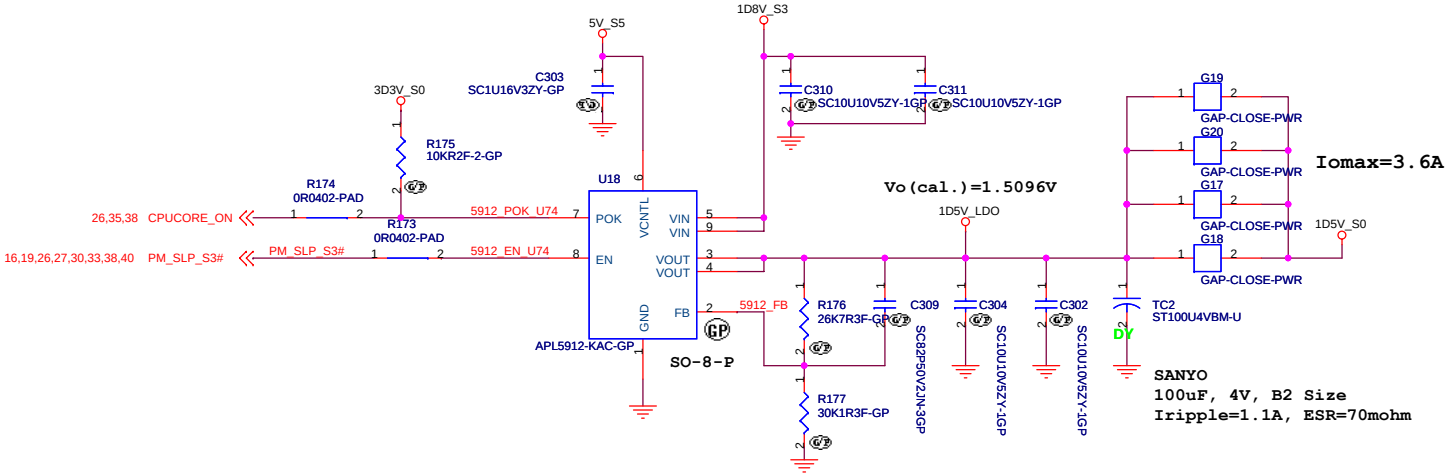
1D5V_S0
Iomax=3.6A



Vo=0.8*(1+(R1/R2))

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5912_1D5V

Size: A3 | Document Number: Huron | Rev: SD

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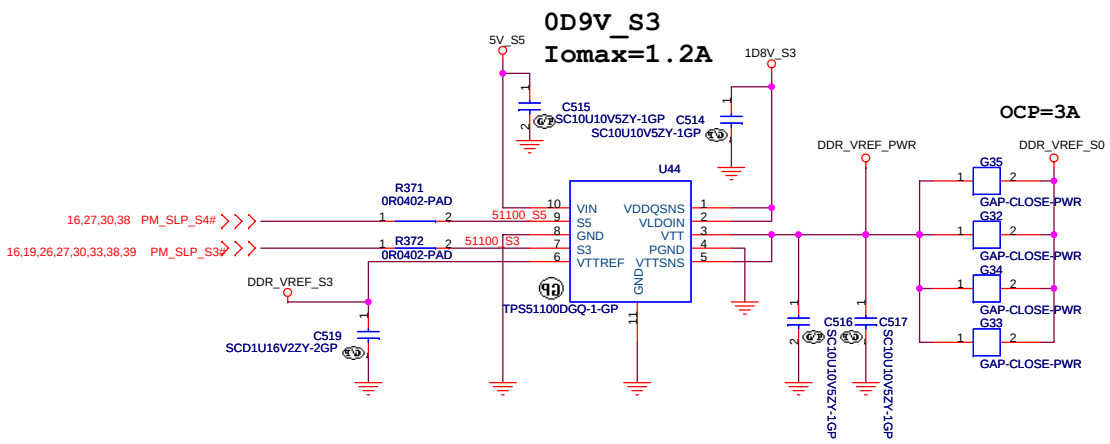

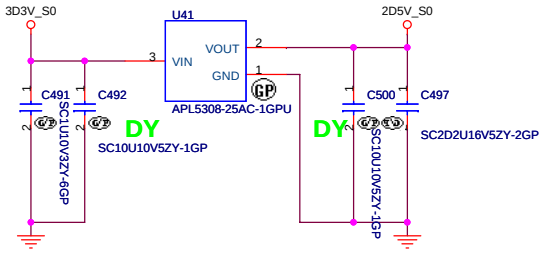

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Title: 0D9V/2D5V

Size: A3 | Document Number: Huron | Rev: SD

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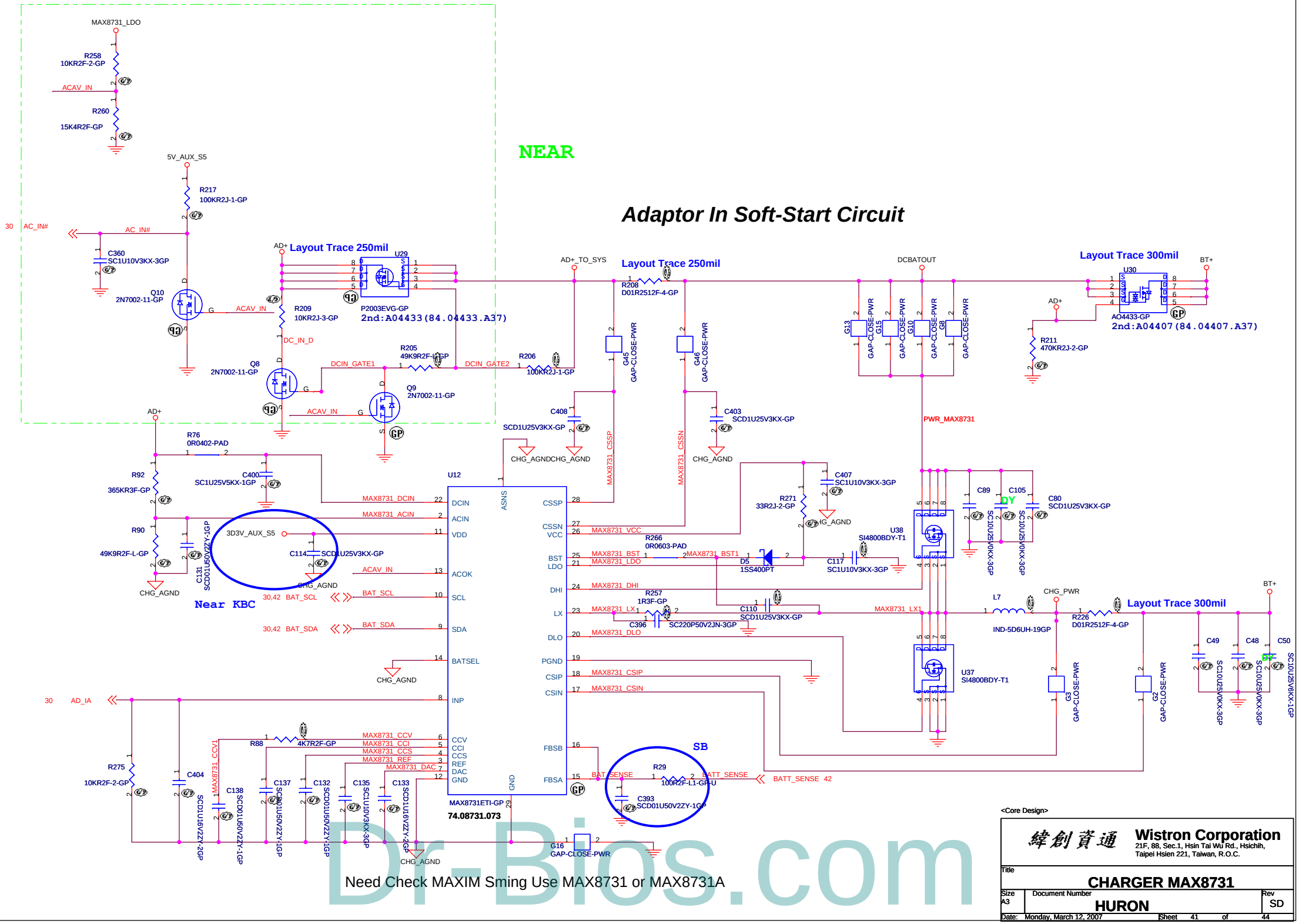
NEAR
Adaptor In Soft-Start Circuit
MAX8731_LDO
R258
10KR2F-2-GP
ACAV_IN
R260
15K4R2F-GP
5V_AUX_S5
R217
100KR2J-1-GP
30 AC_IN#
AC_IN#
C360
SC1U10V3KX-3GP
Q10
2N7002-11-GP
AD+
Layout Trace 250mil
U29
P2003EVG-GP
2nd:A04433(84.04433.A37)
R209
10KR2J-3-GP
DC_IN_D
Q8
2N7002-11-GP
DCIN_GATE1
R205
49K9R2F-GP
DCIN_GATE2
R206
100KR2J-1-GP
Q9
2N7002-11-GP
AD+_TO_SYS
Layout Trace 250mil
R208
D01R2512F-4-GP
DCBATOUT
Layout Trace 300mil
U30
AO4433-GP
2nd:A04407(84.04407.A37)
R211
470KR2J-2-GP
BT+
G45 GAP-CLOSE-PWR
G46 GAP-CLOSE-PWR
G13 GAP-CLOSE-PWR
G15 GAP-CLOSE-PWR
G10 GAP-CLOSE-PWR
G8 GAP-CLOSE-PWR
C408
SCD1U25V3KX-GP
C403
SCD1U25V3KX-GP
CHG_AGNDCHG_AGND
CHG_AGND
MAX8731_CSSP
MAX8731_CSSN
PWR_MAX8731
R76
0R0402-PAD
R92
365KR3F-GP
C400
SC1U25V5KX-1GP
R90
49K9R2F-L-GP
C131
SCD01U50V2ZY-1GP
3D3V_AUX_S5
C114
SCD1U25V3KX-GP
CHG_AGND
Near KBC
U12
MAX8731_DCIN
MAX8731_ACIN
MAX8731_VCC
MAX8731_BST
MAX8731_LDO
MAX8731_DHI
MAX8731_LX
MAX8731_DLO
MAX8731_CSIP
MAX8731_CSIN
ACAV_IN
BAT_SCL
BAT_SDA
DCIN
ACIN
VDD
ACOK
SCL
SDA
BATSEL
INP
CCV
CCI
CCS
REF
DAC
GND
ASNS
CSSP
CSSN
VCC
BST
LDO
DHI
LX
DLO
PGND
CSIP
CSIN
FBSB
FBSA
MAX8731ETI-GP
74.08731.073
R271
33R2J-2-GP
C407
SC1U10V3KX-3GP
IG_AGND
R266
0R0603-PAD
MAX8731_BST1
D5
1SS400PT
U38
SI4800BDY-T1
C117
SC1U10V3KX-3GP
C89
C105
DY
C80
SCD1U25V3KX-GP
SC10U25V0KX-3GP
R257
1R3F-GP
C396
SC220P50V2JN-3GP
C110
SCD1U25V3KX-GP
L7
IND-5D6UH-19GP
CHG_PWR
R226
D01R2512F-4-GP
Layout Trace 300mil
U37
SI4800BDY-T1
G3 GAP-CLOSE-PWR
G2 GAP-CLOSE-PWR
C49
C48
C50
SY
SC10U25V6KX-1GP
30 AD_IA
R275
10KR2-2-GP
C404
SCD1U16V2ZY-2GP
C138
SCD01U50V2ZY-1GP
R88
4K7R2F-GP
MAX8731_CCV1
C137
SCD01U50V2ZY-1GP
C132
SCD01U50V2ZY-1GP
C135
SC1U10V3KX-3GP
C133
SCD1U16V2ZY-2GP
SB
R29
100R2F-L1-GP-U
C393
SCD01U50V2ZY-1GP
BAT_SENSE
BATT_SENSE
BATT_SENSE 42
G16 GAP-CLOSE-PWR
Need Check MAXIM Sming Use MAX8731 or MAX8731A
Dr-Bios.com
<Core Design>
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
CHARGER MAX8731
Size A3
Document Number
HURON
Rev SD
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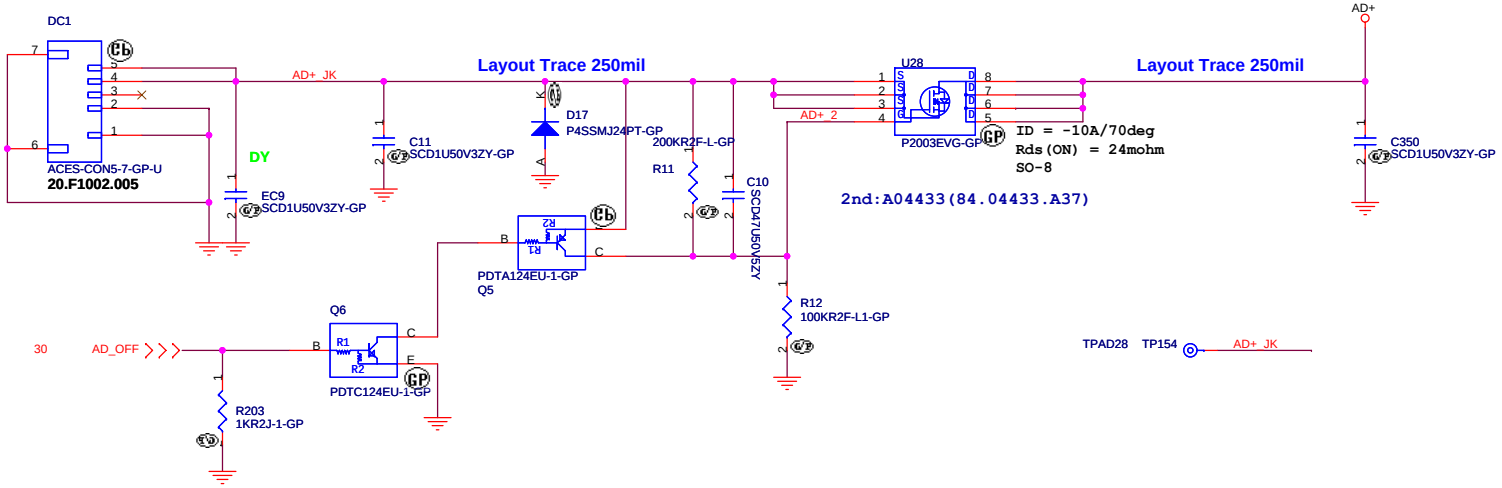
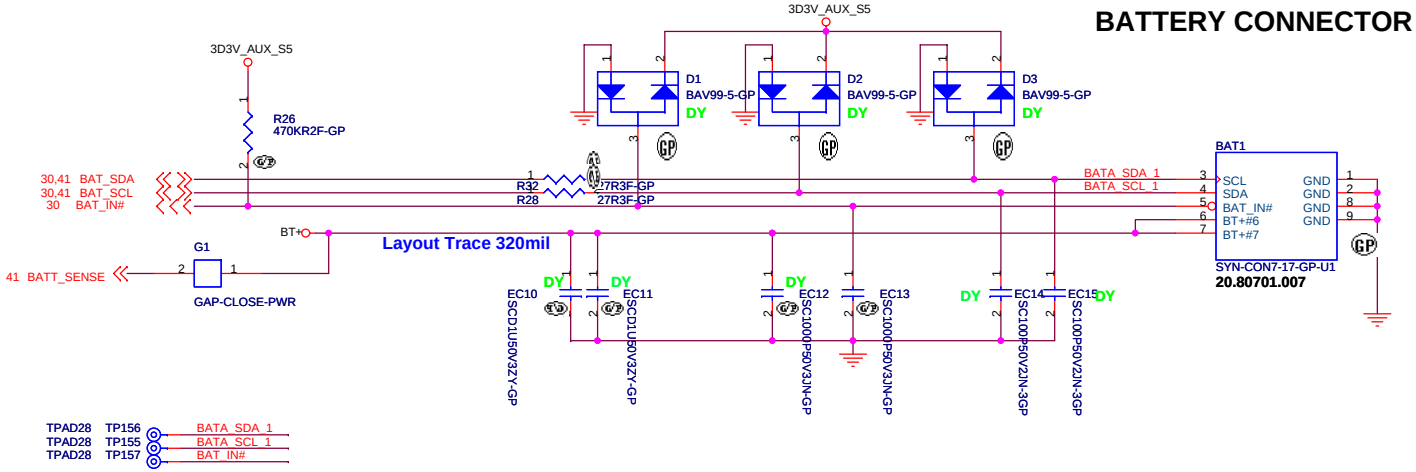
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title: AD/BATT CONN

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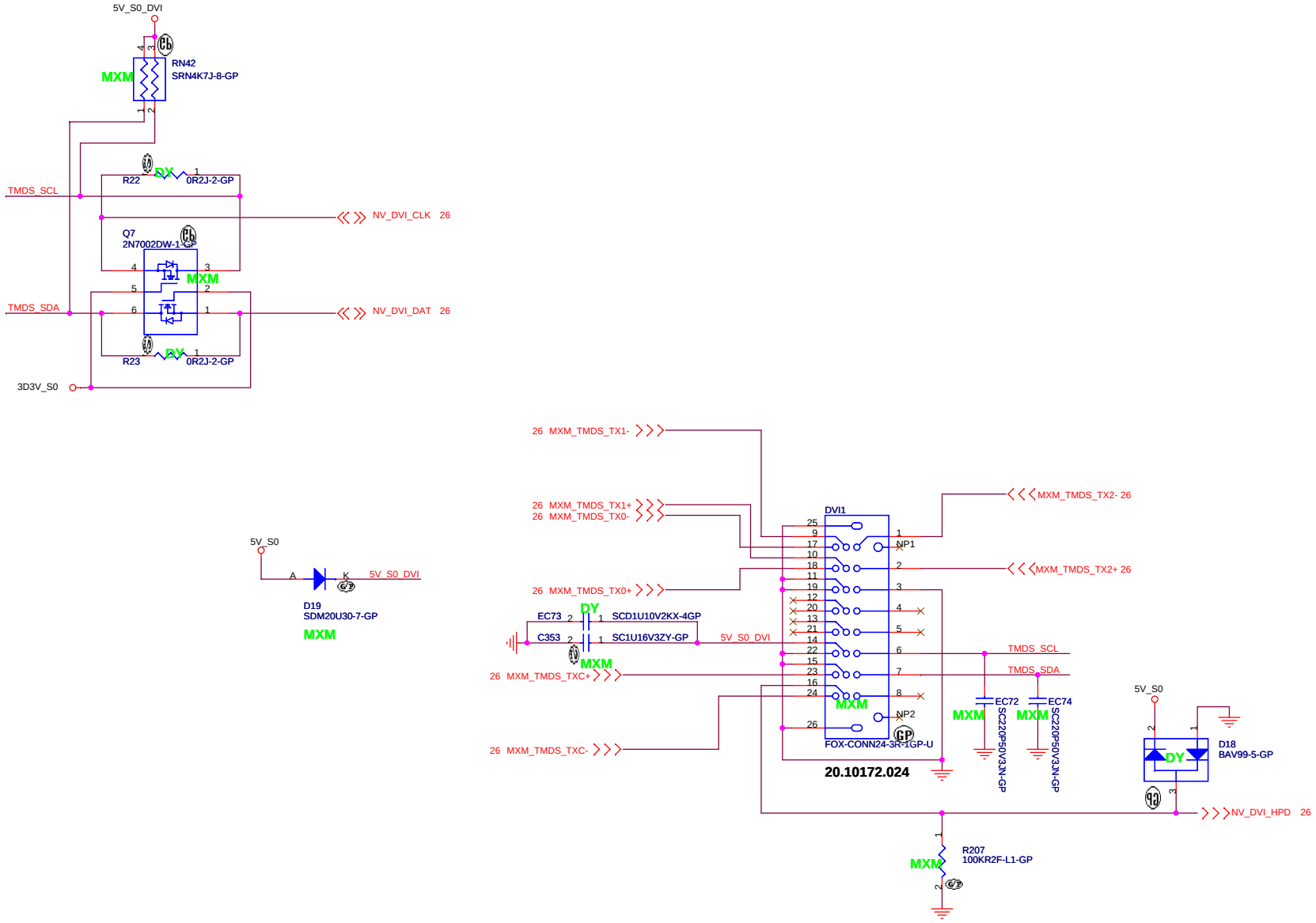
</core_design>



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Title: DVI CONNECTOR

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A3	HURON	SD

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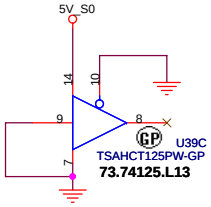
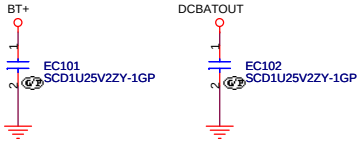
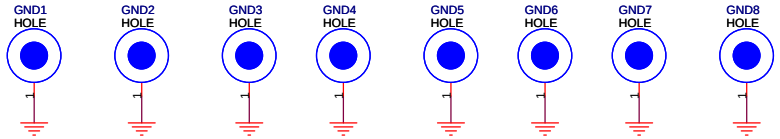
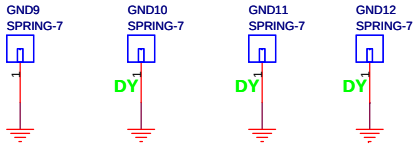


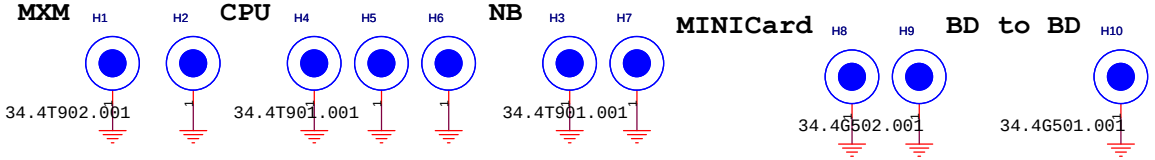


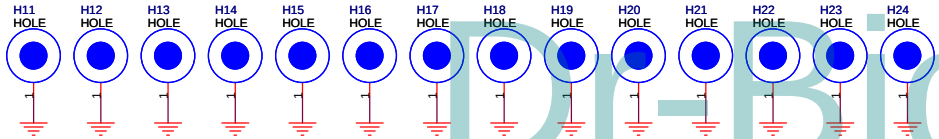


Spring



MXM **CPU** **NB** **MINICard** **BD to BD**





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Title: **EMI/Spring/Boss**

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