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PEW71_81_91 UMA <LA-6582P> M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

2010-07-08

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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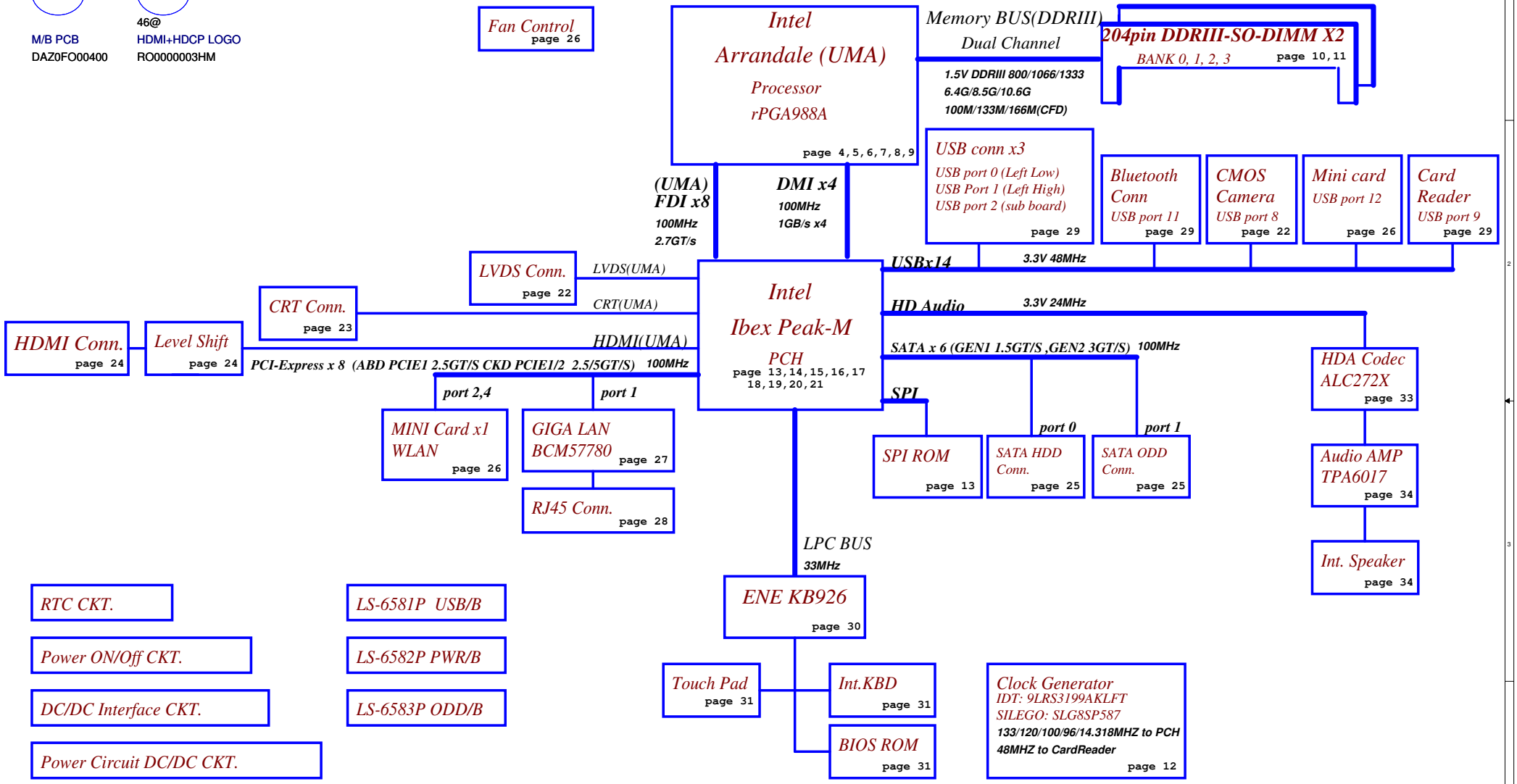
Compal Confidential

Model Name PEW71_81_91 UMA
File Name : LA-6582P

ZZZ1
M/B PCB
DAZ0FO00400

ZZZ2
46@
HDMI+HDCP LOGO
RO0000003HM



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Title	Block Diagrams		
Size B	Document Number PEW71 M/B LA-6582P Schematic		Rev 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.05VS_VTT	1.05V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Project ID / Board ID Table for EC-AD channel

Vcc	3.3V +/- 5%
Ra/Rc	100K +/- 5%

	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Board ID	Project ID
0	0	0 V	0 V	0 V	0.1	Original NEW70/80/90/50/71/91
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2	PEW71/81/91 Audio Mono/Crystal
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	0.3	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	1.0	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V		
5	100K +/- 5%	1.453 V	1.650 V	1.759 V		
6	200K +/- 5%	1.935 V	2.200 V	2.341 V		PEW71/81/91 Audio Mono/SUSCLK
7	NC	2.500 V	3.300 V	3.300 V		NEW71/91 Optumis

BTO Option Table

BTO Item	BOM Structure
HDMI	HDMI@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 Left Low USB	Ext1 Left Low USB
		1	Ext2 Left High USB	Ext2 Left High USB
	UHCI1	2	Ext3 Right USB	Ext3 Right USB
		3		
	UHCI2	4		
		5		
	UHCI3	6		
		7		
EHCI2	UHCI4	8	Camera	Camera
		9	Card Reader	Card Reader
	UHCI5	10		
		11	Blue Tooth	Blue Tooth
	UHCI6	12	1st Min-Card	1st Min-Card
		13		

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Title: Notes List

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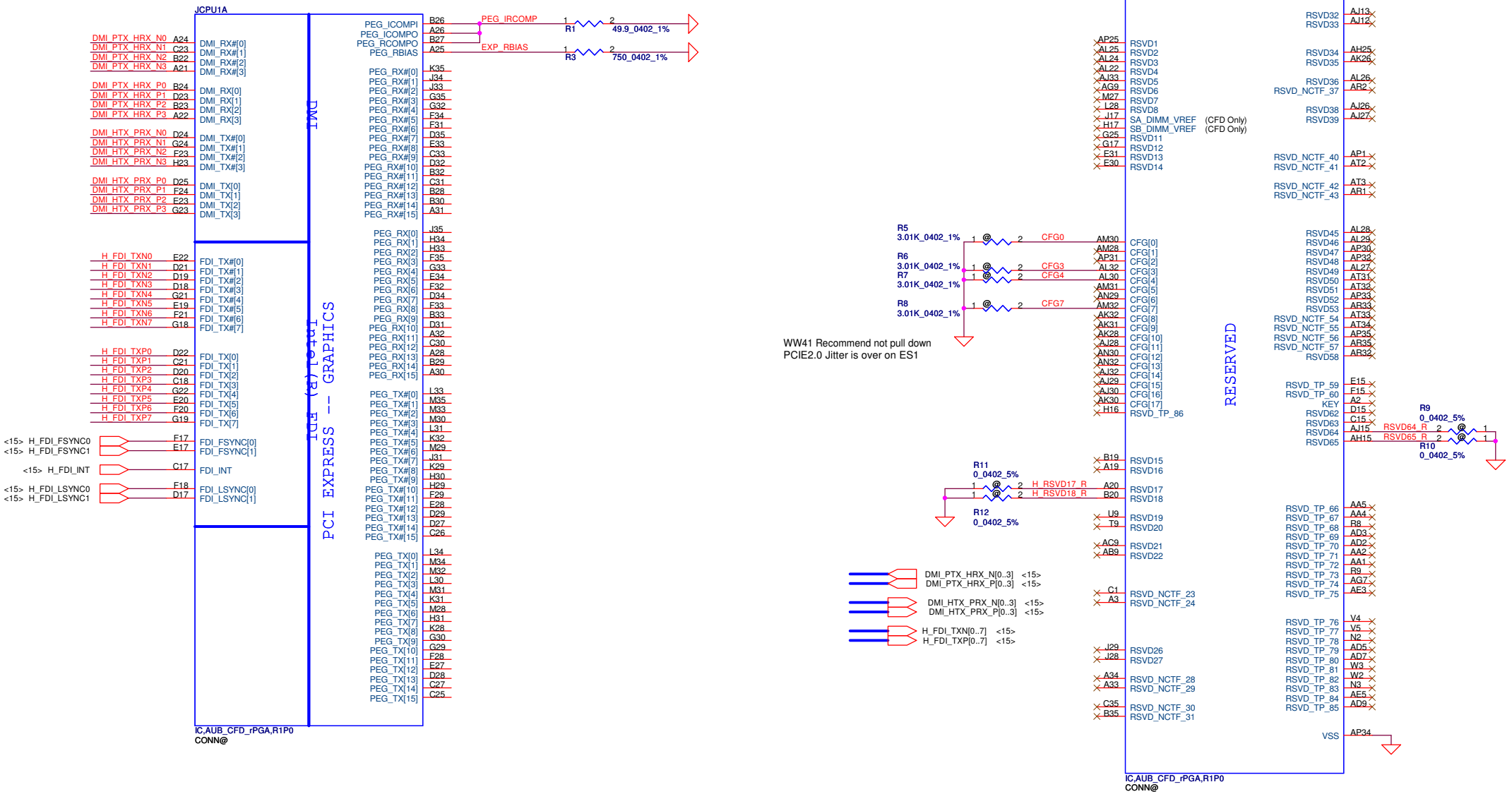

eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Title: PROCESSOR (1/6) DMI,FDI,PEG

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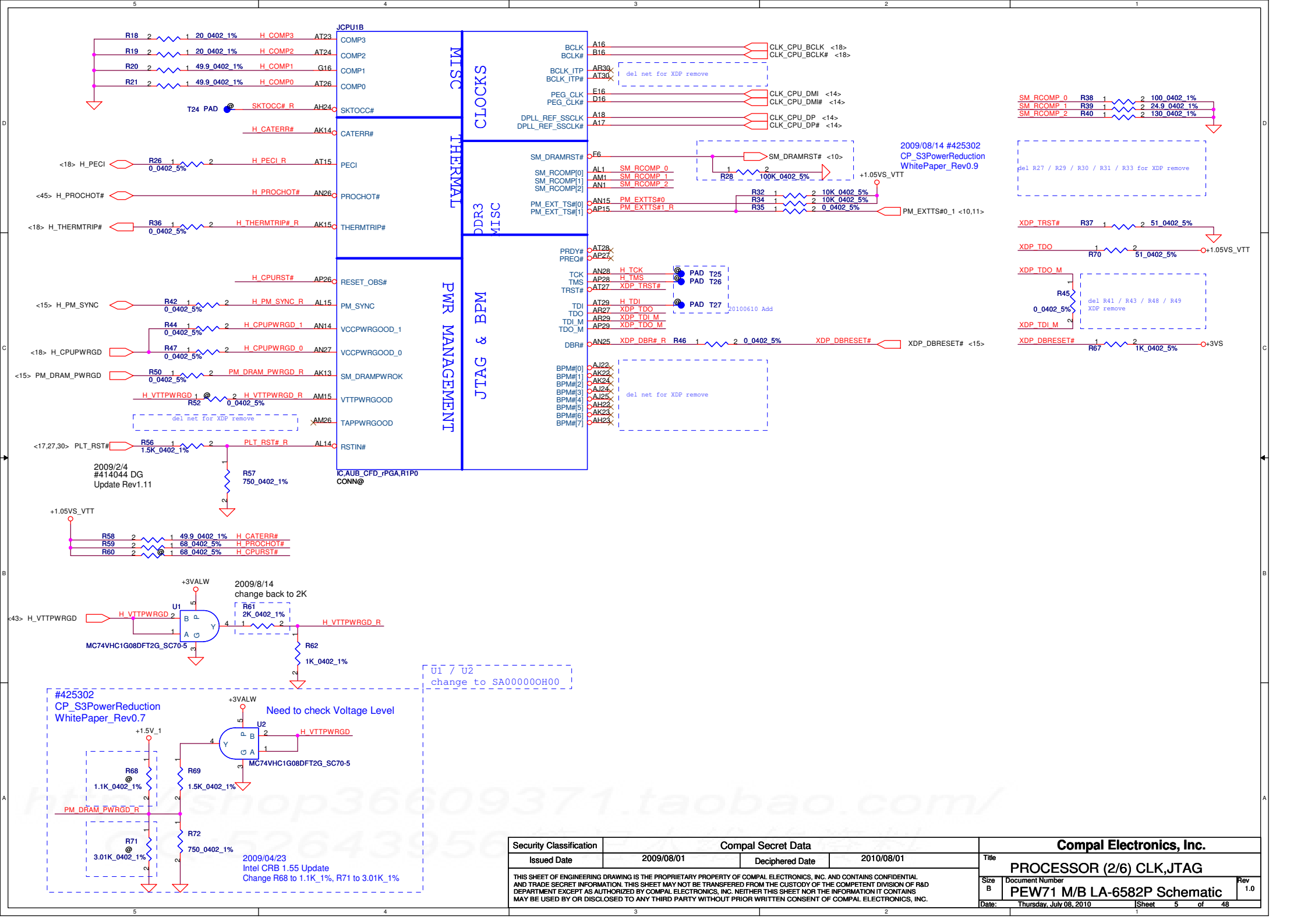

Compal Electronics, Inc.	
Title	PROCESSOR (2/6) CLK,JTAG
Size B	Document Number PEW71 M/B LA-6582P Schematic
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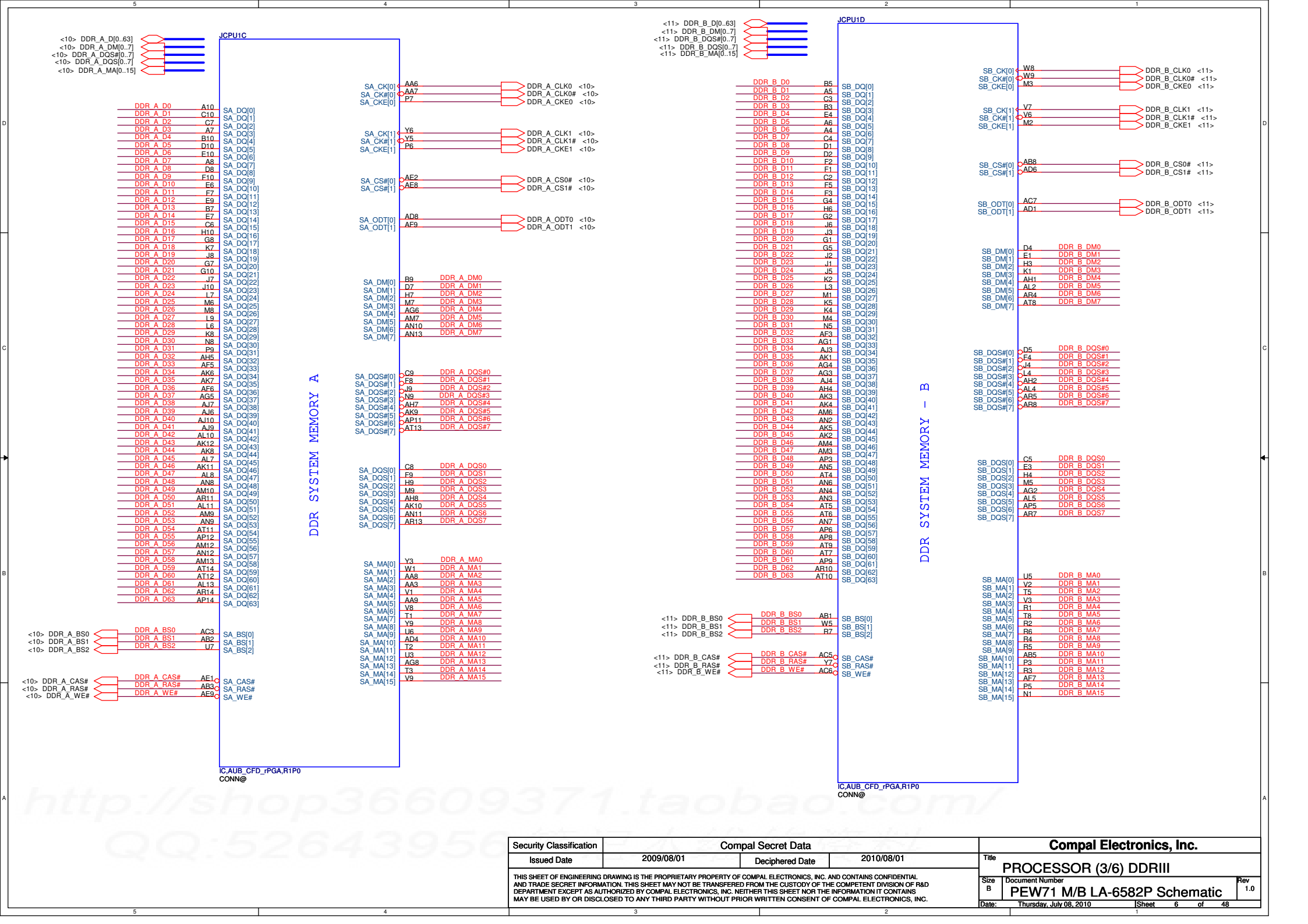

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Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	PEW71 M/B LA-6582P Schematic	1.0

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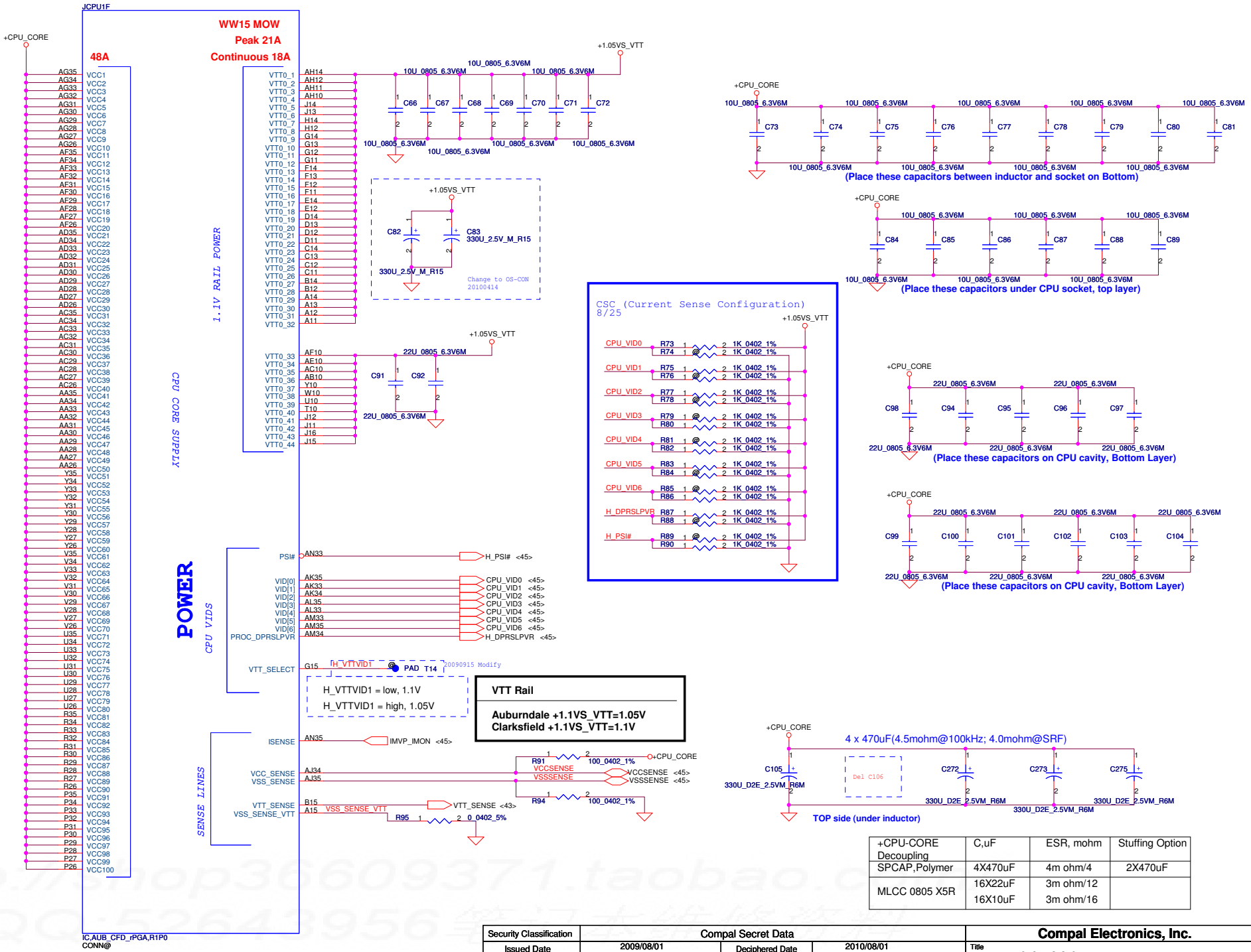

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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Title: PROCESSOR (4/6) PWR,Bypass

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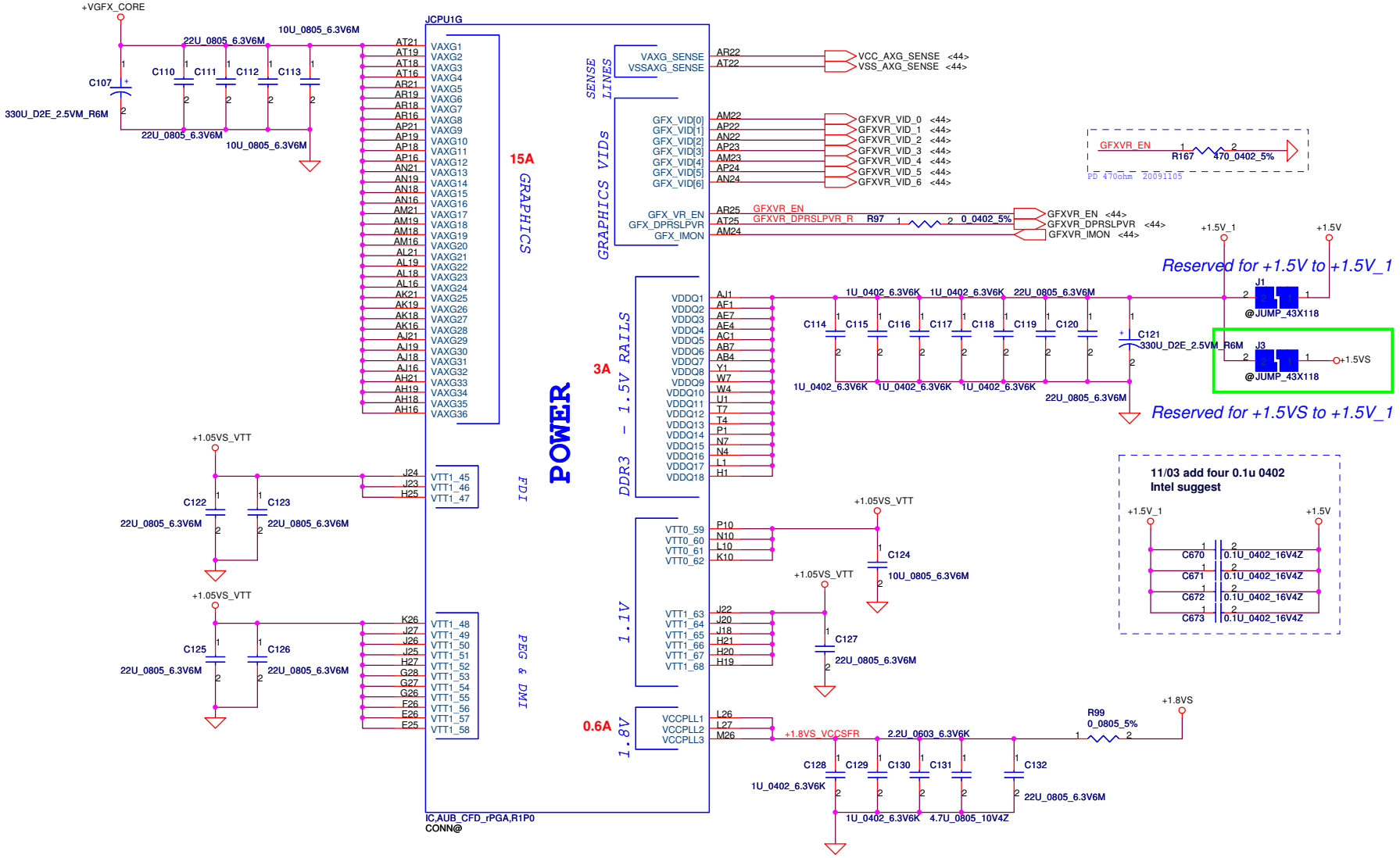

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Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

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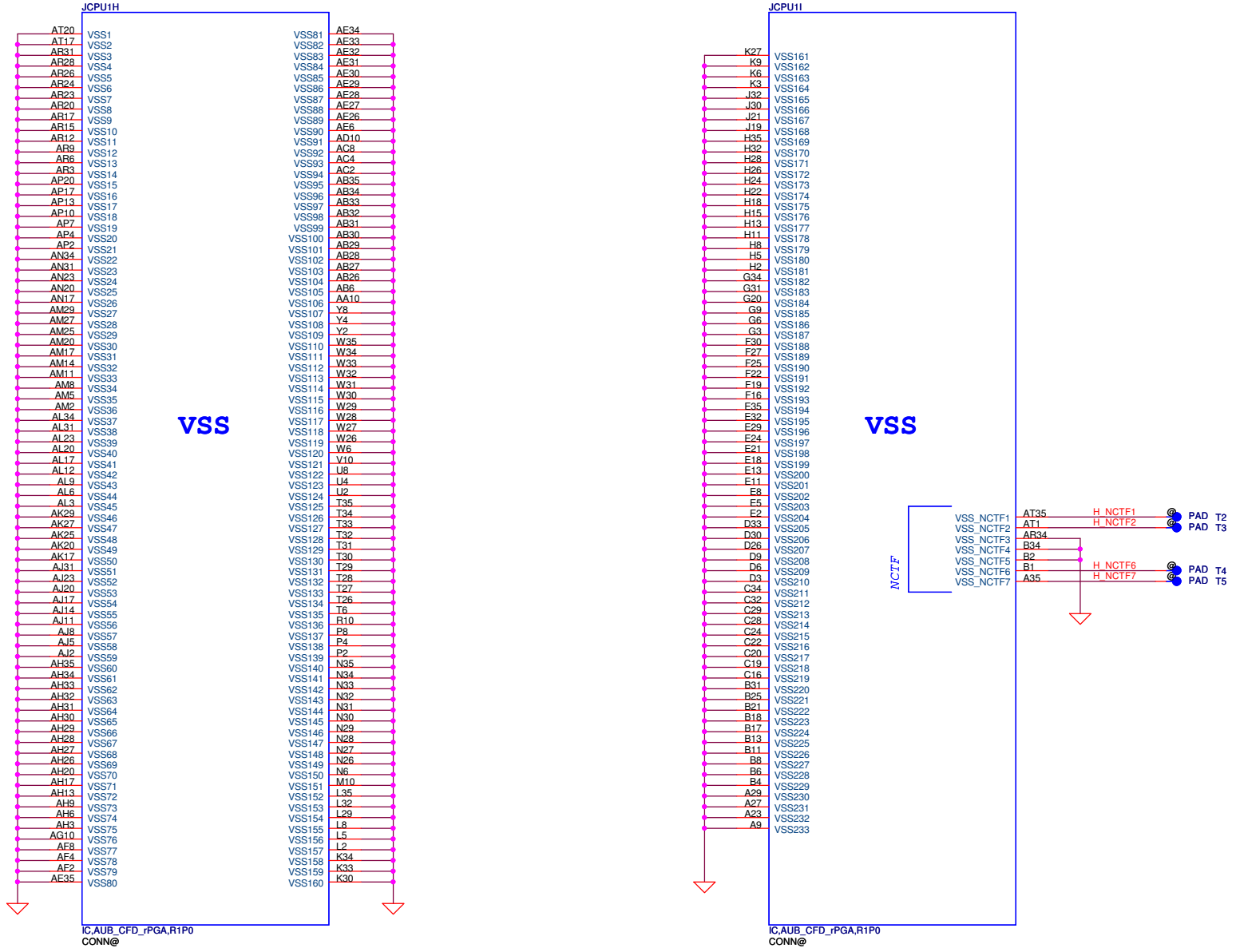

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Title: PROCESSOR (6/6) VSS

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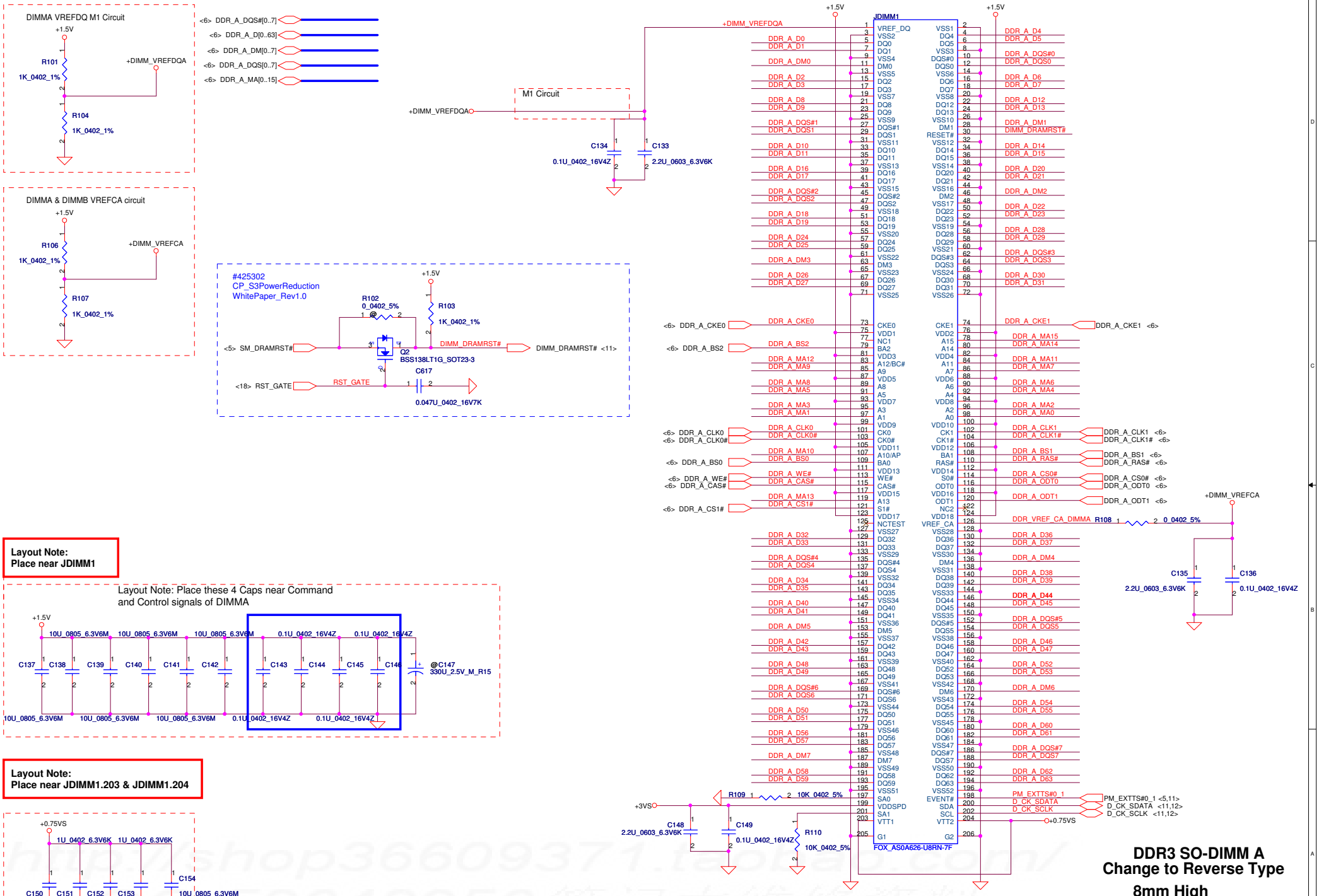

DDR3 SO-DIMM A
Change to Reverse Type
8mm High

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Title: *DDRIII-SODIMM SLOT1*

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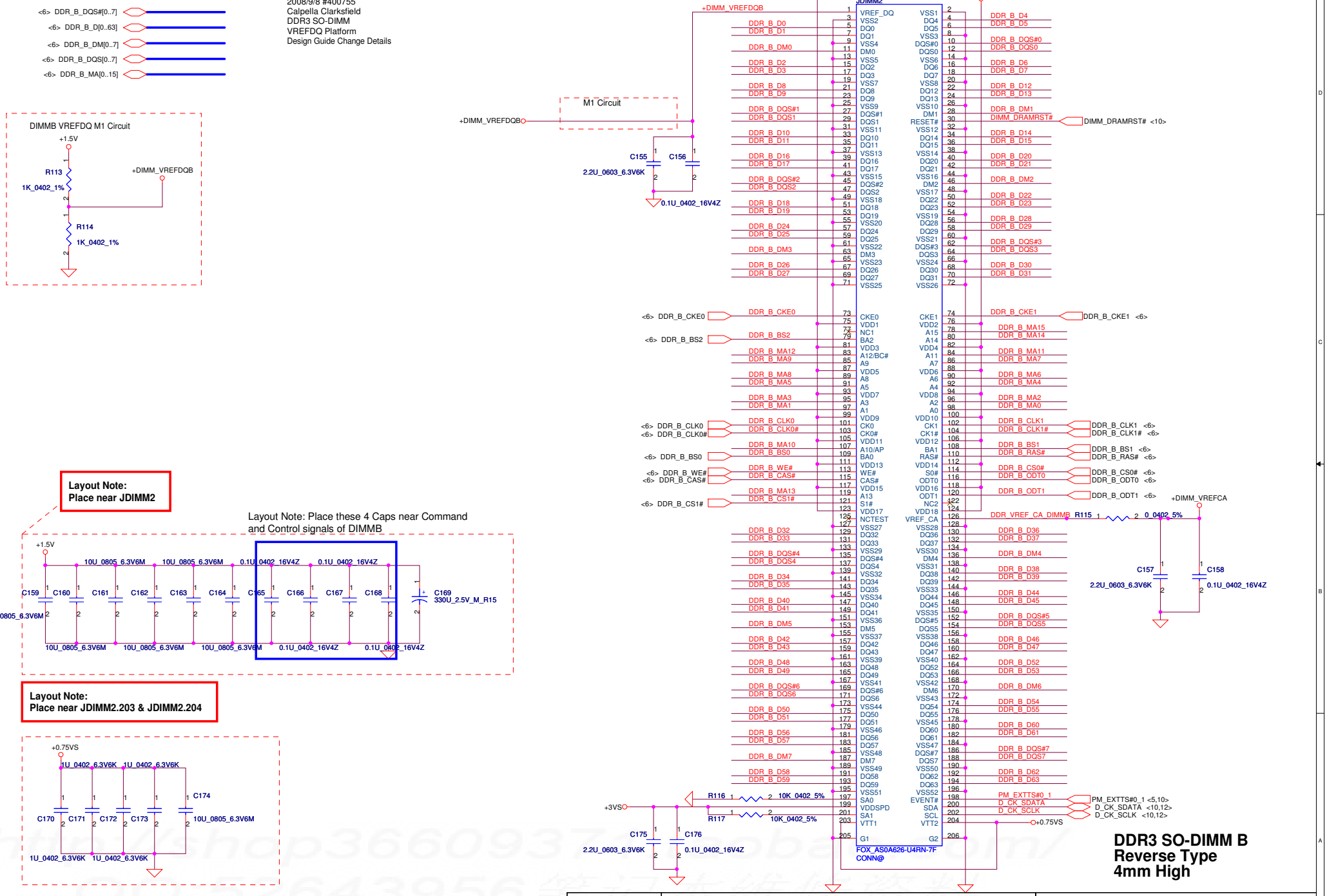
2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details
<6> DDR_B_DQS#[0..7]
<6> DDR_B_D[0..63]
<6> DDR_B_DM[0..7]
<6> DDR_B_DQS[0..7]
<6> DDR_B_MA[0..15]
DIMMB VREFDQ M1 Circuit
+1.5V
R113
1K_0402_1%
+DIMM_VREFDQB
R114
1K_0402_1%
Layout Note:
Place near JDIMM2
Layout Note: Place these 4 Caps near Command
and Control signals of DIMMB
+1.5V
10U_0805_6.3V6M
0.1U_0402_16V4Z
C159
C160
C161
C162
C163
C164
C165
C166
C167
C168
C169
330U_2.5V_M_R15
Layout Note:
Place near JDIMM2.203 & JDIMM2.204
+0.75VS
1U_0402_6.3V6K
C170
C171
C172
C173
C174
JDIMM2
M1 Circuit
C155
C156
2.2U_0603_6.3V6K
0.1U_0402_16V4Z
DDR_B_CKE0
DDR_B_BS2
DDR_B_CLK0
DDR_B_CLK0#
DDR_B_BS0
DDR_B_WE#
DDR_B_CAS#
DDR_B_CS1#
DDR_B_CKE1
DDR_B_CLK1
DDR_B_CLK1#
DDR_B_BS1
DDR_B_RAS#
DDR_B_CS0#
DDR_B_ODT0
DDR_B_ODT1
DIMM_DRAMRST#
DDR_B_CKE1 <6>
DDR_B_CLK1 <6>
DDR_B_CLK1# <6>
DDR_B_BS1 <6>
DDR_B_RAS# <6>
DDR_B_CS0# <6>
DDR_B_ODT0 <6>
DDR_B_ODT1 <6>
+DIMM_VREFCA
DDR_VREF_CA_DIMMB
R115
0_0402_5%
C157
C158
R116
R117
10K_0402_5%
C175
C176
+3VS
+0.75VS
PM_EXTTS#0_1 <5,10>
D_CK_SDATA <10,12>
D_CK_SCLK <10,12>
FOX_AS0A626-U4RN-7F
CONN@
DDR3 SO-DIMM B
Reverse Type
4mm High
Security Classification
Compal Secret Data
Issued Date
2009/08/01
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2010/08/01
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DDRIII-SODIMM SLOT2
Size
Document Number
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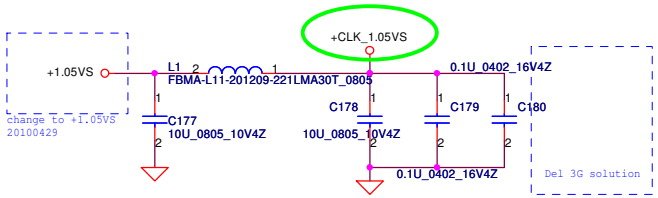
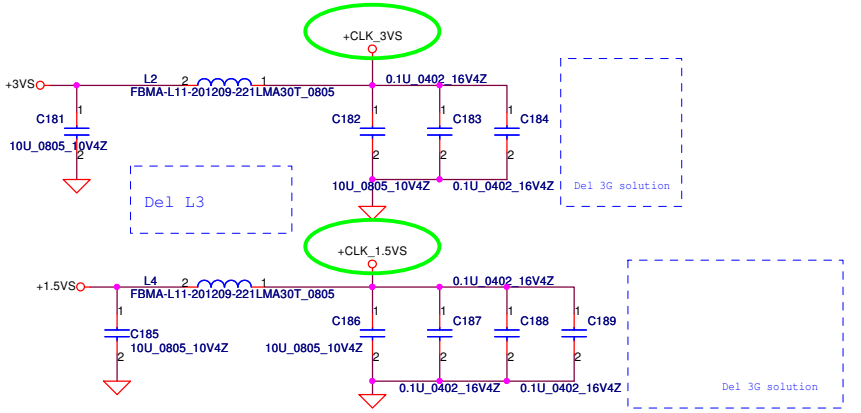
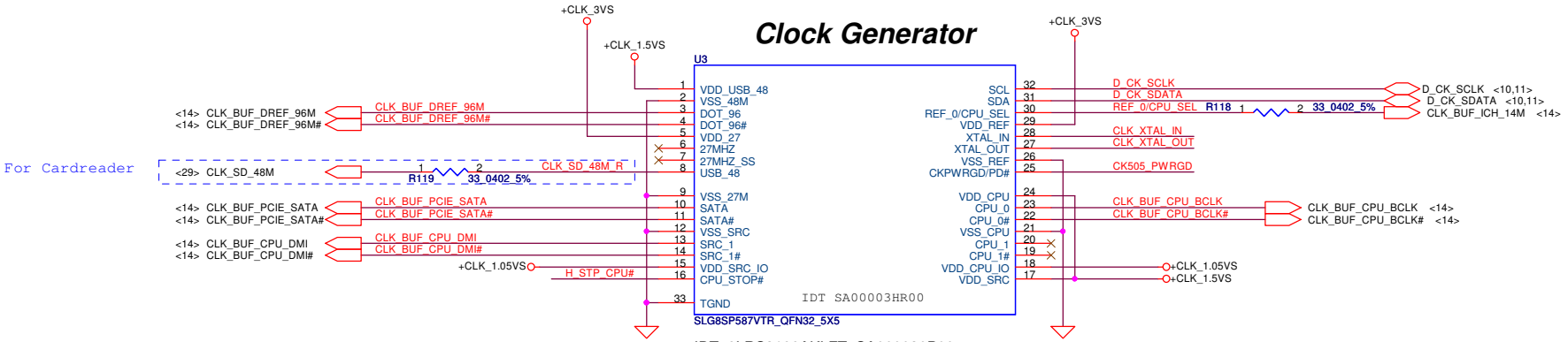
Clock Generator







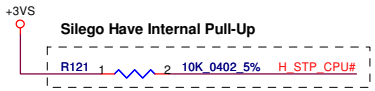
IDT: 9LRS3199AKLFT, SA000030P00

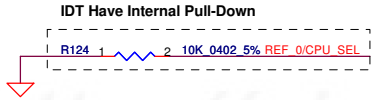
SILEGO: SLG8SP587V(WF), SA00002XY10

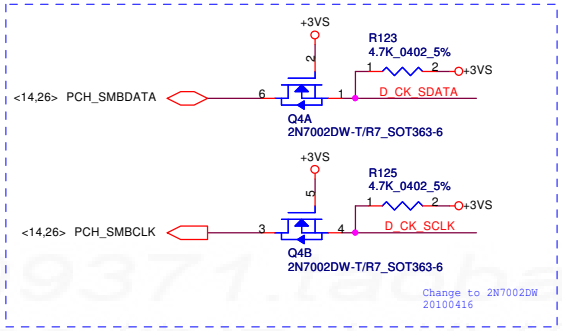
Low Power:

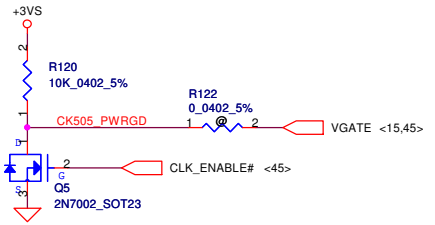
IDT: 9LVS3199AKLFT, SA00003HR00

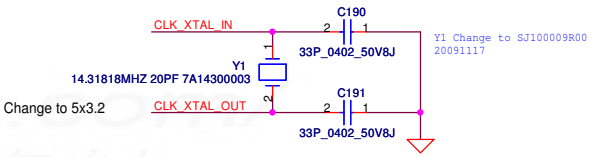
Realtek: RTM890N-631-GRT, SA00003HQ00











PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

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Title: Clock Generator (CK505)

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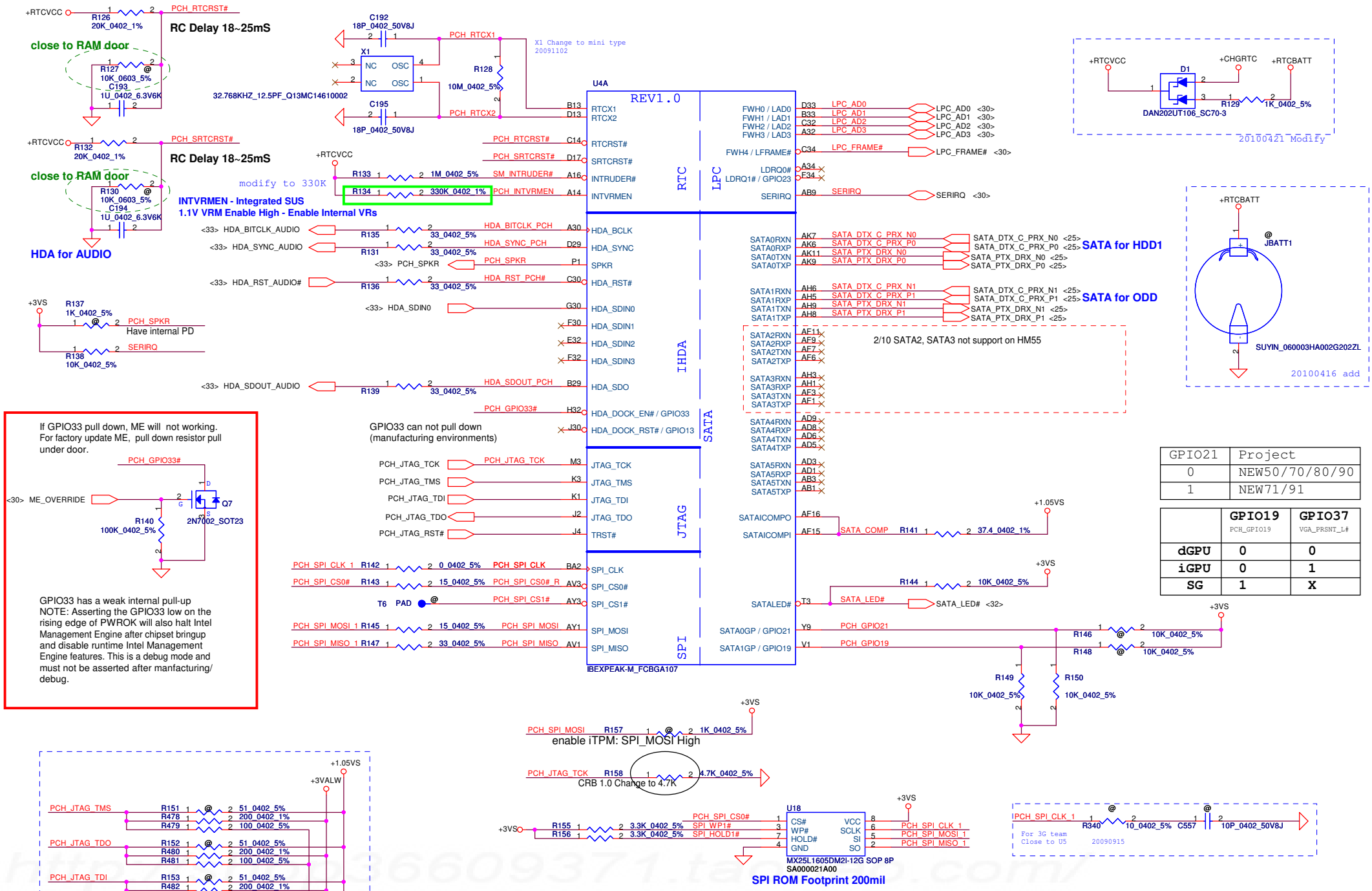

GPIO21	Project
0	NEW50/70/80/90
1	NEW71/91

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	X

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Title: PCH (1/9) SATA,HDA,SPI, LPC

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1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

U4B

REV1.0

IBEXPEAK-M_FCBGA107

For PCIE LAN

For Wireless LAN

2/10 PCIE7, PCIE8 not support on HM55

For PCIE LAN

For Wireless LAN

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

Change to 5x3.2

Project Port ID

0602 GPIO65 no use
PULL HIGH:PVT
PULL DOWN:DVT

GPIO66 6L/8L SATA register separe		
GPIO66	0	6L *
	1	8L

2009/09/23:Change to +3VALW
2009/08/13: Change back to +3VALW

Pull high +3VS at KB926 side

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Title: PCH (2/9) PCIE, SMBUS, CLK

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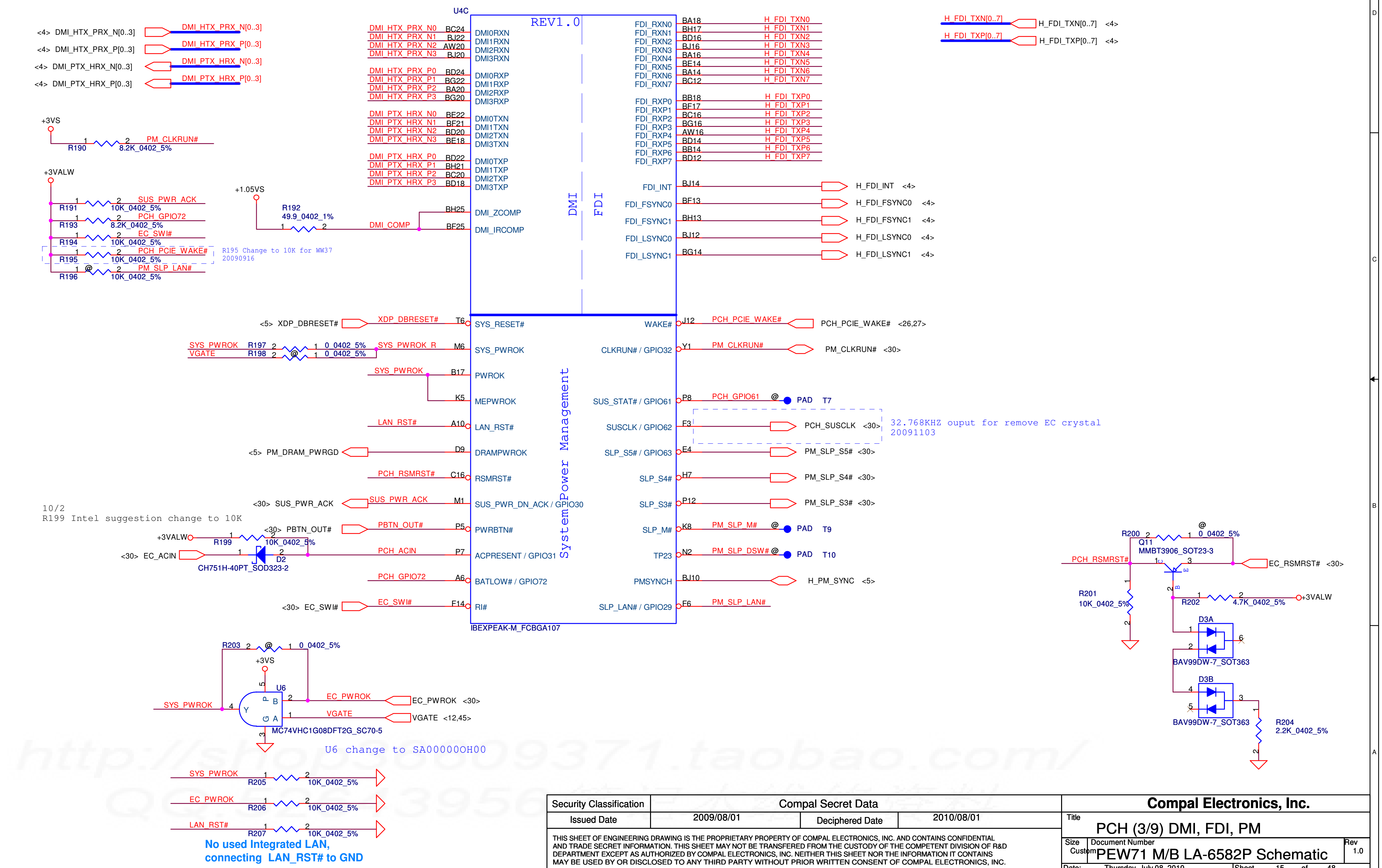

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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title: PCH (3/9) DMI, FDI, PM
				Size: Custom; Document Number: PEW71 M/B LA-6582P Schematic; Rev: 1.0
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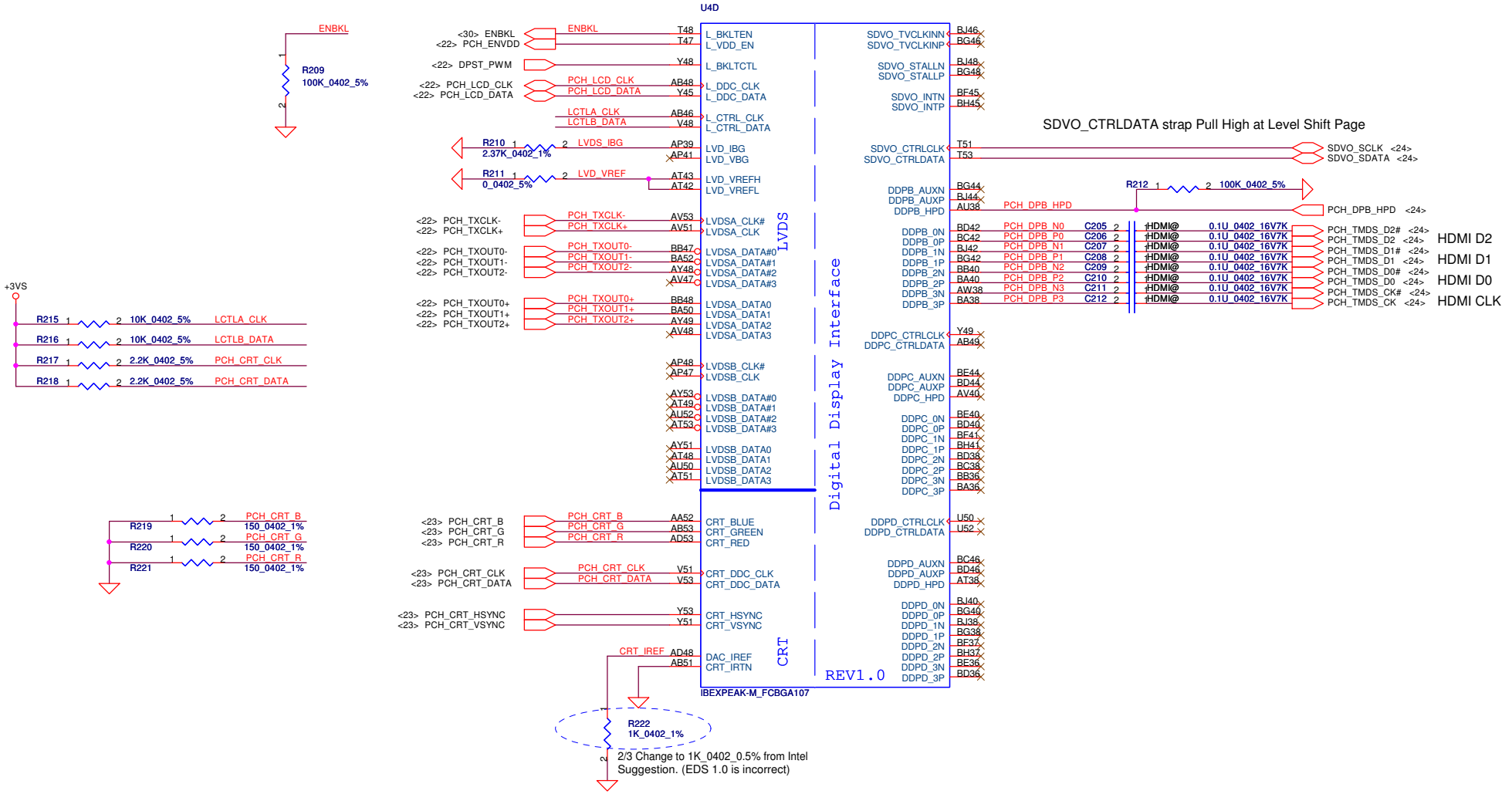

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Issued Date	2009/08/01	Deciphered Date	2010/08/01

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Title: PCH (4/9) LVDS, CRT, DPI

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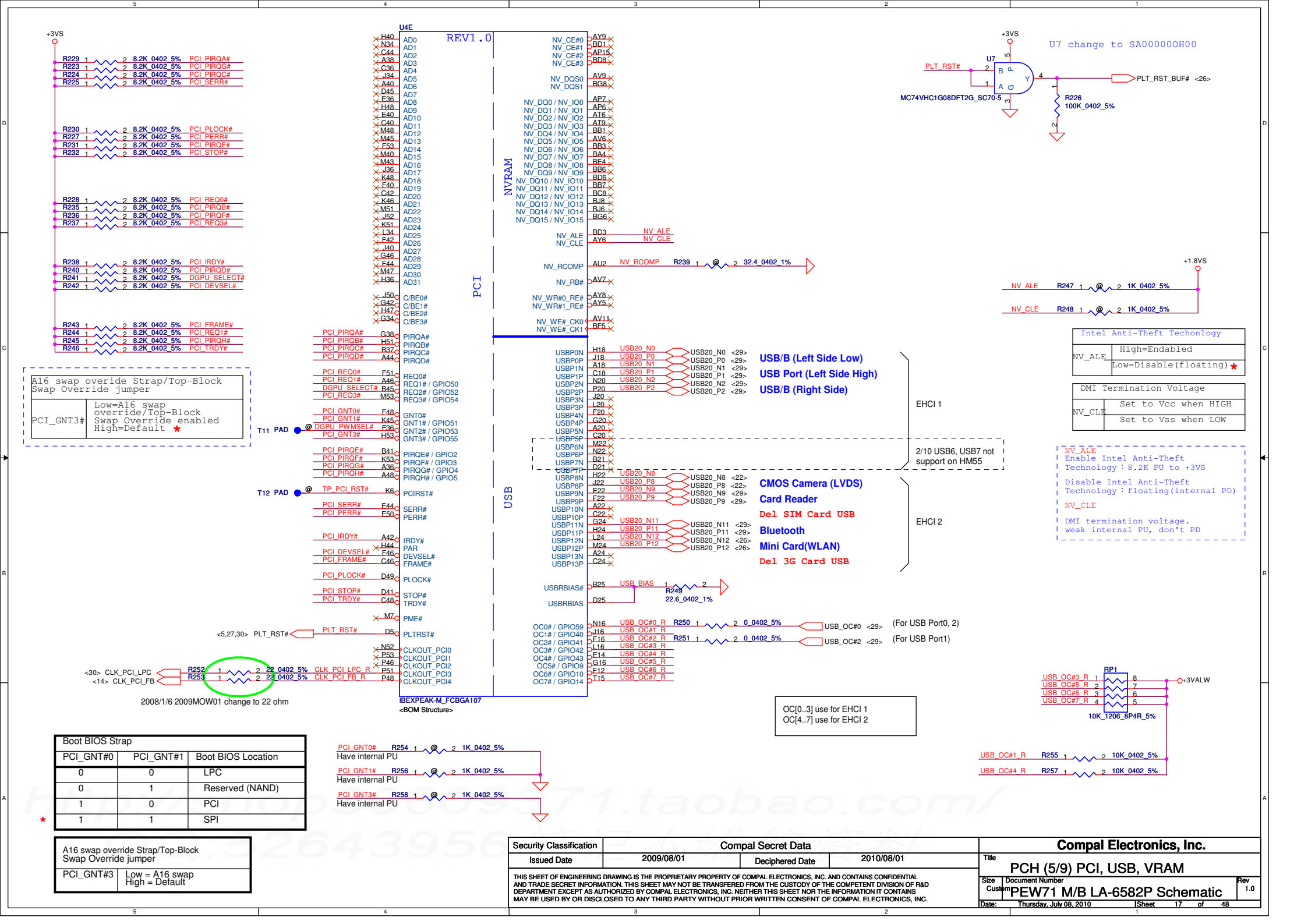

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

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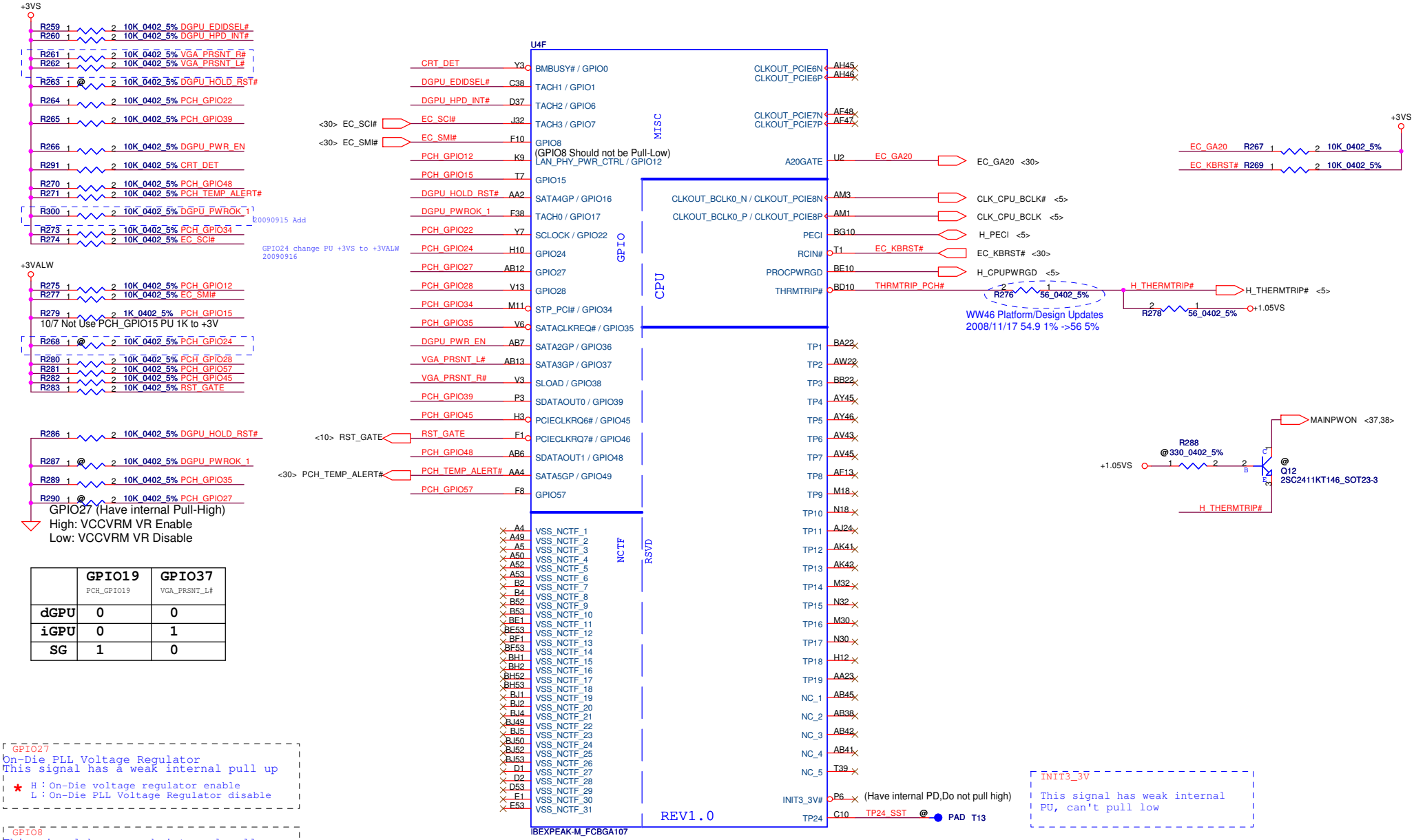

Security Classification	Compal Secret Data			
Issued Date	2009/08/01	Deciphered Date	2010/08/01	

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

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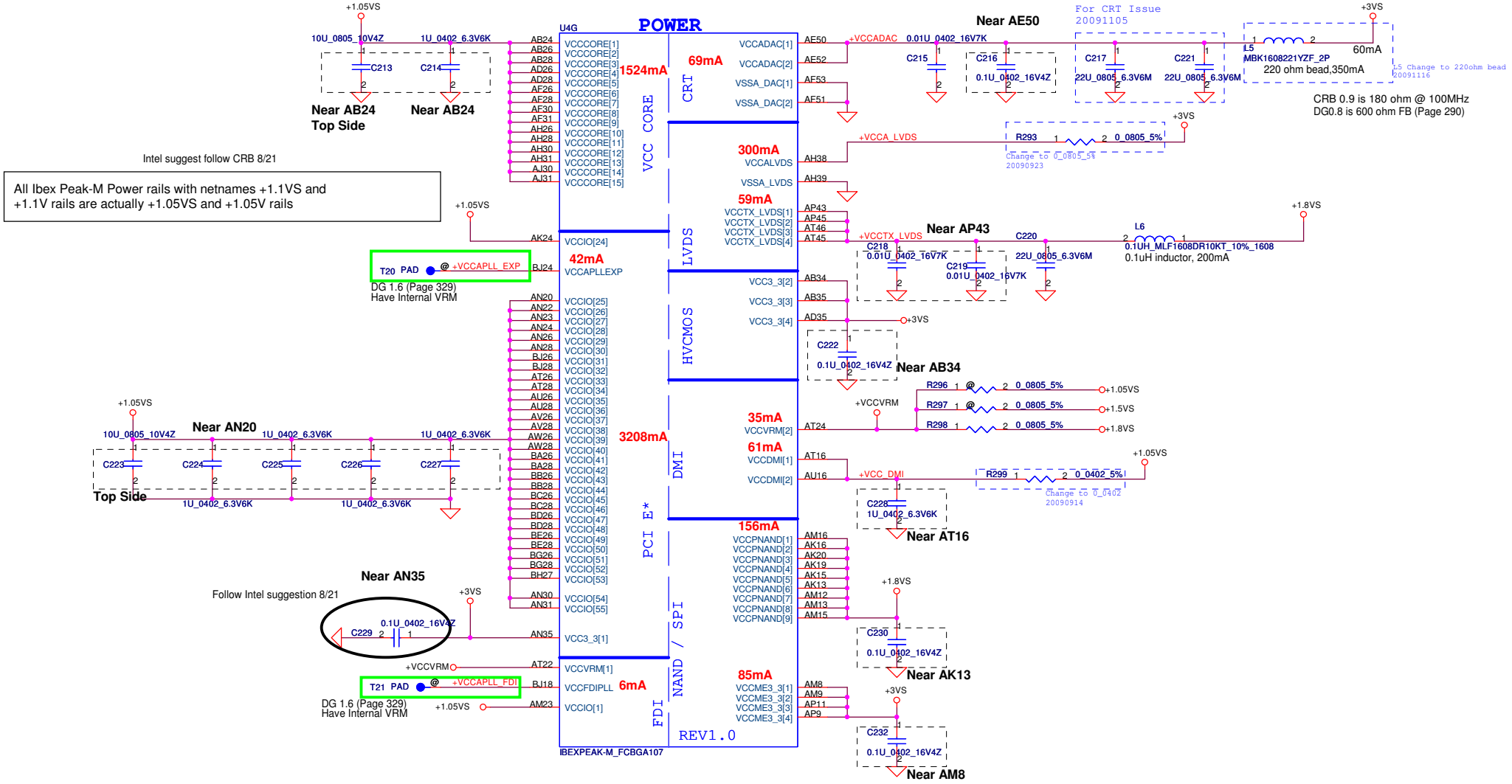

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: PEW71 M/B LA-6582P Schematic | Rev: 1.0

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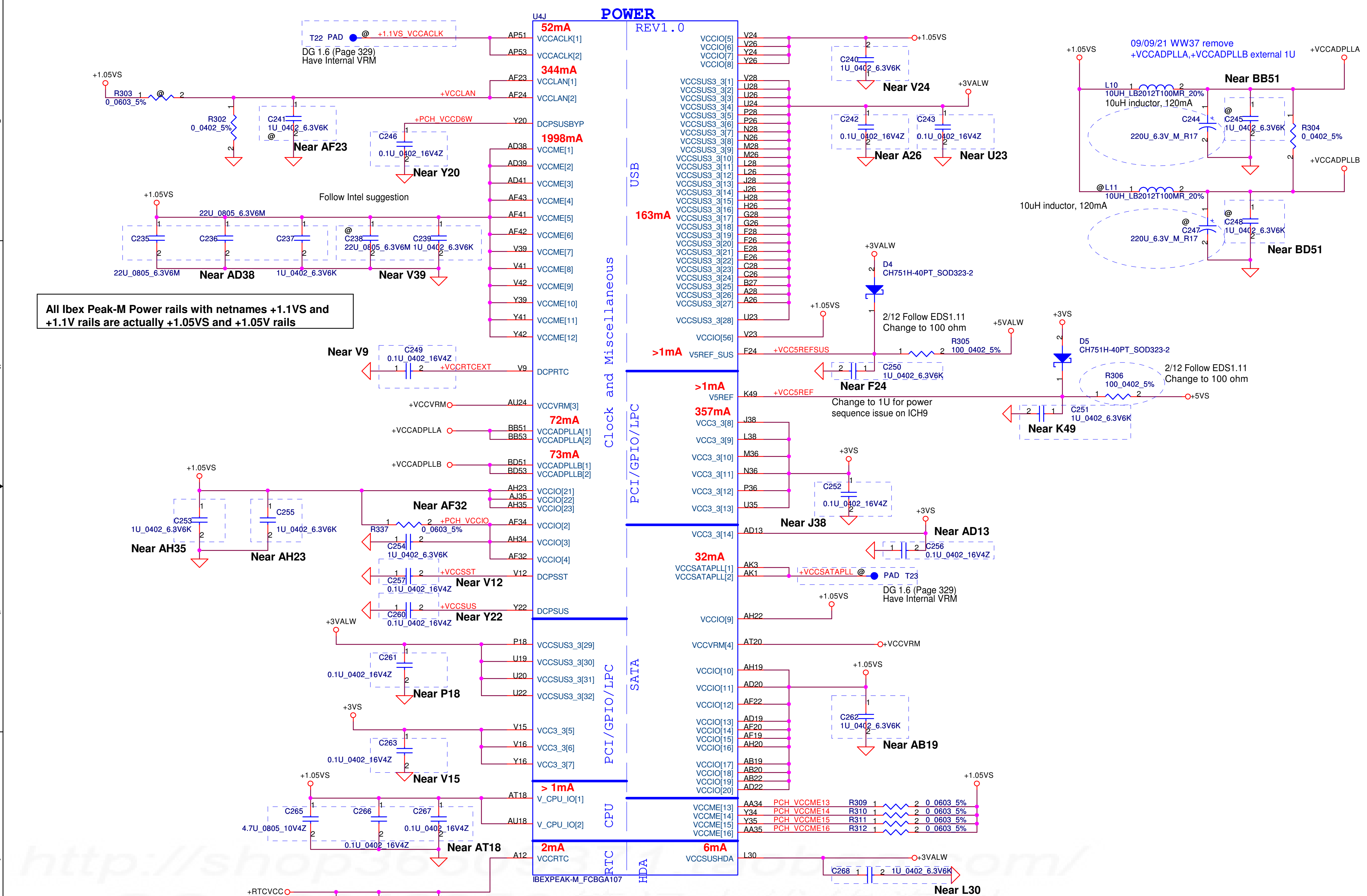

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/08/01	Deciphered Date 2010/08/01	Title: PCH (8/9) PWR
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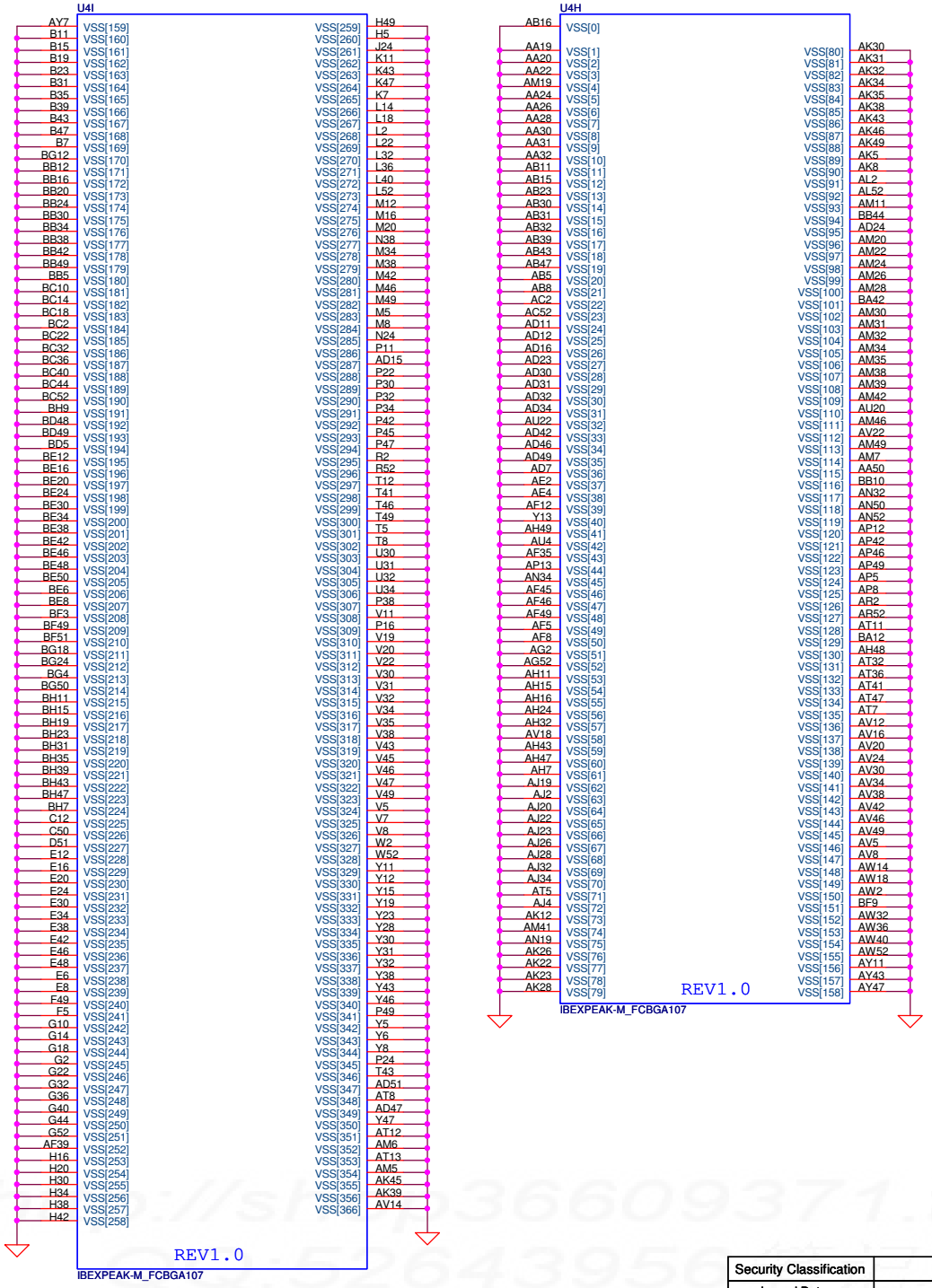
			Date: Thursday, July 08, 2010; Sheet 20 of 48



Del PCH XDP

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size: Custom | Document Number: PEW71 M/B LA-6582P Schematic | Rev: 1.0

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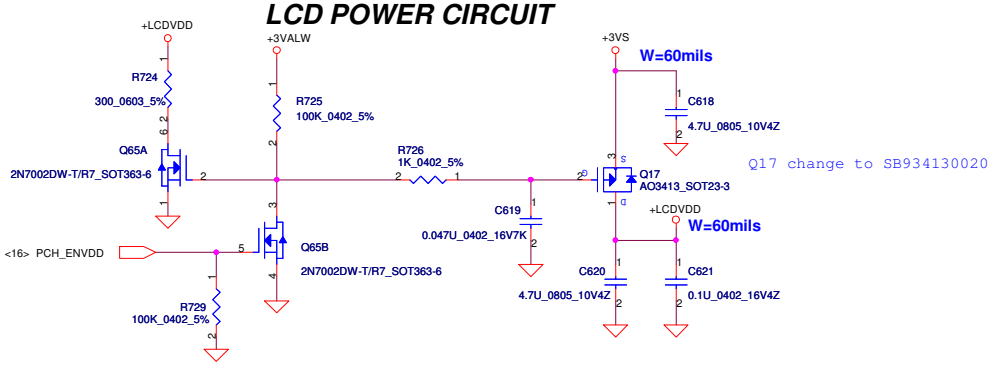
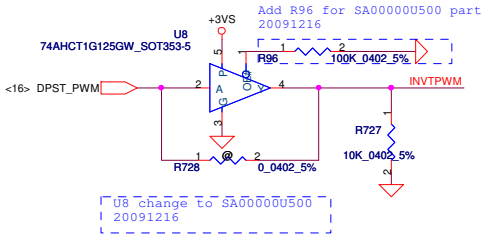
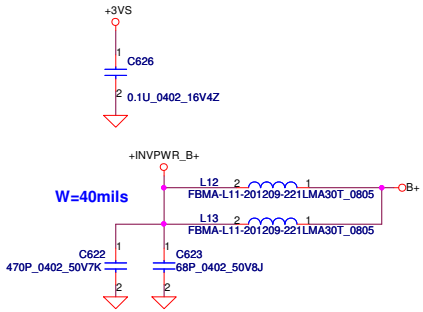
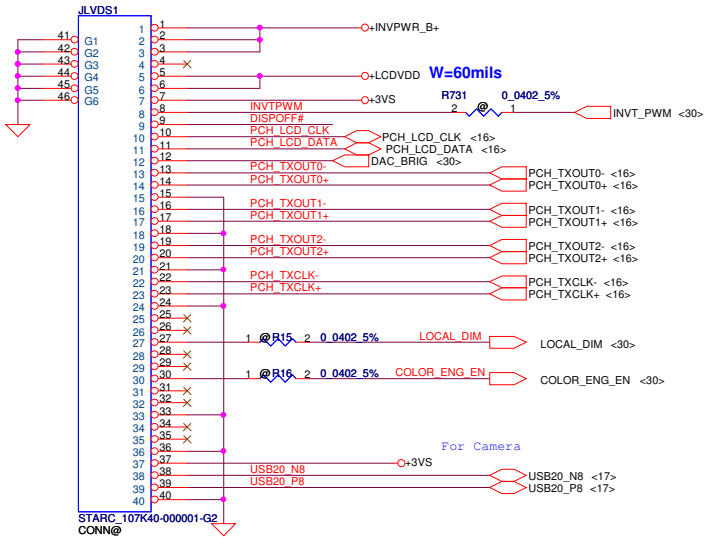
LCD POWER CIRCUIT

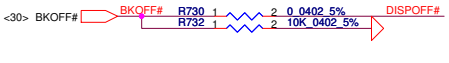


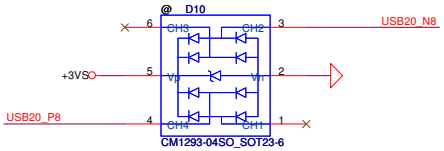


LED PANEL Conn.









Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

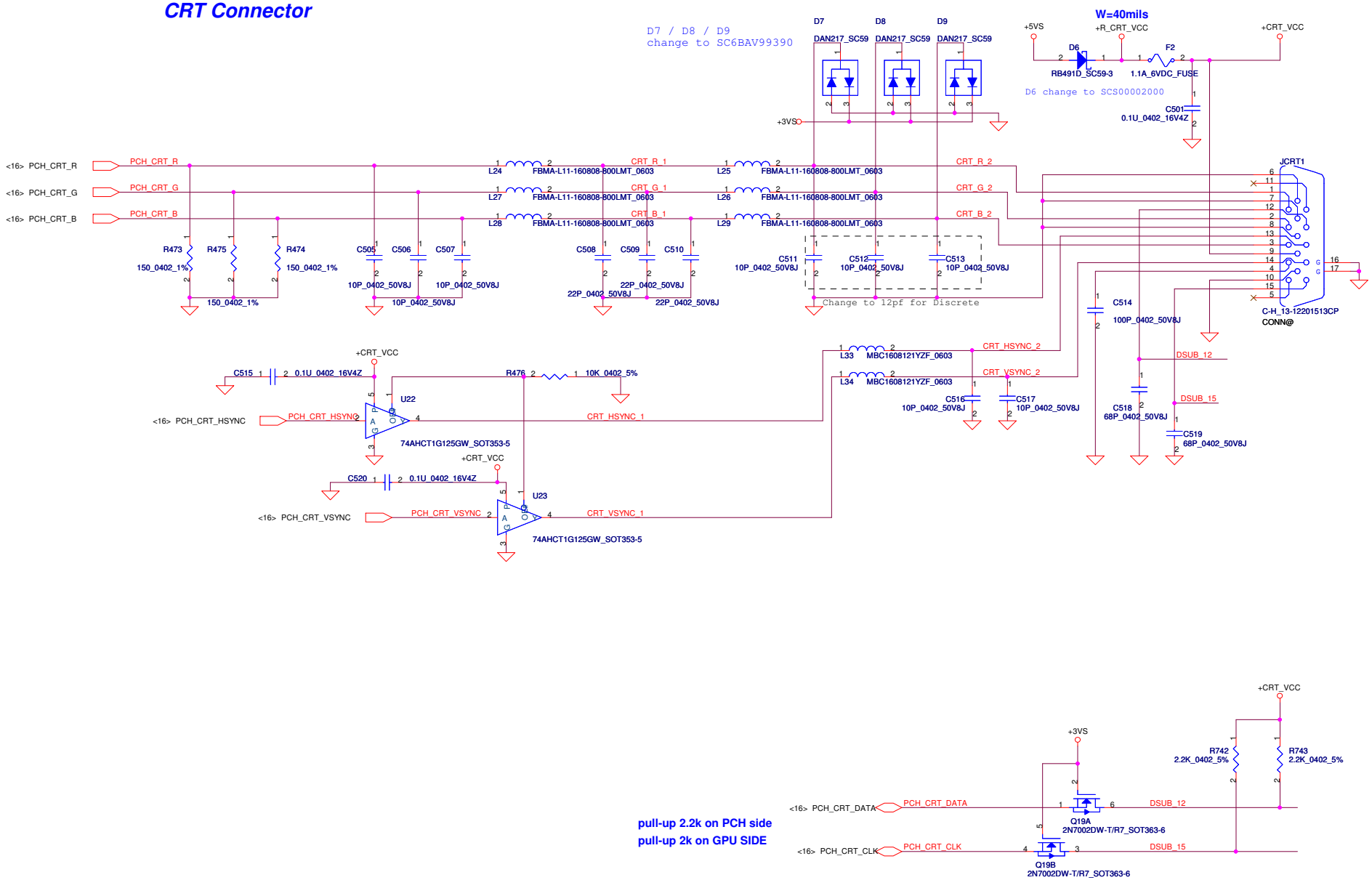
Compal Electronics, Inc.

Title: LVDS Connector

Size	Document Number	Rev
Custom	PEW71 M/B LA-6582P Schematic	1.0

Date: Thursday, July 08, 2010 | Sheet 22 of 48

CRT Connector



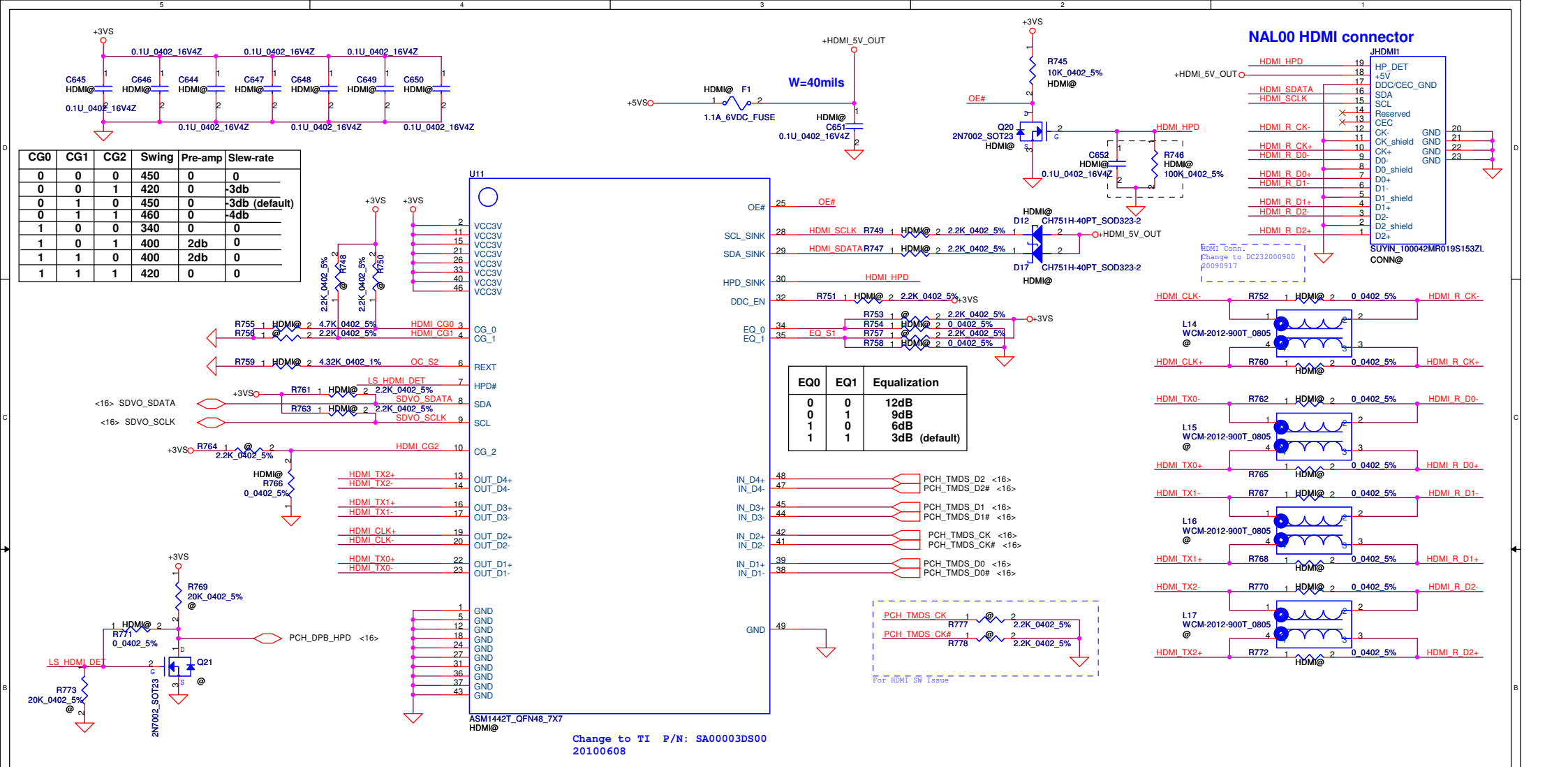
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
B	PEW71 M/B LA-6582P Schematic	1.0

Date: Thursday, July 08, 2010 | Sheet 23 of 48



CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

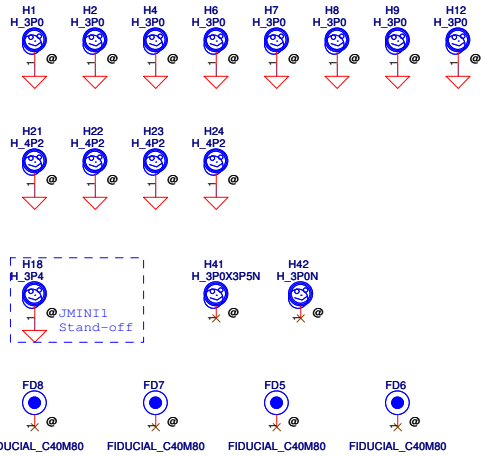
Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

Compal Electronics, Inc.

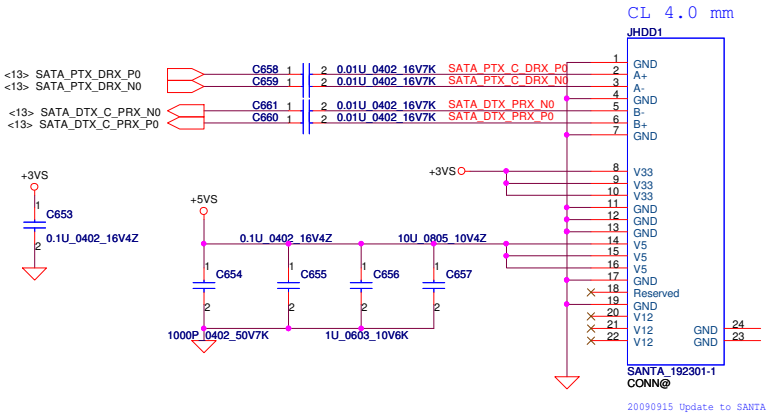
Title: HDMI Level Shife & Conn

Size: Custom | Document Number: PEW71 M/B LA-6582P Schematic | Rev: 1.0

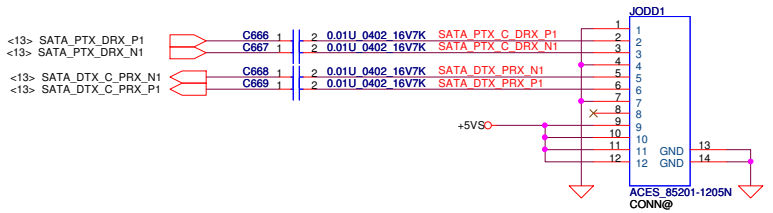
Date: Thursday, July 08, 2010 | Sheet 24 of 48



SATA HDD1 Conn.



SATA ODD FFC Conn.



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title	HDD & ODD & Screw Hole	
Size B	Document Number PEW71 M/B LA-6582P Schematic	Rev 1.0
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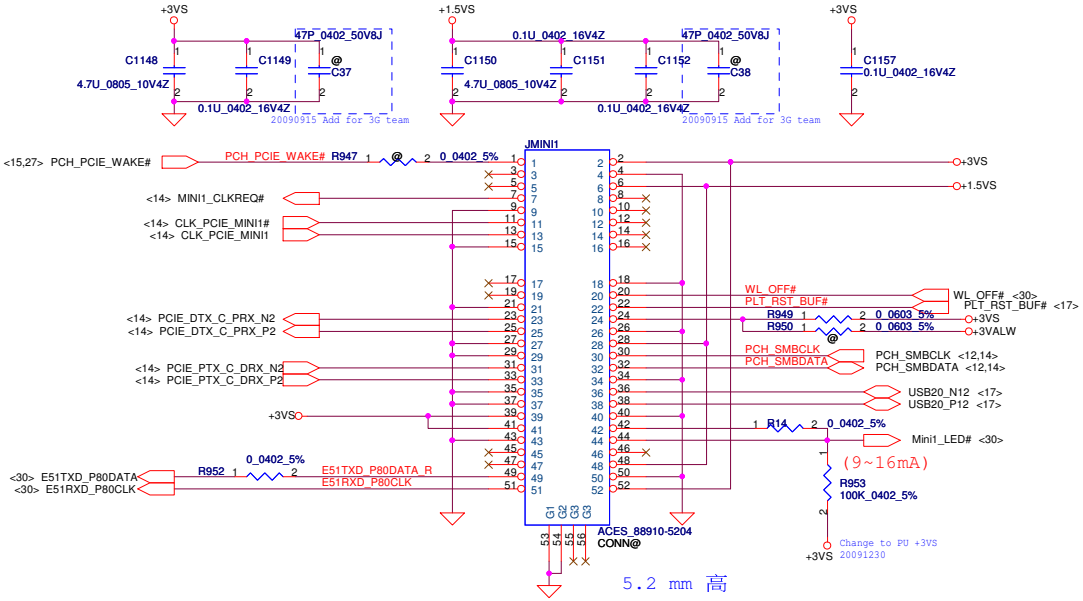
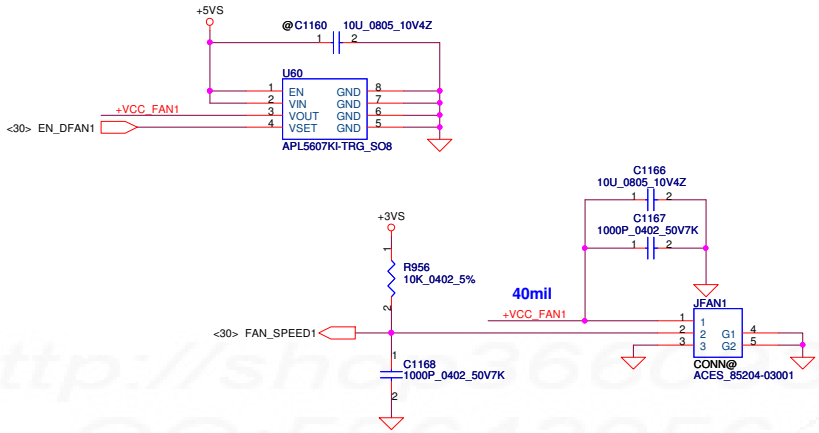
For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Del 3G / GPS Module Connect

FAN1 Conn



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: MINI CARD (WLAN & 3G)/FAN

Size	Document Number	Rev
B	PEW71 M/B LA-6582P Schematic	1.0

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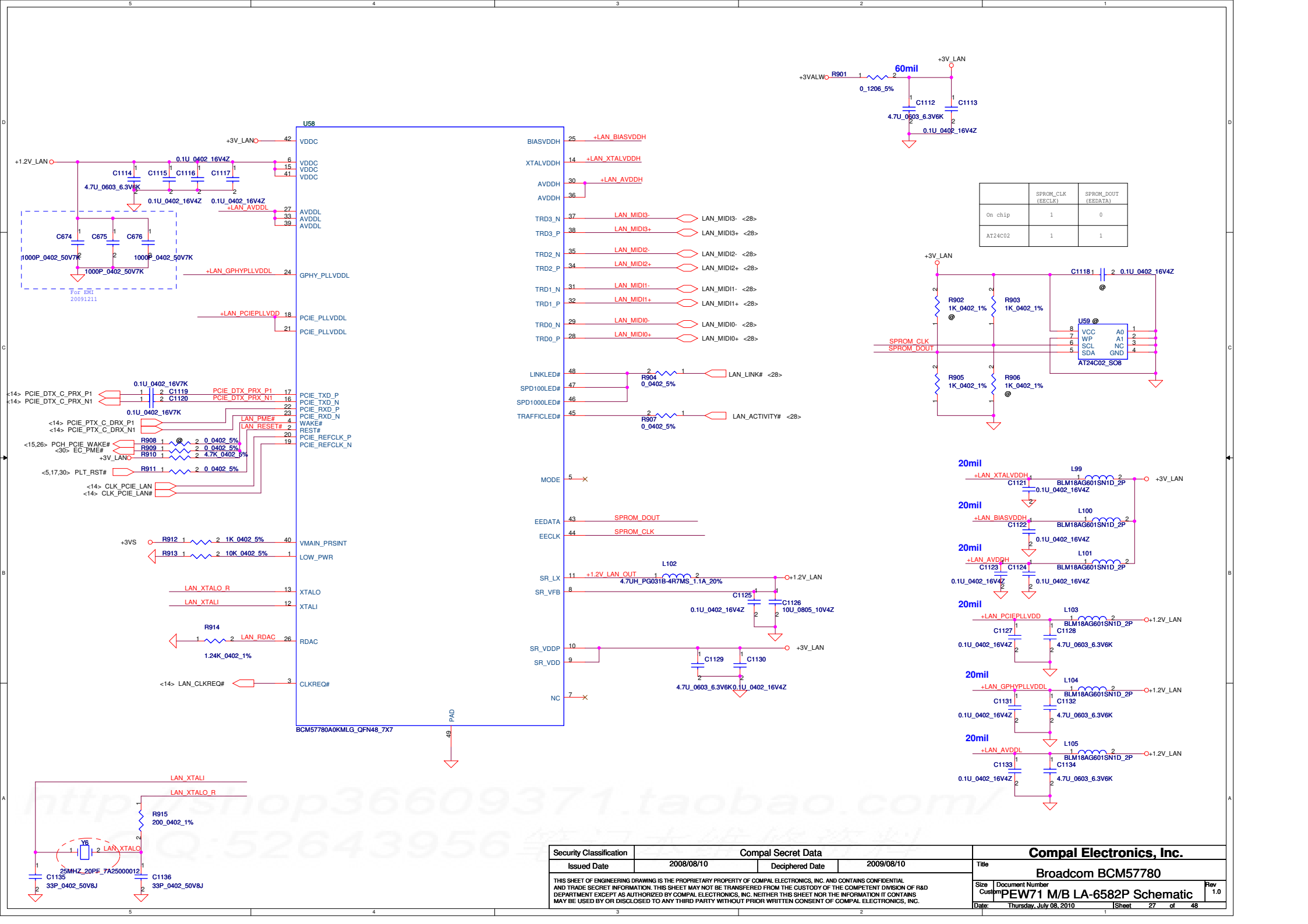

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title: Broadcom BCM57780

Size: Custom | Document Number: PEW71 M/B LA-6582P Schematic | Rev: 1.0

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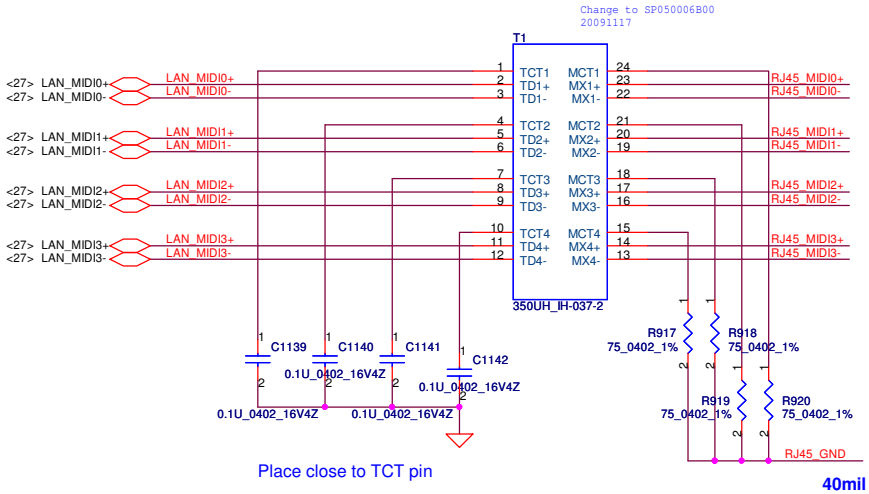
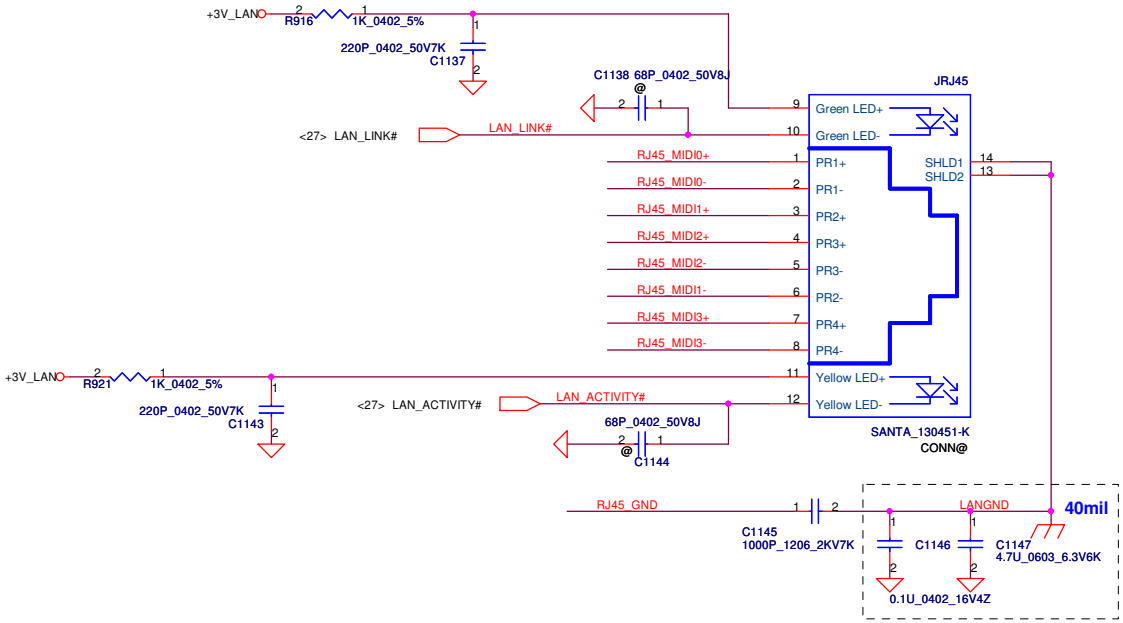
LAN Connector





Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.		
Title: LAN Magnetic & RJ45		
Size: Custom	Document Number: PEW71 M/B LA-6582P Schematic	Rev: 1.0
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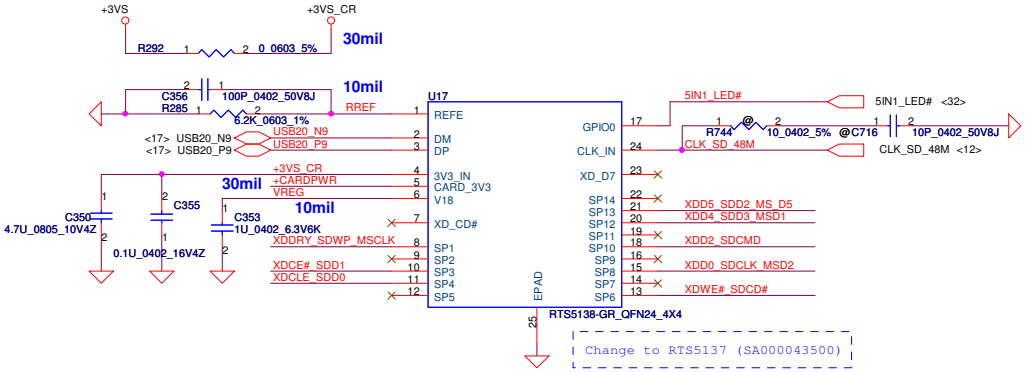
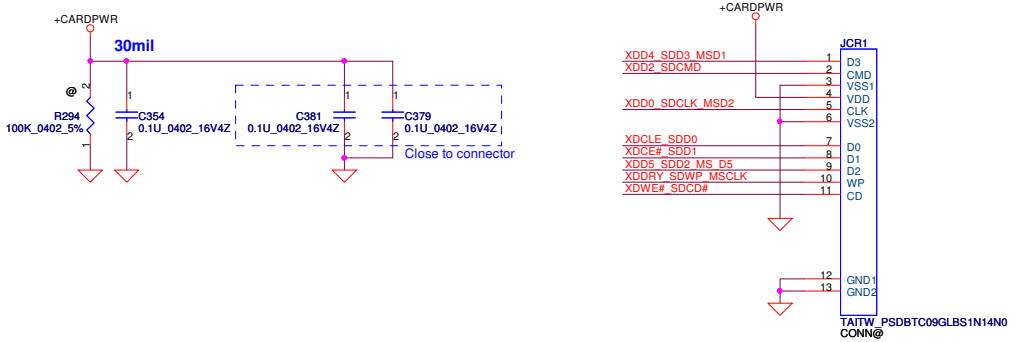
Card Reader RTS5138 / RTS5137
(only SD+MMC function)

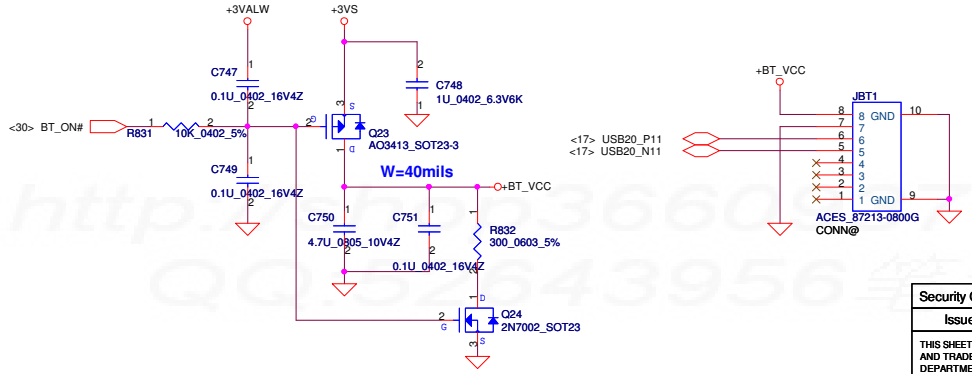


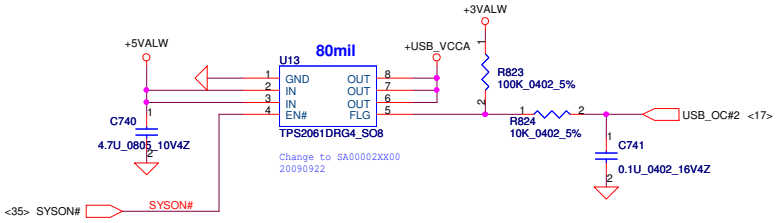
Card Reader Connector

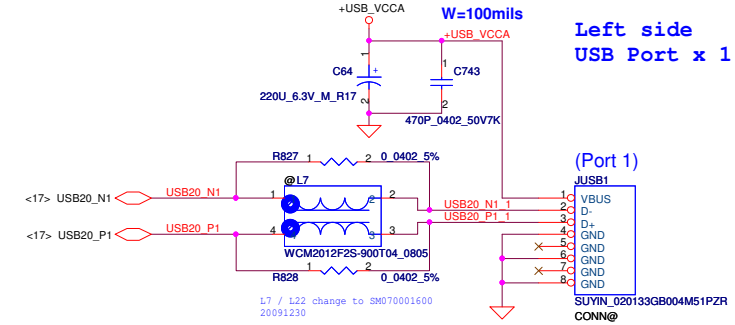


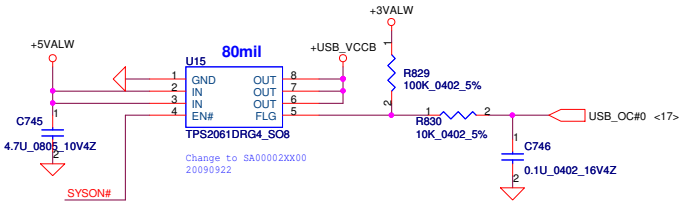
Bluetooth Conn.

Q23 change to SB934130020



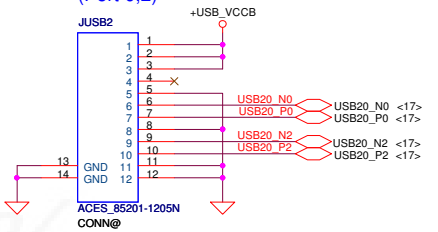






USB/B Conn.

(Port 0,2)



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: USB & Card reader& BT Connector

Size	Document Number	Rev
B	PEW71 M/B LA-6582P Schematic	1.0

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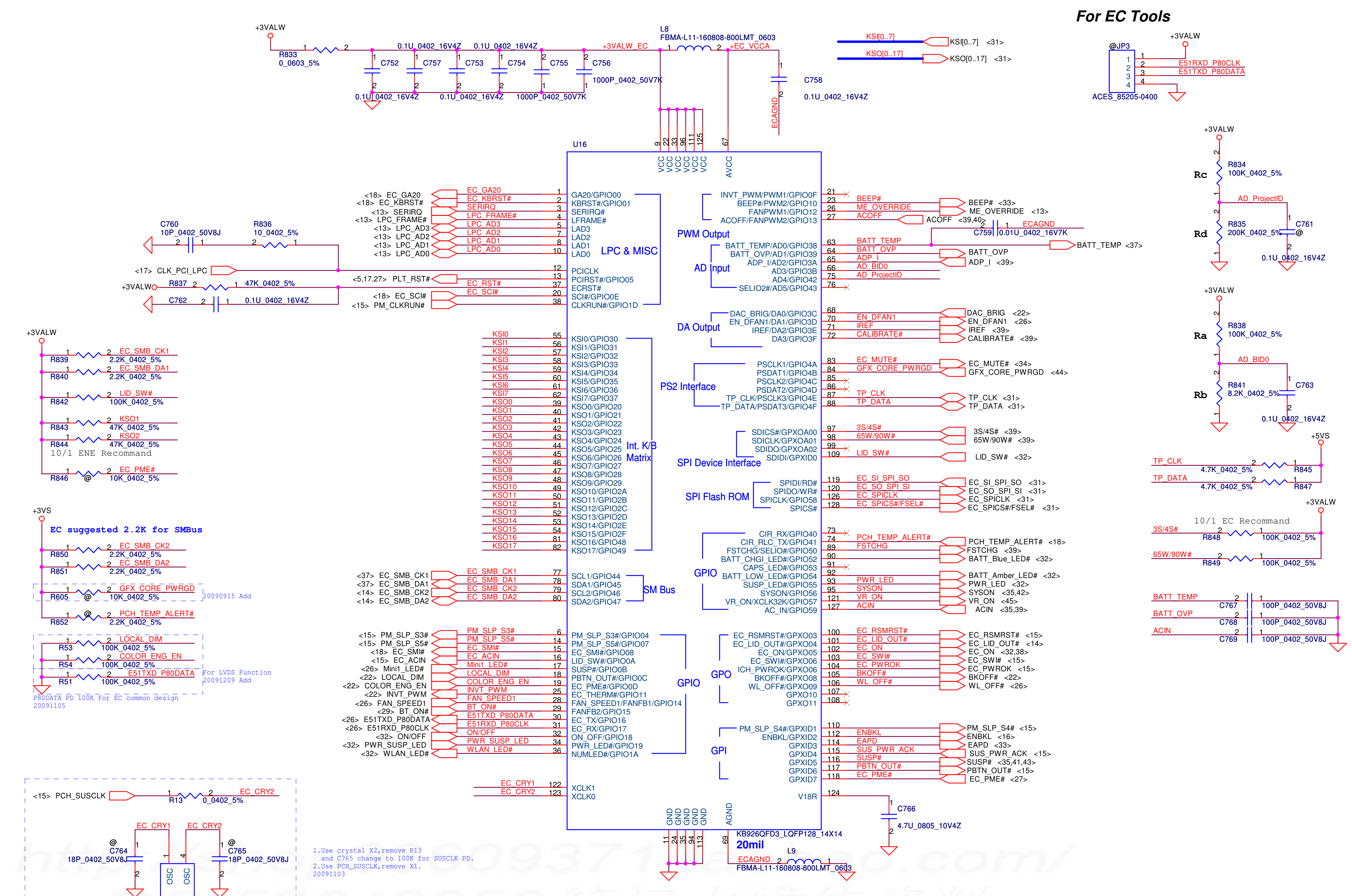
For EC Tools
+3VALW
R833
0_0603_5%
0.1U_0402_16V4Z
C752
C757
C753
C754
C755
C756
1000P_0402_50V7K
+3VALW_EC
L8
FBMA-L11-160808-800LMT_0603
+EC_VCCA
C758
0.1U_0402_16V4Z
ECAGND
KSI[0..7]
KSO[0..17]
KSI[0..7] <31>
KSO[0..17] <31>
@JP3
E51RXD_P80CLK
E51TXD_P80DATA
ACES_85205-0400
U16
VCC
AVCC
GA20/GPIO00
KBRST#/GPIO01
SERIRQ#
LFRAME#
LAD3
LAD2
LAD1
LAD0
LPC & MISC
PCICLK
PCIRST#/GPIO05
ECRST#
SCI#/GPIO0E
CLKRUN#/GPIO1D
<18> EC_GA20
<18> EC_KBRST#
<13> SERIRQ
<13> LPC_FRAME#
<13> LPC_AD3
<13> LPC_AD2
<13> LPC_AD1
<13> LPC_AD0
C760
10P_0402_50V8J
R836
10_0402_5%
<17> CLK_PCI_LPC
<5,17,27> PLT_RST#
R837
47K_0402_5%
C762
0.1U_0402_16V4Z
<18> EC_SCI#
<15> PM_CLKRUN#
EC_RST#
EC_SCI#
PWM Output
INVT_PWM/PWM1/GPIO0F
BEEP#/PWM2/GPIO10
FANPWM1/GPIO12
ACOFF/FANPWM2/GPIO13
BEEP# <33>
ME_OVERRIDE <13>
ACOFF <39,40>
C759
0.01U_0402_16V7K
AD Input
BATT_TEMP/AD0/GPIO38
BATT_OVP/AD1/GPIO39
ADP_I/AD2/GPIO3A
AD3/GPIO3B
AD4/GPIO42
SELIO2#/AD5/GPIO43
BATT_TEMP <37>
BATT_OVP
ADP_I <39>
AD_BID0
AD_ProjectID
DA Output
DAC_BRIG/DA0/GPIO3C
EN_DFAN1/DA1/GPIO3D
IREF/DA2/GPIO3E
DA3/GPIO3F
DAC_BRIG <22>
EN_DFAN1 <26>
IREF <39>
CALIBRATE# <39>
PS2 Interface
PSCLK1/GPIO4A
PSDAT1/GPIO4B
PSCLK2/GPIO4C
PSDAT2/GPIO4D
TP_CLK/PSCLK3/GPIO4E
TP_DATA/PSDAT3/GPIO4F
EC_MUTE# <34>
GFX_CORE_PWRGD <44>
TP_CLK <31>
TP_DATA <31>
Int. K/B Matrix
SPI Device Interface
SDICS#/GPXOA00
SDICLK/GPXOA01
SDIDO/GPXOA02
SDIDI/GPXID0
3S/4S# <39>
65W/90W# <39>
LID_SW# <32>
SPI Flash ROM
SPIDI/RD#
SPIDO/WR#
SPICLK/GPIO58
SPICS#
EC_SI_SPI_SO <31>
EC_SO_SPI_SI <31>
EC_SPICLK <31>
EC_SPICS#/FSEL# <31>
GPIO
CIR_RX/GPIO40
CIR_RLC_TX/GPIO41
FSTCHG/SELIO#/GPIO50
BATT_CHGI_LED#/GPIO52
CAPS_LED#/GPIO53
BATT_LOW_LED#/GPIO54
SUSP_LED#/GPIO55
SYSON/GPIO56
VR_ON/XCLK32K/GPIO57
AC_IN/GPIO59
PCH_TEMP_ALERT# <18>
FSTCHG <39>
BATT_Blue_LED# <32>
BATT_Amber_LED# <32>
PWR_LED <32>
SYSON <35,42>
VR_ON <45>
ACIN <35,39>
SM Bus
SCL1/GPIO44
SDA1/GPIO45
SCL2/GPIO46
SDA2/GPIO47
<37> EC_SMB_CK1
<37> EC_SMB_DA1
<14> EC_SMB_CK2
<14> EC_SMB_DA2
GPO
EC_RSMRST#/GPXO03
EC_LID_OUT#/GPXO04
EC_ON/GPXO05
EC_SWI#/GPXO06
ICH_PWROK/GPXO06
BKOFF#/GPXO08
WL_OFF#/GPXO09
GPXO10
GPXO11
EC_RSMRST# <15>
EC_LID_OUT# <14>
EC_ON <32,38>
EC_SWI# <15>
EC_PWROK <15>
BKOFF# <22>
WL_OFF# <26>
GPIO
PM_SLP_S3#/GPIO04
PM_SLP_S5#/GPIO07
EC_SMI#/GPIO08
LID_SW#/GPIO0A
SUSP#/GPIO0B
PBTN_OUT#/GPIO0C
EC_PME#/GPIO0D
EC_THERM#/GPIO11
FAN_SPEED1/FANFB1/GPIO14
FANFB2/GPIO15
EC_TX/GPIO16
EC_RX/GPIO17
ON_OFF/GPIO18
PWR_LED#/GPIO19
NUMLED#/GPIO1A
<15> PM_SLP_S3#
<15> PM_SLP_S5#
<18> EC_SMI#
<15> EC_ACIN
<26> Mini1_LED#
<22> LOCAL_DIM
<22> COLOR_ENG_EN
<22> INVT_PWM
<26> FAN_SPEED1
<29> BT_ON#
<26> E51TXD_P80DATA
<26> E51RXD_P80CLK
<32> ON/OFF
<32> PWR_SUSP_LED
<32> WLAN_LED#
GPI
PM_SLP_S4#/GPXID1
ENBKL/GPXID2
GPXID3
GPXID4
GPXID5
GPXID6
GPXID7
PM_SLP_S4# <15>
ENBKL <16>
EAPD <33>
SUS_PWR_ACK <15>
SUSP# <35,41,43>
PBTN_OUT# <15>
EC_PME# <27>
XCLK1
XCLK0
V18R
C766
4.7U_0805_10V4Z
GND
AGND
KB926QFD3_LQFP128_14X14
20mil
L9
ECAGND
FBMA-L11-160808-800LMT_0603
+3VALW
R839
R840
2.2K_0402_5%
EC_SMB_CK1
EC_SMB_DA1
R842
LID_SW#
100K_0402_5%
R843
R844
KSO1
KSO2
47K_0402_5%
10/1 ENE Recommand
R846
EC_PME#
10K_0402_5%
+3VS
EC suggested 2.2K for SMBus
R850
R851
EC_SMB_CK2
EC_SMB_DA2
R605
GFX_CORE_PWRGD
20090915 Add
R852
PCH_TEMP_ALERT#
R53
LOCAL_DIM
R54
COLOR_ENG_EN
R51
E51TXD_P80DATA
For LVDS Function
20091209 Add
P80DATA PD 100K for EC common design
20091105
<15> PCH_SUSCLK
R13
0_0402_5%
EC_CRY1
EC_CRY2
C764
18P_0402_50V8J
C765
X2
32.768KHZ_12.5PF_Q13MC14610002
1.Use crystal X2,remove R13
and C765 change to 100K for SUSCLK PD.
2.Use PCH_SUSCLK,remove X1.
20091103
For EC SUSCLK PD 100K
C765
100K_0402_5%
+3VALW
Rc
R834
100K_0402_5%
Rd
R835
200K_0402_5%
C761
0.1U_0402_16V4Z
Ra
R838
100K_0402_5%
Rb
R841
8.2K_0402_5%
C763
+5VS
TP_CLK
TP_DATA
4.7K_0402_5%
R845
R847
+3VALW
10/1 EC Recommand
3S/4S#
65W/90W#
R848
R849
100K_0402_5%
BATT_TEMP
BATT_OVP
ACIN
C767
C768
C769
100P_0402_50V8J

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/4/15	Deciphered Date 2010/04/15	Title: EC ENE KB926

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Size	Document Number	Rev
B	PEW71 M/B LA-6582P Schematic	1.0

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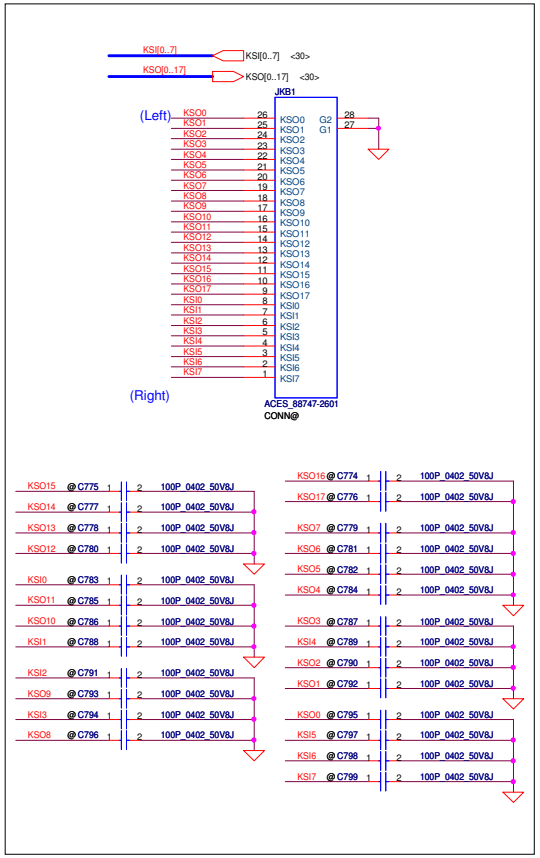

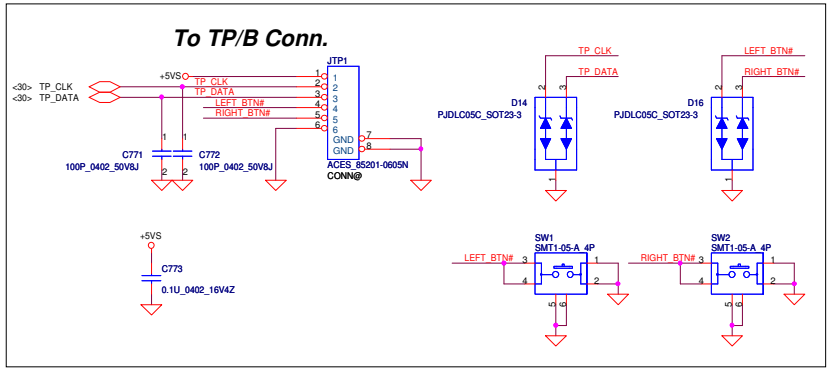

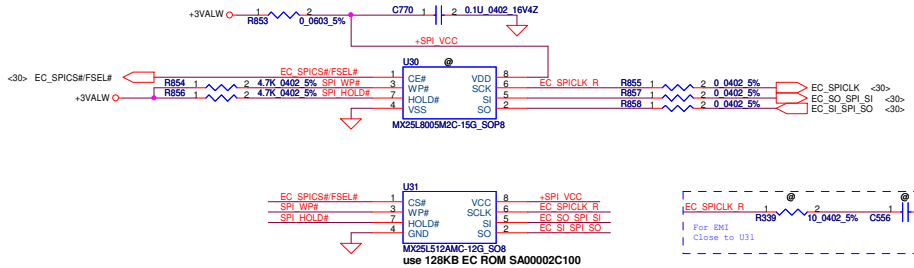

ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

To BTN/B Conn.

	KSO0	KSO3
KSI1	WL_BTN#	Program_BTN#
KSI2	T/P lock_BTN#	
KSI3	Back up_BTN#	Volum up_BTN#
KSI4	BT_BTN#	Volum down_BTN#
KSI5	Power save_BTN#	

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size: C | Document Number: PEW71 M/B LA-6582P Schematic | Rev: 1.0

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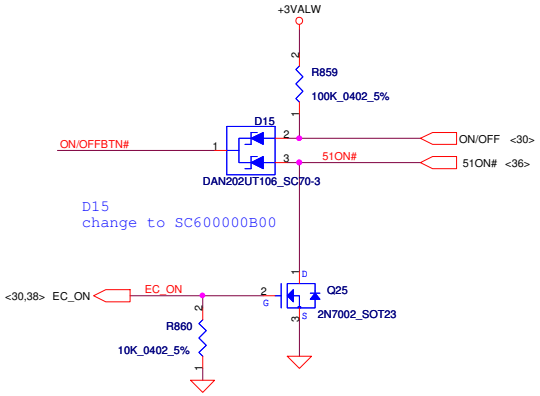
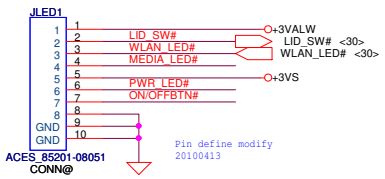
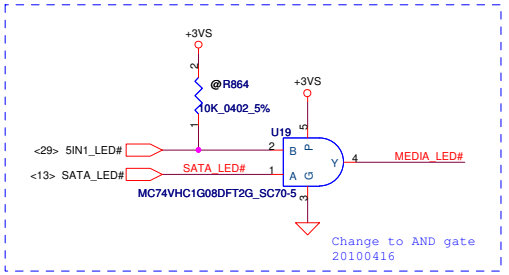
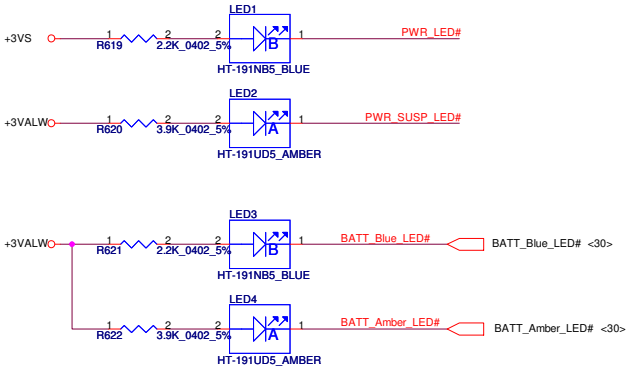
Power Button

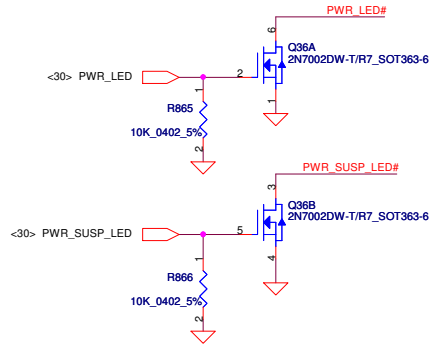


LED/B LEFT









Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: <Title>

Size	Document Number	Rev
B	PEW71 M/B LA-6582P Schematic	1.0

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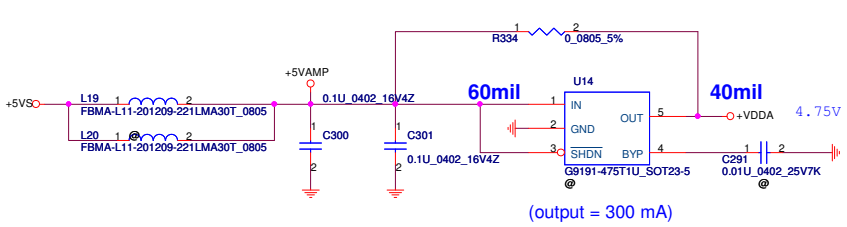
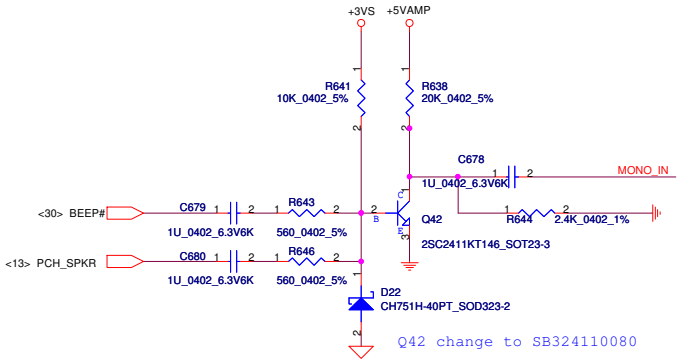
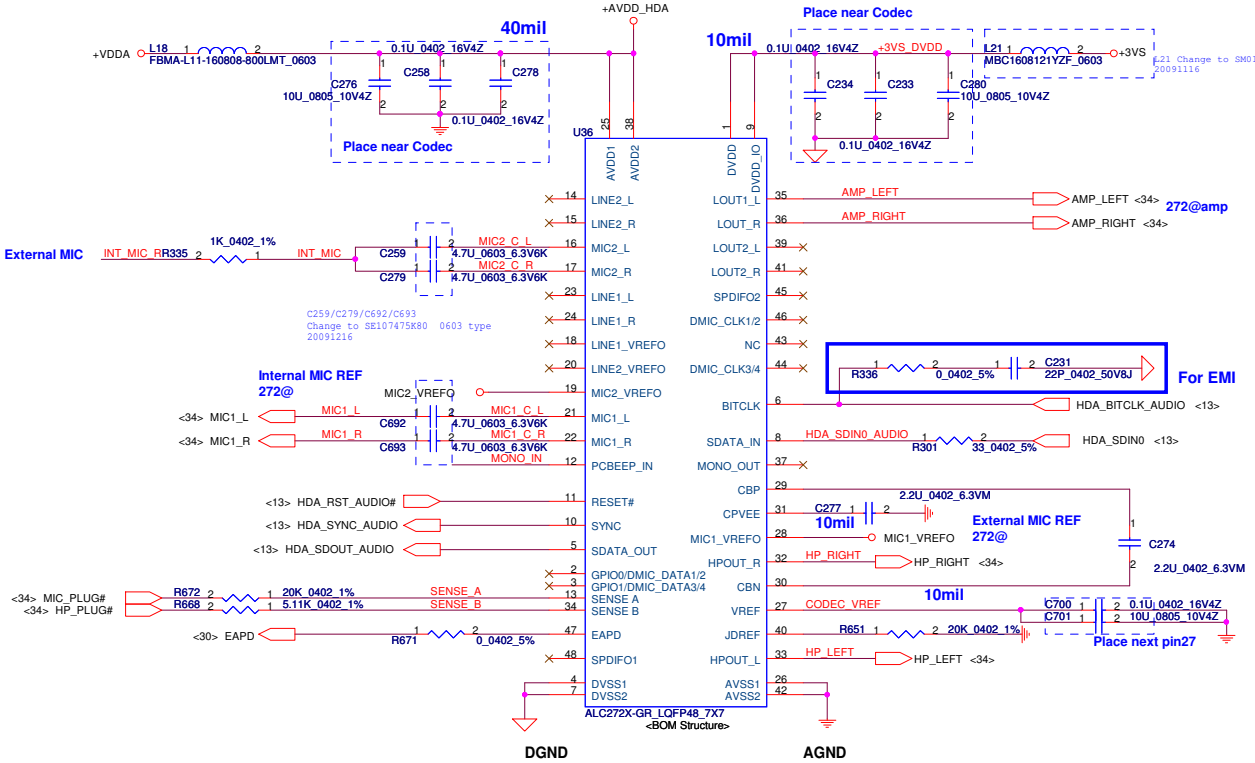
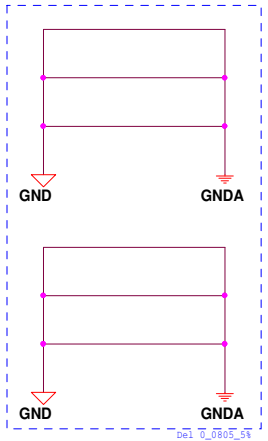




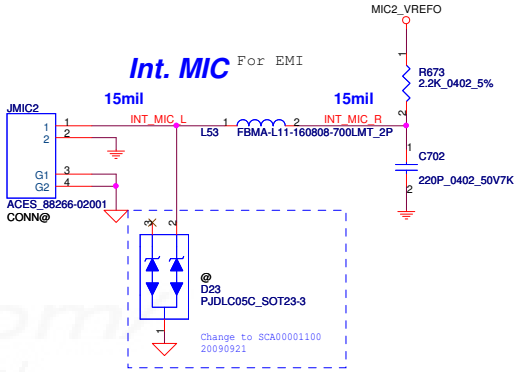
HD Audio Codec





Int. MIC

For EMI



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

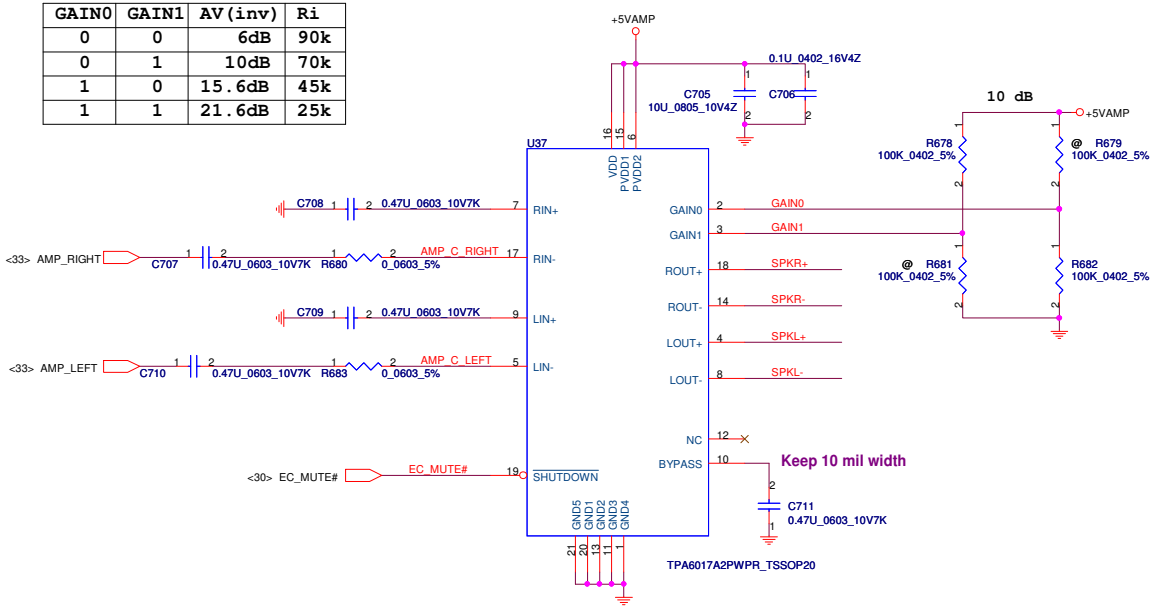
Compal Electronics, Inc.

Title: HD Audio Codec ALC271X/272X

Size: Custom | Document Number: PEW71 M/B LA-6582P Schematic | Rev: 1.0

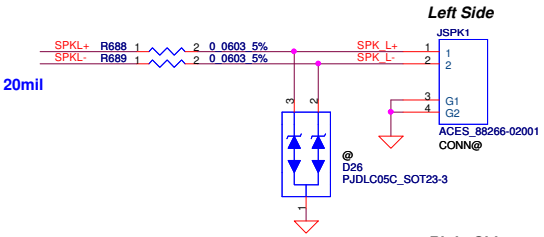
Date: Thursday, July 08, 2010 | Sheet 33 of 48

GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

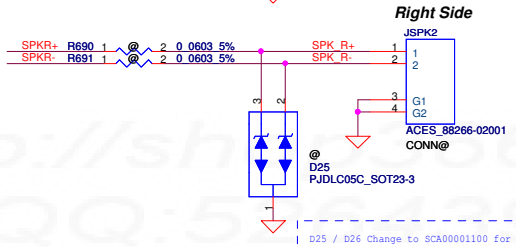


Int. Speaker Conn.

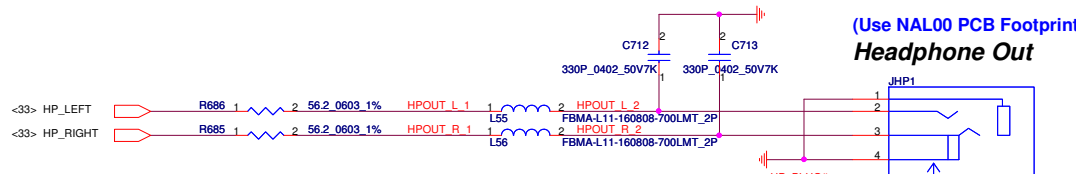
Left Side

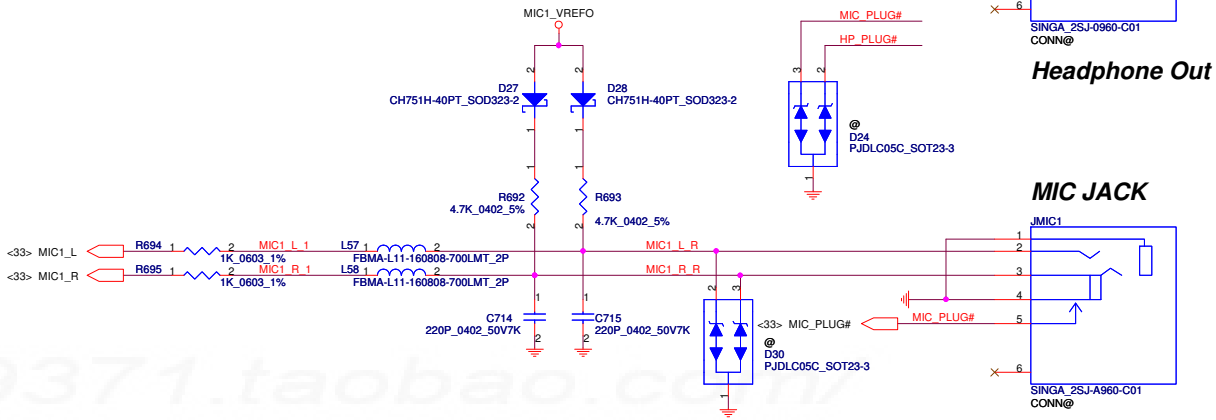


Right Side



D25 / D26 Change to SCA00001100 for ESD 20090921





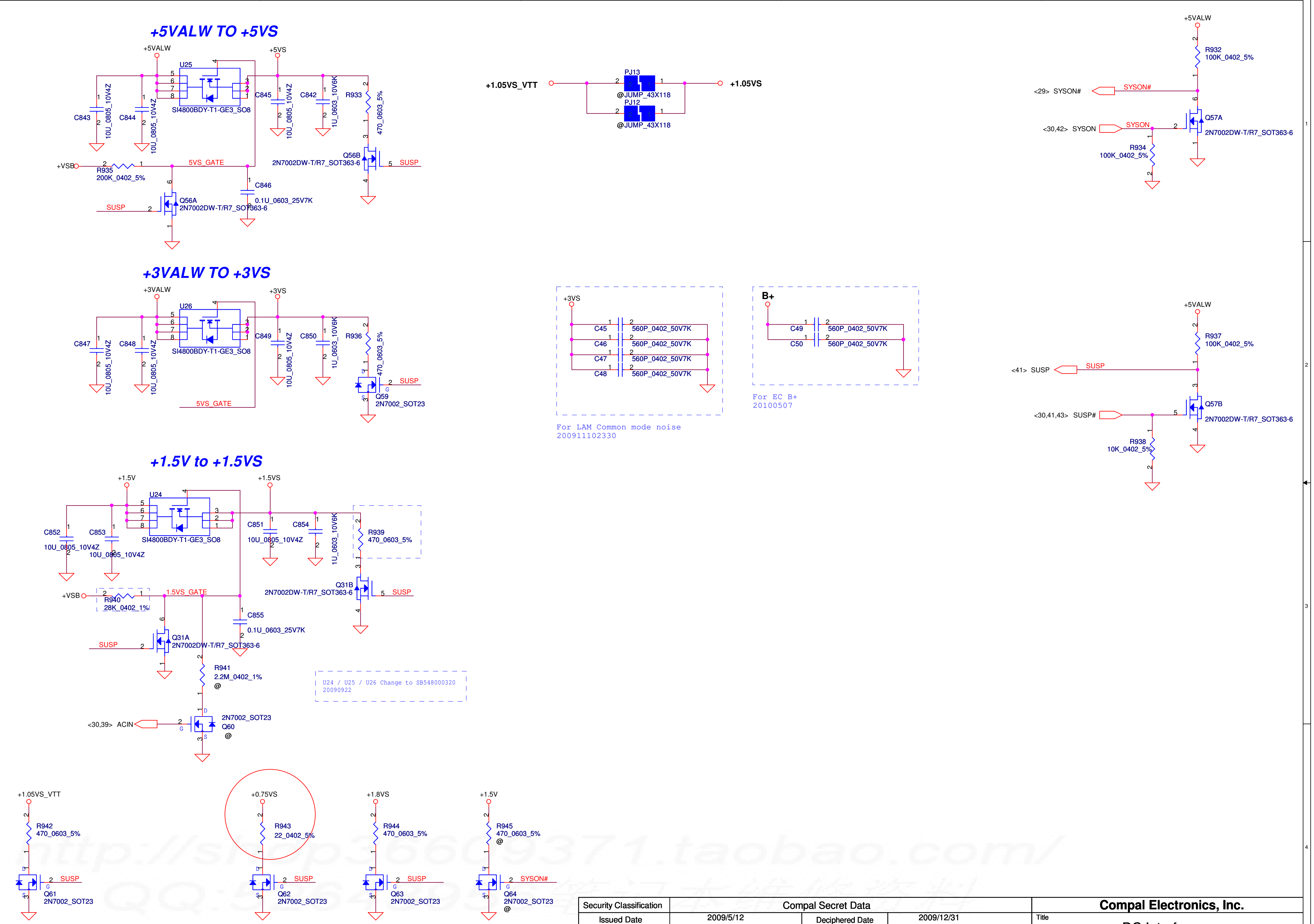
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title: Amplifier & Audio Jack

Size: Custom | Document Number: PEW71 M/B LA-6582P Schematic | Rev: 1.0

Date: Thursday, July 08, 2010 | Sheet 34 of 48



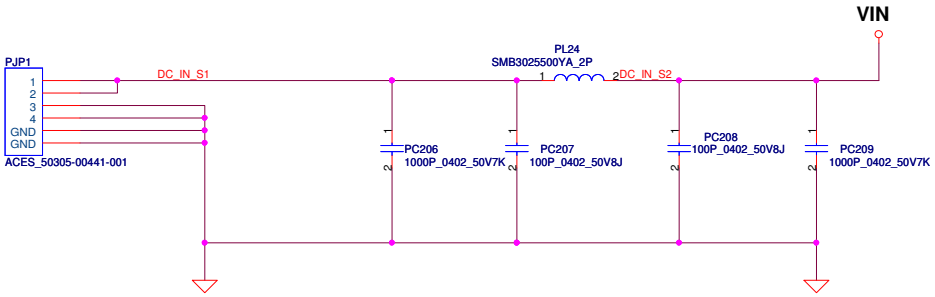
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

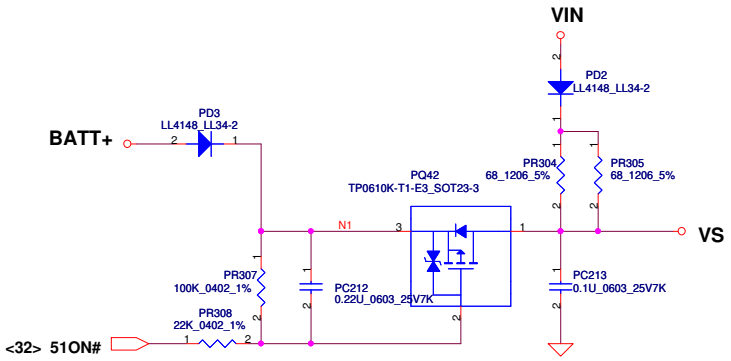
Compal Electronics, Inc.

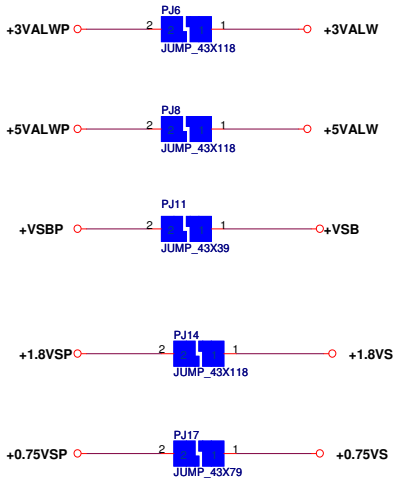
Title: DC Interface

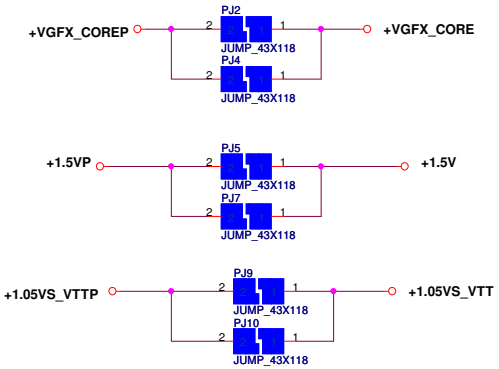
Size: B | Document Number: PEW71 M/B LA-6582P Schematic | Rev: 1.0

Date: Thursday, July 08, 2010 |









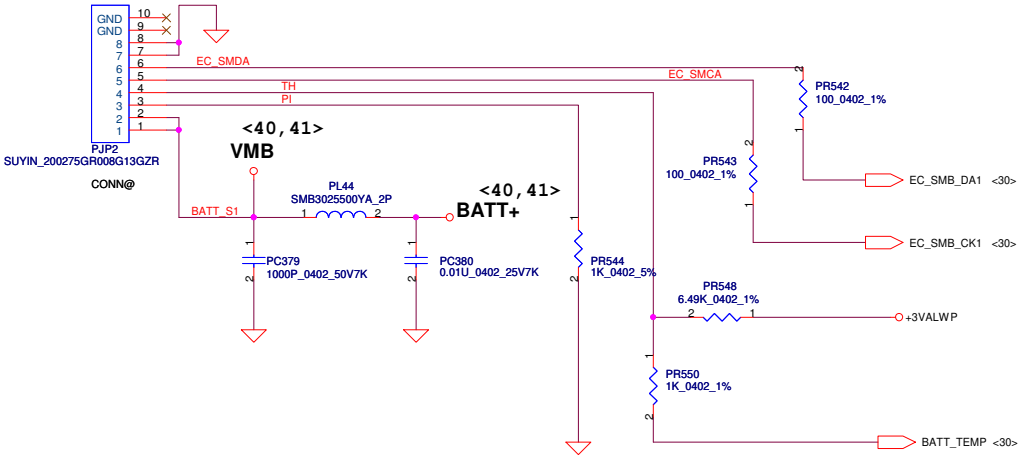
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: **DCIN**

Size	Document Number	Rev
Custom	PEW71 M/B LA-6582P Schematic	1.0

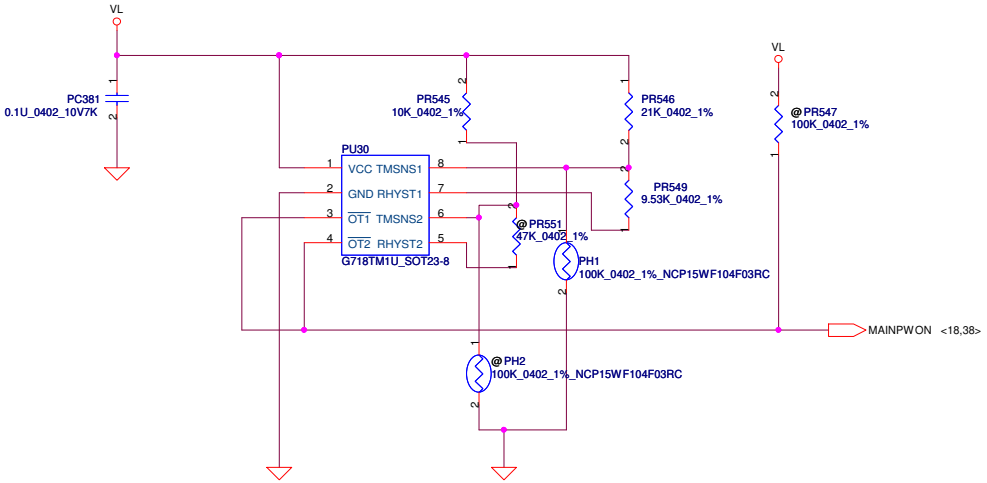
Date: Thursday, July 08, 2010 | Sheet 36 of 48

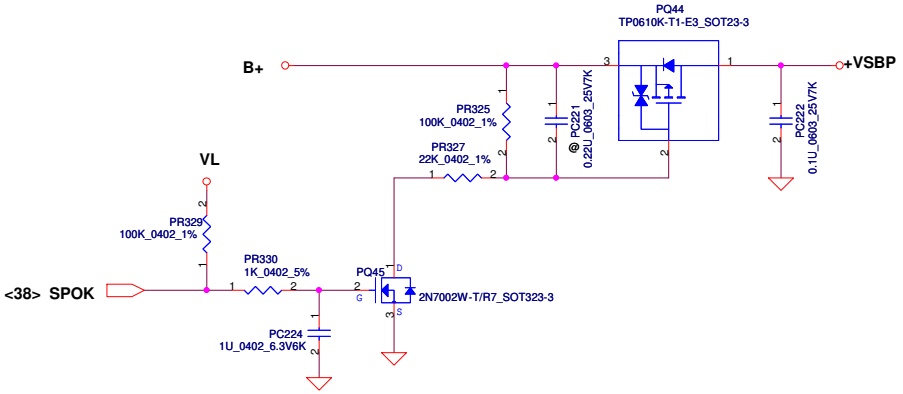


PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
Custom	PEW71 M/B LA-6582P Schematic	1.0

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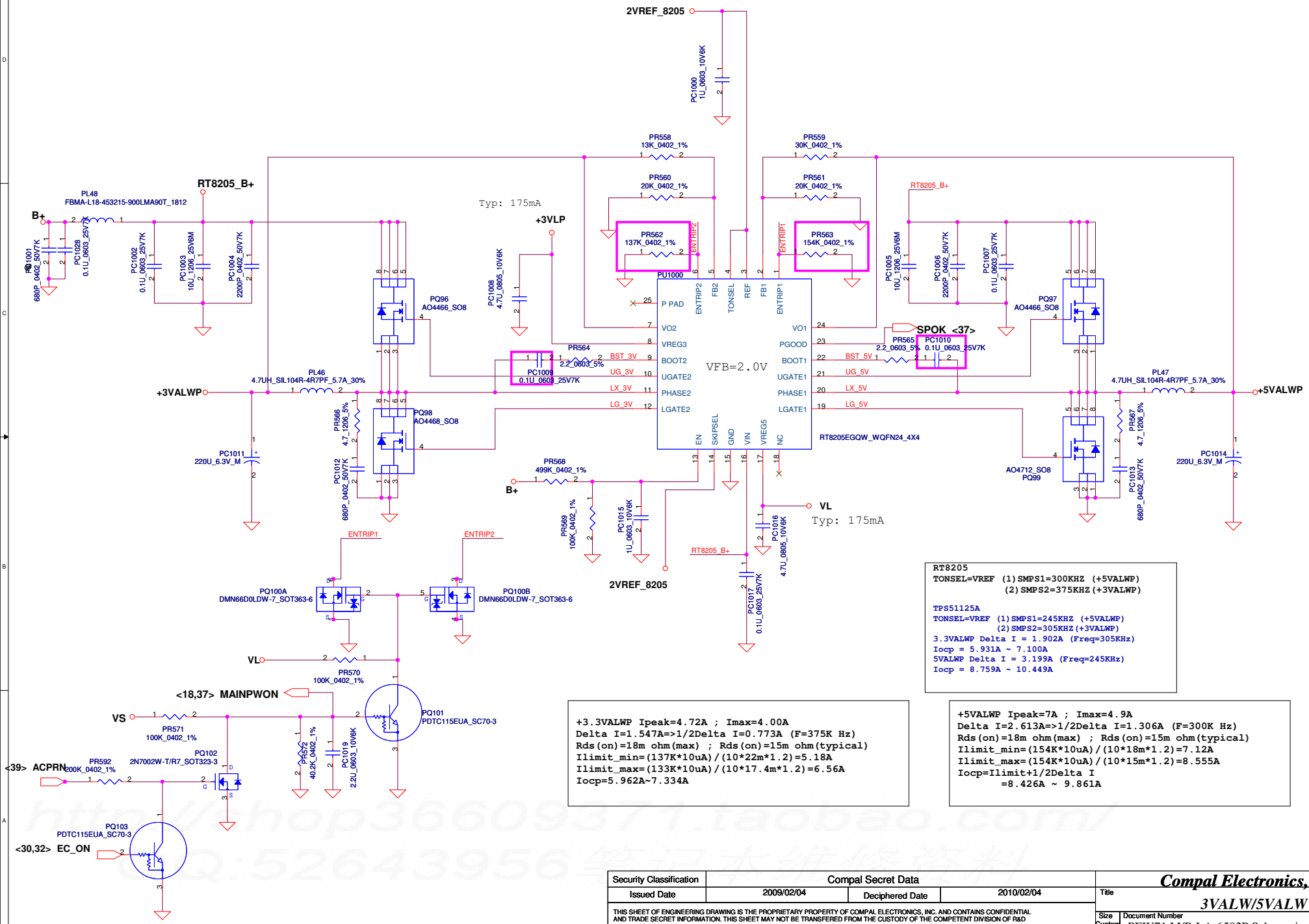
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ (+3VALWP)

TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ (+3VALWP)
3.3VALWP Delta I = 1.902A (Freq=305KHz)
Iocp = 5.931A ~ 7.100A
5VALWP Delta I = 3.199A (Freq=245KHz)
Iocp = 8.759A ~ 10.449A

+3.3VALWP Ipeak=4.72A ; Imax=4.00A
Delta I=1.547A=>1/2Delta I=0.773A (F=375K Hz)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(137K*10uA)/(10*22m*1.2)=5.18A
Ilimit_max=(133K*10uA)/(10*17.4m*1.2)=6.56A
Iocp=5.962A~7.334A

+5VALWP Ipeak=7A ; Imax=4.9A
Delta I=2.613A=>1/2Delta I=1.306A (F=300K Hz)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(154K*10uA)/(10*18m*1.2)=7.12A
Ilimit_max=(154K*10uA)/(10*15m*1.2)=8.555A
Iocp=Ilimit+1/2Delta I
=8.426A ~ 9.861A

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: 3VALW/5VALW

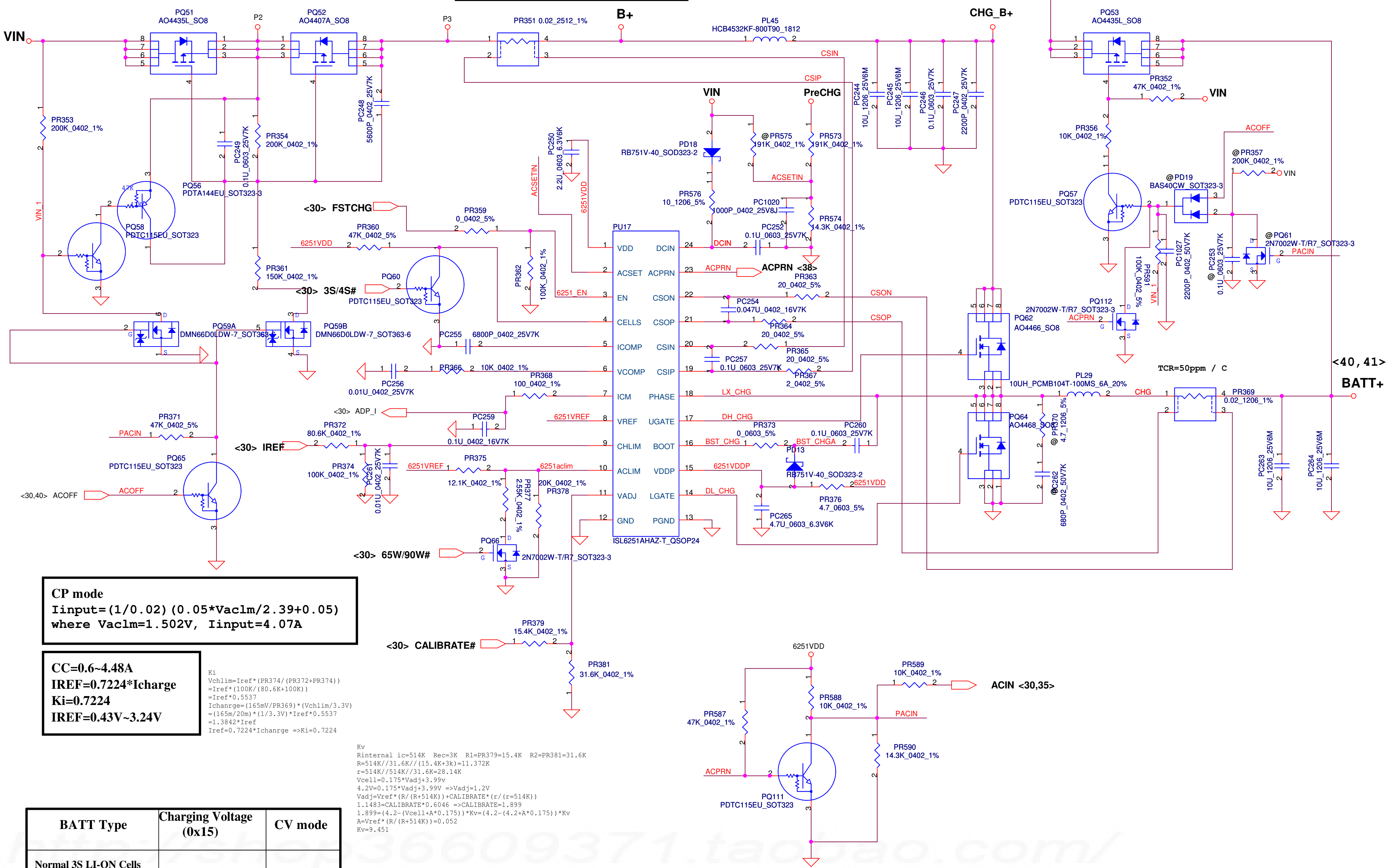
Size	Document Number	Rev
Custom	PEW71 M/B LA-6582P Schematic	1.0

Date: Thursday, July 08, 2010 Sheet 38 of 48

Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
IREF=0.7224*Icharge
Ki=0.7224
IREF=0.43V~3.24V

```
Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224
```

```
Kv
Rinternal ic=514K  Rec=3K  R1=PR379=15.4K  R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451
```

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

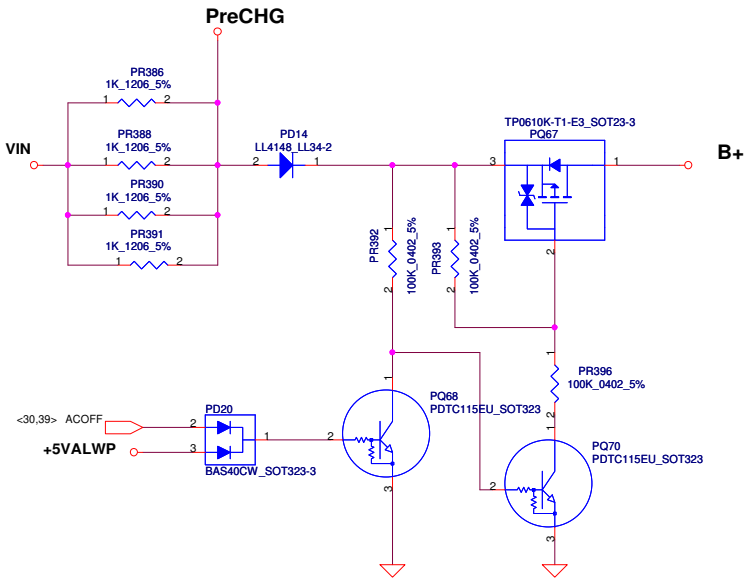
-

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title
CHARGER

Size Custom | Document Number PEW71 M/B LA-6582P Schematic | Rev 1.0



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

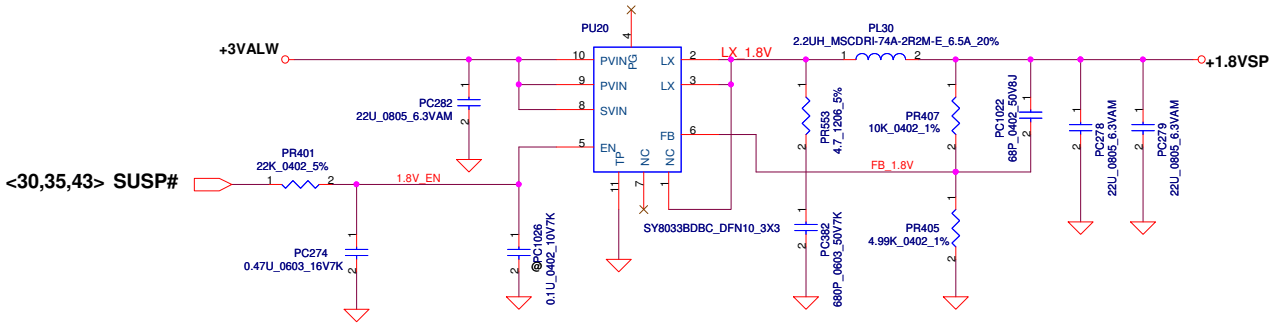
Compal Electronics, Inc.

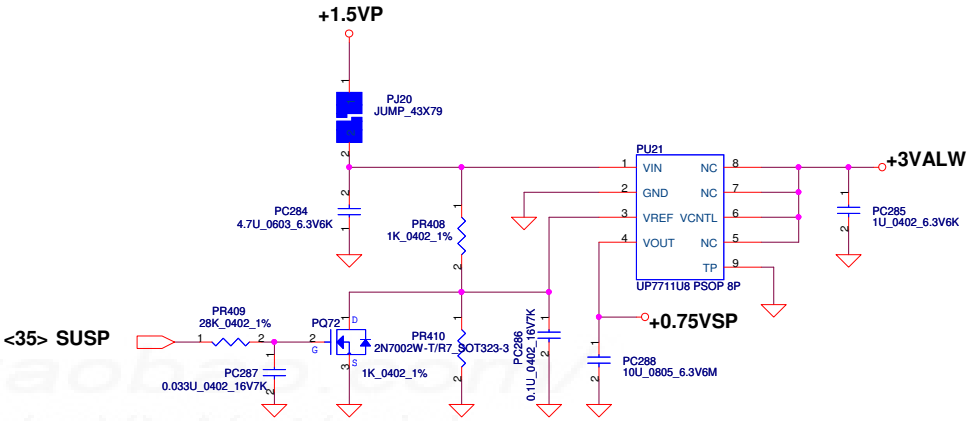
Title: **PRECHARGE**

Size	Document Number	Rev
Custom	PEW71 M/B LA-6582P Schematic	1.0

Date: Thursday, July 08, 2010 | Sheet 40 of 48

FB=0.6V
Note:Iload(max)=3.5A





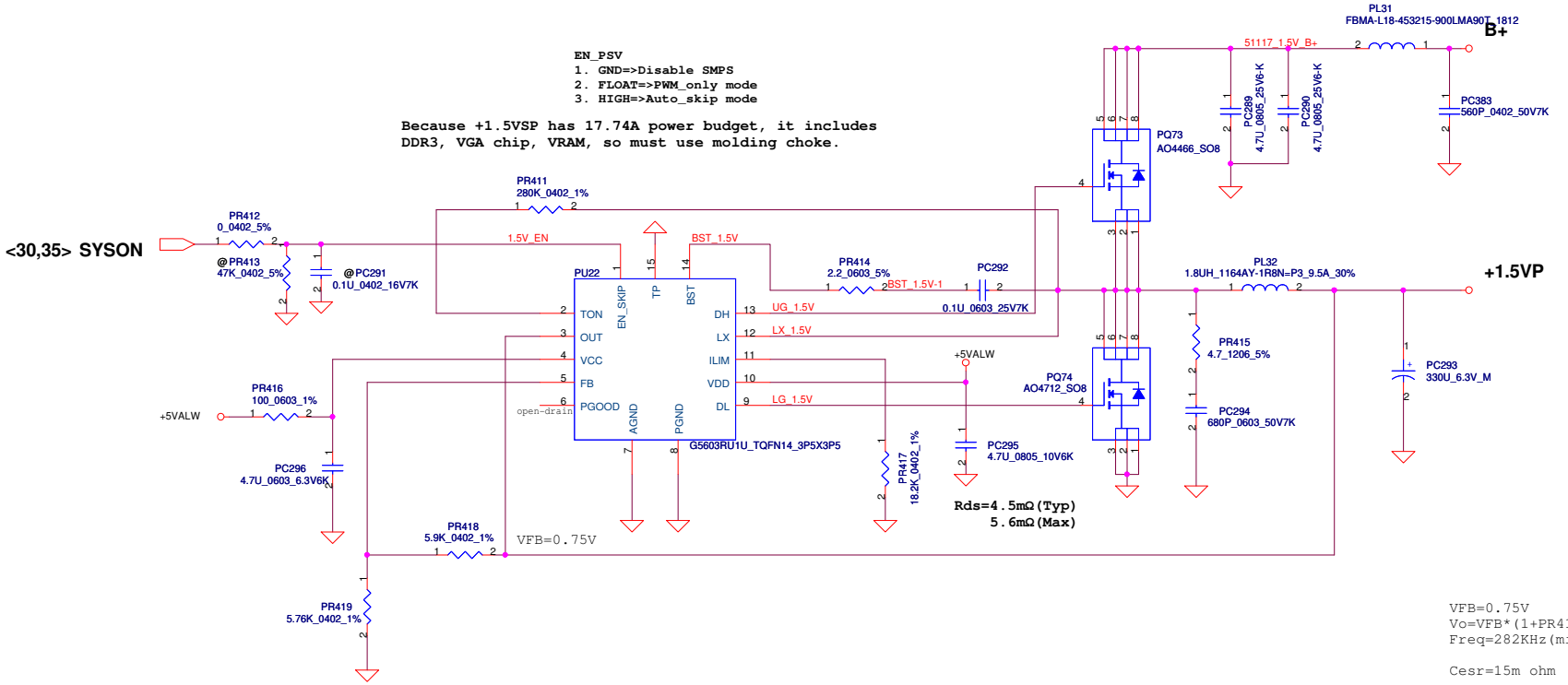
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: **+1.8VSP/+0.75VSP**

Size	Document Number	Rev
Custom	PEW71 M/B LA-6582P Schematic	1.0

Date: Thursday, July 08, 2010 | Sheet 41 of 48



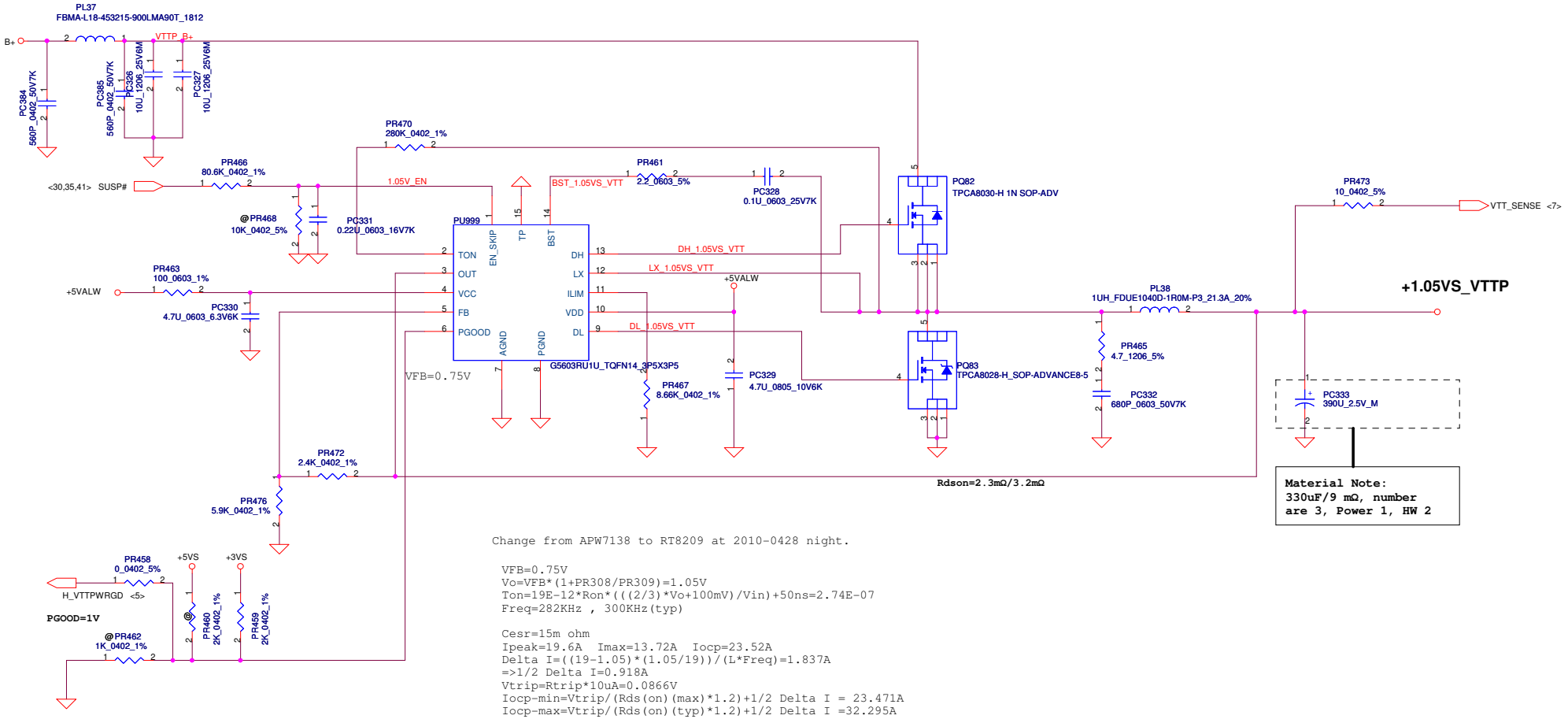
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title: **1.5VP**

Size	Document Number	Rev
Custom	PEW71 M/B LA-6582P Schematic	1.0

Date: Thursday, July 08, 2010 | Sheet 42 of 48



Change from APW7138 to RT8209 at 2010-0428 night.

VFB=0.75V
Vo=VFB*(1+PR308/PR309)=1.05V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=2.74E-07
Freq=282KHz , 300KHz(typ)

Cesr=15m ohm
Ipeak=19.6A Imax=13.72A Iocp=23.52A
Delta I=((19-1.05)*(1.05/19))/(L*Freq)=1.837A
=>1/2 Delta I=0.918A
Vtrip=Rtrip*10uA=0.0866V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+1/2 Delta I = 23.471A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+1/2 Delta I =32.295A
Iocp=22.4A~30.8A

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

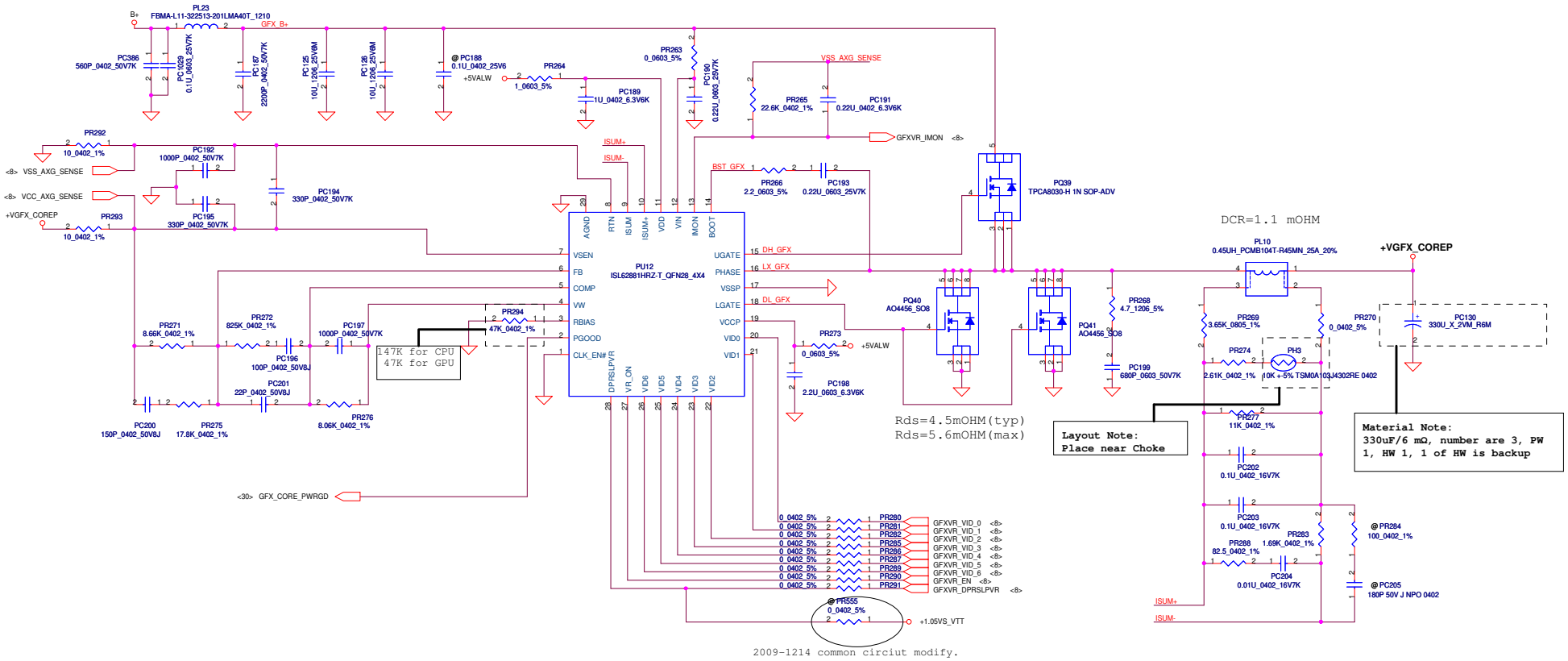
Compal Electronics, Inc.

Title: +1.1VS_VTTP

Size: Custom | Document Number: PEW71 M/B LA-6582P Schematic | Rev: 1.0

Date: Thursday, July 08, 2010 | Sheet 43 of 48

Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



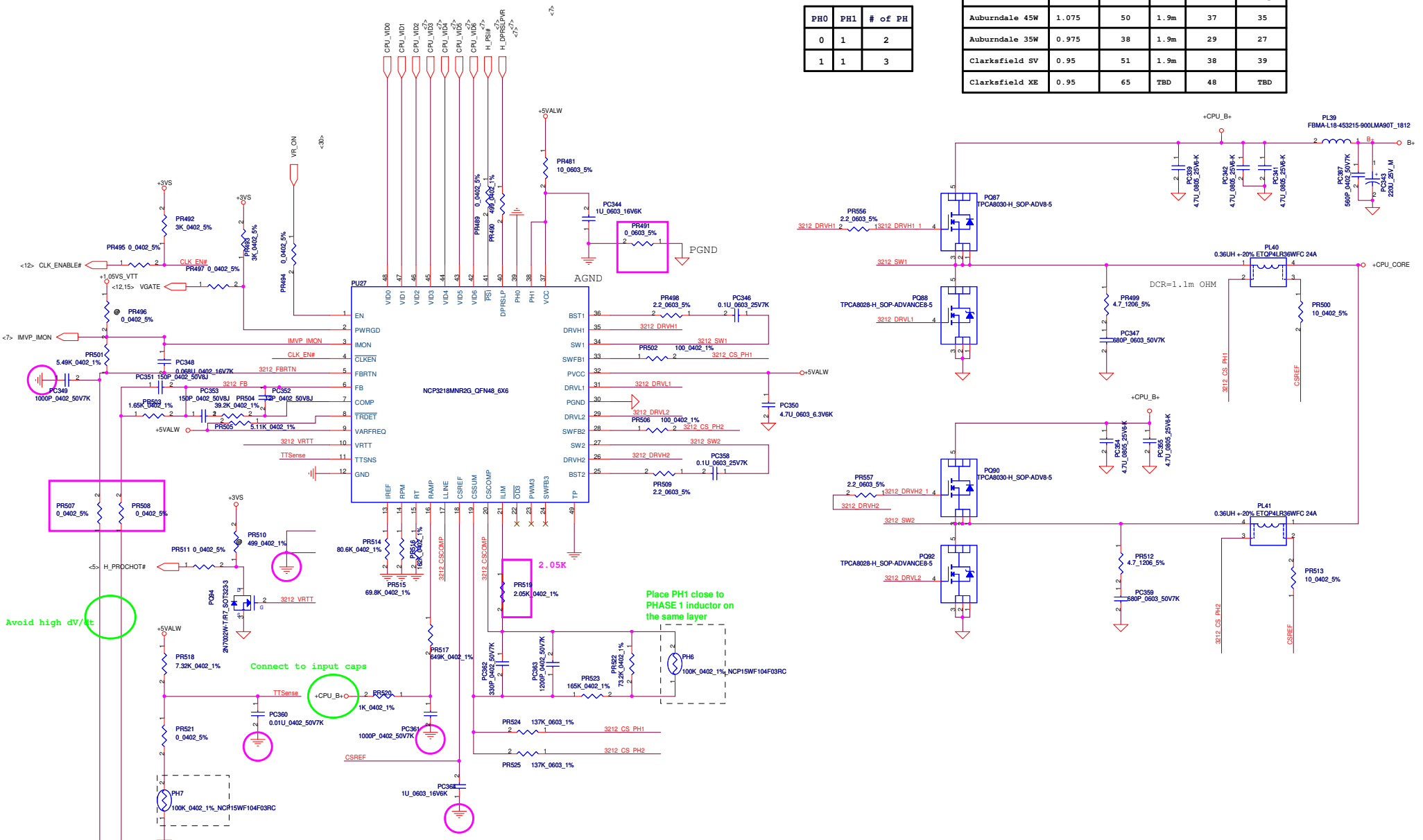
2009-1214 common circiut modify.

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

Compal Electronics, Inc.			
Title	GFX_COREP		
Size C	Document Number PEW71 M/B LA-6582P Schematic		Rev 1.0
Date: Thursday, July 08, 2010		Sheet 44 of 48	

PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Compal Electronics, Inc.

Title: CPU_CORE

Size: C | Document Number: PEW71 M/B LA-6582P Schematic | Rev: 1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1 2 3	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	39	Change PR353 from SD034470280 to SD034200380. Change PR371 from SD034220280 to SD034470280. Change PR587 from SD034100380 to SD034470280. Change PR590 from SD034200280 to SD034143280. Change PR591 from SD028470280 to SD028100380. Add PC1027 SE074222K80(S CER CAP 2200P 0402 50V7K) Change PQ111 from SB000006800 to SB301150200	2010/06/08	to PVT
4	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	38	Add PQ102 and PQ103 SB301150200. Add PR592 SD034200380.	2010/06/08	to PVT
5 6	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	40	Change PR386 from SD011000080 to SD011100180. Add PR388, PR390, PR391 SD011100180. Add PD14 SC100001Y80 LL4148_LL34-2	2010/06/08	to PVT
7 8	EMI fail, add 3/5V snubber and Boost Resister to silve it.	EMI request to solve EMI issue.	0.1	38	Add PR566 and PR567 SD001470B80 S RES 4.7 1206 5% Add PC1012 and PC1013 SE074681K80 S CER CAP 680P 0402 50V7K Change PR564 and PR565 from SD013000080 to SD013220B80	2010/06/08	to PVT
	EMI fail, add 1.5V snubber.	EMI request to solve EMI issue.	0.1	42	Add PR415 SD001470B80 4.7 1206 5%. Add PC294 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
9 10	EMI fail, add 1.05V snubber. and Boost Resister.	EMI request to solve EMI issue.	0.1	43	Add PR465 SD001470B80 4.7 1206 5%. Add PC332 SE025681K80 S CER CAP 680P 50V K X7R 0603 Change PR461 from SD013000080 to SD013220B80	2010/06/08	to PVT
11	EMI fail, add GFX_CORE snubber.	EMI request to solve EMI issue.	0.1	44	Add PR268 SD001470B80 4.7 1206 5%. Add PC199 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
12 13	HW power sequence modify.	HW request.	0.1	43	Change PR466 from SD034576280 S RES 1/16W 57.6K +-1% 0402 to SD034806280 S RES 80.6K 0402 1%) Change PC331 from SE076104K80 S CER CAP .1U 16V K X7R to SE00000R700 S CER CAP 0.22U 16V K X7R 0402	2010/06/08	to PVT
14	BOM unique.	BOM unique.	0.1	38	Chnage PQ101 from SB301150000 to SB301150200.	2010/06/08	to PVT
15	EMI request.	EMI request.	0.1	38	Add PC1028 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
16	EMI request.	EMI request.	0.1	44	Add PC1029 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
17	Sourcer request to change a common part.	Sourcer request.	0.1	38	Change PC1019 from SE00000GC00 S CER CAP 2.2U 10V K X7R 0603 to SE000003H00 S CER CAP 2.2UF 10V K X5R 0603	2010/06/08	to PVT
18	Per sourcer request.	Sourcer request to change PC331 from SE00000R700 to SE026224K80 for common part.	0.1	43	change PC331 from SE00000R700 to SE026224K80	2010/06/08	to PVT
19	CPU transient issue.	Need modify PC362 to 330P due to transient fail.	0.1	45	Change PC362 from SE074561K80 S CER CAP 560P 50V K X7R 0402 to SE074331K80 S CER CAP 330P 50V K X7R 0402	2010/06/08	to PVT
20	Per sourcer request.	Per sourcer request.	0.1	43 44	Chnage PQ39/PQ82 from SB000008L80 to SB00000HL00.	2010/06/08	to PVT
21	Cost down.	Cost down 3VALWP and Charger Low Side MOS.	0.1	38 39	Change PQ98 from SB00000AJ00 to SB000009580(AO4468). Change PQ64 from SB00000CG00 to SB000009580(AO4468).	2010/06/08	to PVT
22	Cost down.	Cost down +1.5VP Low side MOS and choke.	0.1	42	Chnage PQ74 from SB000009F80 to SB00000AJ00(AO4712). CHnage PL32 from SH000009U00 to SH000009680.	2010/06/08	to PVT
23	Cost down.	re-caculate 1.5VP OCP.	0.1	42	Change PR417 from SD034110280 to SD034182280.	2010/06/08	to PVT

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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title: PIR (PWR)
				Size: Custom; Document Number; Rev 1.0
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Cost down.	re-caculate +3VALWP OCP.	0.1	38	Change PR562 from SD034107380 to SD034137380.	2010/06/08	to PVT
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Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Title: PIR (PWR)

Size	Document Number	Rev
Custom		1.0

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Version change list (P.I.R. List)

Item	Phase	PAGE	DATE	Modifycatio list	Purpose
1	EVT		04 / 08	N/A	
			04 / 16	Modify RTC SCH Change LAN to AR8152 Update Power SCH	
			04 / 21	Update AND Gate symbol - U1 / U2 / U6 / U7 / U19 Update Power MOS symbol - U24 / U25 / U26 C196 change to 1U for INTEL disign CLK GEN del C35 / C36 / C30 / C31 / C32 / C33 / C34 / L3 (for 3G@ and @ function) Q4+Q6 change to 2N7002DW Update U8 symbol Add DMIC function Modify USB define.	
			04 / 26	Update Power SCH	
			04 / 27	Add R17 for DMIC power	
			04 / 29	Update Power SCH Change LAN to GIGA&10/100 co-lay Del R307 (LVDS conn.) Change +1.05VS_VTT to +1.05VS (CLK GEN) Change C842 / C850 / C854 / C656 to SE080105K80 1U_0603_10V6K Change R940 to 28K (S3 Power sequence)	
			04 / 29	SW T1 pin define (LAN)	
			05 / 03	Change R907 (0_0603) to 0_1206 5% Remove C40 / C41 / C42 / C43 / C44 Change FAN Conn.	
			05 / 03	Update Power SCH Change LAN to BCM57780 GIGA	
			05 / 06	Del R637 / R639 / R640 / R645 / R647 / R648 (AUDIO) Del DMIC	
			05 / 07	Update Power SCH Add C49 / C50 (EC B+)	
			05 / 10	Update Power SCH	
			05 / 11	C764 / C765 change to 18P_0402_50V8J (EC) Reserve D13 / D24 / D30 (ESD)	
			05 / 12	U17 change to RTS5137 (SA000043500) Card reader	
			05 / 13	Update Power SCH	
			06 / 01	Unpop L11 / C247 & Pop R304 for cost down Unpop C764 / X2 & Pop R13 & C765 Change to 100K for EC remove Crystal Pop R834 & R835 change to 200K for Project ID	
			06 / 02	Unpop D24 / D30 Unpop R690 / R691 Pop C49 / C50 For HDMI Unpop R753 / R757 , Add R754 / R758 to 0 ohm. Change R759 to 3.9K. Change R755 to 4.7K ohm , Unpop R748. Unpop R778. R833 / R292 0_0805 change to 0_0603.	
			06 / 03	C190 / C191 & C1135 / C1136 change to 33P 0402 50V8J for Vender test report	
			06 / 04	Unpop C774~C799 for EMI cost down.	
			06 / 10	Update Power SCH Add T25 / T26 / T27	
			07 / 07	Update Power SCH	
			07 / 08	Change R759 to 4.32K_1% SD00000J280	

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Size	Document Number	Rev
Custom	PEW71 M/B LA-6582P Schematic	1.0

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