

Discrete/UMA /Muxless Schematics Document

AMD LIANO CPU FS1

AMD GPU Manhattan(Park/Madison M2) and Vancouver(Seymour/Whistler M2)

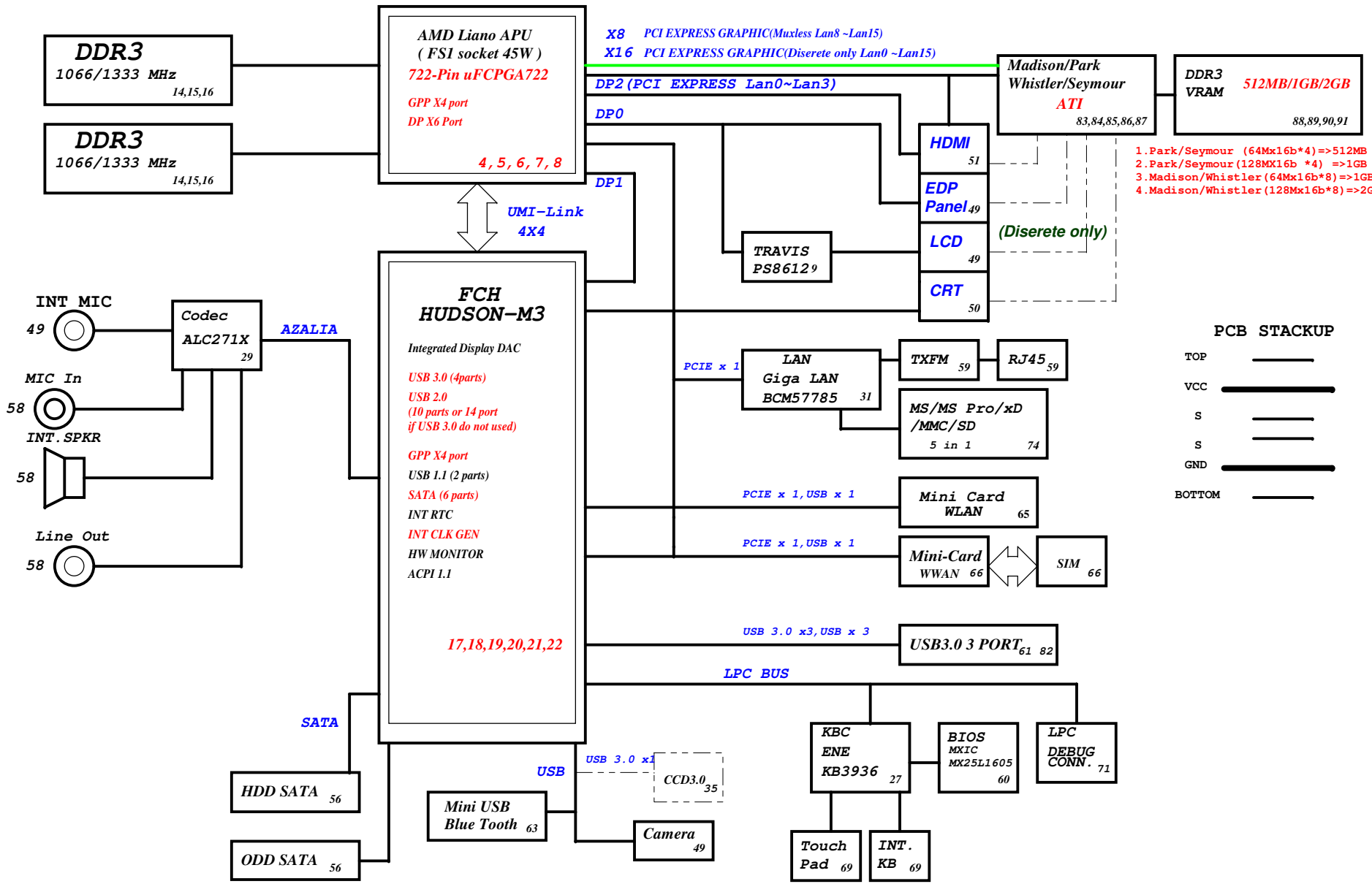
<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover Page			
Size	Document Number		Rev
A4	JE50 SB		SB
Date:	Friday, April 01, 2011	Sheet 1 of	102

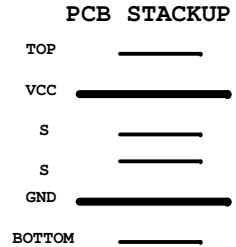
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JE50-SB Block Diagram

JE50-SB Project code:91.4M701.001



1. Park/Seymour (64Mx16b*4)=>512MB
2. Park/Seymour (128MX16b *4) =>1GB
3. Madison/Whistler (64Mx16b*8)=>1GB
4. Madison/Whistler (128Mx16b*8)=>2GB



SYSTEM DC/DC	
RT8239 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (5.5A) 3D3V_S5 (5A)
SYSTEM DC/DC	
RT8207 44	
5V_S5	1D5V_S3 (15A)
RT8207 44	
5V_S5	0D75_S0 (1.2A)
SYSTEM DC/DC	
RT8238 46	
INPUTS	OUTPUTS
5V_S5	1D1V_S5 (1.4A)
RT8238 45	
5V_S5	1D2V_S0 (5.2A)
RT9025 93	
3D3V_S5	1D8V_VGA_S0
1D5V_S3	1V_VGA_S0
RT9025 48	
3D3V_S0	2D5V_S0 (200mA)
RT8208 92	
5V_S5	VGA_CORE
CHARGER	
BQ24745 40	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA
CPU DC/DC	
ISL6267 42,43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.55V 18A VDDNB 0~1.55V 4A

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Title: **Block Diagram**

Size A3 Document Number: **JE50 SB** Rev: **SB**

Date: Friday, April 01, 2011 Sheet 2 of 102

Strapping

REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2_PCH_GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USB Table

USB	
Pair	Device
0	USB 2.0 EXT2 (For SW Debug)
1	WLAN
2	NC
3	WWAN
4	BT
5	3G SIM Card
6	NC
7	CCD
8	NC
9	Card Reader
10	USB 3.0 port 1
11	USB 2.0 EXT2
12	USB 2.0 EXT3
13	NC

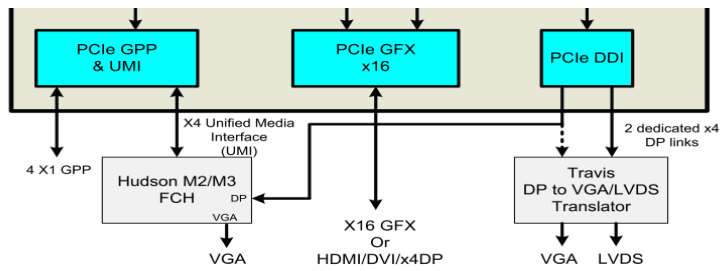
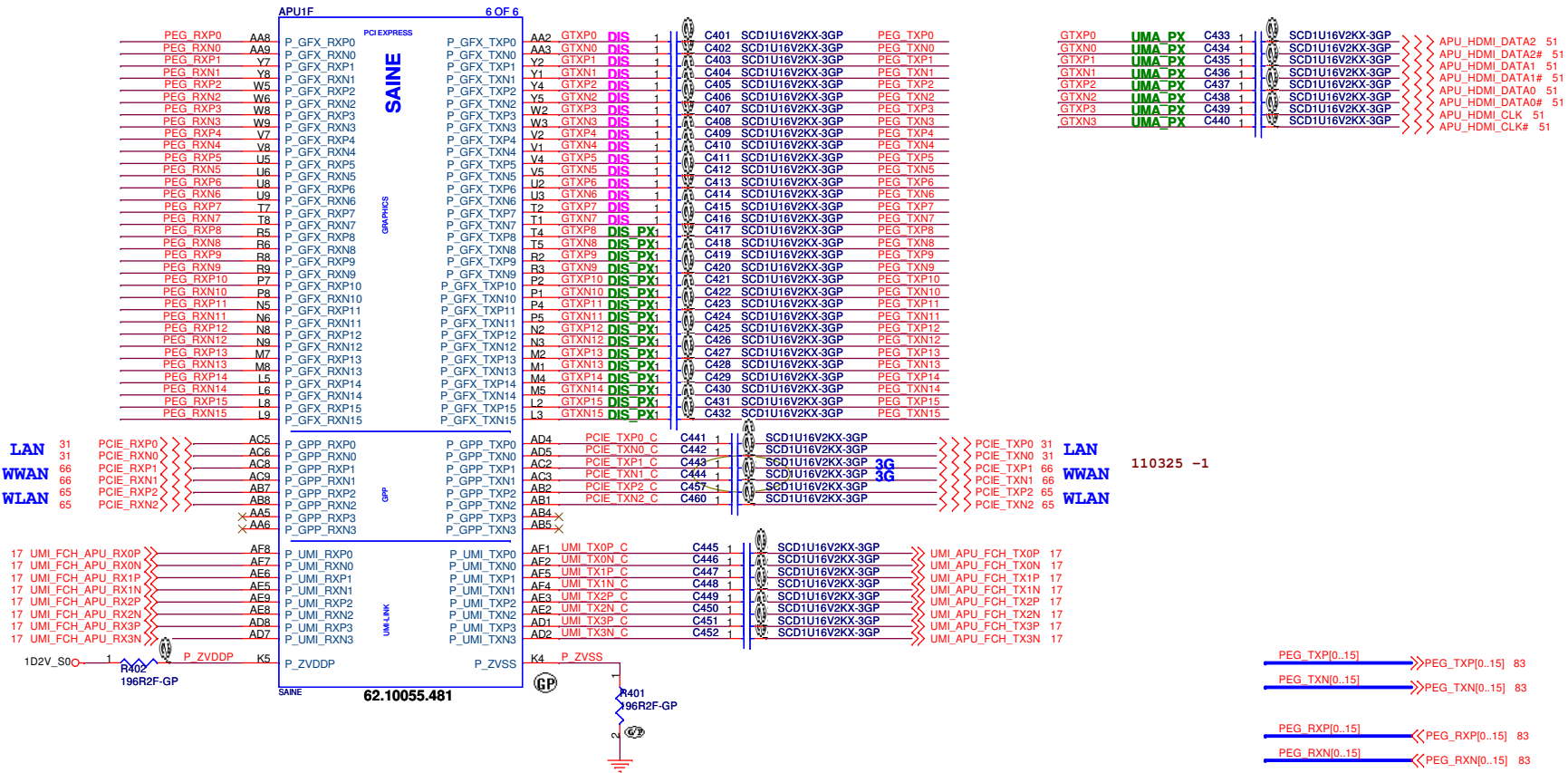
PCIE Routing

APU	
LANE0	LAN
LANE1	WWAN
LANE2	LAN
LANE3	

FCH	
LANE0	
LANE1	
LANE2	
LANE3	

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Title			
Table of Content			
Size A3	Document Number JE50 SB	Rev SB	
Date: Friday, April 01, 2011	Sheet 3	of 102	



PEG_TXP[0..15] >>> PEG_TXP[0..15] 83
 PEG_TXN[0..15] >>> PEG_TXN[0..15] 83
 PEG_RXP[0..15] <<< PEG_RXP[0..15] 83
 PEG_RXN[0..15] <<< PEG_RXN[0..15] 83

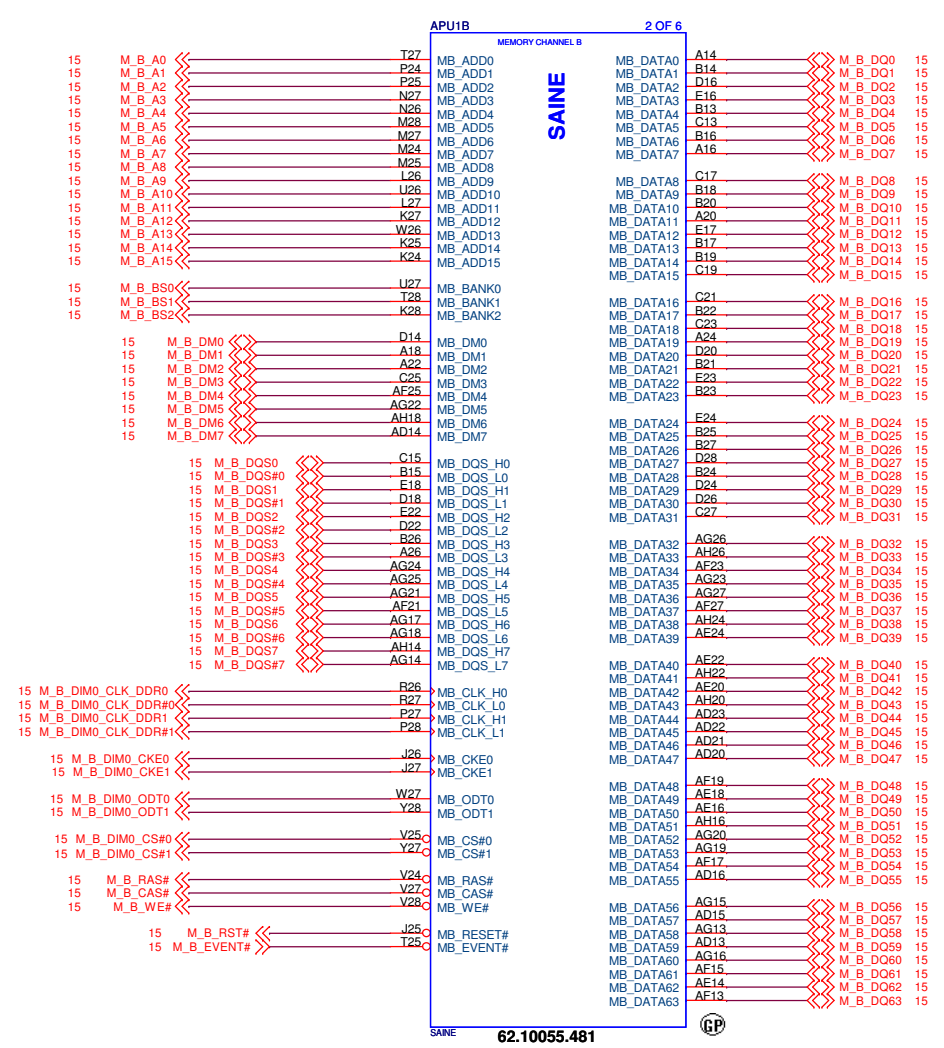
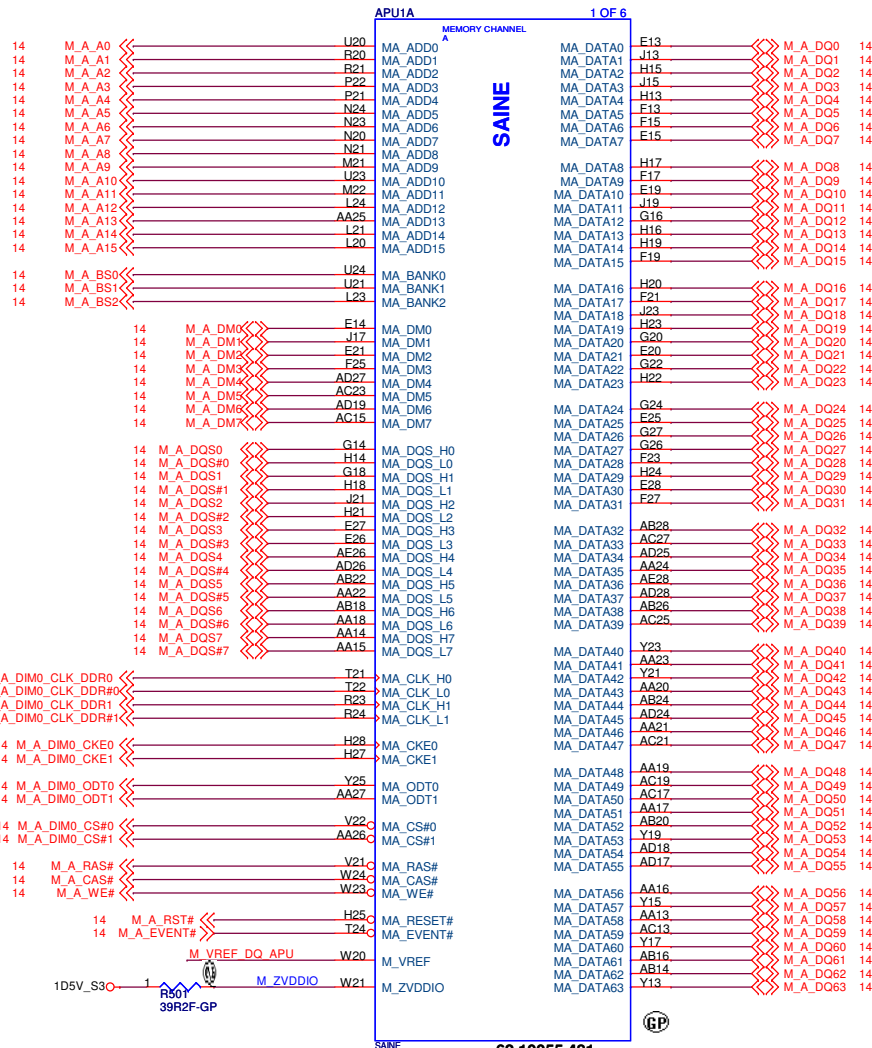
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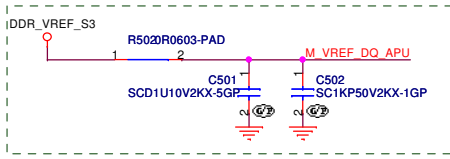
Title: **APU PCIE(1/5)**

Size A3 Document Number **JE50 SB** Rev **SB**

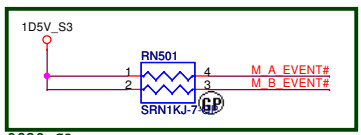
Date: Friday, April 01, 2011 Sheet 4 of 102



APU_VREF_DQ



LAYOUT: place them close to APU



0920-SA

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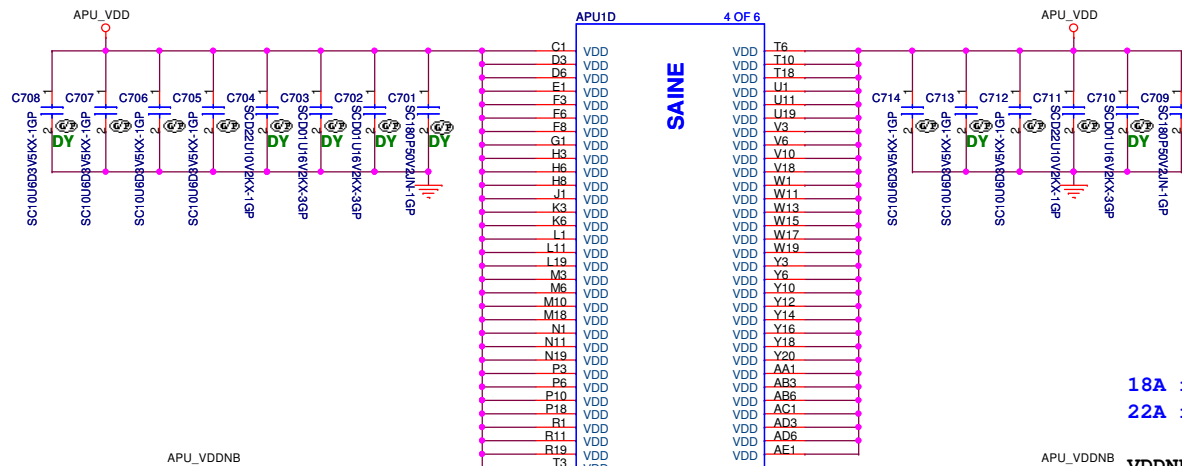
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **APU DDR(2/5)**

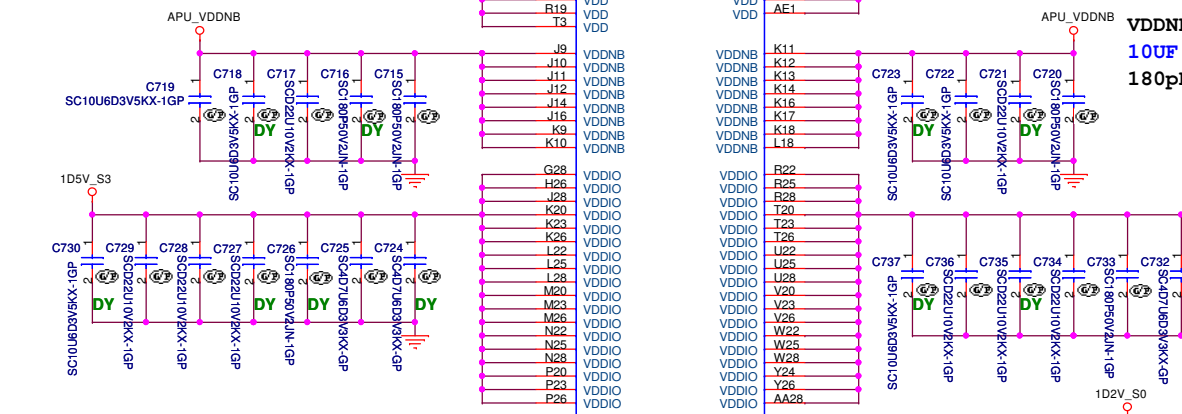
Size A3 Document Number **JE50 SB** Rev **SB**

Date: Friday, April 01, 2011 Sheet 5 of 102



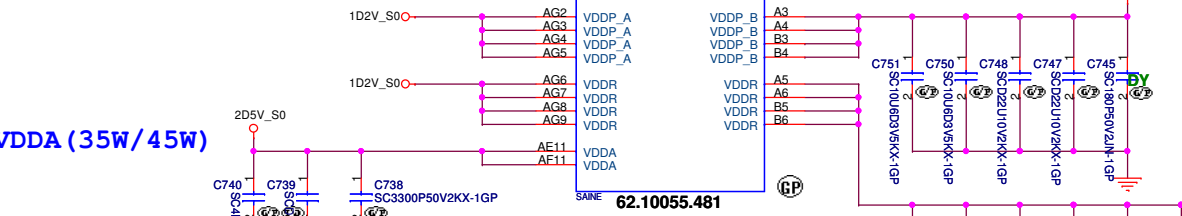
36A for VDD (35W CPU)
45A for VDD (45W CPU)

VDD:
10UF X7 0.22UF X2 10nF X3
180pF Cap for EMI requirement



18A for VDDNB (35W CPU)
22A for VDDNB (45W CPU)

VDDNB:
10UF X4 0.22UF X2
180pF Cap for EMI requirement



4A for VDDIO (35W CPU)
4.6A for VDDIO (45W CPU)

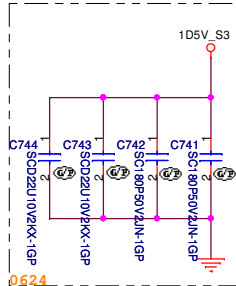
VDDIO:
10UF X2 0.22UF X6 4.7uFUF X4
180pF Cap for EMI requirement
3.5A for VDDP (35W/45W)



VDDP:
10UF X2 0.22uF X2
180pF Cap for EMI requirement

3A for VDDR (35W)
3.5A for VDDR (45W)

0.75A for VDDA (35W/45W)



Decoupling between processor and DIMMs across VDDIO and VSS Split

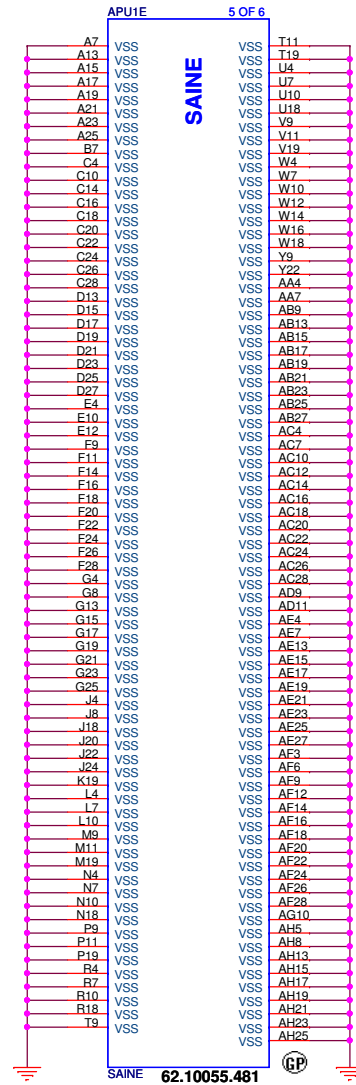
VDDR:
4.7UF X2 0.22uF X2
180pF Cap for EMI requirement

<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

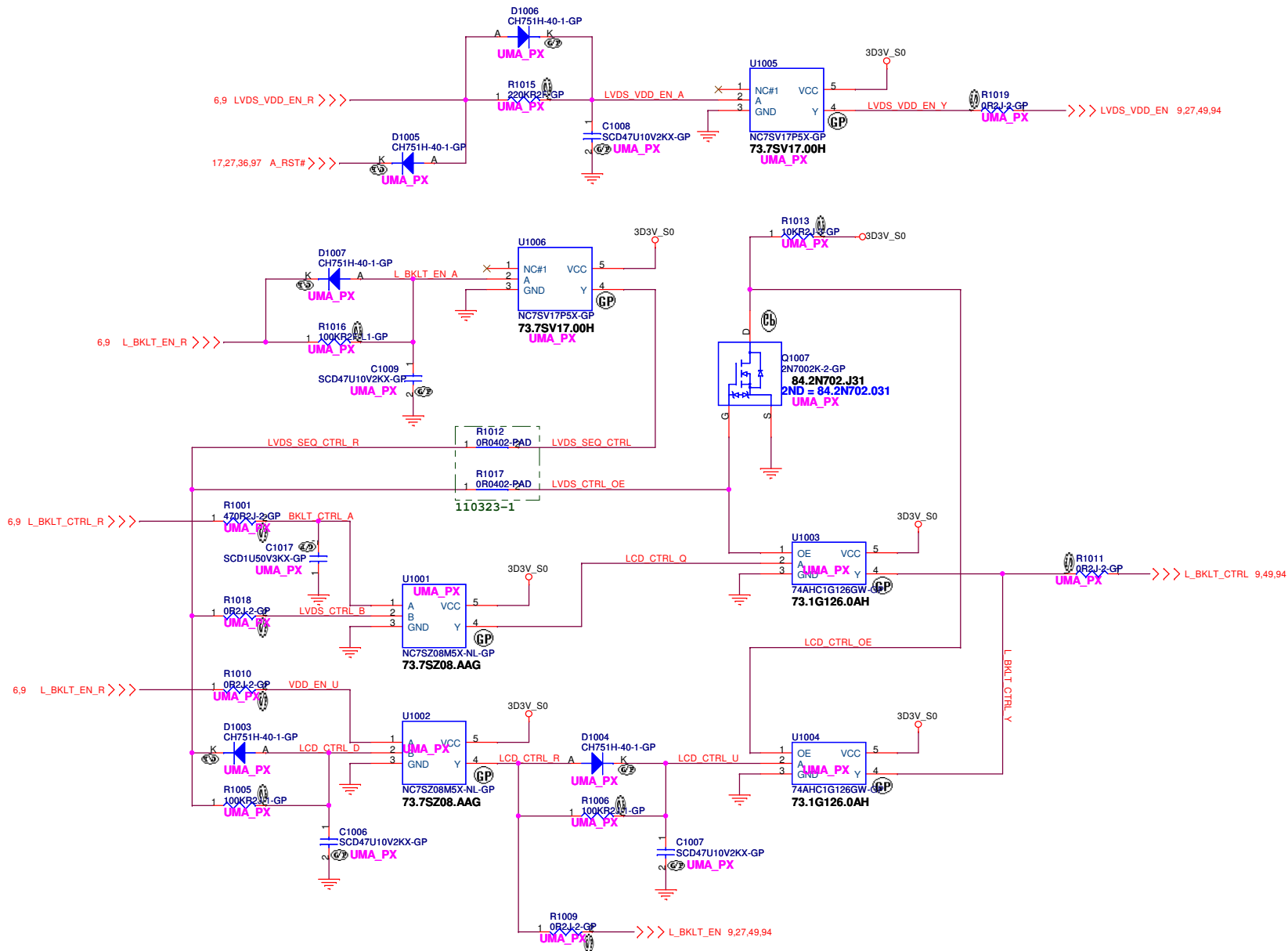
Title APU Power(4/5)		
Size A3	Document Number JE50 SB	Rev SB
Date: Friday, April 01, 2011	Sheet 7 of 102	





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APU VSS(5/5)		
Size A3	Document Number JE50 SB	Rev SB
Date: Friday, April 01, 2011	Sheet 8 of	102



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Title		
Reserved		
Size A3	Document Number	Rev
	JE50 SB	SB
Date: Friday, April 01, 2011	Sheet 10 of 102	

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Title **Reserved**

Size A4	Document Number JE50 SB	Rev SB
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Date: Friday, April 01, 2011 Sheet 11 of 102

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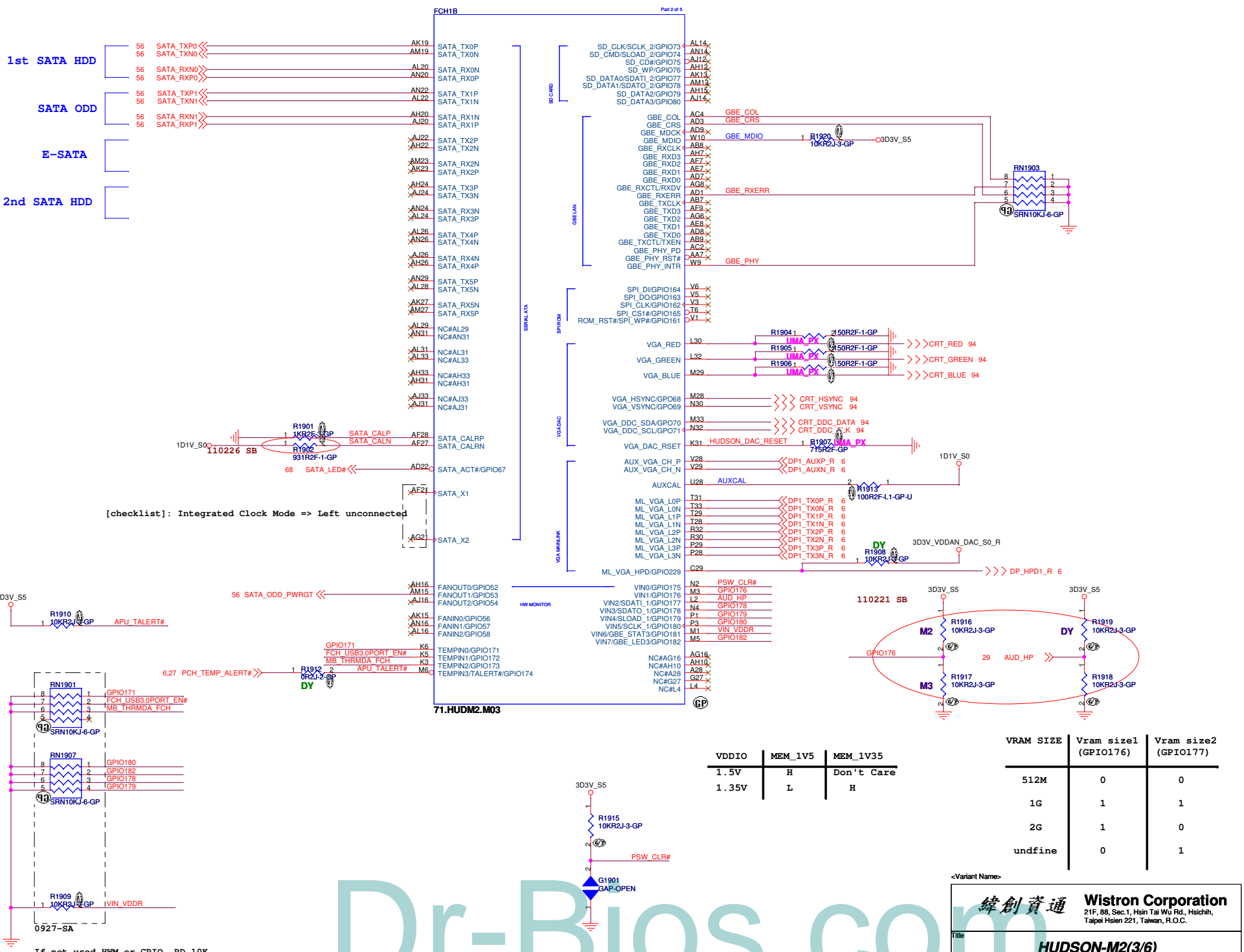
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Title **Reserved**

Size A4	Document Number JE50 SB	Rev SB
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Date: Friday, April 01, 2011 Sheet 16 of 102



[checklist]: Integrated Clock Mode => Left unconnected

VDDIO	MEM_1V5	MEM_1V35
1.5V	H	Don't Care
1.35V	L	H

VRAM SIZE	Vram size1 (GPIO176)	Vram size2 (GPIO177)
512M	0	0
1G	1	1
2G	1	0
undfine	0	1

If not used HWM or GPIO ,PD 10K

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<Variant Name>

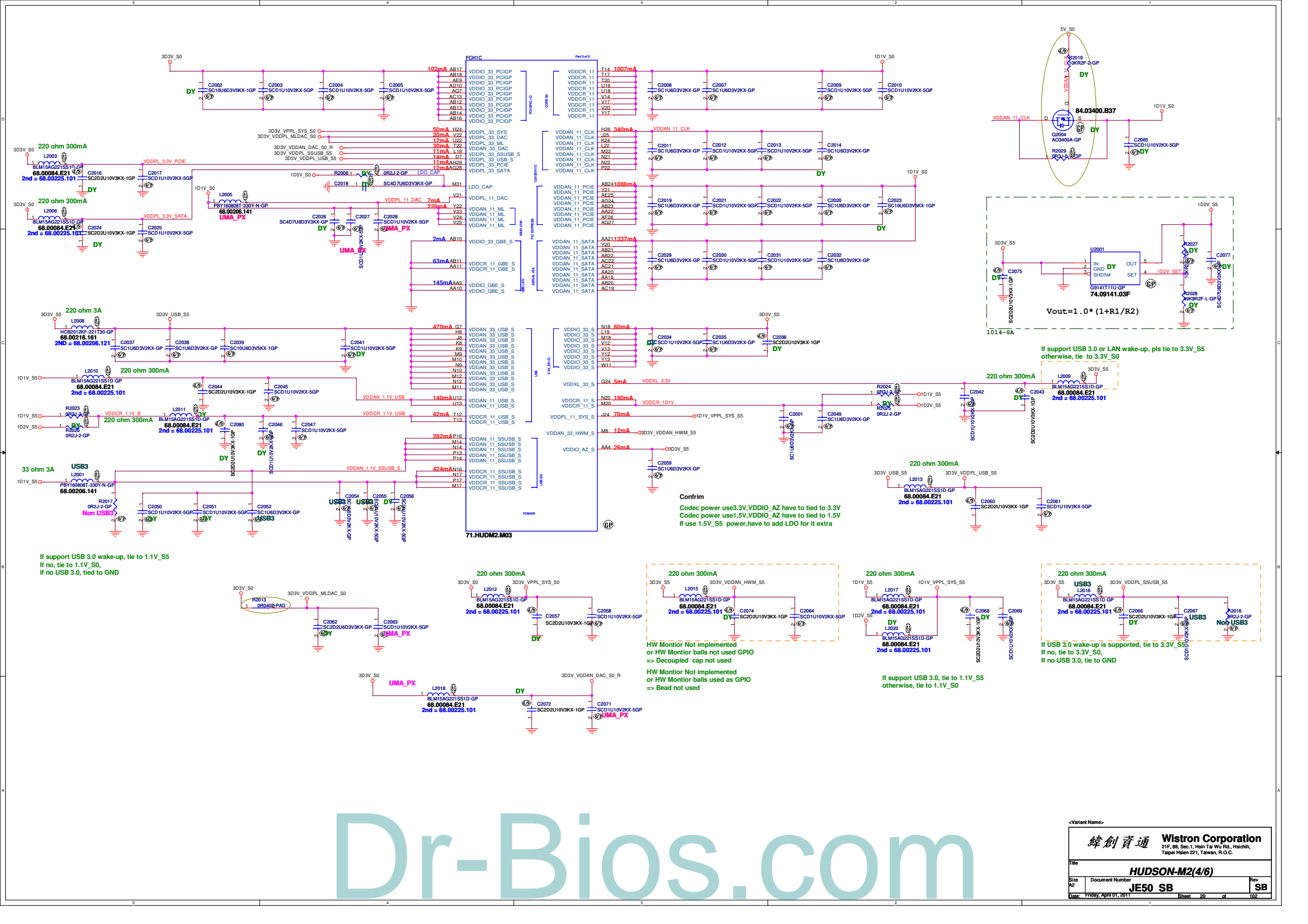
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Title: **HUDSON-M2(3/6)**

Size: JE50 SB

Customer: **JE50 SB**

Date: Friday, April 01, 2011 Sheet 19 of 102



If support USB 3.0 wake-up, tie to 1.1V_S5
 If no, tie to 1.1V_S0
 If no USB 3.0, tied to GND

Confrim
 Codec power use 3.3V, VDDIO_AZ have to tied to 3.3V
 Codec power use 1.5V, VDDIO_AZ have to tied to 1.5V
 If use 1.5V_S5 power, have to add LDO for it extra

If support USB 3.0 or LAN wake-up, pls tie to 3.3V_S5
 otherwise, tie to 3.3V_S0

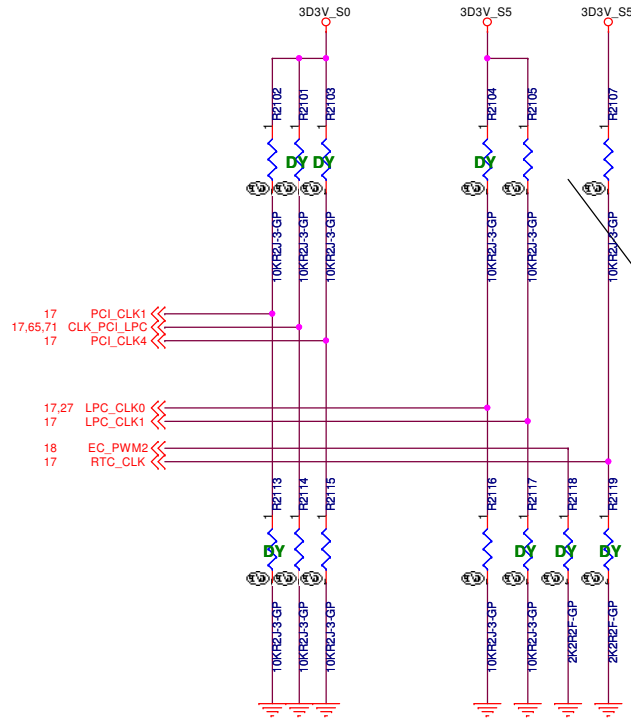
HW Monitor Not implemented
 or HW Monitor balls not used GPIO
 => Decoupled cap not used

If support USB 3.0, tie to 1.1V_S5
 otherwise, tie to 1.1V_S0

If USB 3.0 wake-up is supported, tie to 3.3V_S5
 If no, tie to 3.3V_S0
 If no USB 3.0, tie to GND

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REQUIRED STRAPS



CRB:PU 3.3V_AUX_S5
 checklist:PU 3.3V_S5
 no support S5 PLUS function,PU 3.3V_S5

LPC ROM implemented
 checklist suggestion:
 no PU or PD required
 (integrated PU 10K)
 CRB: do not stuff PU Res

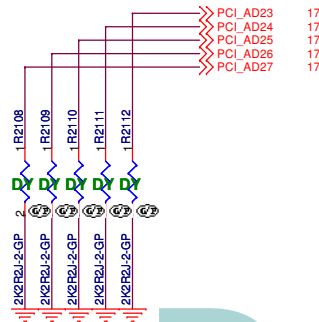
REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

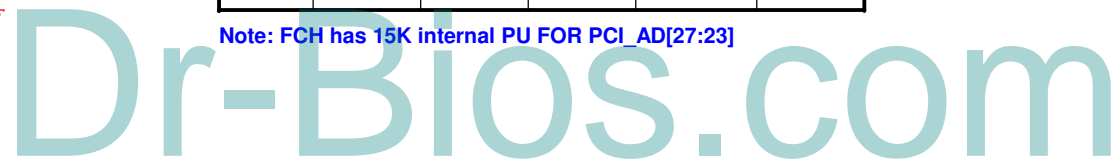
Ball Name	Strap Function	Description
EC_PWM2	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]



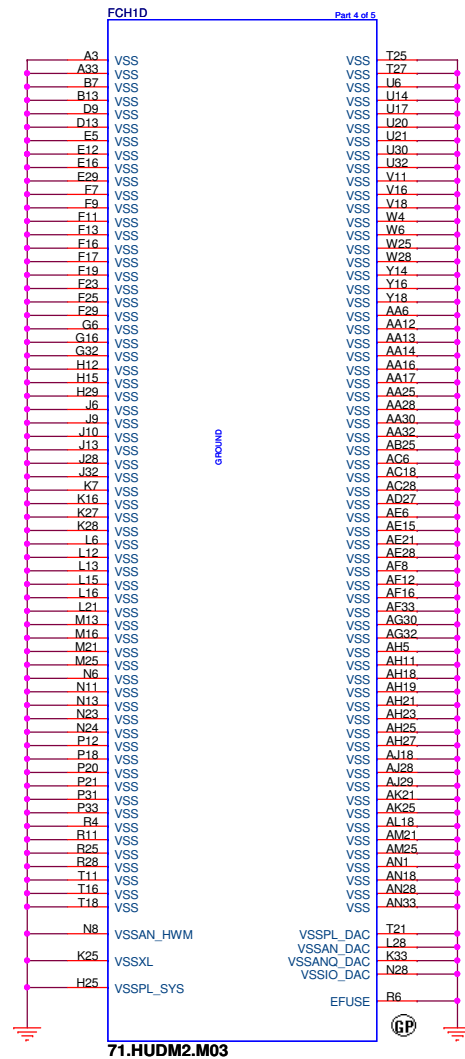
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Title: **HUDSON-M2(5/6)**

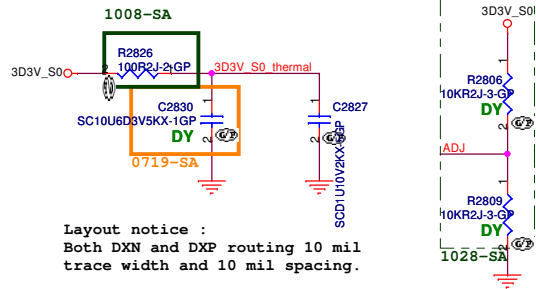
Size A3 Document Number: **JE50 SB** Rev: **SB**

Date: Friday, April 01, 2011 Sheet 21 of 102



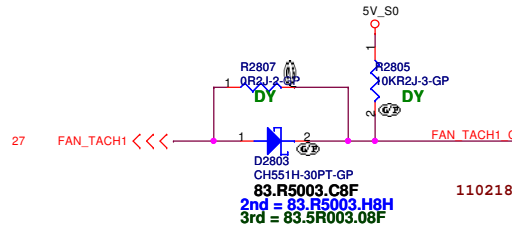
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Size	Document Number
A3	JE50 SB
Date:	Rev
Friday, April 01, 2011	SB
Sheet	of
22	102

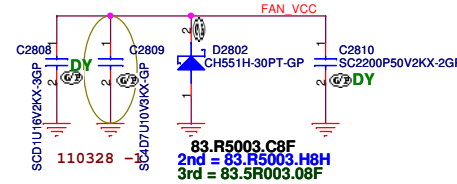


Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

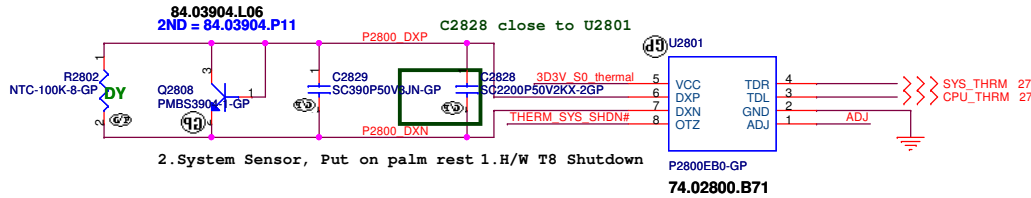
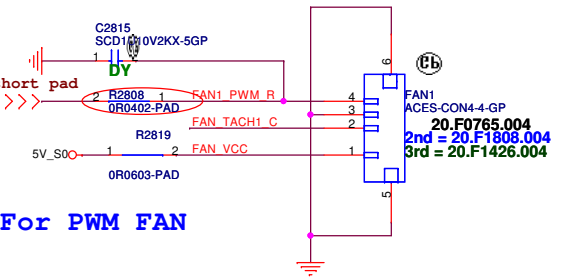
ADJ IN
Over temperature threshold setting by external resistor divider
Floating= 85oC; GND=90oC; VCC=95oC



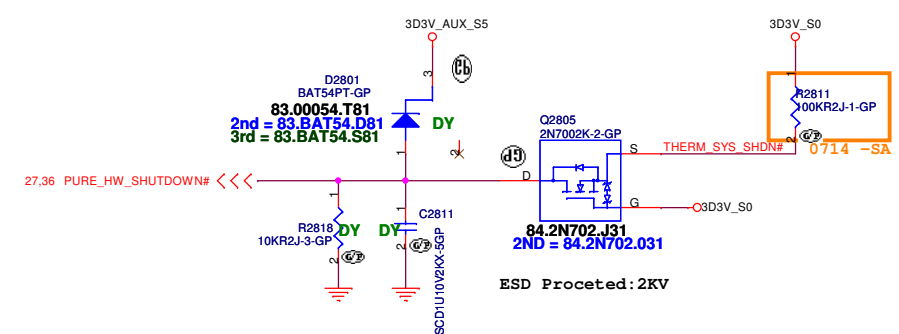
Layout 15 mil



For PWM FAN

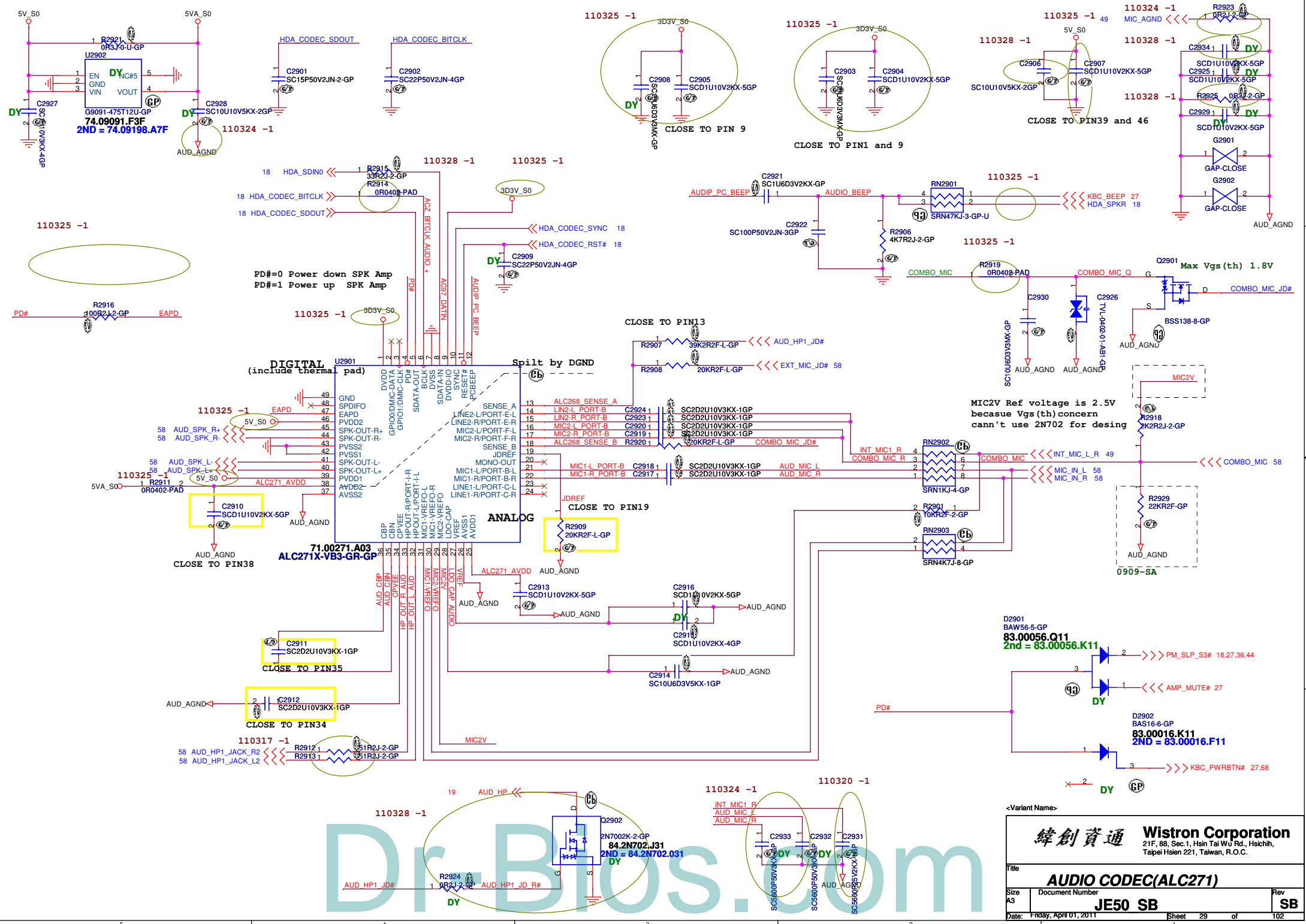


VGA Thermal sensor P2800



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Thermal P2800	
Size A3	Document Number
Date: Friday, April 01, 2011	JE50 SB
Sheet 28	Rev SB
of 102	

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PD#=0 Power down SPK Amp
 PD#=1 Power up SPK Amp

DIGITAL
 (include thermal pad)

ANALOG

71.00271.A03
 ALC271X-VB3-GR-GP

MIC2V Ref voltage is 2.5V
 because Vgs(th) concern
 can't use 2N702 for desing

D2901
 BAW56-5-GP
 83.00056.Q11
 2nd = 83.00056.K11

D2902
 BAS16-6-GP
 83.00016.K11
 2ND = 83.00016.F11

Q2902
 2N7002K-2-GP
 84.2N702.J31
 2ND = 84.2N702.031

<Variant Name>

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Title	AUDIO CODEC(ALC271)	
Size A3	Document Number	Rev
	JE50 SB	SB
Date: Friday, April 01, 2011	Sheet 29	of 102

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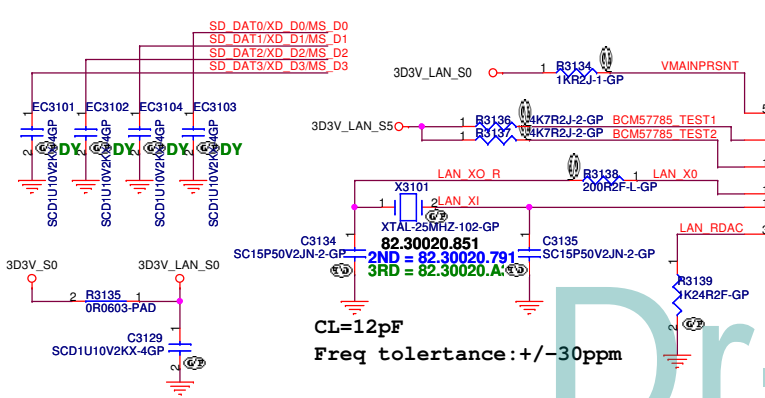
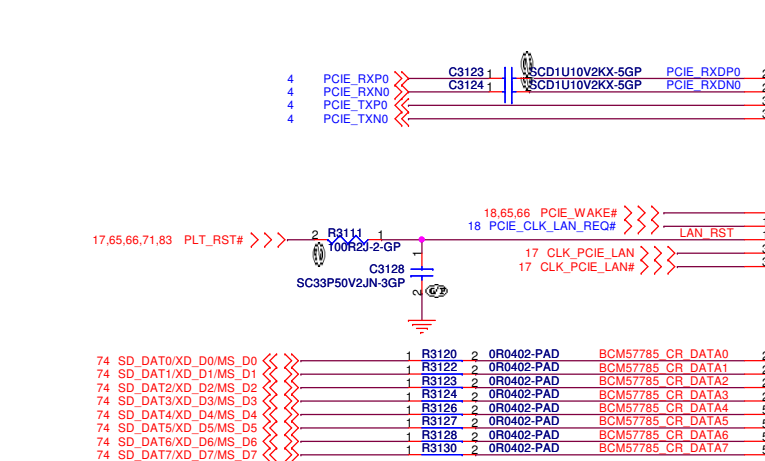
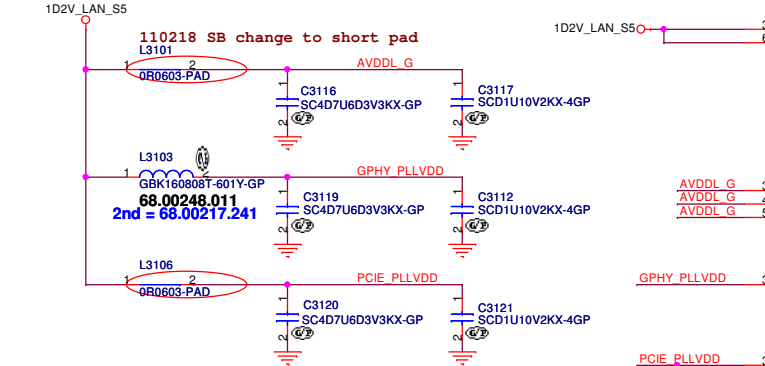
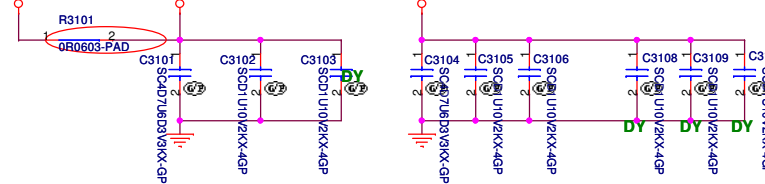
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Title **AMP**

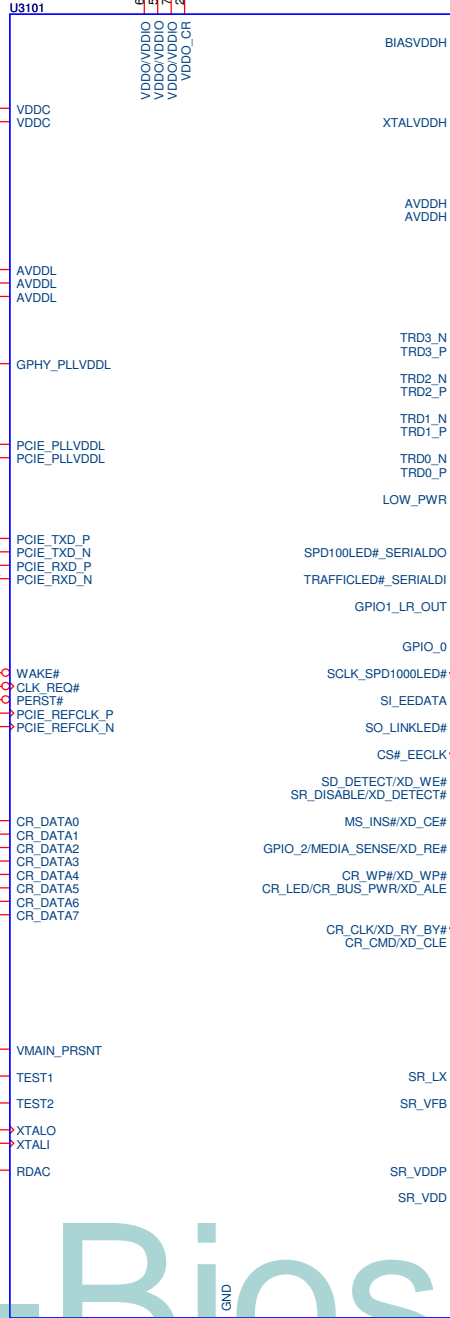
Size A4	Document Number JE50 SB	Rev SB
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Date: Friday, April 01, 2011 Sheet 30 of 102

110218 SB change to short pad

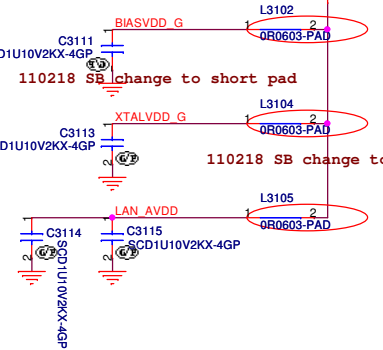


CL=12pF
Freq tolerance: +/-30ppm

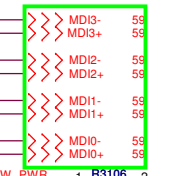


BCM57785XA0KMLG-GP
JE40-HR SB change to B version
P/N: 71.57785.M03

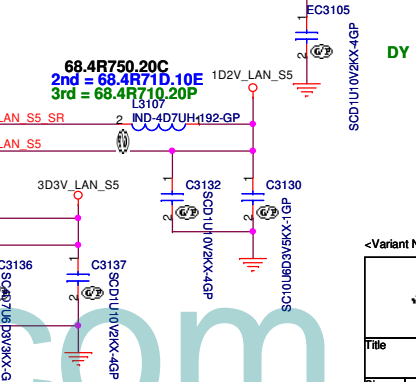
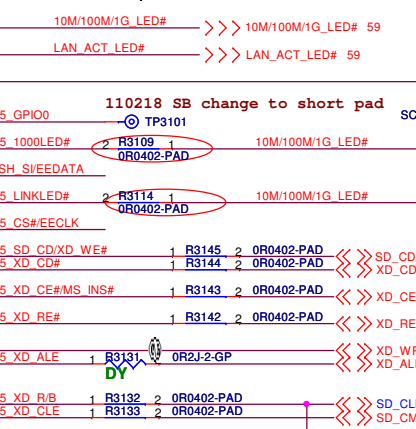
110218 SB change to short pad



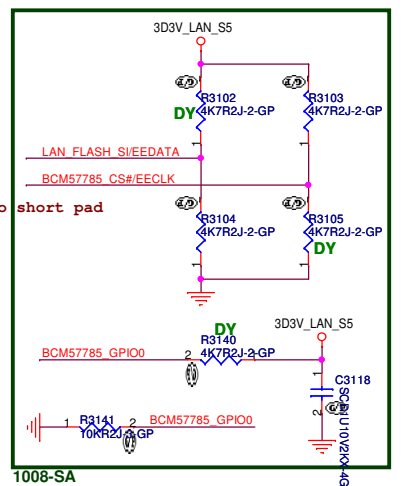
LAN MDI Off-Page



LOW_PWR 1 R3106 2 0R2J-2-GP

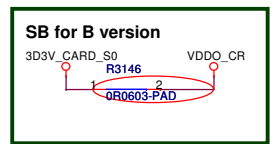


68.4R750.20C
2nd = 68.4R71D.10E
3rd = 68.4R71D.20P

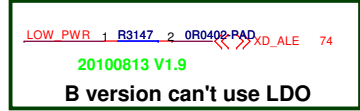


1008-SA

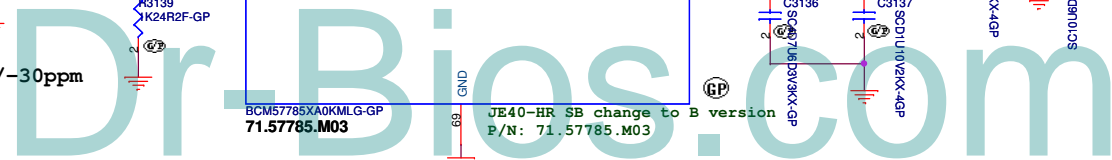
110218 SB change to short pad



0914-SA



20100813 V1.9
B version can't use LDO



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File: **LOM**

Size A3 Document Number: **JE50 SB** Rev: **SB**

Date: Friday, April 01, 2011 Sheet 31 of 102

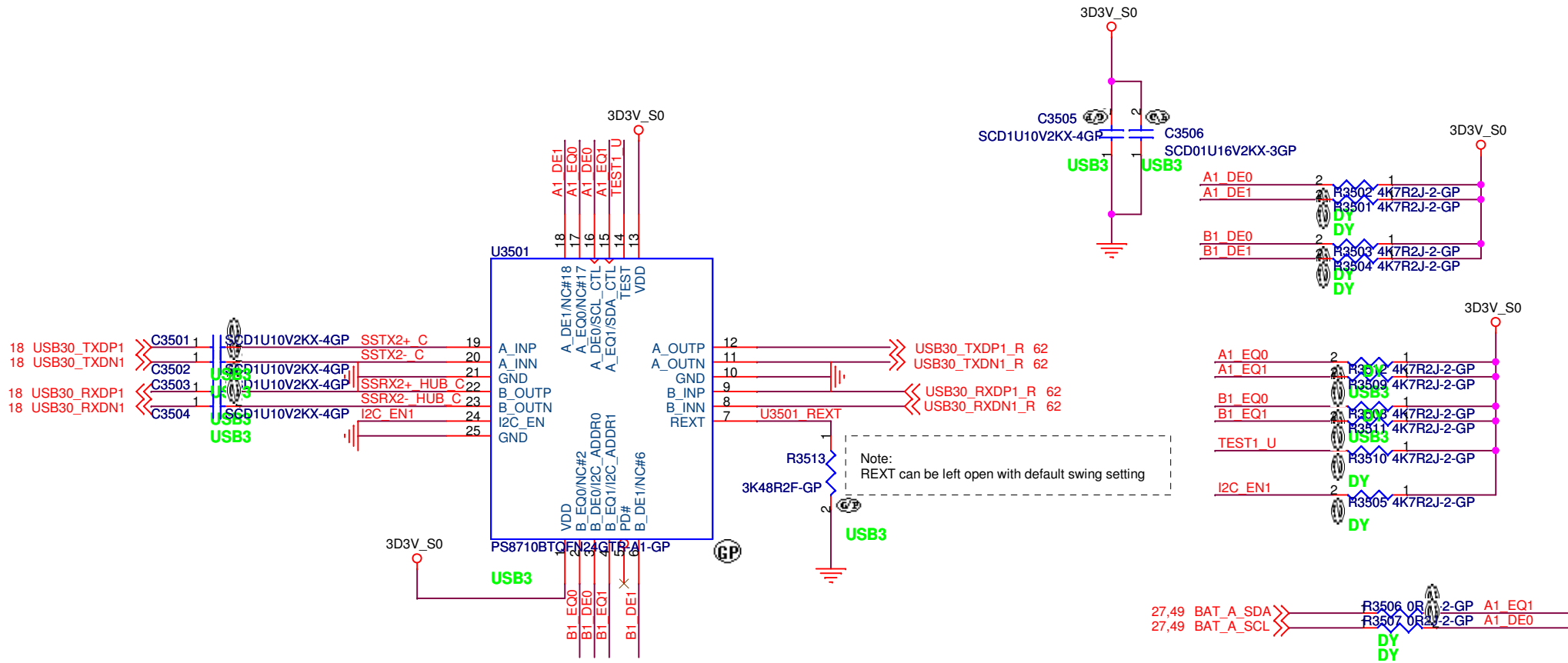
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Title	RTS5138
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Size	Document Number	Rev
A4	JE50 SB	SB

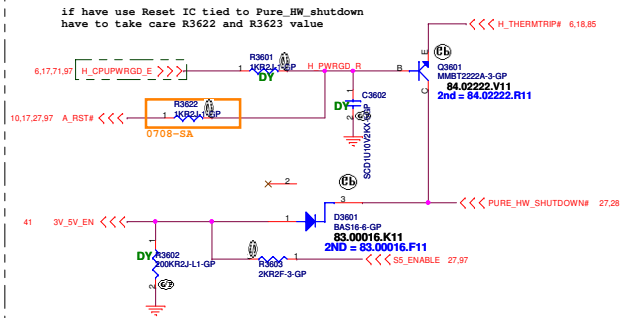
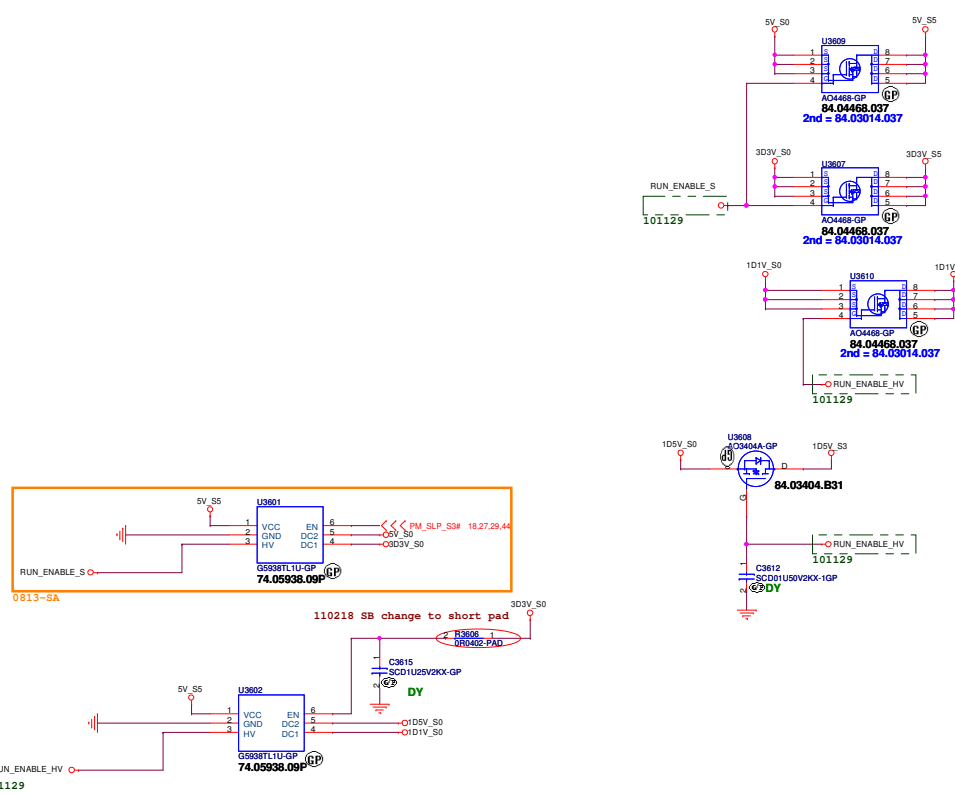


<Variant Name>

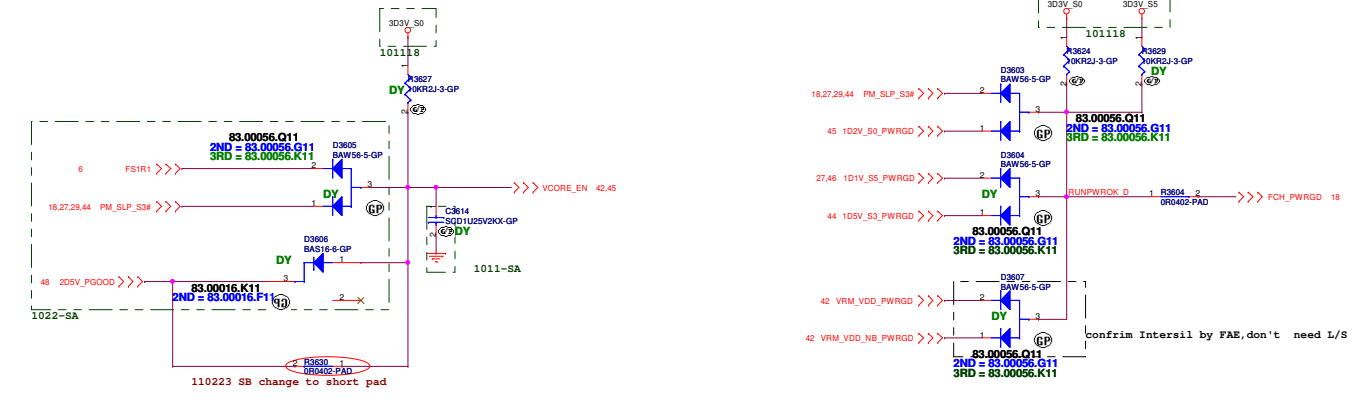
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		Reserved	
Size	Document Number	Rev	
A4	JE50 SB	SB	
Date:	Friday, April 01, 2011	Sheet	35 of 102

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Power Sequence



(Blanking)

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<Variant Name>

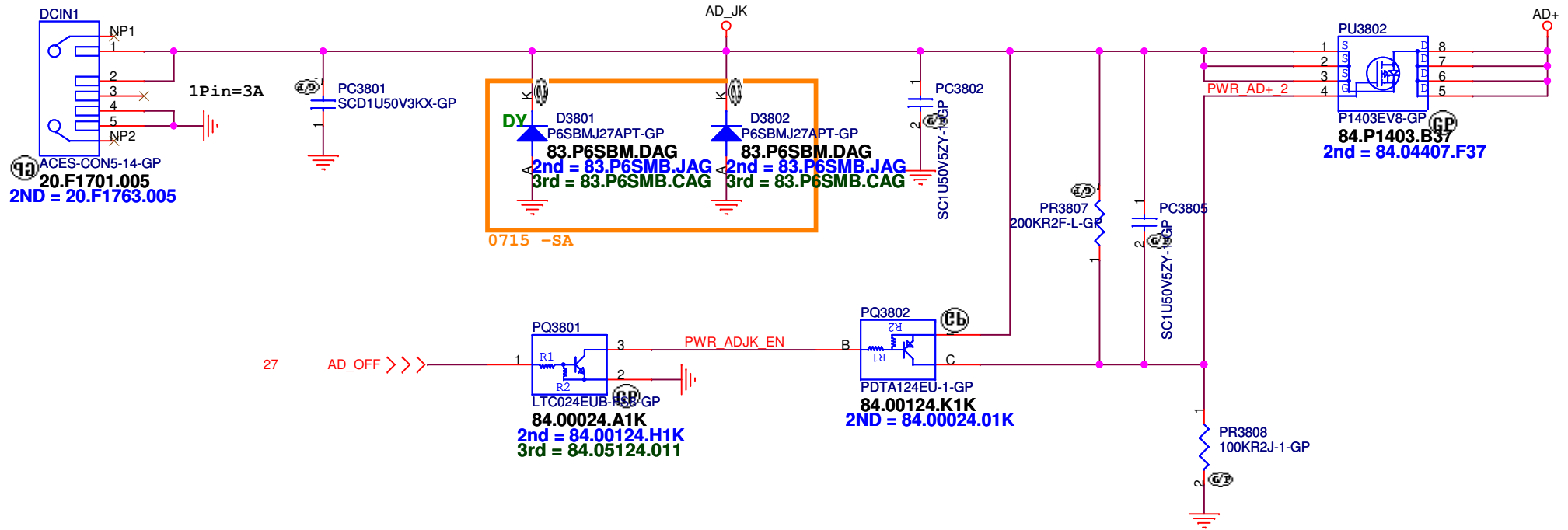
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4	Document Number JE50 SB	Rev SB
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Date: Friday, April 01, 2011 Sheet 37 of 102

Adaptor in to generate DCBATOUT



<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DCIN JACK

Size

A4

Document Number

JE50 SB

Rev

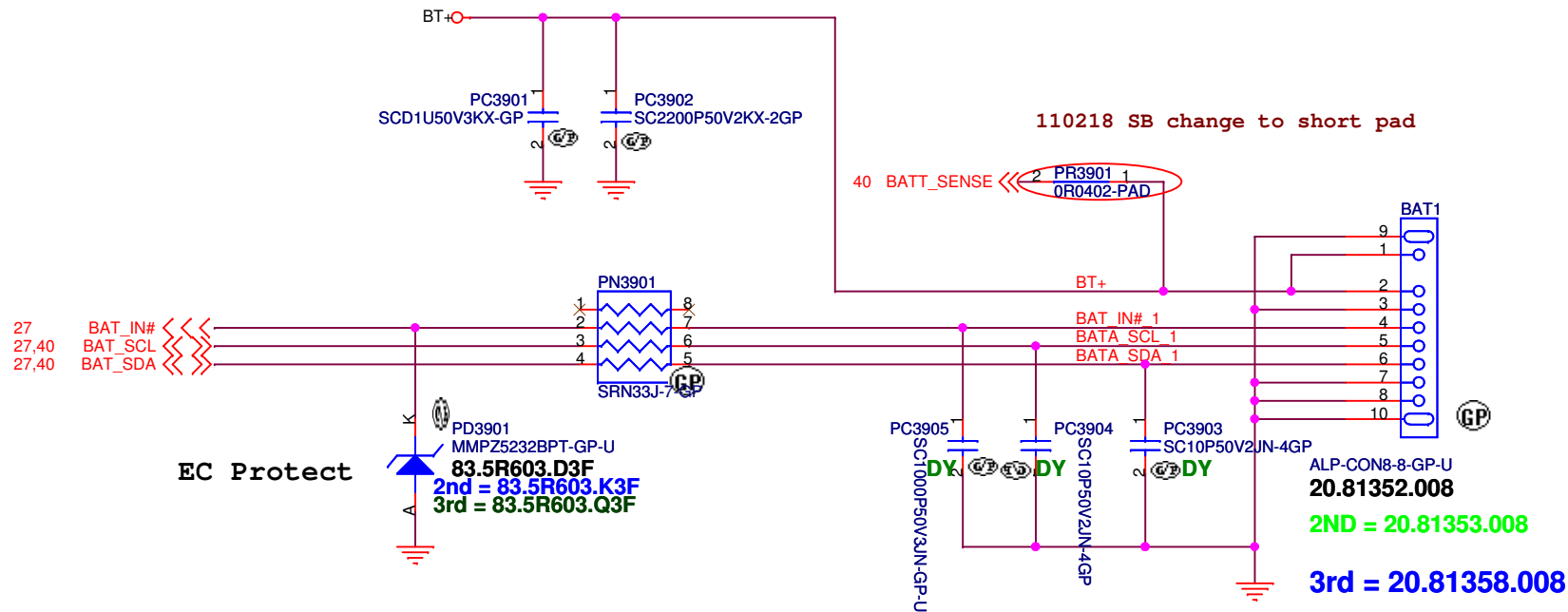
SB

Date: Friday, April 01, 2011

Sheet 38 of 102

Dr-Bios.com

BATTERY CONNECTOR



<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BATT_CONN

Size

A4

Document Number

JE50_SB

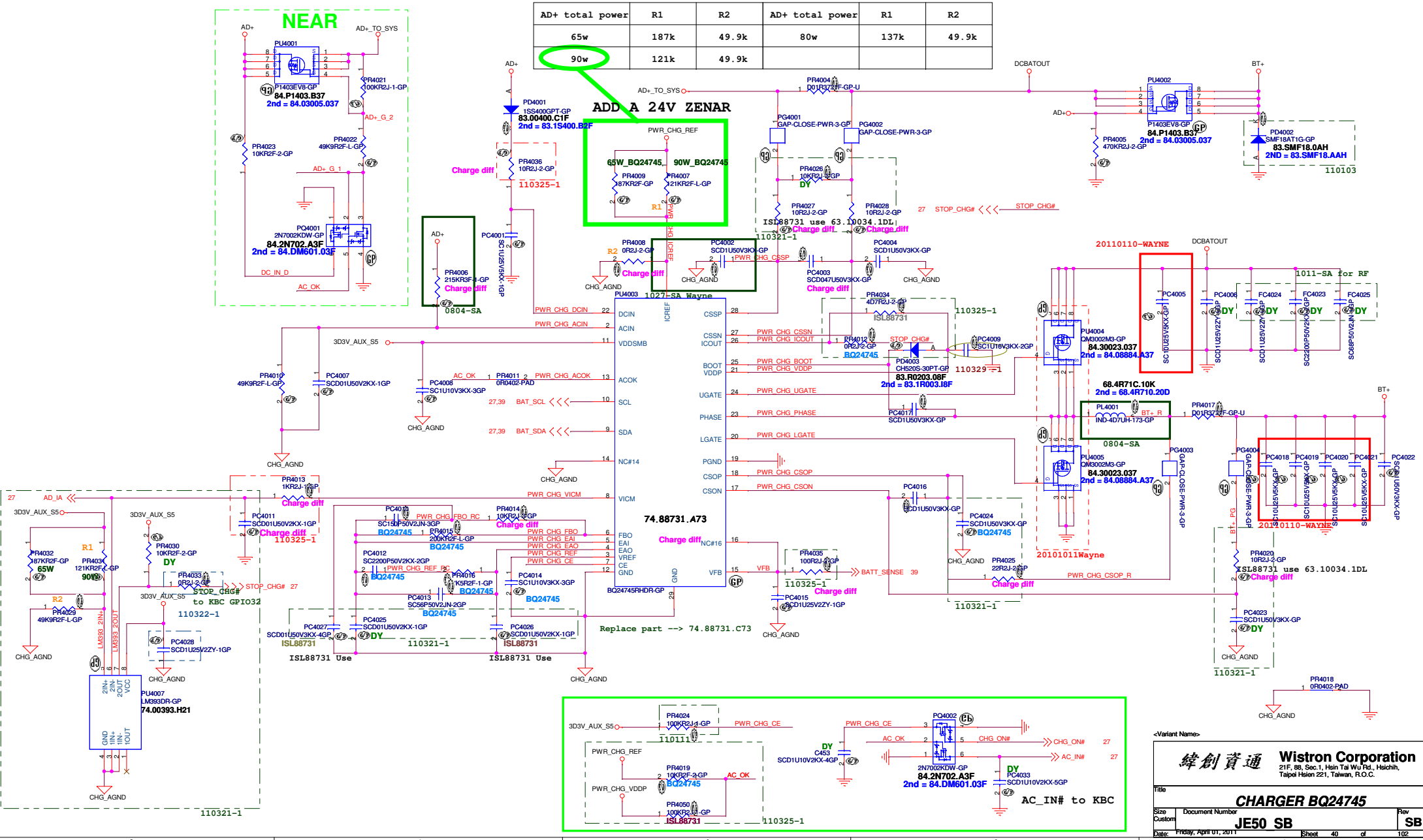
Rev

SB

Date: Friday, April 01, 2011

Sheet 39 of 102

Dr-Bios.com

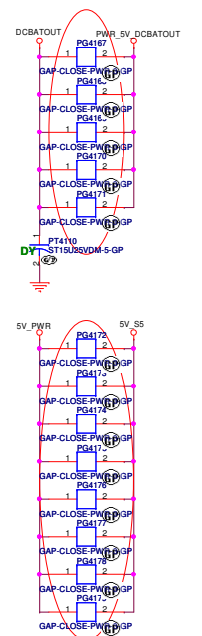
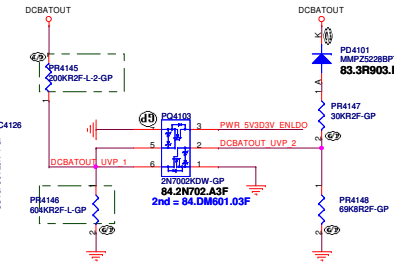
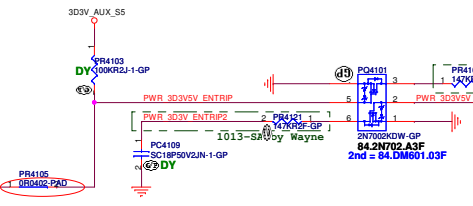
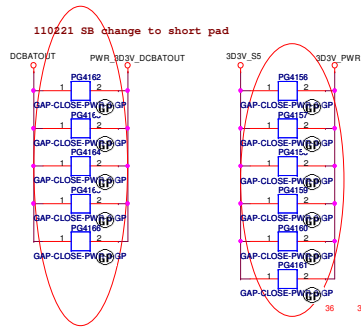


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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

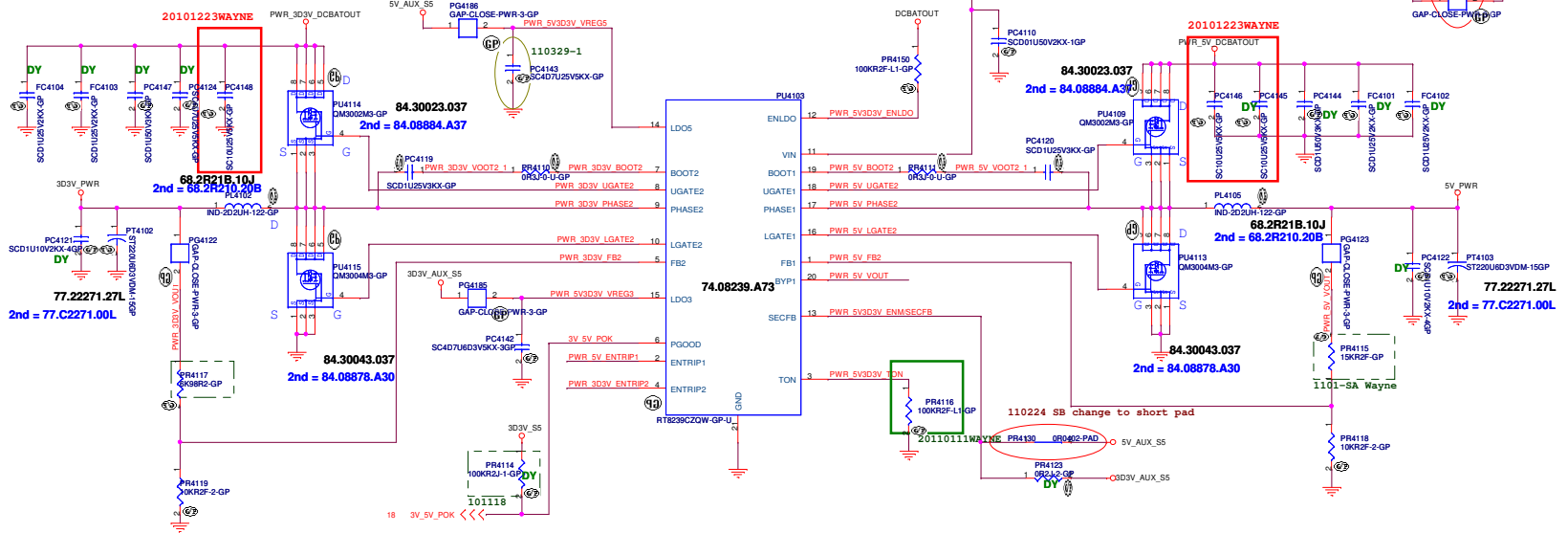
CHARGER BQ24745
 JE50 SB
 Rev SB

Date: Friday, April 01, 2011 Sheet 40 of 102



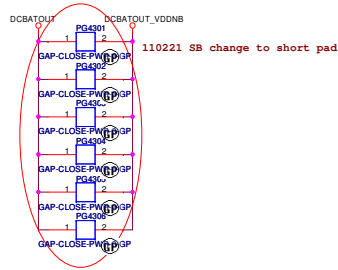
110221 SB change to short pad

Vz=3.9V
UVP Function
DCBATOUT<7.5V 3/5V disable

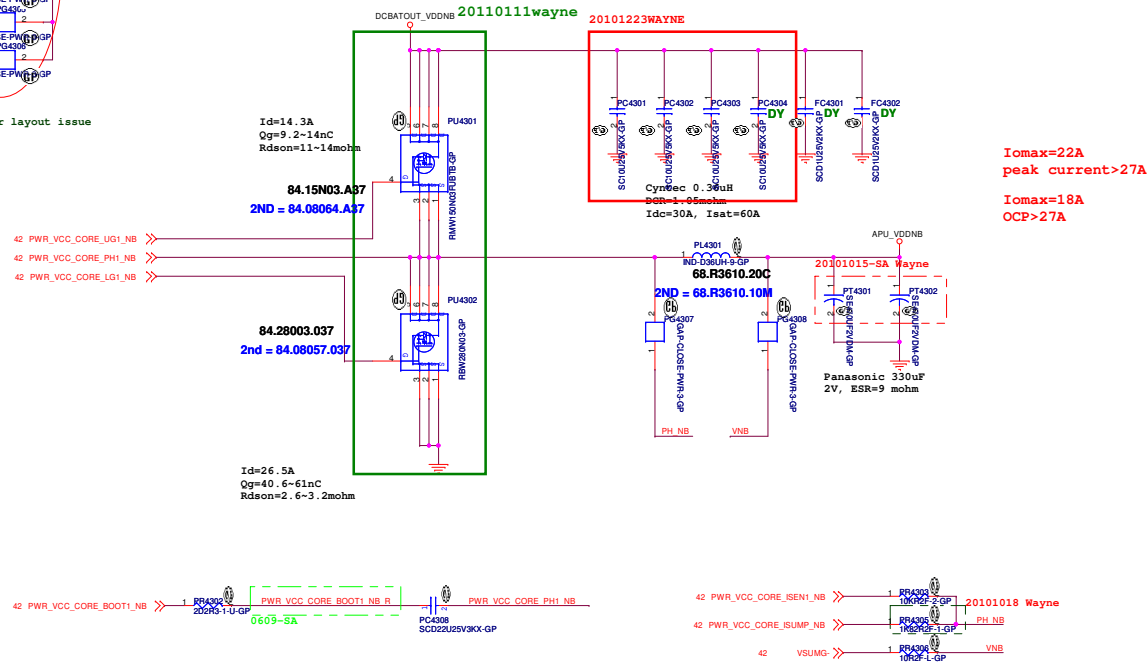


3V_V5_POK <<<

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0803-SA for layout issue

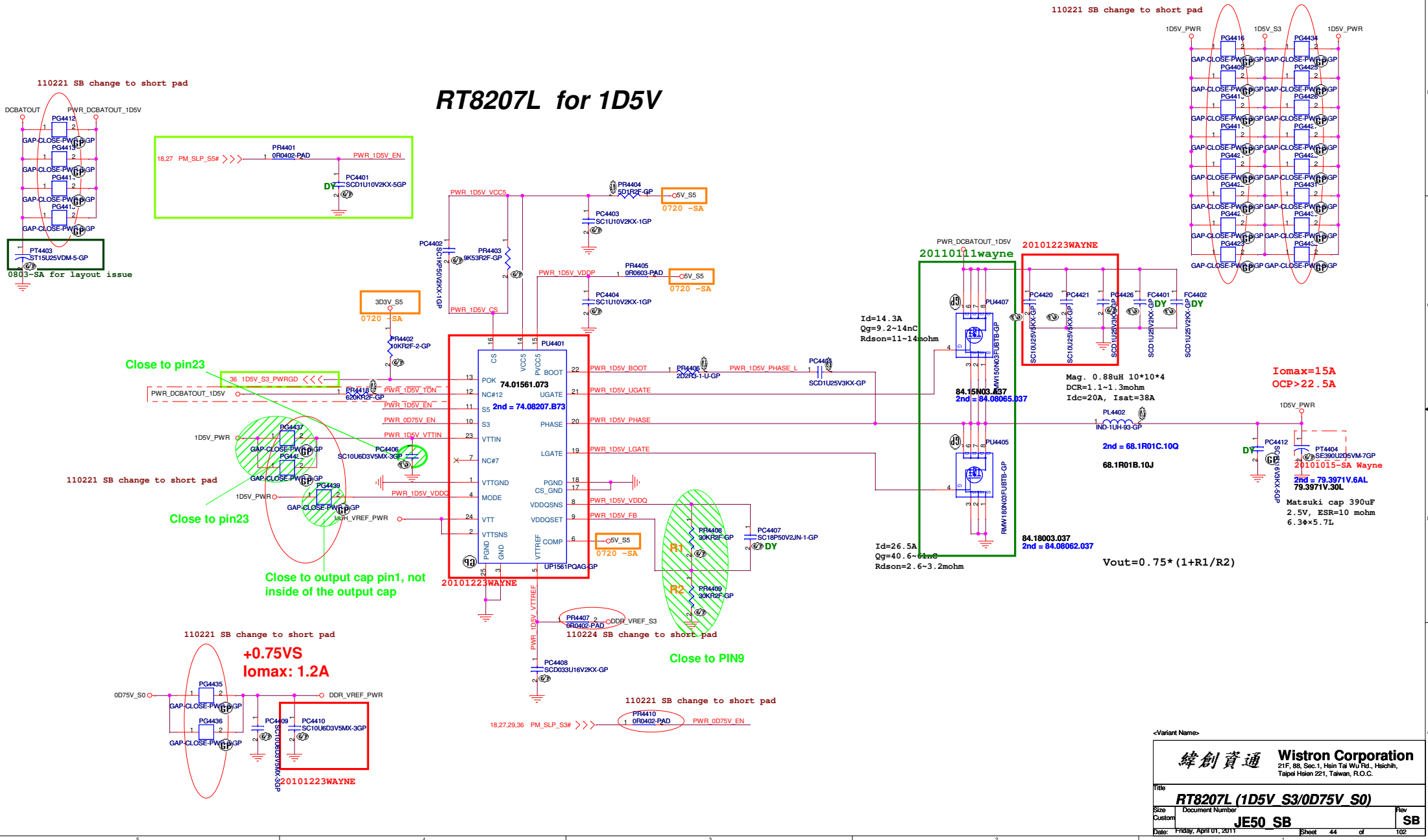


I_{omax}=22A
peak current>27A

I_{omax}=18A
OCP>27A

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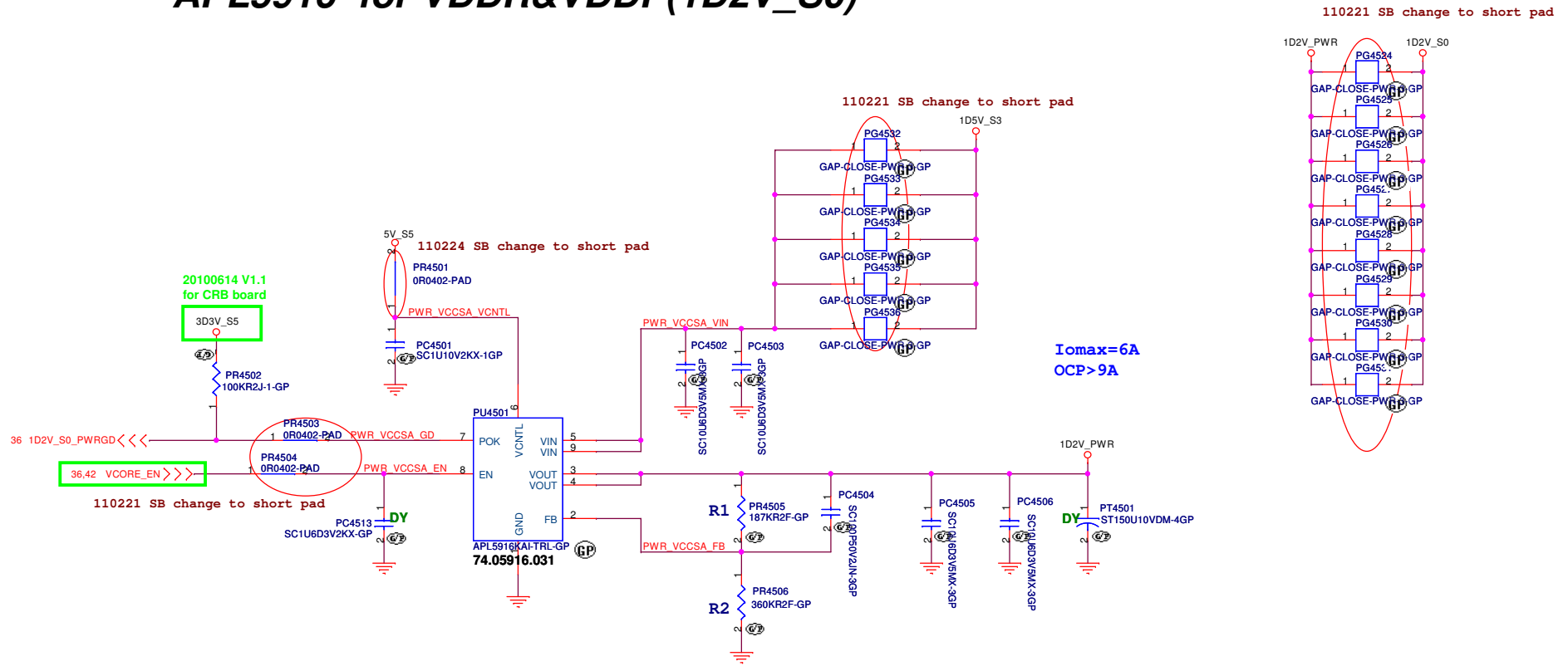
RT8207L for 1D5V



-Variant Name-

緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsieh, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT8207L (1D5V_S3/0D75V_S0)
Size	Document Number
Custom	JE50 SB
Date	Friday, April 01, 2011
Sheet	44 of 102

APL5916 for VDDR&VDDP(1D2V_S0)



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-Variant Name-		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
APL5916(1D2V_S0)		
Size	Document Number	Rev
A3	JE50 SB	SB
Date:	Friday, April 01, 2011	Sheet 45 of 102

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<Variant Name>

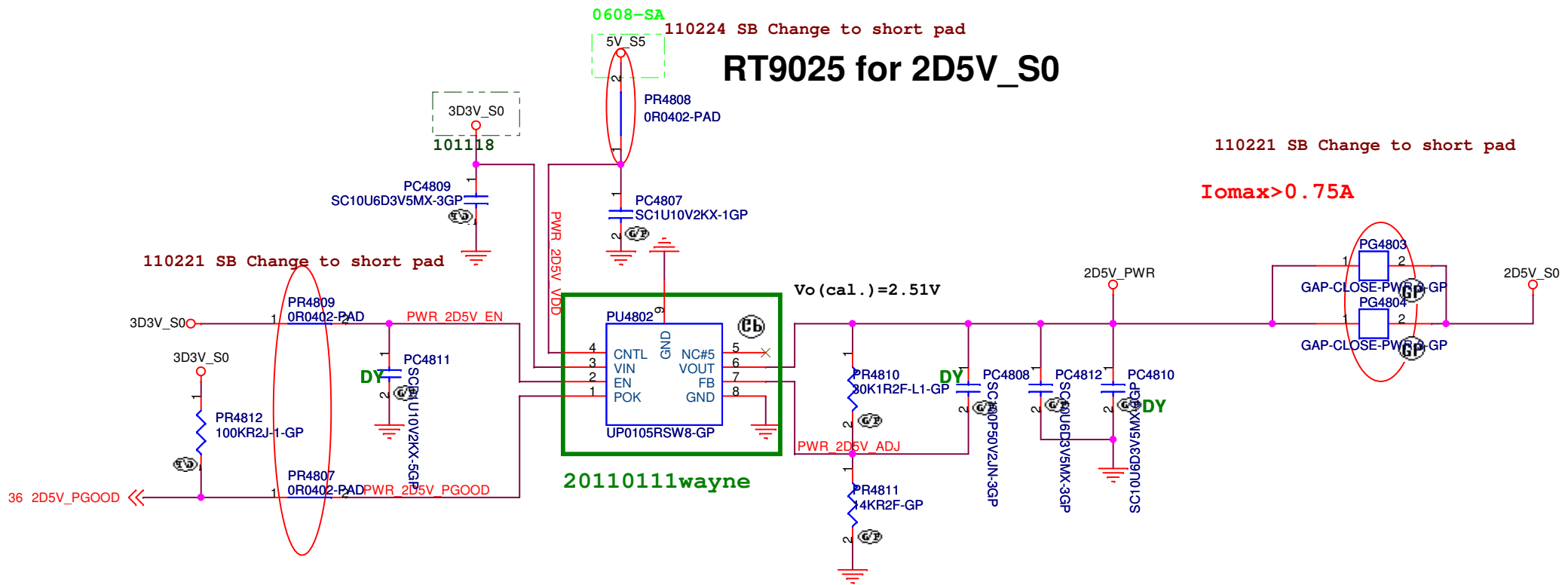
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4	Document Number JE50 SB	Rev SB
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Date: Friday, April 01, 2011 Sheet 47 of 102

RT9025 for 2D5V_S0



<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
RT9025(2D5V_S0)	
Size	Document Number
A4	JE50 SB
Date:	Rev
Friday, April 01, 2011	SB
Sheet 48 of 102	

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

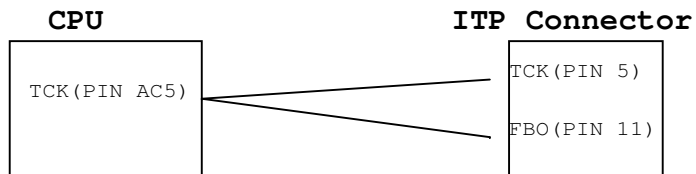
Size A4	Document Number JE50 SB	Rev SB
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Date: Friday, April 01, 2011 Sheet 52 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ITP

Size

Document Number

Rev

A4

JE50 SB

SB

Date: Friday, April 01, 2011

Sheet 55 of 102

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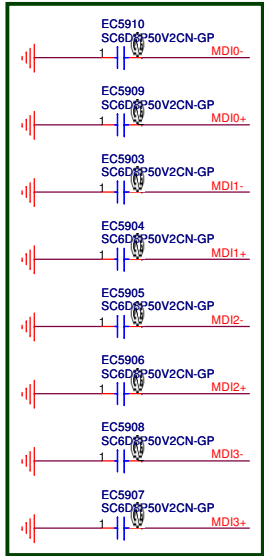
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

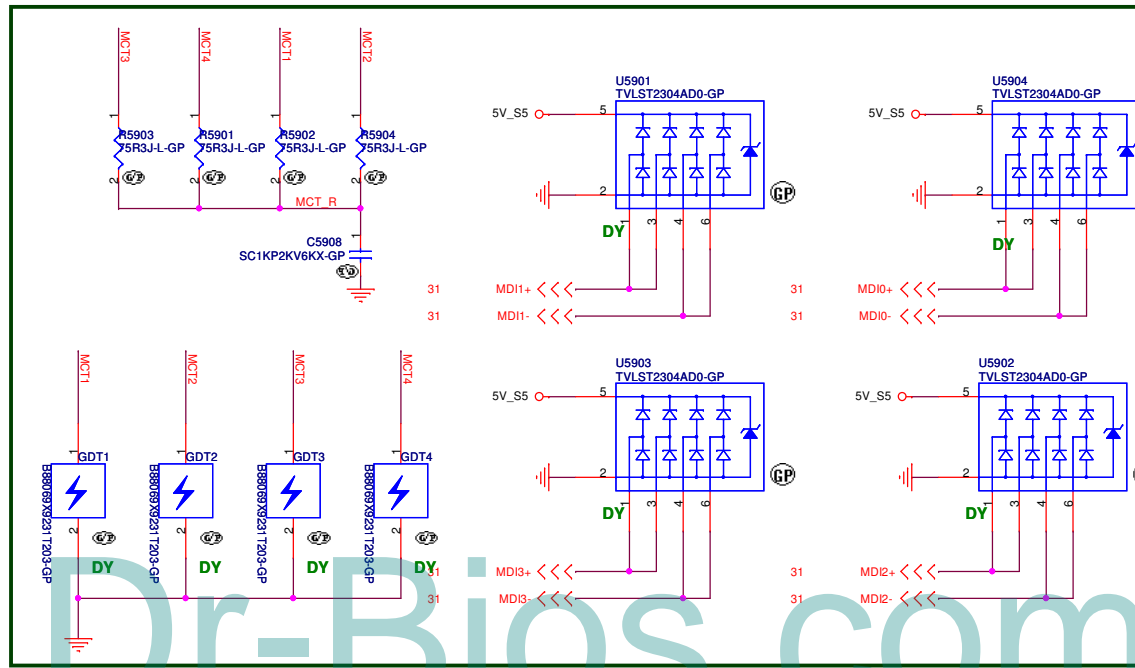
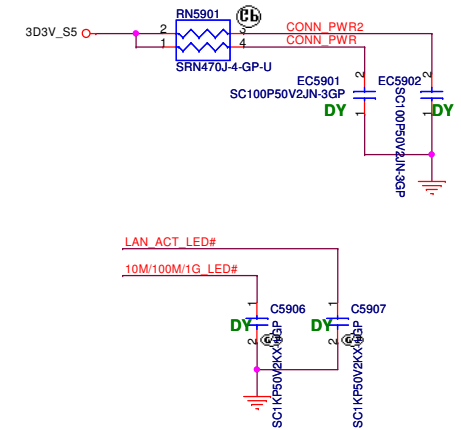
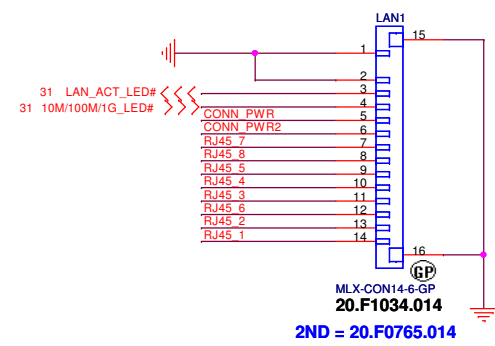
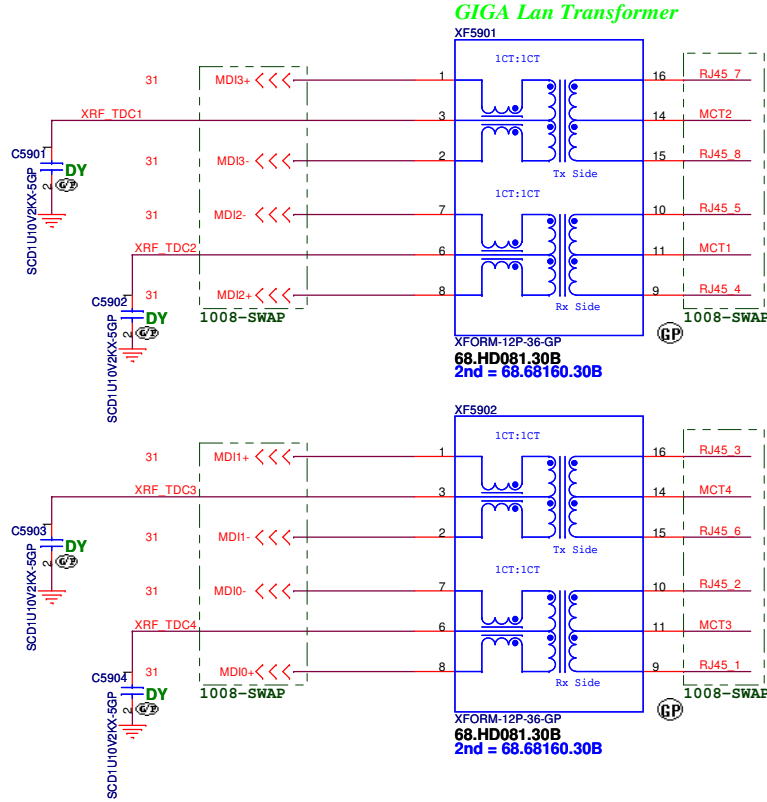
Title **ESATA/USB Charger**

Size A4 Document Number **JE50 SB** Rev **SB**

Date: Friday, April 01, 2011 Sheet 57 of 102



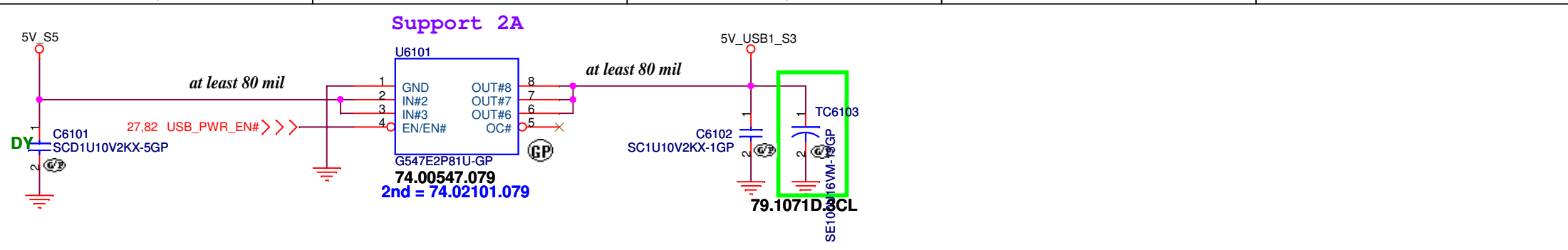
0914-SA for Vendor Suggestion



0914-SA for EMI

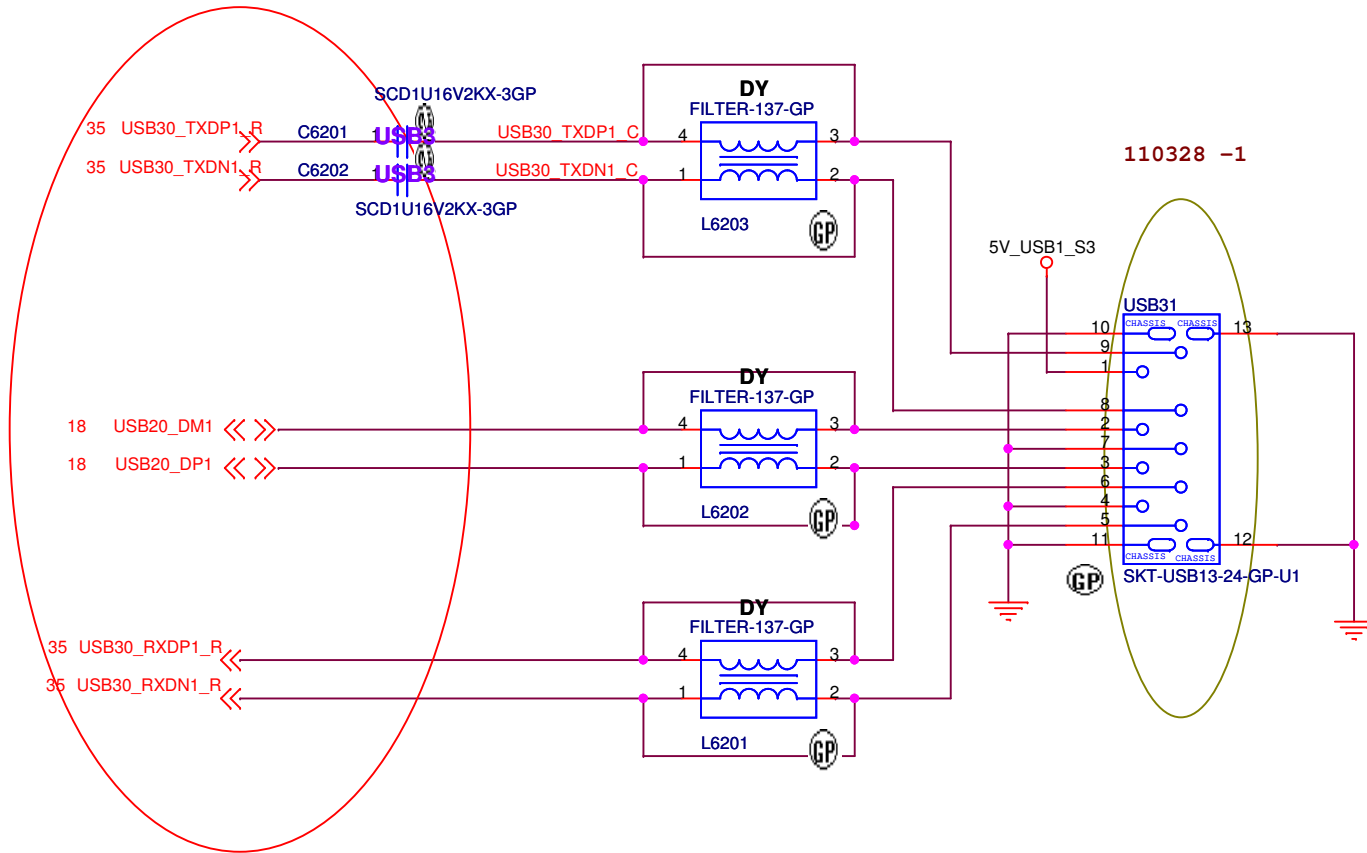
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
LAN CONN			
Title	Document Number		
Size	JE50 SB		Rev
A3			SB
Date:	Friday, April 01, 2011	Sheet	59 of 102



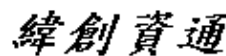
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Title		
USB Power SW		
Size	Document Number	Rev
A4	JE50 SB	SB
Date:	Friday, April 01, 2011	Sheet 61 of 102



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

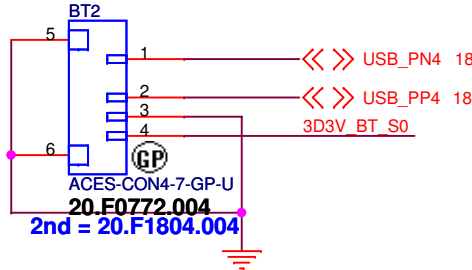
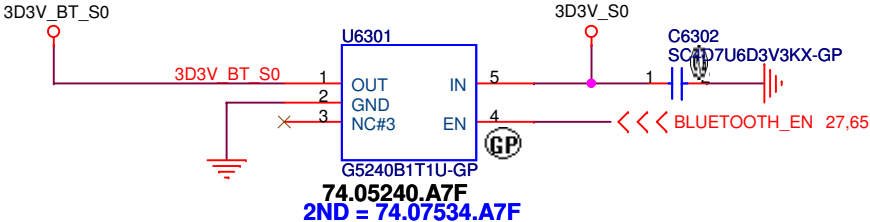
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 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB 3.0	
Size A4	Document Number JE50 SB
Date: Friday, April 01, 2011	Sheet 62 of 102

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ANNIE Bluetooth Module

1.5A / High Active Voltage 2V



<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
BLUE TOOTH	
Size	Document Number
A4	JE50 SB
Date:	Rev
Friday, April 01, 2011	SB
Sheet 63 of 102	

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

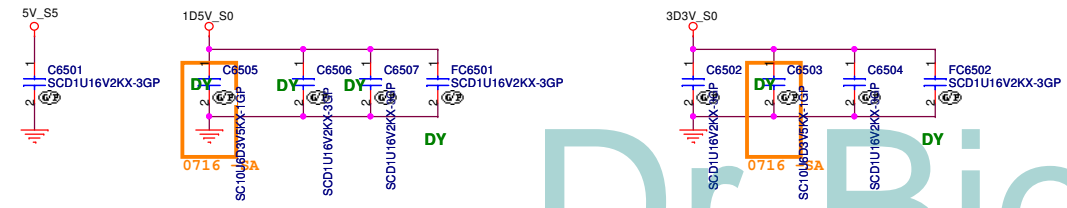
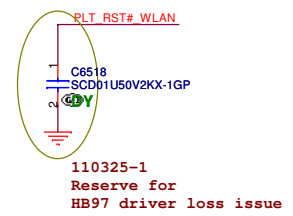
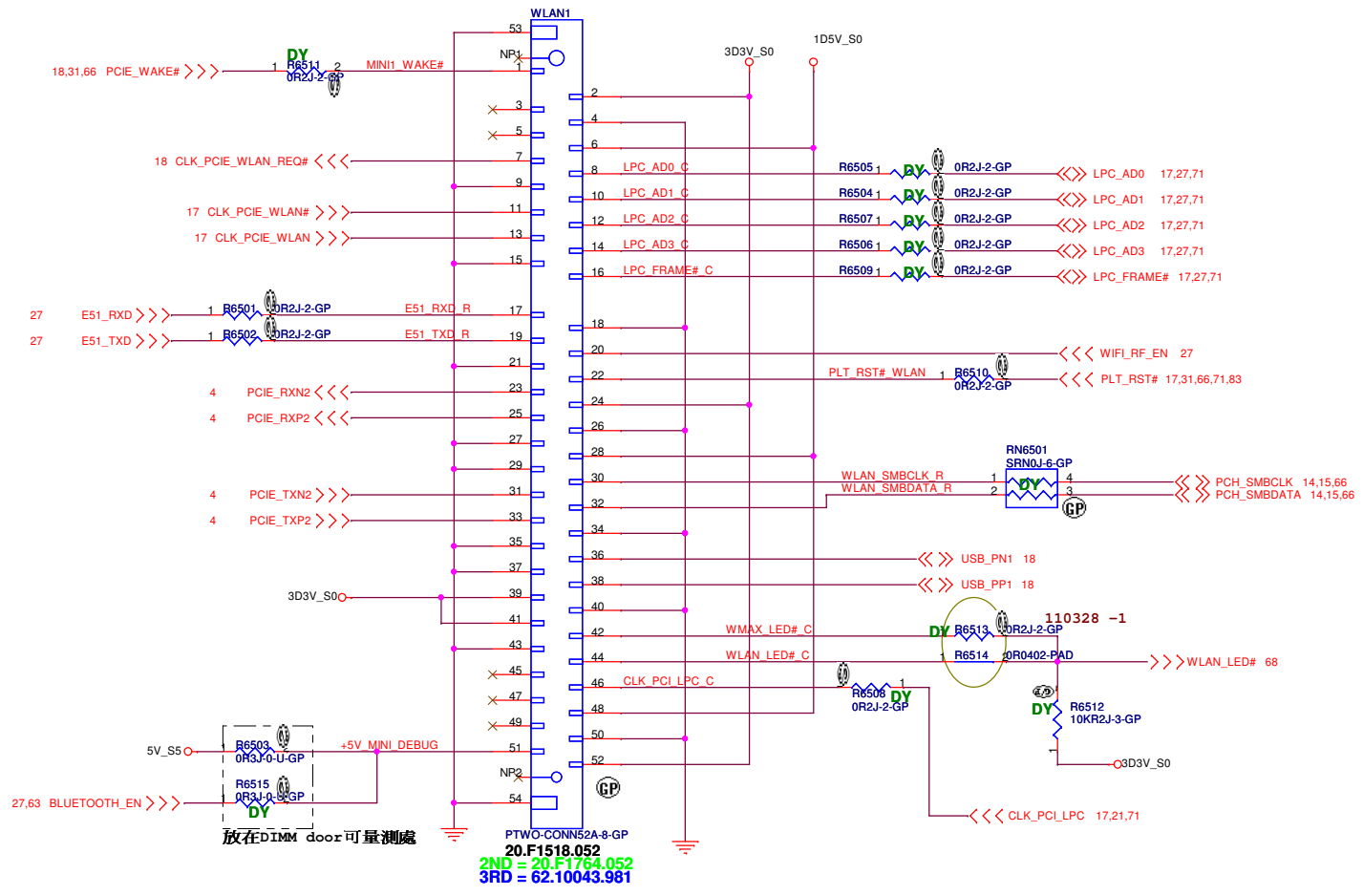
Title **Reserved**

Size A4	Document Number JE50 SB	Rev SB
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Date: Friday, April 01, 2011 Sheet 64 of 102

Mini Card Connector(802.11a/b/g/n)

R6504-R6509 close to Debug connector



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<Variant Name>

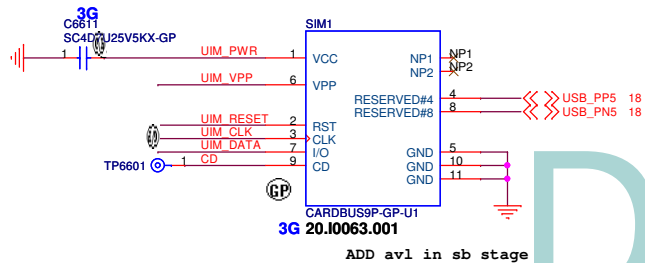
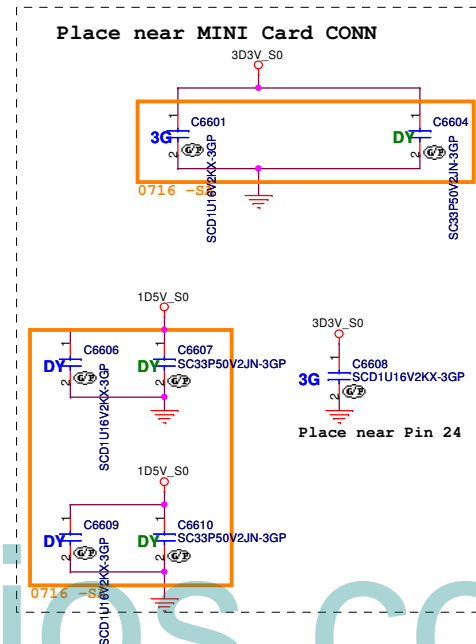
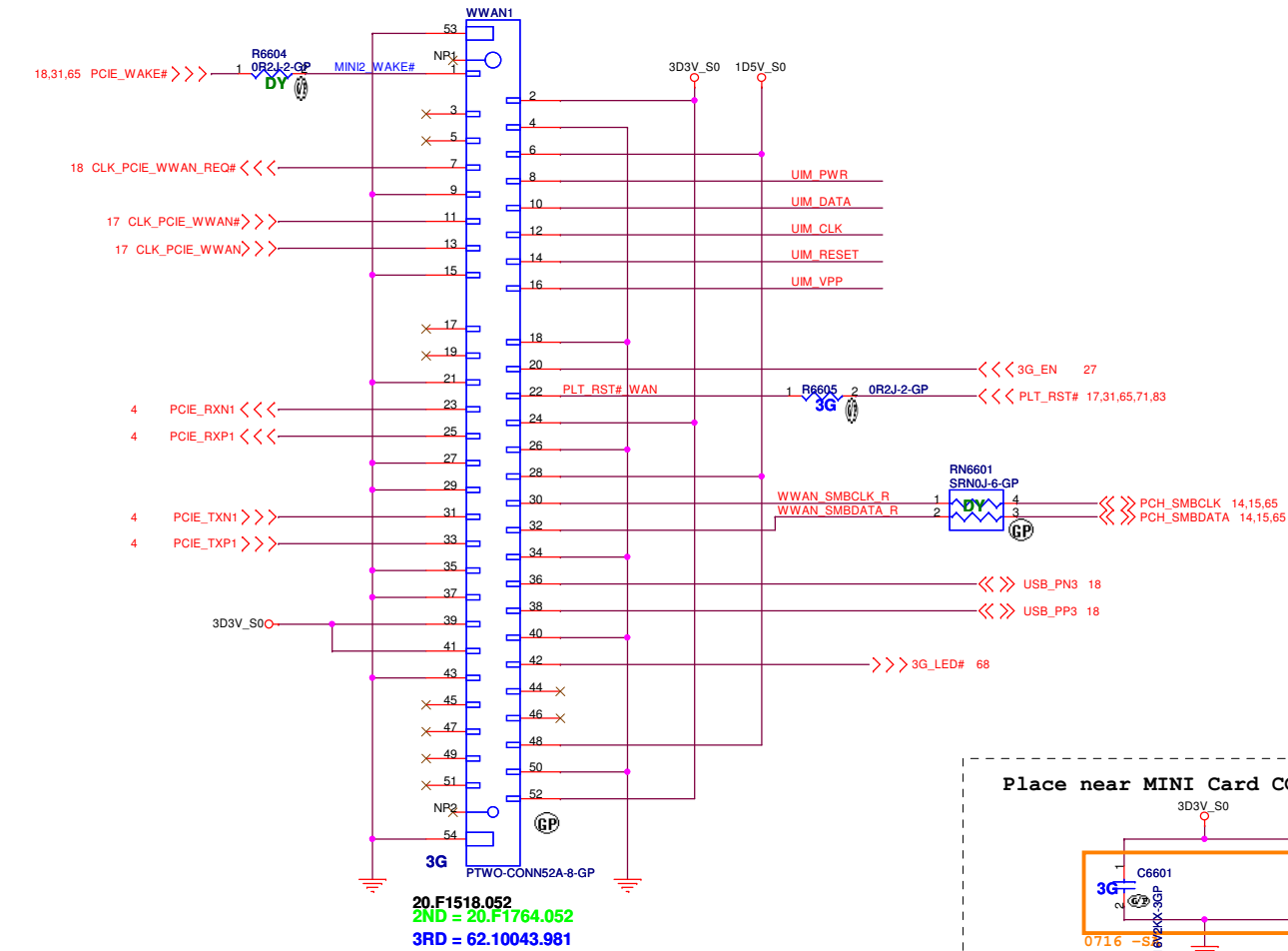
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN

Size A3 Document Number: JE50 SB Rev: SB

Date: Friday, April 01, 2011 Sheet 65 of 102

Mini Card Connector(WWAN)



<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
WWAN			
Size A3	Document Number JE50 SB	Rev SB	
Date: Friday, April 01, 2011	Sheet 66	of	102

Dr-Bios.com

(Blanking)

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<Variant Name>

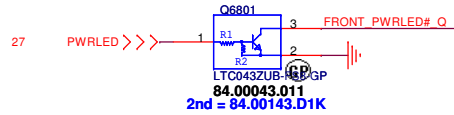
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

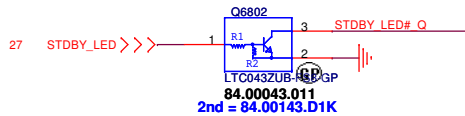
Size A4	Document Number JE50 SB	Rev SB
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Date: Friday, April 01, 2011 Sheet 67 of 102

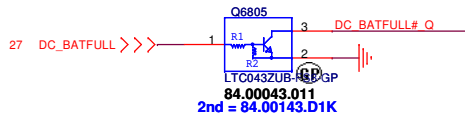
Power button LED



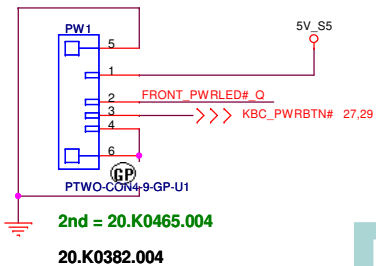
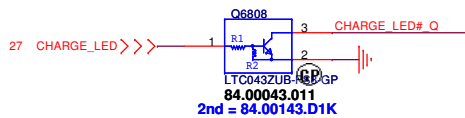
Power STDBY_LED



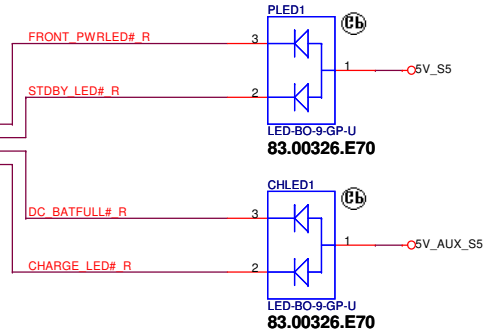
Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)

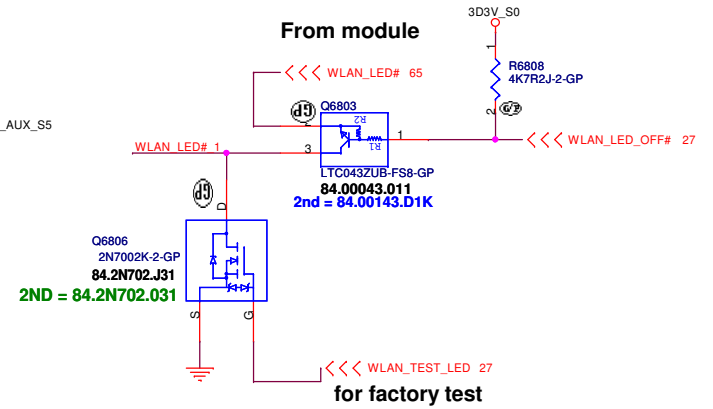


- FRONT_PWRLED#_O R6801 330R2F-GP
- STDBY_LED#_O R6802 470R2F-GP
- DC_BATFULL#_O R6803 330R2F-GP
- CHARGE_LED#_O R6804 470R2F-GP

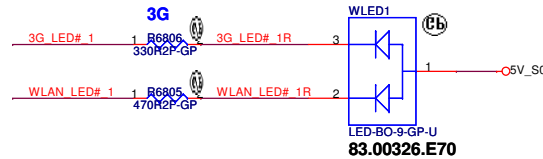
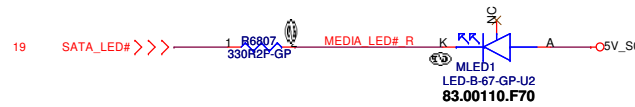


- FRONT_PWRLED#_O EC6801 DY SCD1U10V2KX-4GP
- CHARGE_LED#_O EC6802 DY SCD1U10V2KX-4GP
- STDBY_LED#_O EC6803 DY SCD1U10V2KX-4GP
- DC_BATFULL#_O EC6804 DY SCD1U10V2KX-4GP

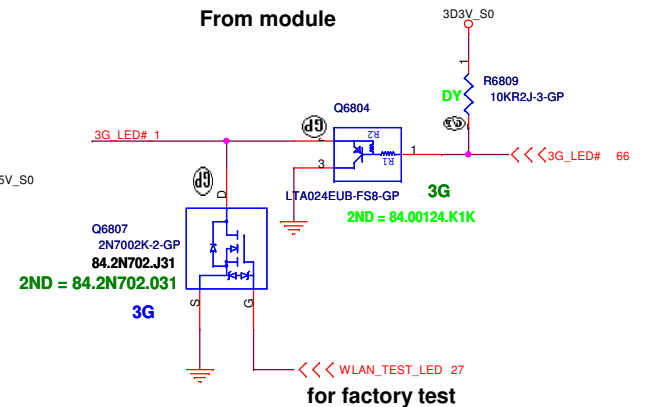
WLAN_LED



SATA HDD LED



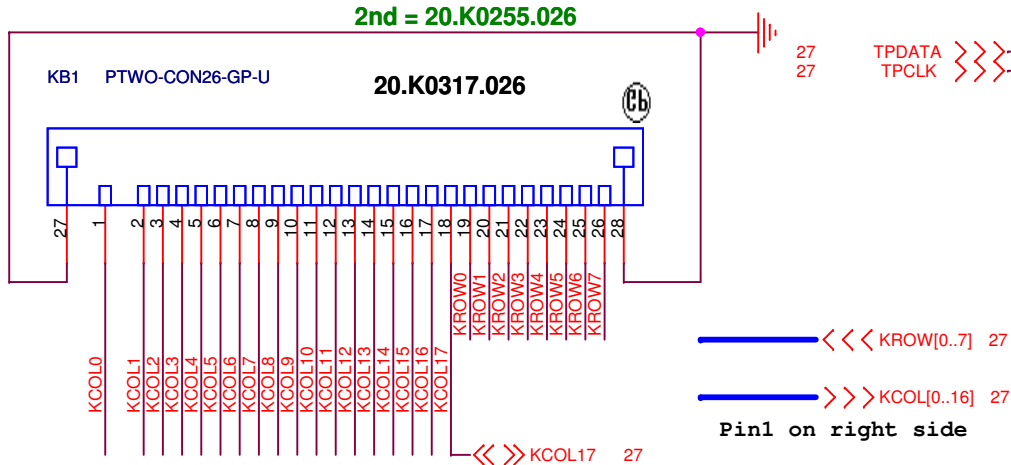
3G LED



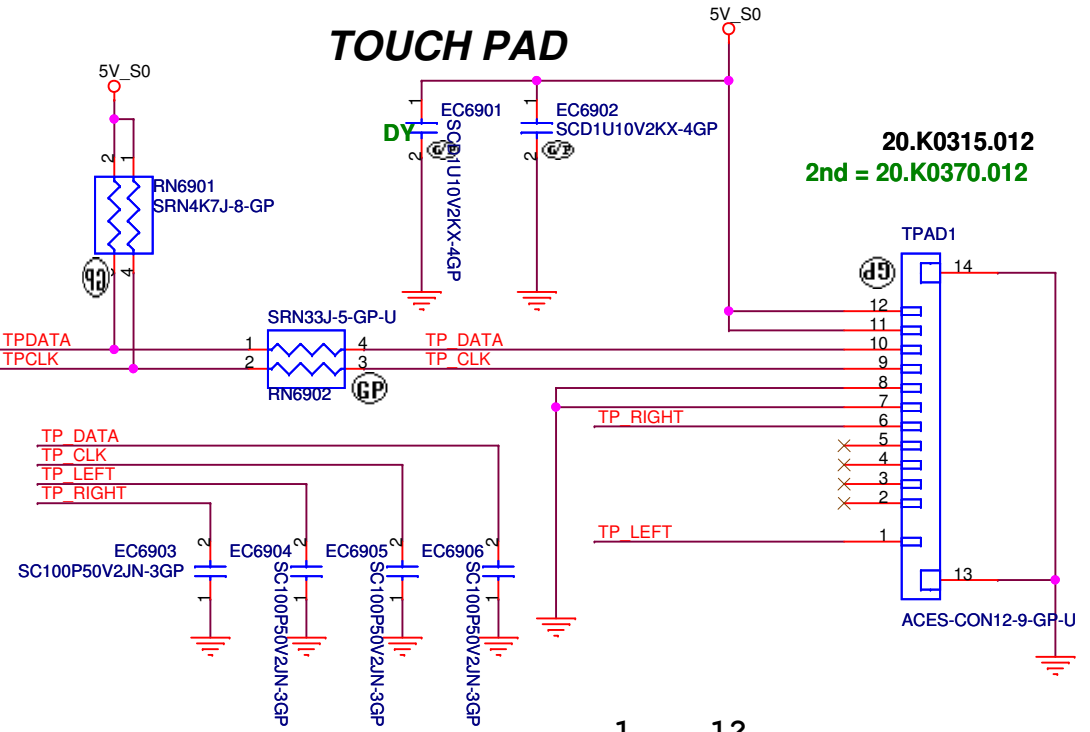
Dr-Bios.com

<Variant Name>		
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Title LED Bard/Power Button		
Size A3	Document Number JE50 SB	Rev SB
Date: Friday, April 01, 2011	Sheet 68	of 102

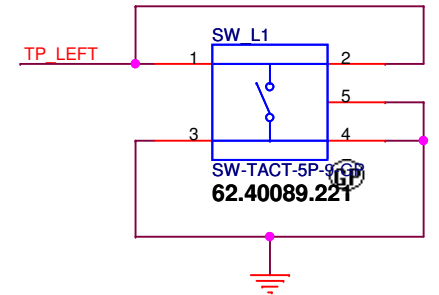
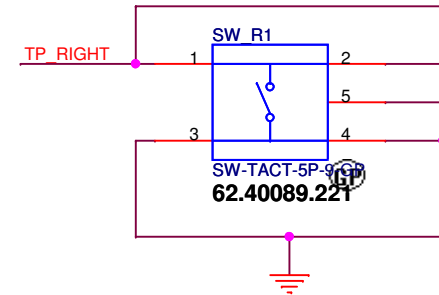
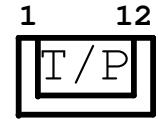
Internal KeyBoard Connector



TOUCH PAD



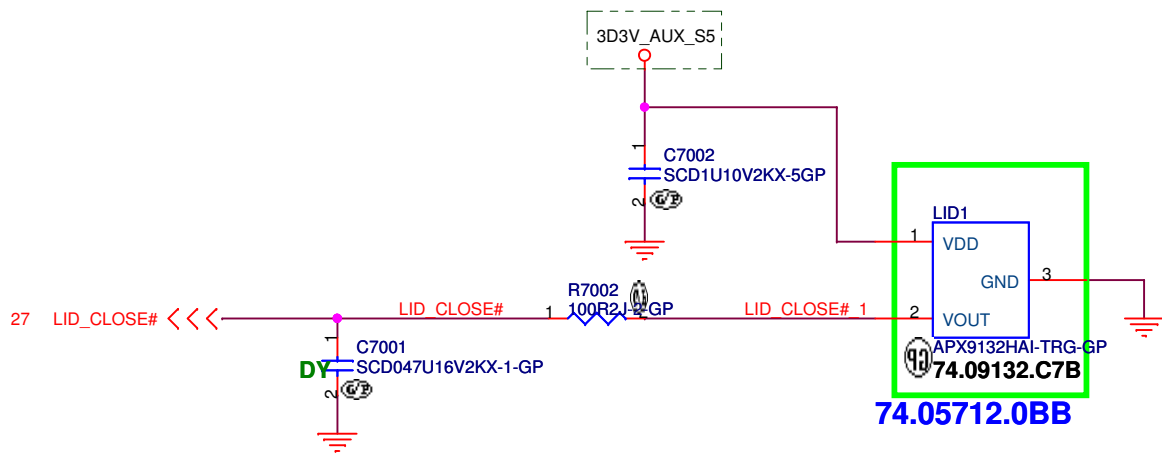
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2nd = 20.K0370.012



<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Key Board/Touch Pad			
Size A4	Document Number JE50 SB	Rev SB	
Date: Friday, April 01, 2011	Sheet 69	of	102

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<Variant Name>

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

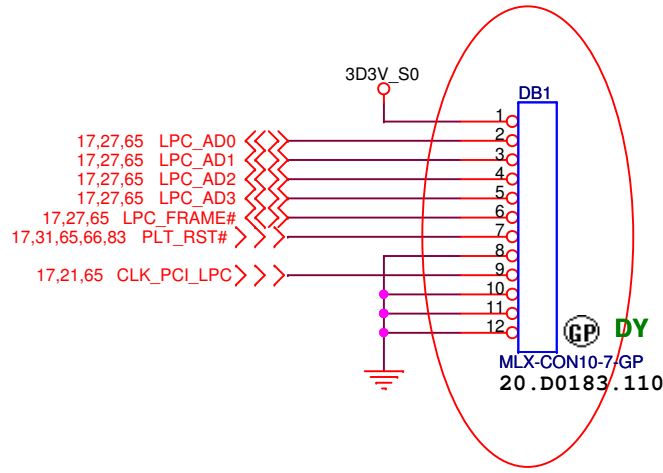
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Size A4 Document Number **JE50 SB** Rev **SB**

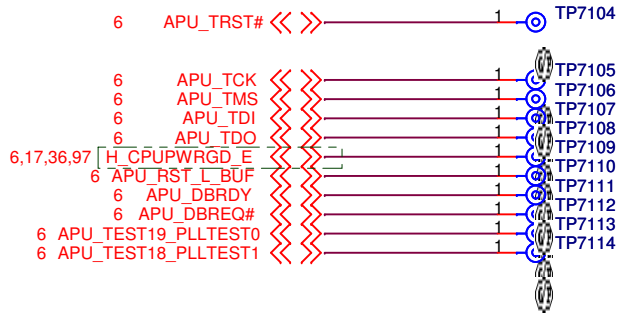
Date: Friday, April 01, 2011 Sheet 70 of 102

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110218 SB BOM Change



HDT+ Connectors



CRB:placed 0-ohm
 Checklist: If both SCAN and HDT+ header are implement
 placed 15-ohm

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
Size A4	Document Number JE50 SB		Rev SB
Date: Friday, April 01, 2011	Sheet 71	of	102

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(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

JE50 SB

Rev

SB

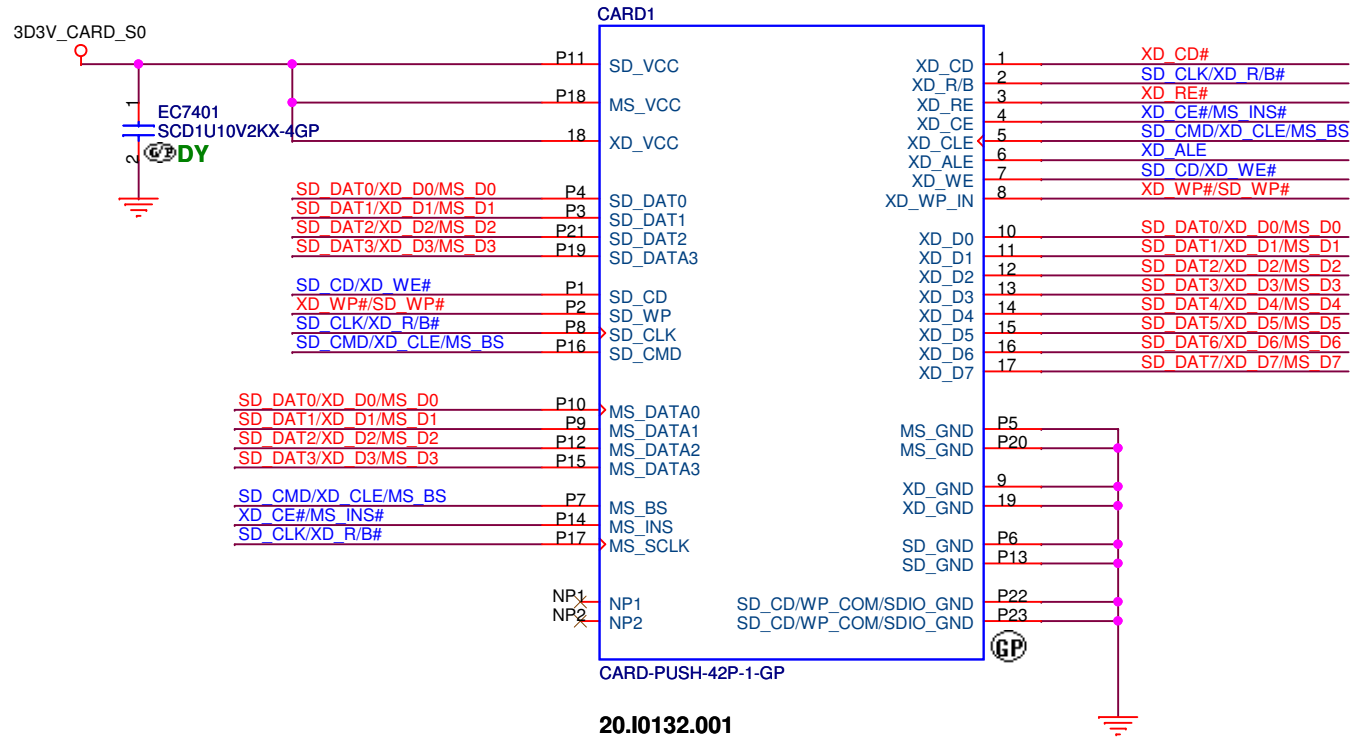
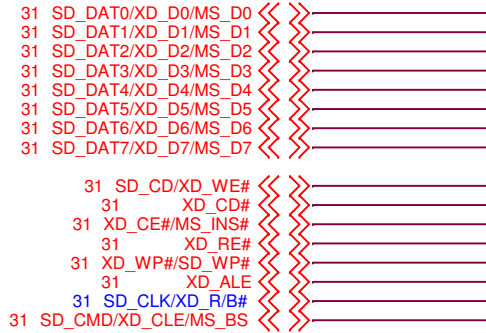
Date: Friday, April 01, 2011

Sheet 72 of 102

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SD/XD/MS Card Reader

SSID = SDIO



Pin No.	SD/MMC	MS/MS PRO	xD
P1	x0-R/B		2P
P2	x0-RE		3P
P3	x0-CE		4P
P4	x0-CLE		5P
P5	x0-ALE		6P
P6	x0-WE		7P
P7	x0-WP		8P
P8	x0-DO		10P
P9	x0-D1		11P
P10	SD-DAT2	8P	
P11	SD-DAT3	1P	
P12	SD-CMD	2P	
P13	4in1-GND	3P/8P	1P/10P 1P/9P
P14	MS-VCC		8P
P15	MS-SCLK		8P
P16	MS-DATA3		7P
P17	MS-INS		6P
P18	MS-DATA2		5P
P19	MS-DATA0		4P

Pin No.	SD/MMC	MS/MS PRO	xD
P20	MS-DATA1		3P
P21	MS-BS		2P
P22	4in1-GND	3P/8P	1P/10P 1P/9P
P23	SD-VCC		4P
P24	SD-CLK		5P
P25	SD-DAT0		7P
P26	x0-D2		12P
P27	x0-D3		13P
P28	x0-D4		14P
P29	SD-DAT1	8P	
P30	x0-D5		15P
P31	x0-D6		16P
P32	x0-D7		17P
P33	x0-VCC		18P
P34	x0-CD-SW		18P
P35	SD-WP-SW	SD-WP-SW	
P36	SD-CD-SW	SD-CD-SW	
P37			
P38	4 IN 1-GND	SD-WP/CD-SW-GND	

<Variant Name>

Card-reader Off-Page

緯創資通

Wistron Corporation

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 Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size

Document Number

Rev

A4

JE50 SB

SB

Date: Friday, April 01, 2011

Sheet 74 of 102

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<Variant Name>

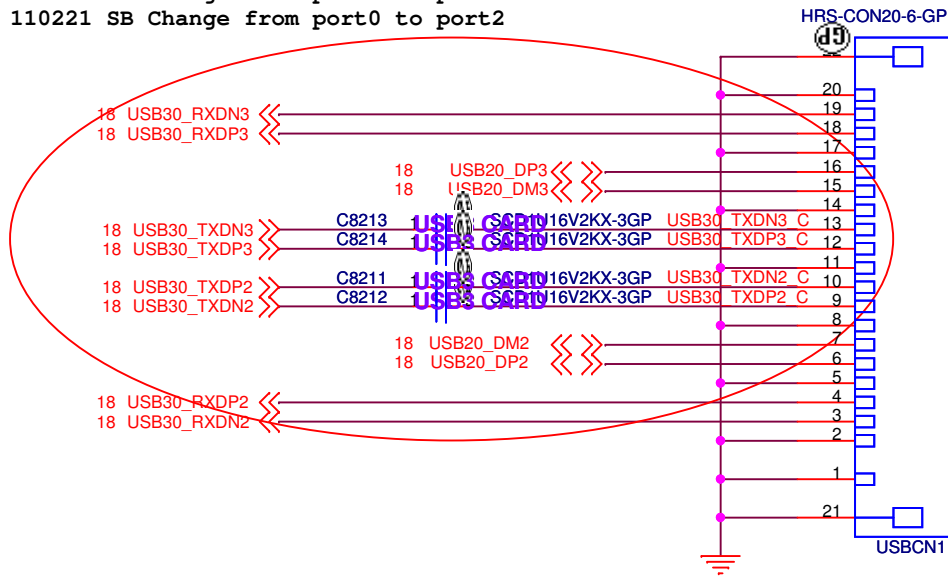
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4	Document Number JE50 SB	Rev SB
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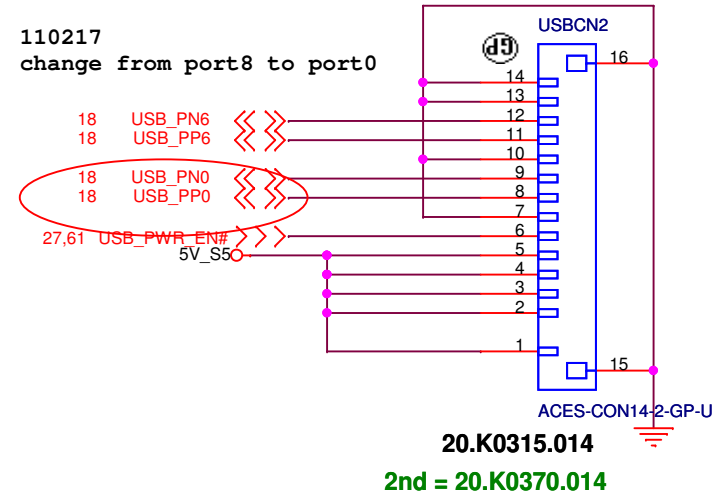
Date: Friday, April 01, 2011 Sheet 75 of 102

110221 SB Change from port1 to port3
 110221 SB Change from port0 to port2



USB3 CARD

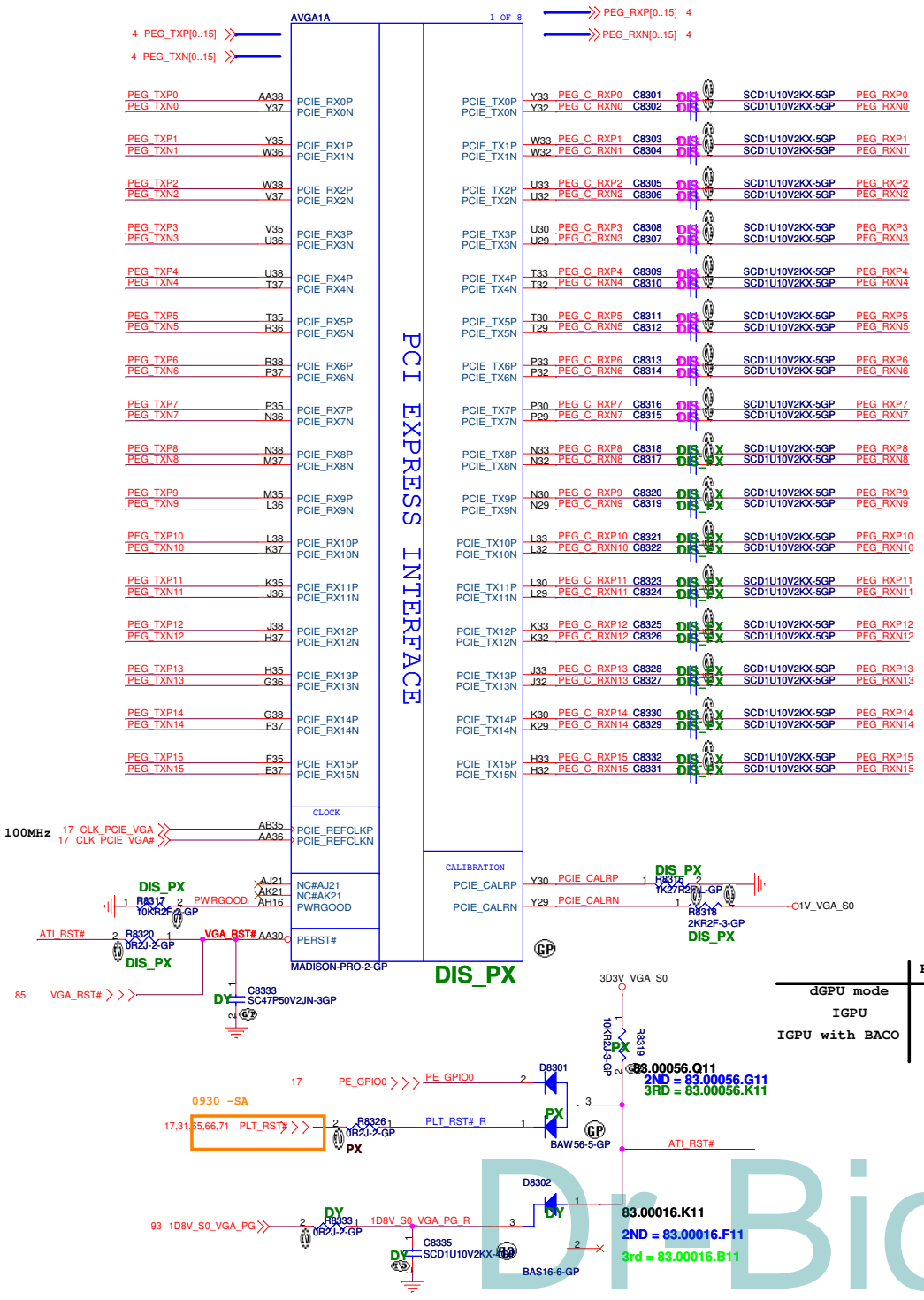
110217
change from port8 to port0



<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
IO Board Connector			
Size A4	Document Number JE50 SB		Rev SB
Date: Friday, April 01, 2011	Sheet 82	of	102

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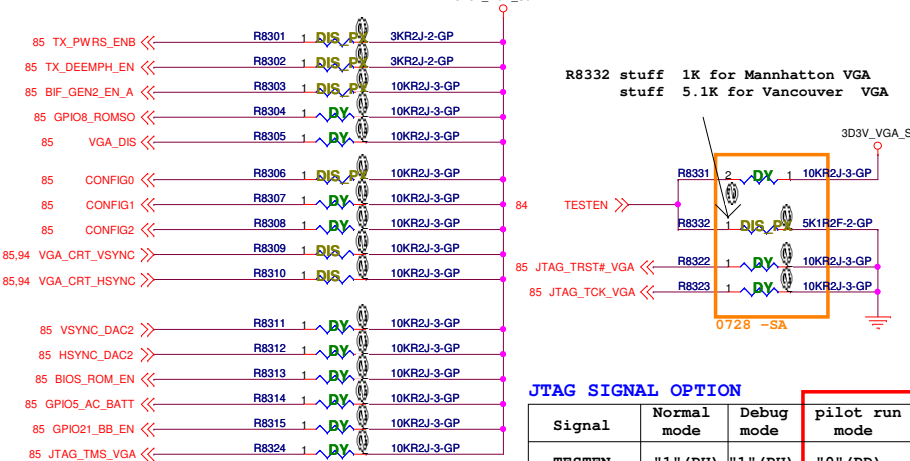


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (2.56MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYS		X	1

PIN STRAPS



R8332 stuff 1K for Manhattan VGA
stuff 5.1K for Vancouver VGA

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC

	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACO	H

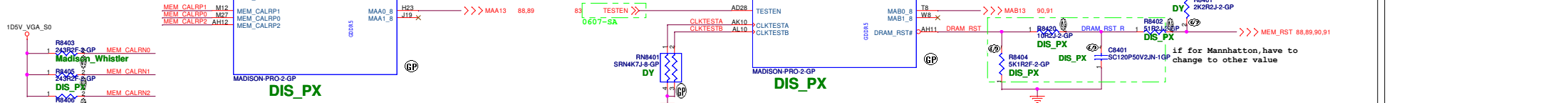
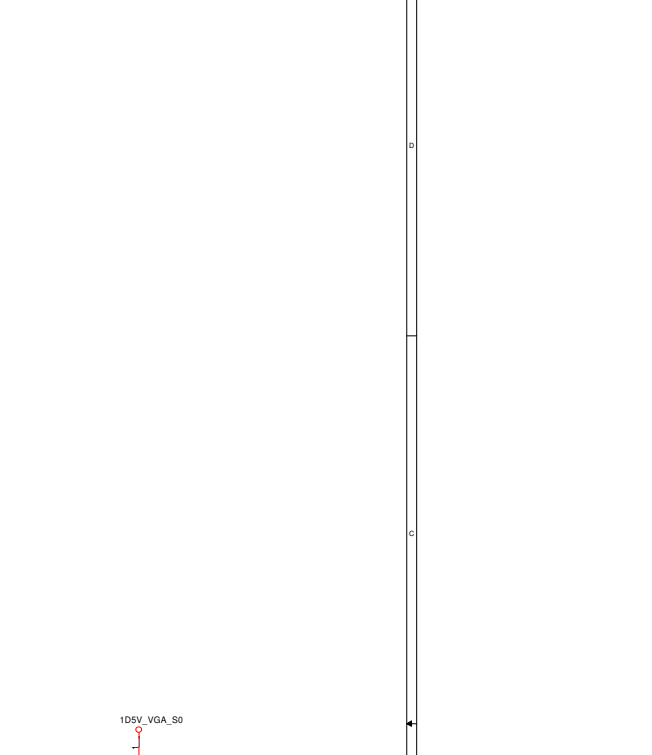
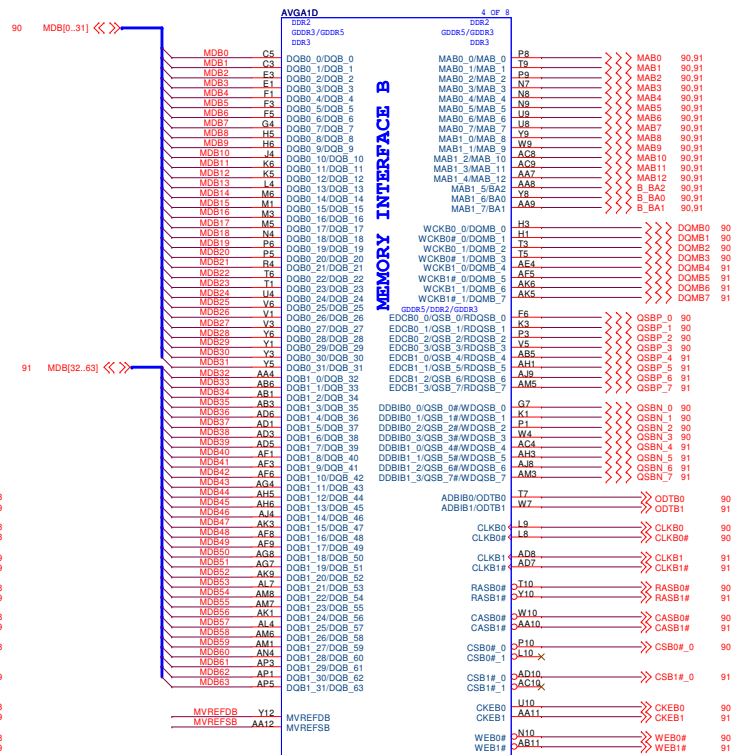
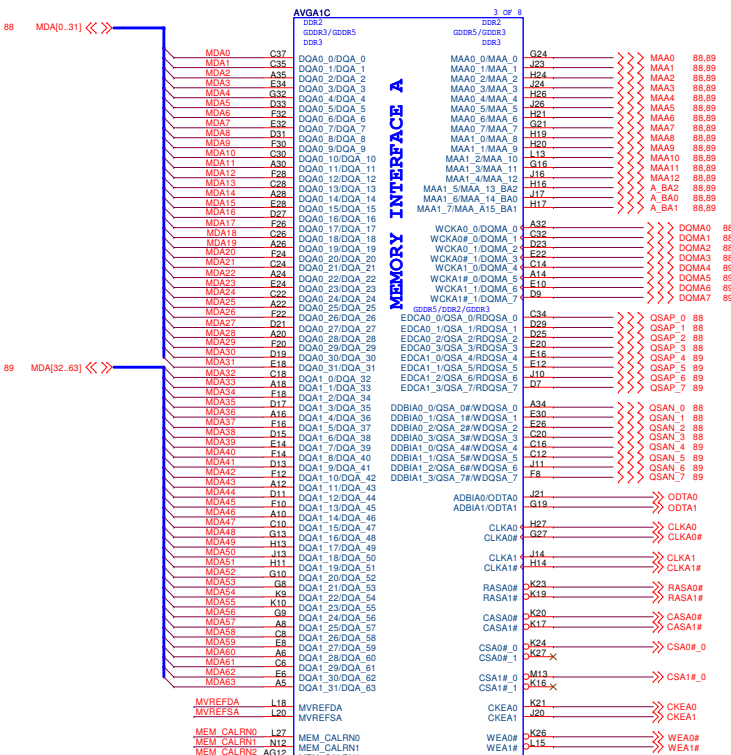
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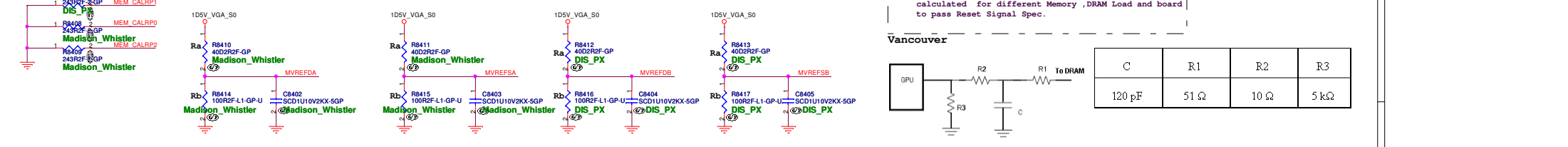
GPU PCIe STRAPPING(1/5)

Size: JE50 SB
Date: Friday, April 01, 2011
Sheet: 83 of 102





PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

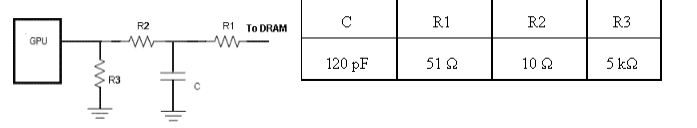


DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

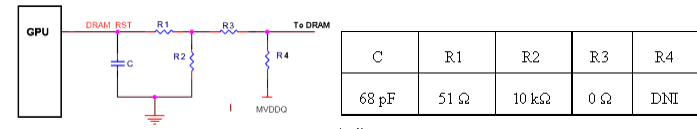
** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Vancouver

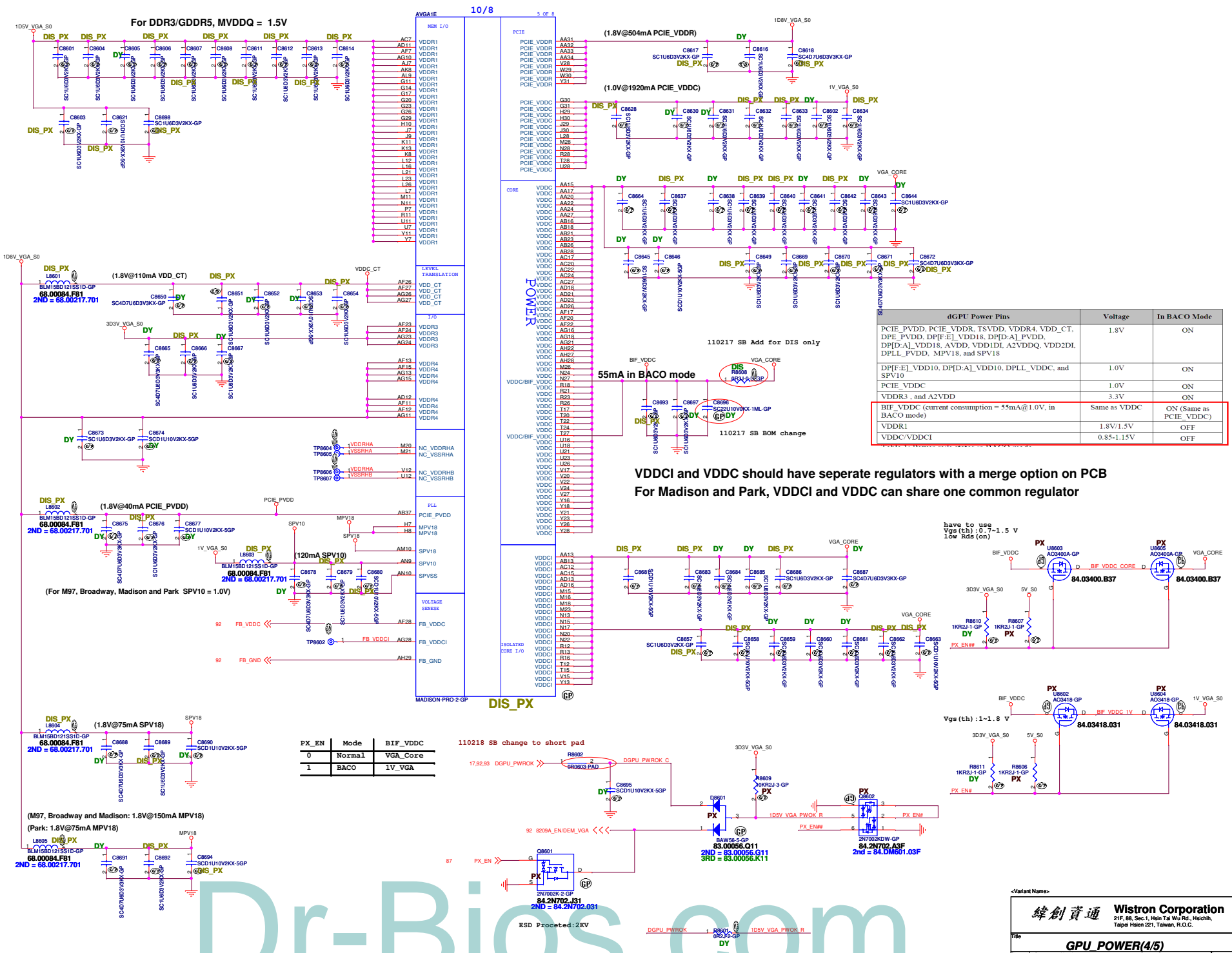


C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

Mannhatton



C	R1	R2	R3	R4
68 pF	51 Ω	10 kΩ	0 Ω	DNI



dGPU Power Plus	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVD, VDDR4, VDD_CT, DPE_PVDD, DP[E-]_VDD18, DP[D-A]_PVDD, DP[D-A]_VDD18, AVDD, VDD1D1, A2VDDQ, VDD2D1, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DP[E-]_VDD10, DP[D-A]_VDD10, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3, and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as BACO mode)
VDDR1	1.8V/1.5V	OFF
VDDC/VDDCI	0.85-1.15V	OFF

VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator

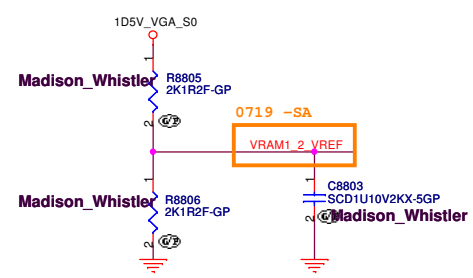
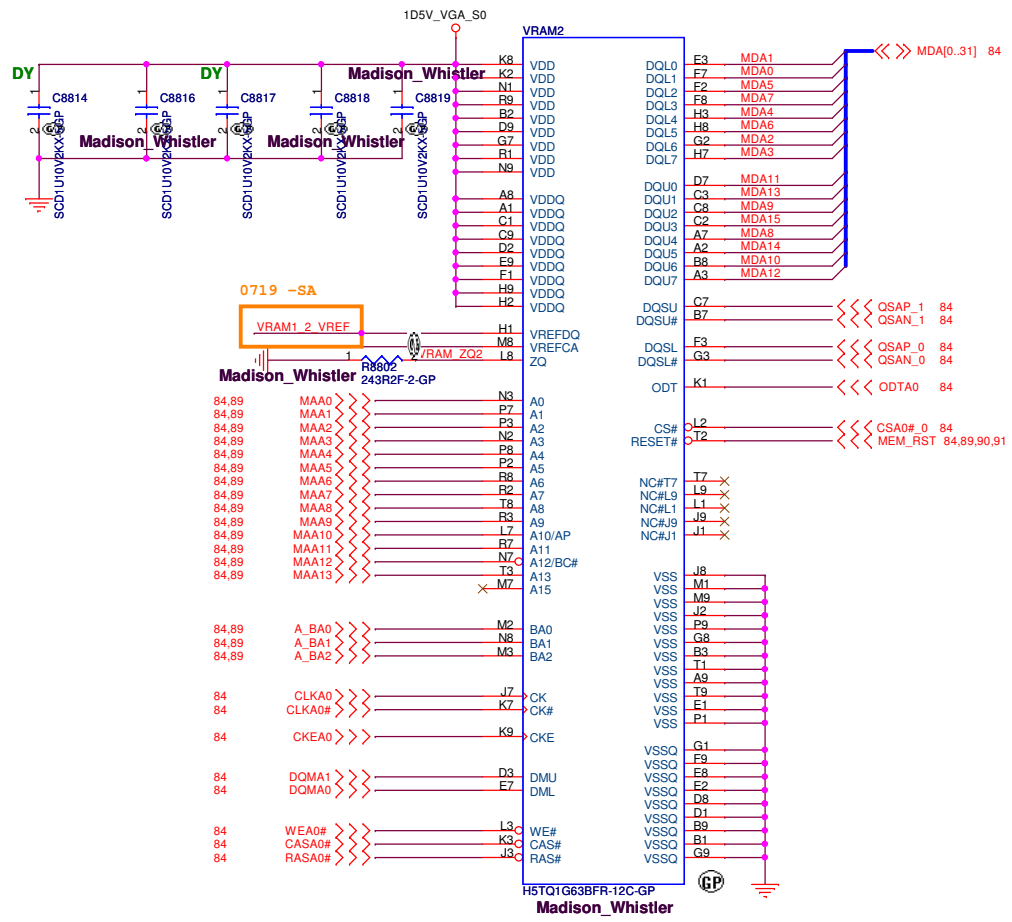
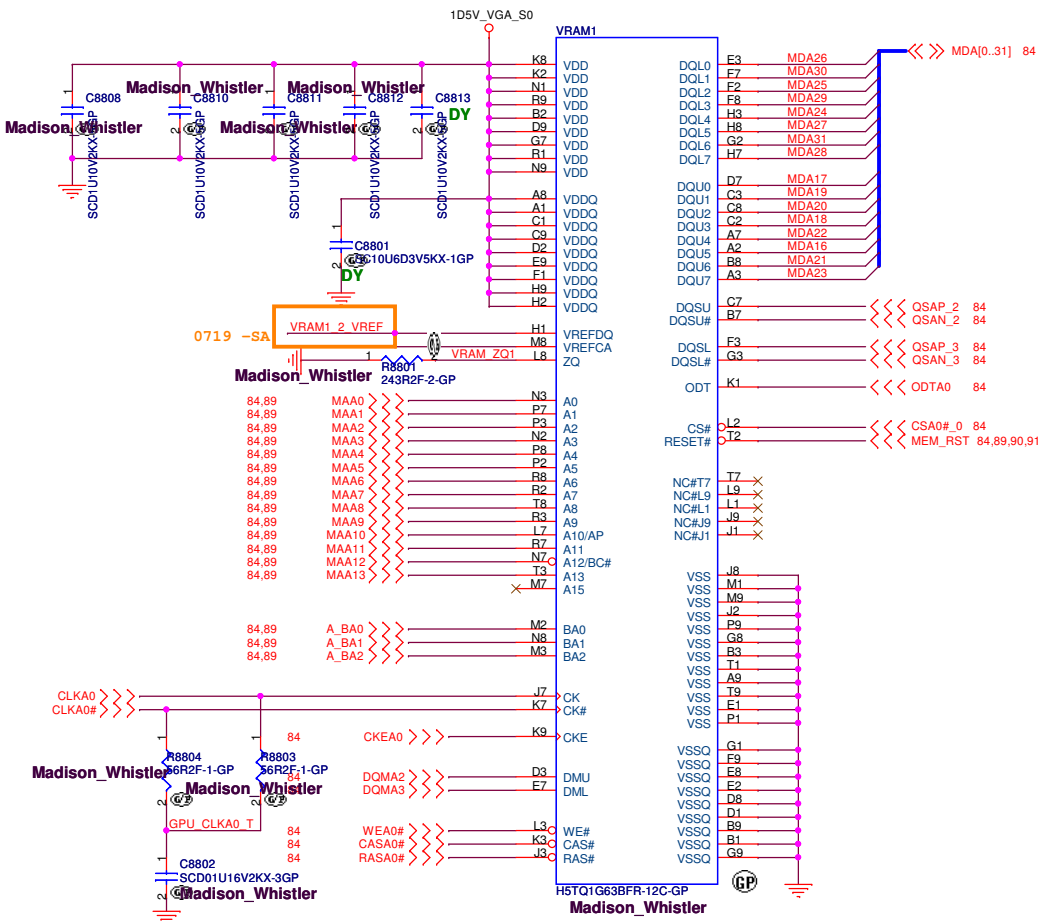
PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

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GPU POWER(4/5)
JE50 SB

Rev SB





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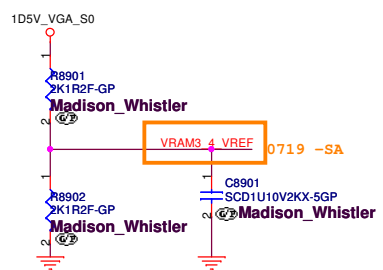
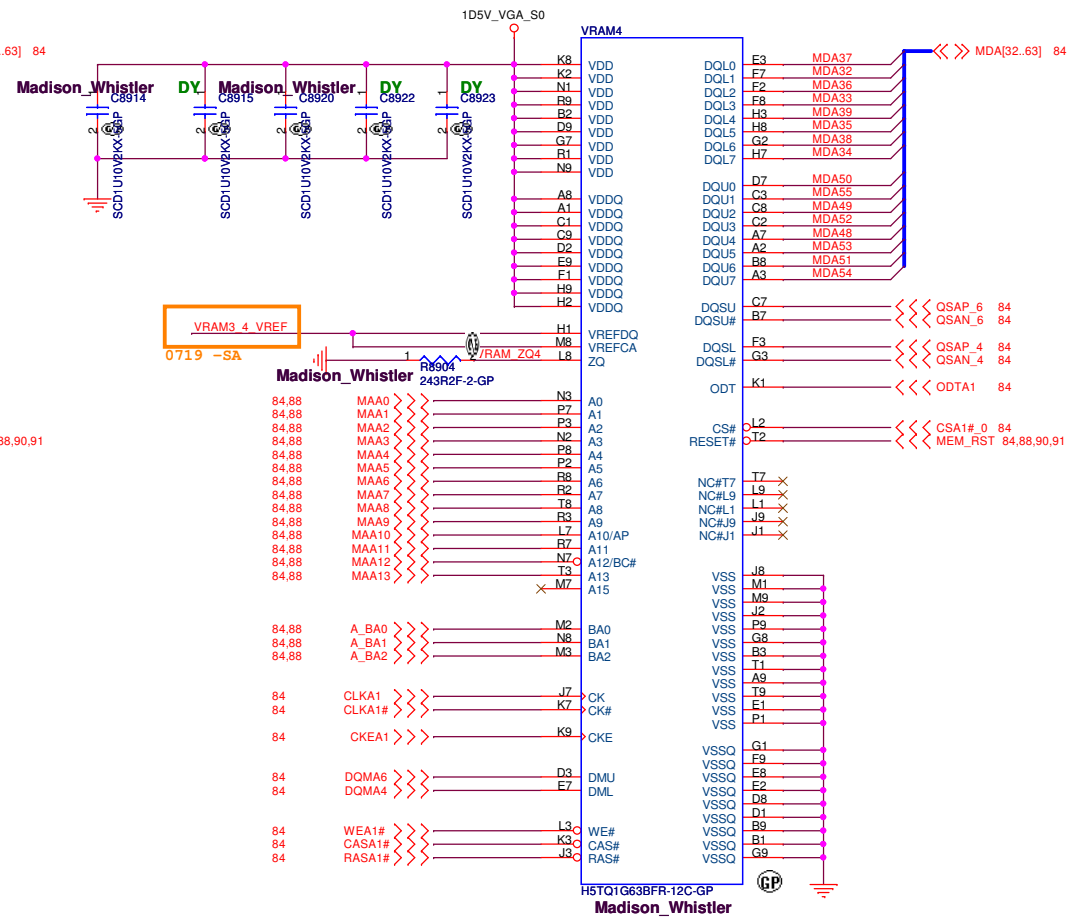
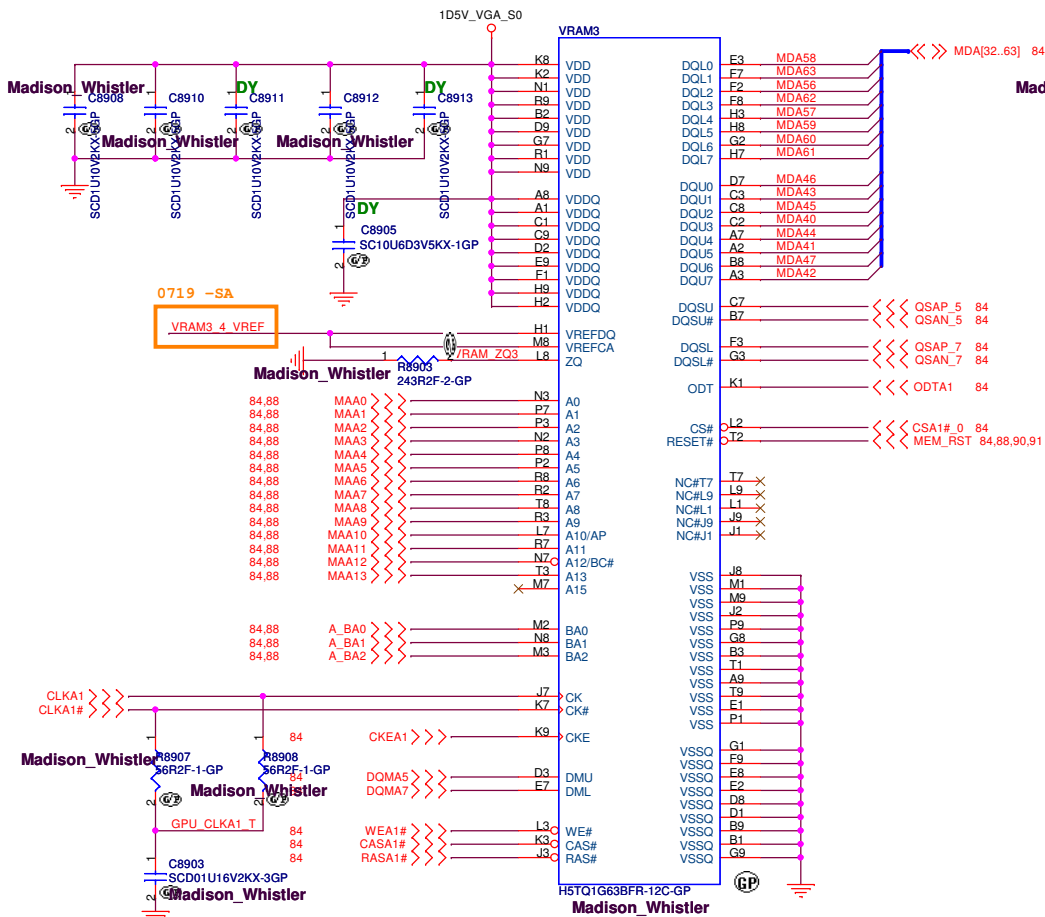
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緯創資通 Wistron Corporation
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Title GPU-VRAM1,2 (1/4)

Size A3 Document Number JE50 SB Rev SB

Date: Friday, April 01, 2011 Sheet 88 of 102



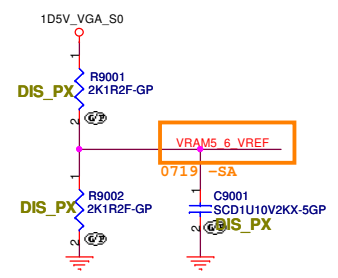
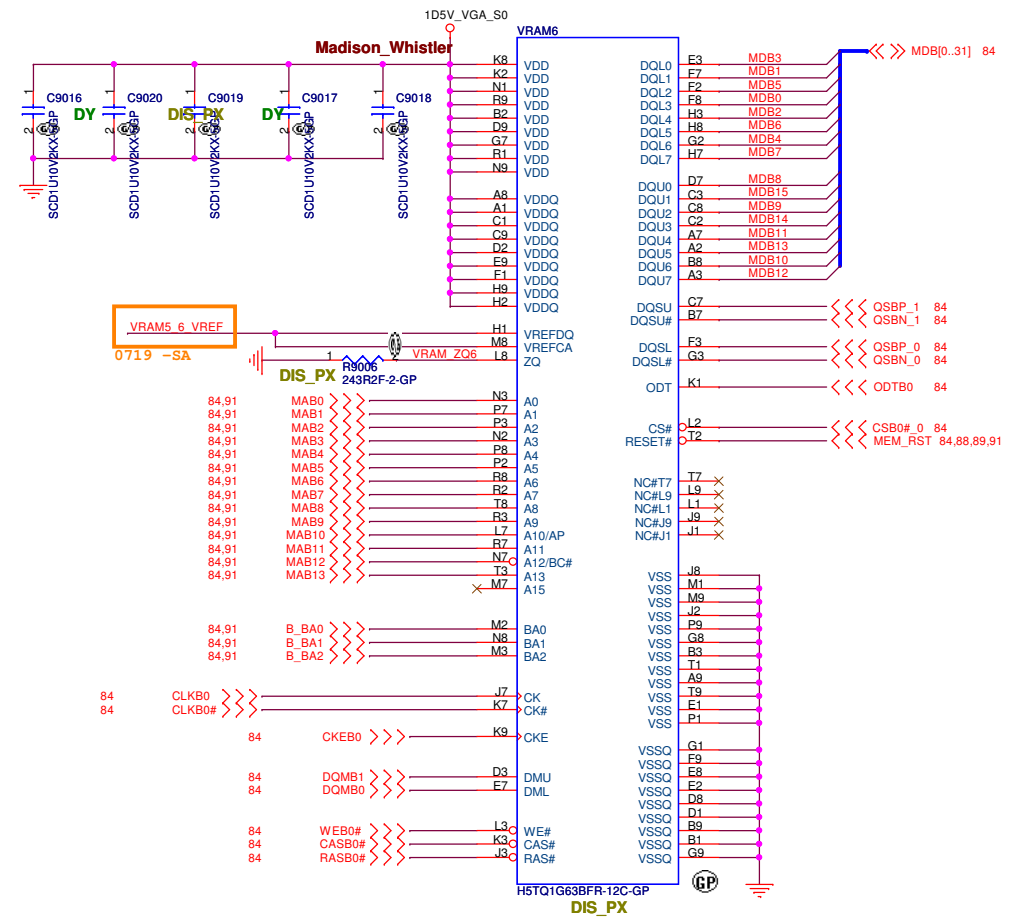
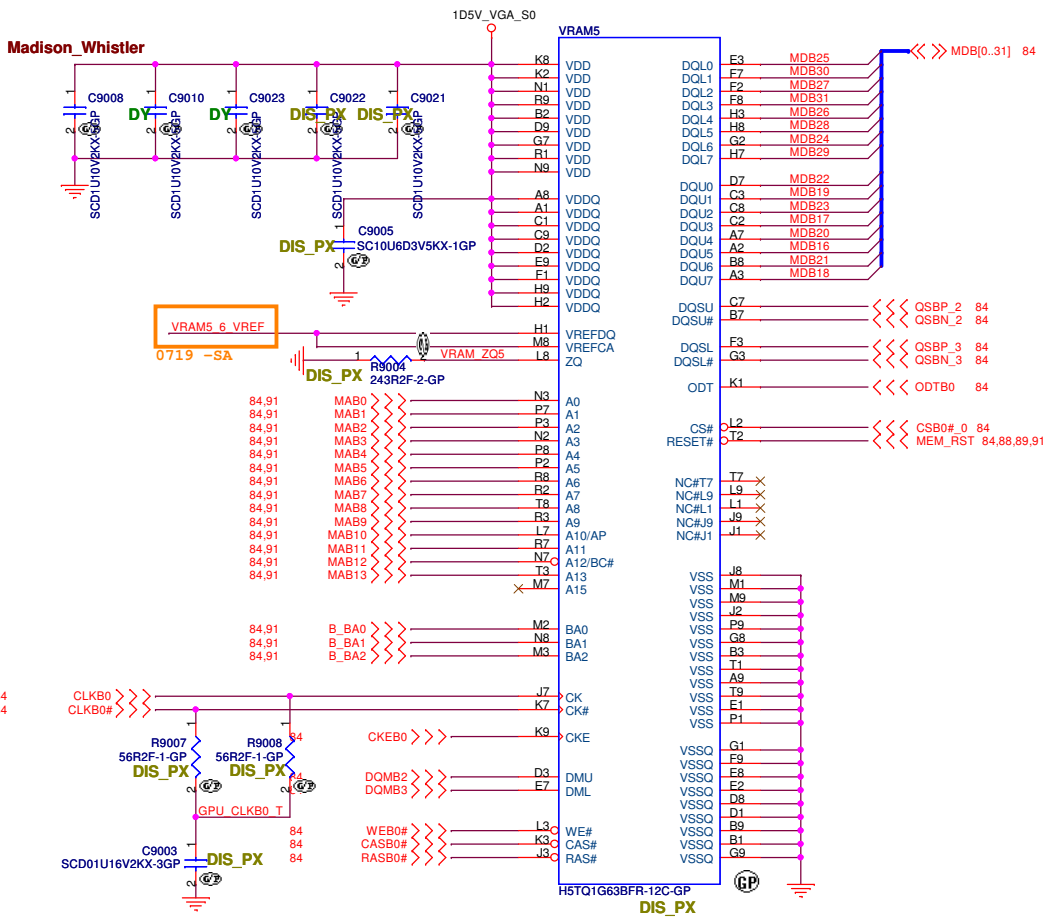
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緯創資通 Wistron Corporation
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Title: GPU-VRAM3,4 (2/4)

Size A3	Document Number JE50 SB	Rev SB
Date: Friday, April 01, 2011	Sheet 89 of 102	



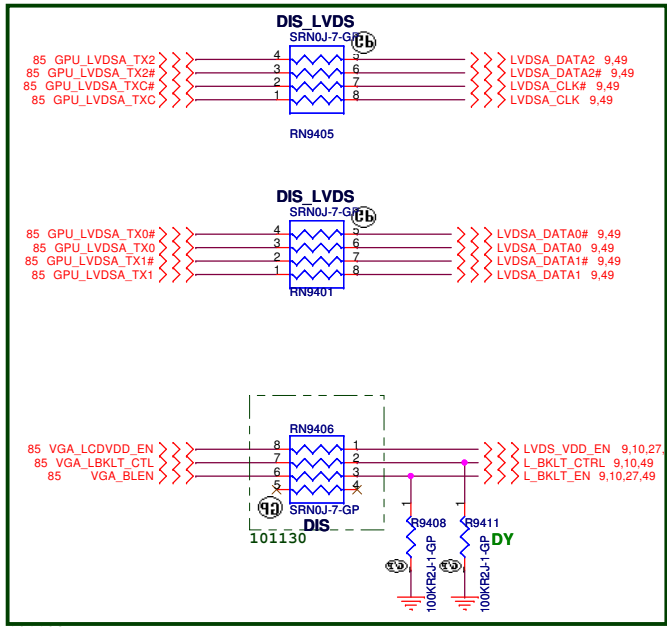
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

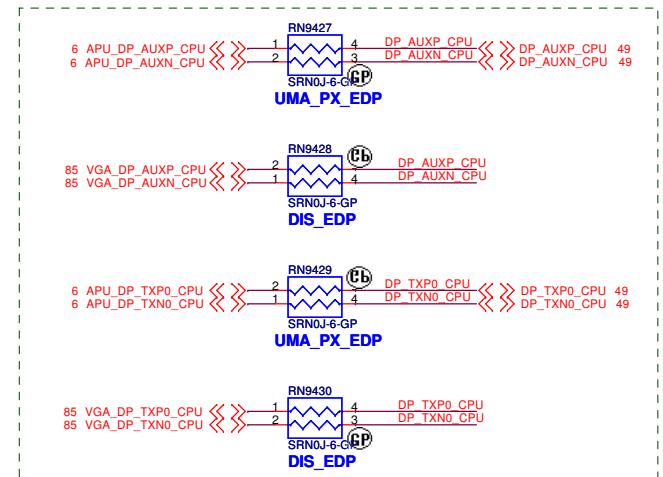
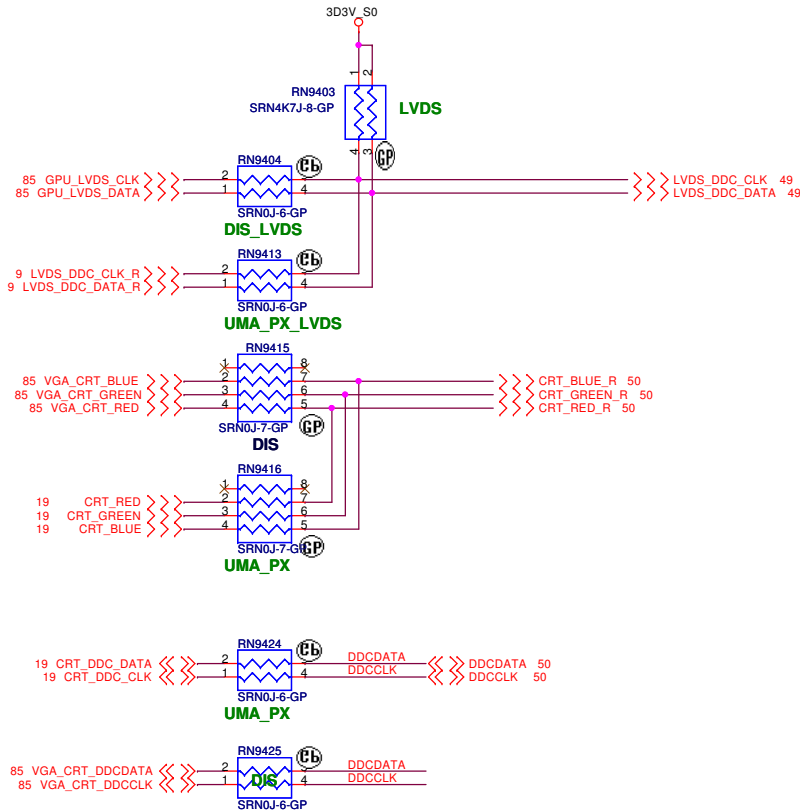
Size A3	Document Number JE50 SB	Rev SB
Date: Friday, April 01, 2011	Sheet 90 of 102	



101123

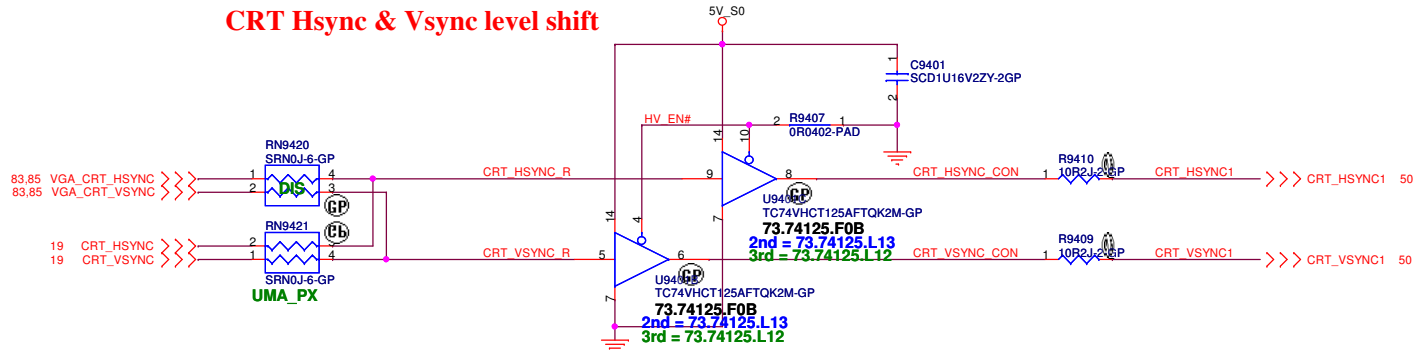


0804-SA



if Co-layout LVDS and EDP panel,
have to place Res near LVDS Cap
for Reflection Prevent

CRT Hsync & Vsync level shift



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Title: LVDS Switch			
Size: A3	Document Number: JE50 SB	Rev: SB	
Date: Friday, April 01, 2011	Sheet: 94	of 102	

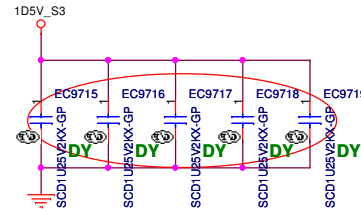
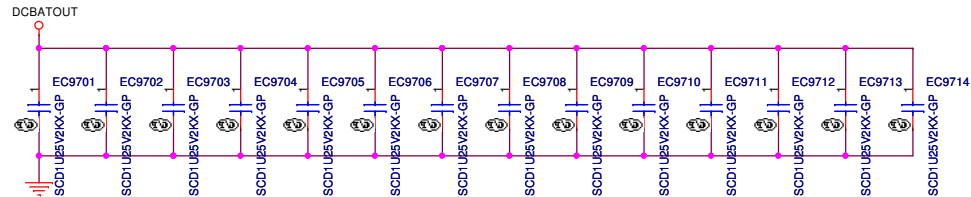
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Title			
Reserved			
Size A	Document Number JE50 SB		Rev SB
Date: Friday, April 01, 2011	Sheet	95 of	102

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110223 SB RF Solution

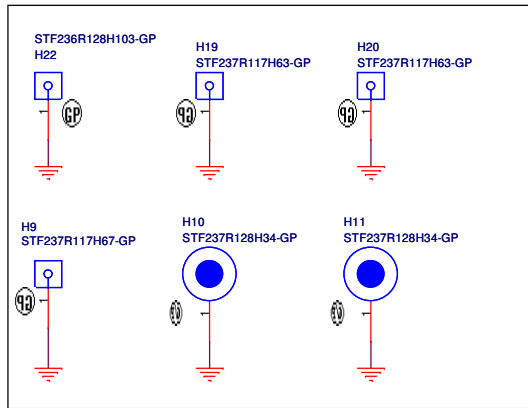
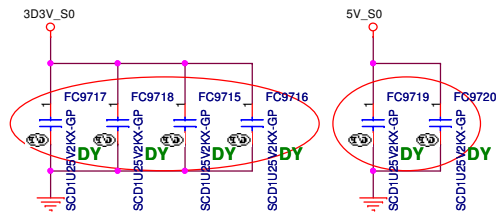
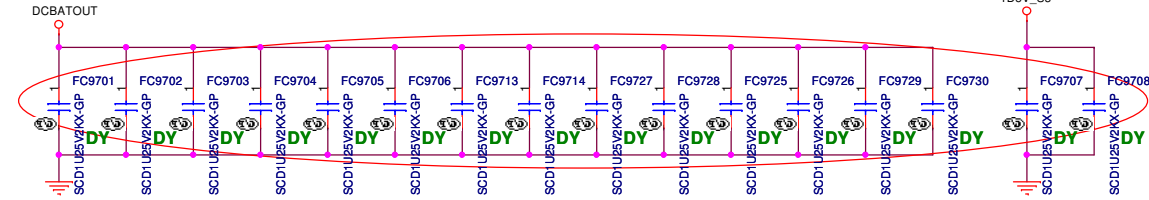


Check test point

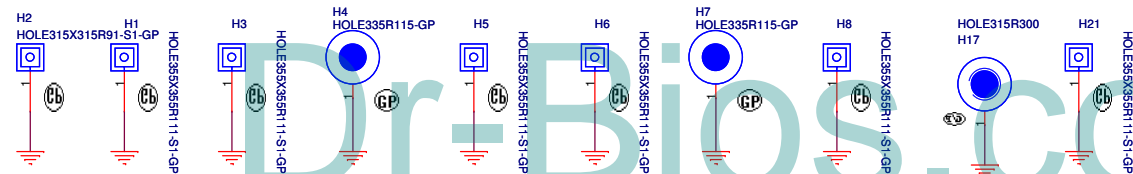
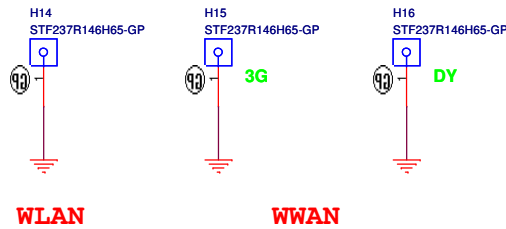
- 3D3V_S0 1 9701
- 3D3V_AUX_S5 1 9702
- 3D3V_S5 1 9703
- 5V_S5 1 9704
- 18.27_PM_PWRBTN# <<< 1 9705
- 6.17.36.71_H_CUPUPWRGD_E >>> 1 9706
- 27.36_S5_ENABLE <<< 1 9707
- 10.17.27.36_A_RST# >>> 1 TP9708

Test Point 放在 Dimm Door 打開可量測處

110218 SB RF Solution



SYSTEM THERMAL



<Core Design>

緯創資通 Wistron Corporation
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Title: **UNUSED PARTS/CAP**

Size A3 Document Number **JE50 SB** Rev **SB**

Date: Friday, April 01, 2011 Sheet 97 of 102

Modify list

65 W: PR4007 -> 187K(64.18735.6DL)
90 W: PR4007 -> 121K (64.12135.6DL)

UMA and PX R5114 ~ R5121 -> 604-ohm (64.60405.6DL)
Diserete -> R5114 ~ R5121-> 499-ohm(64.49905.6DL)

R8332 stuff 1K for Mannhatton VGA
stuff 5.1K(64.51015.6DL) for Vancouver VGA

if use LVDS L8711,L8709 stuff 0-ohm 0603
if use LVDS L8701,L8708 stuff bead 0603
if use EDP L8711,L8709 stuff bead 0603 ohm
if use EDP L8701,L8708 stuff 0-ohm 0603

<Core Design>

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Title			
Change History			
Size	Document Number		Rev
A4	JE50 SB		SB
Date:	Friday, April 01, 2011	Sheet 98 of	102

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POWER SEQUENCE

<Core Design>

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		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
POWER SEQUENCE			
Size	Document Number		Rev
A4	JE50 SB		SB
Date:	Friday, April 01, 2011	Sheet 99	of 102

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