

Compal Confidential

NAL00 Schematics Document

AMD L310/L110 Processor with RS780MN/SB710/M92-S2/S3 LP

2009-04-24

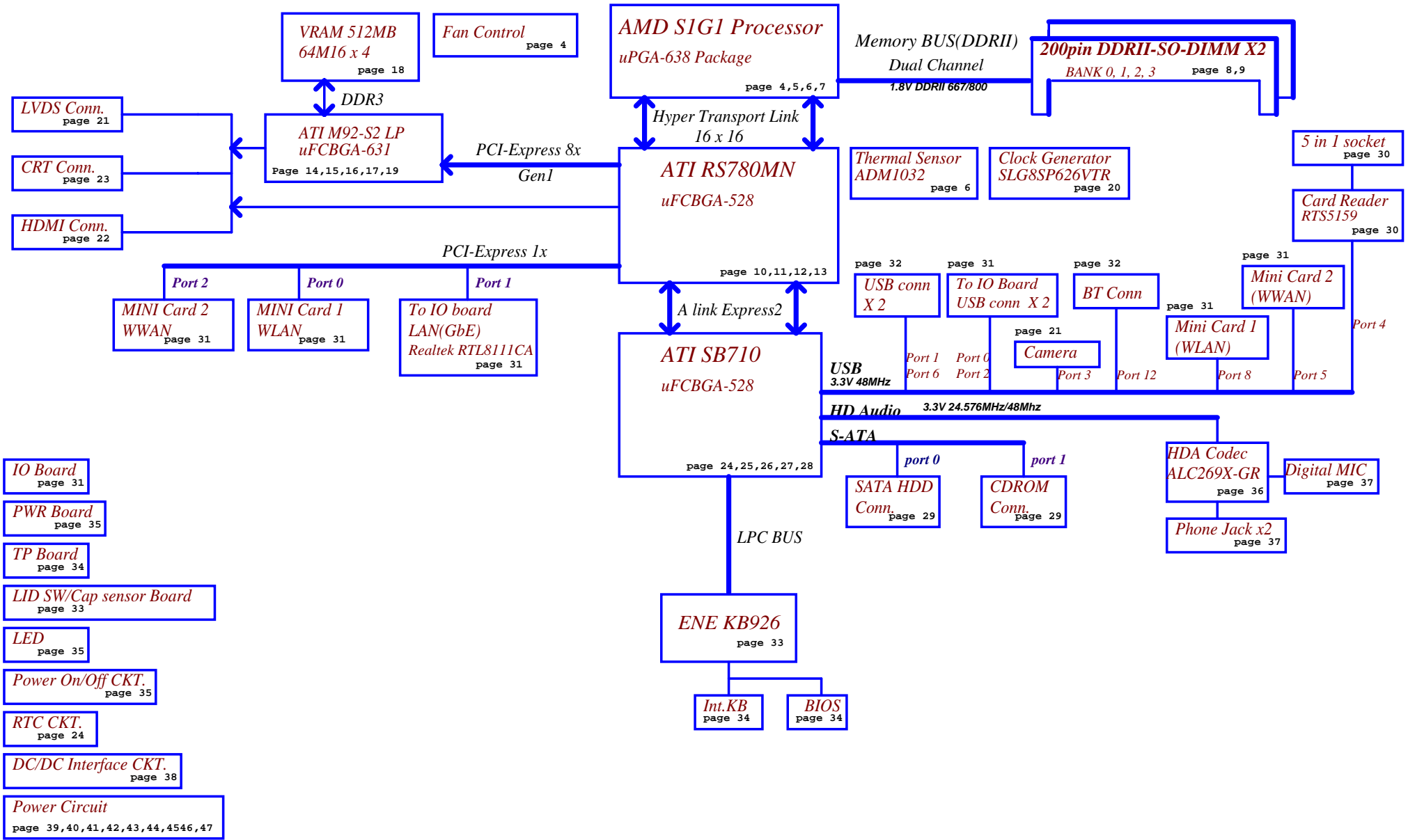
REV: 0.2

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Model Name : NAL00



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+NB_CORE	1.0V switched power rail	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.90-0.95V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Smart Battery	0001 011X b	16H	98H
ADI ADM1032 (CPU)	1001 100X b		98H
SB-Temp Sensor			9CH

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (CPU)	1001 100X b	98H
			SB-Temp Sensor		9CH

EC SM Bus2 address

SB710 SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2	New card	
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

SB700 SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

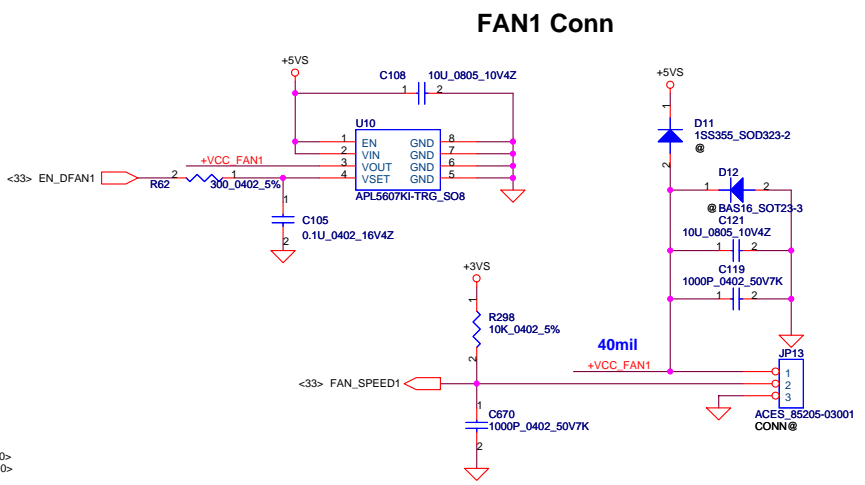
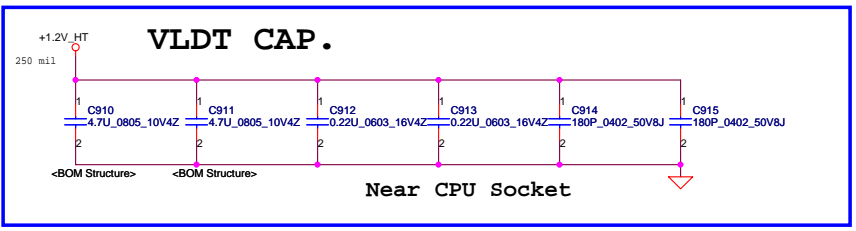
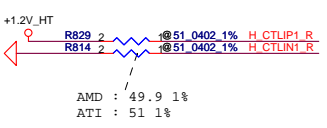
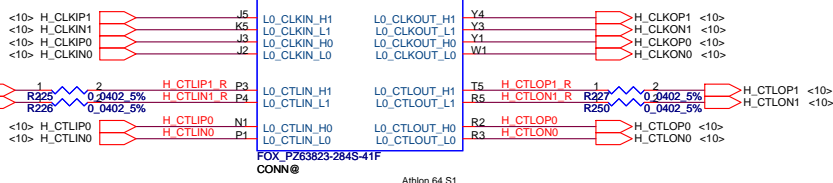
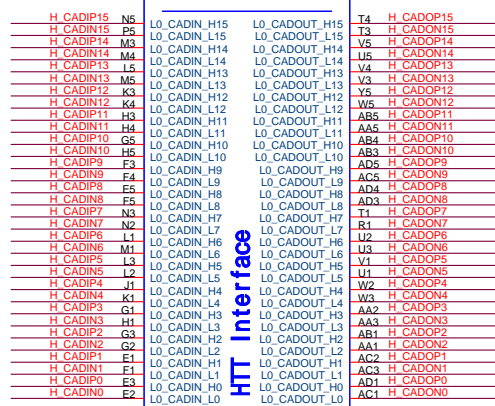
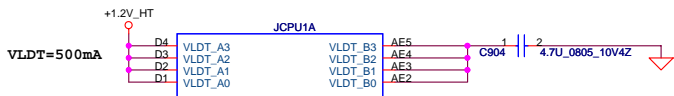
BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@
UMA_HDMI	UMA_H@
Side port	SP@
JM51	JM@
HM52	HM@

	SB700	SB700	RS780MN	DISPLAY OUTPUT
	PX_GPIO0	PX_GPIO1	PX_GPIO2	
Function Description	dGPU_Reset	dGPU_PWR_Enable	PX Mode Switch	
IGP only mode	X	X	X	
PowerXpress mode	H : Enable	H : Enable	L : IGPU(DC) / H : dGPU(AC)	LVDS / CRT

	KB926					
	PX_GPIO1	PX_GPIO2	PX_+3VS	PX_+1.8VS	PX_+VGA_CORE	PX_GPIO2_NB
Function Description	Enable +1.1VS_PX	PX MODE SWITCH	Enable +3VS_DELAY	Enable +1.8VS_PX	Enable +VGA_CORE	Trigger from SB
IGP only mode	X	X	X	X	X	X
PowerXpress mode	H : Enable	Reserved	H : Enable	H : Enable	H : Enable	Reserved

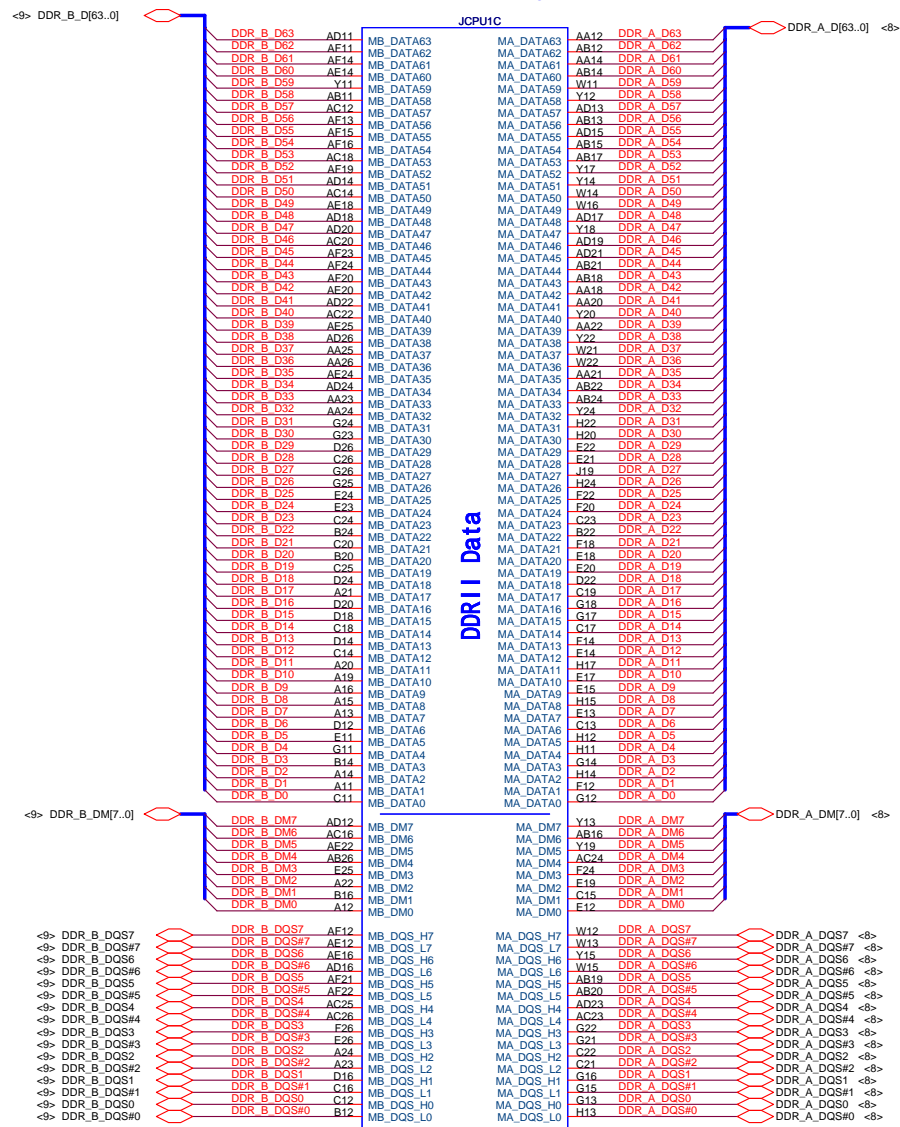
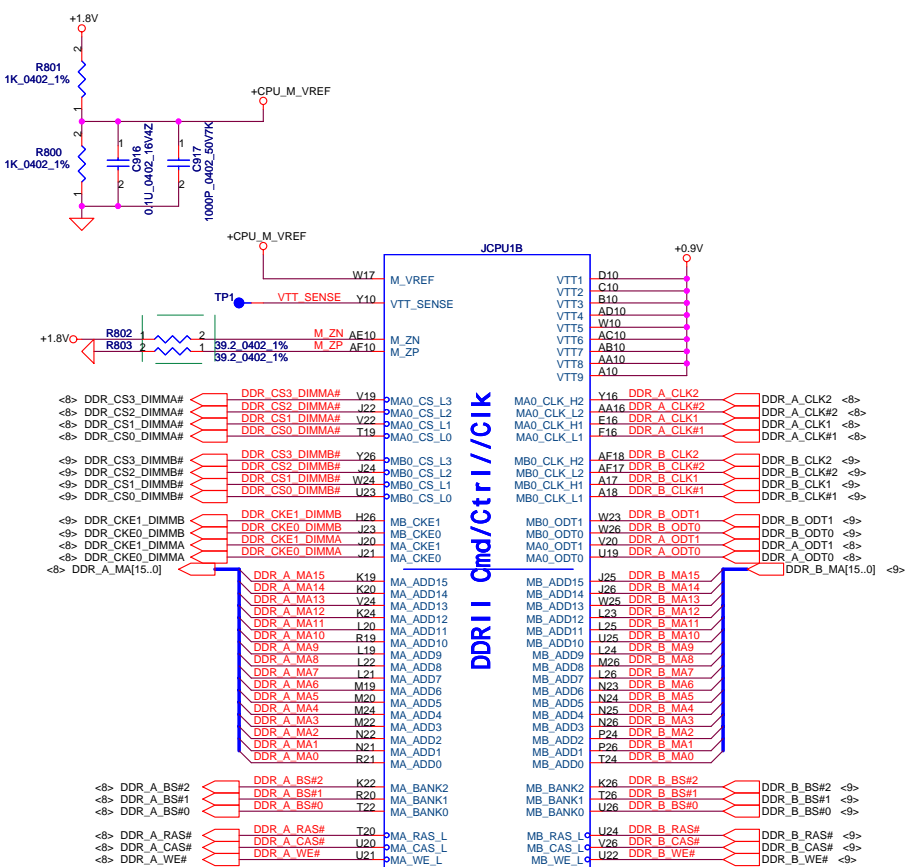
	KB926	
	PX_GPIO1_SB	
Function Description	Trigger from SB to Enable (PX_GPIO1/PX_+3VS/PX_+1.8VS/PX_+VGA_CORE)	
IGP only mode	X	
PowerXpress mode	H : Enable	

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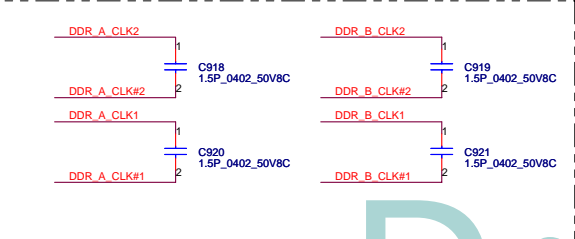


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Processor DDR2 Memory Interface



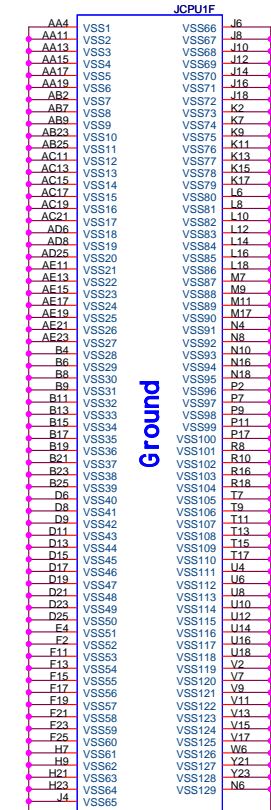
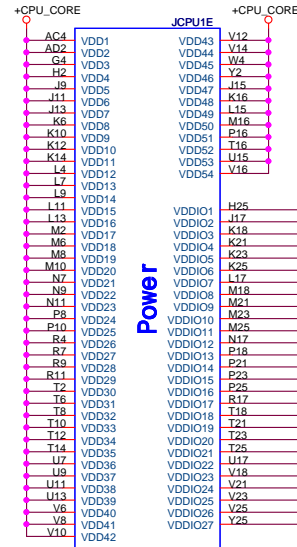
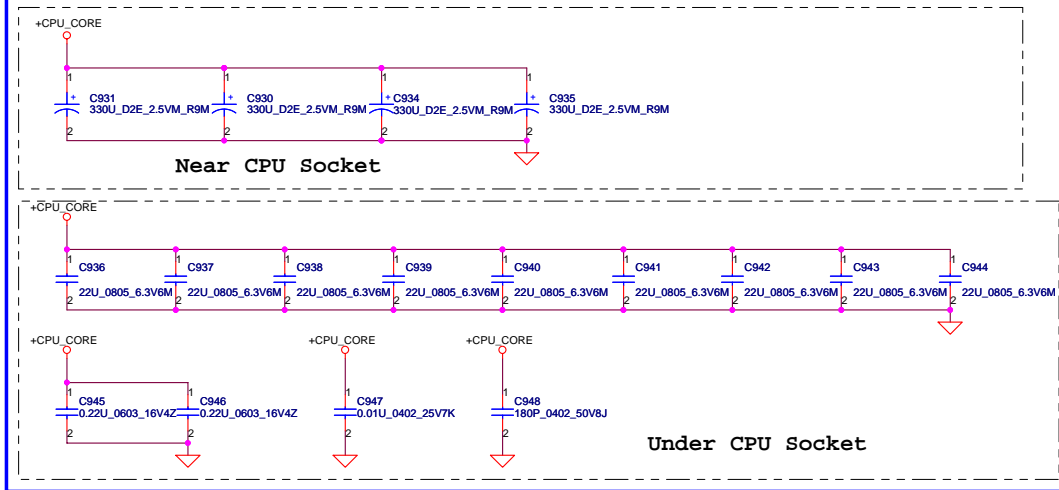
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



CONN@ FOX_P263823-284S-41F
Athlon 64 S1
Processor Socket

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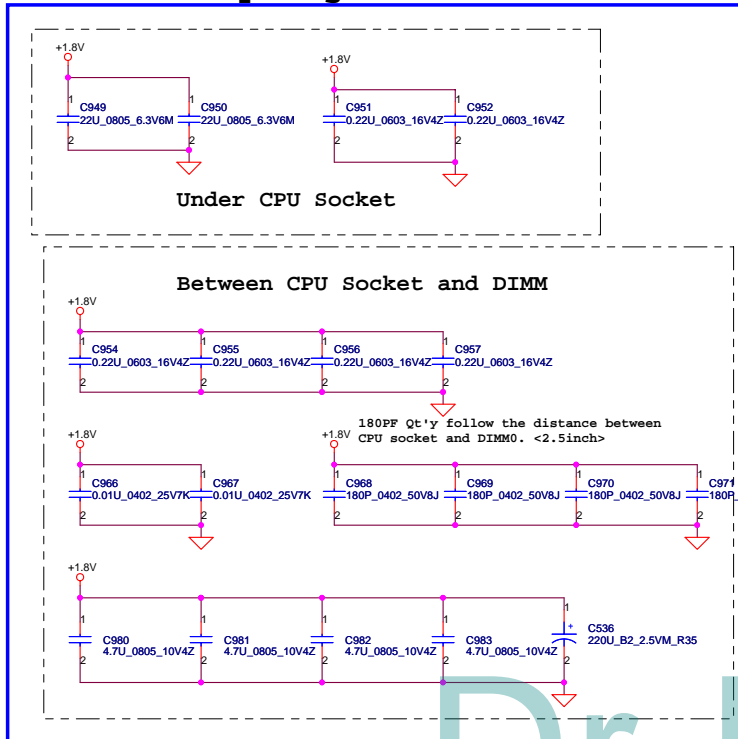
VDD(+CPU_CORE) decoupling.



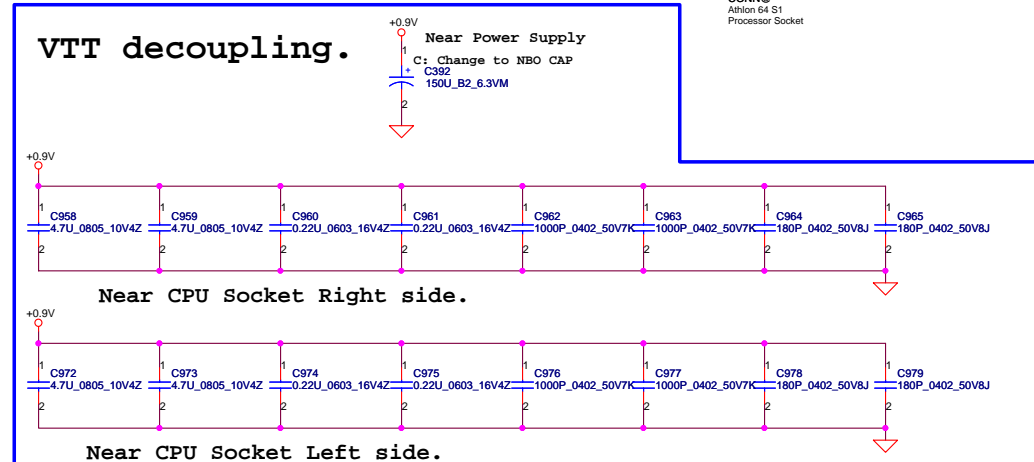
FOX_P263823-284S-41F
CONN@
Arlton 64 S1
Processor Socket

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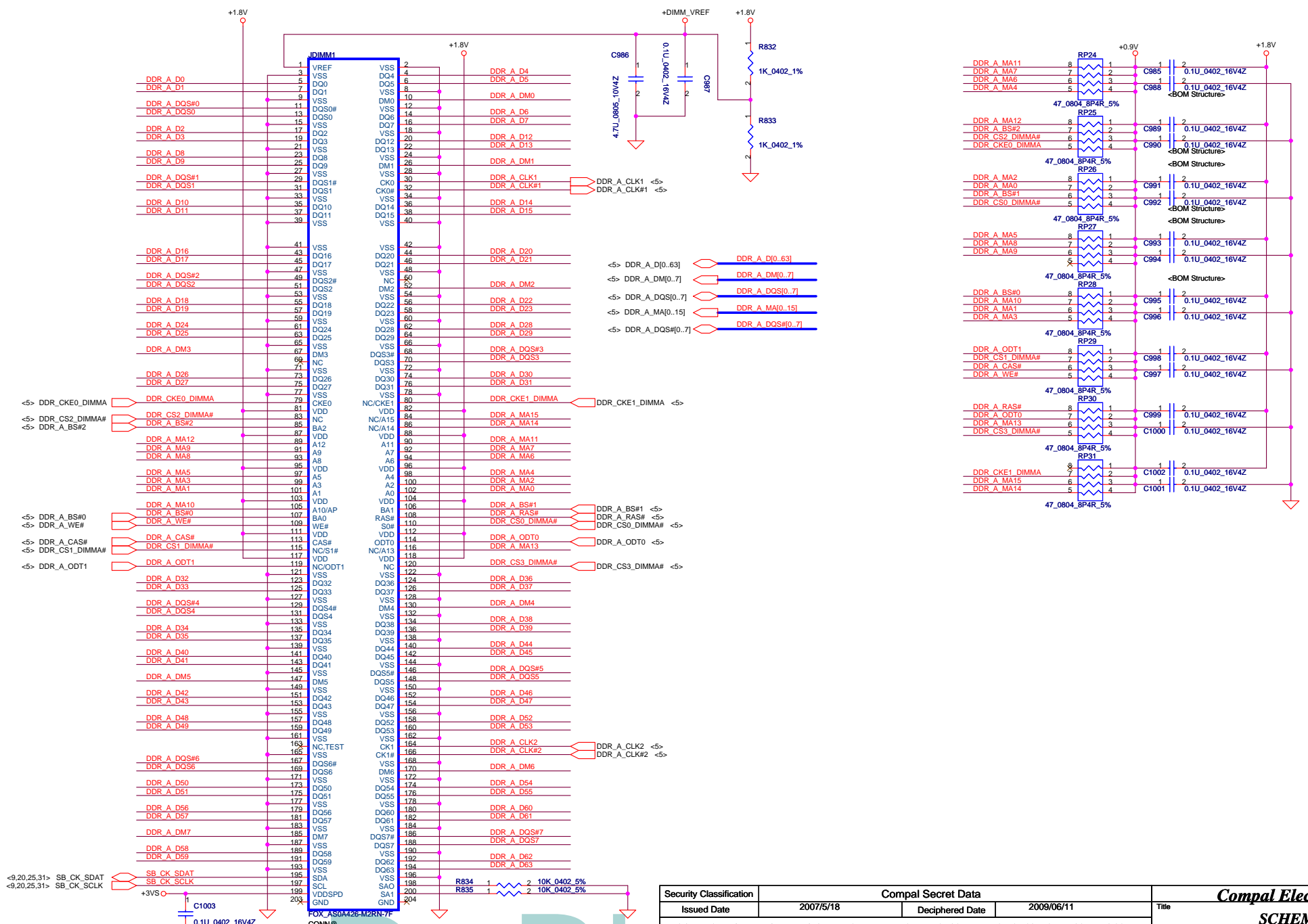
VDDIO decoupling.



VTT decoupling.

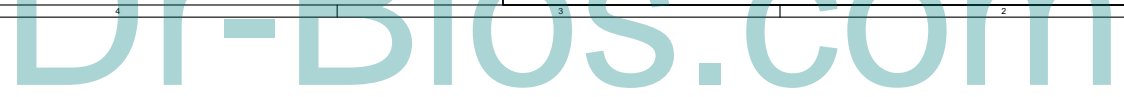


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JAWDO used
DIMM1 REV H:5.2mm (BOT)

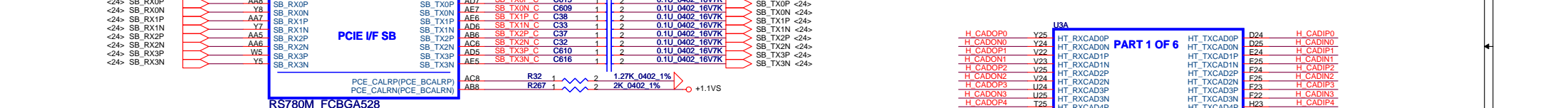
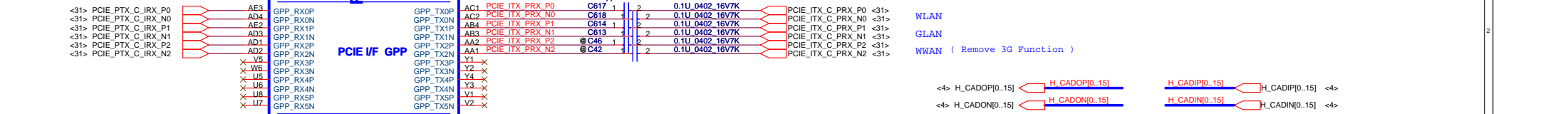
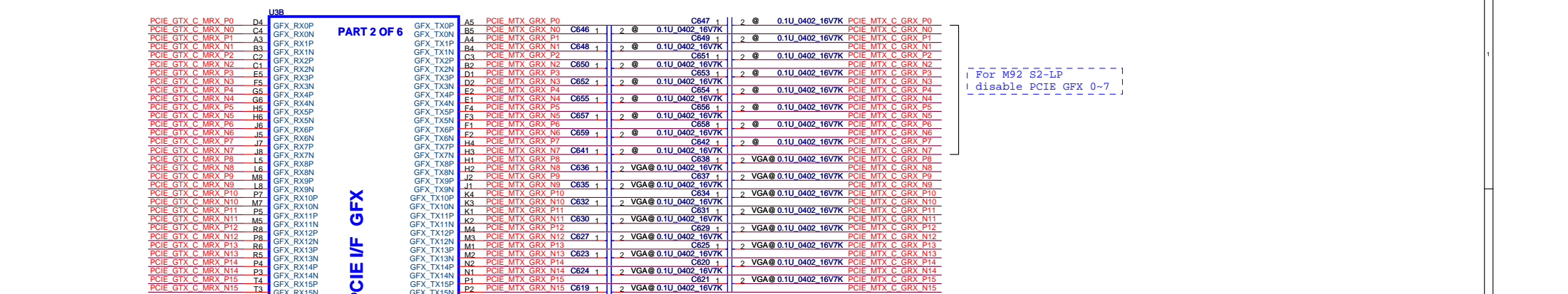
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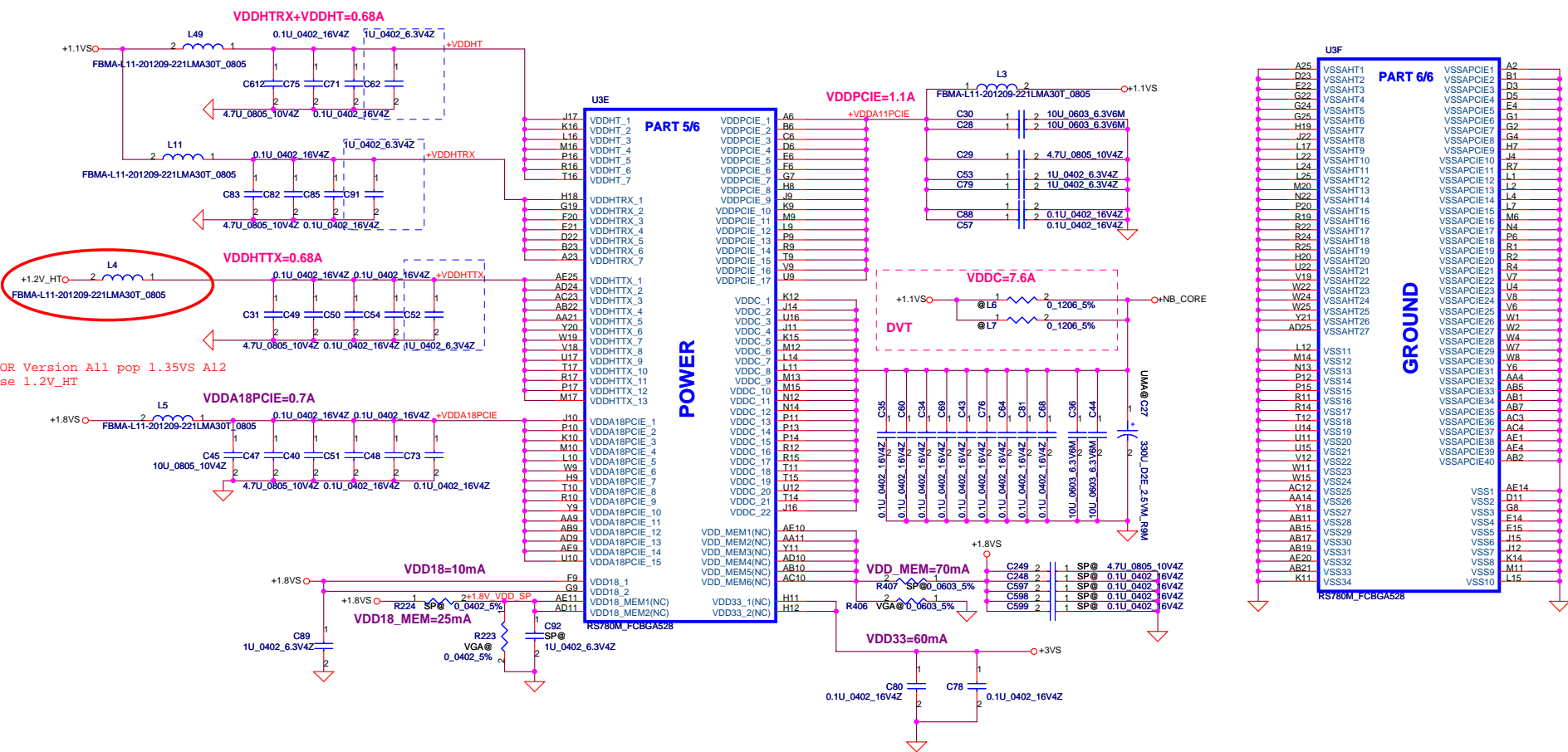


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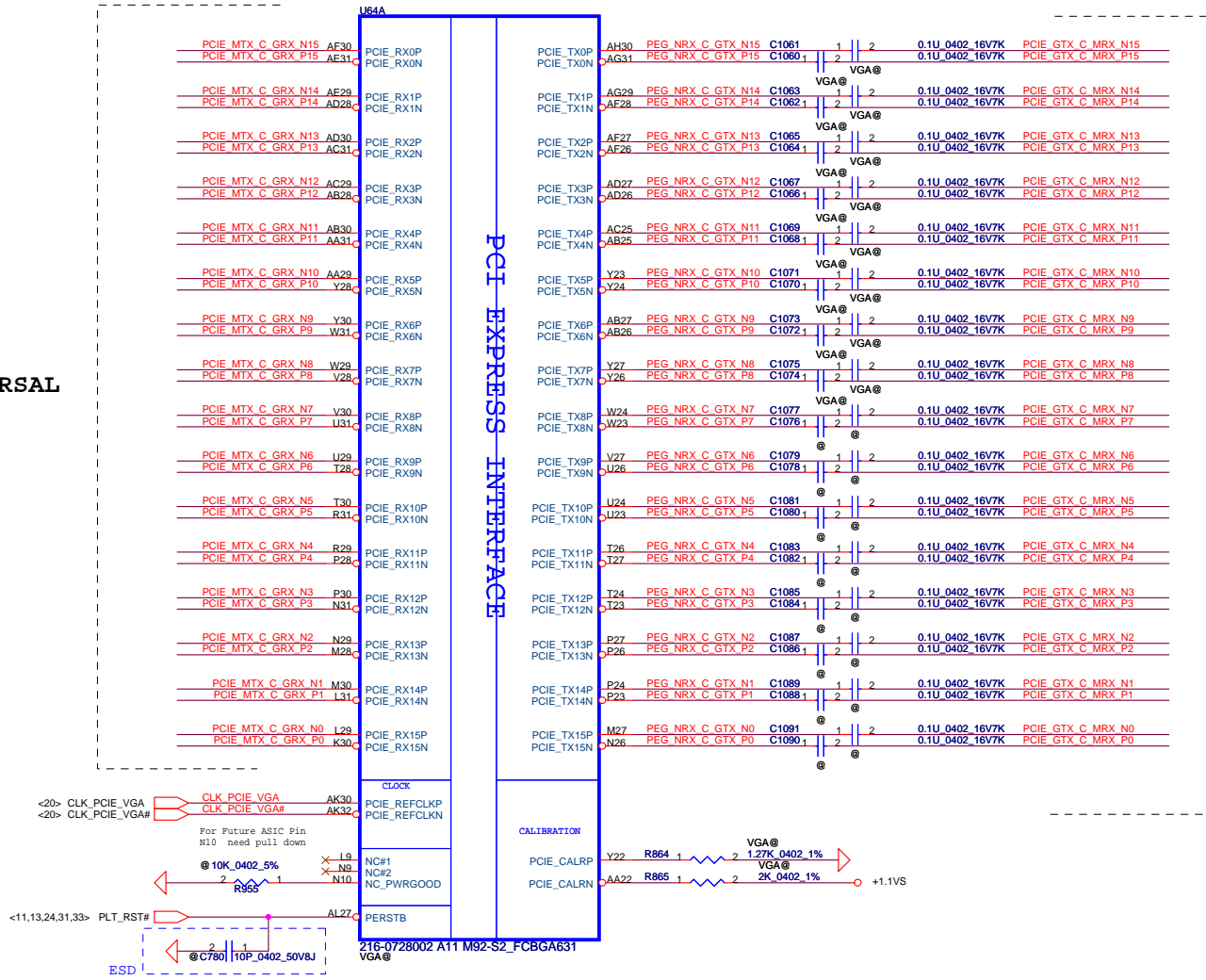




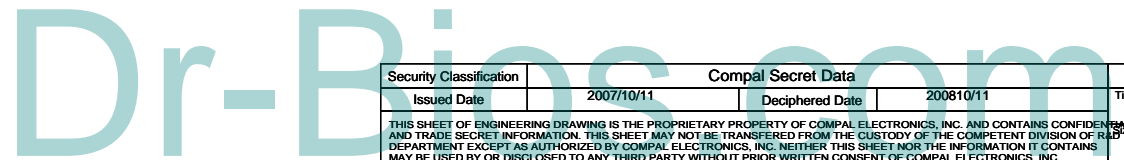
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PCIE LANE REVERSAL

PCIE LANE REVERSAL

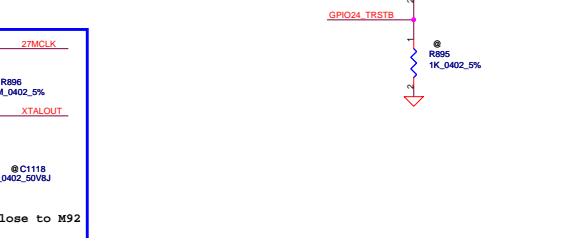
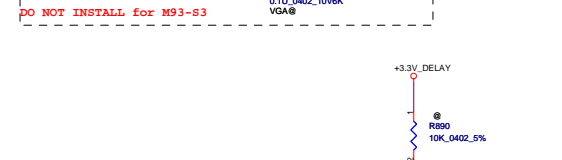
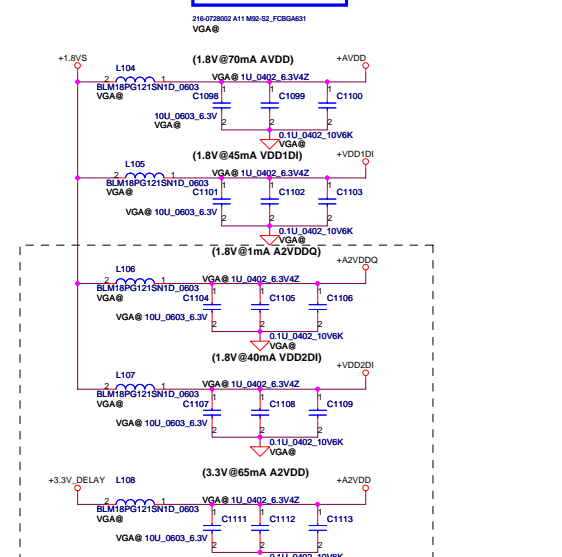
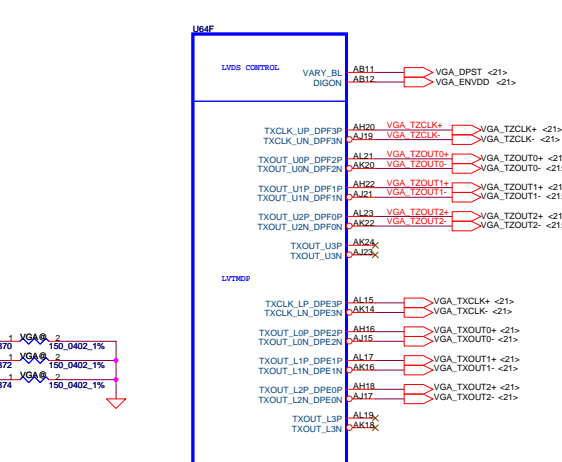
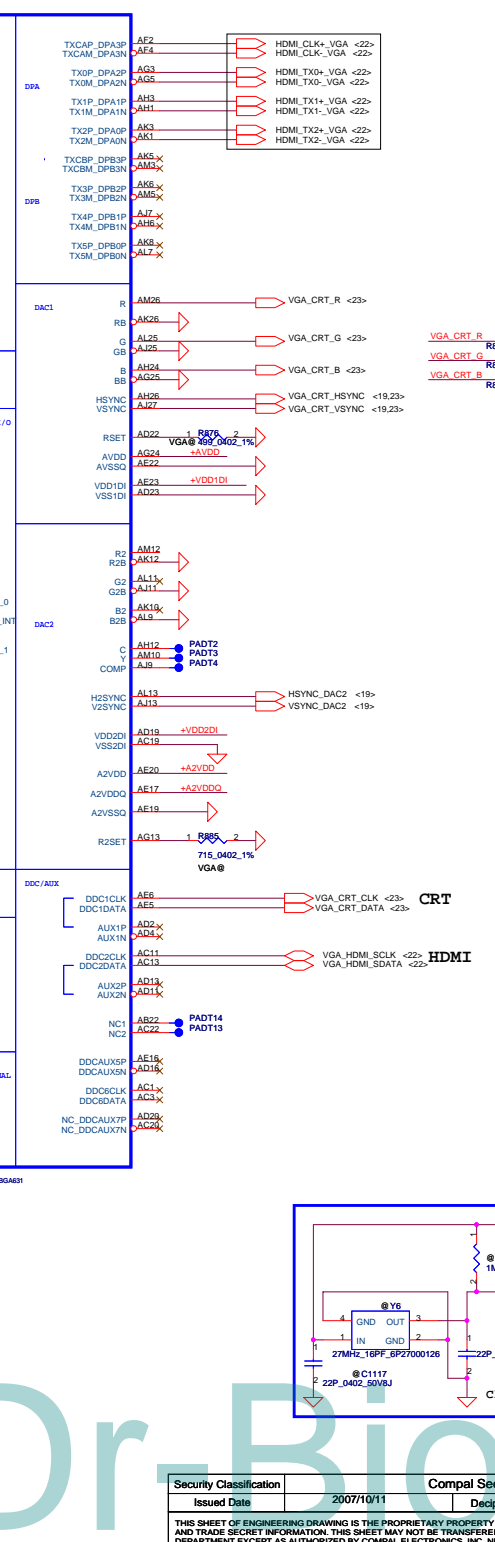
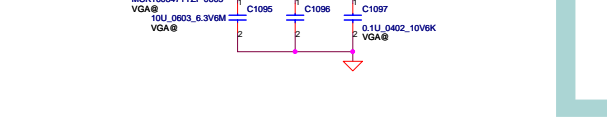
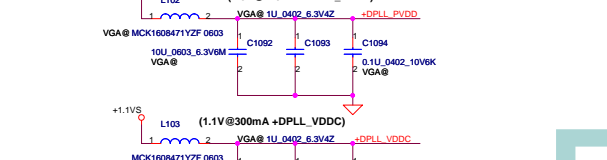
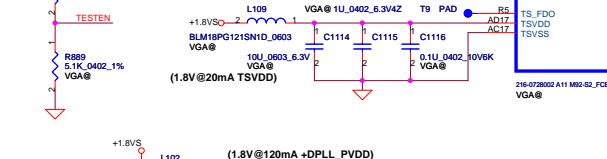
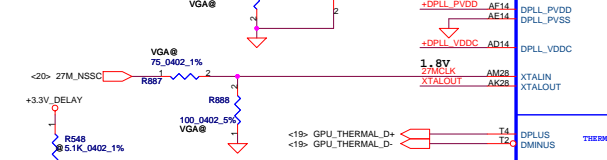
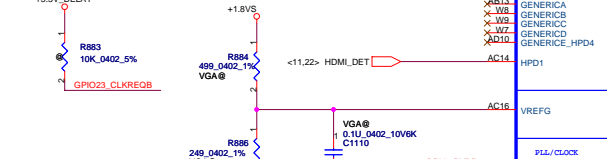
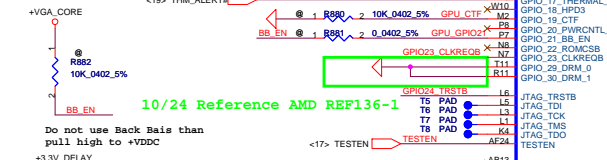
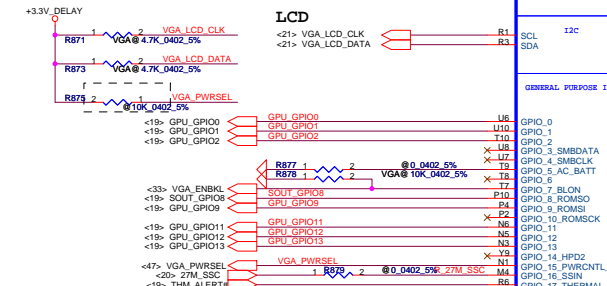
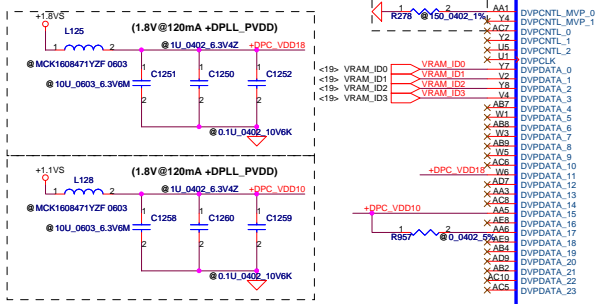


For M92 S2-LP
 disable PCIE GFX 0~7

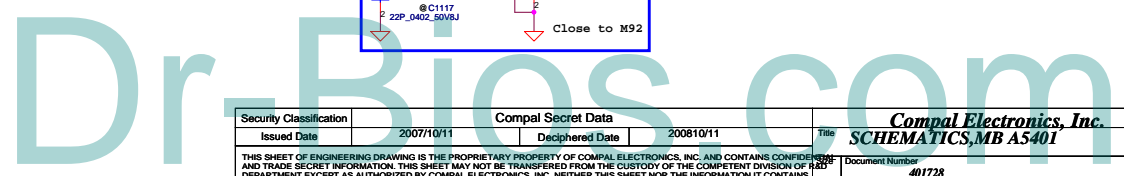


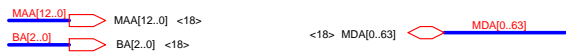
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For M92-S2: DO NOT Install any Component in this Box.

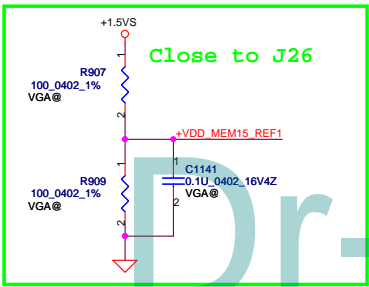
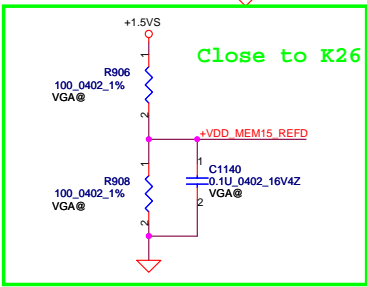
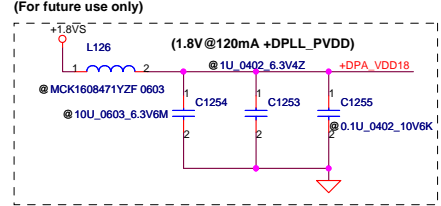
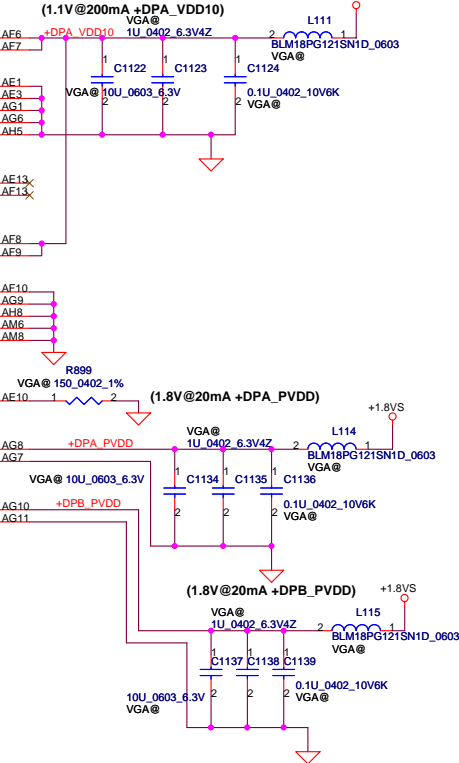
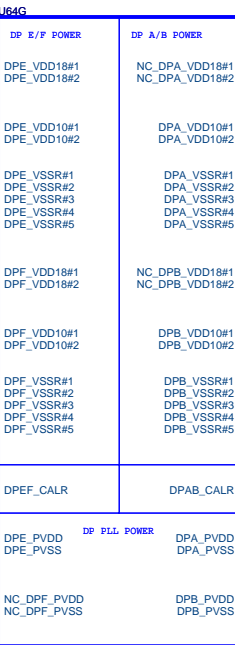
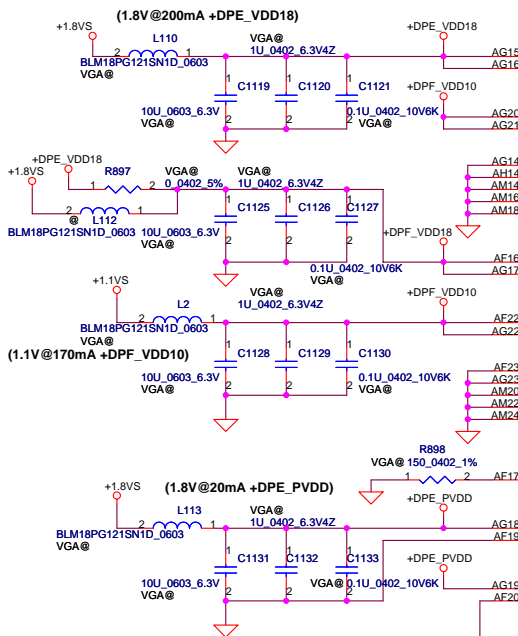
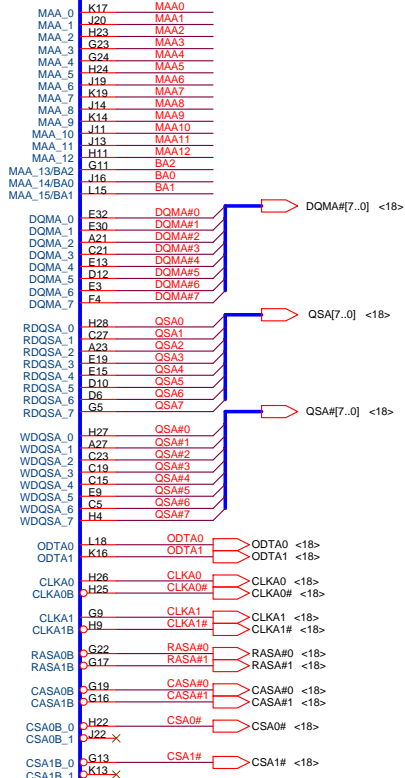
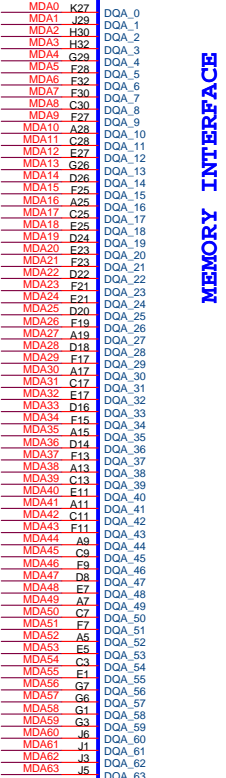


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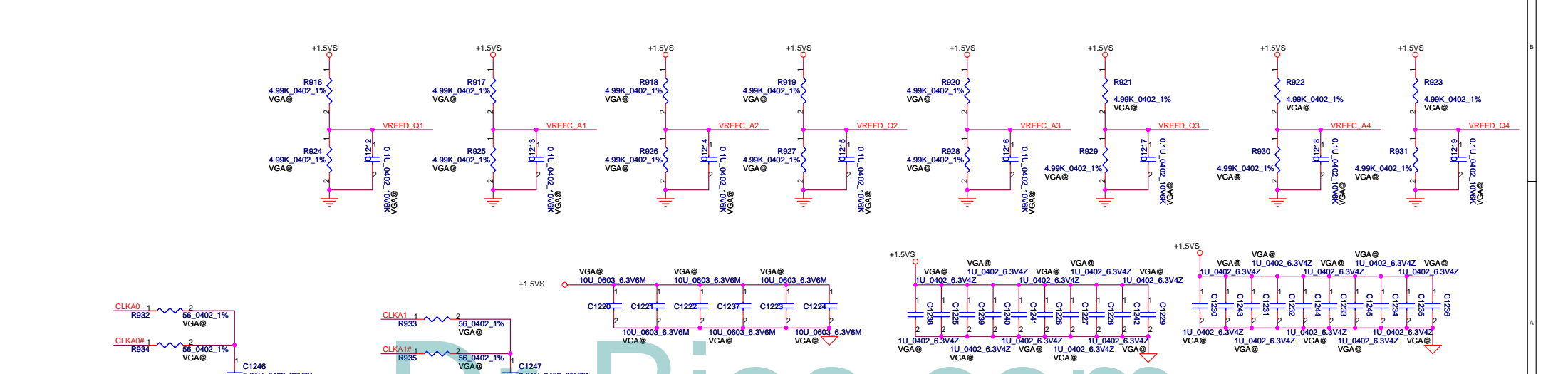
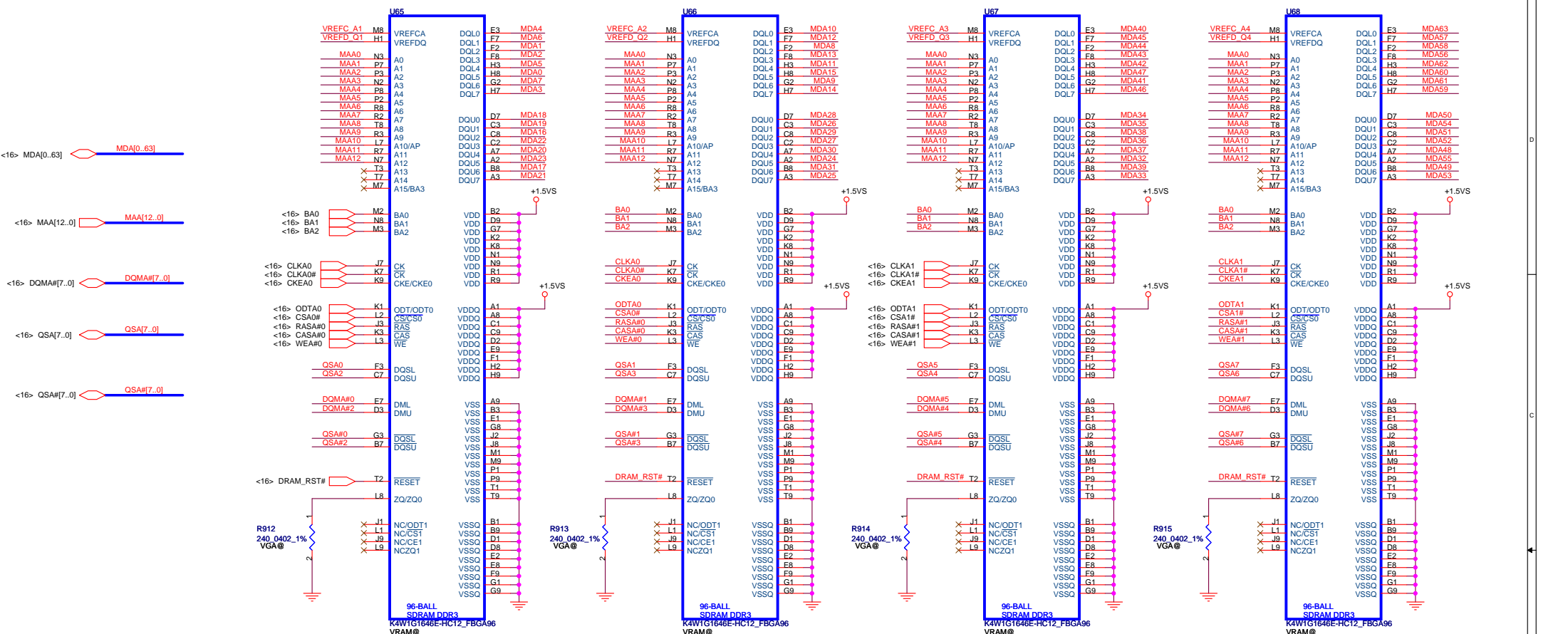




U64C

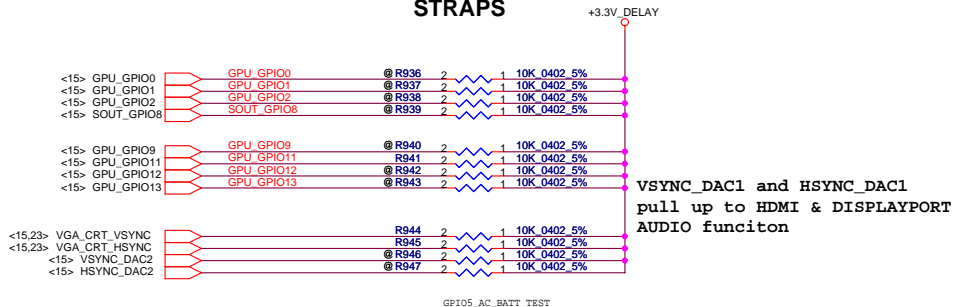


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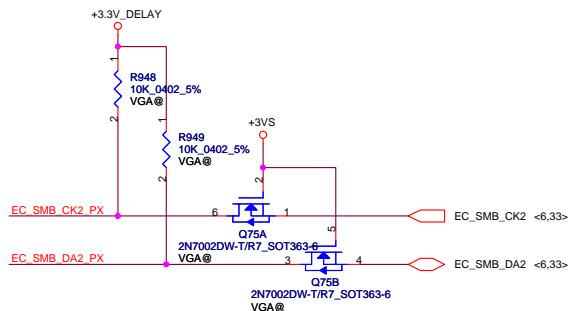


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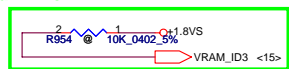
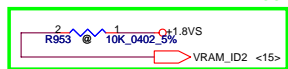
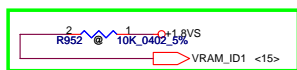
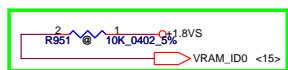
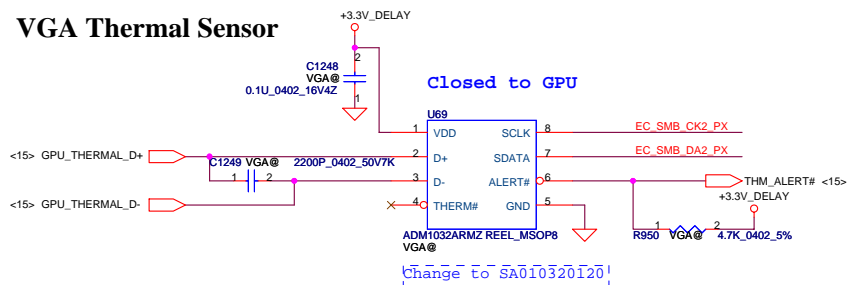
STRAPS



VSYNC_DAC1 and HSYNC_DAC1
pull up to HDMI & DISPLAYPORT
AUDIO function



VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		1
ROMIDCFG(2:0)	GPIO[13:11]	BIF_RX_PLL_CALIB_BP	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYN	ENABLE EXTERNAL BIOS ROM	0
SMS_EN_HARD	H2SYN	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0
CCBPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
AUD[1]	HSYN	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X
AUD[0]	VSYN		

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

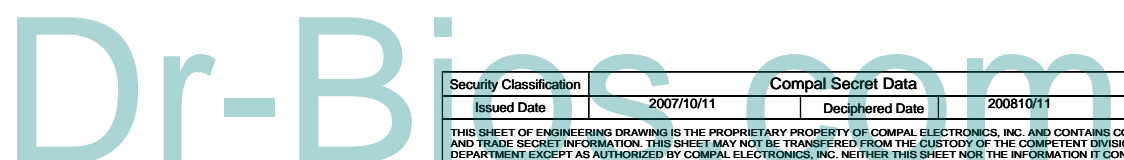
H2SYN GENERICC

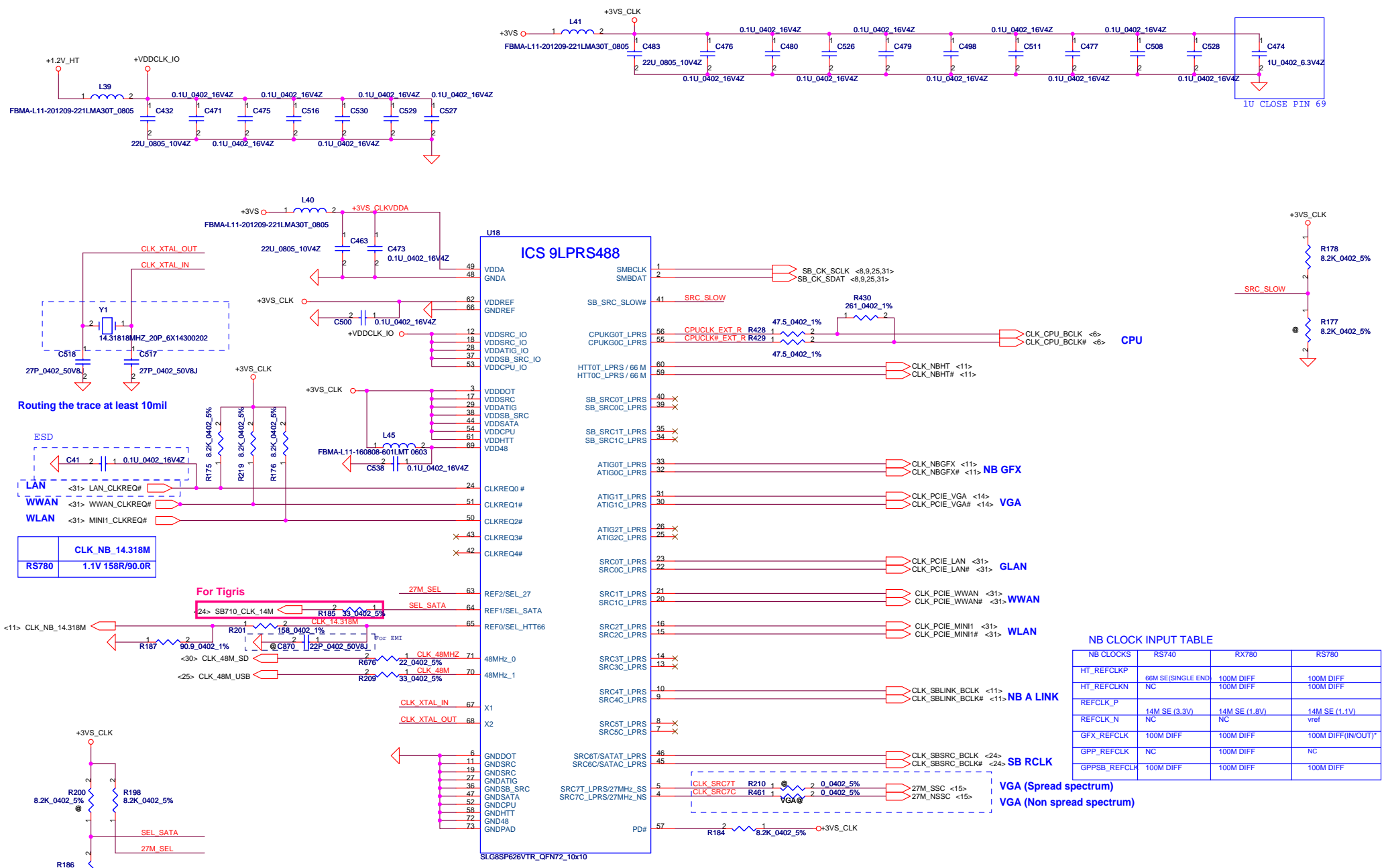
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN

VRAM_ID0=VRAM_ID0_0
VRAM_ID1=VRAM_ID1_1
VRAM_ID2=VRAM_ID2_2
VRAM_ID3=VRAM_ID3_3

STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (3,2,1,0)	M92 S2-LP	JM51_PU	512MB(x4)	Samsung 64Mx16 1.5V	SA000035700	0 0 0 0
			JM51_PU	512MB(x4)	Hynix 64Mx16 1.5V	SA000032400	0 0 1 0
							0 0 1 1
							0 1 0 0
							0 1 0 1





1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN
 2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN

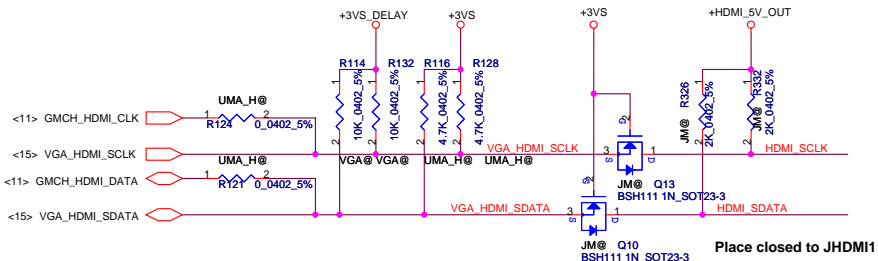
SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1*	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

27M_SEL	1	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC 7 output

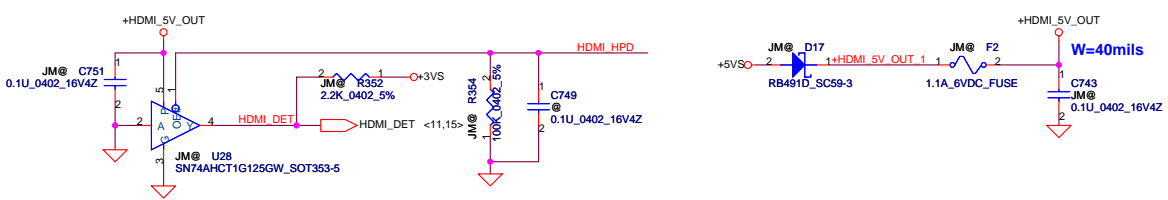
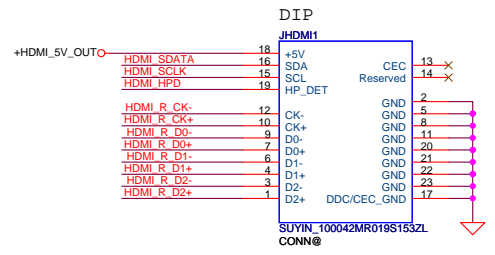
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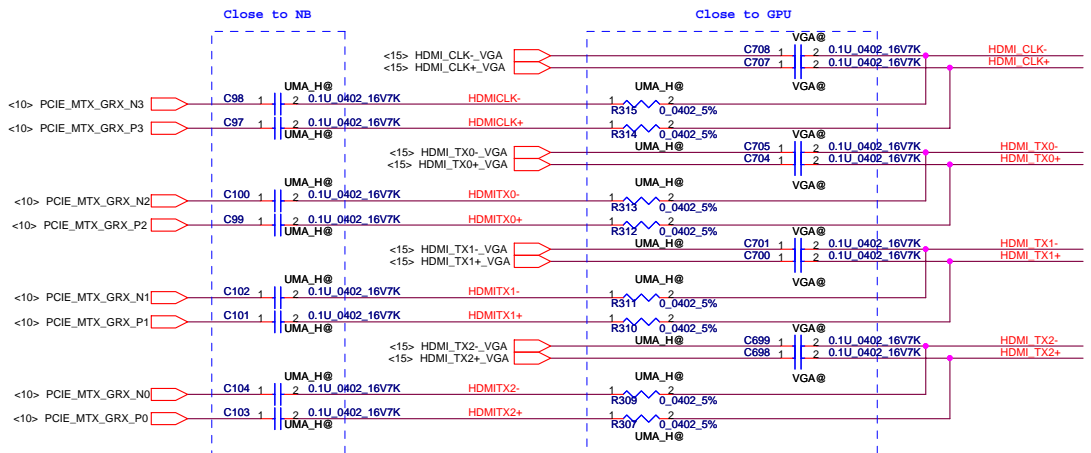
DDC to HDMI CONN



Place closed to JHDMI1

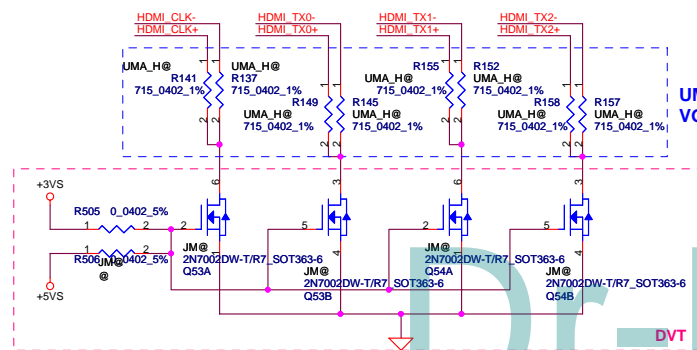
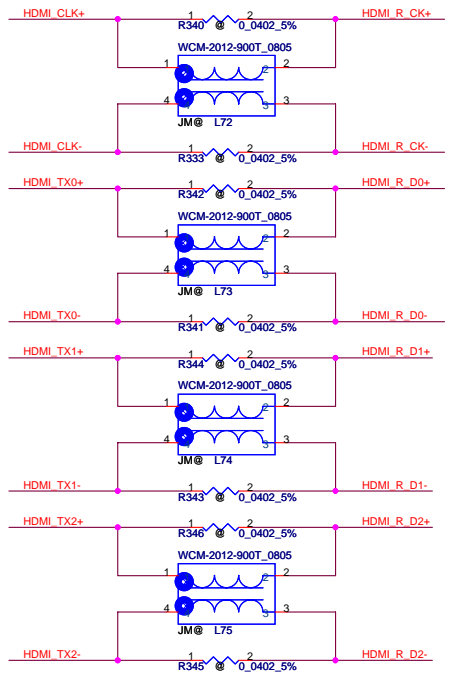


W=40mils



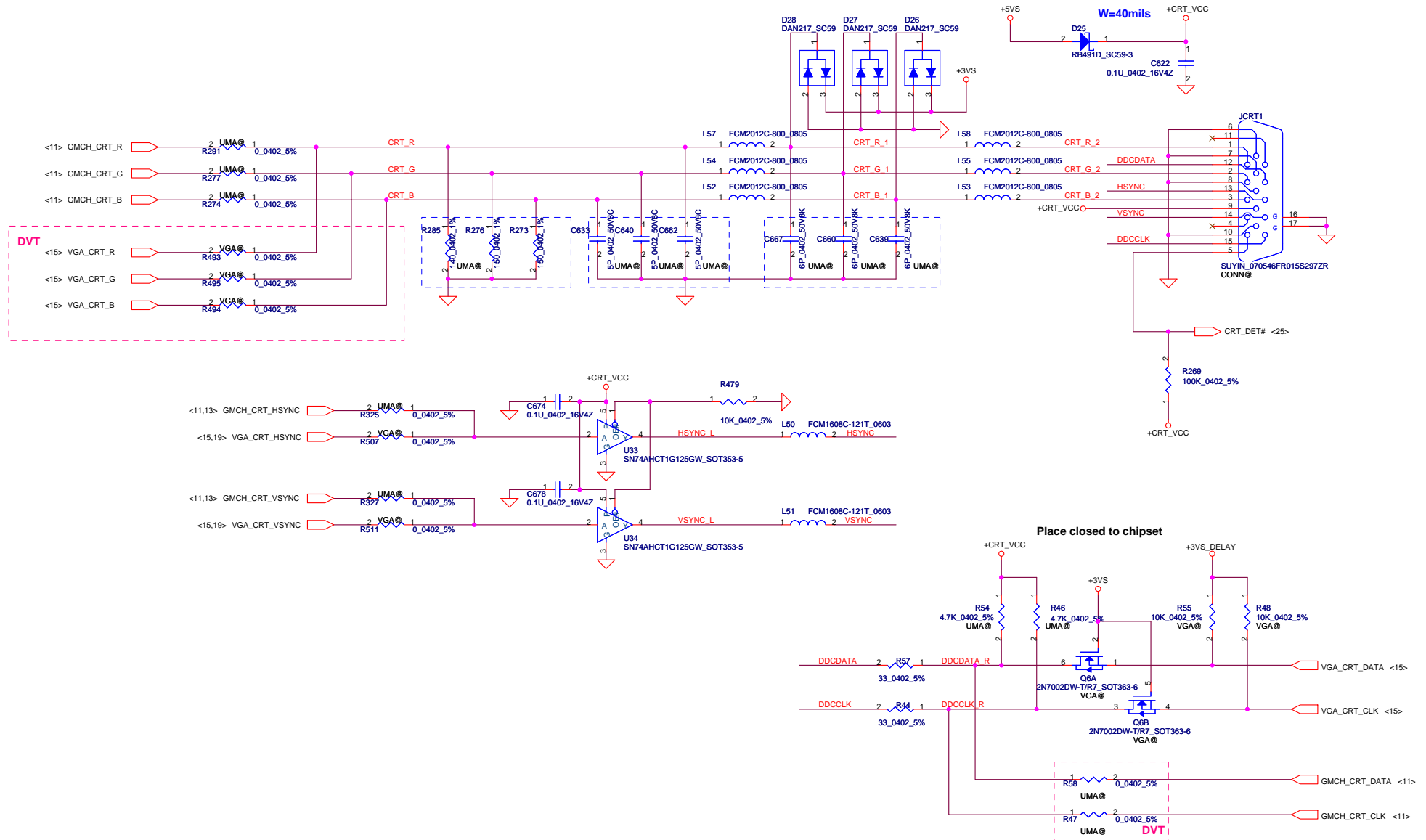
Update (For Puma / Tigris default value)

UMA use 715 ohm
VGA use 499 ohm

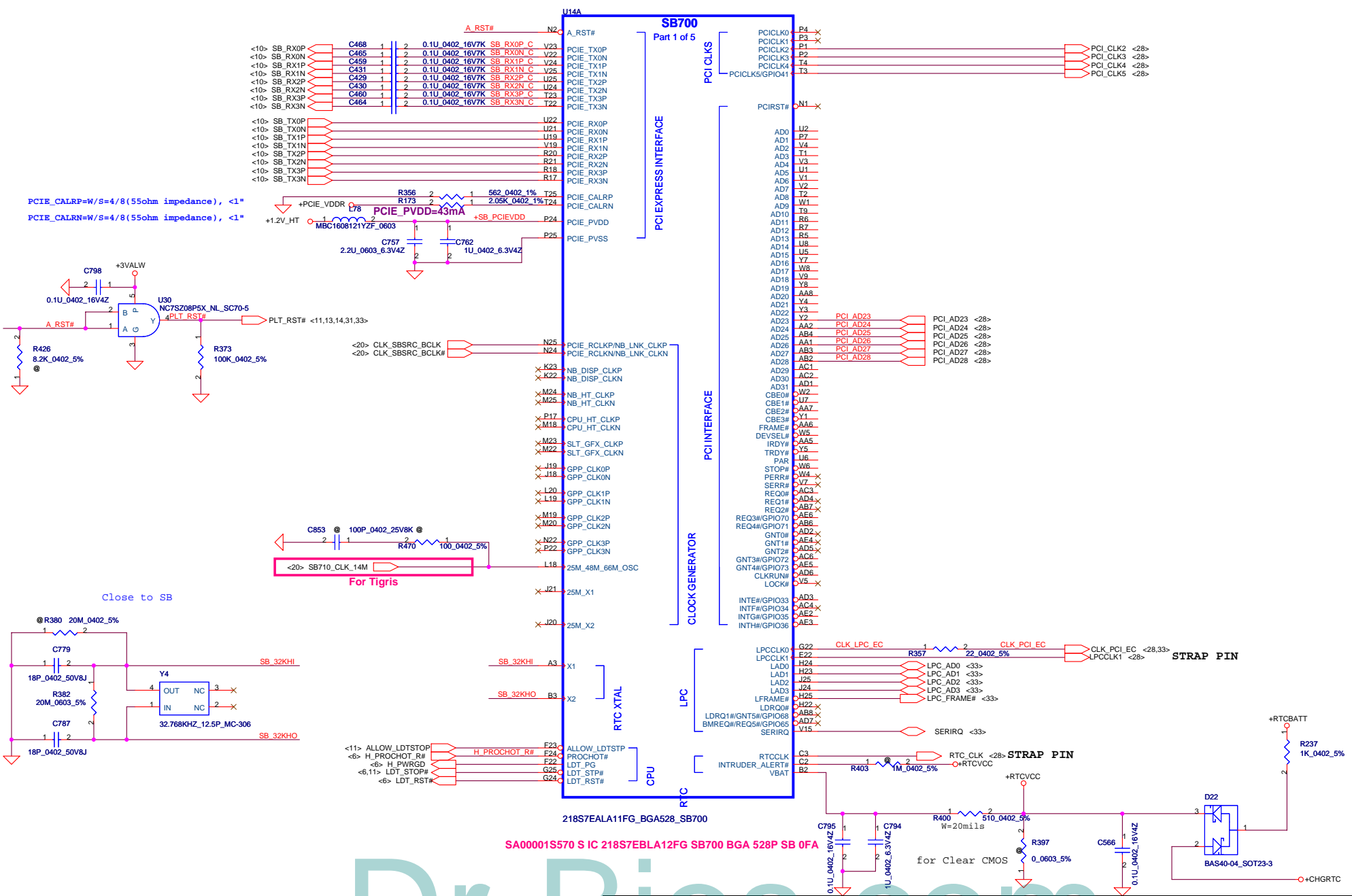


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CRT CONNECTOR



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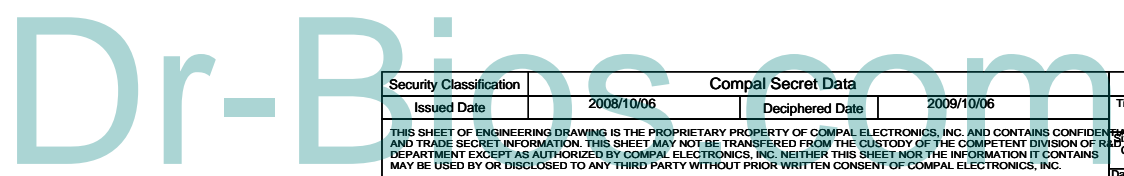
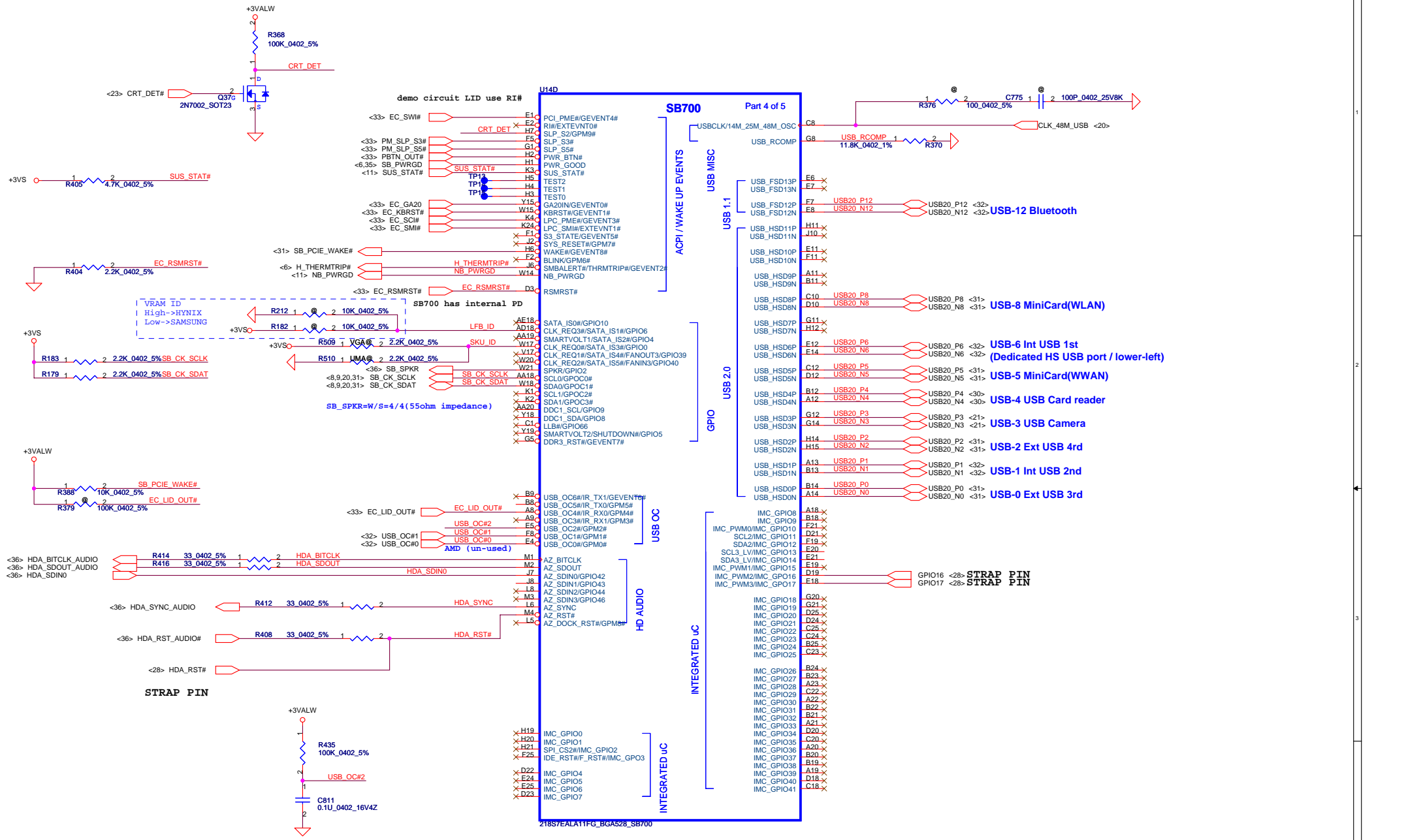
PCIE_CALRP=W/S=4/8(55ohm impedance), <1"
 PCIE_CALRN=W/S=4/8(55ohm impedance), <1"

Close to SB

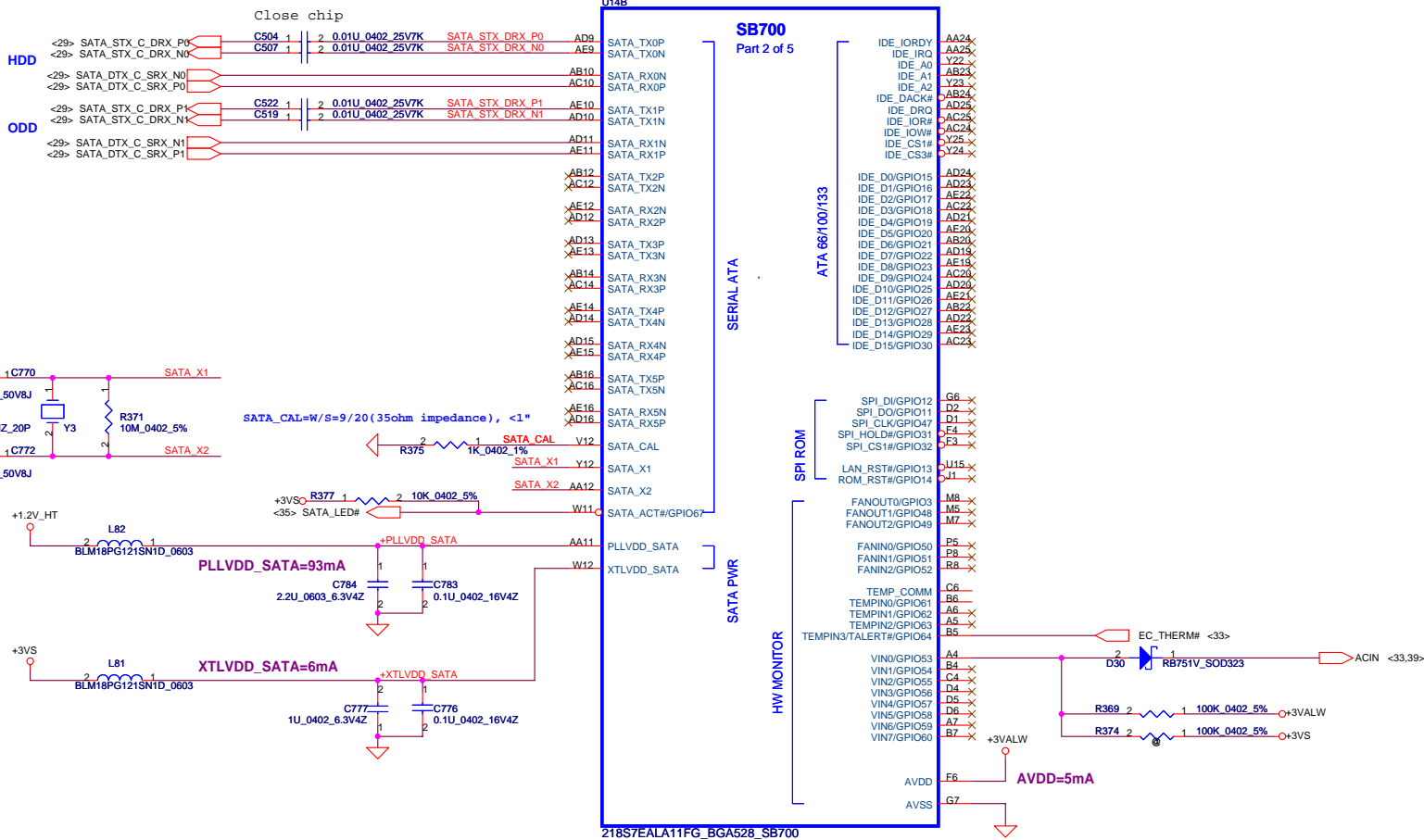
For Tigris

SA00001S570 S IC 218S7EBLA12FG SB700 BGA 528P SB 0FA

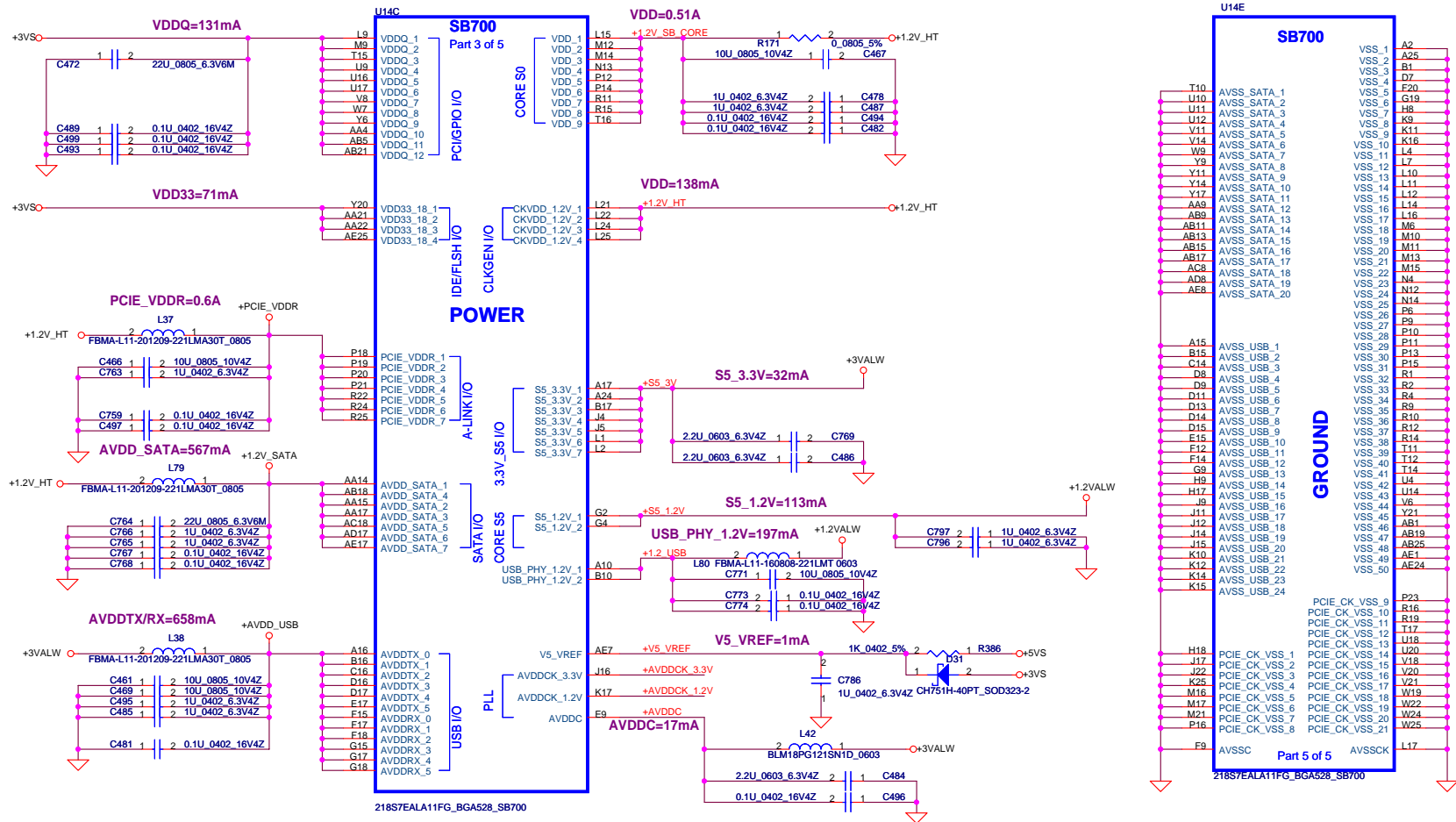
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Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller

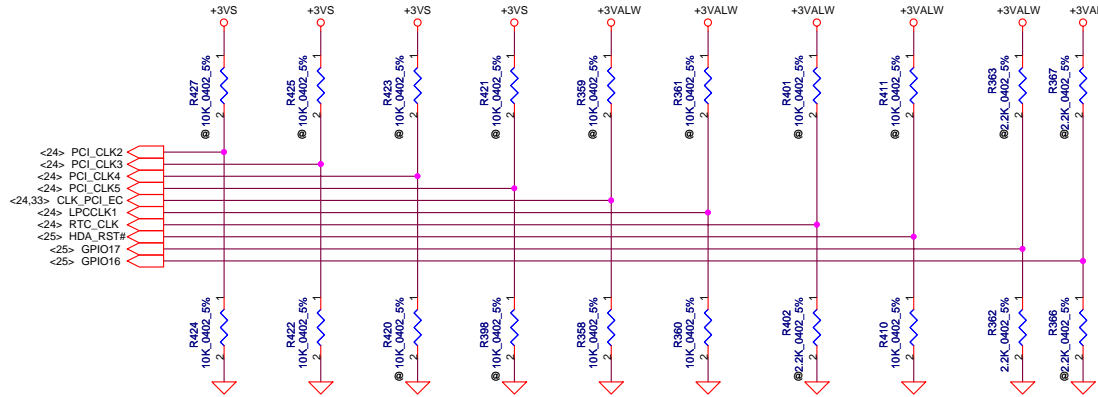


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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

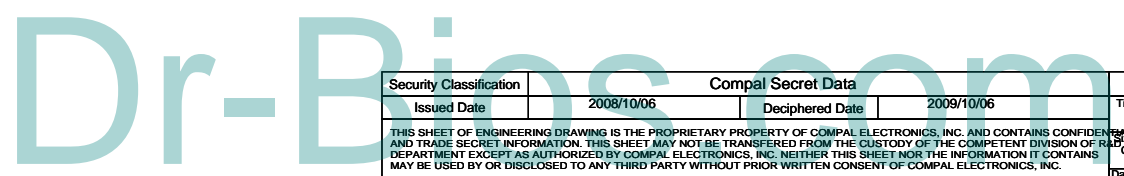
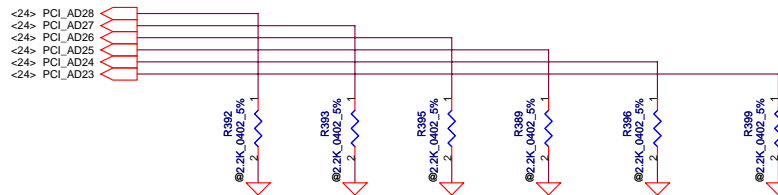
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved L,L = SPI ROM LL = FWH ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (SB700) L,NC = LPC ROM (SB710)



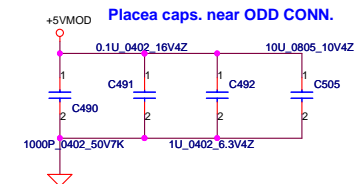
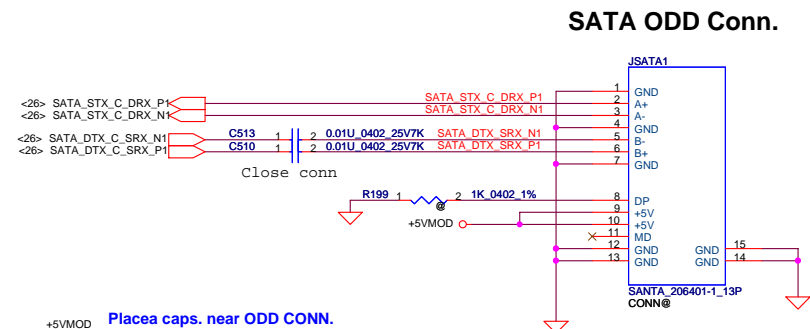
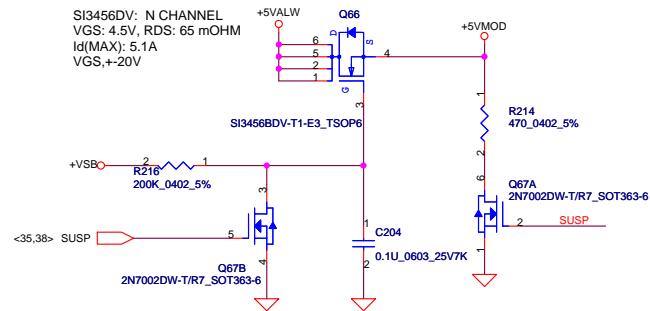
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

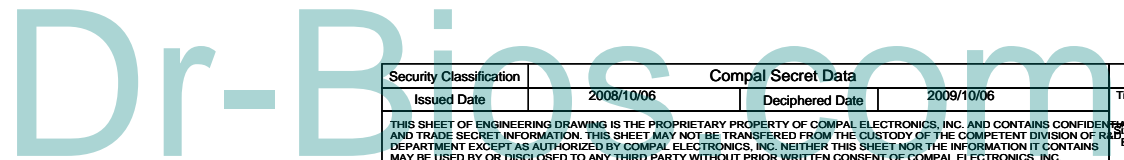
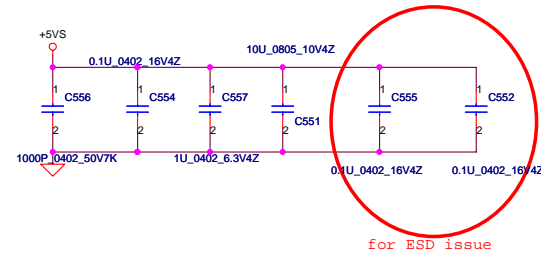
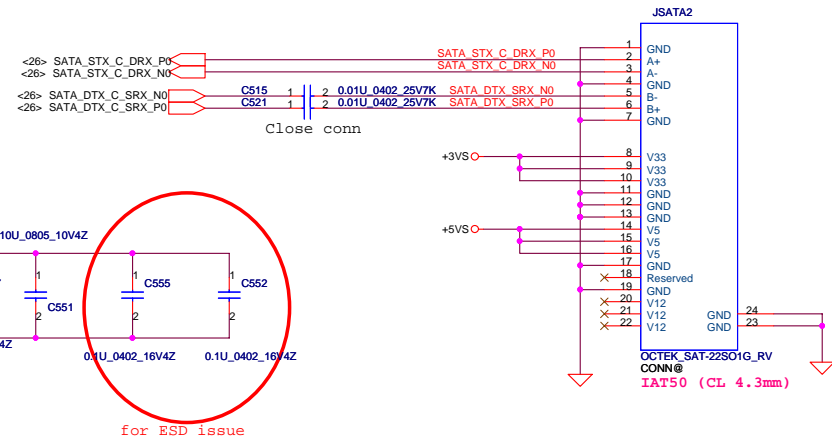
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



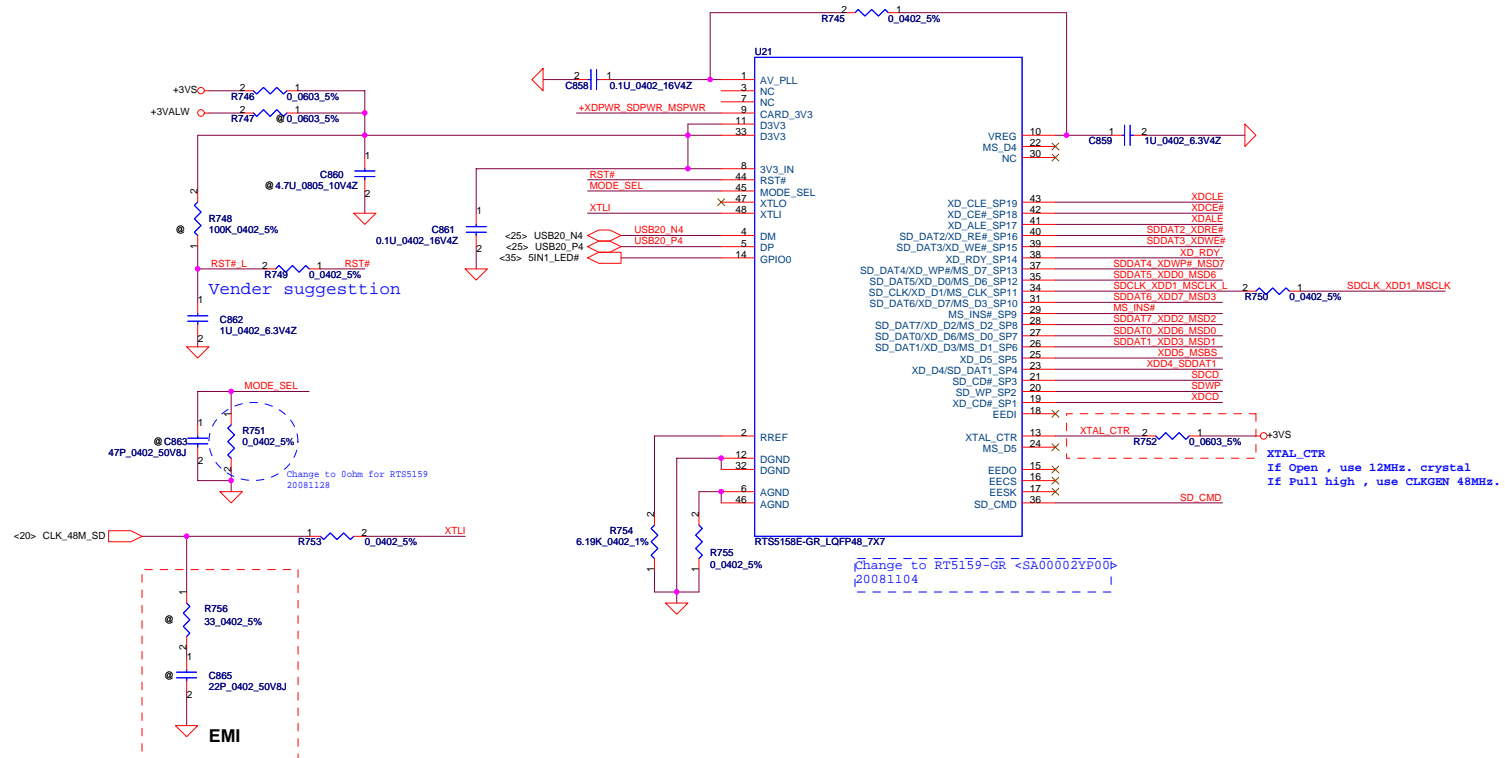
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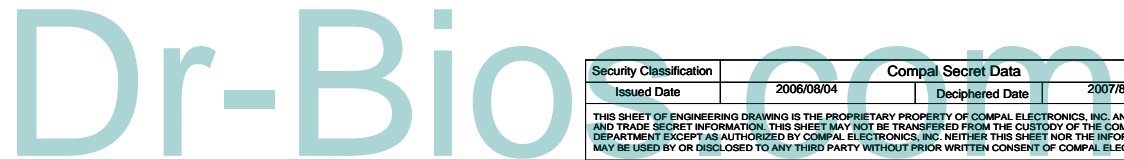
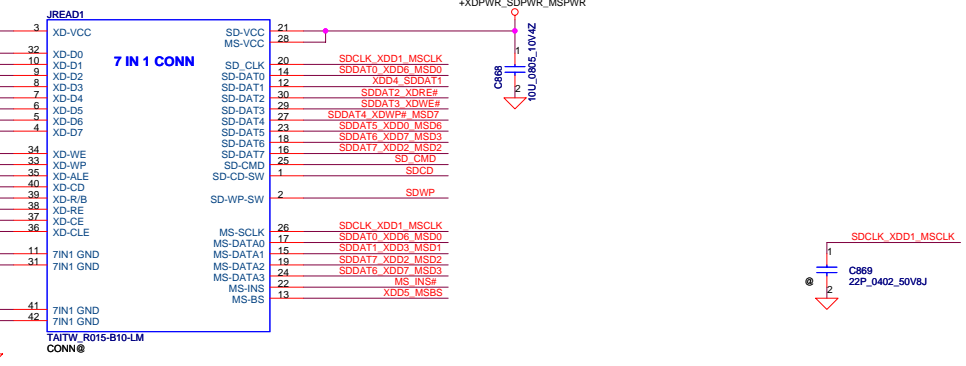
SATA HDD Conn.



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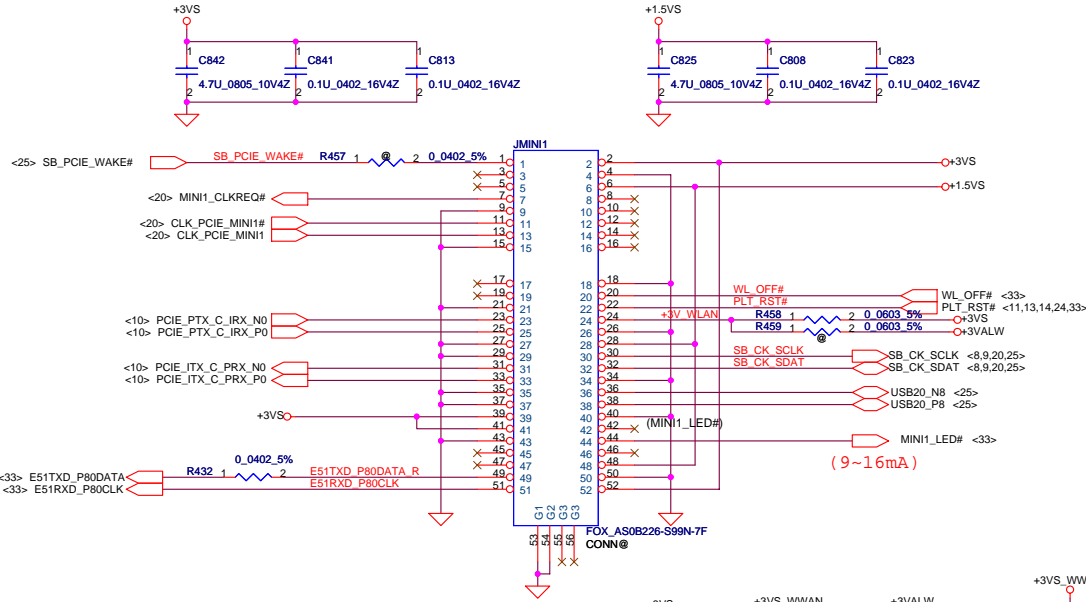


MSCLK and SDCLK 該二電阻是預留給EMI solution使用, (但請靠近RT5158E側).

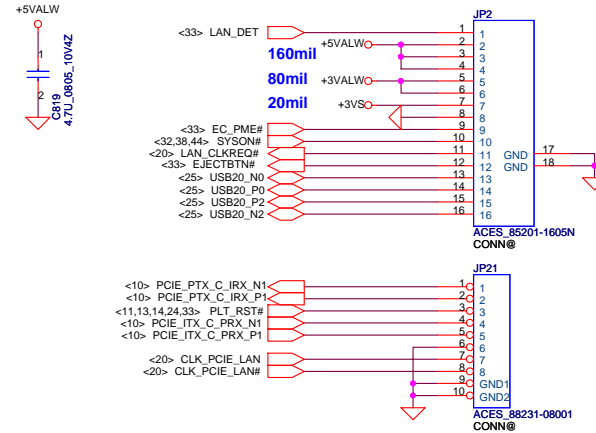


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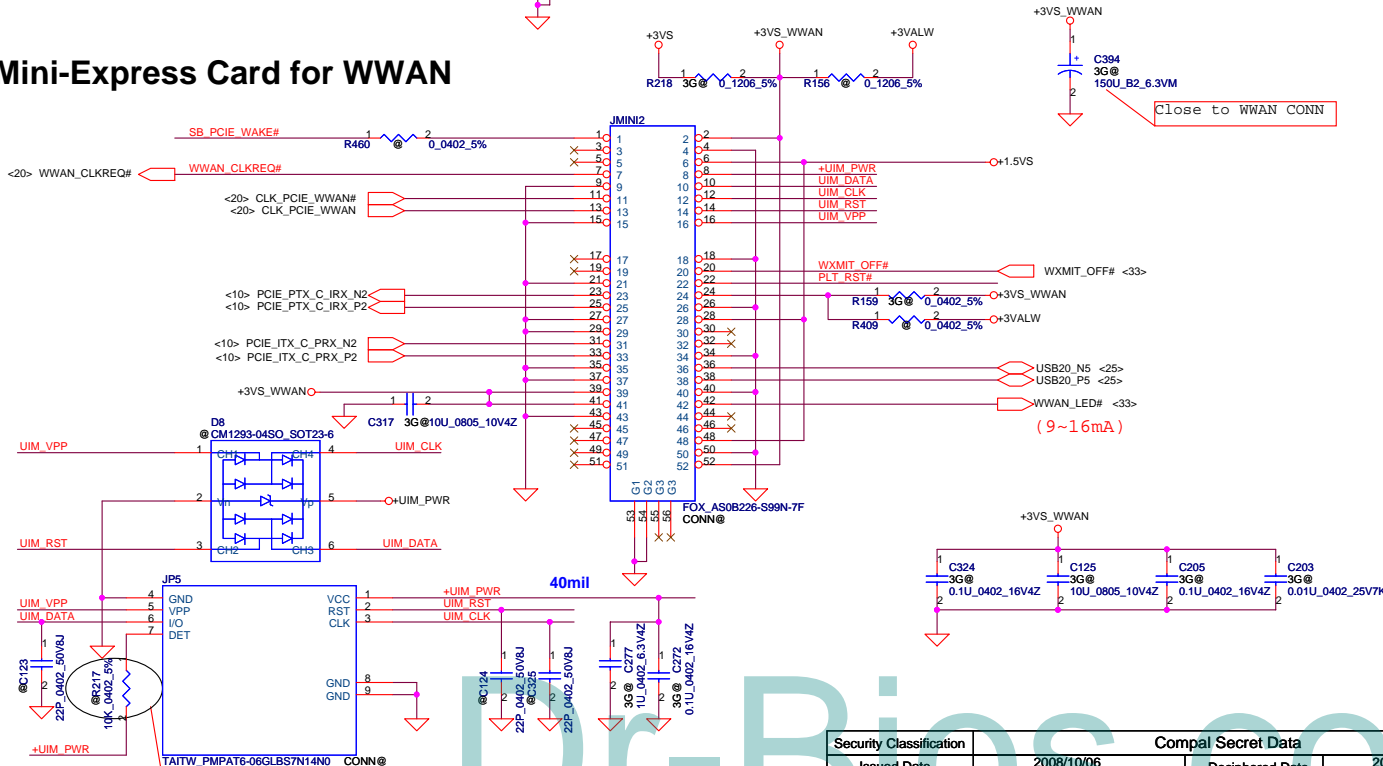
For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



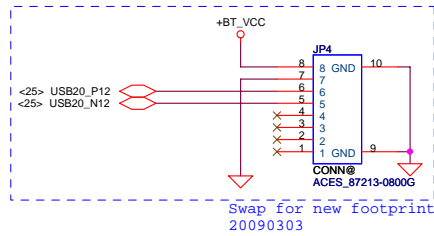
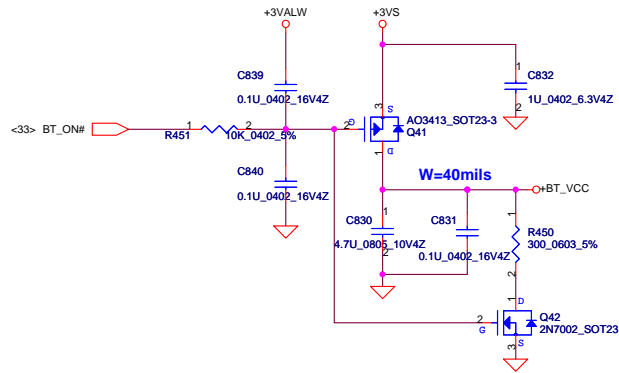
Mini-Express Card for WWAN



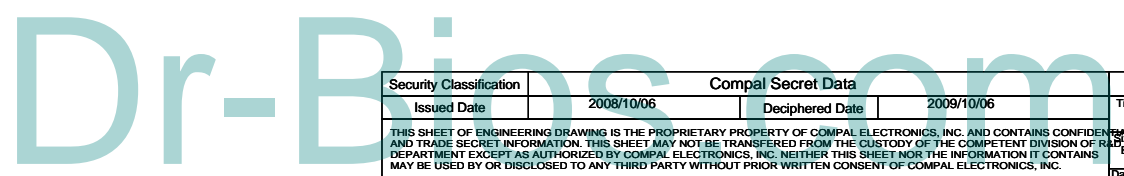
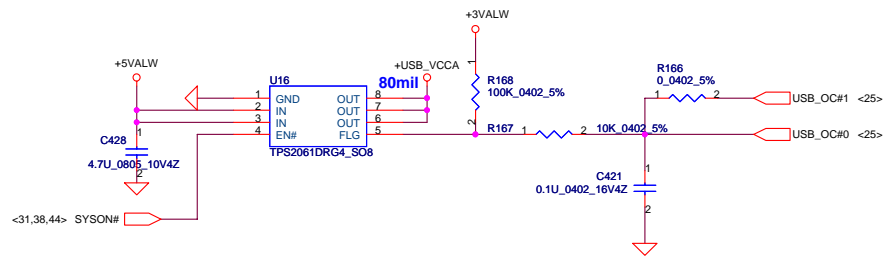
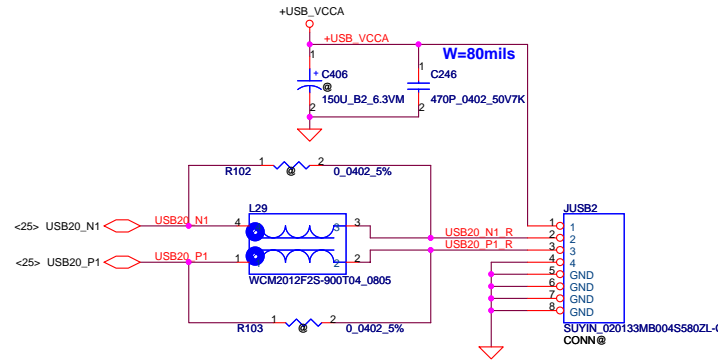
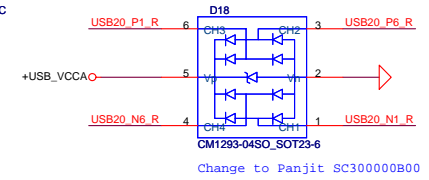
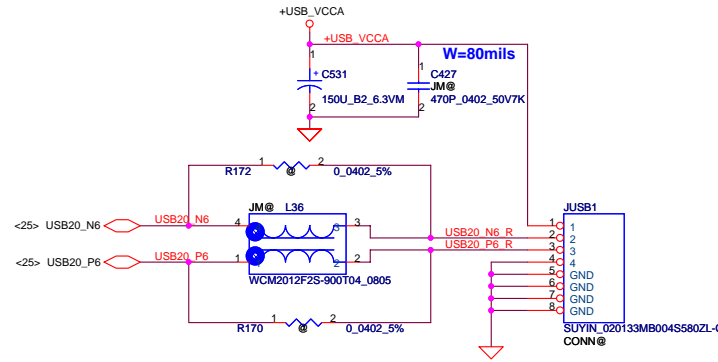
Reserve for SIM card does not meet rise time and pull-up is needed.

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Bluetooth Conn.

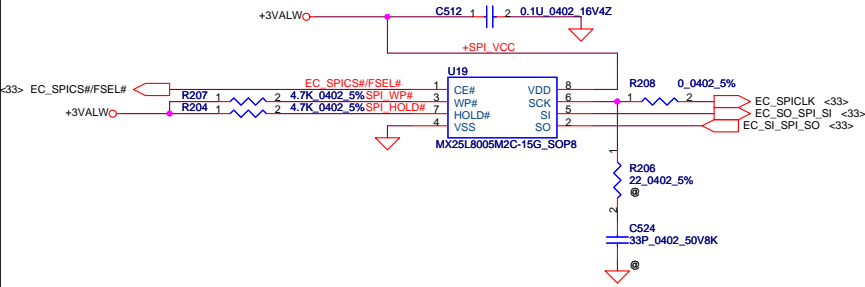


USB PORT x 2

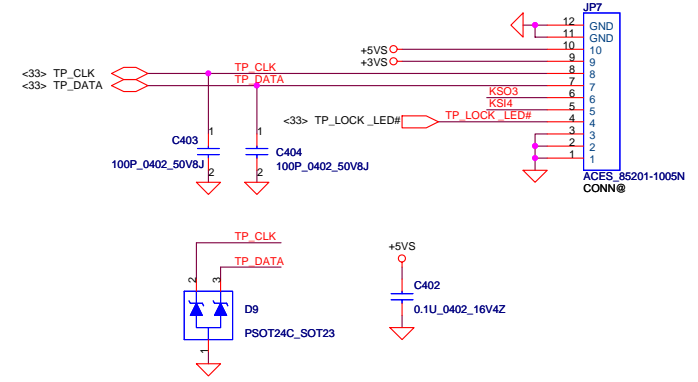


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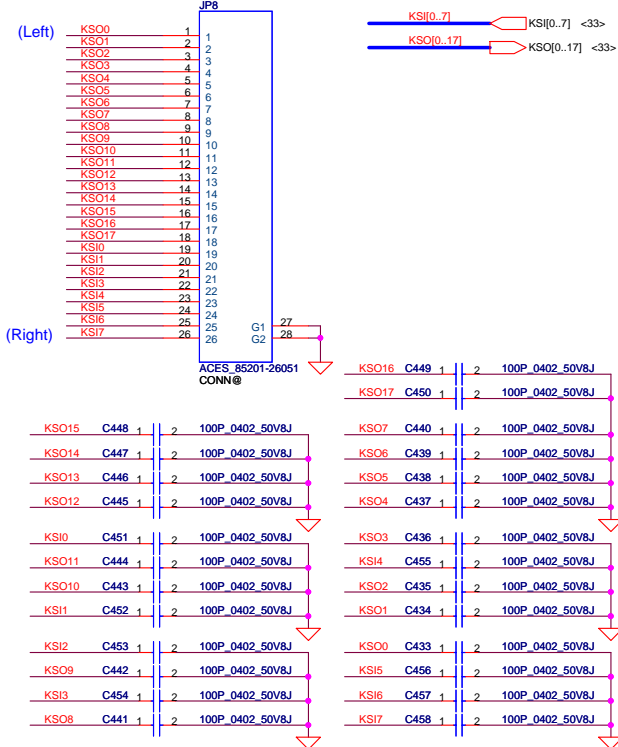
BIOS(SYS / EC / VGA)



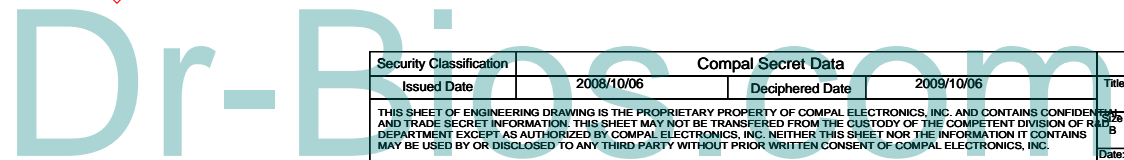
To TP/B Conn.



INT_KBD Conn.



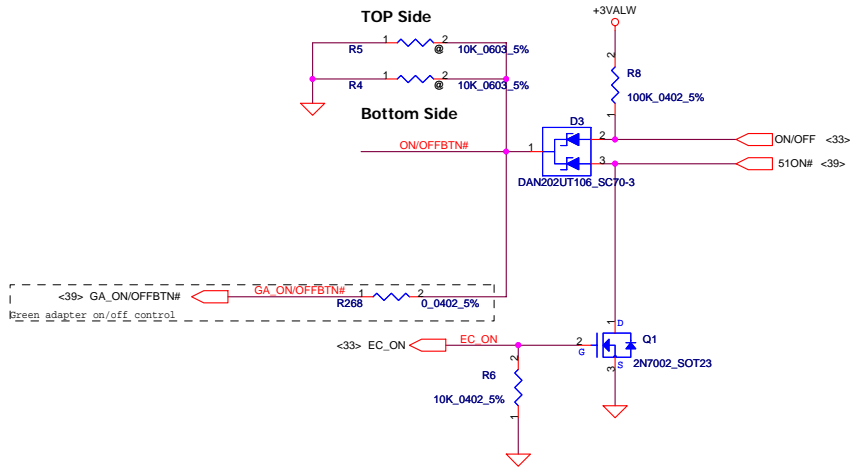
	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)
KSI4			T/P lock



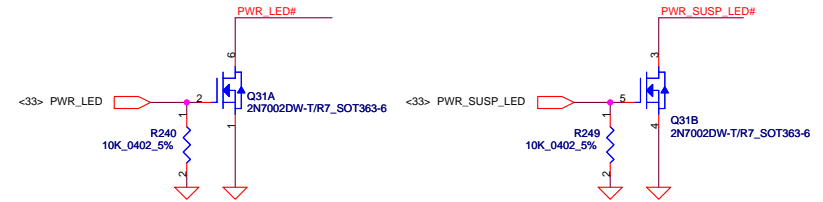
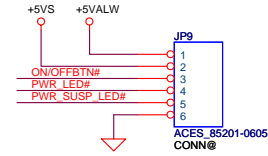
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ON/OFF switch

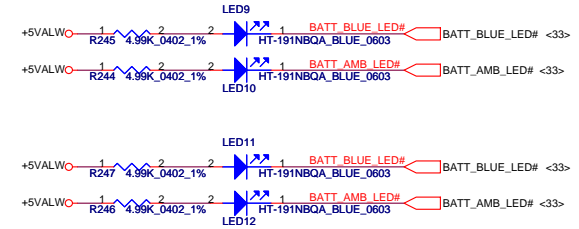
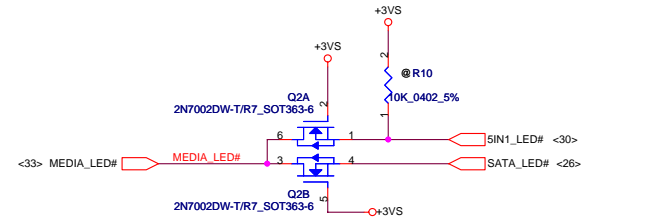
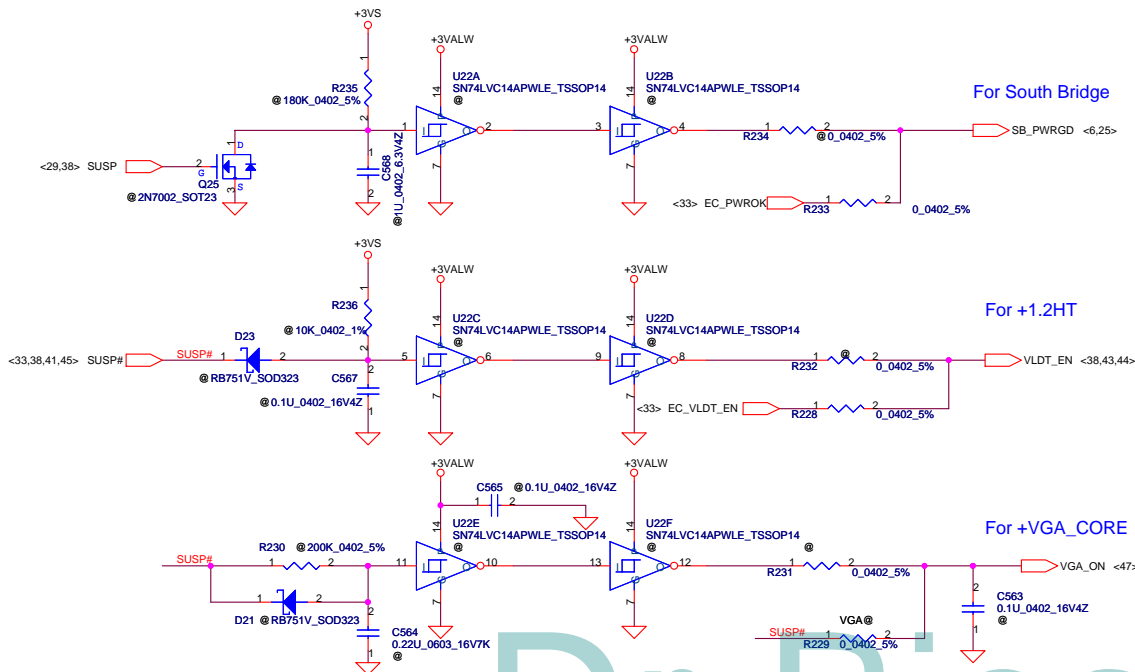
Power Button



To PWR/B Conn.

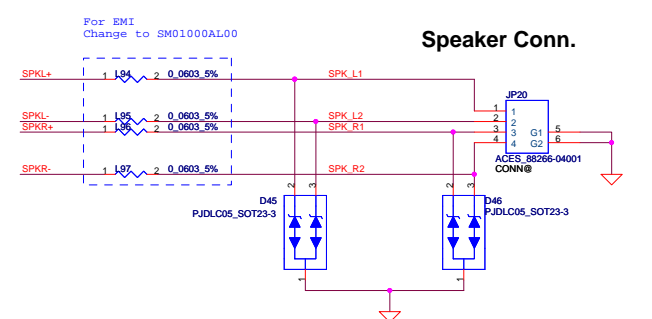
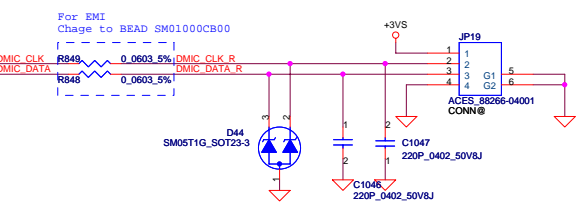
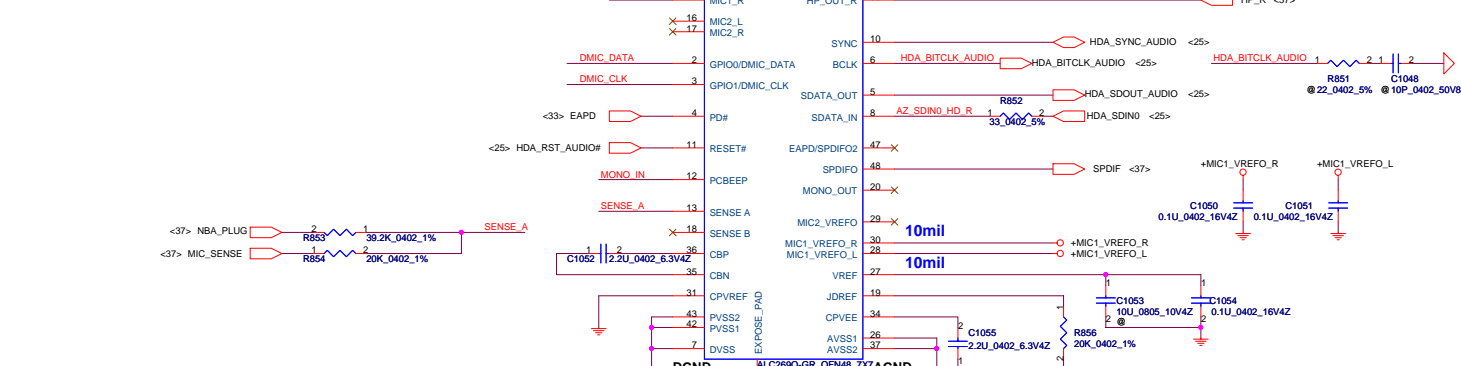
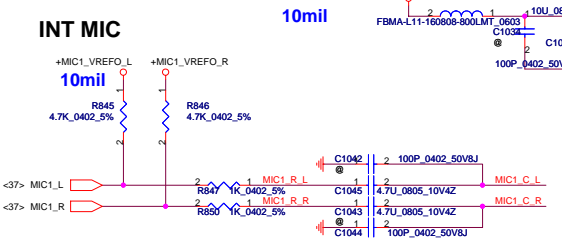
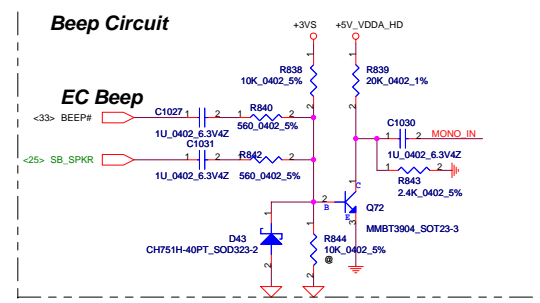
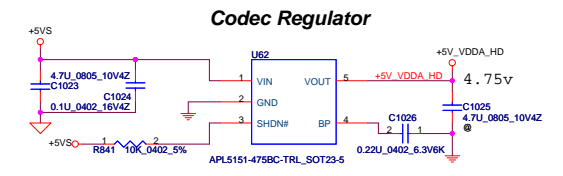


Power ON Circuit

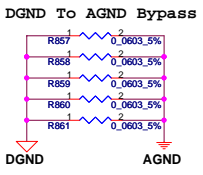


BLUE / AMBER

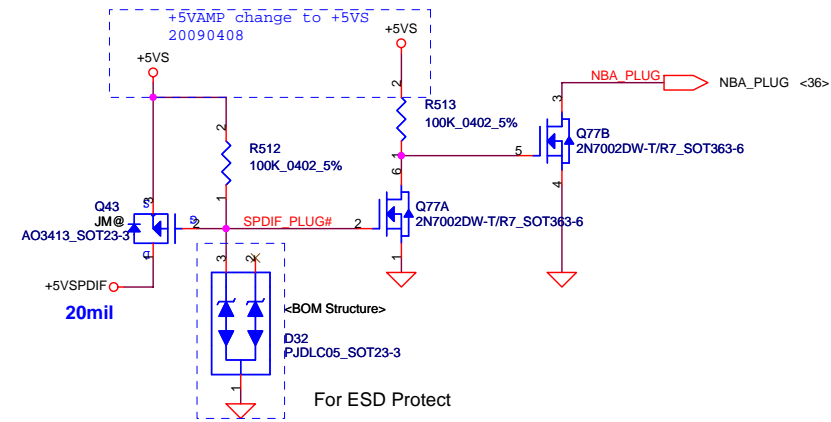
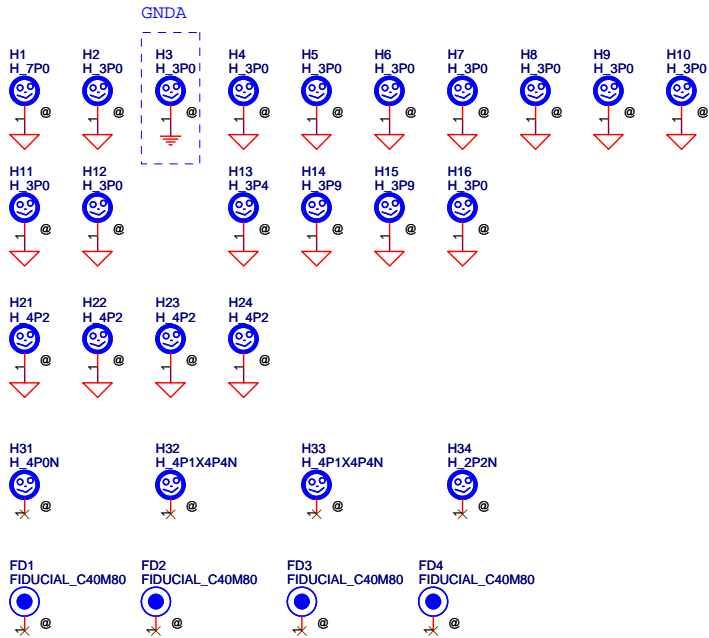
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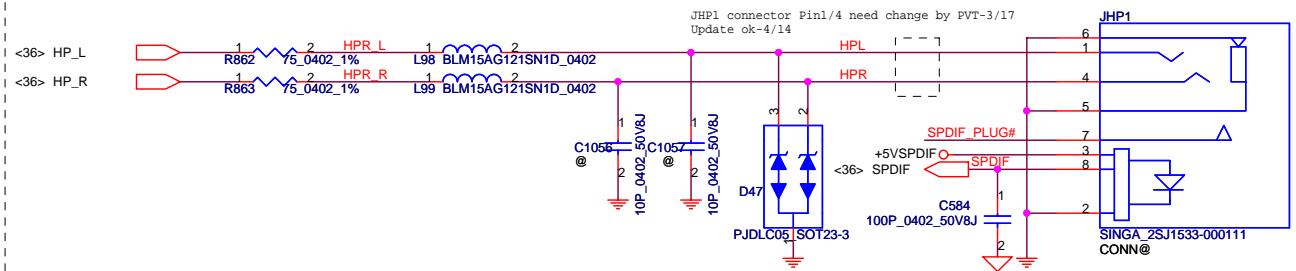
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 32, 33)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 48)
	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 20)
	5.1K	PORT-H (PIN 47)



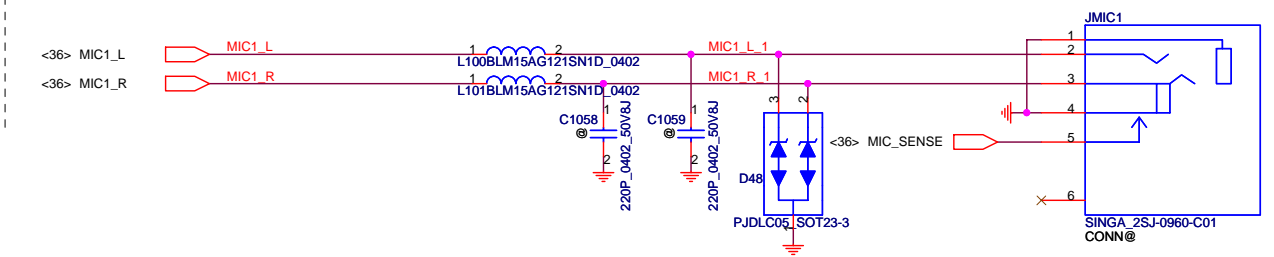
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HeadPhone JACK

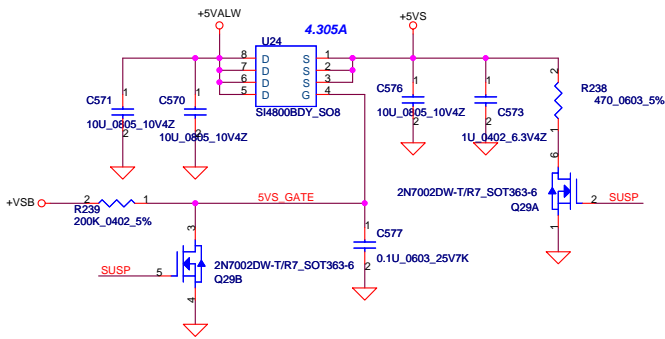


Ext.MIC JACK

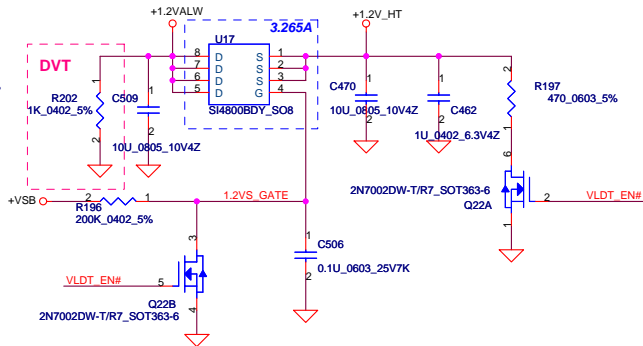


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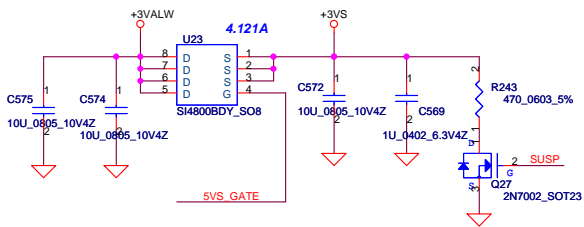
+5VALW TO +5VS



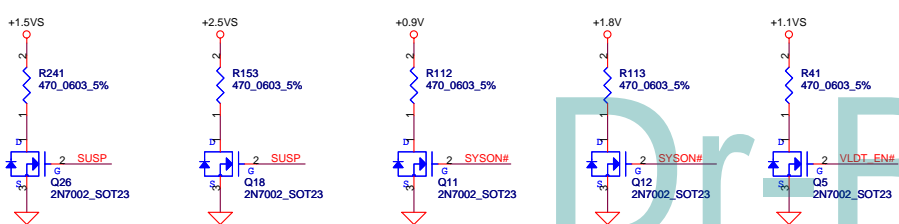
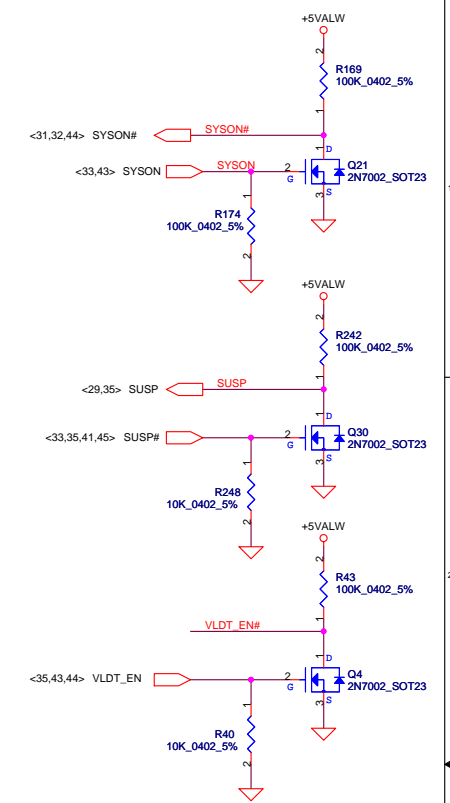
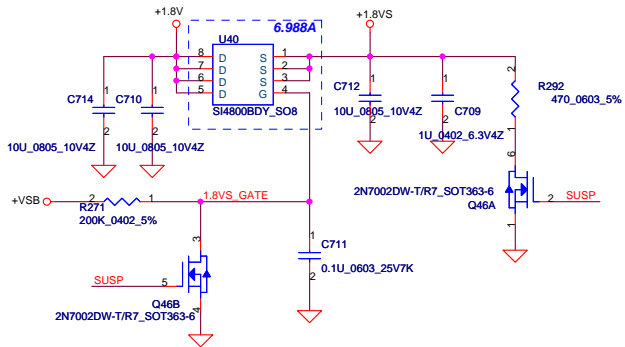
+1.2VALW TO +1.2V_HT



+3VALW TO +3VS

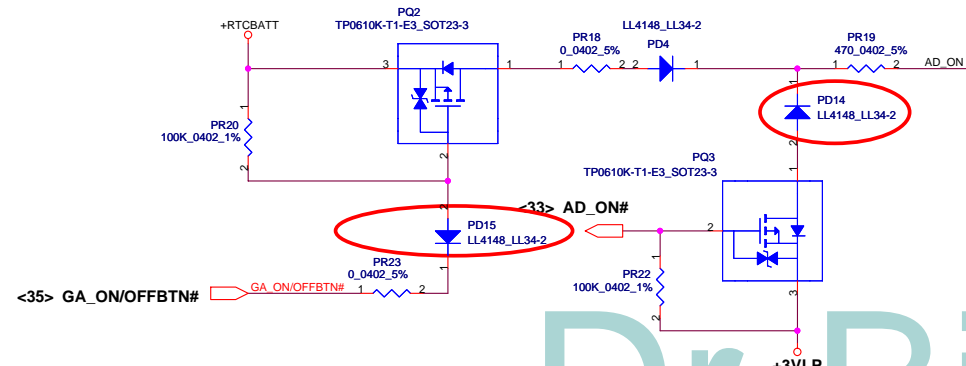
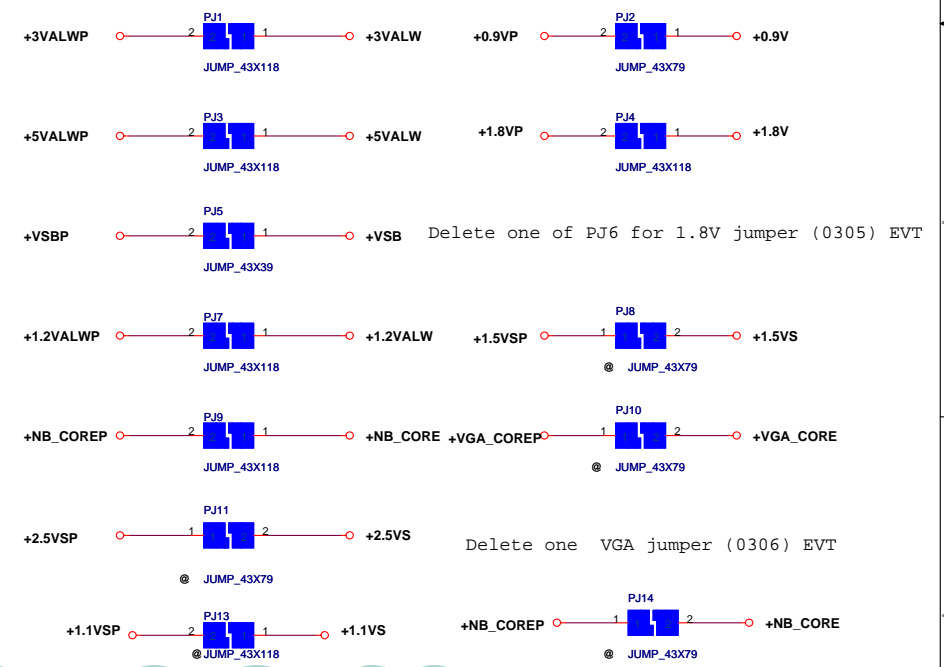
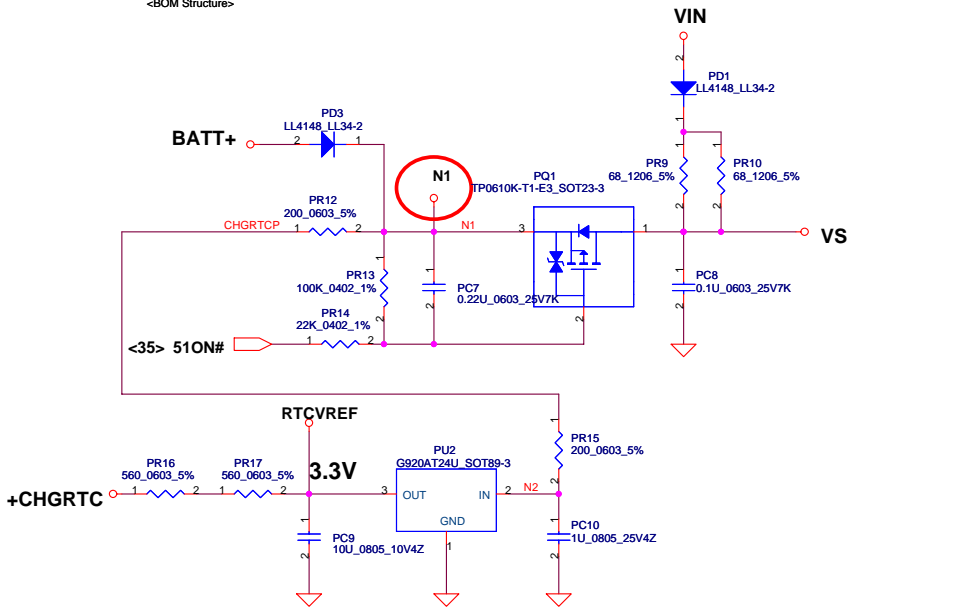
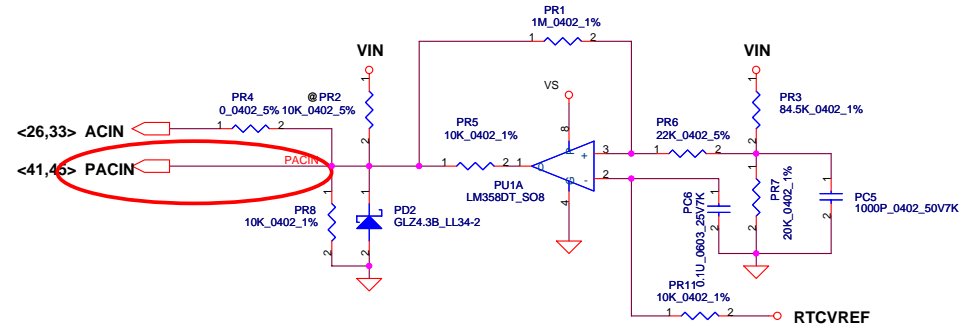
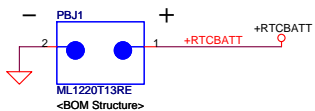
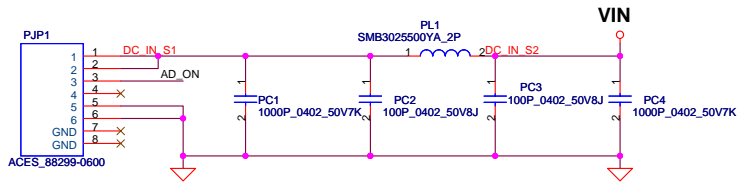


+1.8V to +1.8VS



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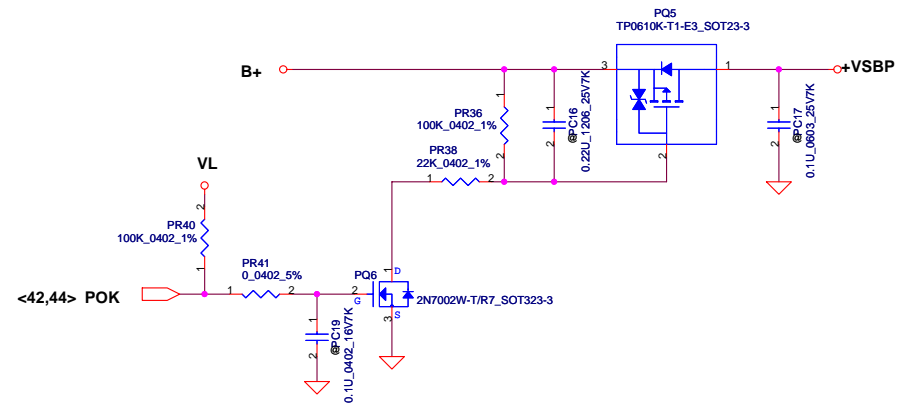
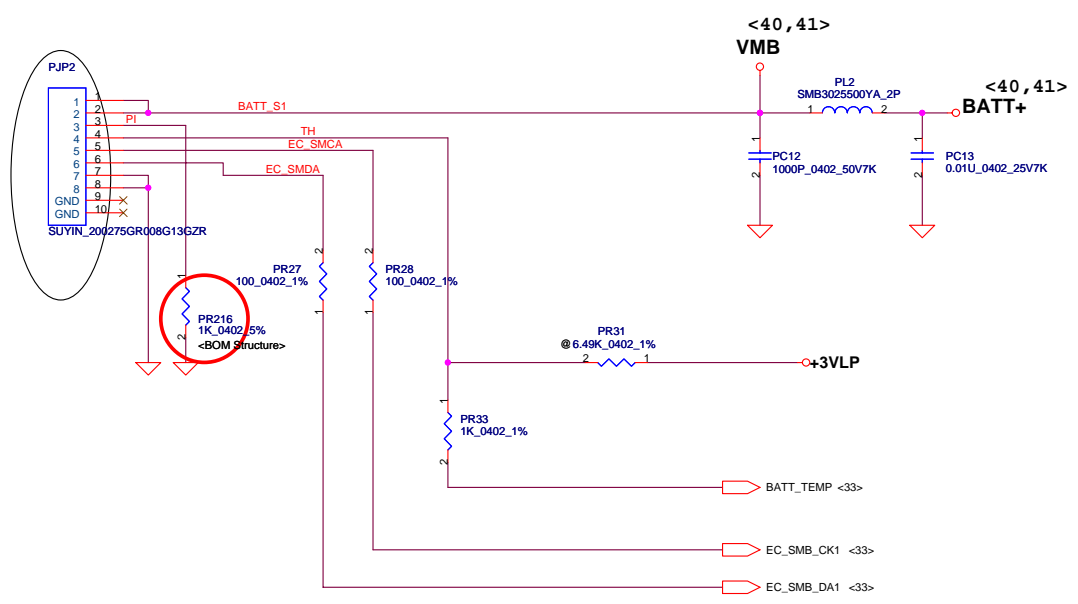
Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



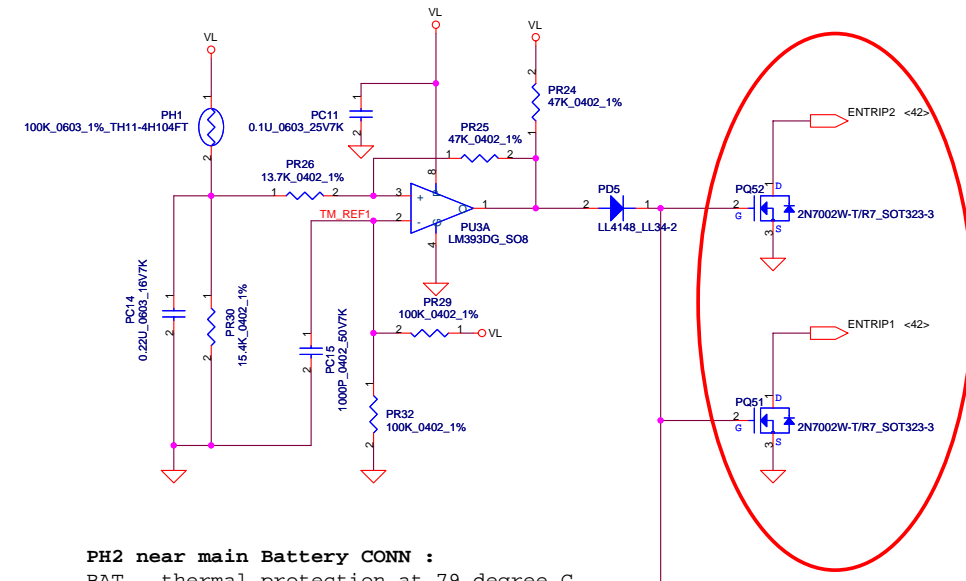
	S5 W/O WOL	S5 W WOL	S3/S0
AD_ON#	H	L	L

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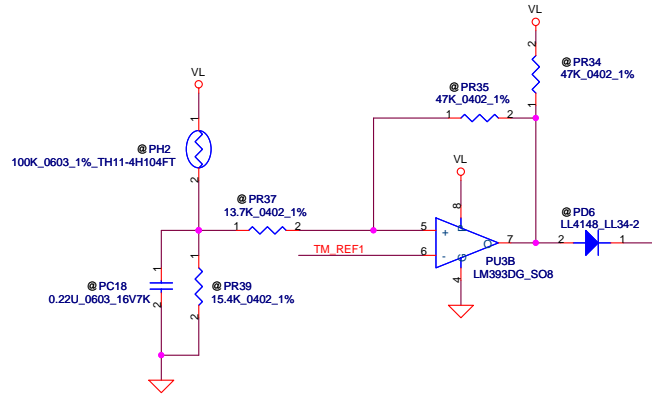
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PH1 under CPU botten side :
 CPU thermal protection at 93 degree C
 Recovery at 57 degree C



PH2 near Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



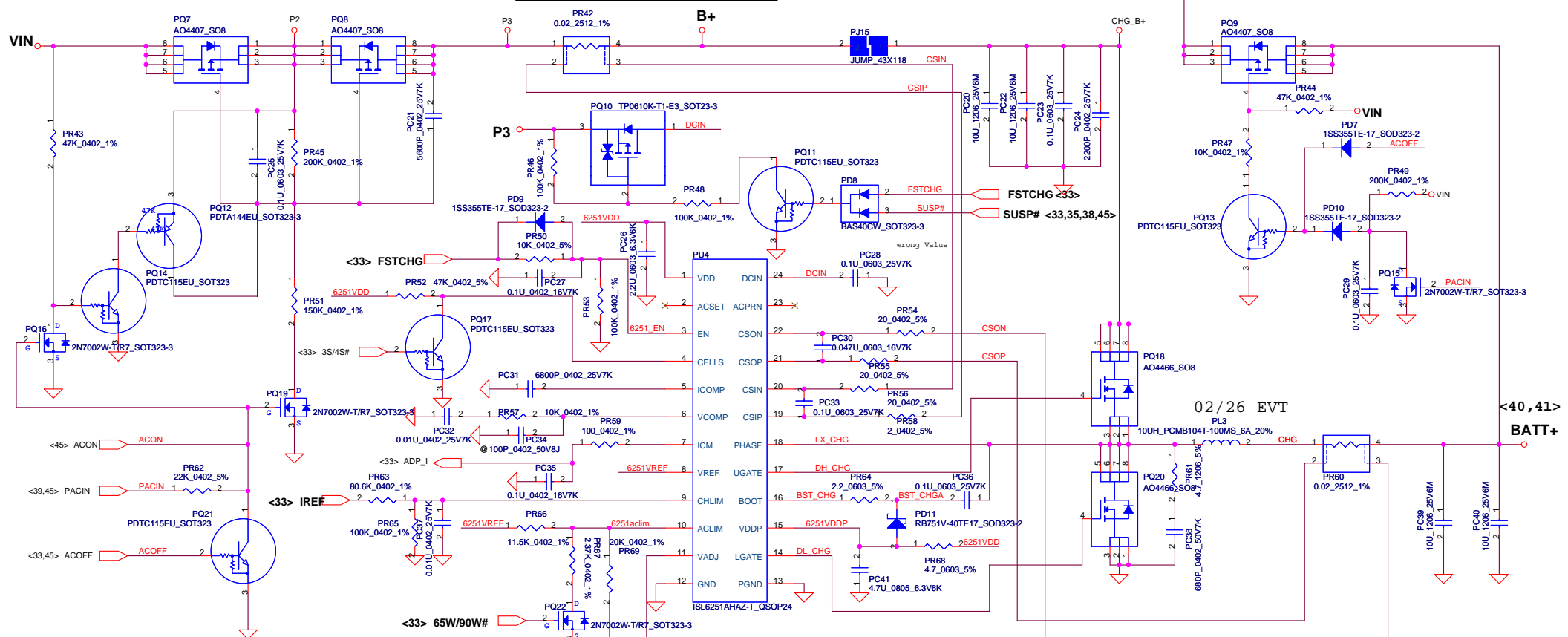
Dr-Bios.com

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Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



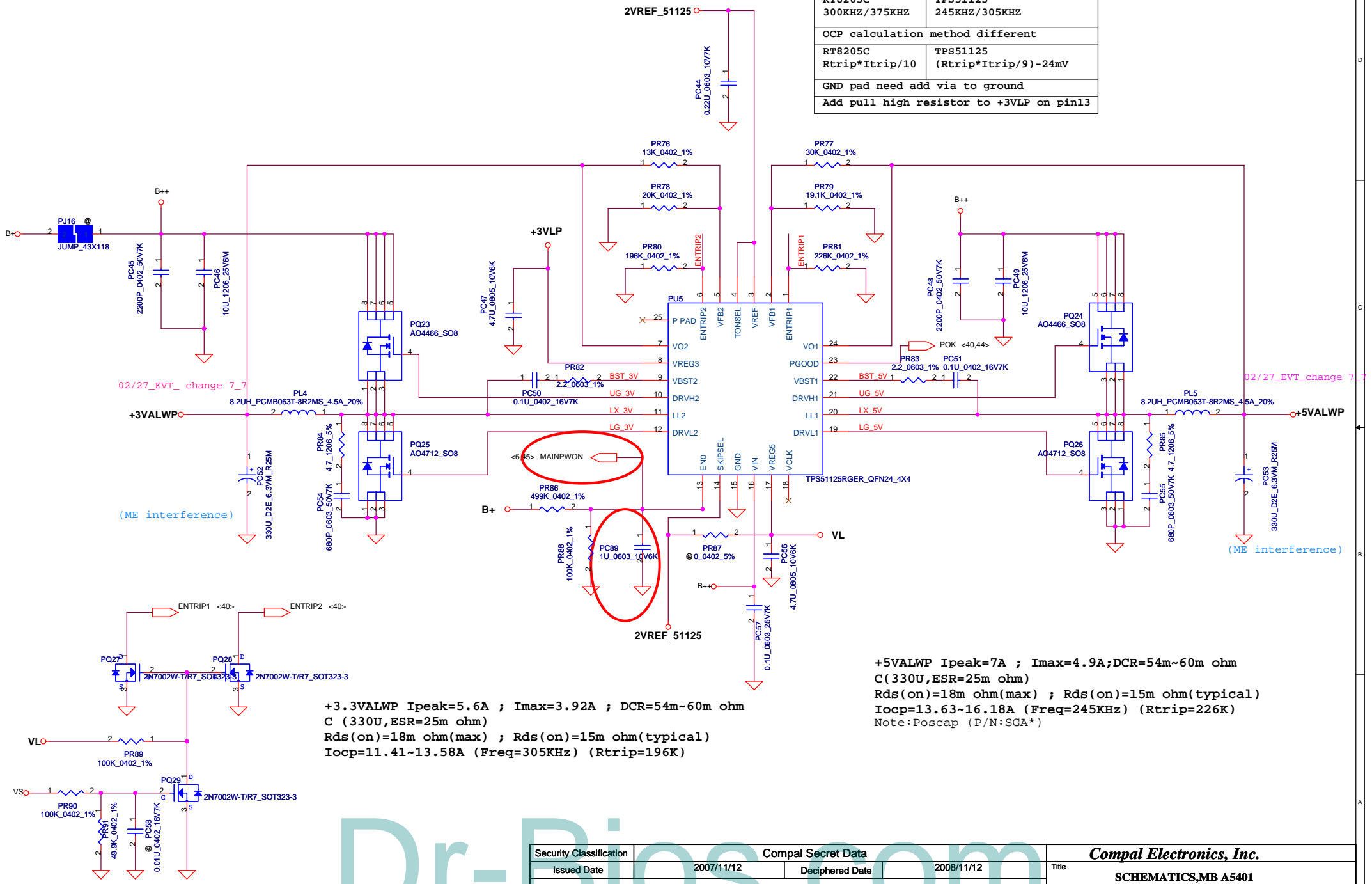
CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

LI-3S :1.3.5V---BATT-OVP=1.5012V
 $BATT-OVP = 0.1112 * V_{MB}$
 Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

Frequency different	
RT8205C 300KHZ/375KHZ	TPS51125 245KHZ/305KHZ
OCP calculation method different	
RT8205C Rtrip*Itrip/10	TPS51125 (Rtrip*Itrip/9)-24mV
GND pad need add via to ground	
Add pull high resistor to +3VLP on pin13	

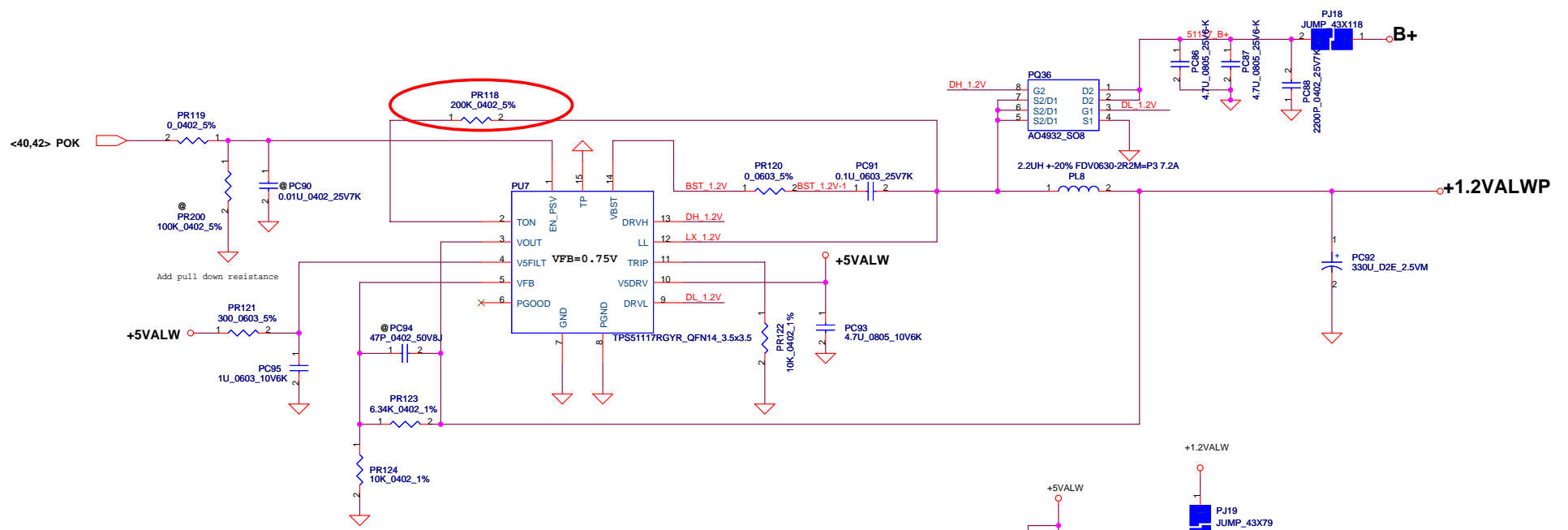


+3.3VALWP Ipeak=5.6A ; Imax=3.92A ; DCR=54m~60m ohm
 C (330U, ESR=25m ohm)
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Iocp=11.41~13.58A (Freq=305KHZ) (Rtrip=196K)

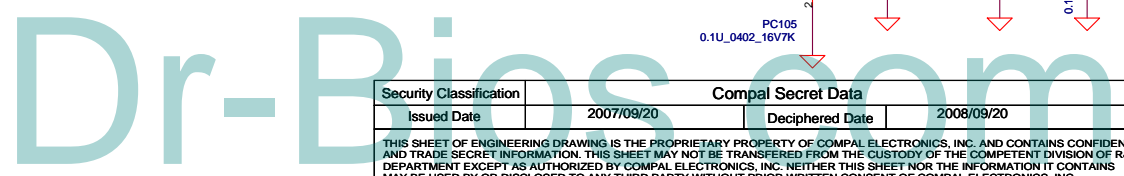
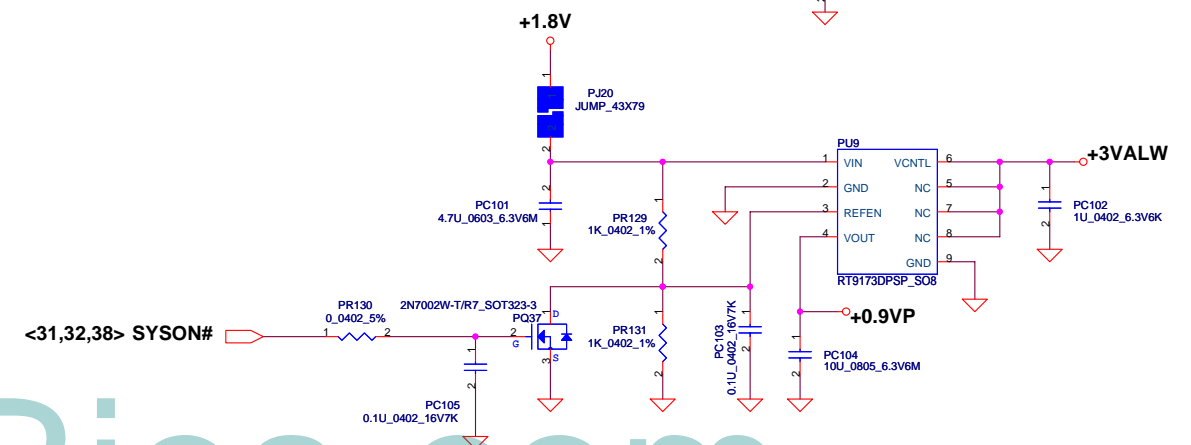
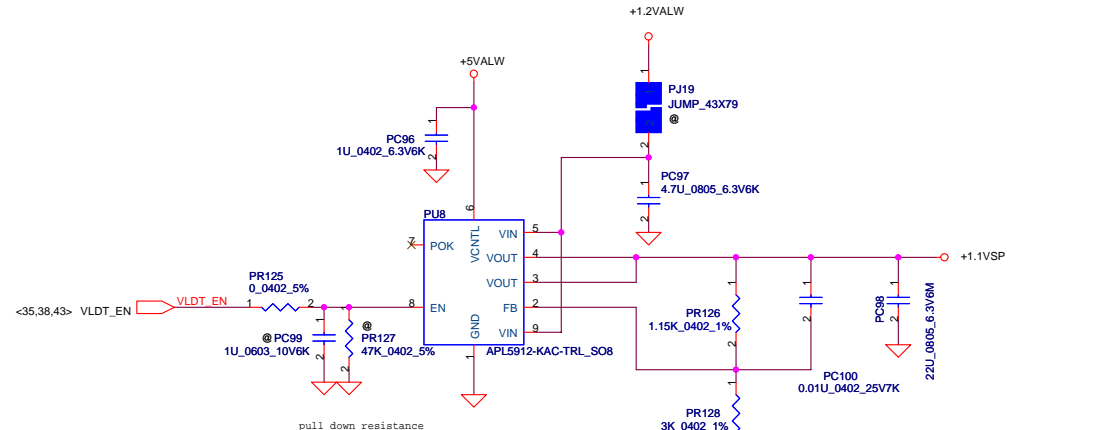
+5VALWP Ipeak=7A ; Imax=4.9A; DCR=54m~60m ohm
 C (330U, ESR=25m ohm)
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Iocp=13.63~16.18A (Freq=245KHZ) (Rtrip=226K)
 Note: Poscap (P/N:SGA*)

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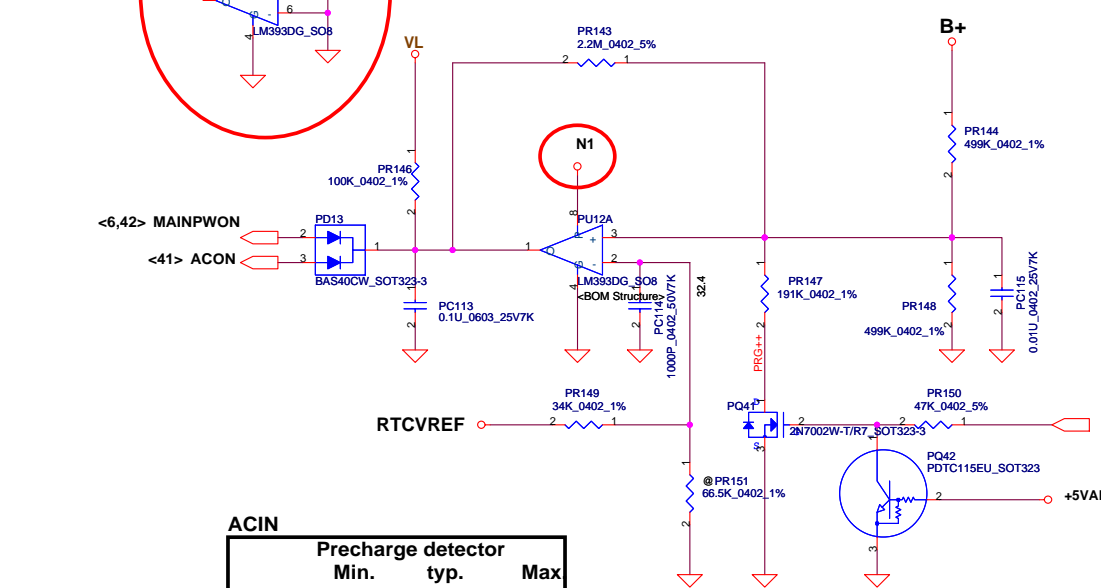
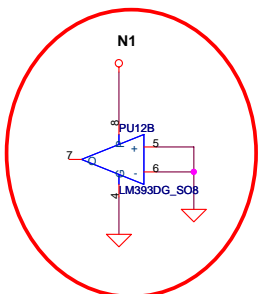
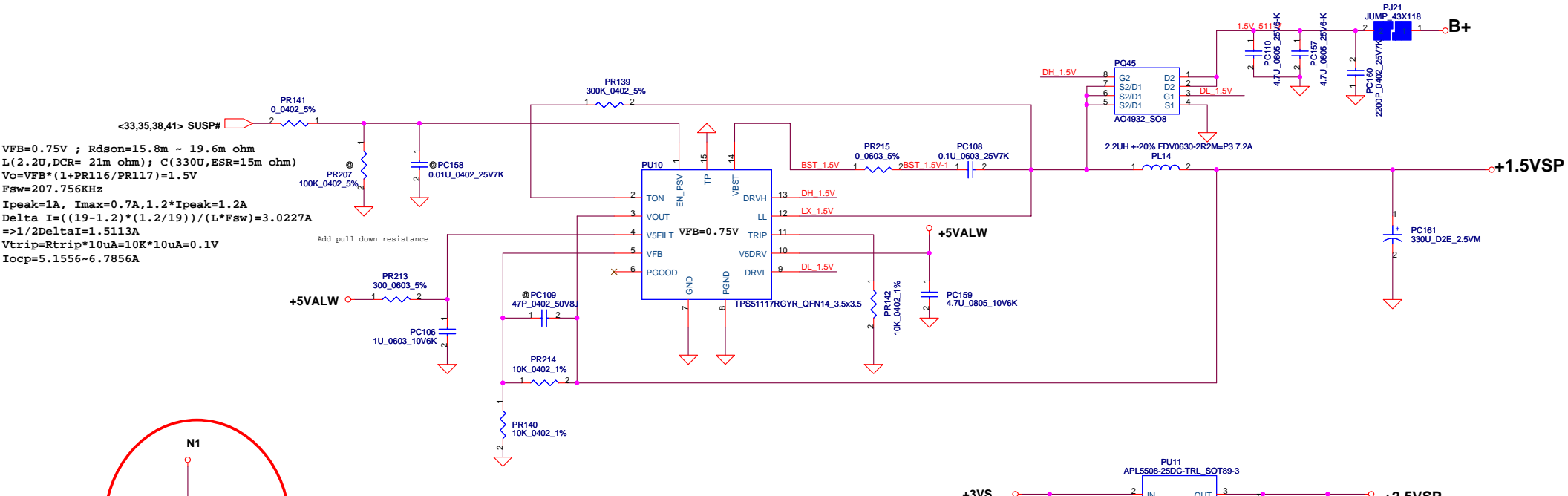


$VFB=0.75V$; $R_{dson}=15.8m \sim 19.6m \text{ ohm}$
 $L(2.2U, DCR=21m \text{ ohm})$; $C(330U, ESR=15 \text{ mohm})$
 $V_o = VFB * (1 + PR116 / PR117) = 1.2V$
 $F_{sw} = 274.6KHz$
 $I_{peak} = 2.865A$, $I_{max} = 2.0055A$, $1.2 * I_{peak} = 3.438A$
 $\Delta I = ((19 - 1.2) * (1.2 / 19)) / (L * F_{sw}) = 2.589A$
 $\Rightarrow 1 / 2 \Delta I = 1.2945A$
 $V_{trip} = R_{trip} * I_{0uA} = 10K * 10uA = 0.1V$
 $I_{ocp} = 4.938 \sim 6.568A$



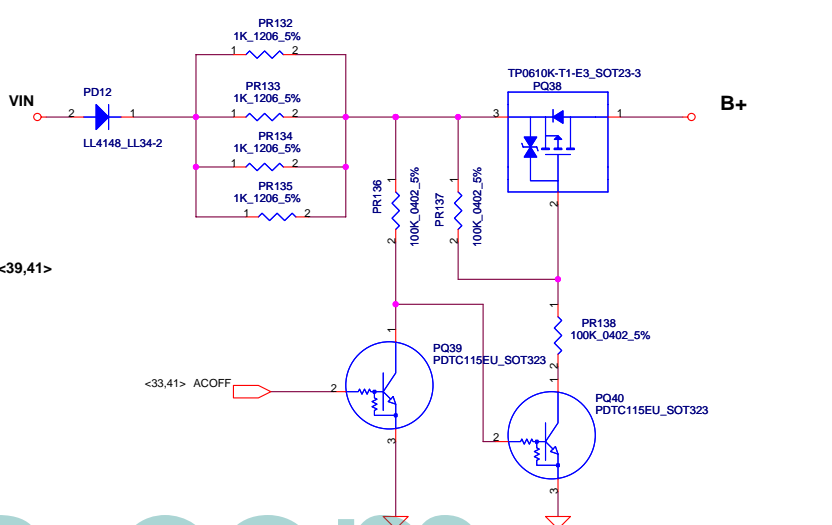
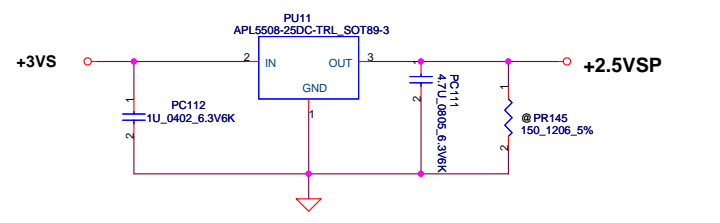
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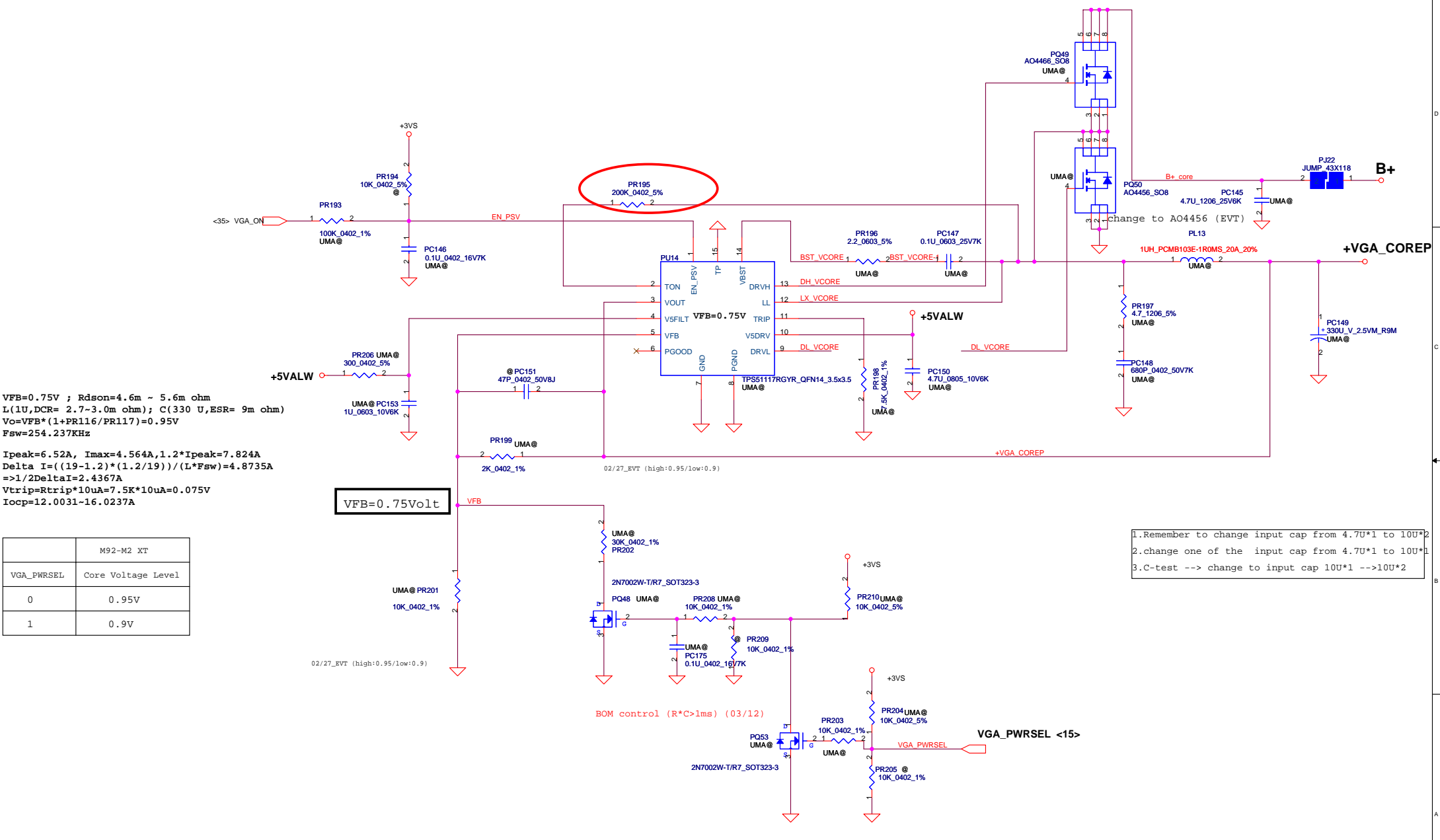
$V_{FB}=0.75V$; $R_{dson}=15.8m \sim 19.6m \text{ ohm}$
 $L(2.2U, DCR=21m \text{ ohm})$; $C(330U, ESR=15m \text{ ohm})$
 $V_o=V_{FB} \cdot (1+PR116/PR117)=1.5V$
 $F_{sw}=207.756KHz$
 $I_{peak}=1A$, $I_{max}=0.7A$, $1.2 \cdot I_{peak}=1.2A$
 $\Delta I = ((19-1.2) \cdot (1.2/19)) / (L \cdot F_{sw}) = 3.0227A$
 $\Rightarrow 1/2 \Delta I = 1.5113A$
 $V_{trip} = R_{trip} \cdot I = 10K \cdot 10uA = 0.1V$
 $I_{ocp} = 5.1556 \sim 6.7856A$



ACIN			
Precharge detector			
	Min.	typ.	Max
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V





VFB=0.75V ; R_{ds(on)}=4.6m ~ 5.6m ohm
 L(1U,DCR= 2.7~3.0m ohm) ; C(330 U,ESR= 9m ohm)
 V_o=VFB*(1+PR116/PR117)=0.95V
 F_{sw}=254.237KHz

I_{peak}=6.52A, I_{max}=4.564A, 1.2*I_{peak}=7.824A
 Delta I=((19-1.2)*(1.2/19))/(L*F_{sw})=4.8735A
 =>1/2Delta I=2.4367A
 V_{trip}=R_{trip}*I_{0uA}=7.5K*10uA=0.075V
 I_{ocp}=12.0031-16.0237A

VFB=0.75Volt

	M92-M2 XT
VGA_PWRSEL	Core Voltage Level
0	0.95V
1	0.9V

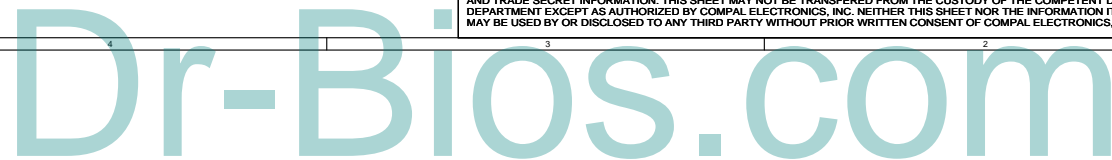
1. Remember to change input cap from 4.7U*1 to 10U*2
2. change one of the input cap from 4.7U*1 to 10U*1
3. C-test --> change to input cap 10U*1 -->10U*2

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD circuit	Switch NB_core voltage	0.1	50	ADD PC107, PC105, PR121, PR123, PR122, PR102, PQ25, PQ28 at UMA Sku	2009/01/04	DVT
2	ADD circuit	Switch NB_core voltage	0.1	51	ADD PC110, PC111, PC108, PC109, PC1113, PR1128, PR194, PR129, PR127 at UMA Sku	2009/01/04	DVT
3	ADD snubber	EMI requestmnt	0.1	50	Add PR104 4.7 ohm and PC83 680p	2009/01/04	DVT
4	ADD snubber	EMI requestmnt	0.1	50	Add PR108 4.7 ohm and PC89 680p	2009/01/04	DVT
5	ADD CPU boot	EMI requestmnt	0.1	53	Add PR229 2.2 ohm	2009/01/04	DVT
6	ADD CPU boot	EMI requestmnt	0.1	53	Add PR243 2.2 ohm	2009/01/04	DVT
7	Change resistance value	Switch NB_core voltage	0.1	50	Change PR95 from 51 Kohm to 39.2 Kohm	2009/01/04	DVT
8	Change resistance value	Switch NB_core voltage	0.1	50	Change PR122 from 12 Kohm to 226 Kohm	2009/01/04	DVT
9	Change resistance value	soft start of Switch NB_core voltage	0.1	50	Change PR123 from 0 ohm to 10 Kohm	2009/01/04	DVT
10	Change capacitor value	soft start of Switch NB_core voltage	0.1	50	Change PC105 from 0.01 uF to 0.1 uF	2009/01/04	DVT
11	Change IC part number	Change IC part number	0.1	48	Change PU4 part number to SA00002V400	2009/01/04	DVT

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PHASE	PAGE	Modification list	PURPOSE
PVT	P.29	Delete Q24 and modify ODD power circuit	Modify ODD power circuit to follow up SUSP#
	P.36	Change L94-L97 to bead , delete C1184/C1193	Follow Realtek suggest
	P.37	Change SPDIF detec power +5VAMP to +5VS C45、C466 Change to 10U	
	P.33	Add R566、R567 for e-machine	
	4/20	Add H34	For FAN
	4/21	Add LAN_DET function IO/B PLT_RST# change to JP21	For FAN For ESD
	4/22	Add R212 Update USB footprint -FOX_UB511AC-RABA7-7F_4P-T C536 Change to 220U	For VRAM ID
	4/23	Add C39、C41、C778、C780	For ESD
	4/24	Change Lid SW power to +3VL	

For Discrete

CRT

R285 VGA@ 150_0402_1%

R54 VGA@ 2.2K_0402_5%

R46 VGA@ 2.2K_0402_5%

C633 C640 C662
VGA@ 3.3P_0402_50V8J
3.3P_0402_50V8J 3.3P_0402_50V8J

C667 C660 C639
VGA@ 8P_0402_50V8J
8P_0402_50V8J 8P_0402_50V8J

HDMI

R141 VGA@ 499_0402_1%

R137 VGA@ 499_0402_1%

R149 VGA@ 499_0402_1%

R145 VGA@ 499_0402_1%

R155 VGA@ 499_0402_1%

R152 VGA@ 499_0402_1%

R158 VGA@ 499_0402_1%

R157 VGA@ 499_0402_1%

For E-Machine
disable side port

R281 HM@ 3K_0402_5%

R223 HM@ 0_0402_5%

R406 HM@ 0_0603_5%

PCB

ZZZ



PCB 06F LA-5401P REV0 MB

LA5401P MB Rev0: DA80000ET00

LA5401P MB Rev1: DA80000ET10

LA5401P MB with Sub/B Rev1: DAZ-

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