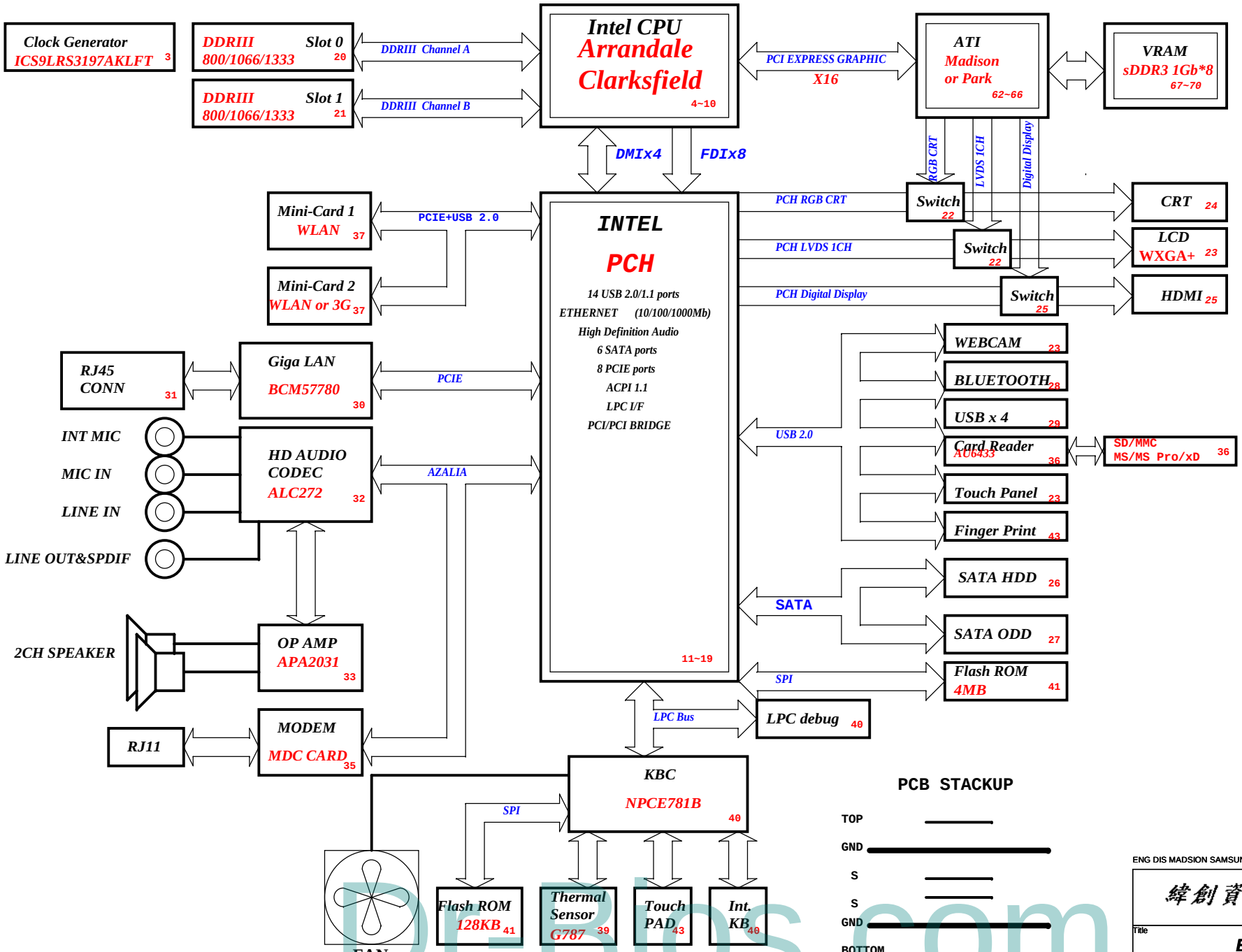
JV50-CP Block Diagram

Project code: 91.4GD01.001
PCB P/N : 48.4GD01.0SB
REVISION : SB 09285



PCB STACKUP

CPU DC/DC ISL62882	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

SYSTEM DC/DC TPS51123	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 50

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 51

RT9025	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0 50

G2997	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 52

SYSTEM DC/DC ISL62881	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 54

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 55

CHARGER ISL88731A	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

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Title: Table of Content

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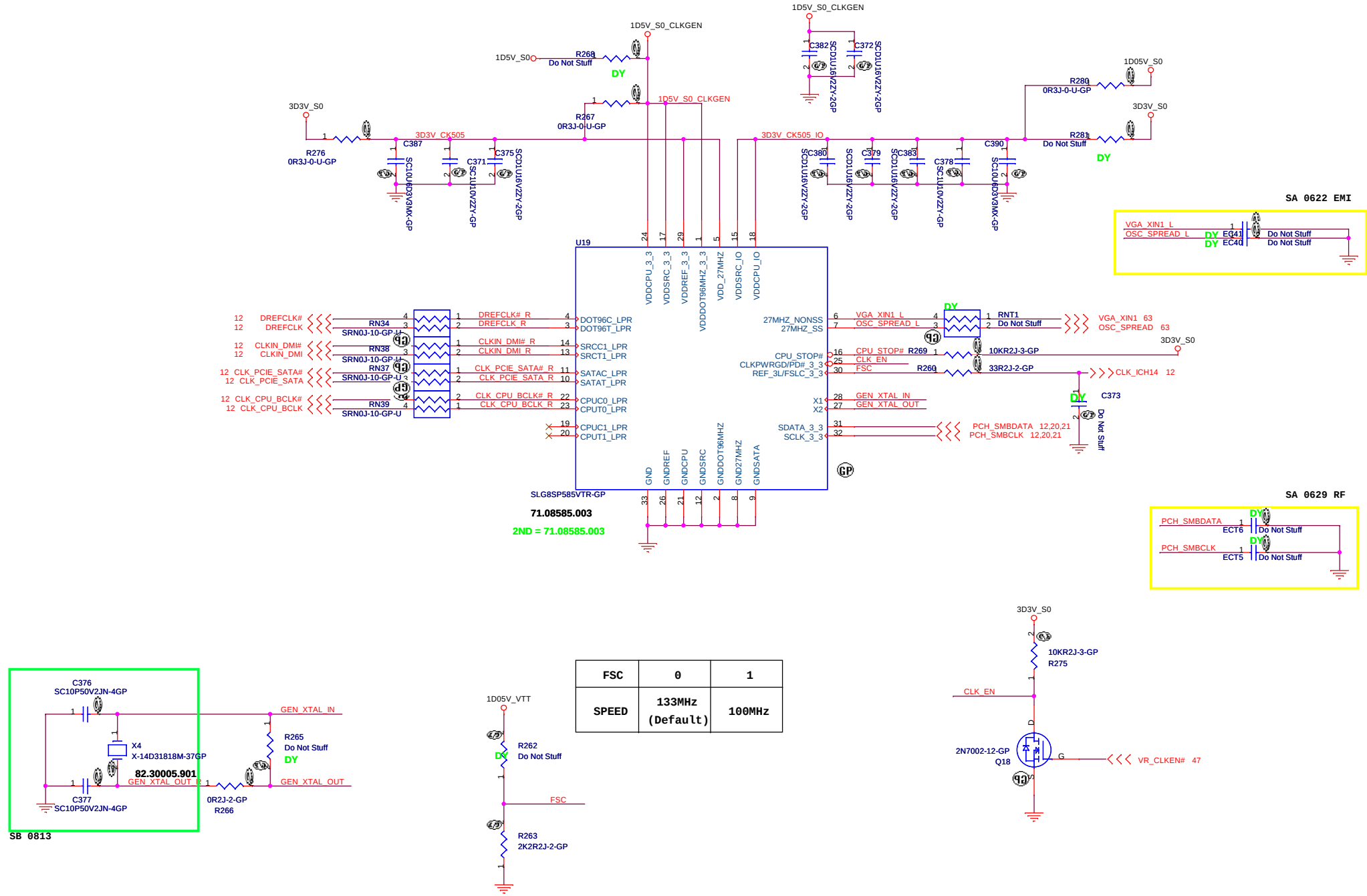

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: **Clock Generator**

Size	Document Number	Rev
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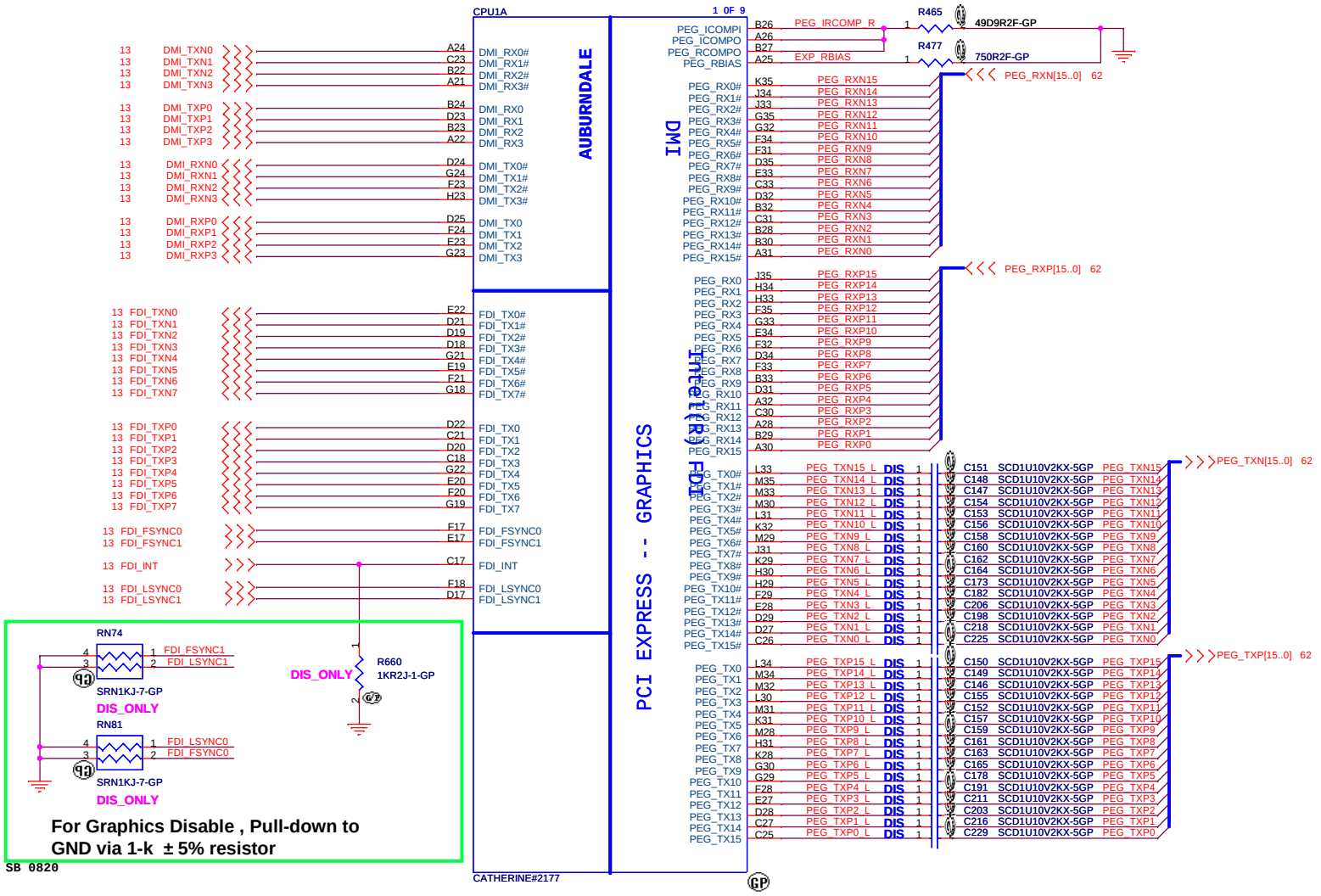

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Title: CPU (1/7)

Size: A3 | Document Number: JV50-CP | Rev: SA

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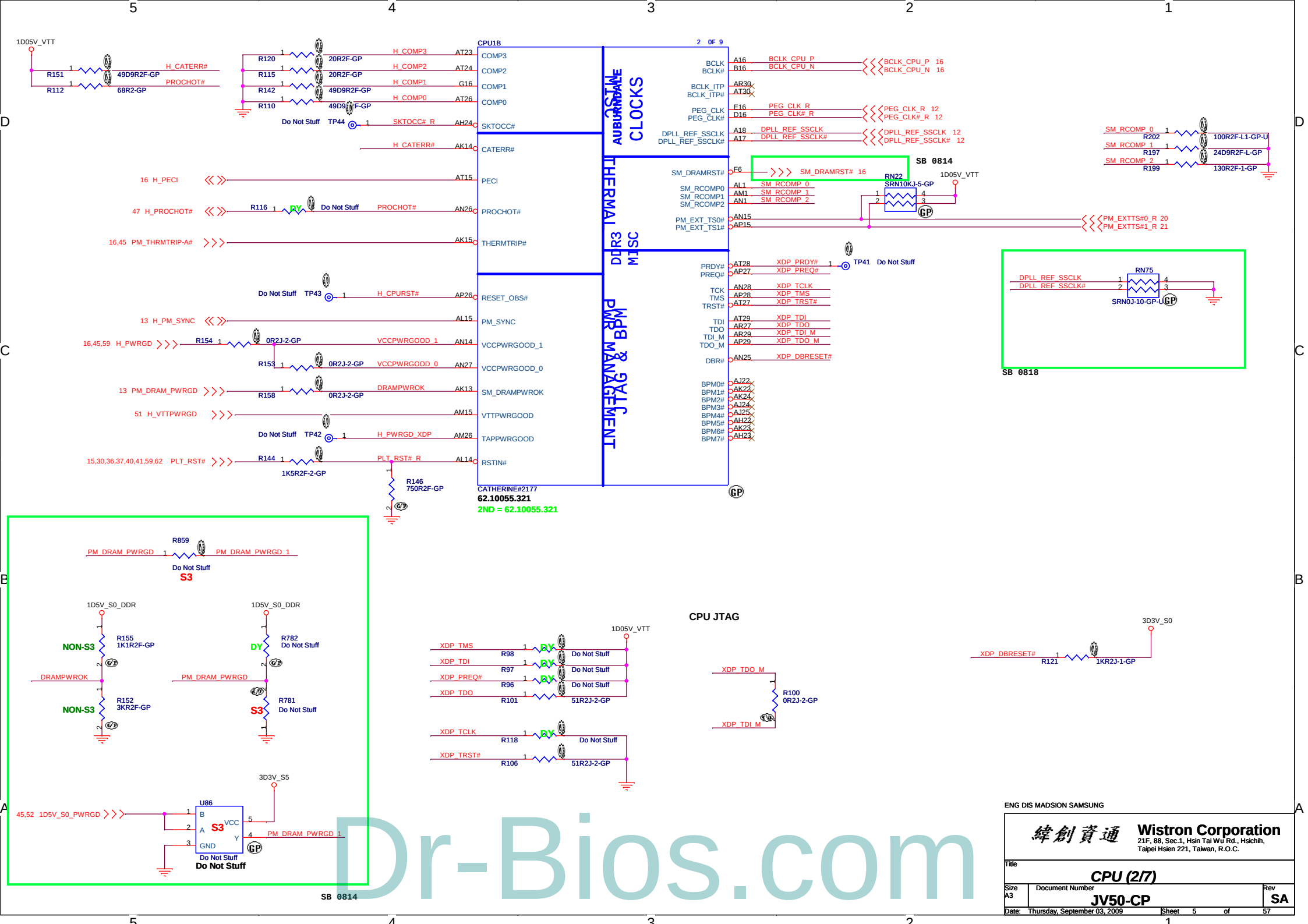
CPU1B
2 OF 9
CLOCKS
THERMAL
DDR3
MISC
PWR MANAGEMENT
JTAG
1D05V_VTT
H_CATERR#
PROCHOT#
H_COMP3
H_COMP2
H_COMP1
H_COMP0
SKTOCC# R
H_PECI
H_PROCHOT#
PM_THRMTRIP#
H_CPURST#
PM_SYNC
H_PWRGD
VCCPWRGOOD_1
VCCPWRGOOD_0
PM_DRAM_PWRGD
DRAMPWROK
H_VTTPWRGD
H_PWRGD_XDP
PLT_RST#
PLT_RST# R
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PM_EXT_TS0#
PM_EXT_TS1#
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM0#
BPM1#
BPM2#
BPM3#
BPM4#
BPM5#
BPM6#
BPM7#
SB 0814
SB 0818
CATHERINE#2177
62.10055.321
2ND = 62.10055.321
CPU JTAG
XDP_TMS
XDP_TDI
XDP_PREQ#
XDP_TDO
XDP_TCLK
XDP_TRST#
XDP_TDO_M
XDP_TDI_M
XDP_DBRESET#
PM_DRAM_PWRGD_1
S3
NON-S3
DY
Do Not Stuff
U86
3D3V_S5
1D5V_S0_DDR
1D5V_S0_PWRGD
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CPU (2/7)
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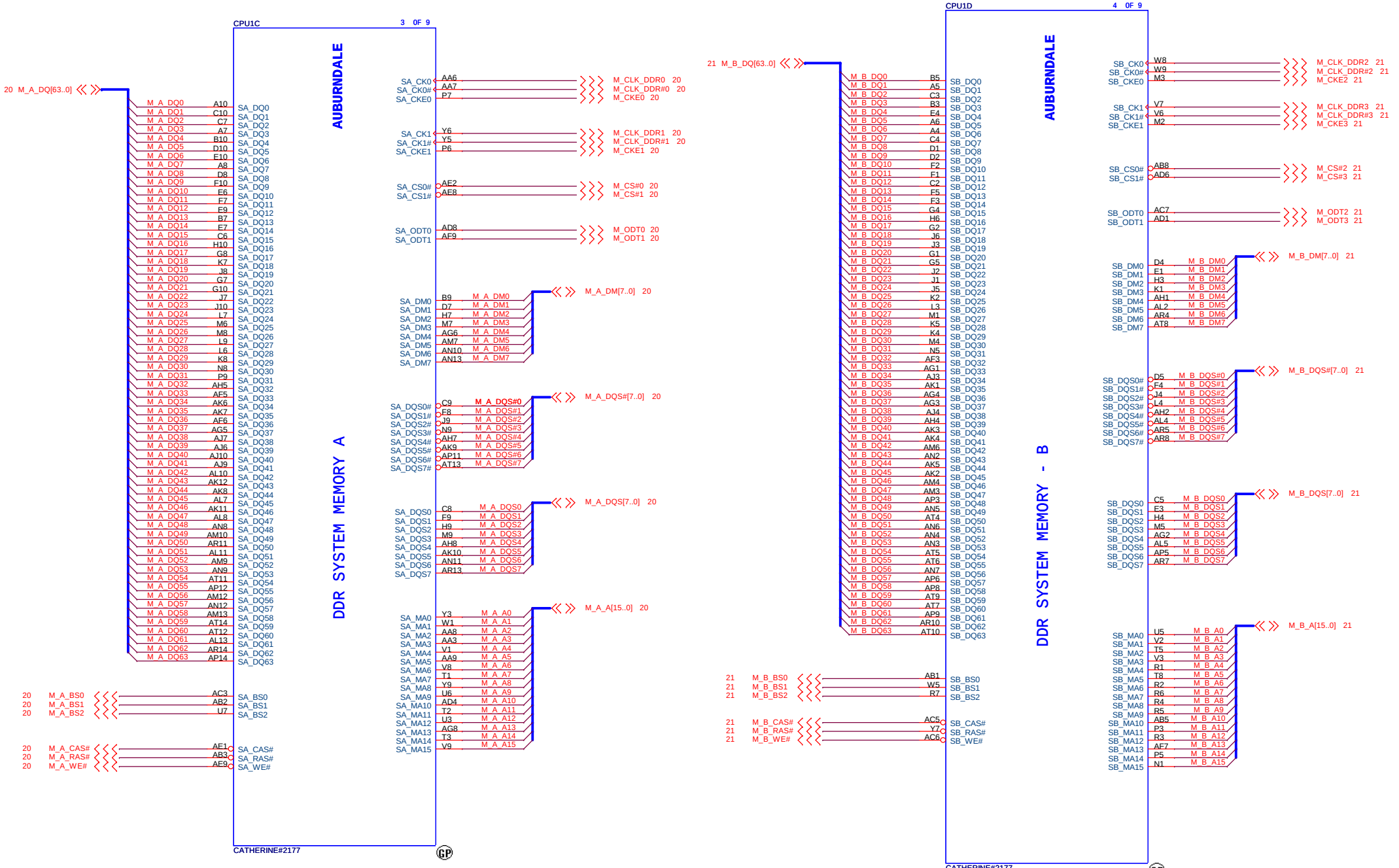

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Title: CPU (3/7)	
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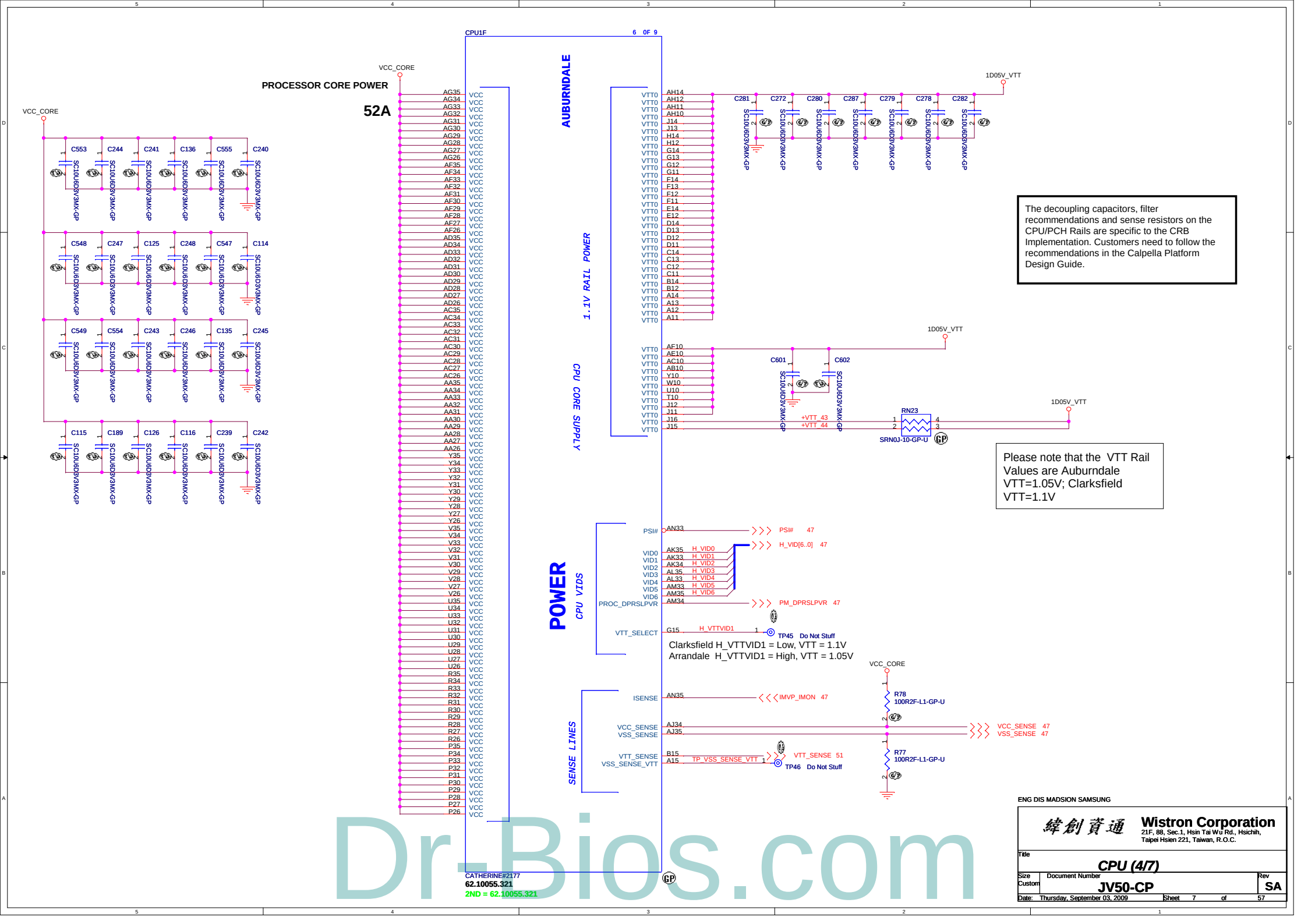
PROCESSOR CORE POWER
52A
CPU1F
6 0F 9
AUBURNDALE
1.1V RAIL POWER
CPU CORE SUPPLY
POWER
CPU VIDS
SENSE LINES
VCC_CORE
1D05V_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
TP45 Do Not Stuff
TP46 Do Not Stuff
RN23
SRN0J-10-GP-U
R78 100R2F-L1-GP-U
R77 100R2F-L1-GP-U
CATHERINE#2177
62.10055.321
2ND = 62.10055.321
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Title
CPU (4/7)
Size Custom
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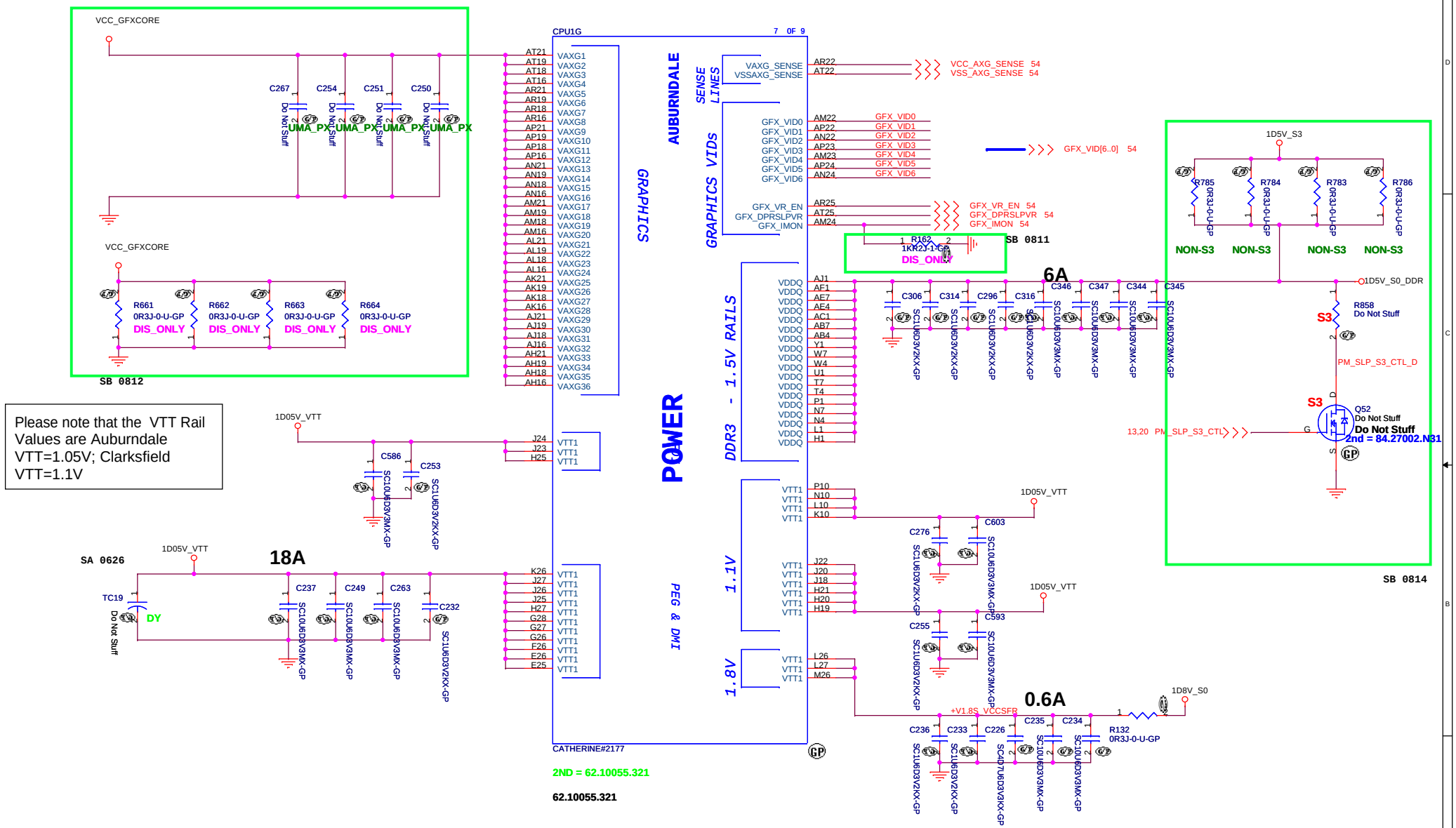

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Title: CPU (5/7)

Size: A3 | Document Number: JV50-CP | Rev: SA

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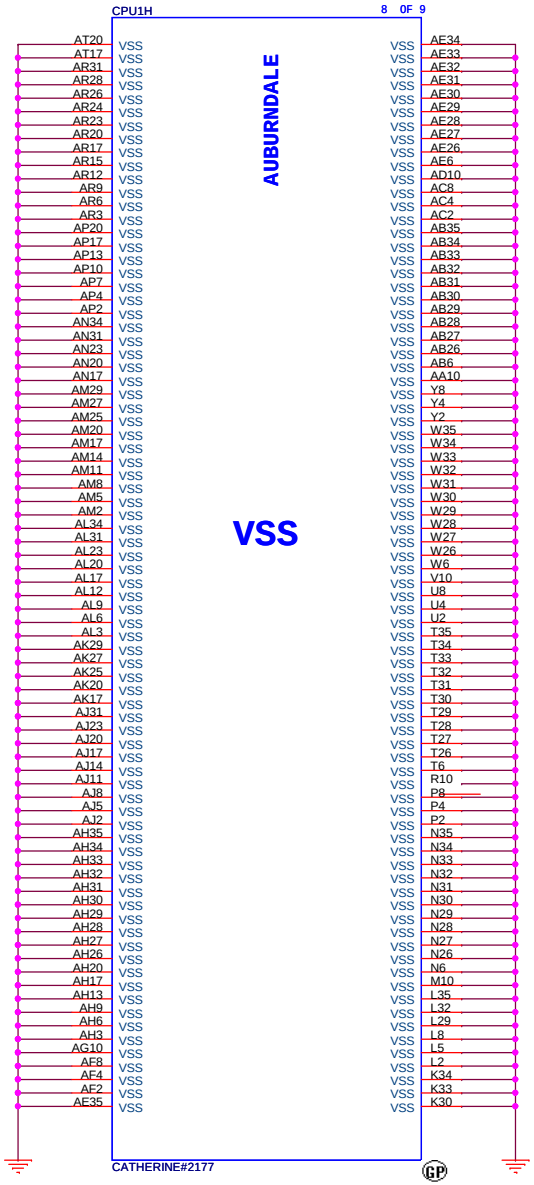

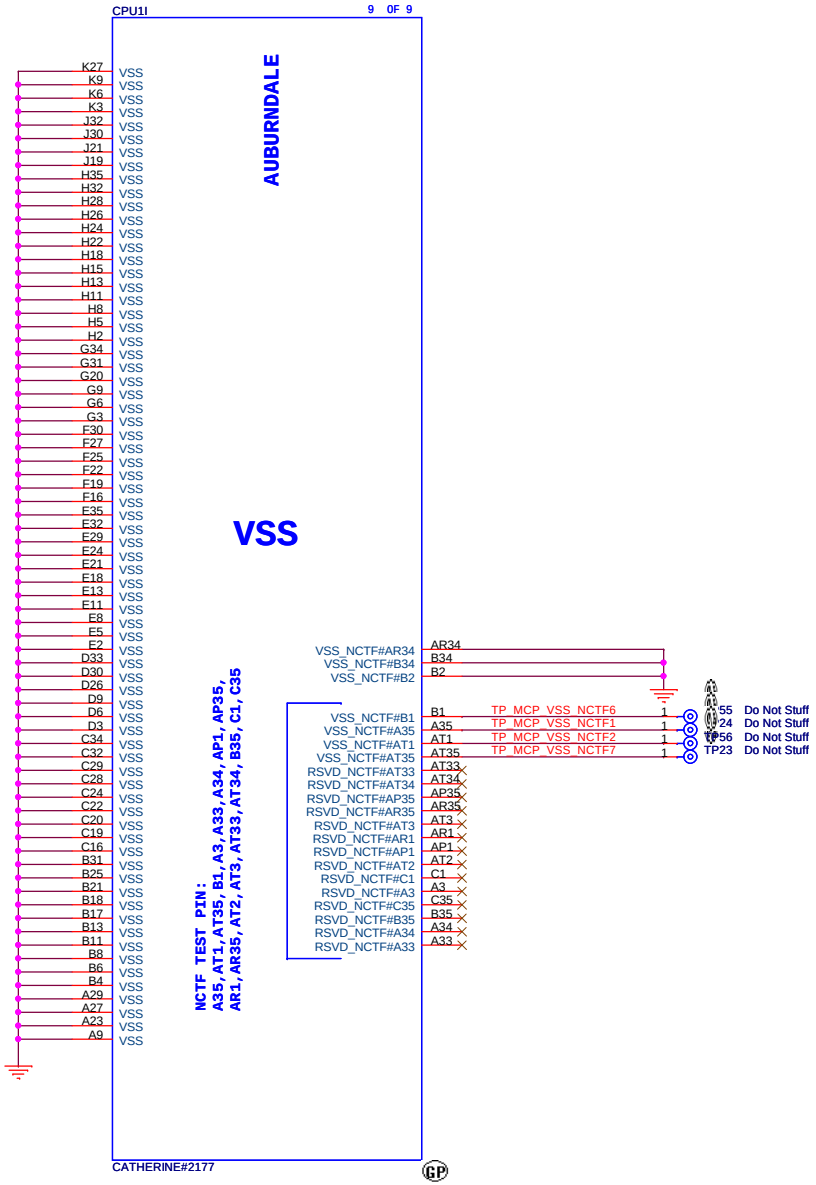

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Title: CPU (6/7)

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SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor

SB 0817

20 M_VREF_DQ_DIMM0
21 M_VREF_DQ_DIMM1

RN28 DY
1 4 H_RSVD9_R
2 3 H_RSVD10_R
Do Not Stuff GP

CPU1E 5 OF 9

AUBURNDALE

AP25	RSVD#AP25
AL25	RSVD#AL25
AL24	RSVD#AL24
AL22	RSVD#AL22
AJ33	RSVD#AJ33
AG9	RSVD#AG9
M27	RSVD#M27
L28	RSVD#L28
J17	SA_DIMM_VREF#
H17	SB_DIMM_VREF#
G25	RSVD#G25
G17	RSVD#G17
E31	RSVD#E31
E30	RSVD#E30

AJ13	RSVD#AJ13
AJ12	RSVD#AJ12
AH25	RSVD#AH25
AK26	RSVD#AK26
AL26	RSVD#AL26
AR2	RSVD_NCTF#AR2
AJ26	RSVD#AJ26
AJ27	RSVD#AJ27

RESERVED

Do Not Stuff TP38	CFG0	AM30 CFG0
Do Not Stuff TP29	CFG1	AM28 CFG1
	CFG2	AP31 CFG2
	CFG3	AL32 CFG3
	CFG4	AL30 CFG4
Do Not Stuff TP32	CFG5	AM31 CFG5
Do Not Stuff TP34	CFG6	AN29 CFG6
	CFG7	AM32 CFG7
Do Not Stuff TP30	CFG8	AK32 CFG8
Do Not Stuff TP33	CFG9	AK31 CFG9
Do Not Stuff TP39	CFG10	AK28 CFG10
Do Not Stuff TP40	CFG11	AJ28 CFG11
Do Not Stuff TP31	CFG12	AN30 CFG12
Do Not Stuff TP28	CFG13	AN32 CFG13
Do Not Stuff TP27	CFG14	AJ32 CFG14
Do Not Stuff TP36	CFG15	AJ29 CFG15
Do Not Stuff TP37	CFG16	AJ30 CFG16
Do Not Stuff TP35	CFG17	AK30 CFG17
	RSVD_TP#H16	H16

AL28	RSVD#AL28
AL29	RSVD#AL29
AP30	RSVD#AP30
AP32	RSVD#AP32
AL27	RSVD#AL27
AT31	RSVD#AT31
AT32	RSVD#AT32
AP33	RSVD#AP33
AR33	RSVD#AR33
AR32	RSVD#AR32
E15	RSVD_TP#E15
F15	RSVD_TP#F15
A2	KEY
D15	RSVD#D15
C15	RSVD#C15
AJ15	RSVD#AJ15
AH15	RSVD#AH15

RSVD64_R 1 4 RSVD65_R
RN20
SRN0J-10-GP-U GP

RN17
1 4 H_RSVD17_R
2 3 H_RSVD18_R
SRN0J-10-GP-U GP

B19	RSVD#B19
A19	RSVD#A19
A20	RSVD#A20
B20	RSVD#B20
U9	RSVD#U9
T9	RSVD#T9
AC9	RSVD#AC9
AB9	RSVD#AB9

AA5	RSVD_TP#AA5
AA4	RSVD_TP#AA4
R8	RSVD_TP#R8
AD3	RSVD_TP#AD3
AD2	RSVD_TP#AD2
AA2	RSVD_TP#AA2
AA1	RSVD_TP#AA1
R9	RSVD_TP#R9
AG7	RSVD_TP#AG7
AE3	RSVD_TP#AE3
V4	RSVD_TP#V4
V5	RSVD_TP#V5
N2	RSVD_TP#N2
AD5	RSVD_TP#AD5
AD7	RSVD_TP#AD7
W3	RSVD_TP#W3
W2	RSVD_TP#W2
N3	RSVD_TP#N3
AE5	RSVD_TP#AE5
AD9	RSVD_TP#AD9
J29	RSVD#J29
J28	RSVD#J28

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

VSS AP34 RSVD_VSS 1 R73 0R2J-2-GP

CATHERINE#2177 GP

2ND = 62.10055.321

62.10055.321

CFG0 1 R74 Do Not Stuff DY 2 GP

SA 0623

CFG3 1 R76 3KR2F-GP 2 GP

CFG4 1 R119 Do Not Stuff DY 2 GP

CFG7 1 R75 Do Not Stuff DY 2 GP

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

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integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

PCH1A 1 OF 10

RTC / LPC / IHDA / SATA / JTAG / SPI

IBEXPEAK-M-GP-NF

SA 0629 RF

SB 0825

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

SA 0709

When unused all JTAG pins may be NC

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

HDD

ODD

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Title: PCH (1/9)

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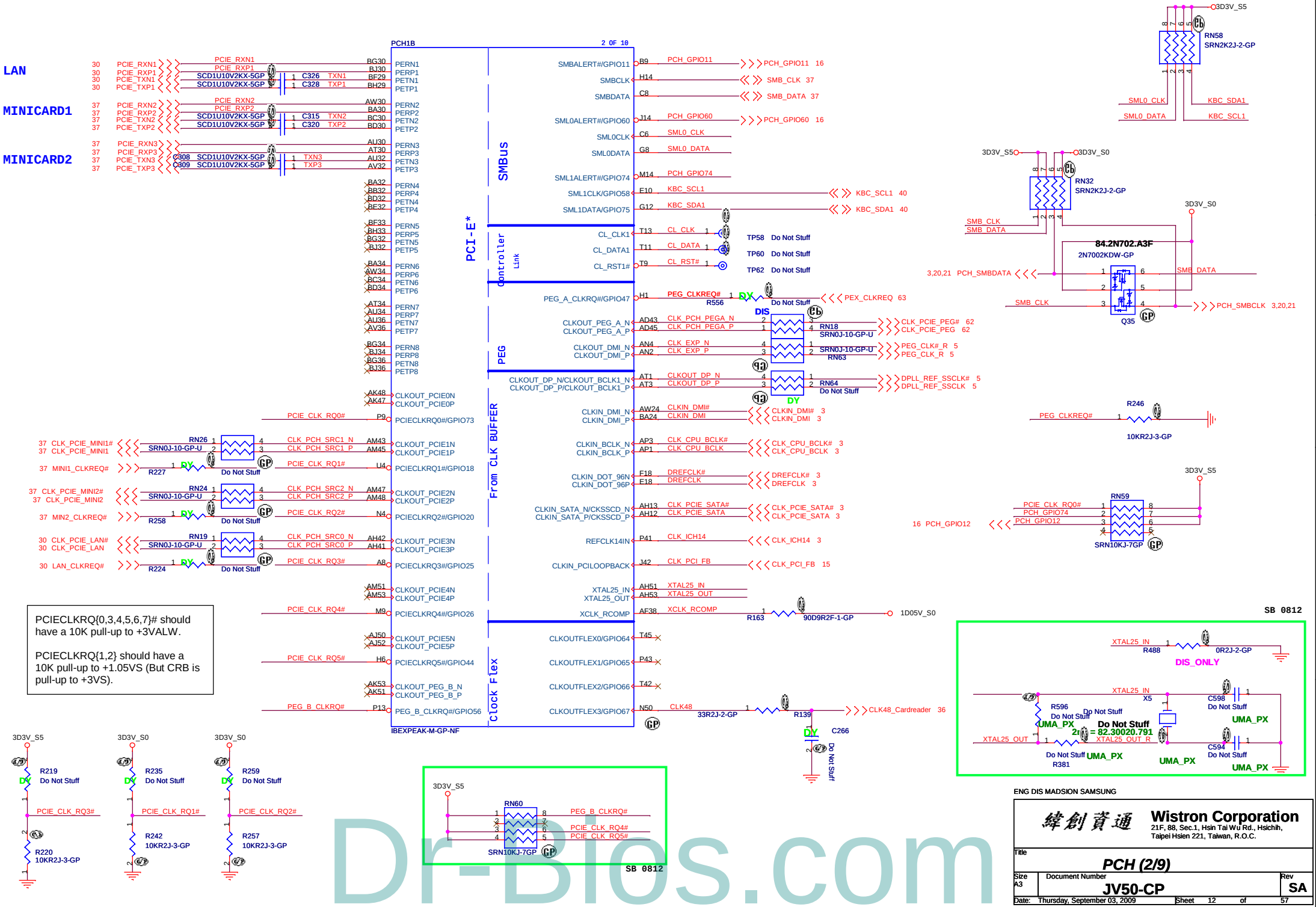
LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
IBEXPEAK-M-GP-NF
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
SB 0812
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Title
PCH (2/9)
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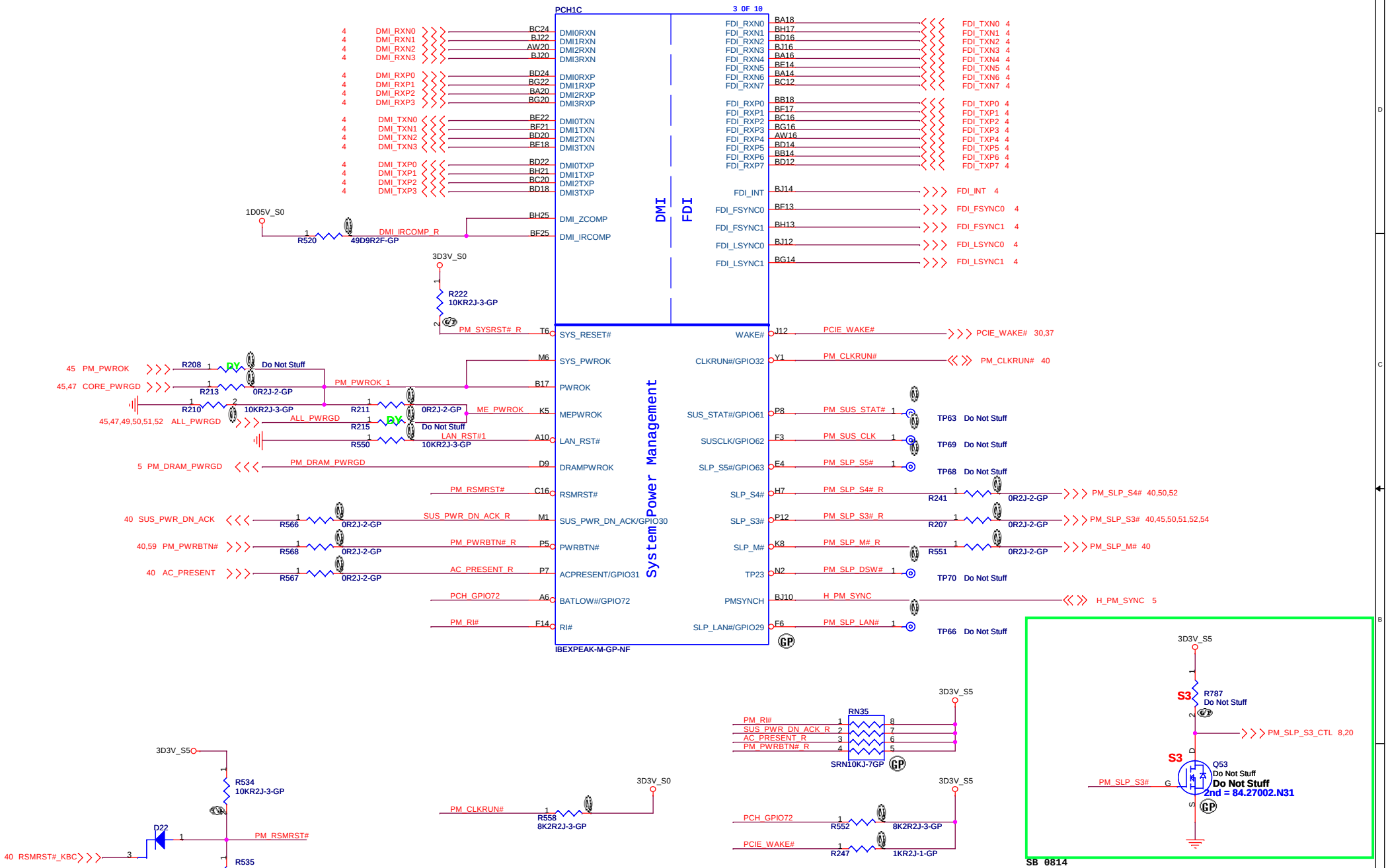

SB 0814

ENG DIS MADSION SAMSUNG

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Title	PCH (3/9)	
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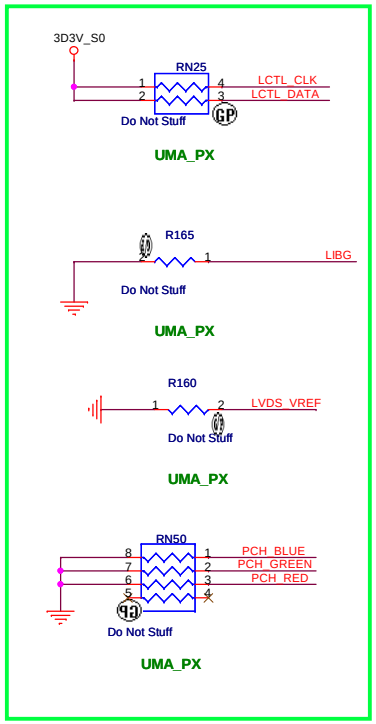
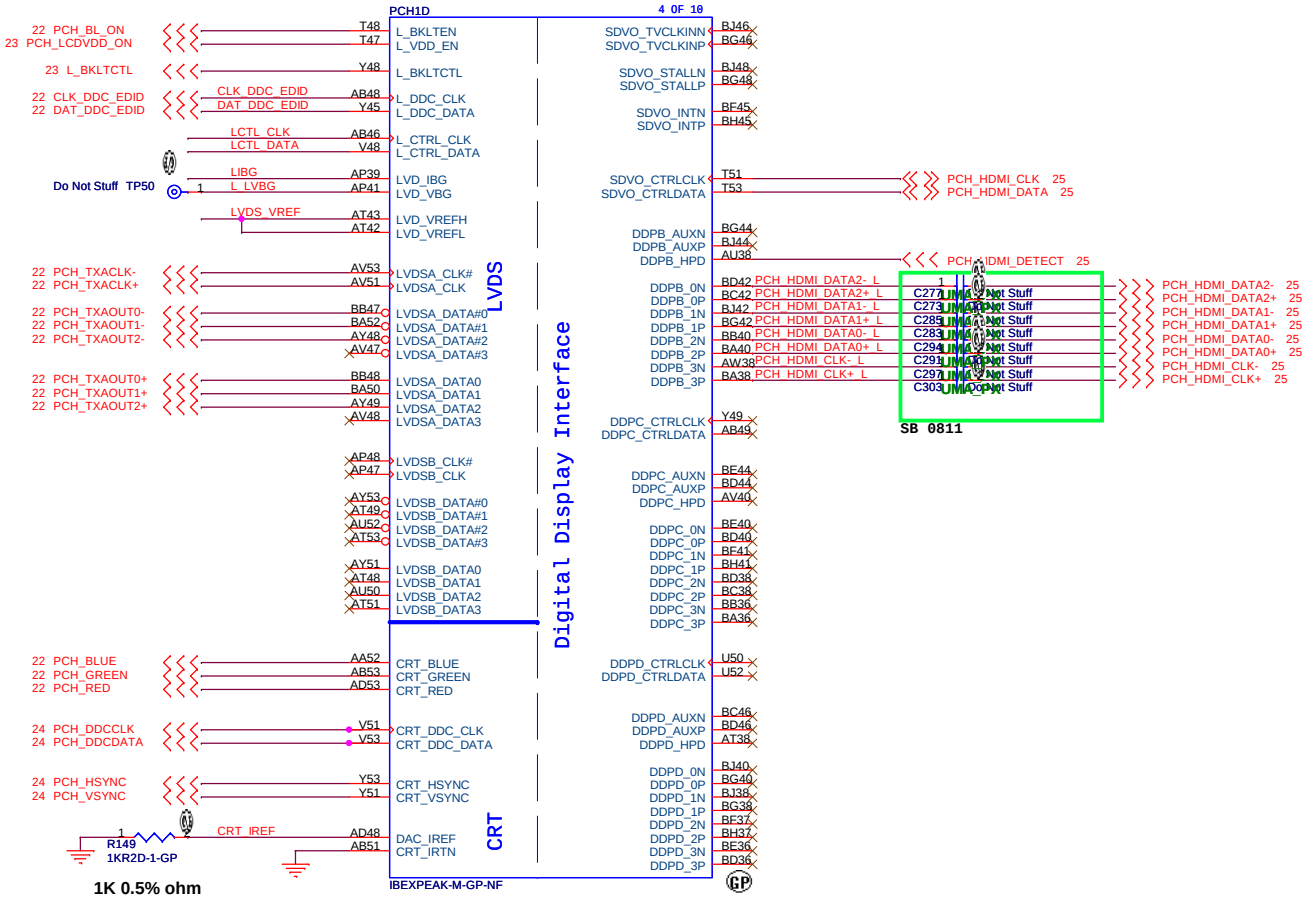


SB 0811



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Title: PCH (4/9)

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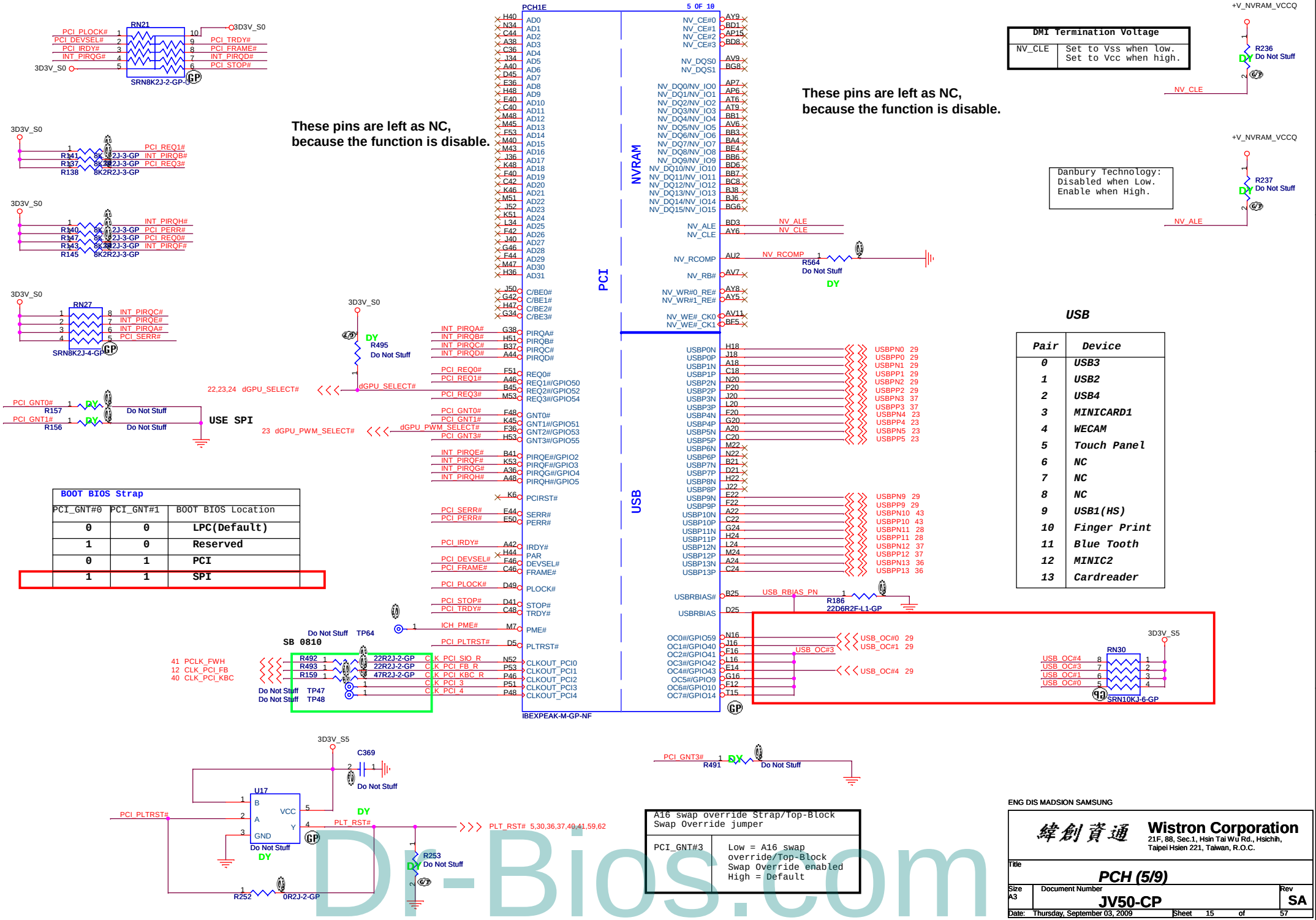
PCH1E
5 OF 10
PCI
NVRAM
USB
IBEXPEAK-M-GP-NF
These pins are left as NC, because the function is disable.
These pins are left as NC, because the function is disable.
DMI Termination Voltage
NV_CLE | Set to Vss when low. Set to Vcc when high.
Danbury Technology: Disabled when Low. Enable when High.
USB
Pair | Device
0 | USB3
1 | USB2
2 | USB4
3 | MINICARD1
4 | WECAM
5 | Touch Panel
6 | NC
7 | NC
8 | NC
9 | USB1(HS)
10 | Finger Print
11 | Blue Tooth
12 | MINIC2
13 | Cardreader
USE SPI
BOOT BIOS Strap
PCI_GNT#0 | PCI_GNT#1 | BOOT BIOS Location
0 | 0 | LPC(Default)
1 | 0 | Reserved
0 | 1 | PCI
1 | 1 | SPI
SB 0810
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled High = Default
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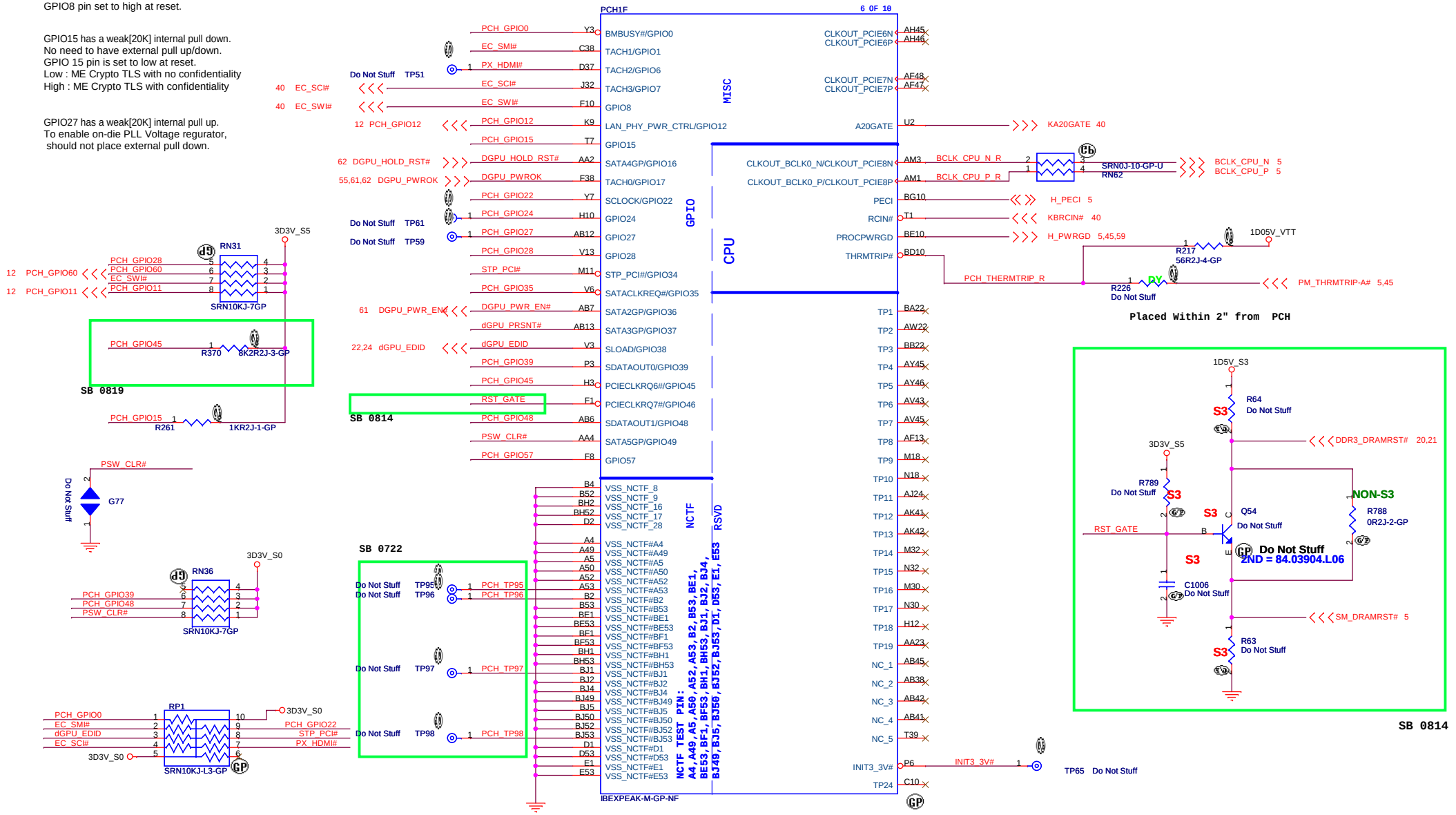
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



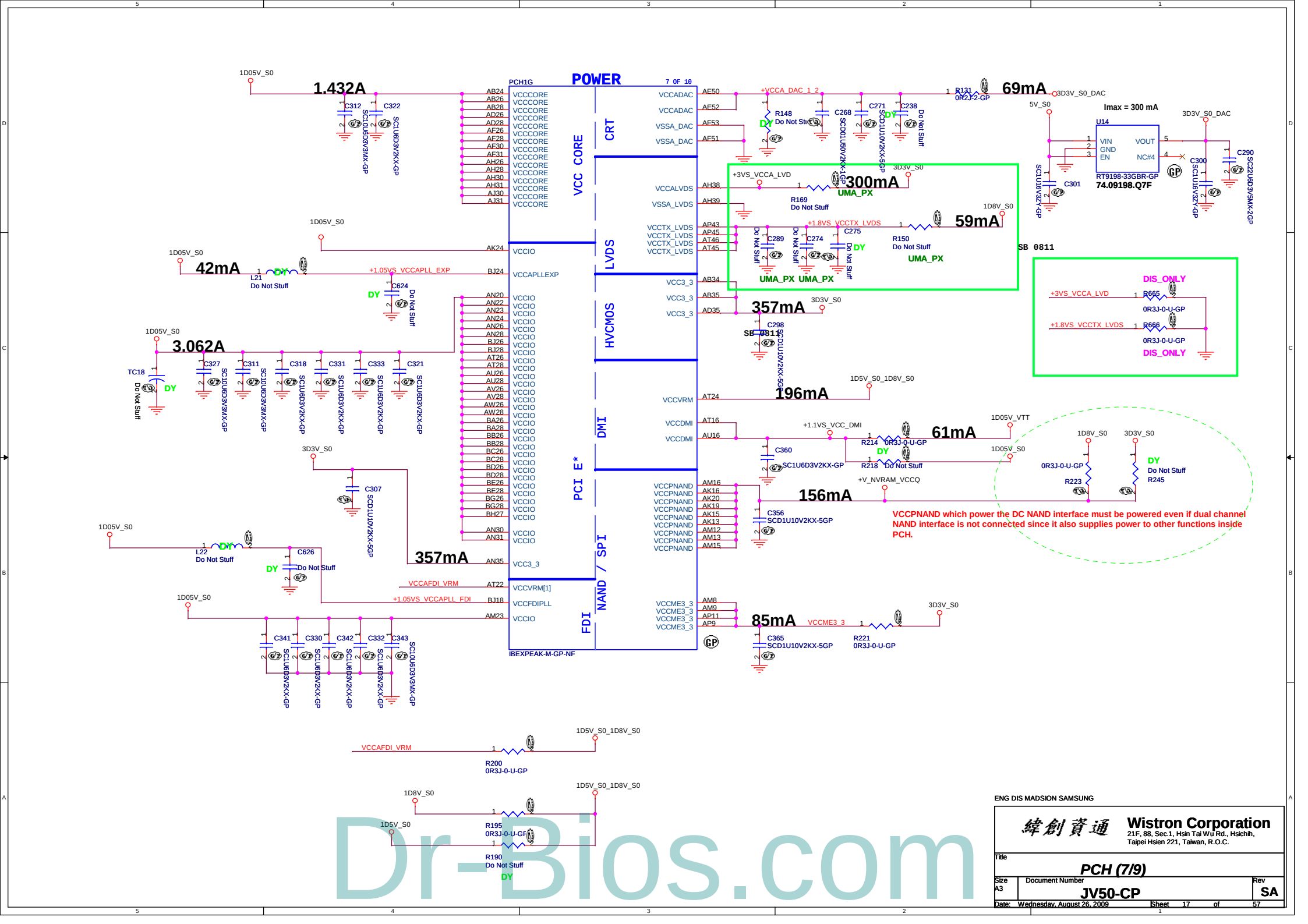
ENG DIS MADSION SAMSUNG

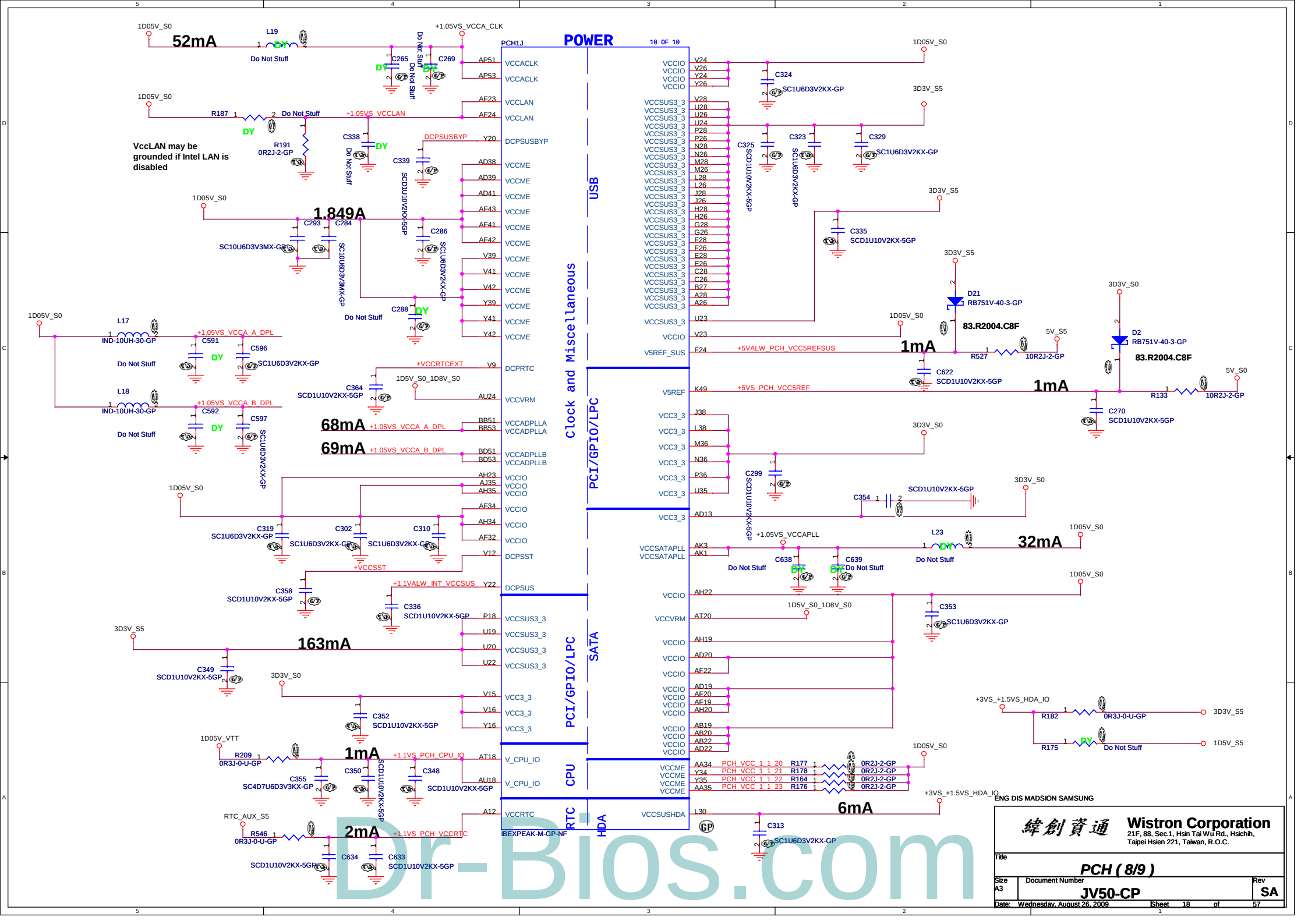
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

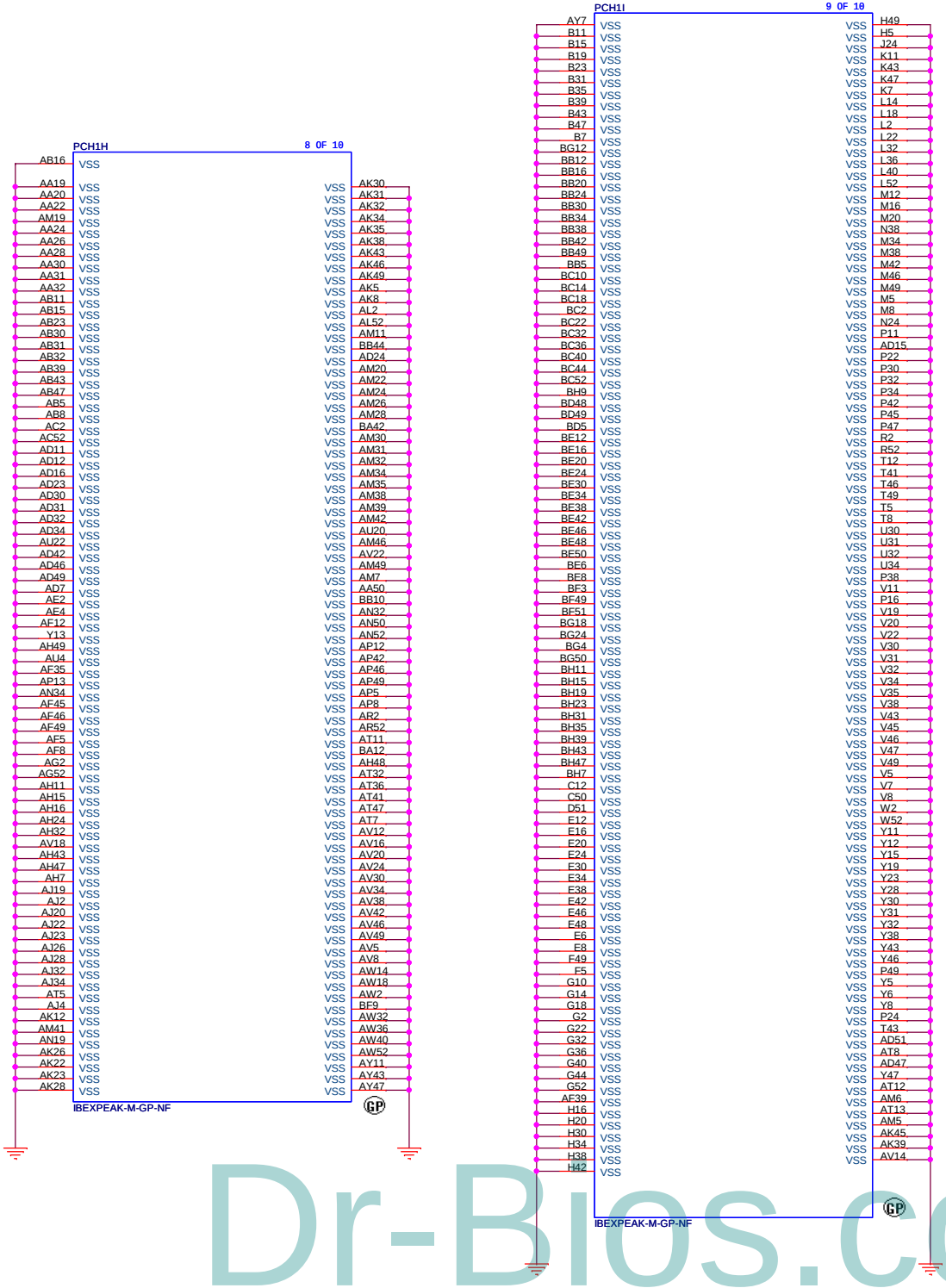
Title: PCH (6/9)

Size: A3 | Document Number: JV50-CP | Rev: SA

Date: Thursday, September 03, 2009 | Sheet 16 of 57


POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
357mA
196mA
61mA
156mA
85mA
69mA
300mA
59mA
Imax = 300 mA
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
IBEXPEAK-M-GP-NF
Dr-Bios.com
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (7/9)
JV50-CP
SA
Wednesday, August 26, 2009
17
57


POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
163mA
68mA
69mA
1mA
2mA
6mA
32mA
83.R2004.C8F
VccLAN may be grounded if Intel LAN is disabled
Do Not Stuff
DY
IBEXPEAK-M-GP-NF
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size A3
Document Number
JV50-CP
Rev SA
Date: Wednesday, August 26, 2009
Sheet 18 of 57



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Title: ***PCH (9/9)***

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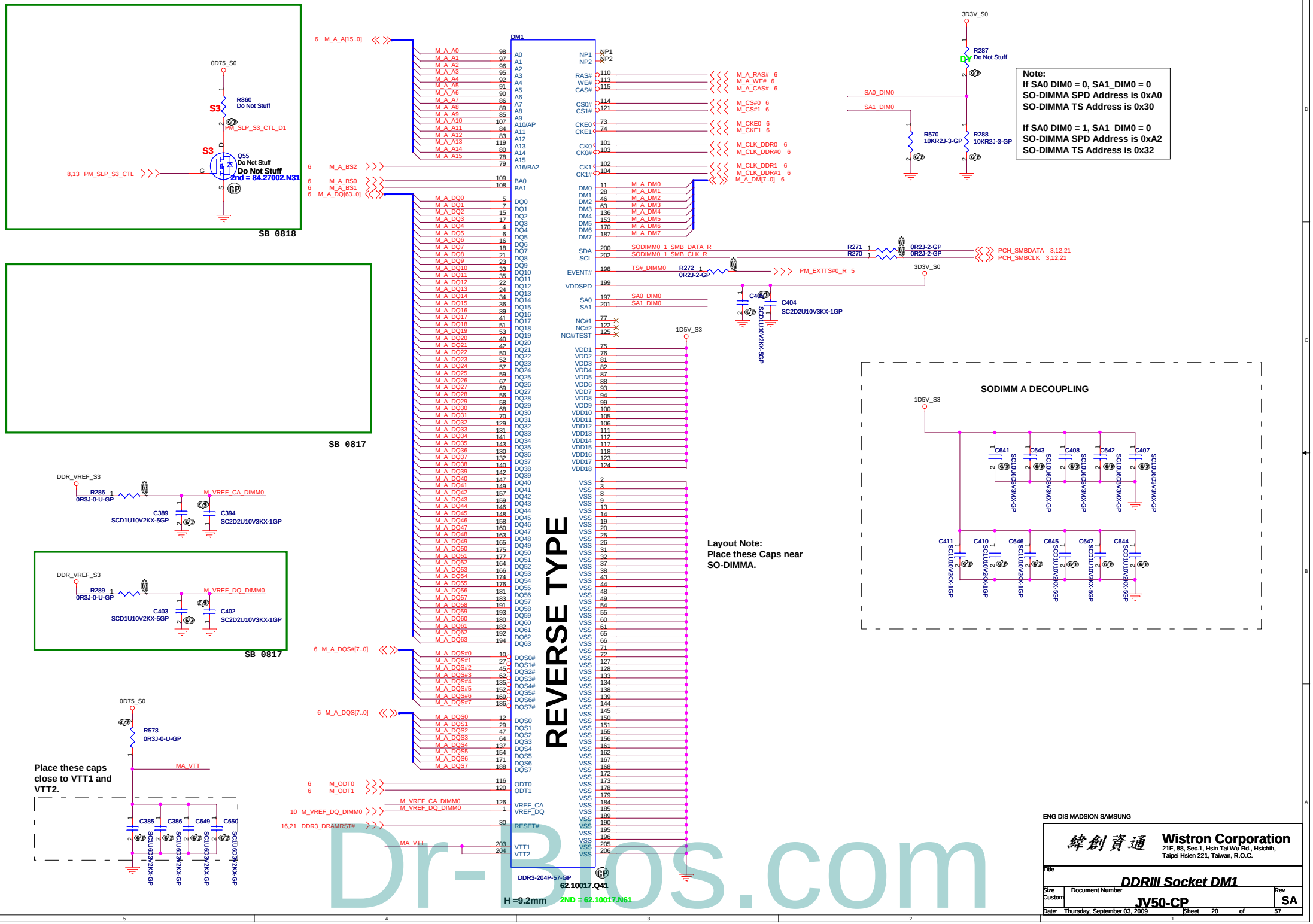
Date: Tuesday, August 18, 2009 Sheet 19 of 57



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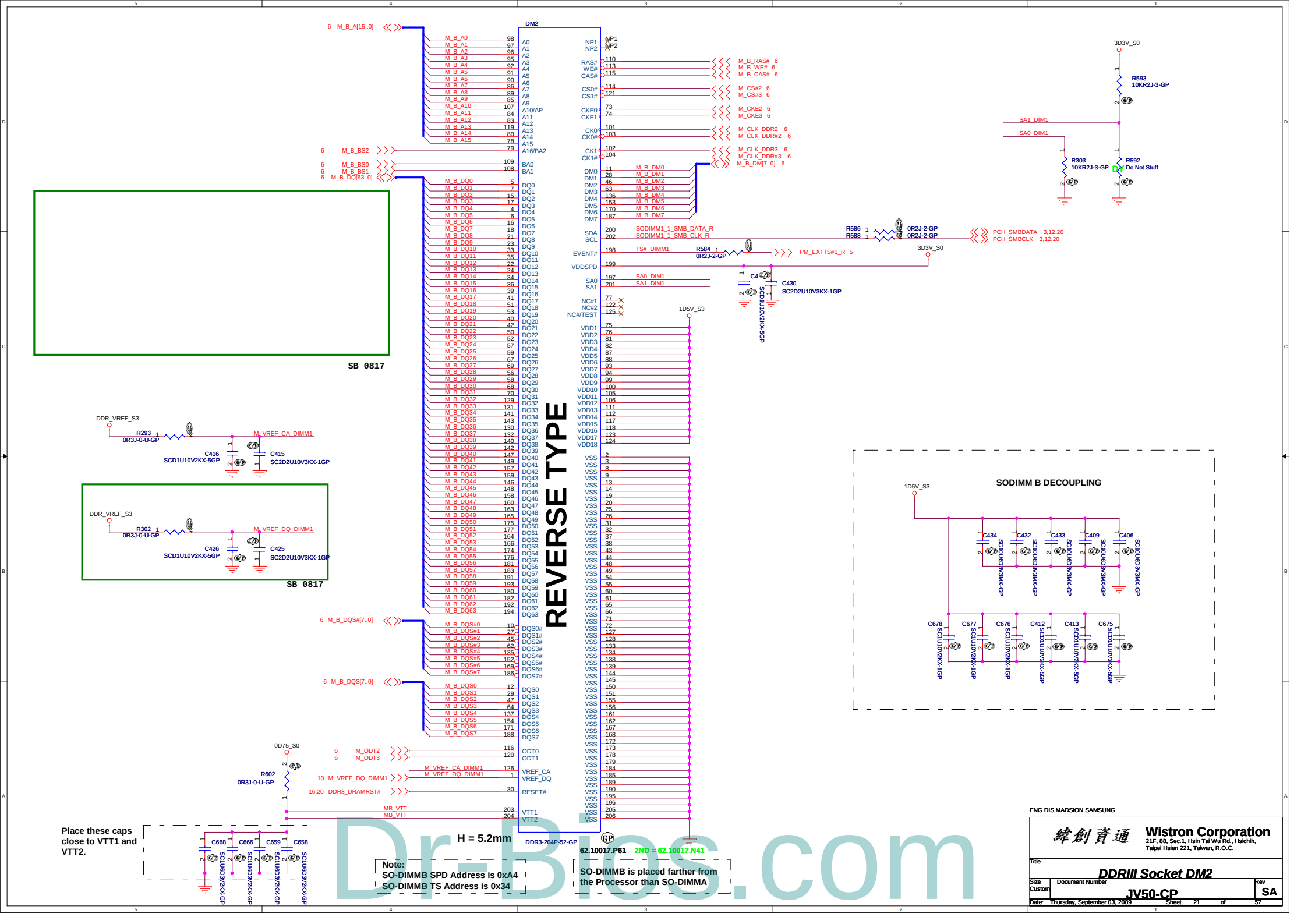
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII Socket DM1

Size: Custom | Document Number: JV50-CP | Rev: SA

Date: Thursday, September 03, 2009 | Sheet 20 of 57


DM2
REVERSE TYPE
DDR3-204P-52-GP
62.10017.P61
2ND = 62.10017.N41
H = 5.2mm
SB 0817
SB 0817
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
ENG DIS MADSION SAMSUNG
Wistron Corporation
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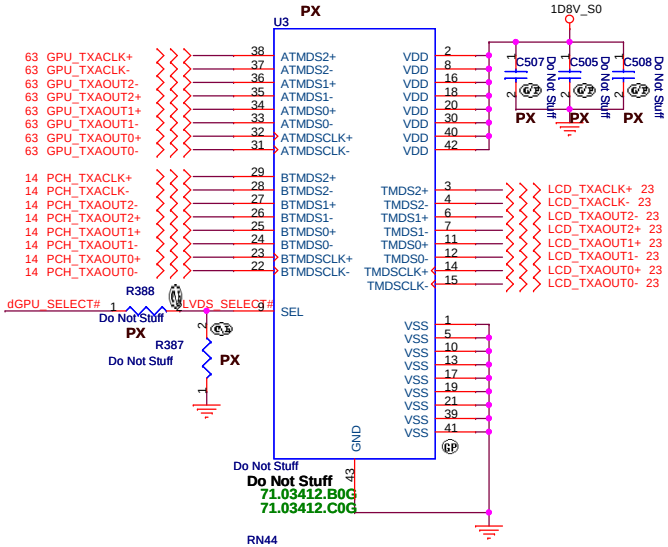
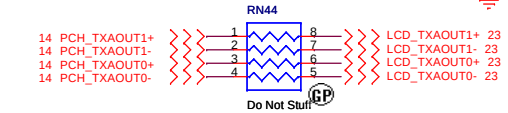
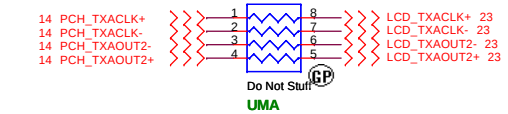
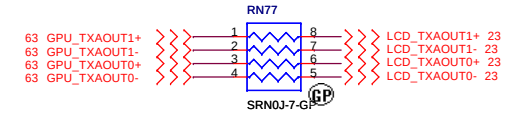
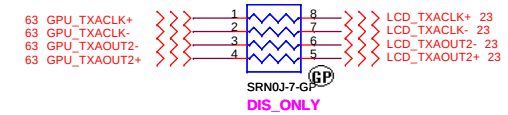
Taipei Hsien 221, Taiwan, R.O.C.
DDRIII Socket DM2
JV50-CP
SA
Thursday, September 03, 2009
21
57

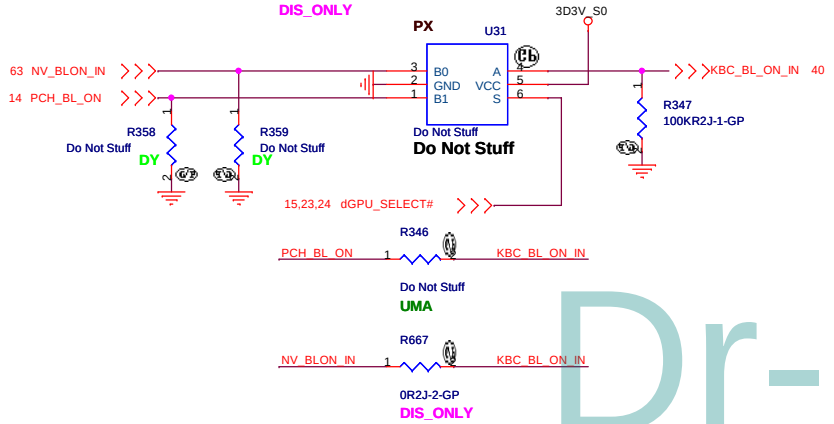


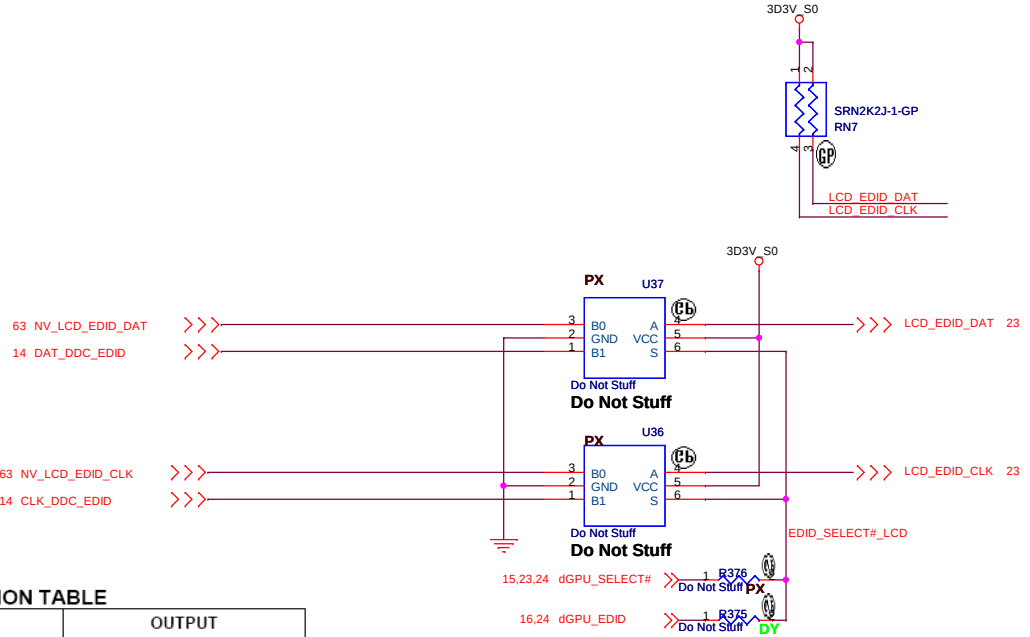


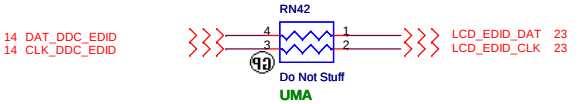


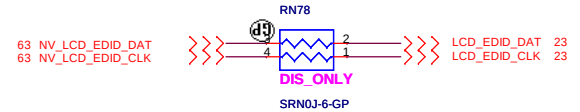






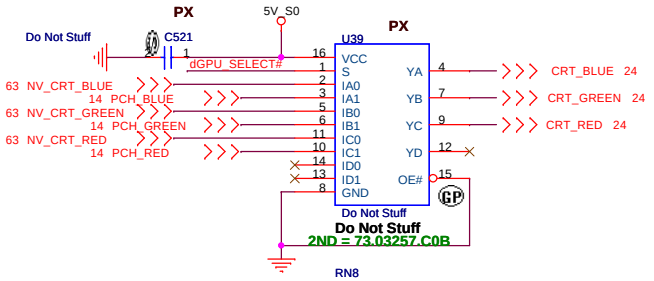


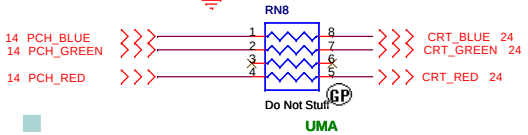


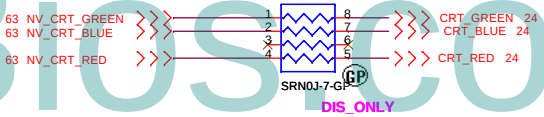


FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-







$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PX SWITCH**

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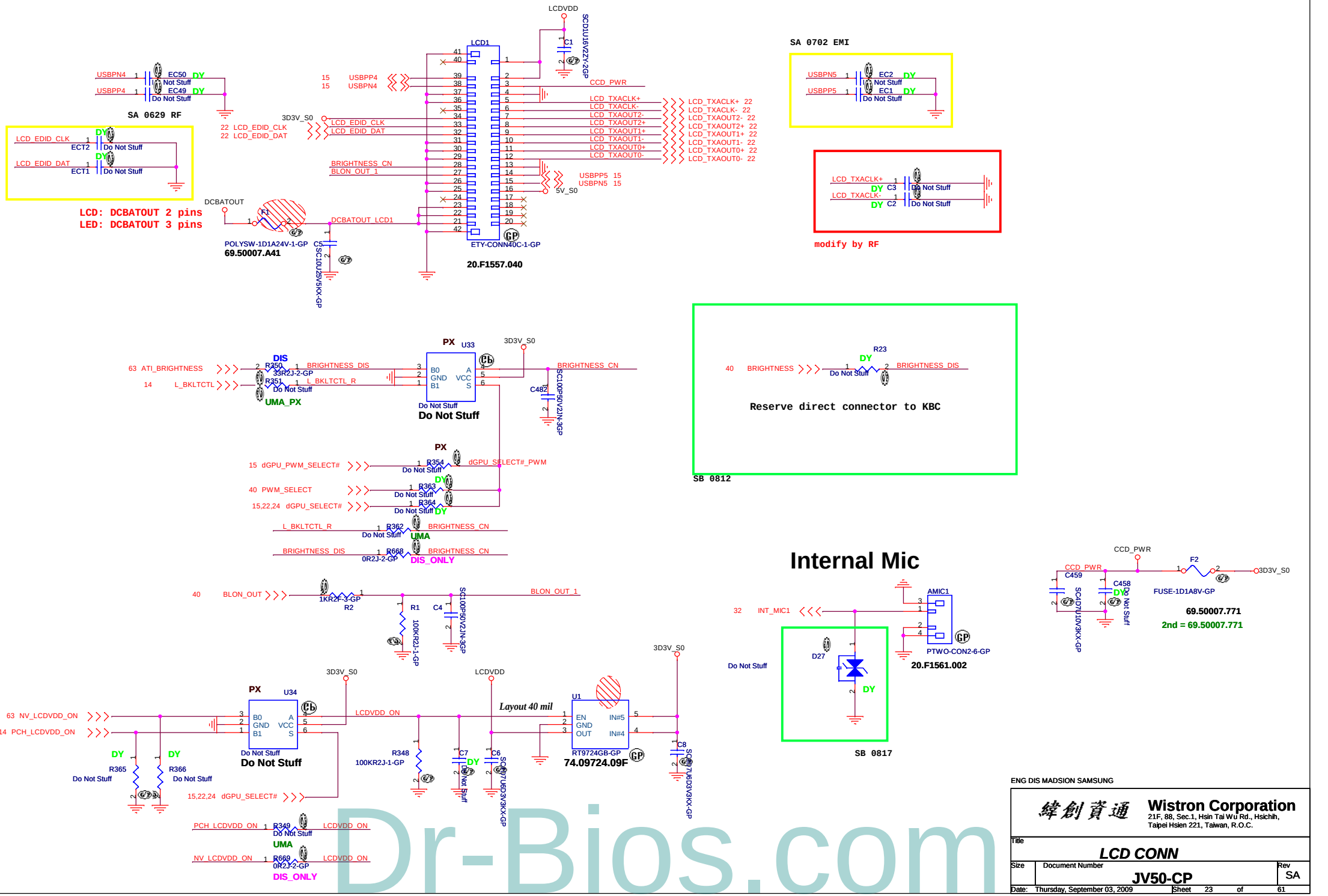
Date: Thursday, September 03, 2009 | Sheet 22 of 57

LCD/INVERTER/CCD CONN



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Title: LCD CONN

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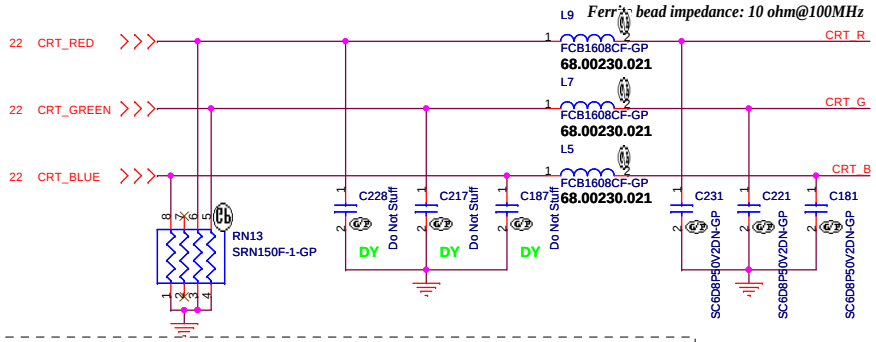
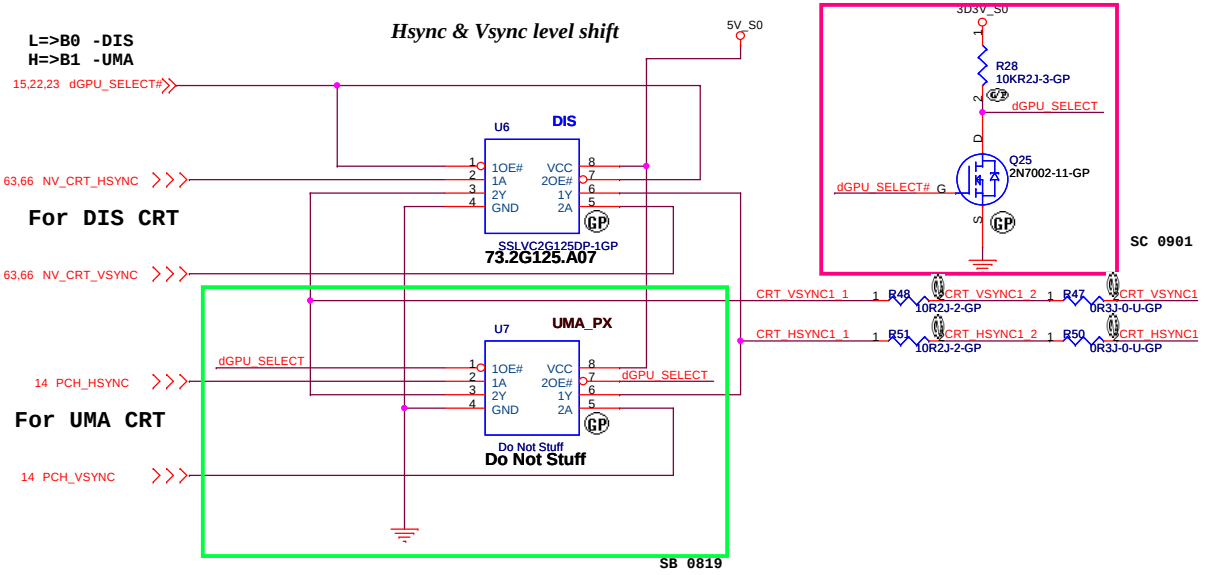
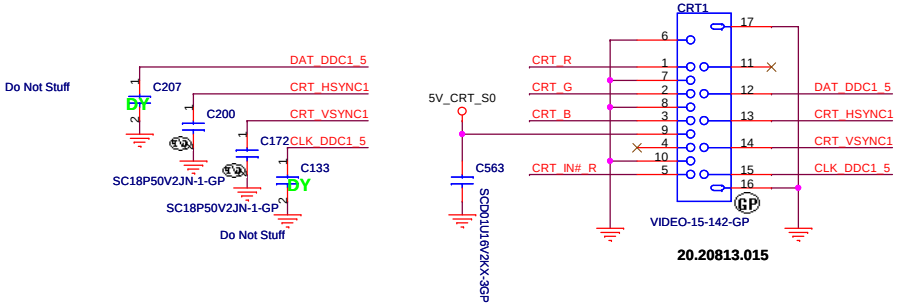
Layout Note:
Place these resistors close to the CRT-out connector

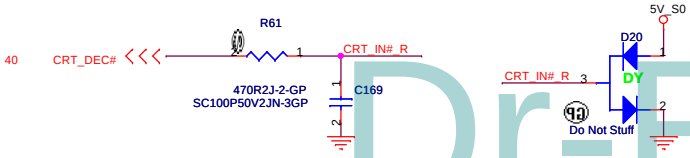


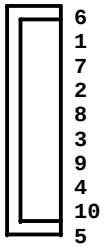
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



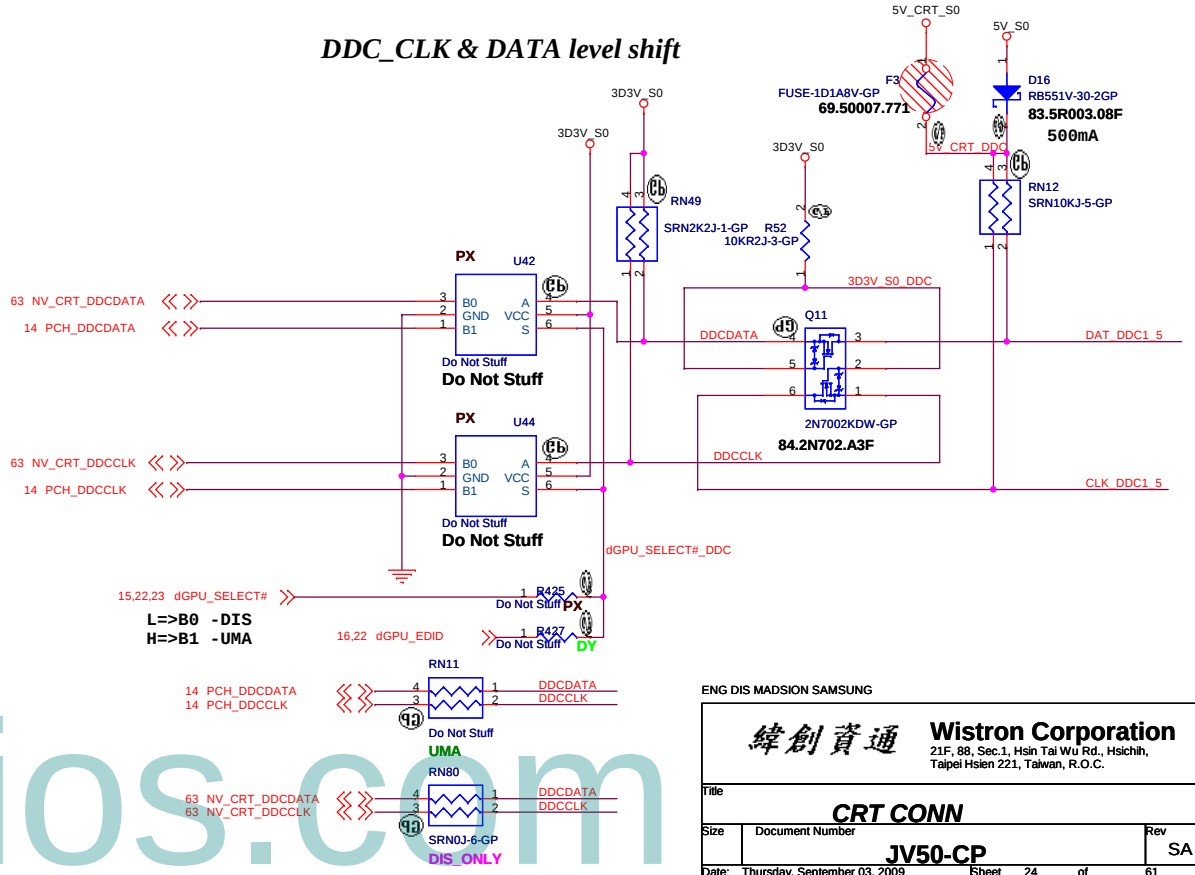
CRT I/F & CONNECTOR







DDC_CLK & DATA level shift



ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT CONN**

Size | Document Number: **JV50-CP** | Rev: SA

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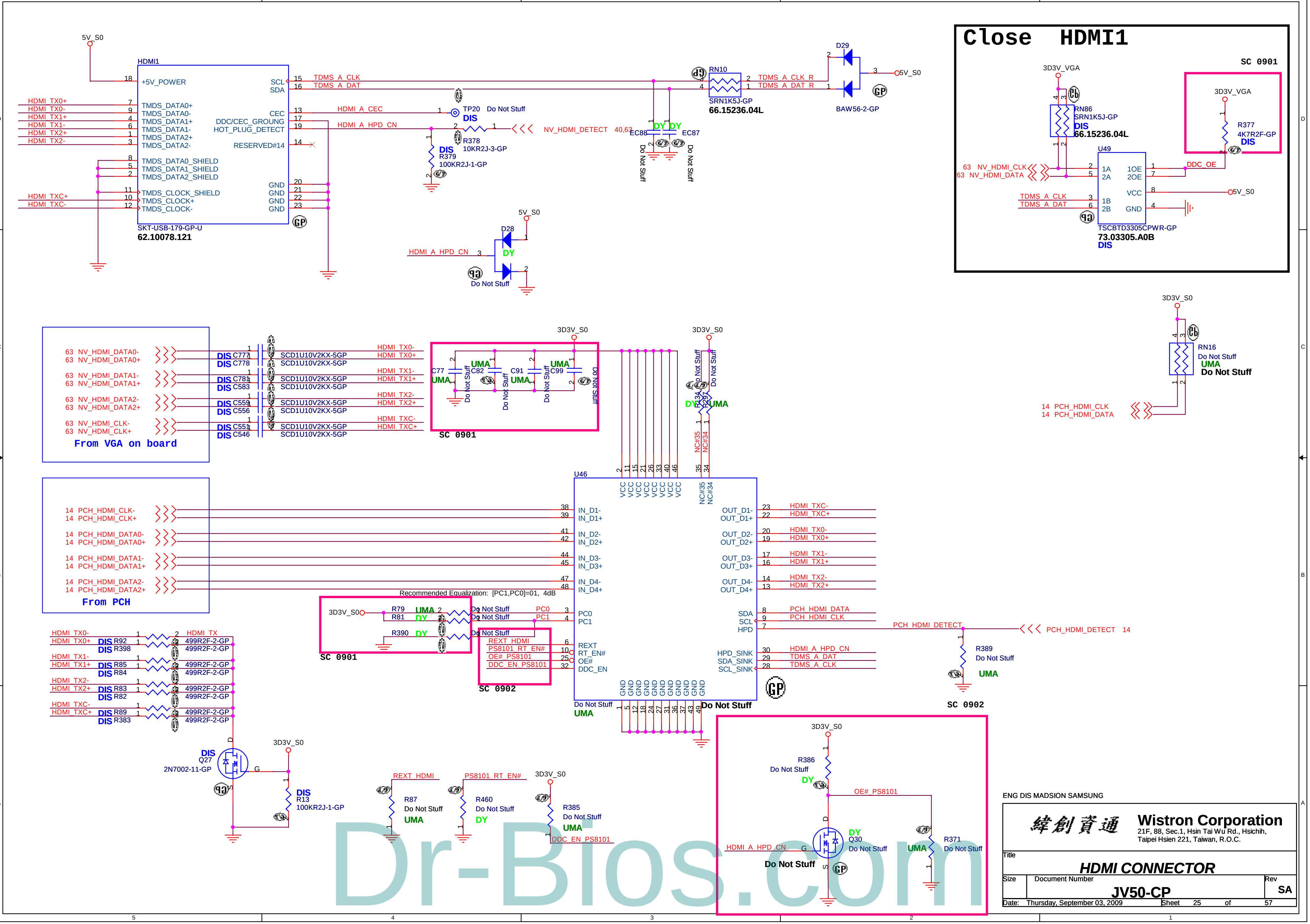
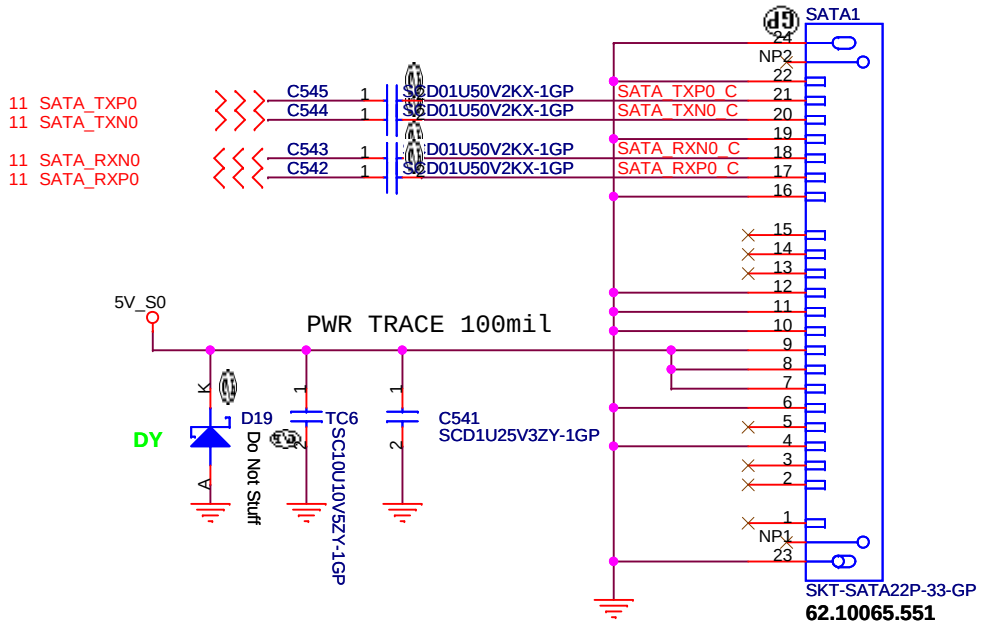


Close HDMI1
SC 0901
SC 0902
HDMI1
SKT-USB-179-GP-U
62.10078.121
+5V_POWER
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
CEC
DDC/CEC_GROUND
HOT_PLUG_DETECT
RESERVED#14
GND
5V_S0
3D3V_S0
3D3V_VGA
HDMI_TX0+
HDMI_TX0-
HDMI_TX1+
HDMI_TX1-
HDMI_TX2+
HDMI_TX2-
HDMI_TXC+
HDMI_TXC-
TDMS_A_CLK
TDMS_A_DAT
TDMS_A_CLK_R
TDMS_A_DAT_R
HDMI_A_CEC
HDMI_A_HPD_CN
NV_HDMI_DETECT 40,63
TP20 Do Not Stuff
DIS
R378 10KR2J-3-GP
R379 100KR2J-1-GP
RN10 SRN1K5J-GP
66.15236.04L
D29 BAW56-2-GP
EC88 EC87 Do Not Stuff
D28 DY
Do Not Stuff
RN86 SRN1K5J-GP DIS 66.15236.04L
R377 4K7R2F-GP DIS
U49 TSCBTD3305CPWR-GP
73.03305.A0B DIS
1A 2A 1B 2B 1OE 2OE VCC GND
63 NV_HDMI_CLK
63 NV_HDMI_DATA
DDC_OE
63 NV_HDMI_DATA0-
63 NV_HDMI_DATA0+
63 NV_HDMI_DATA1-
63 NV_HDMI_DATA1+
63 NV_HDMI_DATA2-
63 NV_HDMI_DATA2+
63 NV_HDMI_CLK-
63 NV_HDMI_CLK+
From VGA on board
DIS C777 C778 C781 C583 C559 C556 C551 C546
SCD1U10V2KX-5GP
C77 C82 C91 C99 UMA Do Not Stuff
R34 R37 DY UMA
NC#35 NC#34
RN16 Do Not Stuff UMA Do Not Stuff
14 PCH_HDMI_CLK
14 PCH_HDMI_DATA
14 PCH_HDMI_CLK-
14 PCH_HDMI_CLK+
14 PCH_HDMI_DATA0-
14 PCH_HDMI_DATA0+
14 PCH_HDMI_DATA1-
14 PCH_HDMI_DATA1+
14 PCH_HDMI_DATA2-
14 PCH_HDMI_DATA2+
From PCH
U46
VCC
IN_D1- IN_D1+ IN_D2- IN_D2+ IN_D3- IN_D3+ IN_D4- IN_D4+
OUT_D1- OUT_D1+ OUT_D2- OUT_D2+ OUT_D3- OUT_D3+ OUT_D4- OUT_D4+
PC0 PC1 REXT RT_EN# OE# DDC_EN
SDA SCL HPD HPD_SINK SDA_SINK SCL_SINK
Recommended Equalization: [PC1,PC0]=01, 4dB
R79 UMA R81 DY R390 DY Do Not Stuff
REXT_HDMI
PS8101_RT_EN#
OE#_PS8101
DDC_EN_PS8101
PCH_HDMI_DATA
PCH_HDMI_CLK
PCH_HDMI_DETECT
14 PCH_HDMI_DETECT
R389 Do Not Stuff UMA
HDMI_TX
R92 R398 R85 R84 R83 R82 R89 R383 DIS
499R2F-2-GP
Q27 2N7002-11-GP DIS
R13 100KR2J-1-GP DIS
R87 Do Not Stuff UMA
R460 Do Not Stuff DY
R385 Do Not Stuff UMA
R386 Do Not Stuff DY
Q30 DY Do Not Stuff
R371 Do Not Stuff UMA
Do Not Stuff
ENG DIS MADSION SAMSUNG
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title HDMI CONNECTOR
Size Document Number JV50-CP Rev SA
Date: Thursday, September 03, 2009 Sheet 25 of 57

SATA Connector



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD CONN***

Size	Document Number	Rev
	JV50-CP	SA

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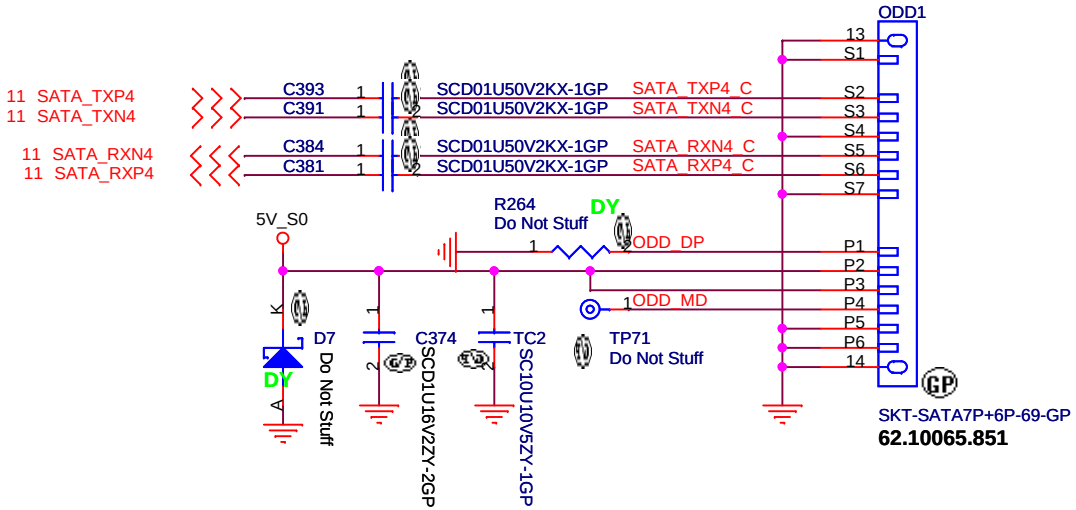
ODD Connector



ENG DIS MADSION SAMSUNG

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ODD	
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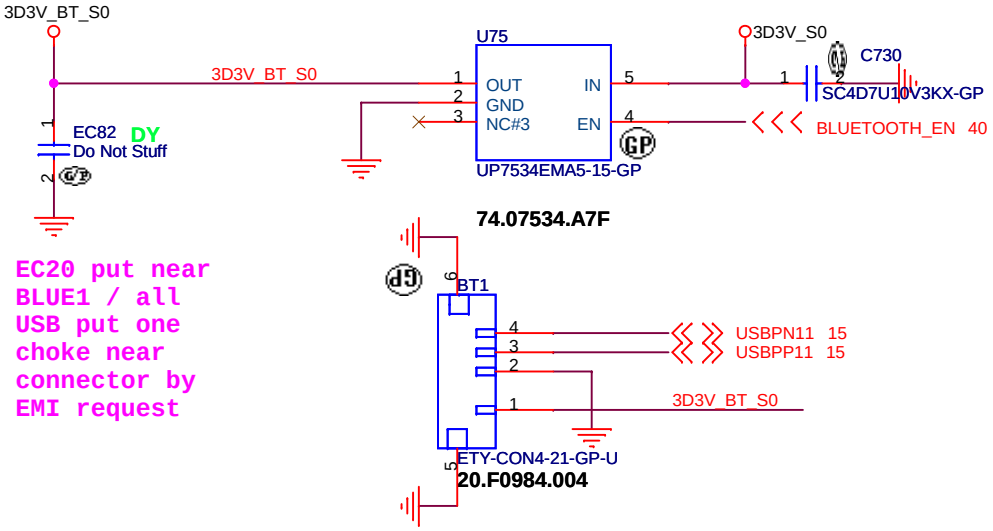
BLUETOOTH MODULE



EC20 put near BLUE1 / all USB put one choke near connector by EMI request

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLUETOOTH***

Size	Document Number	Rev
	JV50-CP	SA

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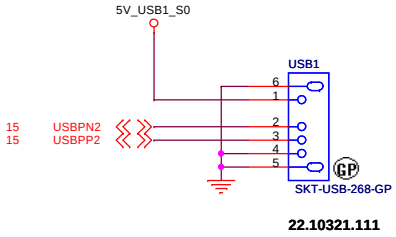
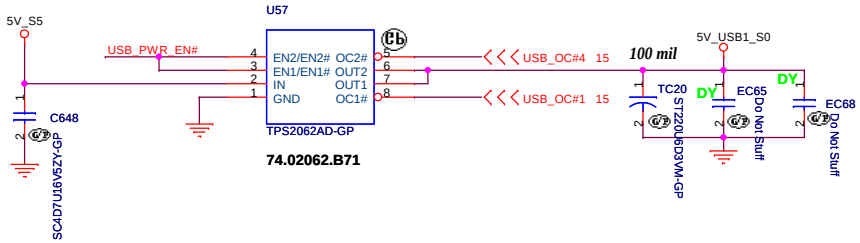
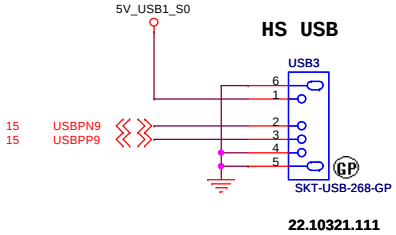
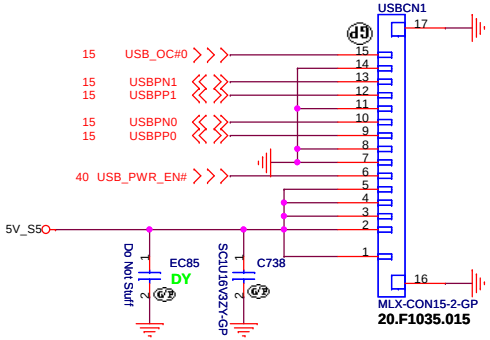




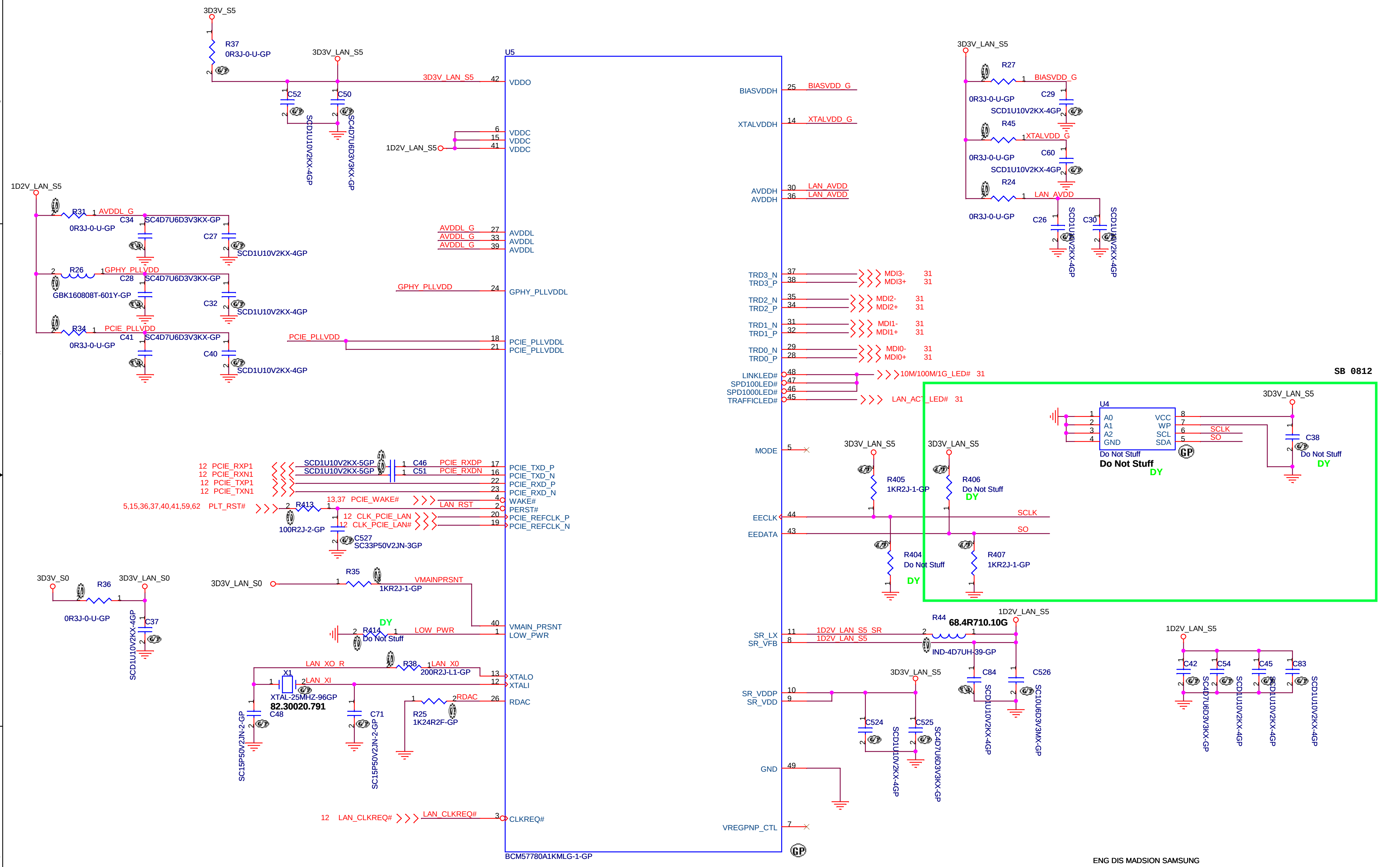




ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB CONN	
Size	Document Number JV50-CP	Rev SA
Date: Thursday, September 03, 2009	Sheet 29 of 61	



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

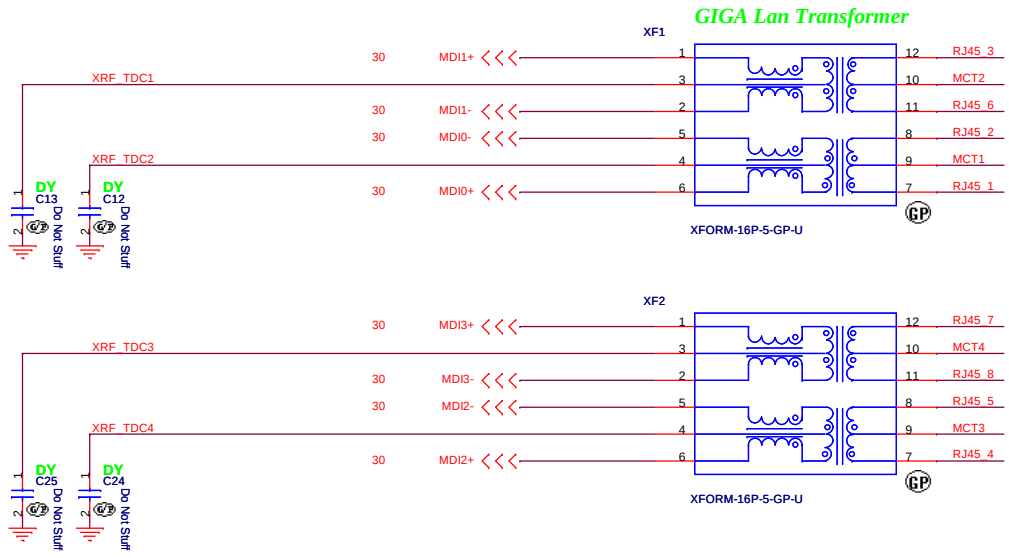
Title	BCM57780	
Size: Custom	Document Number: JV50-CP	Rev: SA
Date: Thursday, September 03, 2009	Sheet 30 of 61	

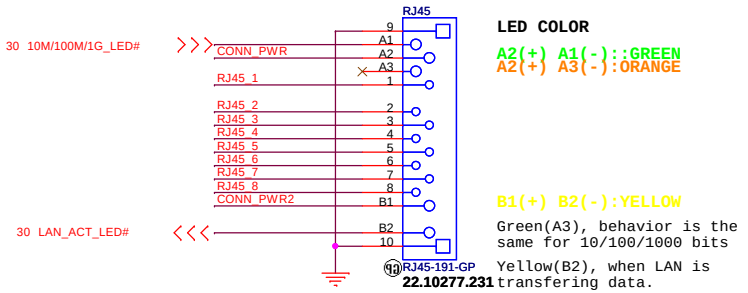
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

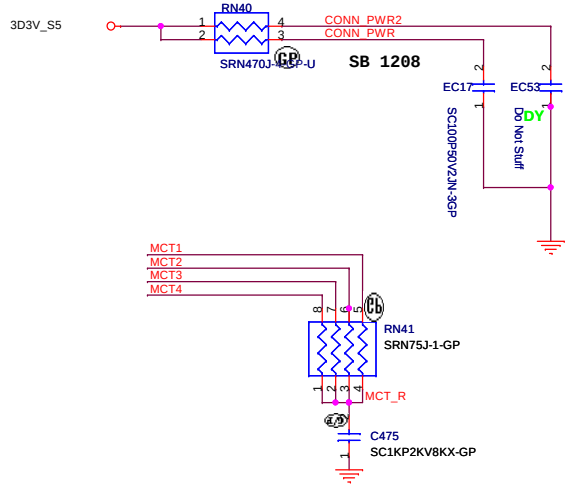
LAN Connector

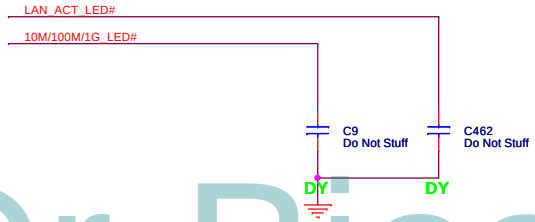
LAN Connector

GIGA Lan Transformer









ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

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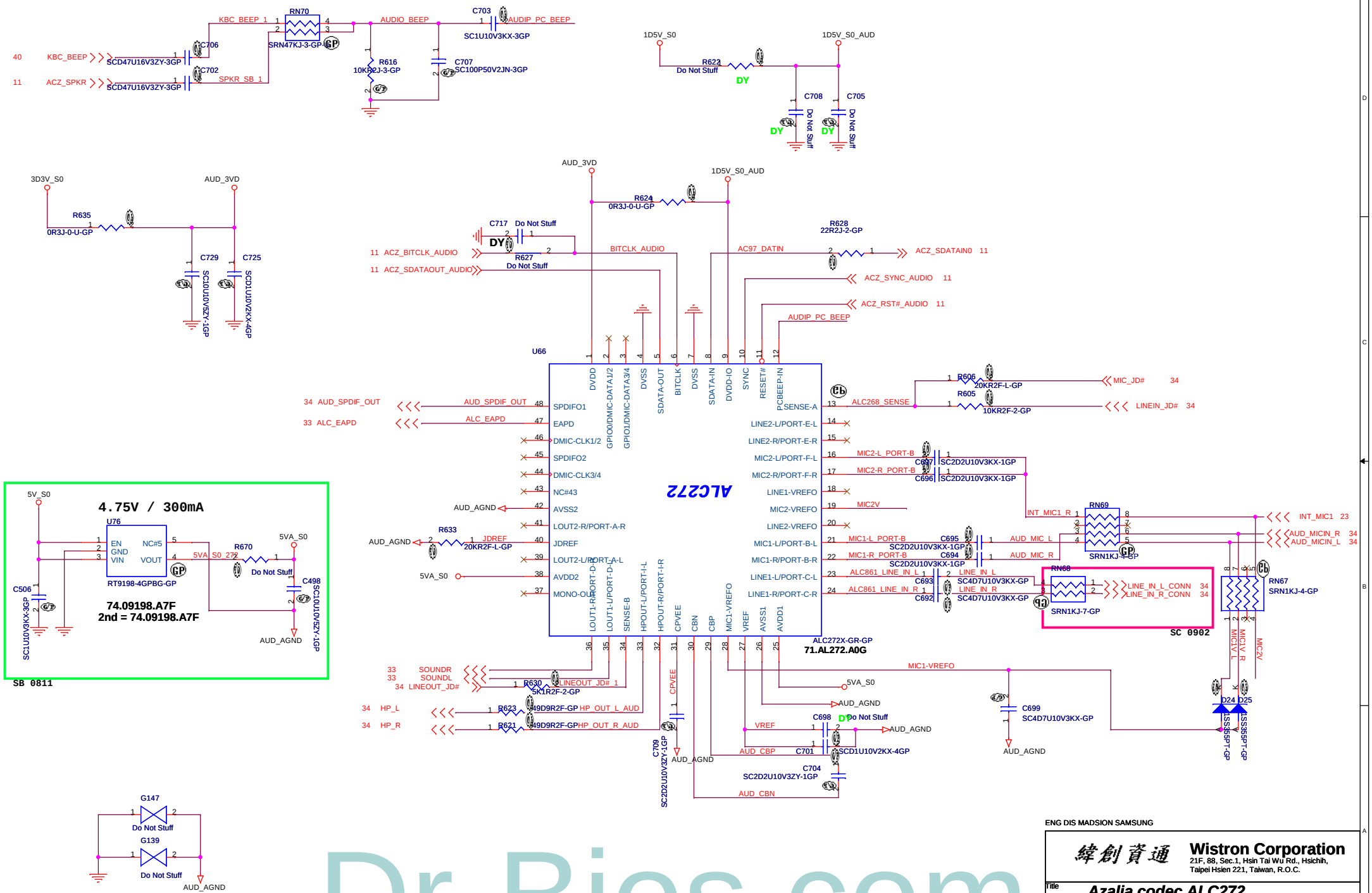

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC272**

Size	Document Number	Rev
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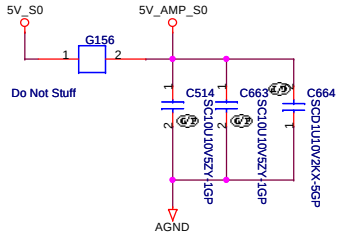
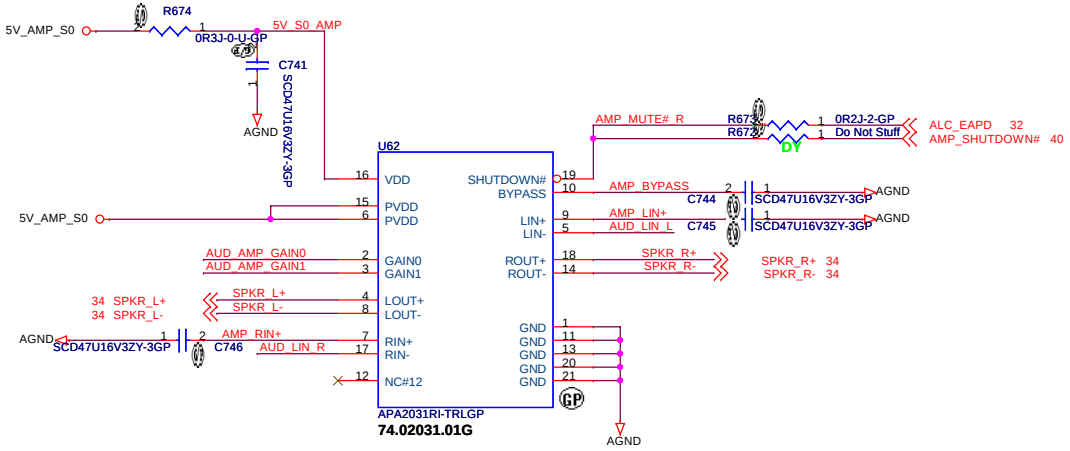
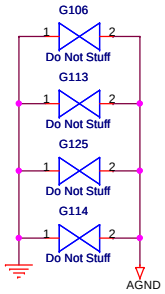
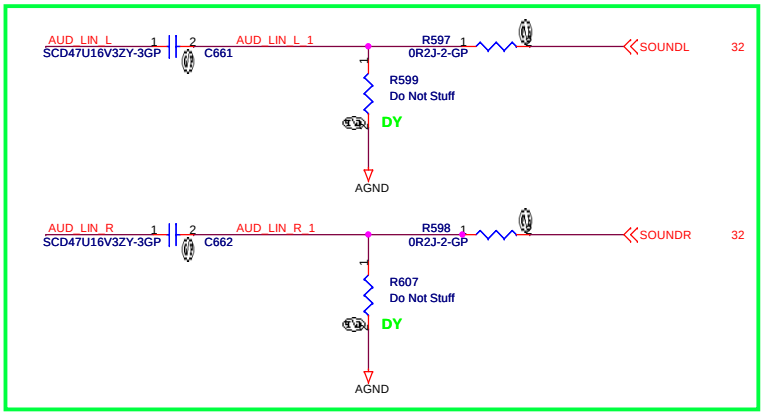


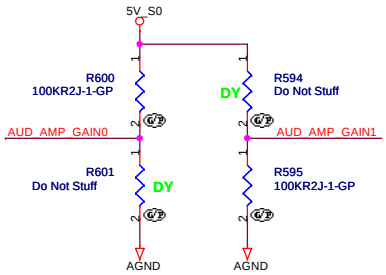






SB 0814

GAIN SETTING



GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO AMP*

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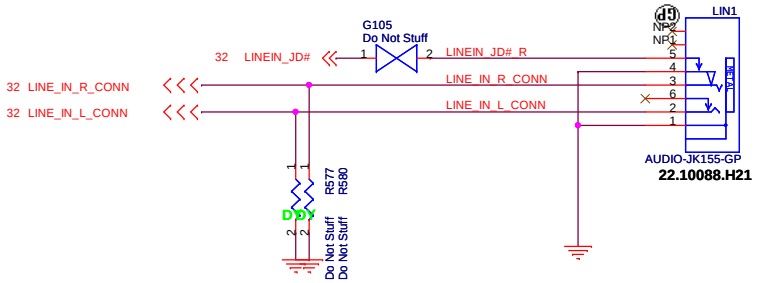
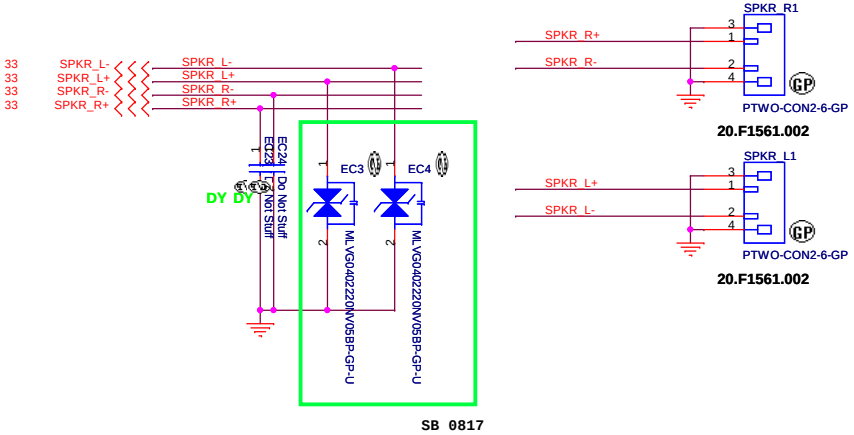
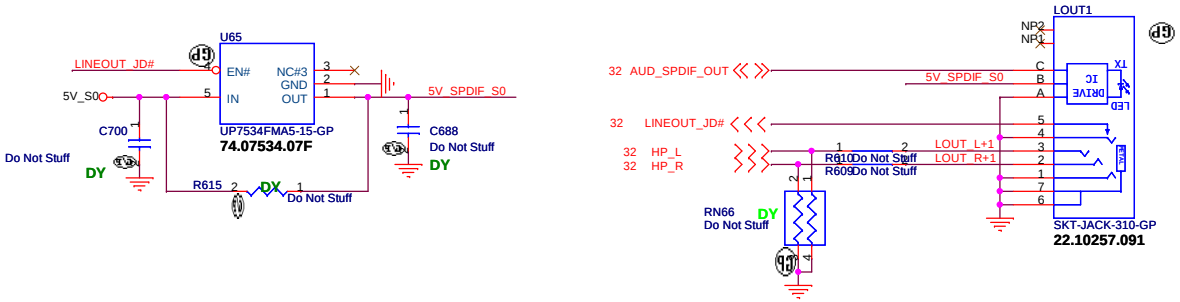
LINE IN

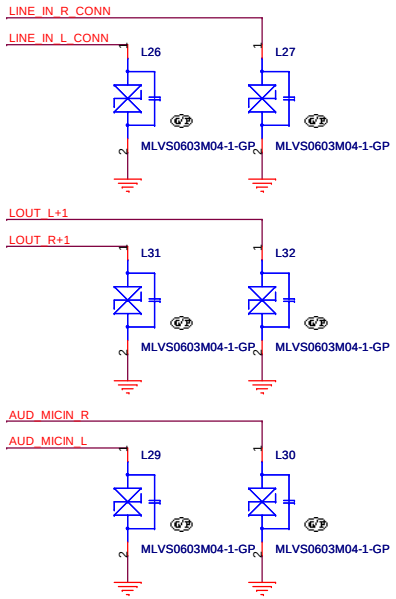


Internal Speaker

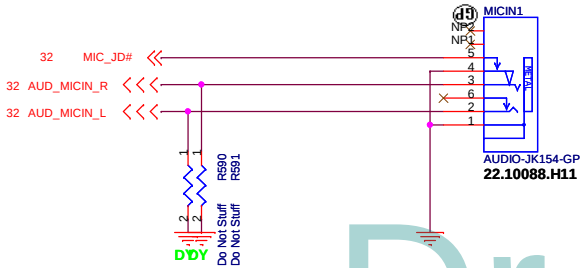


LINE OUT





MIC IN



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO jack

Size | Document Number: JV50-CP | Rev: SA

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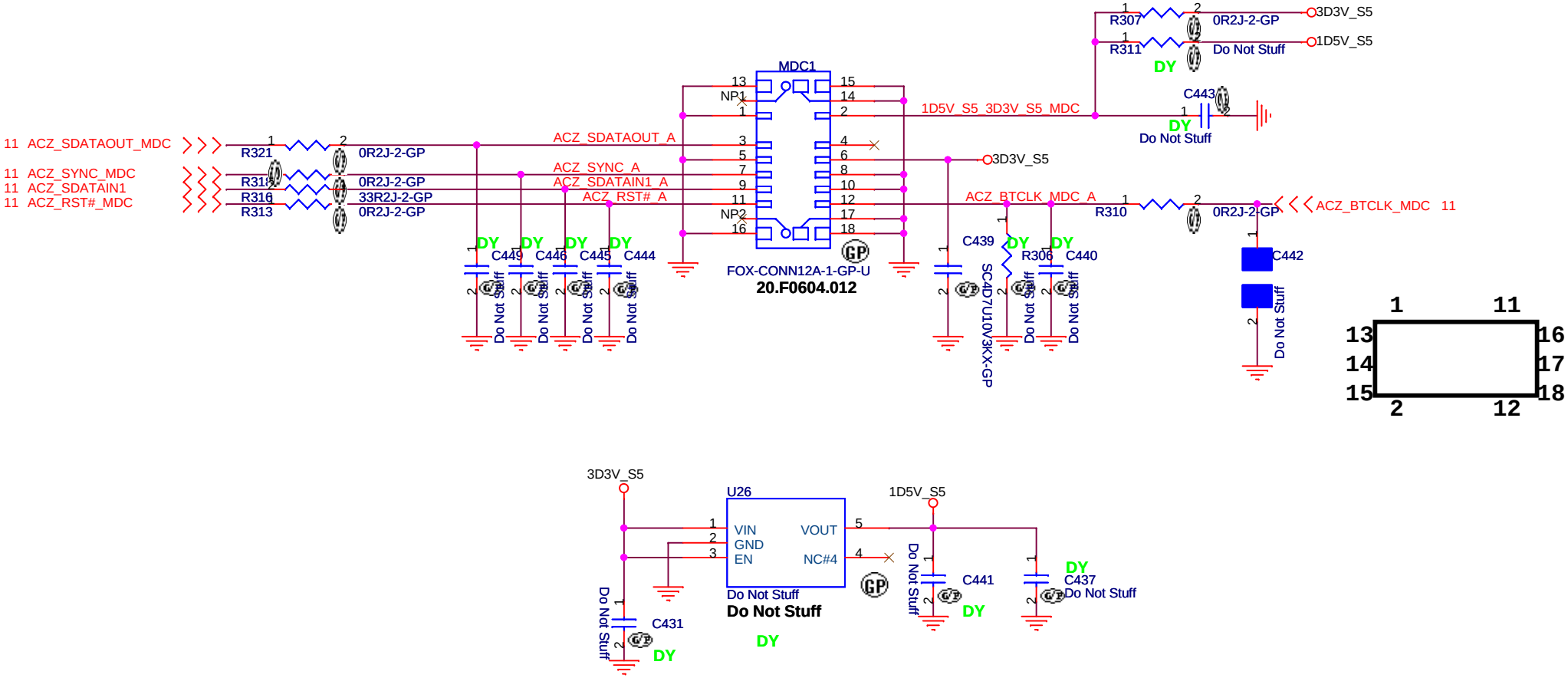
MDC 1.5 CONN



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC

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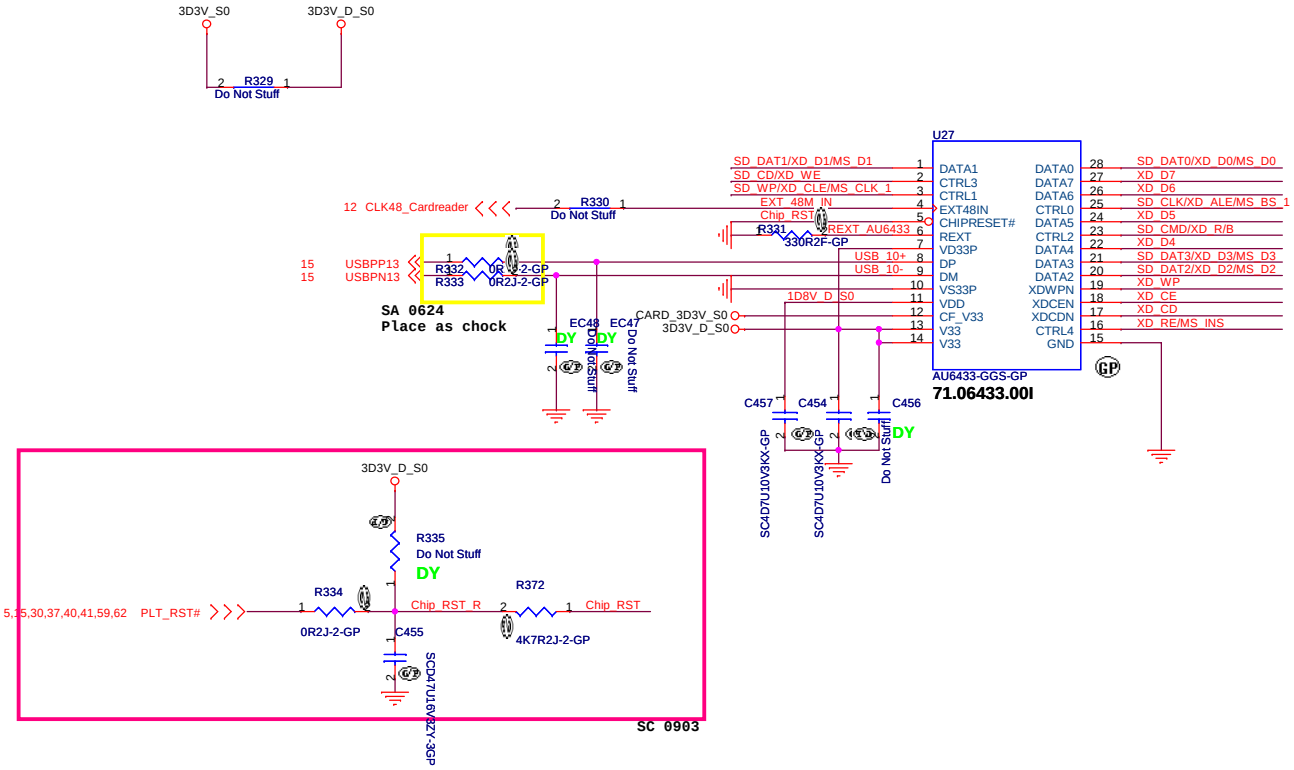
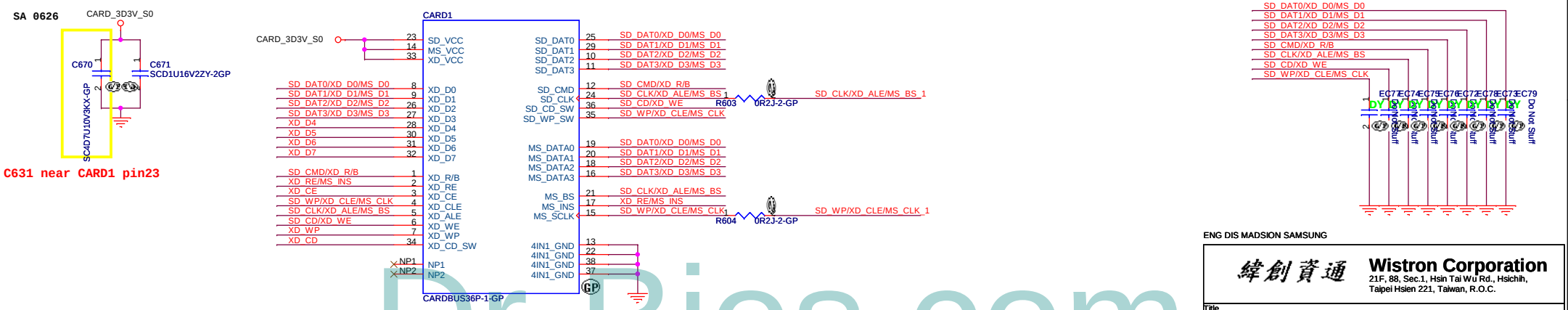


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



2nd = 20.I0079.011

20.I0109.001

ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cardreader	
Size	Document Number JV50-CP	Rev SA
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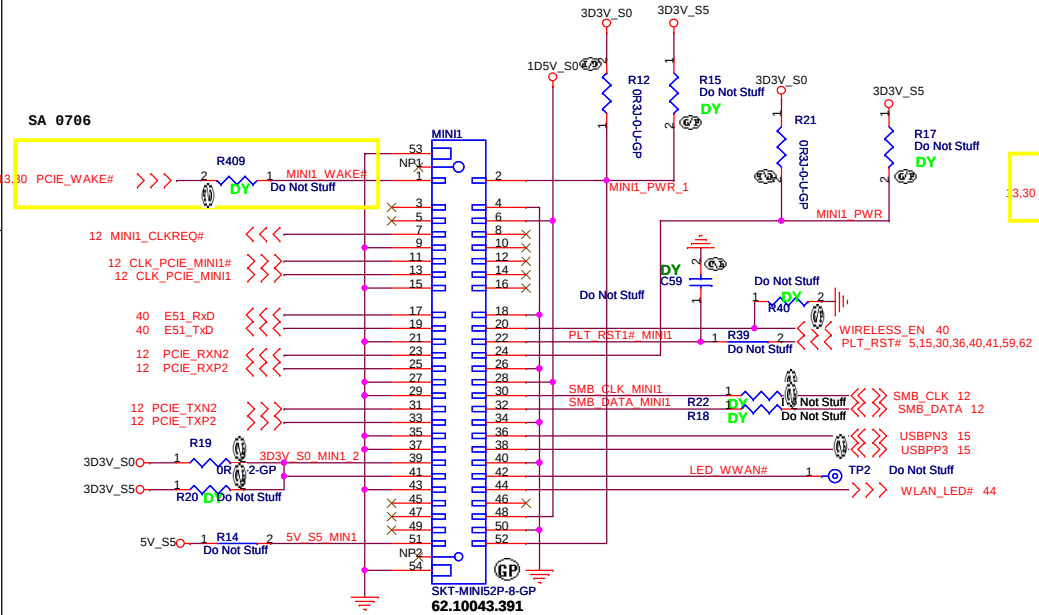
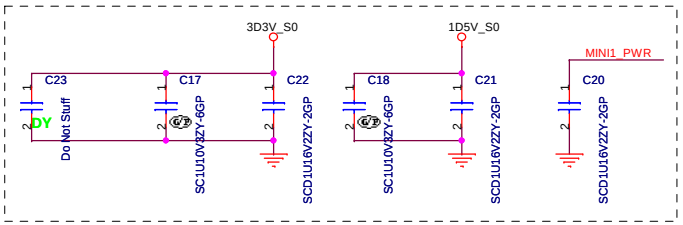
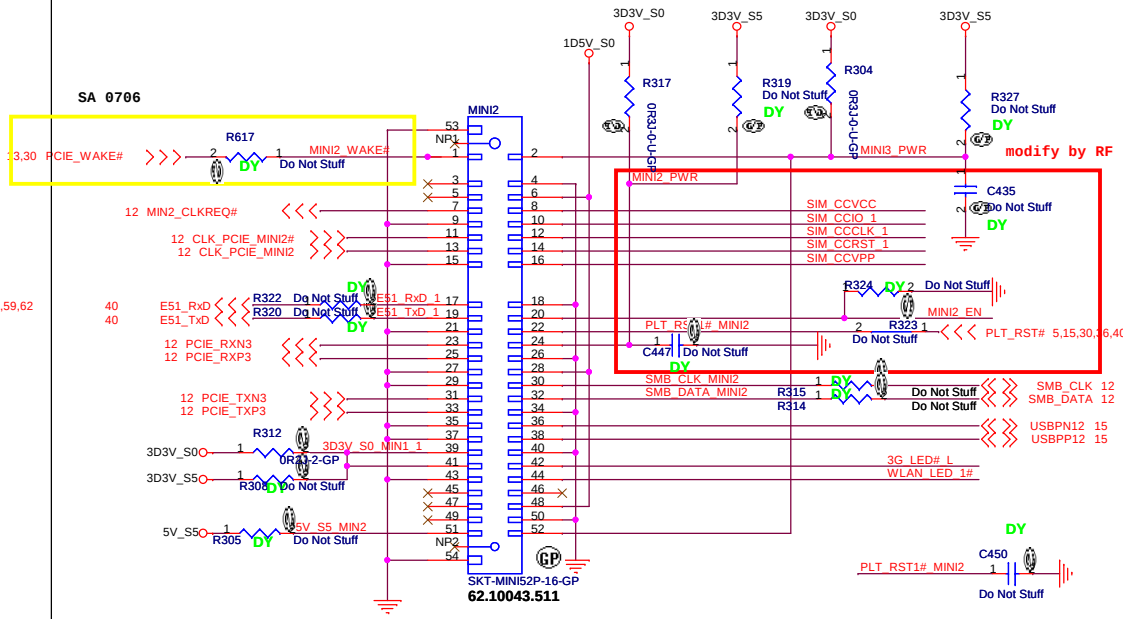
Mini Card Connector(WLAN)
Support debug-card

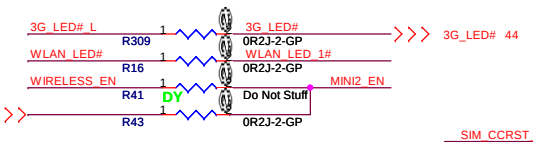


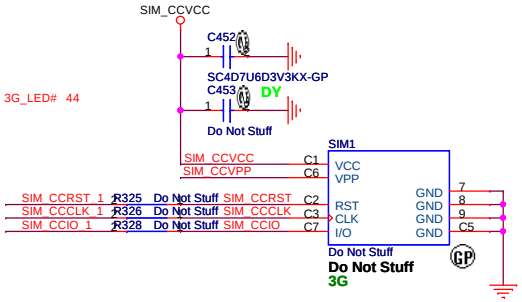
Place near MINI1



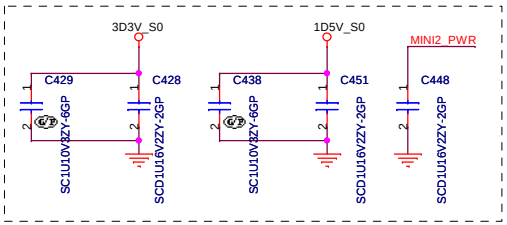
Mini Card Connector(Robson2 and 3G)







Place near MINIC2



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**		
Size: A3	Document Number: **JV50-CP**	Rev: **SA**
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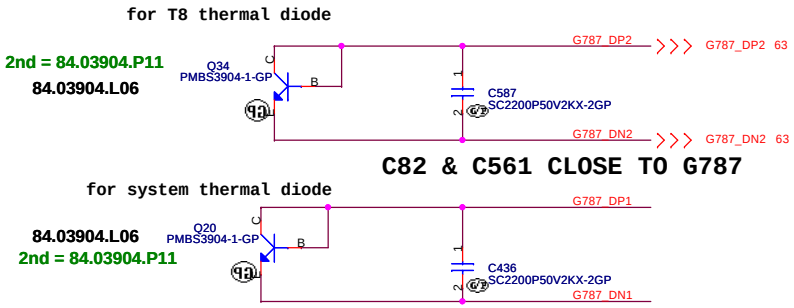

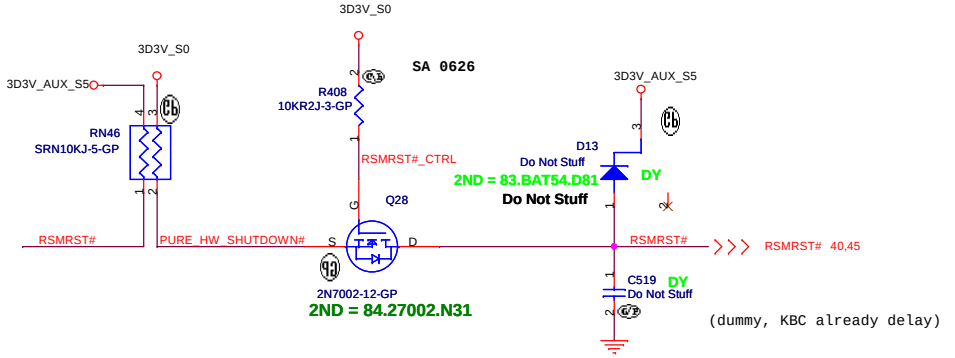

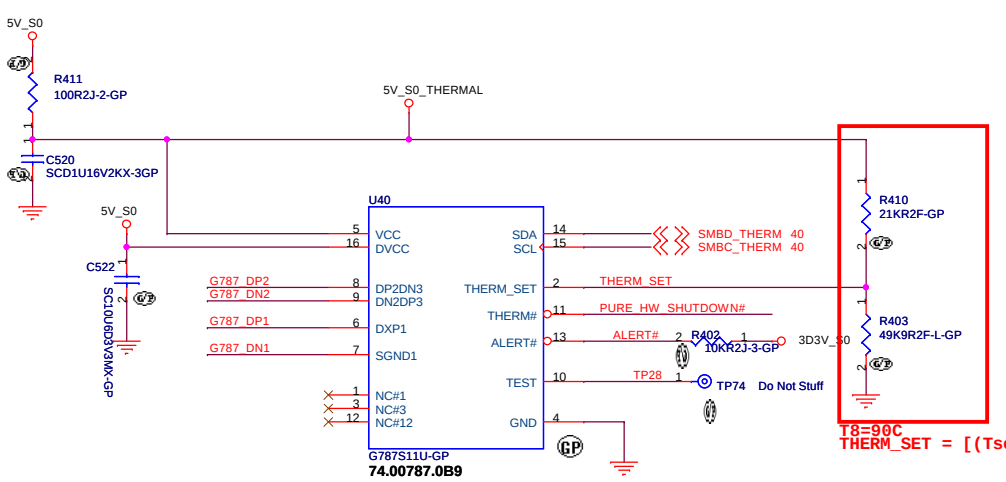

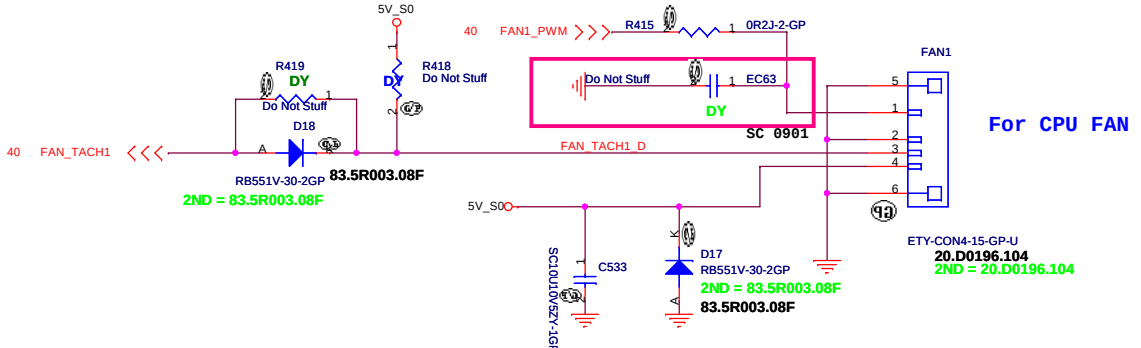

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Connector

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	JV50-CP	SA

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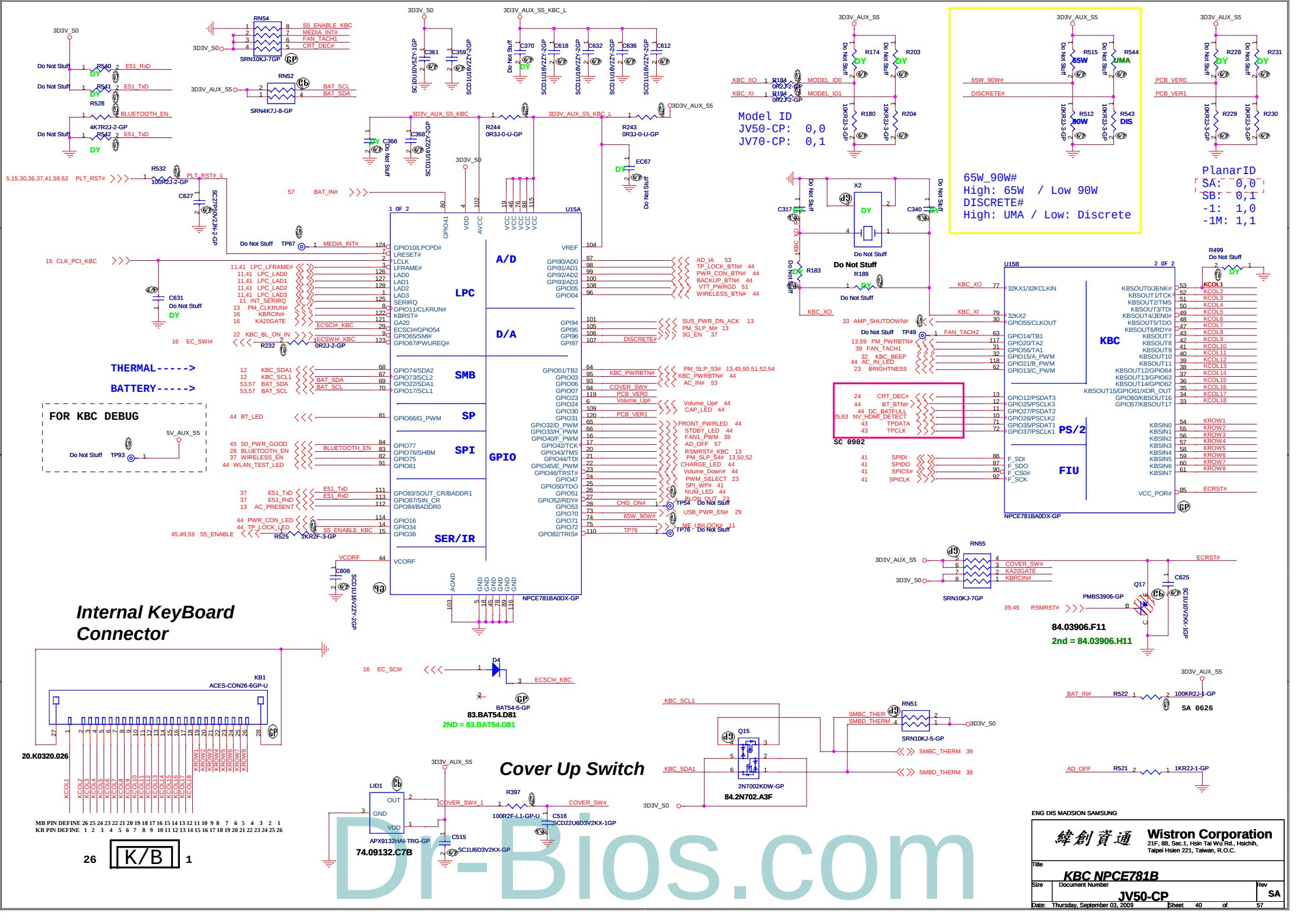
Model ID
JV50-CP: 0,0
JV70-CP: 0,1
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
THERMAL----->
BATTERY----->
FOR KBC DEBUG
Internal KeyBoard Connector
Cover Up Switch
U15A
NPCE781BA0DX-GP
U15B
KBC
PS/2
FIU
SC 0902
20.K0320.026
83.BAT54.D81
2ND = 83.BAT54.D81
84.03906.F11
2nd = 84.03906.H11
74.09132.C7B
84.2N702.A3F
SA 0626
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
26 K/B 1
ENG DIS MADSION SAMSUNG
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
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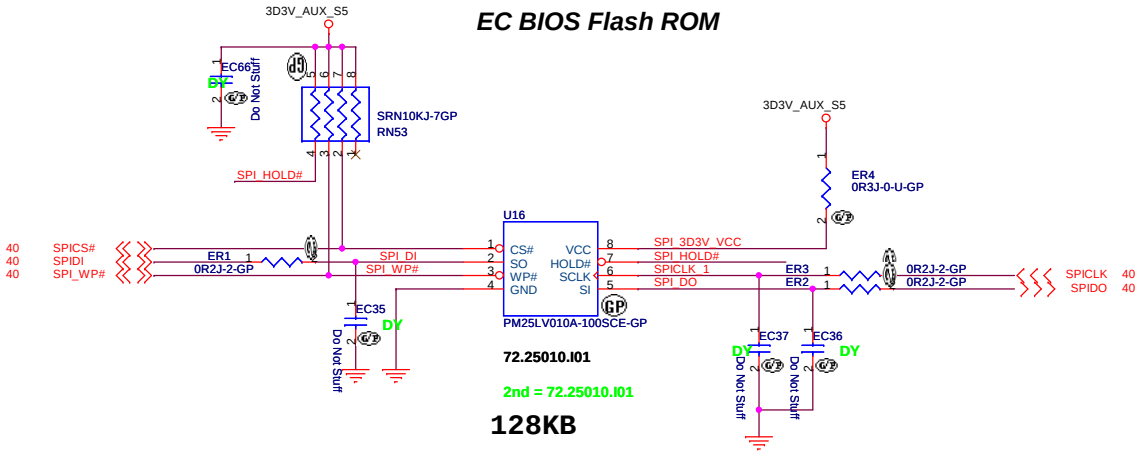
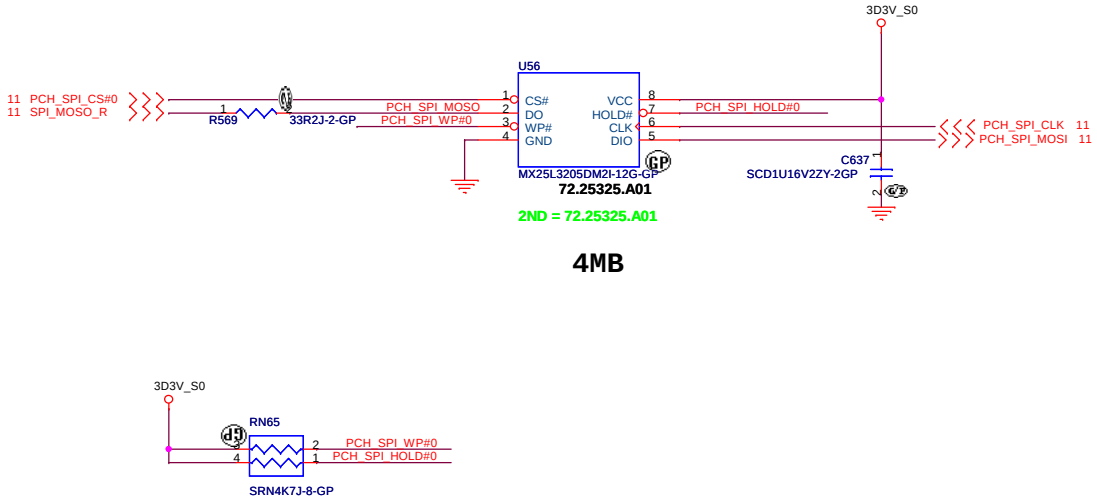
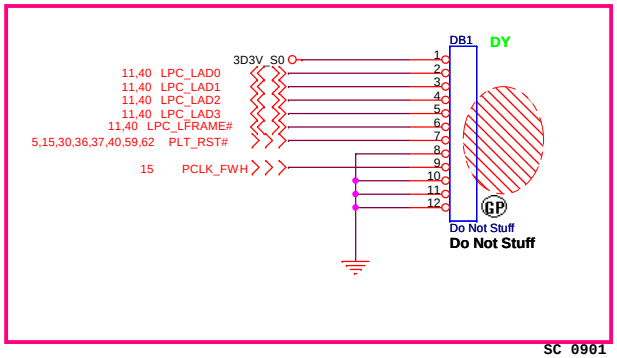
EC BIOS Flash ROM



System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD



SC 0901

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

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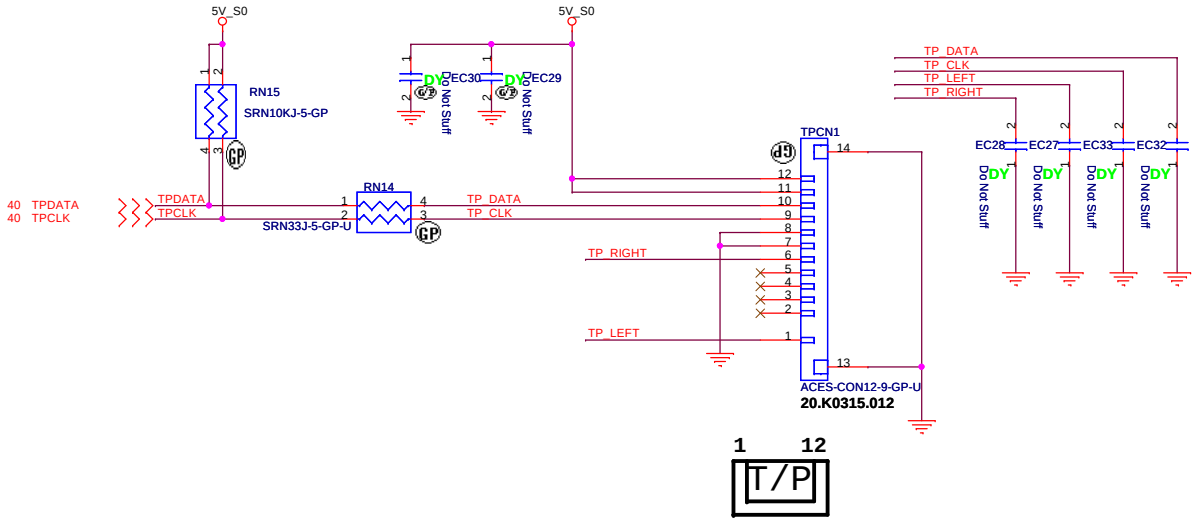
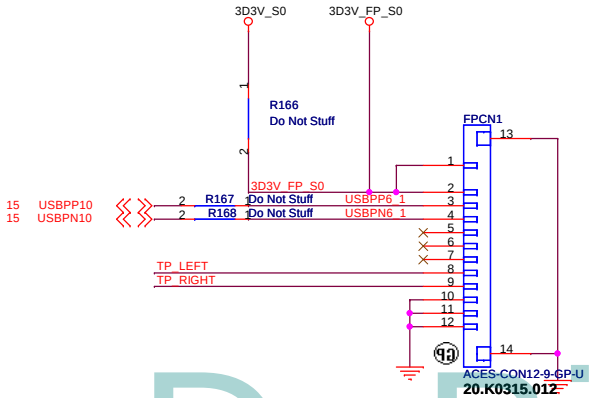
TOUCH PAD



Finger printer



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Touch PAD and FP*

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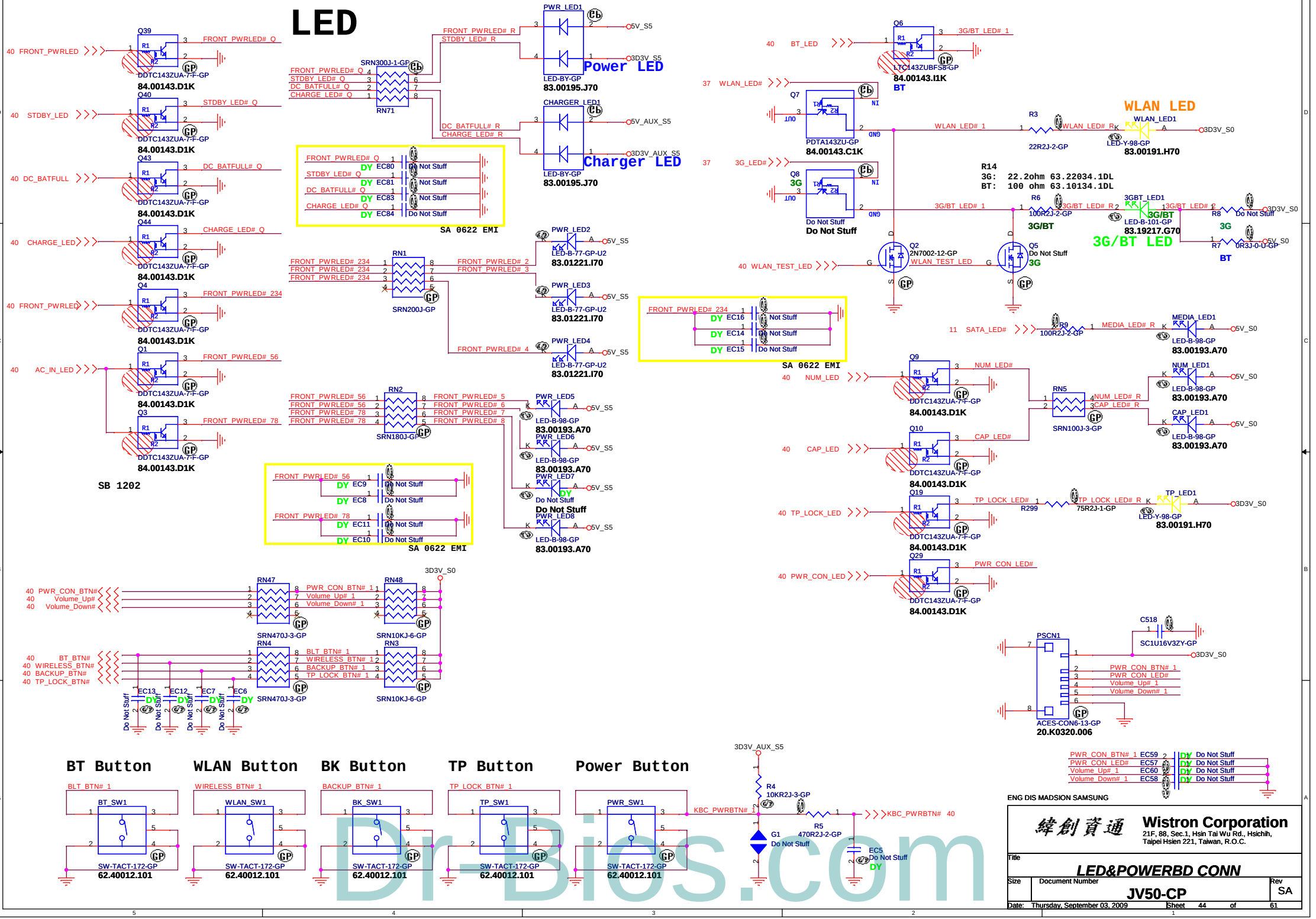
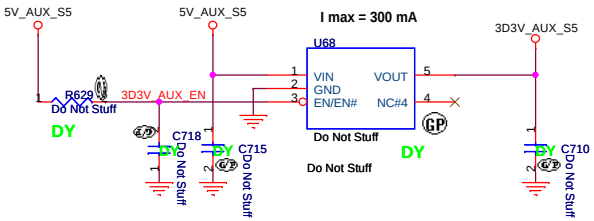
LED

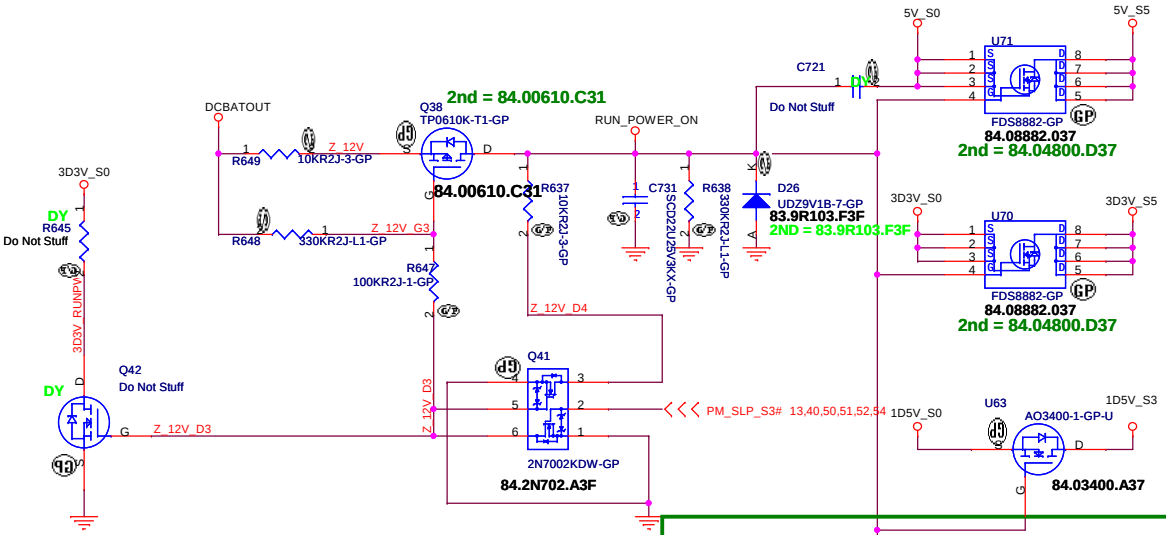


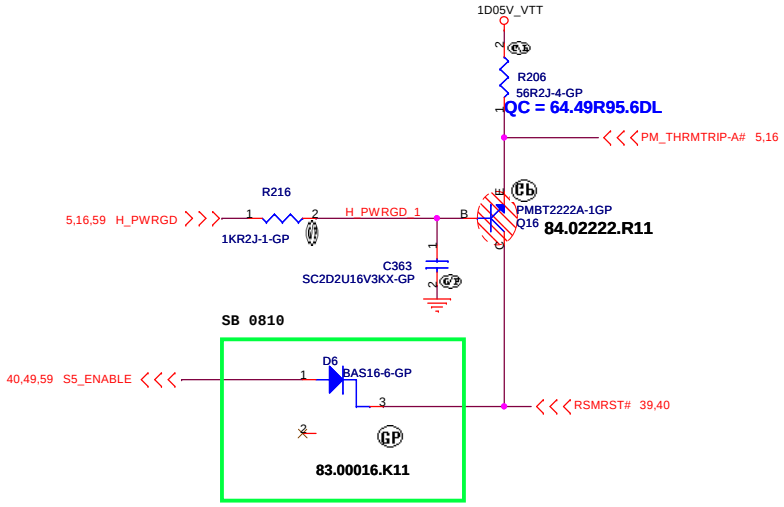
Run Power

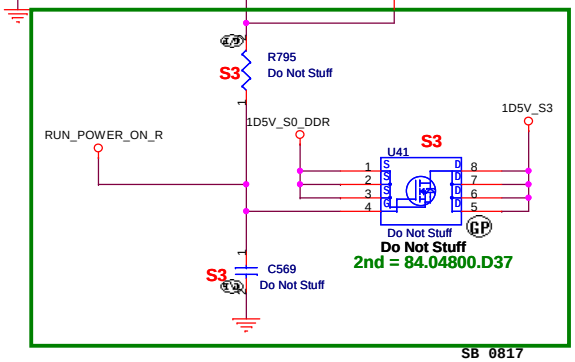
Aux Power

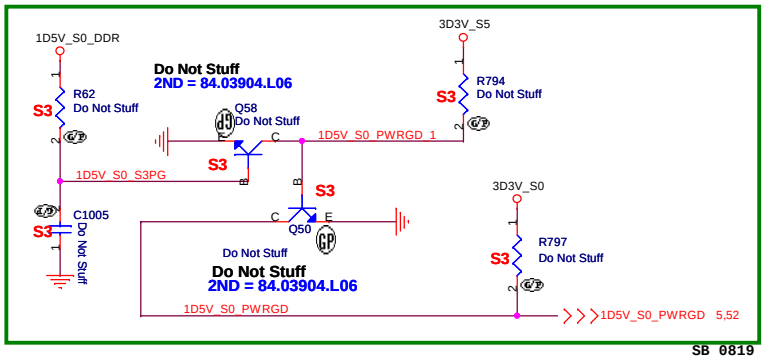
3D3V_AUX_S5

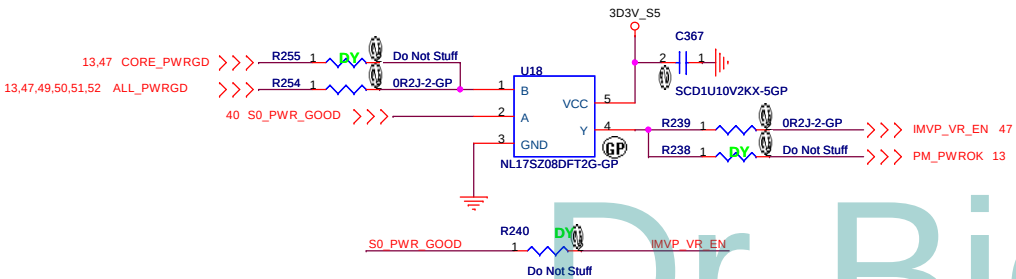












ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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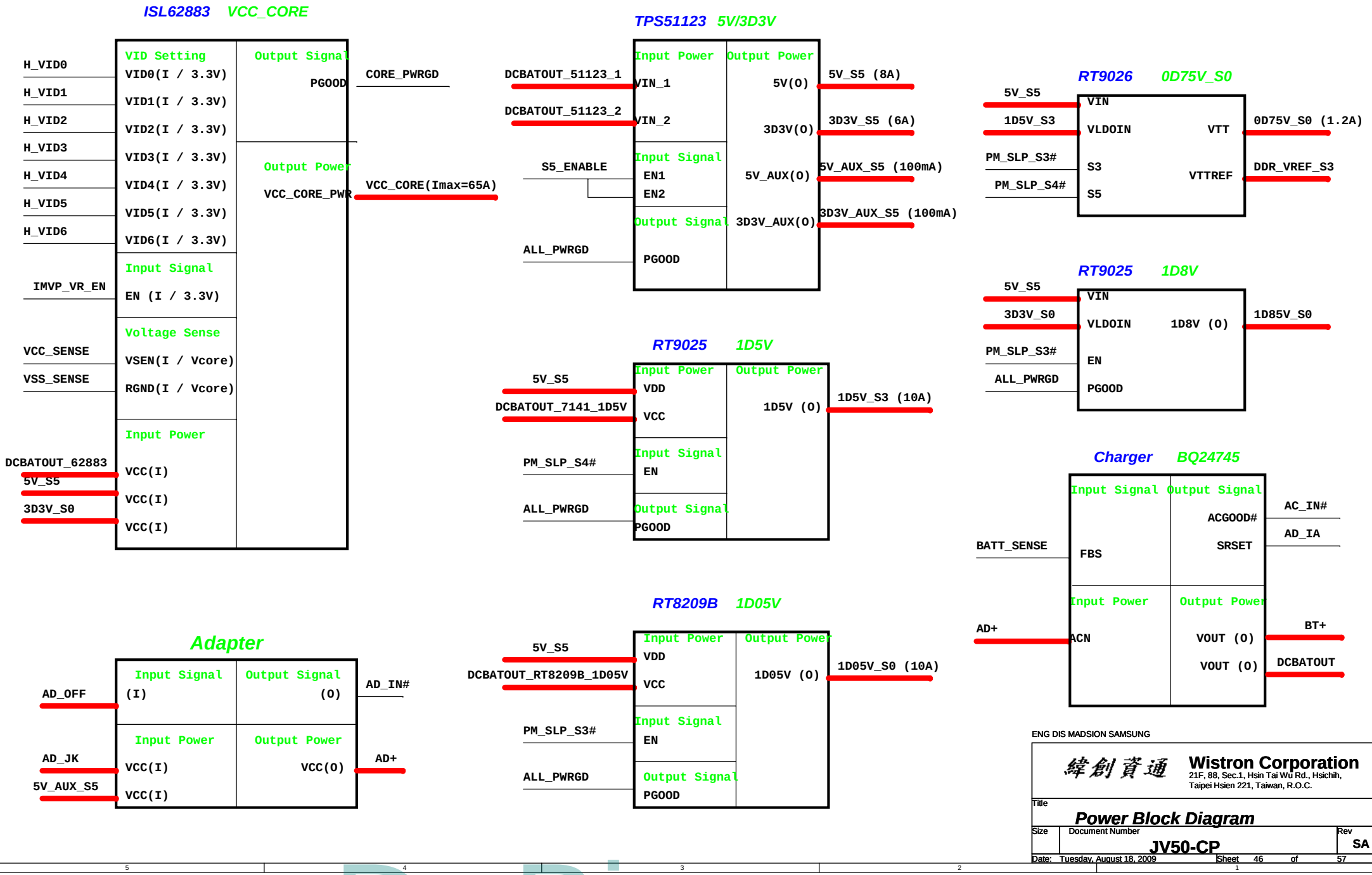
ISL62883 VCC_CORE
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
Input Signal
EN (I / 3.3V)
IMVP_VR_EN
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
VCC_SENSE
VSS_SENSE
Input Power
VCC(I)
VCC(I)
VCC(I)
DCBATOUT_62883
5V_S5
3D3V_S0
Output Signal
PGOOD
CORE_PWRGD
Output Power
VCC_CORE_PWR
VCC_CORE(Imax=65A)
TPS51123 5V/3D3V
Input Power
VIN_1
VIN_2
DCBATOUT_51123_1
DCBATOUT_51123_2
Output Power
5V(O)
3D3V(O)
5V_S5 (8A)
3D3V_S5 (6A)
Input Signal
EN1
EN2
S5_ENABLE
5V_AUX(O)
3D3V_AUX(O)
5V_AUX_S5 (100mA)
3D3V_AUX_S5 (100mA)
Output Signal
PGOOD
ALL_PWRGD
RT9026 0D75V_S0
VIN
VLDOIN
S3
S5
5V_S5
1D5V_S3
PM_SLP_S3#
PM_SLP_S4#
VTT
VTTREF
0D75V_S0 (1.2A)
DDR_VREF_S3
RT9025 1D5V
Input Power
VDD
VCC
5V_S5
DCBATOUT_7141_1D5V
Output Power
1D5V (O)
1D5V_S3 (10A)
Input Signal
EN
PM_SLP_S4#
Output Signal
PGOOD
ALL_PWRGD
RT9025 1D8V
VIN
VLDOIN
EN
PGOOD
5V_S5
3D3V_S0
PM_SLP_S3#
ALL_PWRGD
1D8V (O)
1D85V_S0
Charger BQ24745
Input Signal
FBS
Output Signal
ACGOOD#
SRSET
BATT_SENSE
AC_IN#
AD_IA
Input Power
ACN
Output Power
VOUT (O)
VOUT (O)
AD+
BT+
DCBATOUT
Adapter
Input Signal
(I)
Output Signal
(O)
AD_OFF
AD_IN#
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
AD_JK
5V_AUX_S5
AD+
RT8209B 1D05V
Input Power
VDD
VCC
5V_S5
DCBATOUT_RT8209B_1D05V
Output Power
1D05V (O)
1D05V_S0 (10A)
Input Signal
EN
PM_SLP_S3#
Output Signal
PGOOD
ALL_PWRGD
ENG DIS MADSION SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Block Diagram
Size
Document Number
JV50-CP
Rev
SA
Date: Tuesday, August 18, 2009
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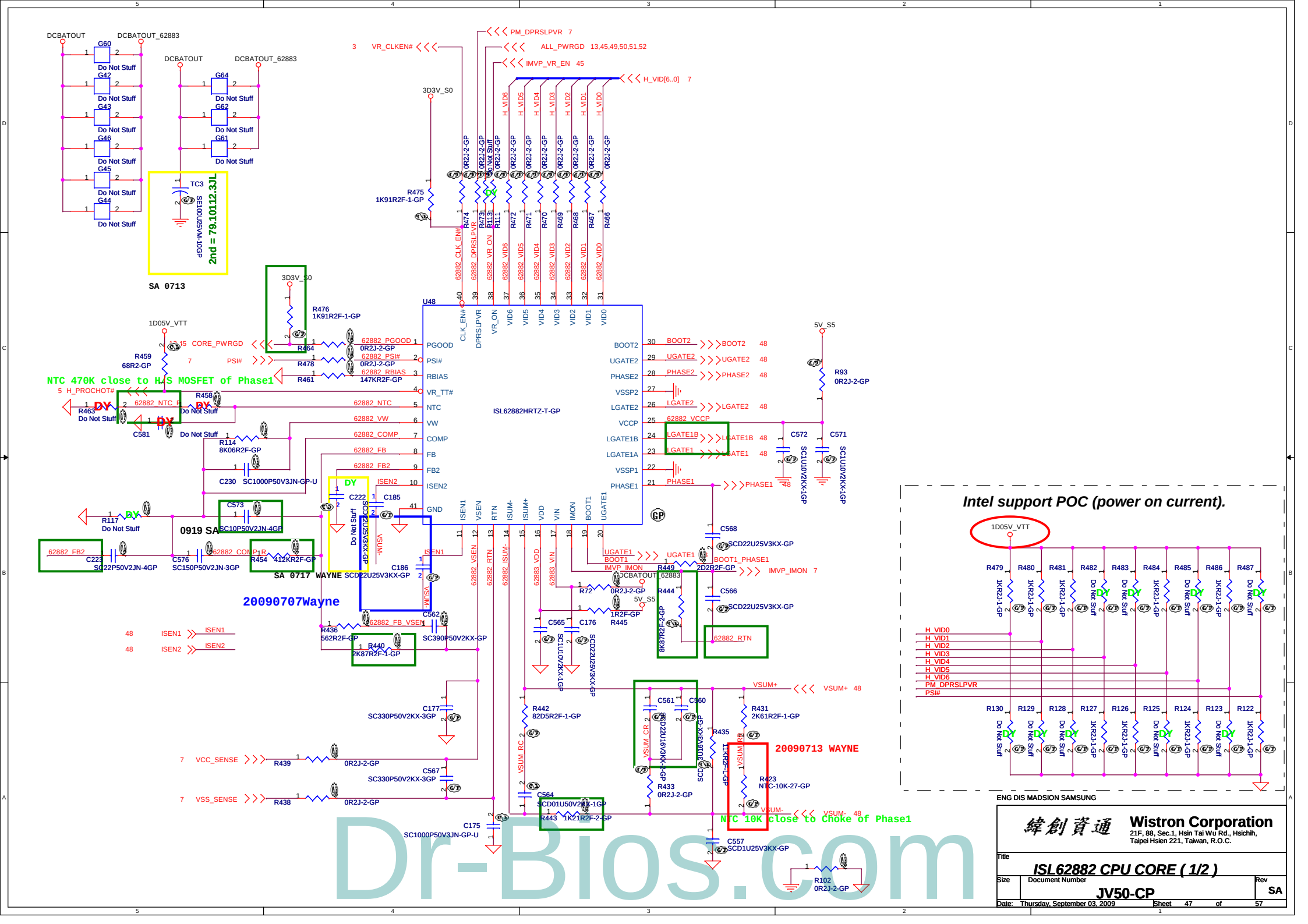
DCBATOUT
DCBATOUT_62883
G60
G42
G43
G46
G45
G44
G64
G62
G61
Do Not Stuff
TC3
SE100U2VM-10GP
2nd = 79.10112.33L
SA 0713
PM_DPRSLPVR 7
ALL_PWRGD 13,45,49,50,51,52
IMVP_VR_EN 45
H_VID[6..0] 7
VR_CLKEN# 3
3D3V_S0
R475
1K91R2F-1-GP
U48
ISL62882HRTZ-T-GP
1D05V_VTT
R476
1K91R2F-1-GP
R464
R478
R461
R459
68R2-GP
R458
R463
C581
R114
8K06R2F-GP
C230
SC1000P50V3JN-GP-U
C573
SC10P50V2JN-4GP
R117
0919 SA
C223
SC22P50V2JN-4GP
C576
SC150P50V2JN-3GP
R454
412KR2F-GP
SA 0717 WAYNE
20090707Wayne
C222
C185
C186
SCD22U25V3KX-GP
C562
SC390P50V2KX-GP
R436
562R2F-GP
R440
2K87R2F-1-GP
NTC 470K close to H/S MOSFET of Phase1
5V_S5
R93
0R2J-2-GP
C572
C571
SC1U10V2KX-1GP
C568
C566
R449
2D2R2F-GP
R72
0R2J-2-GP
1R2F-GP
R445
R444
8K87R2F-2-GP
C565
C176
SCD22U25V3KX-GP
C561
C560
SCD22U16V3KX-GP
R431
2K61R2F-1-GP
R435
11KR2F-1-GP
R433
0R2J-2-GP
R423
NTC-10K-27-GP
20090713 WAYNE
NTC 10K close to Choke of Phase1
R442
82D5R2F-1-GP
C564
SCD01U50V2KX-1GP
R443
1K21R2F-2-GP
C557
SCD1U25V3KX-GP
R102
0R2J-2-GP
C177
SC330P50V2KX-3GP
C567
SC330P50V2KX-3GP
C175
SC1000P50V3JN-GP-U
R439
R438
0R2J-2-GP
VCC_SENSE 7
VSS_SENSE 7
VSUM+ 48
VSUM- 48
ISEN1 48
ISEN2 48
Intel support POC (power on current).
1D05V_VTT
R479
R480
R481
R482
R483
R484
R485
R486
R487
R130
R129
R128
R127
R126
R125
R124
R123
R122
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PM_DPRSLPVR
PSI#
ENG DIS MADSION SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62882 CPU CORE (1/2)
Size
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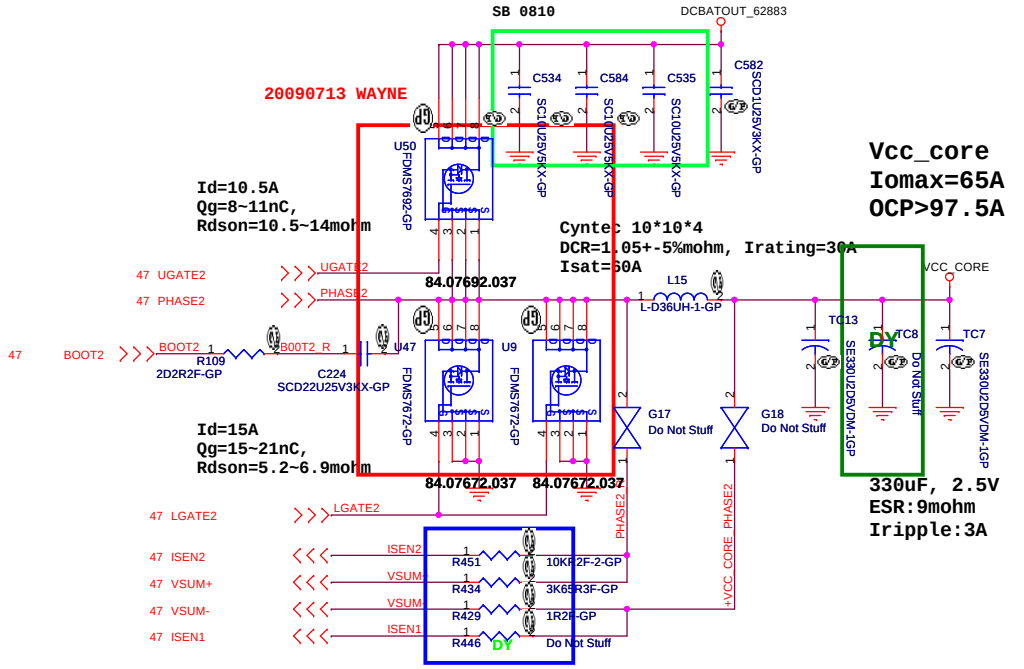
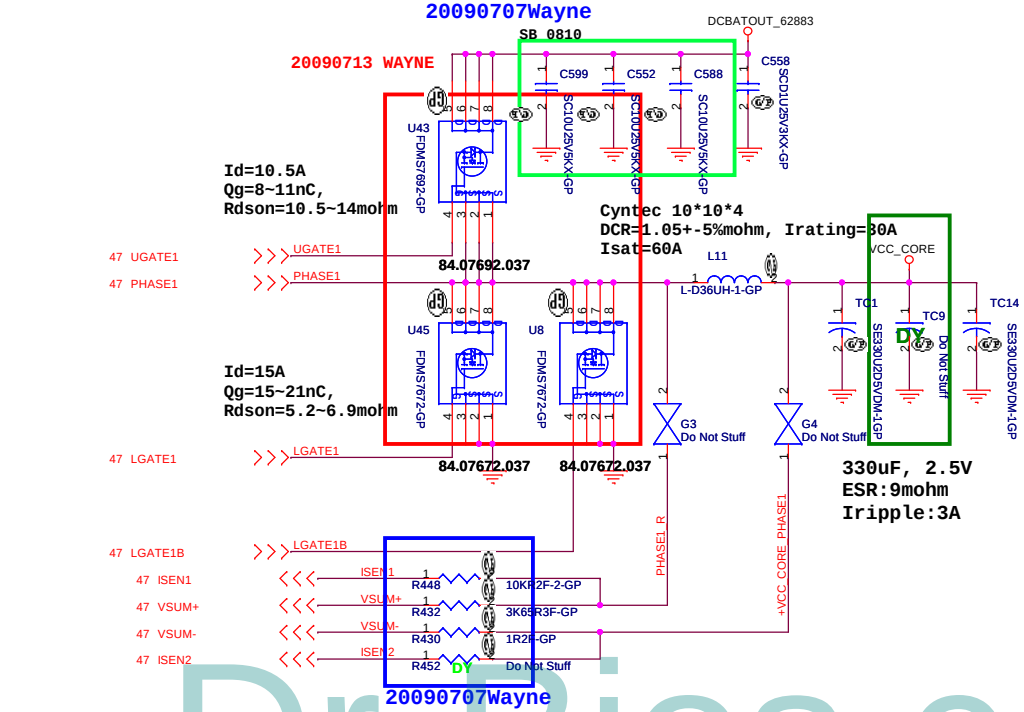


20090707Wayne



20090707Wayne

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62882 CPU CORE (1/2)

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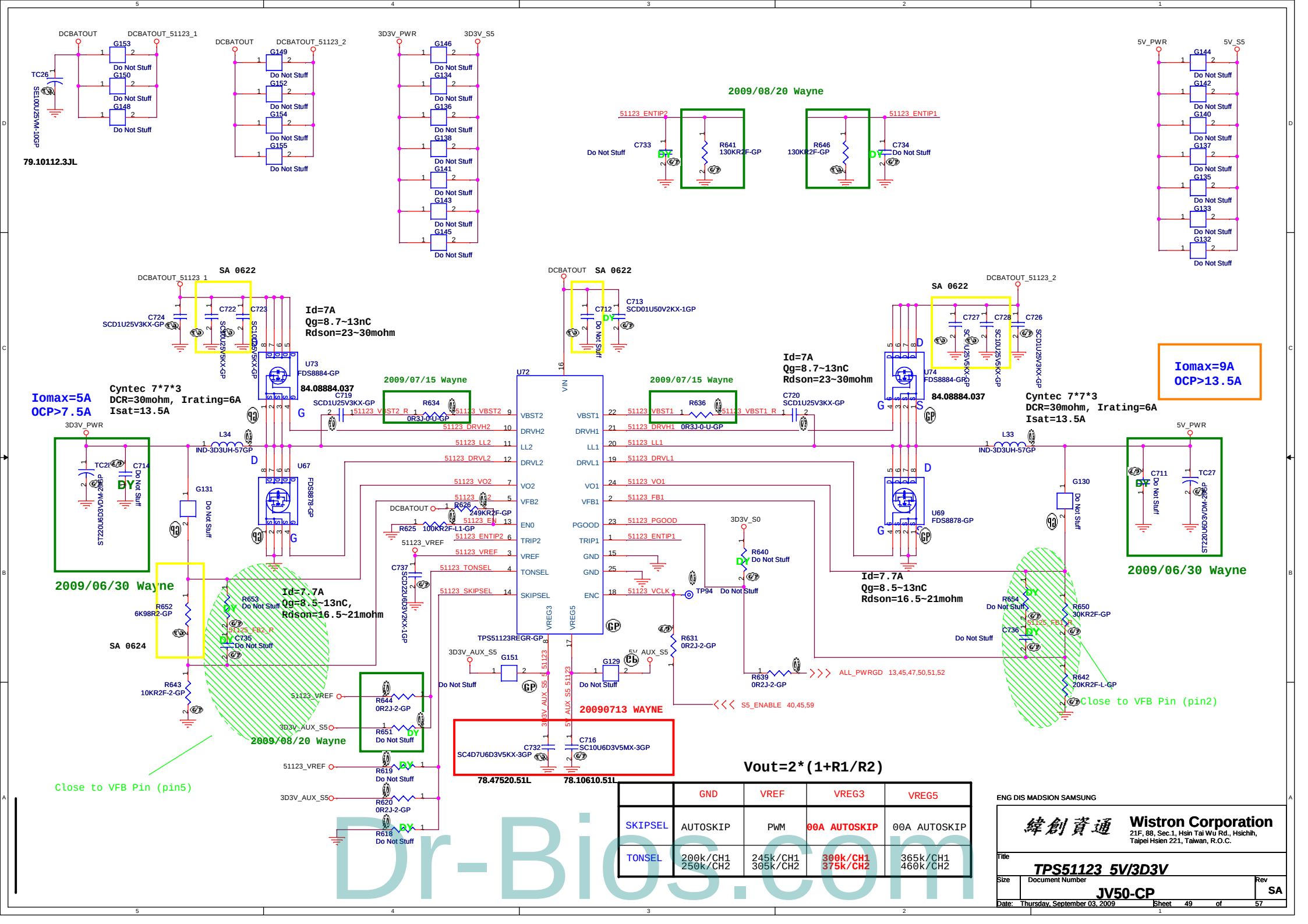
DCBATOUT
DCBATOUT_51123_1
TC26
SE100U25VM-10GP
G153
G150
G148
Do Not Stuff
79.10112.3JL
DCBATOUT_51123_2
G149
G152
G154
G155
3D3V_PWR
3D3V_S5
G146
G134
G136
G138
G141
G143
G145
2009/08/20 Wayne
51123_ENTIP2
51123_ENTIP1
C733
R641
130KR2F-GP
R646
C734
5V_PWR
5V_S5
G144
G142
G140
G137
G135
G133
G132
SA 0622
SA 0624
C724
SCD1U25V3KX-GP
C722
C723
SC10U25V5KX-GP
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
U73
FDS8884-GP
84.08884.037
C719
R634
0R3J-0-U-GP
2009/07/15 Wayne
U72
C712
C713
SCD01U50V2KX-1GP
U74
C727
C728
C726
C720
R636
Iomax=5A
OCP>7.5A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Iomax=9A
OCP>13.5A
L34
IND-3D3UH-57GP
L33
U67
FDS8878-GP
U69
TC27
C714
ST220U6D3VDM-2GP
G131
G130
2009/06/30 Wayne
Id=7.7A
Qg=8.5~13nC,
Rdson=16.5~21mohm
R653
R652
6K98R2-GP
R654
R650
30KR2F-GP
C735
C736
R643
10KR2F-2-GP
R642
20KR2F-L-GP
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
R644
0R2J-2-GP
R651
R619
R620
R618
R626
249KR2F-GP
R625
100KR2F-L1-GP
C737
SCD22U6D3V2KX-1-GP
TPS51123REGR-GP
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
TRIP2
VREF
TONSEL
SKIPSEL
VIN
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
TRIP1
GND
ENC
VREG3
VREG5
51123_VBST2
51123_DRVH2
51123_LL2
51123_DRVL2
51123_VO2
51123_EN
51123_ENTIP2
51123_VREF
51123_TONSEL
51123_SKIPSEL
51123_VBST1
51123_DRVH1
51123_LL1
51123_DRVL1
51123_VO1
51123_FB1
51123_PGOOD
51123_ENTIP1
51123_VCLK
3D3V_S0
R640
TP94
R631
0R2J-2-GP
R639
ALL_PWRGD 13,45,47,50,51,52
S5_ENABLE 40,45,59
3D3V_AUX_S5
5V_AUX_S5
G151
G129
20090713 WAYNE
C732
SC4D7U6D3V5KX-3GP
C716
SC10U6D3V5MX-3GP
78.47520.51L
78.10610.51L
Vout=2*(1+R1/R2)
GND
VREF
VREG3
VREG5
SKIPSEL
AUTOSKIP
PWM
00A AUTOSKIP
TONSEL
200k/CH1
250k/CH2
245k/CH1
305k/CH2
300k/CH1
375k/CH2
365k/CH1
460k/CH2
ENG DIS MADSION SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51123 5V/3D3V
Size
Document Number
JV50-CP
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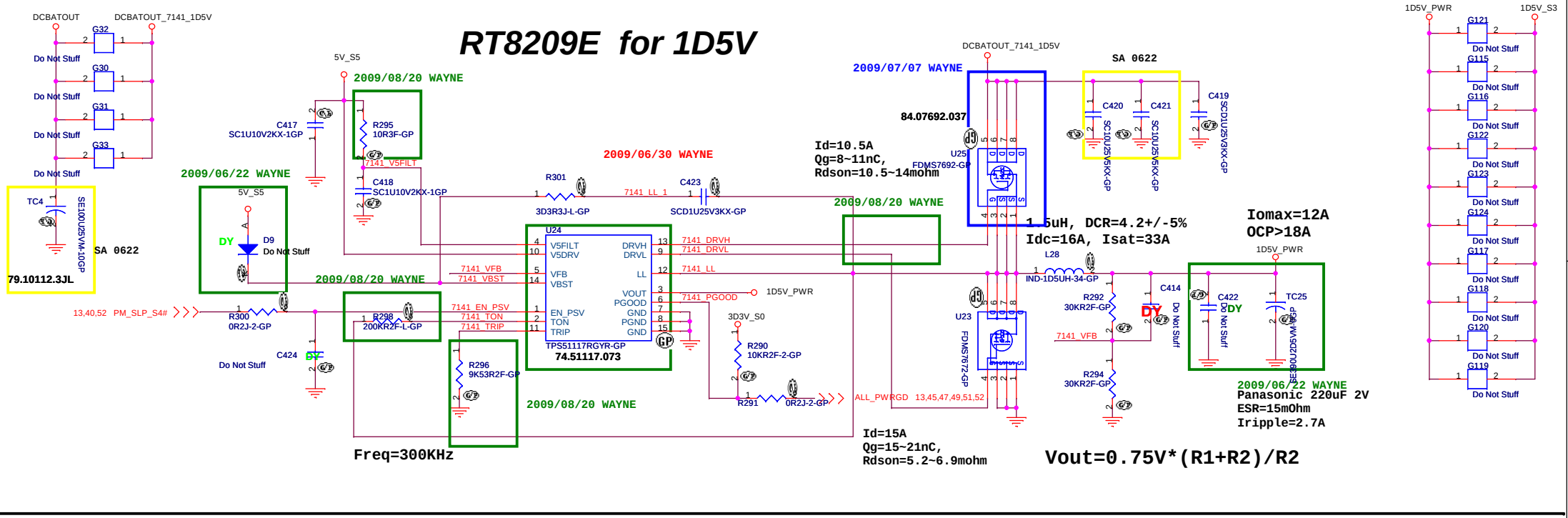
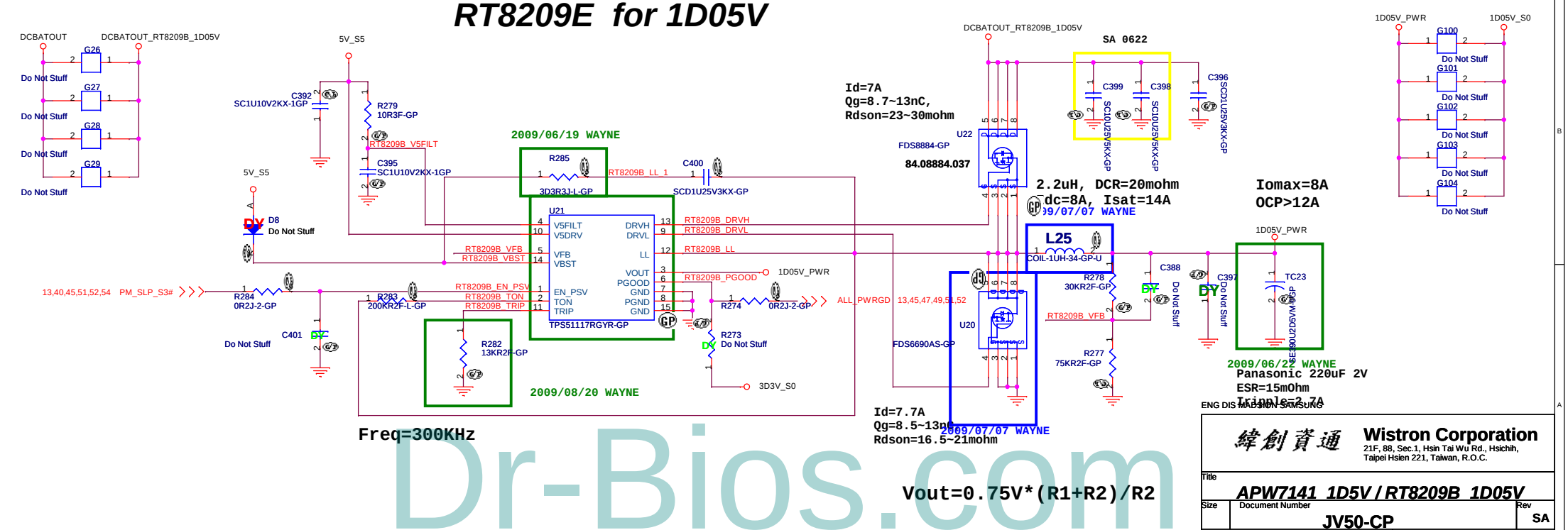
RT8209E for 1D5V



RT8209E for 1D05V



ENG DIS MADE IN SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APW7141 1D5V / RT8209B 1D05V

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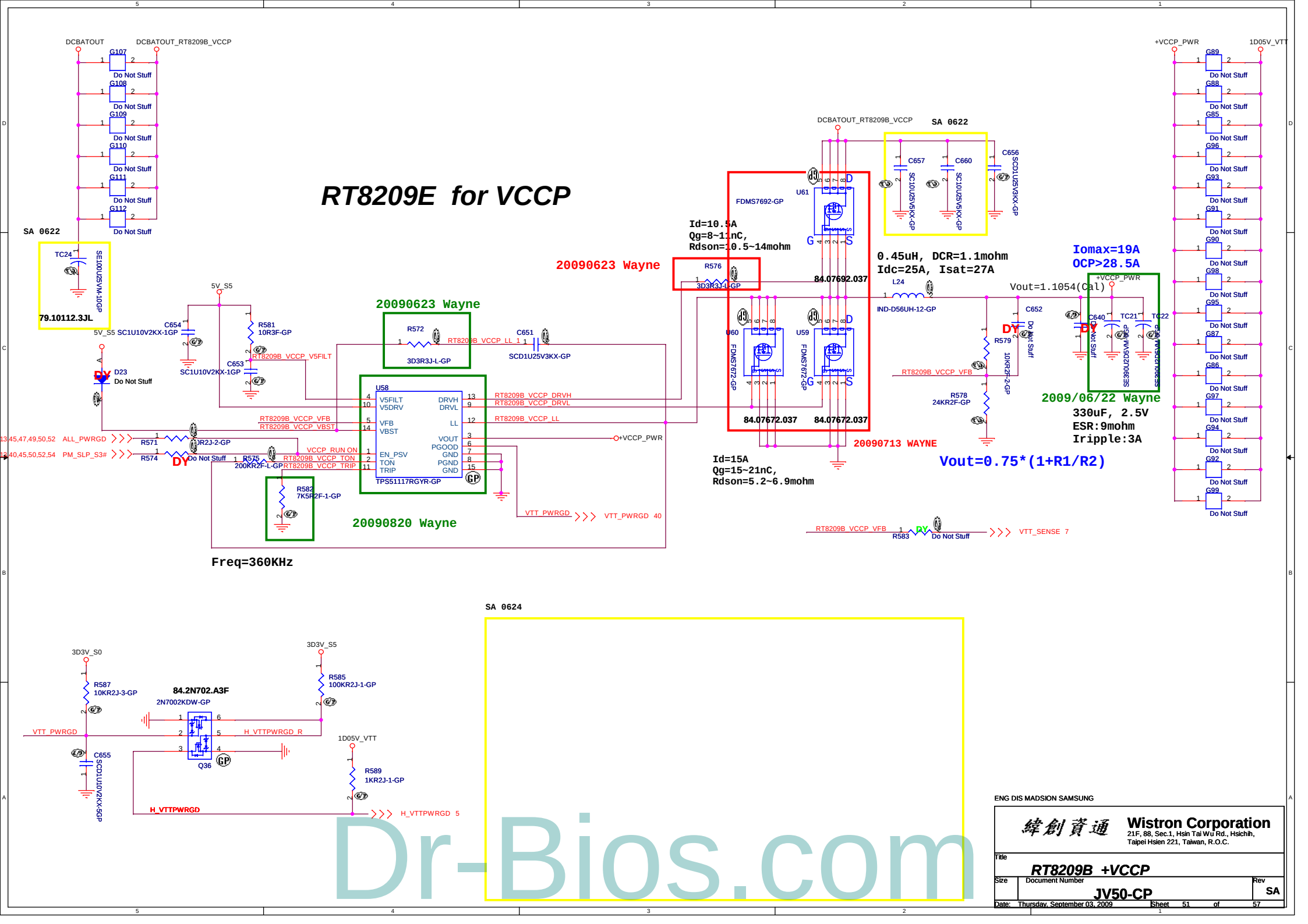
Date: Thursday, September 03, 2009 | Sheet 50 of 57


RT8209E for VCCP
DCBATOUT
DCBATOUT_RT8209B_VCCP
SA 0622
Do Not Stuff
79.10112.3JL
20090623 Wayne
Id=10.5A
Qg=8~11nC,
Rdson=10.5~14mohm
FDMS7692-GP
84.07692.037
0.45uH, DCR=1.1mohm
Idc=25A, Isat=27A
Iomax=19A
OCP>28.5A
Vout=1.1054(Cal)
2009/06/22 Wayne
330uF, 2.5V
ESR:9mohm
Iripple:3A
20090713 WAYNE
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
84.07672.037
FDMS7672-GP
Vout=0.75*(1+R1/R2)
20090820 Wayne
Freq=360KHz
TPS51117RGYR-GP
SA 0624
84.2N702.A3F
2N7002KDW-GP
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
RT8209B +VCCP
JV50-CP
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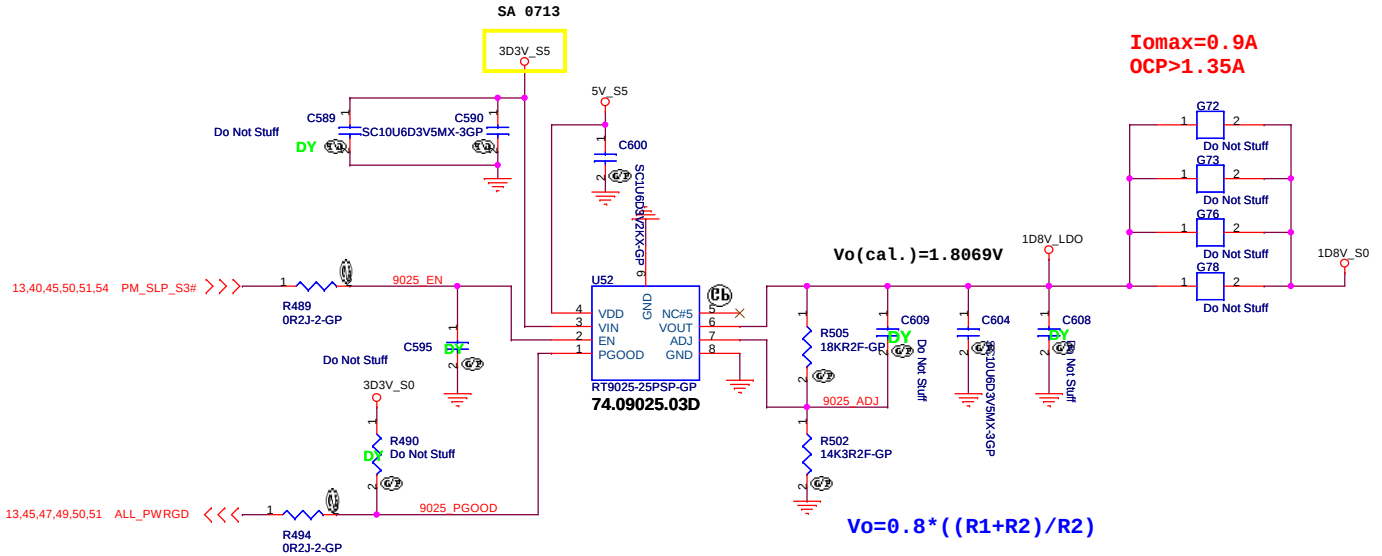
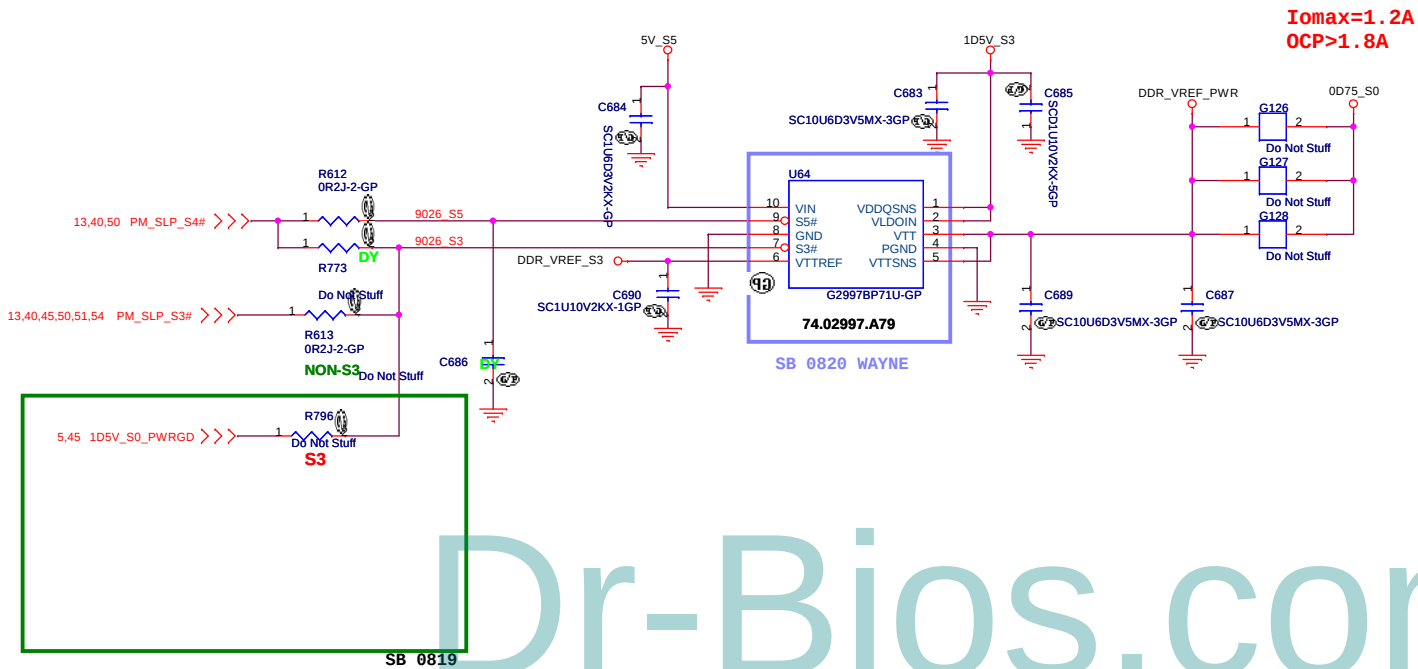
RT9025 for 1D8V_S0



RT9026 for 0D75V_S3



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025_1D8V/RT9026_0D75

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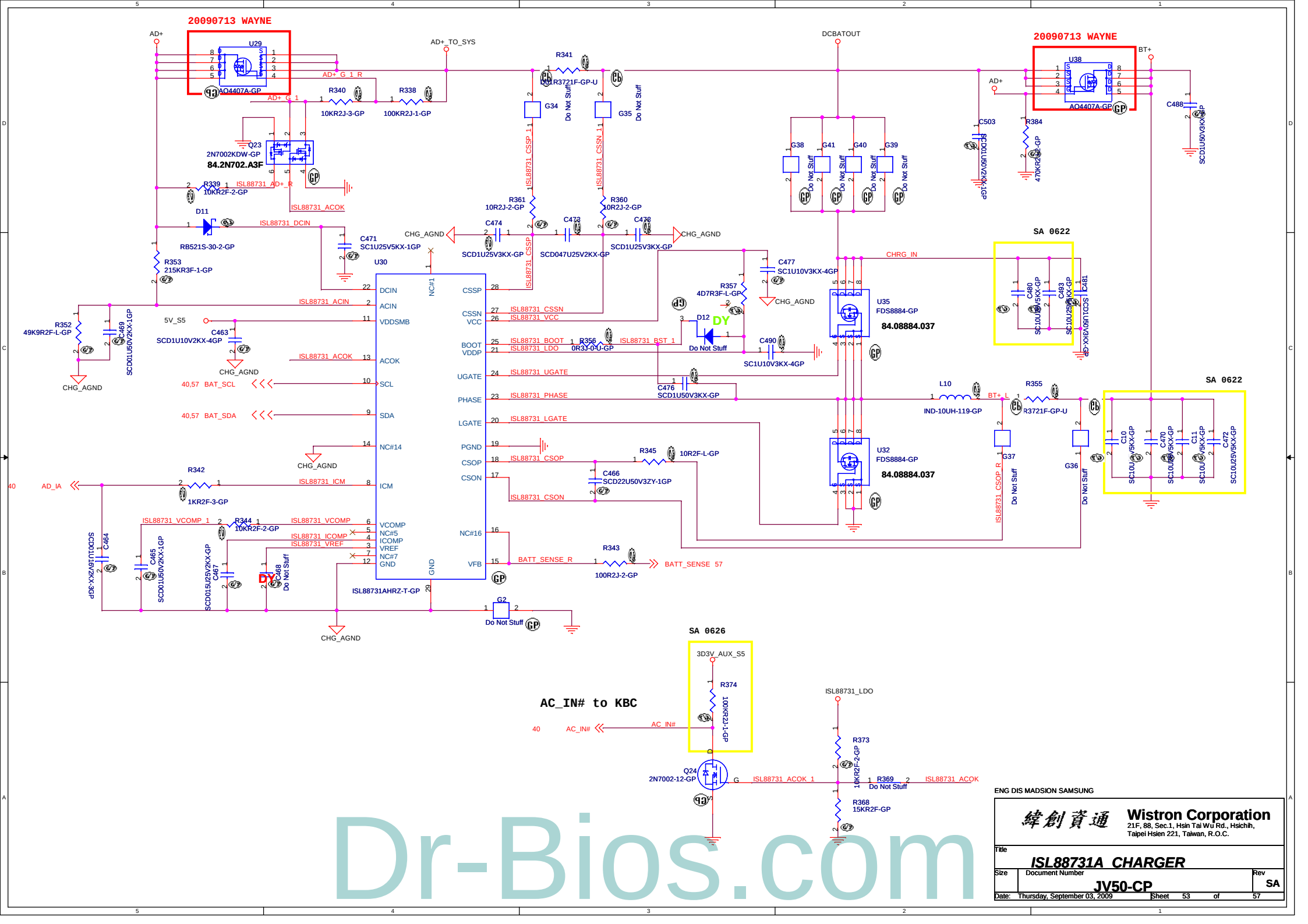
20090713 WAYNE
U29
AO4407A-GP
AD+
AD+_TO_SYS
AD+_G_1_R
AD+_G_1
R340
10KR2J-3-GP
R338
100KR2J-1-GP
Q23
2N7002KDW-GP
84.2N702.A3F
R339
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
D11
RB521S-30-2-GP
ISL88731_DCIN
C471
SC1U25V5KX-1GP
R353
215KR3F-1-GP
U30
ISL88731AHRZ-T-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
R341
R3721F-GP-U
G34
G35
Do Not Stuff
ISL88731_CSSP_1
ISL88731_CSSN_1
R361
10R2J-2-GP
R360
10R2J-2-GP
C474
SCD1U25V3KX-GP
C473
SCD047U25V2KX-GP
C472
SCD1U25V3KX-GP
CHG_AGND
ISL88731_CSSP
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731_CSOP
ISL88731_CSON
R357
4D7R3F-L-GP
D12
DY
Do Not Stuff
R356
0R3J-0-U-GP
ISL88731_BST_1
C490
SC1U10V3KX-4GP
C476
SCD1U50V3KX-GP
C477
SC1U10V3KX-4GP
CHRG_IN
U35
FDS8884-GP
84.08884.037
U32
FDS8884-GP
84.08884.037
L10
IND-10UH-119-GP
BT+_L
R355
R3721F-GP-U
R345
10R2F-L-GP
C466
SCD22U50V3ZY-1GP
R343
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 57
ISL88731_CSOP_R
G37
G36
Do Not Stuff
SA 0622
C480
SC10U25V5KX-GP
C493
SC10U25V5KX-GP
C481
SC1U25V3KX-GP
C10
SC10U25V5KX-GP
C470
SC10U25V5KX-GP
C11
SC10U25V5KX-GP
C472
SC10U25V5KX-GP
20090713 WAYNE
U38
AO4407A-GP
BT+
C488
SCD1U50V3KX-GP
C503
SCD1U50V2KX-1GP
R384
470KR2J-GP
G38
G41
G40
G39
DCBATOUT
R342
1KR2F-3-GP
AD_IA
40
ISL88731_ICM
ISL88731_VCOMP_1
R344
10KR2F-2-GP
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
C464
SCD01U16V2KX-3GP
C465
SCD01U50V2KX-1GP
C467
SCD015U25V2KX-GP
C468
Do Not Stuff
G2
Do Not Stuff
5V_S5
C463
SCD1U10V2KX-4GP
R352
49K9R2F-L-GP
C469
SCD01U50V2KX-1GP
40,57 BAT_SCL
40,57 BAT_SDA
SA 0626
3D3V_AUX_S5
R374
100KR2J-1-GP
AC_IN# to KBC
AC_IN#
Q24
2N7002-12-GP
ISL88731_ACOK_1
R369
Do Not Stuff
R373
10KR2F-2-GP
R368
15KR2F-GP
ISL88731_LDO
ENG DIS MADSION SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A CHARGER
Size
Document Number
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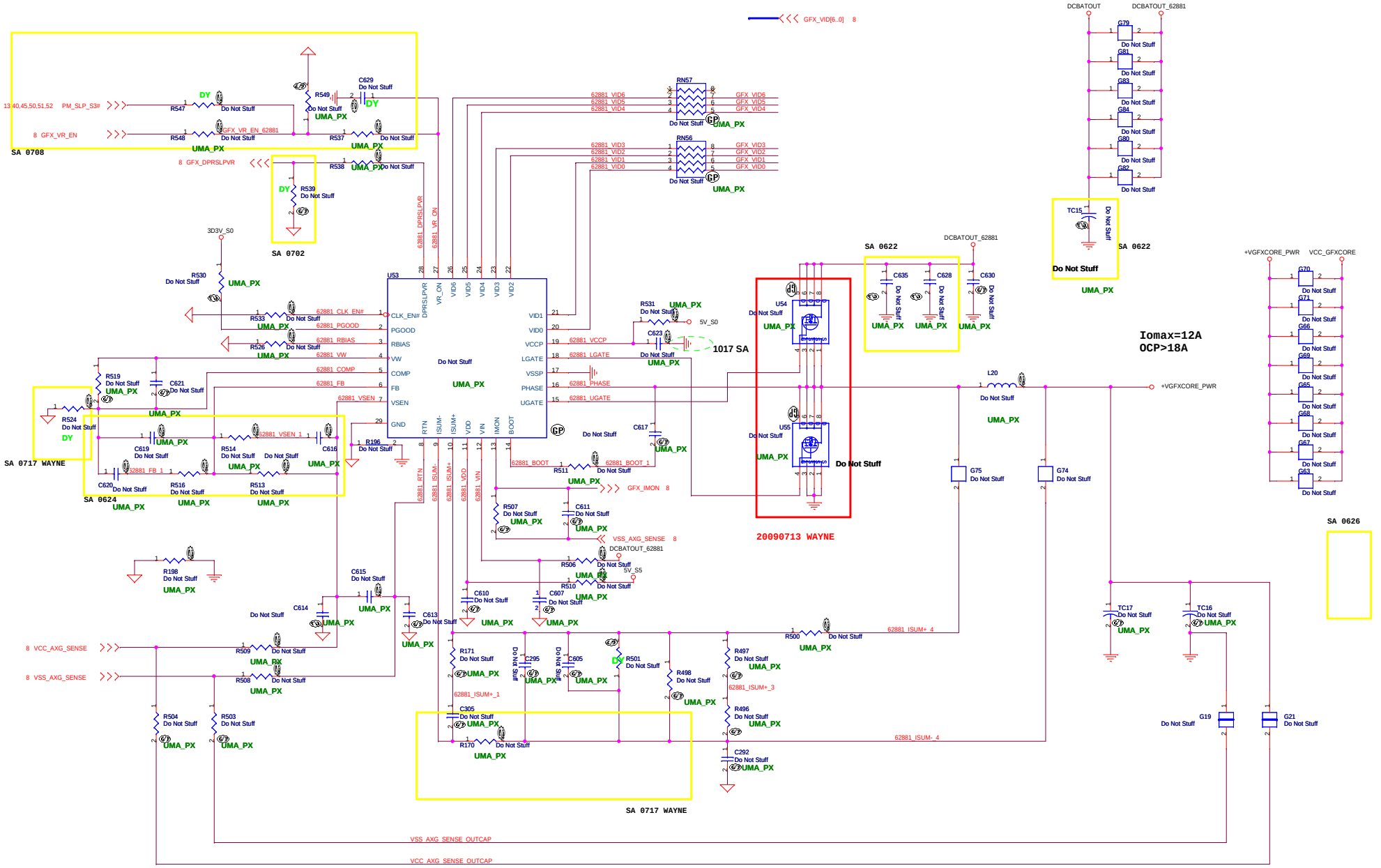

ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62881_+VCC_GFXCORE

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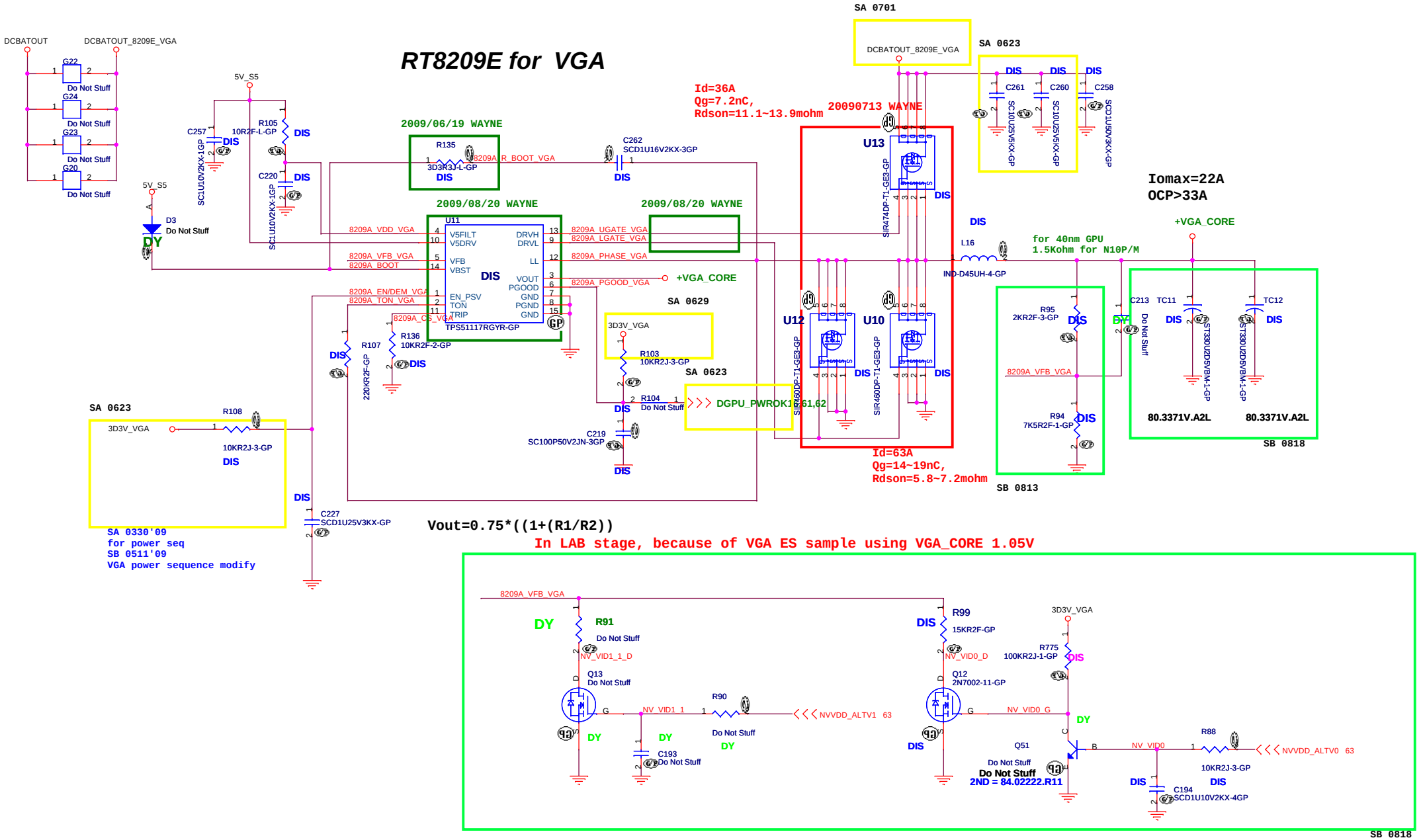
RT8209E for VGA



	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.05V GPU VOLTAGE H: 0.95V

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8209E VGA CORE**

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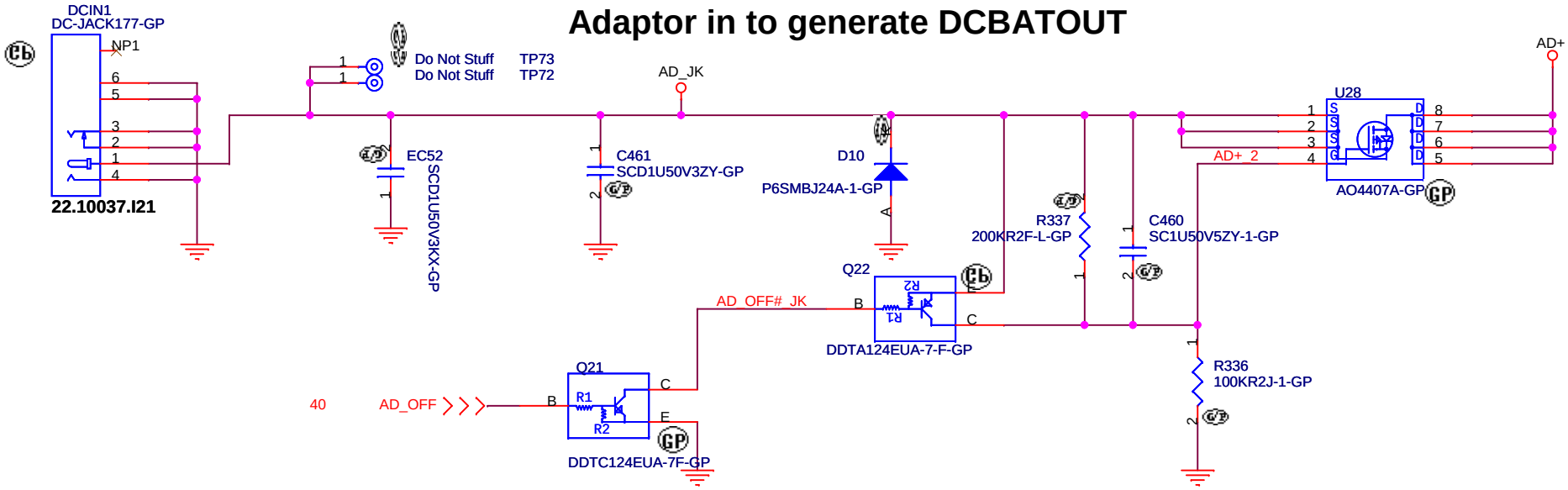
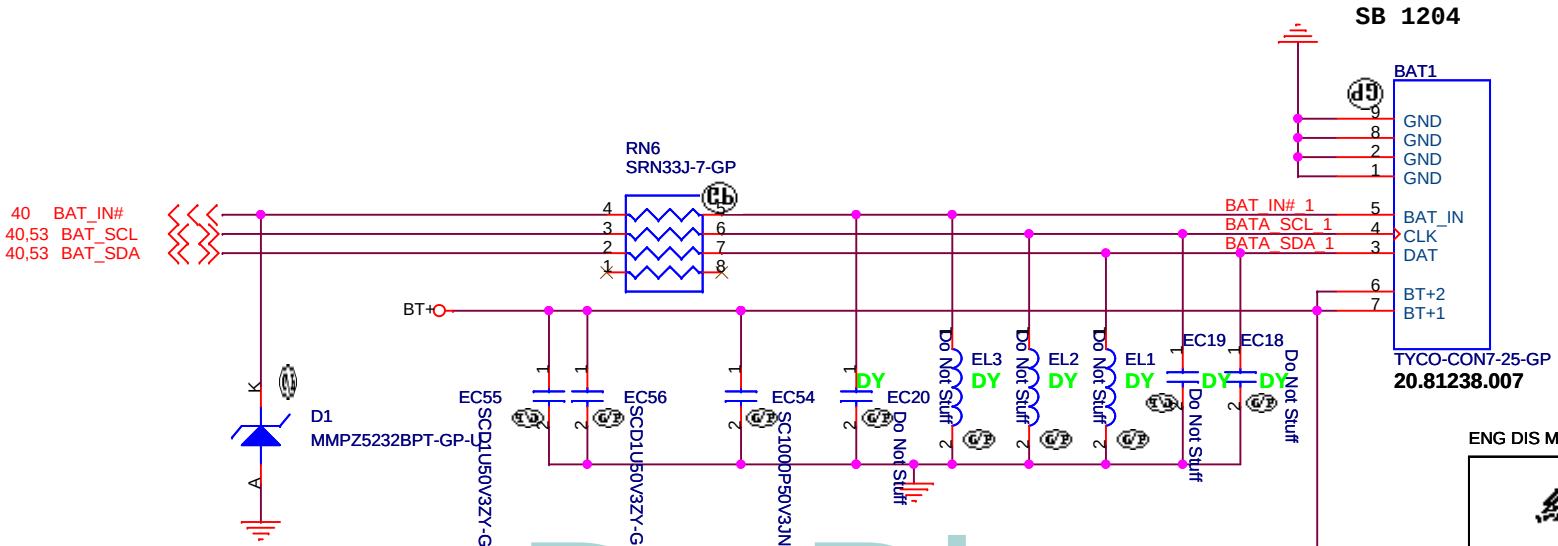
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**		
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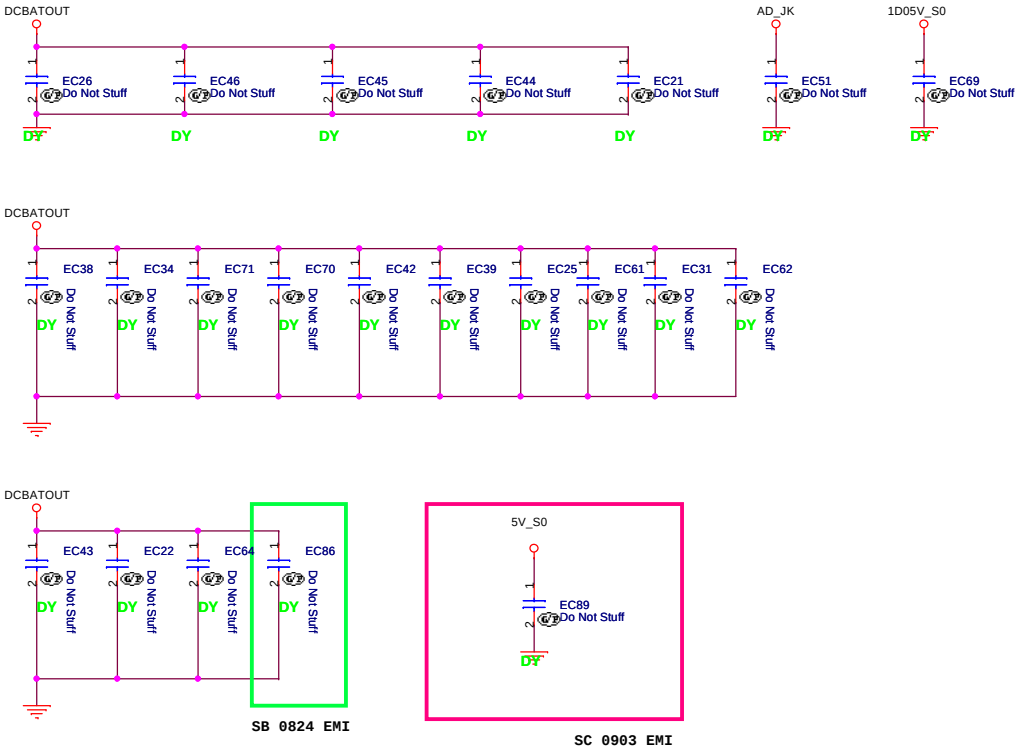

CPU

H1 H2 H3 — STF237R125H42-GP

34.4GD01.001 34.4GD01.001 34.4GD01.001

PCH

H4 — STF237R125H42-GP

34.4GD01.001

VGA

H5 DIS H6 DIS H11 DIS — STF237R125H42-GP

34.4GD01.001 34.4GD01.001 34.4GD01.001

MDC

H7 HOLE ZZ.0HOLE.XXX

34.42Y01.011

MINICARD

H8 HOLE ZZ.0HOLE.XXX

34.4P901.001

H9 Do Not Stuff H10 Do Not Stuff

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND9 GND10 GND11 GND12 — Do Not Stuff

SPRING_GND16 SPRING_GND17 SPRING_GND18 SPRING_GND19 SPRING_GND14 SPRING_GND15 SPRING_GND21 SPRING_GND22 SPRING_GND23 SPRING_GND24 SPRING_GND25 SPRING_GND26 — Do Not Stuff

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

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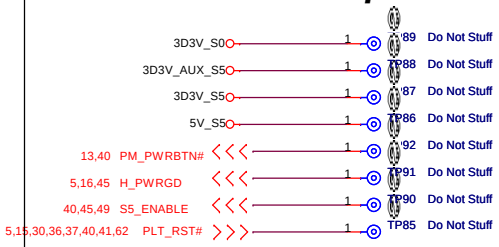
Check test point



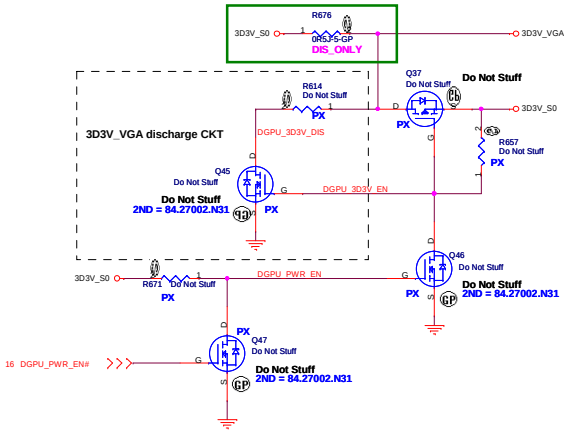
Test Point放在Dimm Door打開可量測處

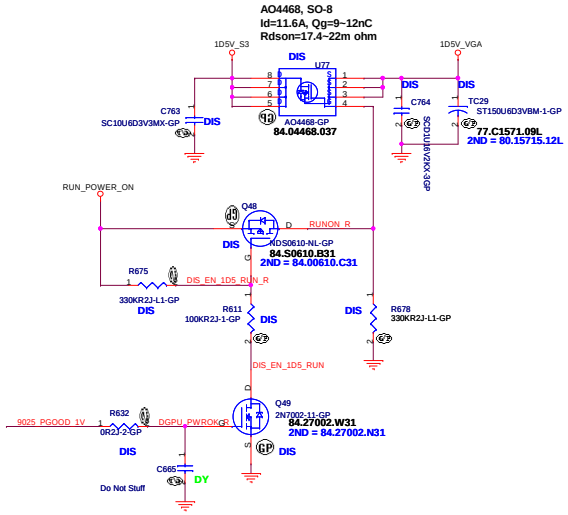
ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

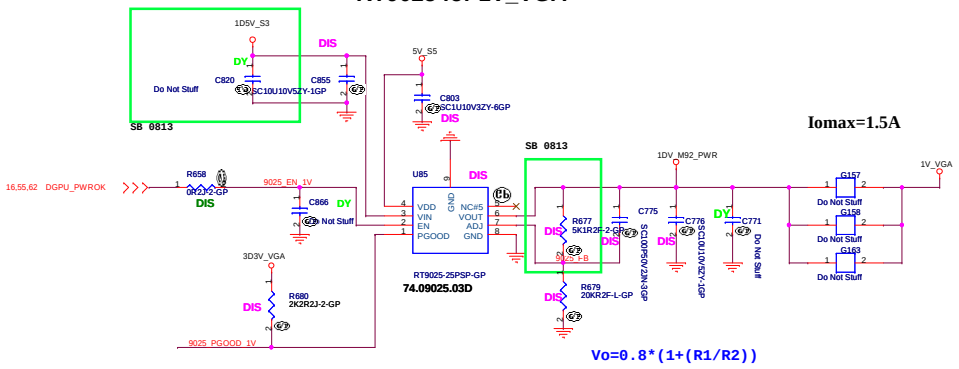
Title	AFTE_TP	
Size	Document Number JV50-CP	Rev SA
Date: Thursday, September 03, 2009	Sheet 59 of 57	

+3VS to 3.3V_DELAY Transfer

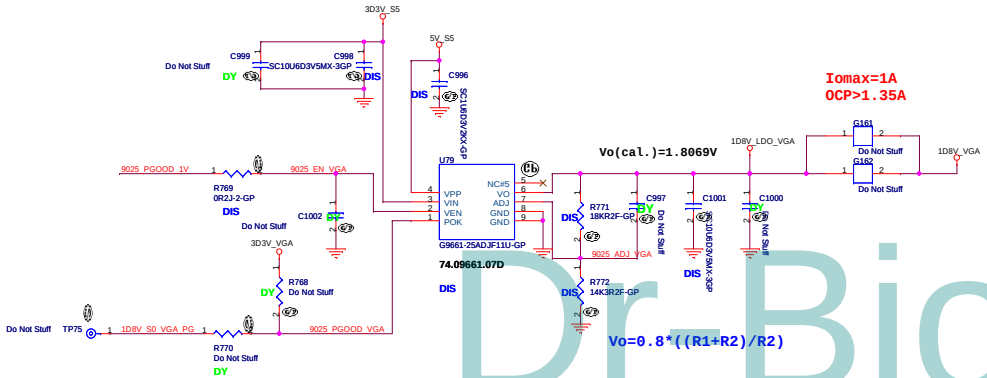




RT9025 for 1V_VGA

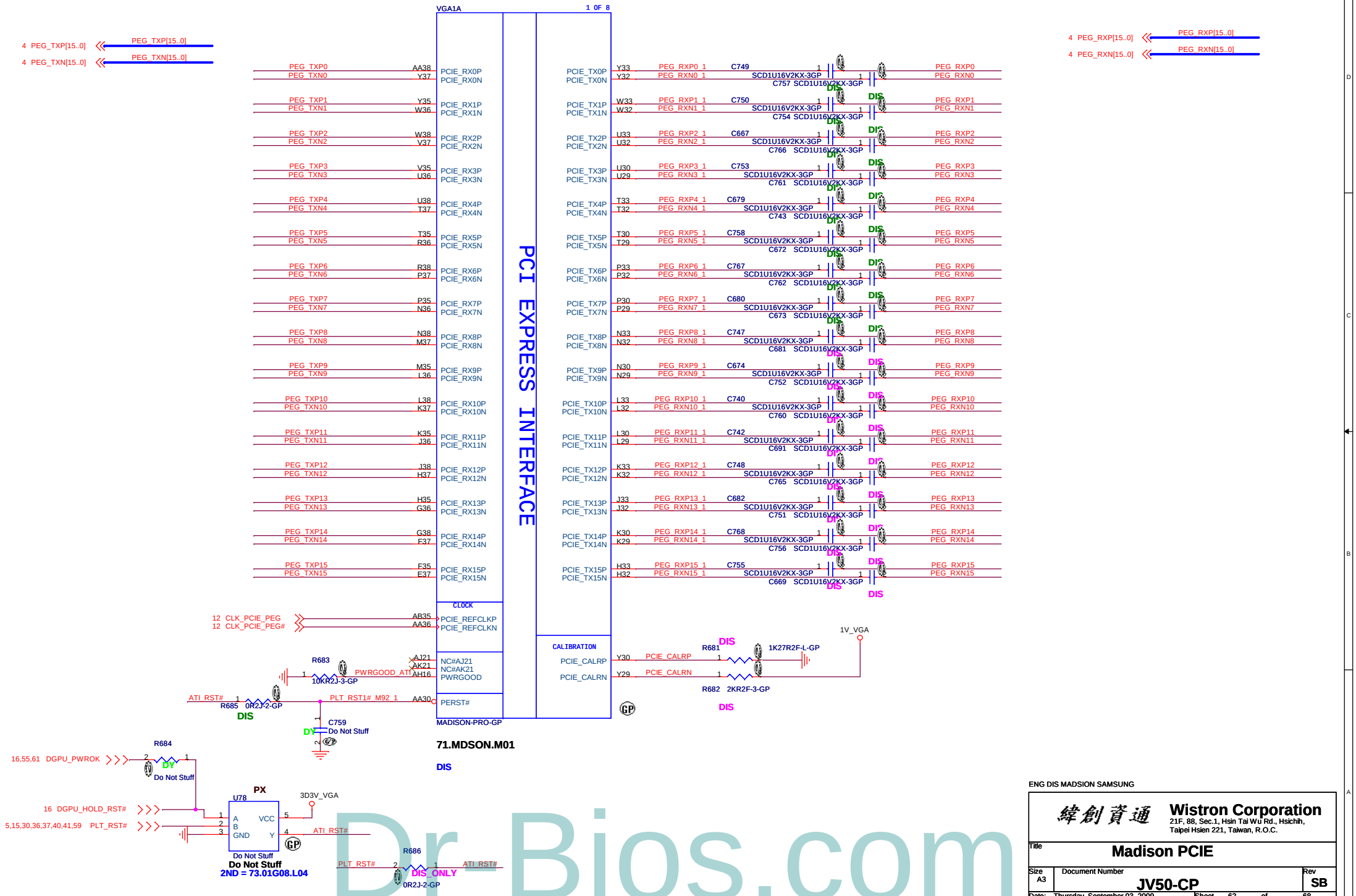


G9661 for 1D8V_VGA



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ATI POWER		
Size: A2	Document Number: JV50-CP	Rev: SB
Date: Thursday, September 03, 2009	Sheet 61 of 68	


VGA1A
1 OF 8
PCI EXPRESS INTERFACE
4 PEG_TXP[15..0]
4 PEG_TXN[15..0]
PEG_TXP[15..0]
PEG_TXN[15..0]
4 PEG_RXP[15..0]
4 PEG_RXN[15..0]
PEG_RXP[15..0]
PEG_RXN[15..0]
PEG_TXP0 AA38 PCIE_RX0P
PEG_TXN0 Y37 PCIE_RX0N
PEG_TXP1 Y35 PCIE_RX1P
PEG_TXN1 W36 PCIE_RX1N
PEG_TXP2 W38 PCIE_RX2P
PEG_TXN2 V37 PCIE_RX2N
PEG_TXP3 V35 PCIE_RX3P
PEG_TXN3 U36 PCIE_RX3N
PEG_TXP4 U38 PCIE_RX4P
PEG_TXN4 T37 PCIE_RX4N
PEG_TXP5 T35 PCIE_RX5P
PEG_TXN5 R36 PCIE_RX5N
PEG_TXP6 R38 PCIE_RX6P
PEG_TXN6 P37 PCIE_RX6N
PEG_TXP7 P35 PCIE_RX7P
PEG_TXN7 N36 PCIE_RX7N
PEG_TXP8 N38 PCIE_RX8P
PEG_TXN8 M37 PCIE_RX8N
PEG_TXP9 M35 PCIE_RX9P
PEG_TXN9 L36 PCIE_RX9N
PEG_TXP10 L38 PCIE_RX10P
PEG_TXN10 K37 PCIE_RX10N
PEG_TXP11 K35 PCIE_RX11P
PEG_TXN11 J36 PCIE_RX11N
PEG_TXP12 J38 PCIE_RX12P
PEG_TXN12 H37 PCIE_RX12N
PEG_TXP13 H35 PCIE_RX13P
PEG_TXN13 G36 PCIE_RX13N
PEG_TXP14 G38 PCIE_RX14P
PEG_TXN14 F37 PCIE_RX14N
PEG_TXP15 F35 PCIE_RX15P
PEG_TXN15 E37 PCIE_RX15N
PCIE_TX0P Y33 PEG_RXP0_1 C749 SCD1U16V2KX-3GP PEG_RXP0
PCIE_TX0N Y32 PEG_RXN0_1 C757 SCD1U16V2KX-3GP PEG_RXN0
PCIE_TX1P W33 PEG_RXP1_1 C750 SCD1U16V2KX-3GP PEG_RXP1
PCIE_TX1N W32 PEG_RXN1_1 C754 SCD1U16V2KX-3GP PEG_RXN1
PCIE_TX2P U33 PEG_RXP2_1 C667 SCD1U16V2KX-3GP PEG_RXP2
PCIE_TX2N U32 PEG_RXN2_1 C766 SCD1U16V2KX-3GP PEG_RXN2
PCIE_TX3P U30 PEG_RXP3_1 C753 SCD1U16V2KX-3GP PEG_RXP3
PCIE_TX3N U29 PEG_RXN3_1 C761 SCD1U16V2KX-3GP PEG_RXN3
PCIE_TX4P T33 PEG_RXP4_1 C679 SCD1U16V2KX-3GP PEG_RXP4
PCIE_TX4N T32 PEG_RXN4_1 C743 SCD1U16V2KX-3GP PEG_RXN4
PCIE_TX5P T30 PEG_RXP5_1 C758 SCD1U16V2KX-3GP PEG_RXP5
PCIE_TX5N T29 PEG_RXN5_1 C672 SCD1U16V2KX-3GP PEG_RXN5
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PCIE_TX7P P30 PEG_RXP7_1 C680 SCD1U16V2KX-3GP PEG_RXP7
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PCIE_TX11P L30 PEG_RXP11_1 C742 SCD1U16V2KX-3GP PEG_RXP11
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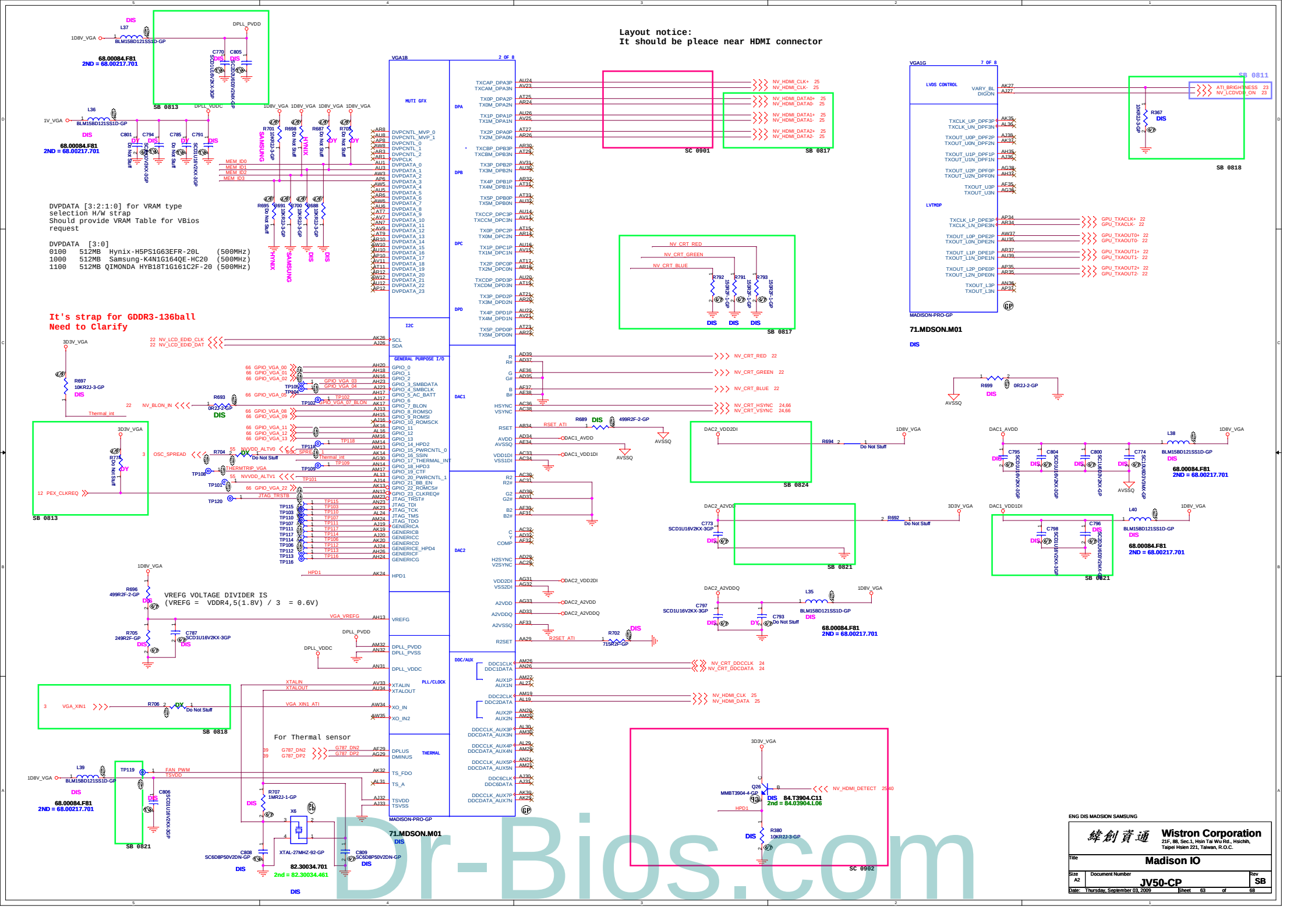
PCIE_TX14N K29 PEG_RXN14_1 C756 SCD1U16V2KX-3GP PEG_RXN14
PCIE_TX15P H33 PEG_RXP15_1 C755 SCD1U16V2KX-3GP PEG_RXP15
PCIE_TX15N H32 PEG_RXN15_1 C669 SCD1U16V2KX-3GP PEG_RXN15
DIS
CLOCK
12 CLK_PCIE_PEG
12 CLK_PCIE_PEG#
AB35 PCIE_REFCLKP
AA36 PCIE_REFCLKN
AJ21 NC#AJ21
AK21 NC#AK21
AH16 PWRGOOD
AA30 PERST#
CALIBRATION
Y30 PCIE_CALRP
Y29 PCIE_CALRN
R681 DIS 1K27R2F-L-GP
R682 2KR2F-3-GP
1V_VGA
R683 10KR2J-3-GP
PWRGOOD_ATI
ATI_RST#
R685 0R2J-2-GP
PLT_RST1#_M92_1
C759 Do Not Stuff
DY
R684 DY Do Not Stuff
16,55,61 DGPU_PWROK
16 DGPU_HOLD_RST#
5,15,30,36,37,40,41,59 PLT_RST#
PX
U78
A
B
GND
VCC
Y
3D3V_VGA
ATI_RST#
Do Not Stuff
Do Not Stuff
2ND = 73.01G08.L04
R686 DIS_ONLY 0R2J-2-GP
PLT_RST#
ATI_RST#
MADISON-PRO-GP
71.MDSON.M01
DIS
ENG DIS MADSION SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Madison PCIE
Size A3
Document Number
JV50-CP
Rev SB
Date: Thursday, September 03, 2009
Sheet 62 of 68


Layout notice:
It should be pleace near HDMI connector
DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request
DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)
It's strap for GDDR3-136ball
Need to Clarify
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
For Thermal sensor
VGA1B
MUTI GFX
I2C
GENERAL PURPOSE I/O
PLL/CLOCK
THERMAL
MADISON-PRO-GP
71.MDSON.M01
VGA1G
LVDS CONTROL
LVTMDP
SC 0901
SB 0817
SB 0824
SB 0821
SB 0813
SB 0818
SB 0811
SC 0902
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison IO
JV50-CP
Rev SB
Thursday, September 03, 2009
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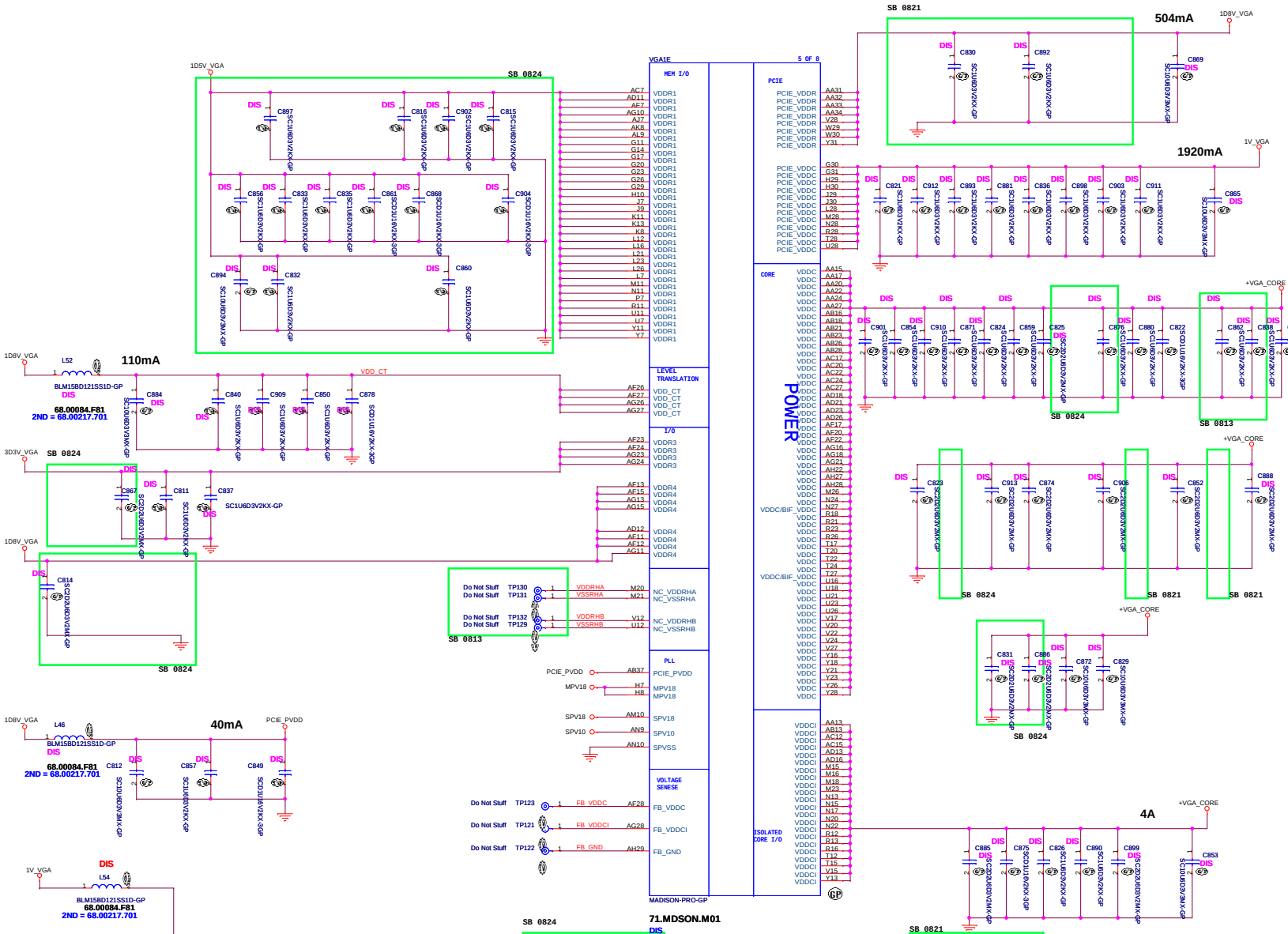
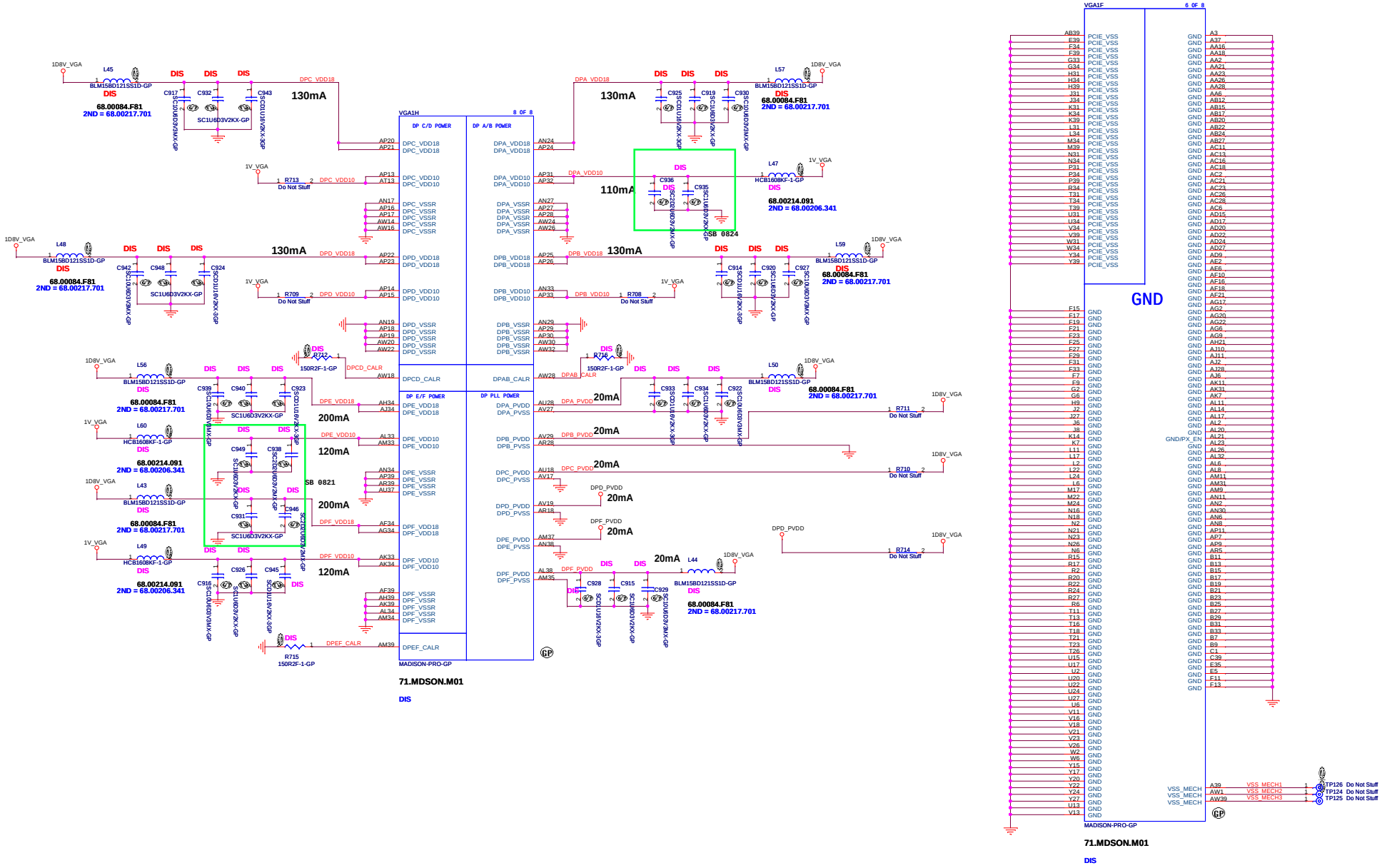


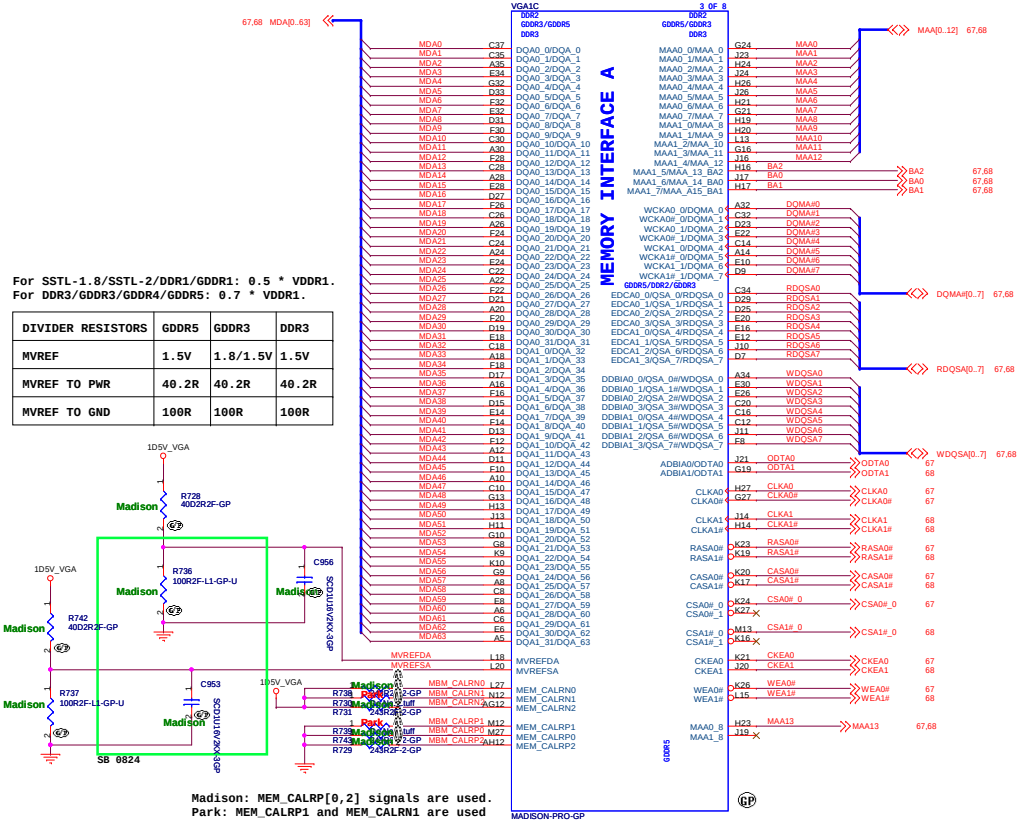
ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Madison POWER		
Size: A2	Document Number: JV50-CP	Rev: SB
Date: Wednesday, August 26, 2009	Sheet 64 of 68	

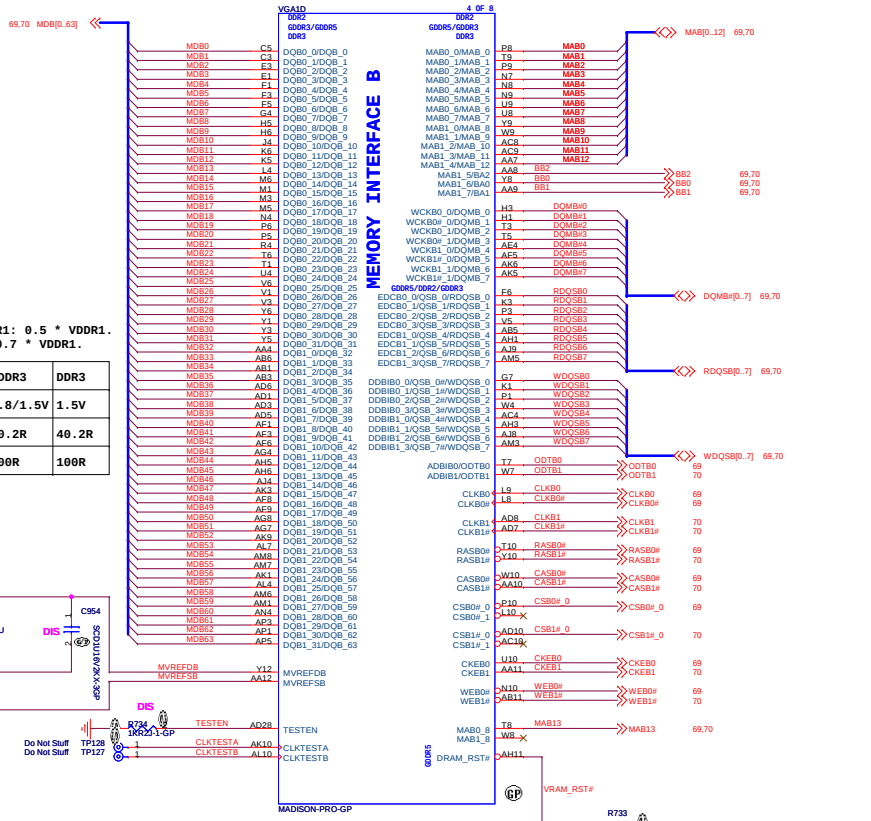


ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DP POWER_GND
Size: A2	Document Number: JV50-CP
Rev: SB	
Date: Wednesday, August 26, 2009	Sheet 65 of 68



DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

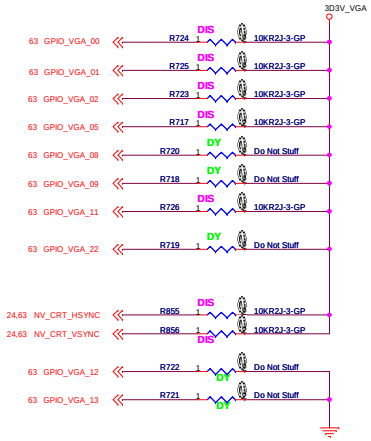
STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			



Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

ENG DIS MADSION SAMSUNG

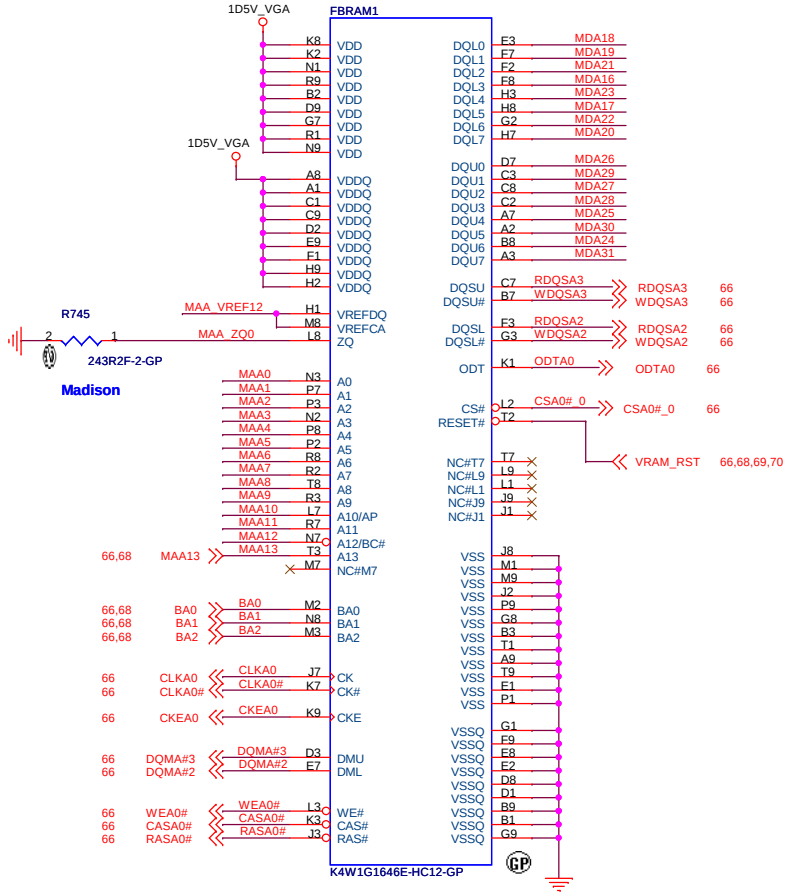
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

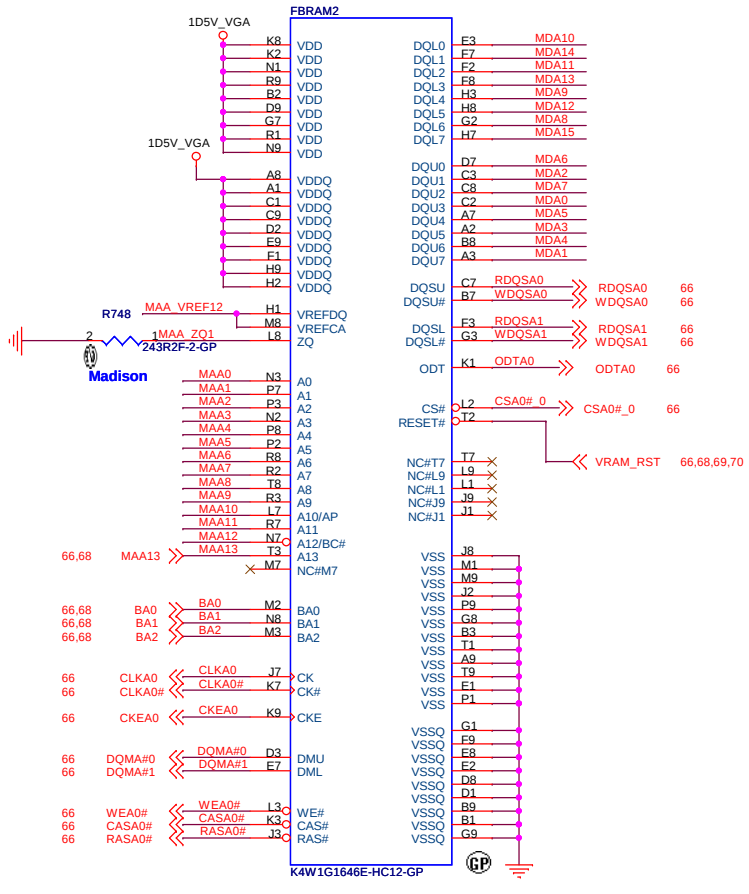
Title: **Madison Memory / Straps**

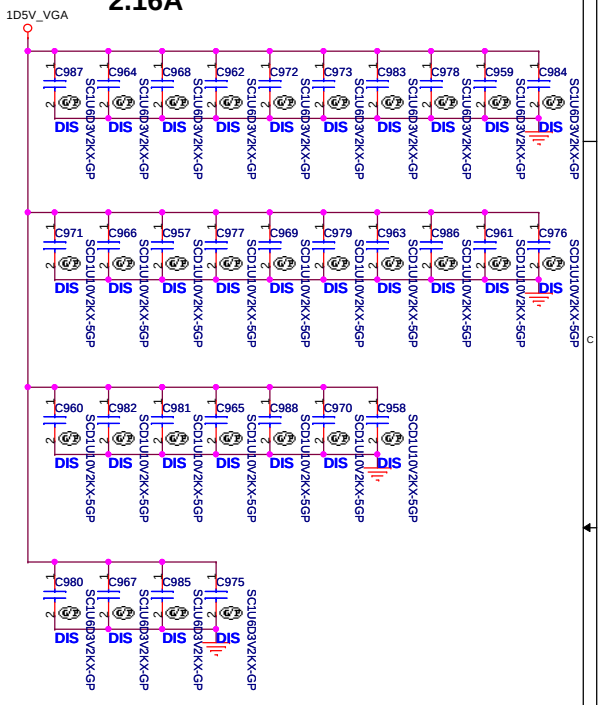
Size: A2 | Document Number: **JV50-CP** | Rev: SB

Date: Thursday, September 03, 2009 | Sheet 66 of 68

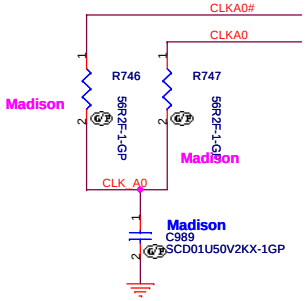
DDR3

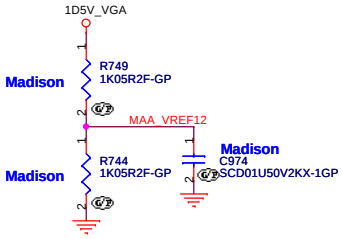


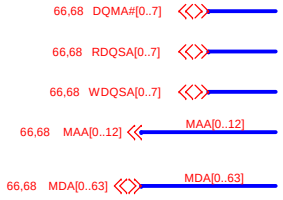




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



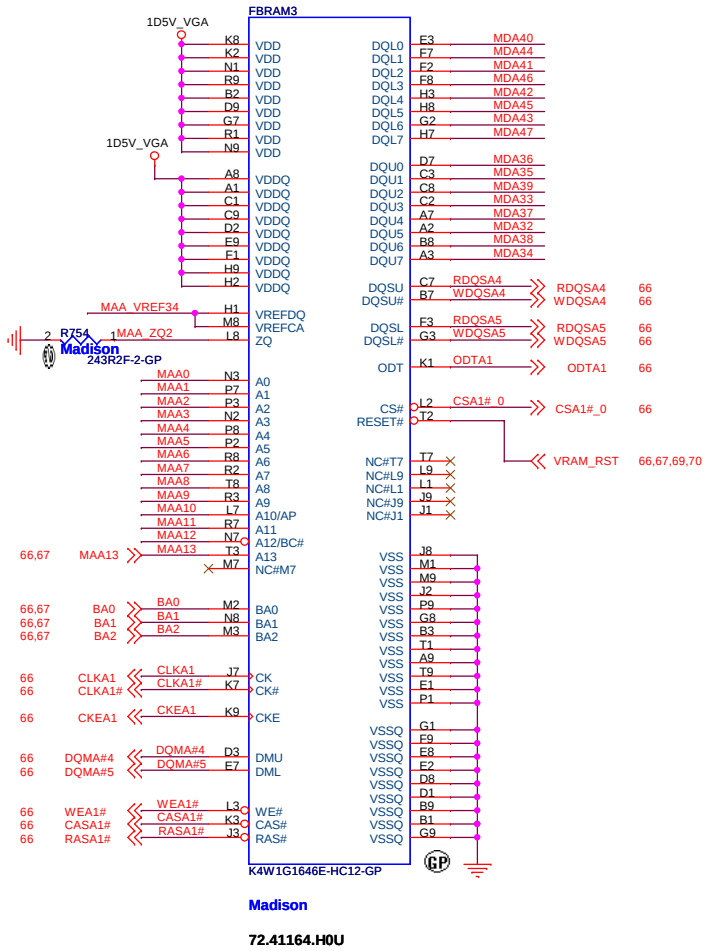


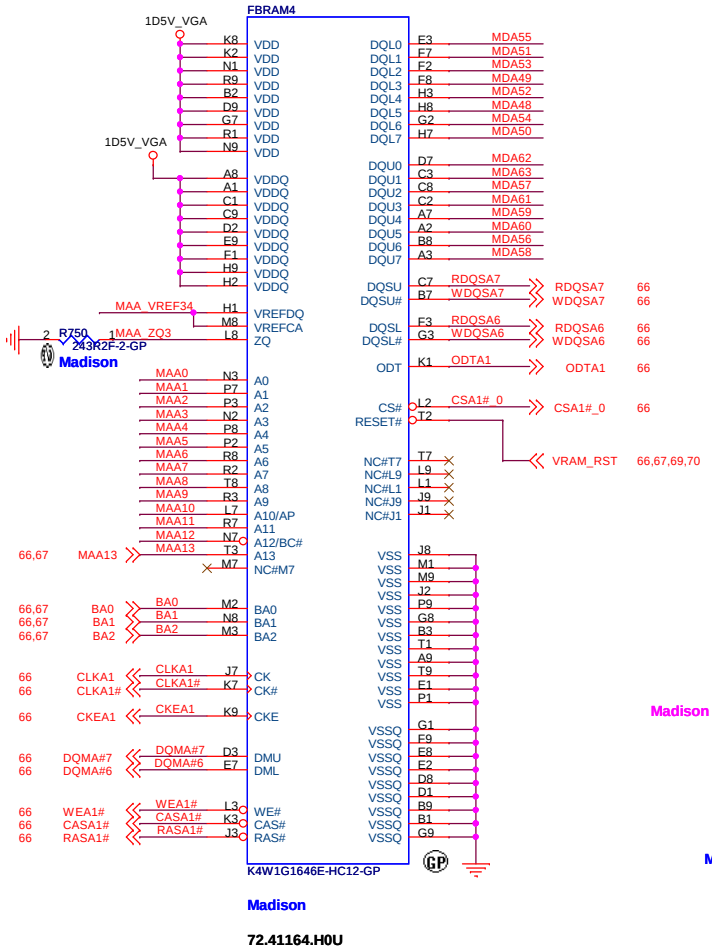


ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(1/4)***	
Size A3	Document Number **JV50-CP**	Rev **SB**
Date: Thursday, September 03, 2009	Sheet 67 of 68	

DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

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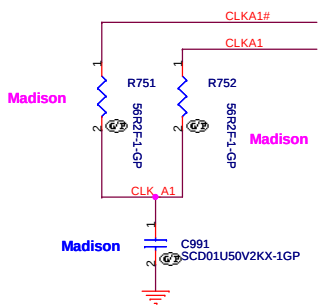
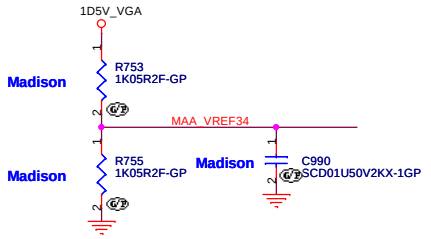
66,67 WDQSA[0..7]
66,67 MAA[0..12]
66,67 MDA[0..63]

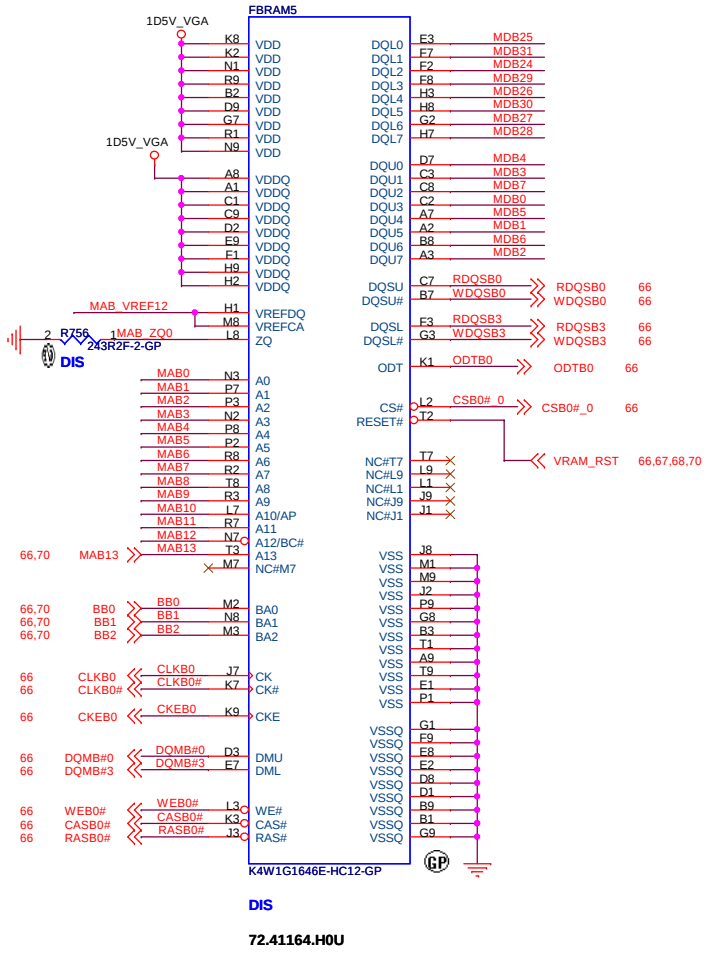


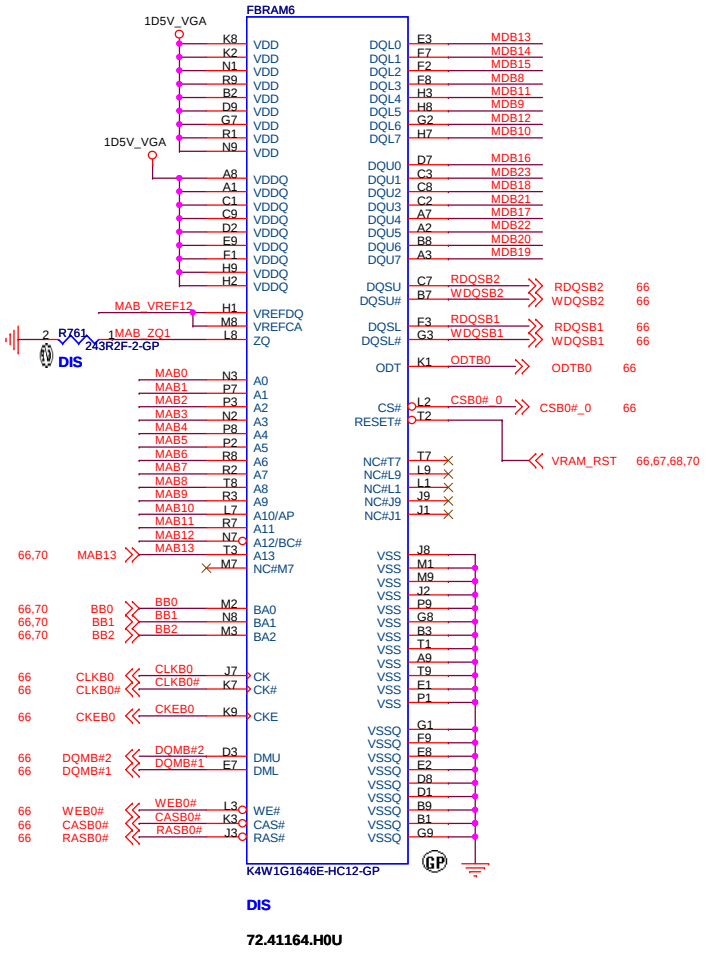


ENG DIS MADSION SAMSUNG

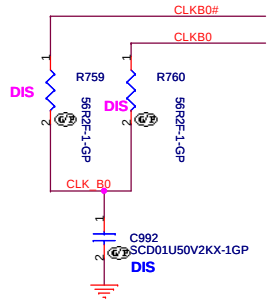
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *VRAM(2/4)*		
Size: A3	Document Number: JV50-CP	Rev: SB
Date: Thursday, September 03, 2009	Sheet 68 of 68	

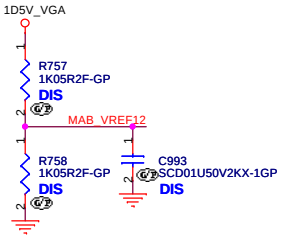
DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U





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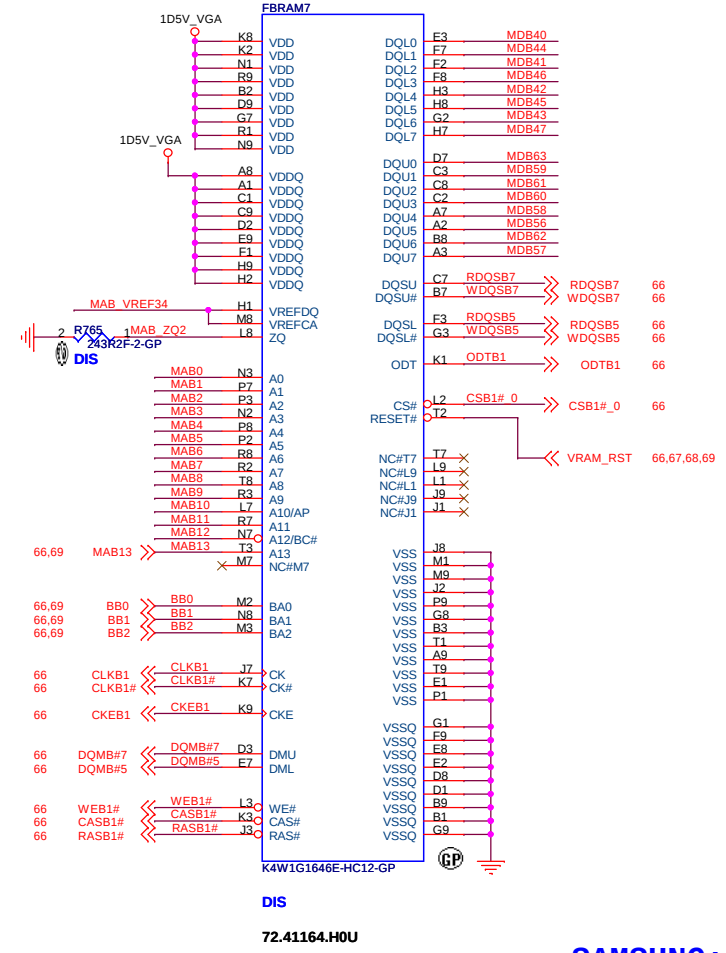
66,70 RDQSB[0..7]
66,70 WDQSB[0..7]
66,70 MAB[0..12] MAB[0..12]
66,70 MDB[0..63] MDB[0..63]

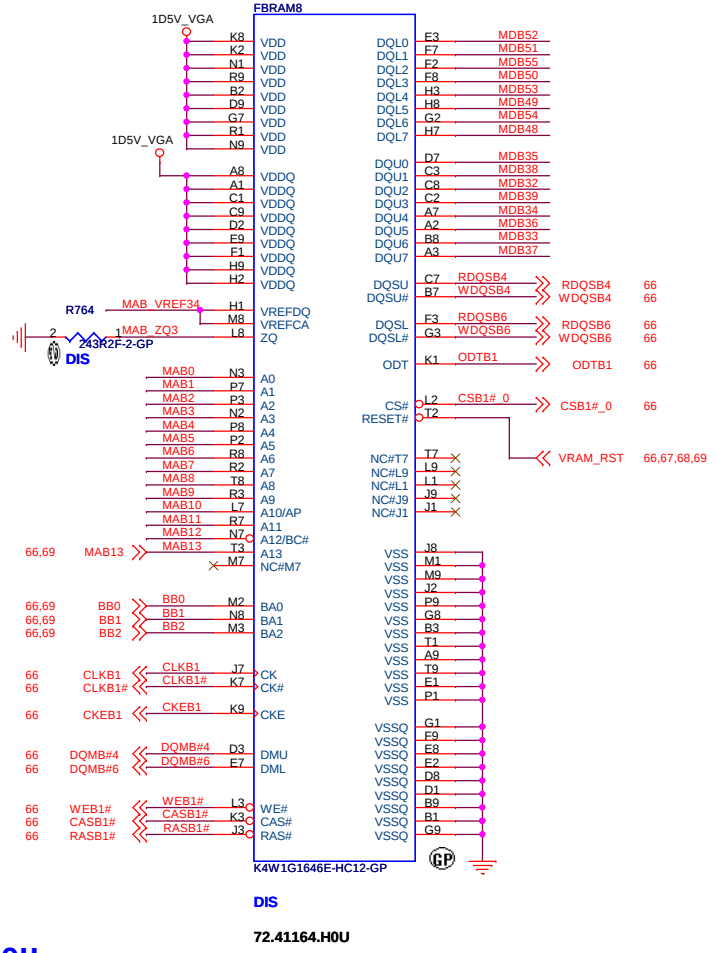
ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM(3/4)	
Size A3	Document Number JV50-CP	Rev SB
Date: Thursday, September 03, 2009	Sheet 69 of 68	

DDR3





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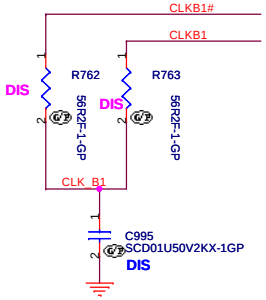

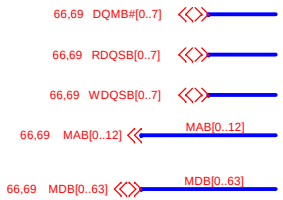

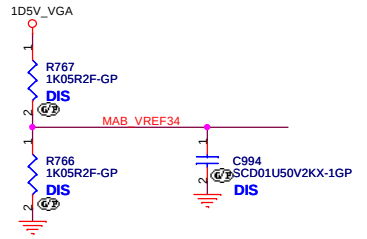

ENG DIS MADSION SAMSUNG

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