

# Compal Confidential

## JDW50/JDY70 Schematics Document

Intel Merom Processor with Crestline(PM945/GM945) + DDRII + ICH7M  
(With ATI MXM/B)

2007-5-3

REV: 1A

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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Card Reader	AD16	0	PIRQE

## EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

## EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b

## ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

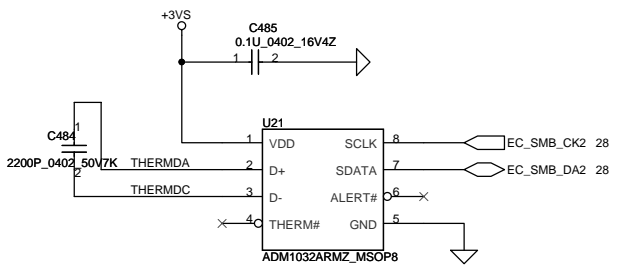
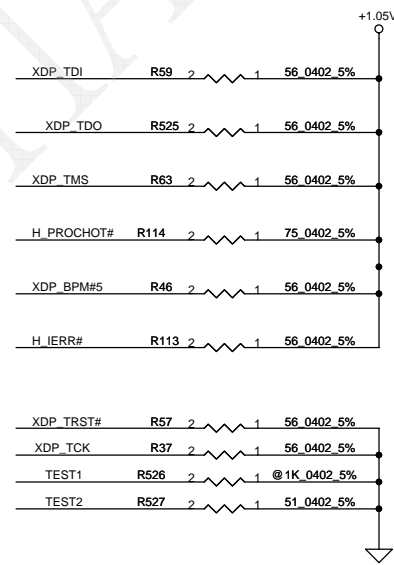
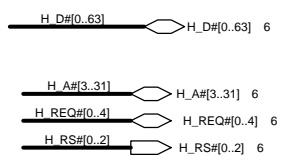
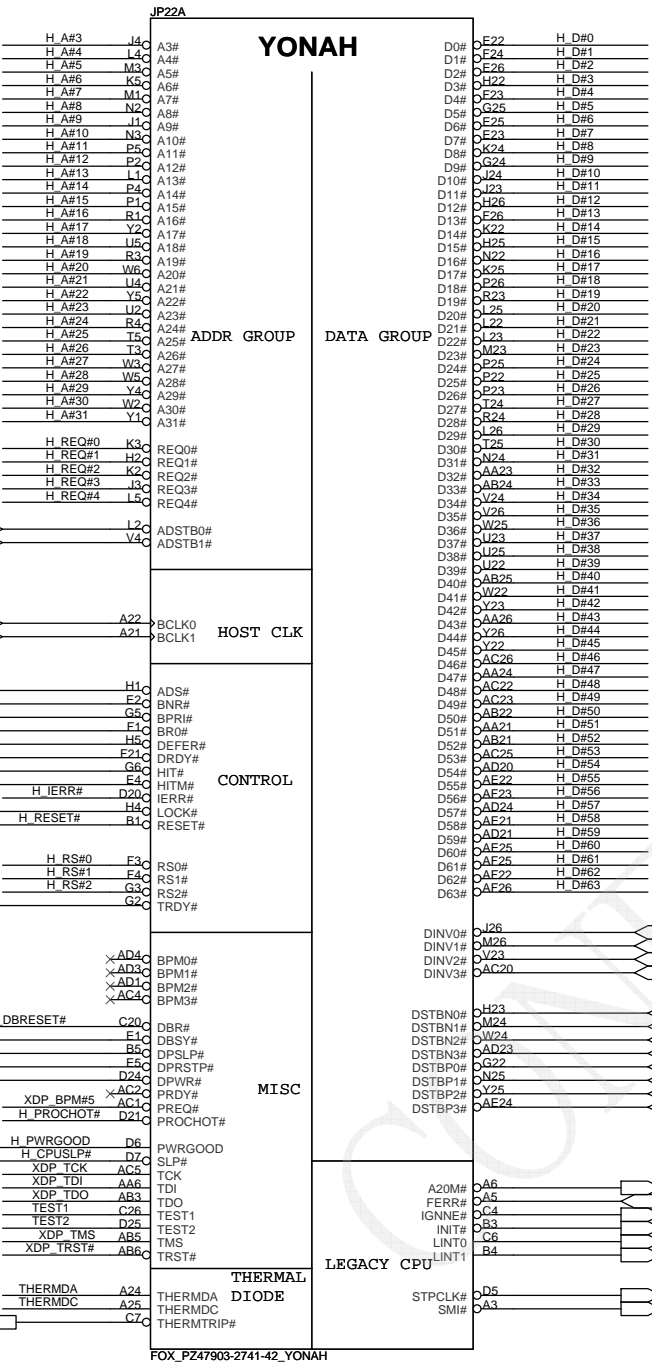
## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

## BTO Option Table

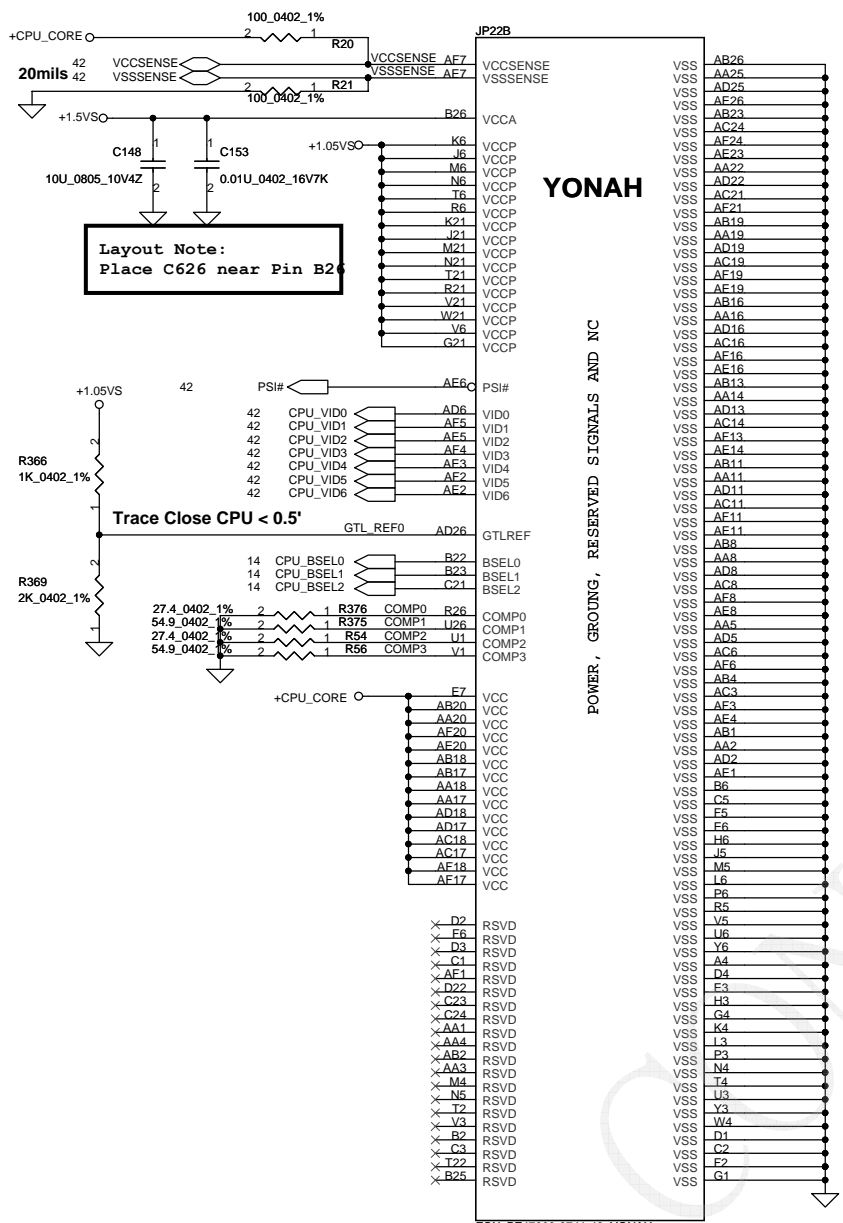
BTO Item	BOM Structure
Discrete	PM@
UMA	GM@
DVI	DVI@
SATA*1	SATA*1@
SATA*2	SATA*2@
Dbg	Dbg@

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**Layout Note:**  
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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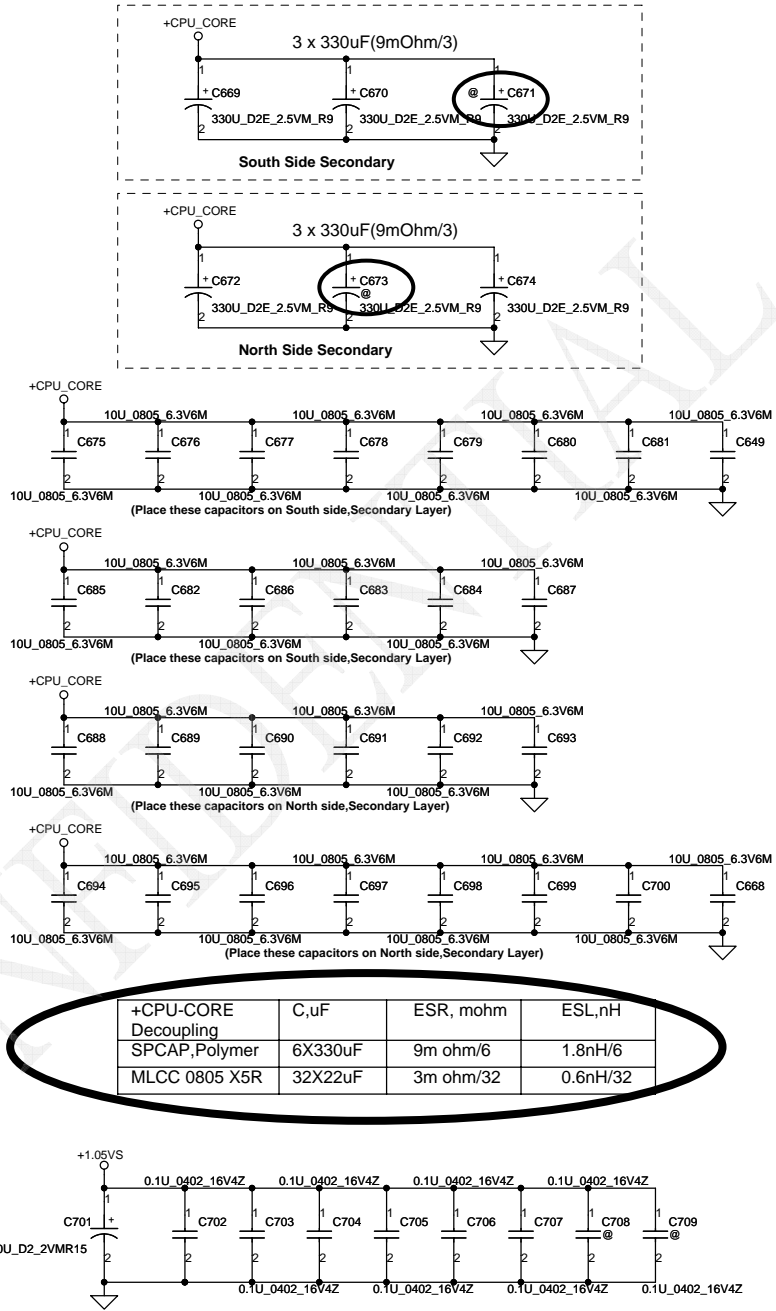
**Layout Note:**  
Place C26 near Pin B2

**Trace Close CPU < 0.5'**

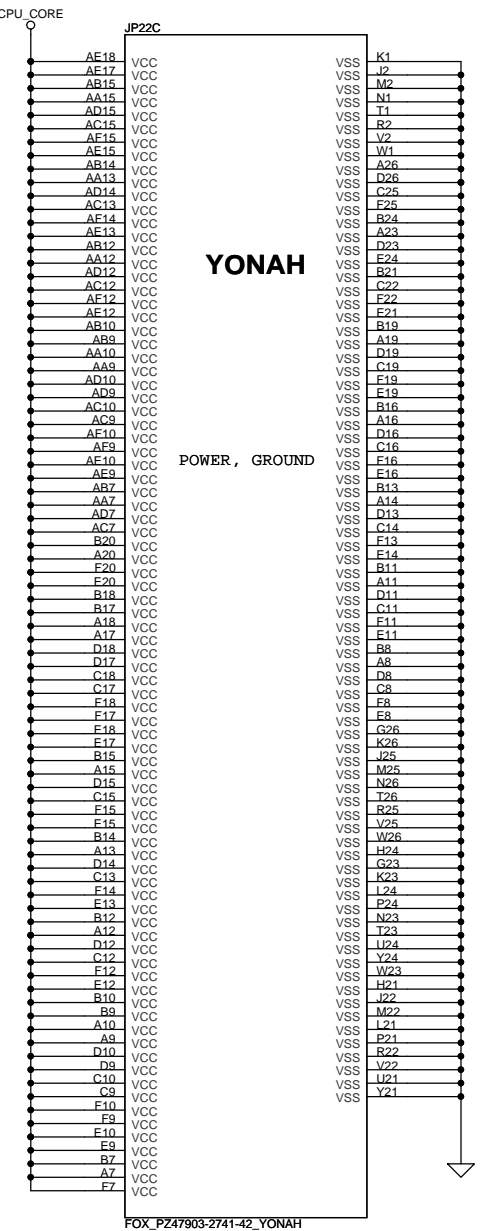
### YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

FOX\_PZ47903-2741-42\_YONAH



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32



### YONAH

POWER, GROUND

FOX\_PZ47903-2741-42\_YONAH

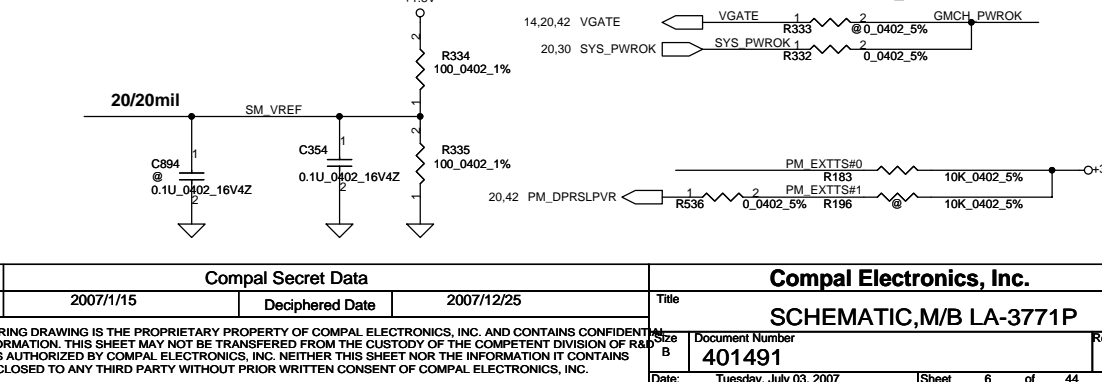
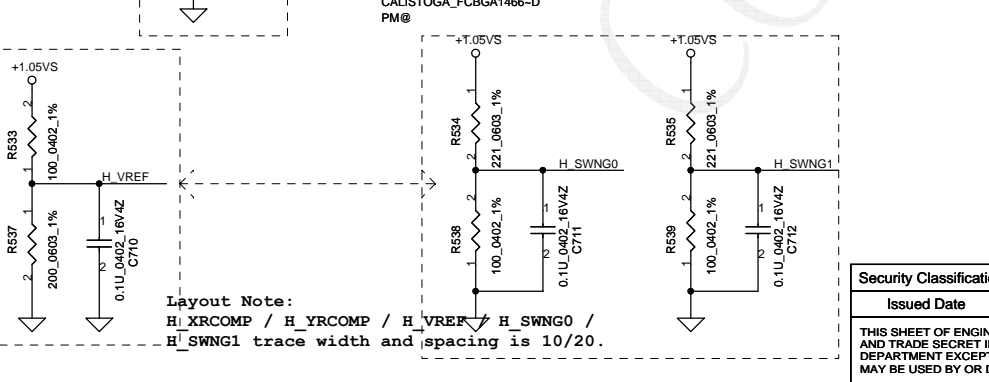
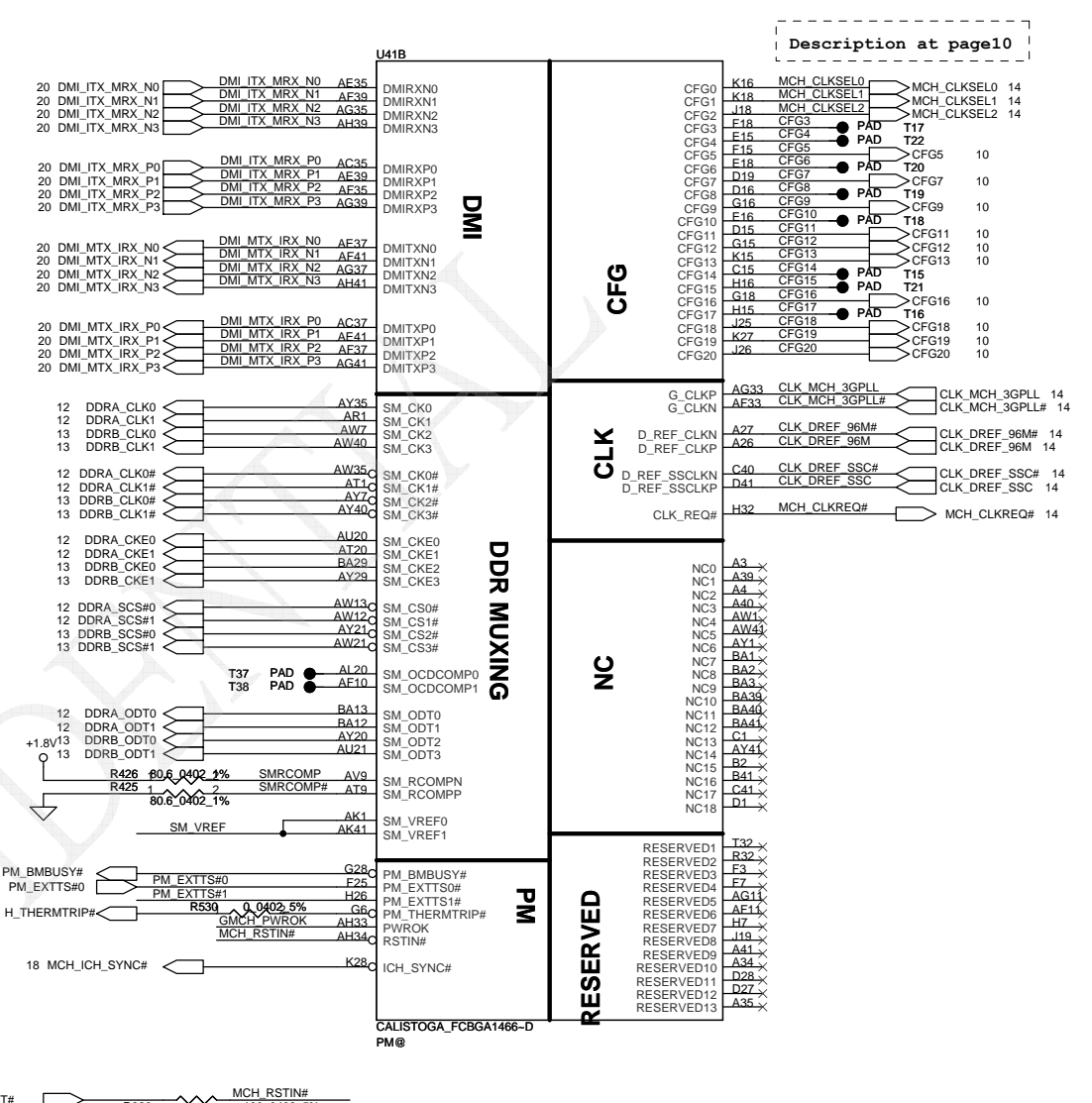
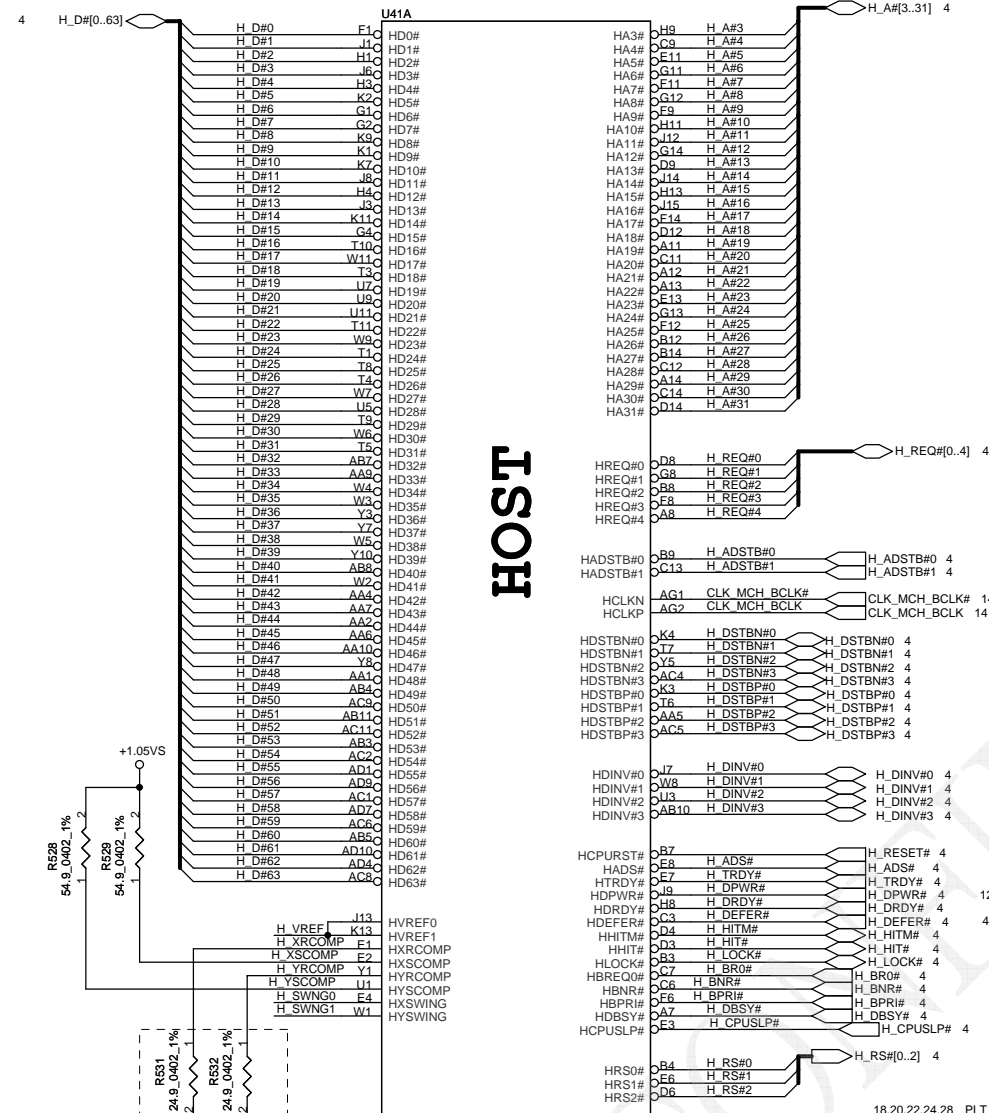
**TRACE CLOSELY CPU < 0.5'**  
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4ohms)  
COMP1, COMP3 layout : Space 25mils (55ohms)

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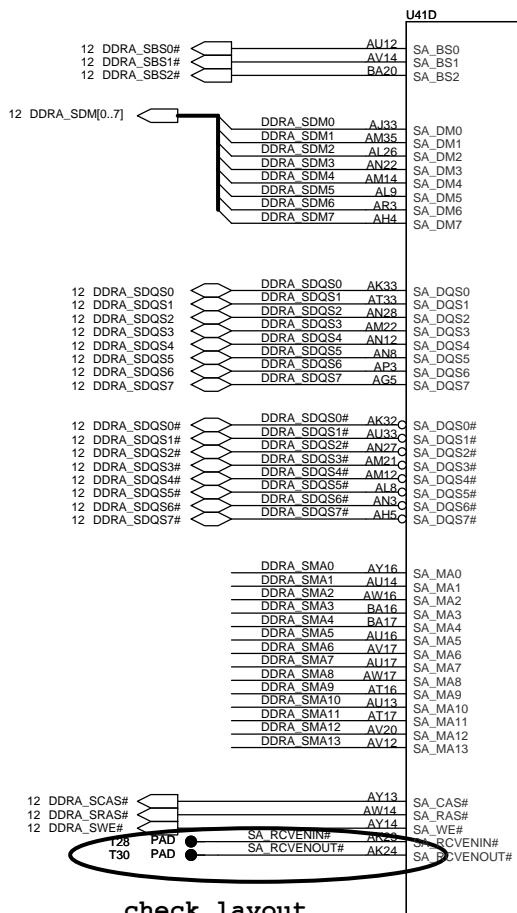
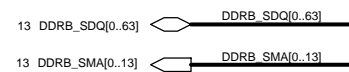
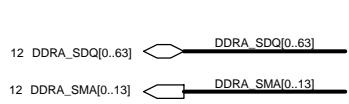
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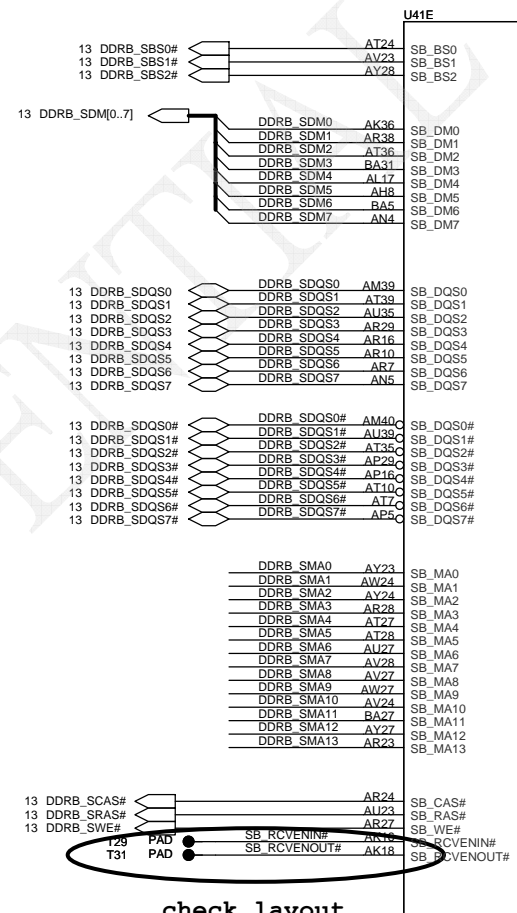
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**DDR SYS MEMORY A**

CALISTOGA\_FCBGA1466-D  
PM@

check layout

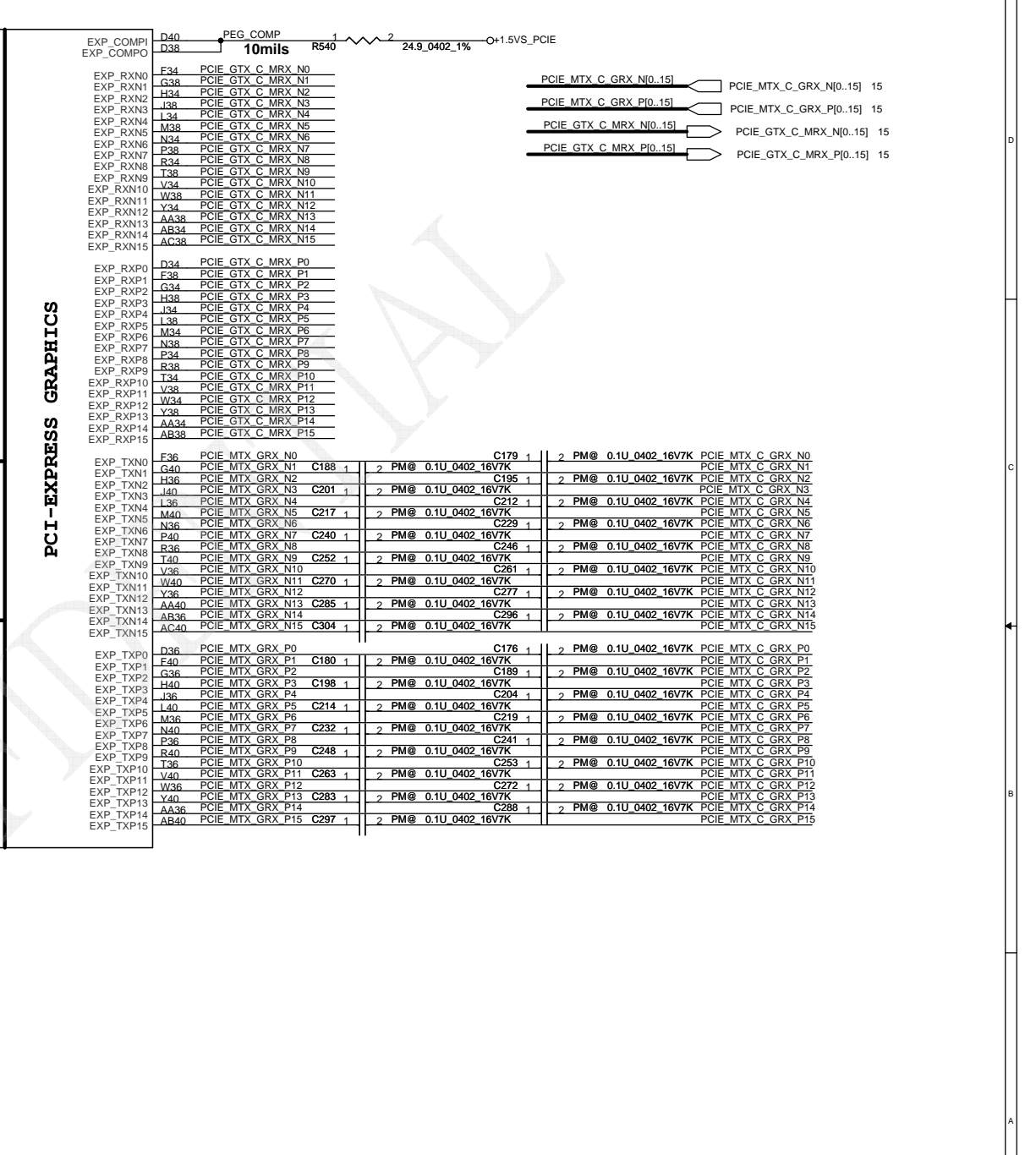
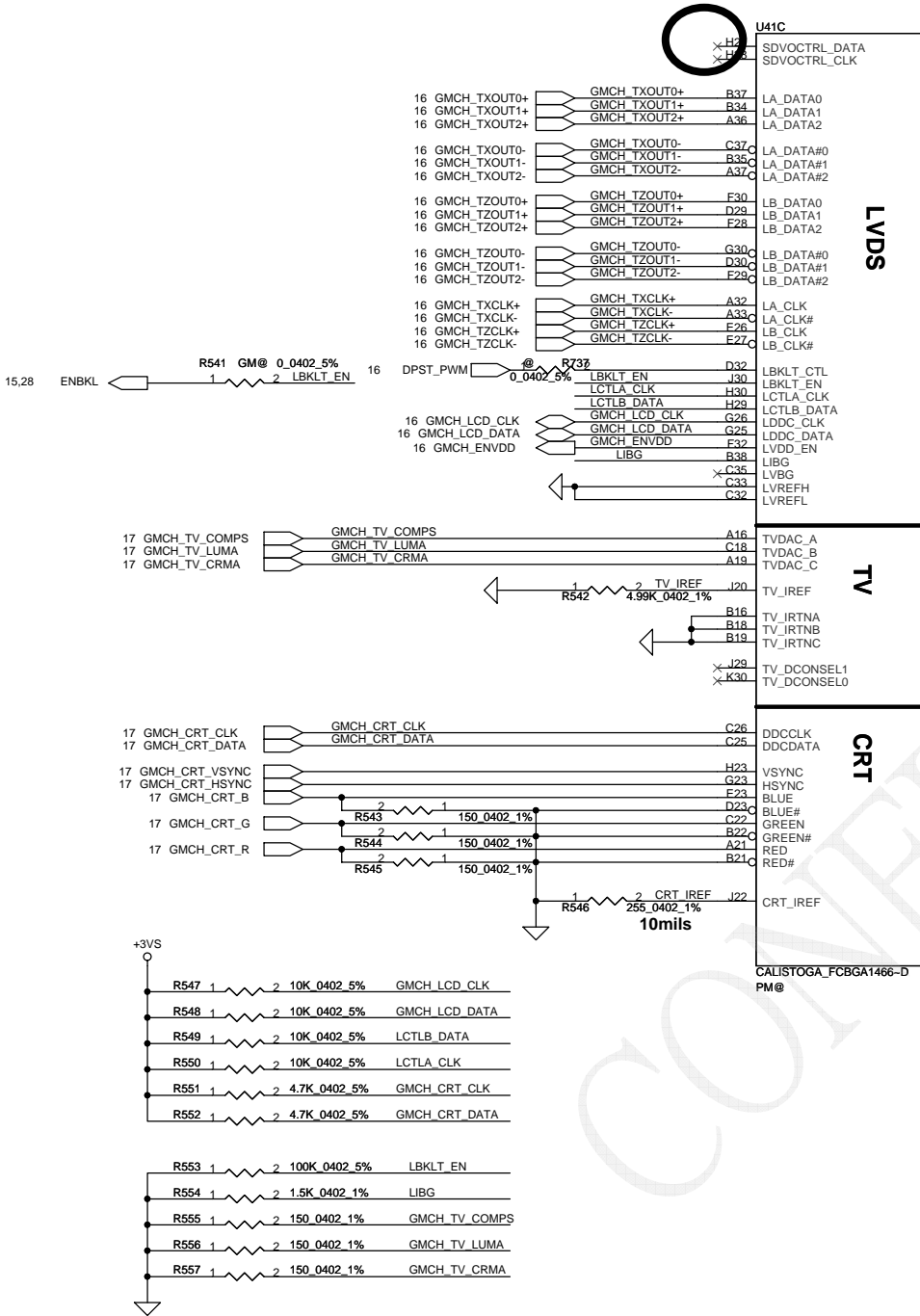


**DDR SYS MEMORY B**

CALISTOGA\_FCBGA1466-D  
PM@

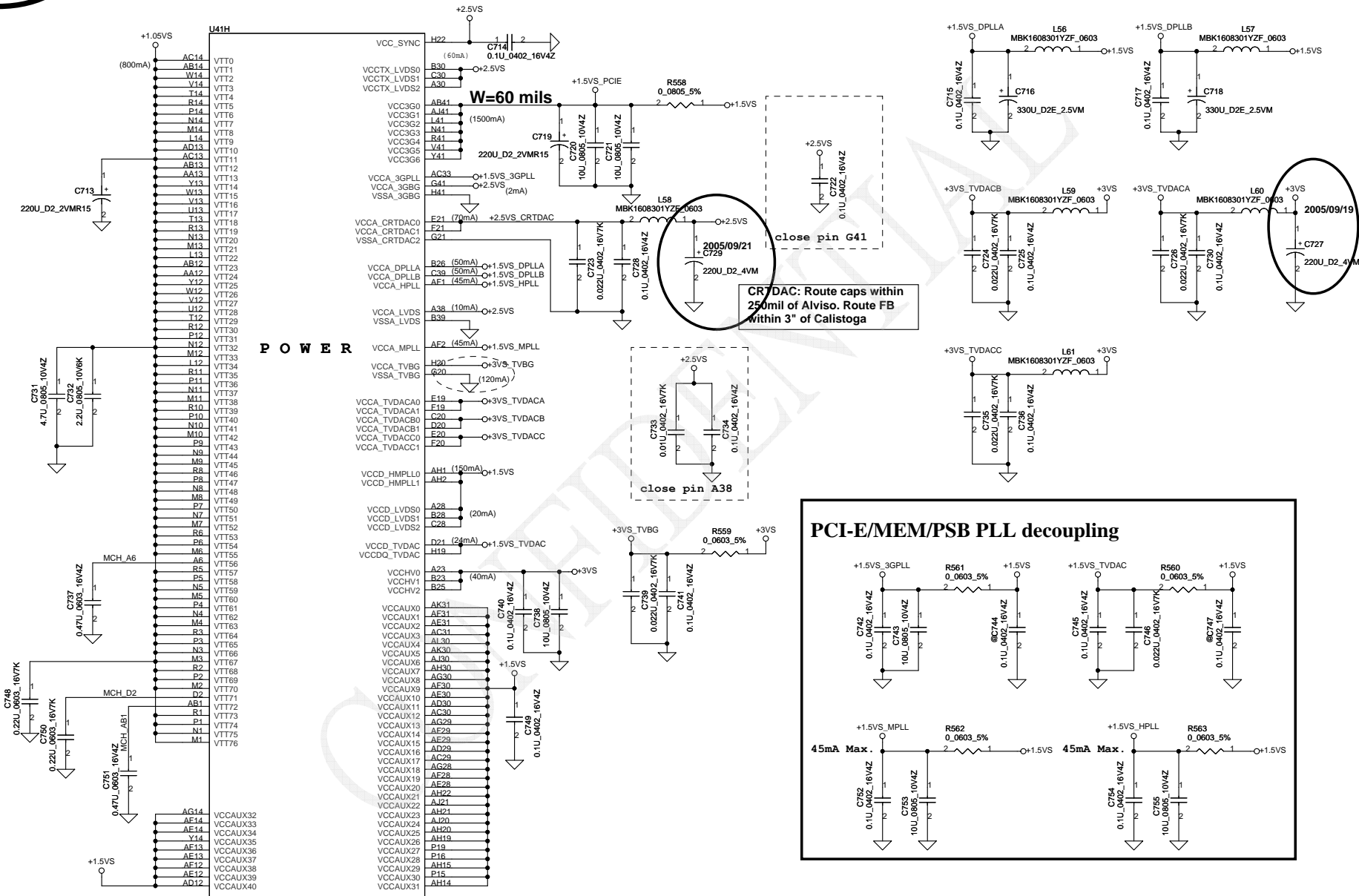
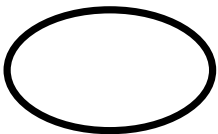
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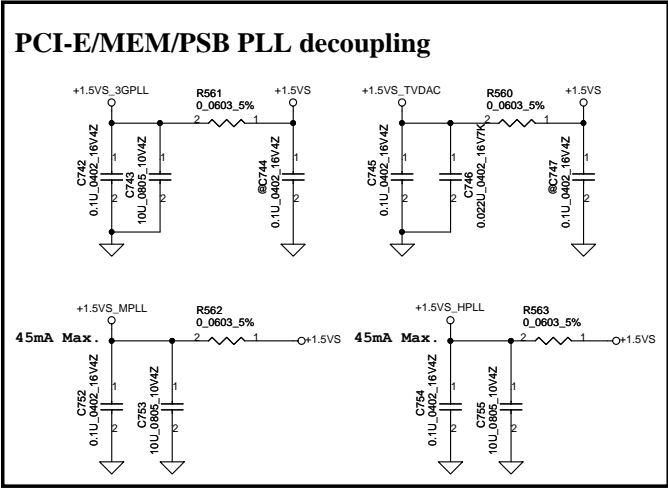


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**P O W E R**



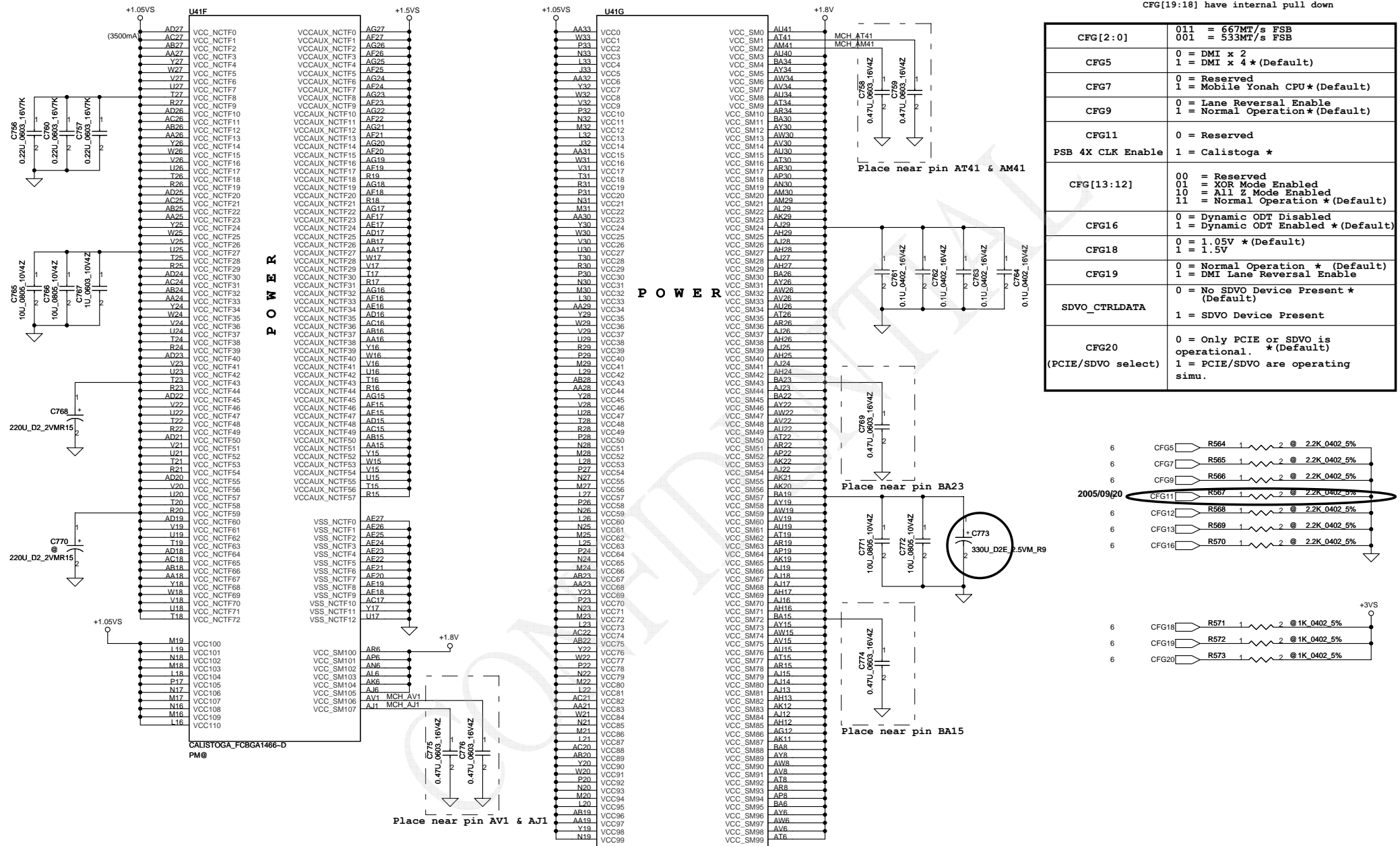
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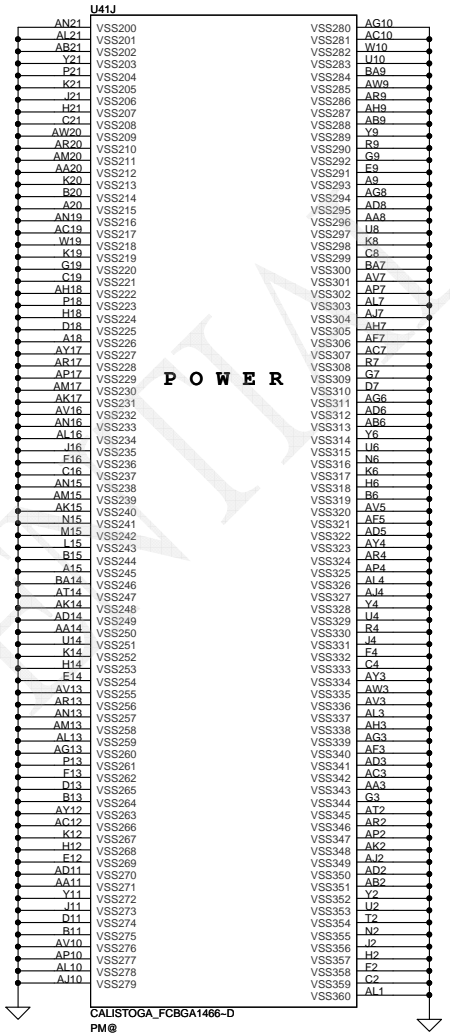
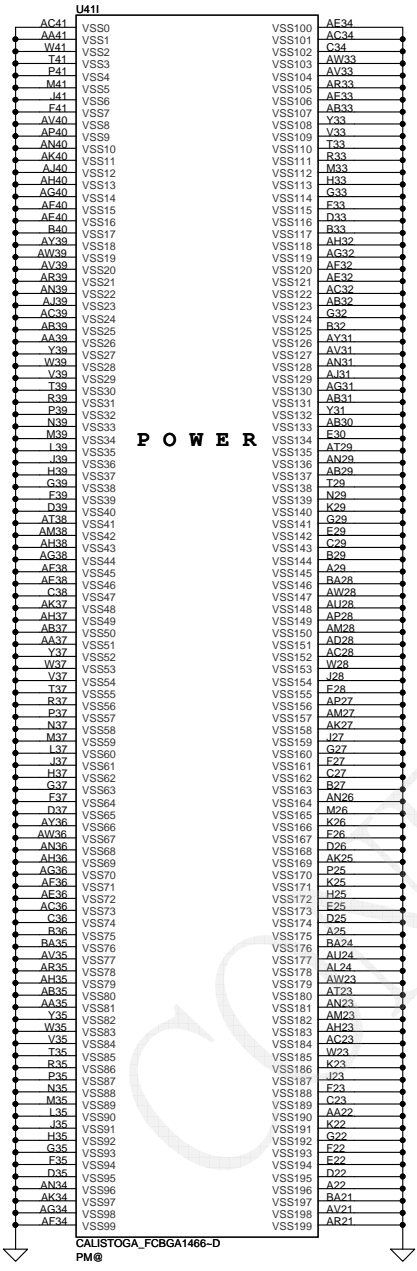
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# Strap Pin Table

CFG[3:17] have internal pull up  
CFG[19:18] have internal pull down

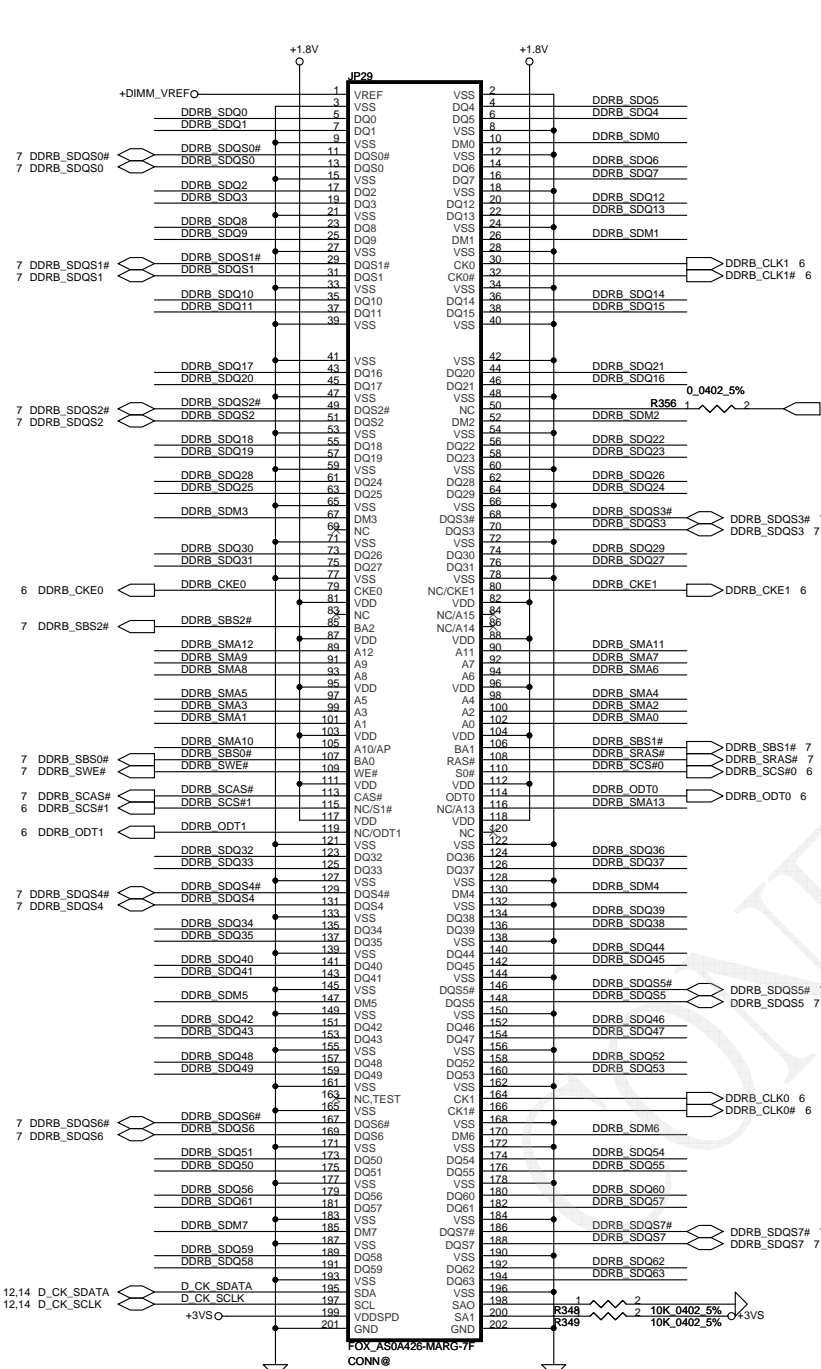
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG18	0 = 1.05V * (Default) 1 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. * (Default) 1 = PCIe/SDVO are operating simu.



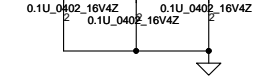
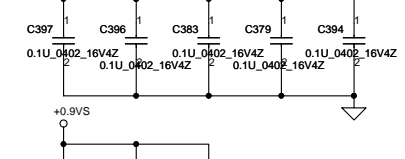
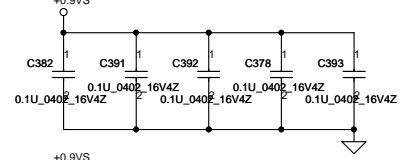
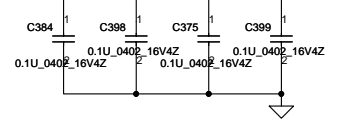
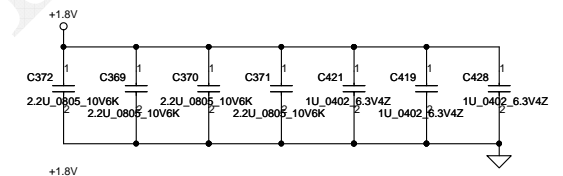
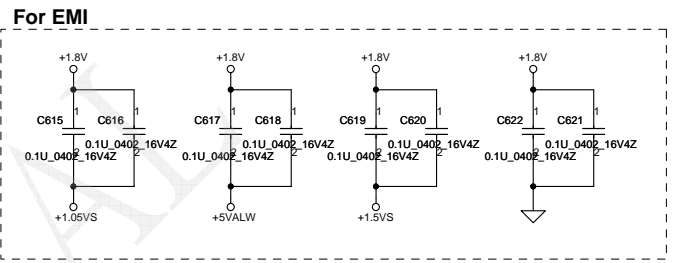
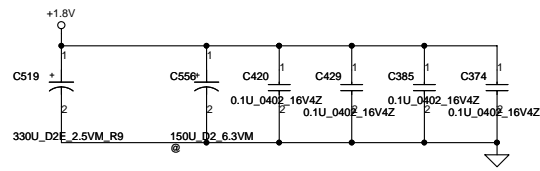
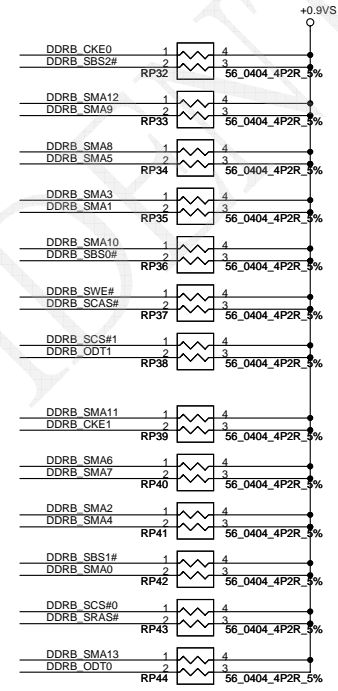
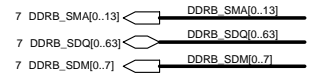
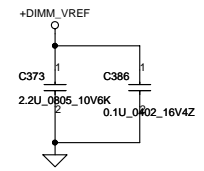


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DIMM1 REV H:9.2mm (BOT)



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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LP325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz_1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

\*\*SEL\_24M/PCICLK2=0=TESTMODE  
\*\*SEL\_PCI6/PCICLK1=0=CLKREQ5#

+3VS  
\*\*SEL\_PCI5=1=PCICLK5  
CLK REF  
R583 10K\_0402\_5%

R586 10K\_0402\_5%  
ITP\_EN/PCICLK\_F0=0=SRC pair

R592 10K\_0402\_5%  
CLK PCI4  
2005/08/31

+3VS  
2005/10/18  
CLK ENABLE# R  
R617 10K\_0402\_5%

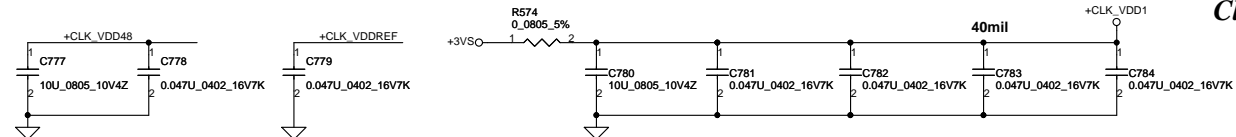
20,24,26,27 ICH\_SMBDAT  
+3VS  
R629 4.7K\_0402\_5%  
Q48  
2N7002\_SOT23  
20,24,26,27 ICH\_SMBCLK  
+3VS  
R638 4.7K\_0402\_5%  
Q49  
2N7002\_SOT23  
2005/08/31

2005/10/18  
CLK ENABLE# R  
Q49  
2N7002\_SOT23

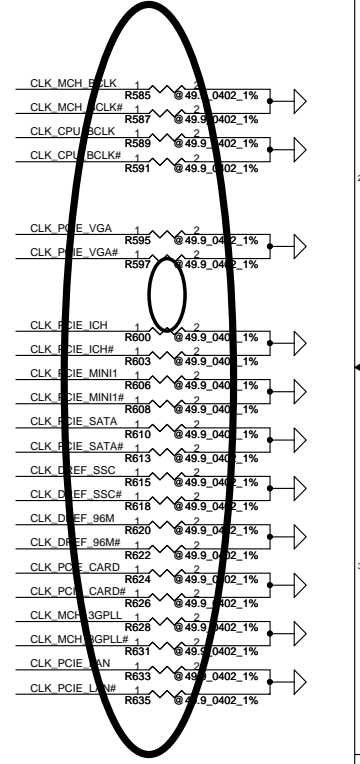
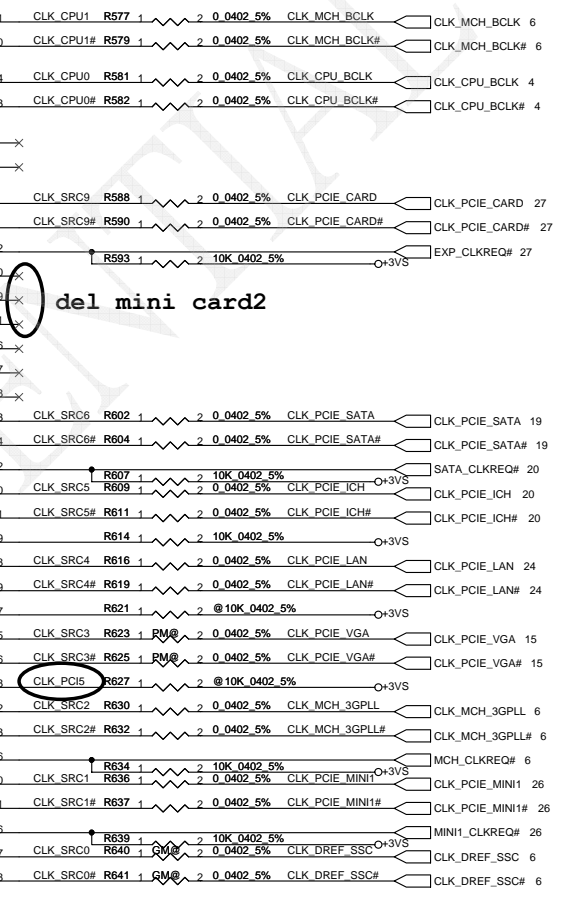
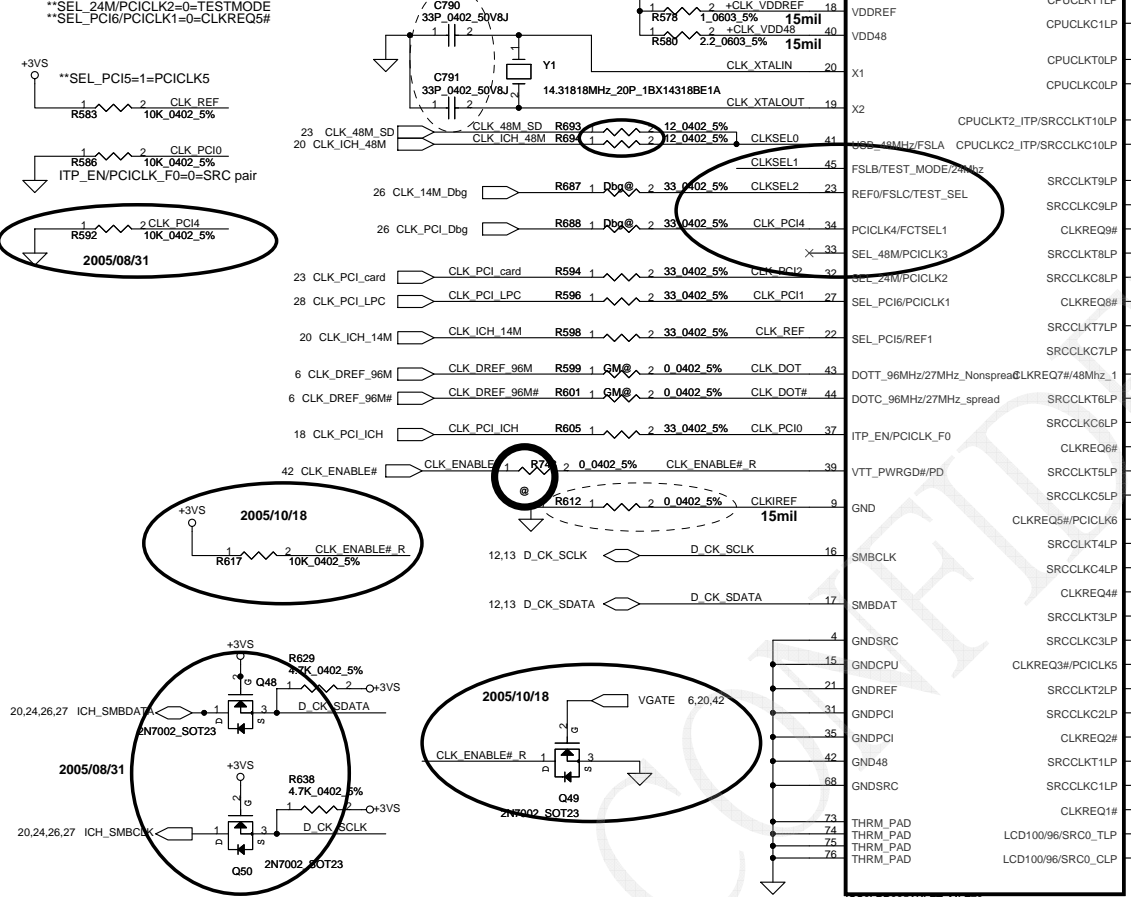
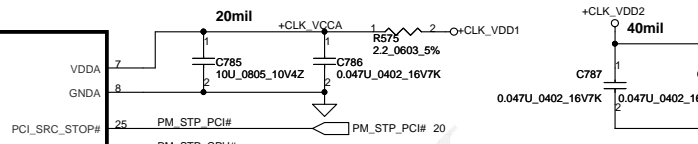
+1.05VS  
R642 @56\_0402\_5%  
R645 8.2K\_0402\_5%  
R646 1K\_0402\_5%  
CLKSEL0 1  
MCH\_CLKSEL0 6  
R655 @1K\_0402\_5%  
R651 0\_0402\_5%  
CPU\_BSEL0 5

+1.05VS  
R643 @1K\_0402\_5%  
R647 1K\_0402\_5%  
CLKSEL1 1  
MCH\_CLKSEL1 6  
R650 @0\_0402\_5%  
R652 0\_0402\_5%  
CPU\_BSEL1 5

+1.05VS  
R644 @1K\_0402\_5%  
R648 8.2K\_0402\_5%  
R649 1K\_0402\_5%  
CLKSEL2 1  
MCH\_CLKSEL2 6  
R653 @0\_0402\_5%  
R654 0\_0402\_5%  
CPU\_BSEL2 5

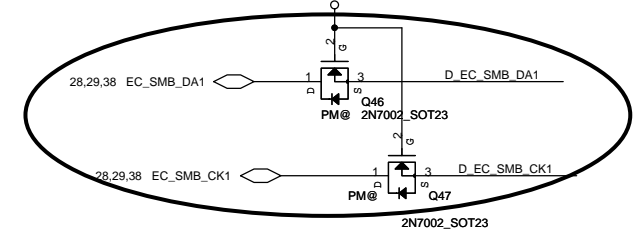
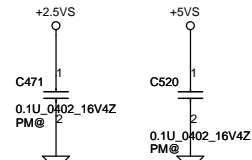
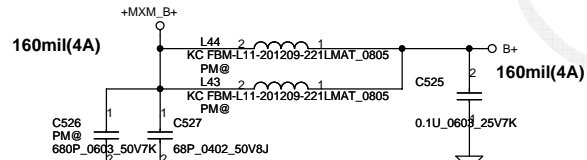
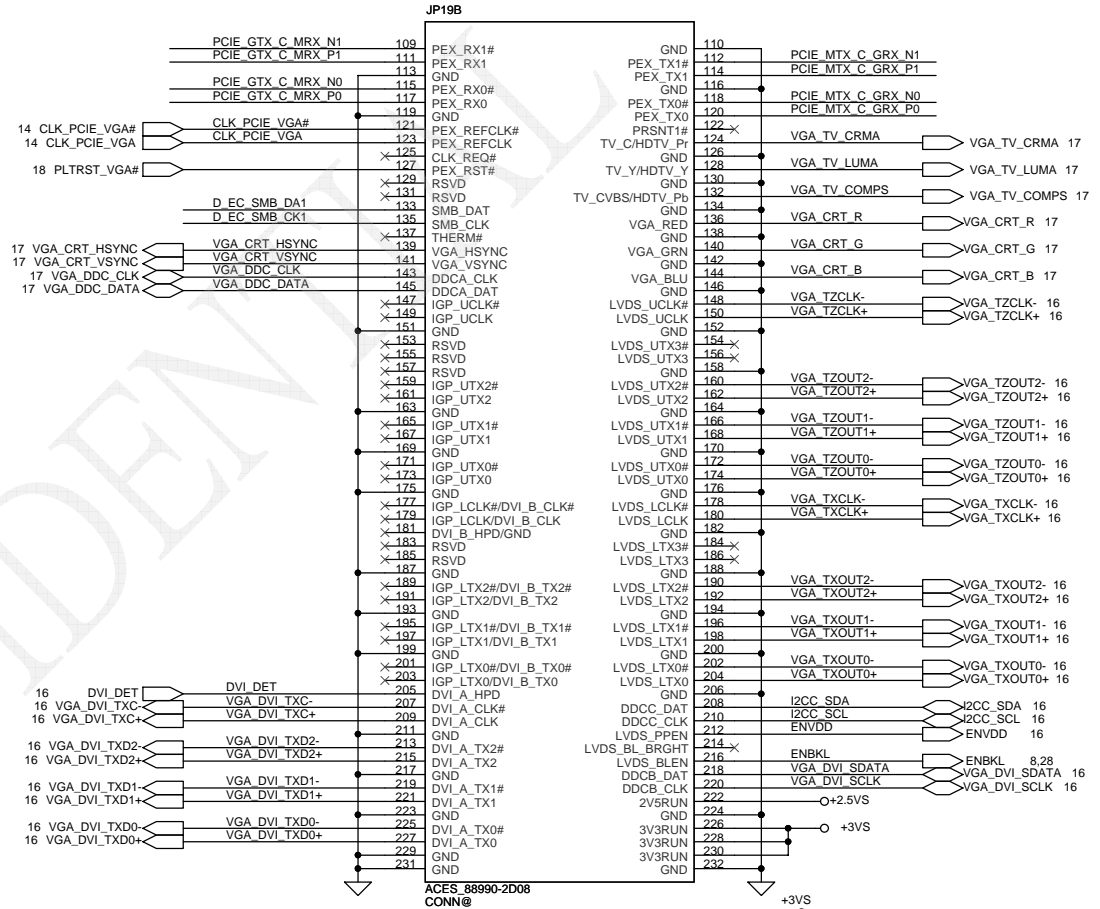
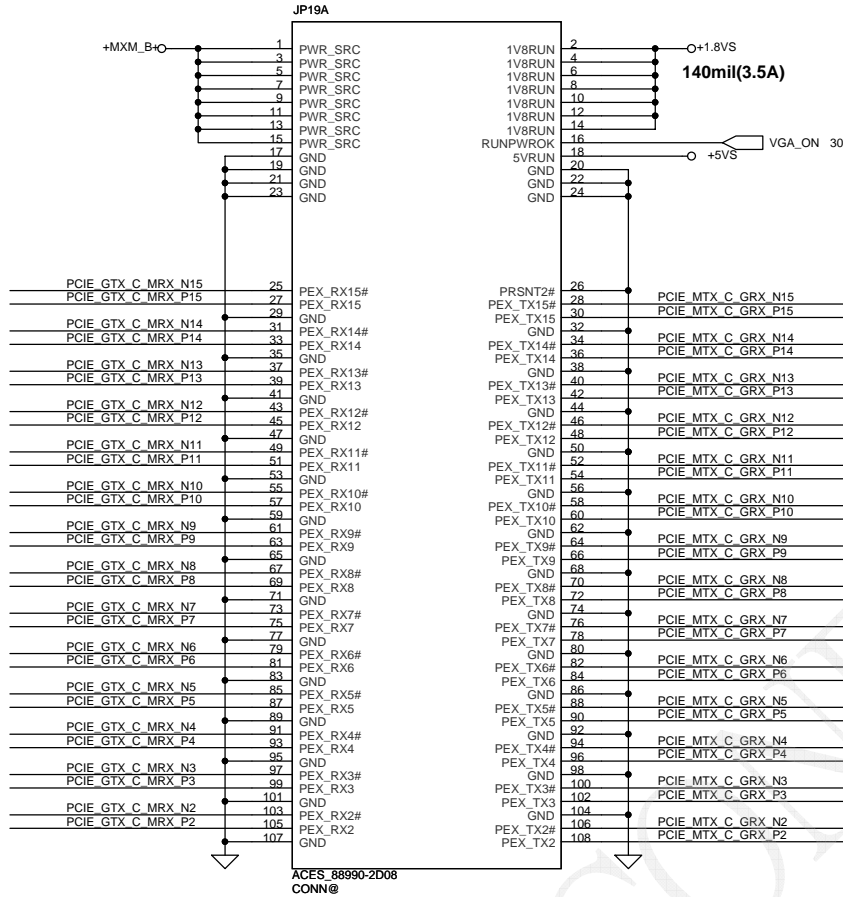
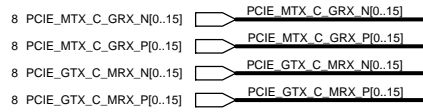


**Clock Generator**



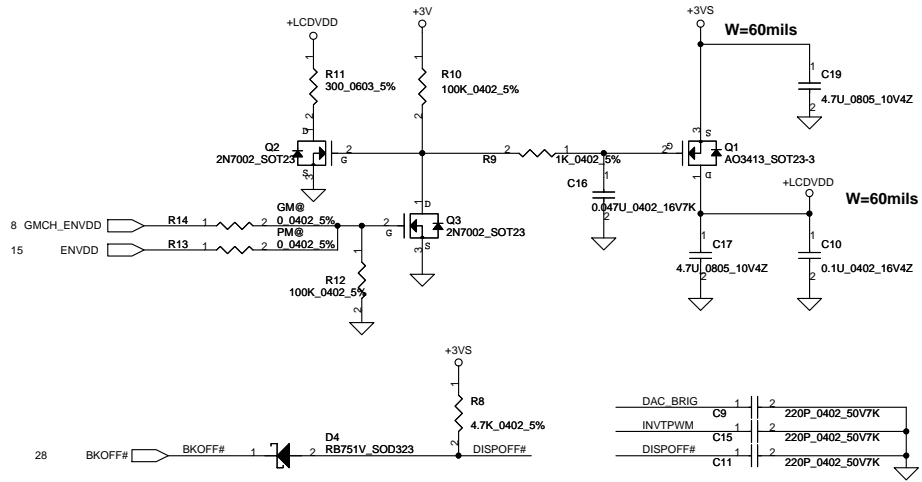
del mini card2

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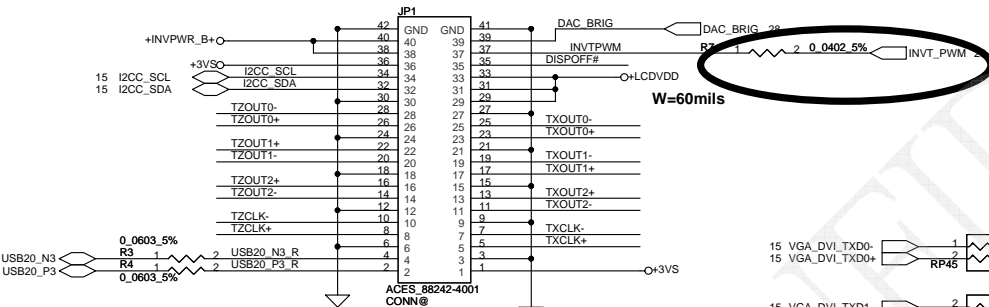


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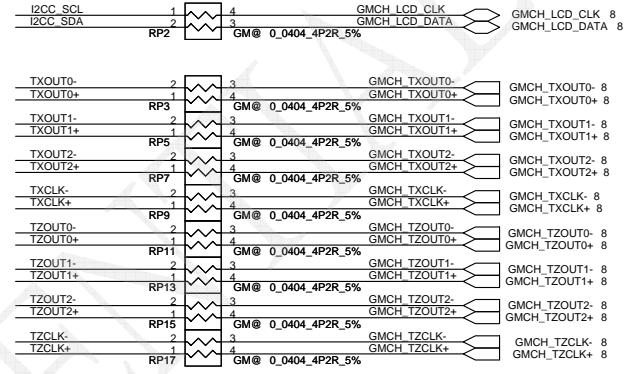
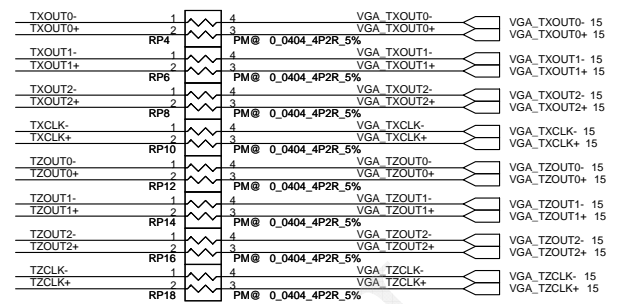
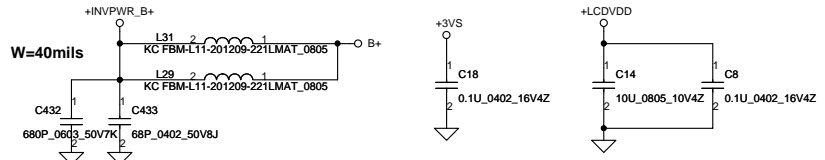
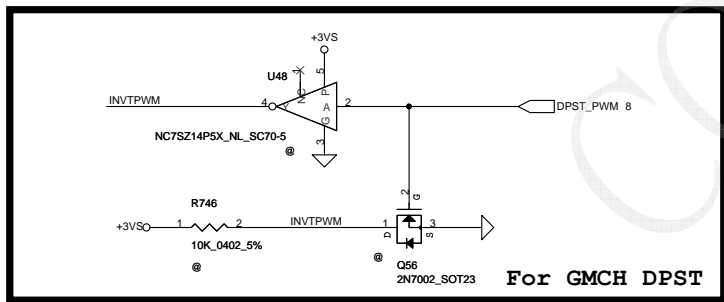
# LCD POWER CIRCUIT



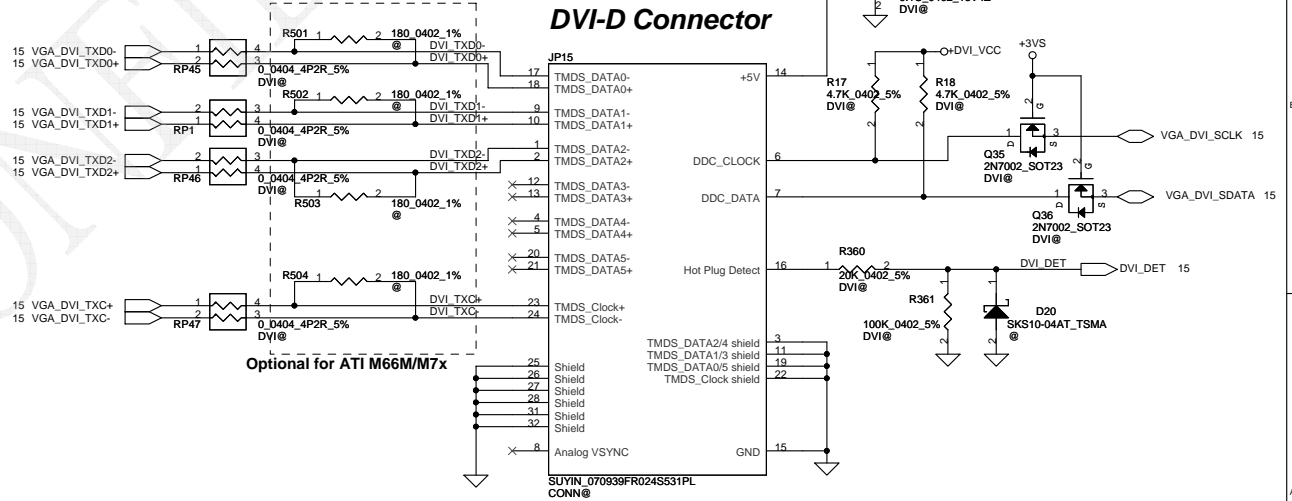
# LCD/PANEL BD. Conn.



# Fro CMOS Camera



# DVI-D Connector

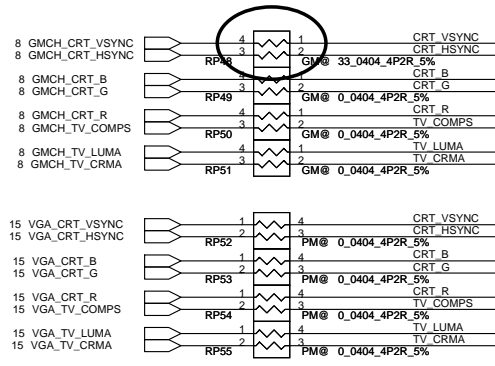
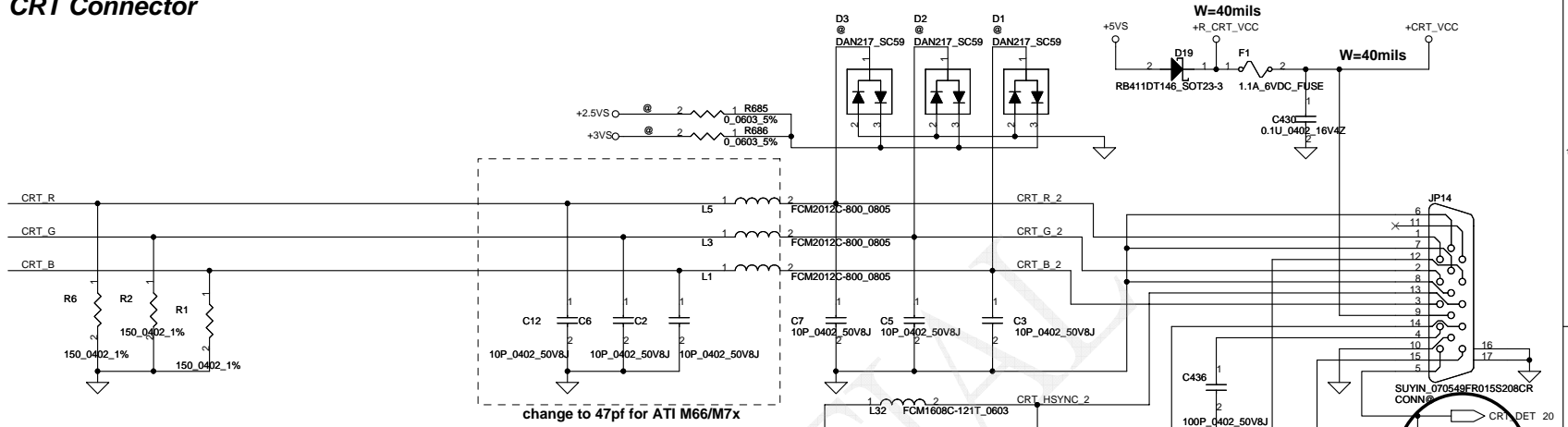


Optional for ATI M66M/M7x

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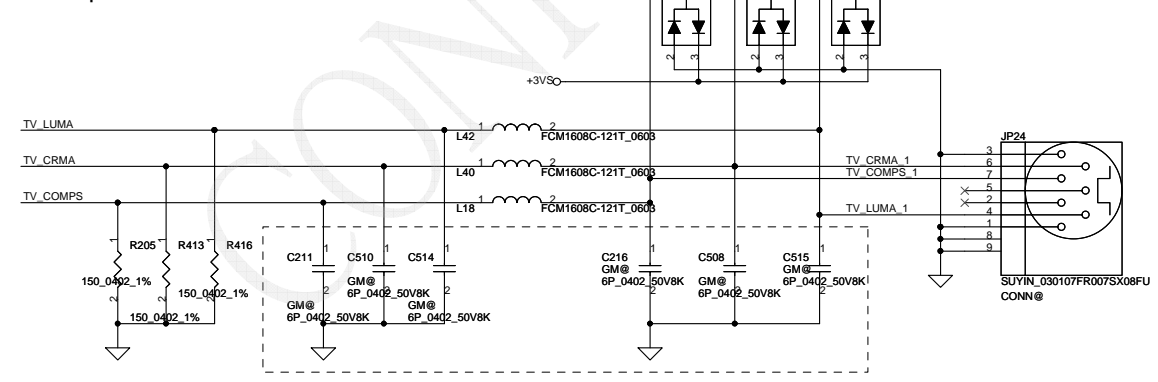


# CRT Connector

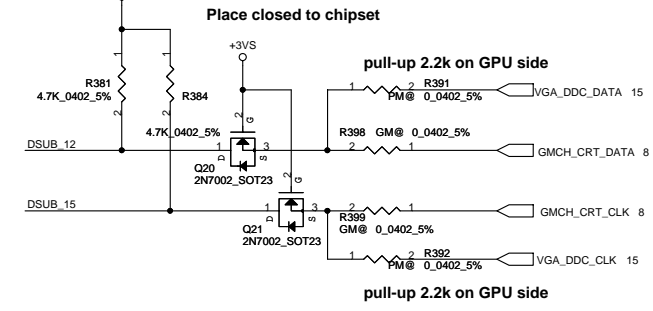


Place closed to chipset

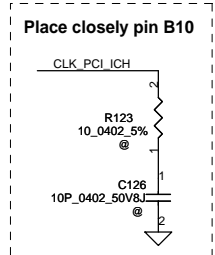
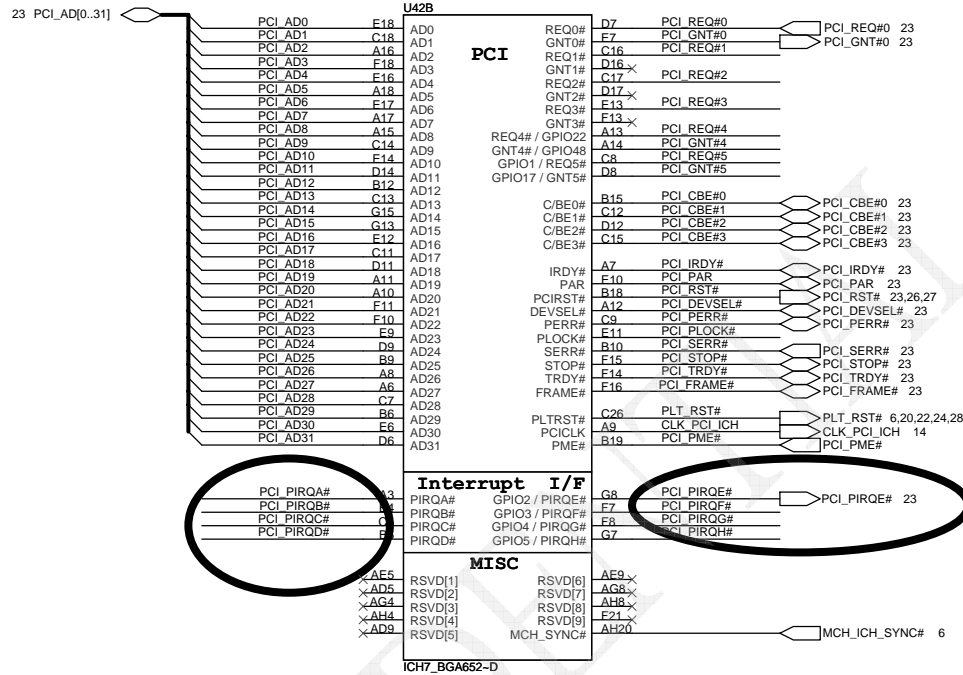
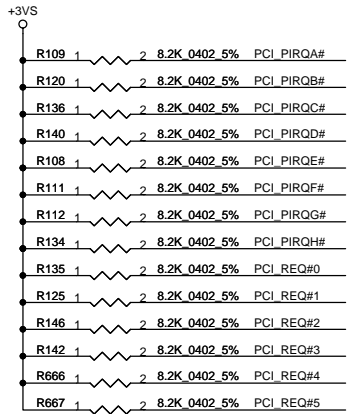
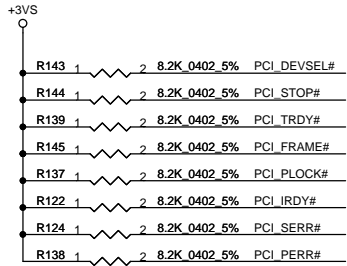
## TV-OUT Conn.



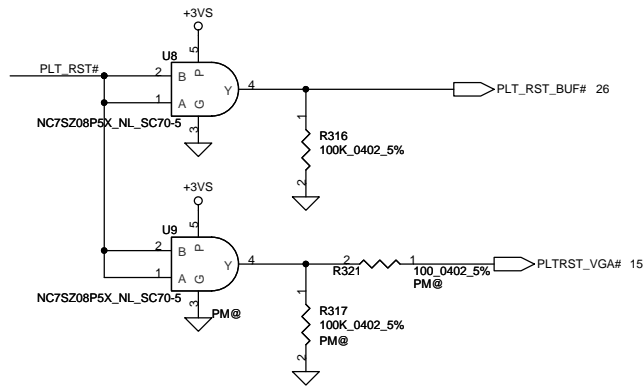
change to 47pf for ATI M66/M7x  
P/N: SE071470J80 ( S CER CAP 47P 50V J NPO 0402 )

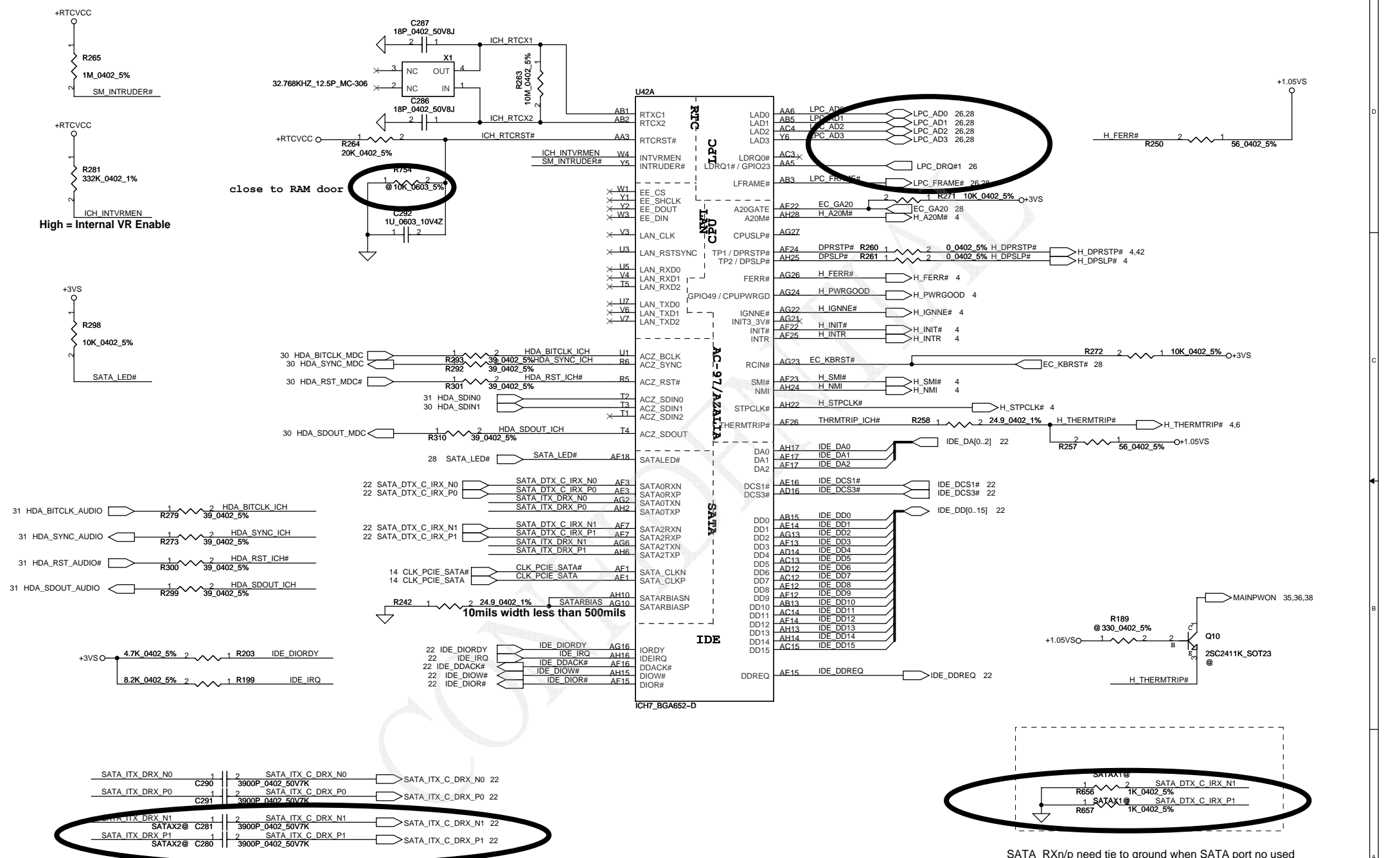


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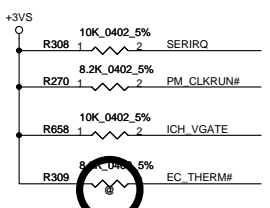
Boot BIOS Strap		
PCI_GNT#5	PCI_GNT#4	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



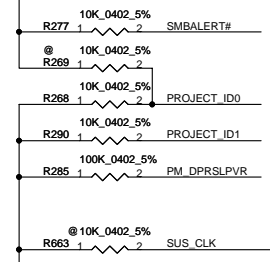
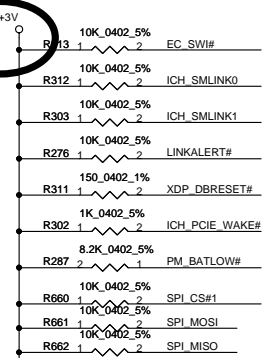


SATA\_RXn/p need tie to ground when SATA port not used

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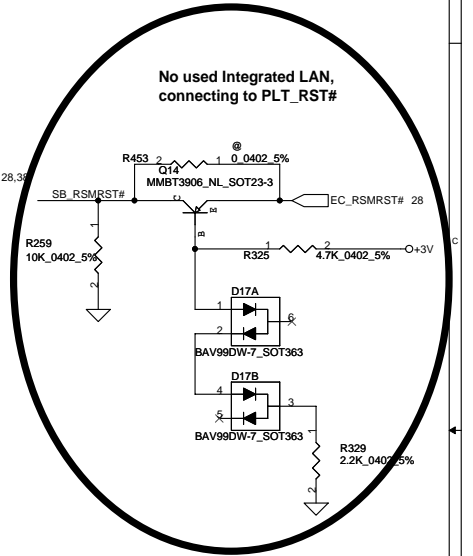
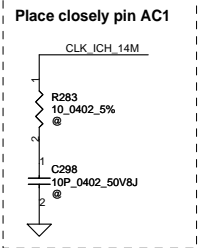
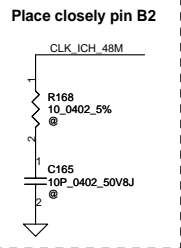
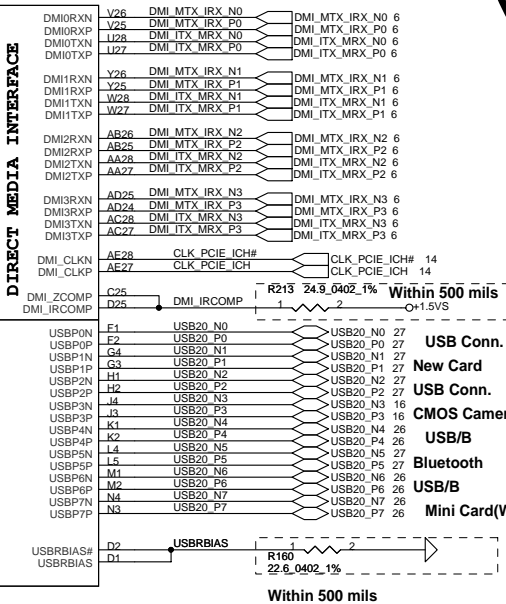
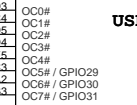
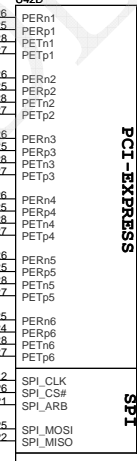
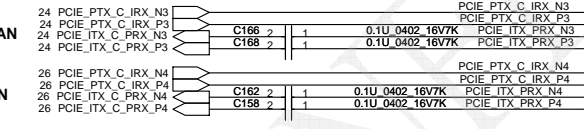
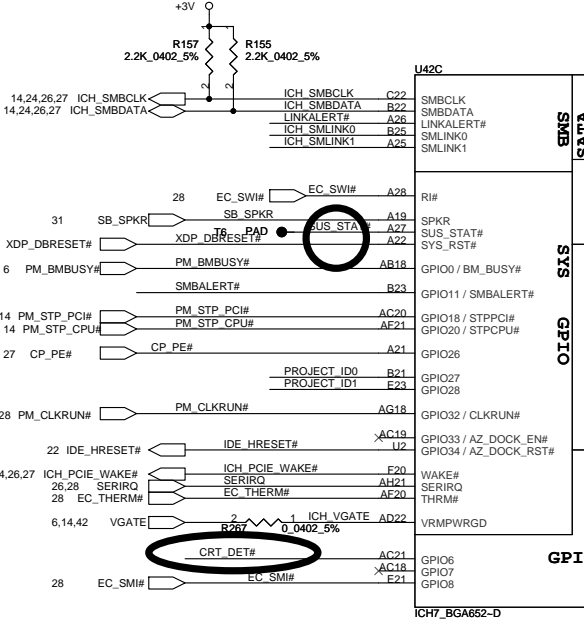
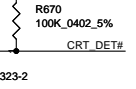
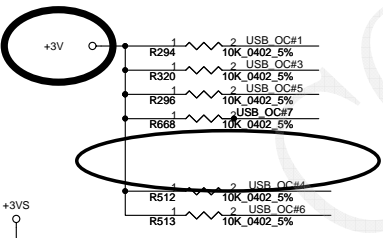
High: CRT Plugged



For Express Card

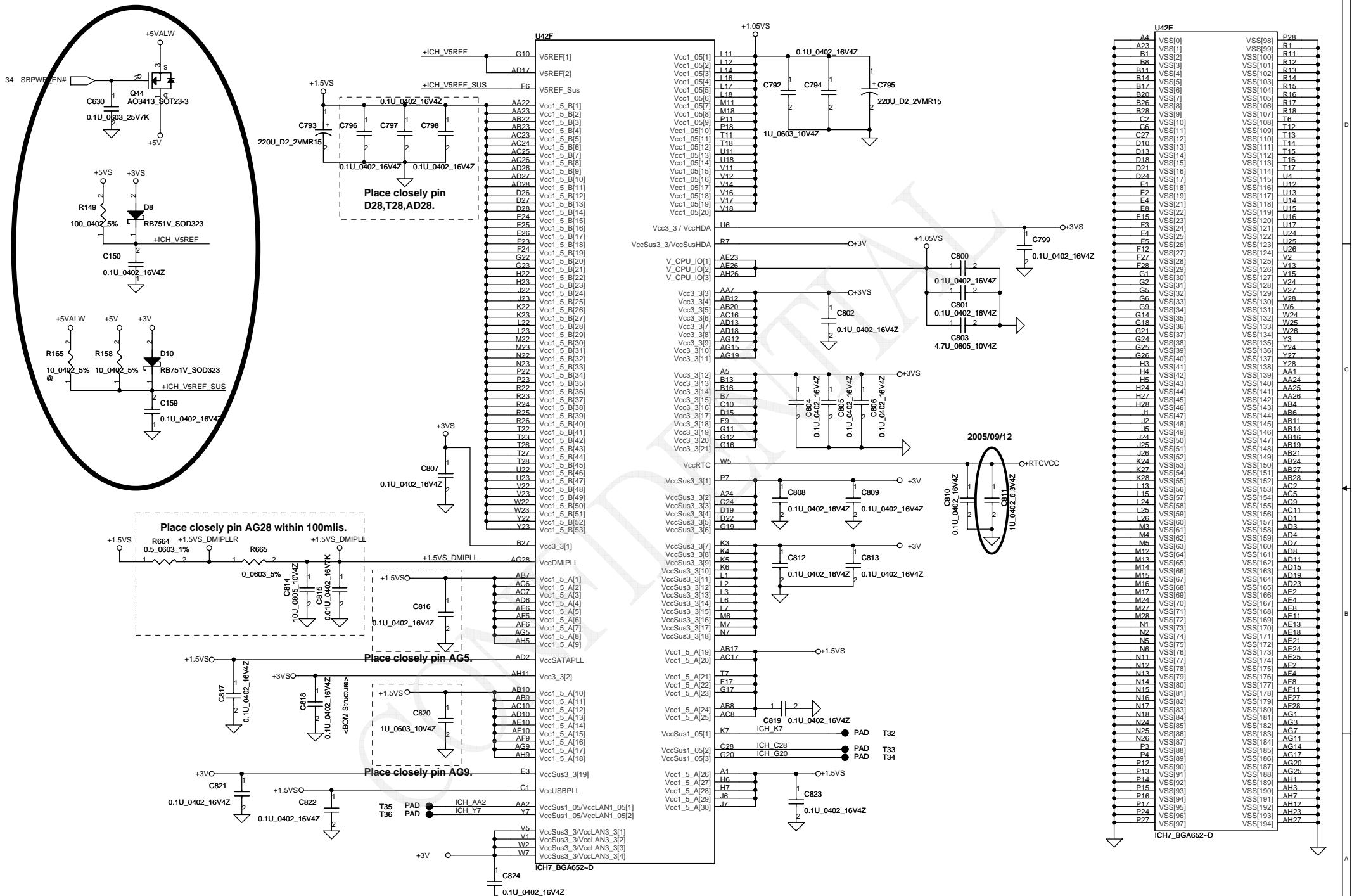
For PCIE LAN

For Wireless LAN

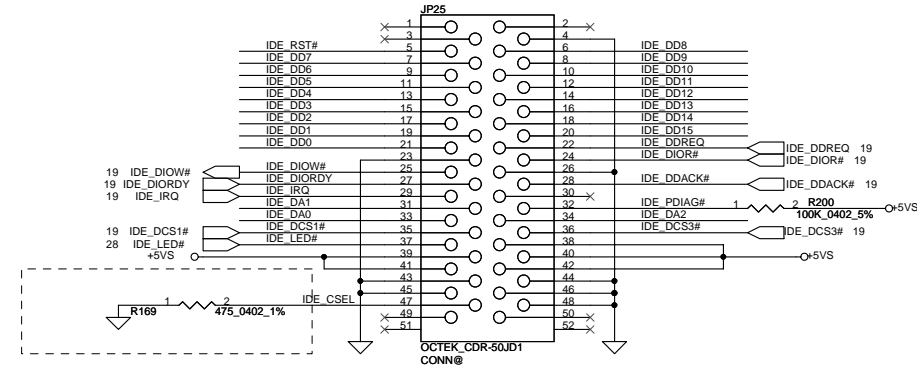
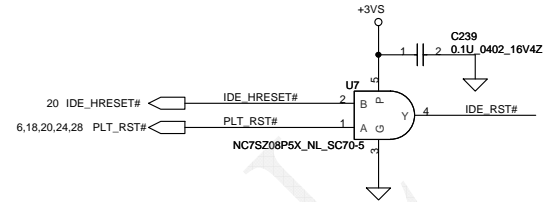
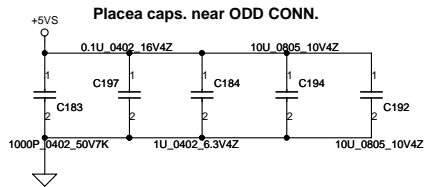


No used integrated LAN, connecting to PLT\_RST#

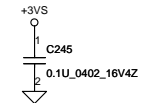
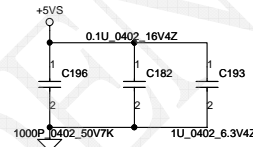
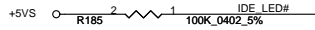
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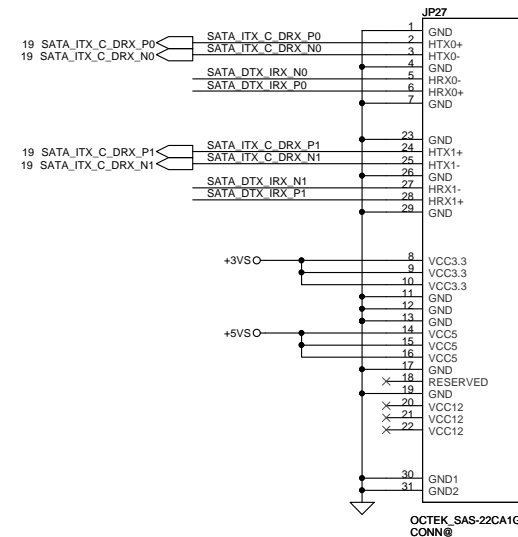
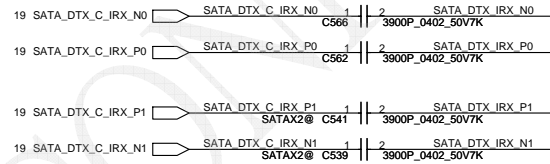
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**IDE\_CSEL**  
Grounding for Master (When use SATA HDD)  
Open or High for Slaver (Normal)



**SATA HDD Conn.(SAS Connector)**



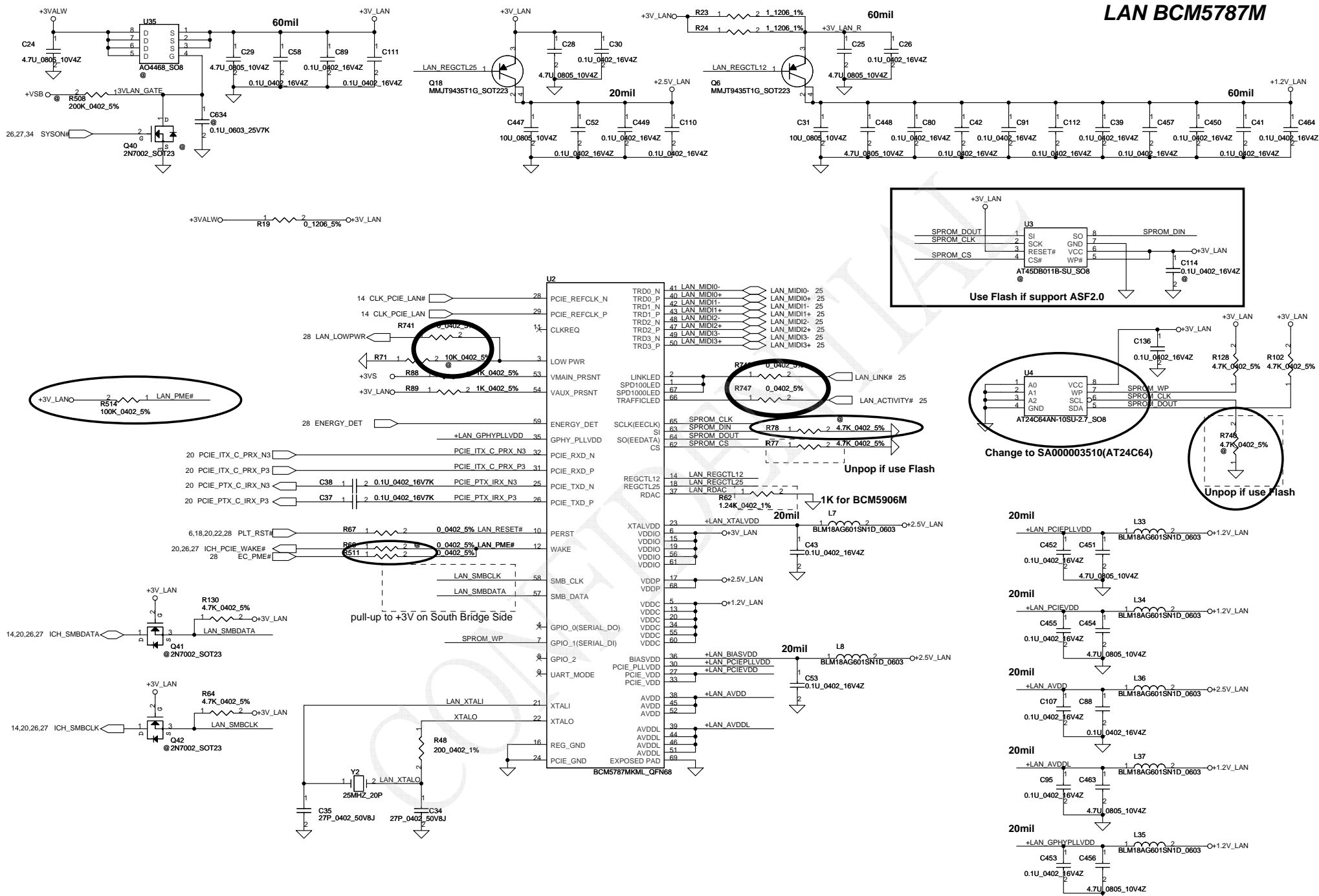
First HDD for 15.4"

2nd HDD for 17"

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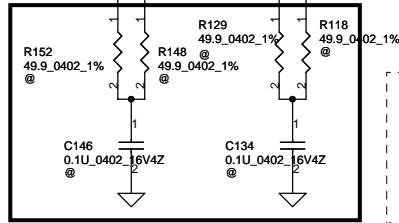
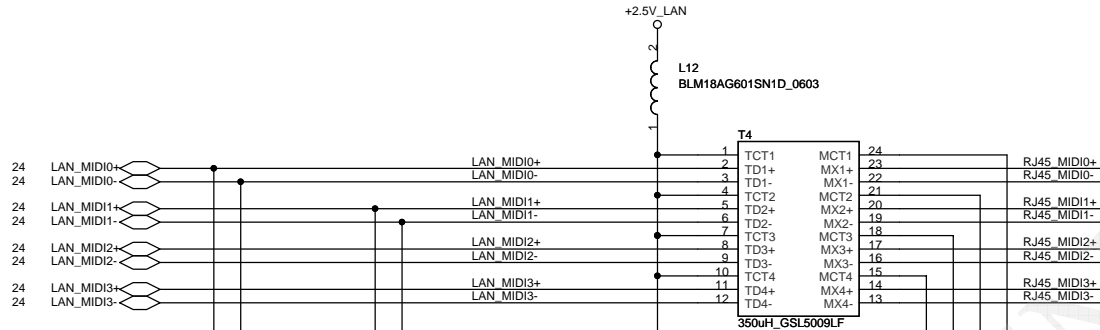
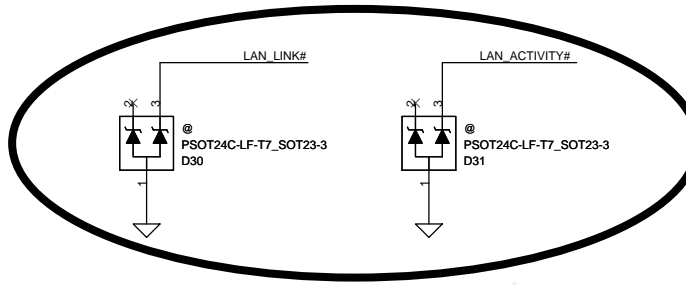
# LAN BCM5787M



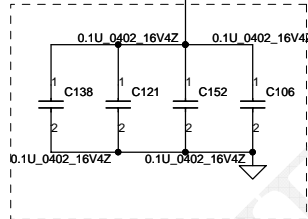
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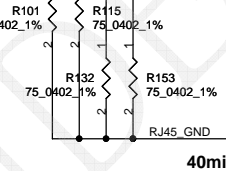
# LAN BCM5787M



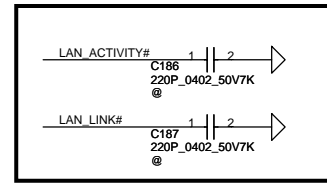
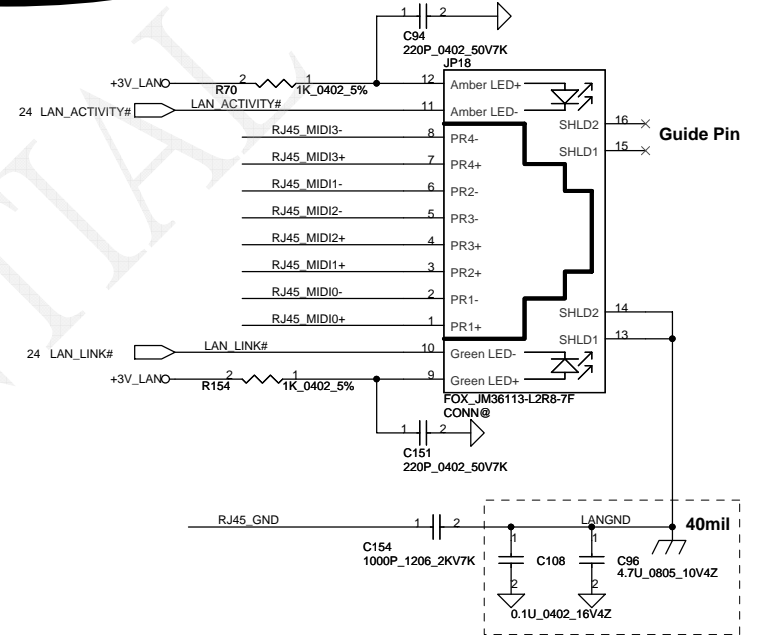
Pop for BCM5906



Place close to TCT pin



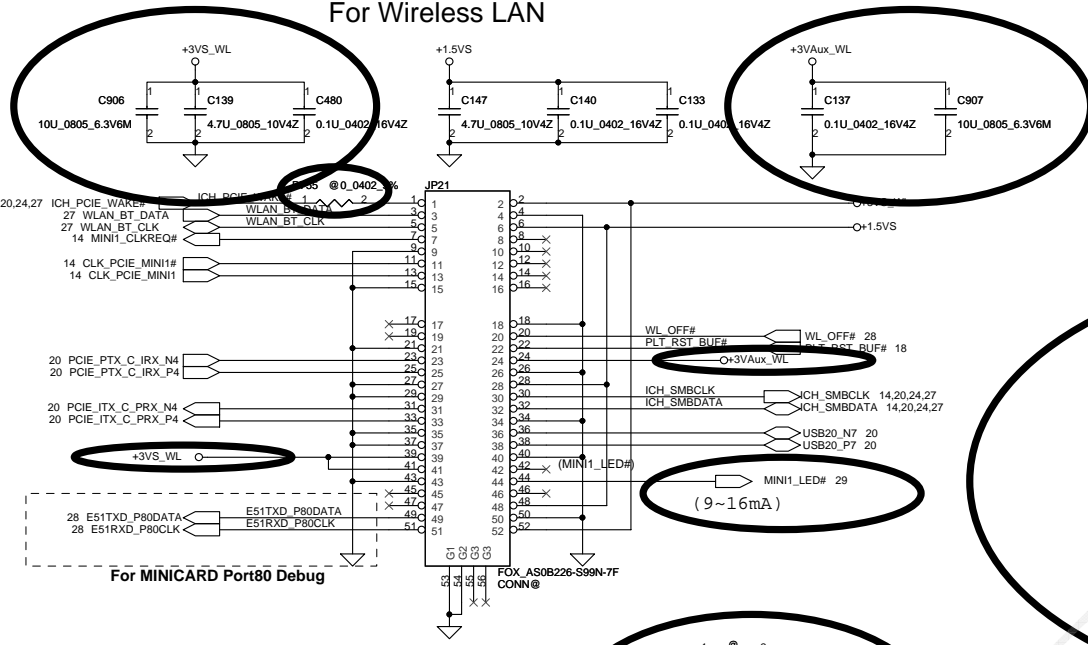
40mil



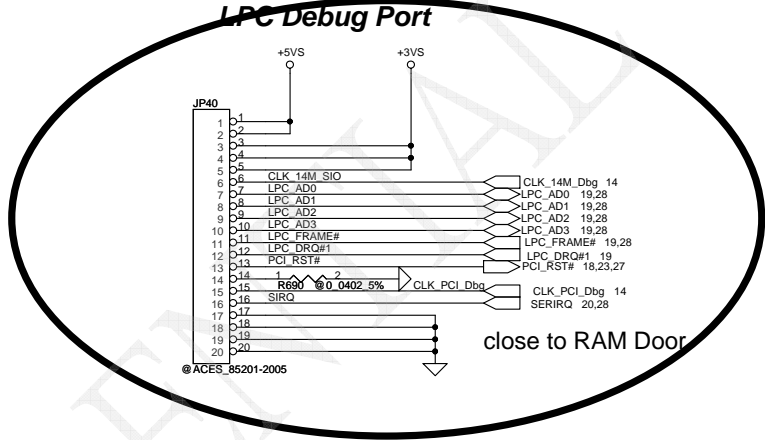
For EMI

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### For Wireless LAN

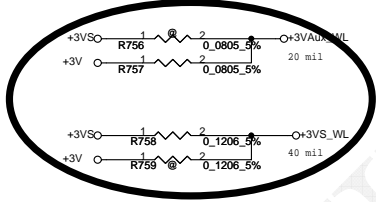


### LPC Debug Port

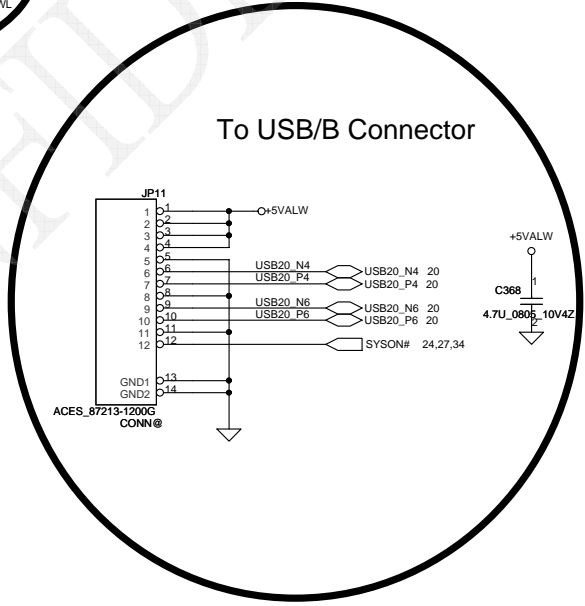


### For MINICARD Port80 Debug

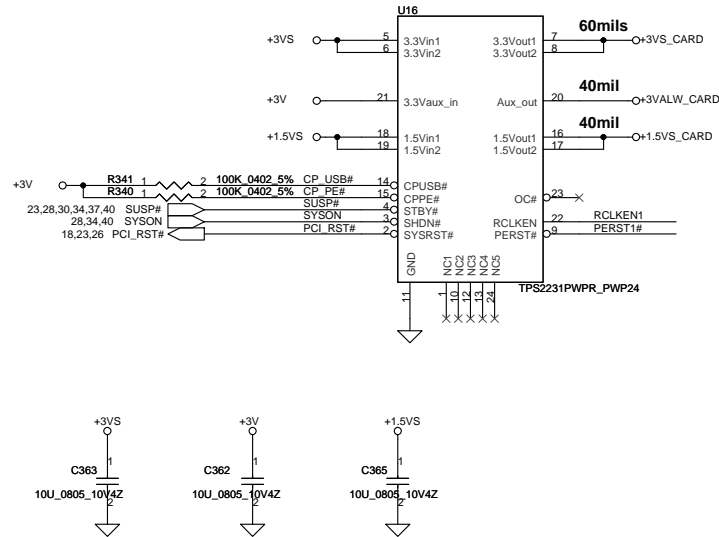
Power	Mini Card Power Rating		
	Primary Power (mA)	Auxiliary Power (mA)	
	Peak	Normal	Normal
<b>+3V_S</b>	<b>1000</b>	<b>750</b>	<b>Normal</b>
<b>+3V</b>	<b>330</b>	<b>250</b>	<b>250 (wake enable)</b>
<b>+1.5V_S</b>	<b>500</b>	<b>375</b>	<b>5 (Not wake enable)</b>



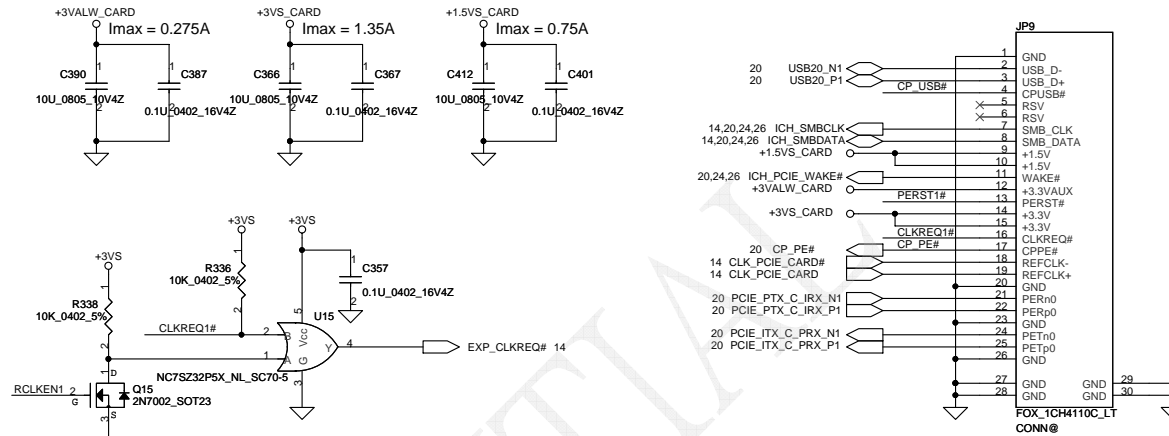
### To USB/B Connector



### New Card Power Switch

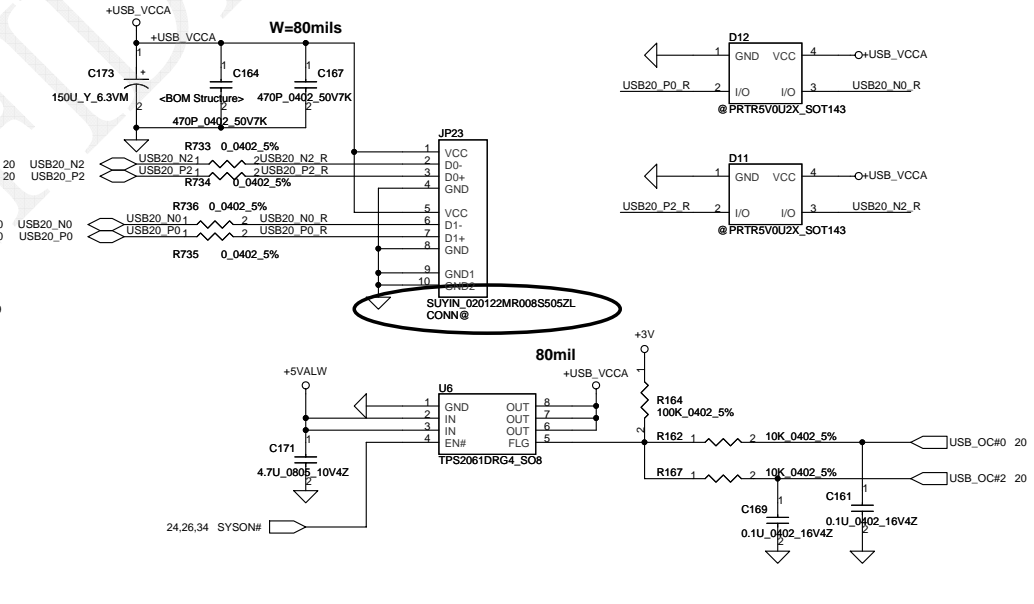
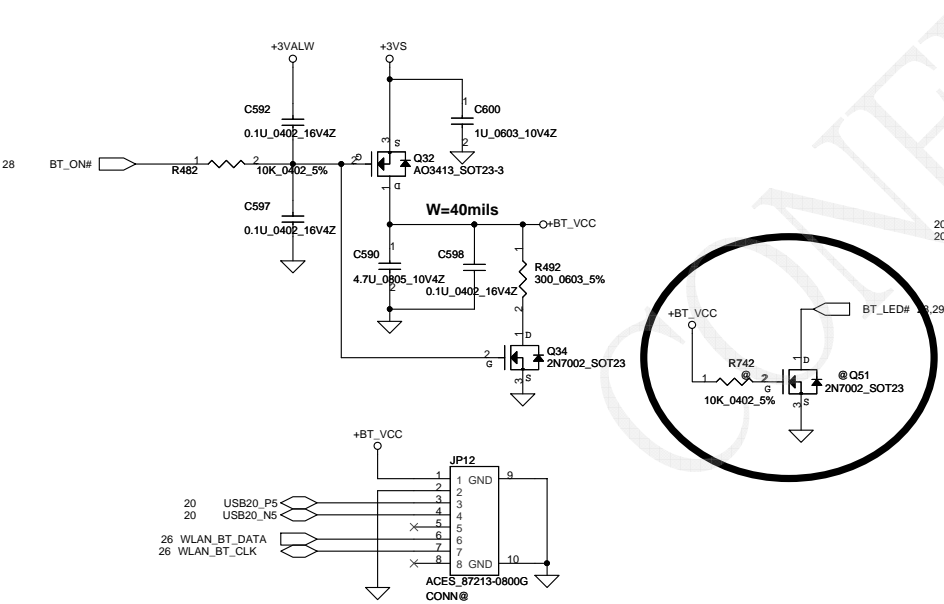


### New Card Socket (Left/TOP)

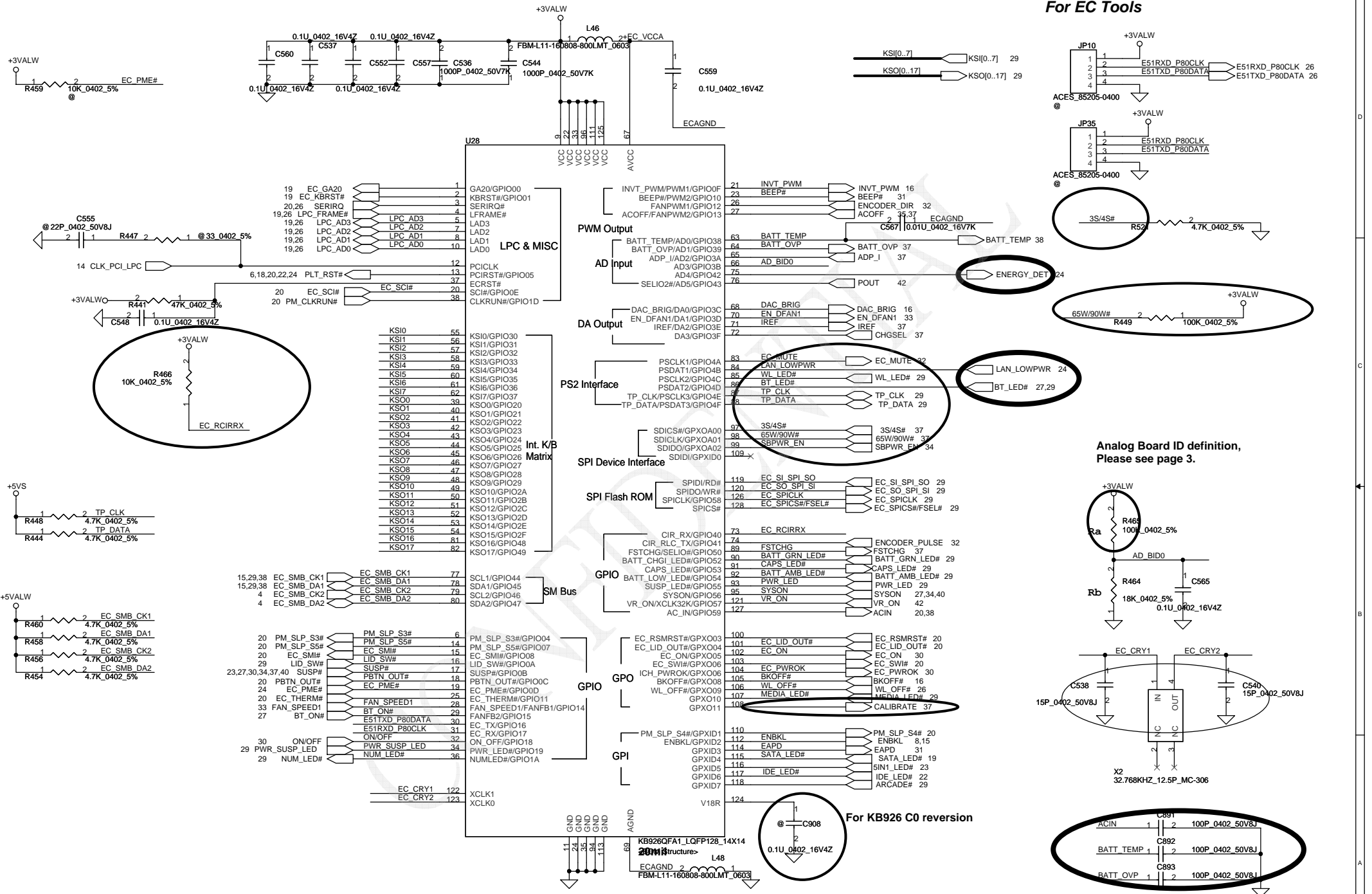


### USB CONN. (Stack-up Type)

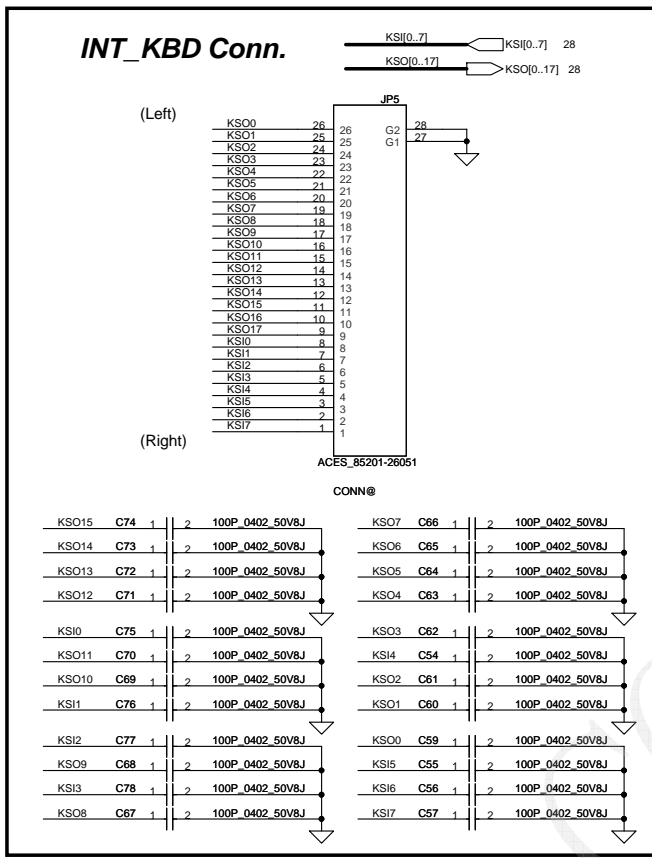
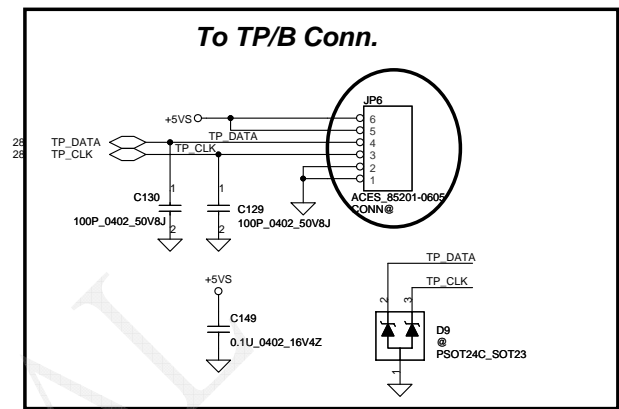
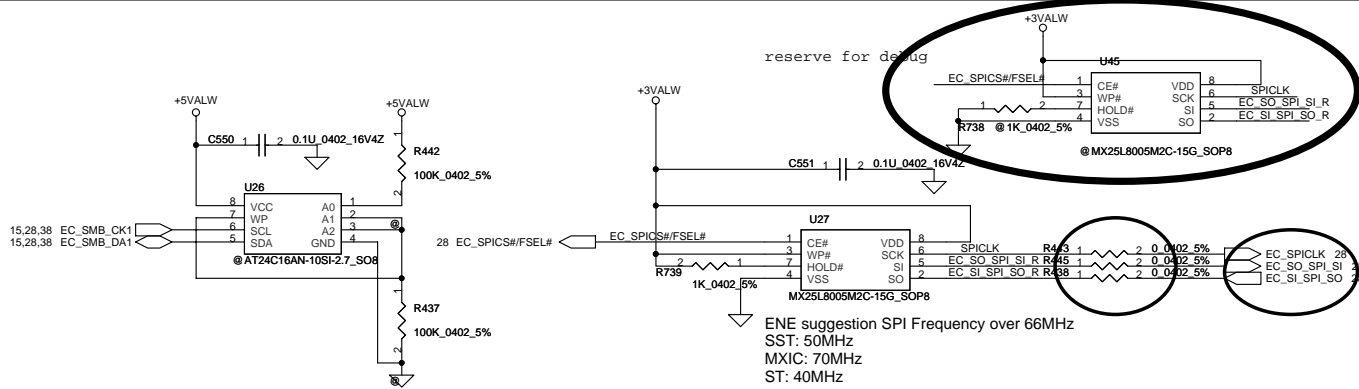
### Bluetooth Conn.



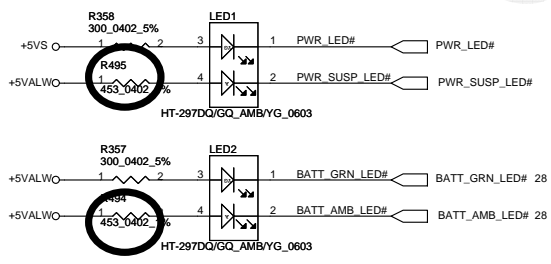
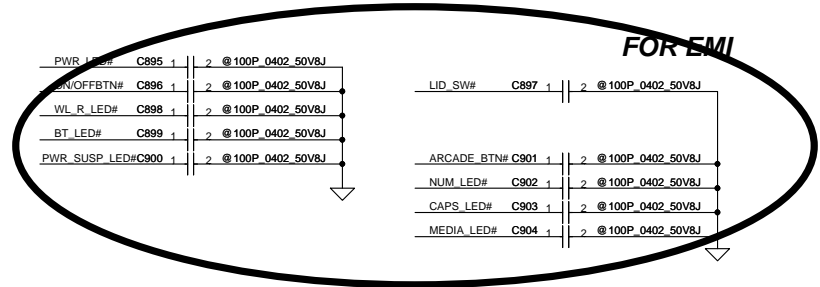
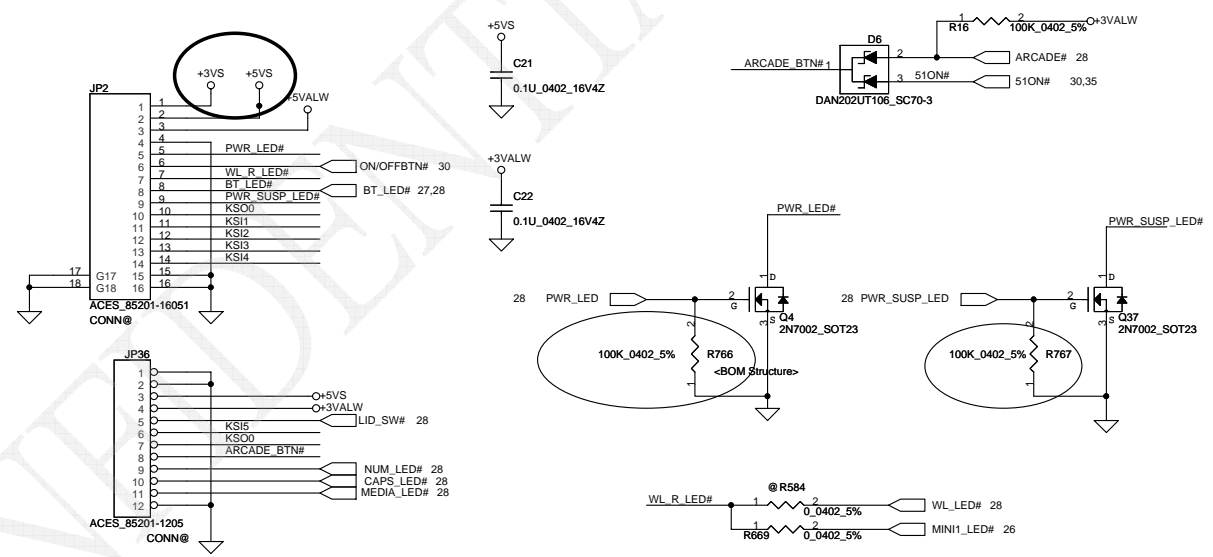
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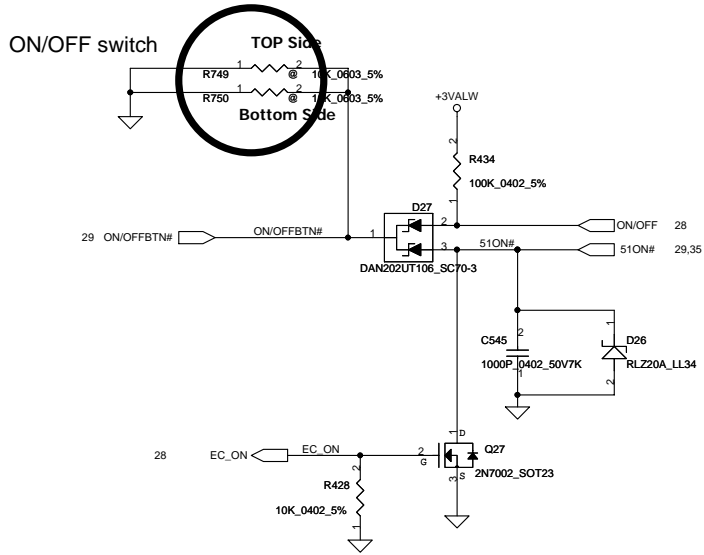
**To BTNB Conn.**



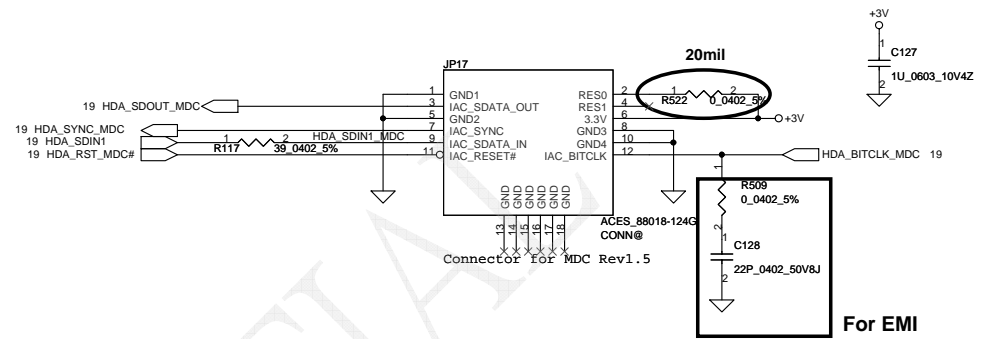
KSO0	
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

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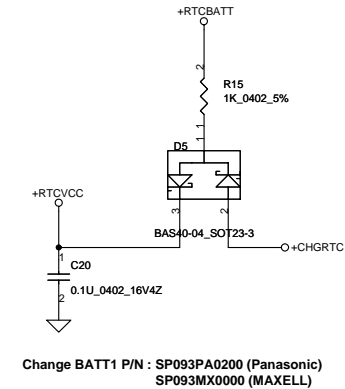
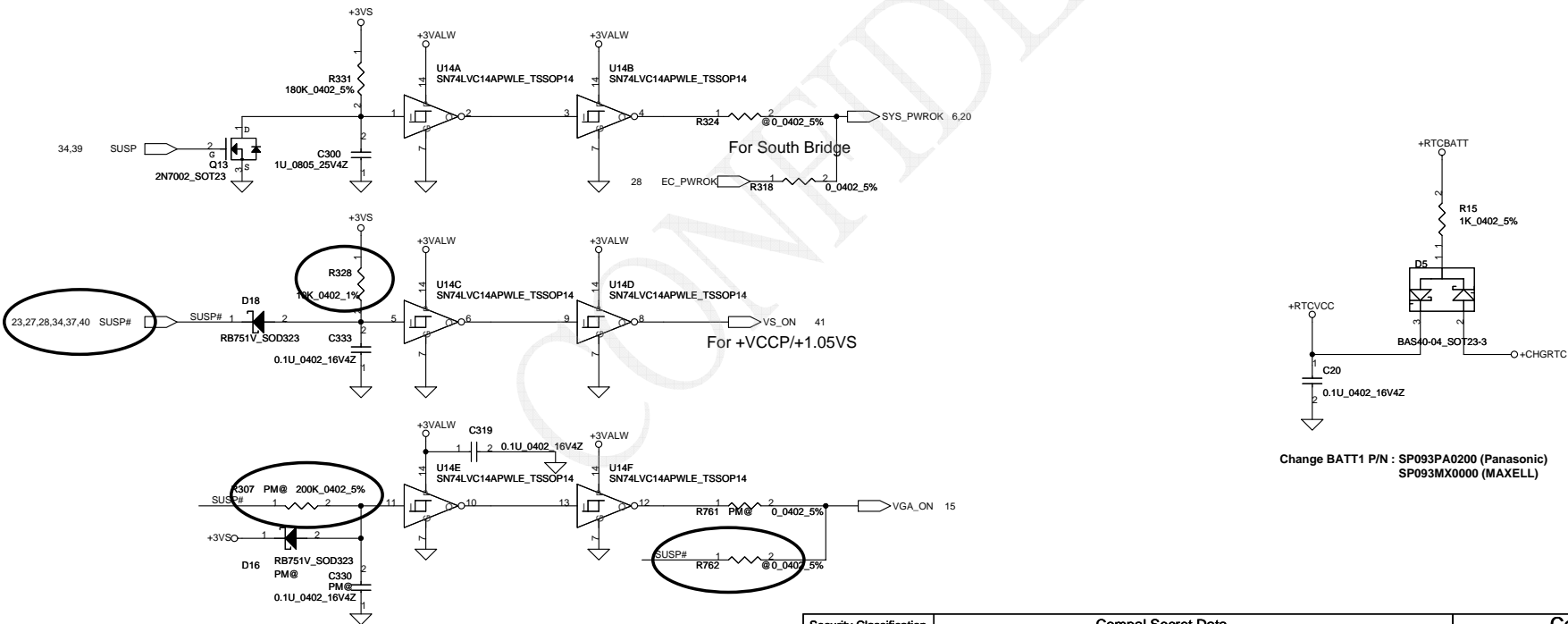
### Power Button



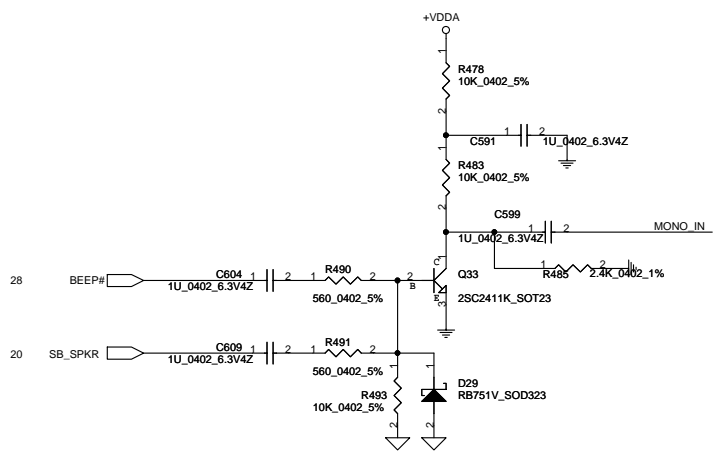
### HDA MDC Conn.



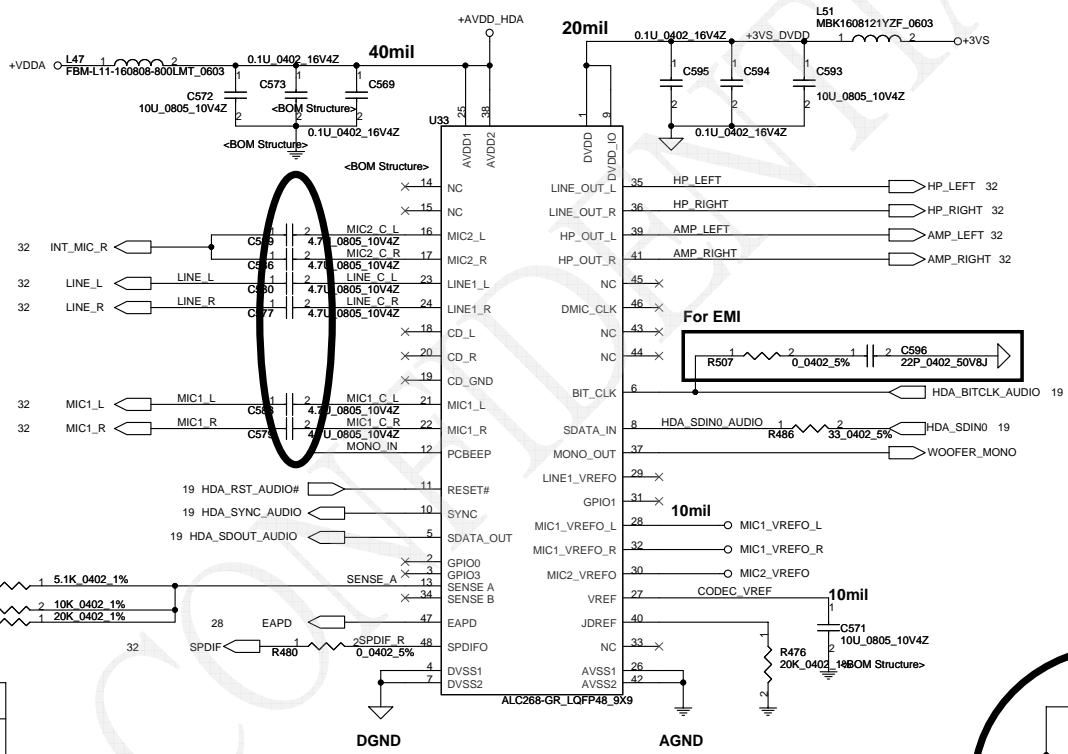
### Power ON Circuit



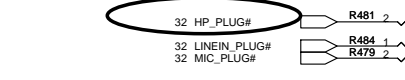
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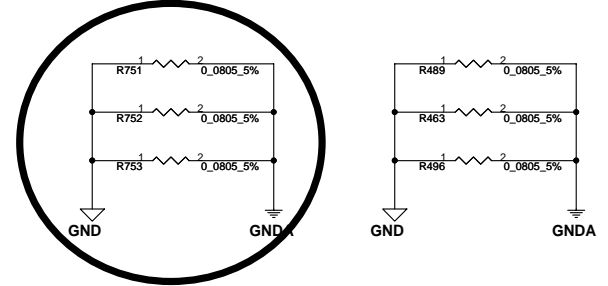
### HD Audio Codec



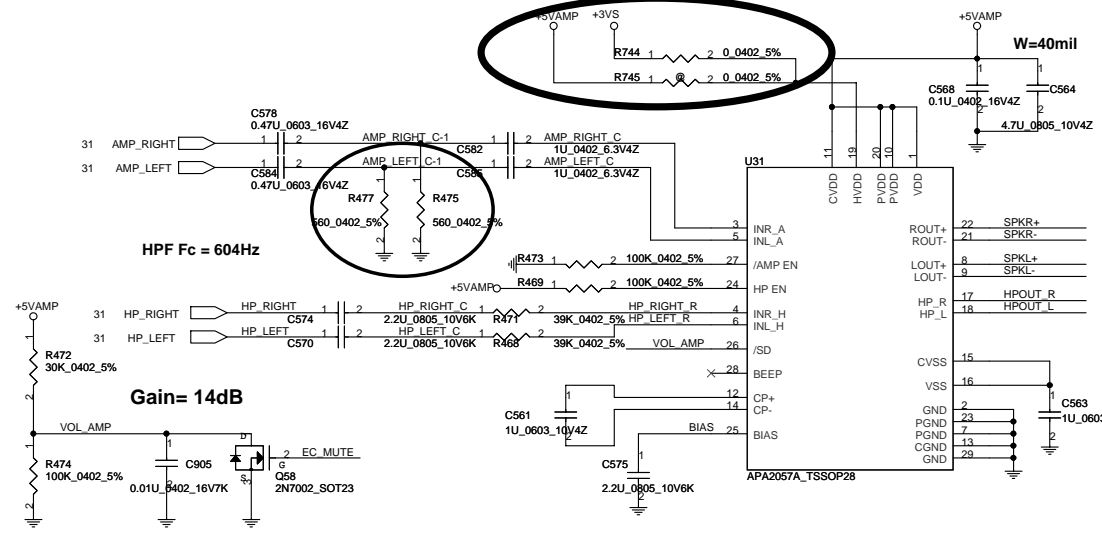
28.7K for Module Design (VDDA = 4.702)  
(output = 250 mA)



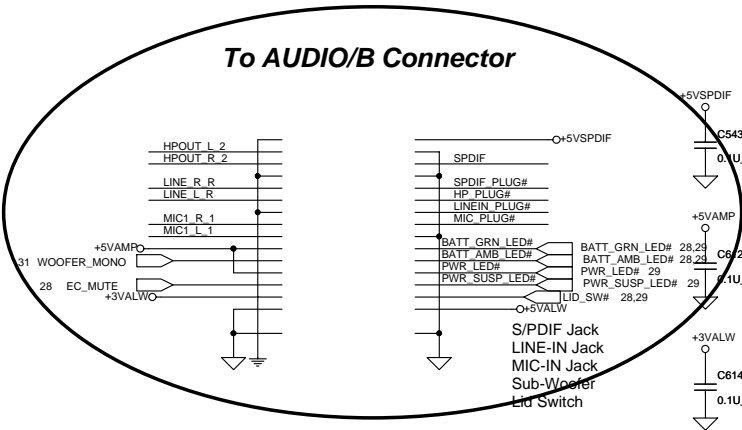
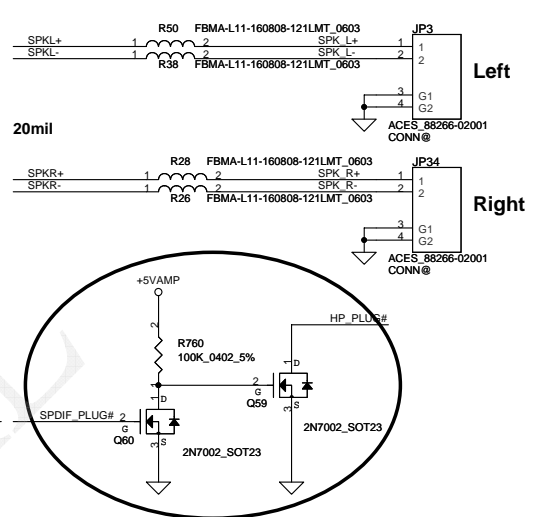
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



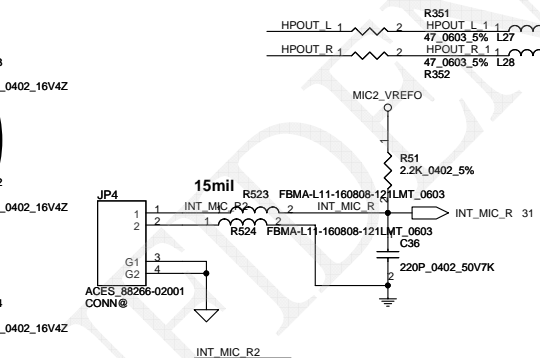
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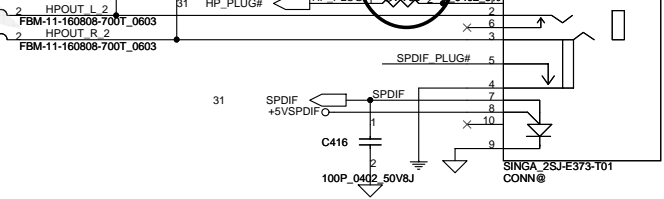
**Int. Speaker Conn.**



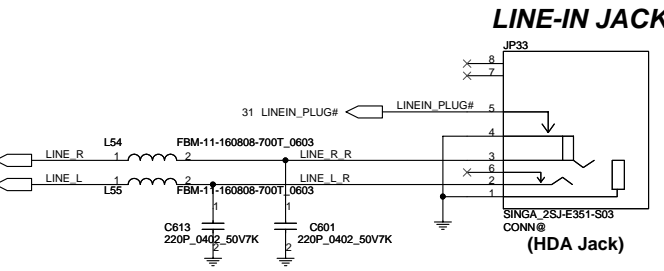
**Int MIC Conn.**



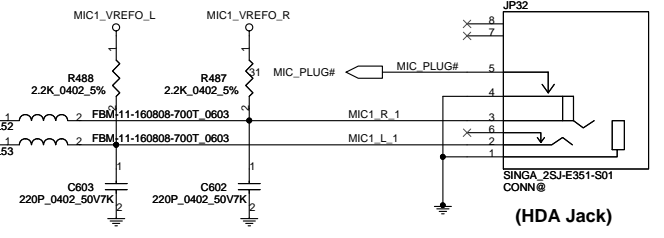
**20mil**



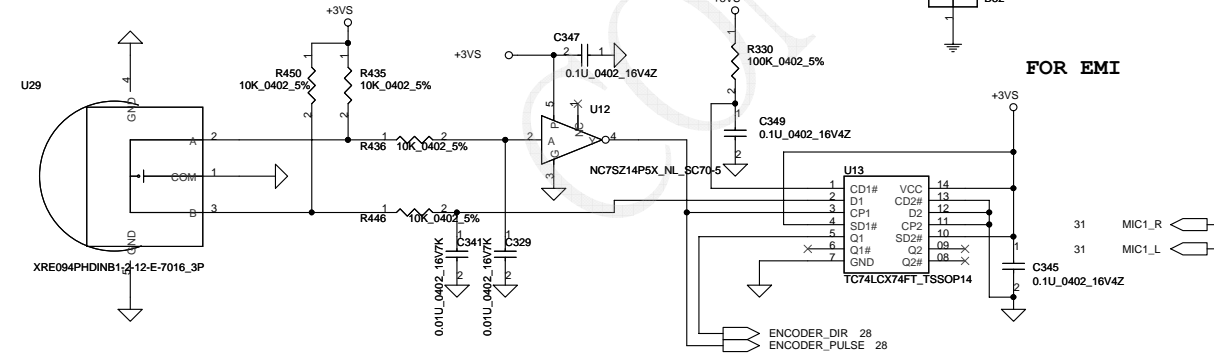
**S/PDIF Out JACK  
LINE Out/Headphone Out**



**MIC JACK**



**Volume Control Circuit**

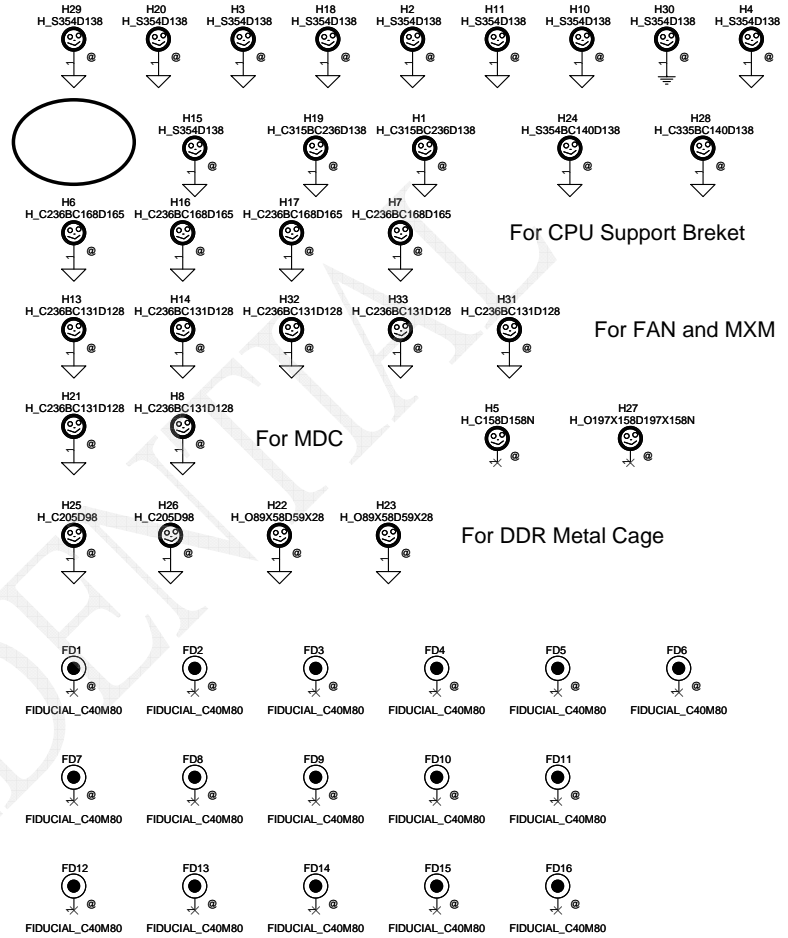
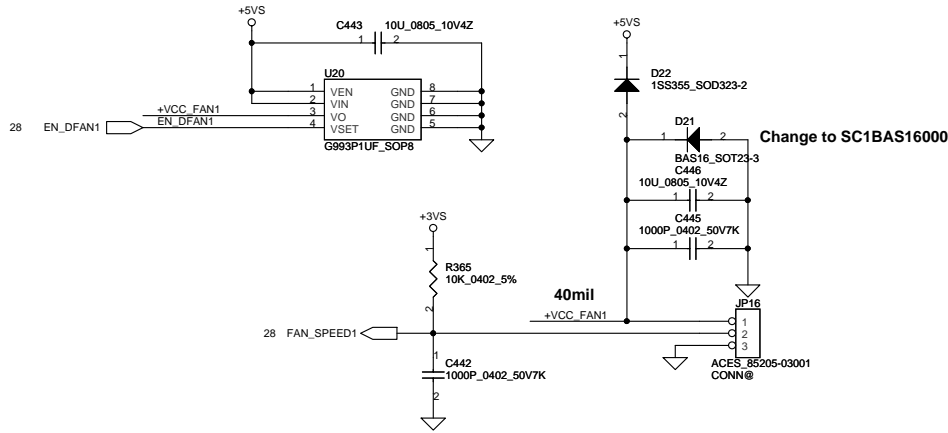


**FOR EMI**

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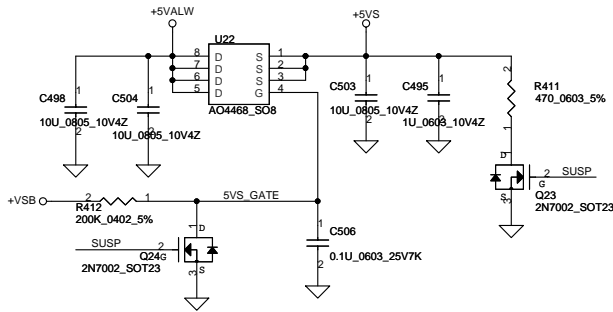
### FAN1 Conn



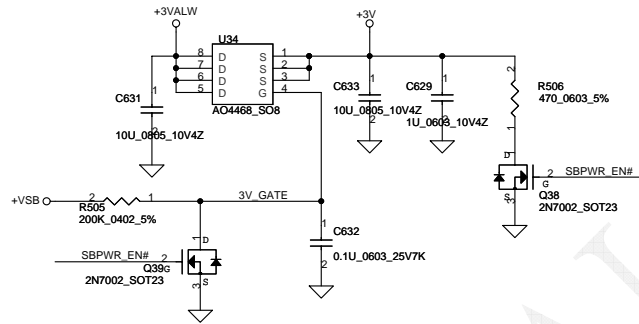
CONFIDENTIAL

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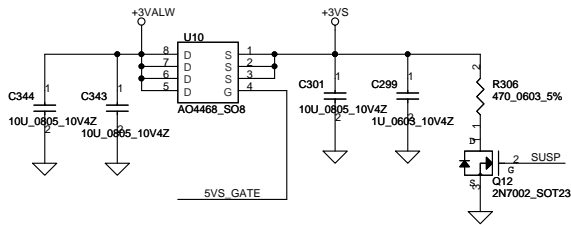
**+5VALW TO +5VS**



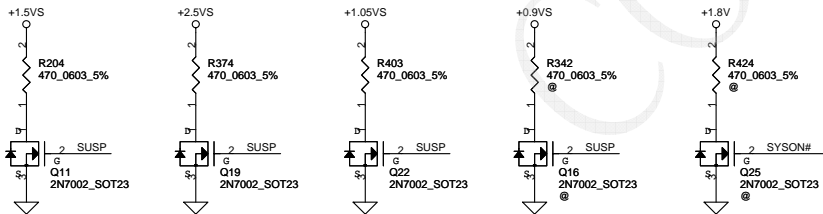
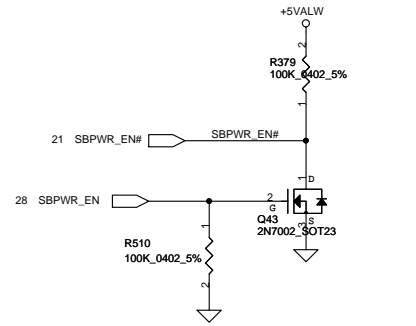
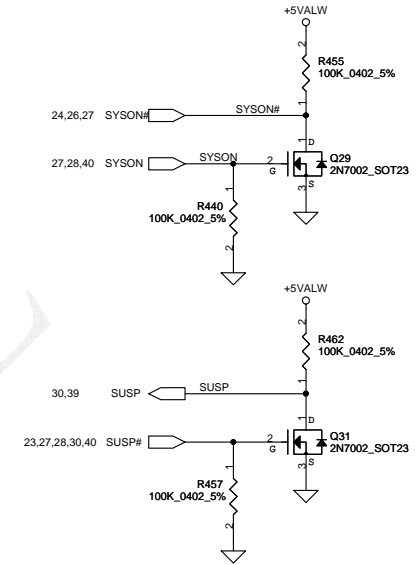
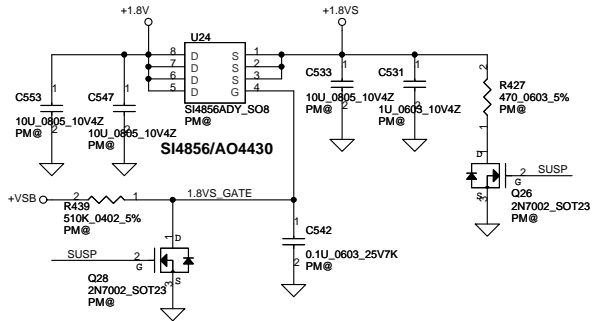
**+3VALW TO +3V\_SB(ICH8M AUX Power)**



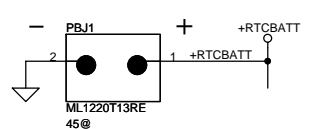
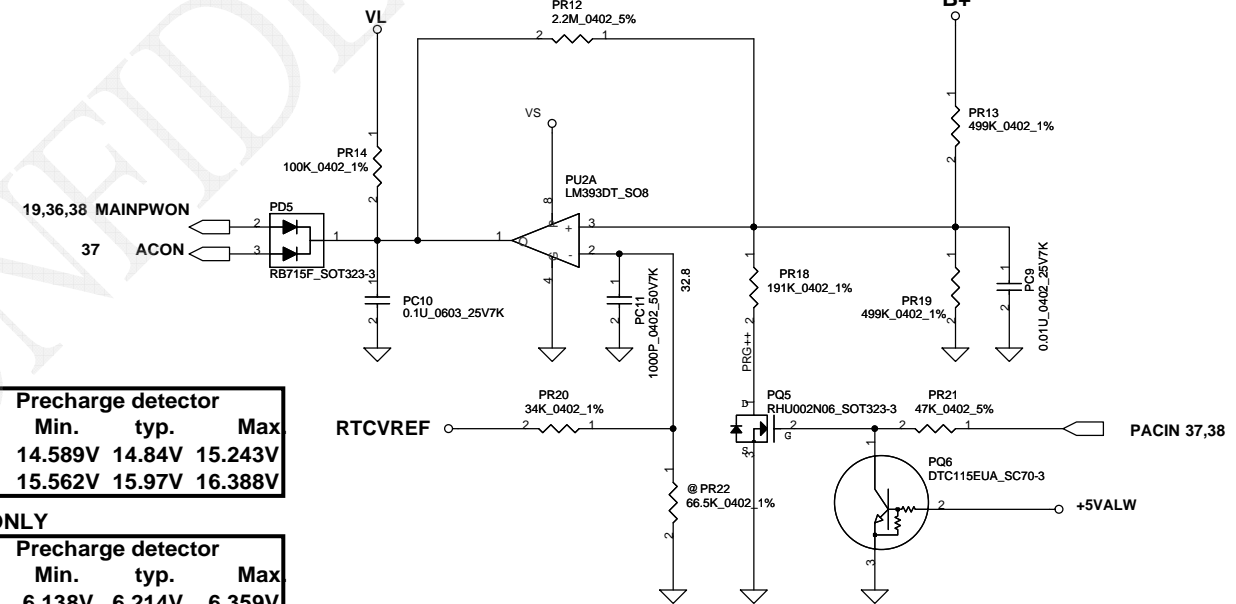
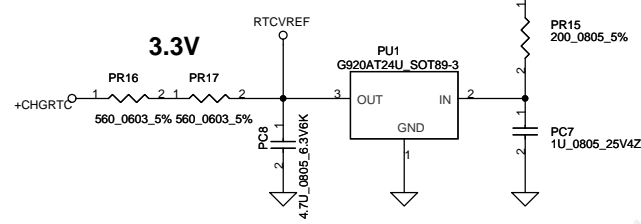
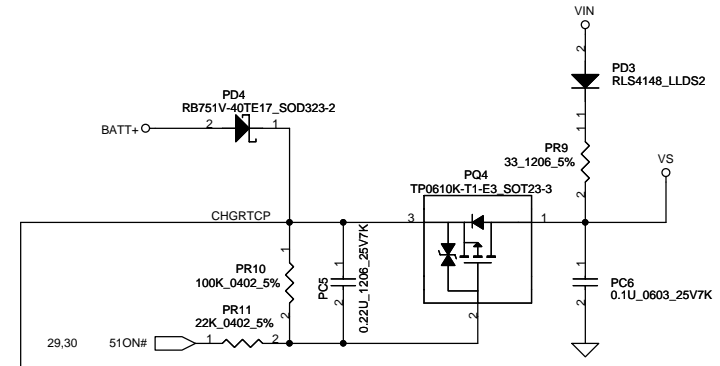
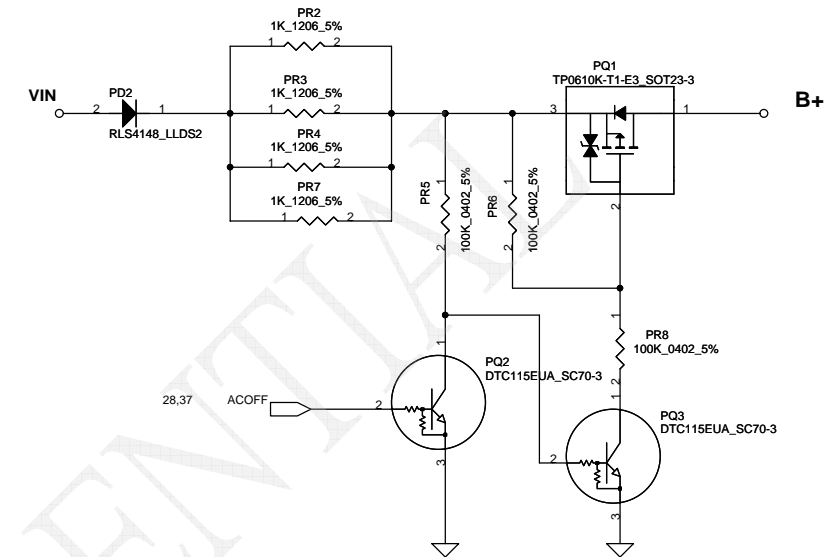
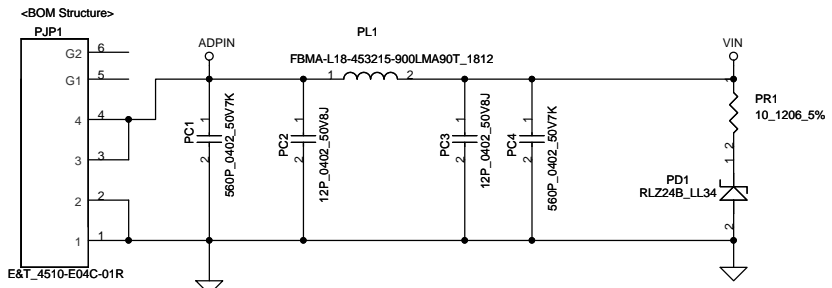
**+3VALW TO +3VS**



**+1.8V to +1.8VS**



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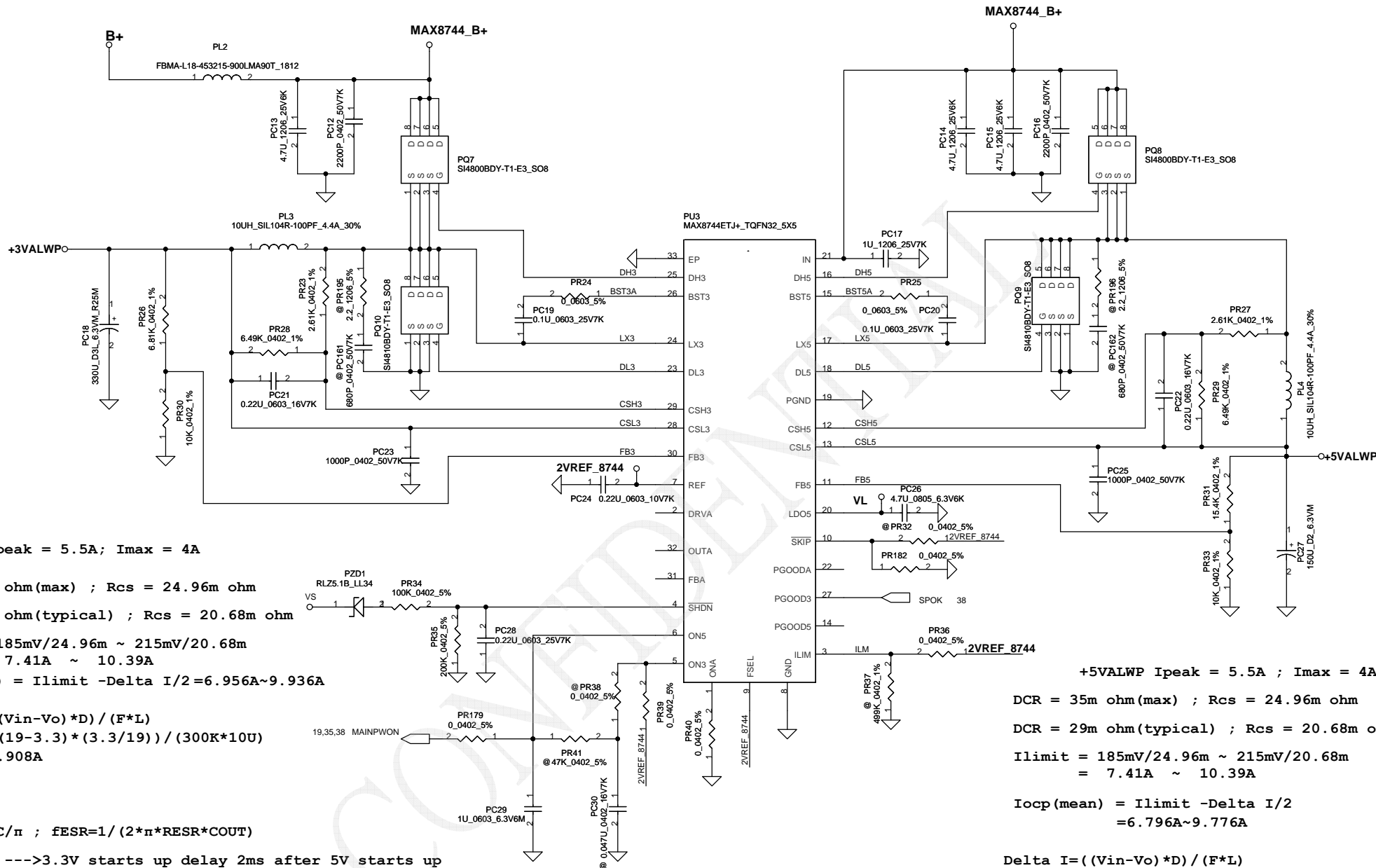
**ACIN**

Precharge detector			
	Min.	typ.	Max
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

**BATT ONLY**

Precharge detector			
	Min.	typ.	Max
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

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**+3VALWP Ipeak = 5.5A; Imax = 4A**  
 DCR = 35m ohm(max) ; Rcs = 24.96m ohm  
 DCR = 29m ohm(typical) ; Rcs = 20.68m ohm  
 Ilimit = 185mV/24.96m ~ 215mV/20.68m  
 = 7.41A ~ 10.39A  
 Iocp(mean) = Ilimit -Delta I/2=6.956A~9.936A

**Delta I = ((Vin-Vo) \*D) / (F\*L)**  
 = ((19-3.3) \* (3.3/19)) / (300K\*10U)  
 = 0.908A

**Notes :**  
 fESR<=fOSC/n ; fESR=1/(2\*π\*RESR\*COU)

**ON3 = REF --->3.3V starts up delay 2ms after 5V starts up**

**+5VALWP Ipeak = 5.5A ; Imax = 4A**  
 DCR = 35m ohm(max) ; Rcs = 24.96m ohm  
 DCR = 29m ohm(typical) ; Rcs = 20.68m ohm  
 Ilimit = 185mV/24.96m ~ 215mV/20.68m  
 = 7.41A ~ 10.39A  
 Iocp(mean) = Ilimit -Delta I/2  
 = 6.796A~9.776A

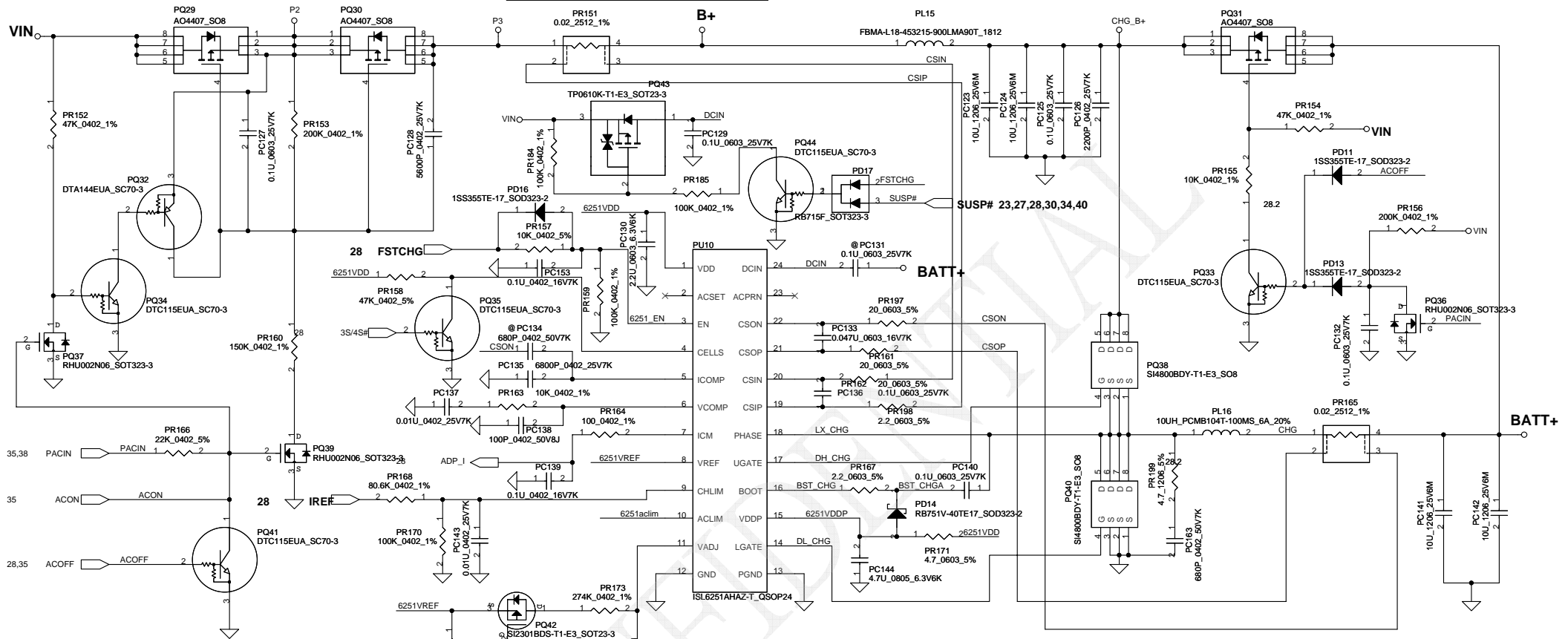
**Delta I = ((Vin-Vo) \*D) / (F\*L)**  
 = ((19-5) \* (5/19)) / (300K\*10U)  
 = 1.228A

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Iada=0~4.74A (90W)

$ADP\_I = 19.9 * I_{adapter} * R_{sense}$

$CP = 85\% * I_{ada} ; CP = 4.07A$

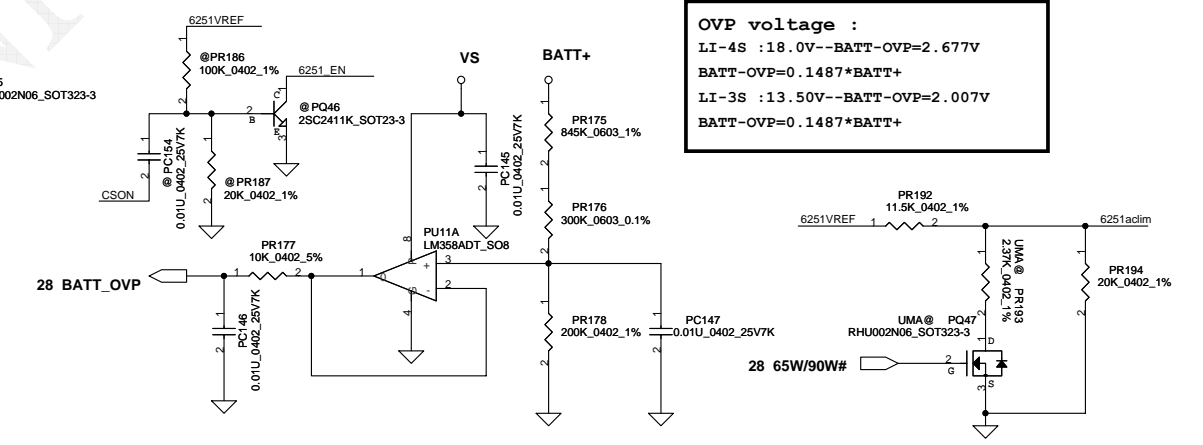
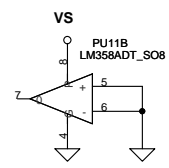


CP mode  
 $I_{input} = (1/0.02) * ((0.05 * V_{aclim}) / 2.39 + 0.05)$   
 where  $V_{aclim} = 1.502V$ ,  $I_{input} = 4.07A$   
 $V_{aclim} = 2.39 * ((10K / 152K) / ((5.76K / 152K) + (10K / 152K))) = 1.502V$

CC=0.6~4.48A  
 $I_{REF} = 0.7224 * I_{charge}$   
 $I_{REF} = 0.43V \sim 3.24V$

BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

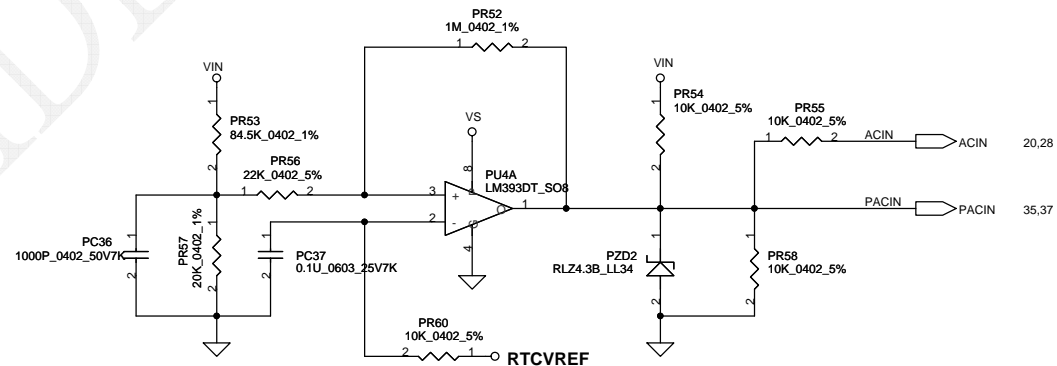
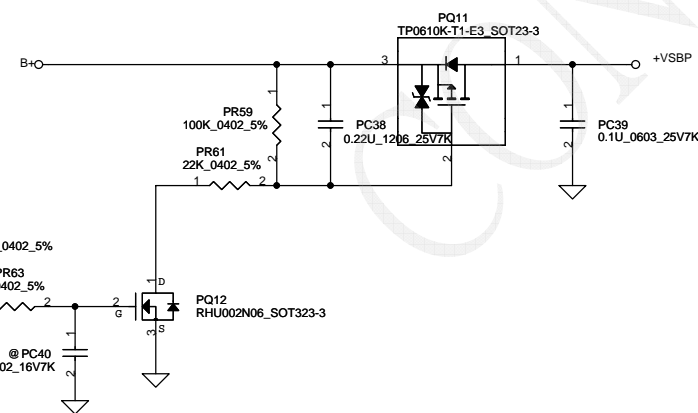
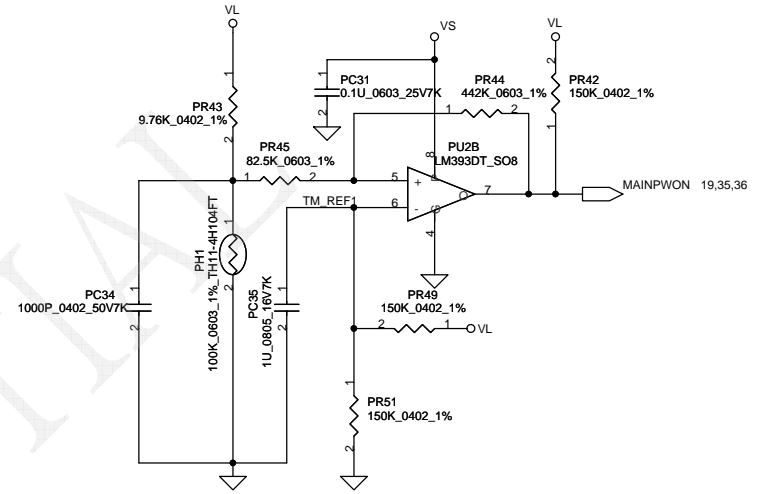
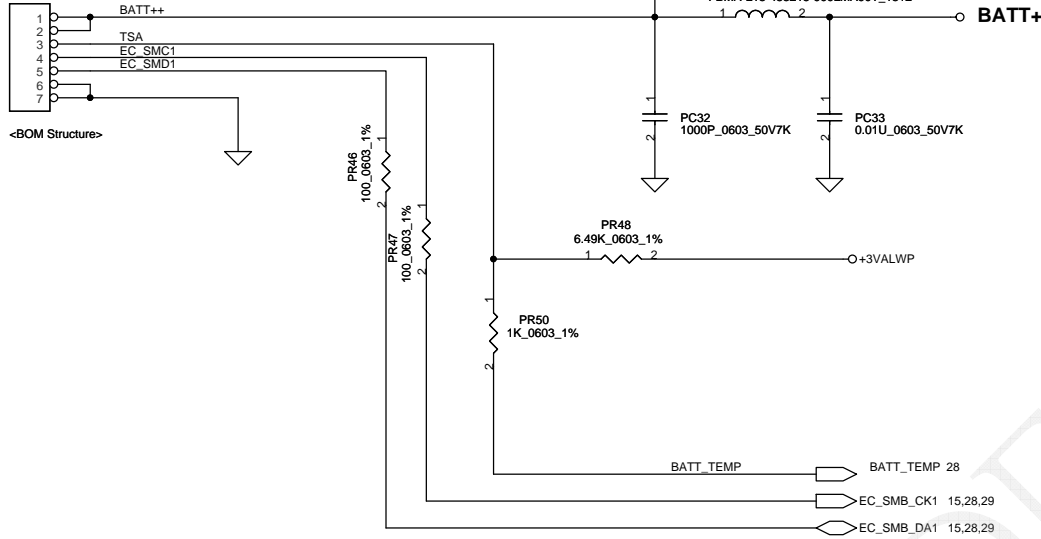
OVP voltage :  
 LI-4S : 18.0V -- BATT-OVP = 2.677V  
 BATT-OVP = 0.1487 \* BATT+  
 LI-3S : 13.50V -- BATT-OVP = 2.007V  
 BATT-OVP = 0.1487 \* BATT+



PH1 under CPU botten side :  
 CPU thermal protection at 90 degree C  
 Recovery at 70 degree C

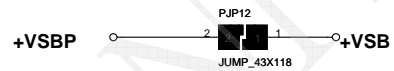
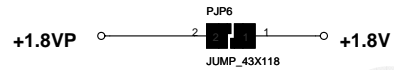
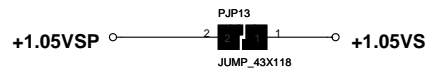
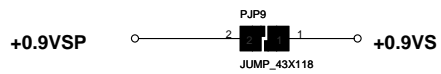
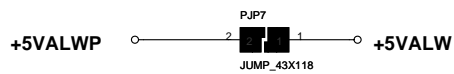
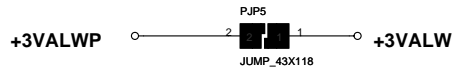
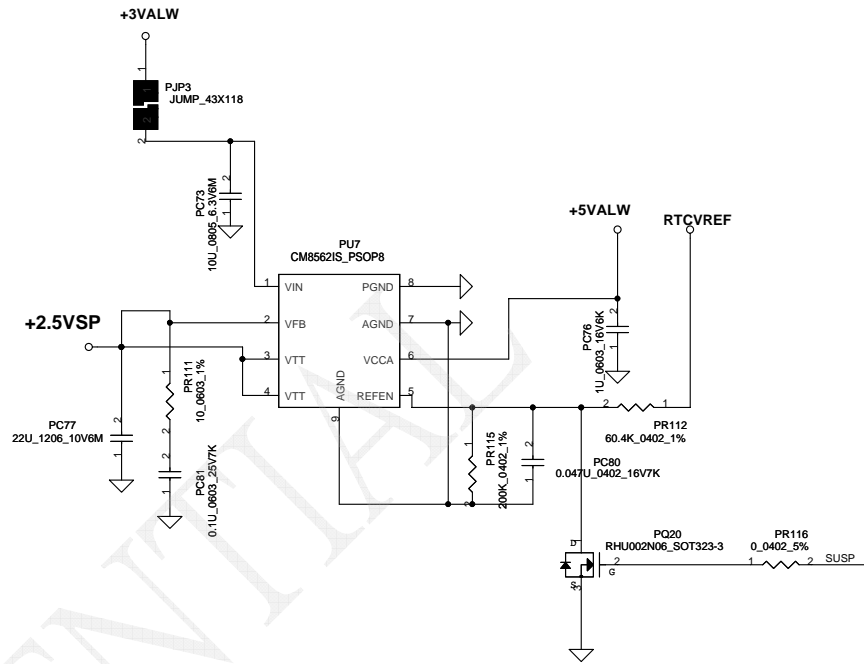
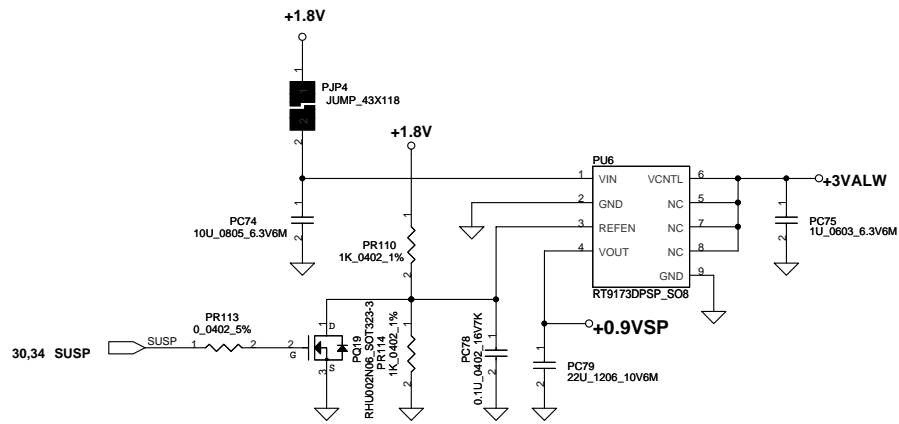
SUYIN\_200275MR007G161ZL

PJP2

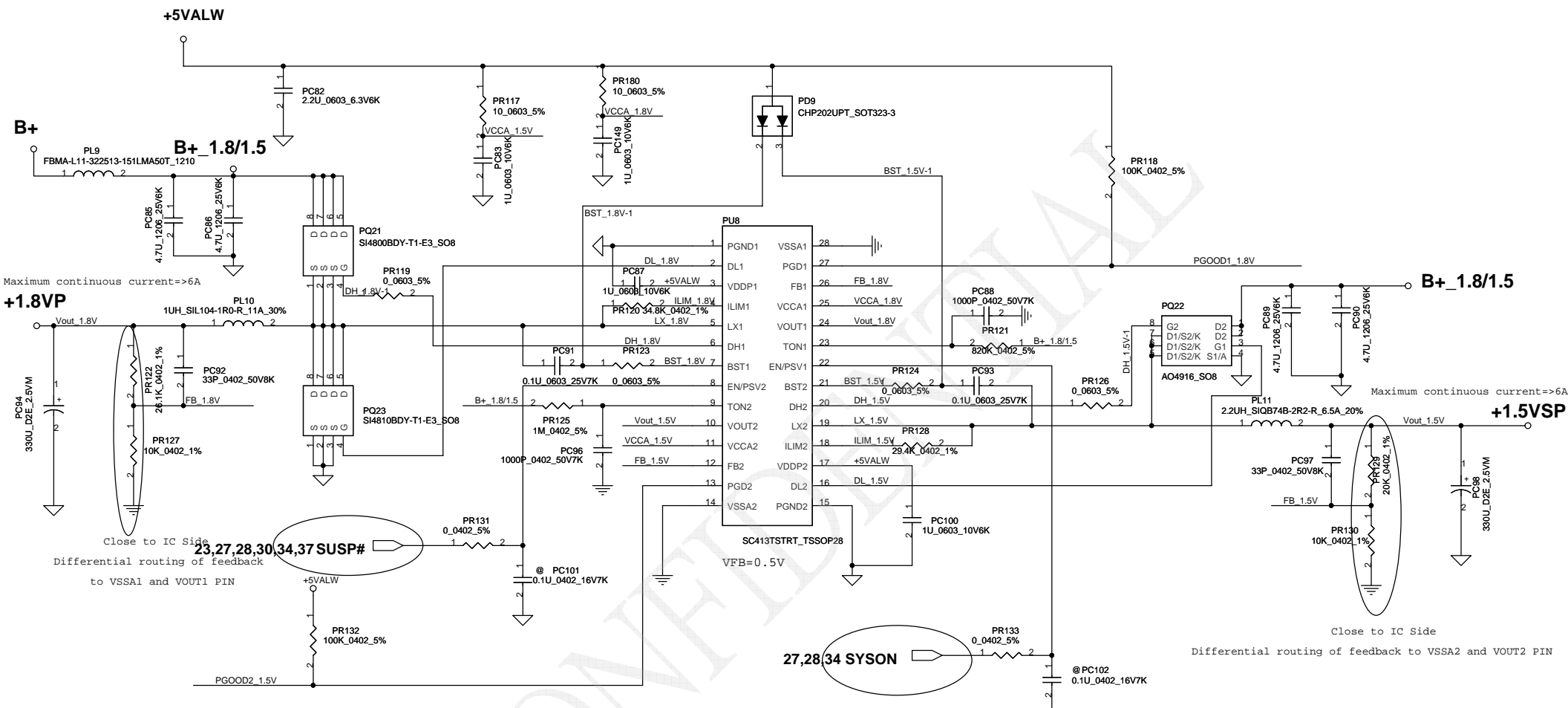


	Min.	typ.	Max.
H-->L	16.976V	17.257V	17.728V
L-->H	17.430V	17.901V	18.384V

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Maximum continuous current => 6A

Maximum continuous current => 6A

Close to IC Side  
Differential routing of feedback  
to VSSA1 and VOUT1 PIN

Close to IC Side  
Differential routing of feedback to VSSA2 and VOUT2 PIN

VFB=0.5V  
 $V_o = VFB * (1 + PR122 / PR127) = 1.805V$   
**Ipeak=12.17A, I<sub>max</sub>=8.519A**  
 $Ton = (3.3E-12 * (PR121 + 37K)) * (Vout / VBat) + 50ns$   
 $= 3.3 * 10e-12 * (820K + 37K) * (1.8 / 19) + 50ns = 0.3179us$   
 FDS6670AS:Rds(on) => Typ: 9 mOhm  
 Max: 11.5 mOhm  
 $Iocp = Ivalley + "Iripple" / 2$   
 $Iripple = (vin - vout) * (Ton / L) = 5.467A, 1/2 Iripple = 2.734A$   
 $Ivalleymin = 10E-6 * (PR120 / Rds(ON))max * 1.5$   
 $= 9 * 10e-6 * (27.4K / 0.0115 * 1.5) = 14.295A > 11.73 * 1.2 = 14.076A$   
 $Ivalleymax = 10E-6 * (PR120 / Rds(ON))typ * 1.2$   
 $= 11 * 10e-6 * (27.4K / 0.009 * 1.2) = 27.907A$   
 OCP ==> 17.029A ~ 30.641A

VFB=0.5V  
 $V_o = VFB * (1 + PR129 / PR130) = 1.5V$   
**Ipeak=5.16A, I<sub>max</sub>=3.612A**  
 $Ton = (3.3E-12 * (PR125 + 37K)) * (Vout / VBat) + 50ns$   
 $= 0.3201us$   
 AO4916 Rds(on) => Typ: 21 mOhm  
 Max: 27 mOhm  
 $Ivalleymin = 9 * 10u * (29.4K / 0.027 * 1.4) = 7A$   
 $Ivalleymax = 11 * E-6 * (29.4K / 0.021 * 1.1) = 12.833A$   
 $Iripple = (vin - vout) * (Ton / L) = 2.546A, 1/2 Iripple = 1.273A$   
 $Iocp = Ivalley + "Iripple" / 2$   
 OCP ==> 8.273A ~ 14.106A

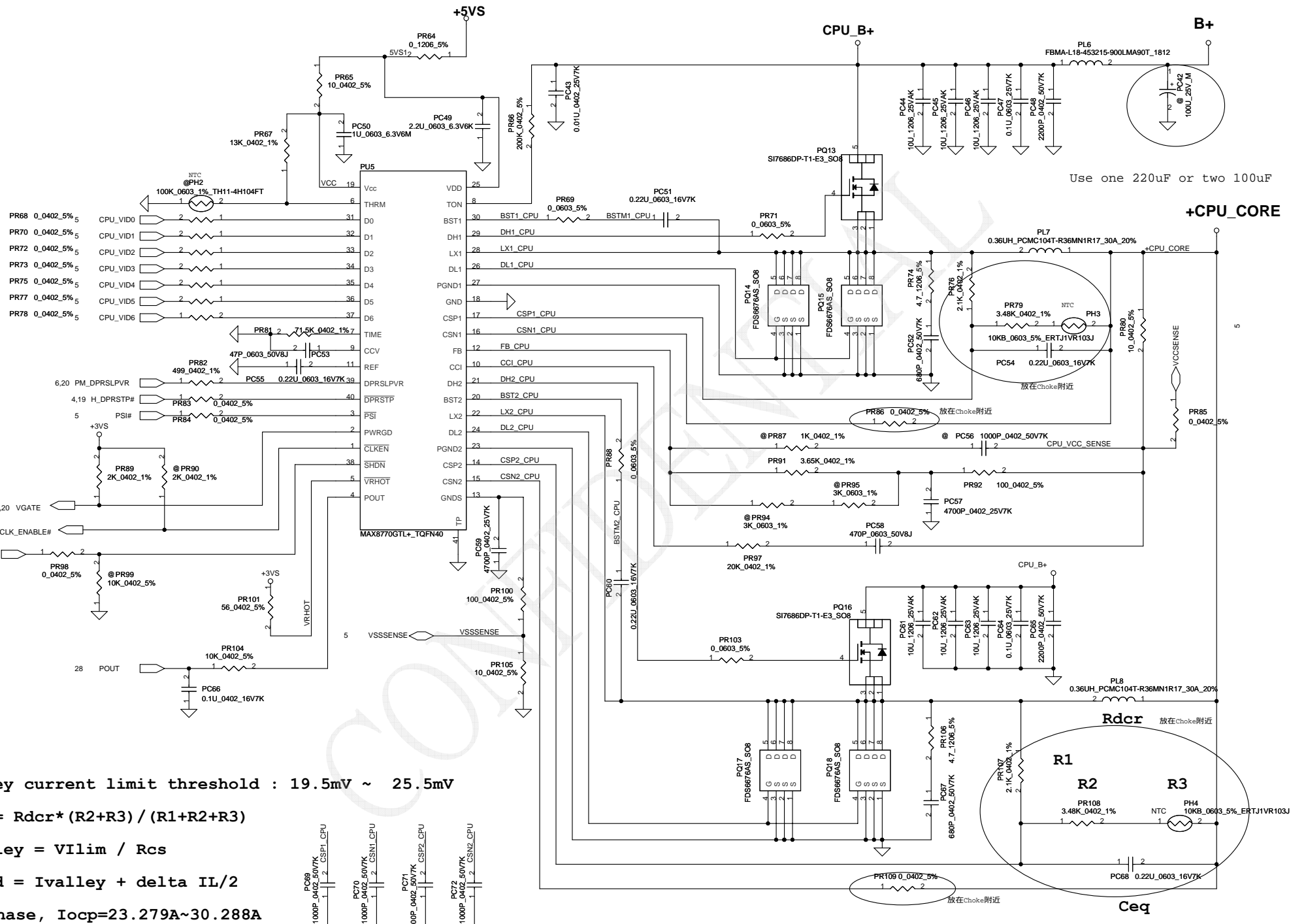


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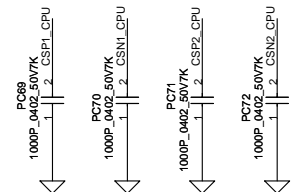
Valley current limit threshold : 19.5mV ~ 25.5mV

$$R_{cs} = R_{dcr} * (R2 + R3) / (R1 + R2 + R3)$$

$$I_{valley} = V_{lim} / R_{cs}$$

$$I_{load} = I_{valley} + \Delta I_L / 2$$

Per phase,  $I_{ocp} = 23.279A \sim 30.288A$



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	EC GPIO pin modify	EC GPIO pin modify	0.1 ==> 0.2	8	DPST_PWM net modify	3/19	
2	clk frequency error	pin error	0.1 ==> 0.2	14	Q48,Q49,Q50 pin error		
3	EC add a GPIO pin	EC GPIO pin modify	0.1 ==> 0.2	16	del DPST_PWM net from North Bridge		
4	follow ICL50	follow ICL50	0.1 ==> 0.2	20	CRT_DET# net modify		
5	EMI request	EMI request	0.1 ==> 0.2	24	Add R477, R748		
6	ESD request	ESD request	0.1 ==> 0.2	25	reserve D30,D31		
7	test	test	0.1 ==> 0.2	26	reserve MINI1_LED#		
8	Blue LED issue	Blue LED issue	0.1 ==> 0.2	27	BT_LED# schematic modify		
9	EC GPIO pin modify	EC GPIO pin modify	0.1 ==> 0.2	28	EC GPIO pin define modify		
10	ESD request	ESD request	0.1 ==> 0.2	29	reserve C895 to C904		
11	easy short	easy short	0.1 ==> 0.2	30	change J1,J2 jumper sybmol to 0603 symbol		
12	ESD request	ESD request	0.1 ==> 0.2	31	Add R751,R752,R753		
13	chip issue	chip issue	0.1 ==> 0.2	32	U31 chip update version		
14	voice too small	modify gain value	0.1 ==> 0.2	32	change R472 form 39k to 30k ohm		
15	EMI request	EMI request	0.1 ==> 0.2	32	change R523,R524,R50,R38,R26,R28 for 0 ohm to bead		
16	DFX request	DFX request	0.1 ==> 0.2	33	del pjp15		
17	Wireless Lan S4 fail	Wireless Lan fail	0.2 ==> 0.3	26	del R756, add R757		
18	Wireless Lan S4 fail	Wireless Lan fail	0.2 ==> 0.3	26	change C906,C907 from 22u_1206 to 10u_0805		
19	Lead Free	non LF==>Lead Free	0.2 ==> 0.3	17	change C211,C510,C514,C216,C508,C515		
20	KBC version update	KBC version update	0.2 ==> 0.3	28	reserve 0.1u at pin 124		
21	SPDIF udpate	SPDIF circuit udpate	0.2 ==> 0.3	32	add q59,q60		
22	DFX	DFX issue	0.2 ==> 0.3	32	del JP13		
23	SPDIF jack	SPDIF jack noise	0.2 ==> 0.3	31	add R764		
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Charger IC damage issue	Charger IC damage issue	0.2	40	Change PR161 from SD013220B80 to SD013200A80		
2	Charger IC damage issue	Charger IC damage issue	0.2	40	Change PR162 from SD013180A80 to SD013200A80		
3	Charger IC damage issue	Charger IC damage issue	0.2	40	Add PR197 SD013200A80		
4	Charger IC damage issue	Charger IC damage issue	0.2	40	Add PR198 SD013220B80		
5	Charger IC damage issue	Charger IC damage issue	0.2	40	Add PC133 SE026473K80		
6	Add EMI solution in charger.	Add EMI solution in charger.	0.3	40	Add PR199 SD001470B80(S RES 1/4 4.7 1206 5%).	04/01/07	FVT
7	Add EMI solution in charger.	Add EMI solution in charger.	0.3	40	Add PC163 SE074681K80(S CER CAP 680P 50V K X7R 0402)	04/01/07	FVT
8	PC28 SE000005ZM8 isn't LF PN.	PC28 SE000005ZM8 isn't LF PN.	0.3	39	Change PC28 from SE000005ZM8 to SE000005Z80.	04/18/07	Pre-MP
9	Cost Down	Cost Down	0.3	40	Delete PC129 SE042104K80( S CER CAP 0.1U 25VK X7R 0603)	04/18/07	Pre-MP
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