

Compal Confidential

JDW50/JDY70 Schematics Document

Intel Merom Processor with Crestline(PM945/GM945) + DDRII + ICH7M
(With ATI MXM/B)

2007-4-12

REV: 0.3

Dr-Bios.com

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Card Reader	AD16	0	PIRQE

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

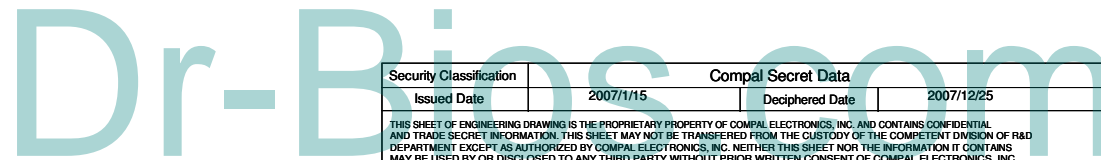
Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

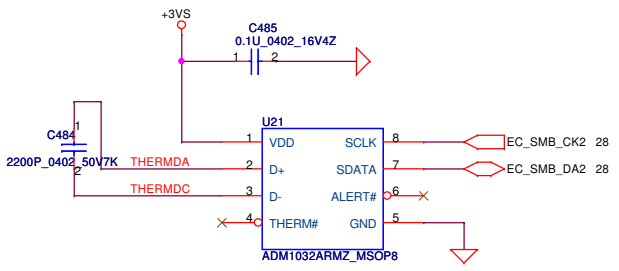
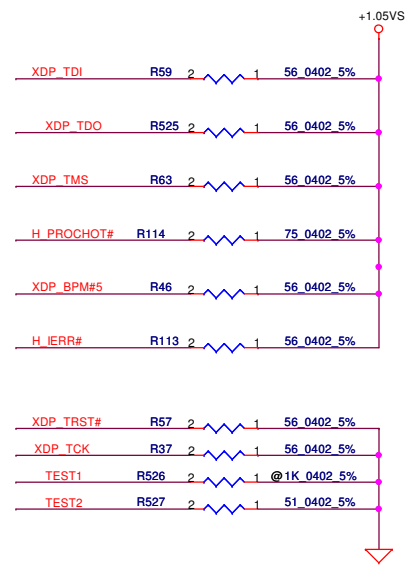
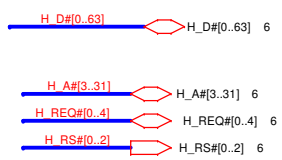
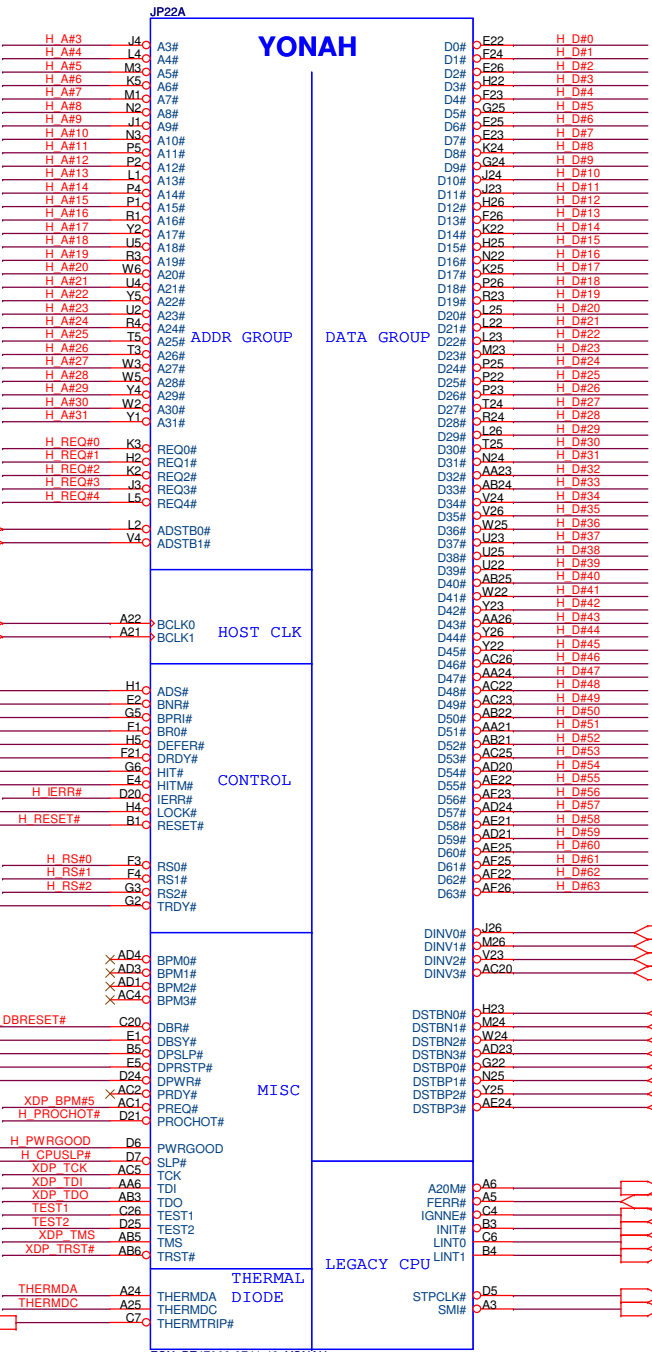
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	PM@
UMA	GM@
DVI	DVI@
SATA*1	SATA*1@
SATA*2	SATA*2@
Dbg	Dbg@



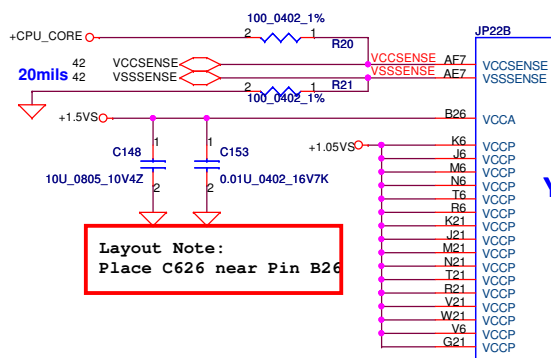
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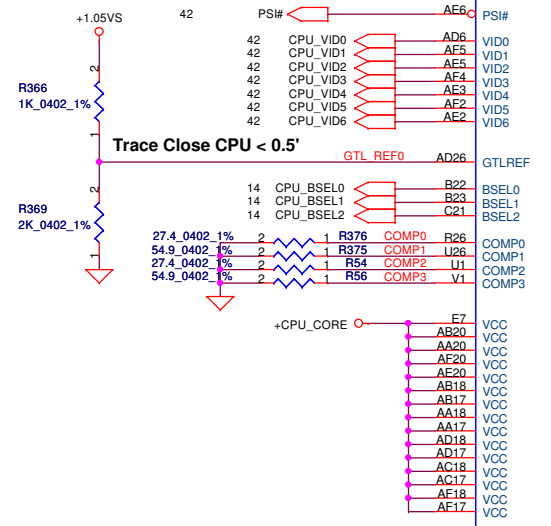
Layout Note:
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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Layout Note:
Place C626 near Pin B26



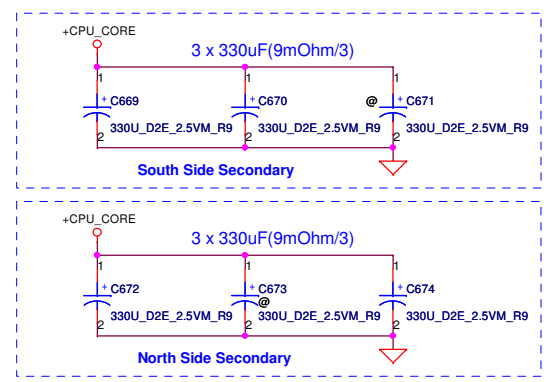
Trace Close CPU < 0.5'



YONAH

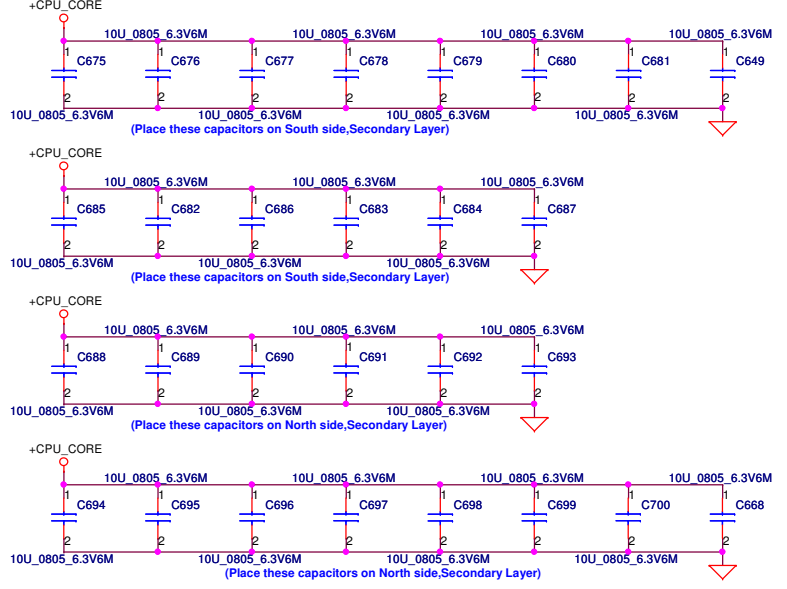
POWER, GROUND, RESERVED SIGNALS AND NC

FOX_PZ47903-2741-42_YONAH

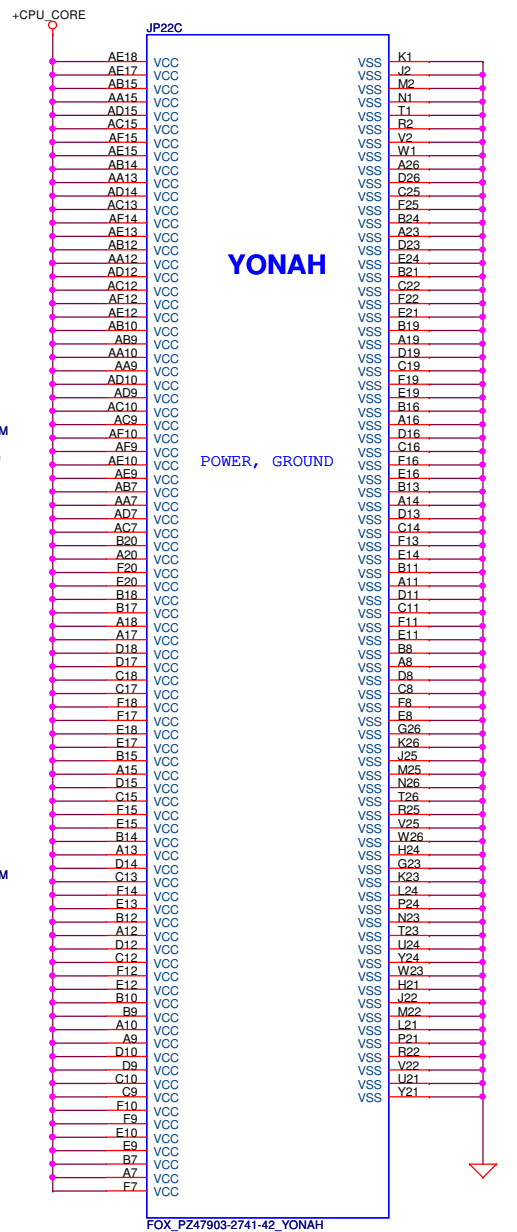
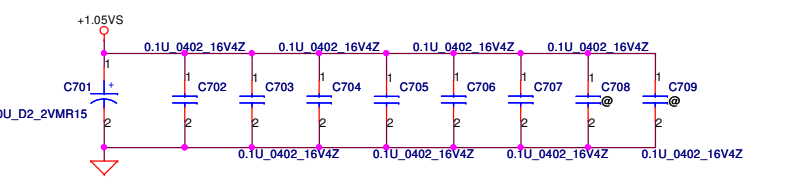


South Side Secondary

North Side Secondary



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32

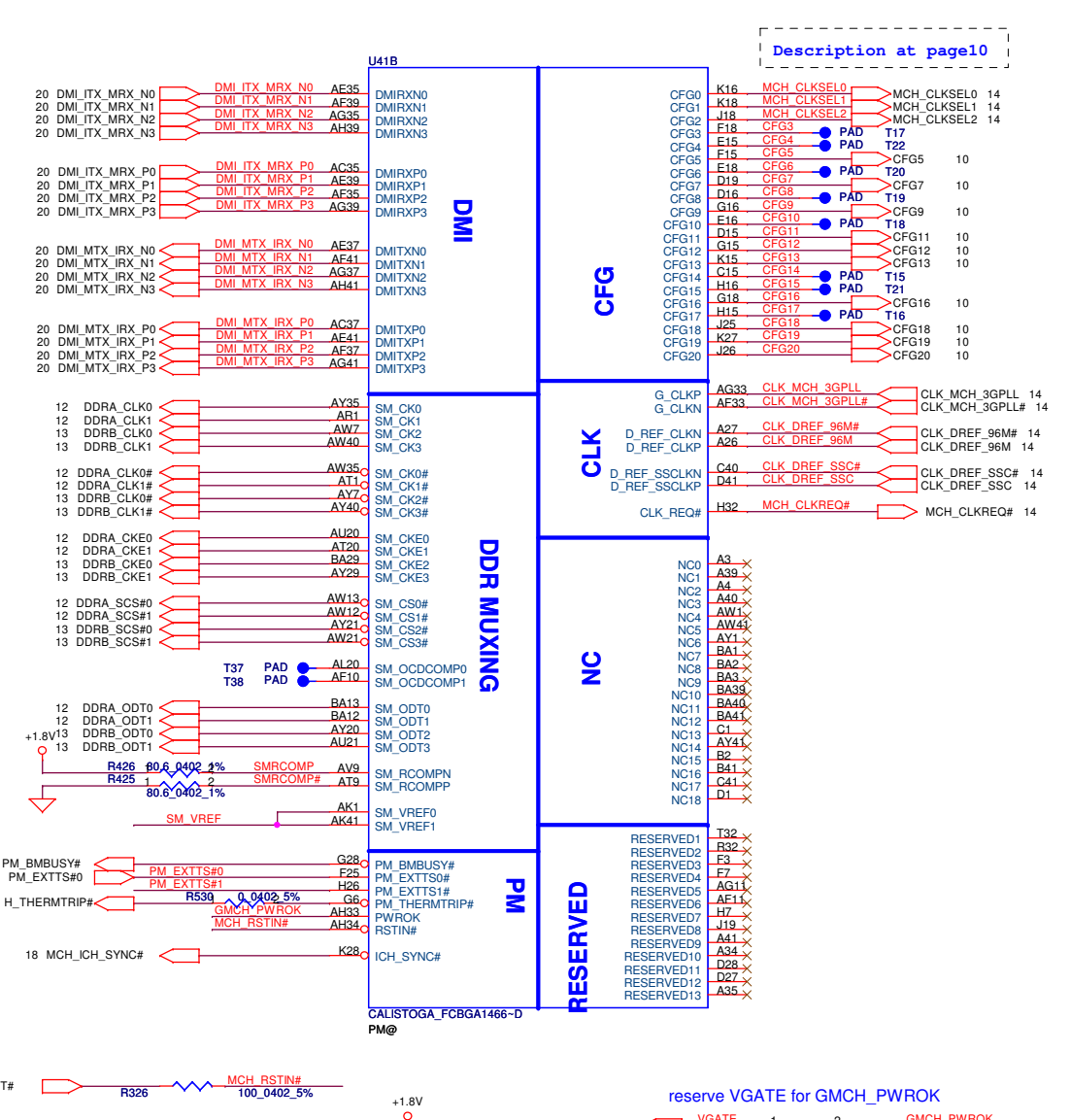
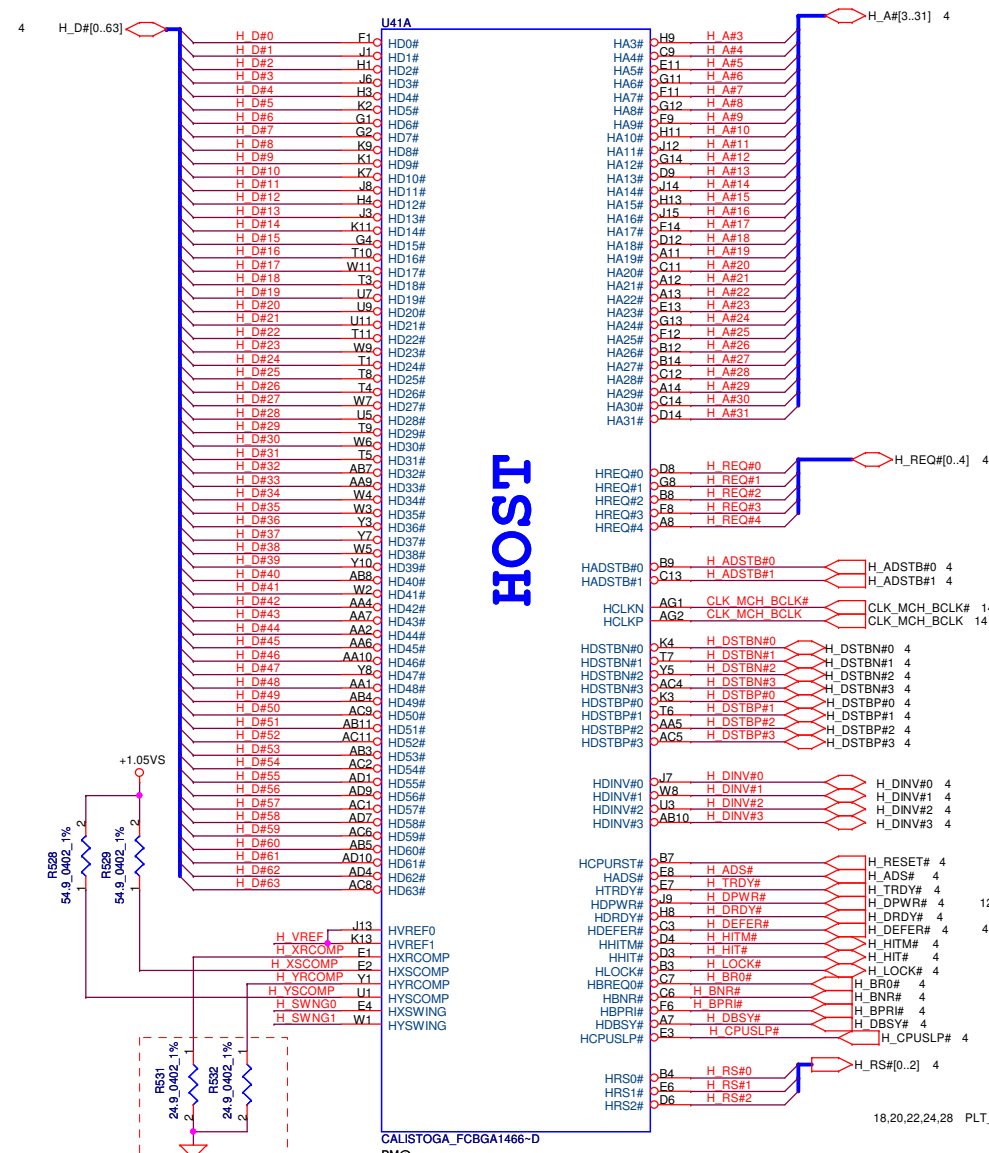


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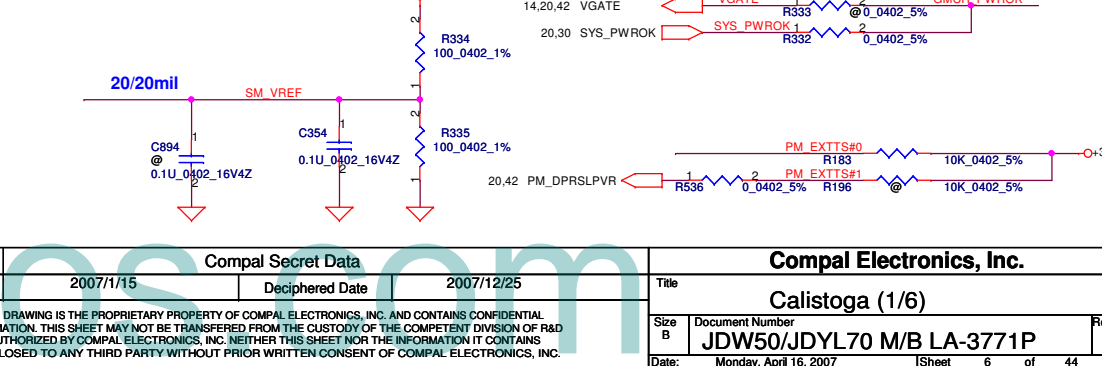
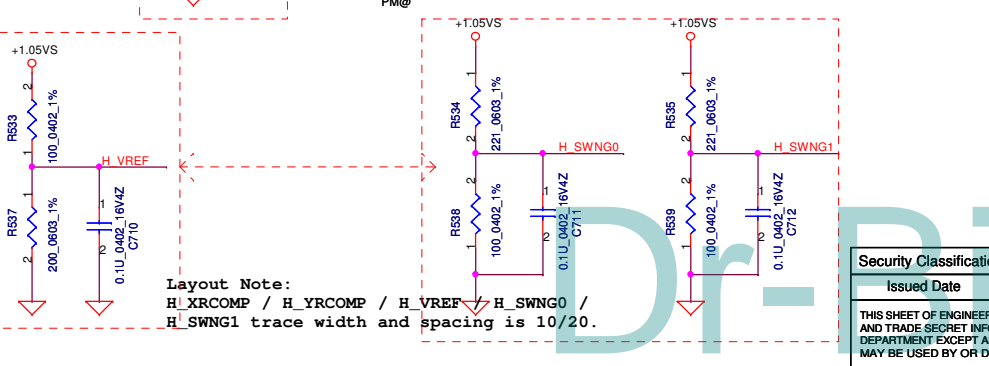
POWER, GROUND

FOX_PZ47903-2741-42_YONAH

TRACE CLOSELY CPU < 0.5'
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4ohms)
COMP1, COMP3 layout : Space 25mils (55ohms)

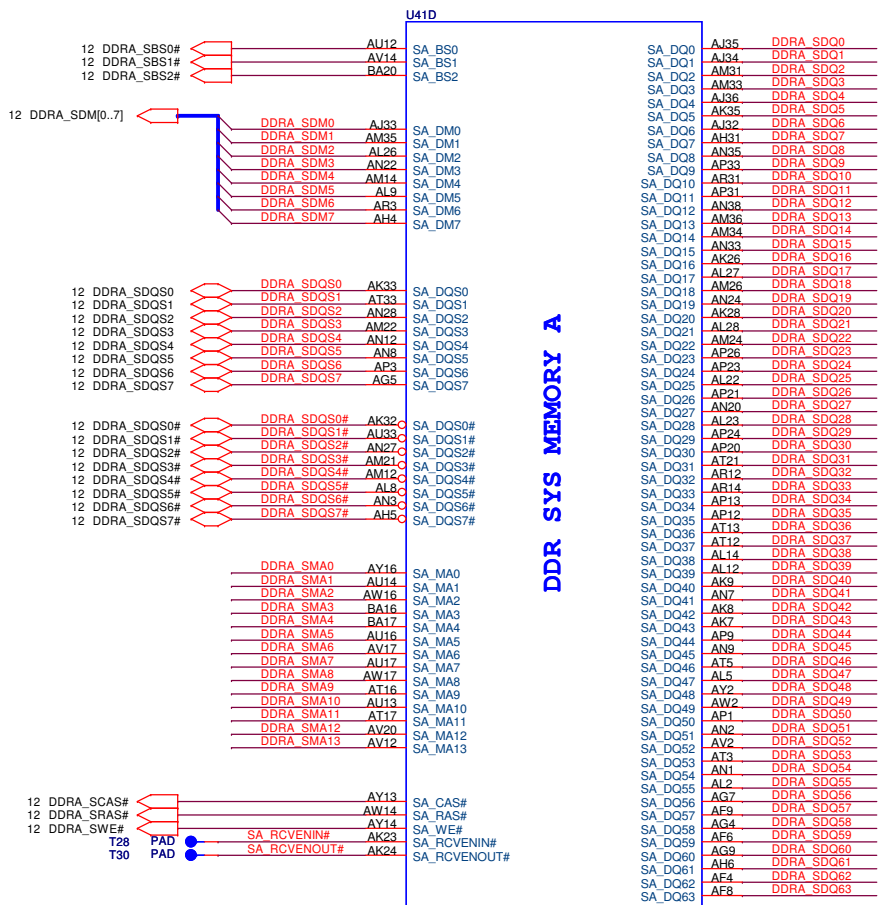
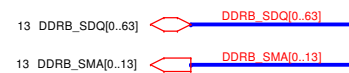
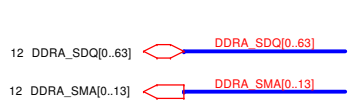


Description at page10

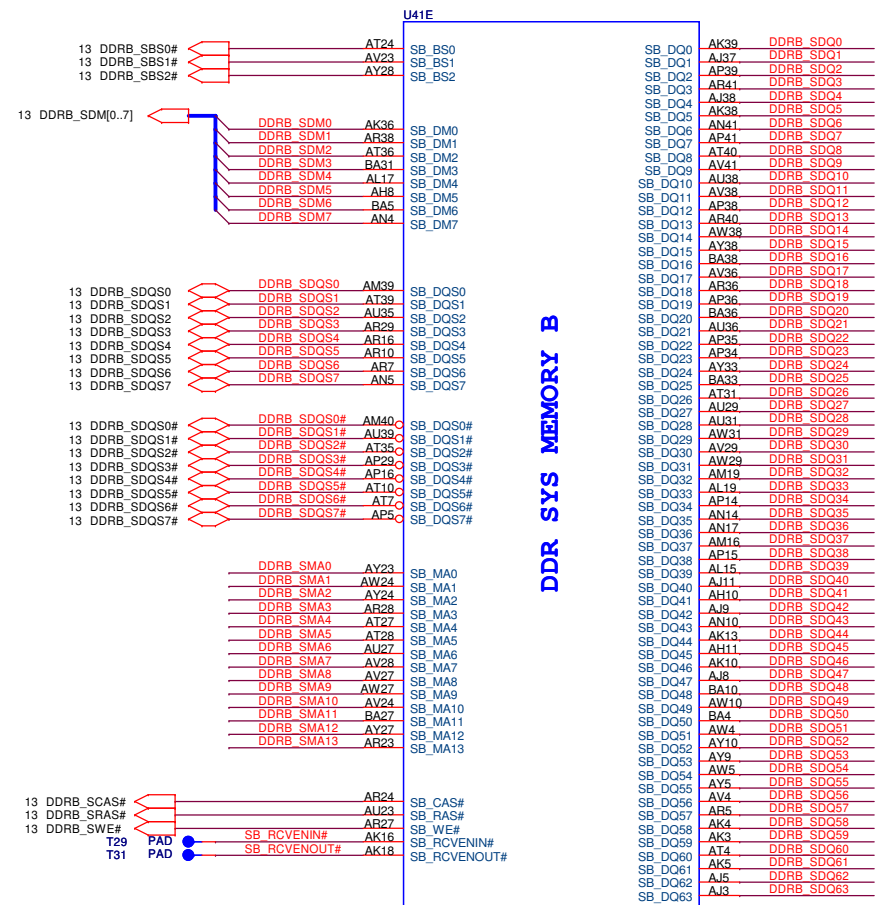


Layout Note:
 H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 /
 H_SWNG1 trace width and spacing is 10/20.

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DDR SYS MEMORY A

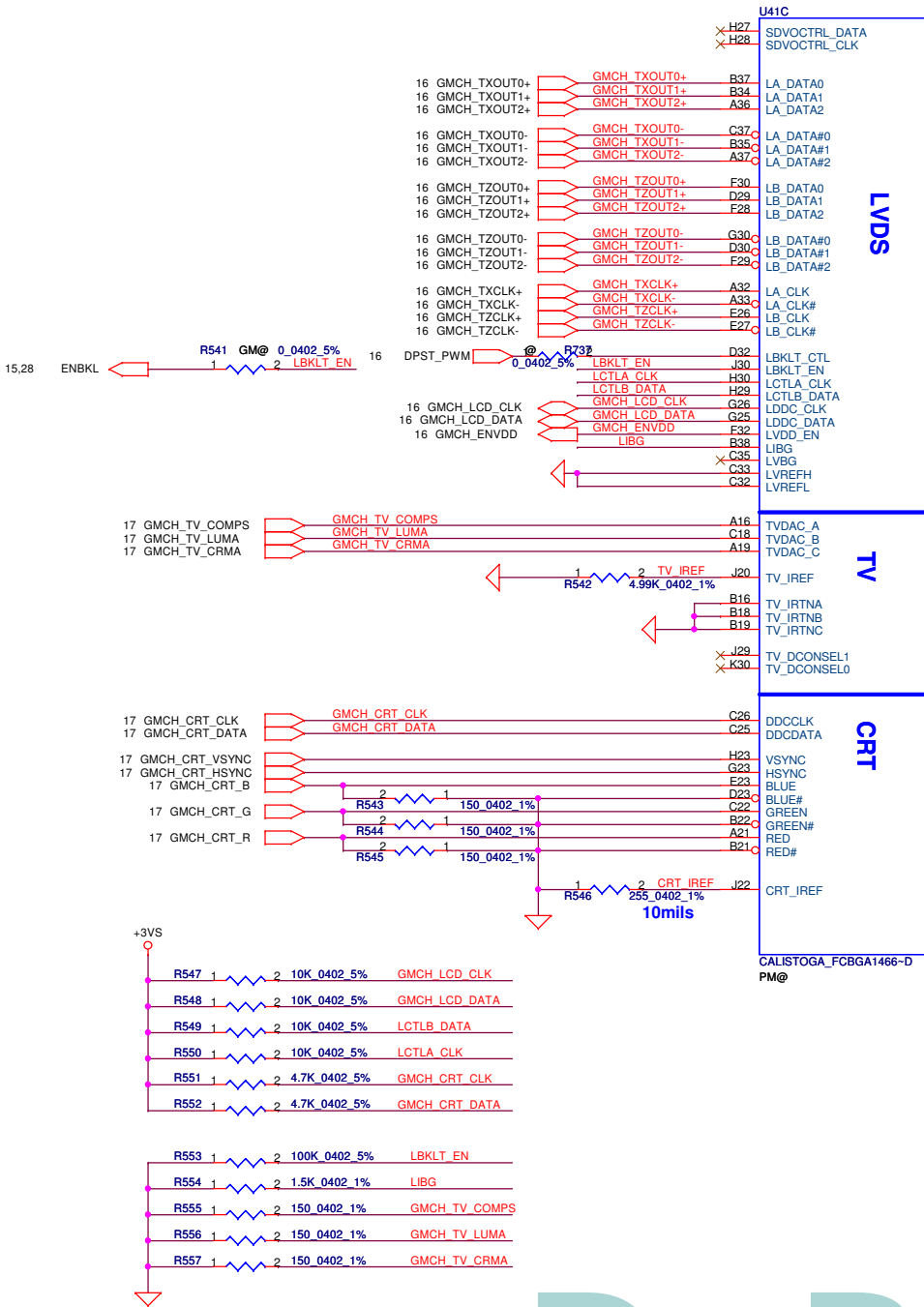


DDR SYS MEMORY B

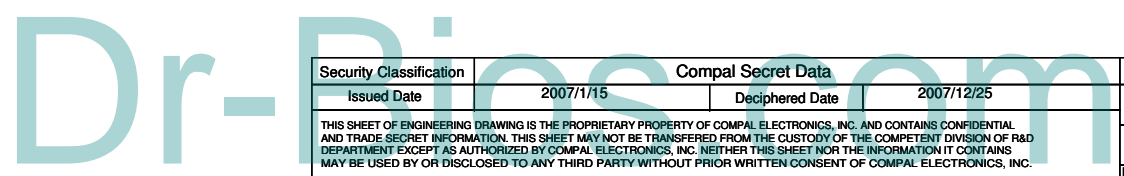
CALISTOGA_FCBGA1466-D
PM@

CALISTOGA_FCBGA1466-D
PM@

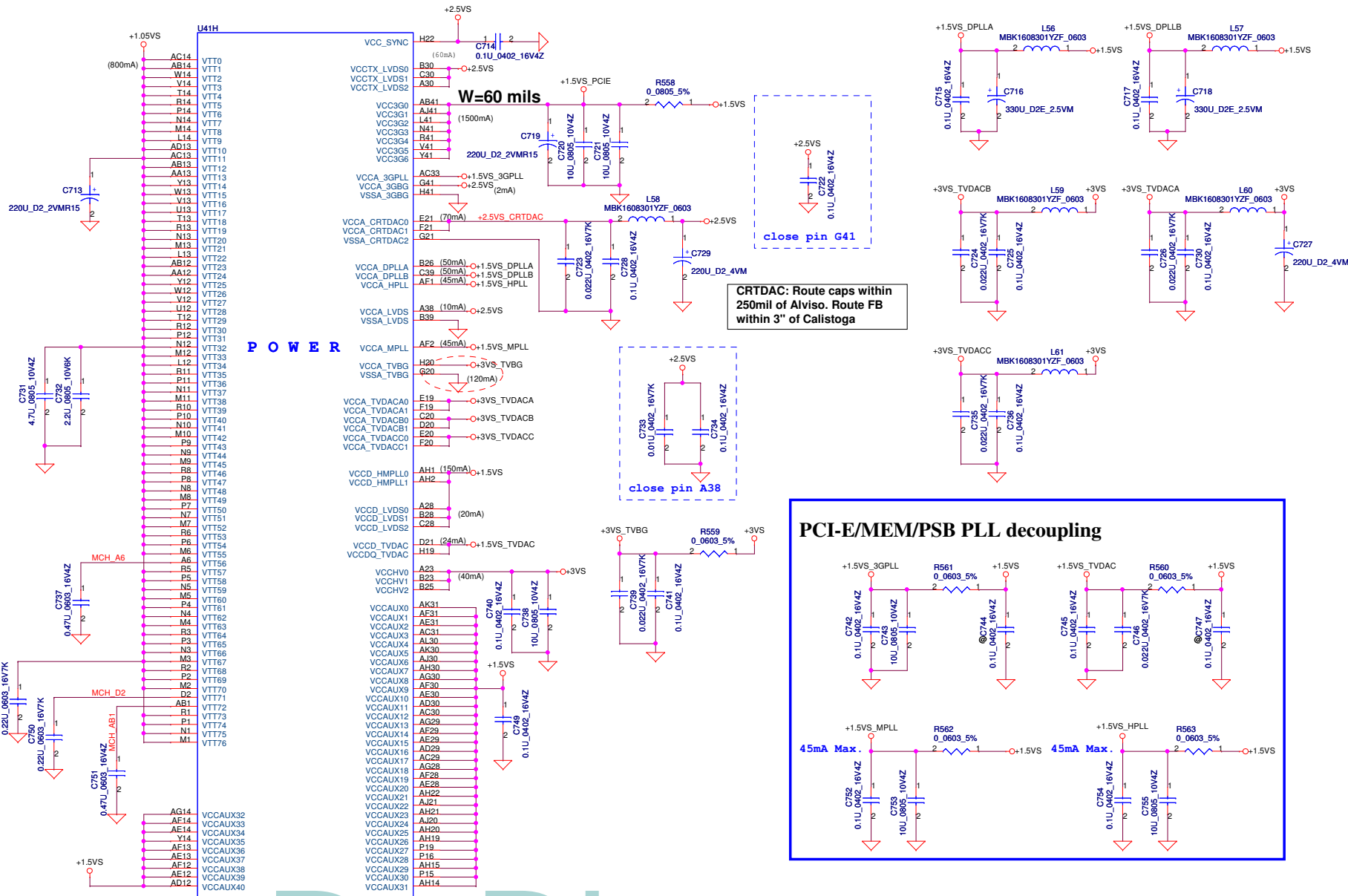
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CALISTOGA_FCBGA1466-D
PM@



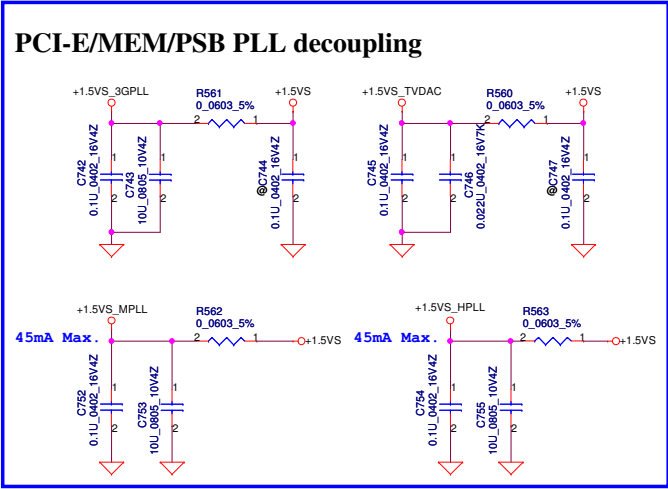
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POWER

CRTDAC: Route caps within 250mil of Alviso. Route FB within 3" of Calistoga

close pin A38

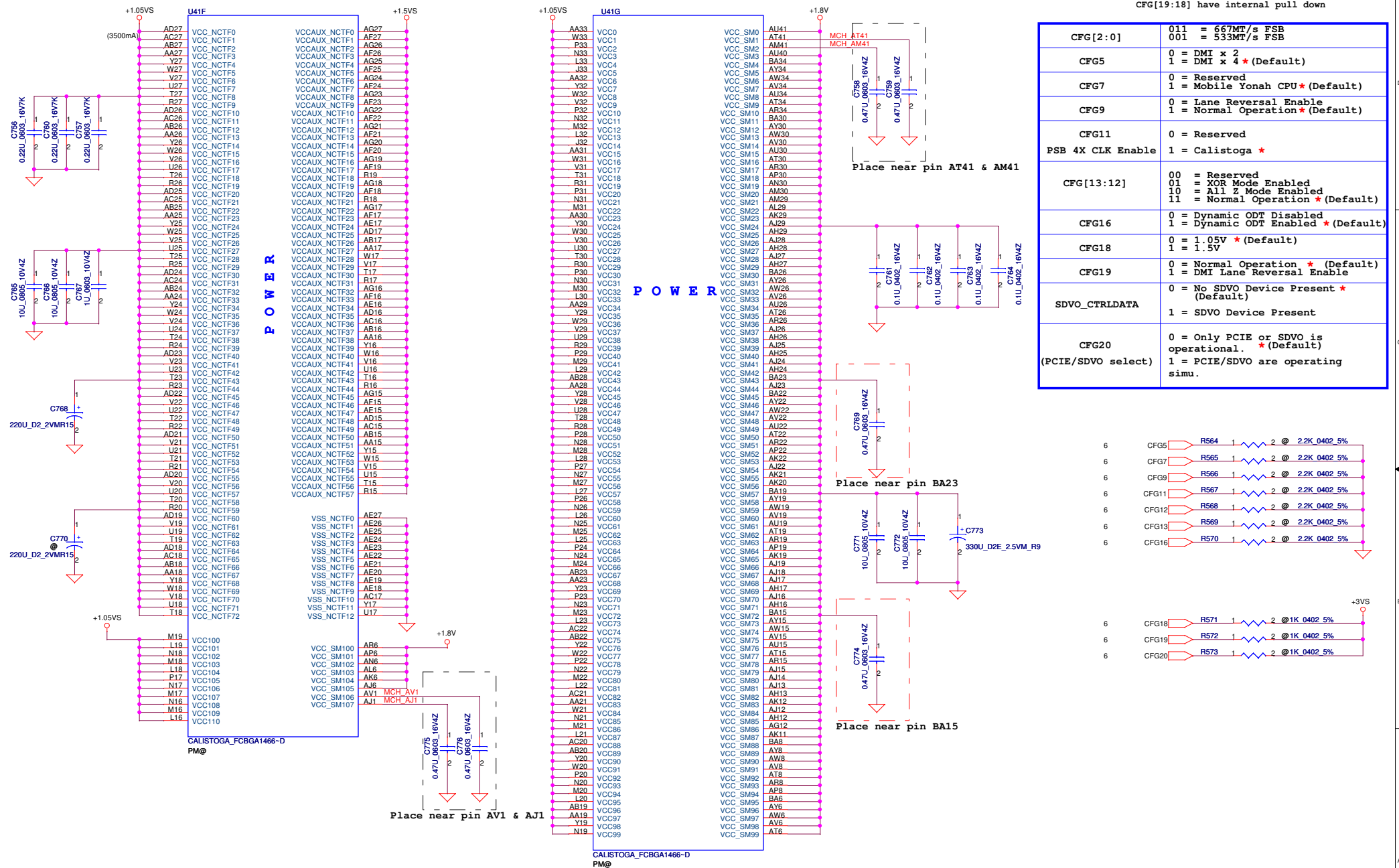


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PM@

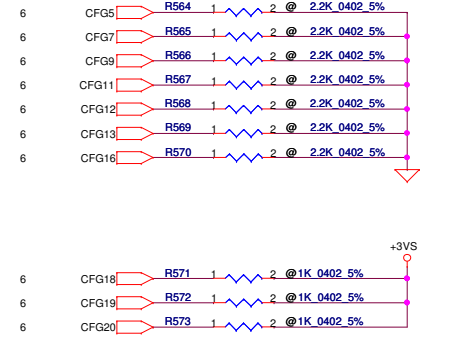
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Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down



CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG18	0 = 1.05V * (Default) 1 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.



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U41I

AC41	VSS0	VSS100	AE34
AA41	VSS01	AC34	AC34
W41	VSS2	VSS102	C34
F41	VSS3	AW33	AW33
P41	VSS4	AV33	AV33
M41	VSS5	AR33	AR33
J41	VSS6	AE33	AE33
F41	VSS7	AB33	AB33
AV40	VSS8	V33	V33
AP40	VSS9	V33	V33
AN40	VSS10	T33	T33
AK40	VSS11	R33	R33
AH40	VSS12	M33	M33
AH40	VSS13	H33	H33
AG40	VSS14	G33	G33
AF40	VSS15	F33	F33
AE40	VSS16	D33	D33
E40	VSS17	B33	B33
AY39	VSS18	AH32	AH32
AW39	VSS19	AG32	AG32
AV39	VSS20	AF32	AF32
AP39	VSS21	AE32	AE32
AN39	VSS22	AC32	AC32
AJ39	VSS23	AB32	AB32
AC39	VSS24	G32	G32
AB39	VSS25	D32	D32
AA39	VSS26	AY31	AY31
Y39	VSS27	AV31	AV31
W39	VSS28	AM31	AM31
V39	VSS29	AJ31	AJ31
T39	VSS30	AG31	AG31
R39	VSS31	AB31	AB31
P39	VSS32	Y31	Y31
N39	VSS33	AE30	AE30
M39	VSS34	E30	E30
L39	VSS35	AT29	AT29
J39	VSS36	AN29	AN29
H39	VSS37	AB29	AB29
G39	VSS38	T29	T29
F39	VSS39	N29	N29
D39	VSS40	K29	K29
AT38	VSS41	G29	G29
AM38	VSS42	E29	E29
AH38	VSS43	C29	C29
AG38	VSS44	B29	B29
AF38	VSS45	A29	A29
AE38	VSS46	BA28	BA28
C38	VSS47	AW28	AW28
AK37	VSS48	AU28	AU28
AH37	VSS49	AP28	AP28
AB37	VSS50	AM28	AM28
AA37	VSS51	AD28	AD28
Y37	VSS52	AC28	AC28
W37	VSS53	H14	H14
V37	VSS54	J28	J28
T37	VSS55	E28	E28
R37	VSS56	AP27	AP27
P37	VSS57	AM27	AM27
N37	VSS58	AK27	AK27
M37	VSS59	AL27	AL27
L37	VSS60	G27	G27
J37	VSS61	F27	F27
H37	VSS62	C27	C27
G37	VSS63	B27	B27
F37	VSS64	AN26	AN26
D37	VSS65	M26	M26
AV36	VSS66	K26	K26
AW36	VSS67	F26	F26
AN36	VSS68	D26	D26
AH36	VSS69	AK25	AK25
AG36	VSS70	P25	P25
AF36	VSS71	H25	H25
AE36	VSS72	K25	K25
AC36	VSS73	E25	E25
C36	VSS74	D25	D25
B36	VSS75	A25	A25
BA35	VSS76	BA24	BA24
AV35	VSS77	AU24	AU24
AR35	VSS78	AL24	AL24
AH35	VSS79	AW23	AW23
AB35	VSS80	AT23	AT23
AA35	VSS81	AN23	AN23
Y35	VSS82	AM23	AM23
W35	VSS83	AH23	AH23
V35	VSS84	AC23	AC23
T35	VSS85	W23	W23
R35	VSS86	K23	K23
P35	VSS87	J23	J23
N35	VSS88	F23	F23
M35	VSS89	C23	C23
L35	VSS90	AA22	AA22
J35	VSS91	K22	K22
H35	VSS92	G22	G22
G35	VSS93	F22	F22
F35	VSS94	E22	E22
D35	VSS95	D22	D22
AN34	VSS96	A22	A22
AK34	VSS97	BA21	BA21
AG34	VSS98	AV21	AV21
AF34	VSS99	AR21	AR21

CALISTOGA_FCBGA1466-D
PM@

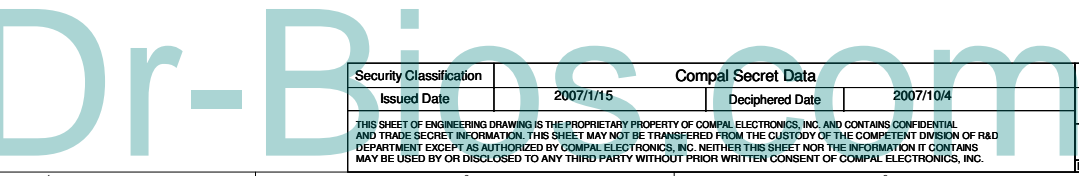
POWER

U41J

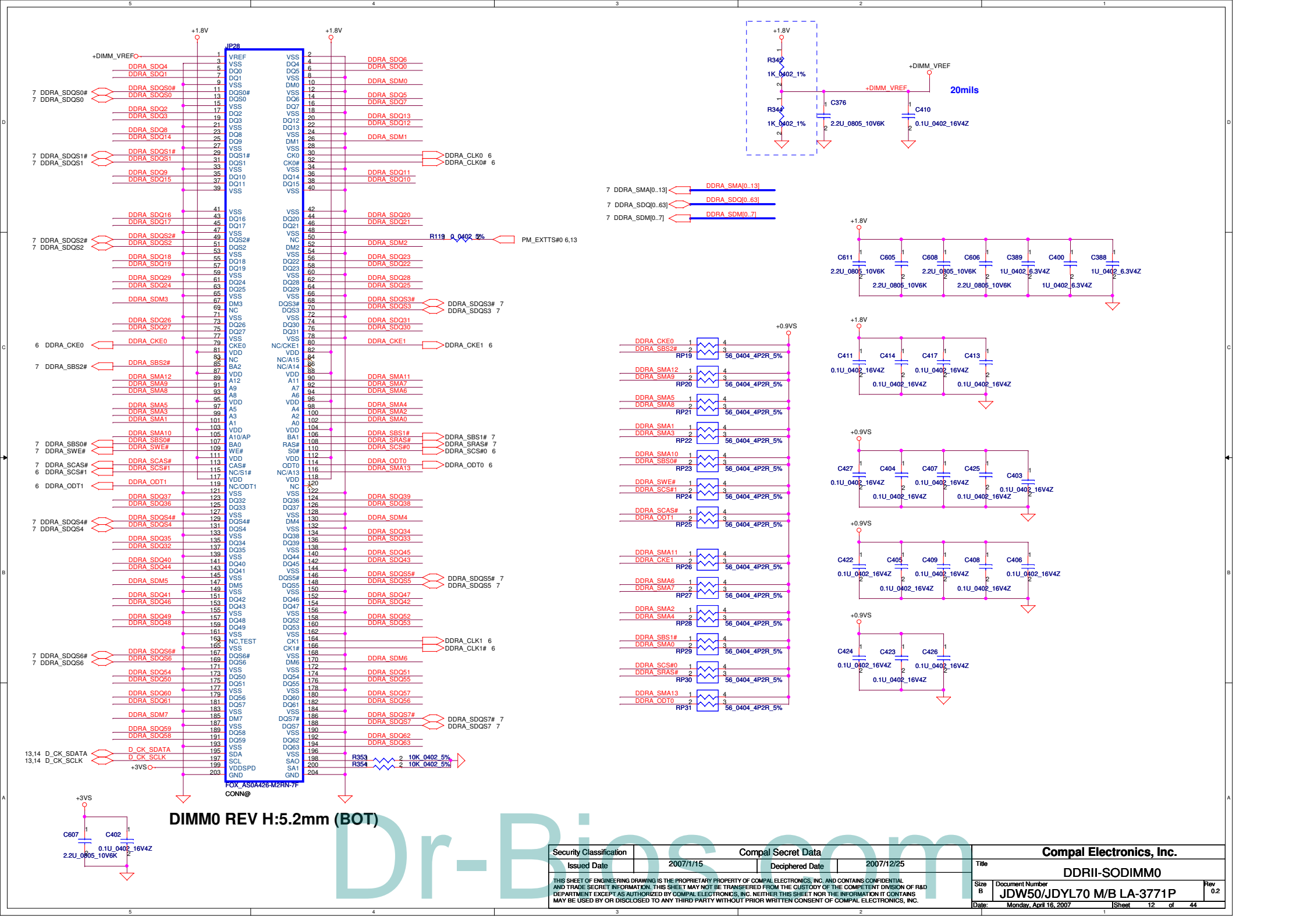
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AL21	VSS201	VSS281	AC10
AB21	VSS202	VSS282	W10
Y21	VSS203	VSS283	U10
P21	VSS204	VSS284	BA9
K21	VSS205	VSS285	AW9
J21	VSS206	VSS286	AR9
H21	VSS207	VSS287	AH9
C21	VSS208	VSS288	AB9
AW20	VSS209	VSS289	Y9
AR20	VSS210	VSS290	R9
AM20	VSS211	VSS292	G9
AK20	VSS212	VSS291	E9
K20	VSS213	VSS291	A9
B20	VSS214	VSS293	AG8
A20	VSS215	VSS294	AG8
AN19	VSS216	VSS295	AD8
AC19	VSS217	VSS296	AA8
W19	VSS218	VSS297	U8
K19	VSS219	VSS297	K8
G19	VSS220	VSS299	C8
P19	VSS221	VSS300	BA7
AH18	VSS222	VSS301	AV7
P18	VSS223	VSS302	AP7
H18	VSS224	VSS303	AL7
D18	VSS225	VSS304	AJ7
A18	VSS226	VSS305	AH7
AY17	VSS227	VSS306	AF7
AM17	VSS228	VSS307	AC7
AK17	VSS229	VSS308	R7
AV16	VSS230	VSS309	C7
AN16	VSS231	VSS310	D7
AC16	VSS232	VSS311	AG6
J16	VSS233	VSS312	AD6
F16	VSS234	VSS313	Y6
C16	VSS235	VSS314	U6
AM15	VSS236	VSS315	N6
AK15	VSS237	VSS316	K6
N15	VSS238	VSS317	H6
M15	VSS239	VSS318	B6
L15	VSS240	VSS319	AV5
B15	VSS241	VSS320	AE5
A15	VSS242	VSS321	AD5
BA14	VSS243	VSS322	AY4
AT14	VSS244	VSS323	AY4
AK14	VSS245	VSS324	AR4
AD14	VSS246	VSS325	AP4
AM14	VSS247	VSS326	AL4
K14	VSS248	VSS327	Y4
H14	VSS249	VSS328	U4
E14	VSS250	VSS329	J4
AV13	VSS251	VSS330	F4
AR13	VSS252	VSS331	C4
AN13	VSS253	VSS332	AY3
AM13	VSS254	VSS333	AW3
AL13	VSS255	VSS334	AV3
AG13	VSS256	VSS335	AL3
P13	VSS257	VSS336	AH3
F13	VSS258	VSS337	AG3
D13	VSS259	VSS338	AF3
B13	VSS260	VSS339	AD3
AY12	VSS261	VSS340	AC3
AC12	VSS262	VSS341	AA3
F26	VSS263	VSS342	G3
H12	VSS264	VSS343	AT2
E12	VSS265	VSS344	AR2
AD11	VSS266	VSS345	AP2
AK11	VSS267	VSS346	AK2
Y11	VSS268	VSS347	AJ2
J11	VSS269	VSS348	AJ2
D11	VSS270	VSS349	AD2
A21	VSS271	VSS350	AB2
AV10	VSS272	VSS351	Y2
AP10	VSS273	VSS352	U2
AL10	VSS274	VSS353	T2
AJ10	VSS275	VSS354	N2
	VSS276	VSS355	J2
	VSS277	VSS356	H2
	VSS278	VSS357	F2
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		VSS359	AL1
		VSS360	

CALISTOGA_FCBGA1466-D
PM@

POWER

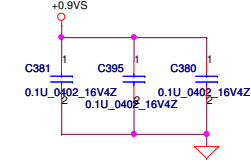
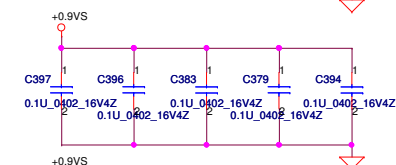
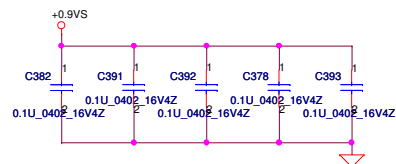
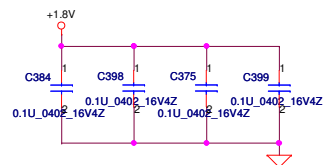
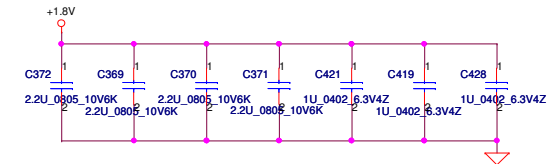
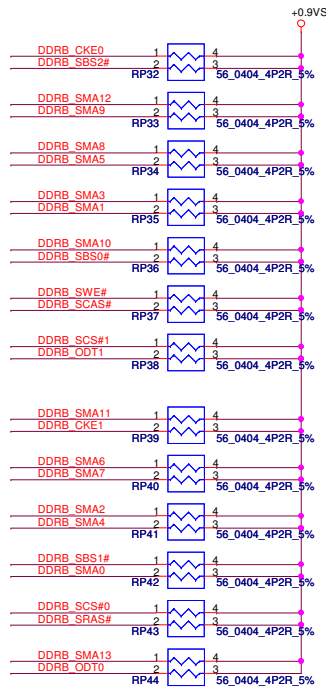
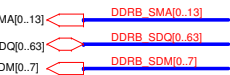
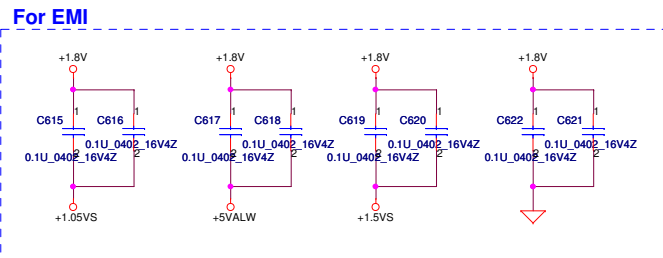
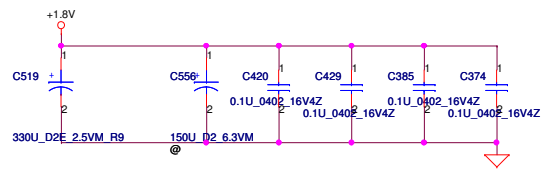
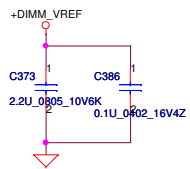
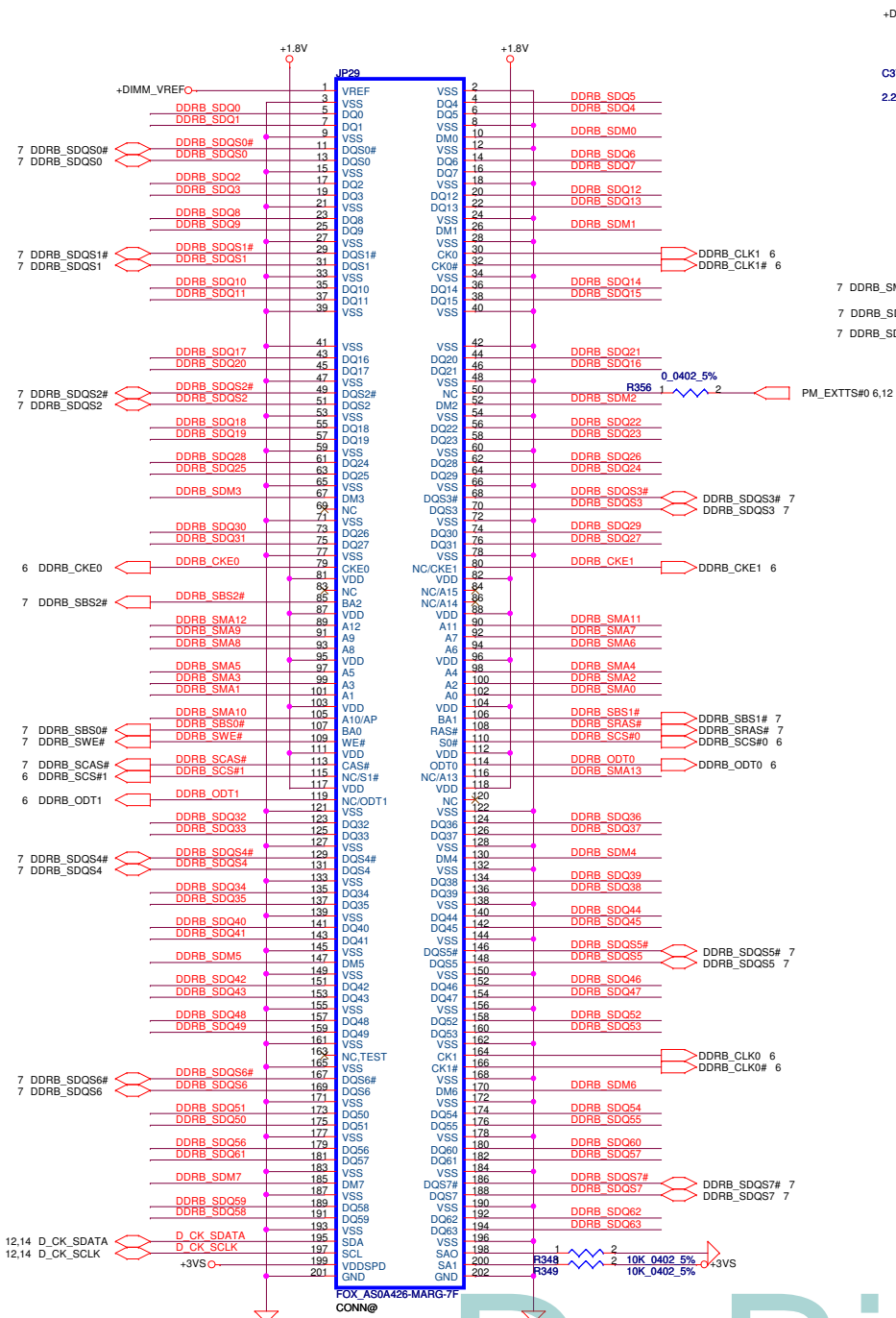


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				Date: Monday, April 16, 2007	Sheet 11 of 44



DIMM0 REV H:5.2mm (BOT)

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DIMM1 REV H:9.2mm (BOT)

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Compal Electronics, Inc.		
DDRII-SODIMM1		
Size B	Document Number	Rev
	JDW50/JDYL70 M/B LA-3771P	0.2
Date:	Monday, April 16, 2007	Sheet 13 of 44

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz_1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

**SEL_24M/PCICLK2=0=TESTMODE
**SEL_PCI6/PCICLK1=0=CLKREQ5#

**SEL_PCI5=1=PCICLK5

ITP_EN/PCICLK_F0=0=SRC pair

CLK_REF

CLK_PCIO

CLK_PCI4

CLK_ENABLE# R

D CK SCLK

D CK SDATA

D CK SCLK

D CK SDATA

D CK SCLK

D CK SDATA

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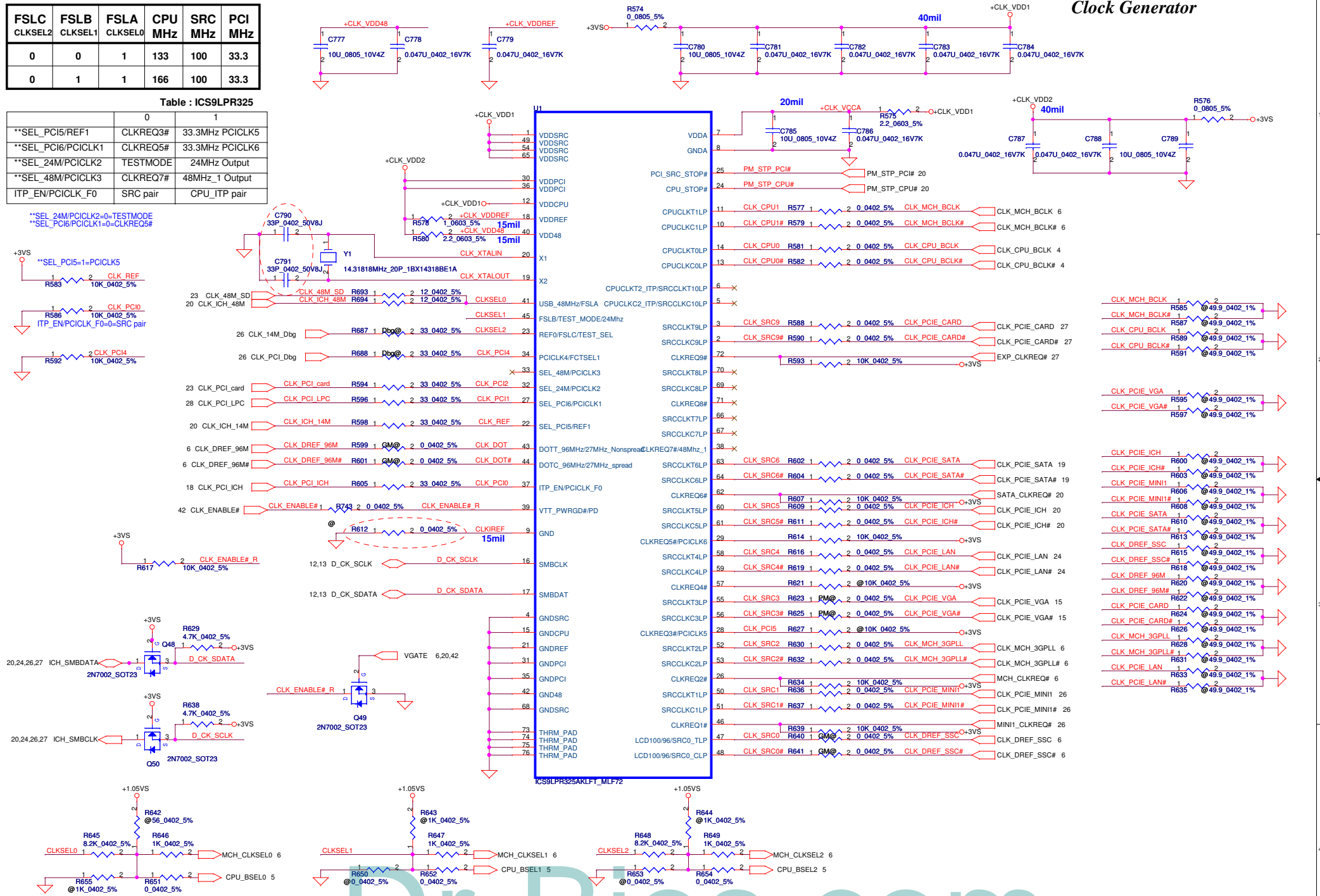
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D CK SDATA

D CK SCLK

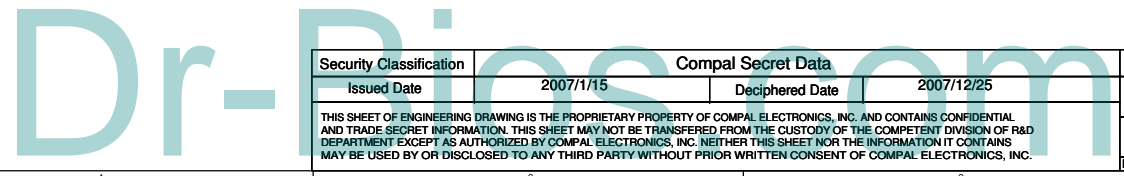
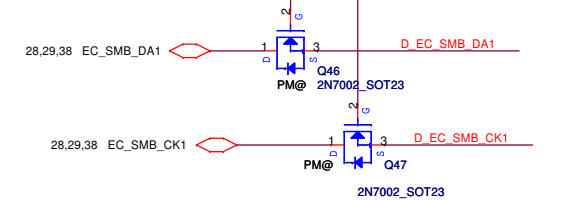
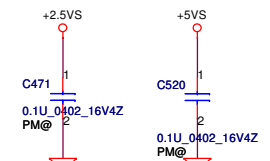
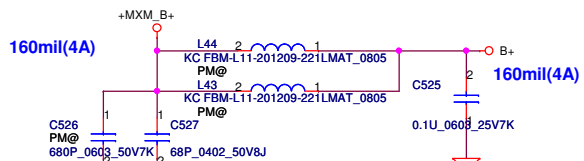
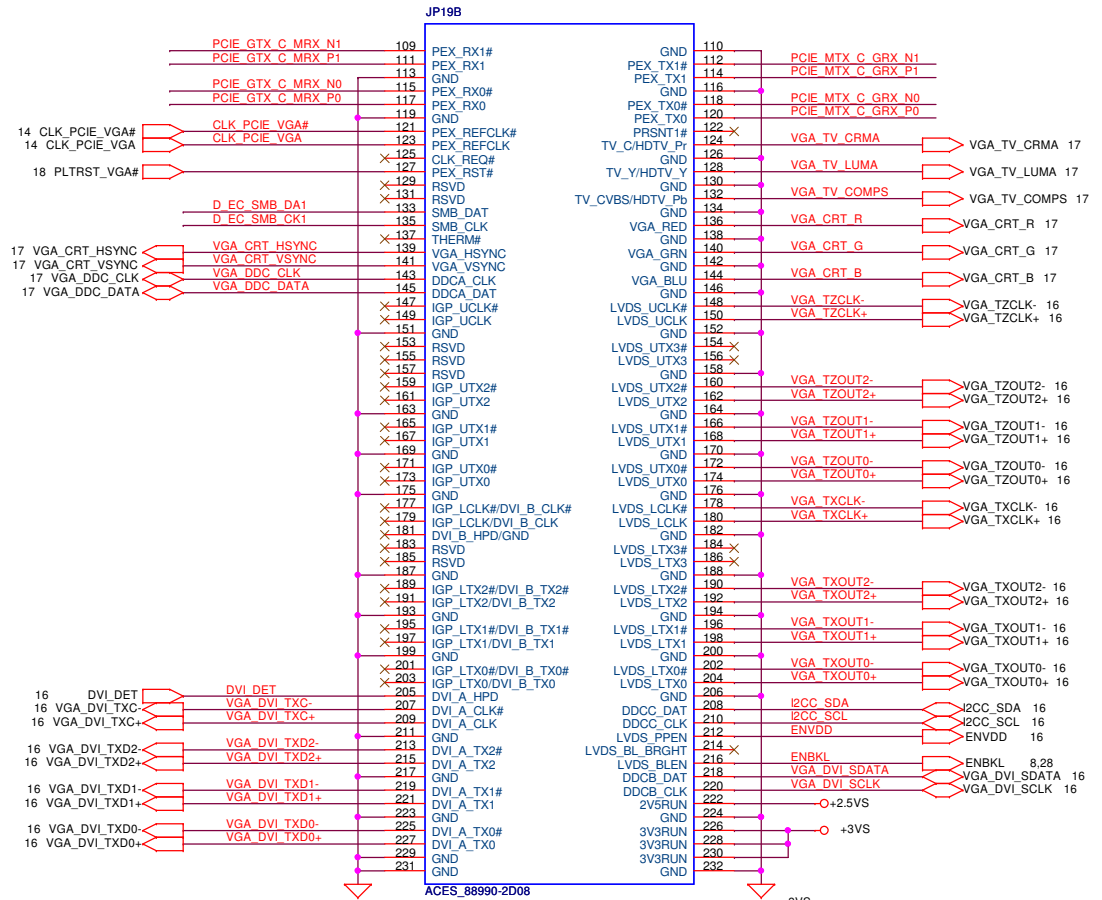
D CK SDATA

Clock Generator



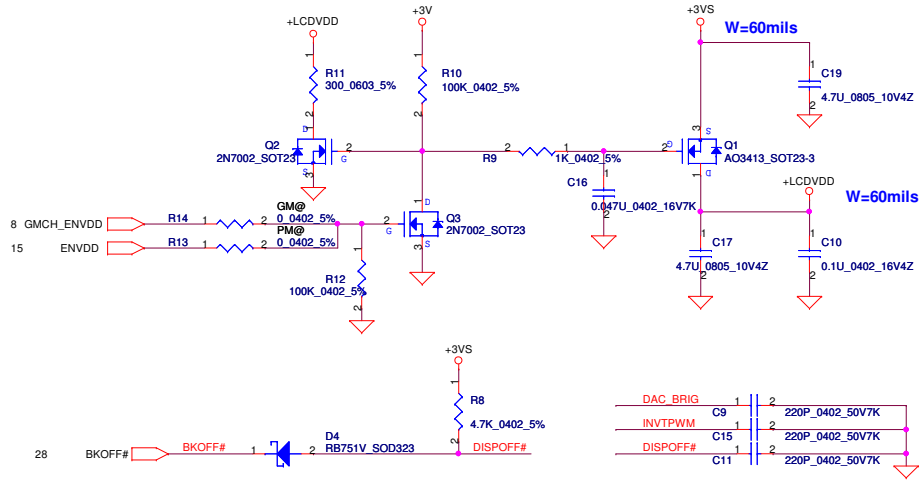
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- 8 PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15]
- 8 PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15]
- 8 PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]
- 8 PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]

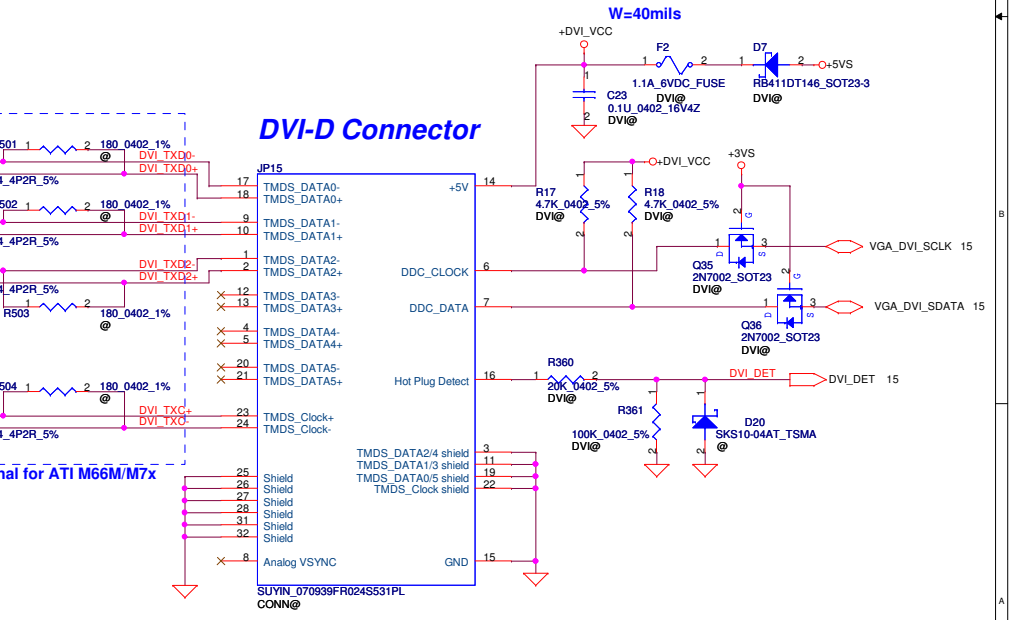
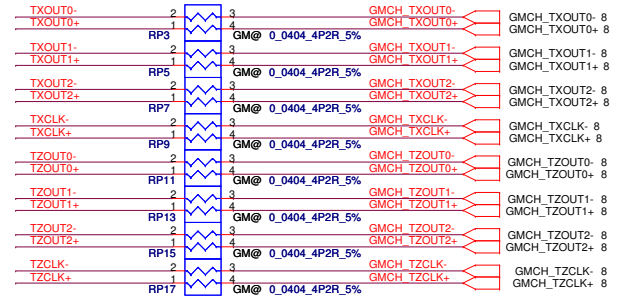
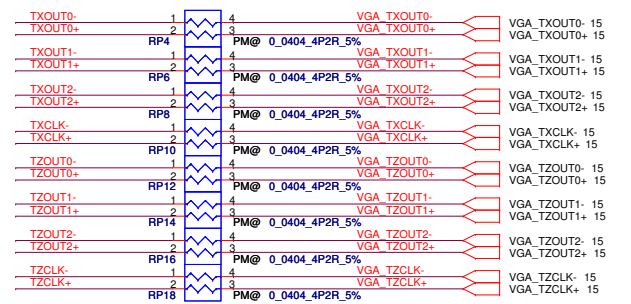
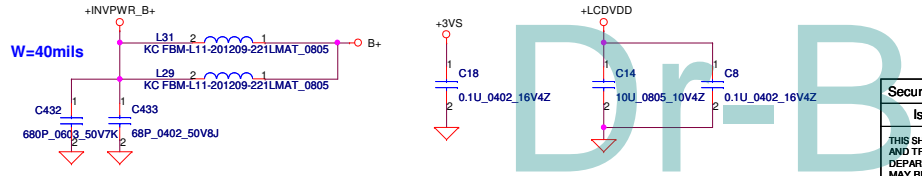
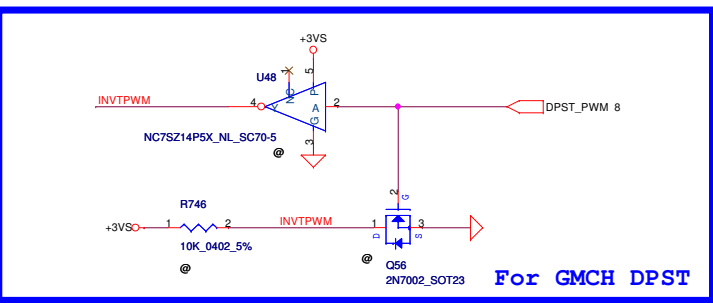
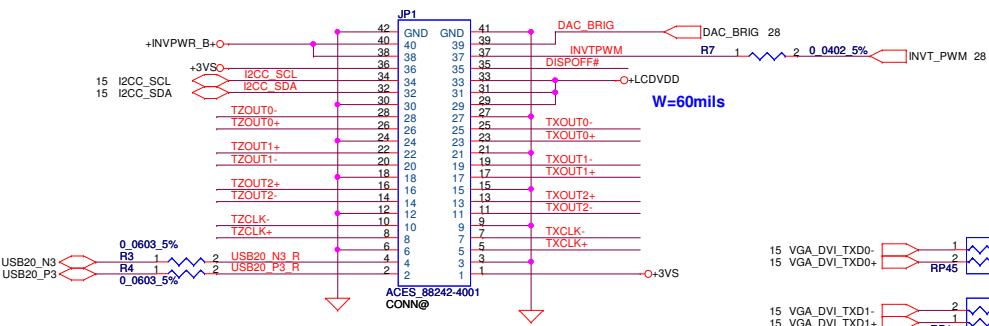


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Size B	Document Number	Date		Rev	0.2
	JDW50/JDYL70 M/B LA-3771P	Monday, April 16, 2007		Sheet	15 of 44

LCD POWER CIRCUIT

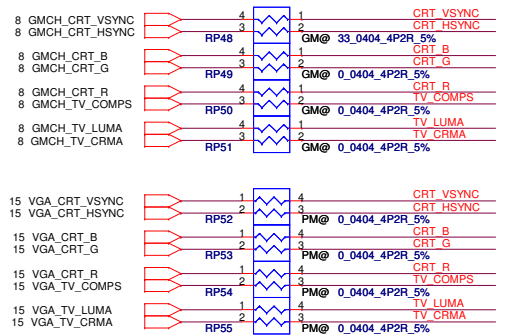
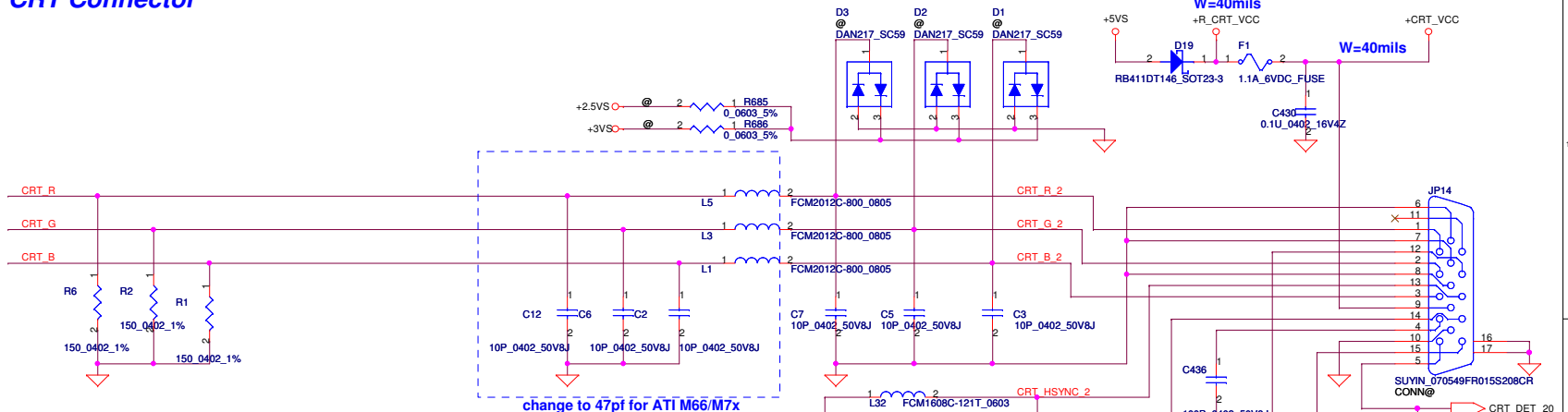


LCD/PANEL BD. Conn.



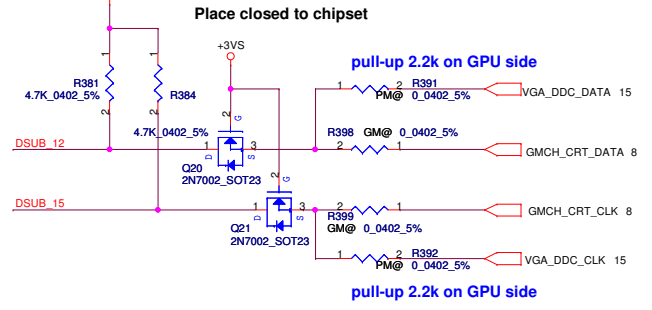
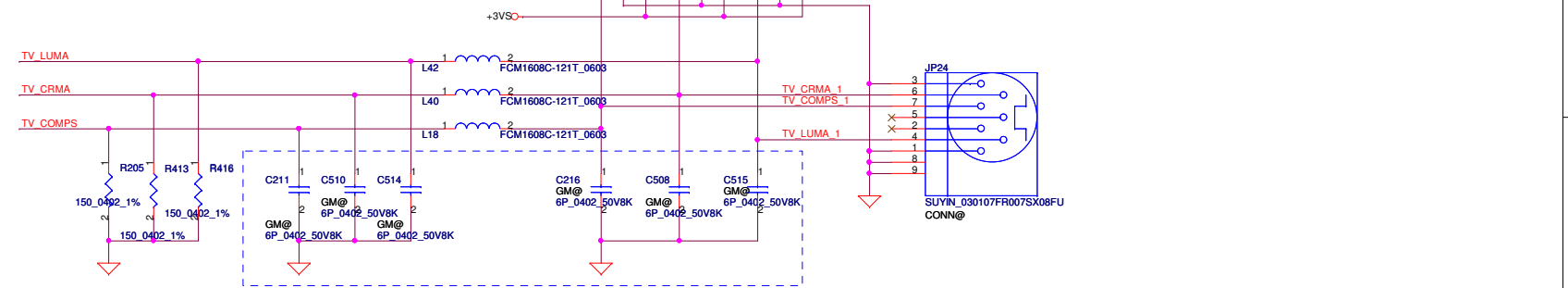
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Issued Date	2007/1/15	Deciphered Date	2007/12/25	LVDS & DVI Connector	
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Size B	Document Number	Date:		Sheet	Rev
	JDW50/JDYL70 M/B LA-3771P	Mondar, April 16, 2007		16	0.2

CRT Connector



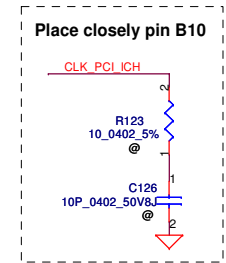
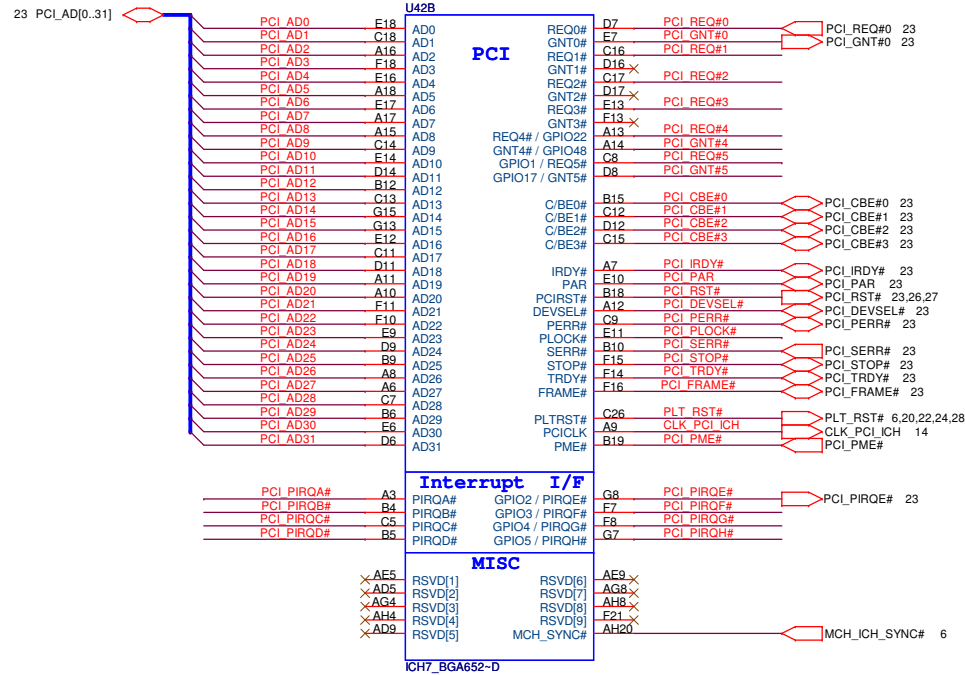
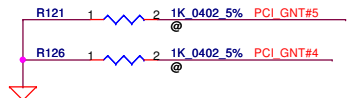
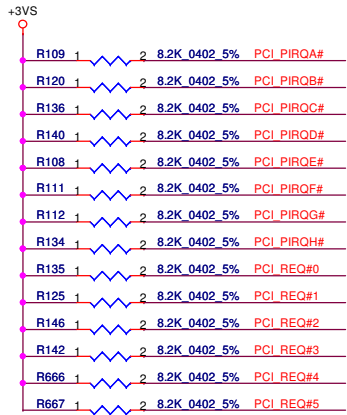
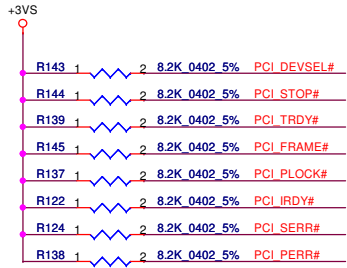
Place closed to chipset

TV-OUT Conn.

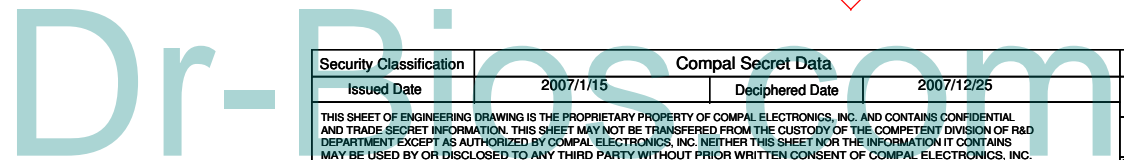
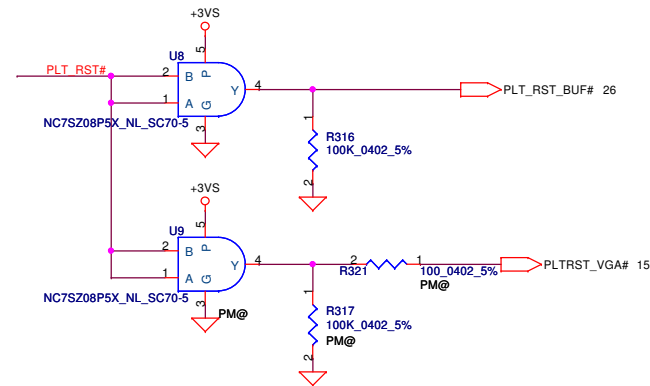


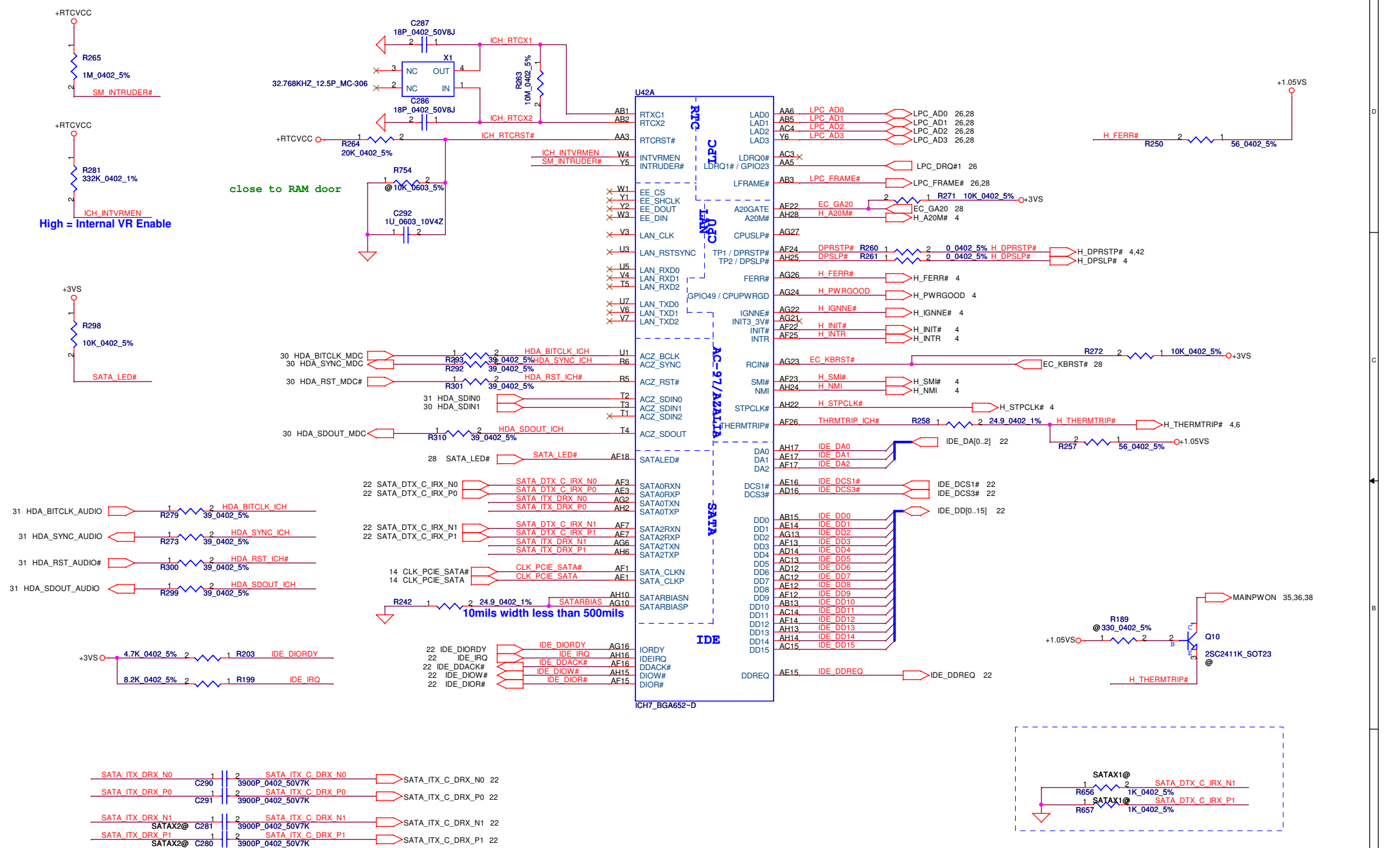
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CRT & TV-OUT Connector		
Size B	Document Number	Rev
	JDW50/JDYL70 M/B LA-3771P	0.2
Date:	Monday, April 16, 2007	Sheet 17 of 44



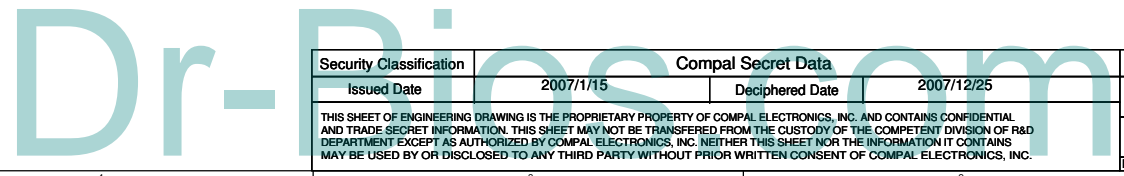
Boot BIOS Strap		
PCI_GNT#5	PCI_GNT#4	Boot BIOS Location
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1	0	PCI
1	1	LPC*



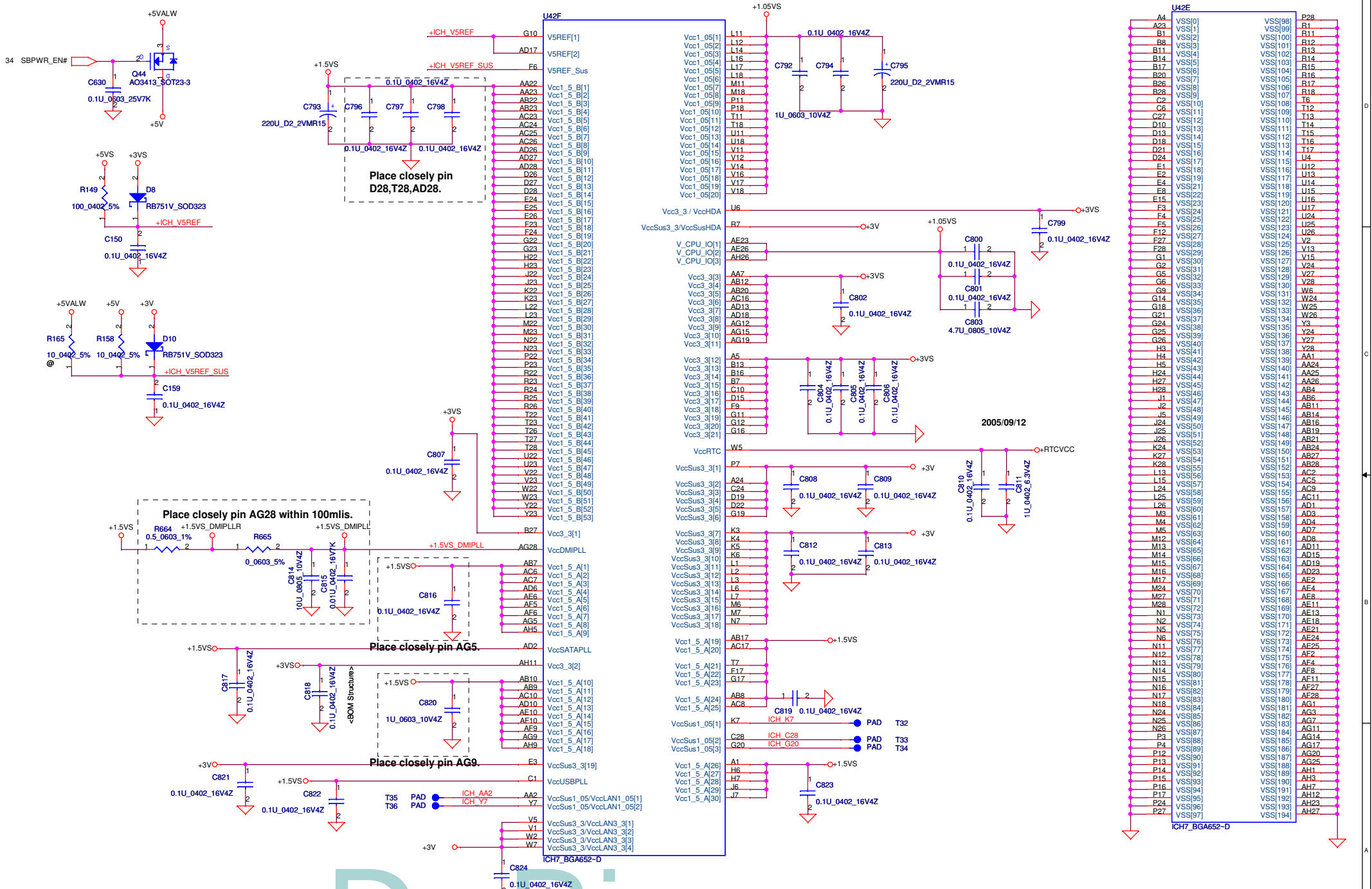


close ICH8

SATA_RXn/p need tie to ground when SATA port not used

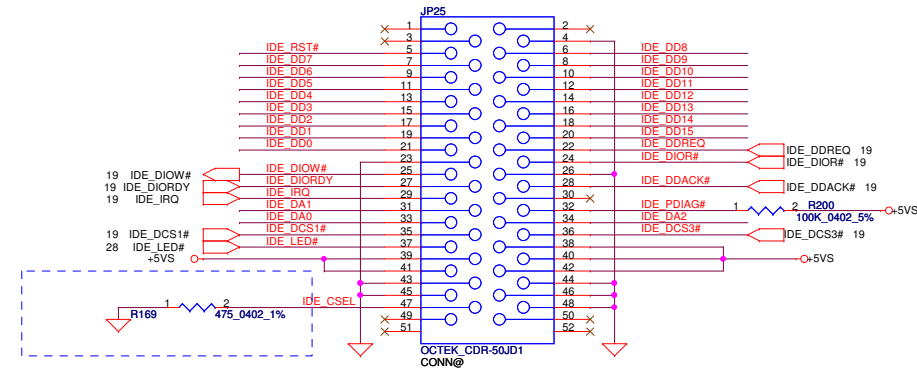
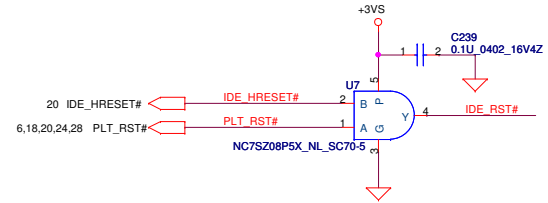
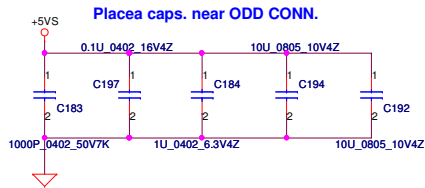


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Size B	Document Number	Date:		Rev	0.2
	JDW50/JDYL70 M/B LA-3771P	Monday, April 16, 2007		Sheet	19 of 44

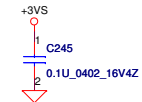
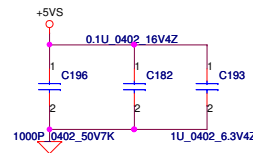
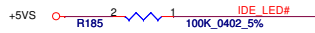


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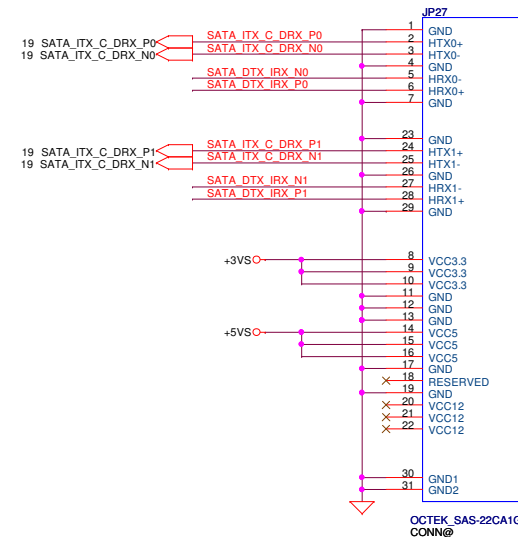
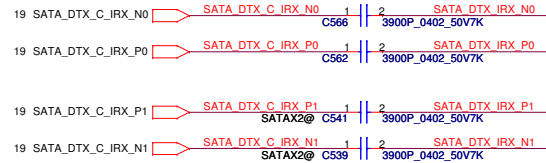
Compal Electronics, Inc.			
Title ICH7M(4)-POWER&GND			
Size	Document Number	Rev	
Custom	JDW50/JDYL70 M/B LA-3711P	0.2	
Date:	Monday, April 16, 2007	Sheet	21 of 44



IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

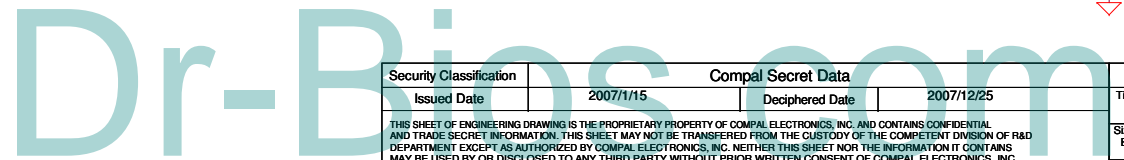


SATA HDD Conn.(SAS Connector)



First HDD for 15.4"

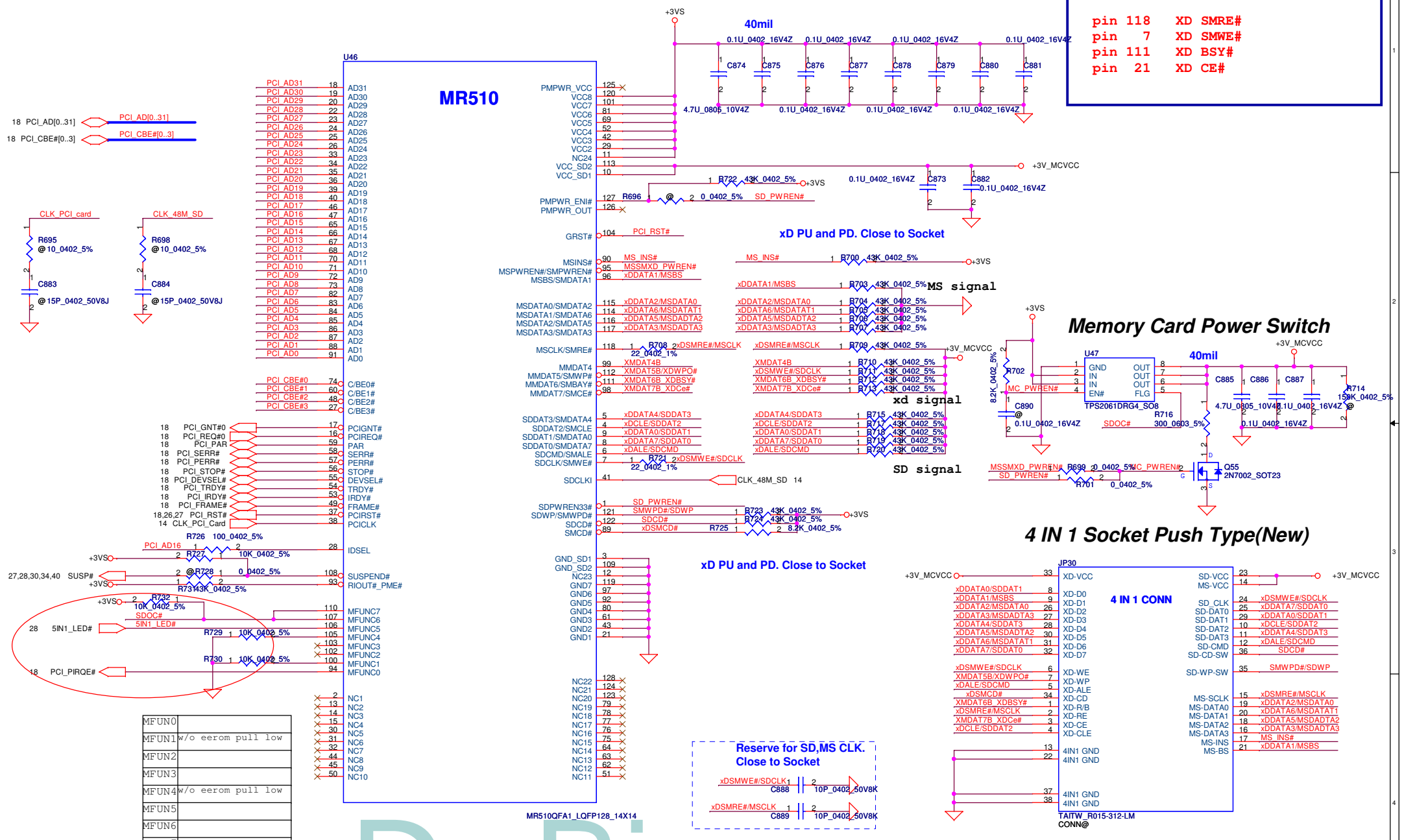
2nd HDD for 17"



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Issued Date	2007/1/15	Deciphered Date	2007/12/25	HDD & ODD Connector	
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				JDW50/JDYL70 M/B LA-3771P	Rev 0.2
				Date: Monday, April 16, 2007	Sheet 22 of 44

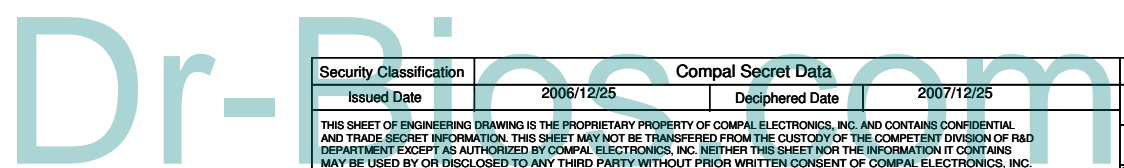
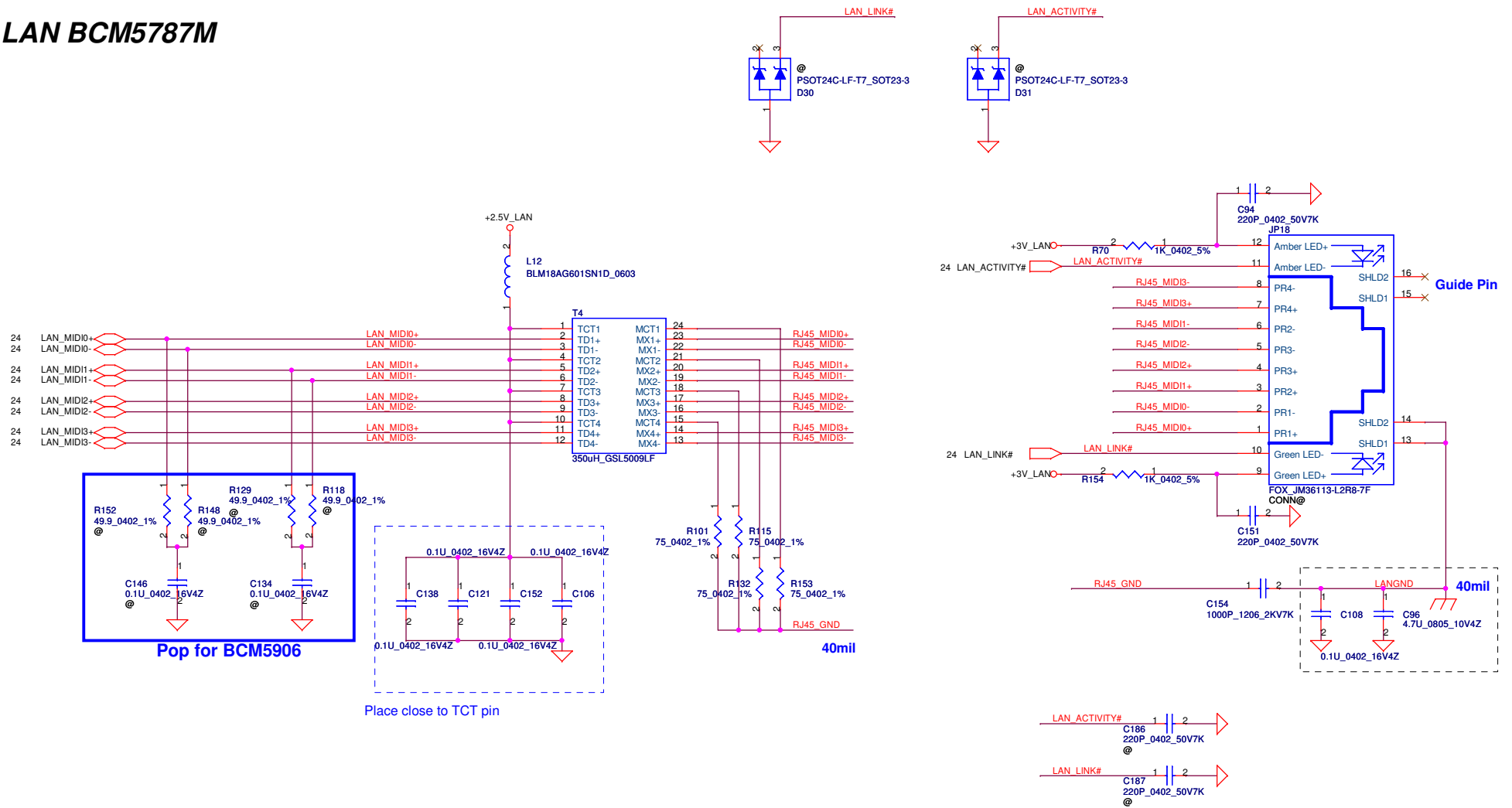
PS: only below need to pull high
others have internal Pull high

pin 118 XD SMRE#
pin 7 XD SMWE#
pin 111 XD BSY#
pin 21 XD CE#



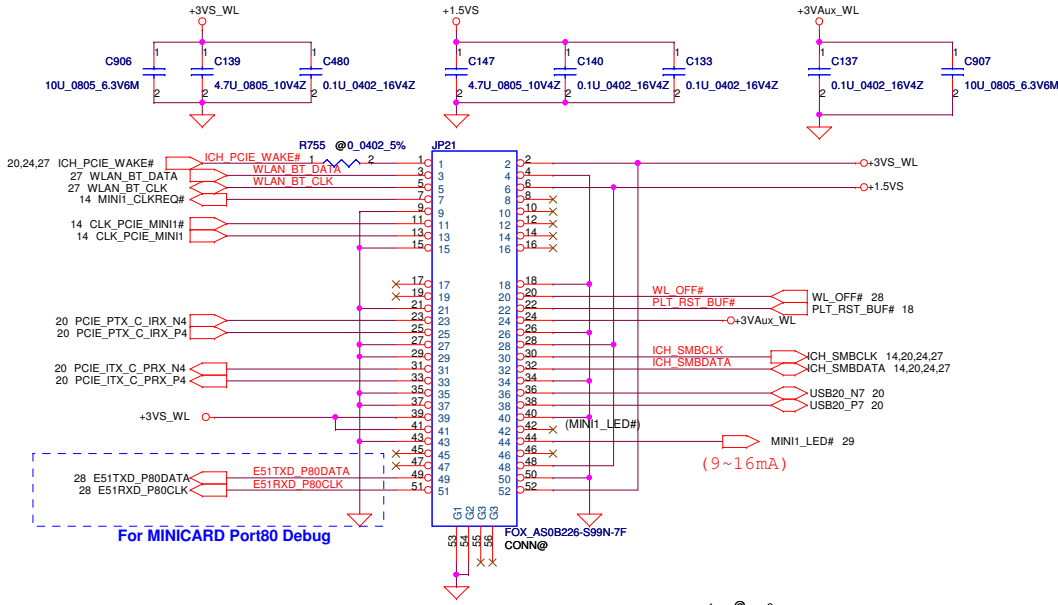
18	PCI_AD[0..31]	PCI AD[0..31]
18	PCI_CBE#[0..3]	PCI CBE#[0..3]
18	CLK_PCI_card	CLK PCI_card
18	CLK_48M_SD	CLK 48M_SD
18	PCI_GNT#	PCI GNT#
18	PCI_REQ#	PCI REQ#
18	PCI_PAR	PCI PAR
18	PCI_SERR#	PCI SERR#
18	PCI_PERR#	PCI PERR#
18	PCI_DEVSEL#	PCI DEVSEL#
18	PCI_TRDY#	PCI TRDY#
18	PCI_IRDY#	PCI IRDY#
18	PCI_FRAME#	PCI FRAME#
18,26,27	PCI_RST#	PCI RST#
14	CLK_PCI_Card	CLK PCI_Card
28	SUSP#	SUSPEND#
28,30,34,40	SUSP#	SUSPEND#
28	5IN1_LED#	5IN1_LED#
18	PCI_PIRQE#	PCI PIRQE#
110	MFUNC7	MFUNC7
107	MFUNC6	MFUNC6
106	MFUNC5	MFUNC5
103	MFUNC4	MFUNC4
102	MFUNC3	MFUNC3
100	MFUNC2	MFUNC2
94	MFUNC1	MFUNC1
94	MFUNC0	MFUNC0

LAN BCM5787M



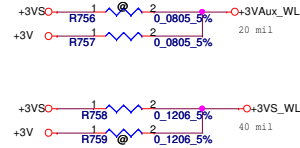
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/12/25	Deciphered Date	2007/12/25	Title	
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Size B	Document Number	JDW50/JDYL70 M/B LA-3771P		Rev	0.2
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For Wireless LAN

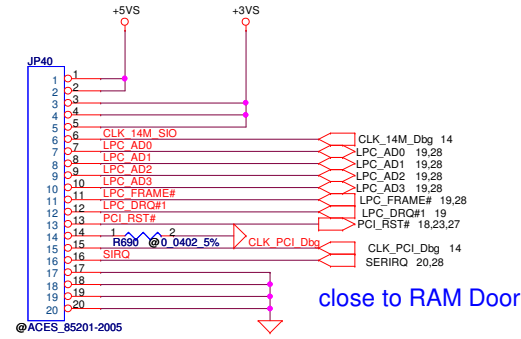


For MINICARD Port80 Debug

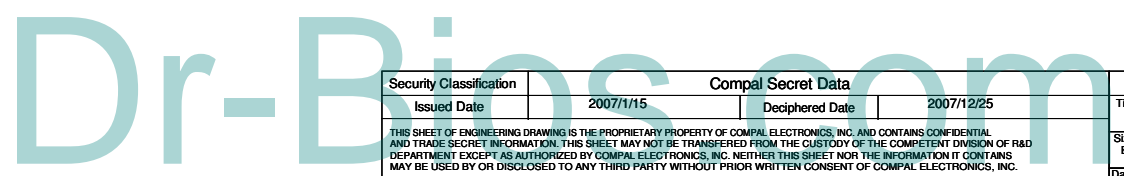
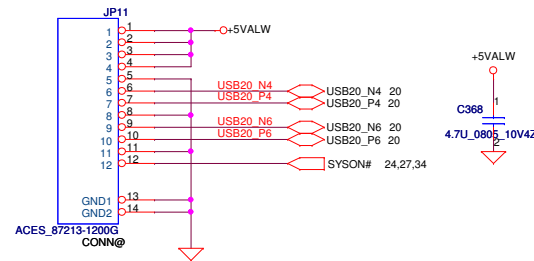
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



LPC Debug Port

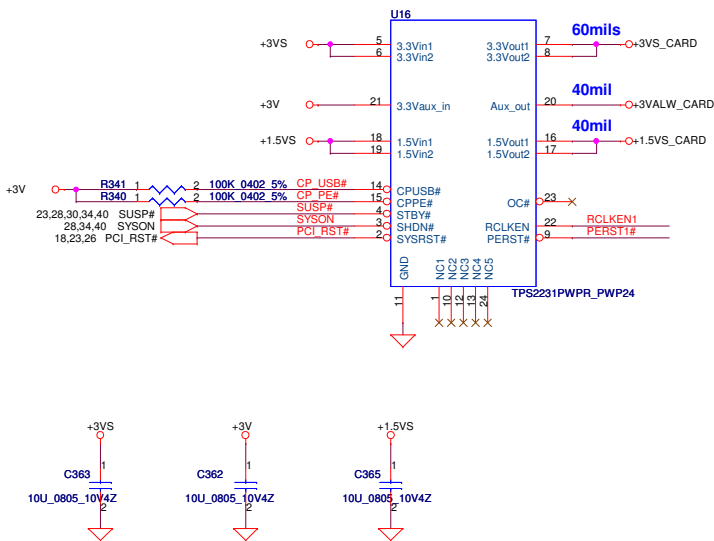


To USB/B Connector

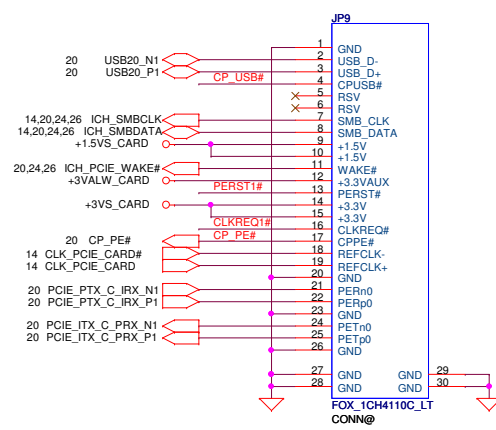


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Issued Date	2007/1/15	Document Number	
Deciphered Date	2007/12/25	MINI CARD (WLAN & TV-Tuner)	
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New Card Power Switch

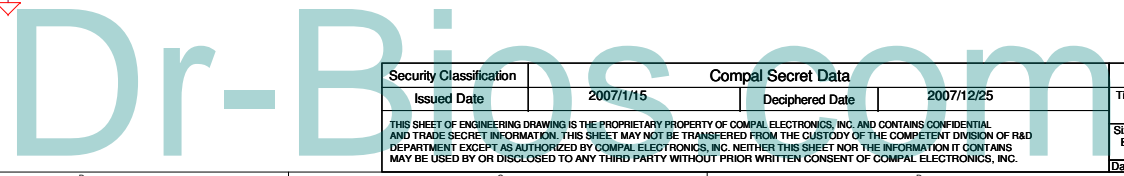
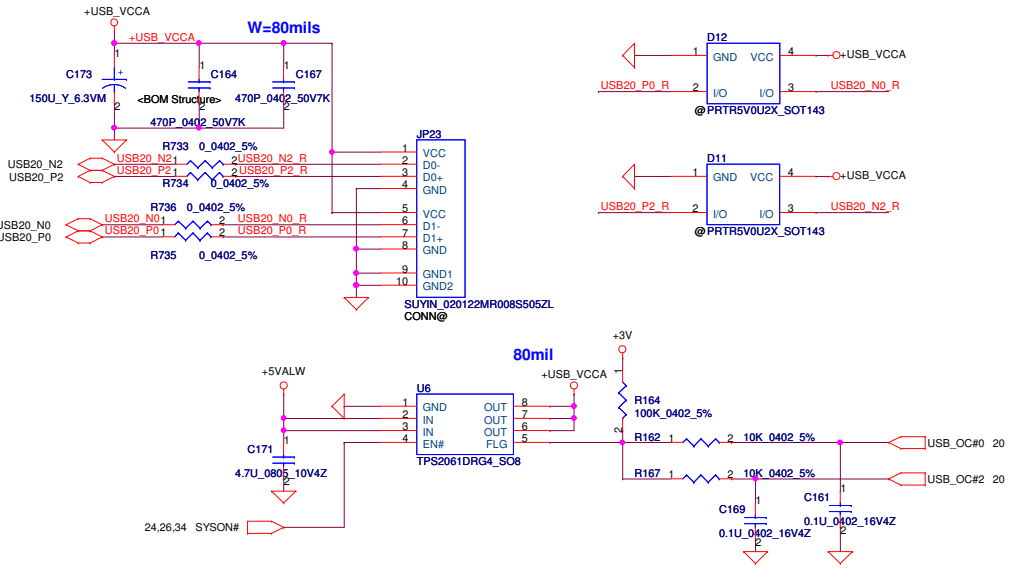
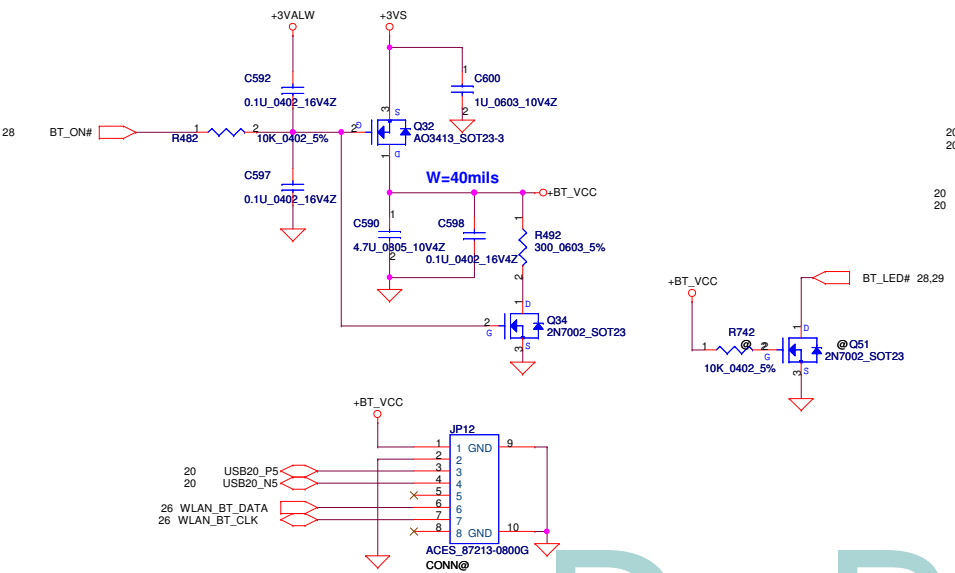


New Card Socket (Left/TOP)

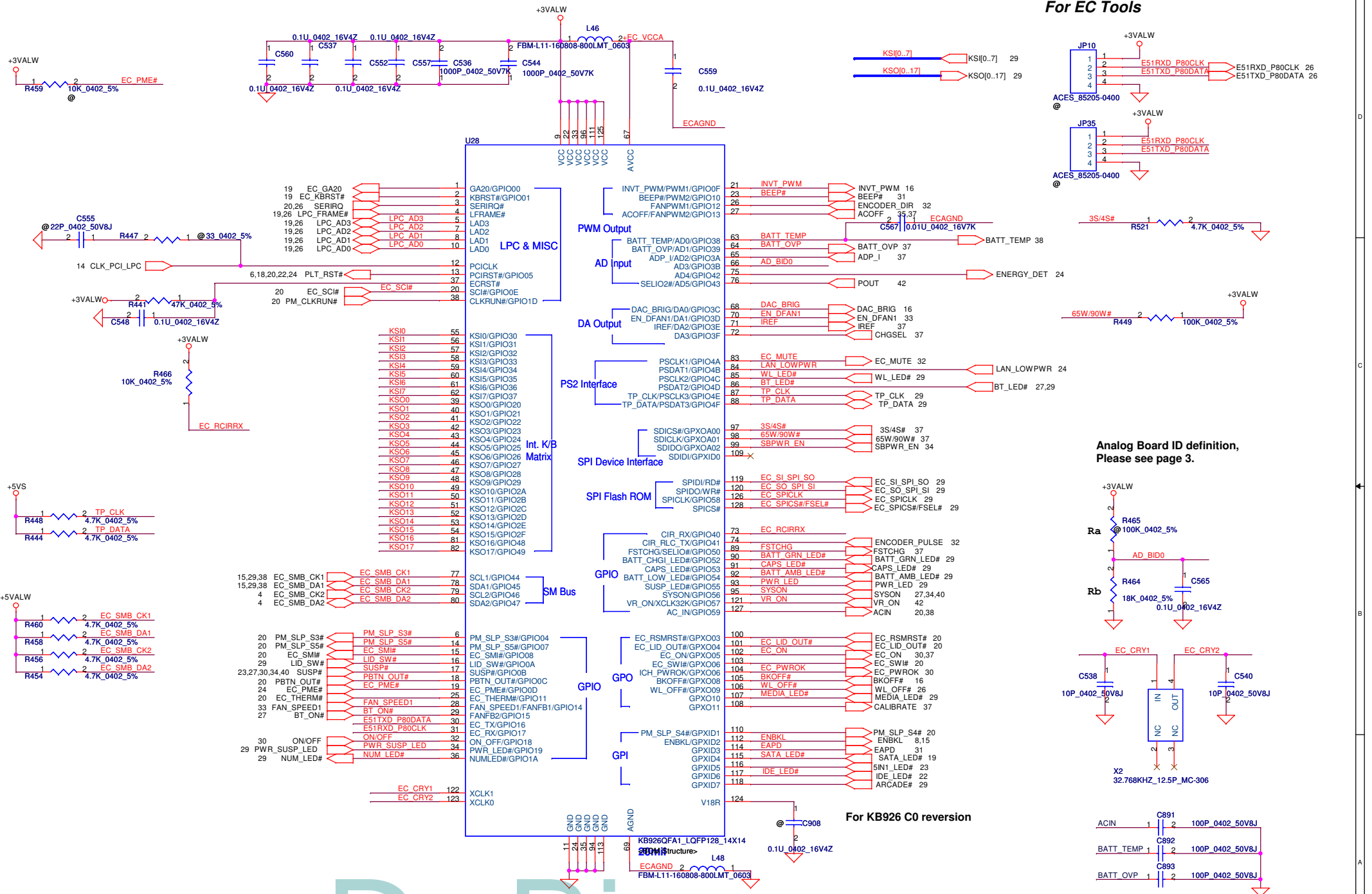


USB CONN. (Stack-up Type)

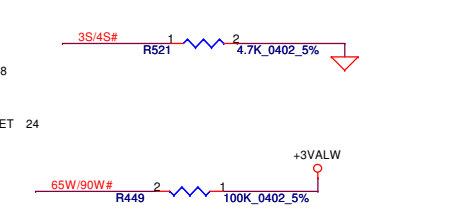
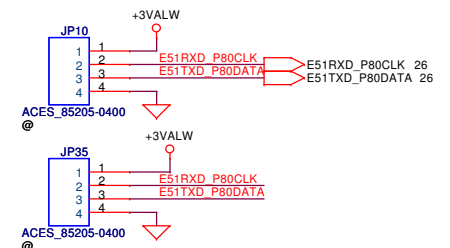
Bluetooth Conn.



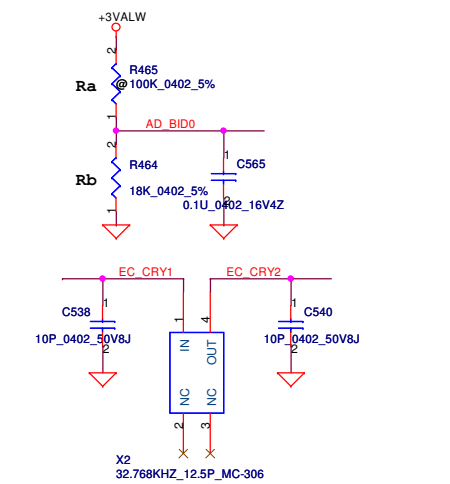
Security Classification	Compal Secret Data	Title	
Issued Date	2007/1/15	NEW CARD & USB Connector	
Deciphered Date	2007/12/25	Size	Document Number
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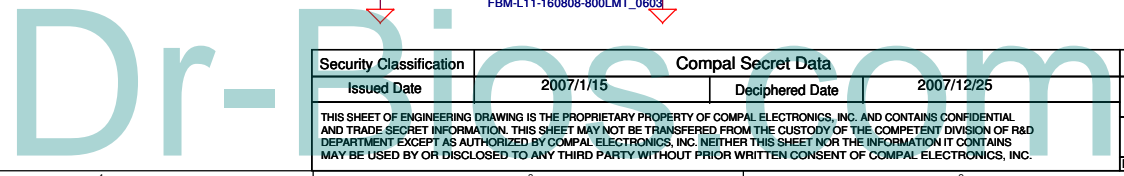
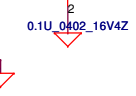
For EC Tools



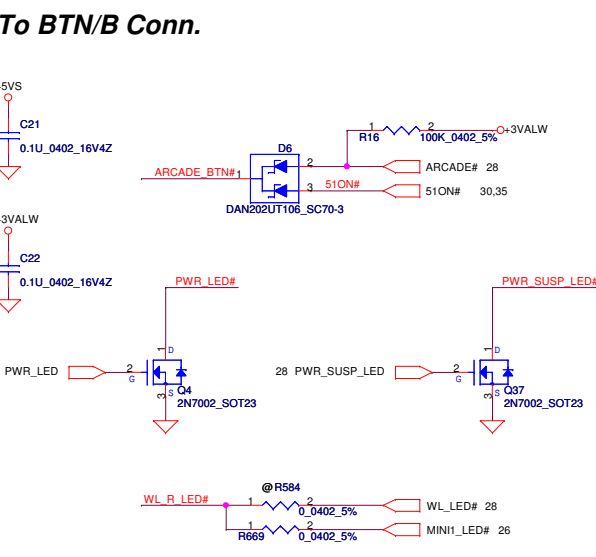
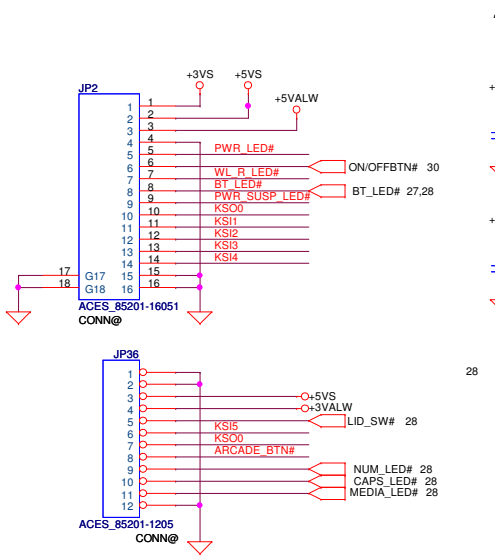
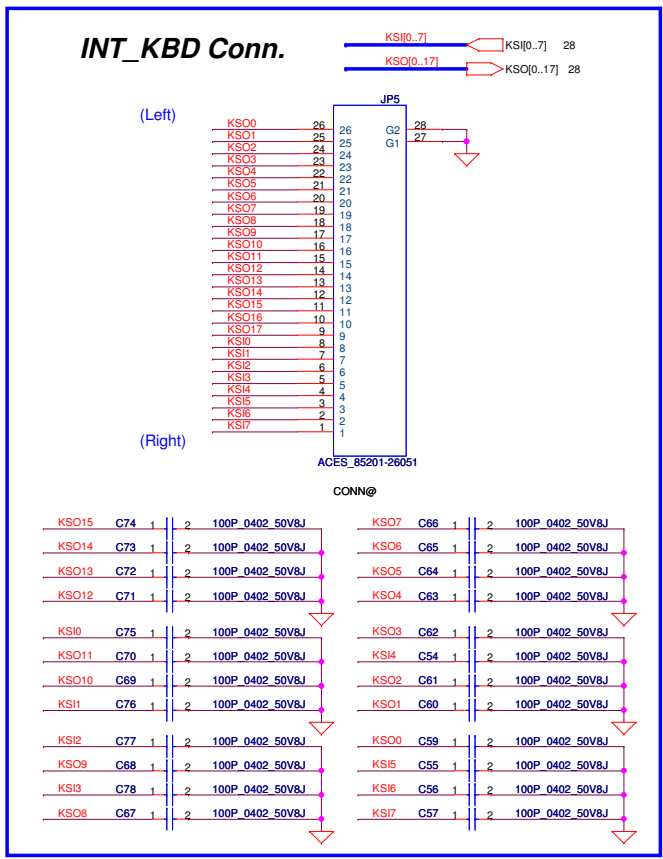
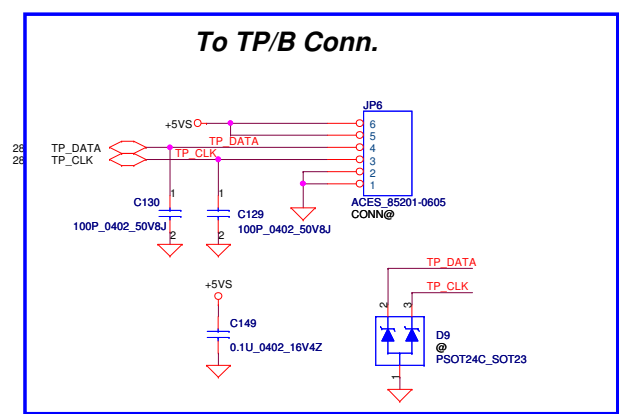
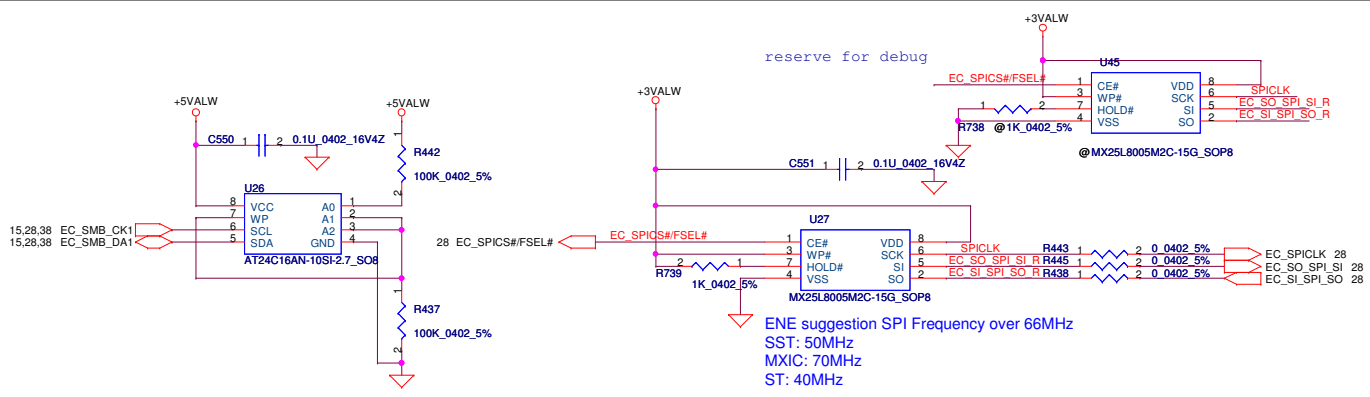
Analog Board ID definition, Please see page 3.



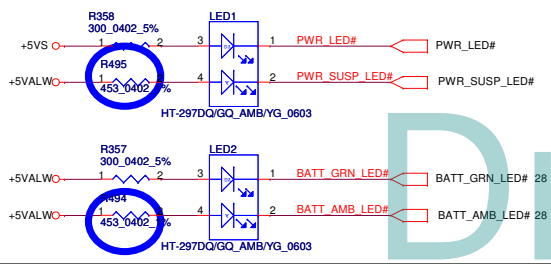
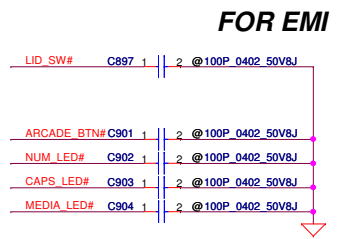
For KB926 C0 reversion



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Size B	Document Number	Date		Rev	
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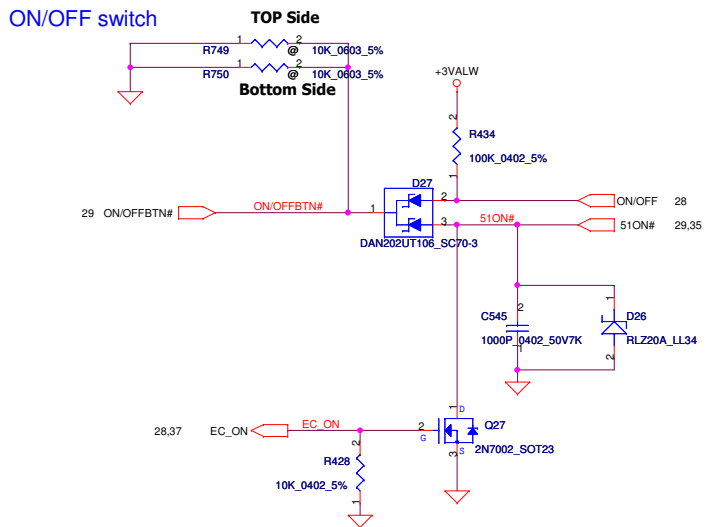


	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

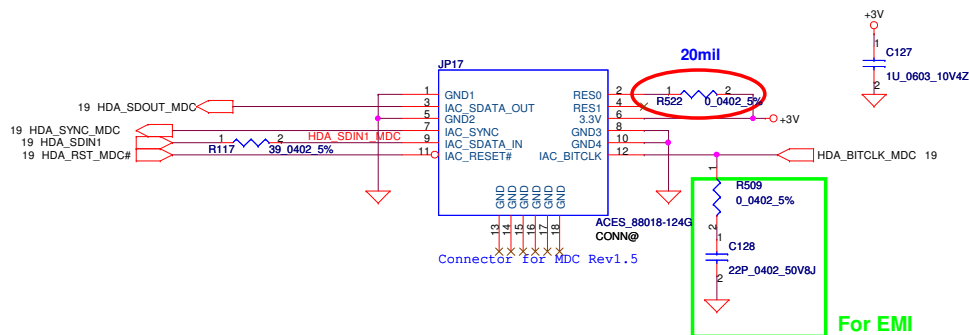


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Size	Document Number			Rev	
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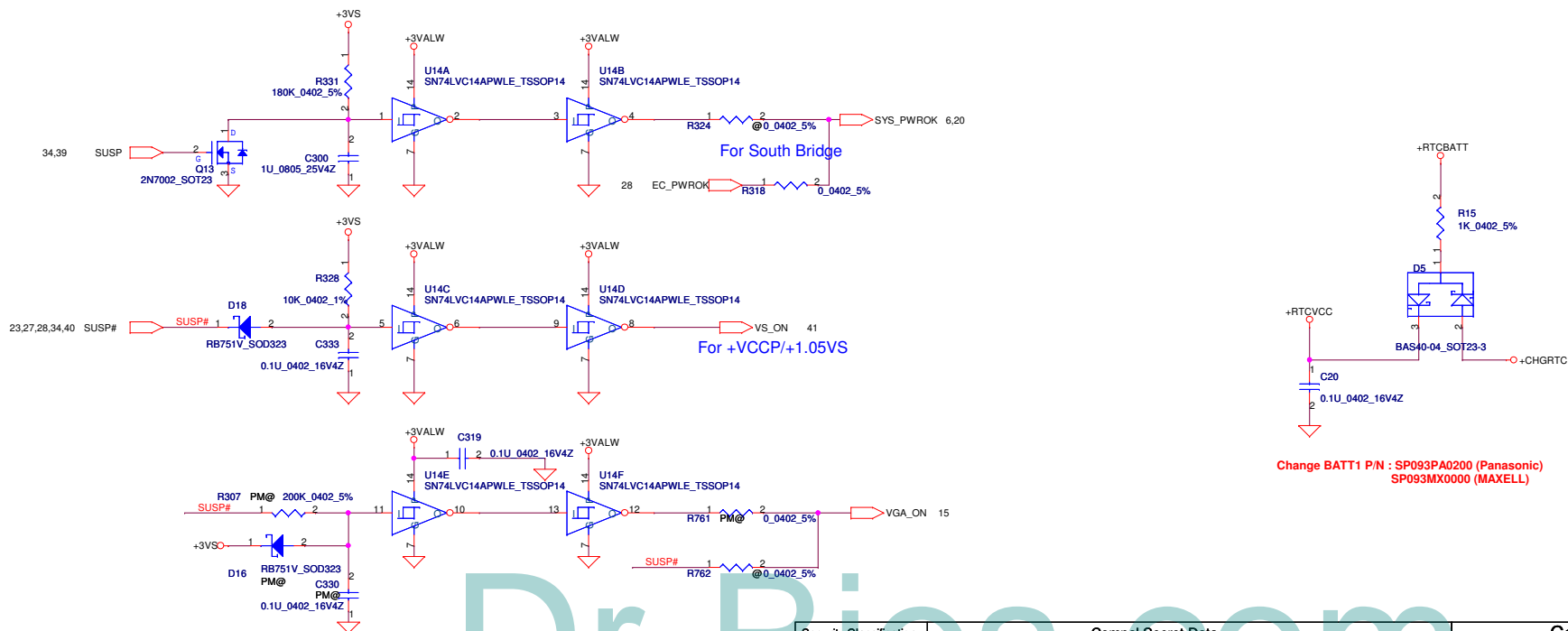
Power Button



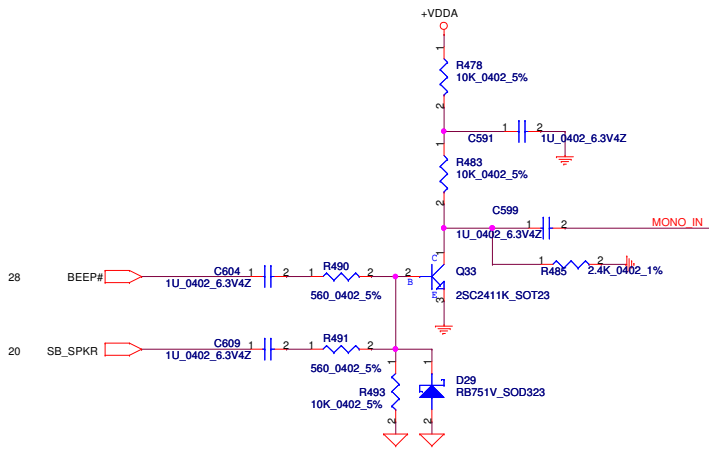
HDA MDC Conn.



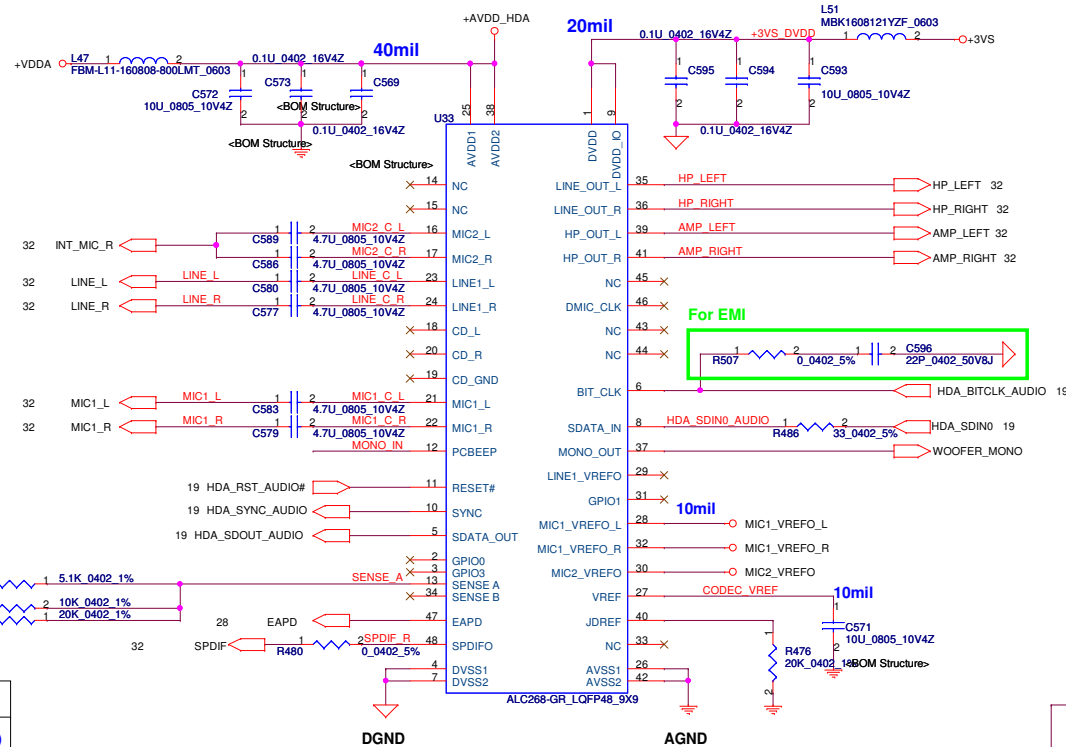
Power ON Circuit



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Size	B	Document Number	JDW50/JDYL70 M/B LA-3771P		Rev
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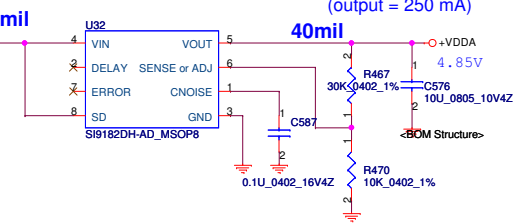


HD Audio Codec

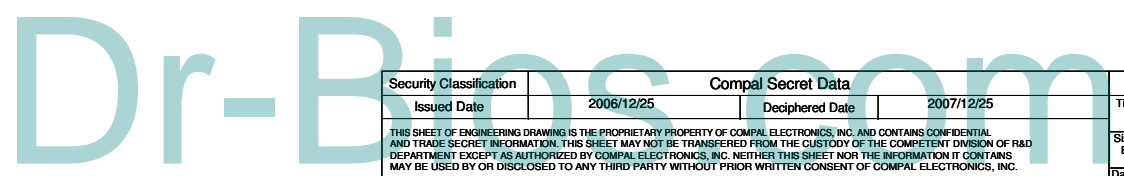
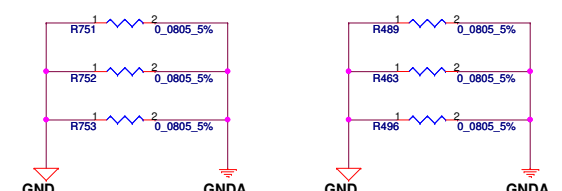


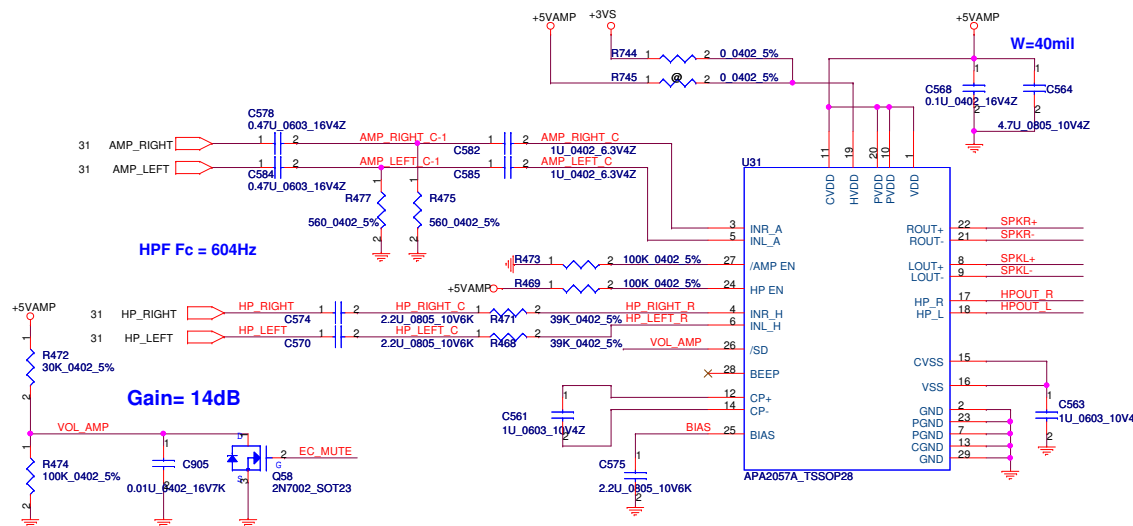
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 35, 36)
	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
5.1K	PORT-H (PIN 45, 46)	

28.7K for Module Design (VDDA = 4.702)
(output = 250 mA)

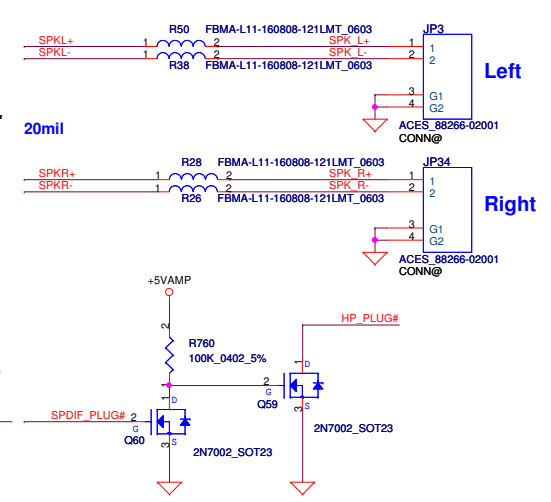


For EMI
R507 0.0402_5% || C596 22P_0402_50V6J



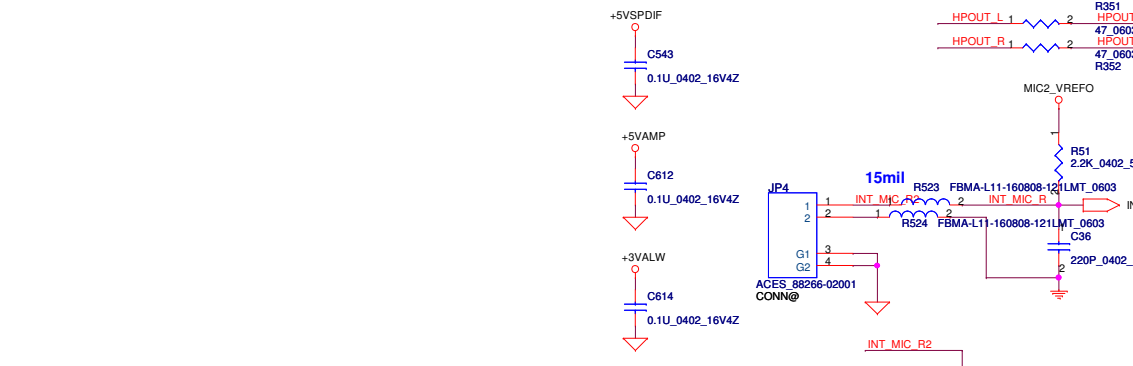


Int. Speaker Conn.

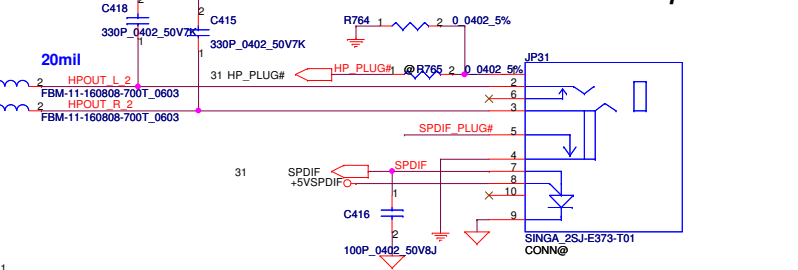


To AUDIO/B Connector

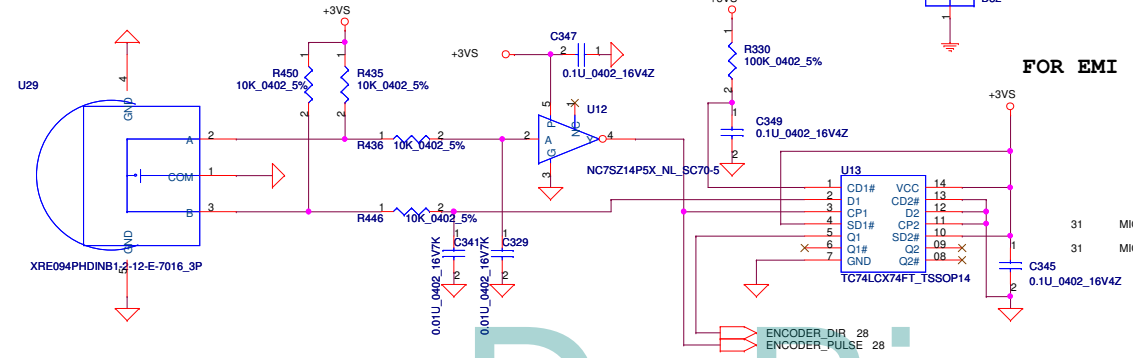
Int MIC Conn.



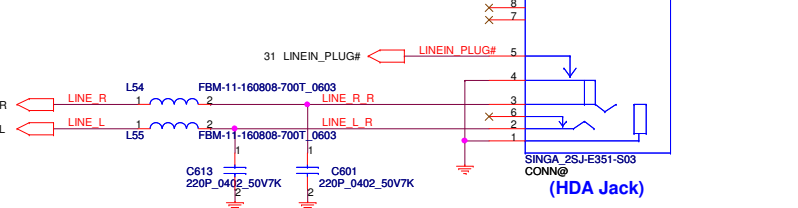
**S/PDIF Out JACK
LINE Out/Headphone Out**



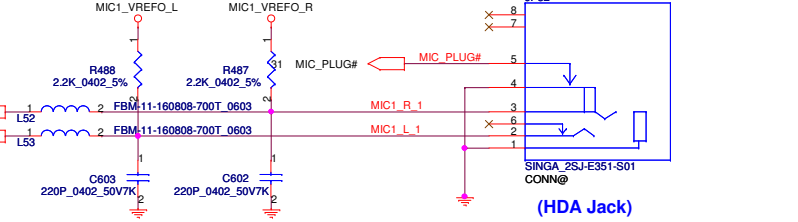
Volume Control Circuit



LINE-IN JACK

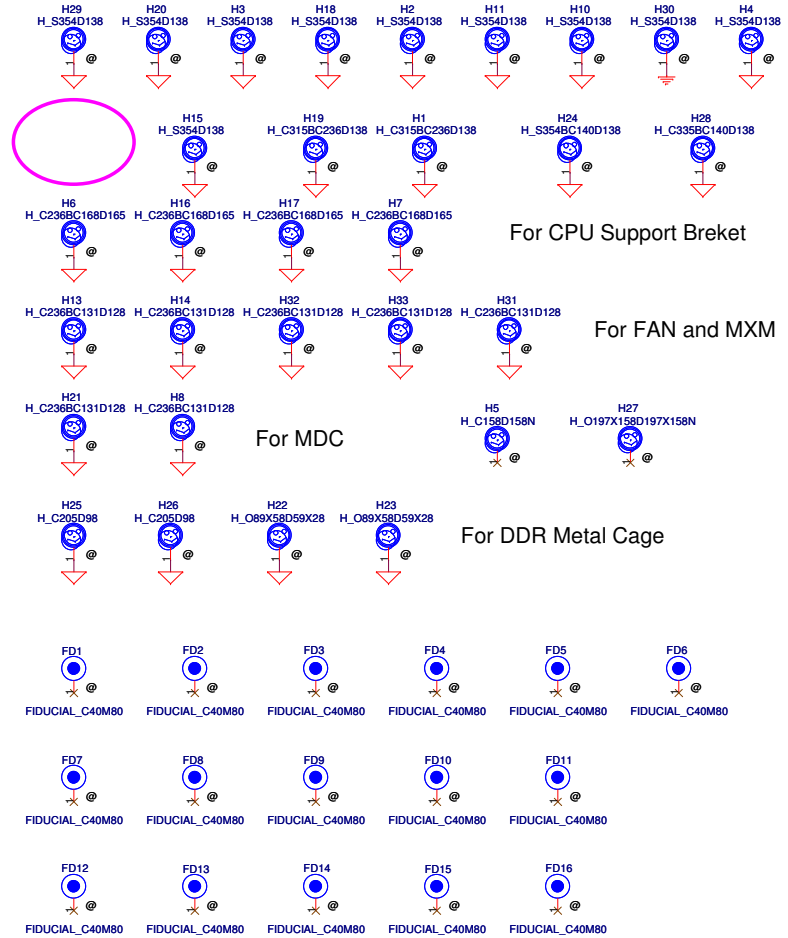
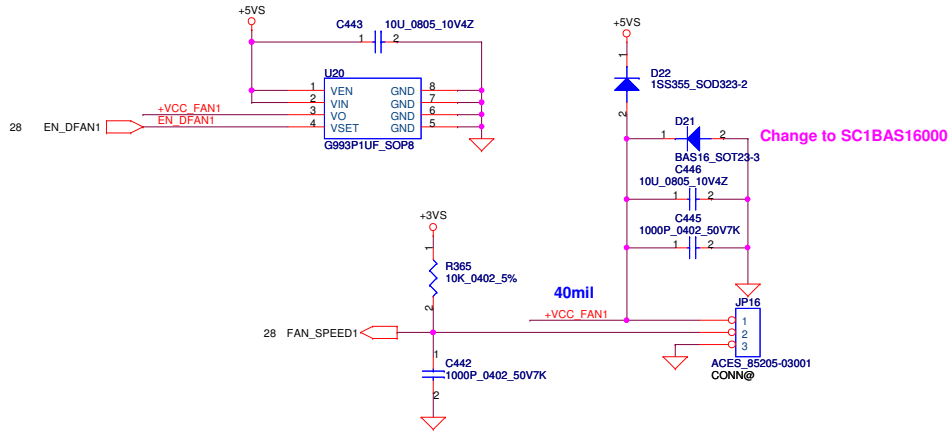


MIC JACK



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Size B	Document Number	JDW50/JDYL70 M/B LA-3771P		Rev 0.2
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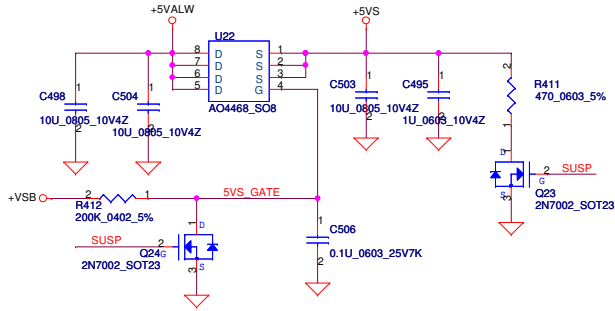
FAN1 Conn



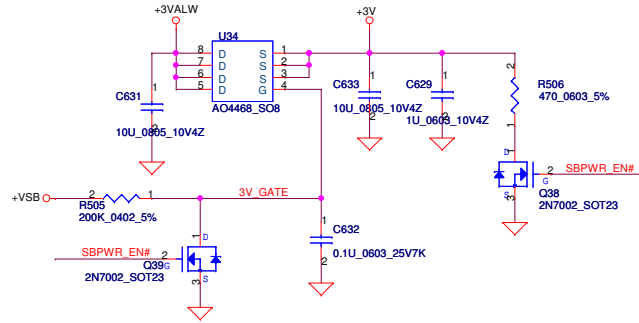
Dr-Engine.com

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Size	Document Number	Rev		
B	JDW50/JDYL70 M/B LA-3771P	0.2		
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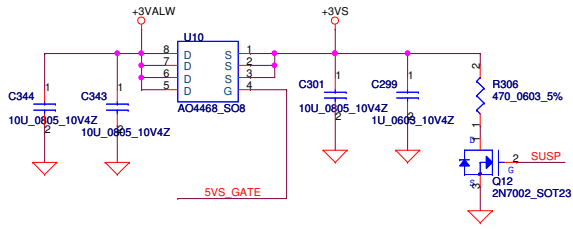
+5VALW TO +5VS



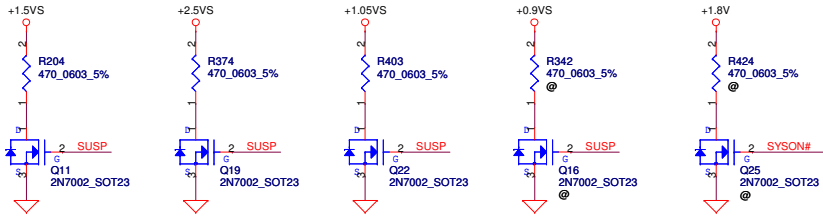
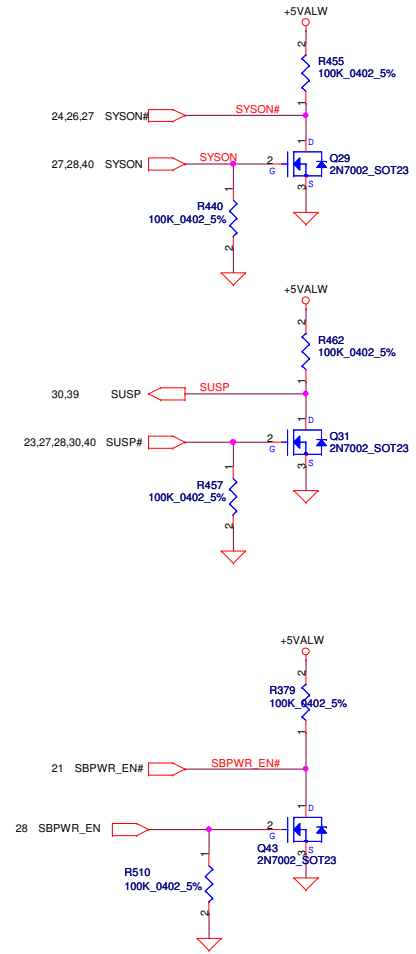
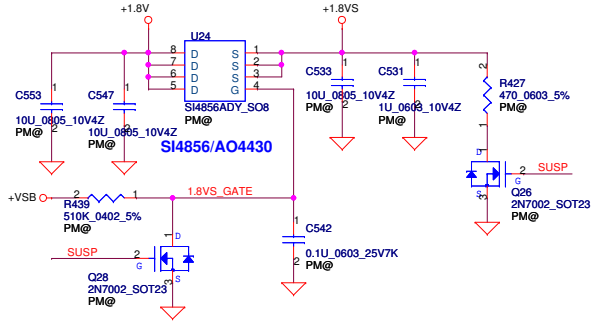
+3VALW TO +3V_SB(ICH8M AUX Power)



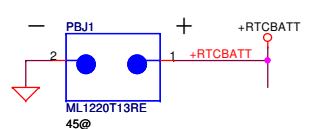
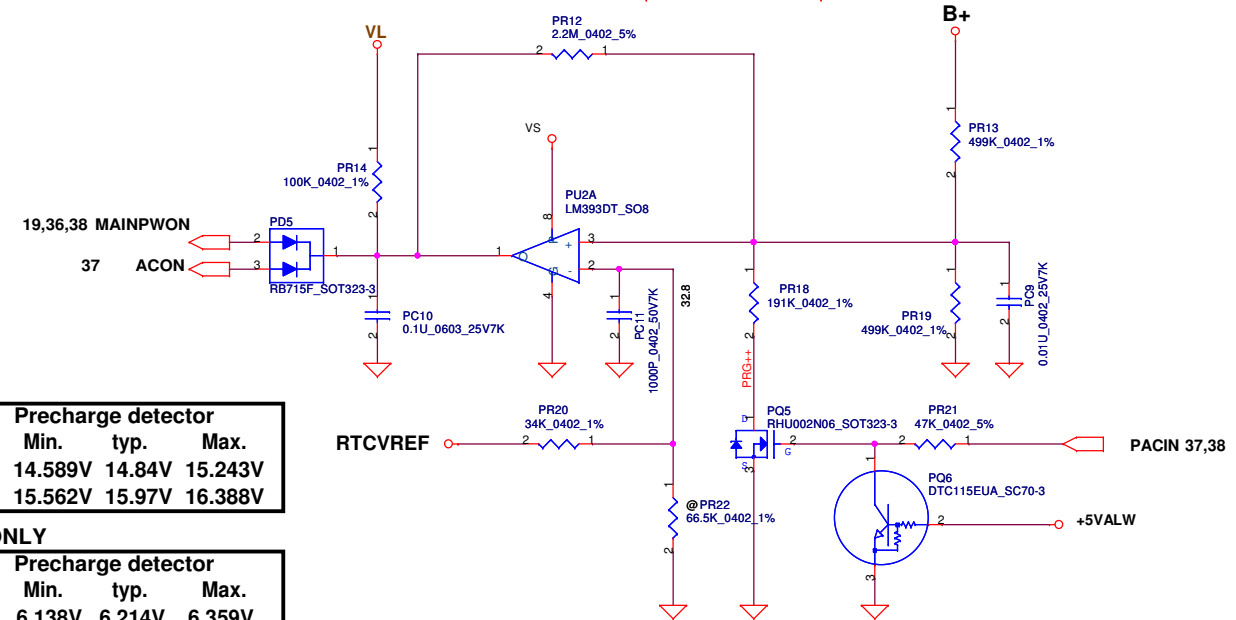
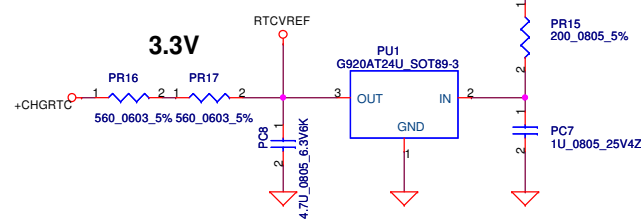
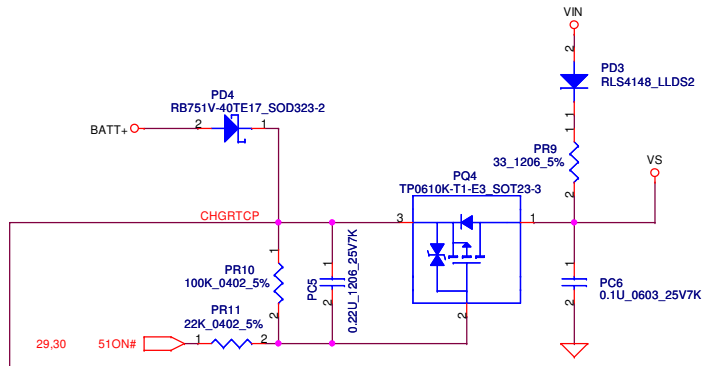
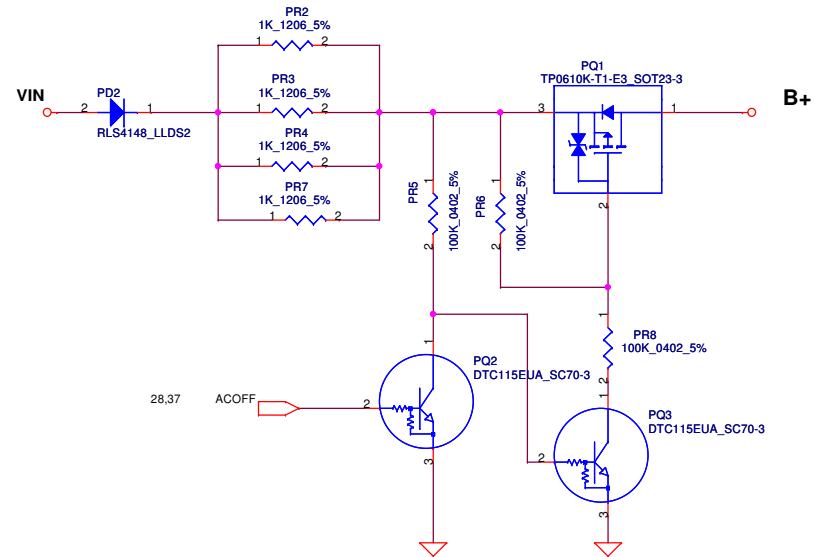
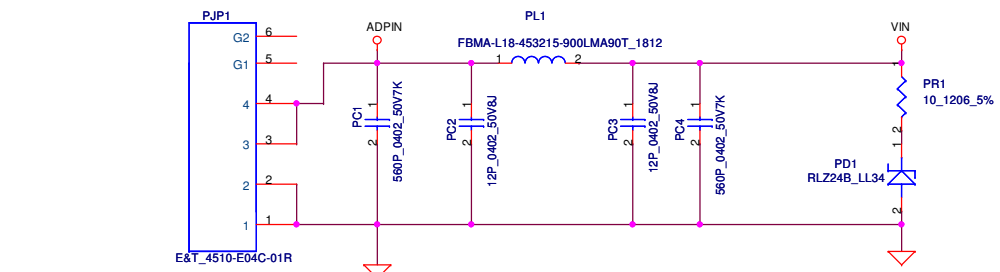
+3VALW TO +3VS



+1.8V to +1.8VS



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Date: Monday, April 16, 2007			Document Number	Rev 0.2
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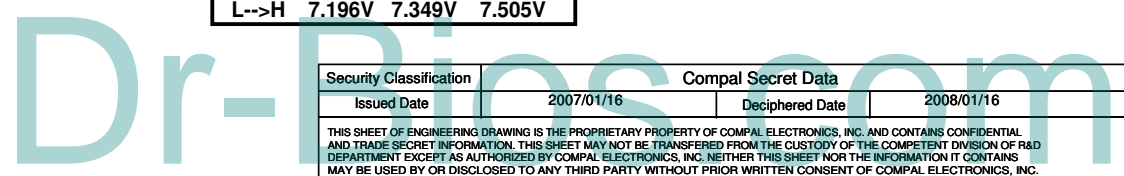


ACIN

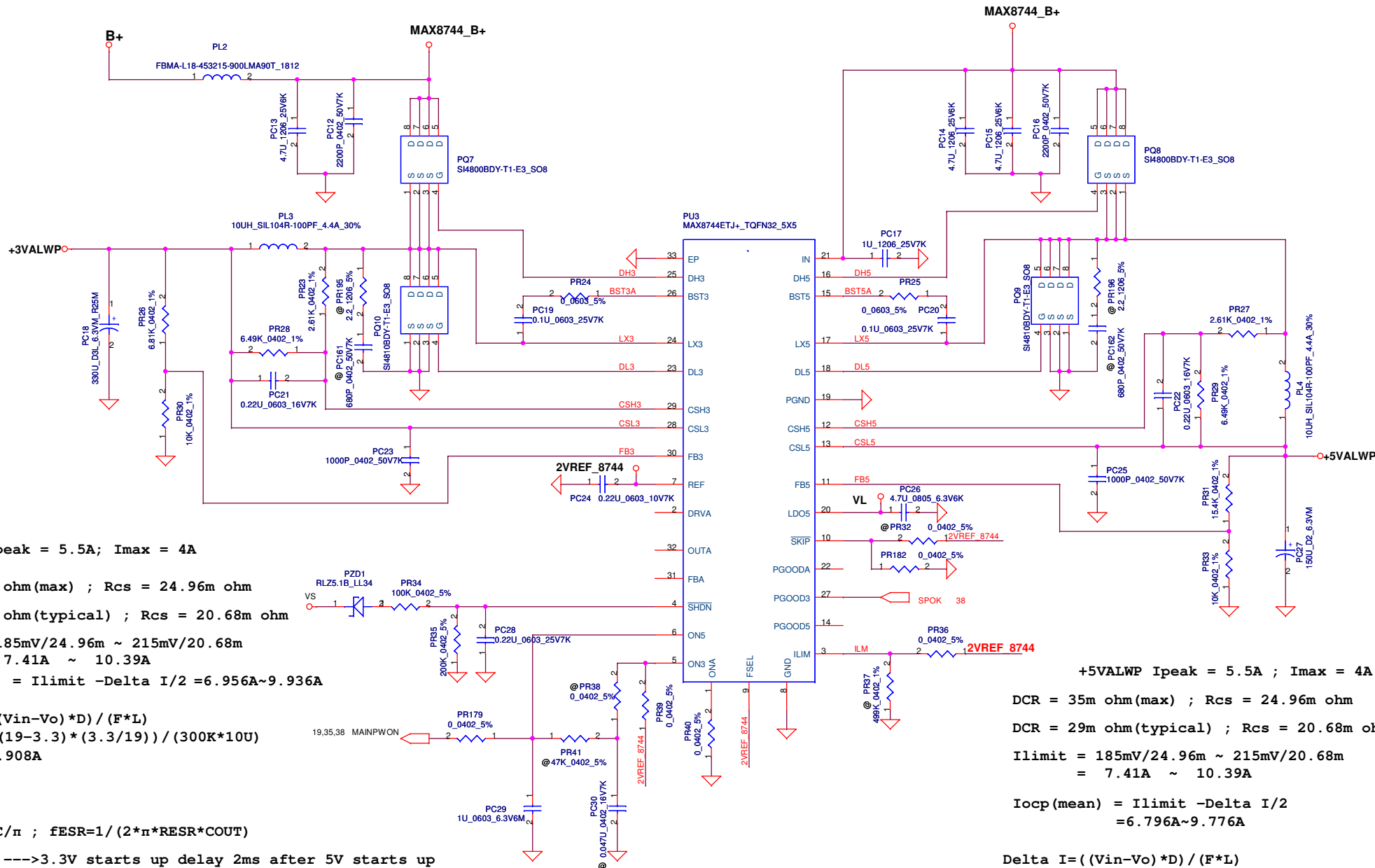
Precharge detector		
Min.	typ.	Max.
H->L	14.589V	15.243V
L->H	15.562V	16.388V

BATT ONLY

Precharge detector		
Min.	typ.	Max.
H->L	6.138V	6.359V
L->H	7.196V	7.505V



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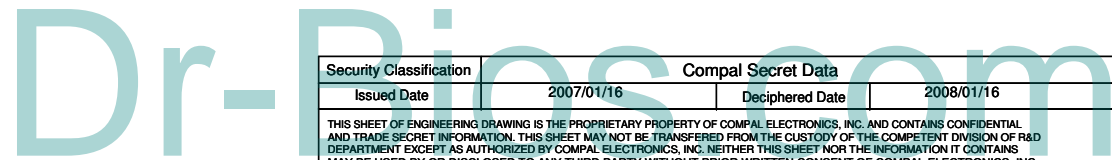
+3VALWP Ipeak = 5.5A; Imax = 4A
 DCR = 35m ohm(max) ; Rcs = 24.96m ohm
 DCR = 29m ohm(typical) ; Rcs = 20.68m ohm
 Ilimit = 185mV/24.96m ~ 215mV/20.68m
 = 7.41A ~ 10.39A
 Iocp(mean) = Ilimit -Delta I/2 = 6.956A~9.936A

Delta I = ((Vin-Vo) * D) / (F * L)
 = ((19-3.3) * (3.3/19)) / (300K * 10U)
 = 0.908A

Notes :
 fESR <= fOSC / pi ; fESR = 1 / (2 * pi * RESR * COUT)
 ON3 = REF ---> 3.3V starts up delay 2ms after 5V

+5VALWP Ipeak = 5.5A ; Imax = 4A
 DCR = 35m ohm(max) ; Rcs = 24.96m ohm
 DCR = 29m ohm(typical) ; Rcs = 20.68m ohm
 Ilimit = 185mV/24.96m ~ 215mV/20.68m
 = 7.41A ~ 10.39A
 Iocp(mean) = Ilimit -Delta I/2
 = 6.796A~9.776A

Delta I = ((Vin-Vo) * D) / (F * L)
 = ((19-5) * (5/19)) / (300K * 10U)
 = 1.228A

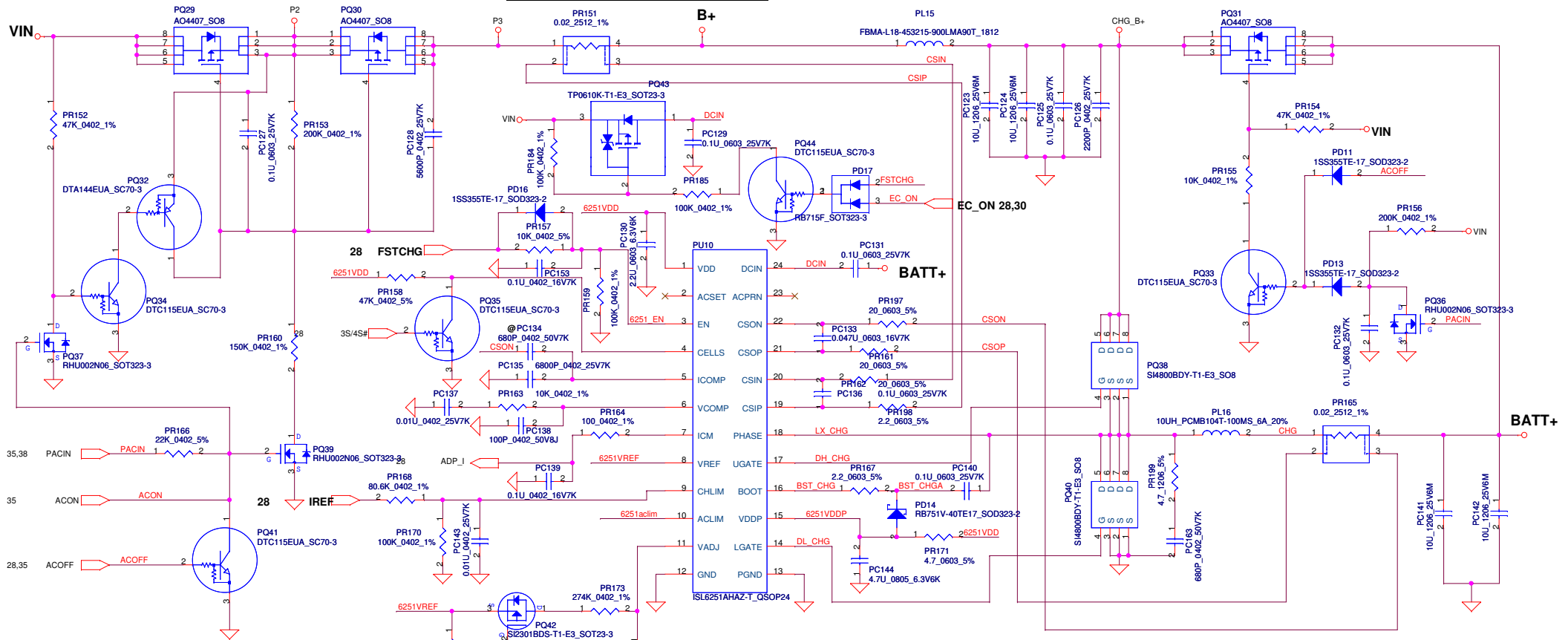


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Iada=0~4.74A (90W)

$ADP_I = 19.9 * I_{adapter} * R_{sense}$

$CP = 85\% * I_{ada} ; CP = 4.07A$

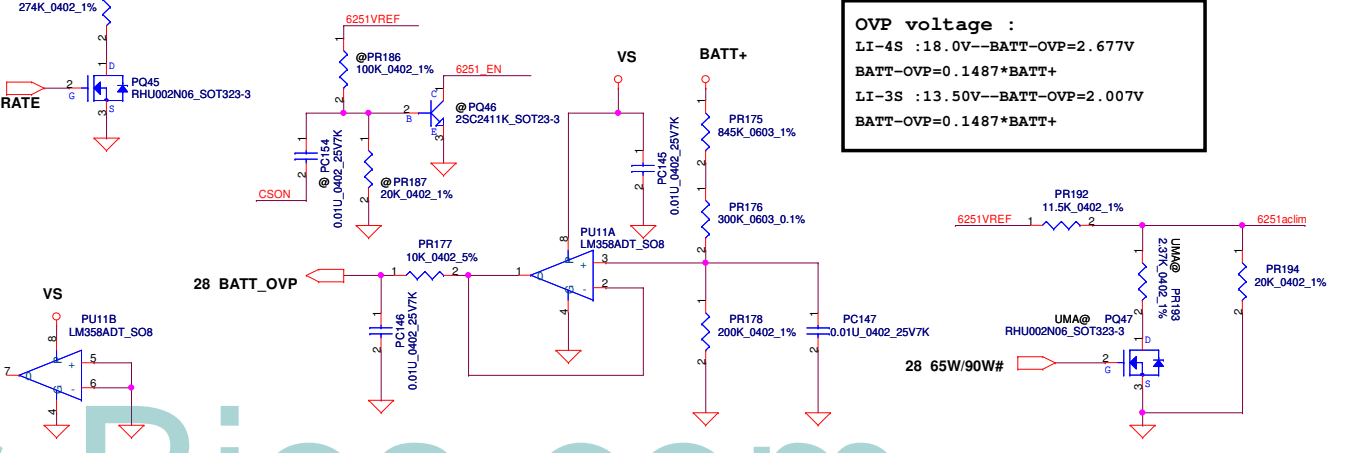


CP mode
 $I_{input} = (1/0.02) * ((0.05 * V_{acim}) / 2.39 + 0.05)$
 where $V_{acim} = 1.502V$, $I_{input} = 4.07A$
 $V_{acim} = 2.39 * ((10K // 152K) / ((5.76K // 152K) + (10K // 152K)))$
 = 1.502V

CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

OVP voltage :
 LI-4S : 18.0V -- BATT-OVP = 2.677V
 BATT-OVP = 0.1487 * BATT+
 LI-3S : 13.50V -- BATT-OVP = 2.007V
 BATT-OVP = 0.1487 * BATT+



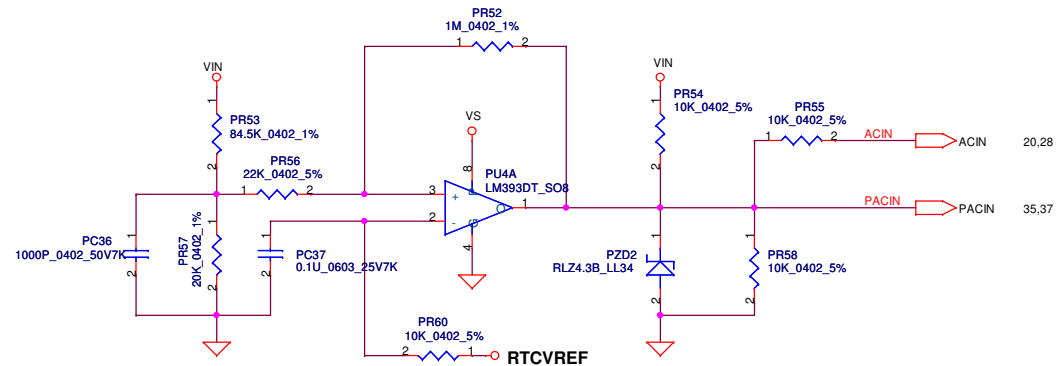
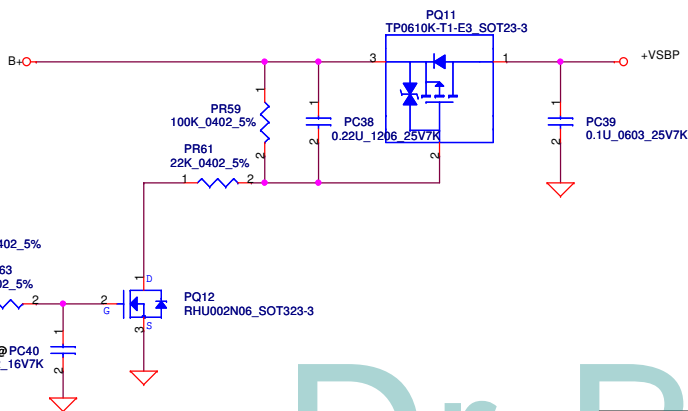
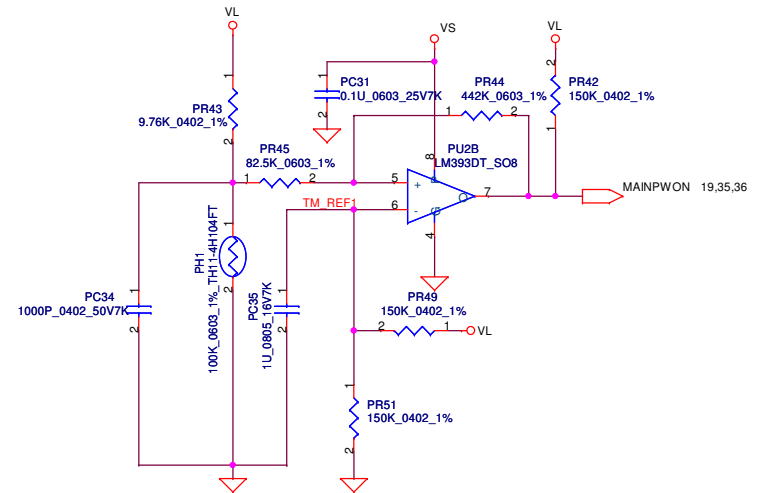
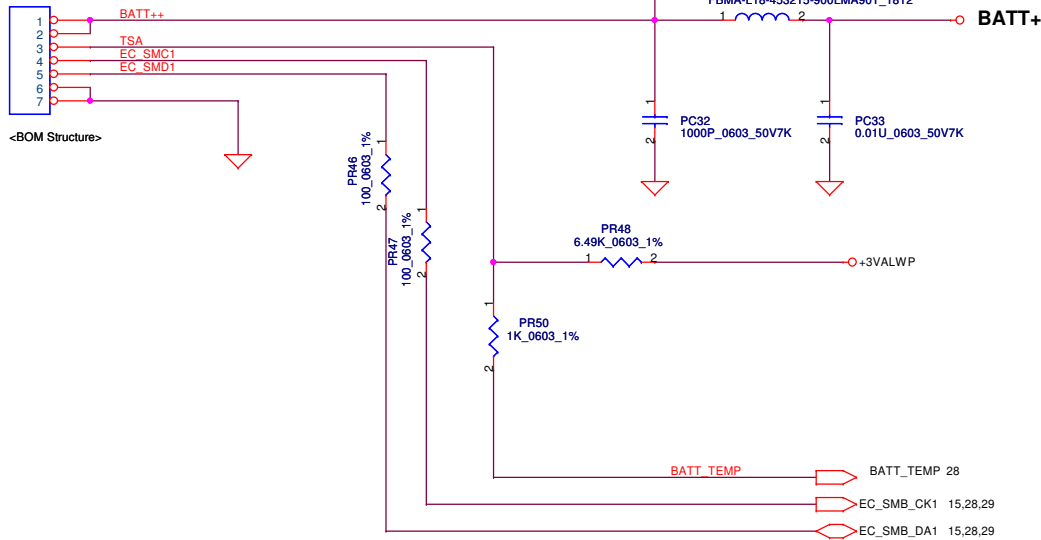
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CHARGER			
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PH1 under CPU botten side :
 CPU thermal protection at 90 degree C
 Recovery at 70 degree C

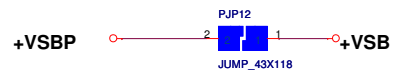
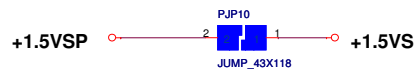
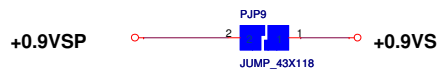
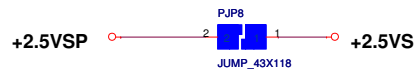
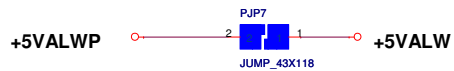
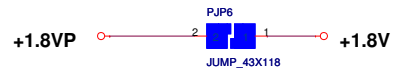
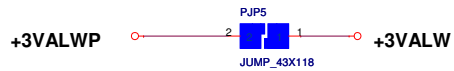
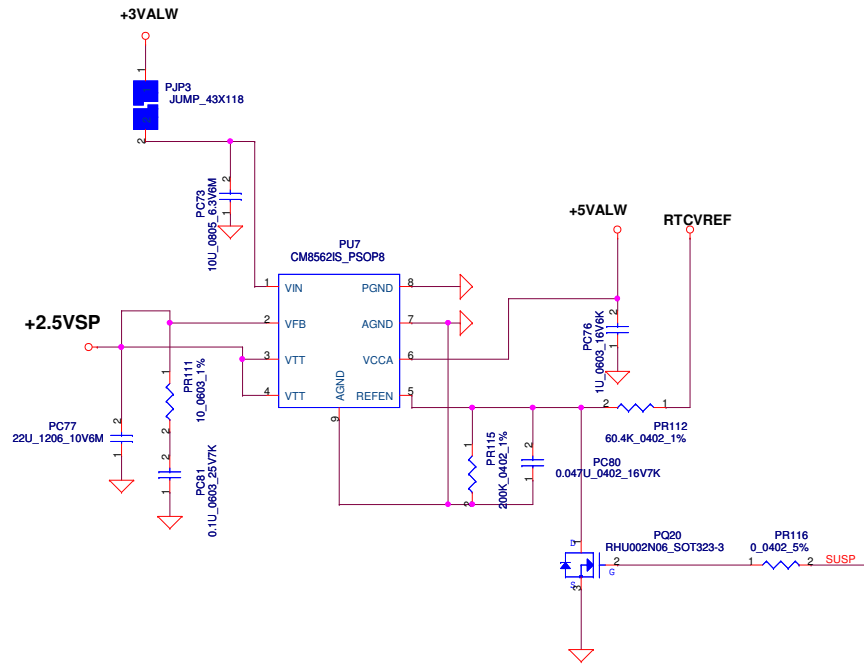
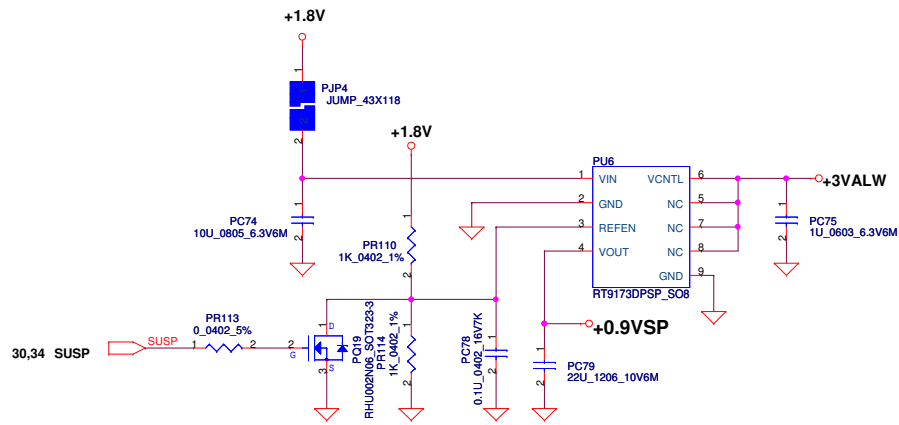
SUYIN_200275MR007G161ZL
 PJP2



Vin Detector		
Min.	typ.	Max.
H-->L 16.976V	17.257V	17.728V
L-->H 17.430V	17.901V	18.384V

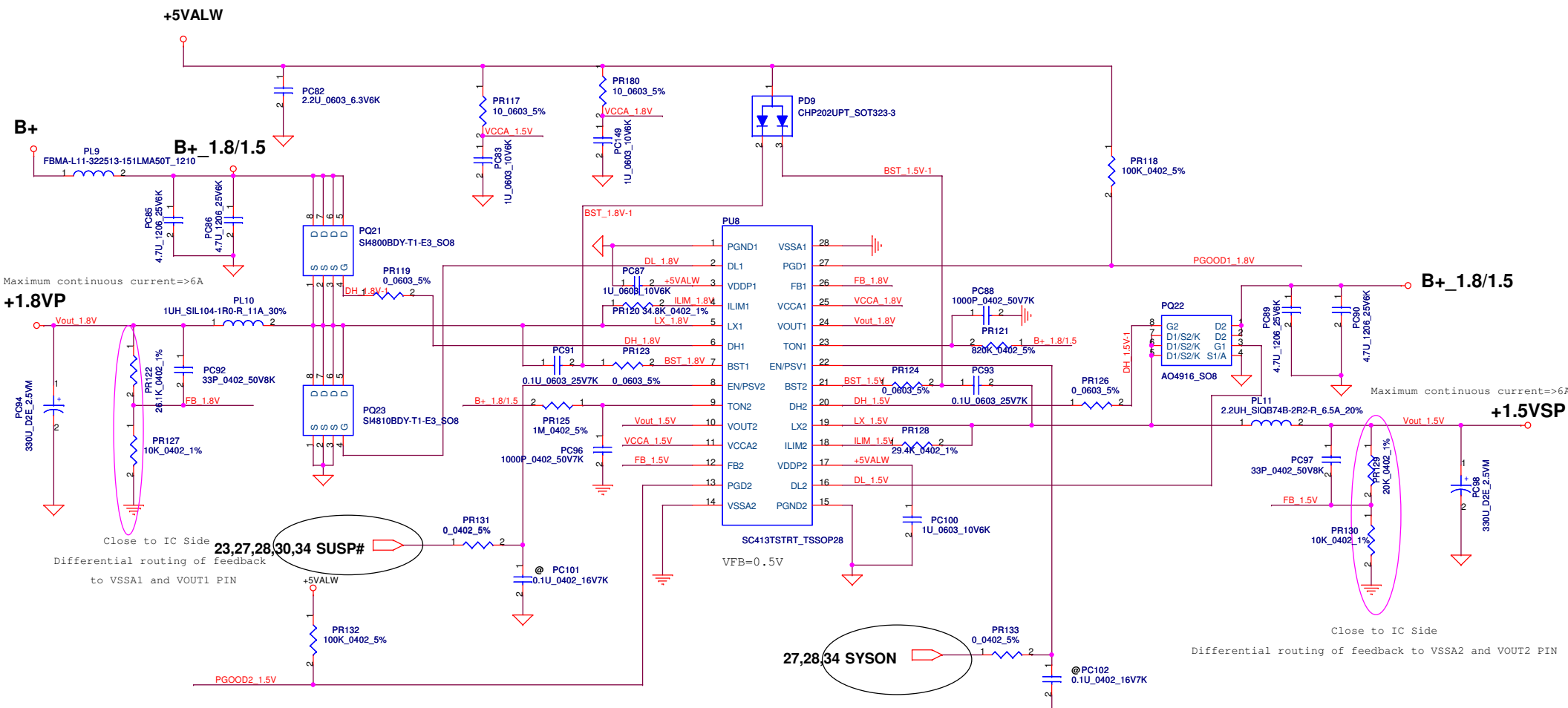
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Title	+0.9VSP/+2.5VSP			
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Maximum continuous current=>6A

Maximum continuous current=>6A

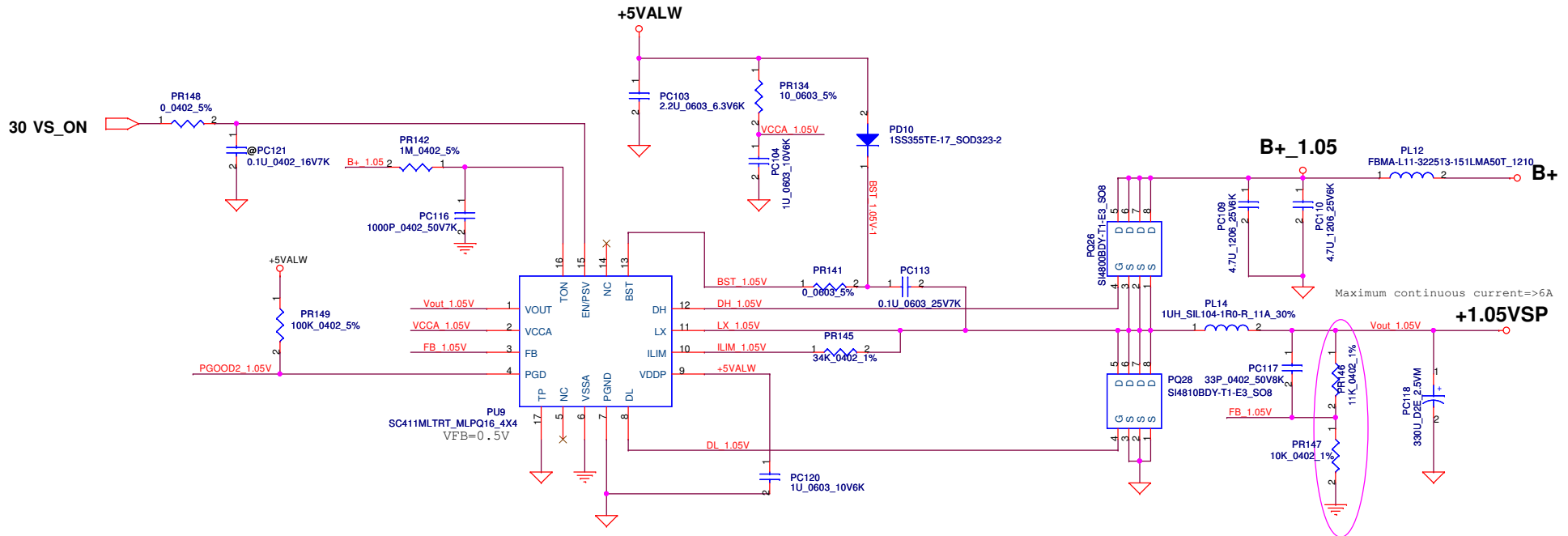
VFB=0.5V
 $V_o = V_{FB} * (1 + PR122 / PR127) = 1.805V$
Ipeak=12.17A, Imax=8.519A
 $T_{on} = (3.3E-12 * (PR121 + 37K) * (V_{out} / V_{Bat})) + 50ns$
 $= 3.3 * 10e-12 * (820K + 37K) * (1.8 / 19) + 50ns = 0.3179us$
 FDS6670AS:Rds(on) => Typ:9 mOhm
 Max:11.5 mOhm
 $I_{ocp} = I_{valley} + I_{ripple} / 2$
 $I_{ripple} = (v_{in} - v_{out}) * (T_{on} / L) = 5.467A, 1/2 I_{ripple} = 2.734A.$
 $I_{valleymin} = 10E-6 * (PR120 / R_{ds}(ON)_{max} * 1.5)$
 $= 9 * 10e-6 * (27.4K / 0.0115 * 1.5) = 14.295A > 11.73 * 1.2 = 14.076A$
 $I_{valleymax} = 10E-6 * (PR120 / R_{ds}(ON)_{typ} * 1.2)$
 $= 11 * 10e-6 * (27.4K / 0.009 * 1.2) = 27.907A.$
 OCP ==> 17.029A ~ 30.641A

VFB=0.5V
 $V_o = V_{FB} * (1 + PR129 / PR130) = 1.5V$
Ipeak=5.16A, Imax=3.612A
 $T_{on} = (3.3E-12 * (PR125 + 37K) * (V_{out} / V_{Bat})) + 50ns$
 $= 0.3201us$
 AO4916 Rds(on) => Typ:21 mOhm
 Max:27 mOhm
 $I_{valleymin} = 9 * 10u * (29.4K / 0.027 * 1.4) = 7A$
 $I_{valleymax} = 11 * E-6 * (29.4K / 0.021 * 1.1) = 12.833A$
 $I_{ripple} = (v_{in} - v_{out}) * (T_{on} / L) = 2.546A, 1/2 I_{ripple} = 1.273A$
 $I_{ocp} = I_{valley} + I_{ripple} / 2$
 OCP ==> 8.273A ~ 14.106A

27,28,34 SYSON

23,27,28,30,34 SUSP#

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Close to IC Side
Differential routing of feedback to VSSA2 and VOUT2 PIN

VFB=0.5V, Ipeak=9.37A, Imax=6.559A

The current rating of +1.05VSP include +VCC_GFX current.

$V_o = VFB * (1 + PR146 / PR147) = 1.05V$

$Ton = (3.3E-12 * (PR142 + 37K) * (Vout / VBat)) + 50ns = 0.2391\mu s$

SI4810BDY: Rds(on) => Typ: 16mOhm
Max: 20mOhm

$Ivalleymin = 9 * 10E-6 * (PR145 / Rds(ON)) * max * 1.5$

= 9 * 10E-6 * (34K / (0.02 * 1.5)) = 10.200A

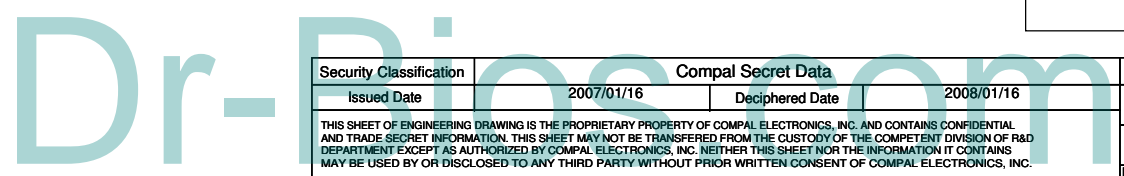
$Ivalleymax = 11 * 10E-6 * (PR145 / Rds(ON)) * min * 1.3$

$= 11 * 10E-6 * (34K / (0.016 * 1.3)) = 17.981A$

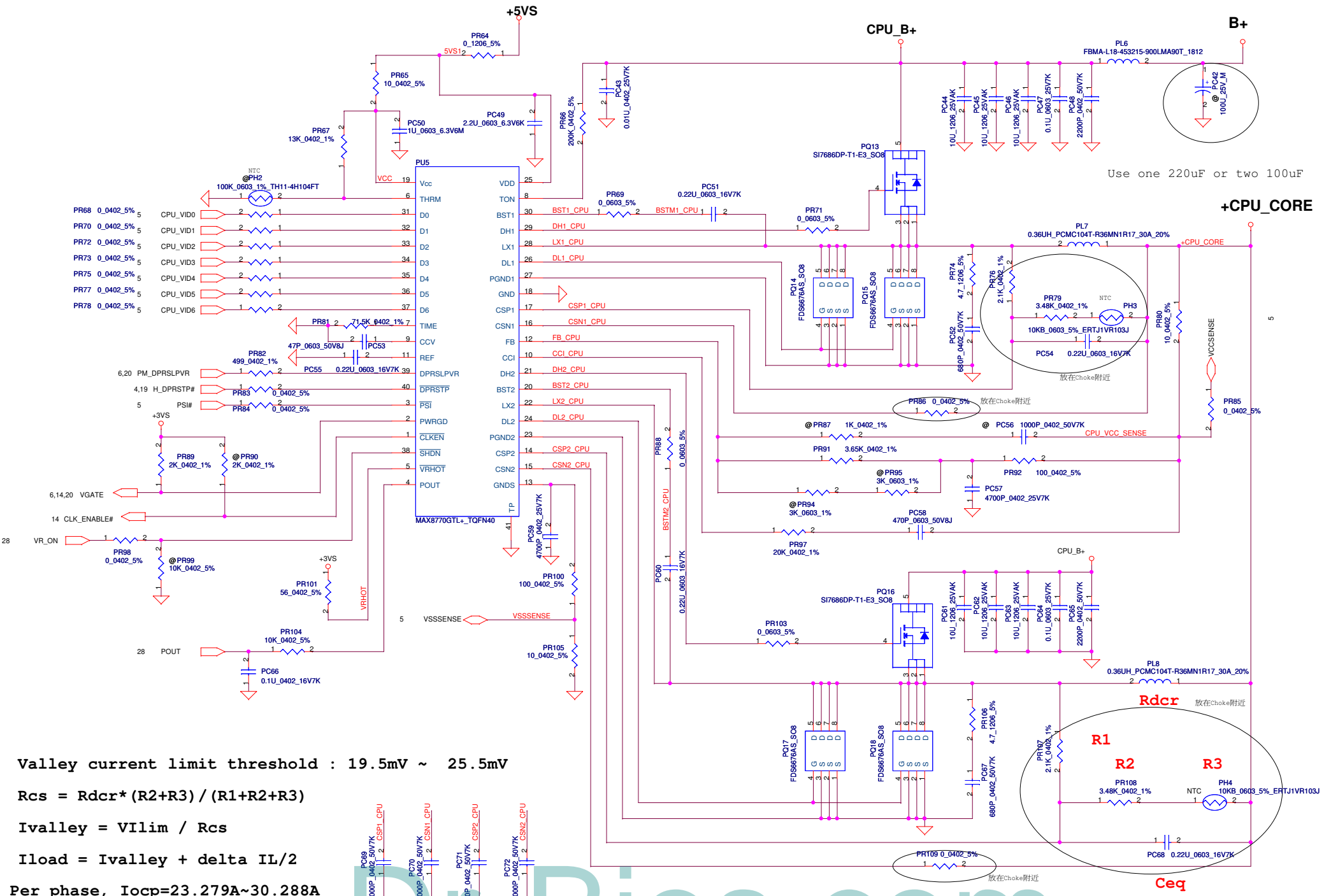
$Iripple = (vin - vout) * (Ton / L) = 4.292A, 1/2 Iripple = 2.146A$

$Iocp = Ivalley + Iripple / 2$

OCP => 12.346A ~ 20.127A



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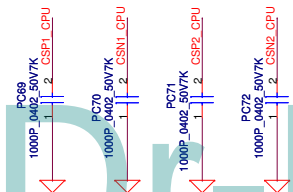
Valley current limit threshold : 19.5mV ~ 25.5mV

$$R_{cs} = R_{dcr} * (R2 + R3) / (R1 + R2 + R3)$$

$$I_{valley} = V_{ilim} / R_{cs}$$

$$I_{load} = I_{valley} + \Delta I_L / 2$$

Per phase, $I_{ocp} = 23.279A \sim 30.288A$



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	EC GPIO pin modify	EC GPIO pin modify	0.1 ==> 0.2	8	DPST_PWM net modify	3/19	
2	clk frequency error	pin error	0.1 ==> 0.2	14	Q48,Q49,Q50 pin error		
3	EC add a GPIO pin	EC GPIO pin modify	0.1 ==> 0.2	16	del DPST_PWM net from North Bridge		
4	follow ICL50	follow ICL50	0.1 ==> 0.2	20	CRT_DET# net modify		
5	EMI request	EMI request	0.1 ==> 0.2	24	Add R477, R748		
6	ESD request	ESD request	0.1 ==> 0.2	25	reserve D30,D31		
7	test	test	0.1 ==> 0.2	26	reserve MINI1_LED#		
8	Blue LED issue	Blue LED issue	0.1 ==> 0.2	27	BT_LED# schematic modify		
9	EC GPIO pin modify	EC GPIO pin modify	0.1 ==> 0.2	28	EC GPIO pin define modify		
10	ESD request	ESD request	0.1 ==> 0.2	29	reserve C895 to C904		
11	easy short	easy short	0.1 ==> 0.2	30	change J1,J2 jumper sybmol to 0603 symbol		
12	ESD request	ESD request	0.1 ==> 0.2	31	Add R751,R752,R753		
13	chip issue	chip issue	0.1 ==> 0.2	32	U31 chip update version		
14	voice too small	modify gain value	0.1 ==> 0.2	32	change R472 form 39k to 30k ohm		
15	EMI request	EMI request	0.1 ==> 0.2	32	change R523,R524,R50,R38,R26,R28 for 0 ohm to bead		
16	DFX request	DFX request	0.1 ==> 0.2	33	del pjp15		
17	Wireless Lan S4 fail	Wireless Lan fail	0.2 ==> 0.3	26	del R756, add R757		
18	Wireless Lan S4 fail	Wireless Lan fail	0.2 ==> 0.3	26	change C906,C907 from 22u_1206 to 10u_0805		
19	Lead Free	non LP=>Lead Free	0.2 ==> 0.3	17	change C211,C510,C514,C216,C508,C515		
20	KBC version update	KBC version update	0.2 ==> 0.3	28	reserve 0.1u at pin 124		
21	SPDIF udapte	SPDIF circuit udapte	0.2 ==> 0.3	32	add q59,q60		
22	DFX	DFX issue	0.2 ==> 0.3	32	del JP13		
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Title PIR (HW)			
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Charger IC damage issue	Charger IC damage issue	0.2	40	Change PR161 from SD013220B80 to SD013200A80		
2	Charger IC damage issue	Charger IC damage issue	0.2	40	Change PR162 from SD013180A80 to SD013200A80		
3	Charger IC damage issue	Charger IC damage issue	0.2	40	Add PR197 SD013200A80		
4	Charger IC damage issue	Charger IC damage issue	0.2	40	Add PR198 SD013220B80		
5	Charger IC damage issue	Charger IC damage issue	0.2	40	Add PC133 SE026473K80		
6	Add EMI solution in charger.	Add EMI solution in charger.	0.3	40	Add PR199 SD001470B80(S RES 1/4 4.7 1206 5%).	04/01/07	PVT
7	Add EMI solution in charger.	Add EMI solution in charger.	0.3	40	Add PC163 SE074681K80(S CER CAP 680P 50V K X7R 0402)	04/01/07	PVT
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Title PIR (PWR)			
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