Compal Confidential

Model Name : JM40-HR
File Name : LA-7231P

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JM40-HR M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P-GS/GV-OP

2010-02-22

REV:1.0

ZZZ

Part Number	Description
DAZ0IO00100	

P4LJ0_PCB
PCB P4LJ0 LA-7231P LS-7231P/7233P/7235P/7237P

ZZZ

Part Number	Description
DC30100DT00	DC_IN_CABLE_90W

P4LJ0_DCIN_CABLE_90W
90W@

ZZZ

Part Number	Description
DC30100DS00	DC_IN_CABLE_65W

P4LJ0_DCIN_CABLE_65W
65W@

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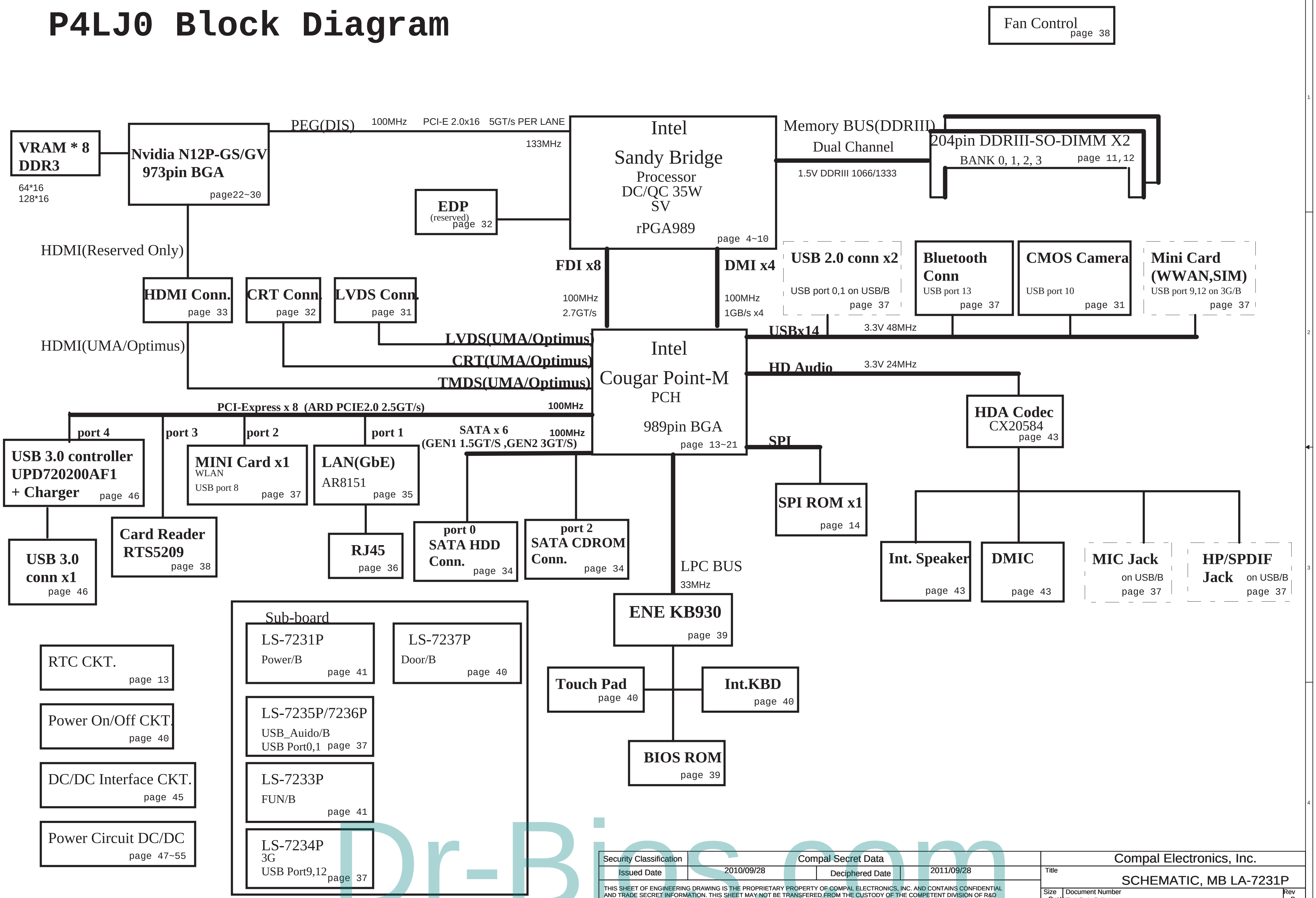
P4LJ0 Block Diagram



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID/ Project ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
N12P-GS	GS@
N12P-GV	GV@
Discrete(OPTIMUS)	OPT@
VRAM	X76@
Blue Tooth	BT@
AR8151	8151@
Connector	CONN@
Unpop	@

Project ID Table

Project ID	Project Name
0	P3LJ0
1	P4LJ0
2	P5LJ0
3	P3LS0
4	P4LS0
5	P5LS0
6	
7	

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
	UHCI1	2	
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	Mini Card(WWAN)
	UHCI5	10	Camera
		11	
	UHCI6	12	SIM Card
		13	Blue Tooth

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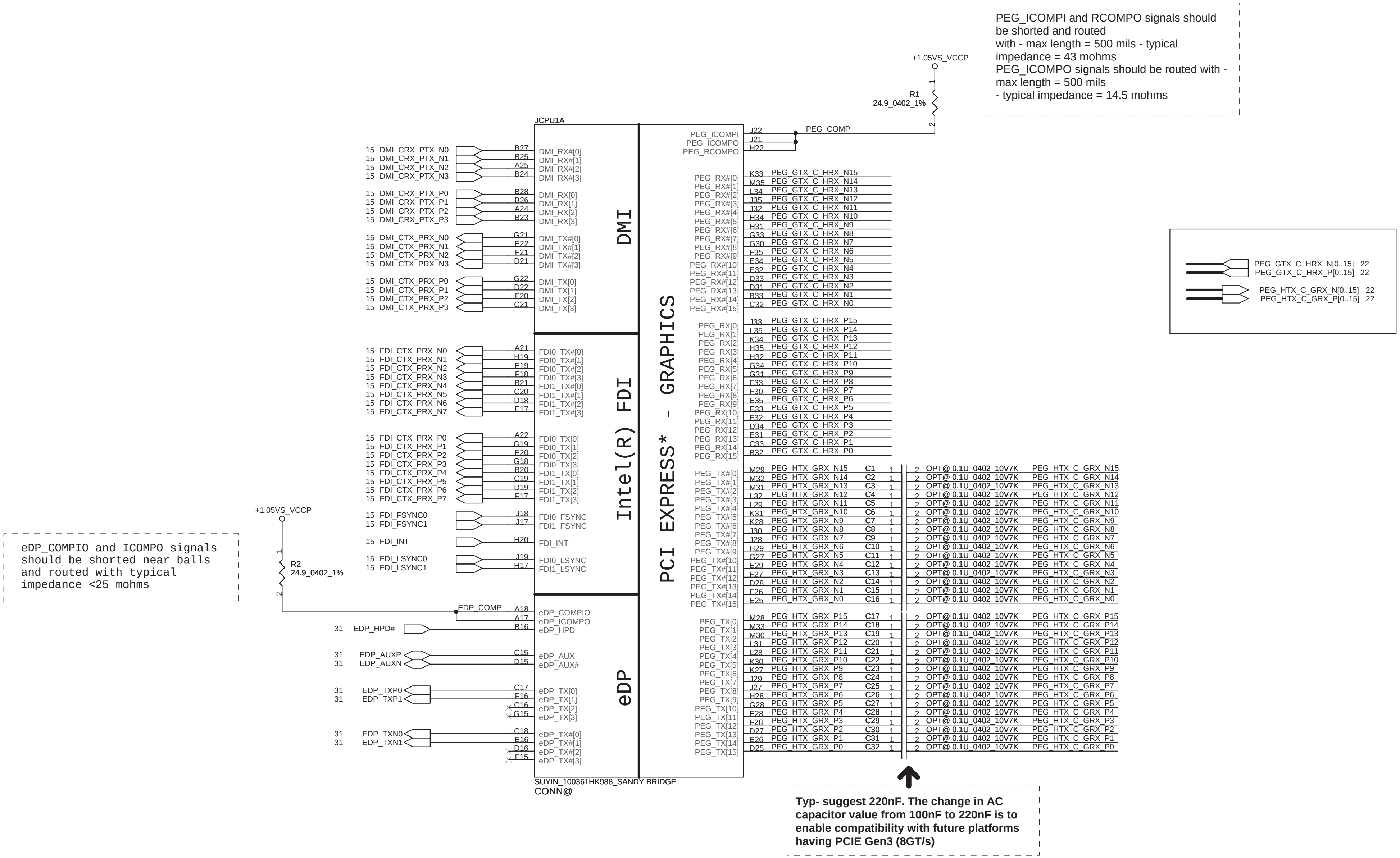

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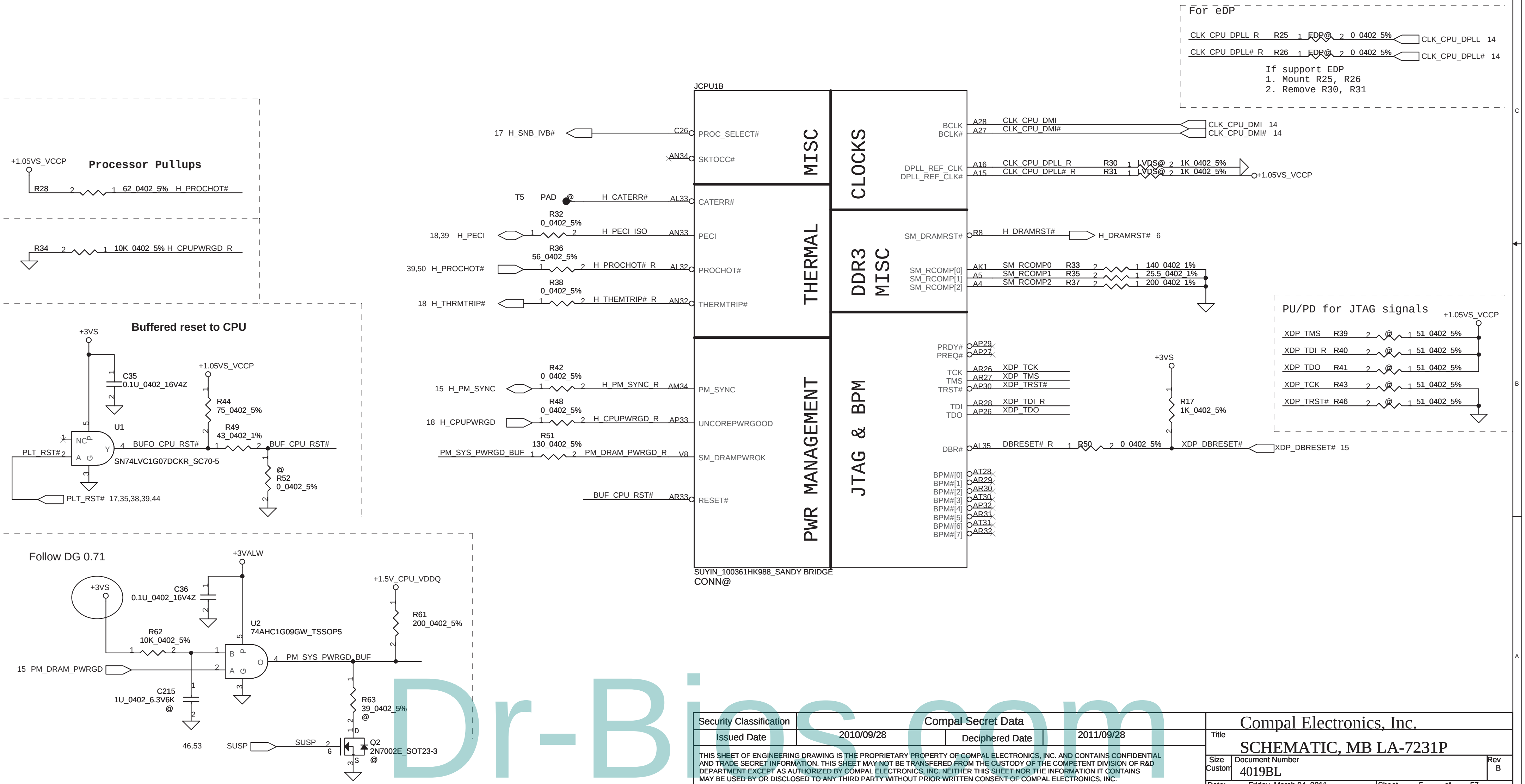

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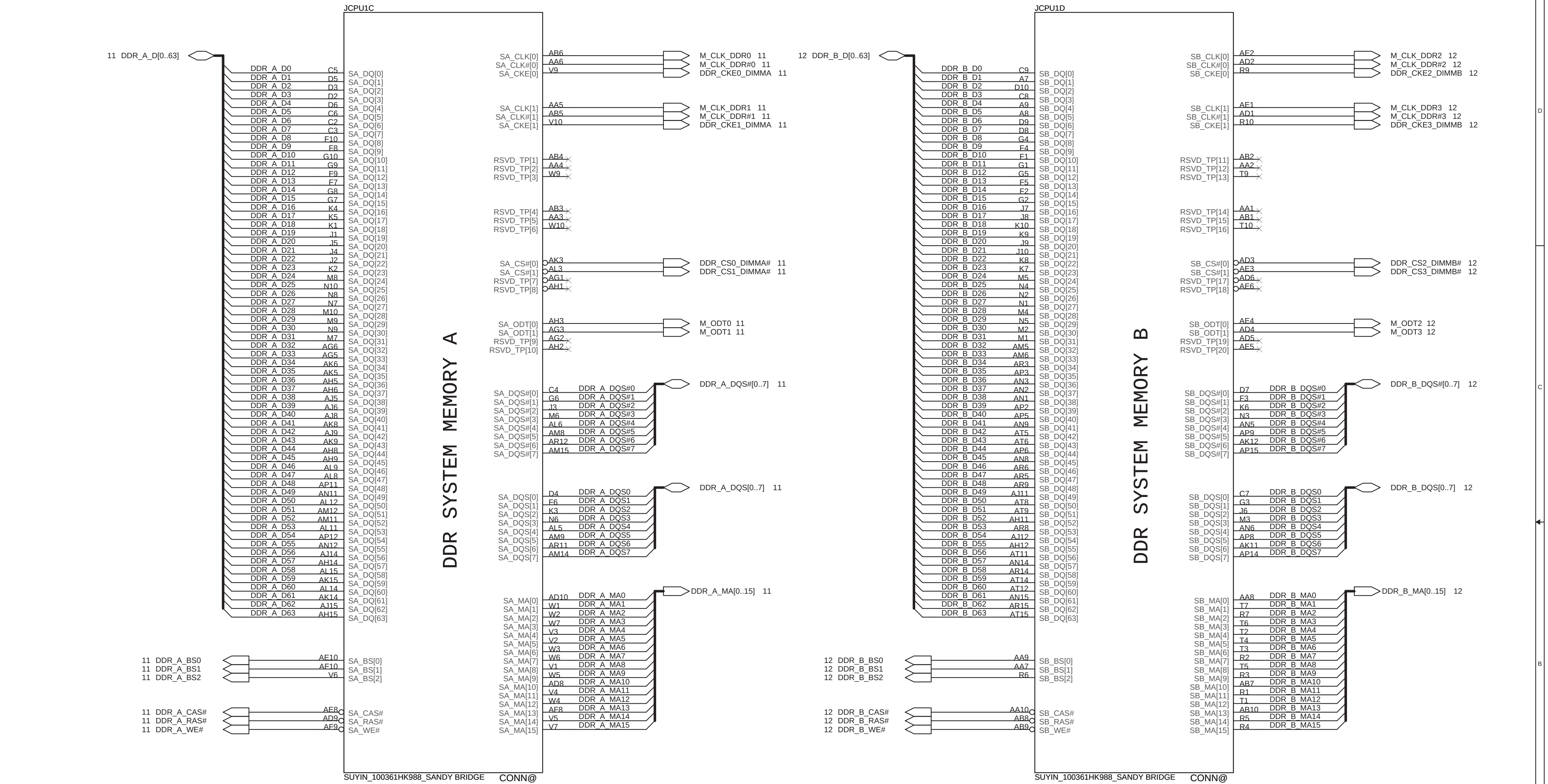

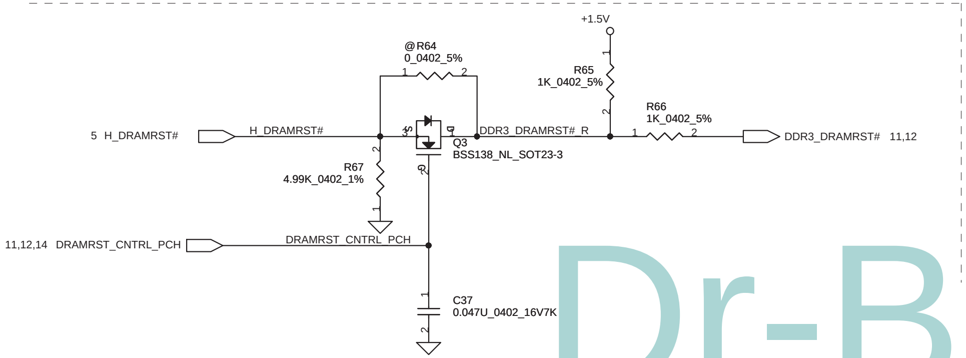

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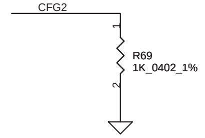
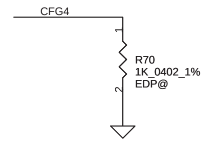
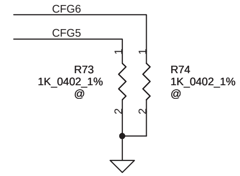
CFG Straps for Processor



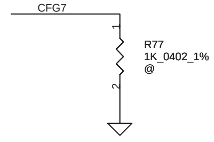
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



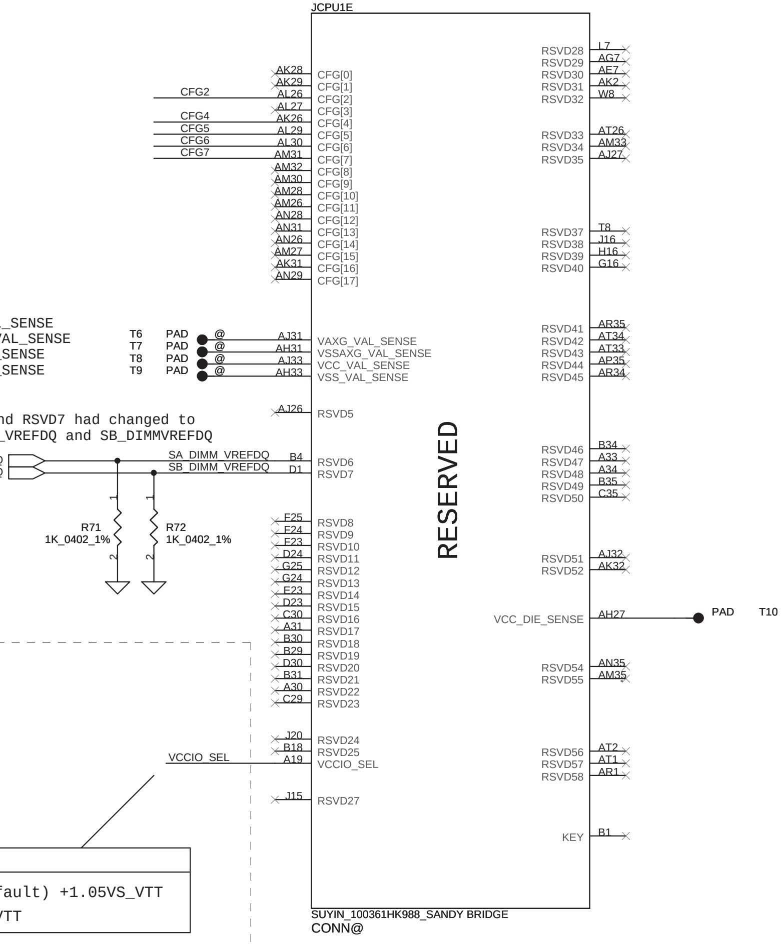
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



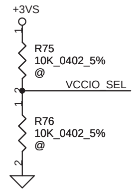
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



AJ31 change to VAXG_VAL_SENSE
AH31 change to VSSAXG_VAL_SENSE
AJ33 change to VCC_VAL_SENSE
AH33 change to VSS_VAL_SENSE

RSVD6 and RSVD7 had changed to
SA_DIMM_VREFDQ and SB_DIMMVREFDQ

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
For Future CPU M3 support,
Sandey bridge not supportM3,
Check list1.0&CRB say can NC



VCCIO_SEL	
A19	* 1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

VCCIO_SEL For 2012 CPU support

RSVD26 had changed the name to VCCIO_SEL
Need PH +3VS 10K at +1.05VS_VTT source
for 2012 processor +1.05V and +1.0V select

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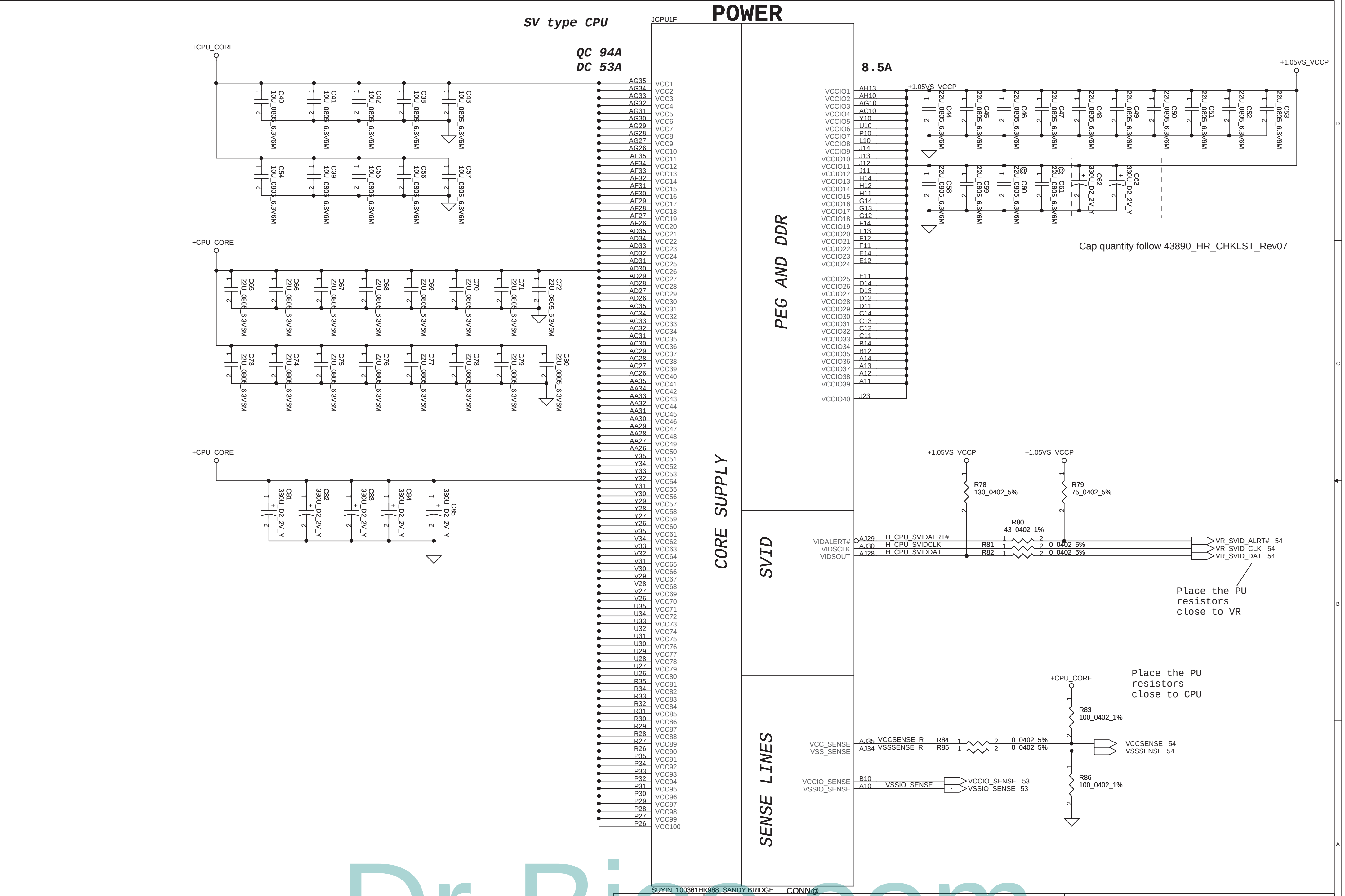

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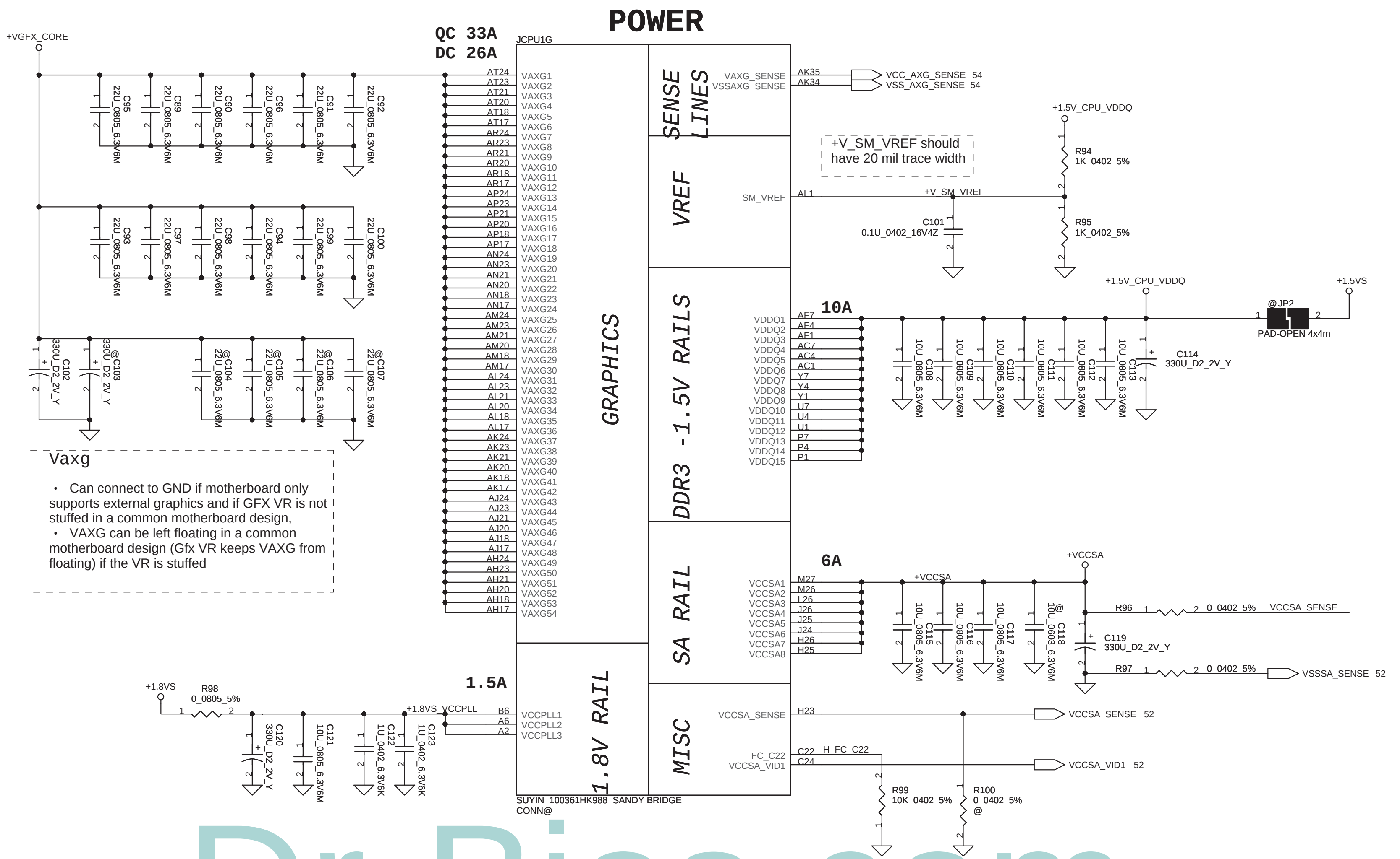

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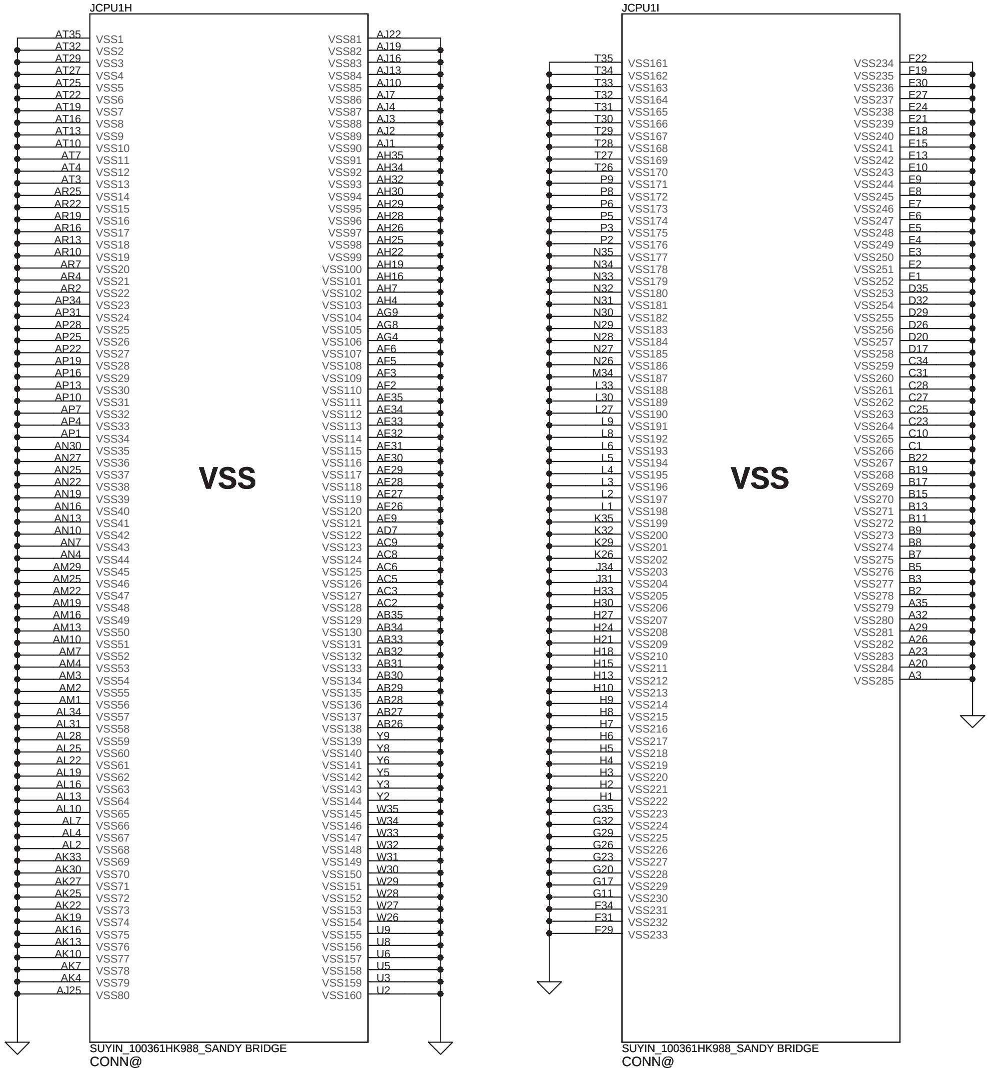

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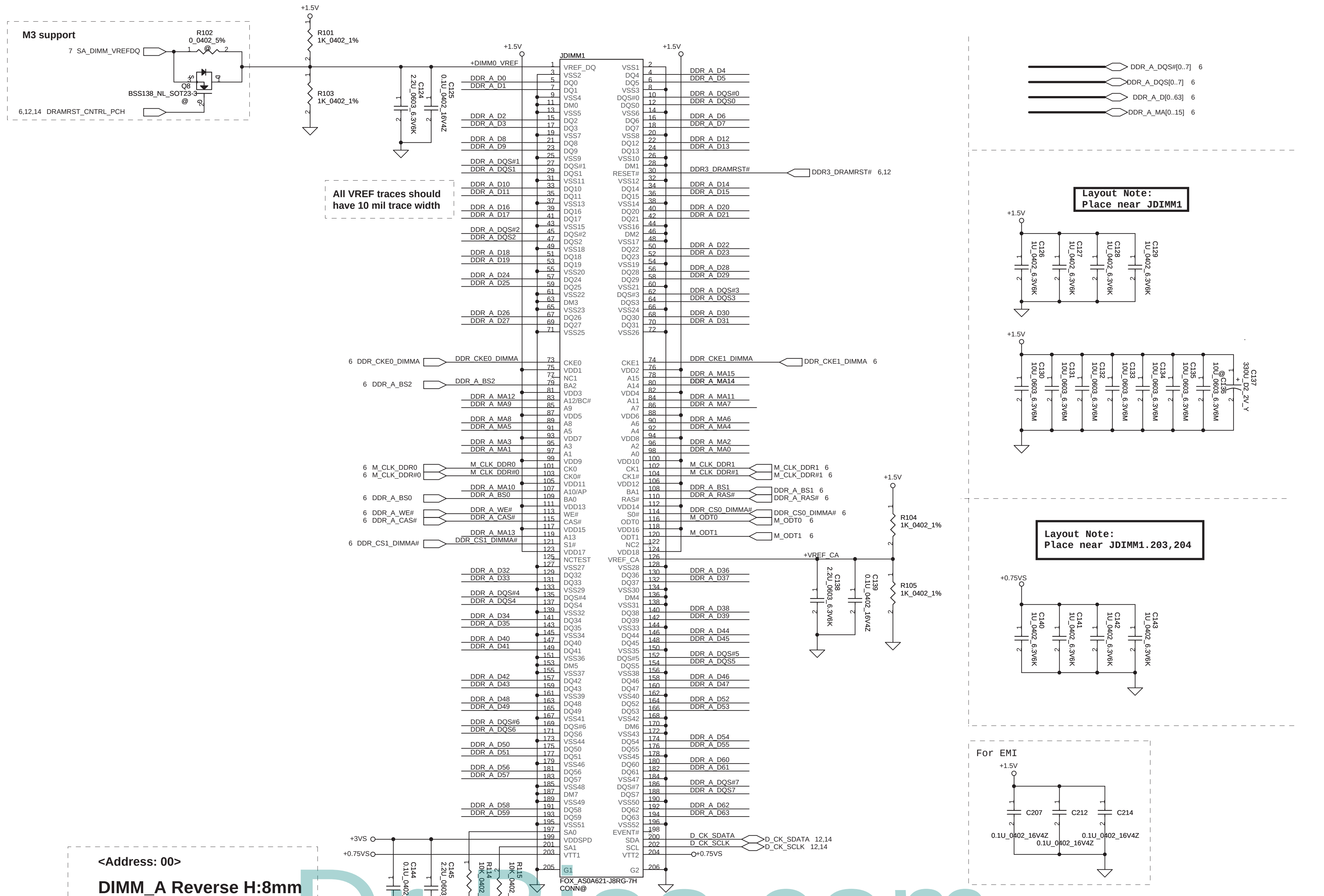

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DIMM_A Reverse H:8mm

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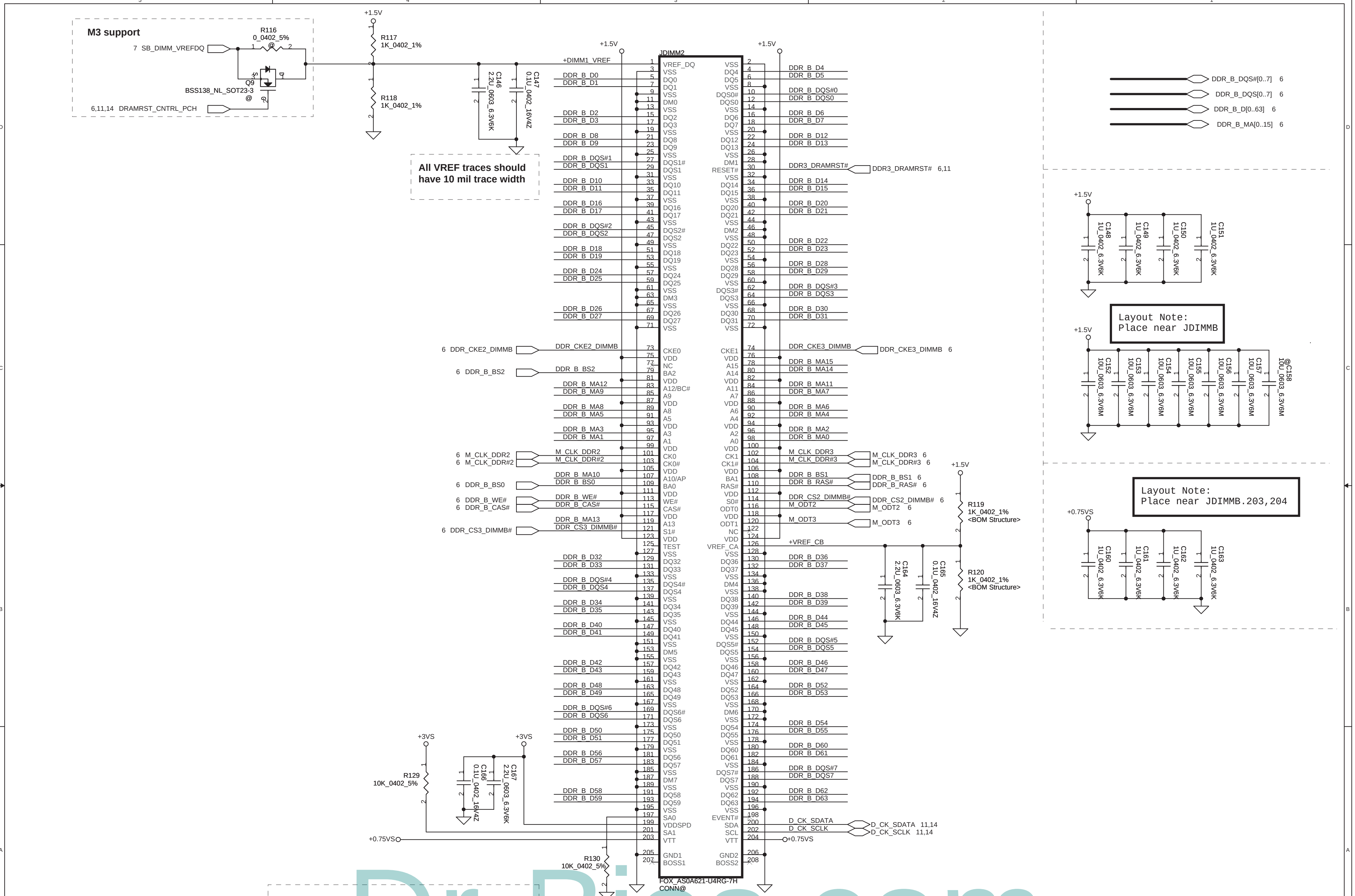

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DIMM_B Reverse type H:4mm

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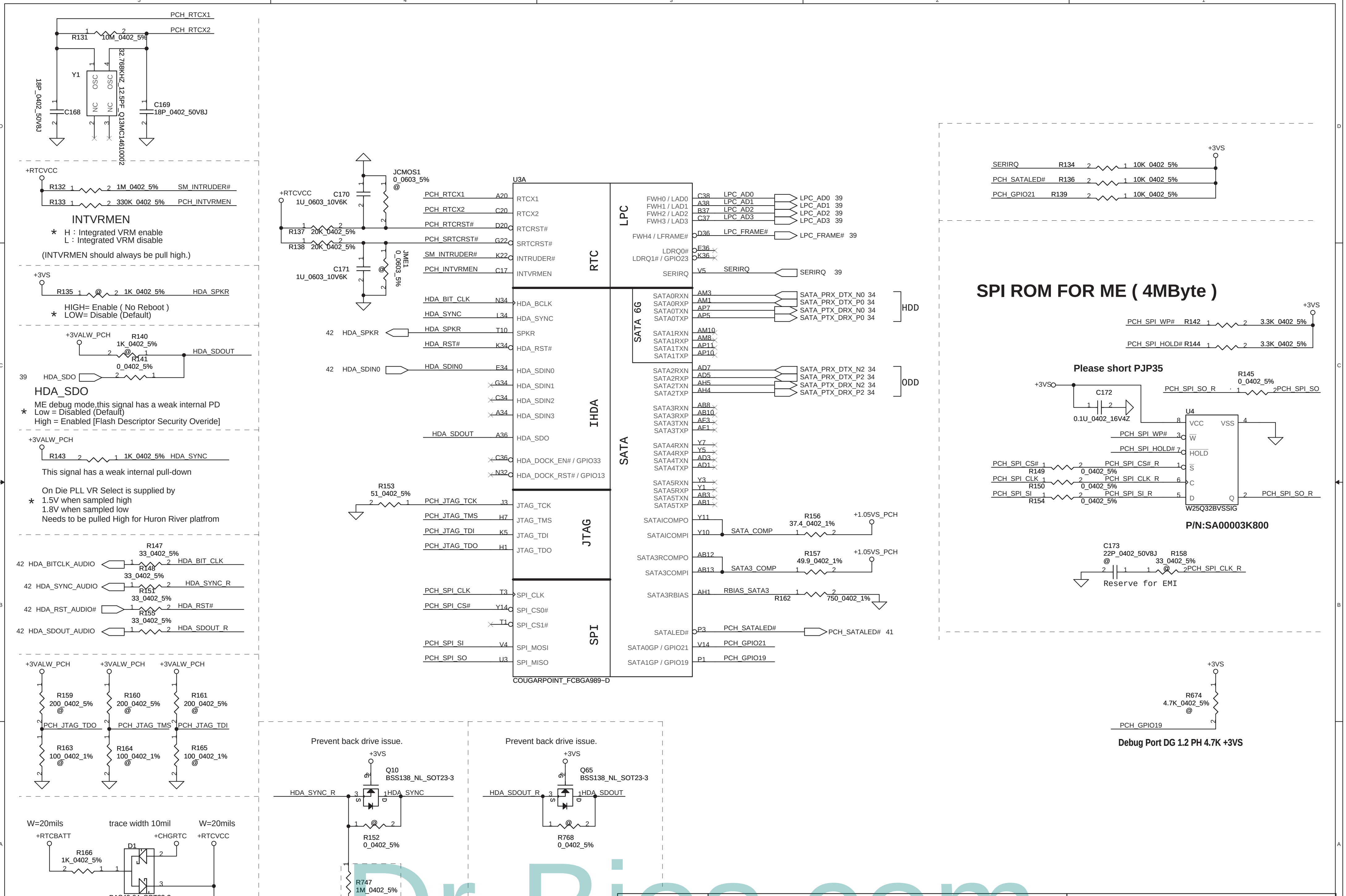

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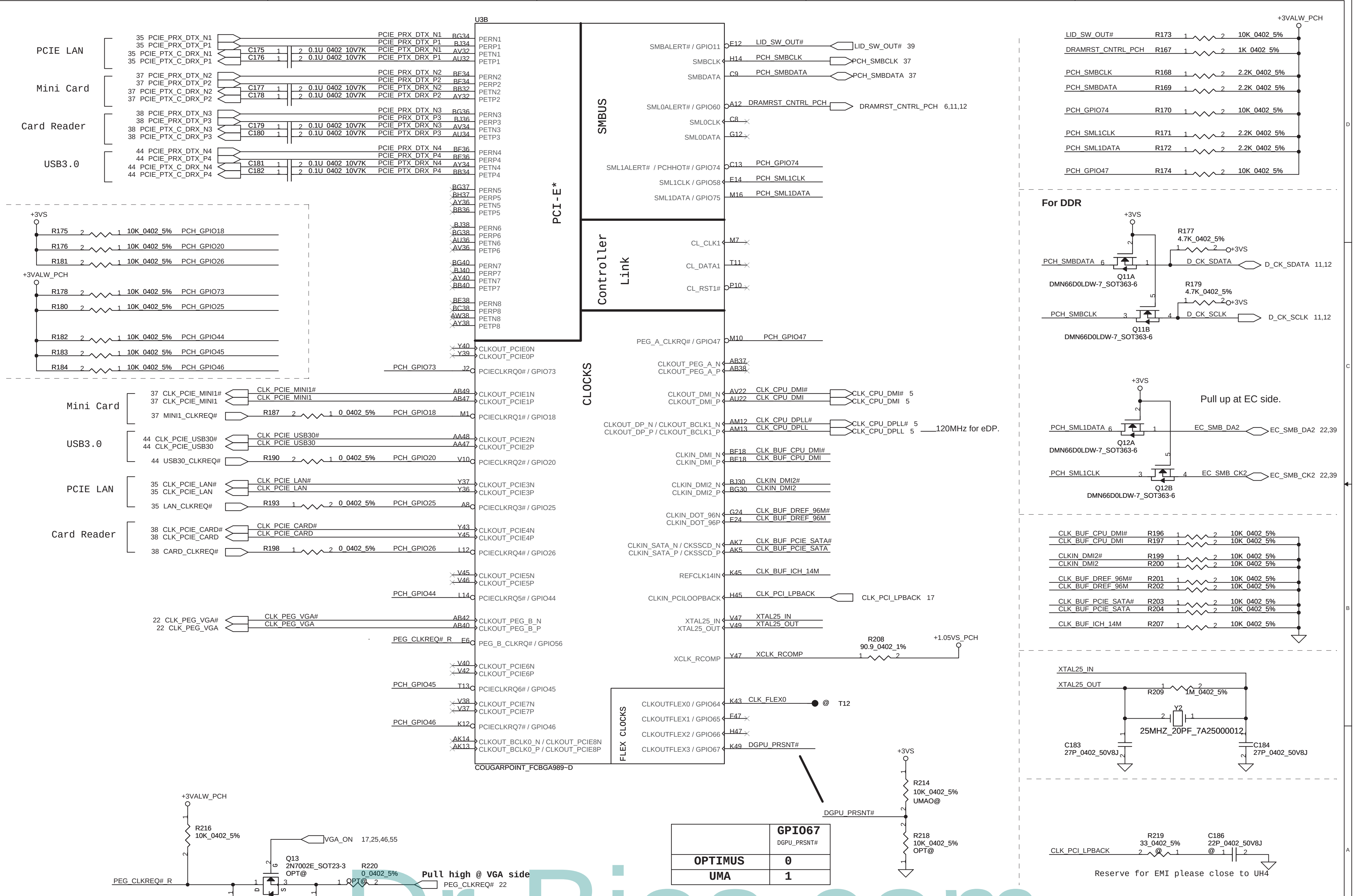

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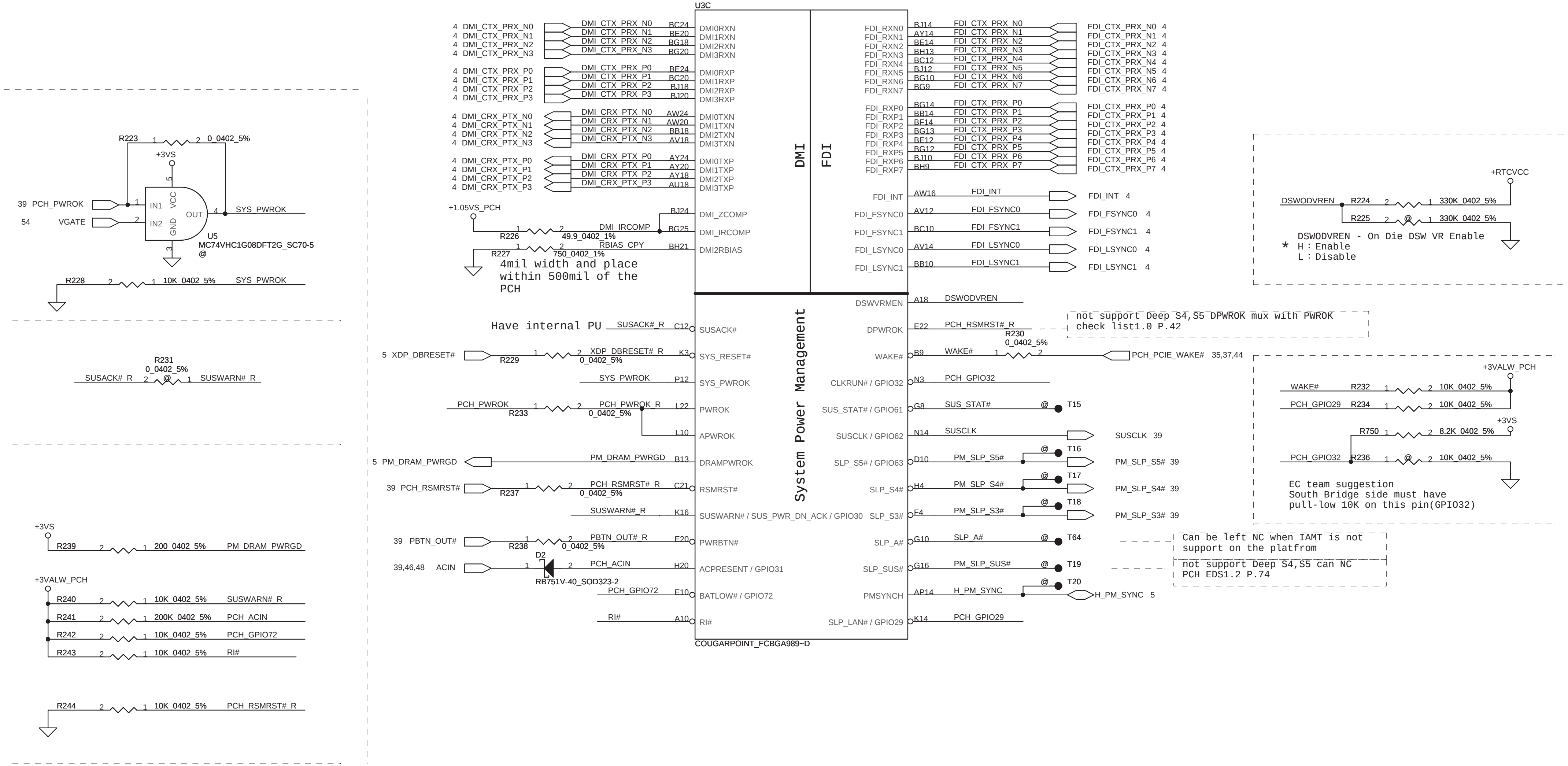

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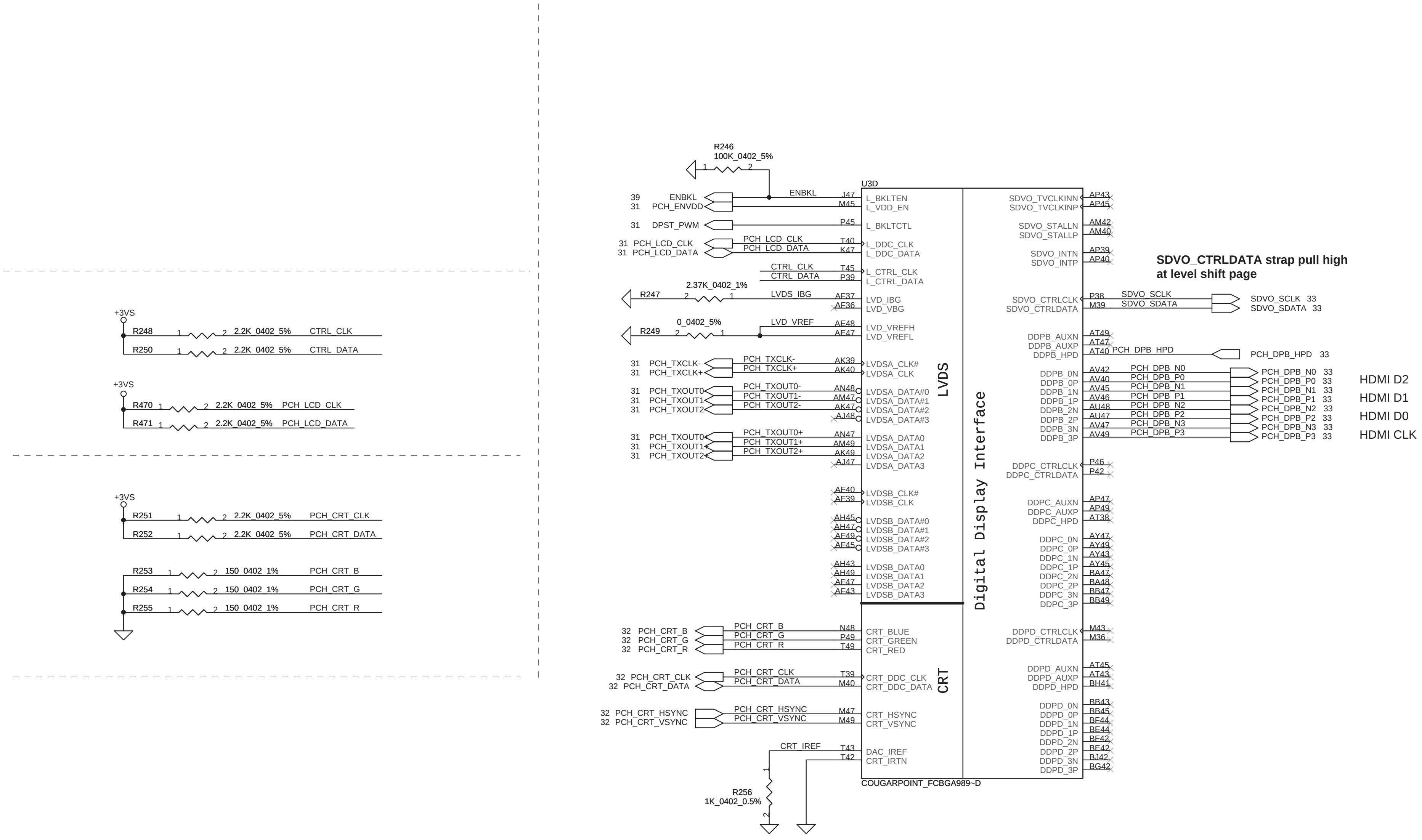

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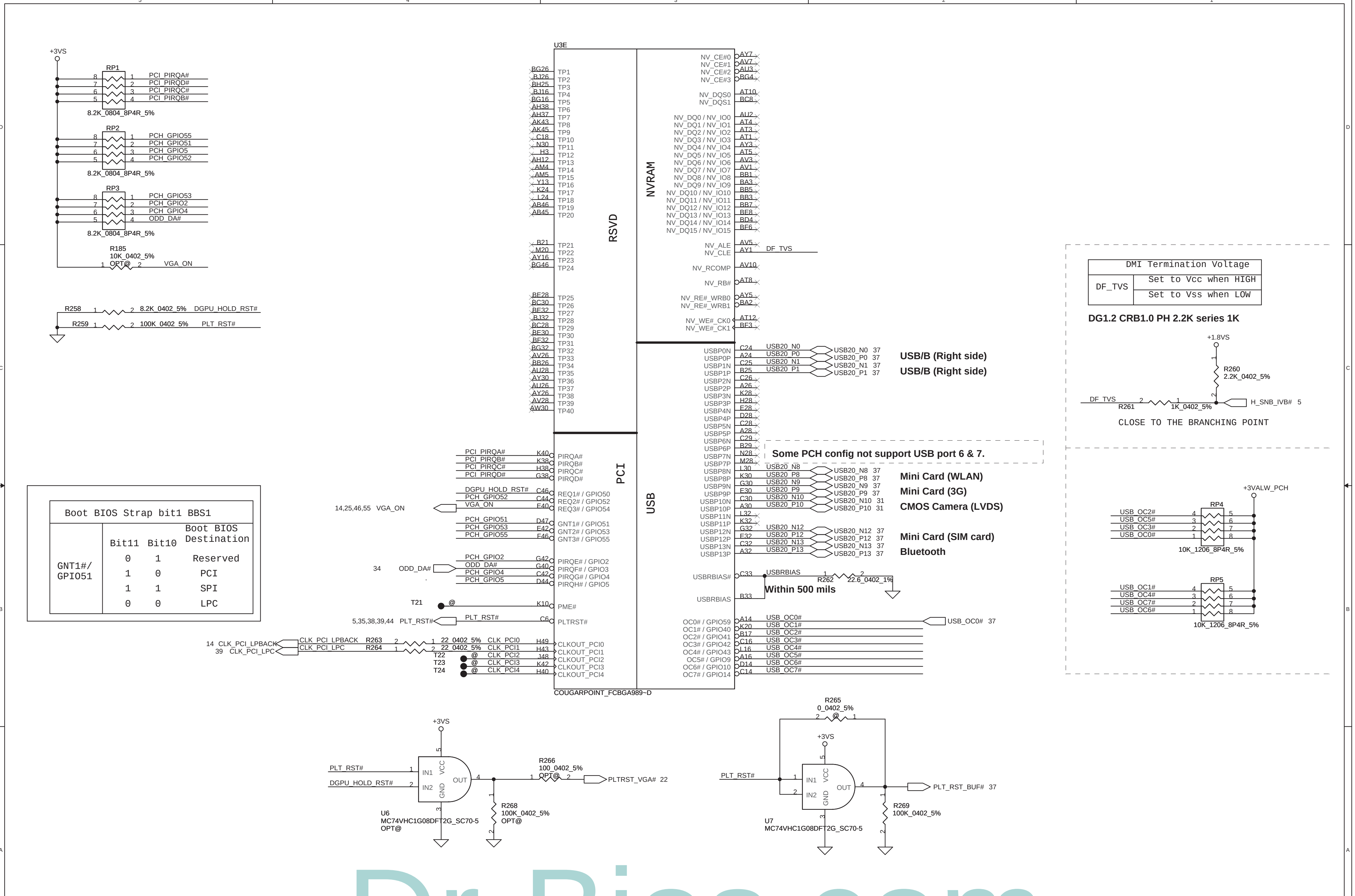
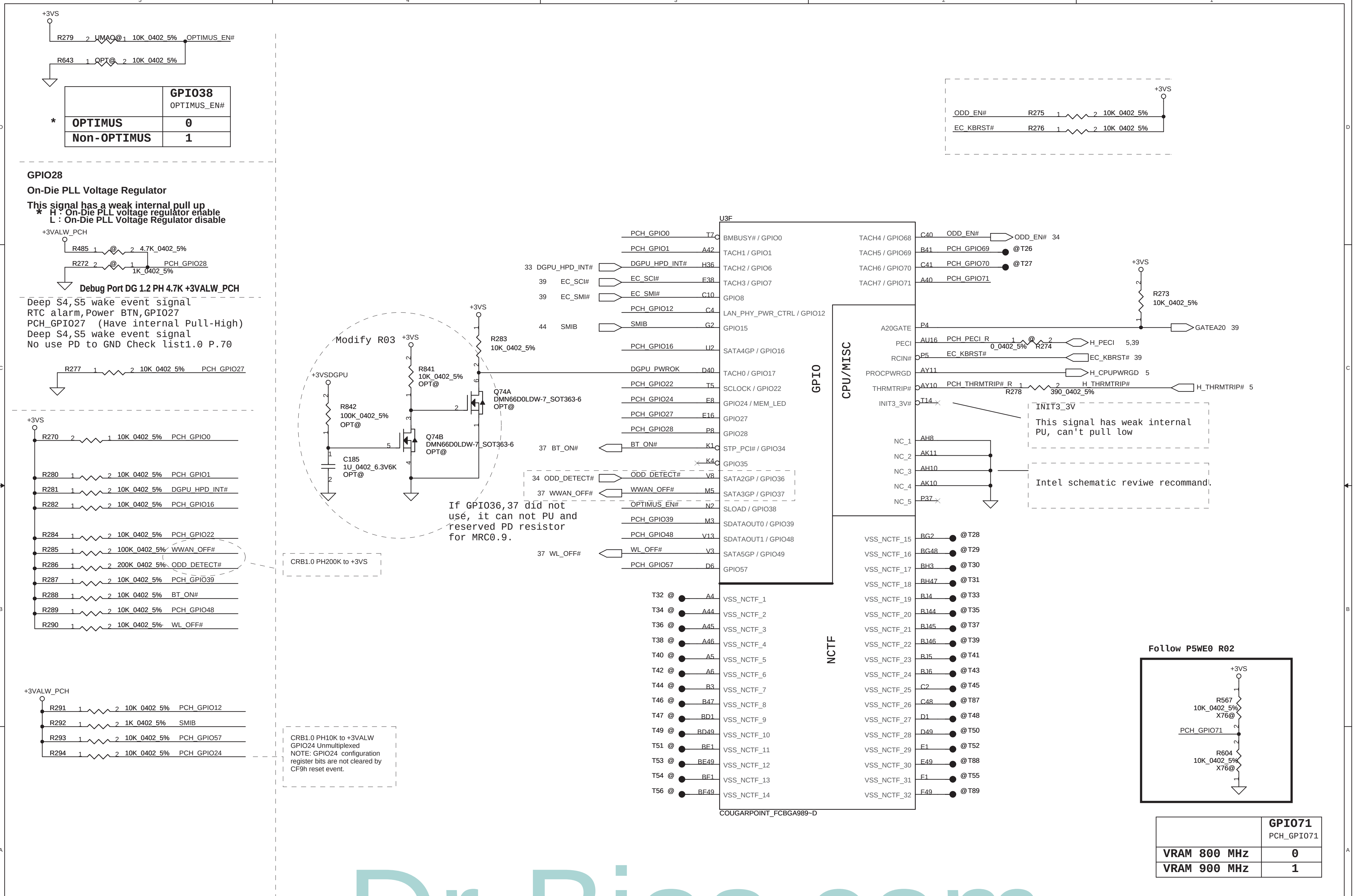


DMI Termination Voltage	
DF_TVS	Set to Vcc when HIGH
	Set to Vss when LOW

Boot BIOS Strap bit1 BBS1

	Bit11	Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC



	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
Non-OPTIMUS	1

	GPIO71 PCH_GPIO71
VRAM 800 MHz	0
VRAM 900 MHz	1

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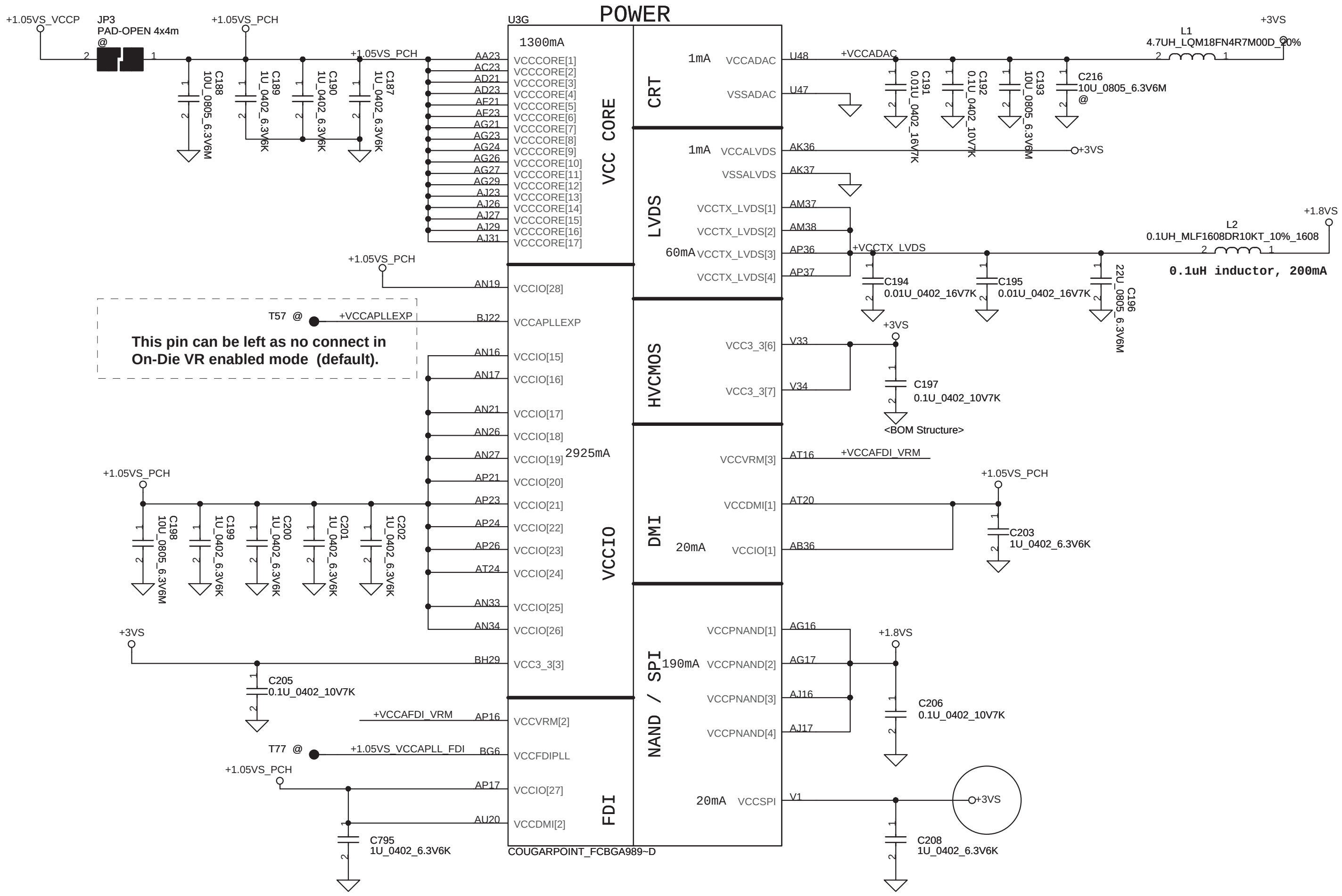

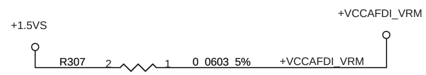

VCCVRM==>1.5V FOR MOBILE
VCCVRM==>1.8V FOR DESKTOP
VCCVRM = 160mA detal waiting for newest spec

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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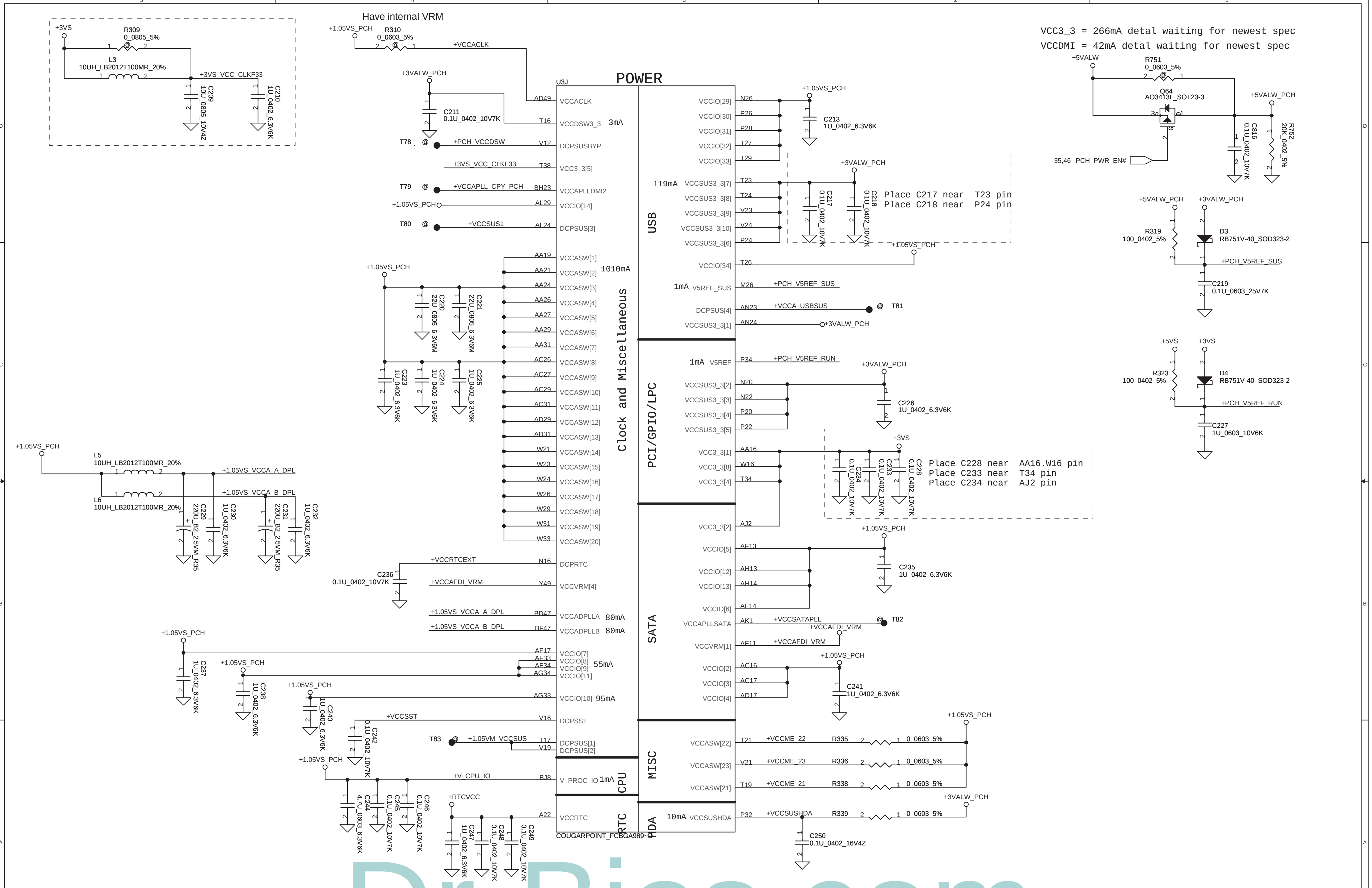

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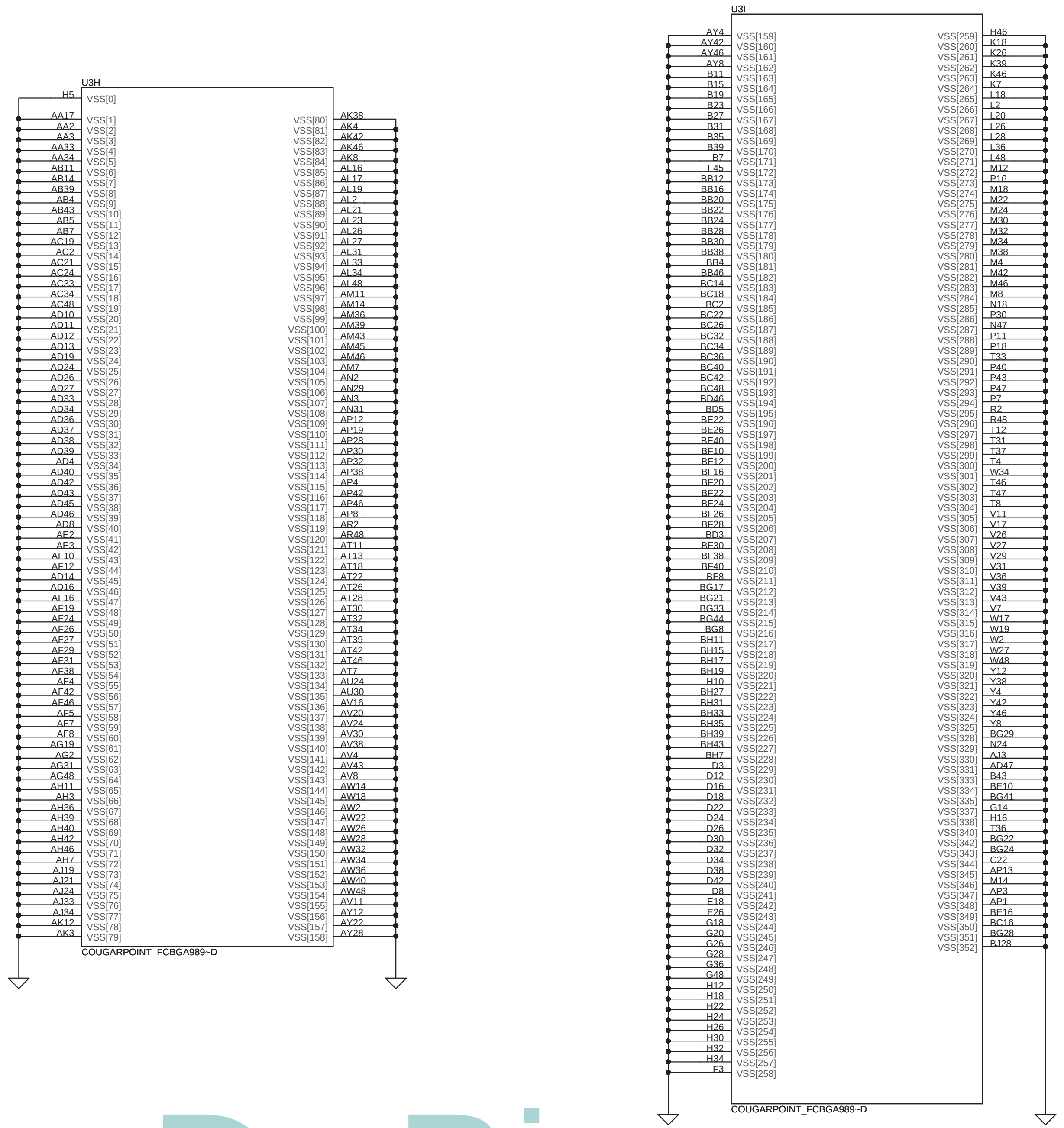

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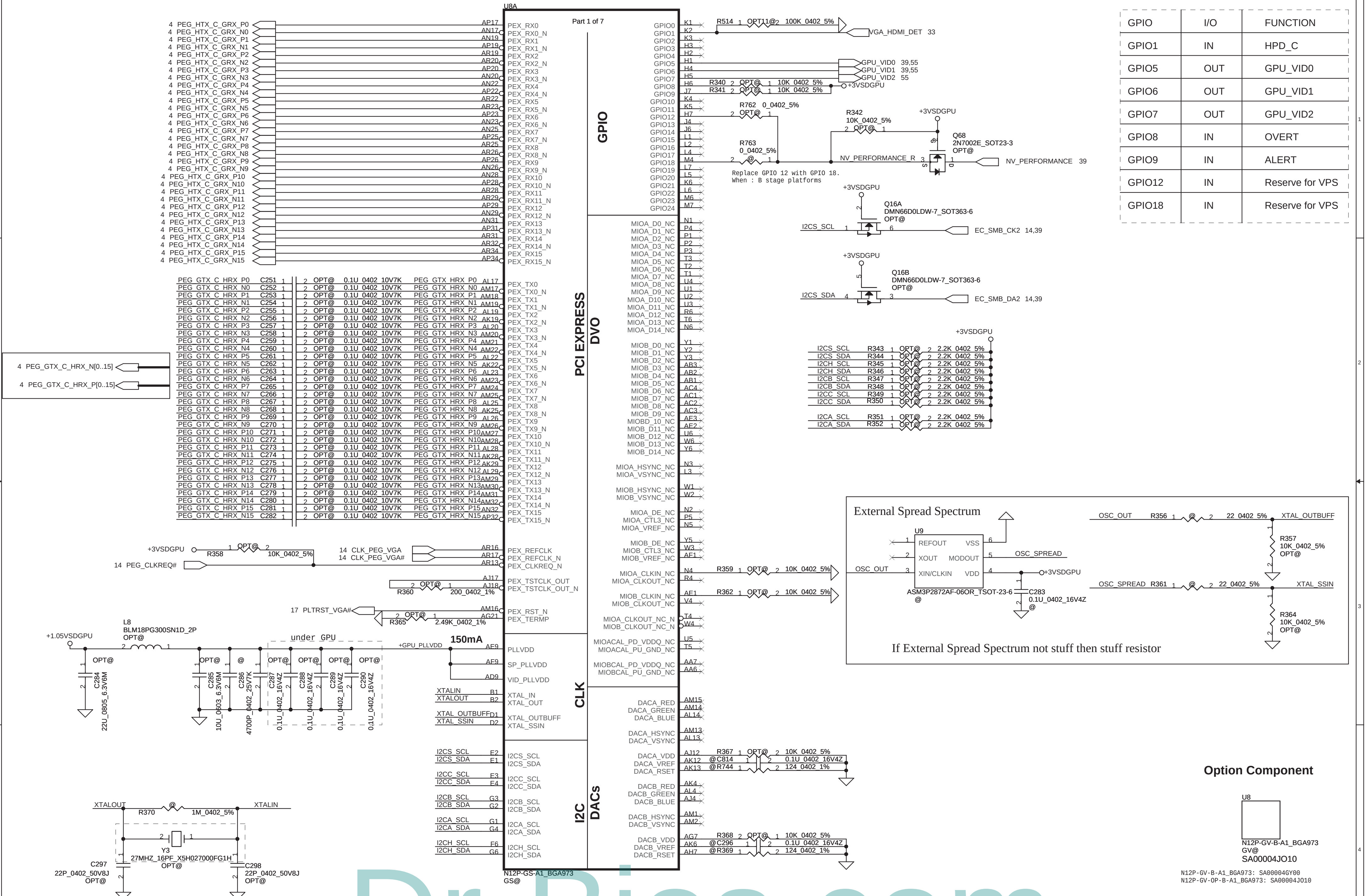

GPIO	I/O	FUNCTION
GPIO1	IN	HPD_C
GPIO5	OUT	GPU_VID0
GPIO6	OUT	GPU_VID1
GPIO7	OUT	GPU_VID2
GPIO8	IN	OVERT
GPIO9	IN	ALERT
GPIO12	IN	Reserve for VPS
GPIO18	IN	Reserve for VPS

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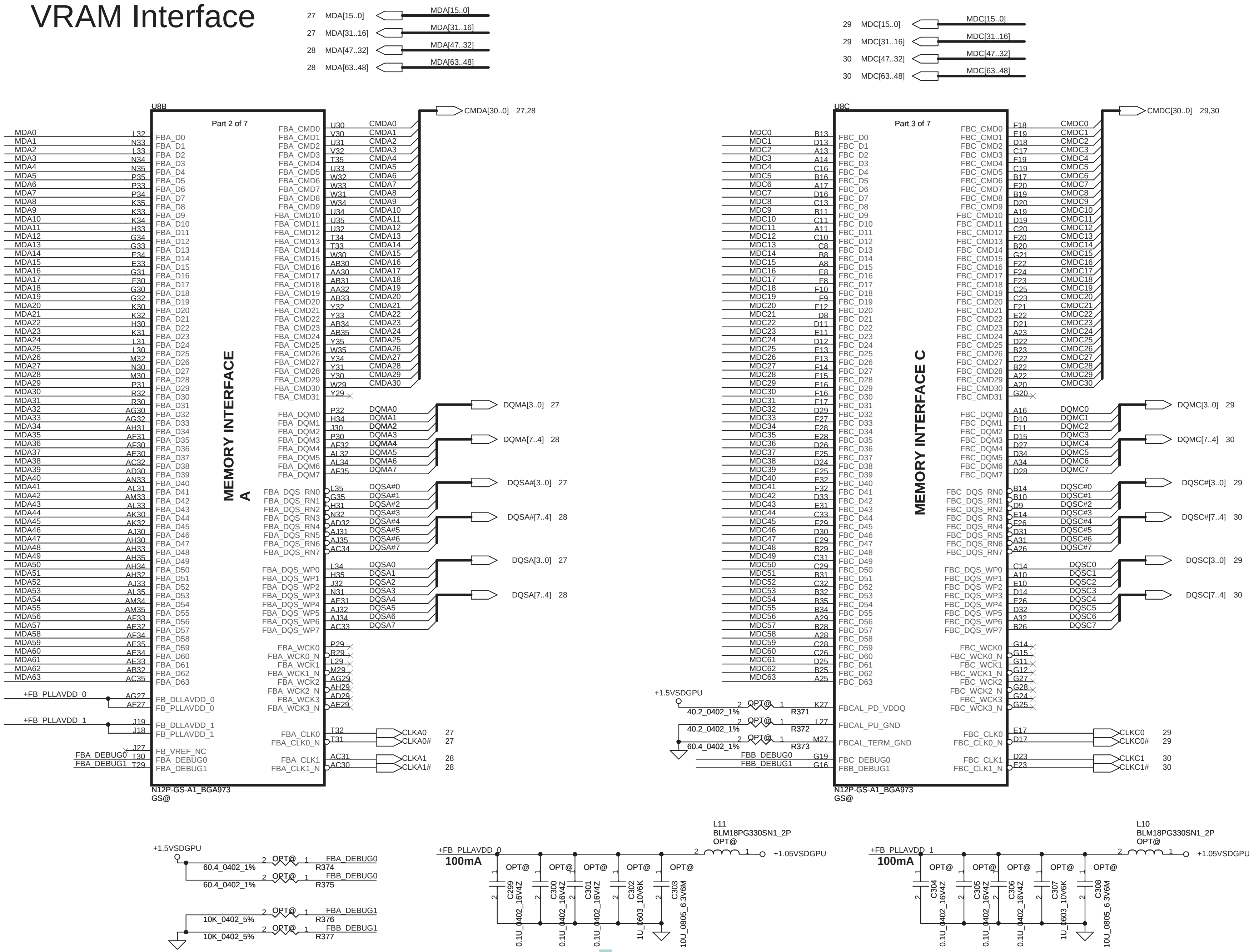
VRAM Interface



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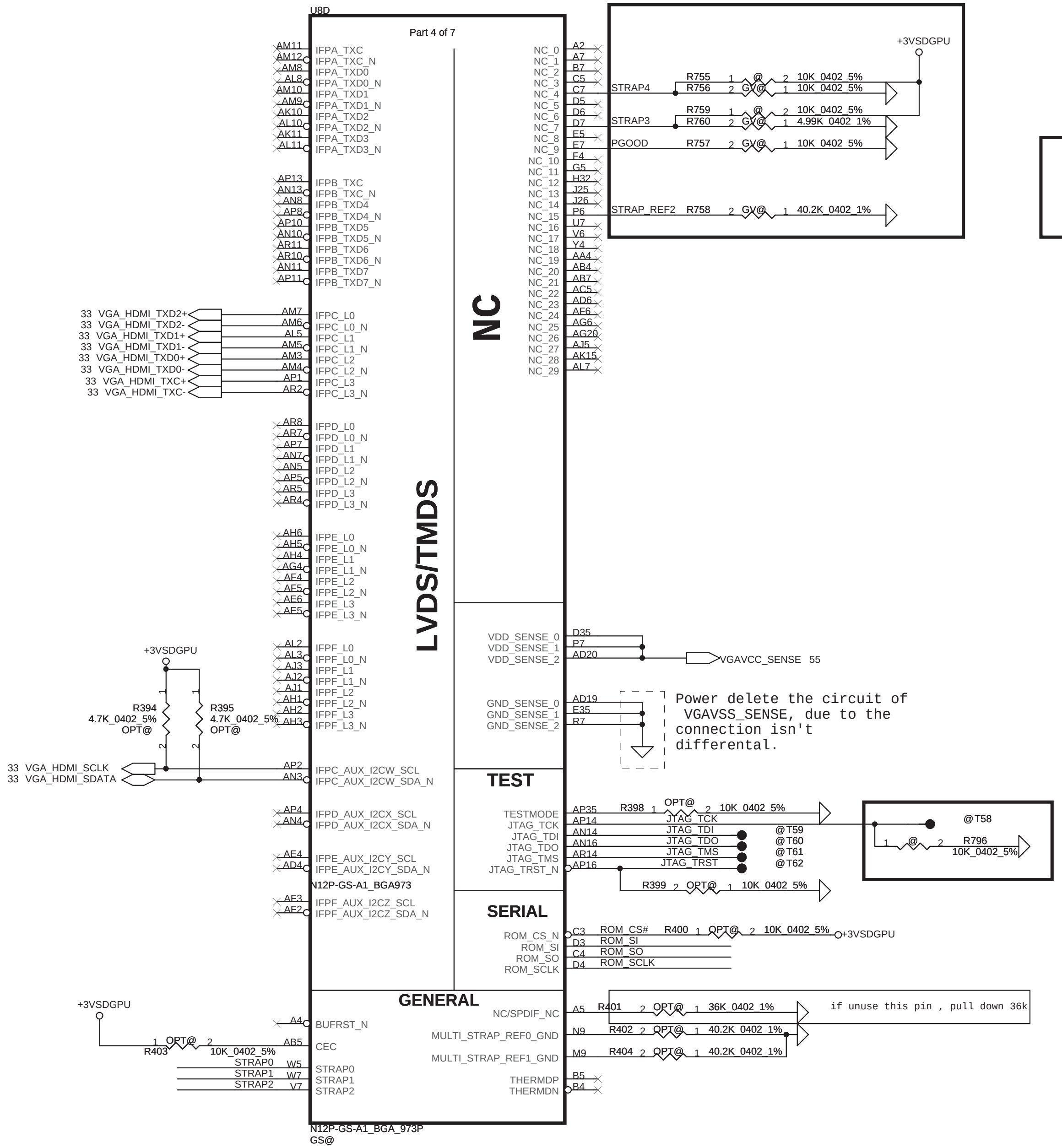
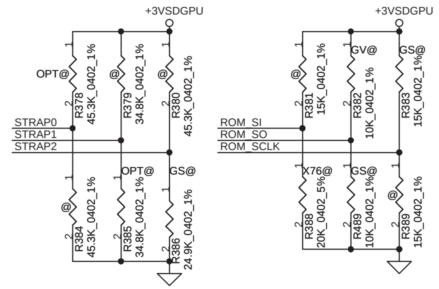
				Date: Friday, March 04, 2011; Sheet 23 of 57

For GB2-128 & GB2b-128 colayout....



MULTI LEVEL STRAPS



Option Component

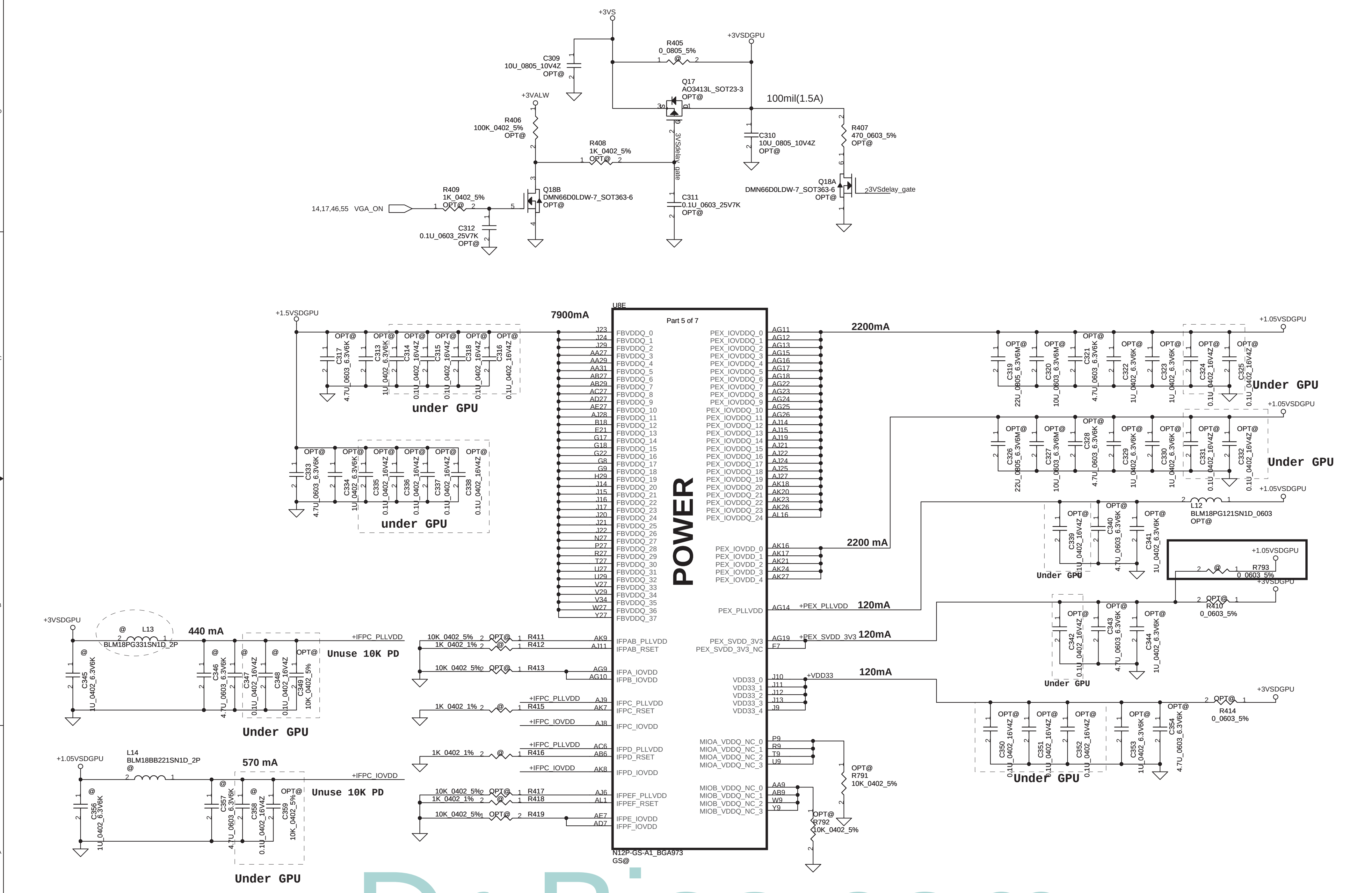
ROM_SCLK ---> R383 2 GV@ 1 4.99K_0402_1%
STRAP2 ---> R386 2 GV@ 1 4.99K_0402_1%

For N12P-GS strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R378 PU 45K	R385 PD 35K	R386 PD 25K	NC	NC	R388 PD 15K	R489 PD 10K	R383 PU 15K
N12P-GS	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS10	R378 PU 45K	R385 PD 35K	R386 PD 25K	NC	NC	R388 PD 20K	R489 PD 10K	R383 PU 15K
N12P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R378 PU 45K	R385 PD 35K	R386 PD 25K	NC	NC	R388 PD 35K	R489 PD 10K	R383 PU 15K
N12P-GS	900 MHz	128M* 16* 8 2GB	Samsung SA000047Q20	R378 PU 45K	R385 PD 35K	R386 PD 25K	NC	NC	R388 PD 45K	R489 PD 10K	R383 PU 15K

For N12P-GV-OP-B-A1 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GV OP-B-A1	900 MHz	64M* 16* 4 512MB	Hynix SA000041S40	R378 PU 45K	R385 PD 35K	R386 PD 5K	R760 PD 5K	R756 PD 10K	R388 PD 15K	R382 PU 10K	R383 PU 5K
N12P-GV OP-B-A1	900 MHz	64M* 16* 4 512MB	Samsung SA00004GS10	R378 PU 45K	R385 PD 35K	R386 PD 5K	R760 PD 5K	R756 PD 10K	R388 PD 20K	R382 PU 10K	R383 PU 5K



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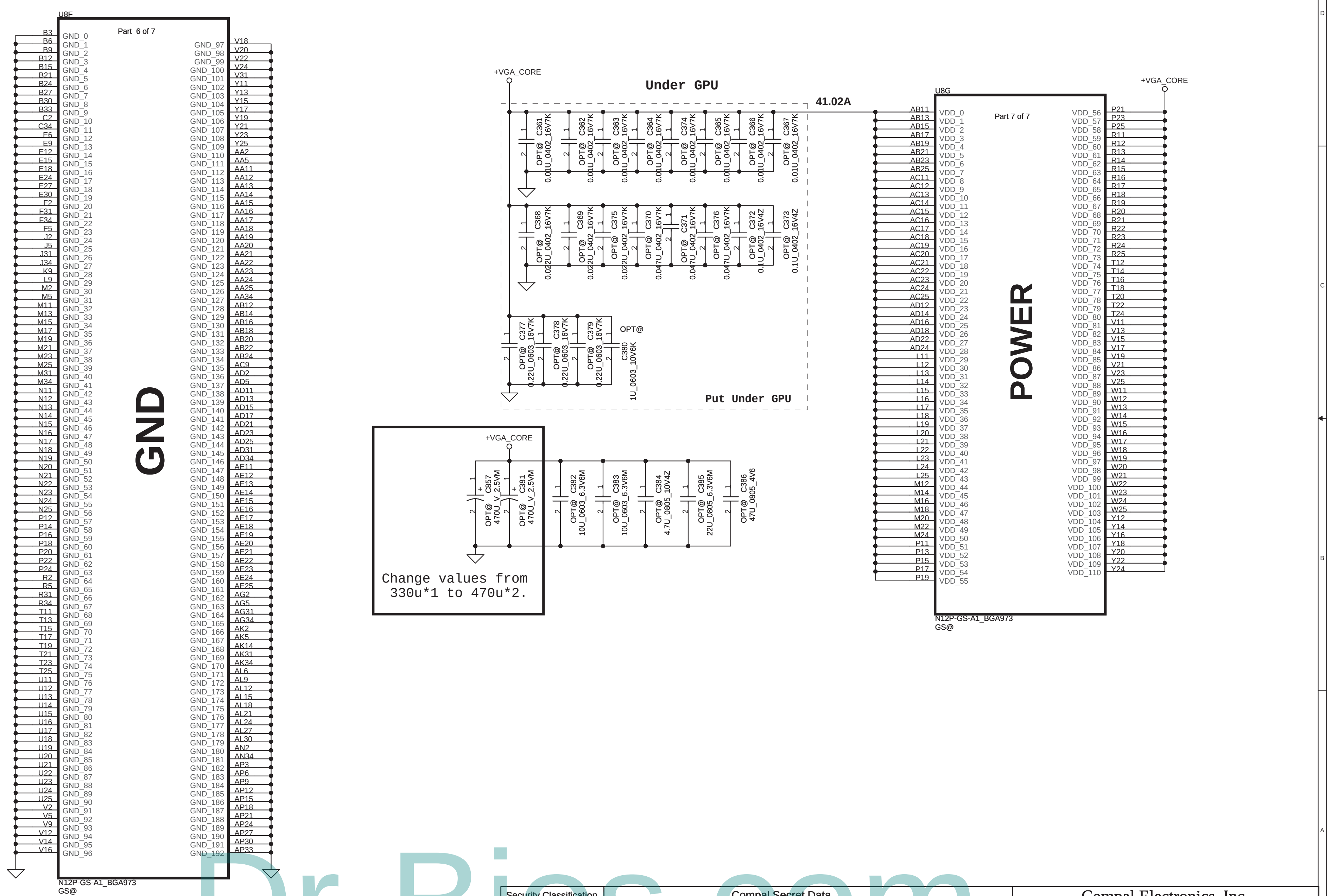
			Date: Friday, March 04, 2011; Sheet 25 of 57



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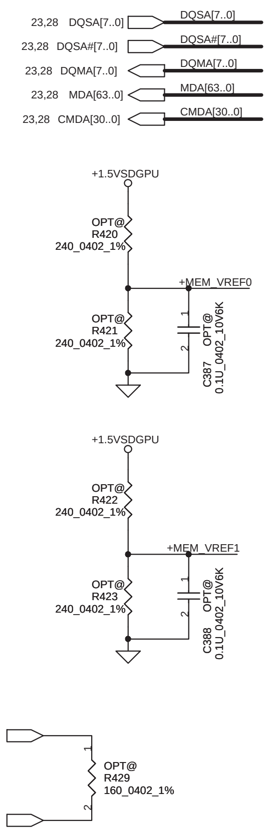
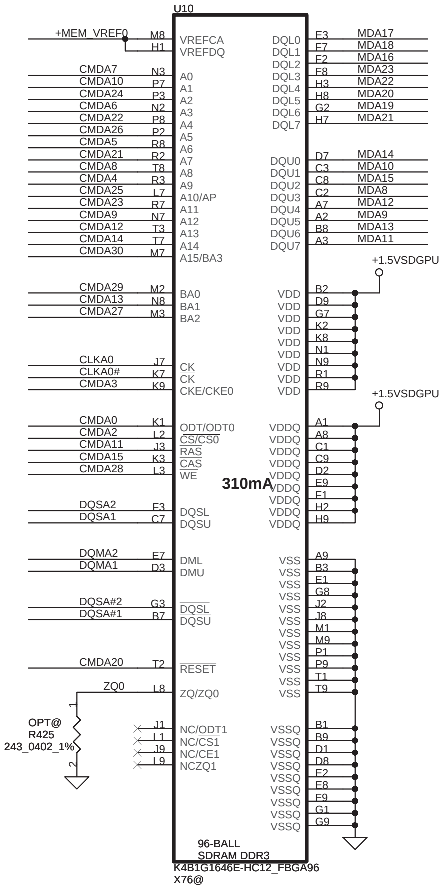
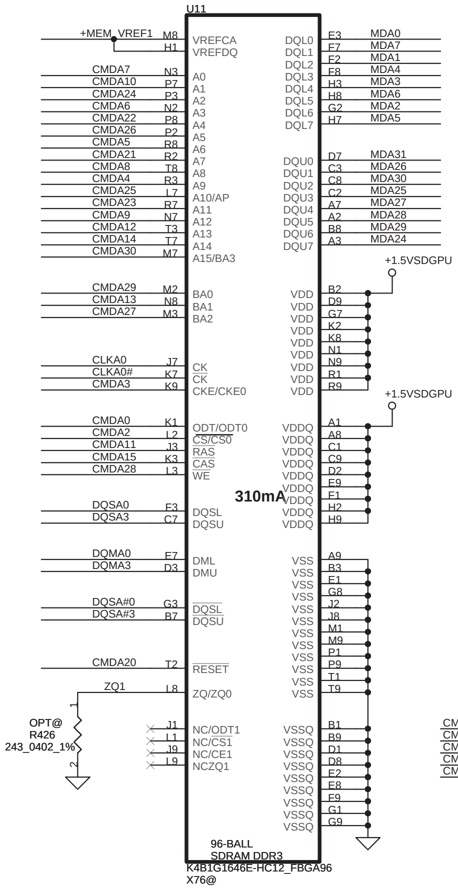
VRAM DDR3 chips (1GB)

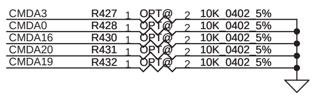
64Mx16 DDR3 *8==>1GB



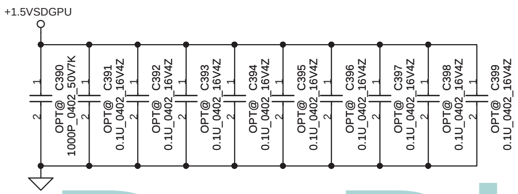


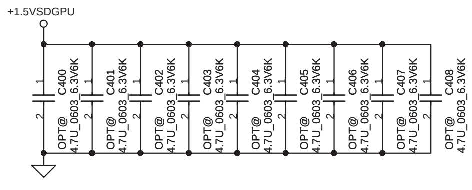


Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





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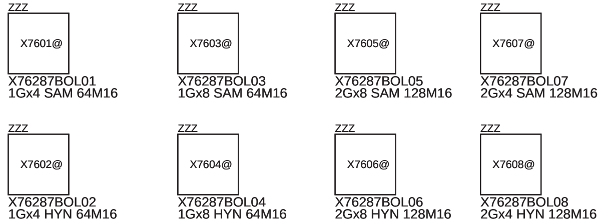

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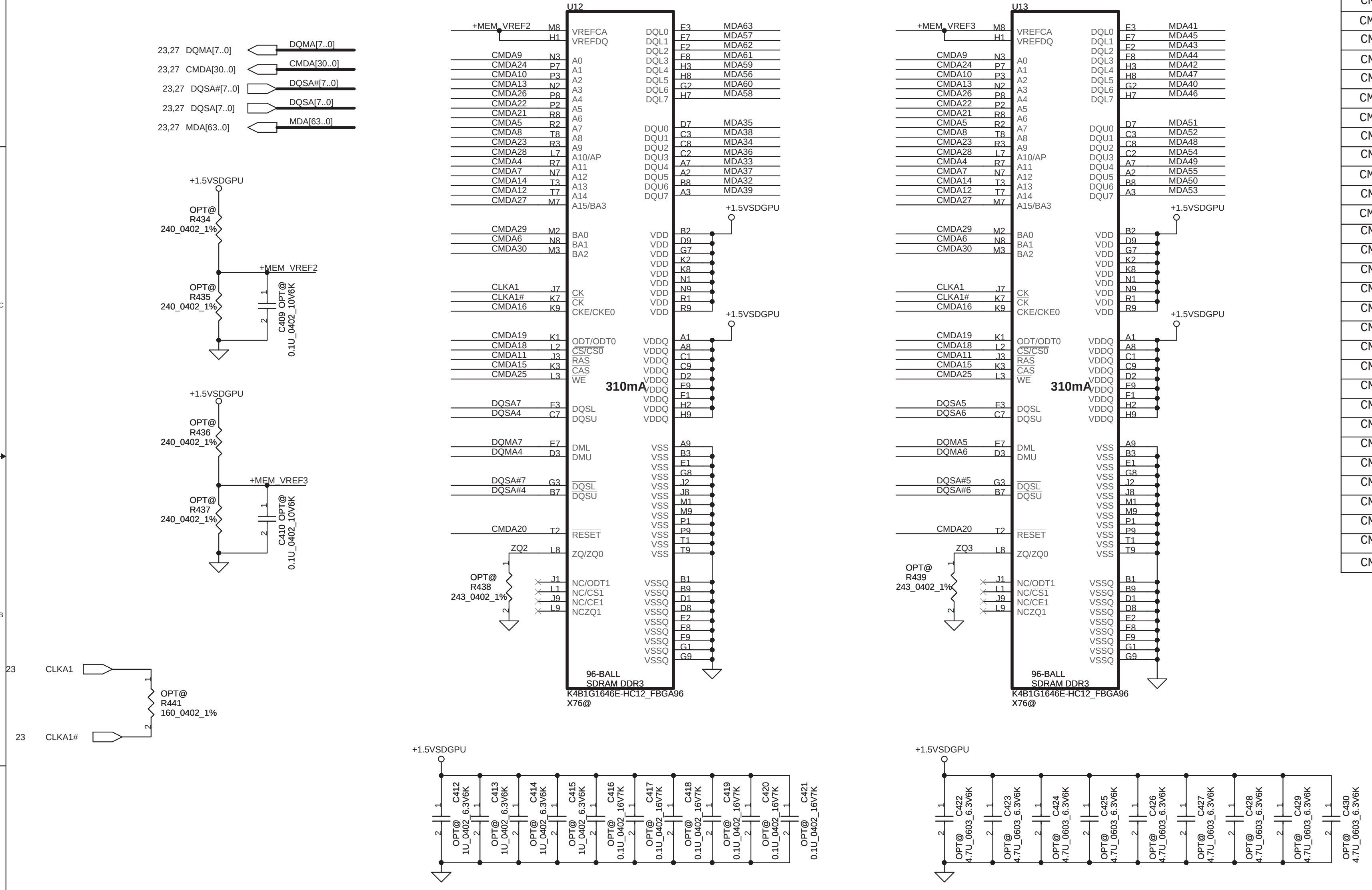
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

Security Classification	Compal Secret Data		
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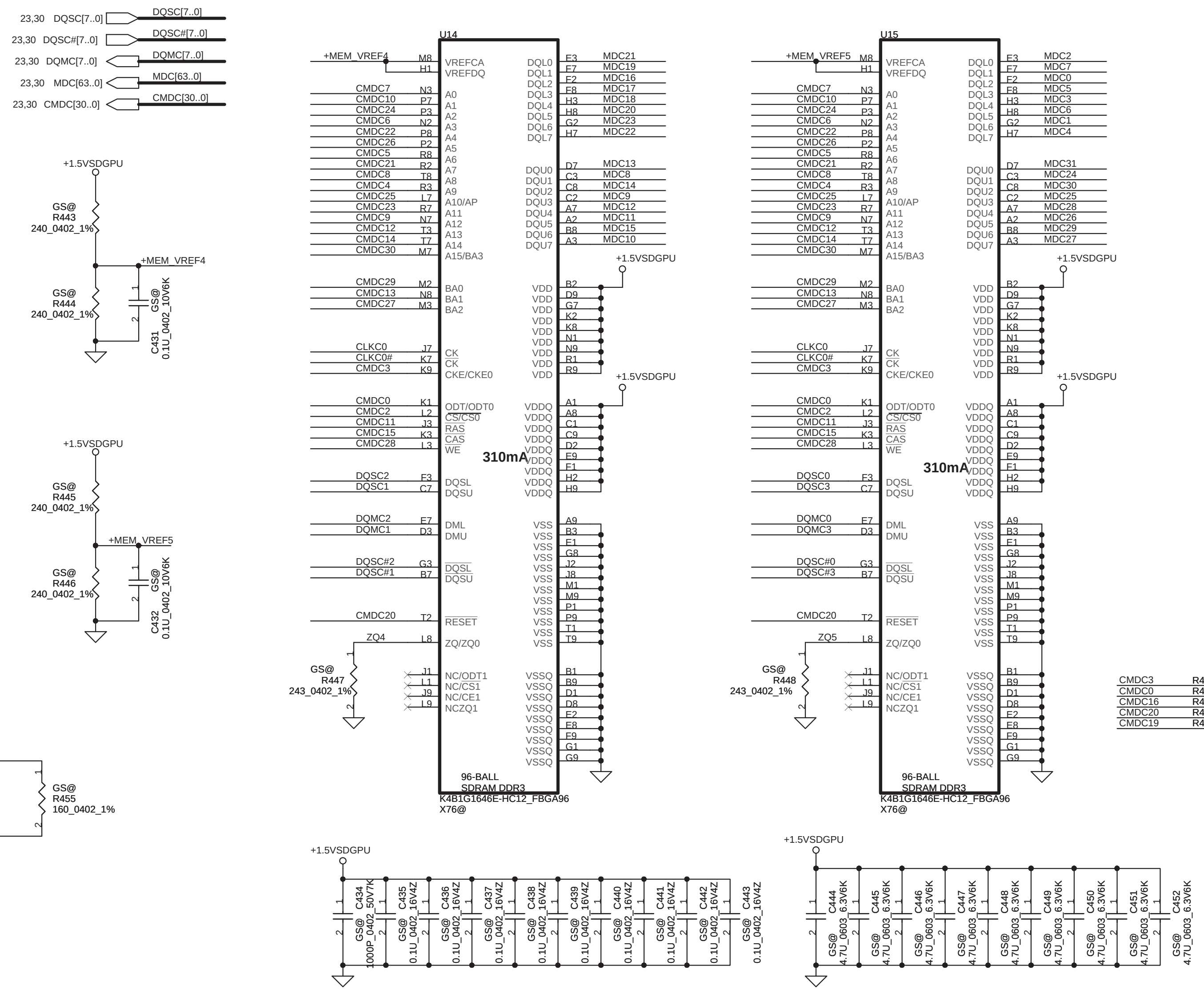
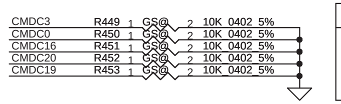
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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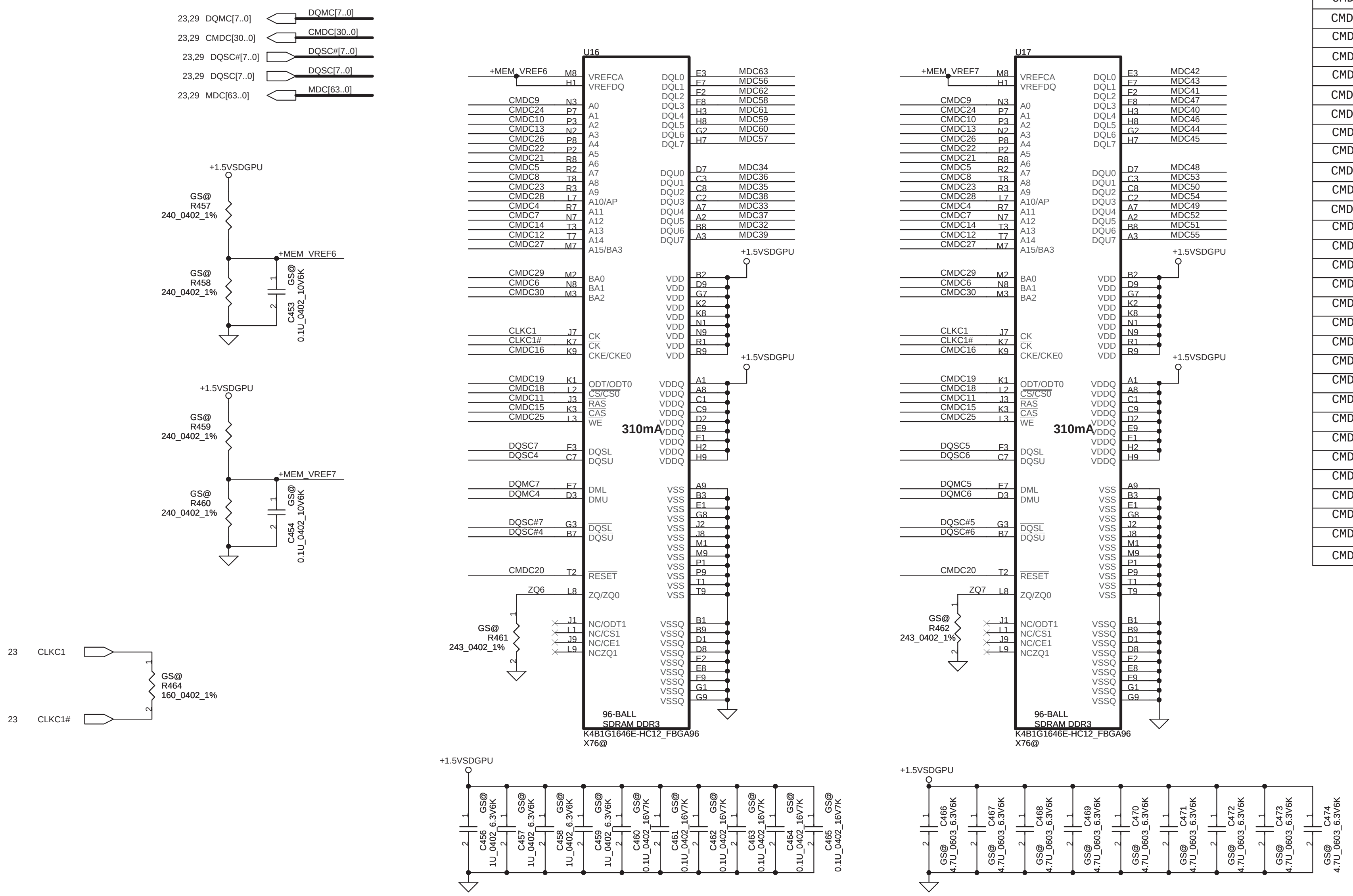
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

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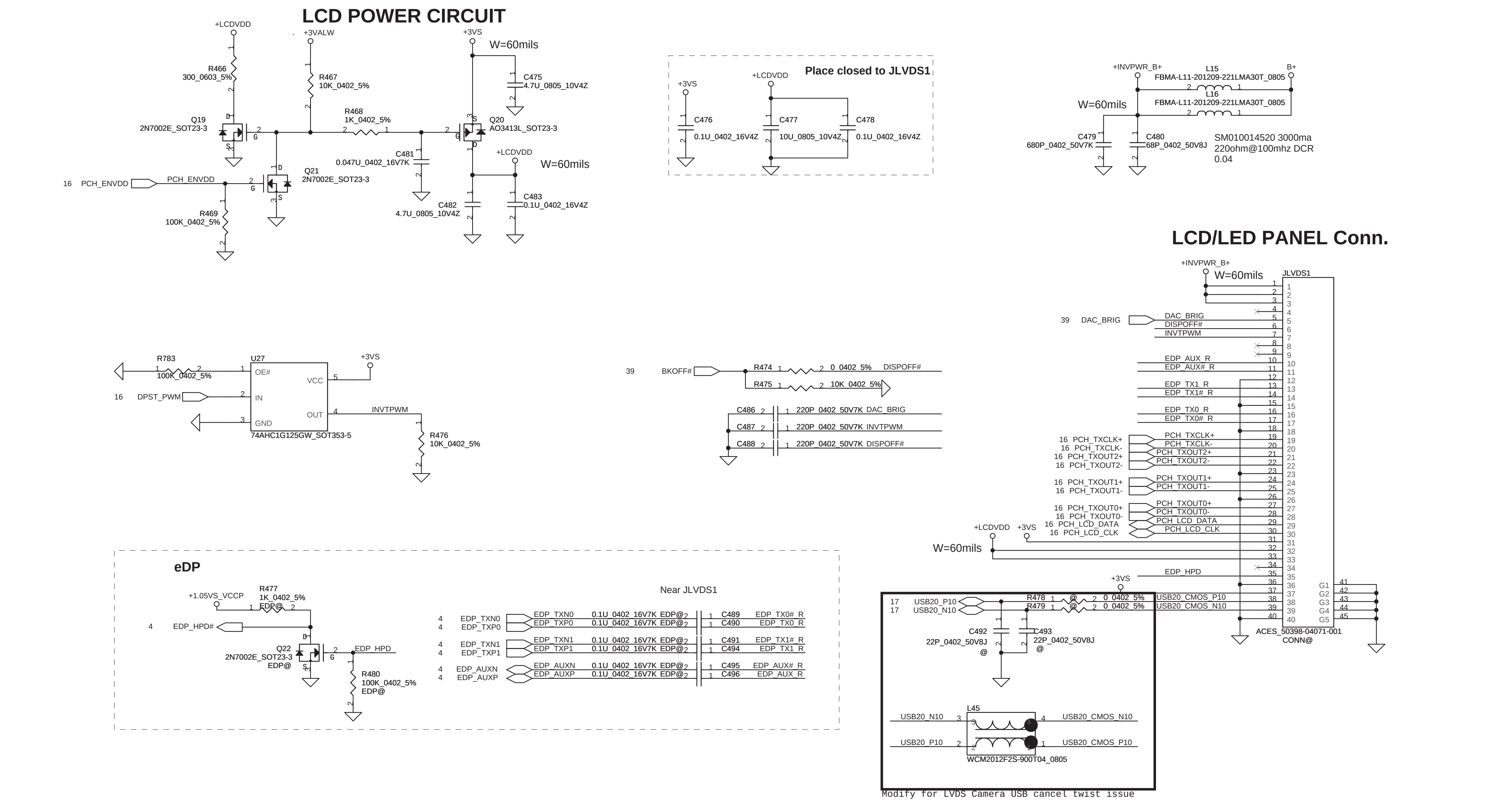

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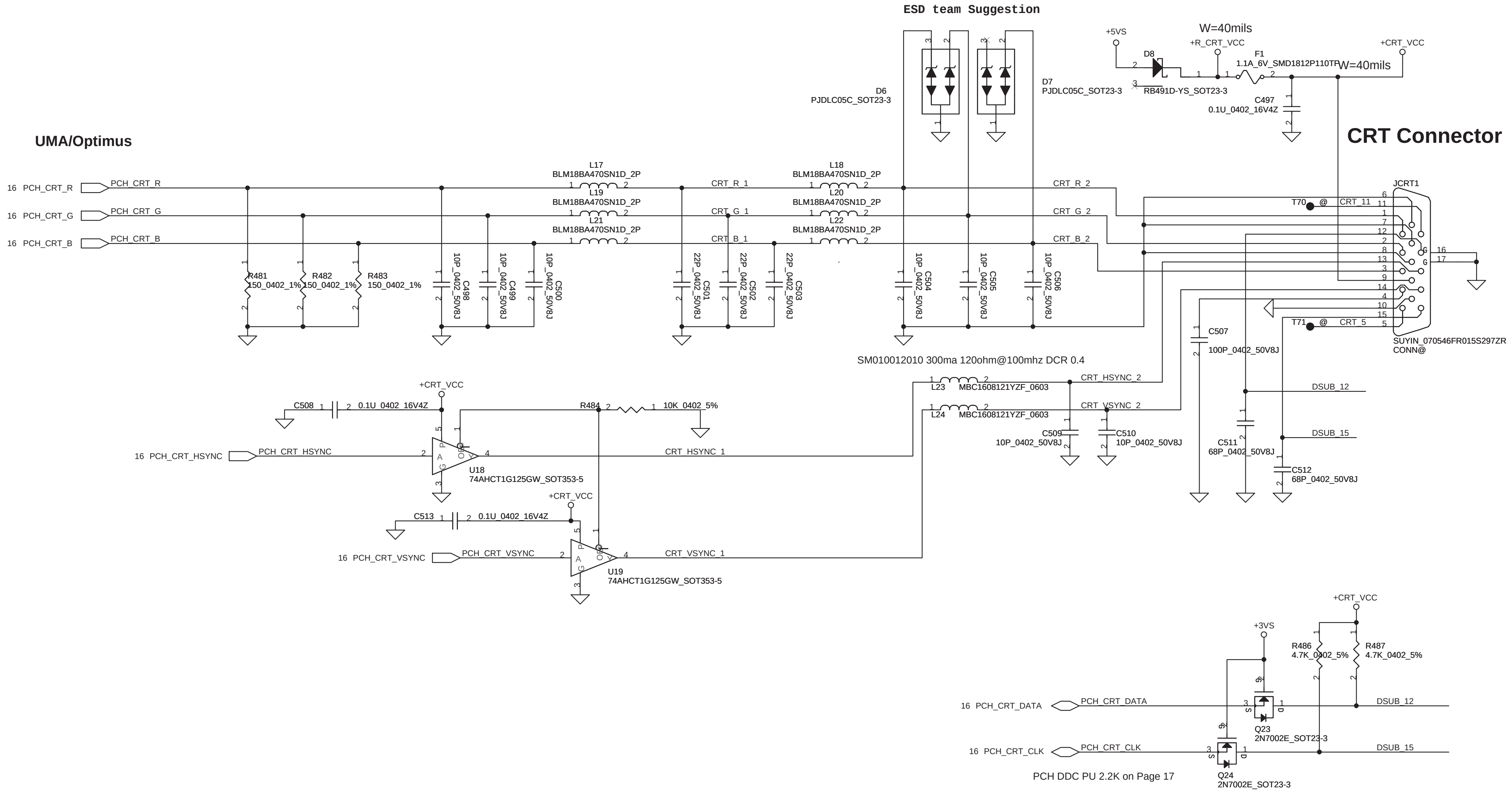

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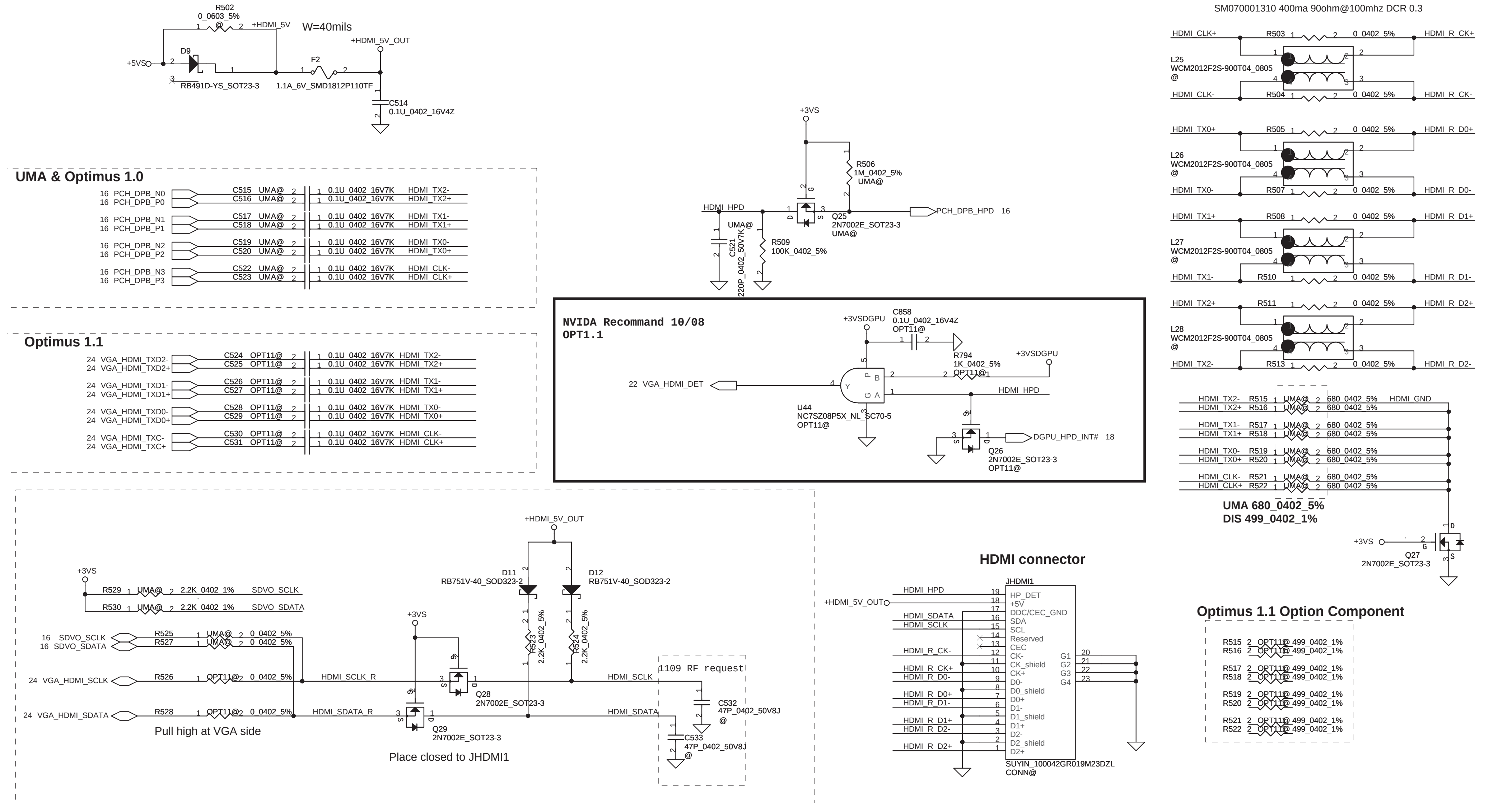

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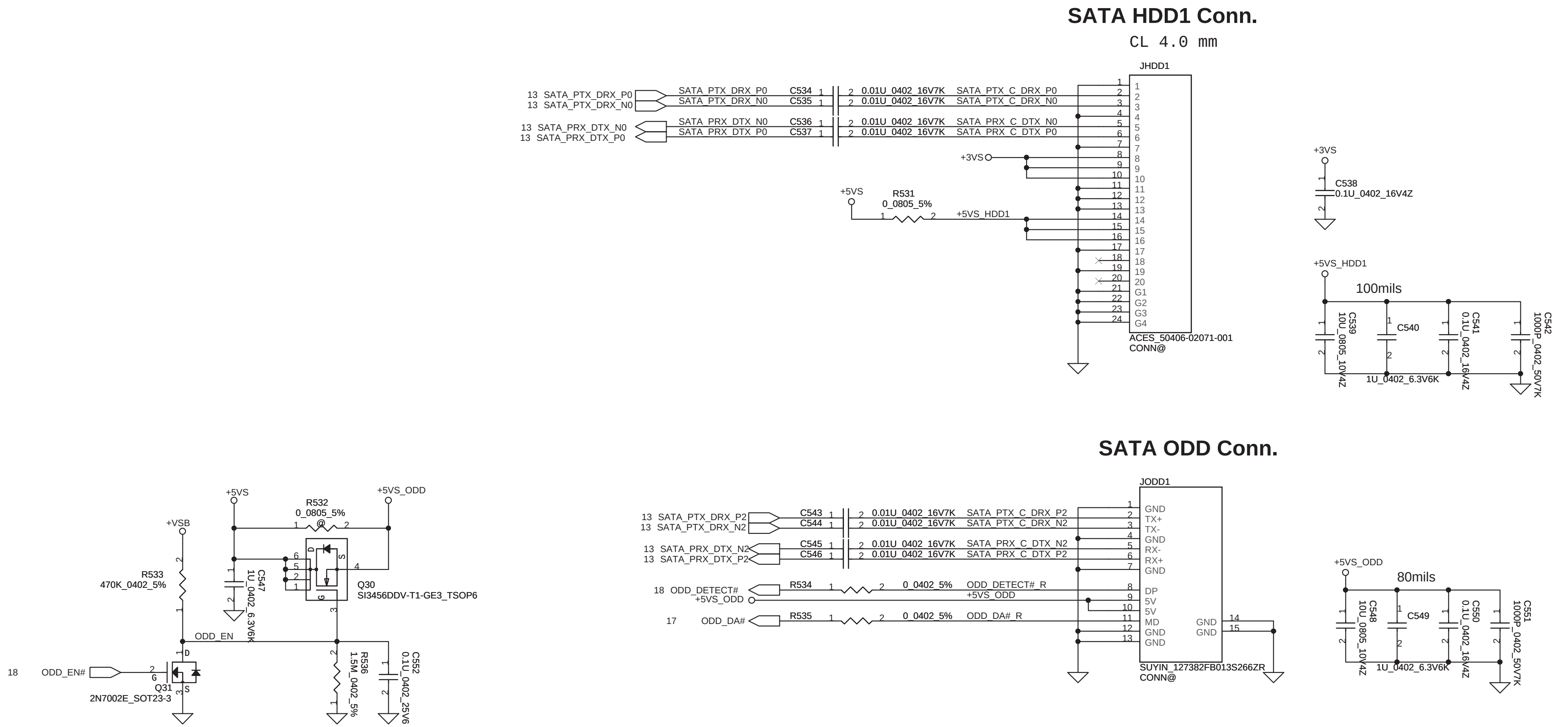

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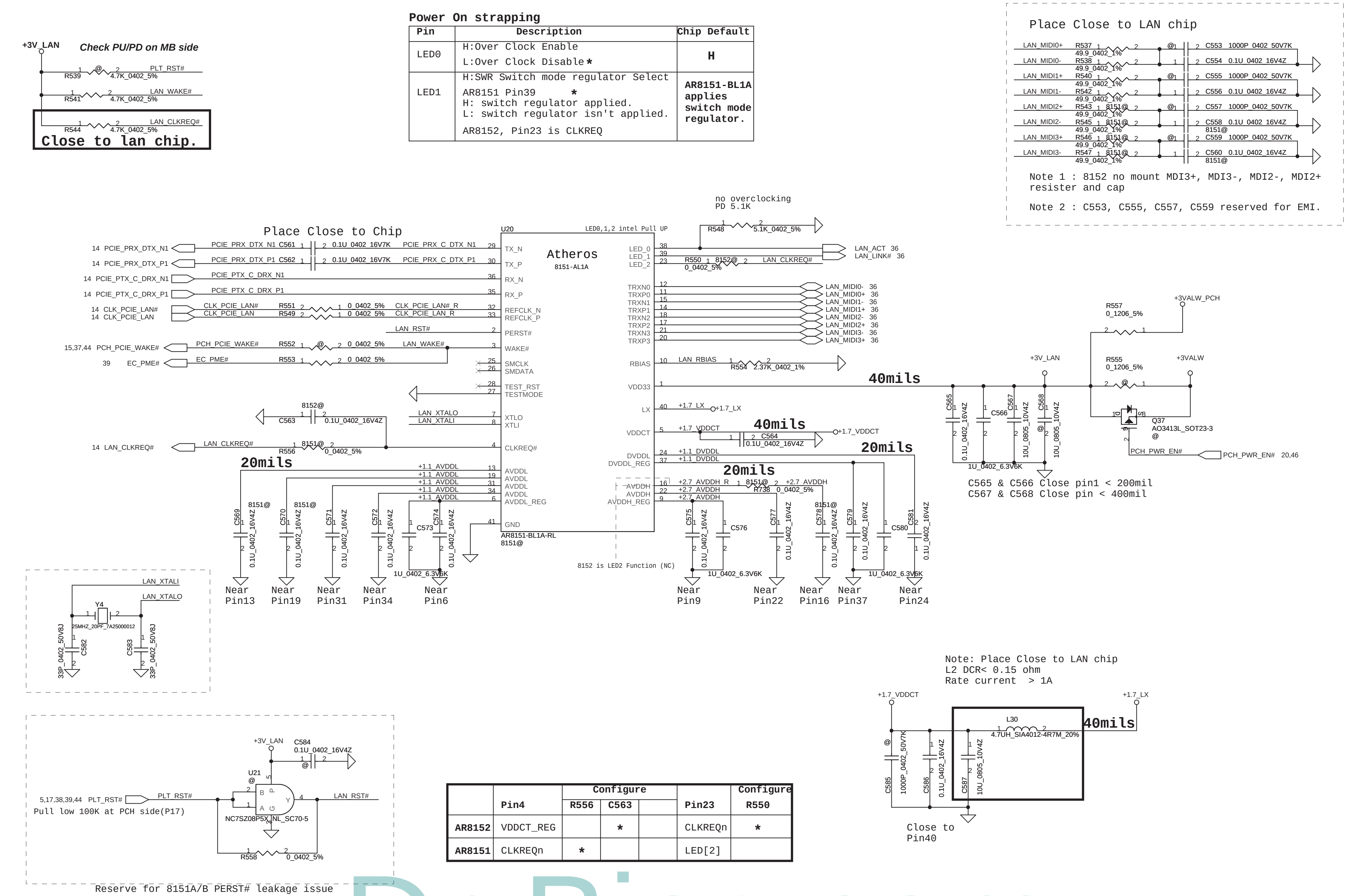
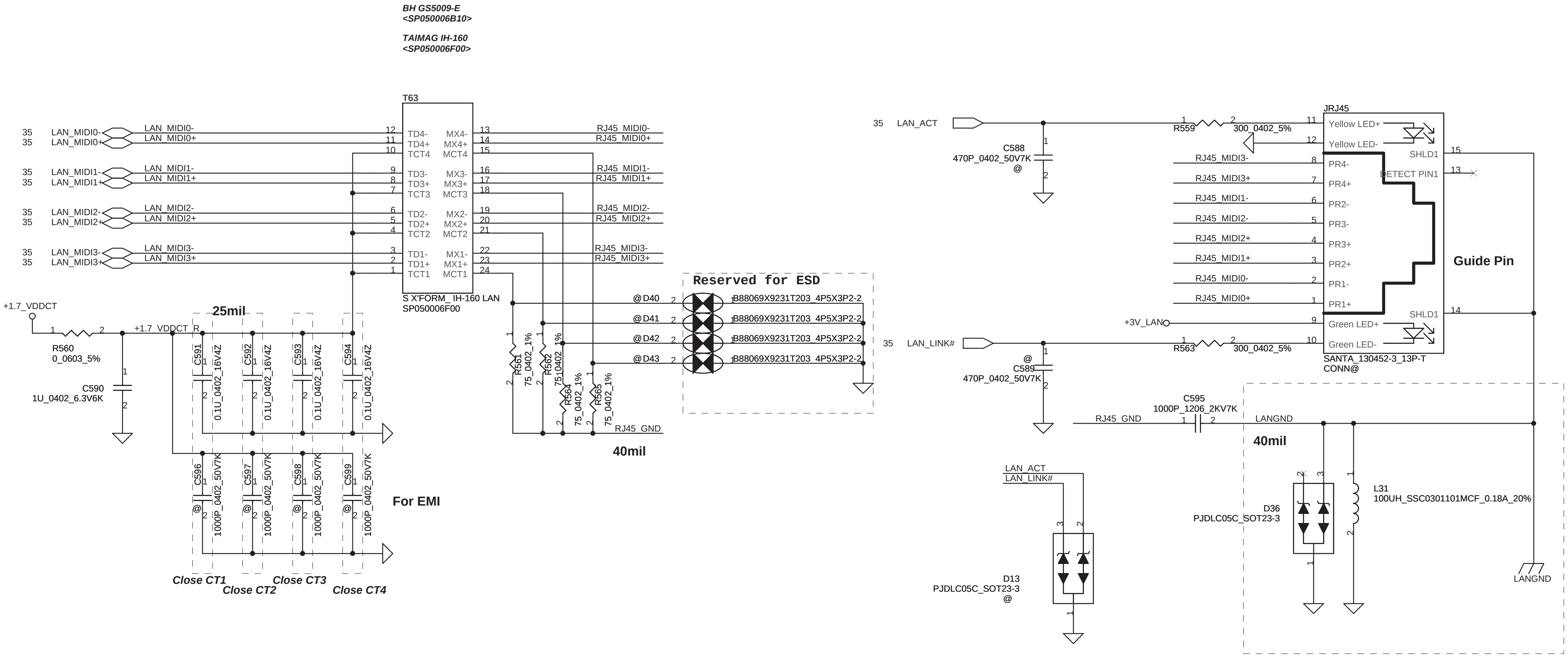


Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable*	H
LED1	H:SWR Switch mode regulator Select AR8151 Pin39 * H: switch regulator applied. L: switch regulator isn't applied. AR8152, Pin23 is CLKREQ	AR8151-BL1A applies switch mode regulator.

	Pin4	Configure R556	Configure C563		Pin23	Configure R550
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	



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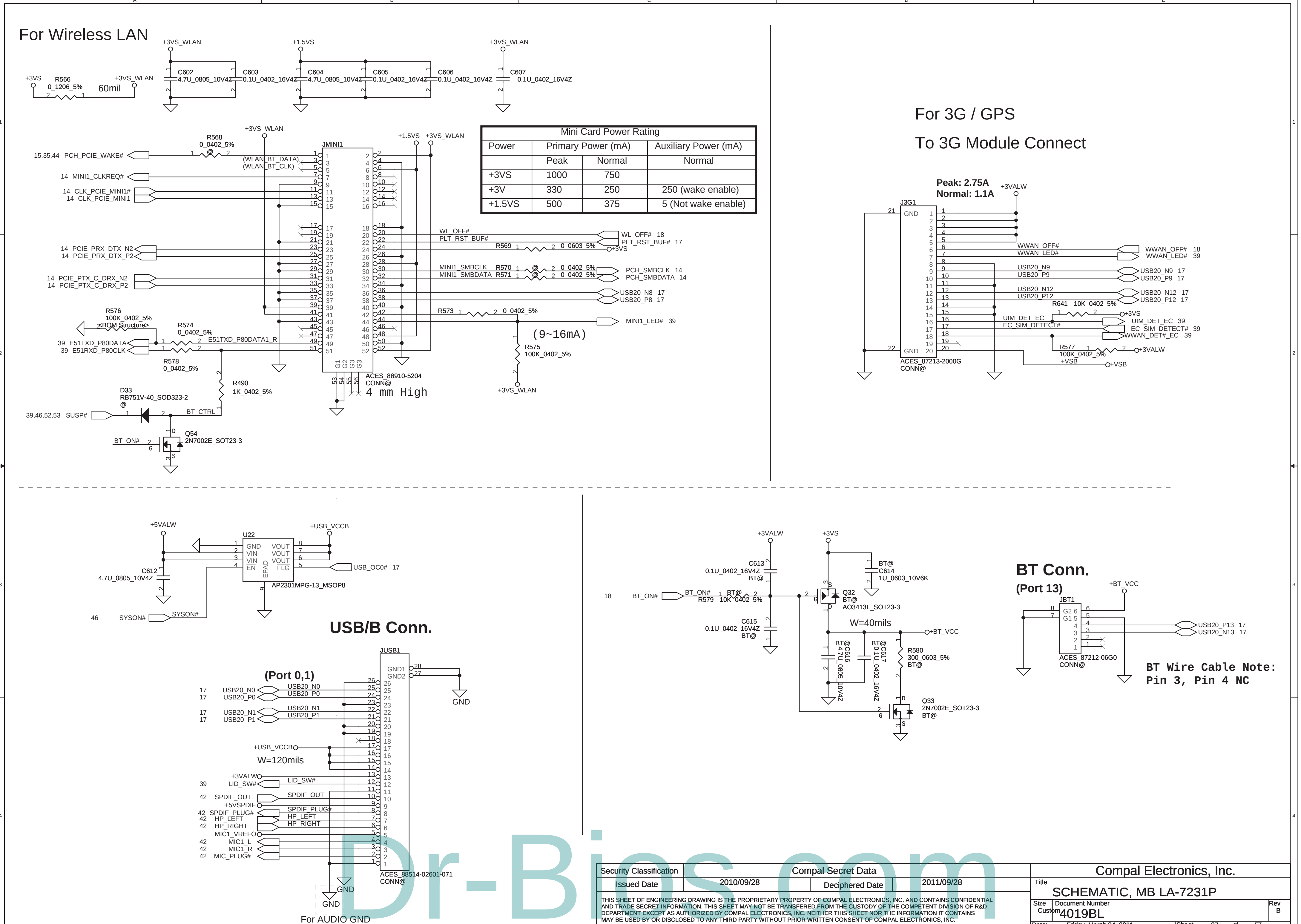

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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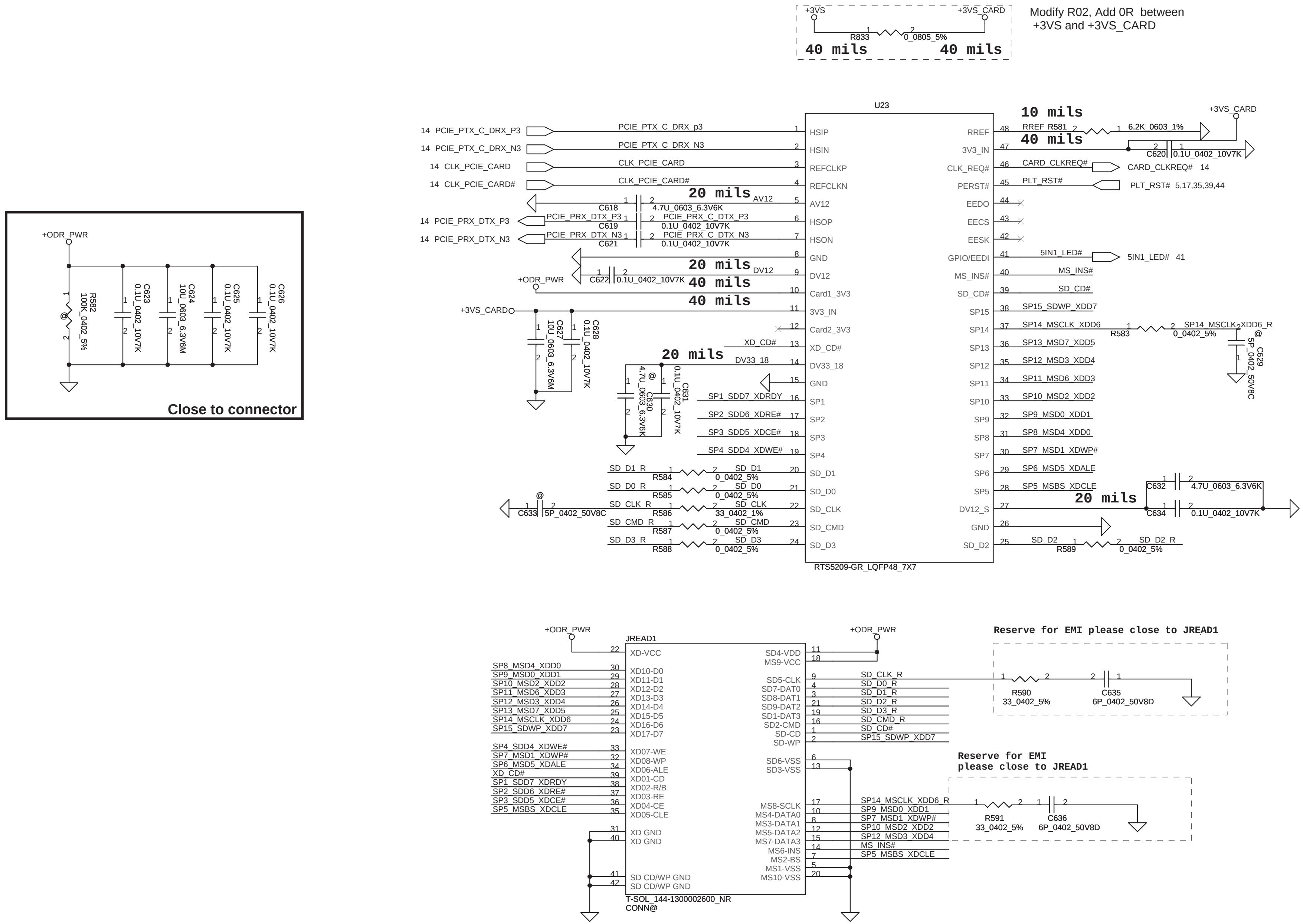
Card Reader



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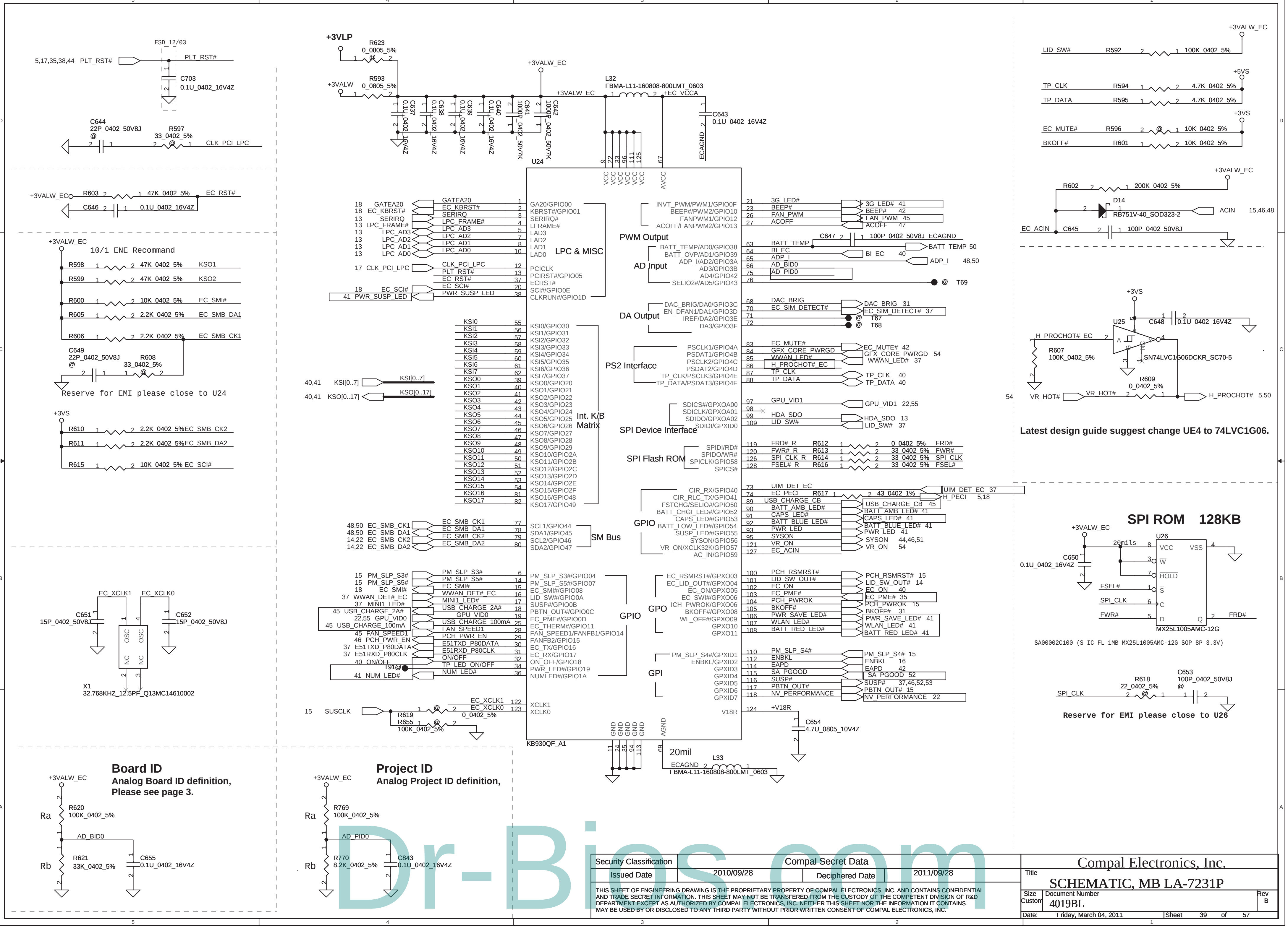

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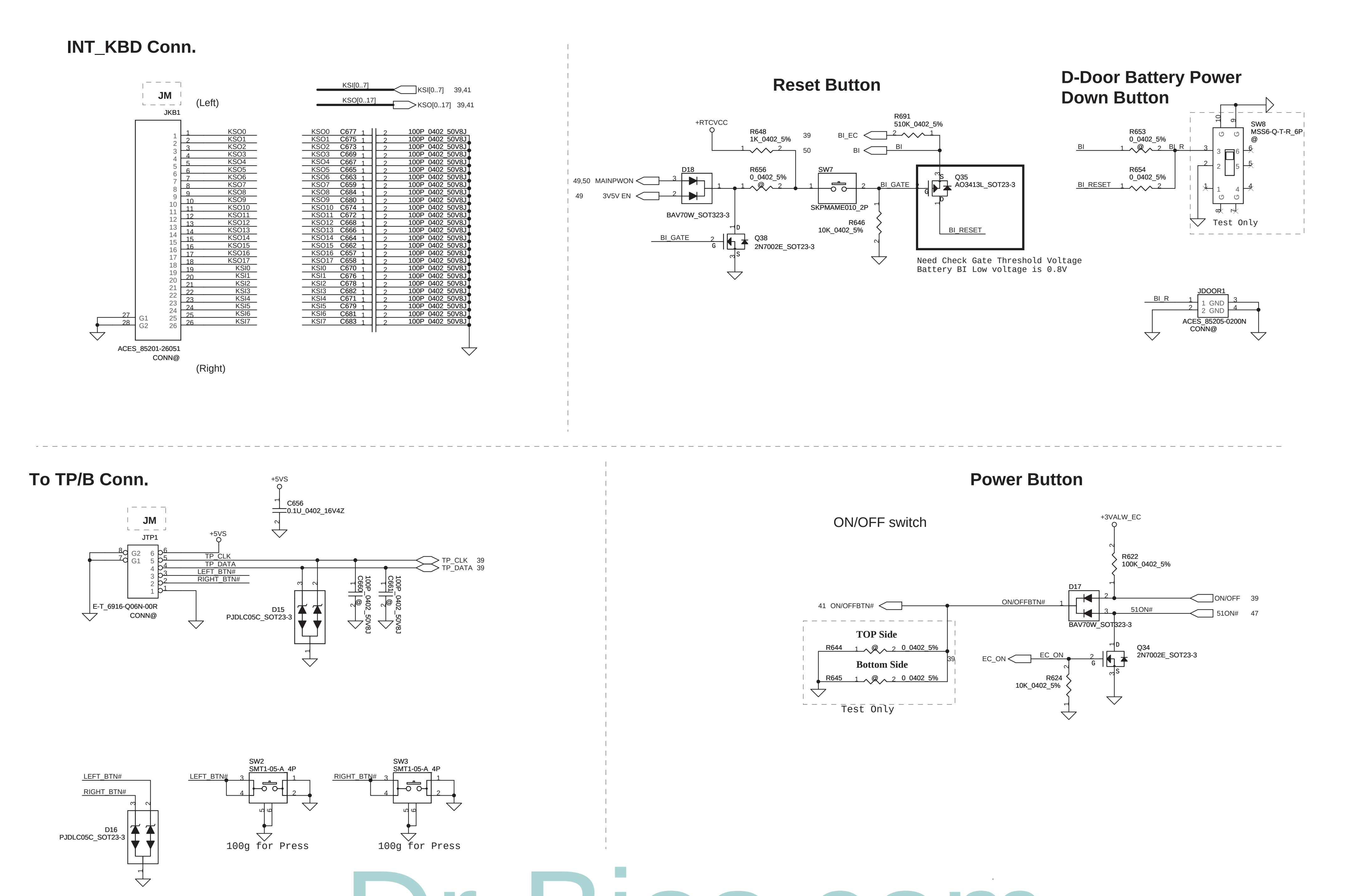

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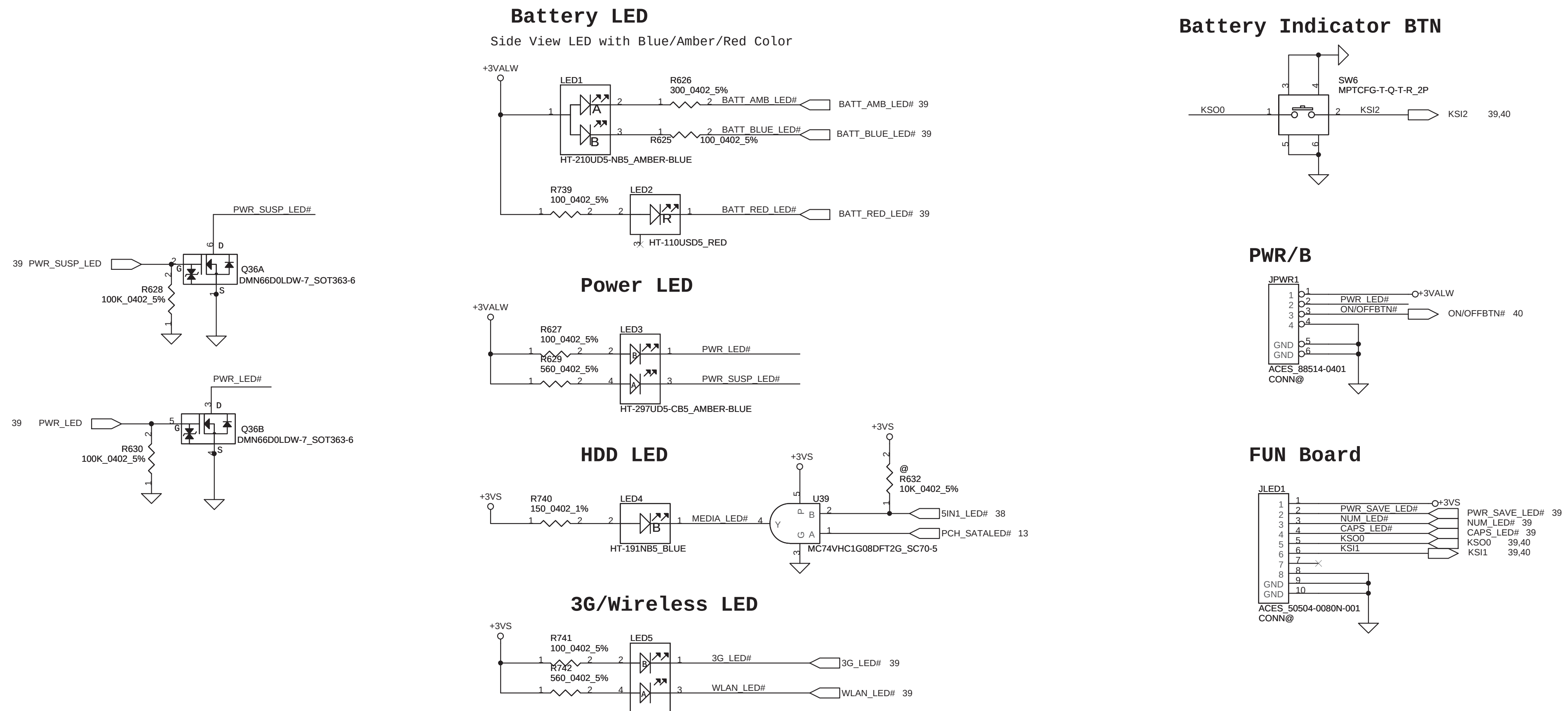

	KSO0
KSI1	PWR SAVE BTN#
KSI2	Battery ID BTN#

LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
	Blue	Amber	Blue	Amber	Blue	Amber		

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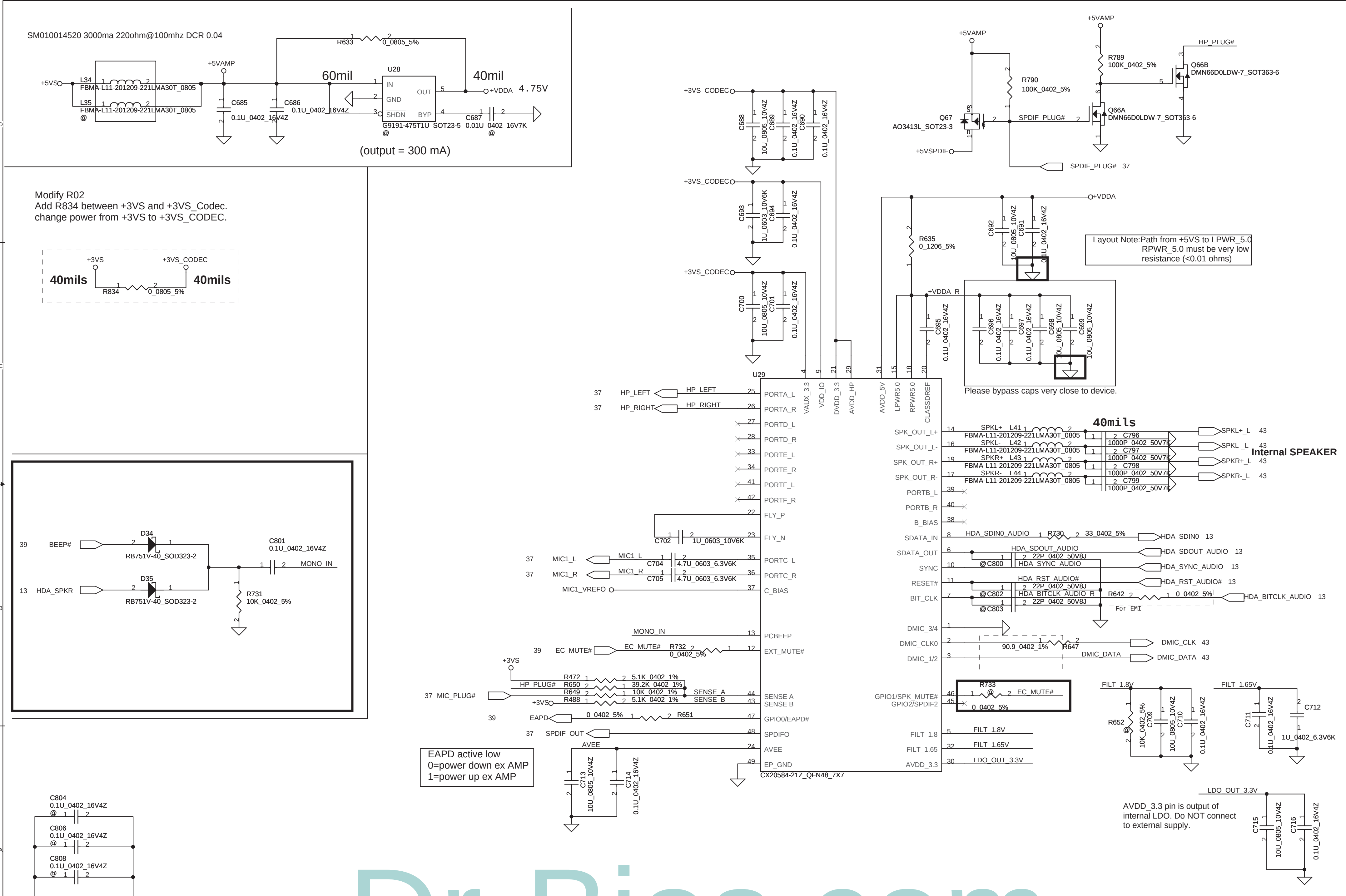

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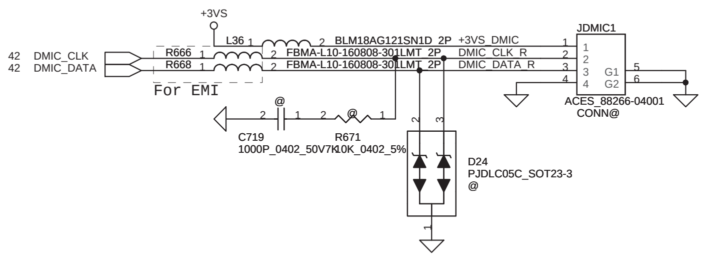
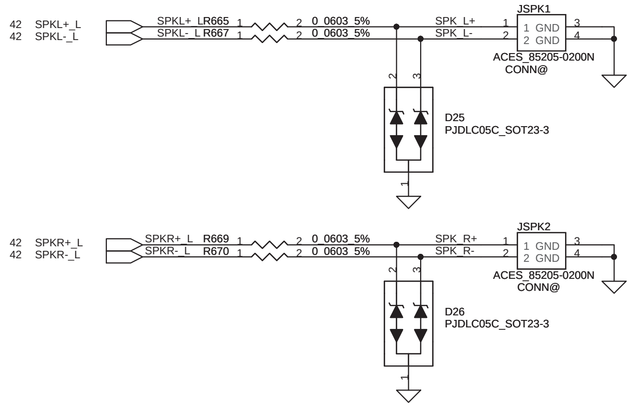
Digital MIC CONN



Int. Speaker Conn.



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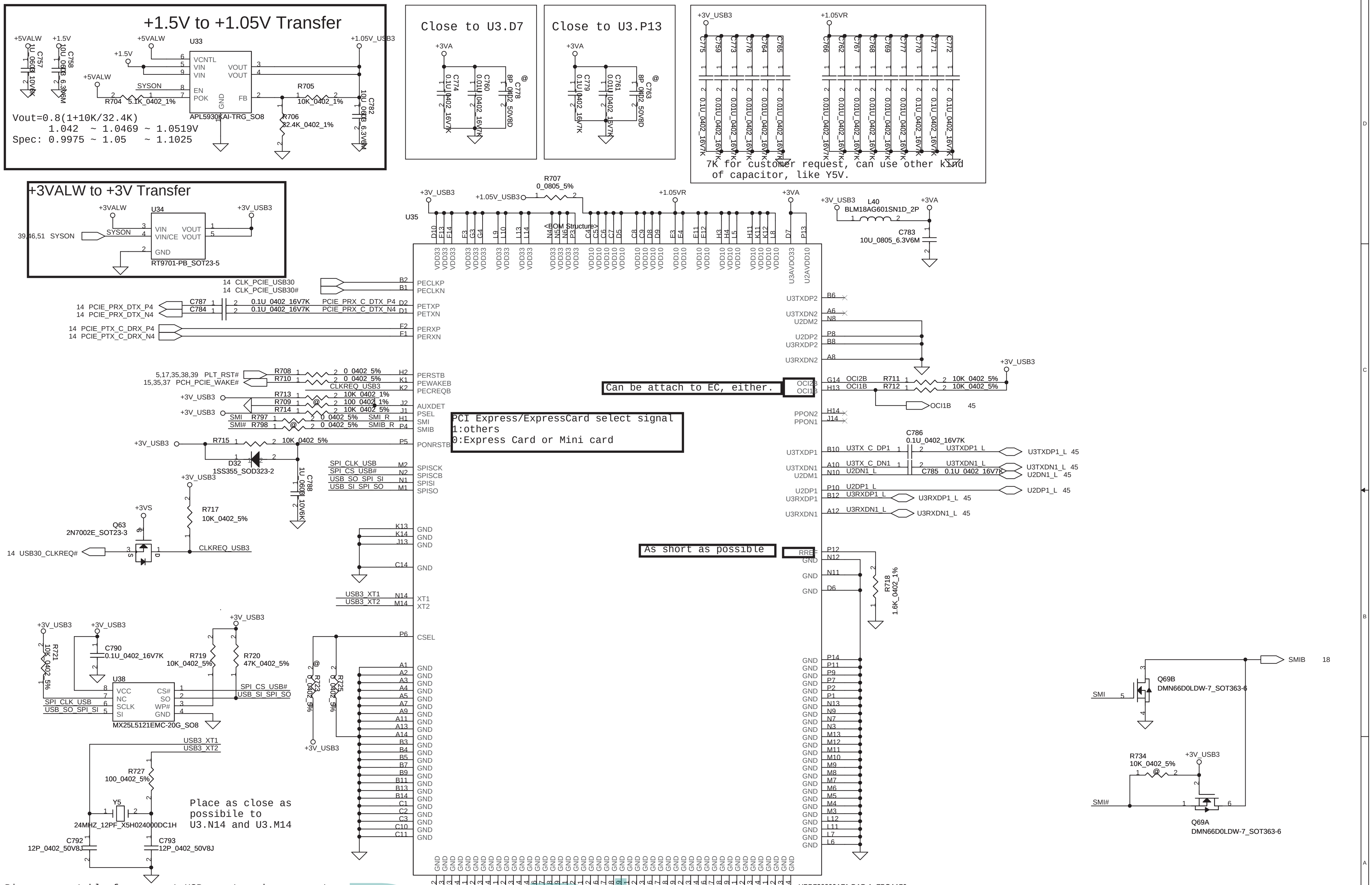


Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

P/N: SA000048H10
(S IC UPD720200AF1-DAP-A FBGA 176P USB3.0)

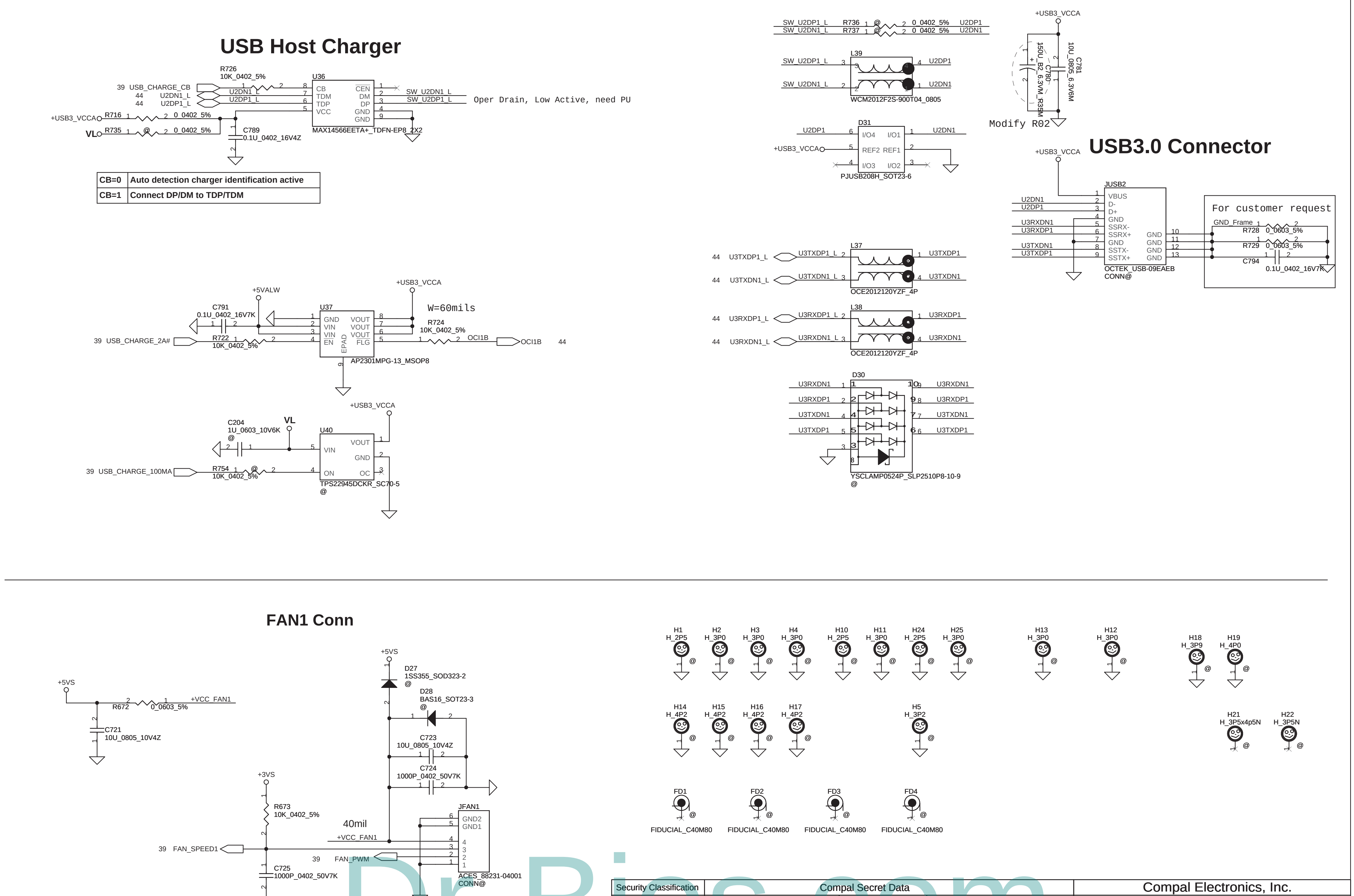
Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

Compal Electronics, Inc.

Title: SCHEMATIC, MB LA-7231P

Size: Custom | Document Number: 4019BL | Rev: B

Date: Friday, March 04, 2011 |



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/09/28	Deciphered Date	2011/09/28	Title: SCHEMATIC, MB LA-7231P
Size: Custom	Document Number: 4019BL		Rev: B	
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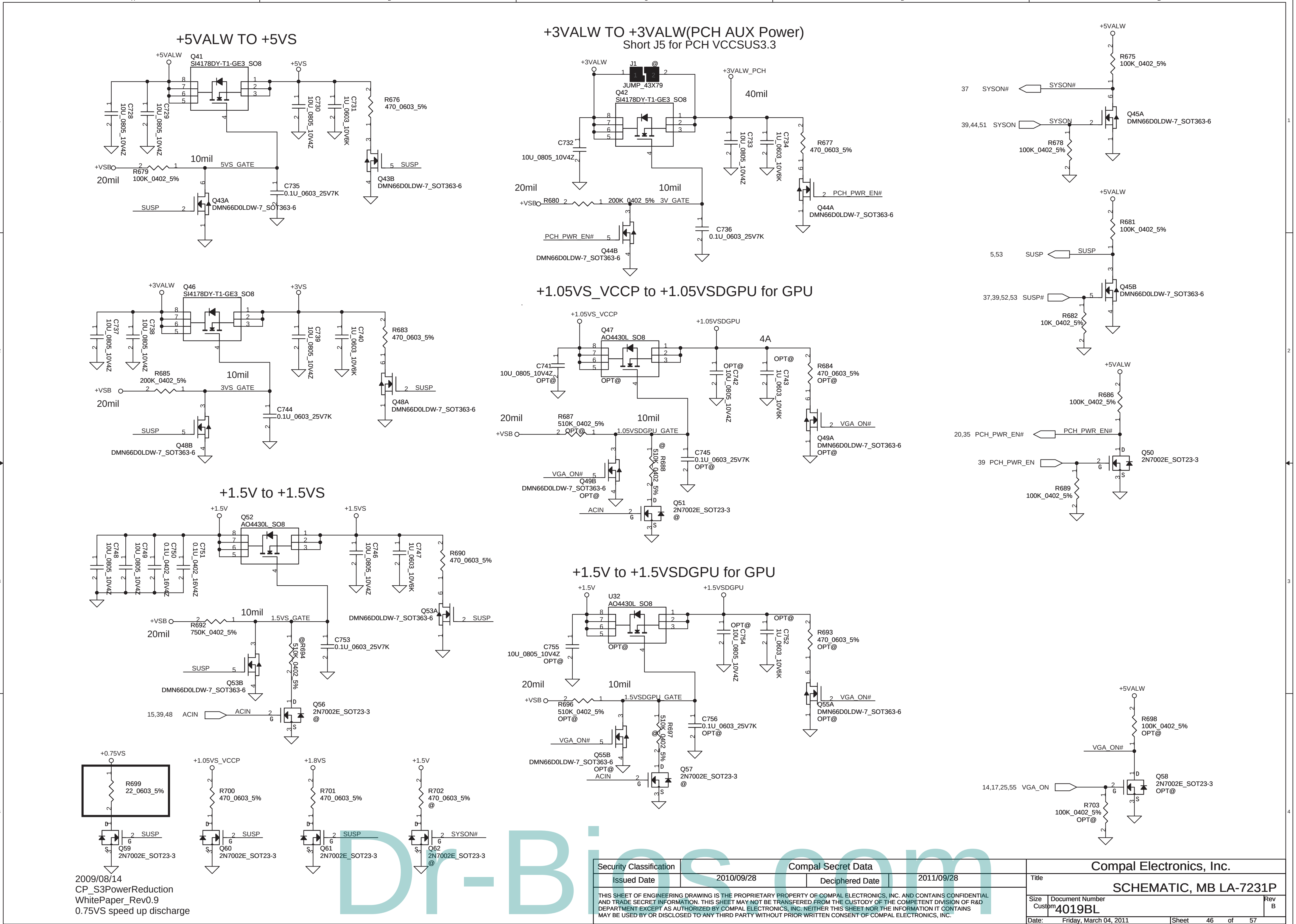

2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

Security Classification		Compal Secret Data	
Issued Date	2010/09/28	Deciphered Date	2011/09/28

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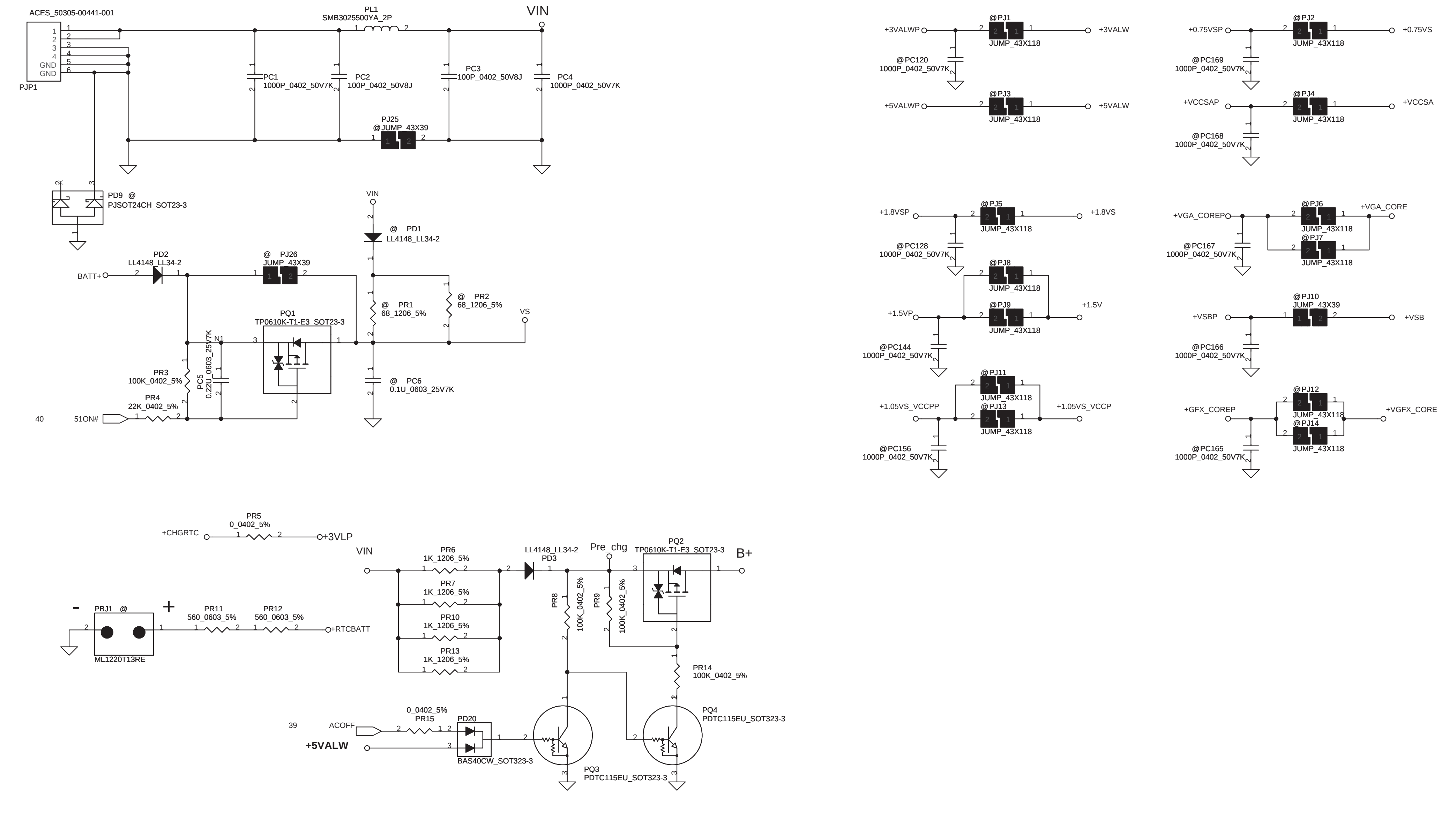
Size: Custom | Document Number: 4019BL | Rev: B
Date: Friday, March 04, 2011 |



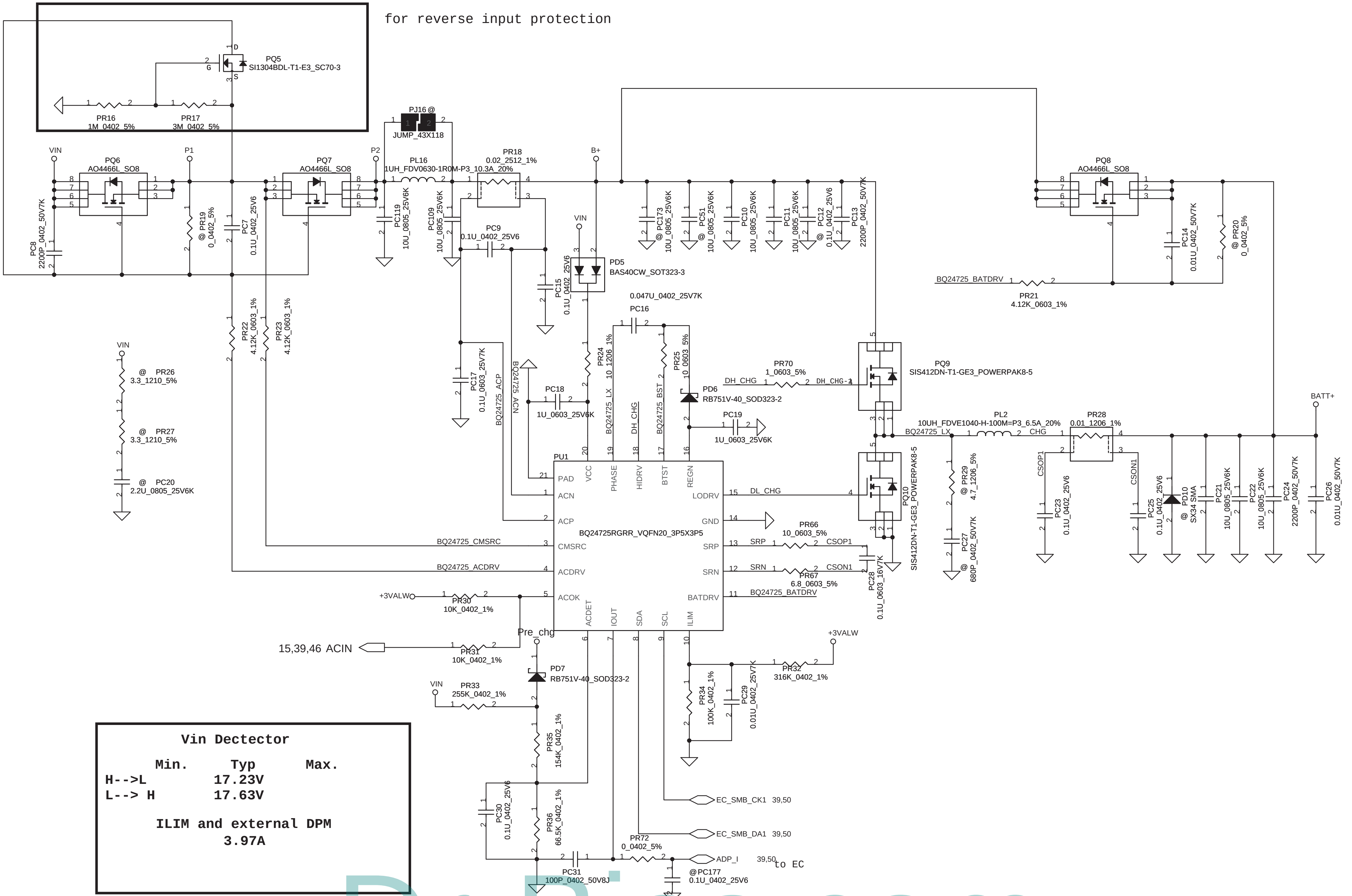
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: SCHEMATIC, MB LA-7231P

Size: Custom | Document Number: 4019BL | Rev: B

Date: Friday, March 04, 2011 |



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

Security Classification	Compal Secret Data	
Issued Date	2010/01/25	Deciphered Date 2010/12/31

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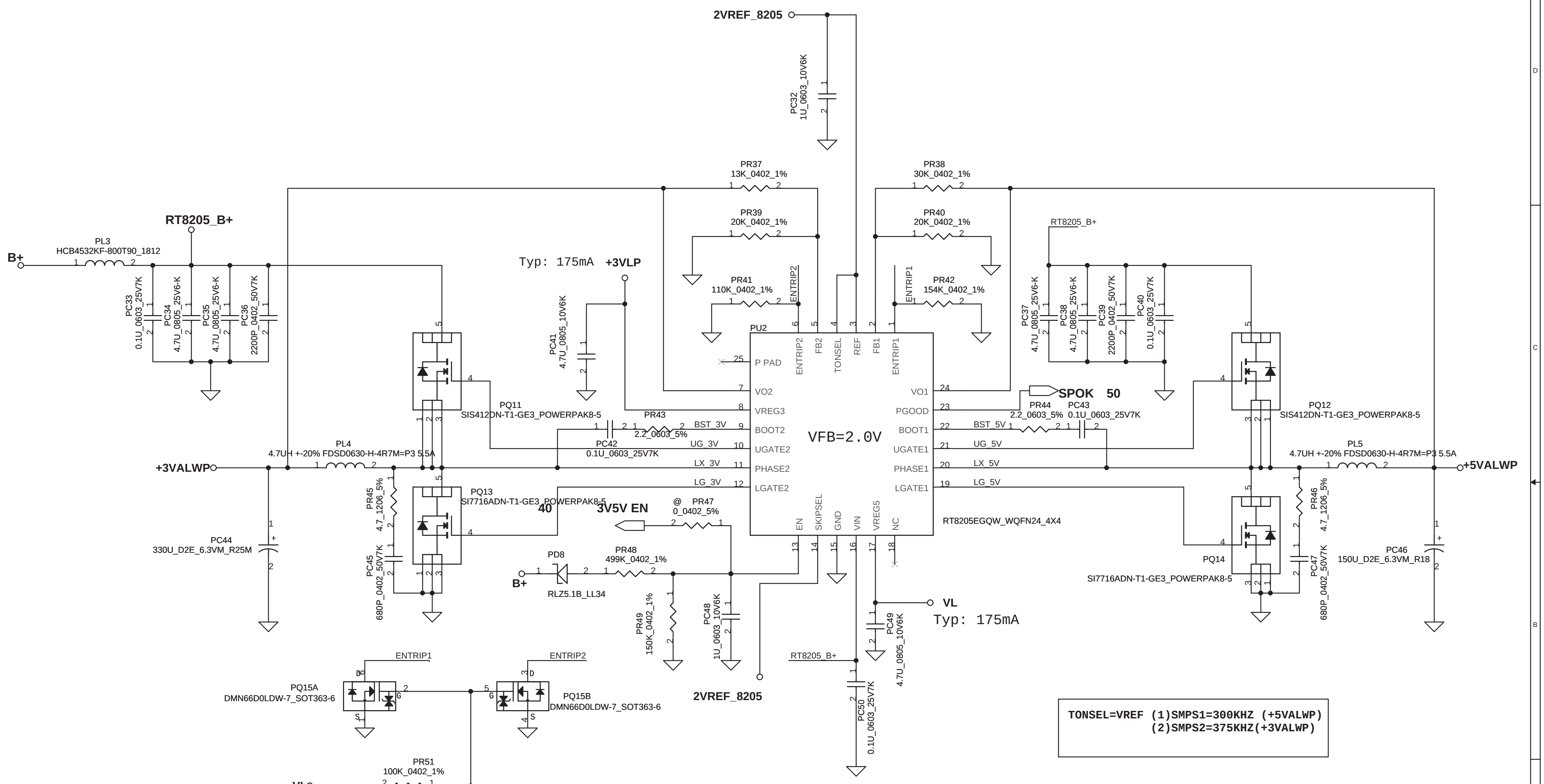

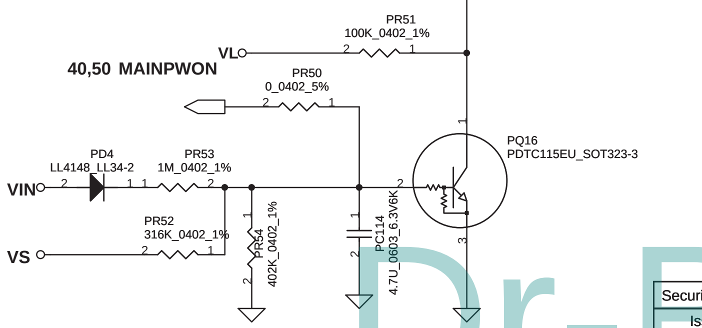

+3.3VALWP
Ipeak=5.78A ; 1.2Ipeak=6.94A; Imax=4.05A
f=375KHz, L=4.7UH
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-3)*(3/19)/(375KHz*4.7UH)=0.716A
Vlimit=10*10^-6*110Kohm/10=0.11V
Ilimit=0.11/(18m*1.2)~0.11/(15m)=6.34A~9.13A
Iocp=7.06A~9.85AA (7.06A>6.94A -> ok) -DVT-

+5VALWP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
f=300KHz, L=4.7UH,Rentrip=154k ohm
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-5)*(5/19)/(300KHz*4.7UH)=1.306A
Vlimit=10*10^-6*154Kohm/10=0.15V
Ilimit=0.15/(18m*1.2)~0.15/(15m)=7.13~10.26A
Iocp=8.44~11.57A (8.44>8.4 -> OK)

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Issued Date	2010/07/13	Deciphered Date	2011/07/13

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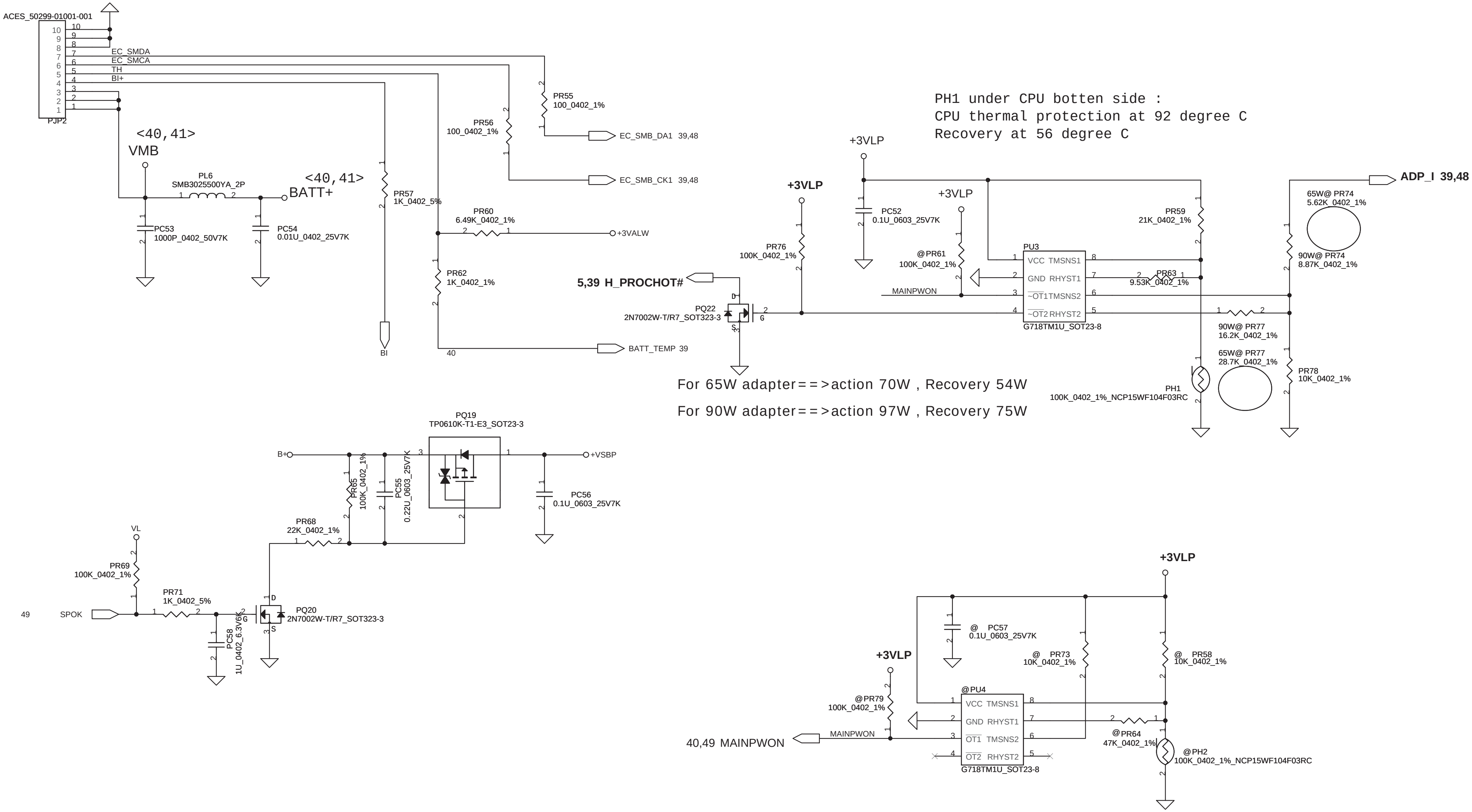

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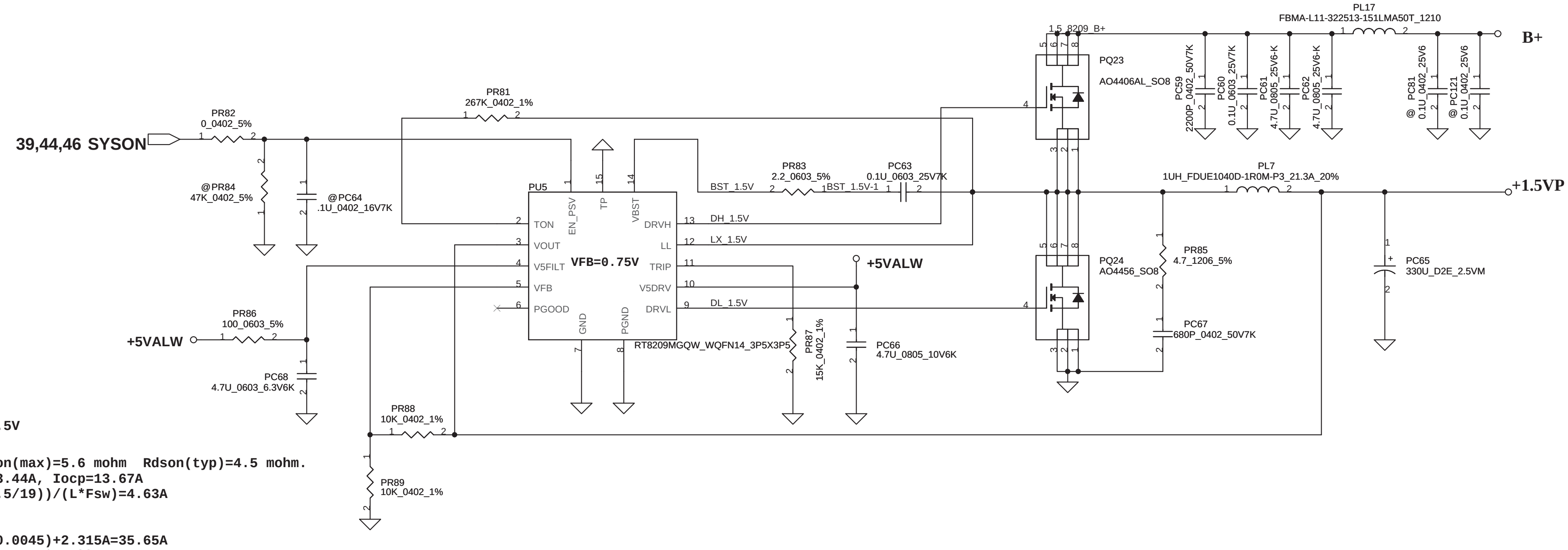
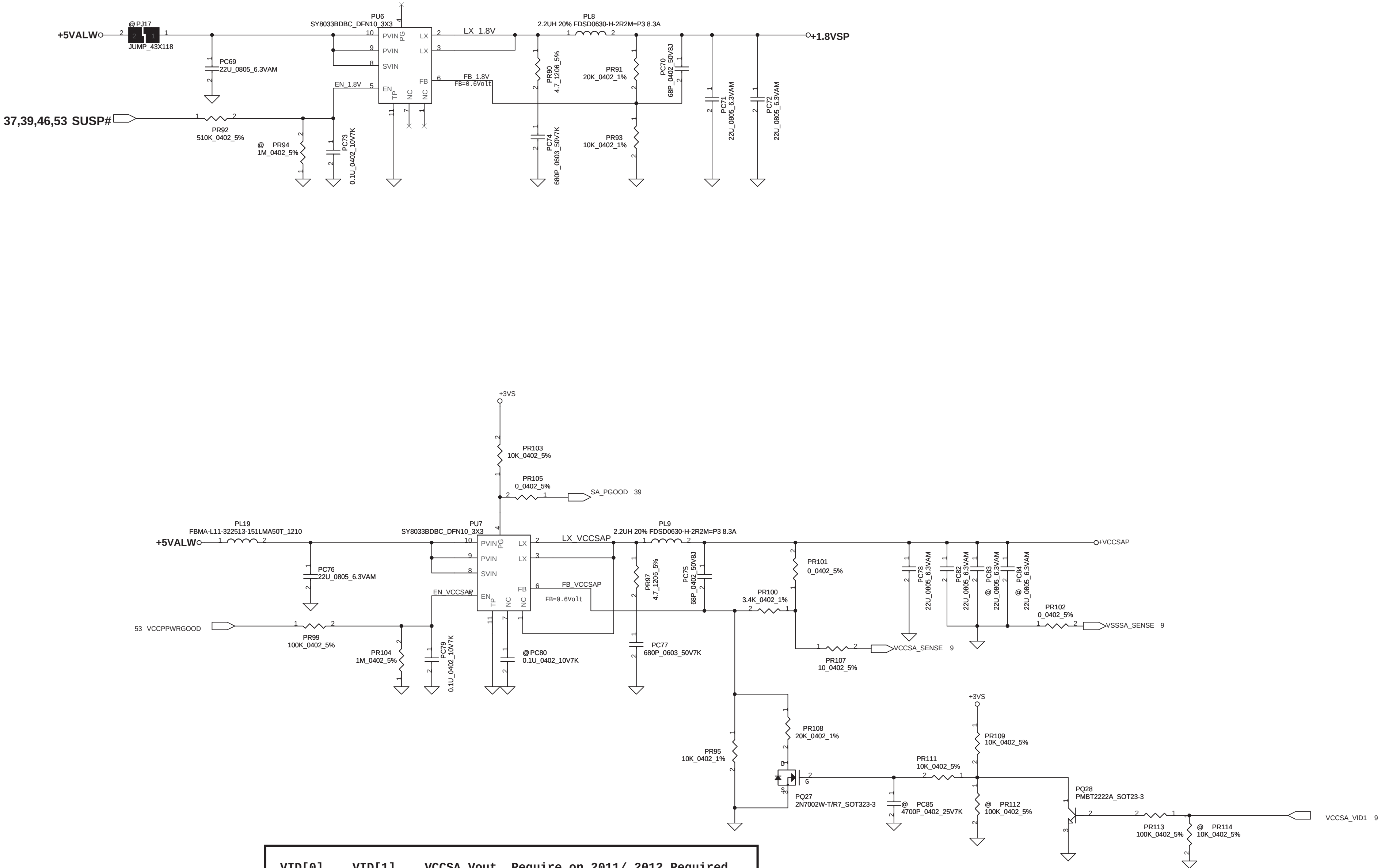
Issued Date	2010/01/25	Deciphered Date 2010/12/31	Title: SCHEMATIC, MB LA-7231P
			Size: Custom; Document Number: 4019BL; Rev: B
			Date: Friday, March 04, 2011; Sheet 50 of 57




```
<Vo=1.5V>  VFB=0.75V
V=0.75*(1+10K/10K)=1.5V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm  Rdson(typ)=4.5 mohm.
Ipeak=19.53A, Imax=23.44A, Iocp=13.67A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.63A
=>1/2Delta I=2.315A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+2.315A=35.65A
Iocpmin=((15K*9uA)/(0.0056*1.3))+2.315A=23.06A
Iocp=23.06A~35.65A
```

```
1.8VSP
Ipeak=3.35A ; 1.2Ipeak=4.02 ;Imax=2.345A
Vout=0.6*(1+(20K/10K))=1.8V
```



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

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Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

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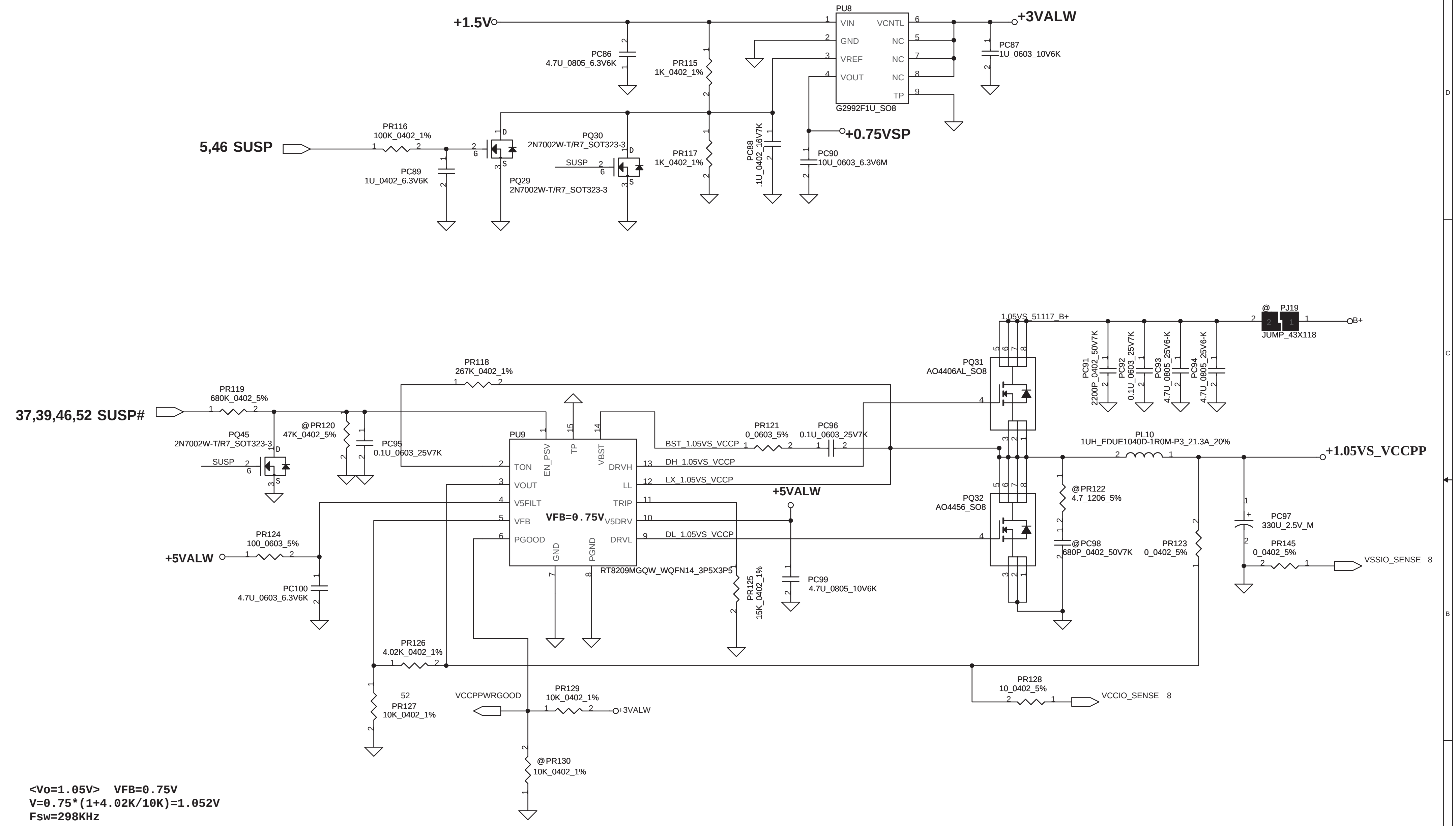


```
<Vo=1.05V>  VFB=0.75V
V=0.75*(1+4.02K/10K)=1.052V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm  Rdson(typ)=4.5 mohm.
Ipeak=12.866A, Imax=9A, Iocp=15.439A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.33A
=>1/2Delta I=1.665A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+1.665A=37.62A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=23.02A
Iocp=23.02A~37.62A
```


Security Classification	Compal Secret Data		
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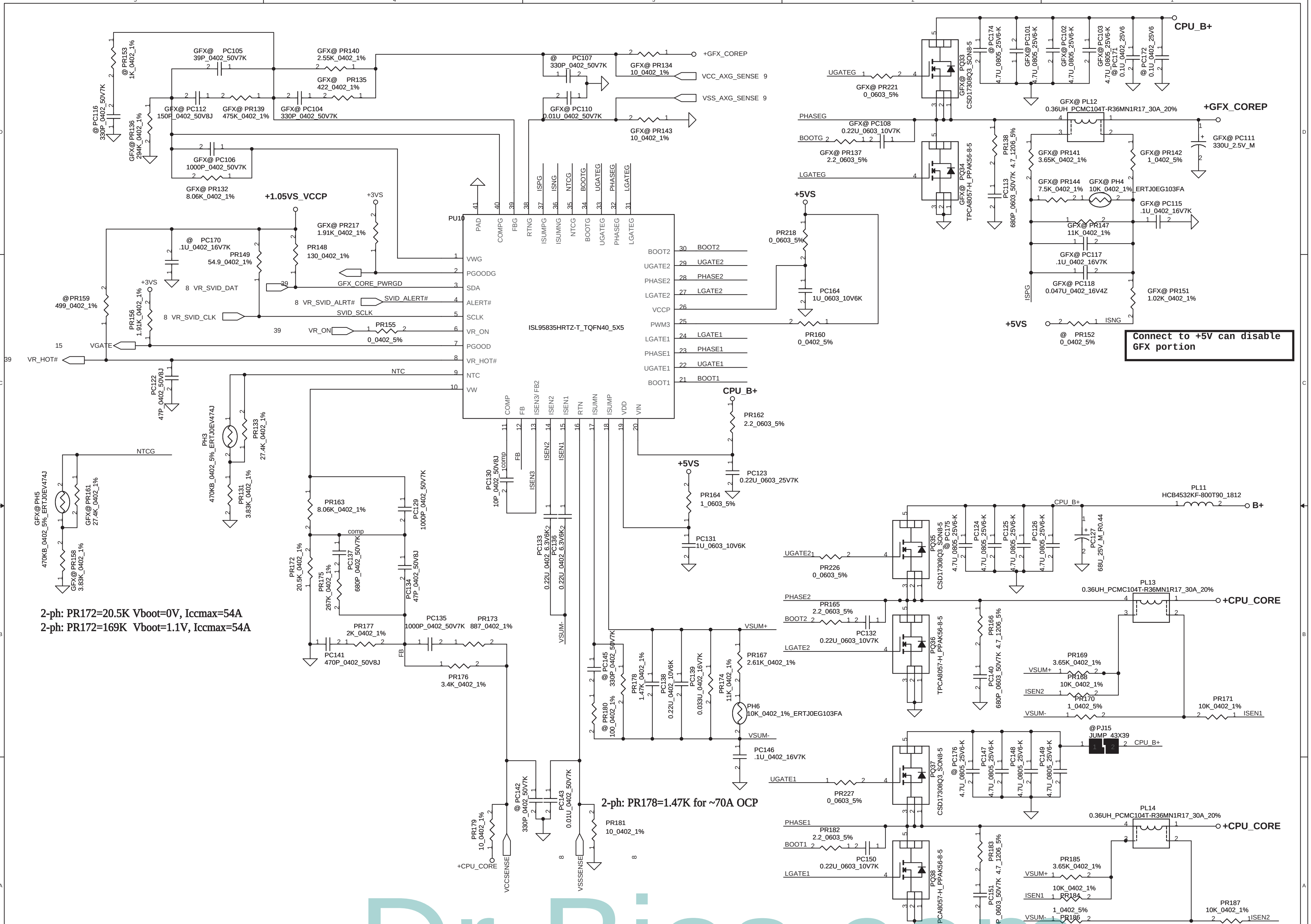


```
+CPU_CORE                    +GFX_CORE
Iocp=72A, IccMAX=53A         Iocp=40A, IccMAX=24A
Load line=1.9mohm            Load line=3.9mohm
DCR=1.1mohm                  DCR=1.1mohm
```


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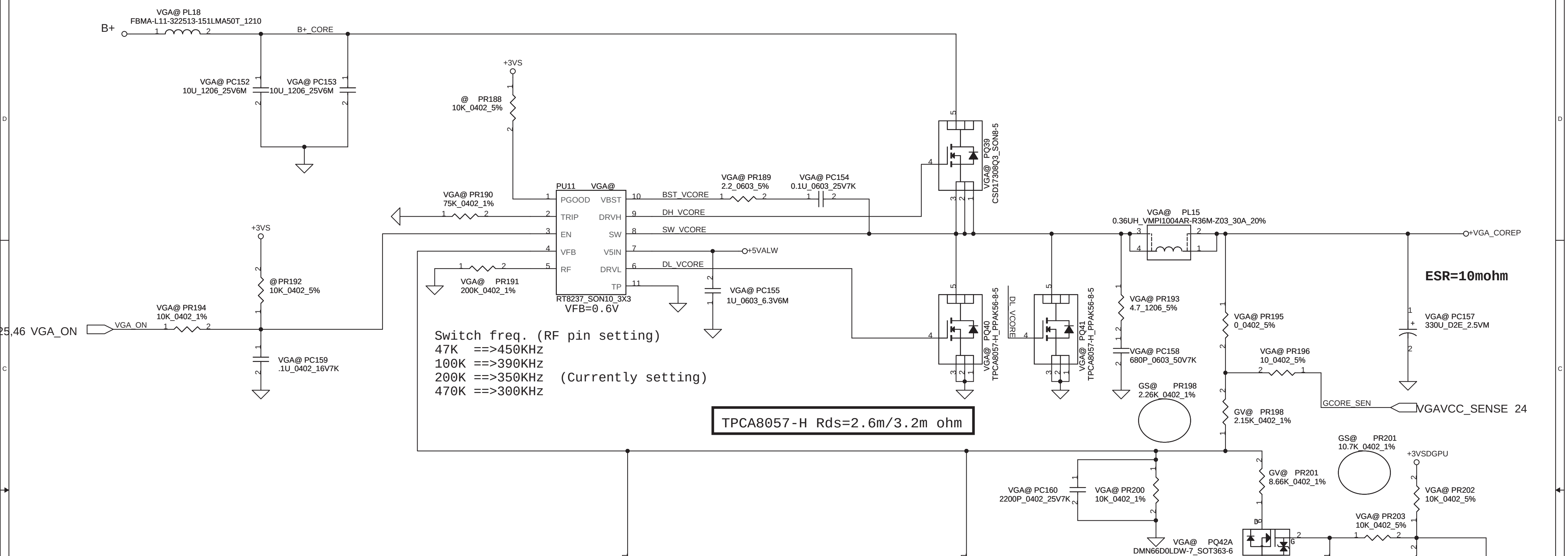
Date: Friday, March 04, 2011 |



Vtrip range ==> 0.2V ~ 3V

VFB=0.7V
V=0.7*(1+Rtop/Rbottom)
Fsw=350KHz

Cout ESR=12m ohm Rdson(max)=3.2 mohm Rdson(typ)=2.6 mohm.
Ipeak=41.02A, Imax=28.714A, Iocp=43A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=6.8A
=>1/2Delta I=3.4A
choose Rcs=75K
Iocpmax=((75K*11uA)/0.0013)+3.4A=75.52A
Iocpmin=((75K*9uA)/(0.0016*1.35))+3.4A=48.42A
Iocp=48.42A~75.52A

		GPU_VID2	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
	P0(Cold)	1	0	1	1.0V	1.025V
	P0(Hot)	1	1	0	0.975V(default)	1.0V
	P8/P12	1	1	1	0.860V	0.85V(default)
SJM only ==>	VPS	0	1	1	0.900V	----

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Compal Electronics, Inc.

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Date: Friday, March 04, 2011 |

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW/Edward request	Meet Turn off sequence		53	Add PQ45	2010 11/24	DVT
2	HW/Edward request	Meet Turn on sequence		53	Change PR119 to 680KΩ, PC95 to 0.1uF	2010 11/27	DVT
3	HW/Edward request	Meet new VGA table		55	Change PR201, PR205, PR219	2010 12/03	DVT
4	Battery Turn on time too long	Change enable 3/5V path				2010 12/04	DVT
5	HW/Edward request	For USB 3.0 charger function		47	Add PJ26	2010 12/04	DVT
6	HW/Edward request	Don't need VGA_PW_OK net		55	Delete net	2010 12/04	DVT
7	HW/Edward request	Tune Power sequence		52	Change PR92 from 100K to 510K Delete PR94	2010 12/08	DVT
8	HW/Edward request	Tune Power sequence		53	Change PR116 from 24.9K to 100K	2010 12/09	DVT
9	Costdown			54	Change PC97, PC111 to OS-CON cap.	2011 01/06	PVT
10	ISN test fail	ISN solution		49	Change PL16 to 1uH Add PC109, PC119	2011 01/07	PVT
11	Trigger ACOC	Prevent to trigger phase to gnd threshold Reserve RC for ADP_I		48	Change PC28 from 2.2u to 0.1u Add PR72	2011 01/24	PVT2
12							
13							
14							
15							
16							
17							

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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: SCHEMATIC, MB LA-7231P

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A --> B Change List

1209-----------------------------------
1. Page 24, Change R383 to GS@
   Change R380 to @
   Add Option Component for R383 and R386 4.99K_0402_1% with BOM structure GV@
2. Page 46, Change R679 to 100K_0402_5%
   Change R685 to 200K_0402_5%
   Change R692 to 750K_0402_5%
3. Page 40, Change SW8 to SN200002800

1206---
1. Page 17, U16 BOM Structure change to OPT@
2. Page 37, C613 BOM structure change to BT@
3. Page 32, Add T70, T71 for JCRT1.
4. Page 45, Change H10 to H2P5.
5. Page 14, Change C183, C184 to 27P
6. Page 22, Change C297, C298 to 22P
7. Page 35, Change C582, C583 to 33P
8. Page 43, Change R666, R668 to SM010017710 (For EMI)
9. Page 38, Pop R590, R591 with 33 ohm, C635, C636 with 6P for EMI

1203---
1. Page 39, Add C703 for ESD.

1202---
1. Update power schematics
2. Change H24 to H2P5
3. Page 35, Add R557 for power source +3VALW_PCH reserved

1201---
1. Page 40, Update Reset Button circuit
   Add R656, Q38
2. Page 17, delete VGA_ON for PD only.
   Change PR3.2 to PCH_GPIO2, PR3.1 to PCH_GPIO53
   Delete R257
3. Update Power Schematics 1201

1130b---
1. Page 38, U23.11 change to +3VS_CARD
2. Q2, Q13, Q19, Q21~Q29, Q31, Q33, Q34, Q50, Q51, Q54, Q56~Q63, Q68, Q74 change to SB00000J200

1130---
1. Page 18, Add Q75,Q74,R841 (The new circuit for DGPU_PWROK after 1.5V).
   Delete R271
2. Page40, Change R646 to 10K
   Change R648 to 1K
   Pop R646, R648, D18, Q35, R645 for Reset mainpower and BI
   Change R653 BOM structure to @
   Change SW8 to SN200002700

1129---
1. Page 07, Correct R70 bom structure to EDP@
2. Page 15,Change R244.1 net name from PCH_RSMRST# to PCH_RSMRST#_R
   Unpop R231
3. Page 17, U6, U7 change to SA00000OH00 (Same as U5/U39)
4. Page 24, Delete R390, R391, R392 for space issue.
5. Page 35, Add Q37 and Unpop R555
6. Page 38, Add R833 between +3VS and +3VS_CARD
   Change U23.47 to +3VS_CARD
7. Page 39,Change R621 from 0ohm to 8.2k(Board ID)
8. Page 42, Unpop R733
   Pop R732, R299
   Delete R637, R638, Q38, Q39, R299, R634, R636, R639, R640
   Change netname of PD# to EC_MUTE#
   Connect U29.4.9.21.29 to +3VS_CODEC
9. Page 45, Change C780 from SGA19151410(D size) to SGA00002N80(B2 size)
   Unpop U40, C204, R754
10. Page 46, Change Q47, Q52 to AO4430L_SO8
11. Update Power Schematics (11/25)
12. C226, C540, C549, C566, C573, C576, C580, C590, C712 change material to SE000000K80
13. D8, D9 change material to SCS00003600 (Need check again)
14. D32 change to SC100001K00 (Need apply CIS Symbol)

1123---
1. Page 22, Change R342 PU location from R762.2 to Q68.3
2. Page 24, Fix N12P-GV device ID
   R489 change BOM Structure to GS@
   R382, R380, R760, R756, R758, R757 change BOM Structure to GV@
   R380 change to 45.3K_0402_1% (SD034453280)
   R760 change to 4.99K_0402_1% (SD034499180)
   Delete Option compoent of R386
3. Page35, Modify auto boot-up issue
   Unpop R552
   POP R553, R541
   Change R541 PU location from R552.1 to R552.2
4. Page36, L31 update CIS Symbol and PCB footprint
5. Page 40, Change R622 PU to +3VALW_EC
   JTP1 pin definition upside down.
   Update D-Door Circuit
   Delete SW1, R631
   Add JDOOR1, SW
6. Page 41, SW6 change to SN100001D10
7. Page 42, Modify PD# circuit for 3V tolerance.
   Add R299
   Change R637, R638 PU to +3VS
   Fix Headphone/MIC detect issue
   Change R649 to 10K_0402_1%
   Change R650 to 39.2K_0402_1%
8. Page 44, Modify SMI circuit for leakage issue.
   Delete R830
   Add Q69, R734

B --> C Change List

0121A-----------------------------------
1. Page 19, Change L1 to SHI00003Y00
2. Page 41, Change R626 to SD034499080 (499_1%)
   Change R739 to SD034150080 (100_5%)
3. Page 17, Add R185
4. Page 46, Change R703 to 100K

0110A-----------------------------------
1. Change SE107475M80 to SE107475K80
2. Change SE052105Z80 to SE080105K80
3. Change SE068221J80 to SE074221K80
4. Change SE070473Z80 to SE076473K80
5. Page 15, UnPOP U5 and POP R223
6. Page 35, Unpop Q37 and POP R557
7. Change U8 to SA000047U10(N12P-GS) and SA00004JO10(N12P-GV)
8. Page41,
   R625 form 390 to 100
   R626 from 820 to 200
   R739 from 820 to 100
   R627 from 390 to 2.49K
   R629 from 820 to 3K
   R740 from 390 to 3.3K
   R741 from 390 to 2.2K
   R740 from 820 to 3.3K

0107A-----------------------------------
1. Page 40, Unpop SW8
2. Page 05, Add C215.
1. Page 11, Add C207, C212, C214 (0.1U_0402) for EMI reuqire
2. Page 12, Delete C159 for Layout space
3. Page 36, Delete R968, C994
4. Page 45, Reserved R736, R739
5. Page 18, Delete Q75
   Change Q74 to Q74A, A74B (DMN66D0LDW-7_SOT363-6)
   Change R842 PU to +3VSDGPU

0103-----------------------------------
1. Page 40, Add R691 for EC_BI
2. Page 39, Connect EC_BI to U24.64
   Change R621 to 18K_0402_5%
   Delete net 65W/90W#
3. Page 25, Unpop C345, C346, C347, C348 L13, L14, C356, C357, C358
   Change C349, C359 to 10K_5%_0402
   Unpop R415, R416
4. Page 18, Change Q75 to AP2302GN-HF_SOT23-3
   Add R842, C185 with BOM structure OPT@
   Change Q74, Q75, R841 with BOM structure OPT@
5. Page 37, Delete R572
6. Page 08, change C81, C82 to SGA20331E10
7. Page 26, Change C381,C857 to SGA20471D20

C --> Pre-MP Change List

0222A-----------------------------------
1. Page 41, Change R627, R741 to 100_0402_5%
   Change R740 to 150_0402_1%
   Change R627, R742 to 560_0402_5%
2. Page 45, Unpop D30 (Remove USB3.0 ESD Diode)

0218A-----------------------------------
1. Page 31, Add L45 for USB20_P10/N10
   Change R478/R479 to @
   Move C492, C493 to USB20_P10/N10
   Delete D5 for layout space

0215A-----------------------------------
1. Page 44, Mount R720 for EEPROM (EON)
2. Change U3 to B3 version(SA00004EEY0)
3. Page 41, change R626 to 300_0402_5%
   change R739 to 100_0402_5%

0125A-----------------------------------
1. Page39 Change R621 to 33K_0402_5% (Board ID)
2. Update Power Schematics

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