# JE40 HR
# DIS/UMA/Muxless Schematics Document
# Sandy Bridge
# Intel PCH

DY :None Installed
DIS:DIS  installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 1 of 102

# JE40 HR Block Diagram (Discrete/UMA/co-lay)

Project code : 91.4IQ01.001
PCB P/N : 48.4IQ01.0SA
Revision : 10267-1

##OnMainBoard

VRAM
2GB/1GB/512MB
88,89,90,91

DDR3
800MHz

Nvidia N12P
83.84,85,86,87

PCIe x 16
(Discrete only)

Intel CPU
Sandy Bridge
FSB: 1066 MHz
4,5,6,7,8,9,10,11,12,13

DDRIII 1066/1333 Channel A
DDRIII 1066/1333 Channel B

DDRIII Slot 0 1066/1333 14
DDRIII Slot 1 1066/1333 15

Discreet/UMA/PX Co-lay

FDIx4x2
(UMA only)

DMIx4

HDMI 51
LCD 49
CRT 50

HDMI
LVDS(Dual Channel)
RGB CRT
Level shifter 57

Intel
PCH
Cougar Point

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1

17,18,19,20,21,22,23,24,25,26

PCIE x 1
USB x 2
USB3.0
uPD720200
75

PCIE x 1
USB x 1
Mini-Card
802.11a/b/g
65

PCIE x 1
1000 NIC
BCM57780A1
31

RJ45 CONN 59

SD/MMC+/MS/
MS Pro/xD

PCIE x 1,USB x 1
Mini-Card
WWAN 66

SIM 66

USB 2.0 x 1
Right Side:
USB x 1

Left Side:
USB x 1

Bluetooth 63

CAMERA 49

64

USB2.0 x 4

AZALIA

Azalia
CODEC
ALC271X
29

Internal Analog MIC
HP1
MIC IN
2CH SPEAKER

SPI

Flash ROM
4MB 60

LPC Bus

LPC debug port 71

SATA x 2

HDD 56

ODD 56

KBC
NUVOTON
NPCE795P
27

SMBus

Touch PAD 69

Int. KB 69

Thermal
ENE P2800
ENE P2793 28

Fan 28

| SYSTEM DC/DC APL5916KAI 48 | |
|---|---|
| INPUTS | OUTPUTS |
| 1D05V_PWR | 0D85V_S0 |

| CPU DC/DC NCP6131S52MNR 42~43 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE |

| SYSTEM DC/DC UP6128PQDD 45 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | 1D05V_VTT |

| SYSTEM DC/DC UP6183PQAG 41 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | 5V_AUX_S5<br>3D3V_AUX_S5<br>5V_S5<br>3D3V_S5 |

| SYSTEM DC/DC UP6165BQKF 46 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | 1D5V_S3<br>0D75V_S0<br>DDR_VREF_S3 |

| SYSTEM DC/DC NCP5911MNTBG 44 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_GFXCORE_PWR |

| VGA RT8208BGQW 92 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | VGA_CORE |

| TI CHARGER BQ24745RHDR 40 | |
|---|---|
| INPUTS | OUTPUTS |
| DCBATOUT | BT+ |

| SYSTEM DC/DC RT9025 47 | |
|---|---|
| INPUTS | OUTPUTS |
| 3D3V_S0 | 1D8V_S0 |

| SYSTEM DC/DC RT9025-25PSP 93 | |
|---|---|
| INPUTS | OUTPUTS |
| 1D5V_S3 | 1V_VGA_S0 |
| 3D3V_S5 | 1D8V_VGA_S0 |

| Switches | |
|---|---|
| INPUTS | OUTPUTS |
| 1D5V_S3 | 1D5V_VGA_S0 |
| 3D3V_S0 | 3D3V_VGA_S0 |

## PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 2 of 102

# PCH Strapping

Huron River Schematic Checklist Rev.0_7

| Name | Schematics Notes |
|---|---|
| SPKR | **Reboot option at power-up**<br>**Default Mode:** Internal weak Pull-down.<br>**No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. |
| INIT3_3V# | Weak internal pull-up. Leave as "No Connect". |
| GNT3#/GPIO55<br>GNT2#/GPIO53<br>GNT1#/GPIO51 | GNT[3:0]# functionality is not available on Mobile.<br>Mobile: Used as GPIO only<br>Pull-up resistors are not required on these signals.<br>If pull-ups are used, they should be tied to the Vcc3_3power rail. |
| SPI_MOSI | **Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor.<br>**Disable Danbury:** Left floating, no pull-down required. |
| NV_ALE | **Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor]<br>**Disable Danbury:** Leave floating (internal pull-down) |
| NC_CLE | DMI termination voltage. Weak internal pull-up. Do not pull low. |
| HAD_DOCK_EN#<br>/GPIO[33] | Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.<br>High (1) - Security measure defined in the Flash Descriptor will be enabled.<br>Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently.<br>Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions. |
| HDA_SDO | Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#. |
| HDA_SYNC | Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#. |
| GPIO15 | Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality<br>Note : This is an un-muxed signal.<br>This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#.<br>CRB has a 1-kohm pull-up on this signal to +3.3VA rail. |
| GPIO8 | GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled. |
| GPIO27 | **Default = Do not connect (floating)**<br>High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit.<br>Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails. |

# Processor Strapping

Huron River Schematic Checklist Rev.0_7

| Pin Name | Strap Description | Configuration (Default value for each bit is 1 unless specified otherwise) | Default Value |
|---|---|---|---|
| CFG[2] | **PCI-Express Static Lane Reversal** | **1:** Normal Operation.<br>**0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ... | 1 |
| CFG[4] | | **1:** Disabled - No Physical Display Port attached to Embedded DisplayPort.<br>**0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port | 0 |
| CFG[6:5] | **PCI-Express Port Bifurcation Straps** | 11 : x16 - Device 1 functions 1 and 2 disabled<br>10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled<br>01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled)<br>00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled | 11 |
| CFG[7] | **PEG DEFER TRAINING** | **1:** PEG Train immediately following xxRESETB de assertion<br>**0:** PEG Wait for BIOS for training | 1 |

## Voltage Rails

| POWER PLANE | VOLTAGE | ACTIVE IN | DESCRIPTION |
|---|---|---|---|
| 5V_S0<br>3D3V_S0<br>1D8V_S0<br>1D5V_S0<br>1D05V_VTT<br>0D85V_S0<br>0D75V_S0<br>VCC_CORE<br>VCC_GFXCORE<br>1D8V_VGA_S0<br>3D3V_VGA_S0<br>1V_VGA_S0 | 5V<br>3.3V<br>1.8V<br>1.5V<br>1.05V<br>0.95 - 0.85V<br>0.75V<br>0.35V to 1.5V<br>0.4 to 1.25V<br>1.8V<br>3.3V<br>1V | S0 | CPU Core Rail<br>Graphics Core Rail |
| 5V_USBX_S3<br>1D5V_S3<br>DDR_VREF_S3 | 5V<br>1.5V<br>0.75V | S3 | |
| BT+<br>DCBATOUT<br>5V_S5<br>5V_AUX_S5<br>3D3V_S5<br>3D3V_AUX_S5 | 6V-14.1V<br>6V-14.1V<br>5V<br>5V<br>3.3V<br>3.3V | All S states | AC Brick Mode only |
| 3D3V_LAN_S5 | 3.3V | WOL_EN | Legacy WOL |
| 3D3V_AUX_KBC | 3.3V | DSW, Sx | ON for supporting Deep Sleep states |
| 3D3V_AUX_S5 | 3.3V | G3, Sx | Powered by Li Coin Cell in G3 and +V3ALW in Sx |

# PCIE Routing

| | |
|---|---|
| LANE1 | Mini Card2(WWAN) |
| LANE2 | Mini Card1(WLAN) |
| LANE3 | Card Reader |
| LANE4 | Onboard LAN |
| LANE5 | USB3.0 |
| LANE6 | Intel GBE LAN |
| LANE7 | Dock |
| LANE8 | New Card |

# SATA Table

| SATA | |
|---|---|
| Pair | Device |
| 0 | HDD1 |
| 1 | HDD2 |
| 2 | N/A |
| 3 | N/A |
| 4 | ODD |
| 5 | ESATA |

# USB Table

| Pair | Device |
|---|---|
| 0 | Touch Panel / 3G SIM |
| 1 | USB Ext. port 1 (HS) |
| 2 | Fingerprint |
| 3 | BLUETOOTH |
| 4 | Mini Card2 (WWAN) |
| 5 | CARD READER |
| 6 | X |
| 7 | X |
| 8 | USB Ext. port 4 / E-SATA /USB CHARGER |
| 9 | USB Ext. port 2 |
| 10 | EDP CAMERA |
| 11 | Mini Card1 (WLAN) |
| 12 | CAMERA |
| 13 | New Card |

## SMBus ADDRESSES

| I² C / SMBus Addresses<br>Device | Ref Des | HURON RIVER ORB<br>Address | Hex | Bus |
|---|---|---|---|---|
| EC SMBus 1<br>Battery<br>CHARGER | | | | BAT_SCL/BAT_SDA<br>BAT_SCL/BAT_SDA<br>BAT_SCL/BAT_SDA |
| EC SMBus 2<br>PCH<br>eDP | | | | SML1_CLK/SML1_DATA<br>SML1_CLK/SML1_DATA<br>SML1_CLK/SML1_DATA |
| PCH SMBus<br>SO-DIMMA (SPD)<br>SO-DIMMB (SPD)<br>Digital Pot<br>G-Sensor<br>MINI | | | | PCH_SMBDATA/PCH_SMBCLK<br>PCH_SMBDATA/PCH_SMBCLK<br>PCH_SMBDATA/PCH_SMBCLK<br>PCH_SMBDATA/PCH_SMBCLK<br>PCH_SMBDATA/PCH_SMBCLK<br>PCH_SMBDATA/PCH_SMBCLK |

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 3 of 102

**SSID = CPU**

CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

JE40 delete eDP function

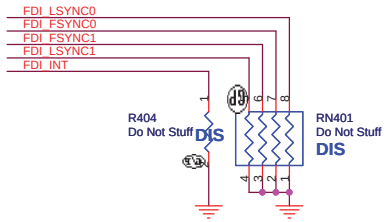
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

**Stuff to disable internal graphics function for power saving.**






HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/DMI/FDI)
Size: A3
Document Number: JE40-HR
Rev: -1
Date: Thursday, December 02, 2010
Sheet 4 of 102

**SSID = CPU**

CPU1B
SANDY

2 OF 9

SANDY

MISC
- 18 H_SNB_IVB# → C26 SNB_IVB#
- JE40 modify AN34 SKTOCC#

THERMAL
- JE40 modify AL33 CATERR#
- 22,27 H_PECI AN33 PECI
- 27,42 H_PROCHOT# → R513 56R2J-4-GP → H_PROCHOT# R AL32 PROCHOT#
- 22,36 H_THERMTRIP# AN32 THERMTRIP#

PWR MANAGEMENT
- 19 H_PM_SYNC AM34 PM_SYNC
- R503 10KR2J-GP
- 22,36,97 H_CPUPWRGD AP33 UNCOREPWRGOOD
- 19,37 PM_DRAM_PWRGD → R505 DX Do Not Stuff → V8 SM_DRAMPWROK
- 37 VDDPWRGOOD
- BUF_CPU_RST# AR33 RESET#

CLOCKS
- BCLK A28 / BCLK# A27 → CLK_EXP_P 20 / CLK_EXP_N 20
- DPLL_REF_SSCLK A16 / DPLL_REF_SSCLK# A15 → CLK_DP_P_R / CLK_DP_N_R → RN502 Do Not Stuff DIS → JE40 modify → 1D05V_VTT

DDR3 MISC
- SM_DRAMRST# R8 → R502 4K99R2F-L-GP → SM_DRAMRST# 37
- SM_RCOMP0 AK1 → SM_RCOMP_0 R506 140R2F-GP
- SM_RCOMP1 A5 → SM_RCOMP_1 R507 25D5R2F-GP
- SM_RCOMP2 A4 → SM_RCOMP_2 R508 200R2F-L-GP

JTAG & BPM
- PRDY# AP29 / PREQ# AP27 JE40 modify
- TCK AR26 / TMS AR27 / TRST# AP30 → XDP_TRST#
- TDI AR28 / TDO AP26 → XDP_TDO
- DBR# AL35 → XDP_DBRESET#
- BPM#0 AT28 / BPM#1 AR29 / BPM#2 AR30 / BPM#3 AT30 / BPM#4 AP32 / BPM#5 AR31 / BPM#6 AT31 / BPM#7 AR32 JE40 modify

1D05V_VTT
- R501 62R2J-GP
- H_PROCHOT#
- C502 SC47P50V2JN-3GP

**CRB : 47pf**
**CEKLT:43pf**

Connect EC to PROCHOT# through inverting OD buffer.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

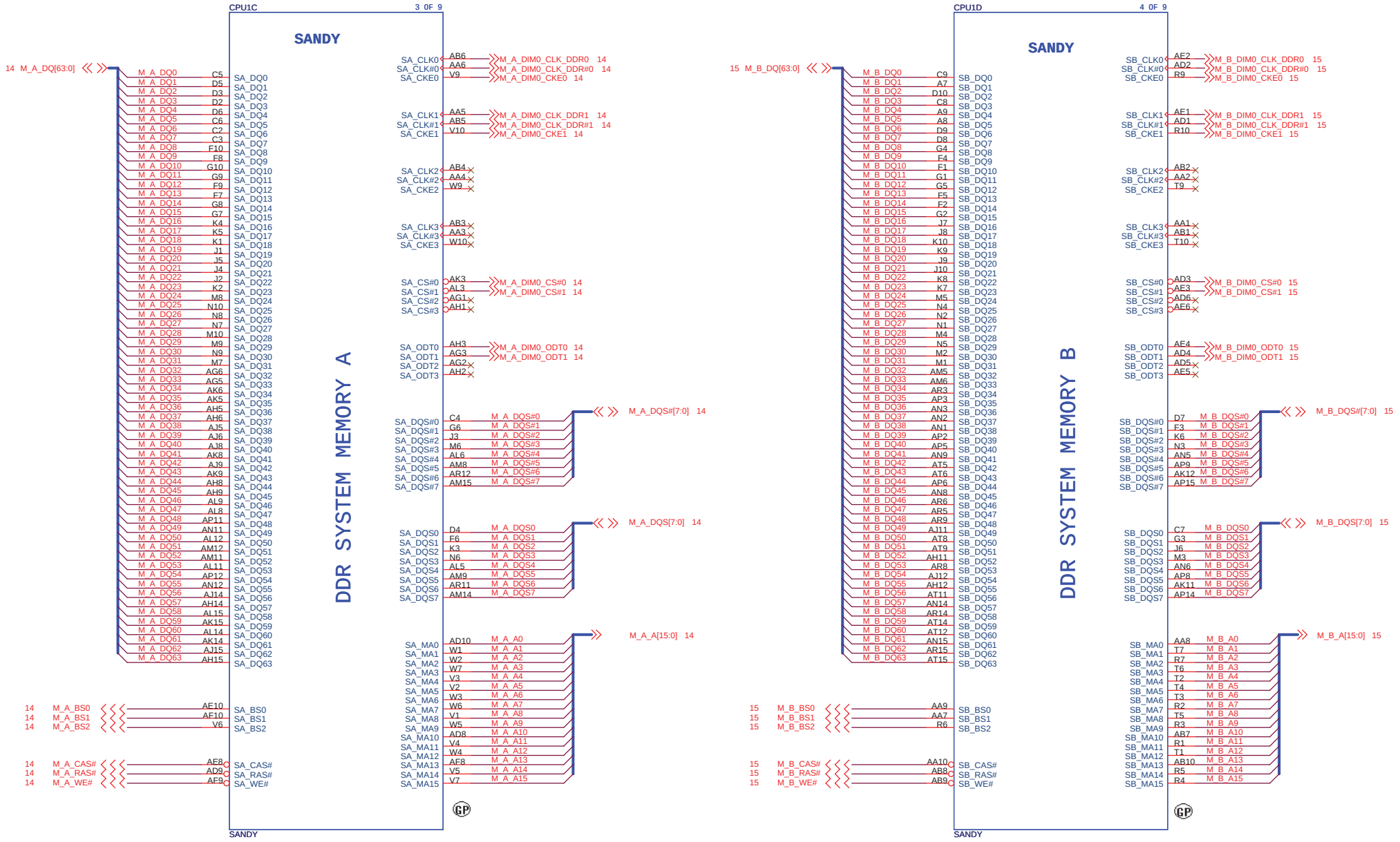
1D05V_VTT
- RN501 SRN51J-GP
- XDP_TDO
- XDP_TRST#

3D3V_S0
- RN503 SRN1K5J-1-GP
- XDP_DBRESET#
- 18,27,31,36,65,66,71,82,97 PLT_RST# → BUF_CPU_RST#

HR UMA

| | | |
|---|---|---|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: CPU (THERMAL/CLOCK/PM ) | | |
| Size: Custom | Document Number: JE40-HR | Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 5 of 102 | |

**SSID = CPU**






HR UMA

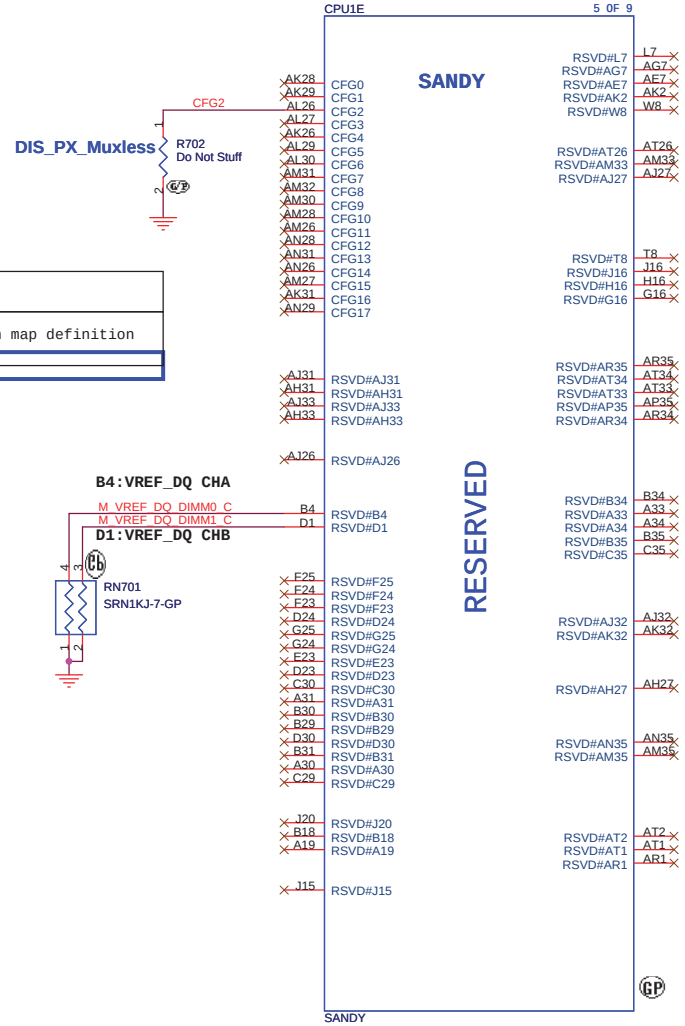
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (DDR)**

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 6 of 102

**SSID = CPU**




| PEG Static Lane Reversal | |
|---|---|
| CFG2 | 1: Normal Operation; Lane # definition matches socket pin map definition<br>0:Lane Reversed |



HR UMA

| | |
|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: CPU (RESERVED) | |
| Size: A3 | Document Number: JE40-HR — Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 7 of 102 |

SSID = CPU

# POWER

PROCESSOR CORE POWER

53A

VCC_CORE

C801 Do Not Stuff, C802 Do Not Stuff, C803 Do Not Stuff, C804 Do Not Stuff, C811 Do Not Stuff

C820 Do Not Stuff, C819 Do Not Stuff, C818 Do Not Stuff, C817 Do Not Stuff, C815 Do Not Stuff

C816 SC10U6D3V5KX-1GP, C821 Do Not Stuff, C822 SC10U6D3V5KX-1GP, C823 SC10U6D3V5KX-1GP, C824 SC10U6D3V5KX-1GP, C825 SC10U6D3V5KX-1GP, C826 SC10U6D3V5KX-1GP, C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP, C836 SC10U6D3V5KX-1GP, C835 SC10U6D3V5KX-1GP, C834 SC10U6D3V5KX-1GP, C833 SC10U6D3V5KX-1GP, C832 Do Not Stuff, C831 Do Not Stuff, C828 SC10U6D3V5KX-1GP

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

CPU1F — SANDY — 6 OF 9

CORE SUPPLY

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

SANDY

PEG AND DDR

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 F14 F12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

C805 C806 C807 C809 C810 C838 C839 C840 C841 SC10U6D3V5KX-1GP

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

C812 C813 C814 C829 C830 C842 Do Not Stuff, C843 Do Not Stuff, C844 SC10U6D3V5KX-1GP, C845 SC10U6D3V5KX-1GP

SVID

VIDALERT# A29 H_CPU_SVIDALRT# — R803 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK A30 H_CPU_SVIDCLK 42
VIDSOUT A28 H_CPU_SVIDDAT 42

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT — H_CPU_SVIDDAT — R804 130R2F-1-GP

SENSE LINES

VCC_CORE

R801,R802 close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE A35 — VCCSENSE 42
VSS_SENSE A34 — VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 — VCCIO_SENSE 45
VSSIO_SENSE A10 — VSSIO_SENSE 45



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 8 of 102

**SSID = CPU**

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

**R906,R907 close to CPU**

# POWER

CPU1G — 7 OF 9 — SANDY

VCC_GFXCORE

**PROCESSOR VAXG: 24A**

C901 Do Not Stuff, C902 SC10U6D3V5KX-1GP, C903 SC10U6D3V5KX-1GP, C904 SC10U6D3V5KX-1GP, C905 SC10U6D3V5KX-1GP, C906 Do Not Stuff — DY — UMA_PX_Muxless

C907 Do Not Stuff, C908 SC10U6D3V5KX-1GP, C918 Do Not Stuff, C919 SC10U6D3V5KX-1GP, C920 SC10U6D3V5KX-1GP, C921 SC10U6D3V5KX-1GP — DY — UMA_PX_Muxless

VAXG: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17

## GRAPHICS

### SENSE LINES

VAXG_SENSE — AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE — AK34 — VSS_AXG_SENSE 42

VCC_AXG_SENSE — R906 100R2F-L1-GP-U
VSS_AXG_SENSE — R907 100R2F-L1-GP-U

**Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.**

**+V_SM_VREF_CNT should have 10 mil trace width**

### VREF

SM_VREF — AL1 — +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

### DDR3 -1.5V RAILS

1D5V_S0

**PROCESSOR VDDQ: 10A**

VDDQ: AF7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

C909 Do Not Stuff — DY, C910 SC10U6D3V5KX-1GP, C911 SC10U6D3V5KX-1GP, C912 SC10U6D3V5KX-1GP, C913 SC10U6D3V5KX-1GP, C914 Do Not Stuff — DY

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

**PROCESSOR VCCSA: 6A**

C916 Do Not Stuff — DY, C915 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

VCCSA: M27, M26, L26, J26, J25, J24, H26, H25

### SA RAIL

0D85V_S0

R902 10R2J-2-GP

**R902 need be close to pin H23.**

VCCSA_SENSE — H23 — VCCUSA_SENSE — TP901 Do Not Stuff

FC_C22 — C22 — H_FC_C22
VCCSA_VID1 — C24 — VCCSA_SEL 48

RN901 SRN1KJ-7-GP

### 1.8V RAIL

1D8V_S0

**PROCESSOR VCCPLL: 1.2A**

VCCPLL: B6, A6, A2

C922 SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

### MISC

SANDY

VCC_GFXCORE

R903 Do Not Stuff — DIS, R904 Do Not Stuff — DIS, R905 Do Not Stuff — DIS, R901 Do Not Stuff — DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

HR UMA

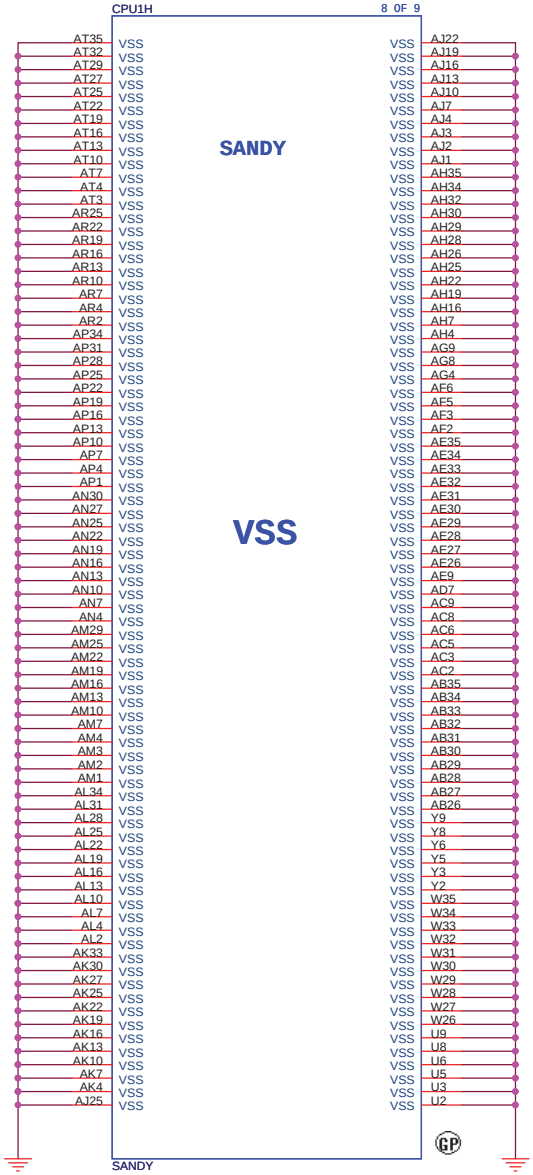
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

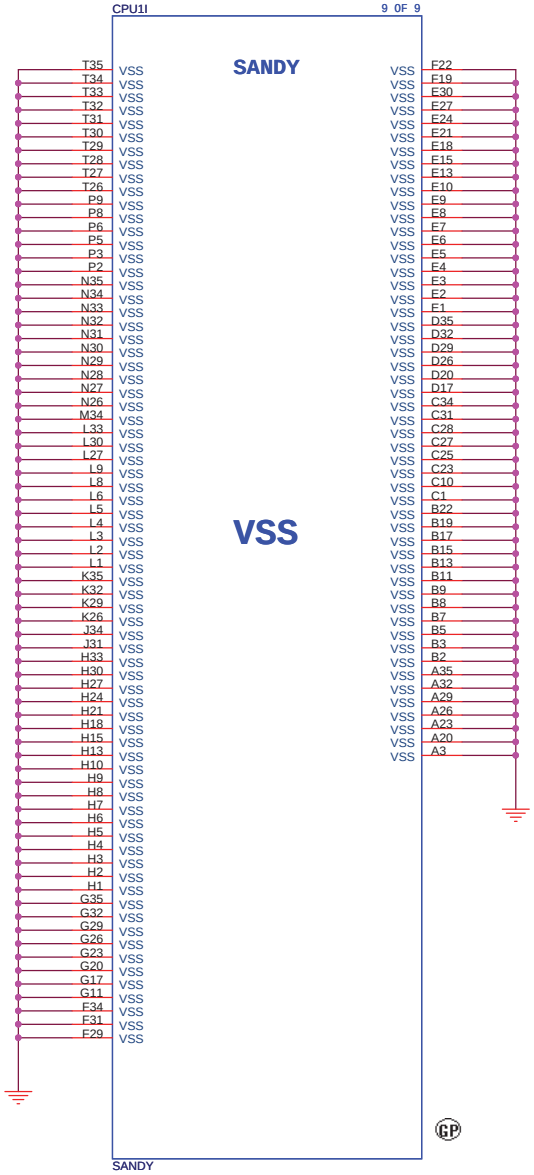
Title: **CPU (VCC_GFXCORE)**

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 — Sheet 9 of 102

SSID = CPU






HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 10 of 102

**JE40 delete XDP function**



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***XDP***

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 11 of 102

(Blanking)

HR UMA

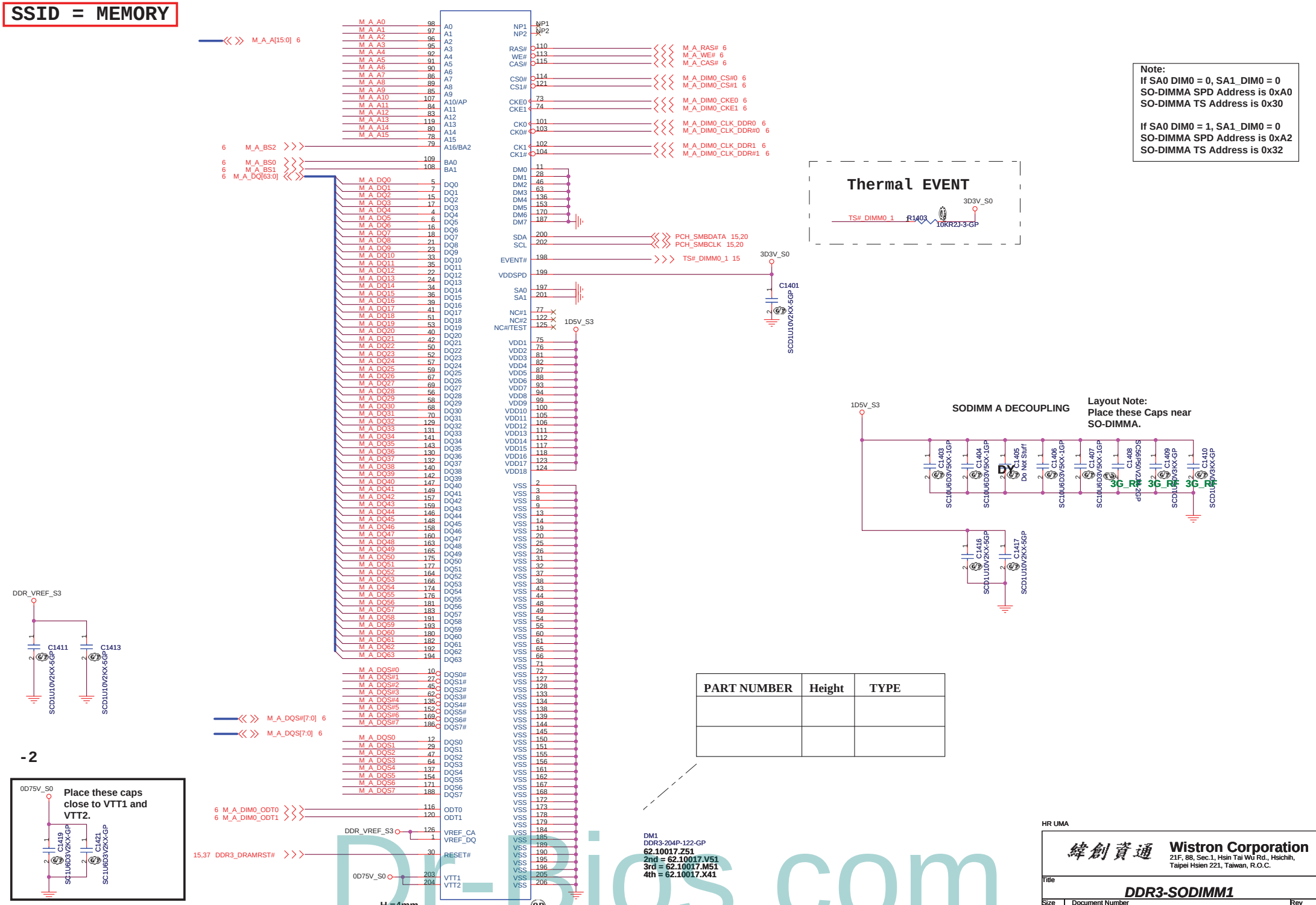
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 13 of 102

# SSID = MEMORY




Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

## Thermal EVENT




## SODIMM A DECOUPLING

Layout Note:
Place these Caps near
SO-DIMMA.




Place these caps close to VTT1 and VTT2.




DM1
DDR3-204P-122-GP
62.10017.Z51
2nd = 62.10017.V51
3rd = 62.10017.M51
4th = 62.10017.X41

| PART NUMBER | Height | TYPE |
|---|---|---|
| | | |
| | | |

-2

HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

| Size | Document Number | Rev |
|---|---|---|
| Custom | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 14 of 102

**SSID = MEMORY**


DM2
DDR3-204P-126-GP
62.10024.D41

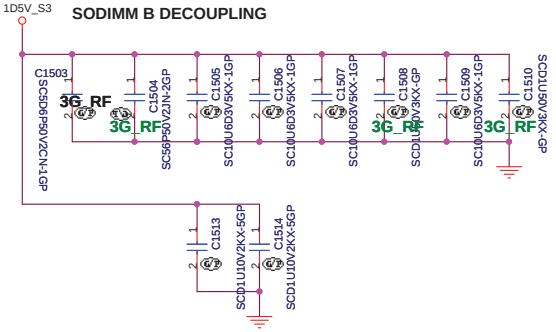
2nd = 62.10017.R91
3rd = 62.10017.V61
4th = 62.10017.X51

H = 8mm

**Note:**
**SO-DIMMB SPD Address is 0xA4**
**SO-DIMMB TS Address is 0x34**

**SO-DIMMB is placed farther from the Processor than SO-DIMMA**

**SODIMM B DECOUPLING**




**Layout Note:**
**Place these Caps near SO-DIMMB.**

DDR_VREF_S3
C1515 SCD1U10V2KX-5GP
C1517 SCD1U10V2KX-5GP

-2

**Place these caps close to VTT1 and VTT2.**

0D75V_S0
C1519 SC10U6D3V2KX-GP
C1521 SC10U6D3V2KX-GP



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

| Size | Document Number | Rev |
|---|---|---|
| Custom | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 15 of 102

(Blanking)

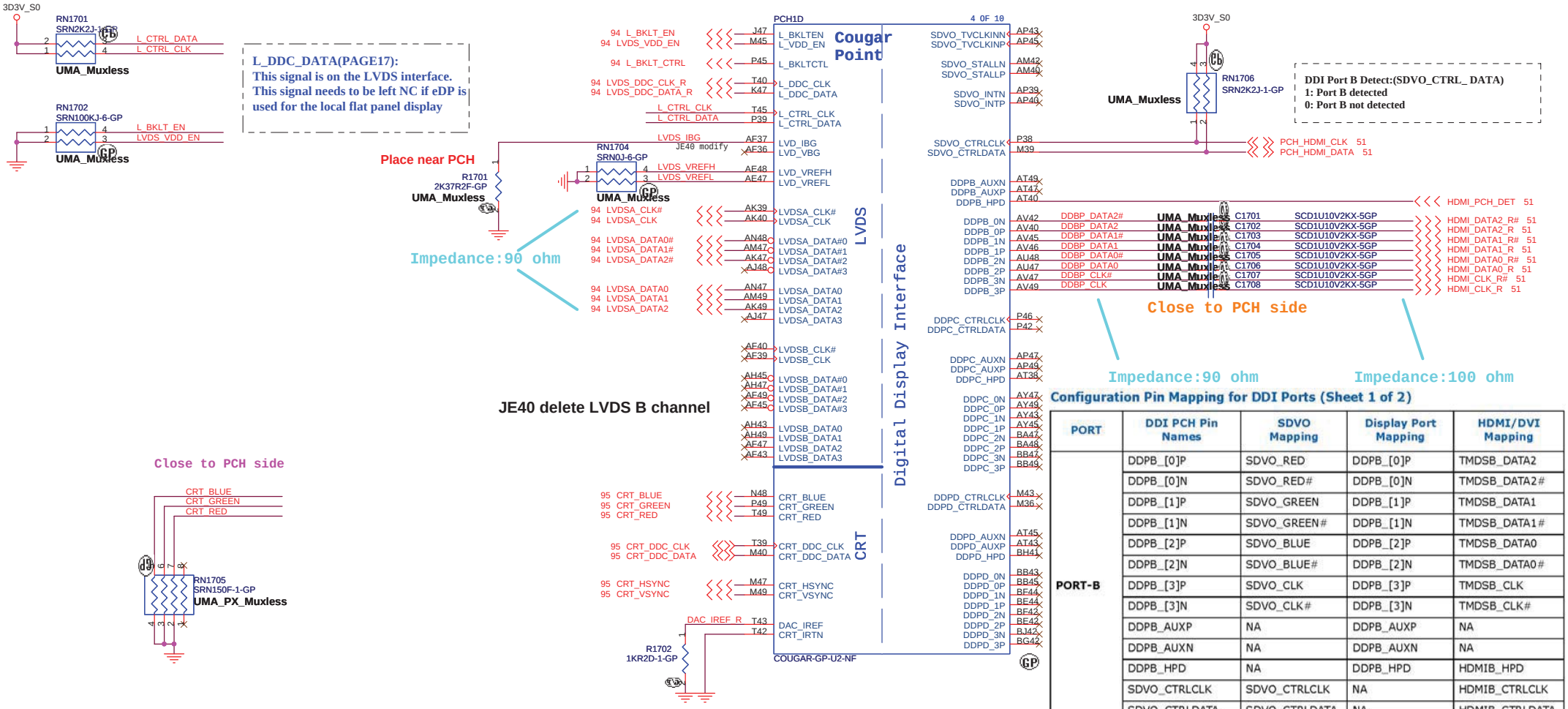
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: A4 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 16 of 102




**Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)**

| PORT | DDI PCH Pin Names | SDVO Mapping | Display Port Mapping | HDMI/DVI Mapping |
|---|---|---|---|---|
| PORT-B | DDPB_[0]P | SDVO_RED | DDPB_[0]P | TMDSB_DATA2 |
| | DDPB_[0]N | SDVO_RED# | DDPB_[0]N | TMDSB_DATA2# |
| | DDPB_[1]P | SDVO_GREEN | DDPB_[1]P | TMDSB_DATA1 |
| | DDPB_[1]N | SDVO_GREEN# | DDPB_[1]N | TMDSB_DATA1# |
| | DDPB_[2]P | SDVO_BLUE | DDPB_[2]P | TMDSB_DATA0 |
| | DDPB_[2]N | SDVO_BLUE# | DDPB_[2]N | TMDSB_DATA0# |
| | DDPB_[3]P | SDVO_CLK | DDPB_[3]P | TMDSB_CLK |
| | DDPB_[3]N | SDVO_CLK# | DDPB_[3]N | TMDSB_CLK# |
| | DDPB_AUXP | NA | DDPB_AUXP | NA |
| | DDPB_AUXN | NA | DDPB_AUXN | NA |
| | DDPB_HPD | NA | DDPB_HPD | HDMIB_HPD |
| | SDVO_CTRLCLK | SDVO_CTRLCLK | NA | HDMIB_CTRLCLK |
| | SDVO_CTRLDATA | SDVO_CTRLDATA | NA | HDMIB_CTRLDATA |



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 17 of 102

# SSID = PCH

RN1801
SRN8K2J-2-GP-U

| | | | |
|---|---|---|---|
| INT_PIRQH# | 1 | 10 | 3D3V_S0 |
| INT_PIRQB# | 2 | 9 | INT_PIRQD# |
| INT_PIRQF# | 3 | 8 | INT_PIRQE# |
| INT_PIRQA# | 4 | 7 | INT_PIRQC# |
| 3D3V_S0 | 5 | 6 | USB30_SMI# |

| A16 swap override Strap/Top-Block Swap Override jumper | |
|---|---|
| PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled<br>High = Default |

**BOOT BIOS Strap**

| GNT1#/GPIO51 | SATA1GP/GPIO19 | BOOT BIOS Location |
|---|---|---|
| 0 | 0 | LPC |
| 0 | 1 | Reserved |
| 1 | 0 | Reserved |
| 1 | 1 | SPI(Default) |

PCH1E — 5 OF 10

Cougar Point

RSVD | NVRAM | PCI | USB

COUGAR-GP-U2-NF

RN1803
SRN10KJ-5-GP

DGPU_HOLD_RST# 2
DGPU_PWR_EN# 1

Do Not Stuff TP1806 — 83 DGPU_HOLD_RST# — DGPU_SELECT#
93 DGPU_PWR_EN#

Do Not Stuff TP1804 — DGPU_PWM_SELECT#

R1813 Do Not Stuff
56 SATA_ODD_DA#
82 USB30_SMI#

JE40 modify 07/16

5,27,31,36,65,66,71,82,97 PLT_RST#

71 CLK_PCI_LPC
20 CLK_PCI_FB
27 CLK_PCI_KBC

R1804 22R2J-2-GP CLK_PCI_LPC_R
R1805 22R2J-2-GP CLK_PCI_FB_R
R1806 22R2J-2-GP CLK_PCI_KBC_R

EC1803 DY Do Not Stuff
EC1802 DY Do Not Stuff
EC1801 DY Do Not Stuff

KBC CLK EMI

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

| DMI & FDI Termination Voltage | |
|---|---|
| NV_CLE | Set to Vss when LOW<br>Set to Vcc when HIGH |

check R1808 R1809 阻值

CRB : 2.2K
CEKLT: 1K

1D8V_S0
R1808 2K2R2J-2-GP
NV_CLE — R1809 1KR2J-1-GP — H_SNB_IVB# 5

USB Ext. port 1 (HS)
External debug port use on Huron river platform

SB add USB port 5

JE40 co-lay USB2.0

JE40 delete FP function
JE40 delete eDP function
JE40 delete New Card function

USB_RBIAS — R1811 22D6R2F-L1-GP

3D3V_S5
R1820 10KR2J-3-GP

## USB Table

| Pair | Device |
|---|---|
| 0 | Touch Panel / 3G SIM |
| 1 | USB Ext. port 1 (HS) |
| 2 | Fingerprint |
| 3 | BLUETOOTH |
| 4 | Mini Card2 (WWAN) |
| 5 | CARD READER(DY) |
| 6 | X |
| 7 | X |
| 8 | USB Ext. port 4 / E-SATA /USB CHARGER |
| 9 | USB Ext. port 2 |
| 10 | EDP CAMERA |
| 11 | Mini Card1 (WLAN) |
| 12 | CAMERA |
| 13 | New Card |

**USB 2.0 Overcurrent Pin Default Usage**

| Pin | Default Port Mapping | Pin | Default Port Mapping |
|---|---|---|---|
| OC0# | Port 0, Port 1 | OC4# | Port 8, Port 9 |
| OC1# | Port 2, Port 3 | OC5# | Port 10, Port 11 |
| OC2# | Port 4, Port 5 | OC6# | Port 12, Port 13 |
| OC3# | Port 6, Port 7 | OC7# | Not Used |

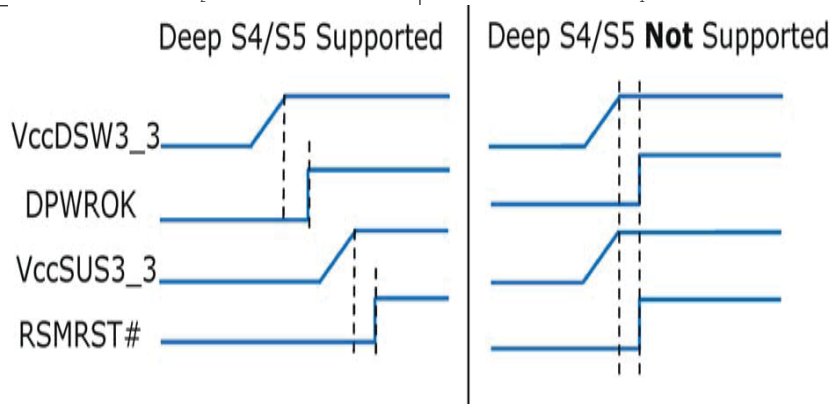
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

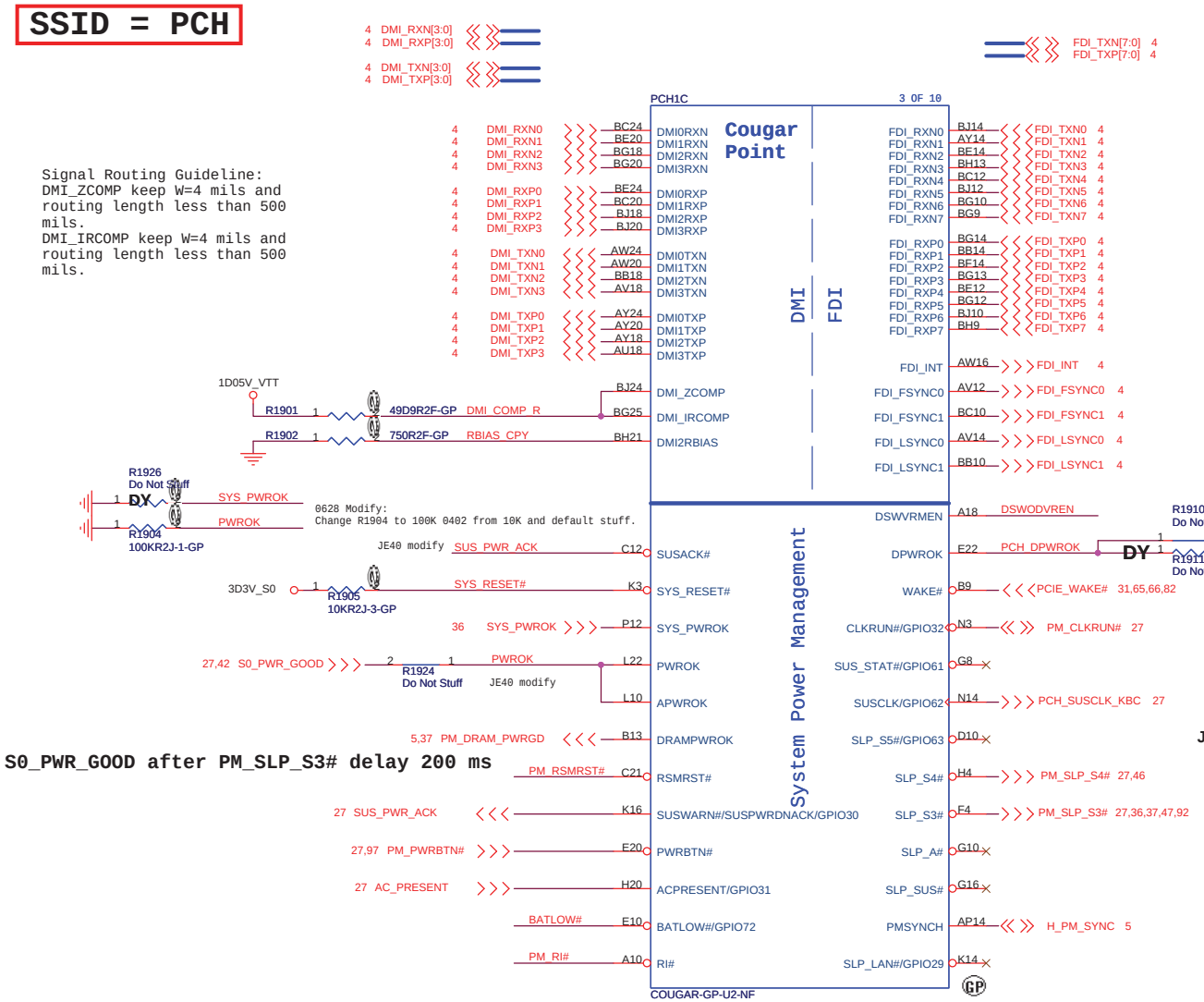
Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 18 of 102

**SSID = PCH**

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.




For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

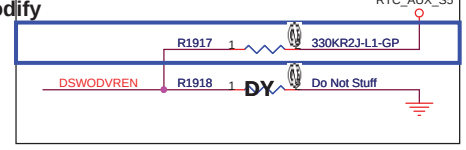


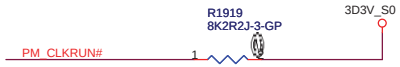

**S0_PWR_GOOD after PM_SLP_S3# delay 200 ms**

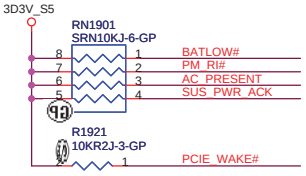
**JE40 modify 07/16**

| DSWODVREN - On Die DSW VR Enable | |
|---|---|
| HIGH | Enabled (DEFAULT) |
| LOW | Disabled |

**SB modify**

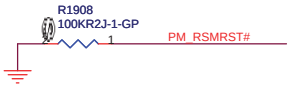


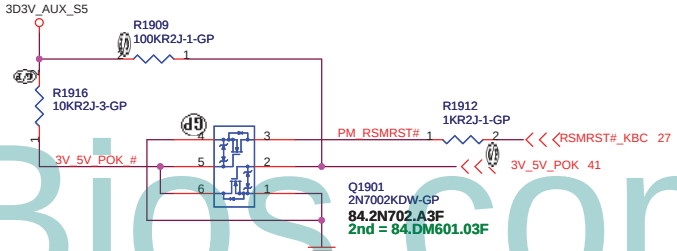




**PCIE_WAKE#**
**CRB : 1K**
**CEKLT: 10K**

**PWRBTN#**
**This signal has an internal pull-up resistor**




**PM_RSMRST#**
**CRB : PL 10K**
**ANNIE : PL 100K**






HR UMA

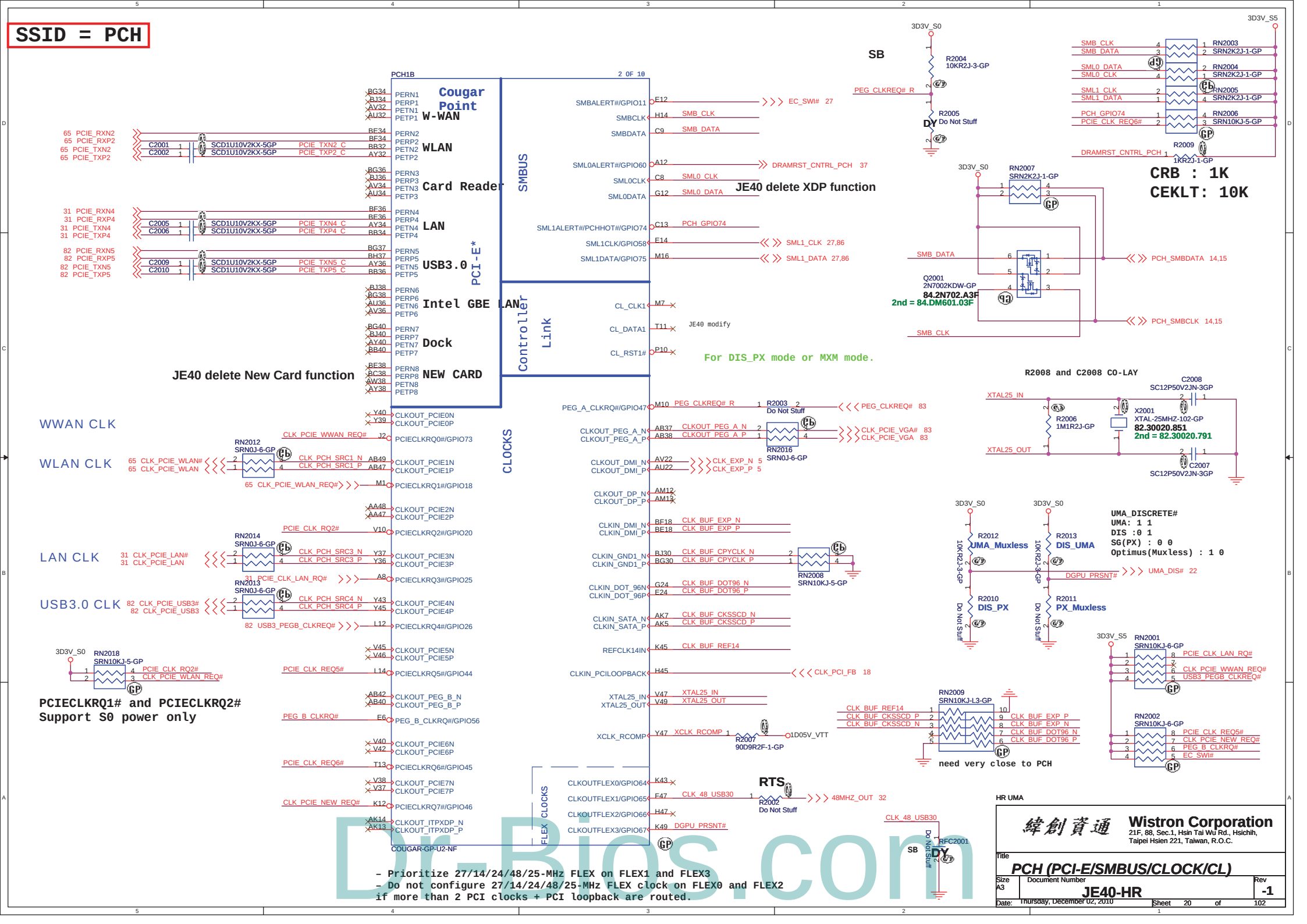
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 19 of 102

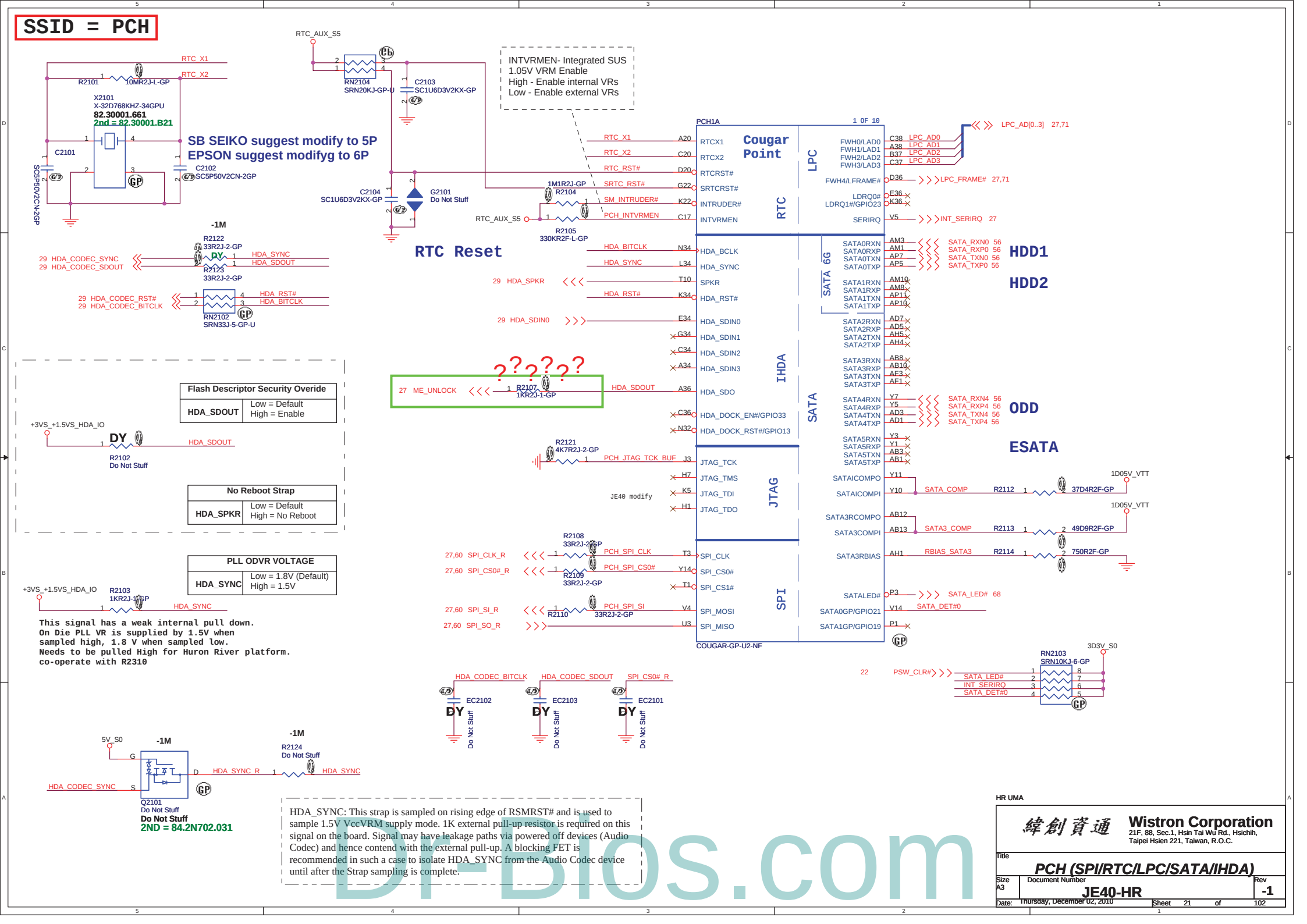
# SSID = PCH






| | |
|---|---|
| Wistron Corporation | 緯創資通 |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | PCH (PCI-E/SMBUS/CLOCK/CL) |
| Size A3 | Document Number JE40-HR |
| Rev | -1 |
| Date: Thursday, December 02, 2010 | Sheet 20 of 102 |

# SSID = PCH






HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 21 of 102

# SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

**GPIO27 has a weak[20K] internal pull up.**
**To enable on-die PLL Voltage regurator,**
**should not place external pull down.**

| | INTERNAL GFX | EXTERNAL GFX |
|---|---|---|
| R2205 | DY | 10K |
| R2206 | 100K | DY |

**Pass Word Clear**

**JE40 delete G Sensor**

**SB add Zero ODD function**

**SB 公板 check different , check need modify or not check intel , R2204**

**TS Signal Disable Guideline:**
**TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.**

| FDI TERMINATION VOLTAGE OVERRIDE | |
|---|---|
| GPIO37 (FDI_OVRVLTG) | LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT) |

| DMI TERMINATION VOLTAGE OVERRIDE | |
|---|---|
| GPIO36 (DMI_OVRVLTG) | LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT) |

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

| Integrated Clock Chip Enable | |
|---|---|
| ICC_EN# | HIGH (R2211 DY)- DISABLED [DEFAULT] |
| | LOW (R2211)- ENABLED |

**GPIO8 has a weak[20K] internal pull up.**
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

**SB VRAM Frequency**
**Pull high: 800MHZ**
**Pull low :900MHZ**

**VRAM Size**

| PLL ON DIE VR ENABLE |
|---|
| NOTE:This signal has a weak internal pull-up 20K<br>ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT<br>DISABLED -- LOW (R2212 STUFFED) |



HR UMA

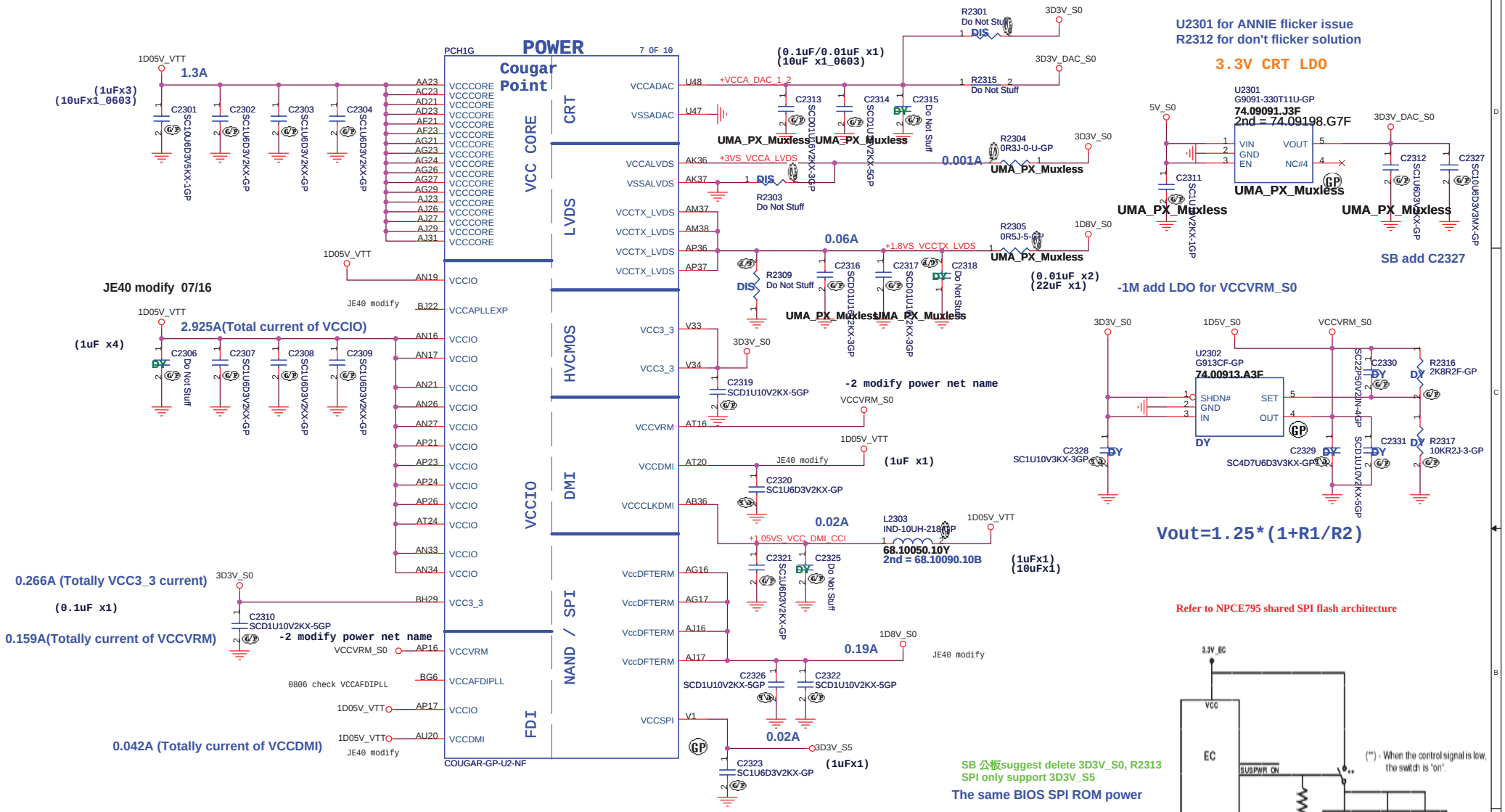
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 22 of 102

**SSID = PCH** 6A






HR UMA

| | | |
|---|---|---|
| 緯創資通 | Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | PCH (POWER1) | |
| Size A3 | Document Number JE40-HR | Rev -1 |
| Date: Thursday, December 02, 2010 | Sheet 23 of 102 | |

JE40 modify 07/16

**SSID = PCH**

PCH1J

POWER

10 OF 10

Cougar Point

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

COUGAR-GP-U2-NF

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.16A (Totally current of VCCVRM

0.08A

0.055A

0.095A

0.001A

6uA

0.01A

-1M

-1M modify power net name

JE40 modify 07/16

DY

Do Not Stuff

2nd = 83.R2004.B8F

2nd = 68.10090.10B

68.10050.10Y

Dr-Bios.com

HR UMA

Wistron Corporation

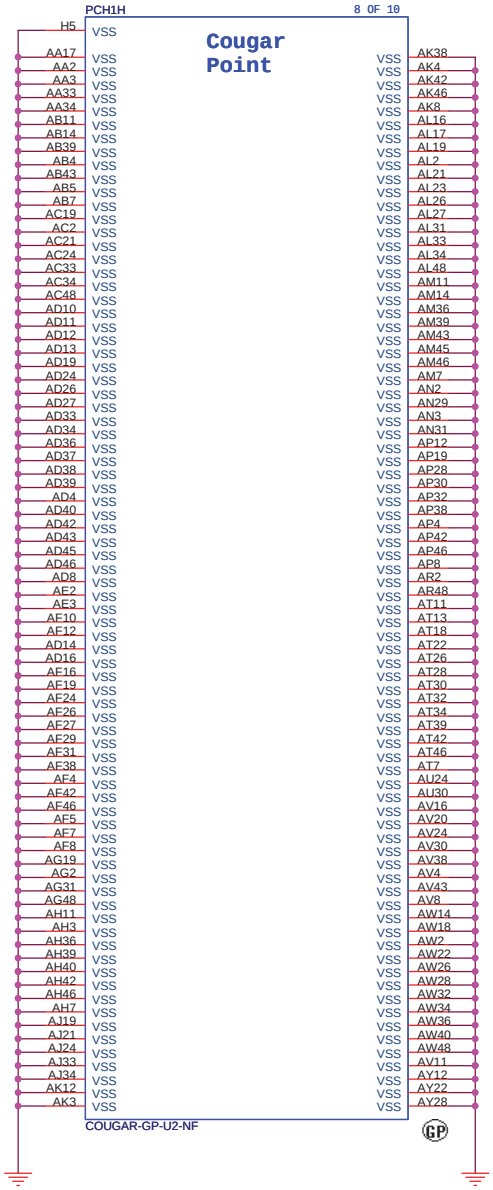
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

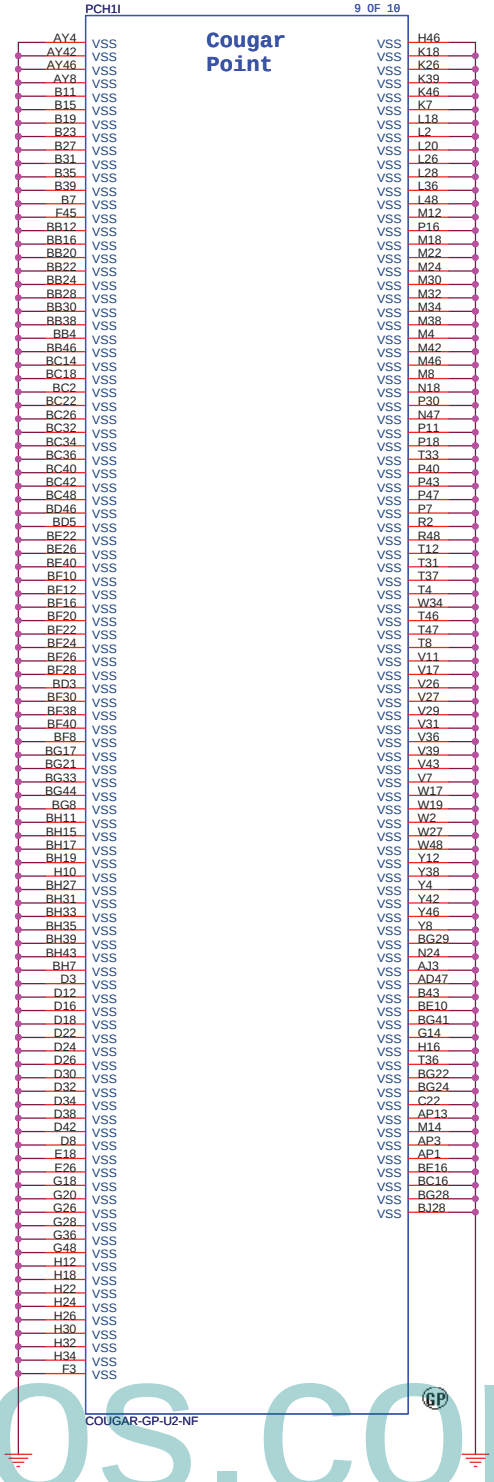
Title: PCH (POWER2)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 24 of 102

**SSID = PCH**






HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 25 of 102

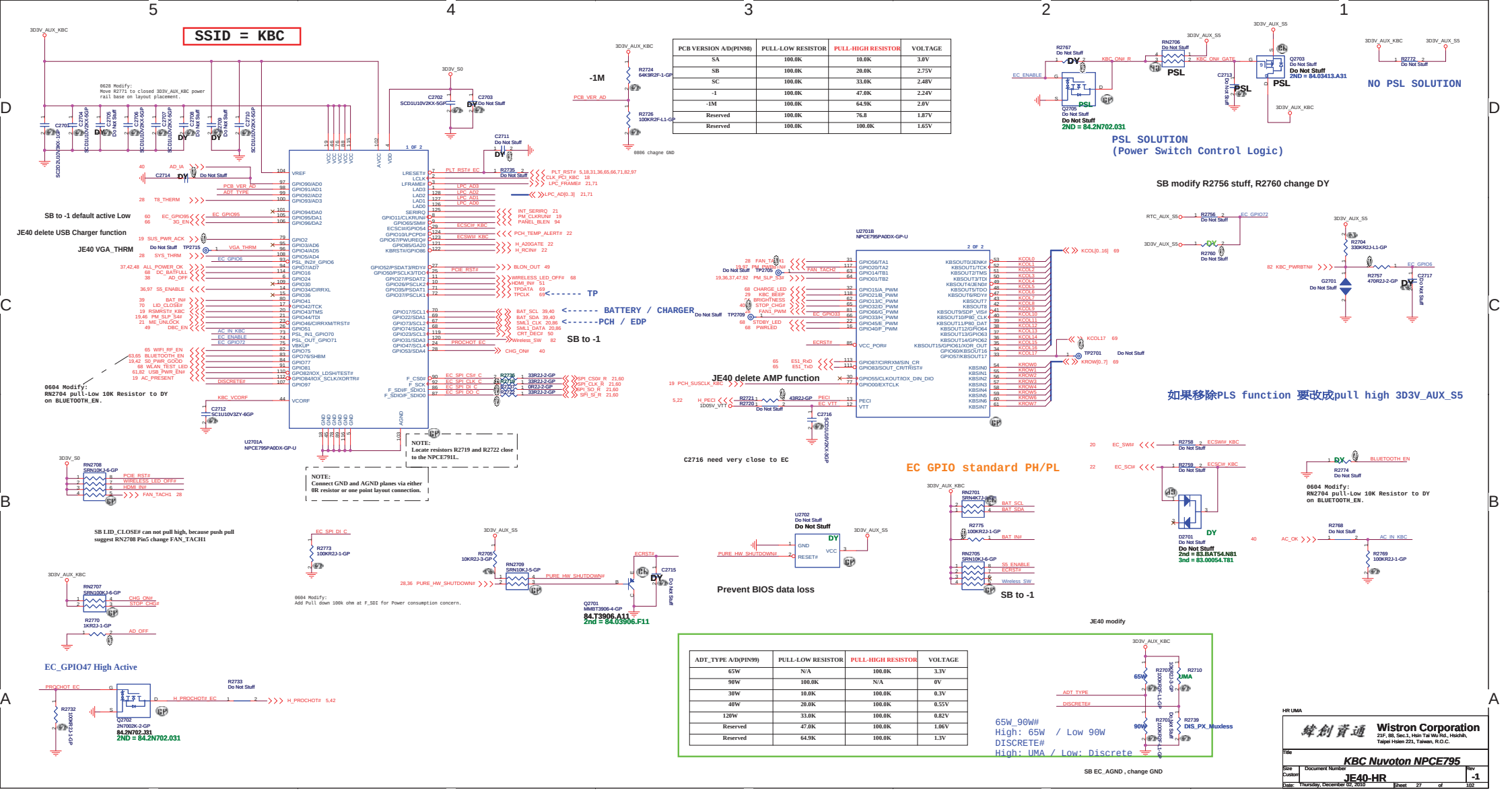
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Clock(colay)***

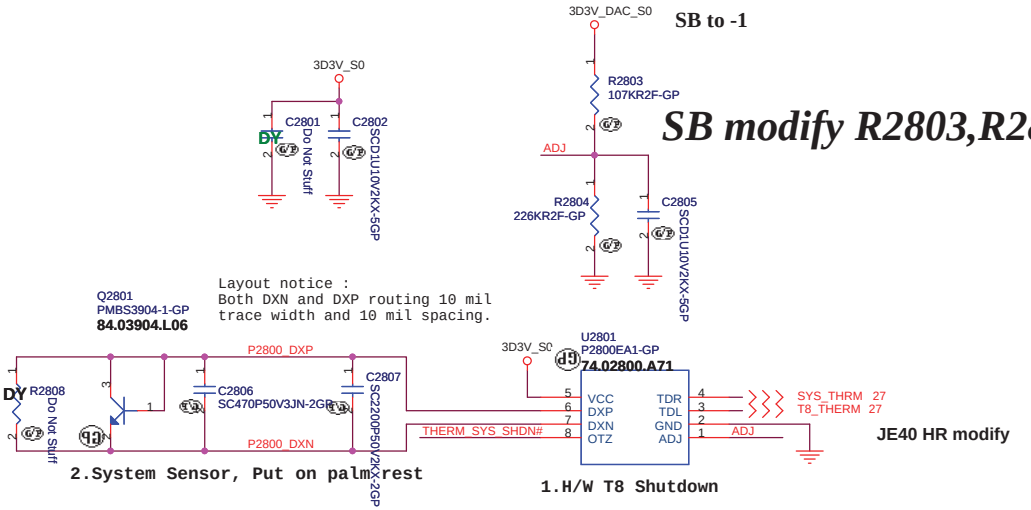
| Size | Document Number | Rev |
|---|---|---|
| A4 | **JE40-HR** | **-1** |

Date: Thursday, December 02, 2010 Sheet 26 of 102


SSID = KBC
0628 Modify:
Move R2771 to closed 3D3V_AUX_KBC power rail base on layout placement.
SB to -1 default active Low
JE40 delete USB Charger function
JE40 VGA_THRM
0604 Modify:
RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.
NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.
NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.
U2701A
NPCE795PA0DX-GP-U
-1M
PCB VERSION A/D(PIN98) | PULL-LOW RESISTOR | PULL-HIGH RESISTOR | VOLTAGE
SA | 100.0K | 10.0K | 3.0V
SB | 100.0K | 20.0K | 2.75V
SC | 100.0K | 33.0K | 2.48V
-1 | 100.0K | 47.0K | 2.24V
-1M | 100.0K | 64.9K | 2.0V
Reserved | 100.0K | 76.8 | 1.87V
Reserved | 100.0K | 100.0K | 1.65V
0886 chagne GND
<------ TP
<------ BATTERY / CHARGER
<------PCH / EDP
SB to -1
JE40 delete AMP function
C2716 need very close to EC
EC GPIO standard PH/PL
Prevent BIOS data loss
SB to -1
SB LID_CLOSE# can not pull high, because push pull suggest RN2708 Pin5 change FAN_TACH1
0604 Modify:
Add Pull down 100k ohm at F_SDI for Power consumption concern.
Q2701
MMBT3906-4-GP
84.T3906.A11
2nd = 84.03906.F11
EC_GPIO47 High Active
Q2702
2N7002K-3-GP
84.2N702.X81
2ND = 84.2N702.031
JE40 modify
ADT_TYPE A/D(PIN99) | PULL-LOW RESISTOR | PULL-HIGH RESISTOR | VOLTAGE
65W | N/A | 100.0K | 3.3V
90W | 100.0K | N/A | 0V
30W | 10.0K | 100.0K | 0.3V
40W | 20.0K | 100.0K | 0.55V
120W | 33.0K | 100.0K | 0.82V
Reserved | 47.0K | 100.0K | 1.06V
Reserved | 64.9K | 100.0K | 1.3V
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
SB EC_AGND , change GND
Q2703
Do Not Stuff
2ND = 84.03413.A31
PSL SOLUTION
(Power Switch Control Logic)
NO PSL SOLUTION
SB modify R2756 stuff, R2760 change DY
如果移除PLS function 要改成pull high 3D3V_AUX_S5
0604 Modify:
RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC Nuvoton NPCE795
JE40-HR
Rev -1
Thursday, December 02, 2010
Sheet 27 of 102

SSID = Thermal

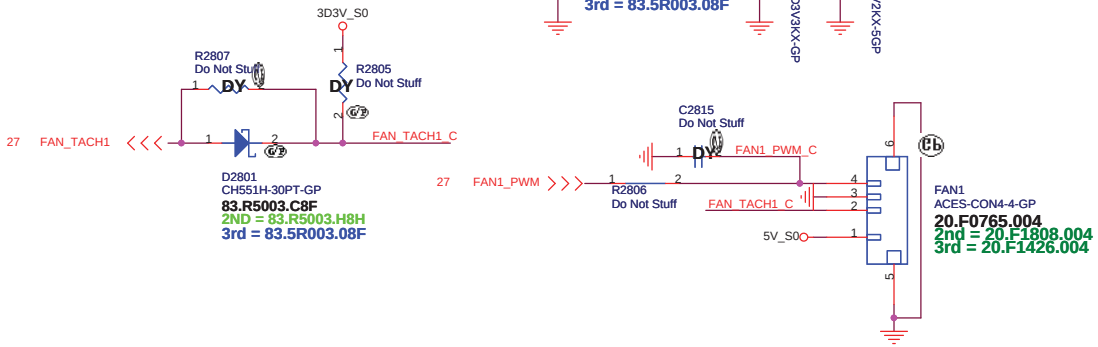
# Thermal sensor P2800




## SB modify R2803,R2804 setting

# Fan controller P2793

*Layout* 15 mil



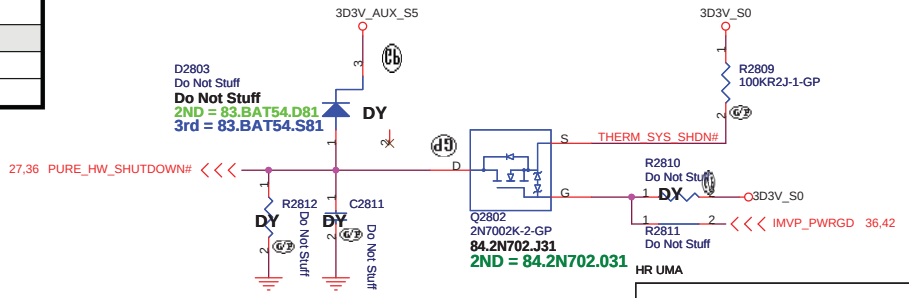

For PWM FAN

**ADJ Table** (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

| RADJ1 (KΩ) | RADJ2 (KΩ) | VADJ (v) | OTZ Threshold Temperature (°C) |
|---|---|---|---|
| 124 | 226 | 2.13 | 101 |
| 118 | 226 | 2.17 | 96.3 |
| 113 | 226 | 2.20 | 92.1 |
| 110 | 226 | 2.22 | 89.6 |
| 107 | 226 | 2.24 | 87 |
| 105 | 226 | 2.25 | 85.3 |
| 100 | 226 | 2.29 | 80.9 |

# VGA Thermal sensor P2800

## SMBUS modify to Page 84



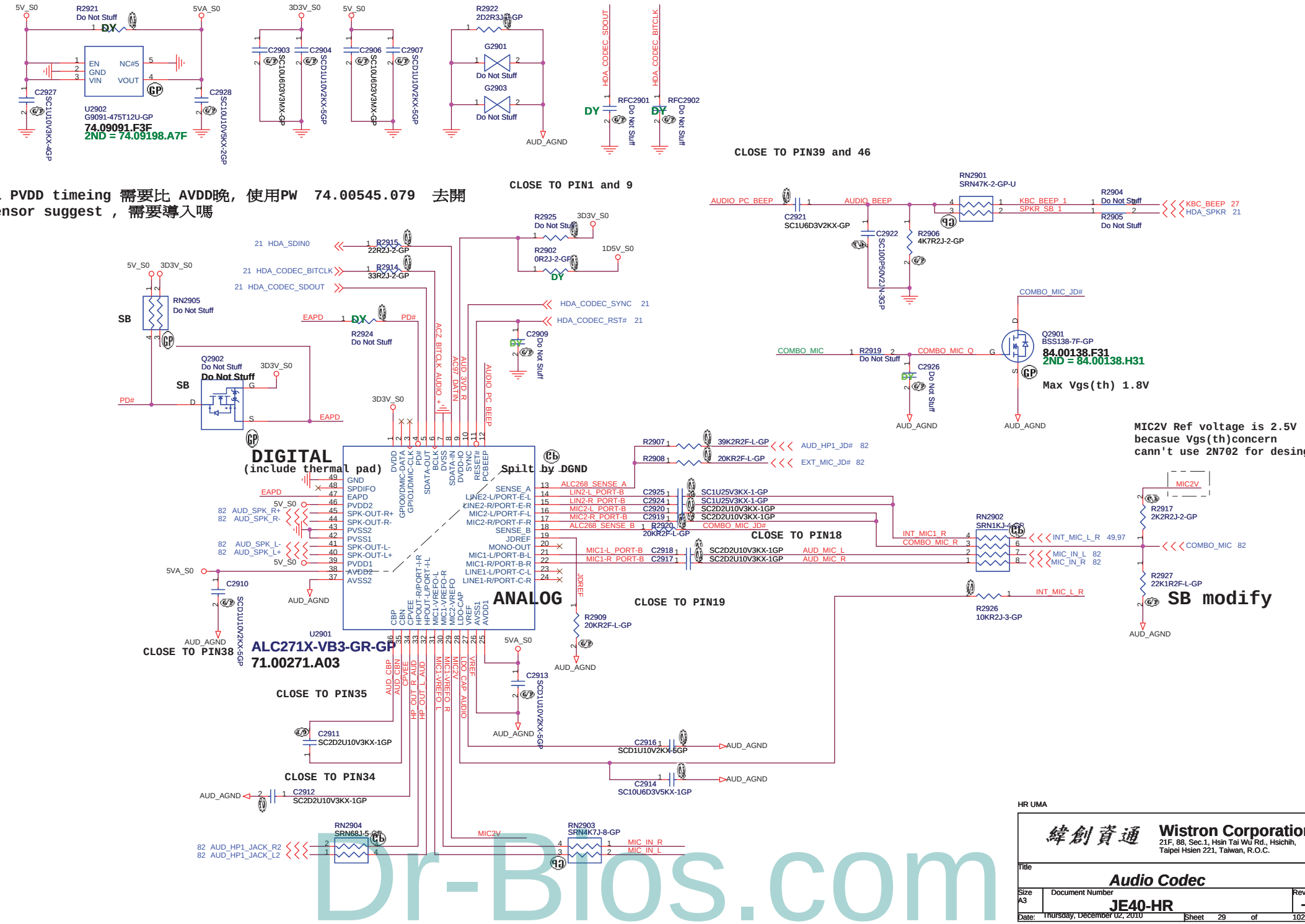


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: Thermal P2800/Fan Controllor P2793

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 28 of 102


-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎
CLOSE TO PIN1 and 9
CLOSE TO PIN39 and 46
CLOSE TO PIN18
CLOSE TO PIN19
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN38
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB3-GR-GP
71.00271.A03
U2901
U2902
G9091-475T12U-GP
74.09091.F3F
2ND = 74.09198.A7F
Q2901
BSS138-7F-GP
84.00138.F31
2ND = 84.00138.H31
Max Vgs(th) 1.8V
MIC2V Ref voltage is 2.5V
becasue Vgs(th)concern
cann't use 2N702 for desing
SB modify
SB
Do Not Stuff
DY
GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
HR UMA
Audio Codec
JE40-HR
-1
Thursday, December 02, 2010
Sheet 29 of 102

# AUDIO OP AMPLIFIER

## JE40 delete AMP function

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title: *Audio AMP* | | |
| Size: A4 | Document Number: JE40-HR | Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 30 of 102 | |

SB modify L3101,2,4,5,6 to 0 ohm

SB modify R3102 DY, R3104 to pull low

SB mmodify vendor suggest

SB delete EEPROM

128K byte

SB delete R3112

SB delete R3117

SB delete R3129 for LDO power

Card-reader Off-Page

Check VDDO_CR power plan

SB for B version

SB for B version can no use LDO delete LDO

SB to -1 modify to short pad

SB C3134, C3135 change 15P

68.00248.011

2nd = 68.00217.241

71.57785.M02

Change:71.57785.M03

10月底改打71.57785.M03

HR UMA

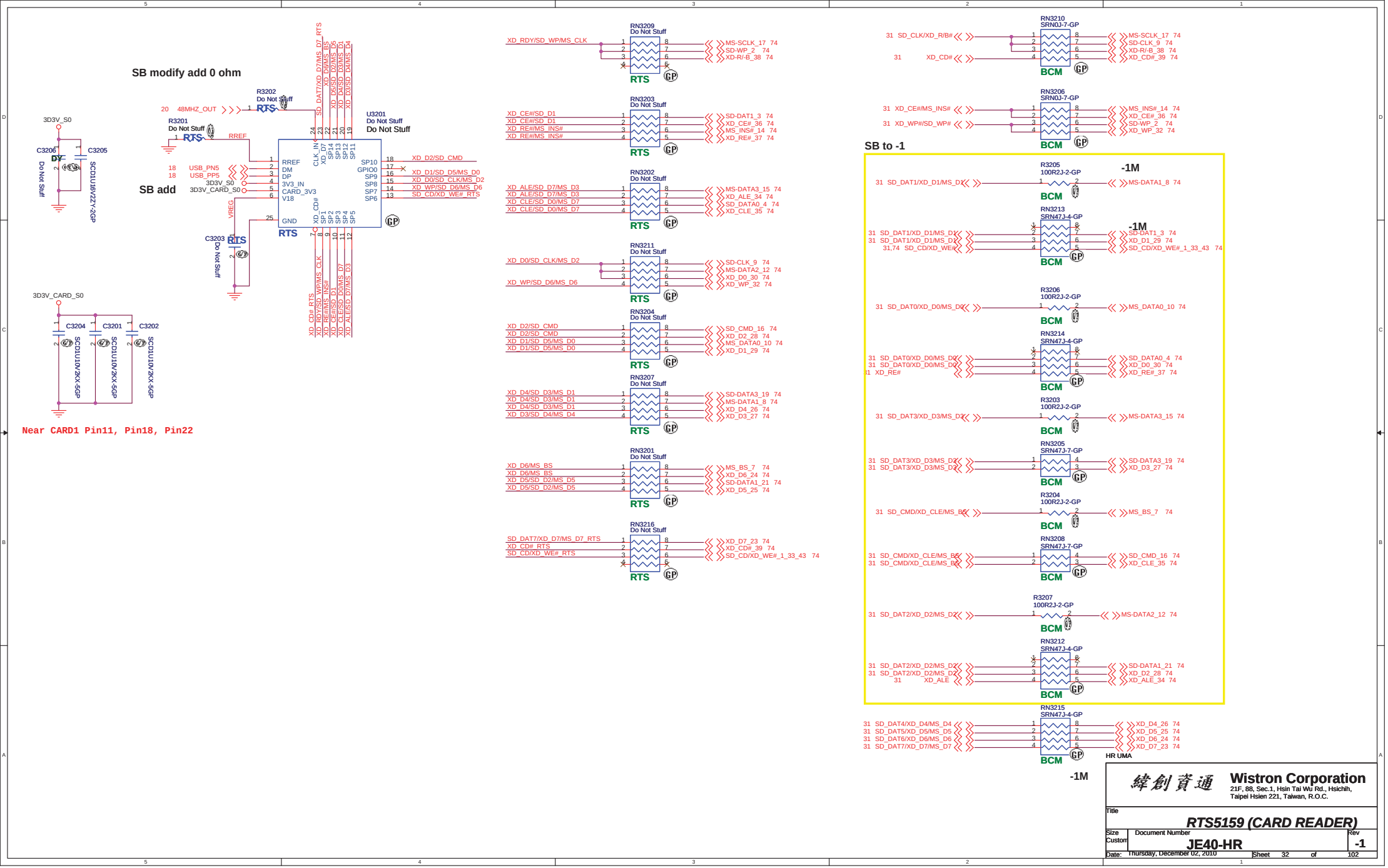
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM57780

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 31 of 102






緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RTS5159 (CARD READER)

| Size | Document Number | Rev |
|---|---|---|
| Custom | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 32 of 102

# (Blanking)

HR UMA

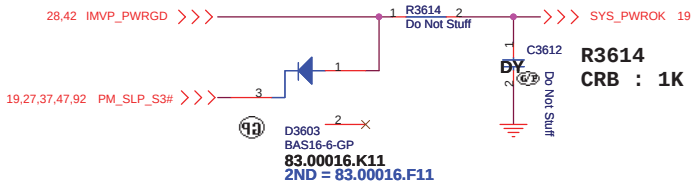
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Reserved***

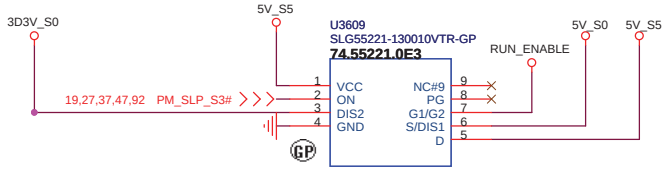
| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

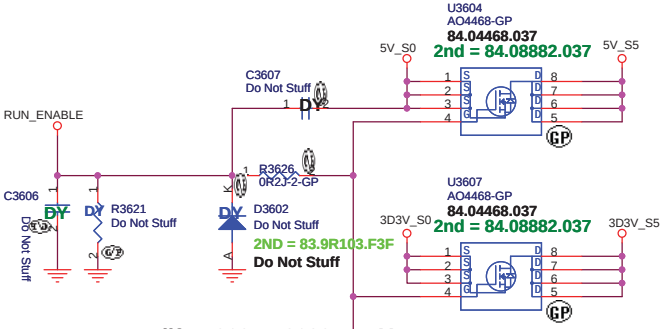
Date: Thursday, December 02, 2010 Sheet 33 of 102

# Power Sequence

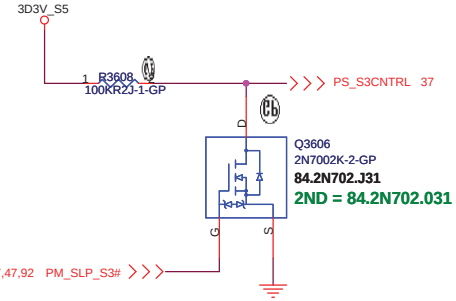



# ANNIE Run Power



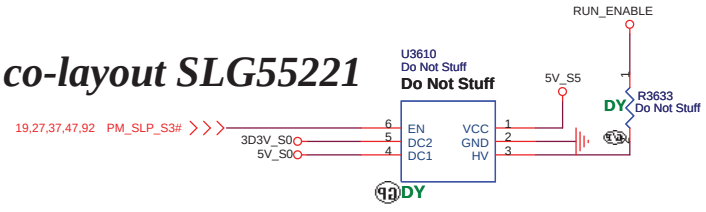



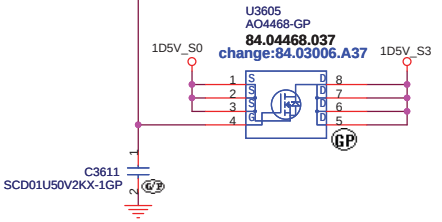

-1 modify R3621,D3602 to DY




SB modify part number

## -1 co-layout SLG55221

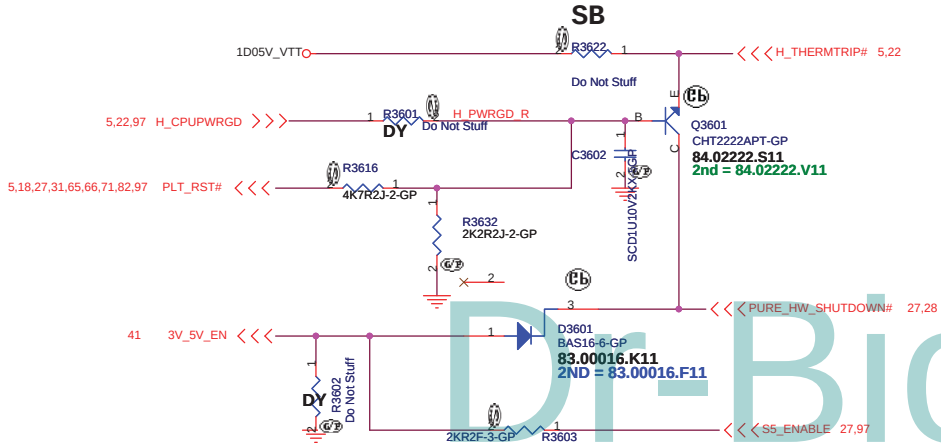



**1D5V_S0**

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

## SB






HR UMA

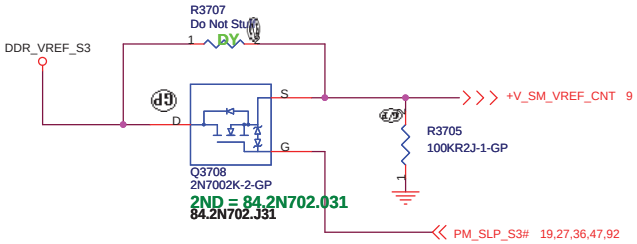
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

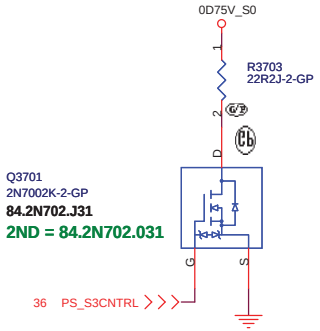
| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 36 of 102

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

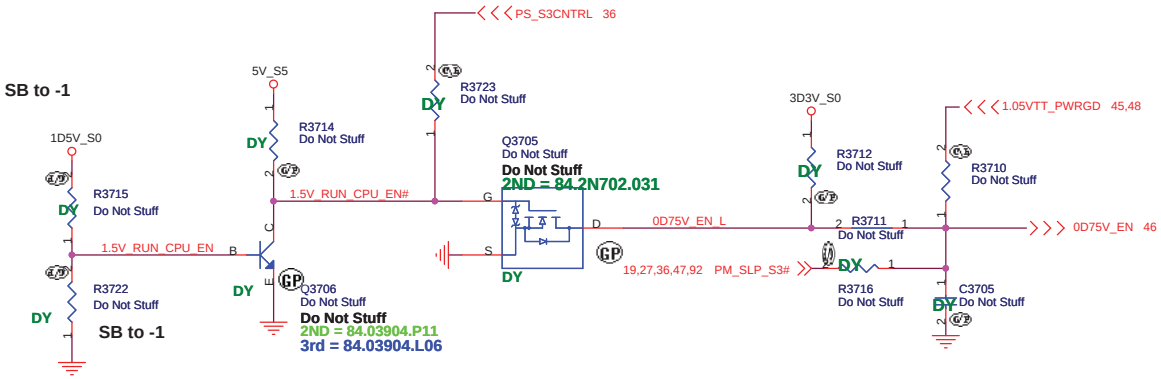



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

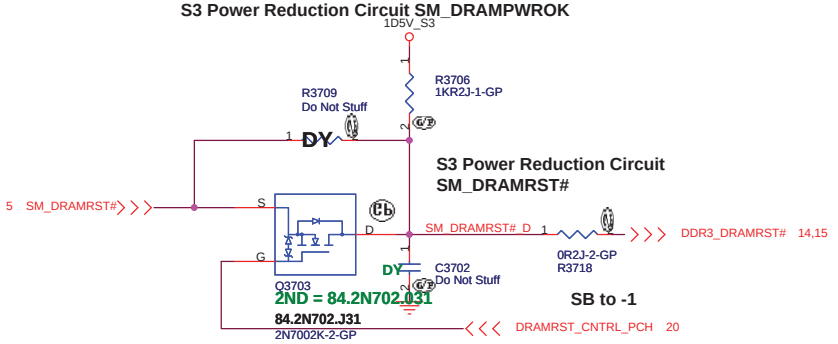



5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

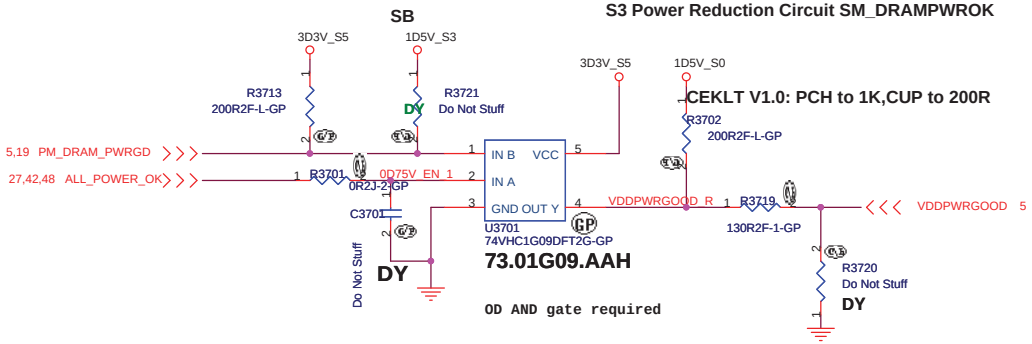
SB to -1 reserve R3723




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK




For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time
over VDDQ * 0.55± 200mV and the edge must be monotonic



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

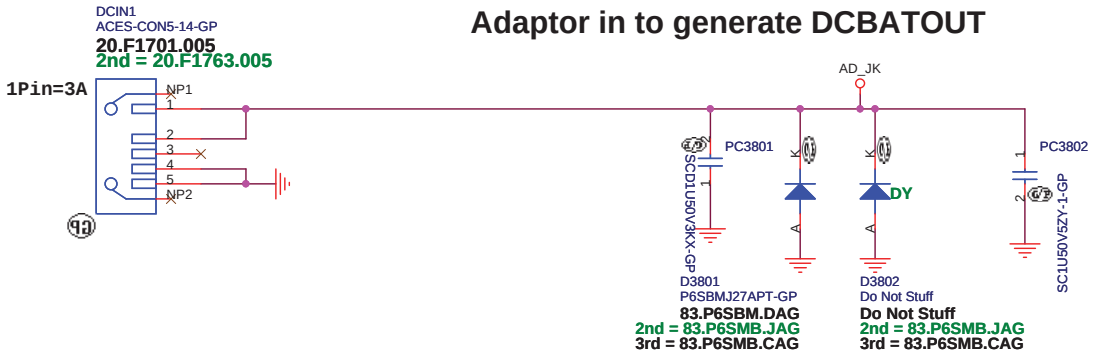
Title: ADAPTER

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

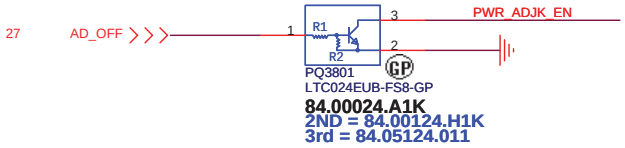
Date: Thursday, December 02, 2010 Sheet 37 of 102

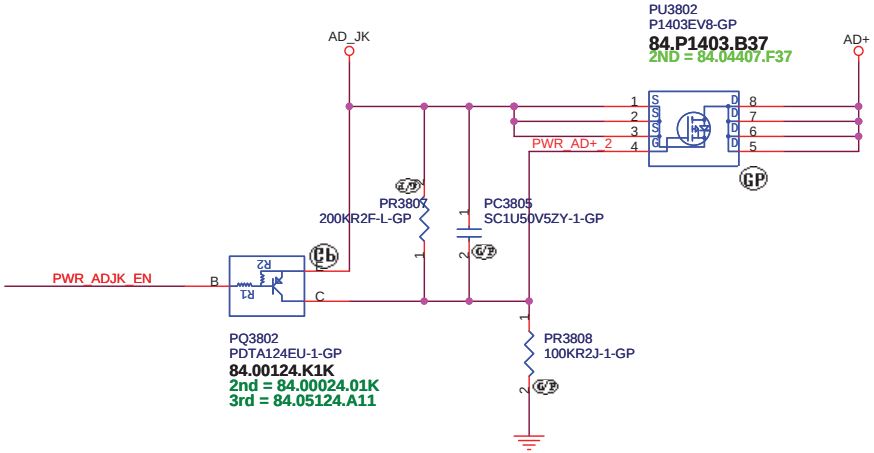
# *ANNIE solution*

## Adaptor in to generate DCBATOUT




**JE40 change DCIN1 part number**

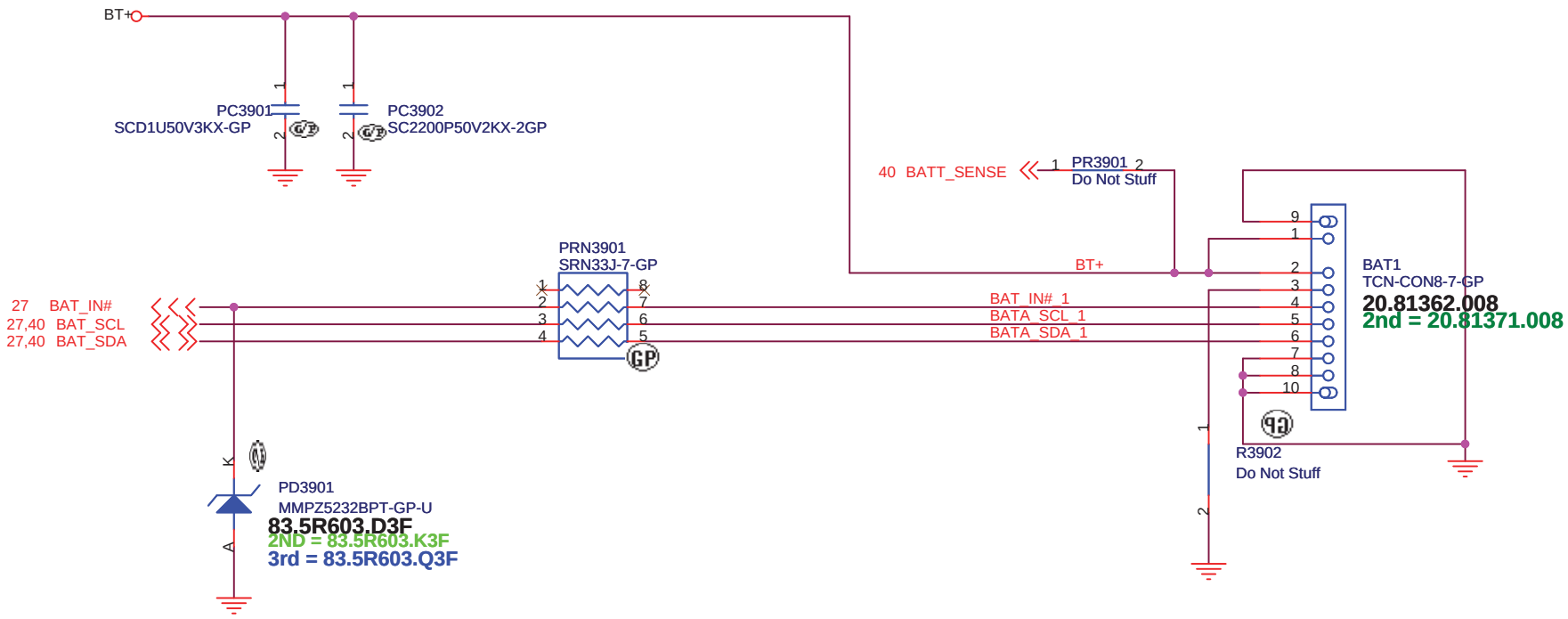



HR UMA

| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***DCIN JACK*** | |
| Size: Custom | Document Number: **JE40-HR** | Rev: **-1** |
| Date: Thursday, December 02, 2010 | Sheet 38 of 102 | |

# BATTERY CONNECTOR




EC Protect

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 39 of 102

| AD+ total power | R1 | R2 | AD+ total power | R1 | R2 |
|---|---|---|---|---|---|
| 65w | 187k | 49.9k | 80w | 137k | 49.9k |
| 90w | 121k | 49.9k | | | |

NEAR

ADD A 24V ZENAR

20100706 Wayne

20100721

20101018

JE40 HR RF

-1M

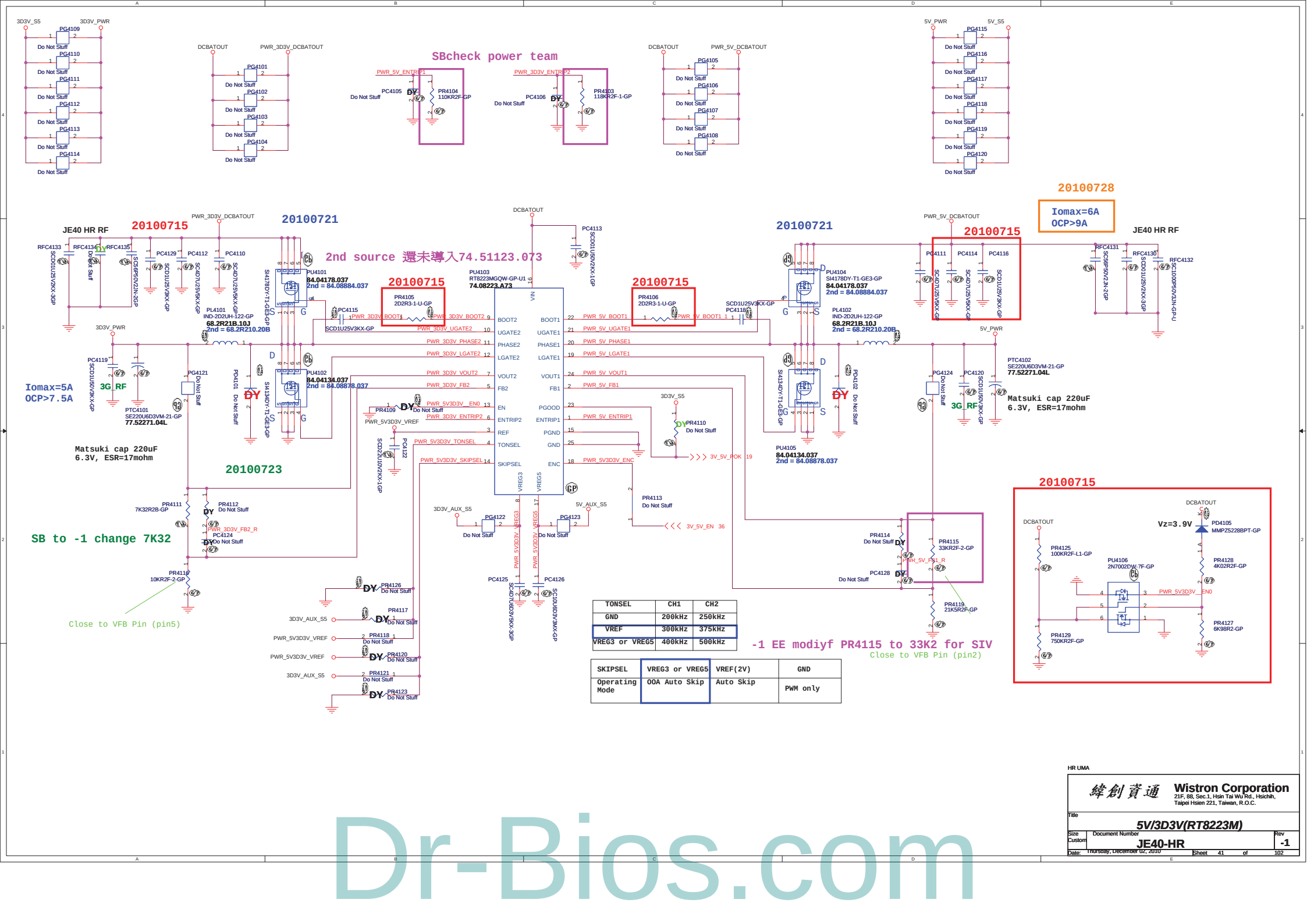
-1M

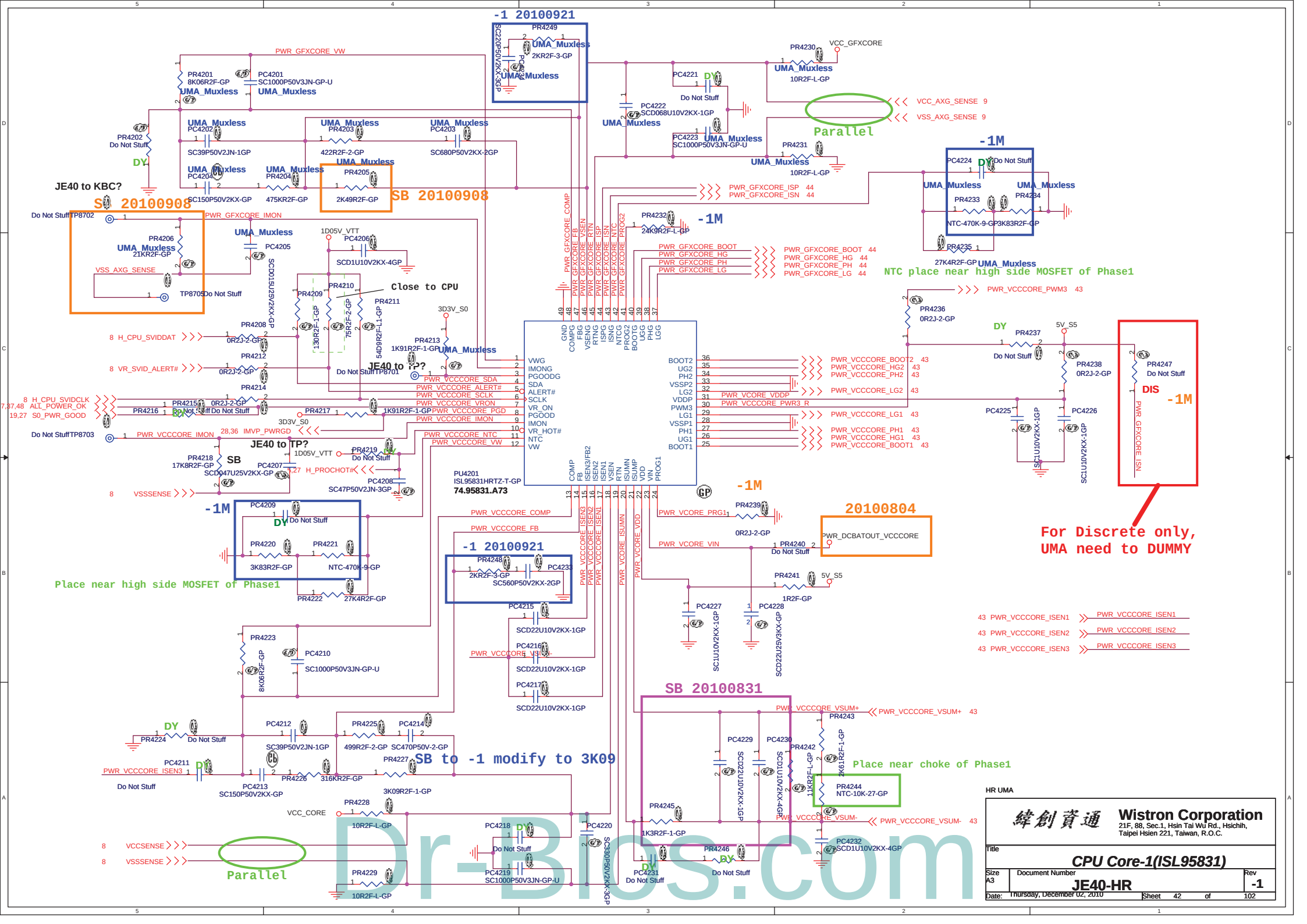
AC_OK to KBC

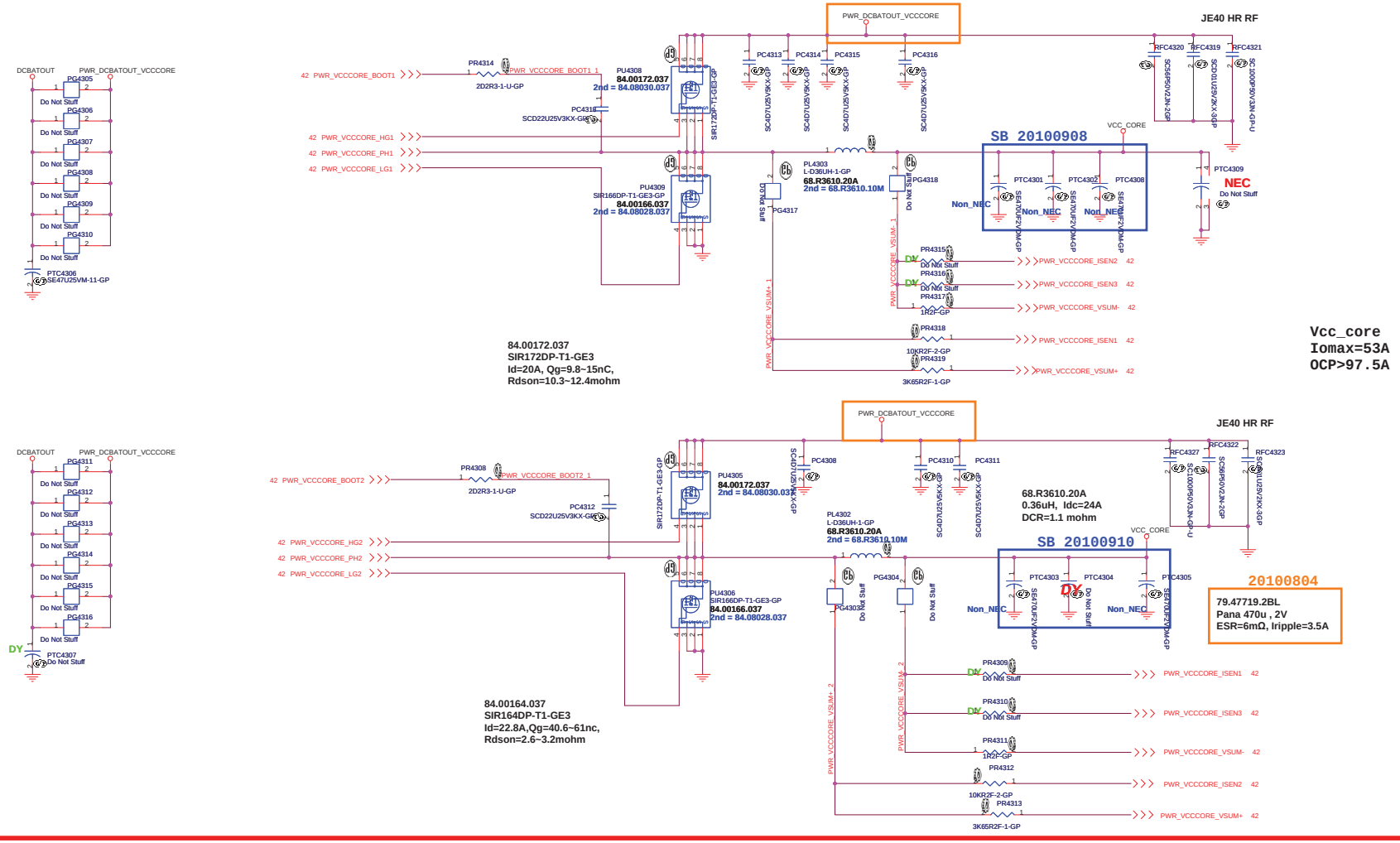
HR UMA

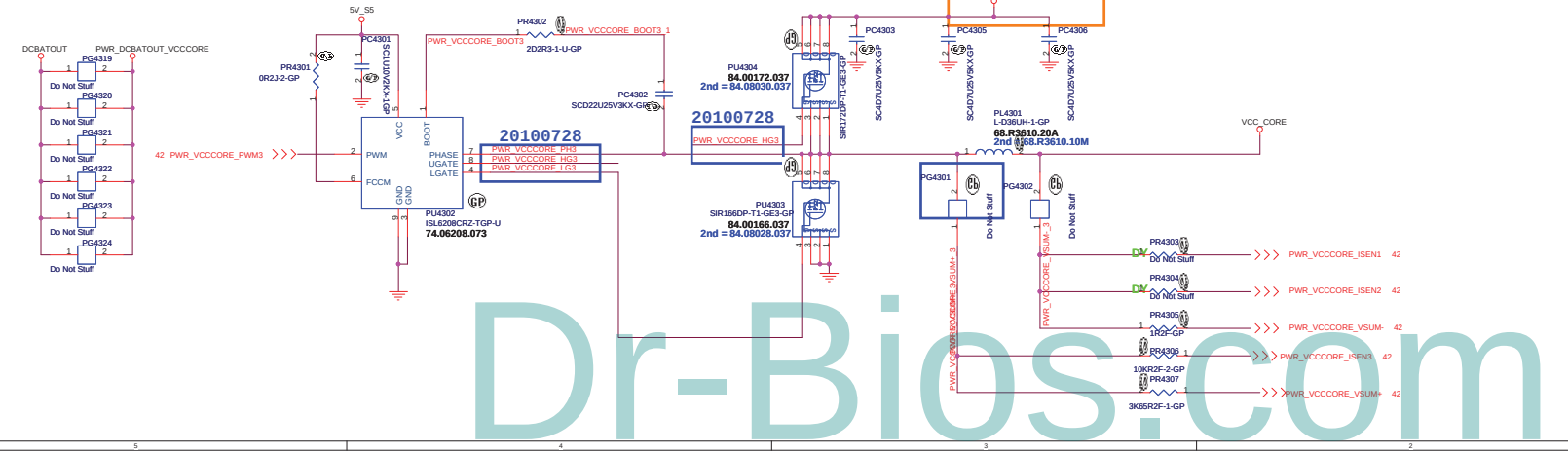


| | |
|---|---|
| Wistron Corporation | 緯創資通 |
| 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: CHARGER BQ24745 | |
| Size: A3 | Document Number: JE40-HR |
| Rev: -1 | |
| Date: Thursday, December 02, 2010 | Sheet 40 of 102 |


SBcheck power team
20100728
Iomax=6A
OCP>9A
JE40 HR RF
20100715
20100721
20100723
2nd source 還未導入74.51123.073
Iomax=5A
OCP>7.5A
3G_RF
Matsuki cap 220uF
6.3V, ESR=17mohm
SB to -1 change 7K32
Close to VFB Pin (pin5)
-1 EE modiyf PR4115 to 33K2 for SIV
Close to VFB Pin (pin2)
Vz=3.9V
Do Not Stuff
DY
TONSEL | CH1 | CH2
GND | 200kHz | 250kHz
VREF | 300kHz | 375kHz
VREG3 or VREG5 | 400kHz | 500kHz
SKIPSEL | VREG3 or VREG5 | VREF(2V) | GND
Operating Mode | OOA Auto Skip | Auto Skip | PWM only
HR UMA
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
5V/3D3V(RT8223M)
JE40-HR
-1
Thursday, December 02, 2010
41
102


-1 20100921
SB 20100908
JE40 to KBC?
SB 20100908
Close to CPU
JE40 to TP?
JE40 to TP?
SB
-1M
Place near high side MOSFET of Phase1
-1 20100921
SB to -1 modify to 3K09
SB 20100831
Place near choke of Phase1
Parallel
Parallel
-1M
NTC place near high side MOSFET of Phase1
-1M
20100804
PWR_DCBATOUT_VCCCORE
For Discrete only,
UMA need to DUMMY
DIS
-1M
PU4201
ISL95831HRTZ-T-GP
74.95831.A73
Dr-Bios.com
HR UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Core-1(ISL95831)
Size A3
Document Number
JE40-HR
Rev -1
Date: Thursday, December 02, 2010
Sheet 42 of 102





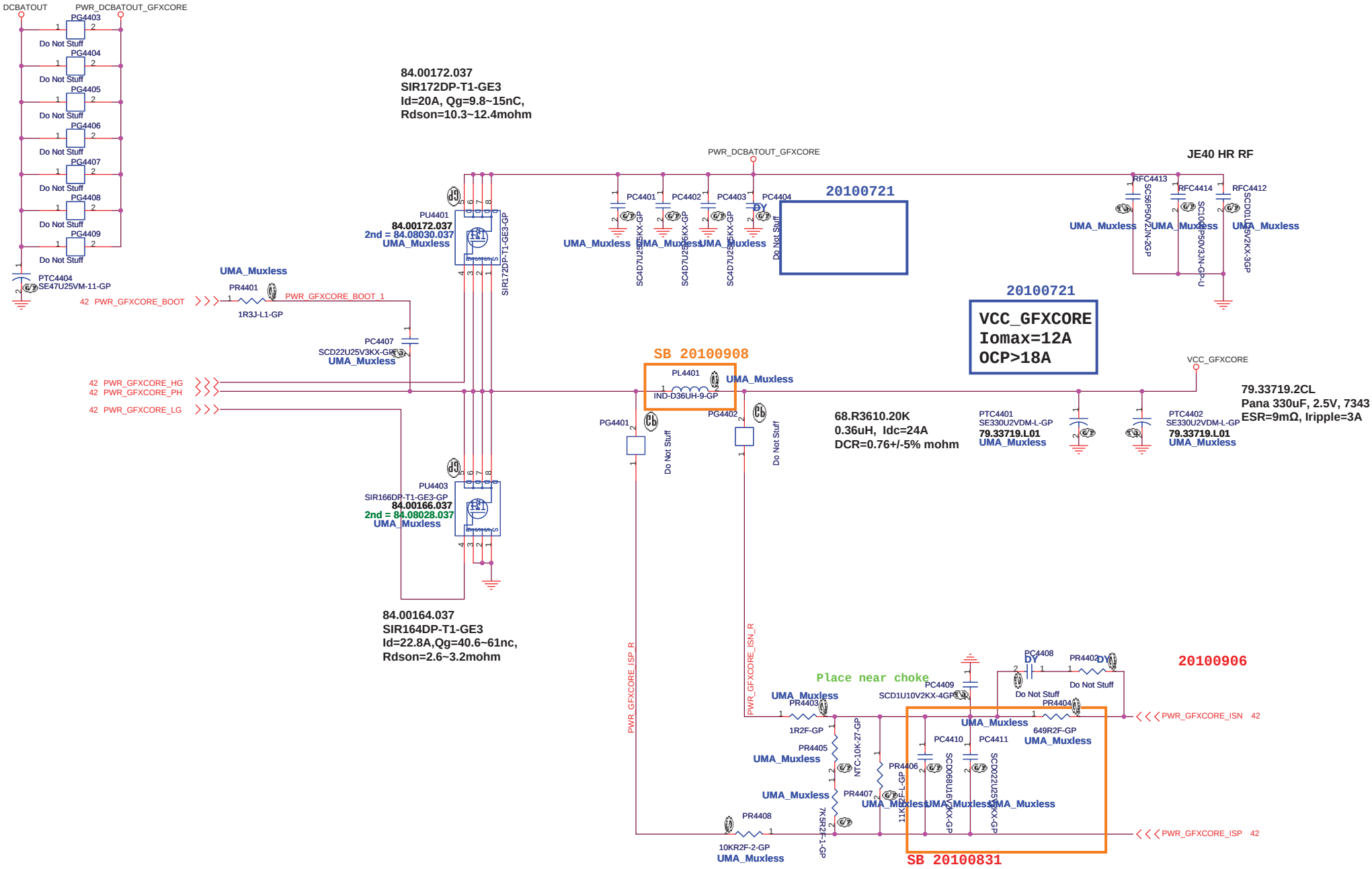

HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Core-2(ISL95831)

Size: A2 | Document Number: JE40-HR | Rev: -1

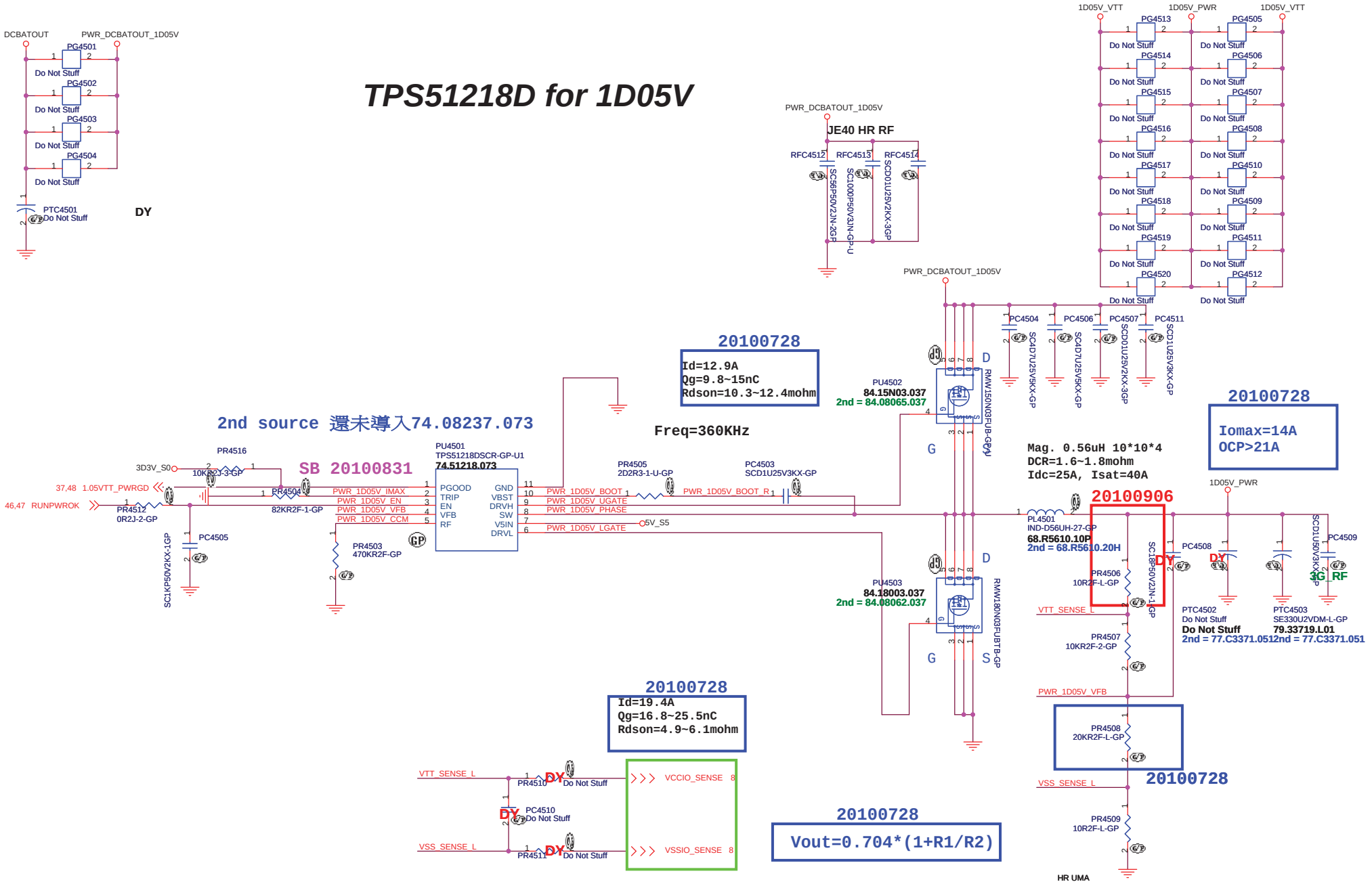
Date: Thursday, December 02, 2010 | Sheet 43 of 102




HR UMA

| | |
|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |
| Title | ***CPU Core-3(ISL95831)*** |
| Size A3 / Document Number | **JE40-HR** / Rev **-1** |
| Date: Thursday, December 02, 2010 | Sheet 44 of 102 |

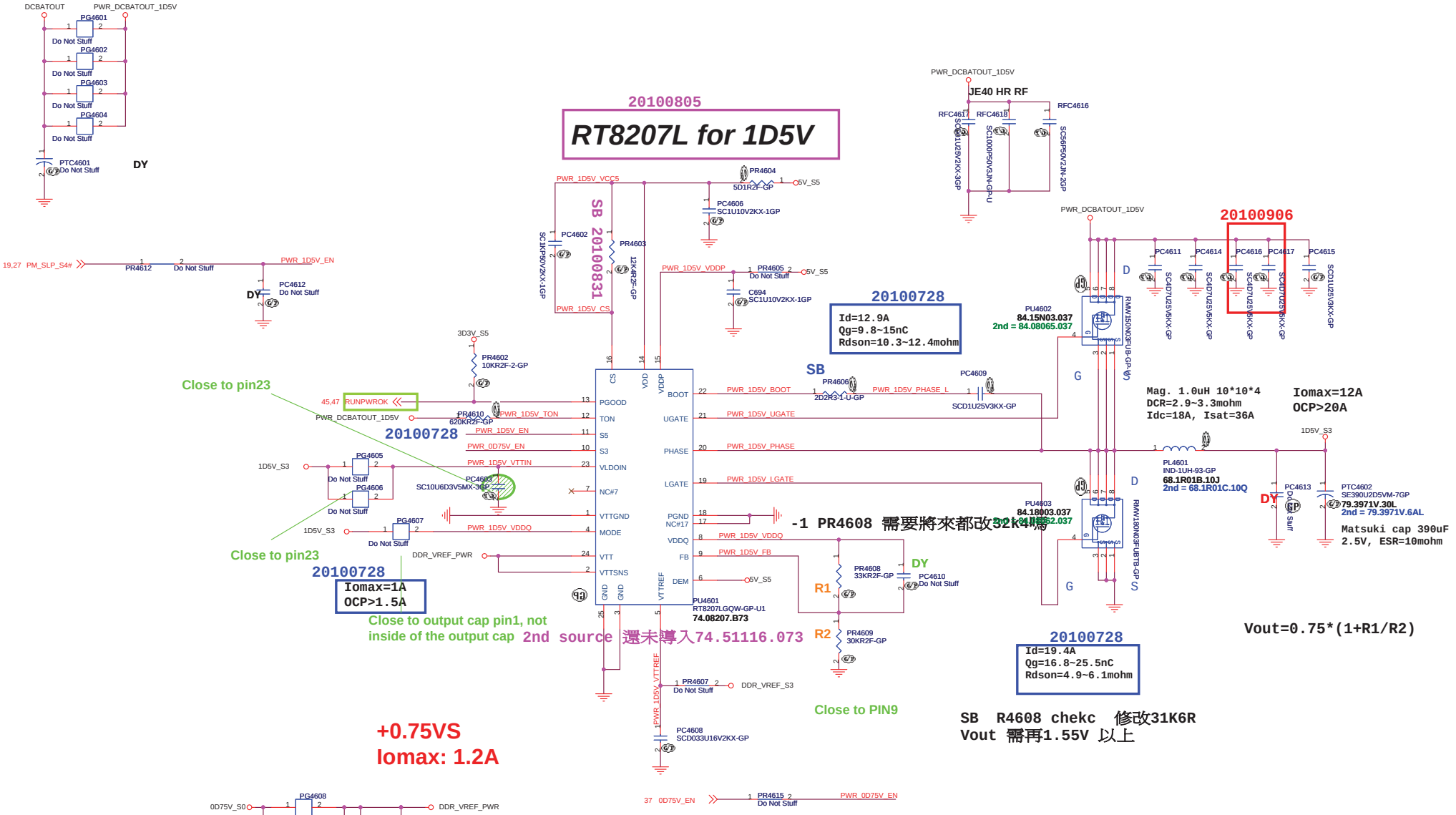
# TPS51218D for 1D05V




HR UMA

| | | |
|---|---|---|
| 緯創資通 | Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | DC to DC 1D05V(TPS51218D) | |
| Size A3 | Document Number JE40-HR | Rev -1 |
| Date: Thursday, December 02, 2010 | Sheet 45 of 102 | |

SSID = PWR.Plane.Regulator_1p5v0p75v



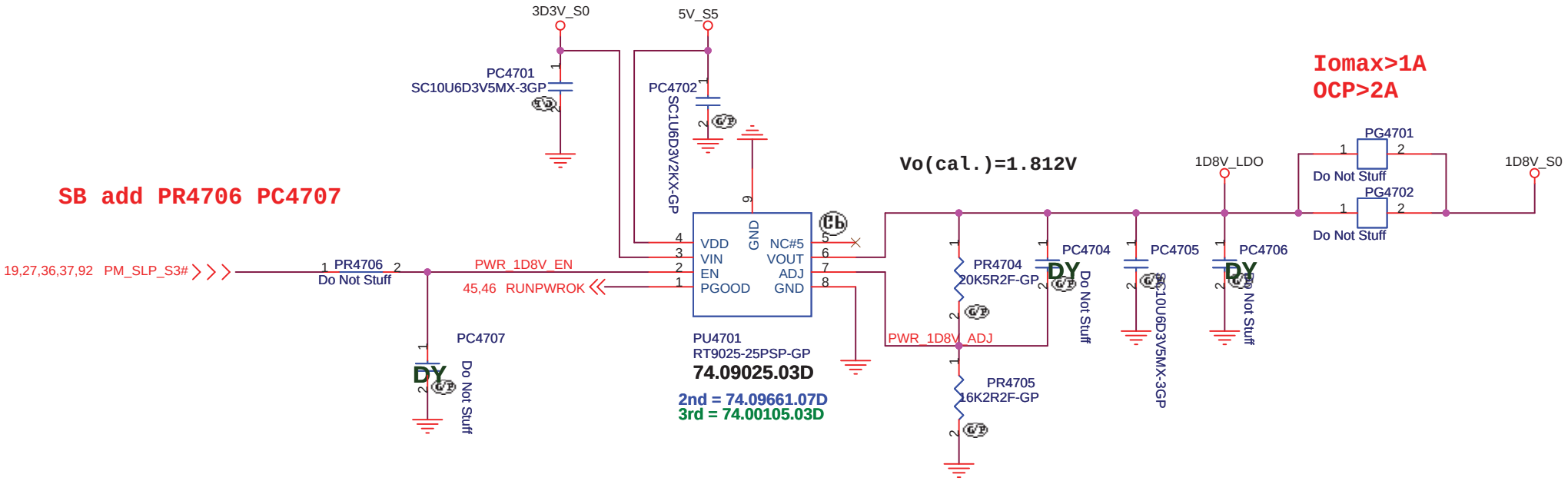



HR UMA

| | | |
|---|---|---|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: TPS5111 | | |
| Size: Custom | Document Number: JE40-HR | Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 46 of 102 | |

**SSID = PWR.Plane.Regulator_1p8v**

# RT9025 for 1D8V_S0




HR UMA

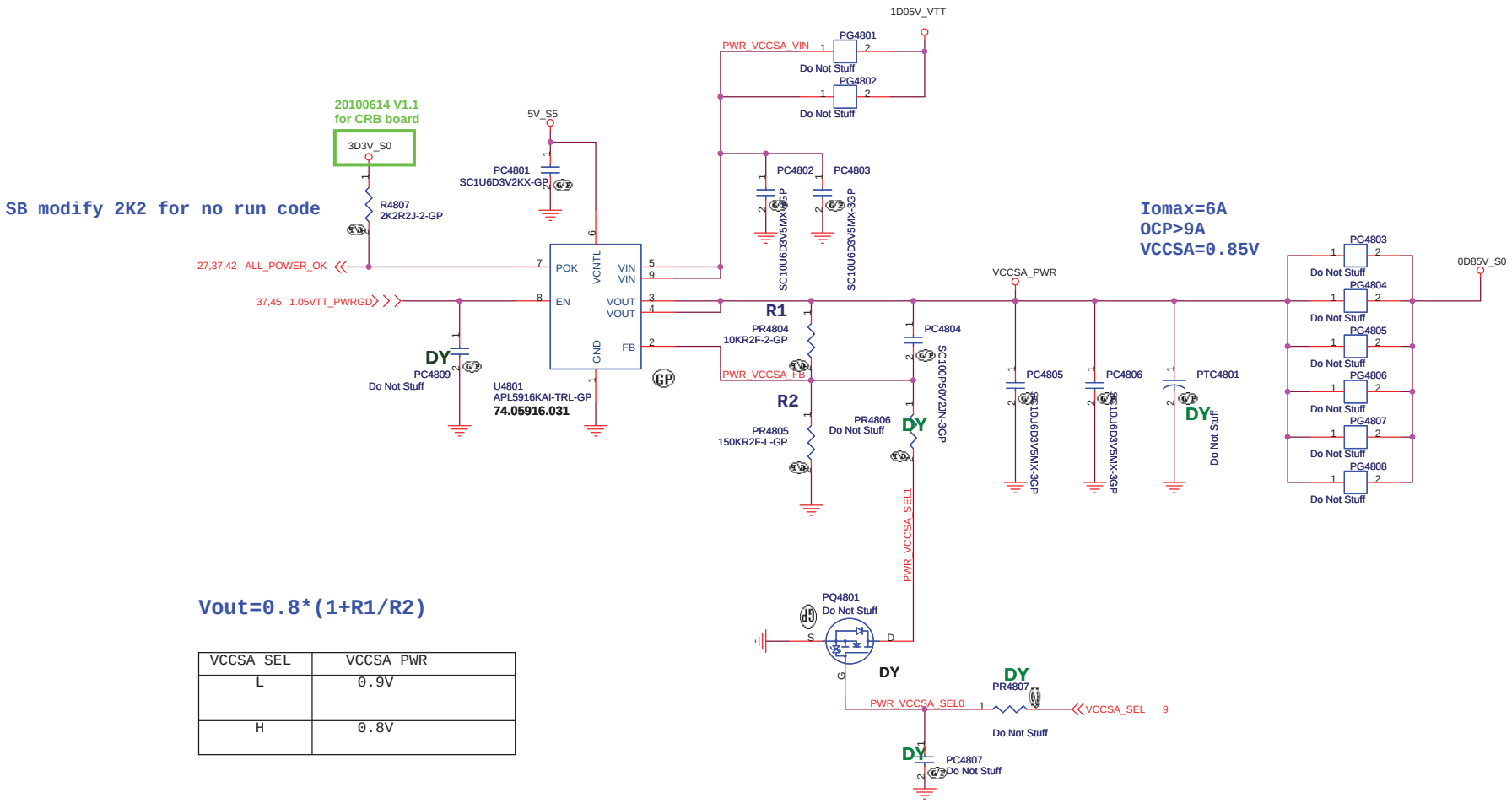
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LDO_1D8V(RT9025)***

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 47 of 102

# APL5916 for VCCSA




Vout=0.8*(1+R1/R2)

| VCCSA_SEL | VCCSA_PWR |
|---|---|
| L | 0.9V |
| H | 0.8V |



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

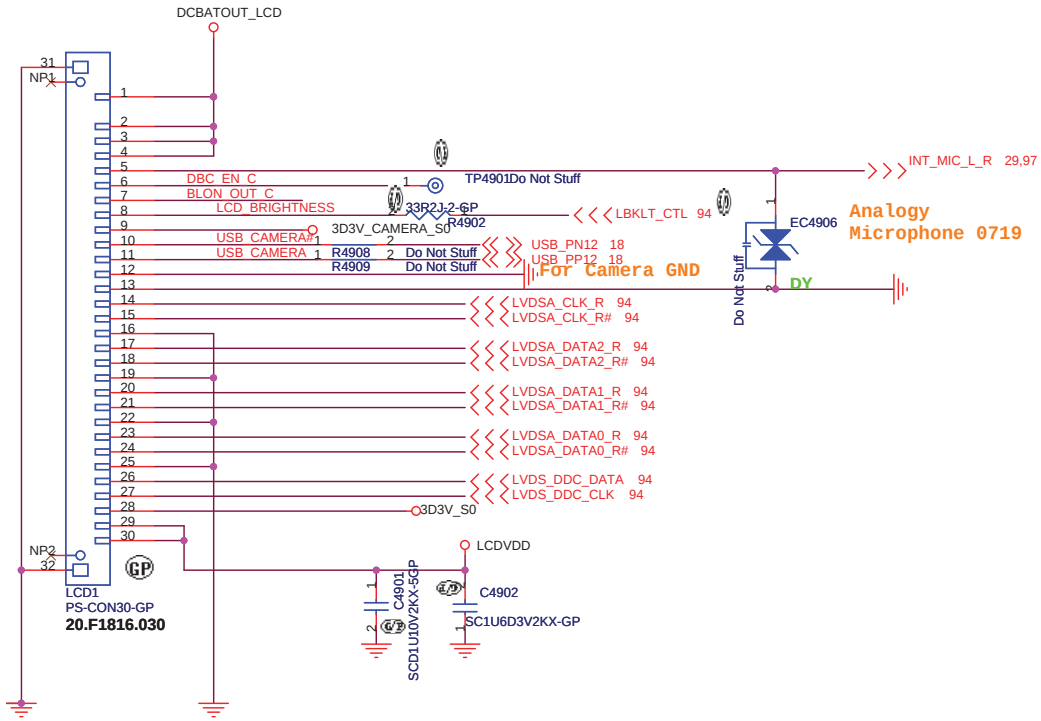
Title: LDO VCCSA(APL5916)

Size: A3 | Document Number: JE40-HR | Rev: -1

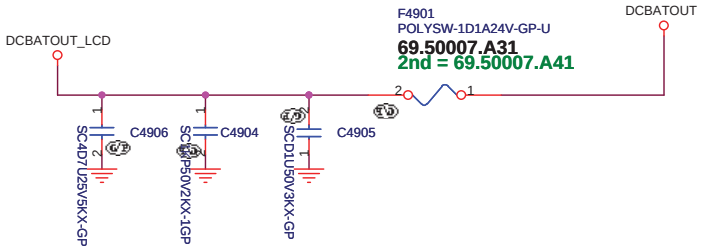
Date: Thursday, December 02, 2010 | Sheet 48 of 102

**SSID = VIDEO**

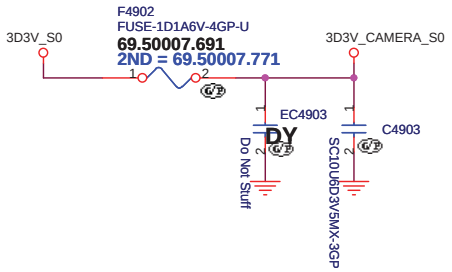
## LVDS CONNECTOR




## INVERTER POWER

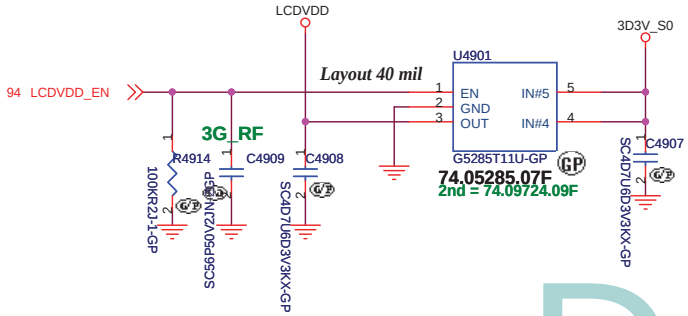


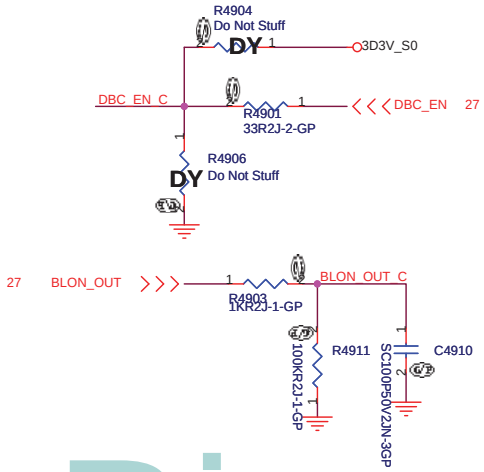

## Camera Power



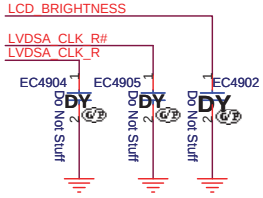

**SSID = VIDEO**

## LCD POWER for ANNIE




**For EMI request**
**Close to LVDS connector**




HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

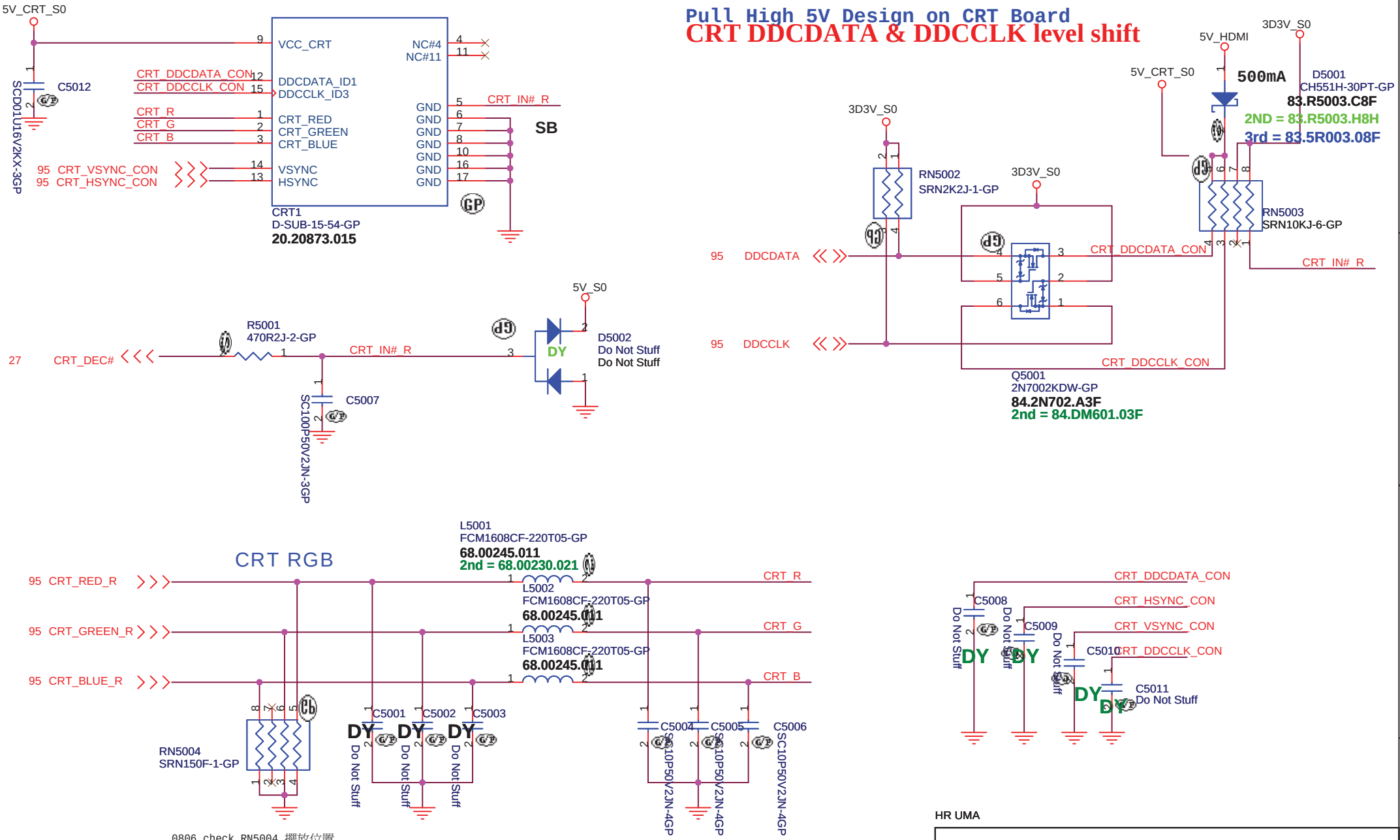
Title: LCD Connector

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 49 of 102

# Pull High 5V Design on CRT Board

# CRT DDCDATA & DDCCLK level shift




0806 check RN5004 擺放位置

HR UMA

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

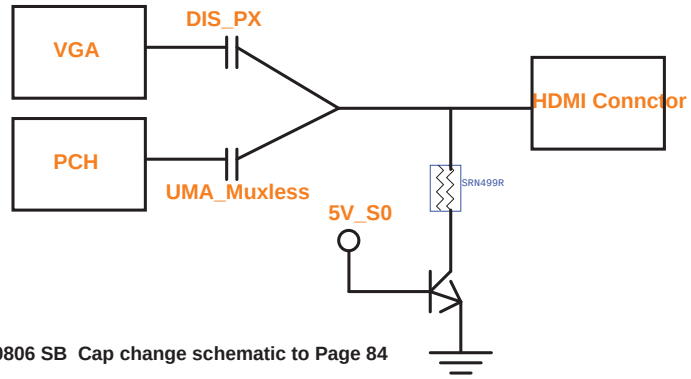
Date: Thursday, December 02, 2010 Sheet 50 of 102

SSID = VIDEO

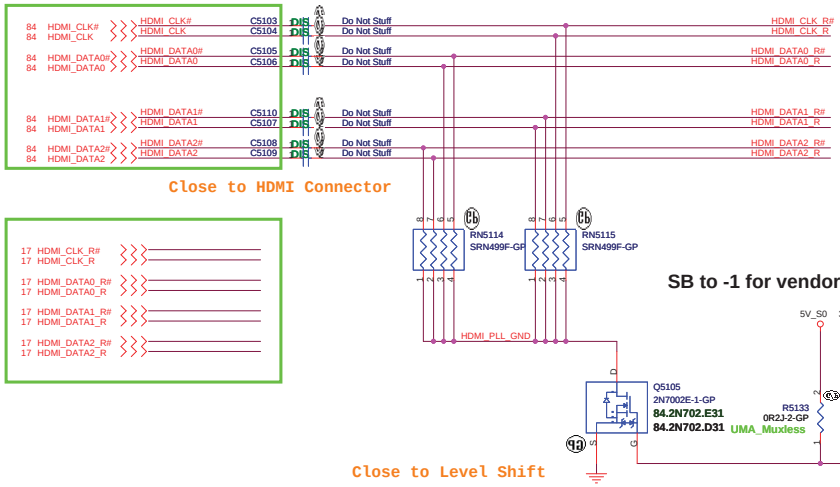
# HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

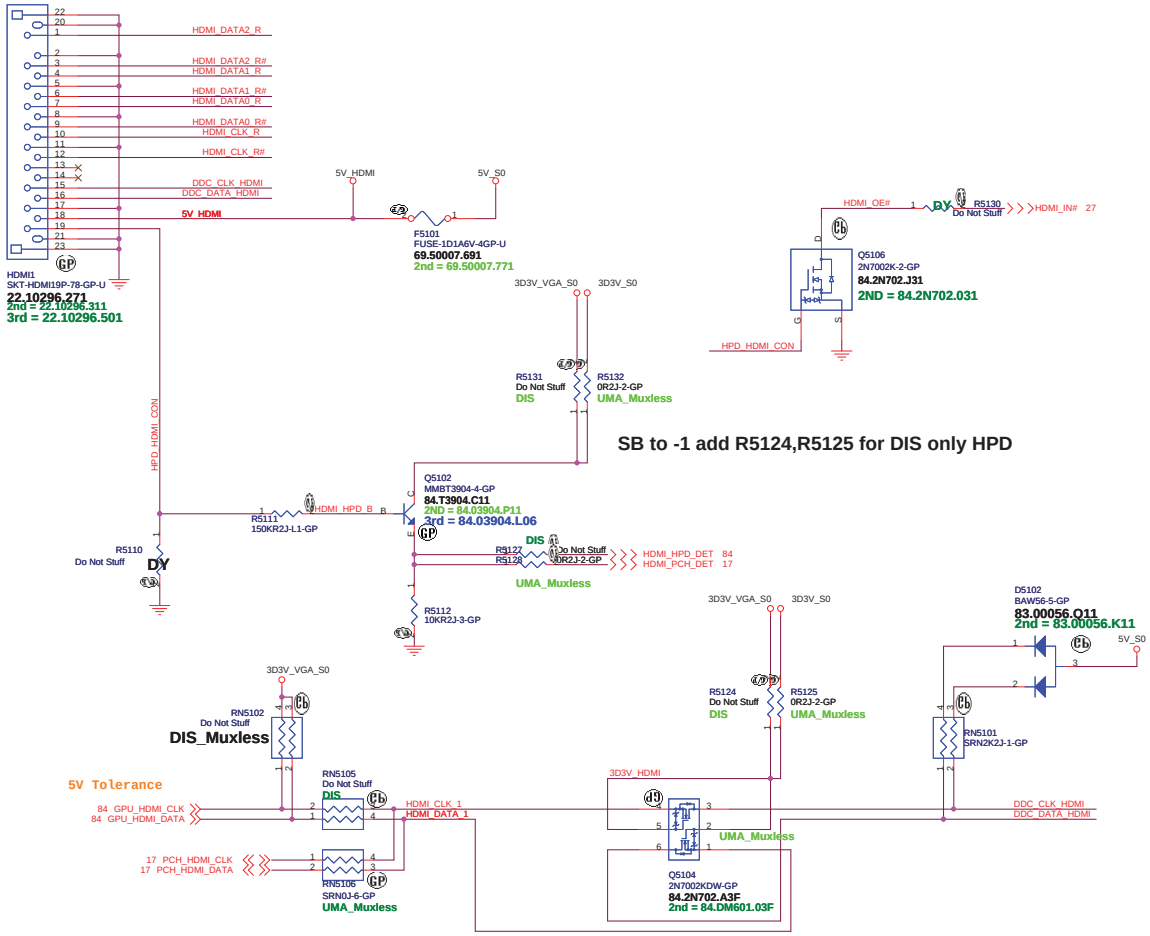
## HDMI DISCRETE/ UMA Co-lay




0806 SB Cap change schematic to Page 84




## HDMI CONN




HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

| Size | Document Number | Rev |
|---|---|---|
| Custom | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 51 of 102

# LED BACKLIGHT CONVERTER POWER

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***eDP***

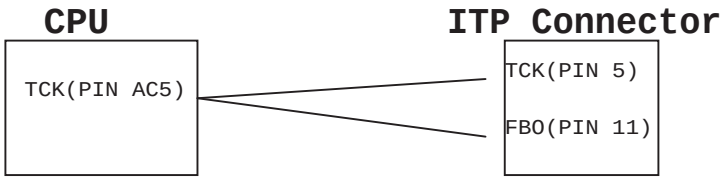
Size: A3 | Document Number: **JE40-HR** | Rev: **-1**

Date: Thursday, December 02, 2010 | Sheet 52 of 102

SSID = User.Interface

# ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil ( max ),
others place near CPU side.




HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

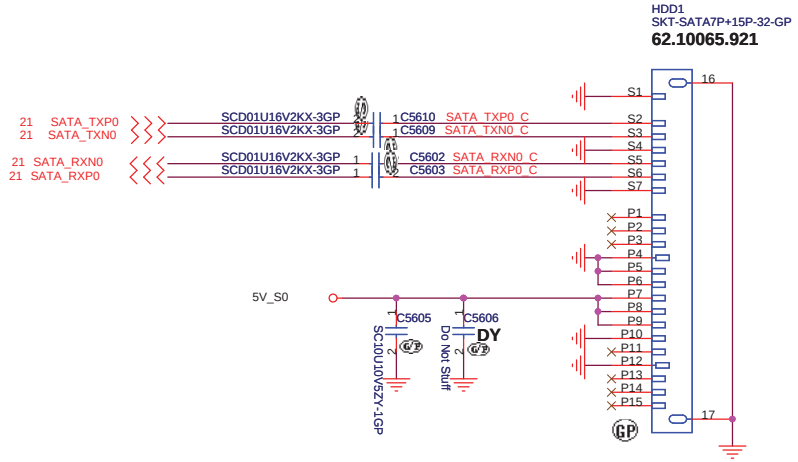
Title: ITP

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

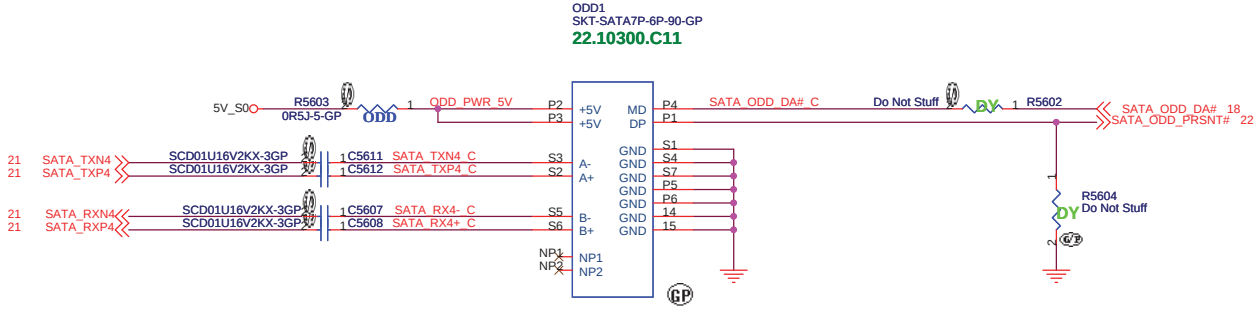
Date: Thursday, December 02, 2010 Sheet 55 of 102

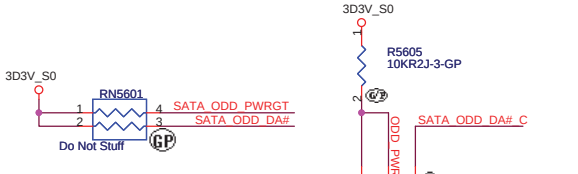
SSID = SATA

# SATA HDD Connector




# ODD Connector





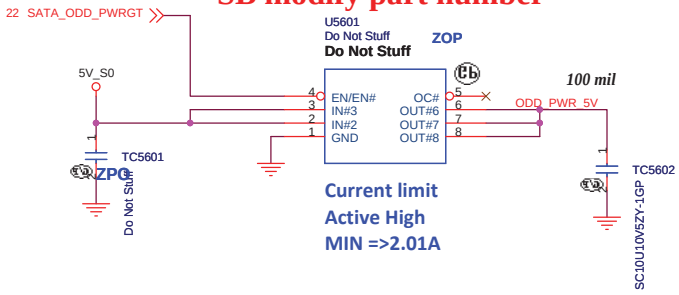


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

# SATA Zero Power ODD

## SB modify part number






HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 56 of 102

**ESATA Power**

# USB CHARGER

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***E-SATA/USB CHARGER***

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 57 of 102

SSID = AUDIO

Speaker Connector

LINE1 OUT
SPDIF

JE40 Modify LINE OUT

Audio at small board

MIC IN

Internal
Microphone

JE40 delete Line in function



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 58 of 102

*GIGA Lan Transformer*

**SSID = LOM**

LAN MDI Off-Page

XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

XF5902
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

## SB modiyf Pin9 Pin10 SWAP

LED COLOR
10(+) 9(-)::GREEN
12(+) 13(-):ORANGE

RJ45
RJ45-12P-16-GP
22.10321.Y21
2nd = 22.10321.Y91

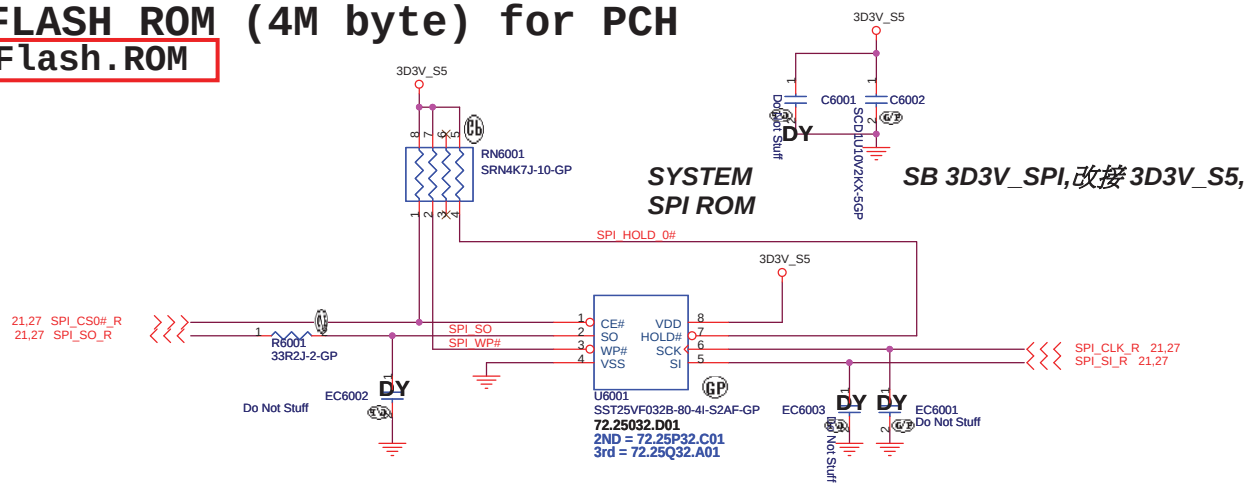
## SB modify For EMI



| | |
|---|---|
| HR UMA | |
| Wistron Corporation | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | LAN CONNECTOR |
| Size: Custom | Document Number: JE40-HR |
| Rev | -1 |
| Date: Thursday, December 02, 2010 | Sheet 59 of 102 |

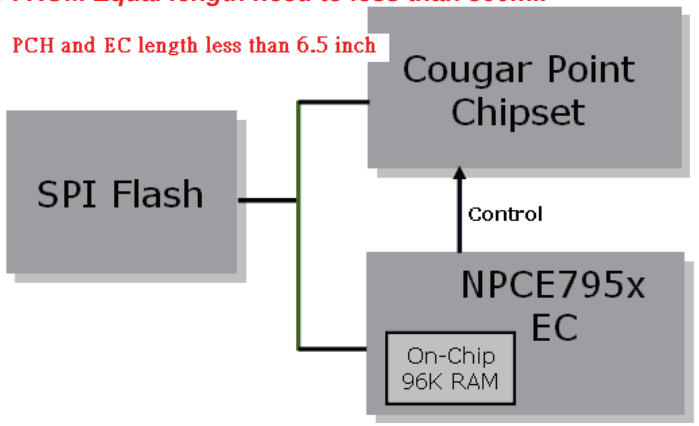
# SPI FLASH ROM (4M byte) for PCH

**SSID = Flash.ROM**

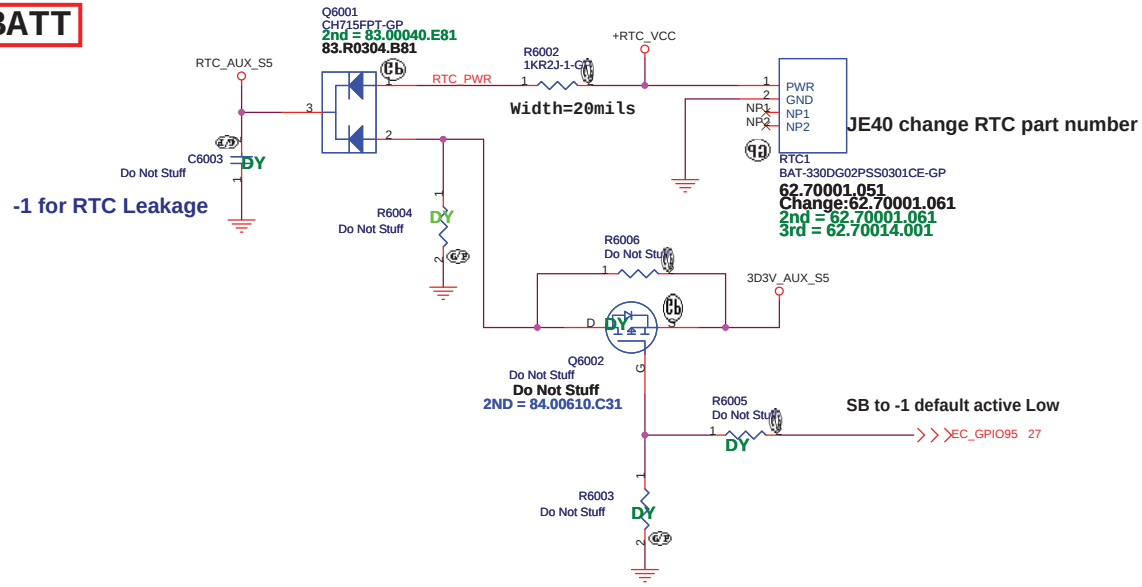



**SPI ROM Equal length need to less than 500mil**

PCH and EC length less than 6.5 inch




**SSID = RBATT**

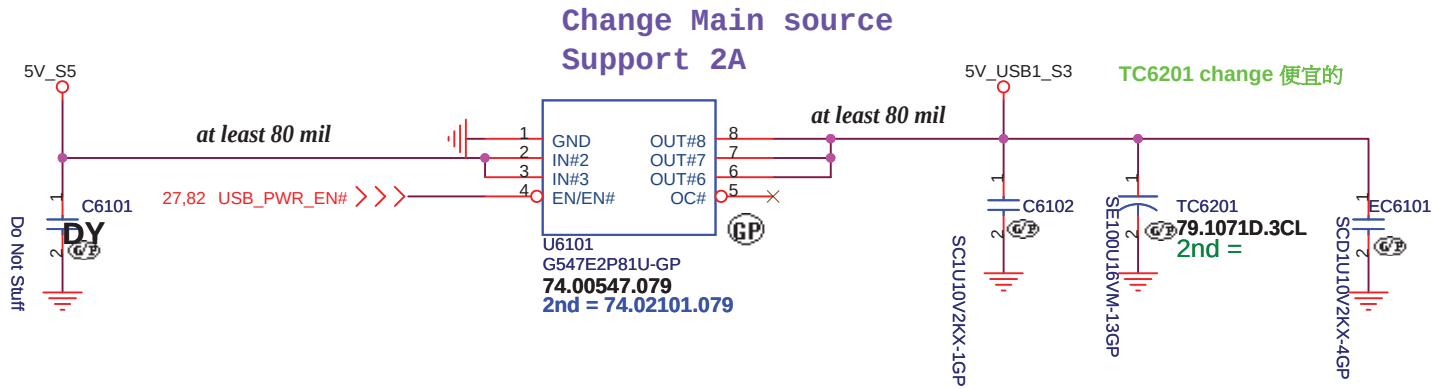


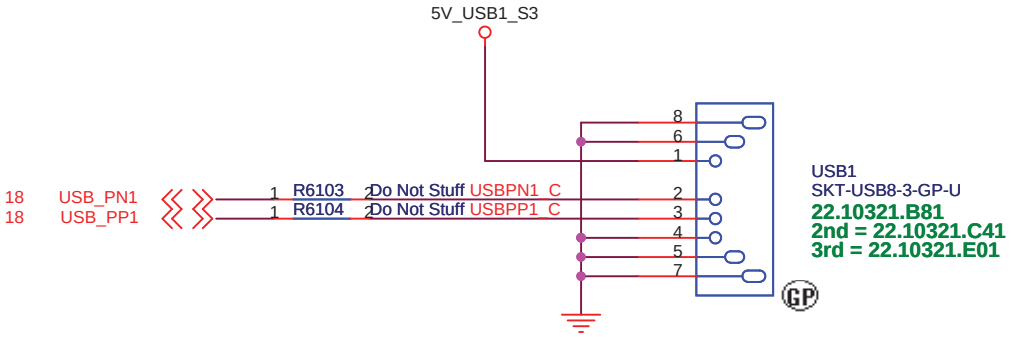

HR UMA

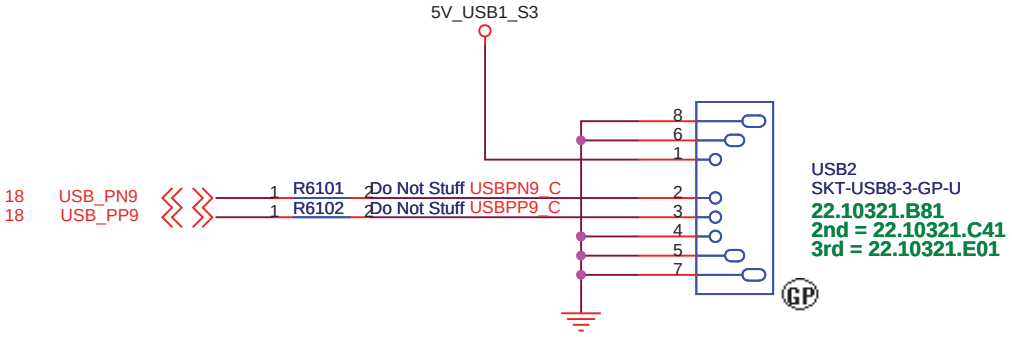
| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: *Flash/RTC* | | |
| Size: Custom | Document Number: JE40-HR | Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 60 of 102 | |

# SSID = USB

## IO Board USB Power




HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 61 of 102

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Port***

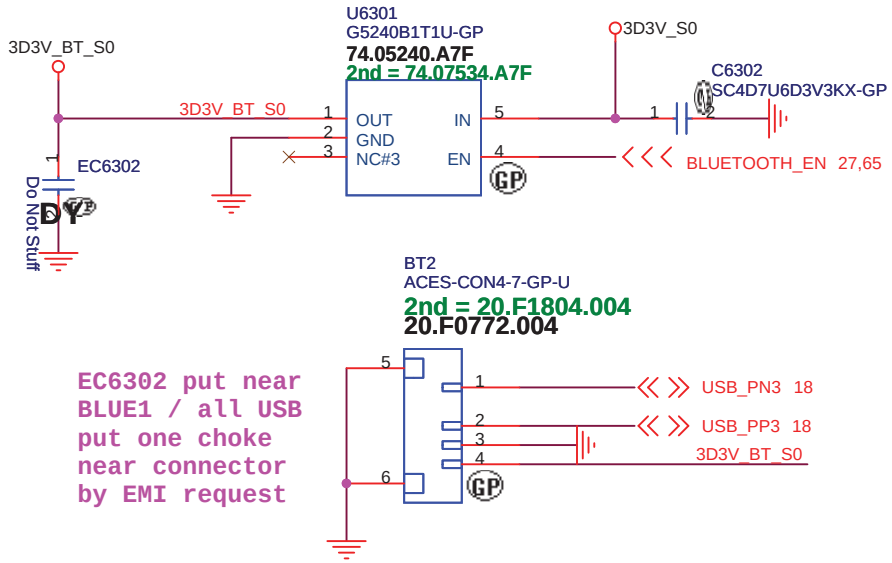
Size: A3 | Document Number: **JE40-HR** | Rev: **-1**

Date: Thursday, December 02, 2010 | Sheet 62 of 102

SSID = User.Interface

Bluetooth Module conn.

# *ANNIE Bluetooth Module*




EC6302 put near BLUE1 / all USB put one choke near connector by EMI request

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title: *Bluetooth* | | |
| Size: A4 | Document Number: JE40-HR | Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 63 of 102 | |

# Finger printer

## JE40 delete FP function


HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

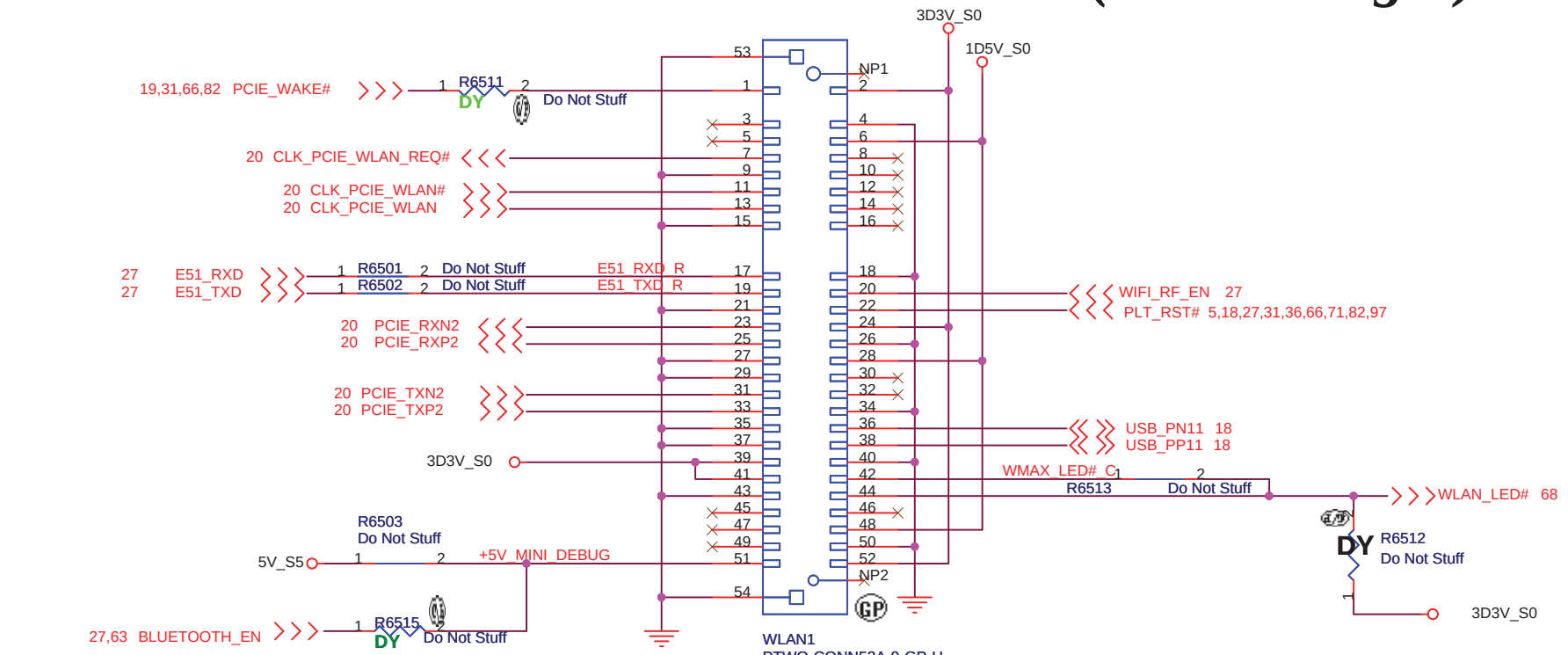
Title: ***RESERVED***

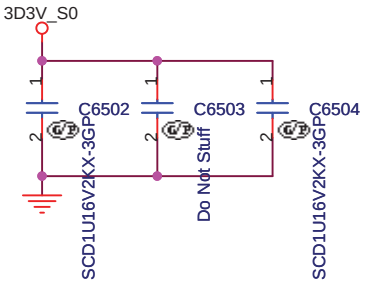
| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 64 of 102

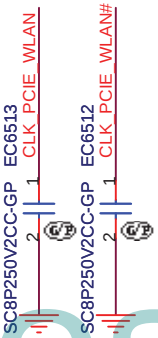
**SSID = Wireless**

# Mini Card Connector(802.11a/b/g/n)

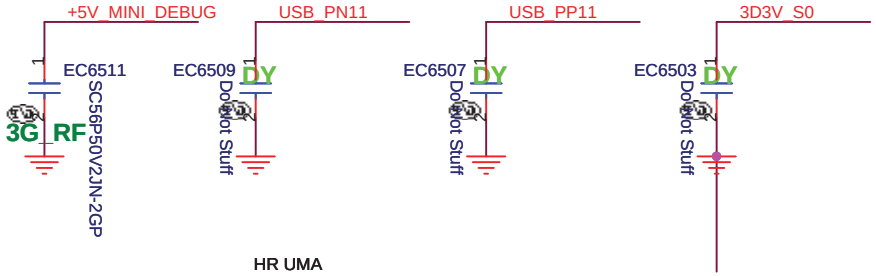


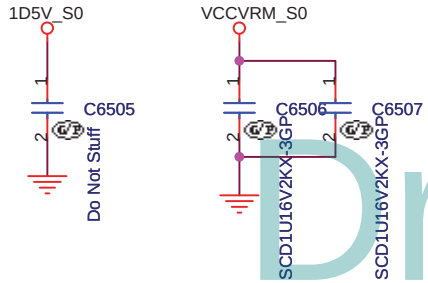

## SB modify for SIV




## RF suggestion




-2




HR UMA



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

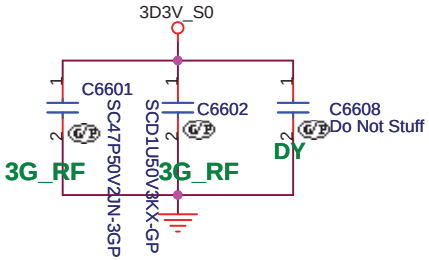
Date: Thursday, December 02, 2010 Sheet 65 of 102

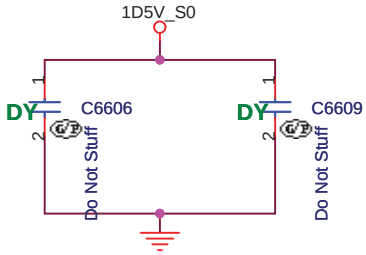
**SSID = Wireless**

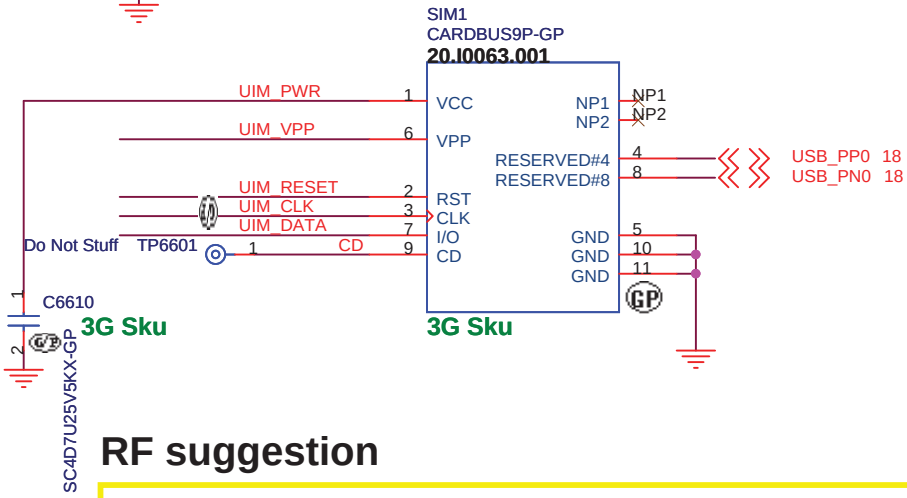
# Mini Card Connector(WWAN)

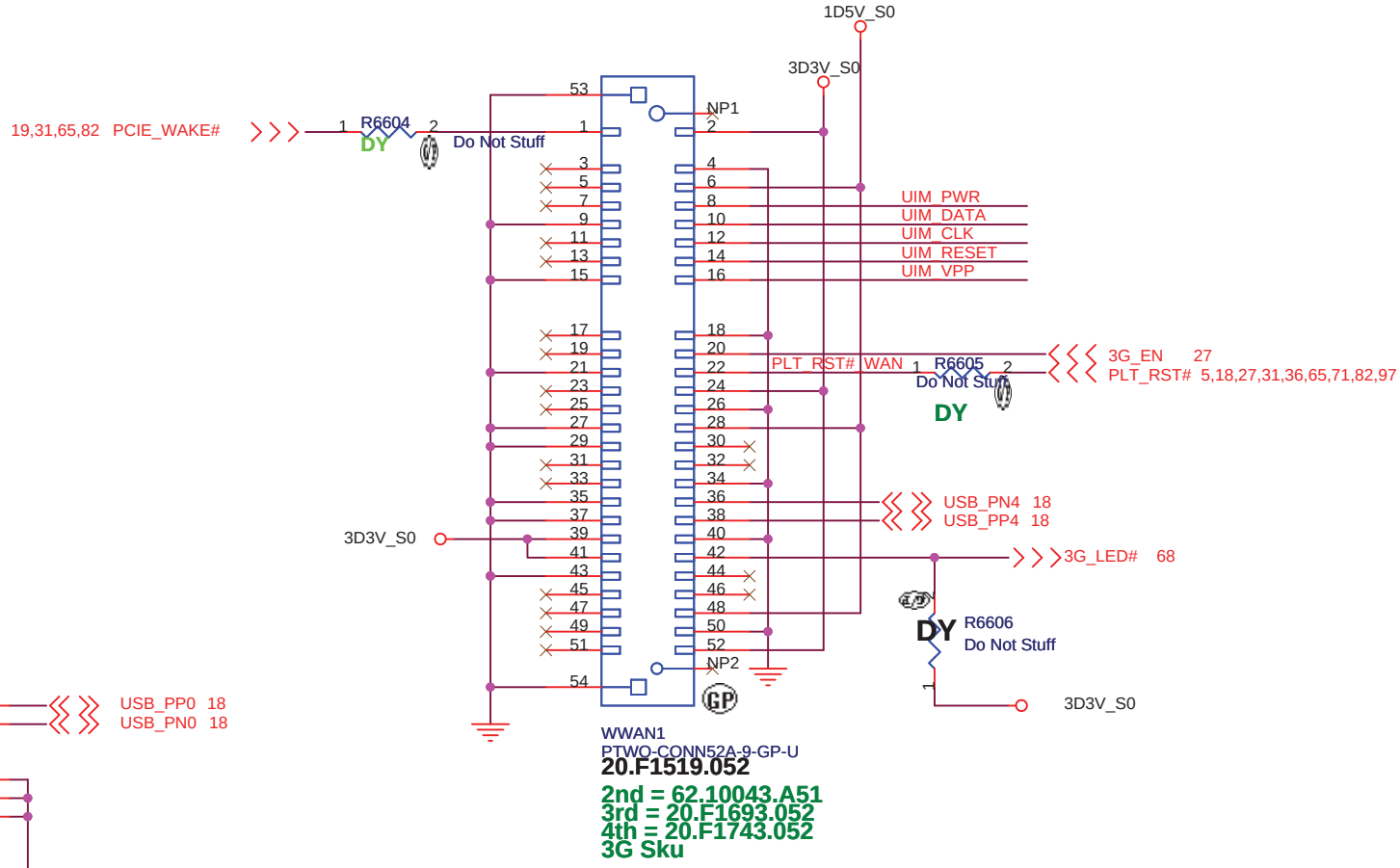
20100712 V1.5

**Place near MINI Card CONN**

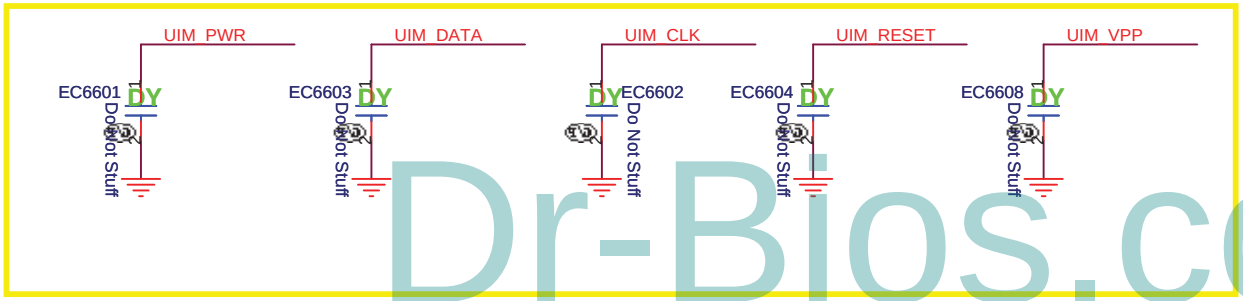



## RF suggestion






HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **WWAN Connector**

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 66 of 102

# (Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

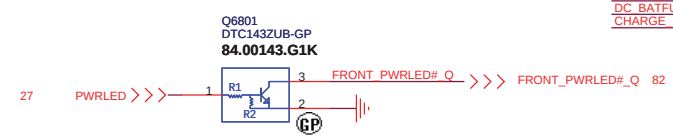
Title: ***Reserved***

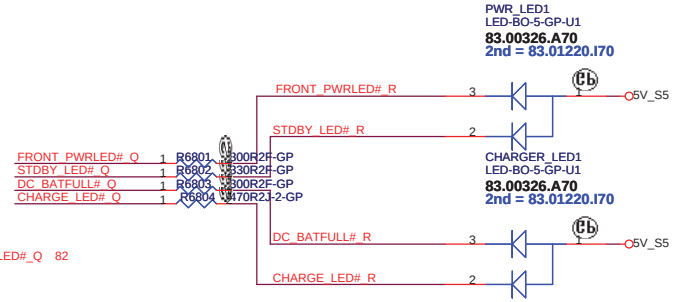
| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 67 of 102

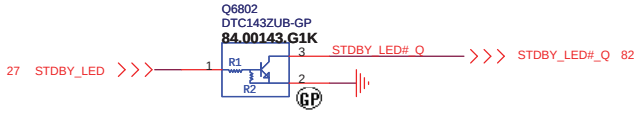
SSID = User.Interface

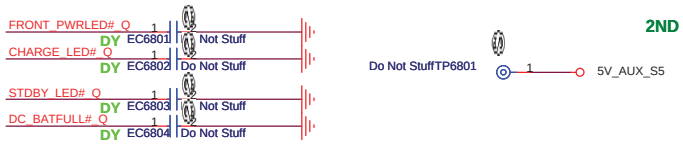
## Power button LED



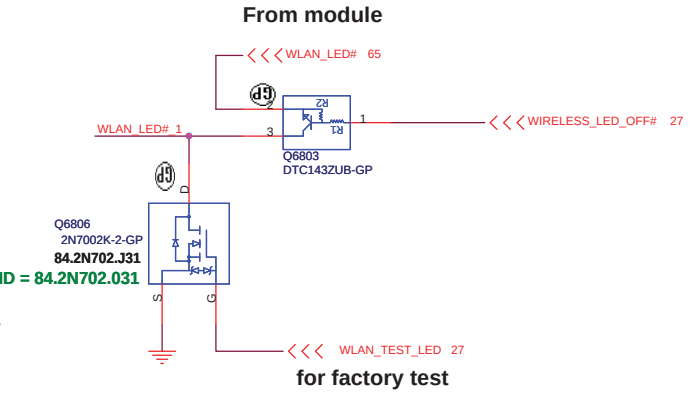




## Power STDBY_LED

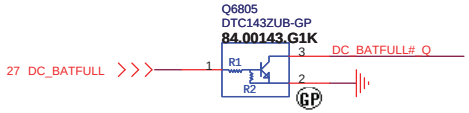


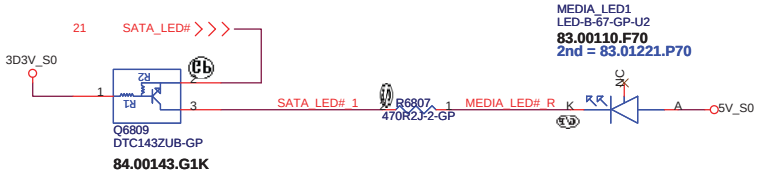

## WLAN_LED



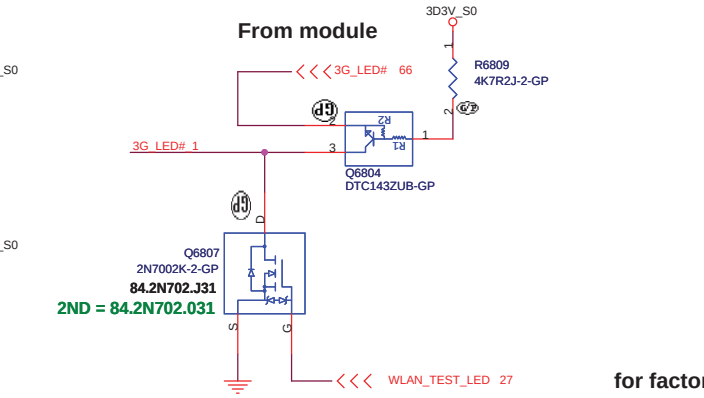

## Battery LED2(DC_BATFULL)



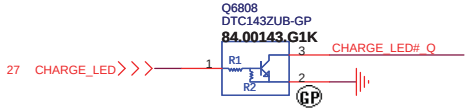

## SATA HDD LED

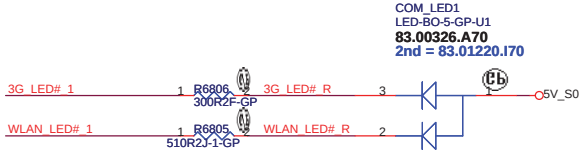



## 3G LED




## Battery LED1(CHARGE)




HR UMA

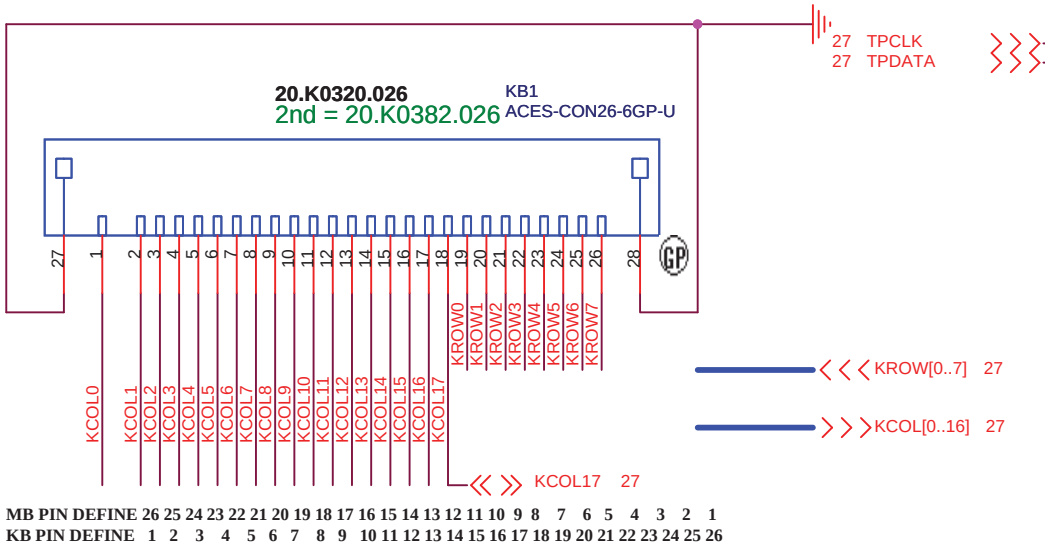
| | | |
|---|---|---|
| 緯創資通 | Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: LED Bard/Power Button | | |
| Size: Custom | Document Number: JE40-HR | Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 68 of 102 | |

**SSID = KBC**

# TOUCH PAD

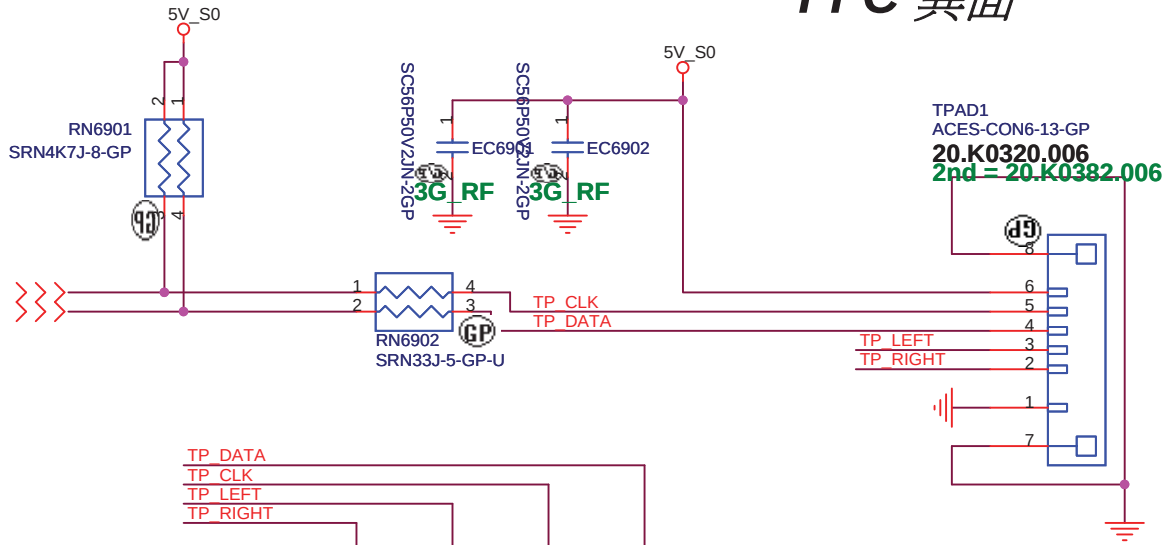
**FFC 異面**

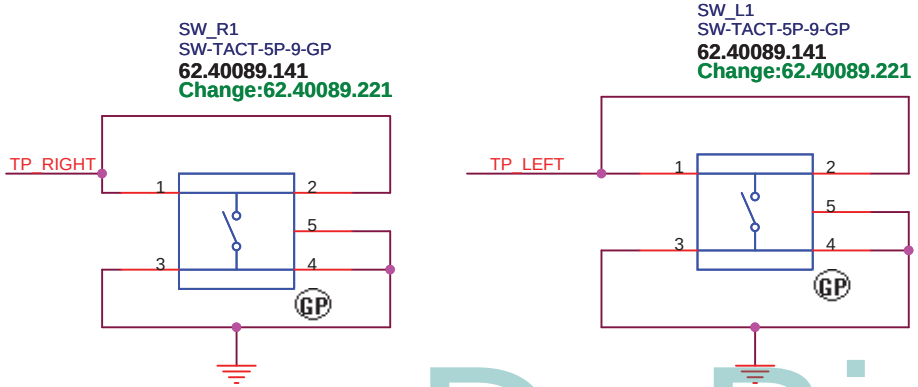
## Internal KeyBoard Connector




MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1 **SB to -1 modify Part number**



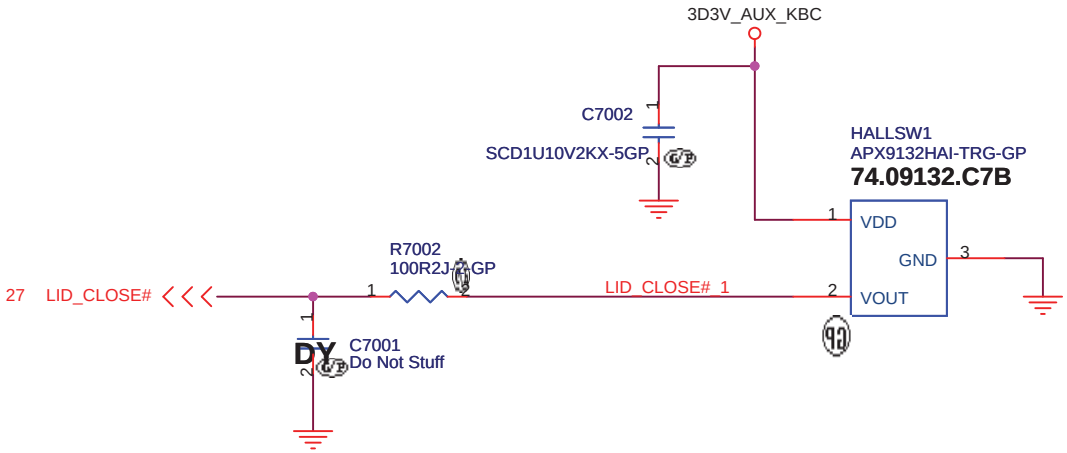

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 69 of 102



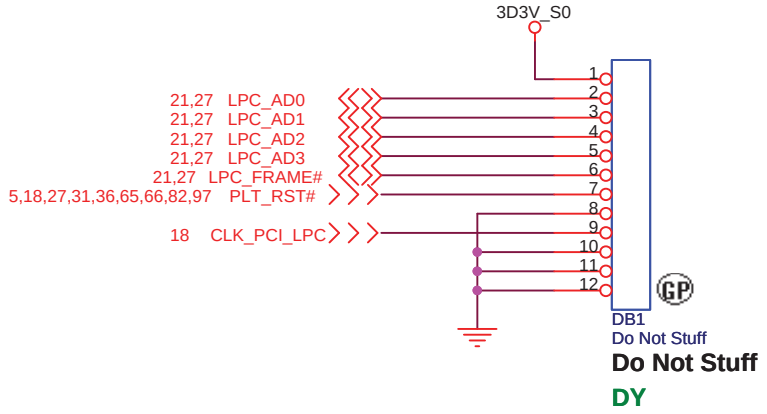

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 70 of 102




HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

| Size | Document Number | Rev |
|---|---|---|
| A4 | **JE40-HR** | **-1** |

Date: Thursday, December 02, 2010 Sheet 71 of 102

(Blanking)



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

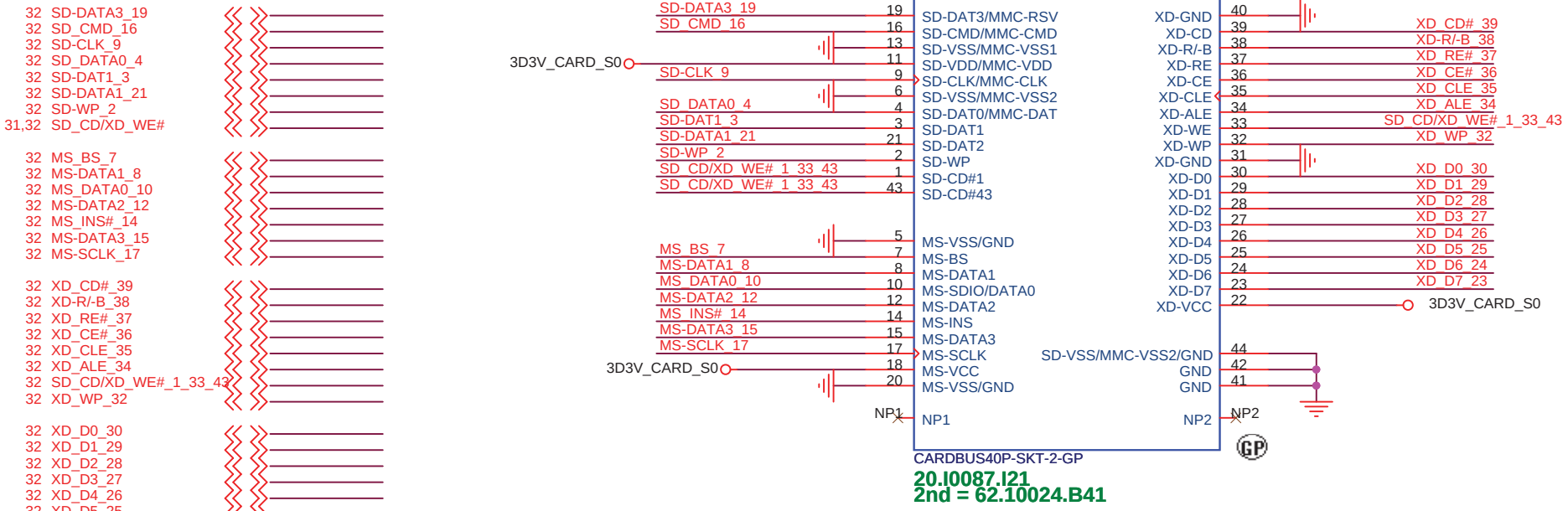
Title: *Reserved*

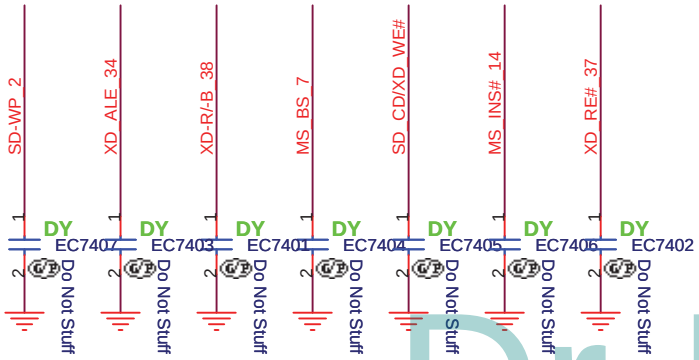
| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 72 of 102

# SD/XD/MS Card Reader

**SSID = SDIO**




HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 74 of 102

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 75 of 102

**SSID = User.Interface**

# Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

**JE40 delete G Sensor Function**

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title: *Free Fall Sensor* | | |
| Size: A4 | Document Number: JE40-HR | Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 79 of 102 | |

# (Blanking)

HR UMA

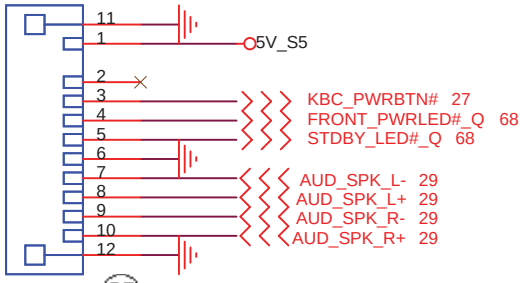
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Reserved***

| Size | Document Number | Rev |
|---|---|---|
| A4 | JE40-HR | -1 |

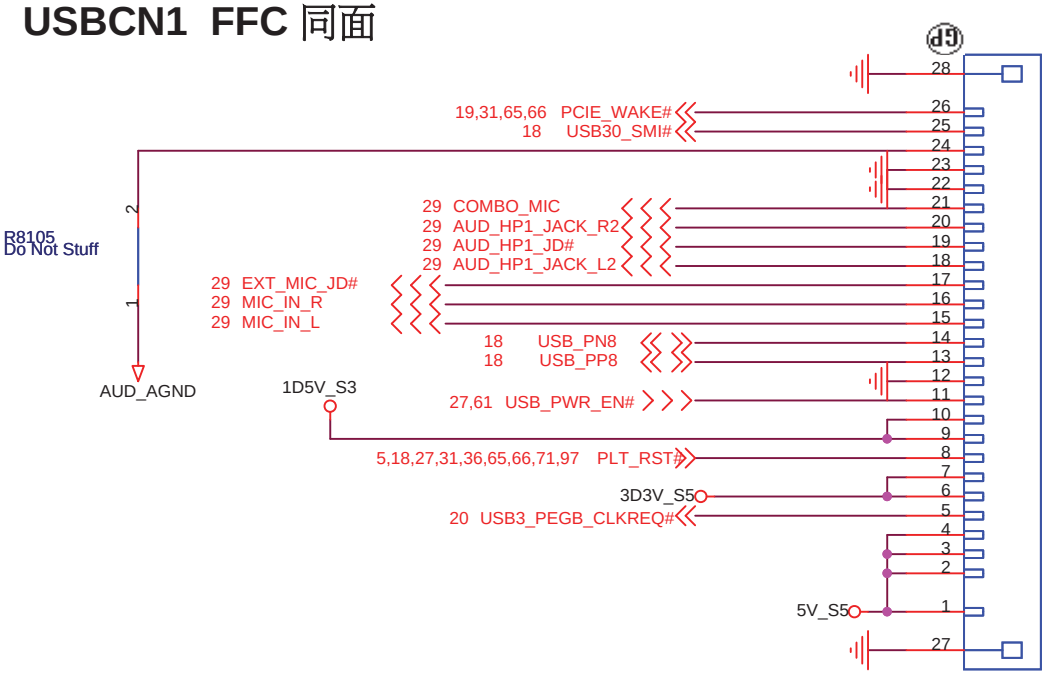
Date: Thursday, December 02, 2010 Sheet 80 of 102

## PWRCN1 FFC 異面




PWRCN1
ACES-CON10-20-GP
**20.K0422.010**
**2nd = 20.K0382.010**

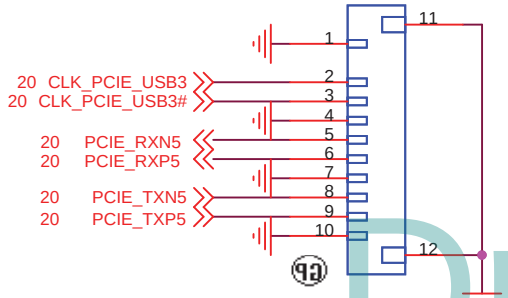
## USBCN1 FFC 同面




USBCN1
ACES-CON26-11-GP
**20.K0315.026**
**2nd = 20.K0370.026**

## 0806 change 10Pin

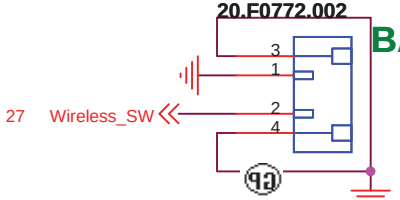
USBCN2
ACES-CON10-18-GP
**20.K0315.010**
**2nd = 20.K0392.010**




## USBCN2 FFC 同面

**-1 add RF connector**
**BAE40 Only**

RF_CN1
ACES-CON2-11-GP
**20.F0772.002**
**BAE40**

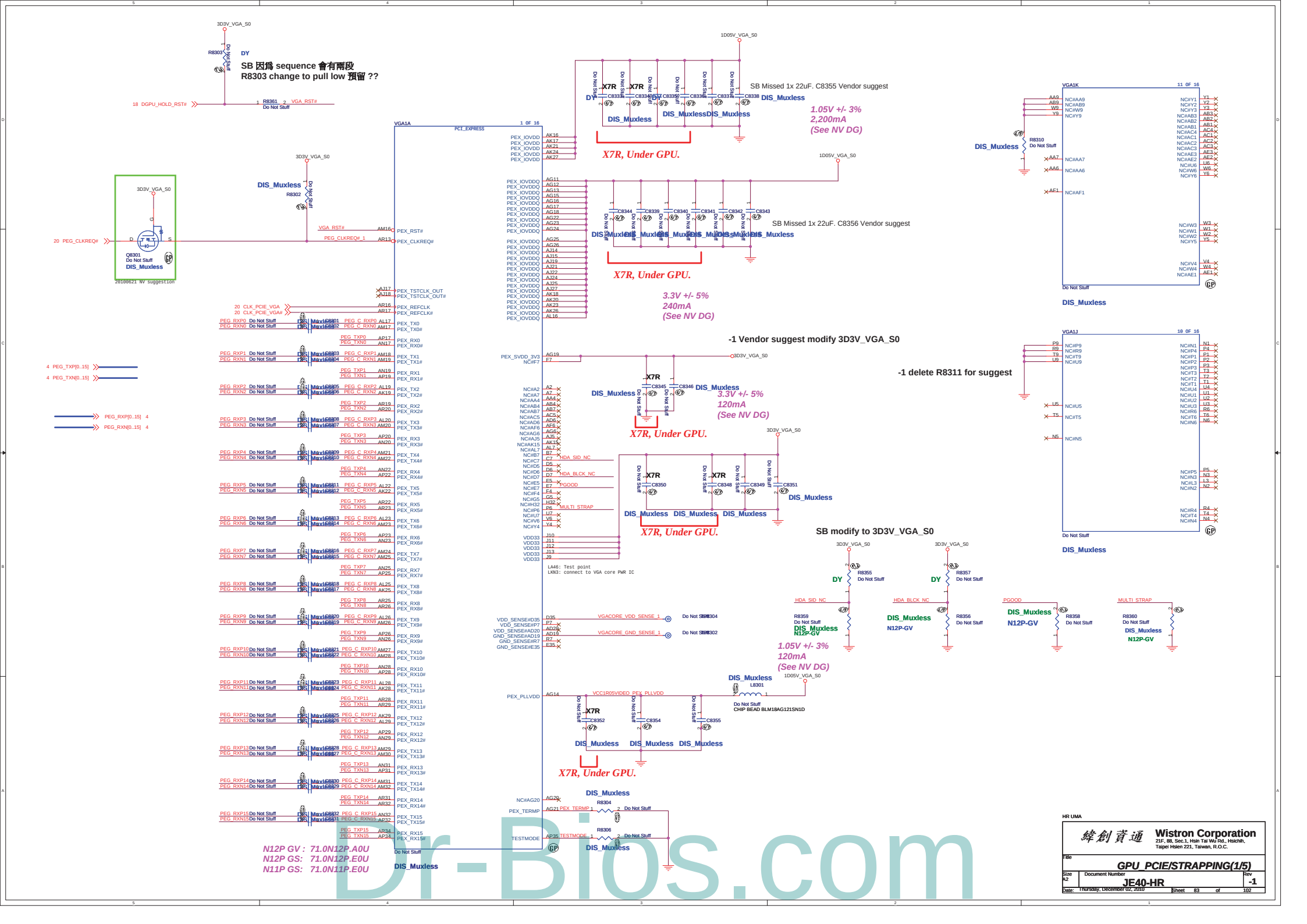



## Cabele Wire to BD

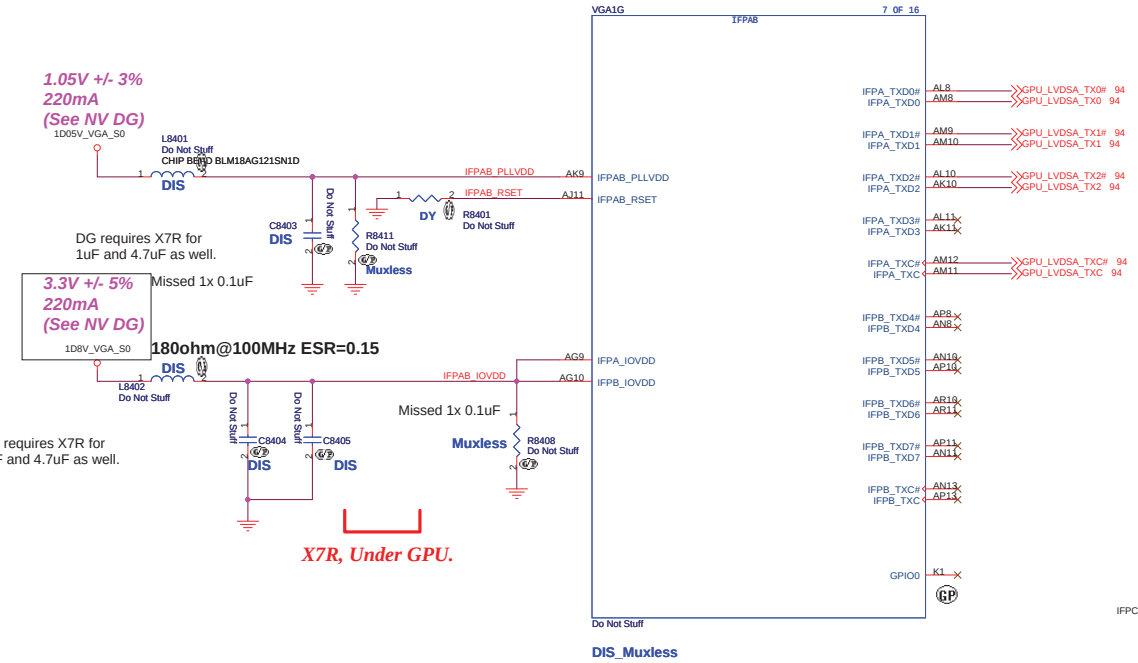
HR UMA

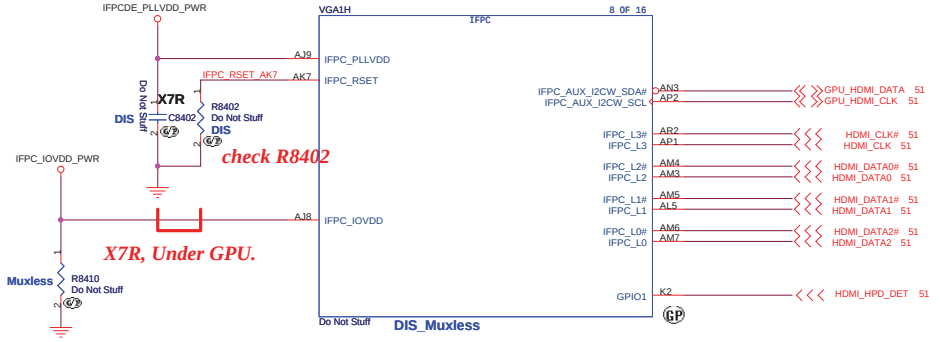


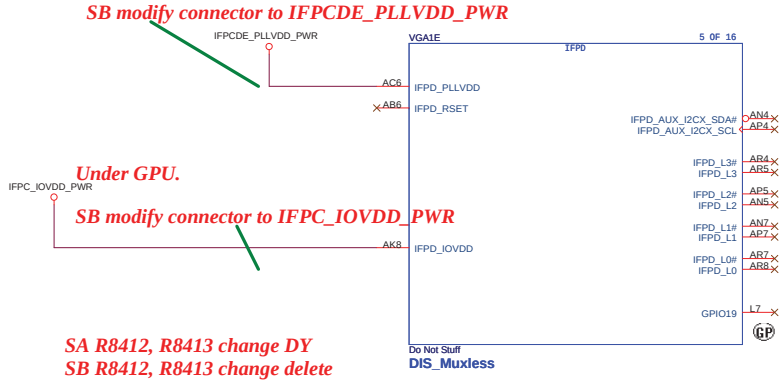
| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: ***IO Board Connector*** | | |
| Size: A4 | Document Number: **JE40-HR** | Rev: **-1** |
| Date: Thursday, December 02, 2010 | Sheet 82 of 102 | |

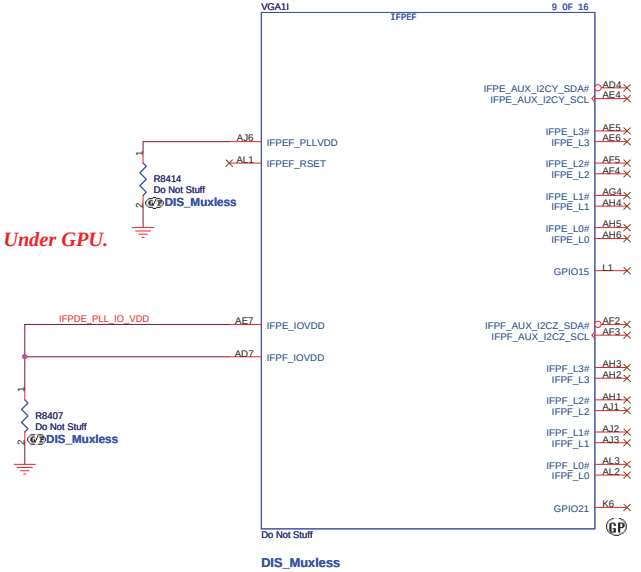

SB 因爲 sequence 會有兩段
R8303 change to pull low 預留 ??
SB Missed 1x 22uF. C8355 Vendor suggest
1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
SB Missed 1x 22uF. C8356 Vendor suggest
3.3V +/- 5%
240mA
(See NV DG)
-1 Vendor suggest modify 3D3V_VGA_S0
3.3V +/- 5%
120mA
(See NV DG)
-1 delete R8311 for suggest
SB modify to 3D3V_VGA_S0
1.05V +/- 3%
120mA
(See NV DG)
N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
N11P GS: 71.0N11P.E0U
Wistron Corporation
GPU_PCIE/STRAPPING(1/5)
JE40-HR
-1
Thursday, December 02, 2010
Sheet 83 of 102

# LVDS Interface

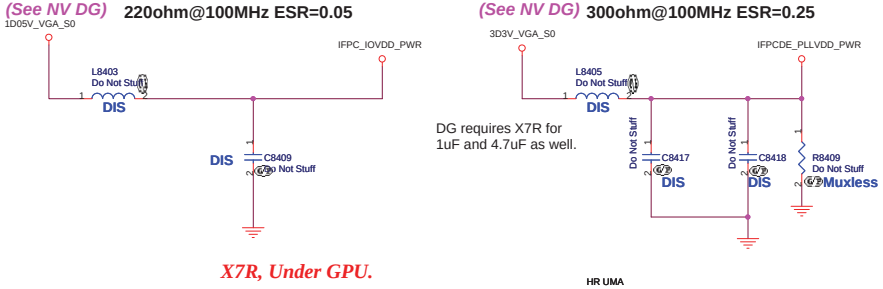



# HDMI Interface




HR UMA

| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: GPU Memory(2/5) | | |
| Size: Custom | Document Number: JE40-HR | Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 84 of 102 | |

# EDP 10A

*DC tolerance +/- 75mV*
*AC tolerance +/- 50mV < 100MHz*

*X7R, Under GPU.*

*X7R, Near GPU.*

*1.05V +/- 3%*
*200mA*
*(See NV DG)*

*X7R, Under GPU.*

*FBCLK Termination place on VRAM side*

*FBCLK Termination place on VRAM side*

Group A

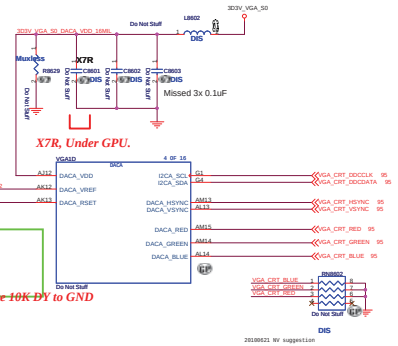
Group B

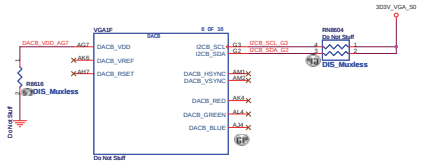


| | |
|---|---|
| Wistron Corporation | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | GPU_DP/LVDS/CRT/GPIO(3/5) |
| Size / Document Number | JE40-HR |
| Rev | -1 |
| Date: Thursday, December 02, 2010 | Sheet 85 of 102 |

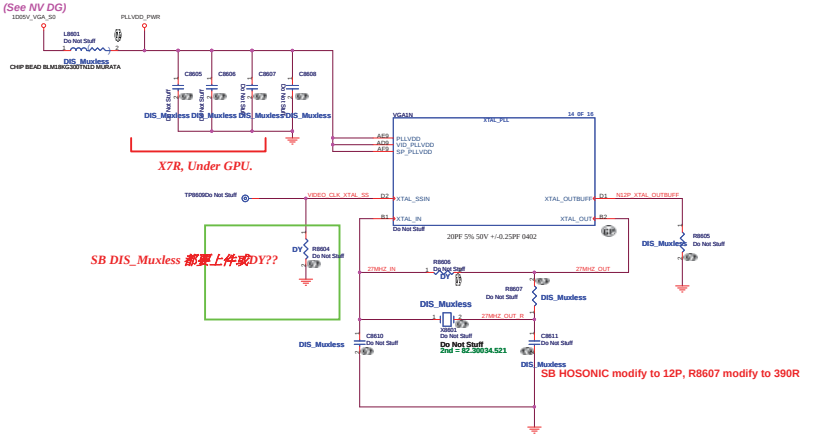
300ohm@100MHz ESR=0.25ohm

3.3V +/- 5%
120mA
(See NV DG)

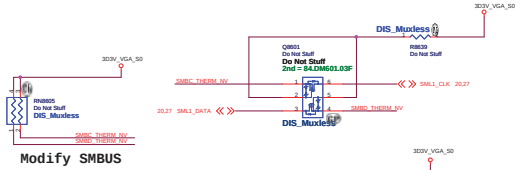


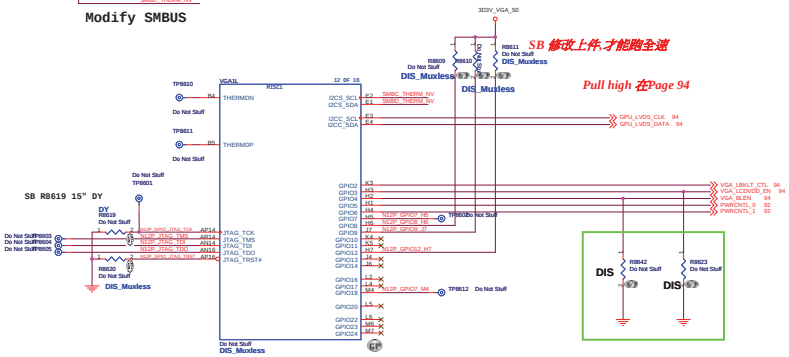




1.05V +/- 3%
150mA
(See NV DG)



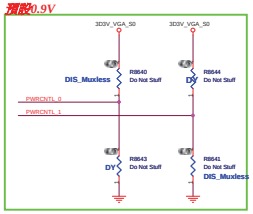

## VGA Thermal sensor P2800




| SJM50-CP SUPPORT | | | | | | | |
|---|---|---|---|---|---|---|---|
| P-STATE | NVVDD_ALTV1 | NVVDD_ALTV0 | N11M-GE1 | N11M-GE2 | N11M-OP1 | N11P-GE1 | N11P-GE Fermi |
| P12 | 0 | 0 | 0.85V | 0.85V | 0.85V | 0.80V | 0.85V |
| P8 | 0 | 1 | 0.85V | 0.85V | 0.85V | 0.85V | 0.9V |
| P0 | 1 | 0 | 1.02V | 1.02V | 1.02V | 0.95V | 0.95V |

預設0.9V




## NVIDIA TABLE

| | Hynix 2G<br>0110<br>128*16*8<br>800MHZ | Hynix 1G<br>0000<br>64*16*8<br>800MHZ | Samsung 1G<br>0011<br>64*16*8<br>800MHZ | Samsung 512<br>64*16*4<br>800MHZ | Samsung 2G<br>0111<br>128*16*8<br>800MHZ |
|---|---|---|---|---|---|
| RO M_SIPD R8627 | 34.8Kohm<br>64.34825.6DL | 5Kohm<br>64.49915.6DL | 20Kohm<br>64.20025.6DL | 20Kohm<br>64.20025.6DL | 45Kohm<br>64.45325.6DL |

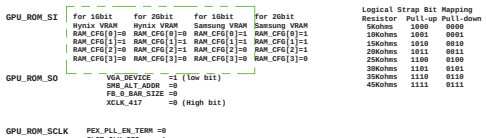
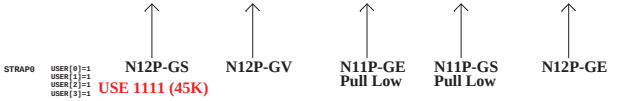


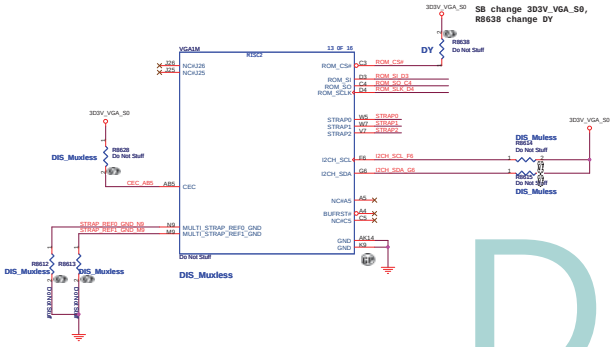


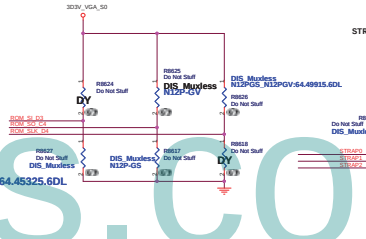
TABLE NVIDIA 71.0N12P.E0U

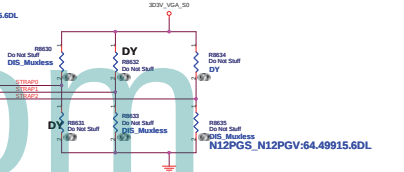
-1 modify N12P GV setting 71.0N12P.A0U

| | N12P-GS<br>DEV ID:<br>0x0DF4 | N12P-GV<br>DEV ID:<br>0x1050 | N11P-GE Fermi<br>DEV ID:<br>0x0DF1<br>(0001) | N11P-GS Fermi<br>DEV ID:<br>0x0DF0<br>(0000) | N12P-GE<br>DEV ID:<br>0x0DF5<br>(0101) |
|---|---|---|---|---|---|
| STRAP2 PU | 25Kohm<br>64.24925.6DL | 45Kohm<br>ES 45K QS 5K<br>64.49915.6DL | 10Kohm<br>63.10334.1DL | 5Kohm<br>64.49915.6DL | 30Kohm<br>64.30025.6DL |



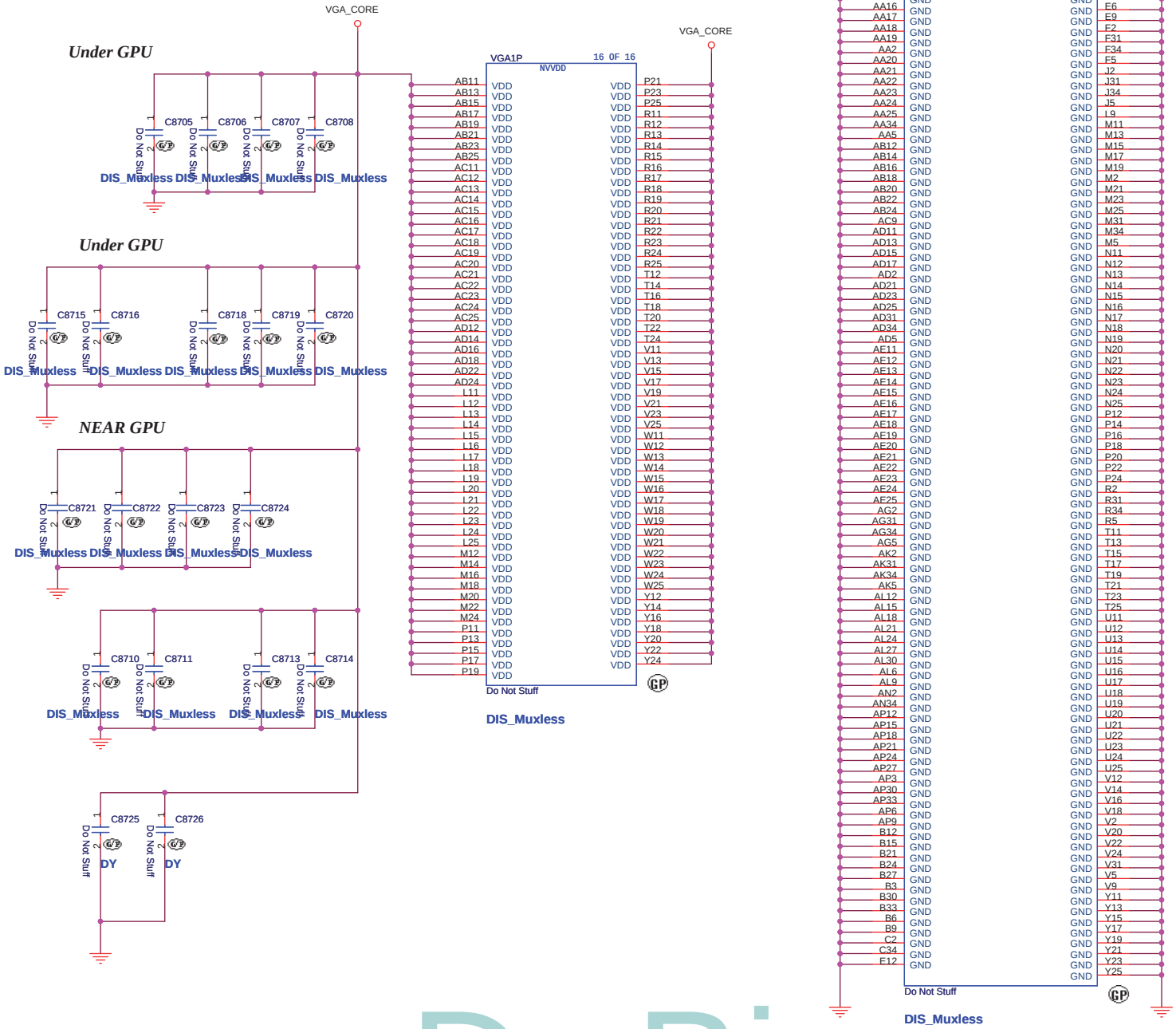




Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL,Sam2G_64.45325.6DL



| | | |
|---|---|---|
| 華創資通 | Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | GPU_POWER(4/5) | |
| Size<br>A1 | Document Number<br>JE40-HR | Rev<br>-1 |
| Date: Thursday, December 09, 2010 | Sheet 85 of 102 | |

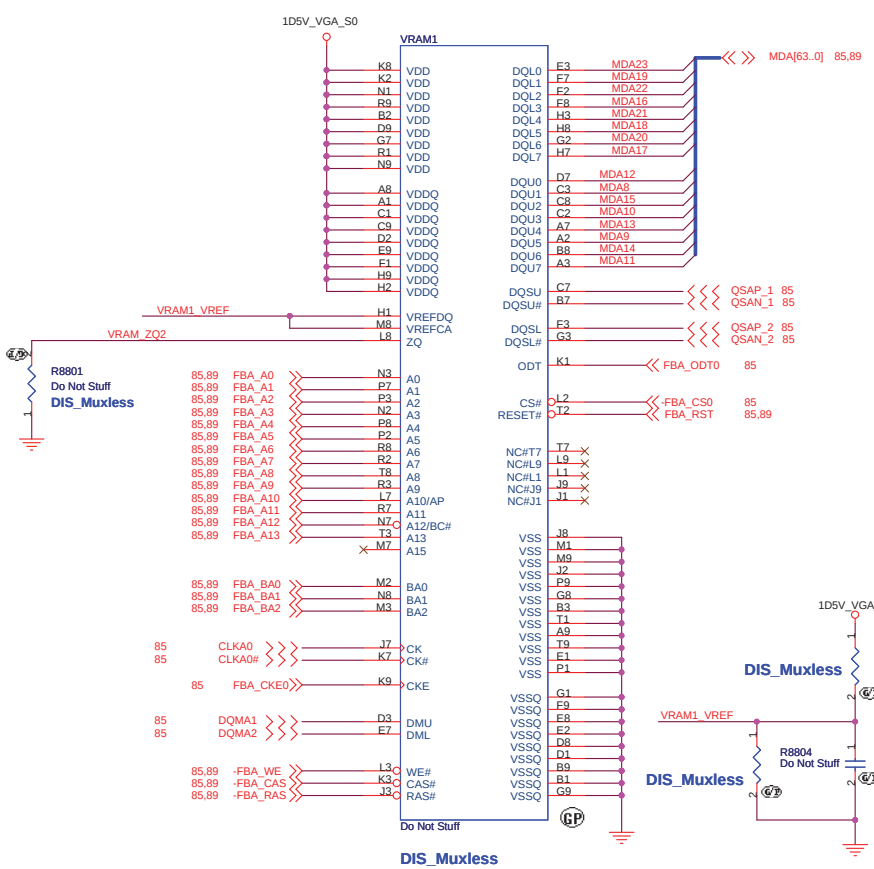
# EDP 50A
# (TDP 37W)



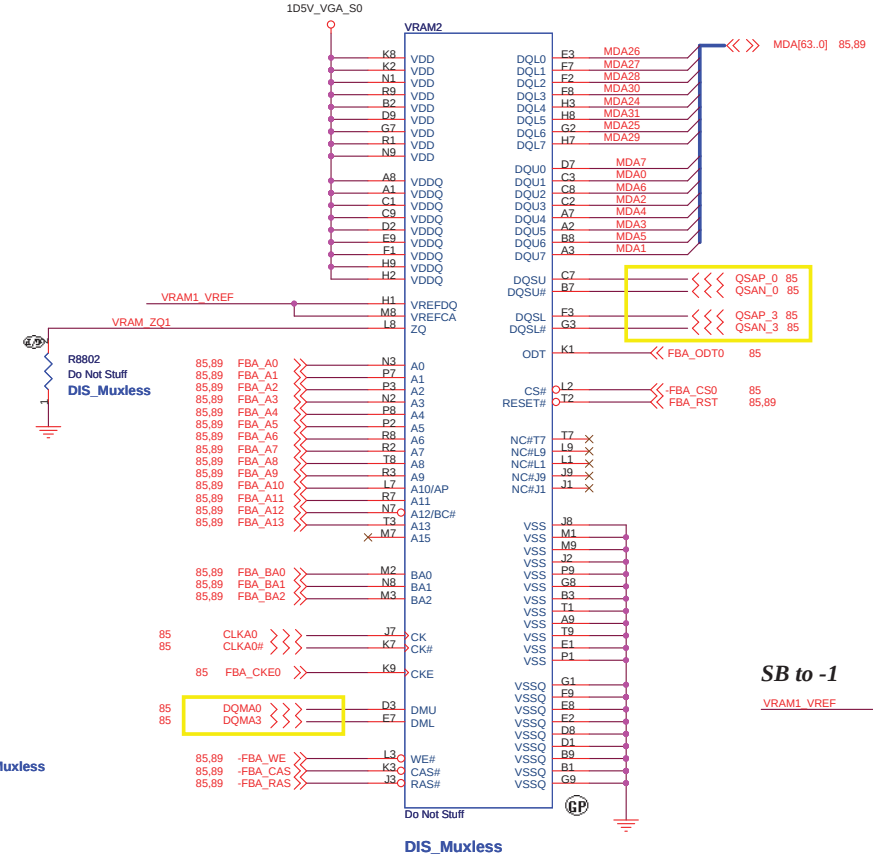



HR UMA

| | |
|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. |
| Title | **GPU_DPPWR/GND(5/5)** |
| Size A3 | Document Number **JE40-HR** Rev **-1** |
| Date: Thursday, December 02, 2010 | Sheet 87 of 102 |




VRAM = N12PGS_N12PGV

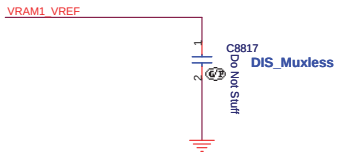



DIS_Muxless

VRAM = N12PGS_N12PGV

*FB CMD mapping Mode D-N12x*

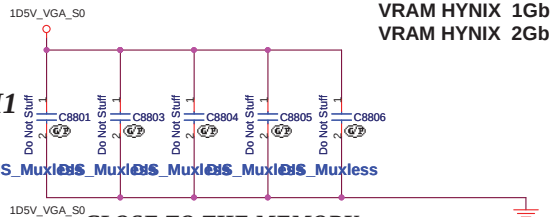
*SB to -1*




VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

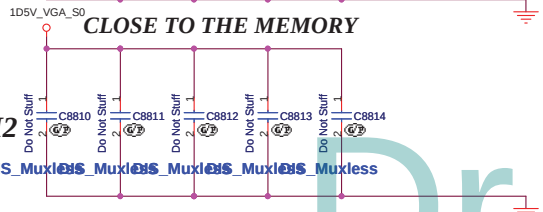
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

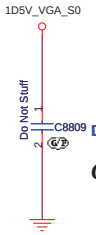
*FOR VRAM1*




*CLOSE TO THE MEMORY*

*FOR VRAM2*




*CLOSE TO THE MEMORY*

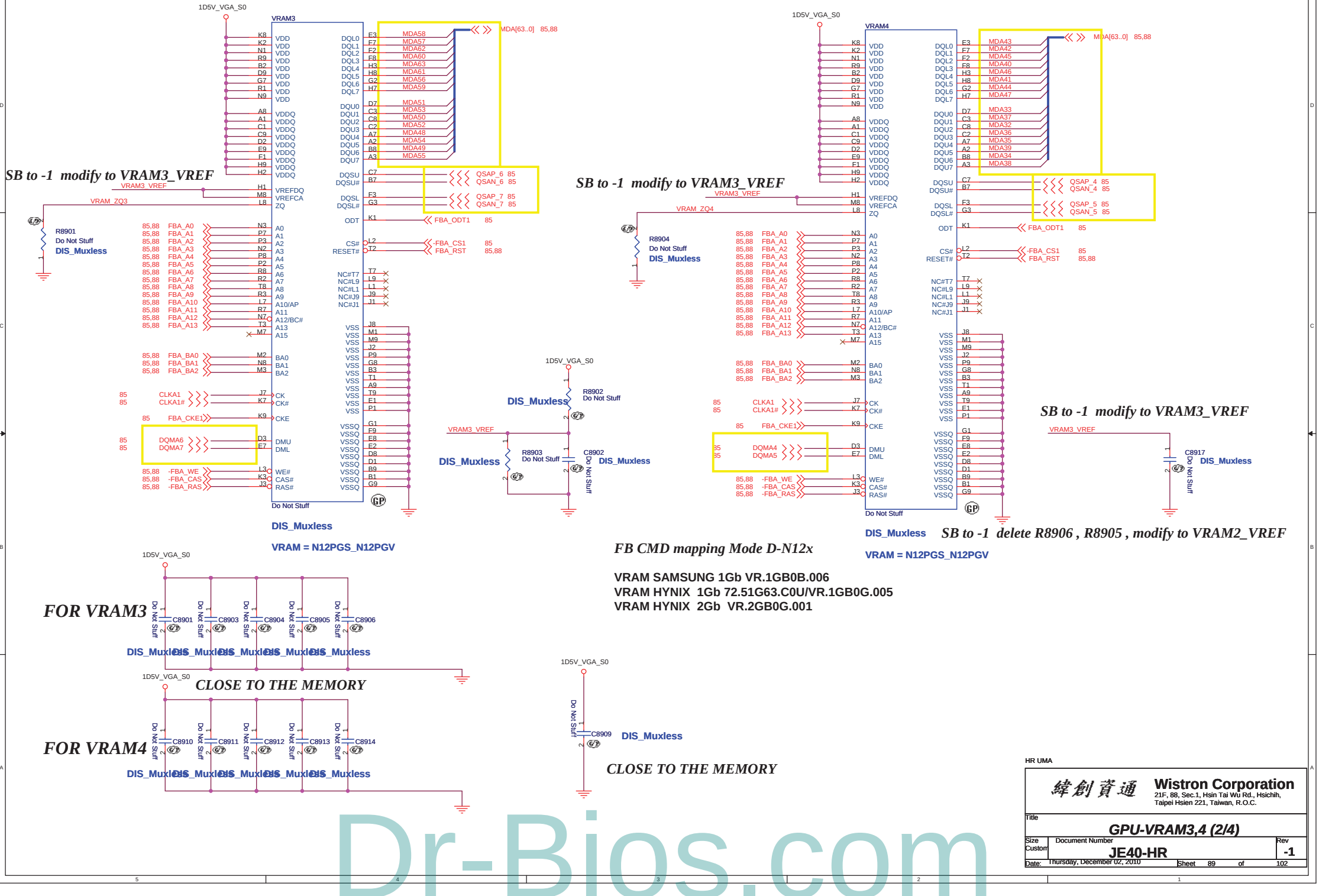
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM1,2 (1/4)***

| Size | Document Number | Rev |
|---|---|---|
| Custom | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 88 of 102





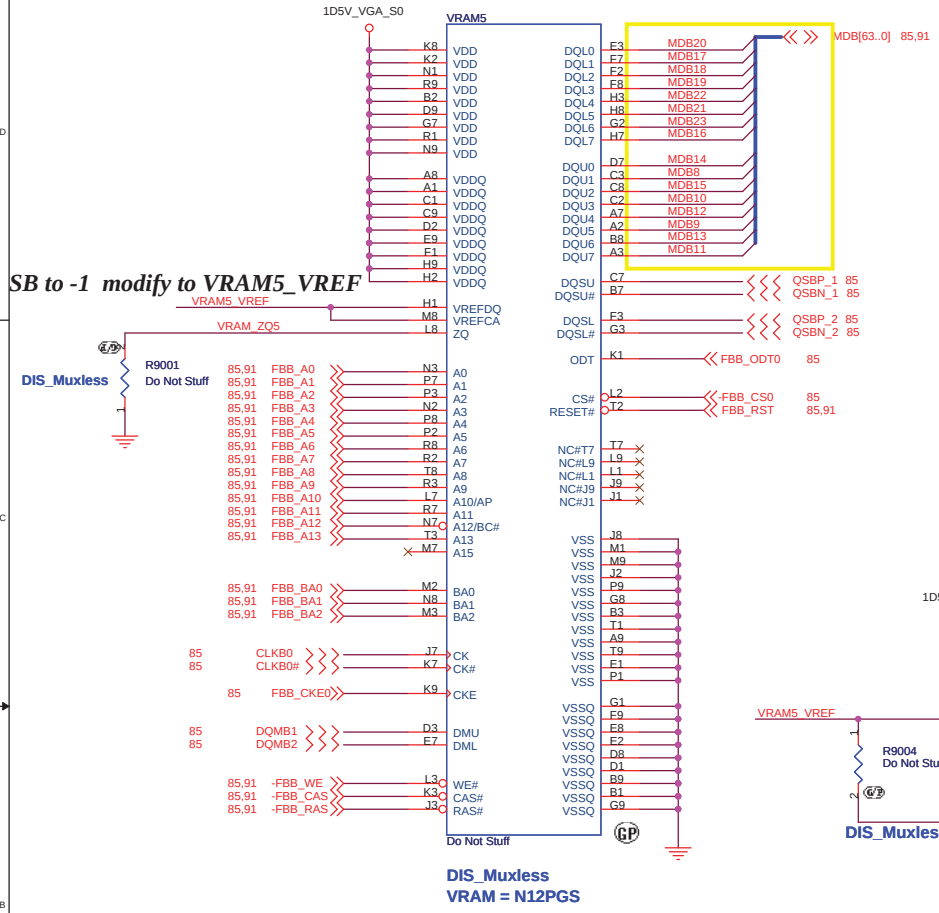

HR UMA

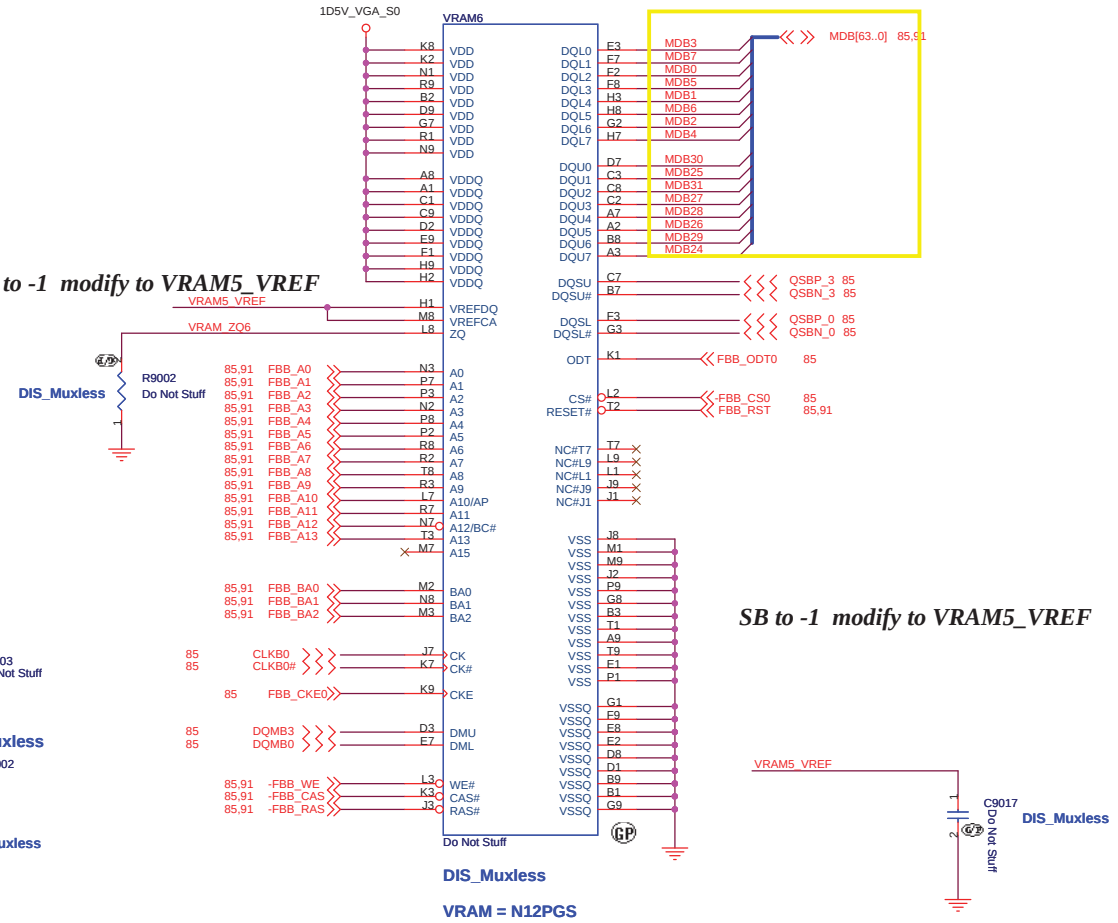
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

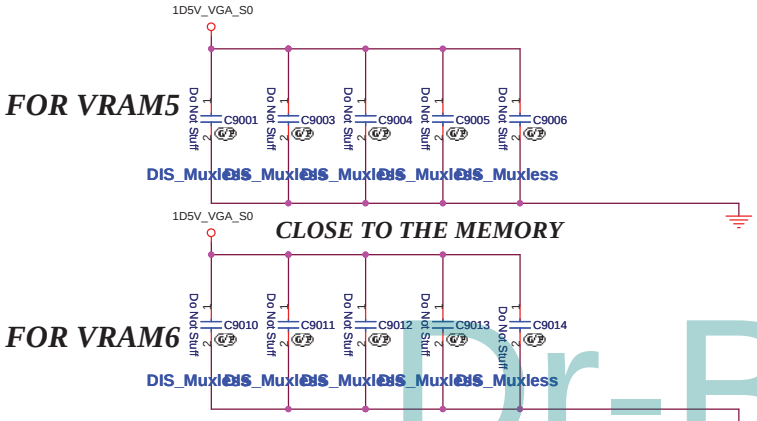
Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 89 of 102

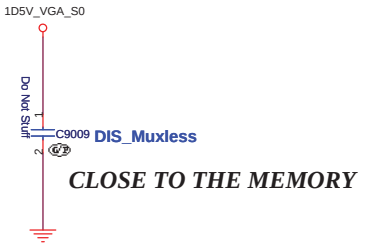



VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001




DG requires 4x0.1uF and 8x1.0uF per VRAM chip





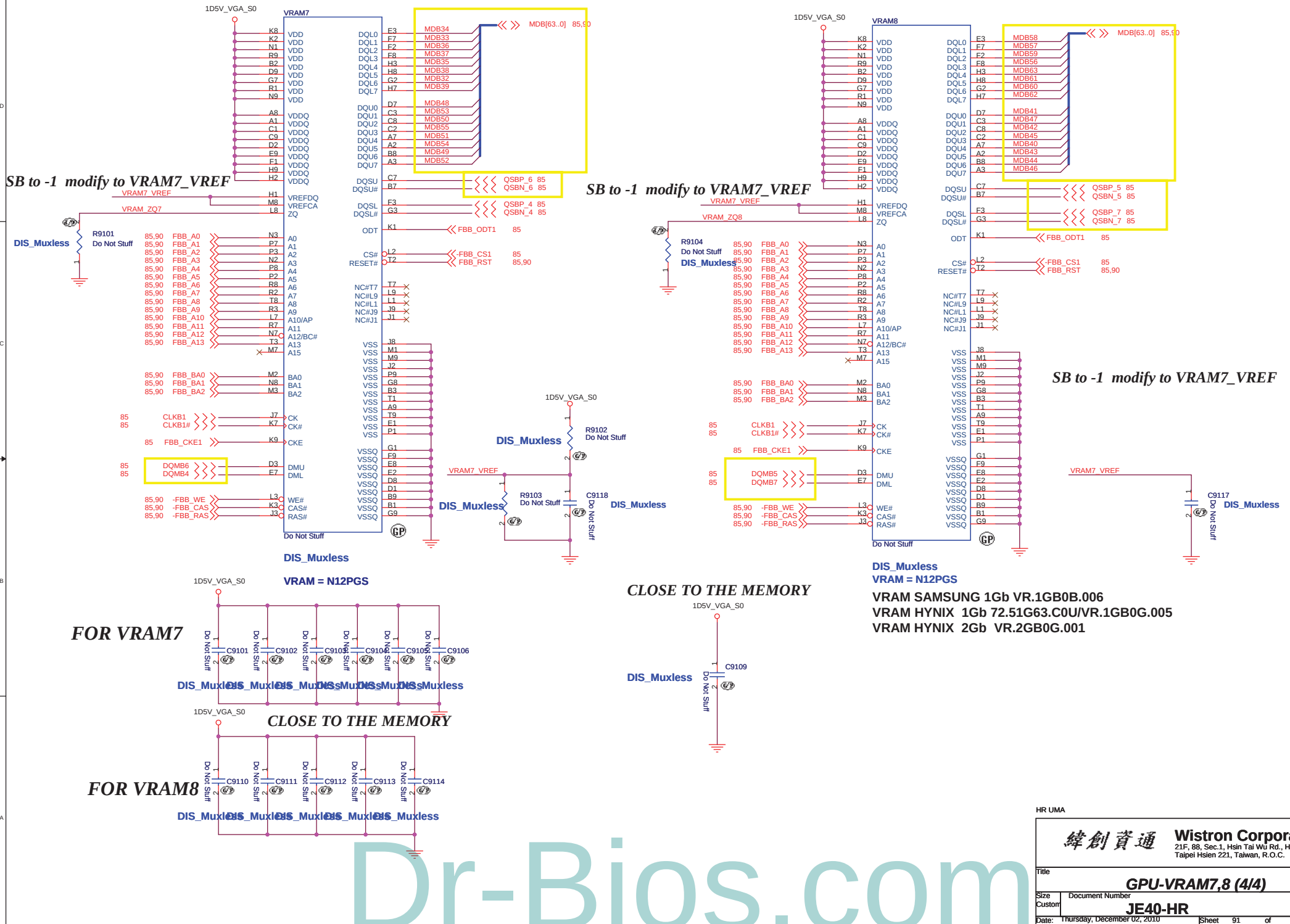

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

| Size | Document Number | Rev |
|---|---|---|
| Custom | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 90 of 102






HR UMA

| | |
|---|---|
| 緯創資通 Wistron Corporation | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | GPU-VRAM7,8 (4/4) |
| Size: Custom | Document Number: JE40-HR |
| Rev | -1 |
| Date: Thursday, December 02, 2010 | Sheet 91 of 102 |

20100715

**SSID = PWR.Plane.Regulator_GFX**

20100719

SB 20100831

20100715

SB 20100831

Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

SB to -1 modify PR9213 VGA_Core to 1.05V

RT8208A

N12P GS

| P-State | PWR_VGA_CORE_D1 | PWR_VGA_CORE_D0 | VGA_CORE_PWR |
|---|---|---|---|
| P8 , P12 | L | L | 0.825V |
| P0 - HOT | L | H | 0.975V |
| P0 - COLD | H | L | 1.00V |
| | H | H | |

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

**Frequency setting**
**470K -->165KHz**
**200K -->323KHz**
**100K -->500KHz**

N12P GV

| P-State | PWR_VGA_CORE_D1 | PWR_VGA_CORE_D0 | VGA_CORE_PWR |
|---|---|---|---|
| P8 , P12 | L | L | 0.85V |
| P0 - HOT | L | H | 1.00V |
| P0 - COLD | H | L | 1.025V |
| | H | H | |

Vout=0.75V*(R1+R2)/R2

HR UMA

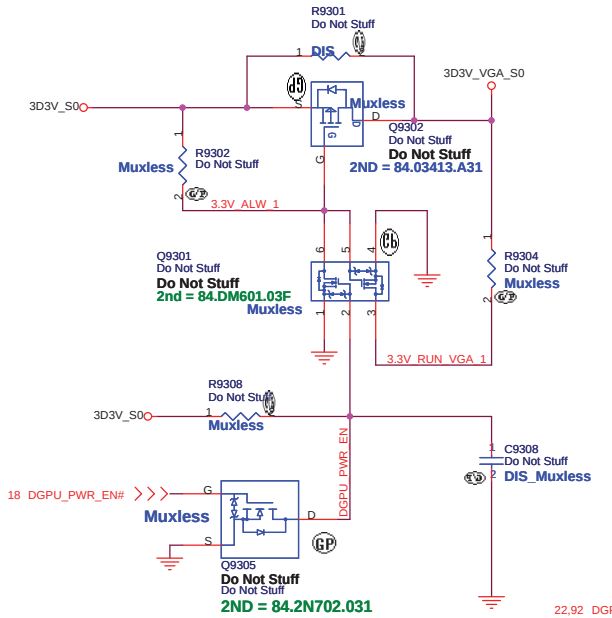
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VGA_CORE

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 92 of 102

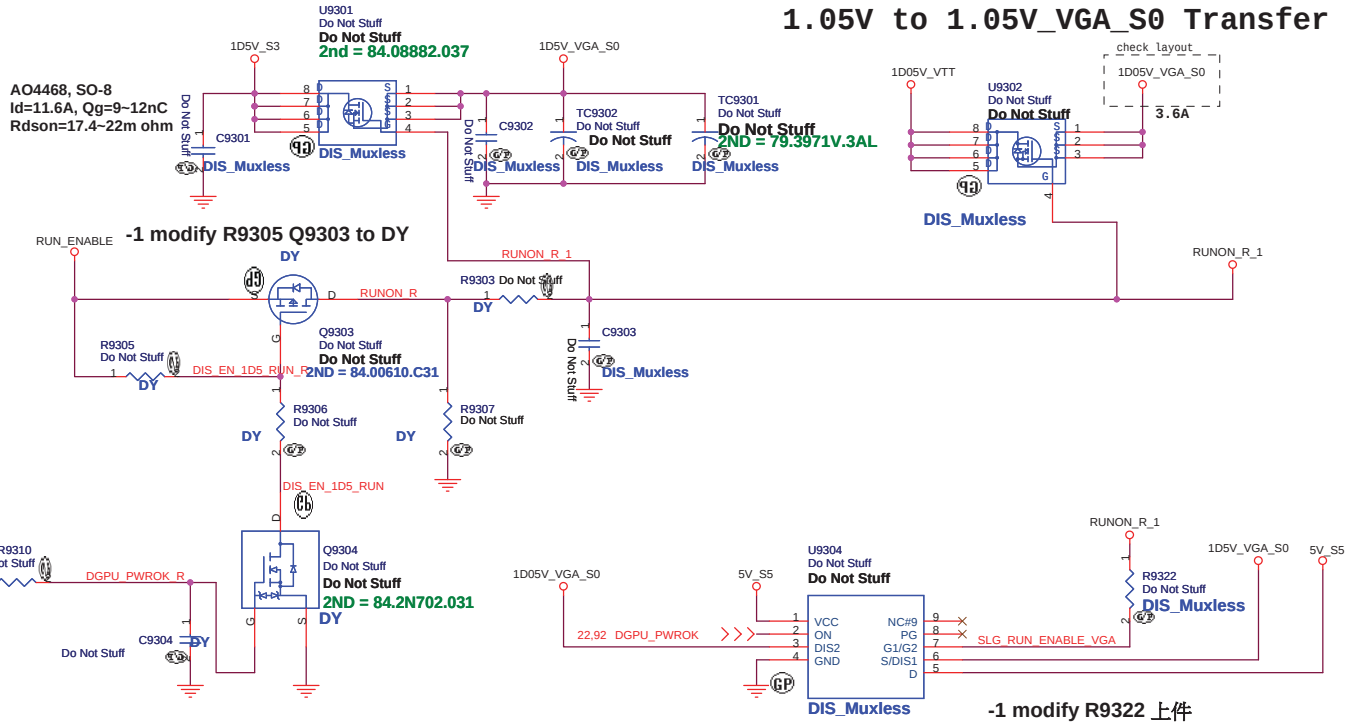
## +3VS to 3.3V_DELAY Transfer




## 1D5V_VGA_S0

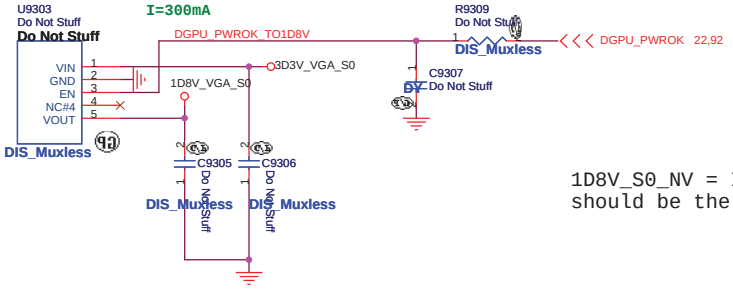
## SB modify to 84.03006.A37

## 1.05V to 1.05V_VGA_S0 Transfer



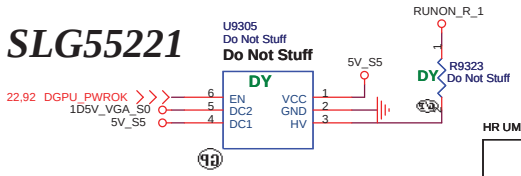

## RT9025 for 1D8V_VGA

## +3VS to 1.8V Transfer




1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

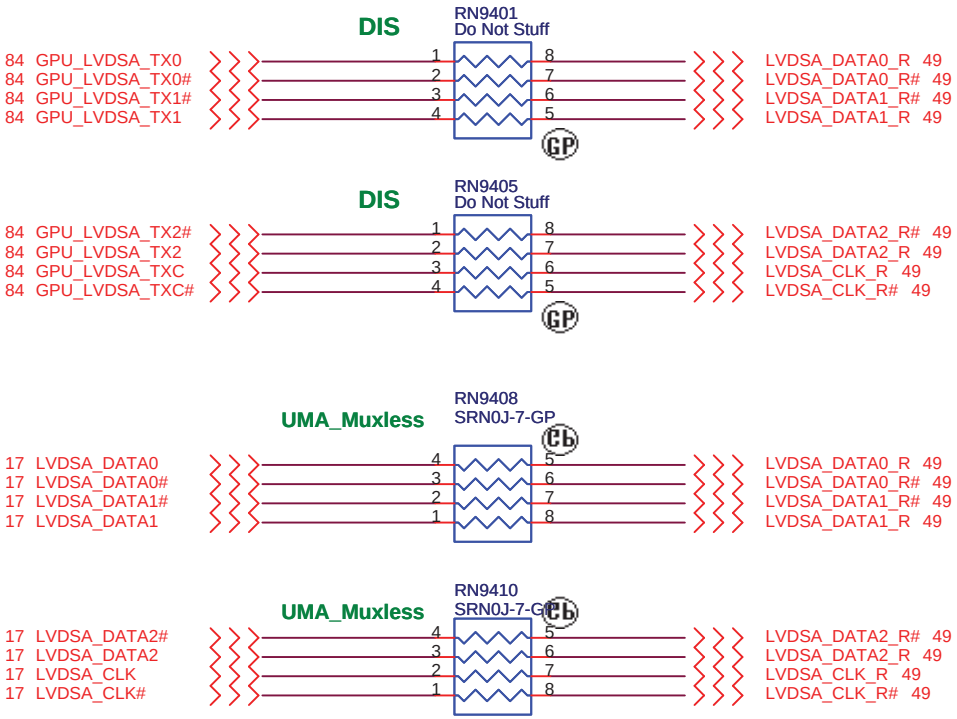
## -1 co-layout SLG55221



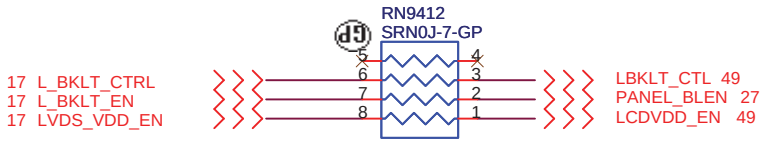

HR UMA

| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: DISCRETE VGA POWER | | |
| Size: Custom | Document Number: JE40-HR | Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 93 of 102 | |

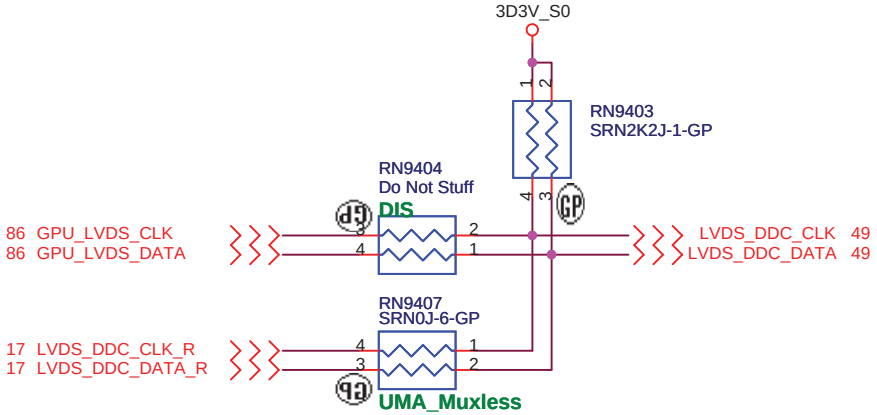
# LVDS Channel A




# Panel BL brightness/Power En/BL En



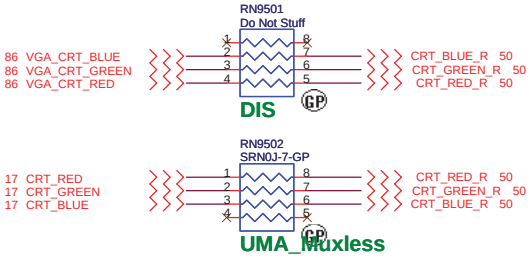




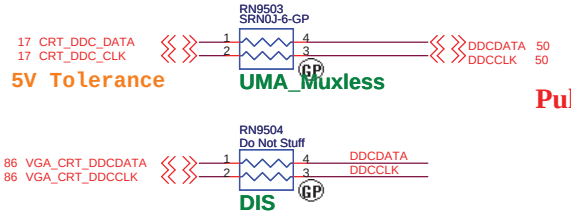

HR UMA

| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: *LVDS_Switch* | | |
| Size: A4 | Document Number: JE40-HR | Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 94 of 102 | |

Close to CRT Board CONN

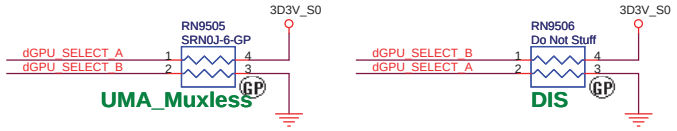



CRT DDCDATA & DDCCLK



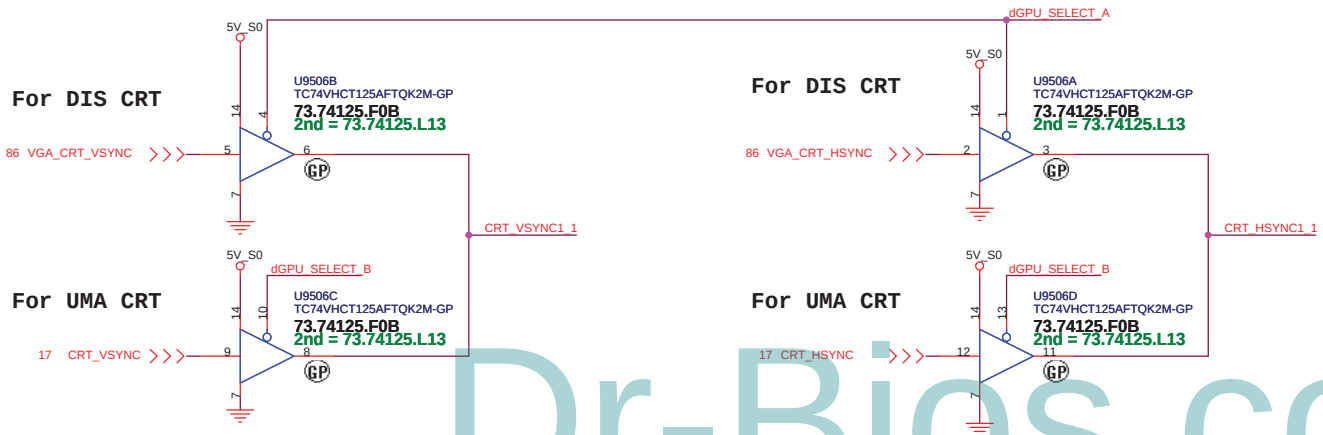

Pull high 在CRT

SB to -1 modify 4 port Logic




CRT Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA




SB to -1 modify R9503,R9504 to 10 ohm




HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Switch

Size: A3 | Document Number: JE40-HR | Rev: -1

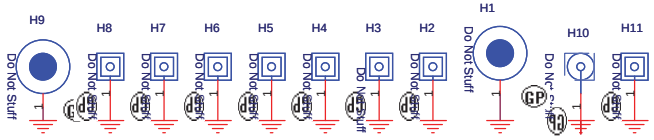
Date: Thursday, December 02, 2010 | Sheet 95 of 102

SSID = SDIO

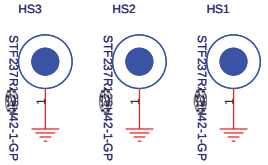


HR UMA

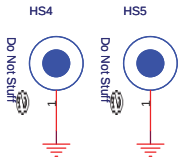
| | |
|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: TOUCH PANEL | |
| Size: A2 | Document Number: JE40-HR Rev: -1 |
| Date: Thursday, December 02, 2010 | Sheet 96 of 102 |



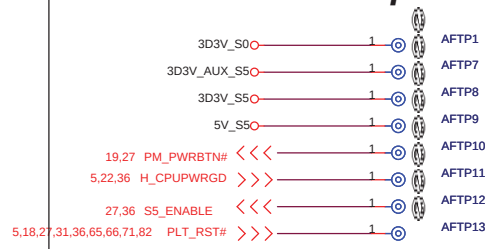

## CPU




## VGA



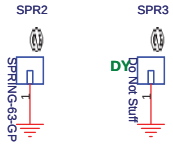

## Check test point




Test Point放在Dimm Door打開可量測處

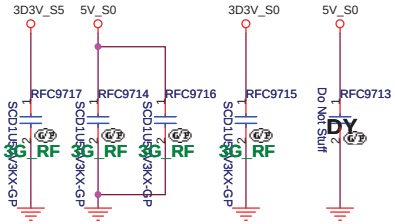
## SB to -1 BOM add SPR2

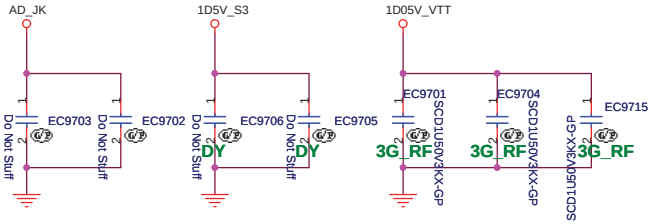
-2 delete SPR5

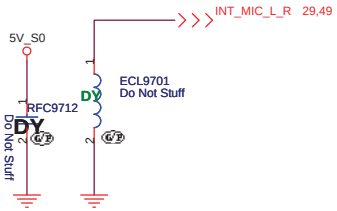


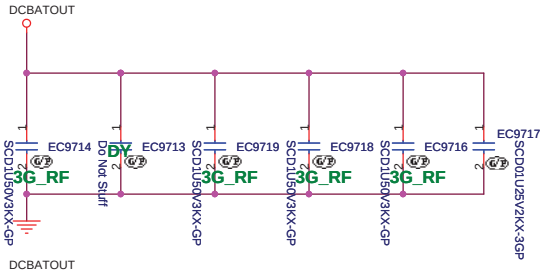

Change:34.40V16.001

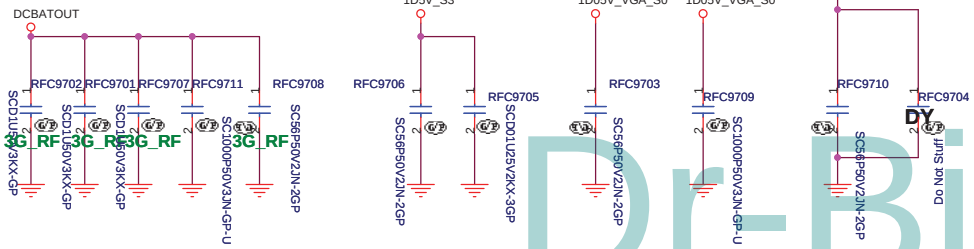

3G Sku

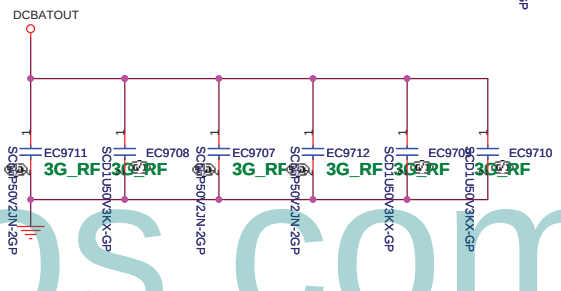





HR UMA

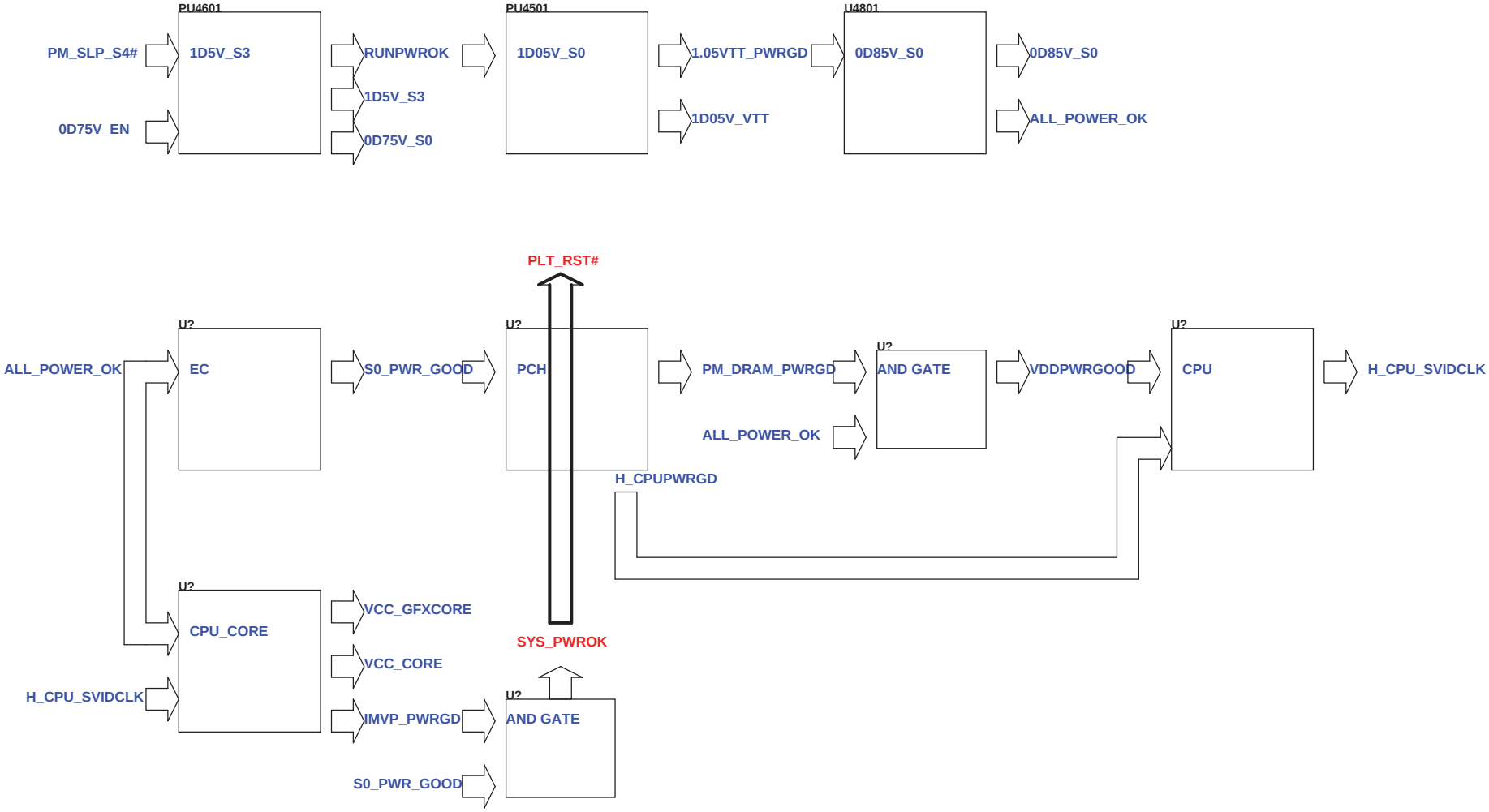
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 97 of 102

# Power Sequence






HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

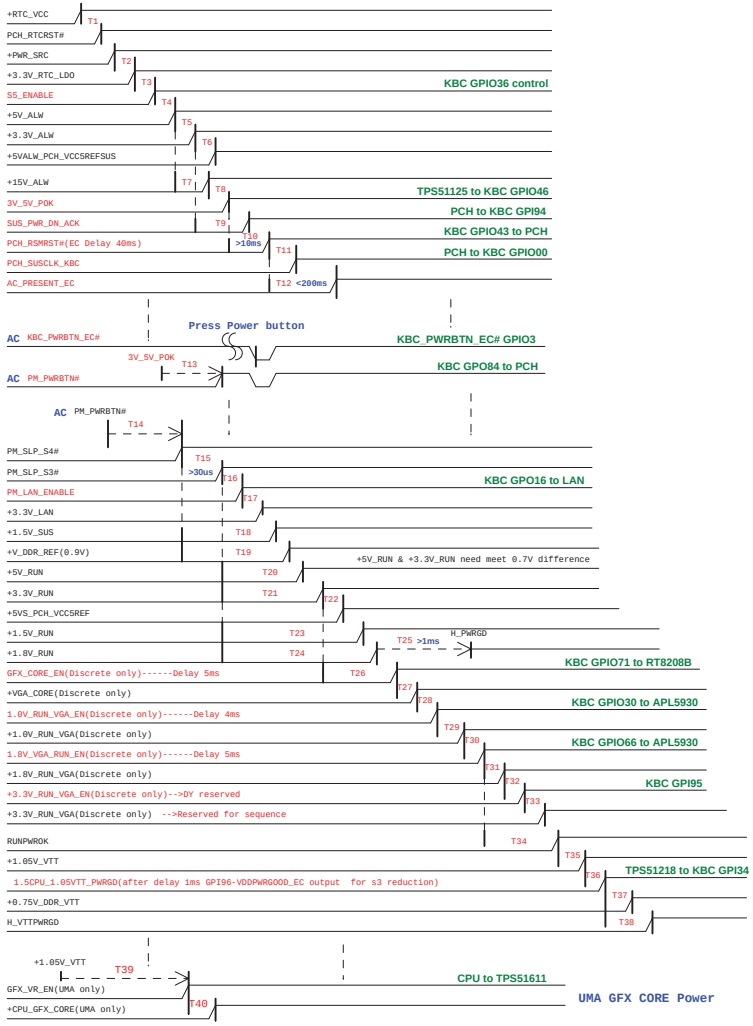
| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 98 of 102

# Intel-Power Up Sequence

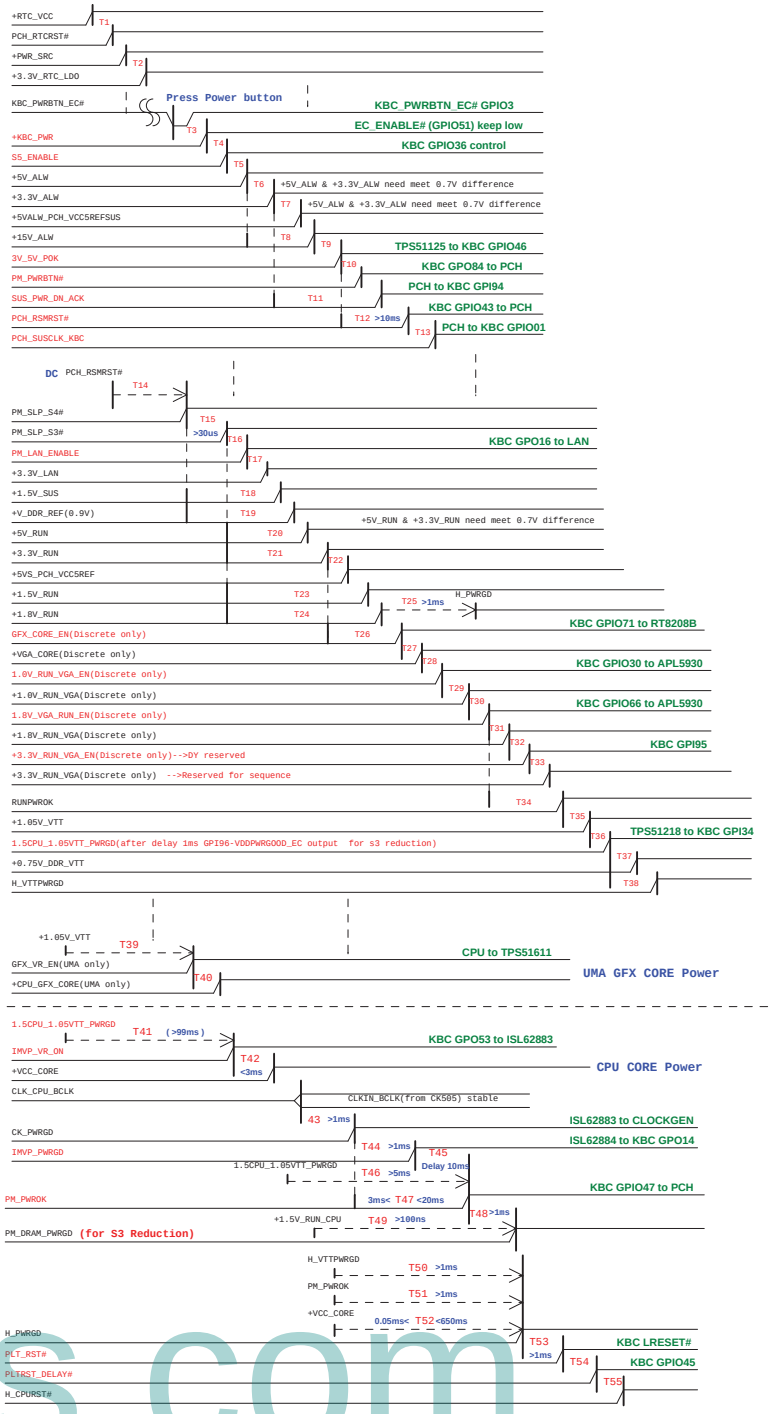
## (AC mode)

red word: KBC GPIO




## (DC mode)

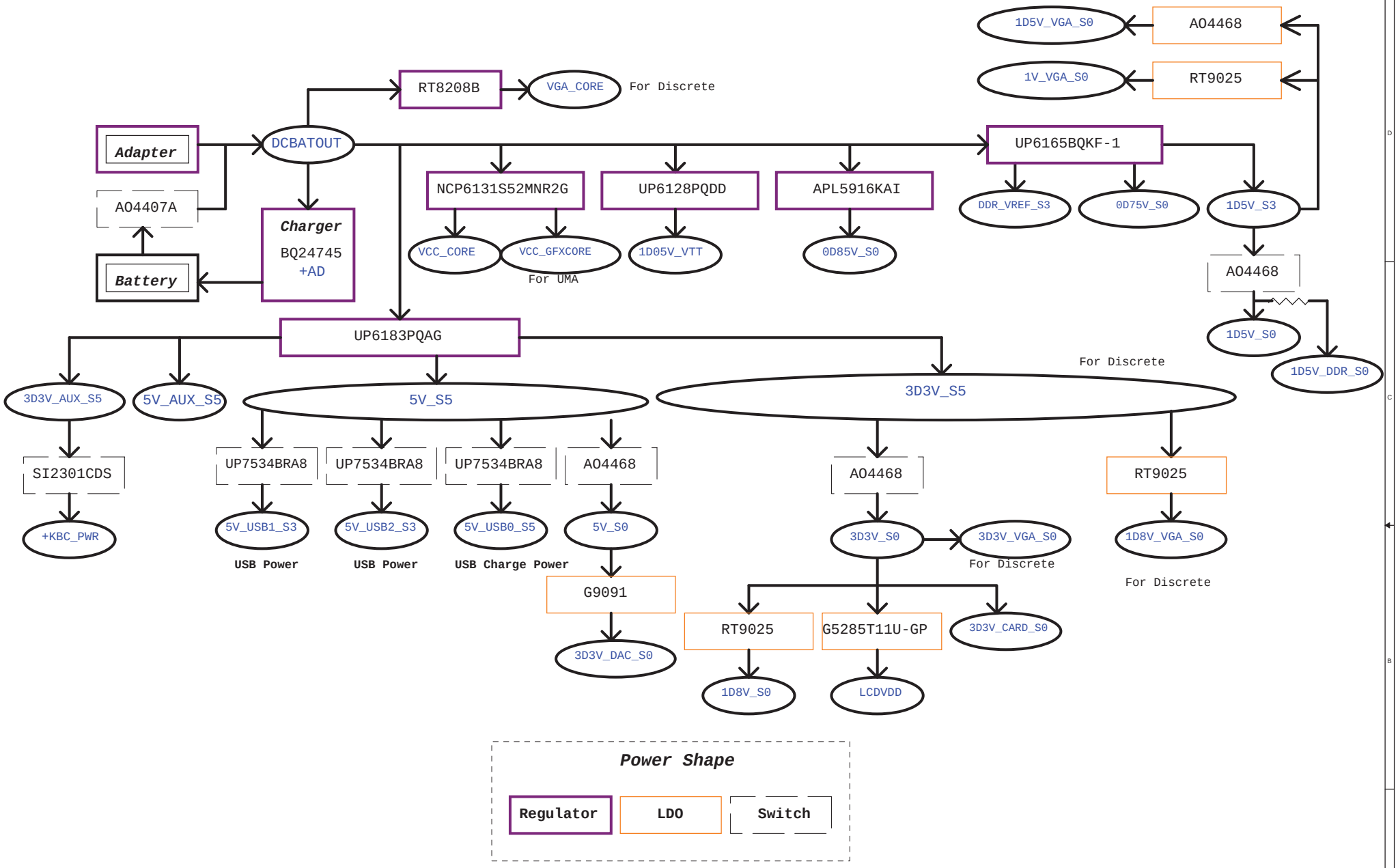
red word: KBC GPIO






HR UMA

| | | |
|---|---|---|
| 鋒創資通 | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: Power Sequence | | |
| Size: A1 | Document Number: JE40-HR | Rev: -1 |
| Date: Tuesday, December 04, 2007 | Sheet 9 of 10 | |






HR UMA

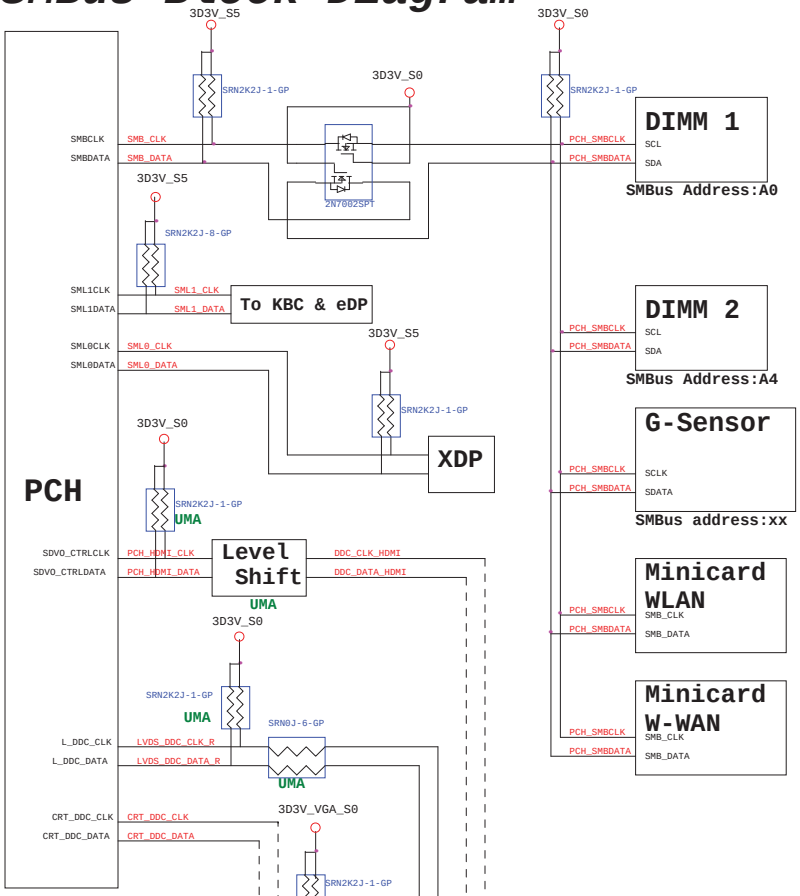
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

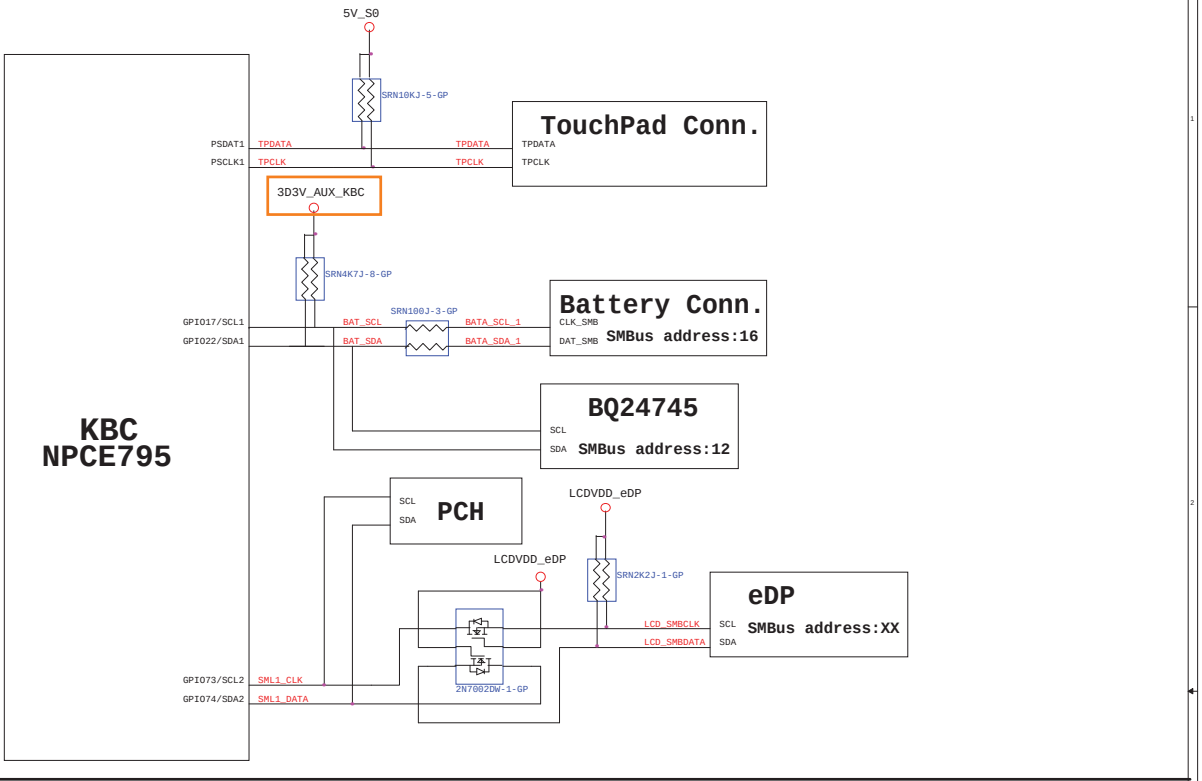
| Size | Document Number | Rev |
|---|---|---|
| A3 | JE40-HR | -1 |

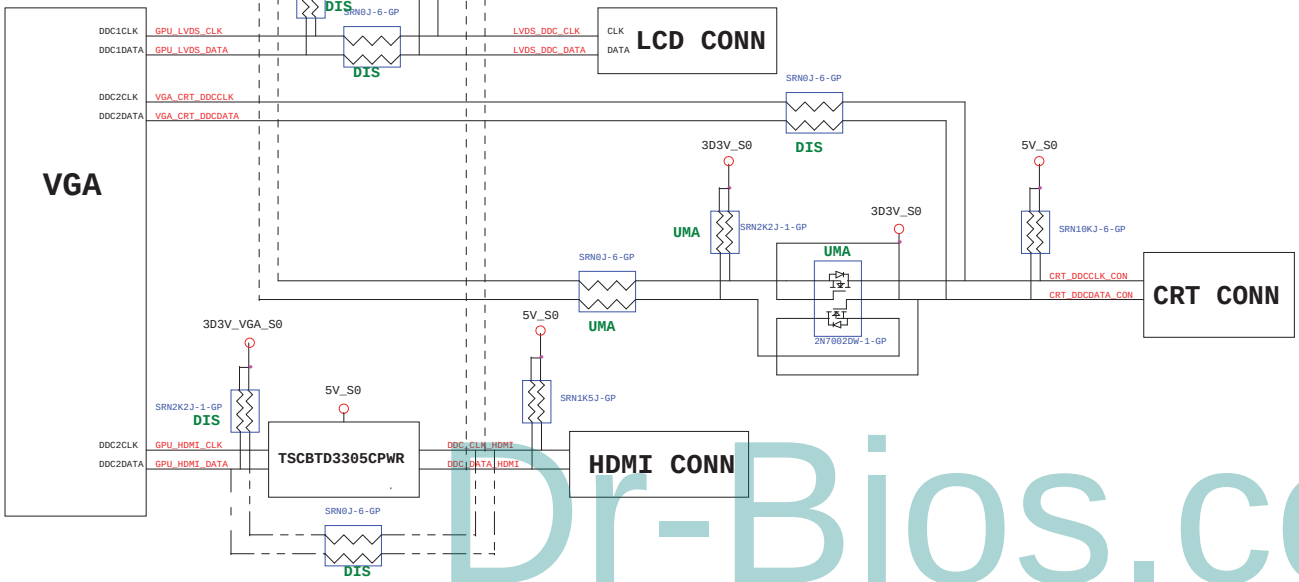
Date: Thursday, December 02, 2010 Sheet 100 of 102

# PCH SMBus Block Diagram




# KBC SMBus Block Diagram



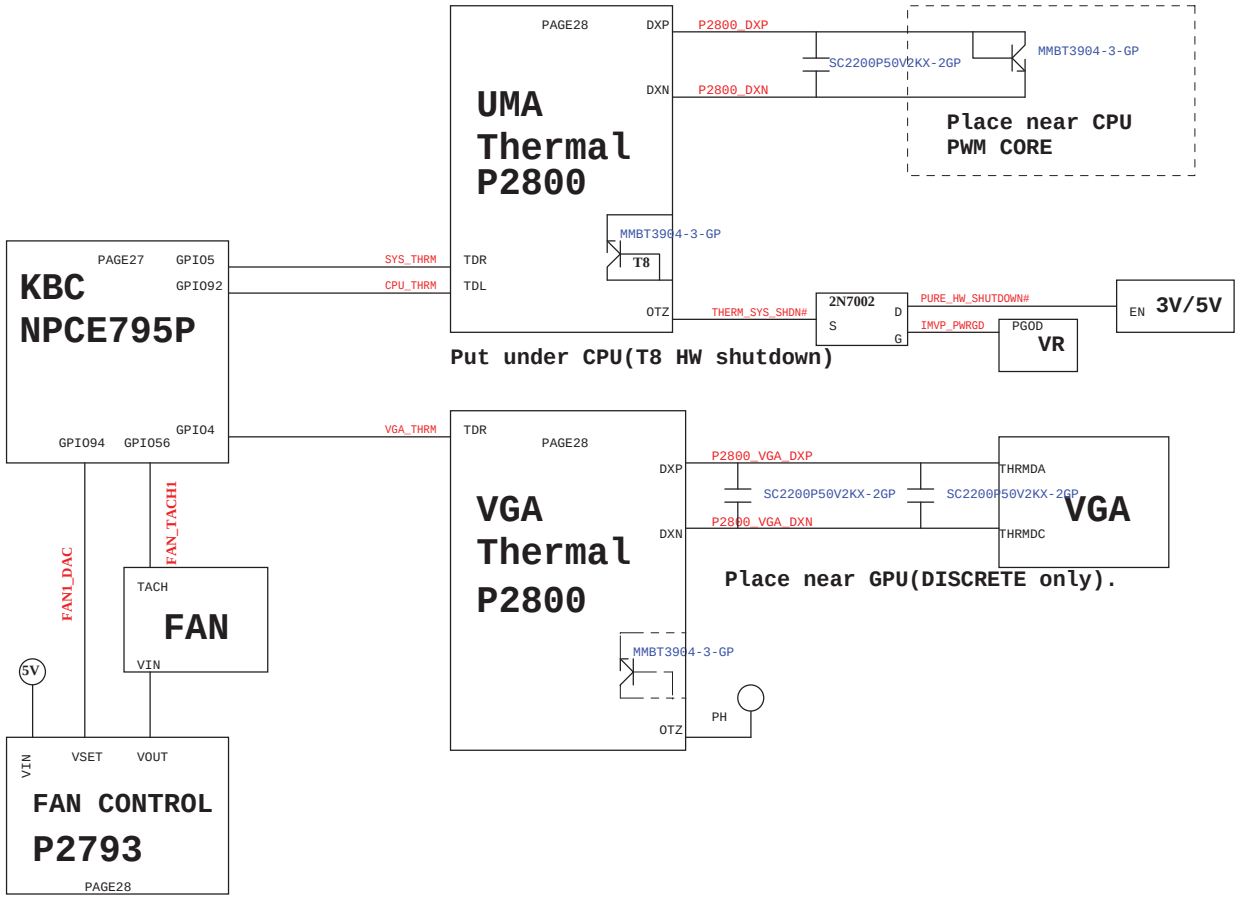





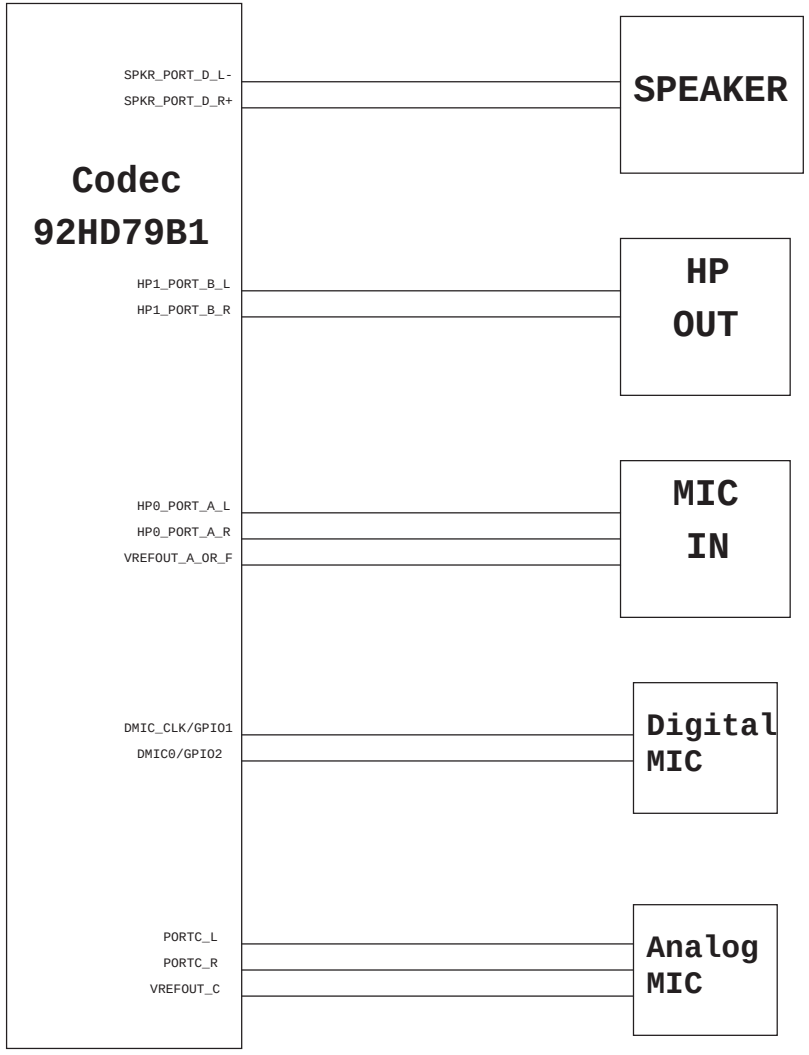

HR UMA

| | |
|---|---|
| 緯創資通 Wistron Corporation | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | SMBUS Block Diagram |
| Size A2 / Document Number | JE40-HR |
| Rev | -1 |
| Date: Thursday, December 02, 2010 | Sheet 101 of 102 |

# Thermal Block Diagram




# Audio Block Diagram






HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

| Size | Document Number | Rev |
|---|---|---|
| Custom | JE40-HR | -1 |

Date: Thursday, December 02, 2010 Sheet 102 of 102