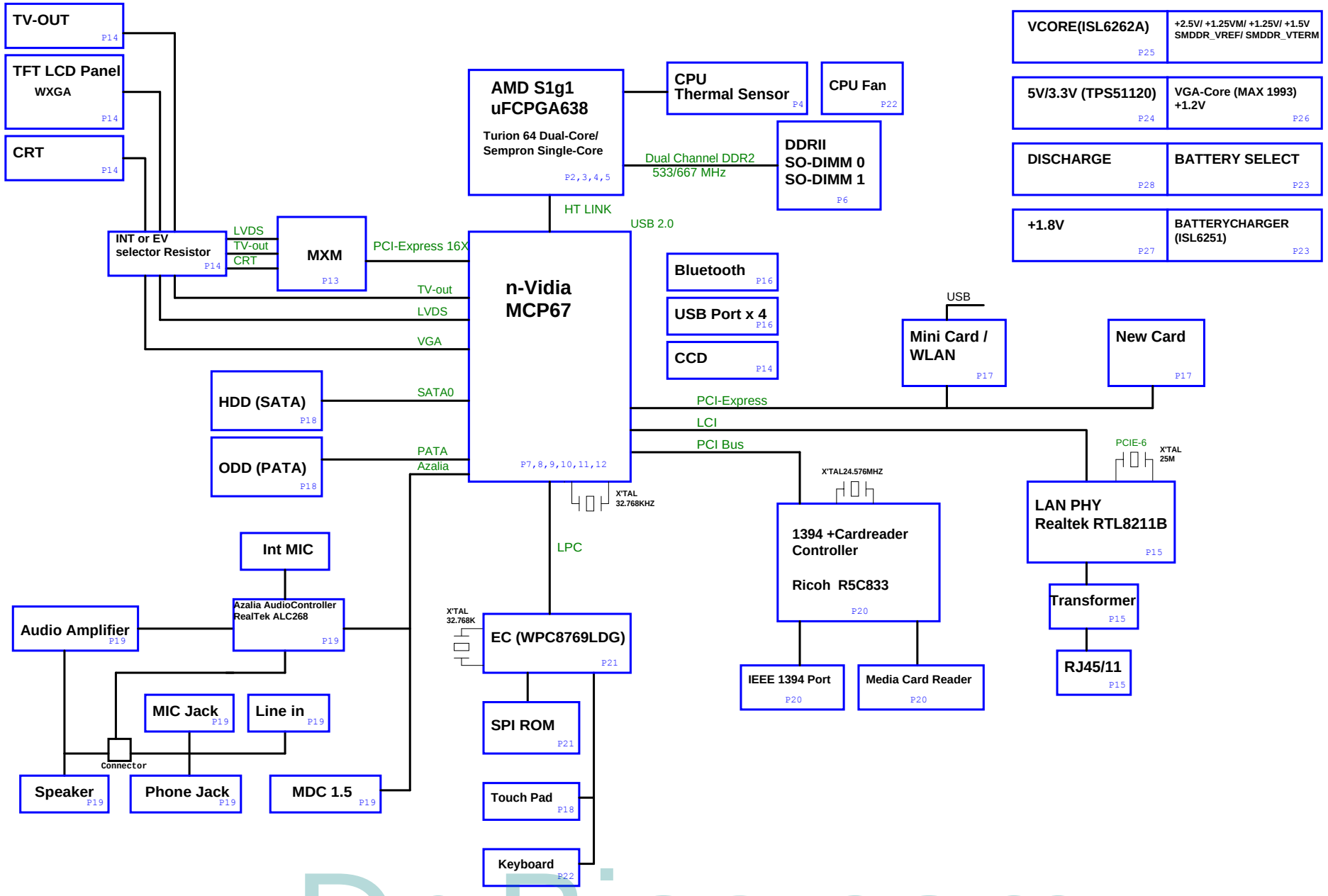
ZO3 SYSTEM BLOCK DIAGRAM



PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A

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(7) HT_RXD#[15..0] HT_RXD#[15..0]
(7) HT_RXD[15..0] HT_RXD[15..0]
(7) HT_TXD[15..0] HT_TXD[15..0]
(7) HT_TXD#[15..0] HT_TXD#[15..0]

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

VLDT_RUN

U21A

D4	VLDT_A3	VLDT_B3	AE5
D3	VLDT_A2	VLDT_B2	AE4
D2	VLDT_A1	VLDT_B1	AE3
D1	VLDT_A0	VLDT_B0	AE2

C516 4.7U_6

HT_RXD15 N5	L0_CADIN_H15	L0_CADOUT_H15	T4 HT_TXD15
HT_RXD#15 P5	L0_CADIN_L15	L0_CADOUT_L15	T3 HT_TXD#15
HT_RXD14 M3	L0_CADIN_H14	L0_CADOUT_H14	V5 HT_TXD14
HT_RXD#14 M4	L0_CADIN_L14	L0_CADOUT_L14	U5 HT_TXD#14
HT_RXD13 L5	L0_CADIN_H13	L0_CADOUT_H13	V4 HT_TXD13
HT_RXD#13 M5	L0_CADIN_L13	L0_CADOUT_L13	V3 HT_TXD#13
HT_RXD12 K3	L0_CADIN_H12	L0_CADOUT_H12	Y5 HT_TXD12
HT_RXD#12 K4	L0_CADIN_L12	L0_CADOUT_L12	W5 HT_TXD#12
HT_RXD11 H3	L0_CADIN_H11	L0_CADOUT_H11	AB5 HT_TXD11
HT_RXD#11 H4	L0_CADIN_L11	L0_CADOUT_L11	AA5 HT_TXD#11
HT_RXD10 G5	L0_CADIN_H10	L0_CADOUT_H10	AB4 HT_TXD10
HT_RXD#10 H5	L0_CADIN_L10	L0_CADOUT_L10	AB3 HT_TXD#10
HT_RXD9 F3	L0_CADIN_H9	L0_CADOUT_H9	AD5 HT_TXD9
HT_RXD#9 F4	L0_CADIN_L9	L0_CADOUT_L9	AC5 HT_TXD#9
HT_RXD8 E5	L0_CADIN_H8	L0_CADOUT_H8	AD4 HT_TXD8
HT_RXD#8 F5	L0_CADIN_L8	L0_CADOUT_L8	AD3 HT_TXD#8
HT_RXD7 N3	L0_CADIN_H7	L0_CADOUT_H7	T1 HT_TXD7
HT_RXD#7 N2	L0_CADIN_L7	L0_CADOUT_L7	R1 HT_TXD#7
HT_RXD6 L1	L0_CADIN_H6	L0_CADOUT_H6	U2 HT_TXD6
HT_RXD#6 M1	L0_CADIN_L6	L0_CADOUT_L6	U3 HT_TXD#6
HT_RXD5 L3	L0_CADIN_H5	L0_CADOUT_H5	V1 HT_TXD5
HT_RXD#5 L2	L0_CADIN_L5	L0_CADOUT_L5	U1 HT_TXD#5
HT_RXD4 J1	L0_CADIN_H4	L0_CADOUT_H4	W2 HT_TXD4
HT_RXD#4 K1	L0_CADIN_L4	L0_CADOUT_L4	W3 HT_TXD#4
HT_RXD3 G1	L0_CADIN_H3	L0_CADOUT_H3	AA2 HT_TXD3
HT_RXD#3 H1	L0_CADIN_L3	L0_CADOUT_L3	AA3 HT_TXD#3
HT_RXD2 G3	L0_CADIN_H2	L0_CADOUT_H2	AB1 HT_TXD2
HT_RXD#2 G2	L0_CADIN_L2	L0_CADOUT_L2	AA1 HT_TXD#2
HT_RXD1 F1	L0_CADIN_H1	L0_CADOUT_H1	AC2 HT_TXD1
HT_RXD#1 F1	L0_CADIN_L1	L0_CADOUT_L1	AC3 HT_TXD#1
HT_RXD0 E3	L0_CADIN_H0	L0_CADOUT_H0	AD1 HT_TXD0
HT_RXD#0 E2	L0_CADIN_L0	L0_CADOUT_L0	AC1 HT_TXD#0

(7) HT_CPU_UPCLK1 J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4 HT_CPU_DWNCLK1 (7)
(7) HT_CPU_UPCLK#1 K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3 HT_CPU_DWNCLK#1 (7)
(7) HT_CPU_UPCLK0 J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1 HT_CPU_DWNCLK0 (7)
(7) HT_CPU_UPCLK#0 J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1 HT_CPU_DWNCLK#0 (7)

VLDT_RUN

R369 51_4 HT_CTLIN1_P P3
R370 51_4 HT_CTLIN1_N P4

	L0_CTLIN_H1	L0_CTLOUT_H1	T5 HT_CPU_DWNCTL1
	L0_CTLIN_L1	L0_CTLOUT_L1	R5 HT_CPU_DWNCTL#1
(7) HT_CPU_UPCTL0 N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2 HT_CPU_DWNCTL0 (7)
(7) HT_CPU_UPCTL#0 P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3 HT_CPU_DWNCTL#0 (7)

T31
T30

Athlon 64 S1
Processor Socket

+1.2V_HT VLDT_RUN

L41 FBJ3216HS800_1206
L40 FBJ3216HS800_1206

80 ohm(4A)

C488 4.7U_6
C493 4.7U_6
C492 .22U_4
C491 .22U_4
C489 180P_4
C490 180P_4

LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

PROJECT : ZO3
Quanta Computer Inc.

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Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

+1.8VSUS

R229 2K/F_4

CPU_M_VREF

C241 .1U_4

C300 1000P_4

R230 2K/F_4

+1.8VSUS

R412 39.2/F_4

T35 VTT_SENSE

R413 39.2/F_4

M_ZN

M_ZP

+SMDDR_VTERM

U21B

W17 MEMVREF

Y10 VTT_SENSE

AE10 MEMZN

AF10 MEMZP

VTT1 D10
VTT2 C10
VTT3 B10
VTT4 AD10
VTT5 W10
VTT6 AC10
VTT7 AB10
VTT8 AA10
VTT9 A10

(6) M_A_CS#3 V19 MA0_CS_L3
(6) M_A_CS#2 J22 MA0_CS_L2
(6) M_A_CS#1 V22 MA0_CS_L1
(6) M_A_CS#0 T19 MA0_CS_L0

MA0_CLK_H2 Y16 M_CLKOUT1 (6)
MA0_CLK_L2 AA16 M_CLKOUT1# (6)
MA0_CLK_H1 E16 M_CLKOUT0 (6)
MA0_CLK_L1 E16 M_CLKOUT0# (6)

(6) M_B_CS#3 Y26 MB0_CS_L3
(6) M_B_CS#2 J24 MB0_CS_L2
(6) M_B_CS#1 W24 MB0_CS_L1
(6) M_B_CS#0 U23 MB0_CS_L0

MB0_CLK_H2 AF18 M_CLKOUT4 (6)
MB0_CLK_L2 AF17 M_CLKOUT4# (6)
MB0_CLK_H1 A17 M_CLKOUT3 (6)
MB0_CLK_L1 A18 M_CLKOUT3# (6)

(6) M_CKE3 H26 MB_CKE1
(6) M_CKE2 J23 MB_CKE0
(6) M_CKE1 J20 MA_CKE1
(6) M_CKE0 J21 MA_CKE0

MB0_ODT1 W23 M_ODT3 (6)
MB0_ODT0 W26 M_ODT2 (6)
MA0_ODT1 V20 M_ODT1 (6)
MA0_ODT0 U19 M_ODT0 (6)

(6) M_A_A[0..15]

M_A_A15 K19 MA_ADD15
M_A_A14 K20 MA_ADD14
M_A_A13 V24 MA_ADD13
M_A_A12 K24 MA_ADD12
M_A_A11 L20 MA_ADD11
M_A_A10 R19 MA_ADD10
M_A_A9 L19 MA_ADD9
M_A_A8 L22 MA_ADD8
M_A_A7 L21 MA_ADD7
M_A_A6 M19 MA_ADD6
M_A_A5 M20 MA_ADD5
M_A_A4 M24 MA_ADD4
M_A_A3 M22 MA_ADD3
M_A_A2 N22 MA_ADD2
M_A_A1 N21 MA_ADD1
M_A_A0 R21 MA_ADD0

MB_ADD15 J25 M_B_A15
MB_ADD14 J26 M_B_A14
MB_ADD13 W25 M_B_A13
MB_ADD12 L23 M_B_A12
MB_ADD11 L25 M_B_A11
MB_ADD10 U25 M_B_A10
MB_ADD9 L24 M_B_A9
MB_ADD8 M26 M_B_A8
MB_ADD7 L26 M_B_A7
MB_ADD6 N23 M_B_A6
MB_ADD5 N24 M_B_A5
MB_ADD4 N25 M_B_A4
MB_ADD3 N26 M_B_A3
MB_ADD2 P24 M_B_A2
MB_ADD1 P26 M_B_A1
MB_ADD0 T24 M_B_A0

M_B_A[0..15] (6)

(6) M_A_BS#2 K22 MA_BANK2
(6) M_A_BS#1 R20 MA_BANK1
(6) M_A_BS#0 T22 MA_BANK0

MB_BANK2 K26 M_B_BS#2 (6)
MB_BANK1 T26 M_B_BS#1 (6)
MB_BANK0 U26 M_B_BS#0 (6)

(6) M_A_RAS# T20 MA_RAS_L
(6) M_A_CAS# U20 MA_CAS_L
(6) M_A_WE# U21 MA_WE_L

MB_RAS_L U24 M_B_RAS# (6)
MB_CAS_L V26 M_B_CAS# (6)
MB_WE_L U22 M_B_WE# (6)

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

Near CPU L<1200mil

M_CLKOUT3 C157 1.5P_4 M_CLKOUT3#

M_CLKOUT4 C282 1.5P_4 M_CLKOUT4#

M_CLKOUT0 C139 1.5P_4 M_CLKOUT0#

M_CLKOUT1 C297 1.5P_4 M_CLKOUT1#

+SMDDR_VTERM

C294 4.7U_6
C145 4.7U_6
C239 4.7U_6
C295 4.7U_6
C141 .22U_4
C285 .22U_4
C289 .22U_4
C287 .22U_4
C290 1000P_4
C288 1000P_4
C142 1000P_4
C286 1000P_4
C301 180P_4
C140 180P_4
C302 180P_4
C284 180P_4

U21C

(6) M_B_DQ[0..63]

M_B_DQ63 AD11 MB_DATA63
M_B_DQ62 AE11 MB_DATA62
M_B_DQ61 AE14 MB_DATA61
M_B_DQ60 AE14 MB_DATA60
M_B_DQ59 Y11 MB_DATA59
M_B_DQ58 AB11 MB_DATA58
M_B_DQ57 AC12 MB_DATA57
M_B_DQ56 AE13 MB_DATA56
M_B_DQ55 AE15 MB_DATA55
M_B_DQ54 AF16 MB_DATA54
M_B_DQ53 AC18 MB_DATA53
M_B_DQ52 AF19 MB_DATA52
M_B_DQ51 AD14 MB_DATA51
M_B_DQ50 AC14 MB_DATA50
M_B_DQ49 AE18 MB_DATA49
M_B_DQ48 AD18 MB_DATA48
M_B_DQ47 AD20 MB_DATA47
M_B_DQ46 AC20 MB_DATA46
M_B_DQ45 AF23 MB_DATA45
M_B_DQ44 AF24 MB_DATA44
M_B_DQ43 AF20 MB_DATA43
M_B_DQ42 AE20 MB_DATA42
M_B_DQ41 AD22 MB_DATA41
M_B_DQ40 AC22 MB_DATA40
M_B_DQ39 AE25 MB_DATA39
M_B_DQ38 AD26 MB_DATA38
M_B_DQ37 AA25 MB_DATA37
M_B_DQ36 AA26 MB_DATA36
M_B_DQ35 AE24 MB_DATA35
M_B_DQ34 AD24 MB_DATA34
M_B_DQ33 AA23 MB_DATA33
M_B_DQ32 AA24 MB_DATA32
M_B_DQ31 G24 MB_DATA31
M_B_DQ30 G23 MB_DATA30
M_B_DQ29 D26 MB_DATA29
M_B_DQ28 C26 MB_DATA28
M_B_DQ27 G26 MB_DATA27
M_B_DQ26 G25 MB_DATA26
M_B_DQ25 E24 MB_DATA25
M_B_DQ24 F23 MB_DATA24
M_B_DQ23 C24 MB_DATA23
M_B_DQ22 B24 MB_DATA22
M_B_DQ21 C20 MB_DATA21
M_B_DQ20 B20 MB_DATA20
M_B_DQ19 C25 MB_DATA19
M_B_DQ18 D24 MB_DATA18
M_B_DQ17 A21 MB_DATA17
M_B_DQ16 D20 MB_DATA16
M_B_DQ15 D18 MB_DATA15
M_B_DQ14 C18 MB_DATA14
M_B_DQ13 D14 MB_DATA13
M_B_DQ12 C14 MB_DATA12
M_B_DQ11 A20 MB_DATA11
M_B_DQ10 A19 MB_DATA10
M_B_DQ9 A16 MB_DATA9
M_B_DQ8 A15 MB_DATA8
M_B_DQ7 A13 MB_DATA7
M_B_DQ6 D12 MB_DATA6
M_B_DQ5 E11 MB_DATA5
M_B_DQ4 G11 MB_DATA4
M_B_DQ3 B14 MB_DATA3
M_B_DQ2 A14 MB_DATA2
M_B_DQ1 A11 MB_DATA1
M_B_DQ0 C11 MB_DATA0

MA_DATA63 AA12 M_A_DQ63
MA_DATA62 AB12 M_A_DQ62
MA_DATA61 AA14 M_A_DQ61
MA_DATA60 AB14 M_A_DQ60
MA_DATA59 W11 M_A_DQ59
MA_DATA58 Y12 M_A_DQ58
MA_DATA57 AD13 M_A_DQ57
MA_DATA56 AB13 M_A_DQ56
MA_DATA55 AD15 M_A_DQ55
MA_DATA54 AB15 M_A_DQ54
MA_DATA53 AB17 M_A_DQ53
MA_DATA52 Y17 M_A_DQ52
MA_DATA51 Y14 M_A_DQ51
MA_DATA50 W14 M_A_DQ50
MA_DATA49 W16 M_A_DQ49
MA_DATA48 AD17 M_A_DQ48
MA_DATA47 Y18 M_A_DQ47
MA_DATA46 AD19 M_A_DQ46
MA_DATA45 AD21 M_A_DQ45
MA_DATA44 AB21 M_A_DQ44
MA_DATA43 AB18 M_A_DQ43
MA_DATA42 AA18 M_A_DQ42
MA_DATA41 AA20 M_A_DQ41
MA_DATA40 Y20 M_A_DQ40
MA_DATA39 AA22 M_A_DQ39
MA_DATA38 Y22 M_A_DQ38
MA_DATA37 W21 M_A_DQ37
MA_DATA36 W22 M_A_DQ36
MA_DATA35 AA21 M_A_DQ35
MA_DATA34 AB22 M_A_DQ34
MA_DATA33 AB24 M_A_DQ33
MA_DATA32 Y24 M_A_DQ32
MA_DATA31 H22 M_A_DQ31
MA_DATA30 H20 M_A_DQ30
MA_DATA29 F22 M_A_DQ29
MA_DATA28 F21 M_A_DQ28
MA_DATA27 J19 M_A_DQ27
MA_DATA26 H24 M_A_DQ26
MA_DATA25 F22 M_A_DQ25
MA_DATA24 E20 M_A_DQ24
MA_DATA23 C23 M_A_DQ23
MA_DATA22 B22 M_A_DQ22
MA_DATA21 E18 M_A_DQ21
MA_DATA20 E20 M_A_DQ20
MA_DATA19 D22 M_A_DQ19
MA_DATA18 C19 M_A_DQ18
MA_DATA17 G18 M_A_DQ17
MA_DATA16 C17 M_A_DQ16
MA_DATA15 H12 M_A_DQ15
MA_DATA14 F14 M_A_DQ14
MA_DATA13 E14 M_A_DQ13
MA_DATA12 H17 M_A_DQ12
MA_DATA11 E17 M_A_DQ11
MA_DATA10 E15 M_A_DQ10
MA_DATA9 H15 M_A_DQ9
MA_DATA8 E13 M_A_DQ8
MA_DATA7 C13 M_A_DQ7
MA_DATA6 H12 M_A_DQ6
MA_DATA5 H11 M_A_DQ5
MA_DATA4 G14 M_A_DQ4
MA_DATA3 H14 M_A_DQ3
MA_DATA2 F12 M_A_DQ2
MA_DATA1 G12 M_A_DQ1
MA_DATA0 M_A_DQ0

M_A_DQ[0..63] (6)

To SODIMM socket B (Far)

To SODIMM socket A (near)

M_B_DM7 AD12 MB_DM7
M_B_DM6 AC16 MB_DM6
M_B_DM5 AE22 MB_DM5
M_B_DM4 AB26 MB_DM4
M_B_DM3 E25 MB_DM3
M_B_DM2 A22 MB_DM2
M_B_DM1 B16 MB_DM1
M_B_DM0 A12 MB_DM0

MA_DM7 Y13 M_A_DM7
MA_DM6 AB16 M_A_DM6
MA_DM5 Y19 M_A_DM5
MA_DM4 AC24 M_A_DM4
MA_DM3 F24 M_A_DM3
MA_DM2 E19 M_A_DM2
MA_DM1 C15 M_A_DM1
MA_DM0 E12 M_A_DM0

(6) M_B_DM[0..7]

M_A_DM[0..7] (6)

M_B_DQS7 AE12 MB_DQS_H7
M_B_DQS#7 AE12 MB_DQS_L7
M_B_DQS6 AE16 MB_DQS_H6
M_B_DQS#6 AD16 MB_DQS_L6
M_B_DQS5 AE21 MB_DQS_H5
M_B_DQS#5 AF22 MB_DQS_L5
M_B_DQS4 AC25 MB_DQS_H4
M_B_DQS#4 AC26 MB_DQS_L4
M_B_DQS3 F26 MB_DQS_H3
M_B_DQS#3 E26 MB_DQS_L3
M_B_DQS2 A24 MB_DQS_H2
M_B_DQS#2 A23 MB_DQS_L2
M_B_DQS1 D16 MB_DQS_H1
M_B_DQS#1 C16 MB_DQS_L1
M_B_DQS0 C12 MB_DQS_H0
M_B_DQS#0 B12 MB_DQS_L0

MA_DQS_H7 W12 M_A_DQS7
MA_DQS_L7 W13 M_A_DQS#7
MA_DQS_H6 Y15 M_A_DQS6
MA_DQS_L6 W15 M_A_DQS#6
MA_DQS_H5 AB19 M_A_DQS5
MA_DQS_L5 AB20 M_A_DQS#5
MA_DQS_H4 AD23 M_A_DQS4
MA_DQS_L4 AC23 M_A_DQS#4
MA_DQS_H3 G22 M_A_DQS3
MA_DQS_L3 G21 M_A_DQS#3
MA_DQS_H2 C22 M_A_DQS2
MA_DQS_L2 C21 M_A_DQS#2
MA_DQS_H1 G16 M_A_DQS1
MA_DQS_L1 G15 M_A_DQS#1
MA_DQS_H0 G13 M_A_DQS0
MA_DQS_L0 H13 M_A_DQS#0

DDR: DATA

Athlon 64 S1
Processor Socket

M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7

(6) M_B_DQS[0..7]

M_B_DQS#0
M_B_DQS#1
M_B_DQS#2
M_B_DQS#3
M_B_DQS#4
M_B_DQS#5
M_B_DQS#6
M_B_DQS#7

(6) M_B_DQS#[0..7]

M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7

M_A_DQS[0..7] (6)

M_A_DQS#0
M_A_DQS#1
M_A_DQS#2
M_A_DQS#3
M_A_DQS#4
M_A_DQS#5
M_A_DQS#6
M_A_DQS#7

M_A_DQS#[0..7] (6)

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Quanta Computer Inc.

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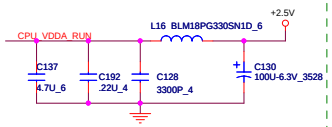
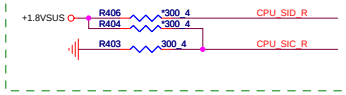
ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

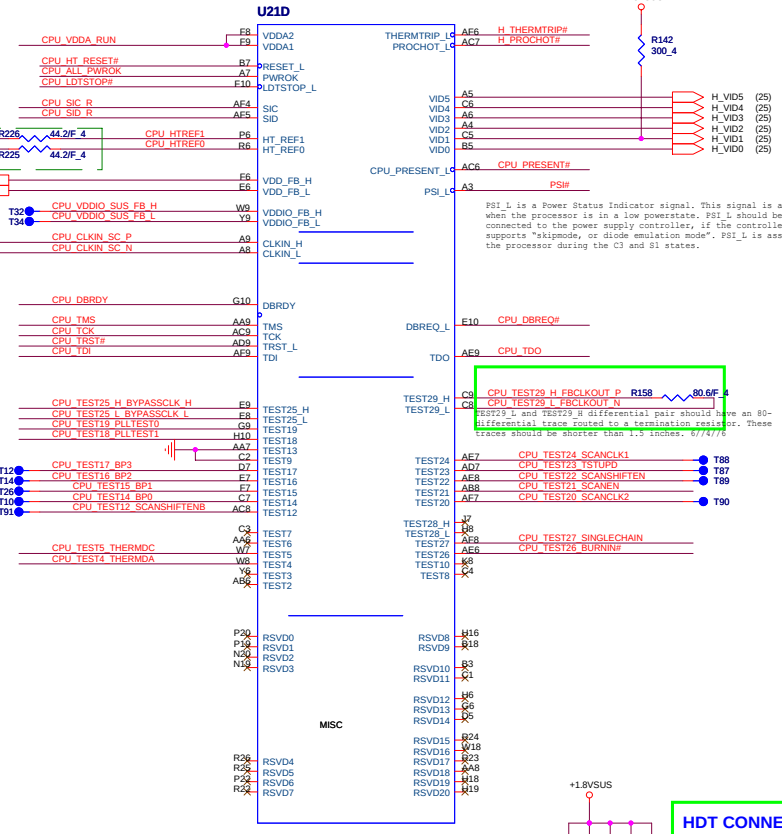
CPU_VDDA_RUN



If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.



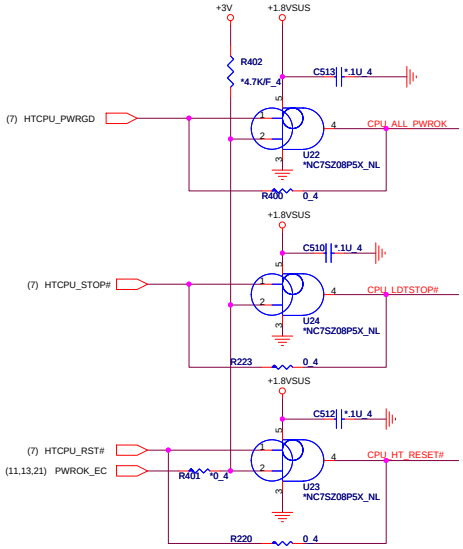
U21D

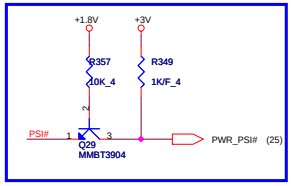


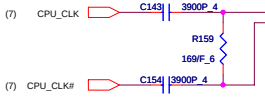
AMD NPT S1 SOCKET
Processor Socket

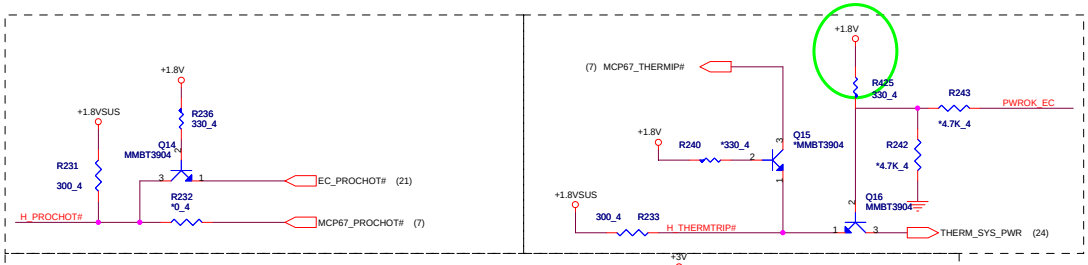
PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

PSP29_L and TEST29_H differential pair should have an 80-differential trace routed to a termination resistor. These traces should be shorter than 1.5 inches. 6/4/06

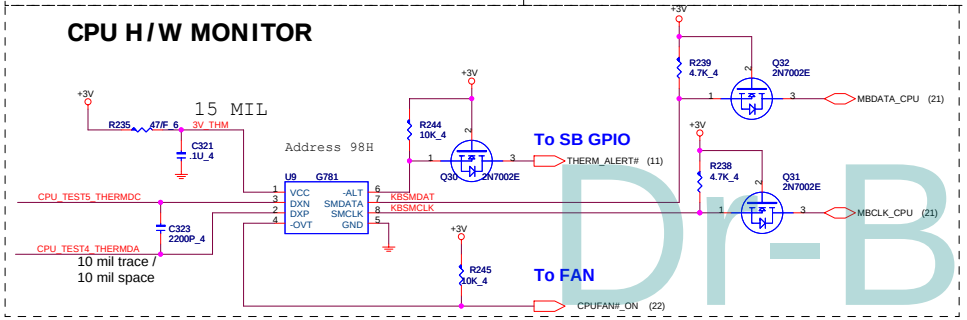


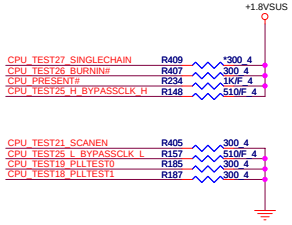




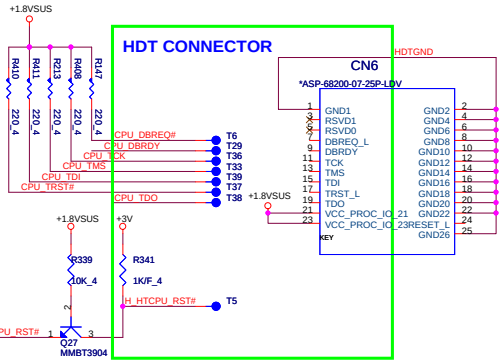


CPU H/W MONITOR





HDT CONNECTOR

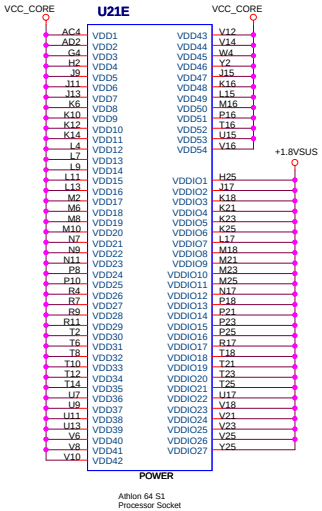


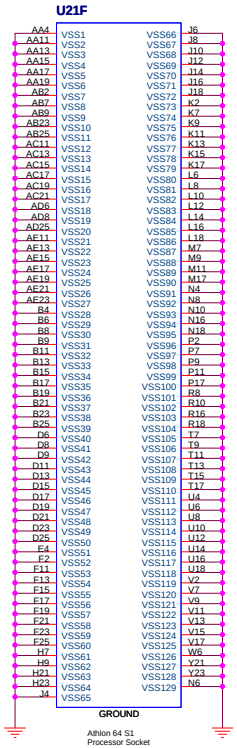
PROJECT : ZO3
Quanta Computer Inc.

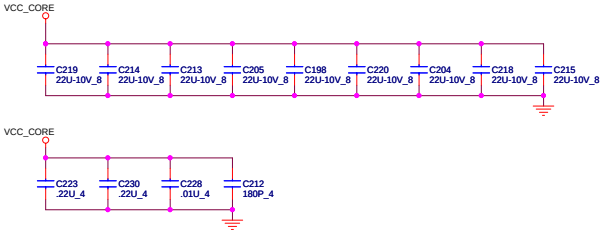
Size	Document Number	Rev
	ATHLON64 CTRL & DEBUG	2A

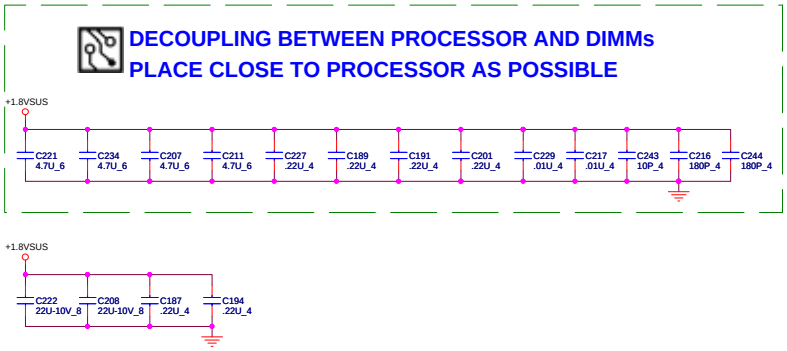
Date: Wednesday, April 25, 2007 Sheet 4 of 30

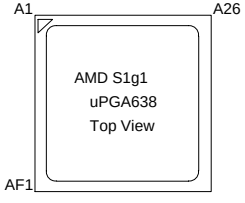
PROCESSOR POWER AND GROUND





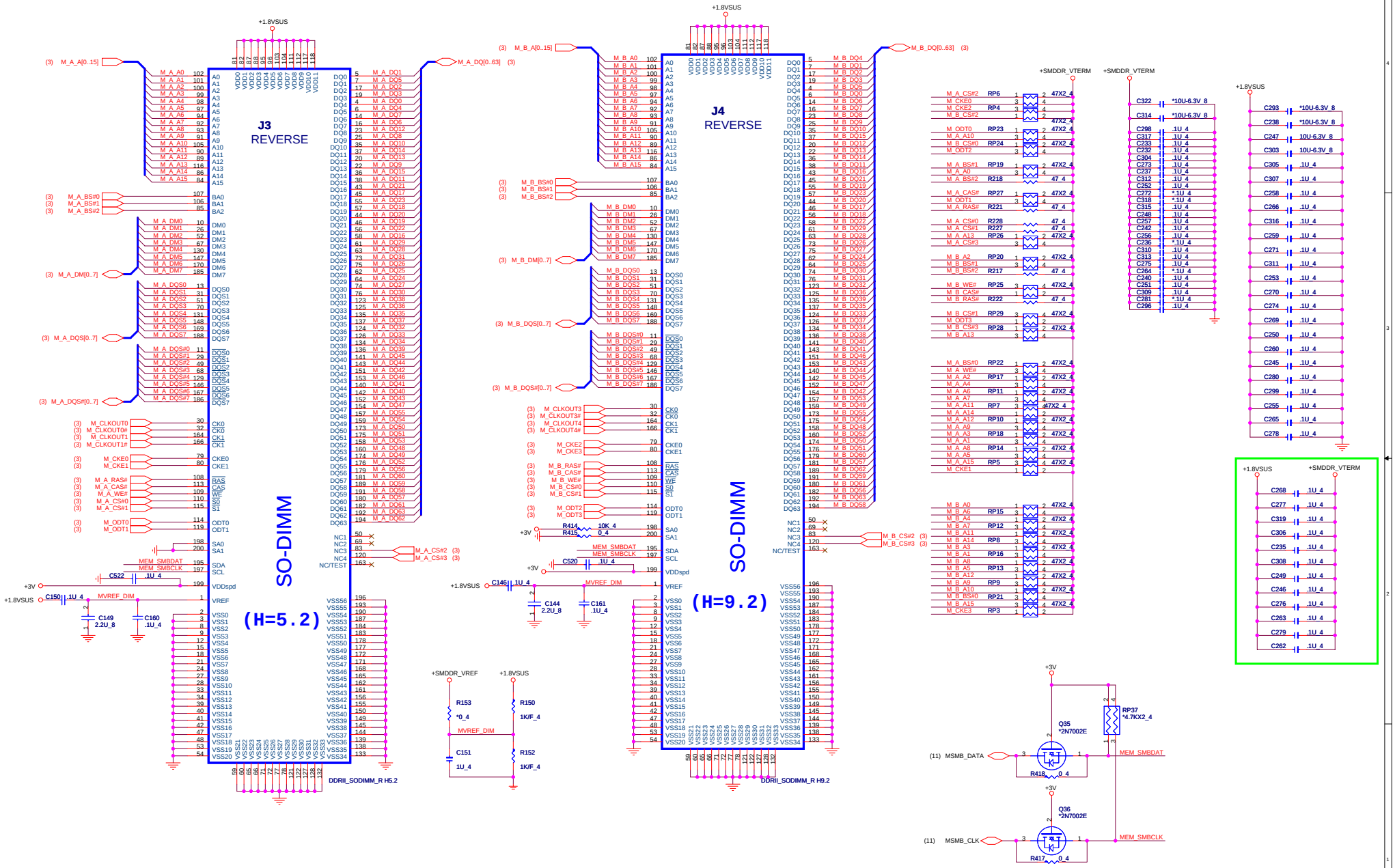






PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 PWR & GND	1A
Date: Wednesday, April 25, 2007	Sheet 5 of 30	



PROJECT : ZO3		
Quanta Computer Inc.		
Size	Document Number: DDR-II SODIMM*2	Rev: 1A
Date: Wednesday, April 25, 2007	Sheet 6 of 30	

A1:AJMCP670T00
A2:AJMCP670T04

MCP67 Used UMA Only	
MCP67 Signal Name	**Component**
RGB_DAC_RSET	STUFF
RGB_DAC_VREF	STUFF
DDC_DATA0	*10K LEAVE NC
TV_DAC_RSET	STUFF
TV_DAC_VREF	STUFF
IFPAB_RST	STUFF
IFPAB_VPROBE	STUFF
DDC_DATA2	*10K LEAVE NC
HPLUG_DET3	22K PULLDOWN
HDMI_RSET	STUFF
HDMI_VPROBE	STUFF
DDC_DATA3_R	10K PULLHIGH
HDCP_ROM_SDATA	10K PULLHIGH
HPLUG_DET2_R	6.2K PULLDOWN

MCP67 Unused UMA Only	
MCP67 Signal Name	**Component**
RGB_DAC_RSET	STUFF
RGB_DAC_VREF	STUFF
DDC_DATA0	10K PULLHIGH
TV_DAC_RSET	STUFF
TV_DAC_VREF	STUFF
IFPAB_RST	STUFF
IFPAB_VPROBE	STUFF
DDC_DATA2	10K PULLHIGH
HPLUG_DET3	22K PULLDOWN
HDMI_RSET	STUFF
HDMI_VPROBE	STUFF
DDC_DATA3_R	10K PULLHIGH
HDCP_ROM_SDATA	10K PULLHIGH
HPLUG_DET2_R	6.2K PULLDOWN

U20A

MCP67 1 OF 7

HT

DACS

FLAT PANEL

MCP67

FOR UMA ONLY

[LVDS]

UNUSED HDMI ONLY

FOR UMA ONLY

FOR DVI IS NOT IMPLEMENTED

B2B: changed CAP value

C3A: Remove C426,R332 for Nvidia suggest.

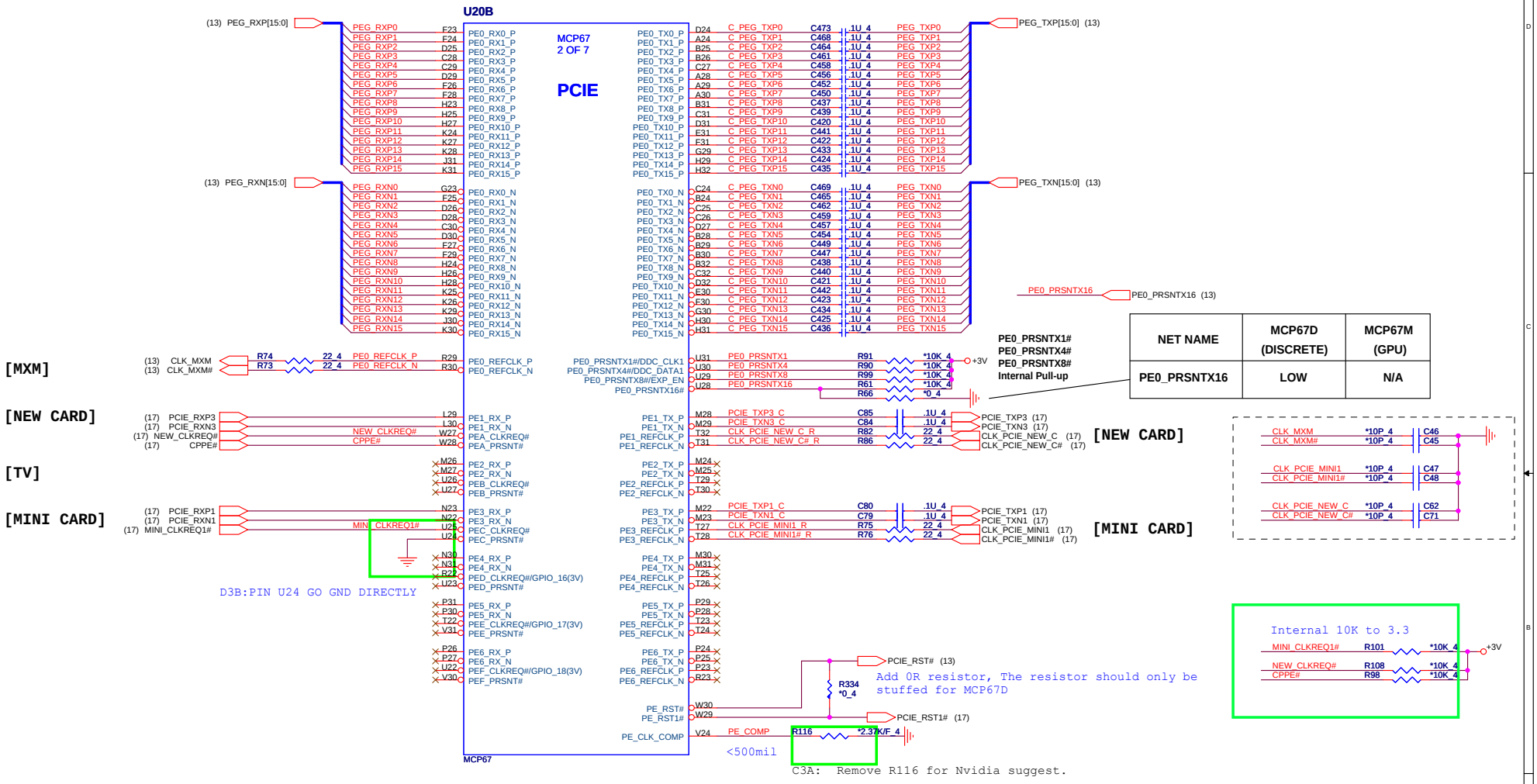
C3A: Remove C77,R331 for Nvidia suggest.

B2A: Remove R168,R139

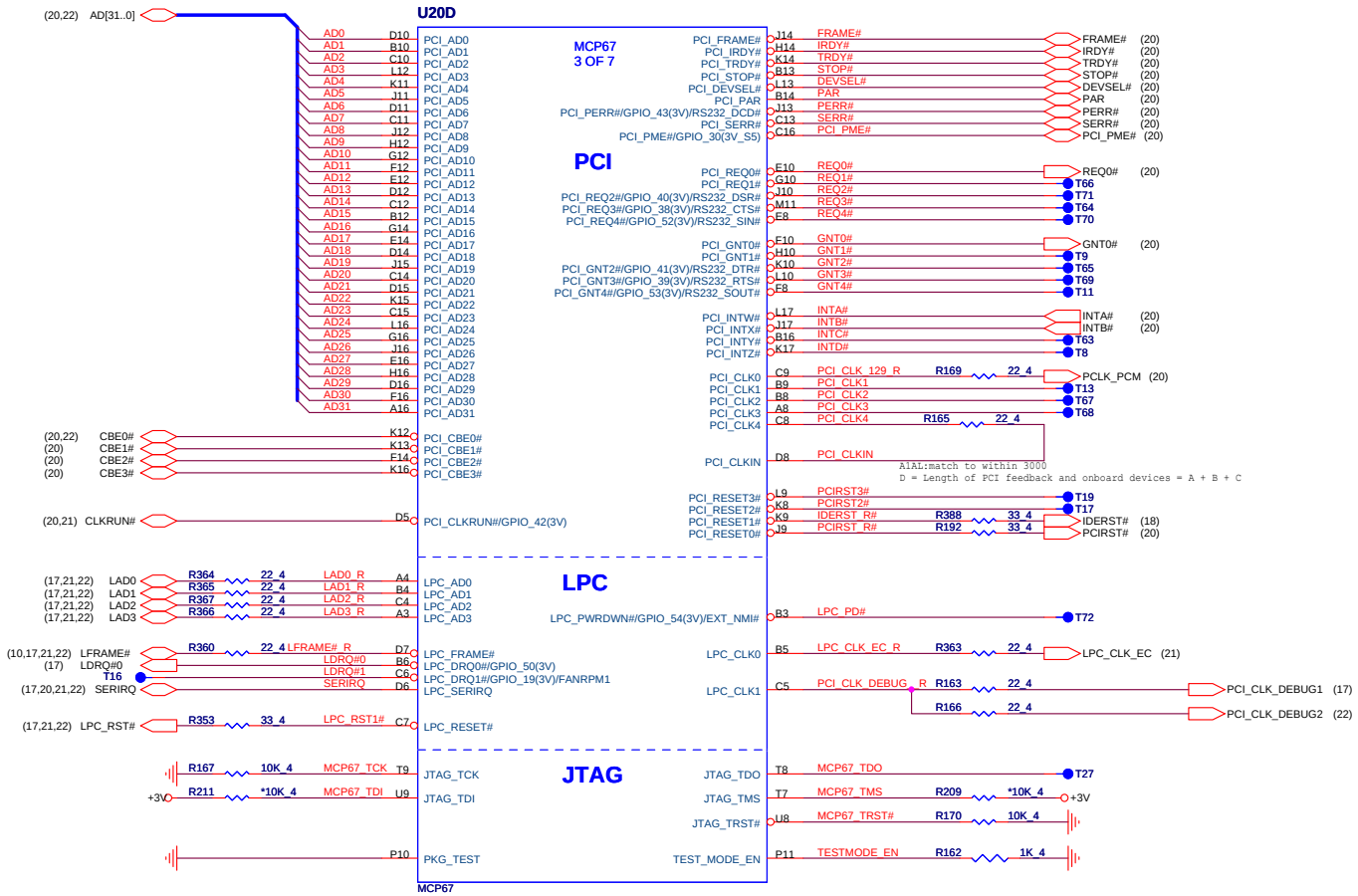
Datasheet error its should be +1.8 plane

PROJECT : ZO3
Quanta Computer Inc.

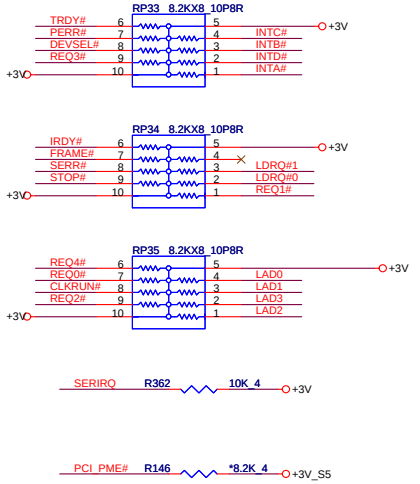
Size	Document Number	Rev
	MCP67(HT/VGA/FLAT_PANEL)	1A
Date: Wednesday, April 25, 2007	Sheet 7 of 30	



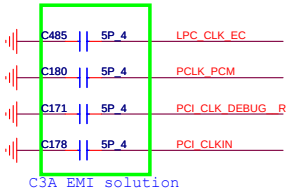
PROJECT : ZO3				
Quanta Computer Inc.				
Size	Document Number			Rev
	MCP67(PCI-E)			1A
Date:	Wednesday, April 25, 2007	Sheet	8 of	30



PCI/LPC PULL-UP

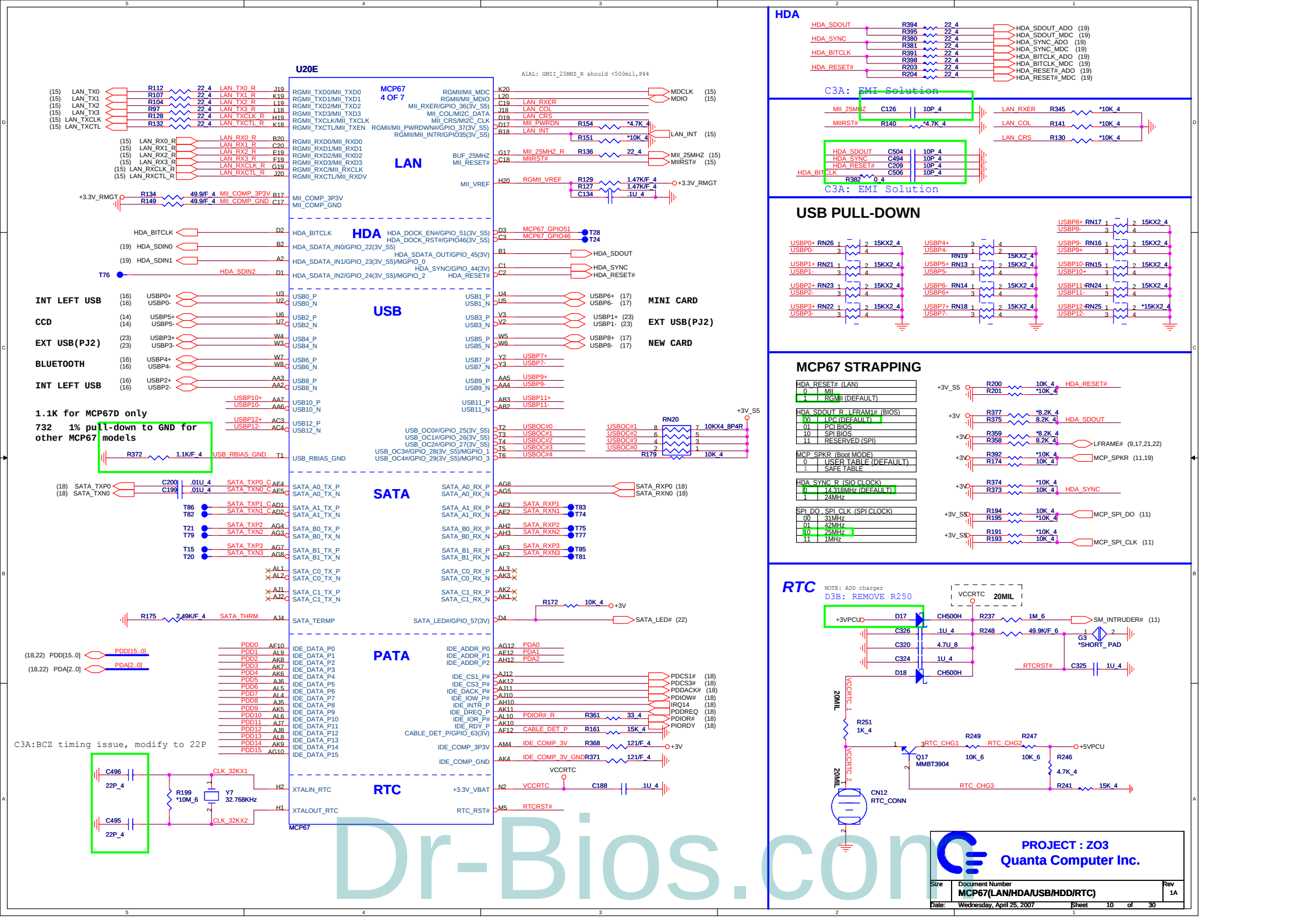


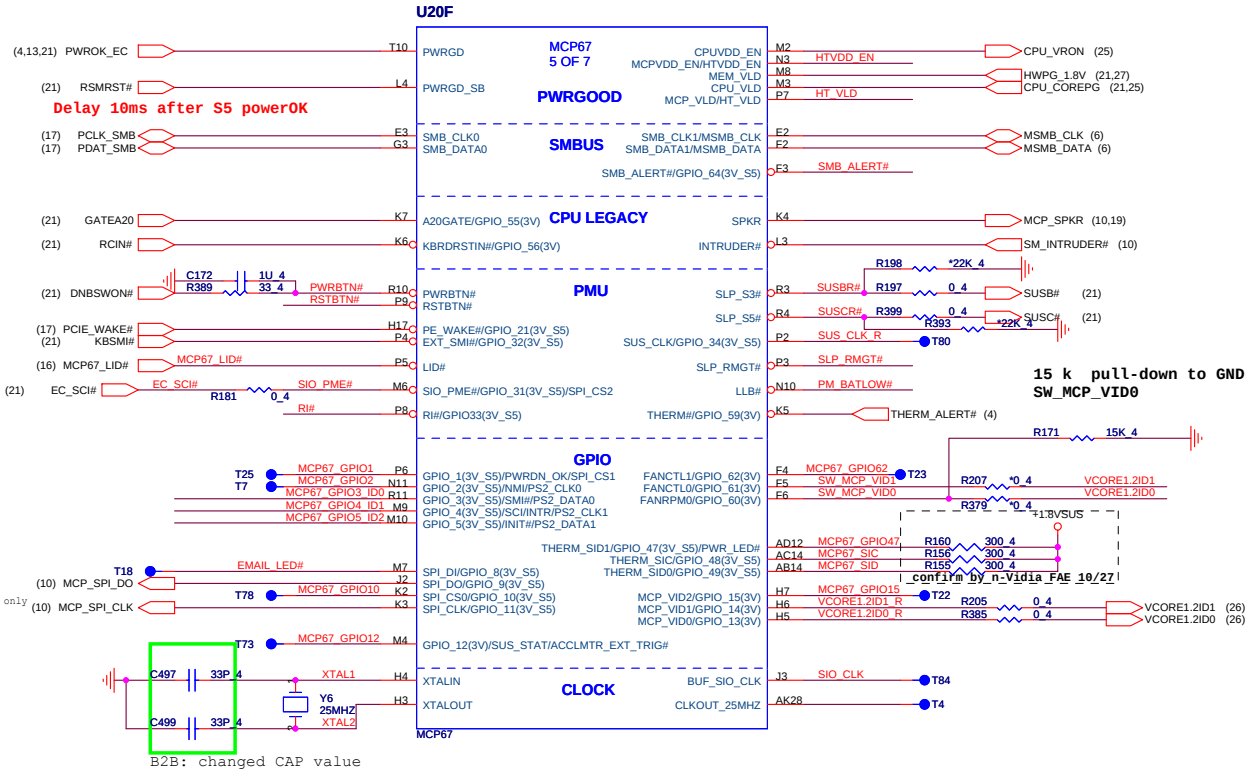
CLOCK BYPASS



PROJECT : ZO3
Quanta Computer Inc.

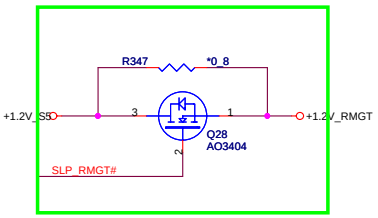
Size	Document Number	Rev
	MCP67(PCI/LPC/JTAG)	1A
Date: Wednesday, April 25, 2007	Sheet 9 of 30	


U20E
MCP67
4 OF 7
LAN
HDA
USB
SATA
PATA
RTC
MCP67
INT LEFT USB
CCD
EXT USB(PJ2)
BLUETOOTH
INT LEFT USB
MINI CARD
EXT USB(PJ2)
NEW CARD
1.1K for MCP67D only
732 1% pull-down to GND for other MCP67 models
C3A:BCZ timing issue, modify to 22P
HDA
C3A: EMI Solution
USB PULL-DOWN
MCP67 STRAPPING
RTC
NOTE: ADD charger
D3B: REMOVE R250
PROJECT : ZO3
Quanta Computer Inc.
MCP67(LAN/HDA/USB/HDD/RTC)
Wednesday, April 25, 2007
Dr-Bios.com

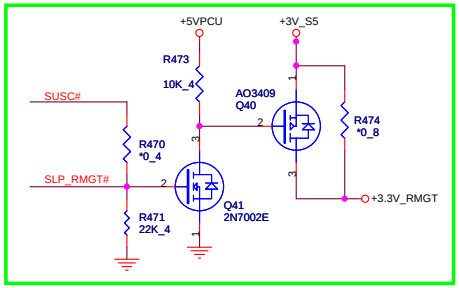


FOR SLEEP MODE CORE POWER CIRCIUT

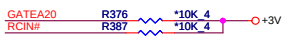
C3A: Mount Q28, unmount R347



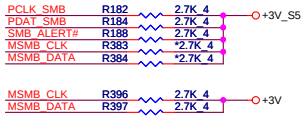
C3A: Mount Q40,Q41,R473,R471, unmount RR74



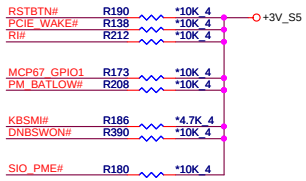
CPU LEGACY PULL-UP



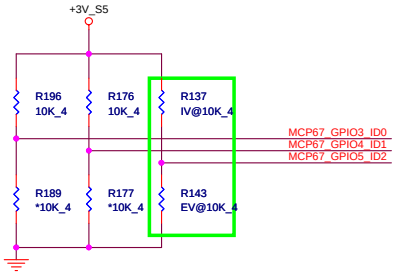
SMB/I2C PULL-UP



PMU PULL-UP

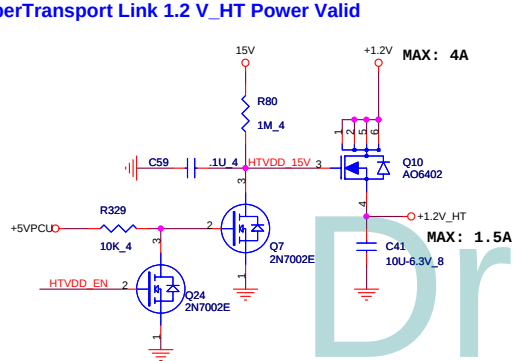


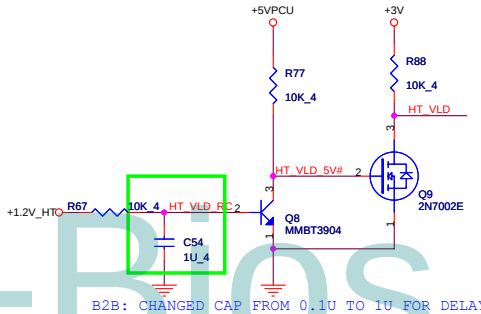
M/B ID for 14"/15"/17"



ID0	ID1	ID2	M/B
0	0	0	17" D
0	0	1	X
0	1	0	15" D
1	0	0	15" U
1	0	1	X
1	1	0	14" D
1	1	1	14" U

HyperTransport Link 1.2 V_HT Power Valid

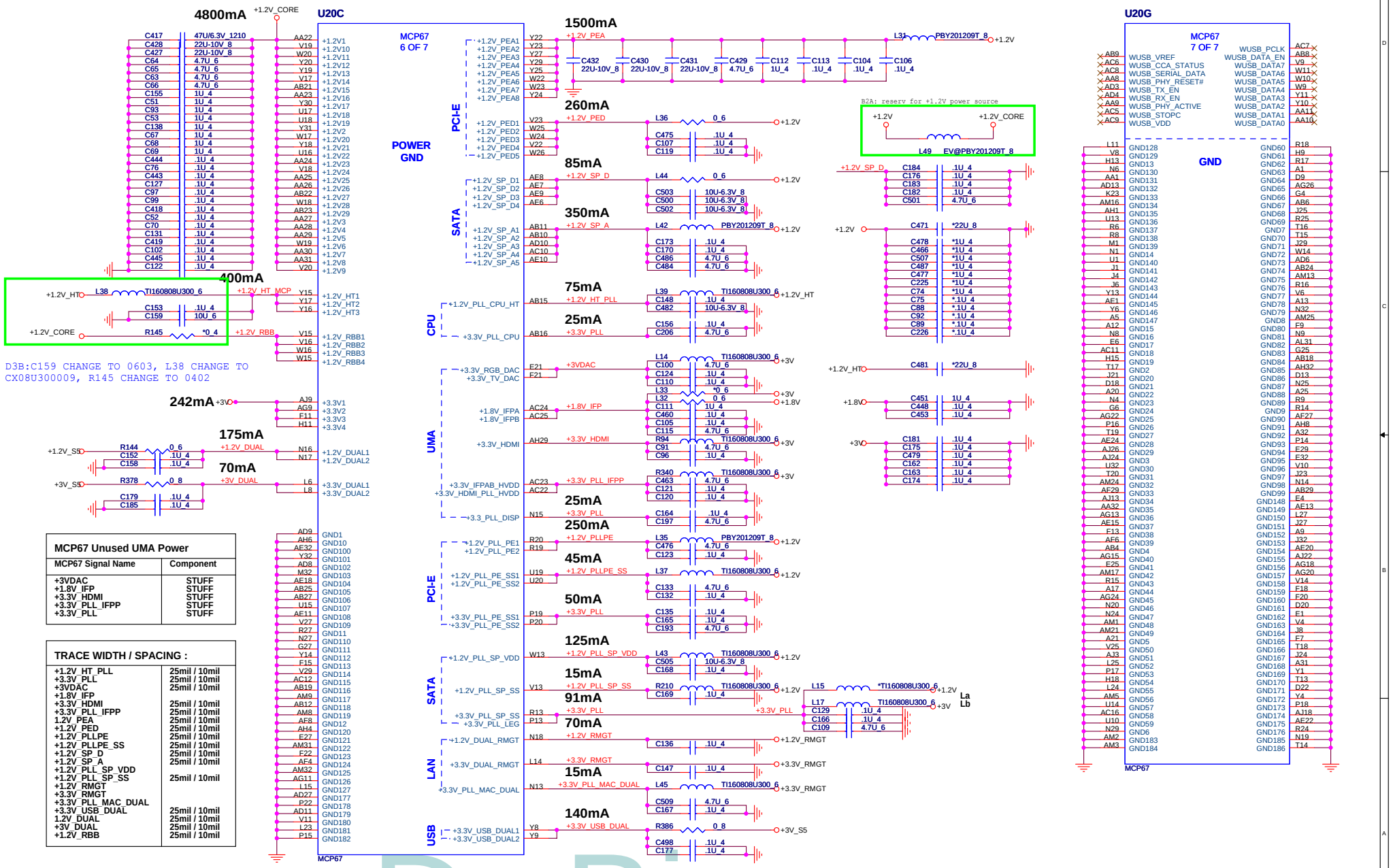




PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	MCP67(SMB/GPIO/CLK/PMU)	1A
Date: Wednesday, April 25, 2007	Sheet 11 of 30	

MCP67 POWER PLANE/GND & BYPASS

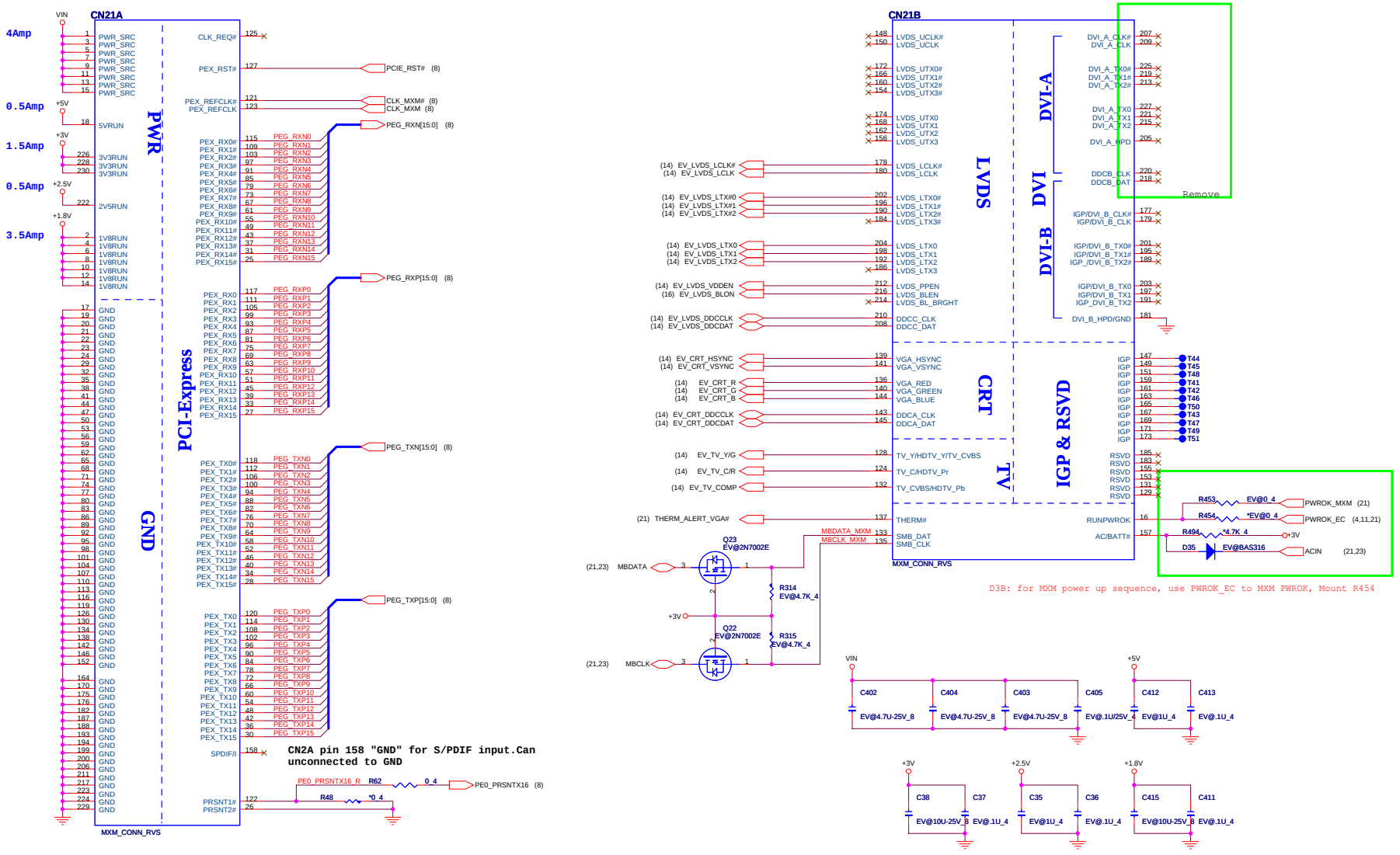


MCP67 Unused UMA Power	
MCP67 Signal Name	Component
+3VDAC	STUFF
+1.8V_IFP	STUFF
+3.3V_HDMI	STUFF
+3.3V_PLL_IFPP	STUFF
+3.3V_PLL	STUFF

TRACE WIDTH / SPACING :	
+1.2V_HT_PLL	25mil / 10mil
+3.3V_PLL	25mil / 10mil
+3VDAC	25mil / 10mil
+1.8V_IFP	
+3.3V_HDMI	25mil / 10mil
+3.3V_PLL_IFPP	25mil / 10mil
1.2V_PEA	25mil / 10mil
+1.2V_PED	25mil / 10mil
+1.2V_PLLPE	25mil / 10mil
+1.2V_PLLPE_SS	25mil / 10mil
+1.2V_SP_D	25mil / 10mil
+1.2V_SP_A	25mil / 10mil
+1.2V_PLL_SP_VDD	
+1.2V_PLL_SP_SS	25mil / 10mil
+1.2V_RMGT	
+3.3V_RMGT	
+3.3V_PLL_MAC_DUAL	
+3.3V_USB_DUAL	25mil / 10mil
1.2V_DUAL	25mil / 10mil
+3V_DUAL	25mil / 10mil
+1.2V_RBB	25mil / 10mil

PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	MCP67(POWER/GND)	1A
Date: Wednesday, April 25, 2007	Sheet 12 of 30	



PROJECT : ZO3		
Quanta Computer Inc.		
Size	Document Number: MXM	Rev: 1A
Date: Wednesday, April 25, 2007	Sheet 13 of 30	

LVDS

SINGLE_CH

Close MXM CONN

(7) INT_TXLCLKOUT-
(7) INT_TXLCLKOUT+
(7) INT_TXLOUT0-
(7) INT_TXLOUT0+
(7) INT_TXLOUT1-
(7) INT_TXLOUT1+
(7) INT_TXLOUT2-
(7) INT_TXLOUT2+
(13) EV_LVDS_LCLK#
(13) EV_LVDS_LCLK
(13) EV_LVDS_LTX#0
(13) EV_LVDS_LTX0
(13) EV_LVDS_LTX#1
(13) EV_LVDS_LTX1
(13) EV_LVDS_LTX#2
(13) EV_LVDS_LTX2

IV@0X2_4 RN9 TXLCLKOUT- TXLCLKOUT+
IV@0X2_4 RN12 TXLOUT0- TXLOUT0+
IV@0X2_4 RN11 TXLOUT1- TXLOUT1+
IV@0X2_4 RN10 TXLOUT2- TXLOUT2+
EV@0X2_4 RN4
EV@0X2_4 RN7
EV@0X2_4 RN6
EV@0X2_4 RN5

Edison-- 1025 Modify the LVDS pin difinition

CN4
CON30X2_0

TXLOUT0+ TXLOUT0- TXLOUT1+ TXLOUT1- TXLOUT2+ TXLOUT2- TXLCLKOUT+ TXLCLKOUT-
LCD_EDIDCLK LCD_EDIDDATA VIN_LCD BL_ON BRIGHTNESS LCD_VCC CCD_PWR
BL_ON (16)
C23 .1U_4
+3V
(10) USBP5-
(10) USBP5+

BRIGHTNESS R18 *0_6 R19 0_6 L_BKLT_CTRL (7) EC_L_BKLT_CTRL (21)

VIN R20 0_8 VIN_LCD
C18 1000P-25V_4
4.7U-25V_8 C21

+3V
R321 2.2K_4
(13) EV_LVDS_DDCCLK R322 EV@0_4 LCD_EDIDCLK
(7) INT_LVDS_EDIDCLK R326 IV@0_4
R324 2.2K_4
(13) EV_LVDS_DDCDAT R323 EV@0_4 LCD_EDIDDATA
(7) INT_LVDS_EDIDDATA R327 IV@0_4

LCD POWER

Close to CONN CN3

+3V
C24 1U_4
U4
AAT4280
IN IN ON/OFF OUT GND GND
LCDVCC_1 R21 0_8 LCD_VCC
C26 .1U_4
C25 10U-6.3V_8
C27 .1U_4
C20 .01U_4
C22 10U-6.3V_8

(7) INT_LVDS_DIGON R16 IV@0_4 DISP_ON
(13) EV_LVDS_VDDEN R15 EV@0_4
R17 IV@10K_4

<demo circuit>
Crestline suggest 100K
G73 suggest 10K(ZS1 Default)

Unstuff R275 for EV_LVDS_VDDEN signal

CAMERA MODULE POWER

+3V CCD_PWR
R497 0_8
Q4 *AO3413
C17 10U-6.3V_8
C19 1000P_4
R14 *4.7K_4
Q3 *DTC144EU
CCD_POWERON (21)

BECUASE UR'S SUGGESTION,
ACTICE CHANGE FROM LOW TO HIGH.
Confirm by Joms

B2A: unstuff Q4, mount R497 for saving Q4

CRT

Close MXM CONN

(13) EV_CRT_R
(13) EV_CRT_G
(13) EV_CRT_B
(13) EV_CRT_HSYNC
(13) EV_CRT_VSYNC
(13) EV_CRT_DDCCLK
(13) EV_CRT_DDCDAT
(7) INT_CRT_RED
(7) INT_CRT_GRN
(7) INT_CRT_BLU
(7) INT_HSYNC
(7) INT_VSYNC
(7) INT_CRT_DDCCLK
(7) INT_CRT_DDCDAT

R42 EV@0_4 SYS_VGA_RED
R43 EV@0_4 SYS_VGA_GRN
R44 EV@0_4 SYS_VGA_BLU
R36 EV@0_4 HSYNC
R38 EV@0_4 VSYNC
R34 EV@0_4 CRTDCLK
R35 EV@0_4 CRTDDAT
R45 IV@0_4
R46 IV@0_4
R47 IV@0_4
R37 IV@0_4
R39 IV@0_4
R40 IV@0_4
R41 IV@0_4

+5V D3 1N5819HW CRTVDD5
R13 150/F_4 R12 150/F_4 R10 150/F_4
C14 10P_4 C11 10P_4 C9 10P_4
C8 10P_4 C10 10P_4 C15 10P_4
L7 BK1608LL680_6 CRT_R1
L6 BK1608LL680_6 CRT_G1
L5 BK1608LL680_6 CRT_B1

CN18
CRT_CONN
DDCDAT_1
CRTHSYNC
CRTVSYNC
DDCCLK_1

C3A: Add C9,C11,C14 for EMI solution

R3 0_4 CRT_SENSE# (21)

CRTVDD5 .1U_4 C5
CRTVSYNC *10P_4 C6
CRTHSYNC *10P_4 C7
DDCCLK_1 10P_4 C3
DDCDAT_1 10P_4 C12

+5V C4 1U_4 C13 .22U_6 CRTVDD5
+3V C16 1U_4
U3
CM2009
VCC_SYNC SYNC_OUT2 SYNC_OUT1 VCC_DDC BYP VCC_VIDEO SYNC_IN2 SYNC_IN1 VIDEO_1 VIDEO_2 VIDEO_3 GND DDC_IN1 DDC_IN2 DDC_OUT1 DDC_OUT2
SYS_VGA_RED SYS_VGA_GRN SYS_VGA_BLU
VSYNC1 L3 BLM18BA220SN1_6 CRTVSYNC
HSYNC1 L4 BLM18BA220SN1_6 CRTHSYNC
VSYNC HSYNC
CRTDCLK CRTDDAT
R9 2.7K_4 R8 2.7K_4
R11 2.7K_4 R7 2.7K_4
DDCCLK_1 DDCDAT_1

TV Out (SVHS) MiniDIN 7-pin

D3B: Change L8,L9,L10 P/N

(13) EV_TV_Y/G
(13) EV_TV_C/R
(13) EV_TV_COMP
(7) INT_TV_Y/G
(7) INT_TV_C/R
(7) INT_TV_COMP

R50 EV@0_4 SYS_TV_Y/G
R49 EV@0_4 SYS_TV_C/R
R51 EV@0_4 SYS_TV_COMP
R53 IV@0_4
R52 IV@0_4
R54 IV@0_4

CN20
S_VIDEO
SYS_TV_C/R L10 BK1608LL680_6 TV-CHROMA
R33 150/F_4 C33 6P_4 C34 6P_4
TV-LUMA L9 BK1608LL680_6 SYS_TV_Y/G
C31 6P_4 C32 6P_4 R32 150/F_4
TV-COMP L8 BK1608LL680_6 SYS_TV_COMP
C28 6P_4 C29 6P_4 R27 150/F_4

Remove HDMI

ESD Protect

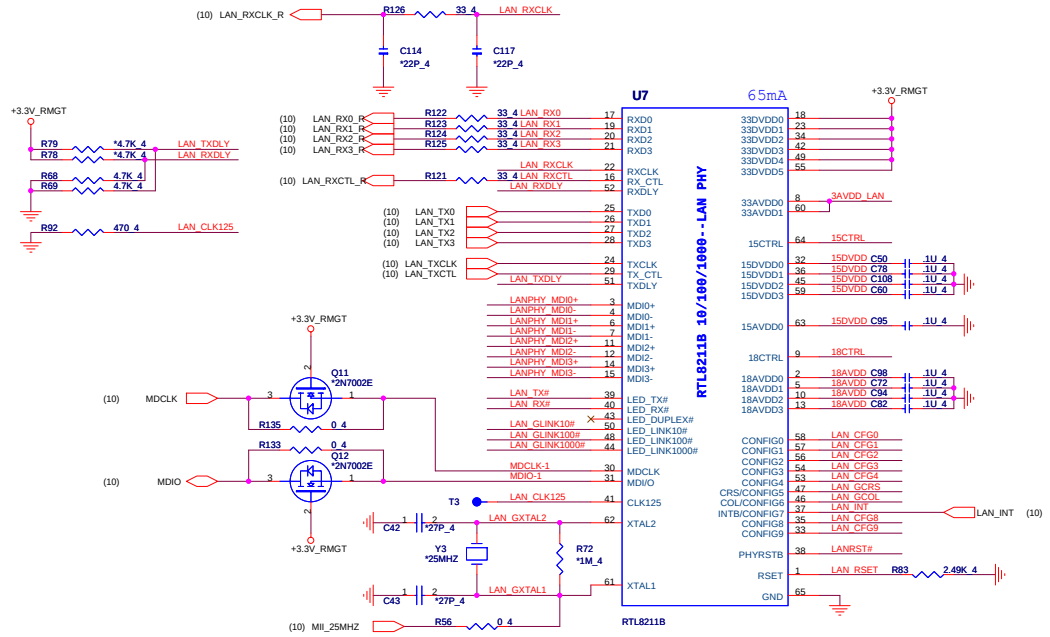
+3V D7 TV-COMP *DA204U
+3V D9 TV-CHROMA *DA204U
+3V D8 TV-LUMA *DA204U

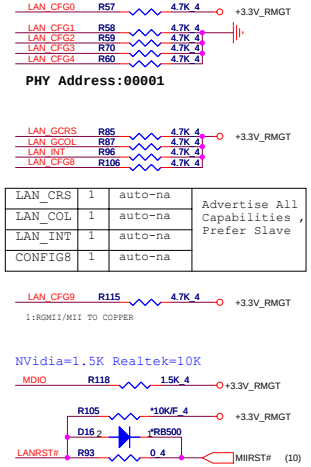
PROJECT : ZO3
Quanta Computer Inc.

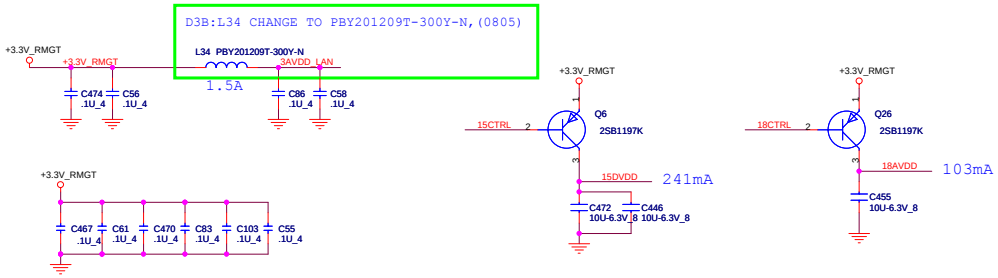
Size	Document Number	Rev
	LVDS/CRT/TV-OUT/HDMI	1A

Date: Wednesday, April 25, 2007 Sheet 14 of 30

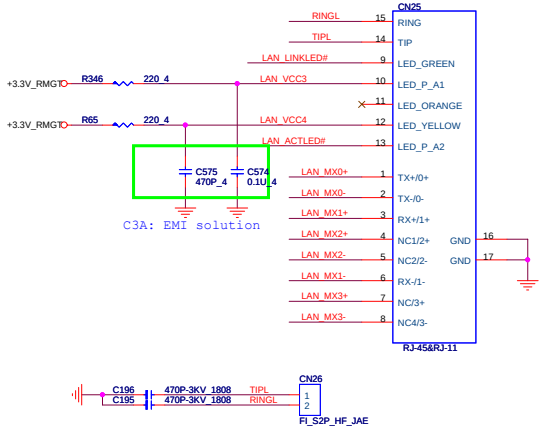
LAN



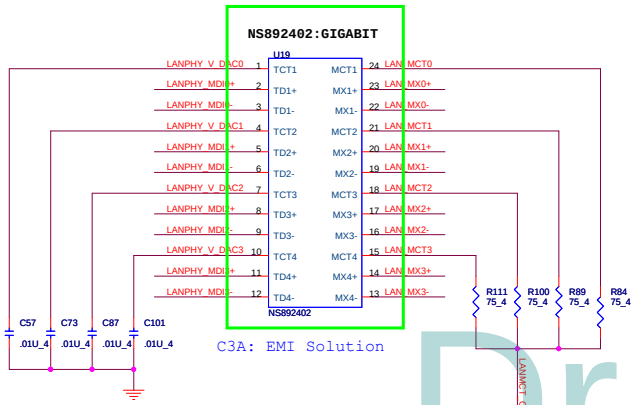




RJ45-11

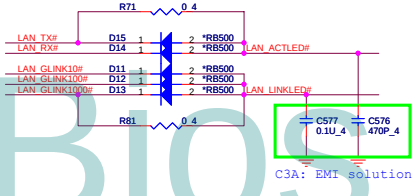


Transformer



LED Configuration

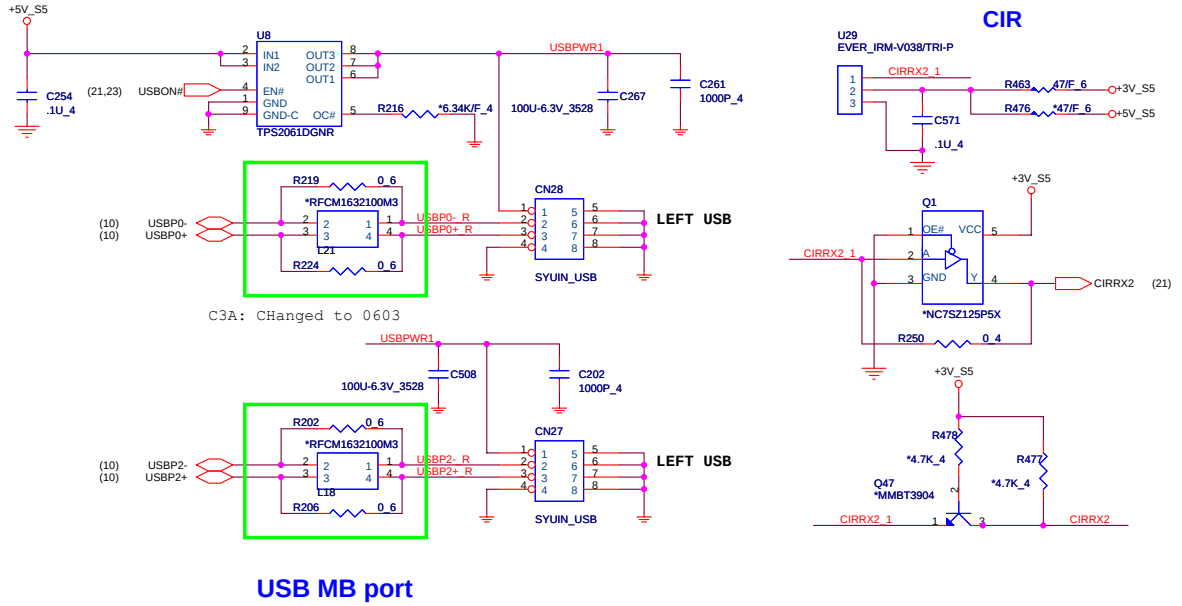
	Set Register 24 Control Bit=1
LED_LINK1000	LOW=LINK UP (ANY SPEED)
LED_TX	BLINKING=TRANSMITTING OR RECEIVING

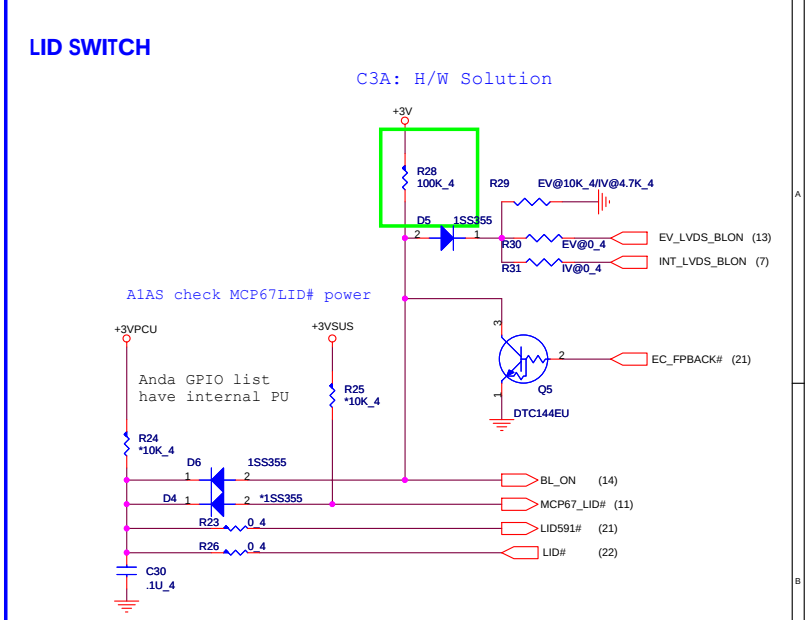


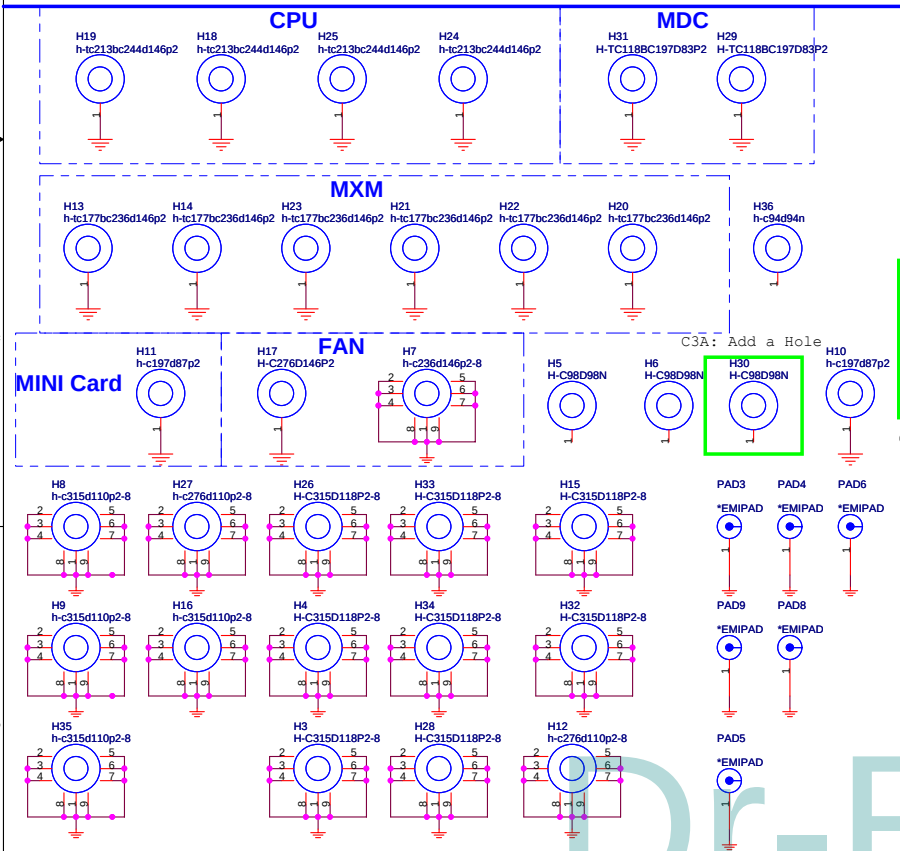
PROJECT : ZO3
Quanta Computer Inc.

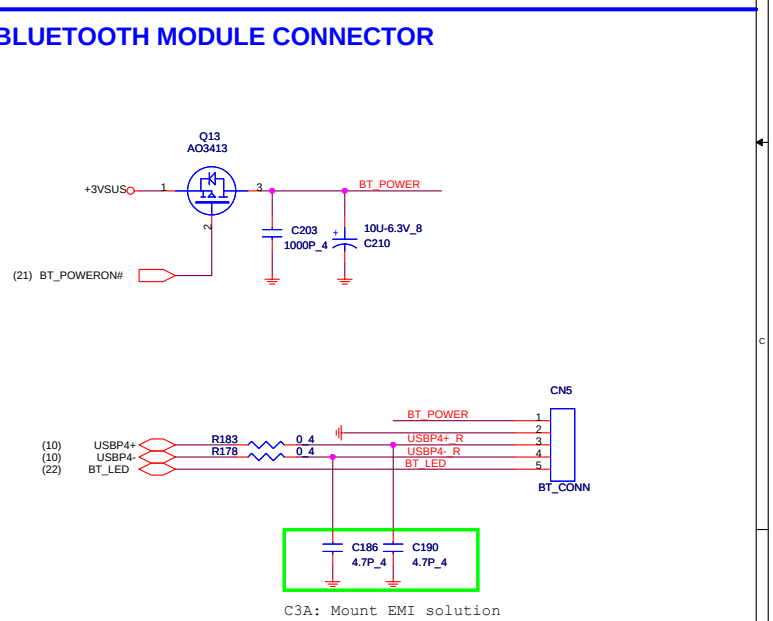
Size	Document Number	Rev
	RTL8211B (GigaLAN)	1A

Date: Wednesday, April 25, 2007 Sheet 15 of 30





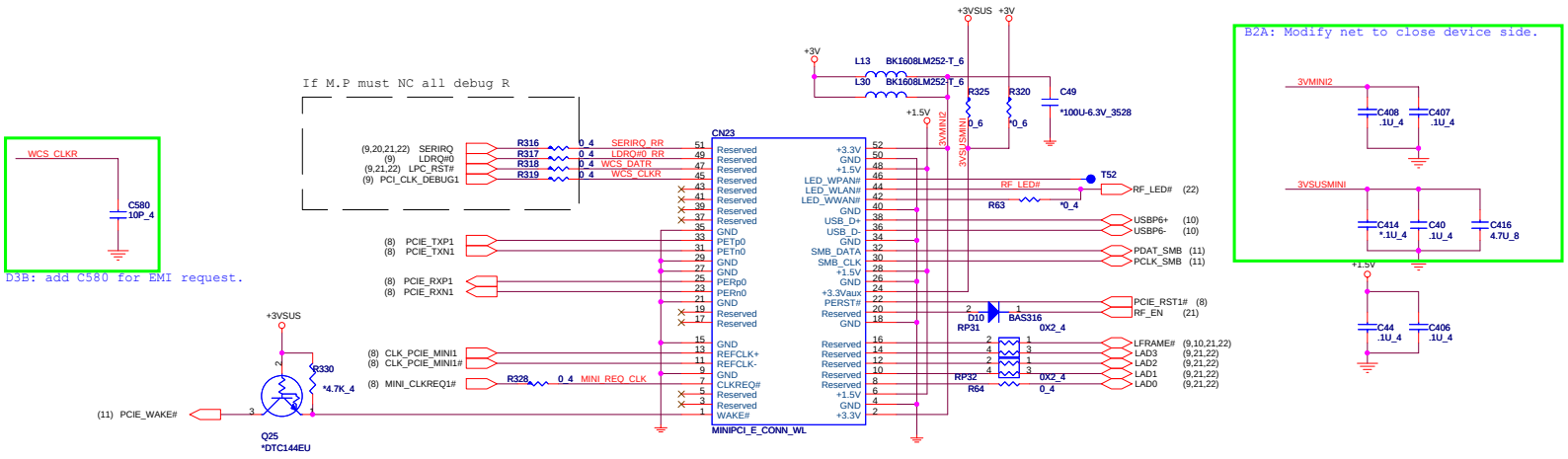




PROJECT : ZO3
Quanta Computer Inc.

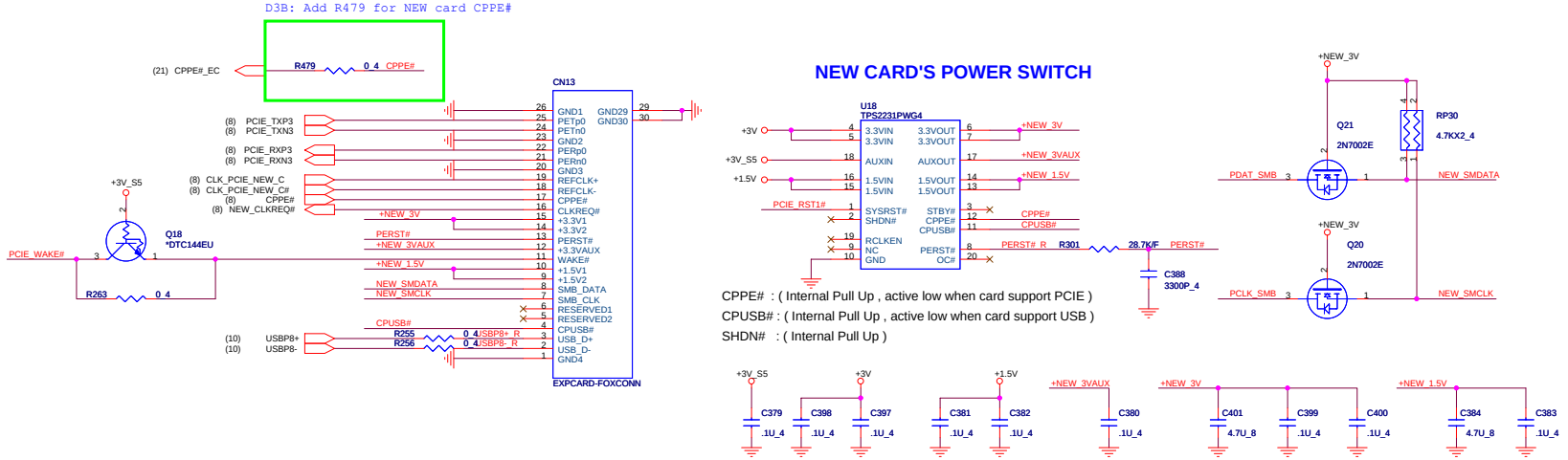
Size	Document Number	Rev
	USB/BLUETOOTH/CCD/CIR	1A
Date: Wednesday, April 25, 2007	Sheet 16 of 30	

MINI-Card



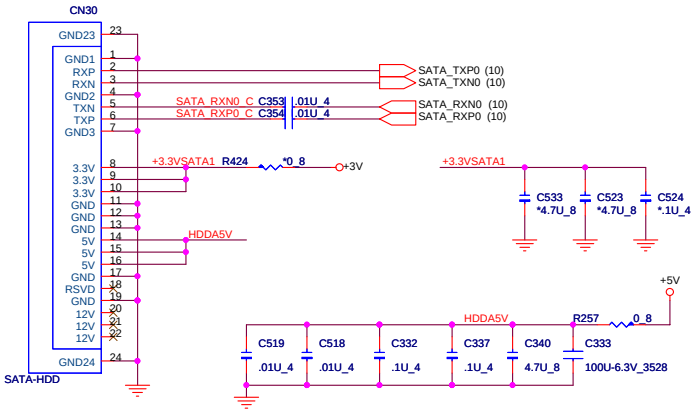
Need reserve 3G pin define
Check Footprint

New card

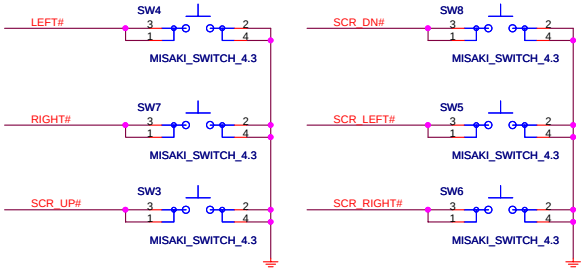


PROJECT : ZO3		
Quanta Computer Inc.		
Size	Document Number: MINI PCI-E card & NEW CARD	Rev: 1A
Date: Wednesday, April 25, 2007	Sheet 17 of 30	

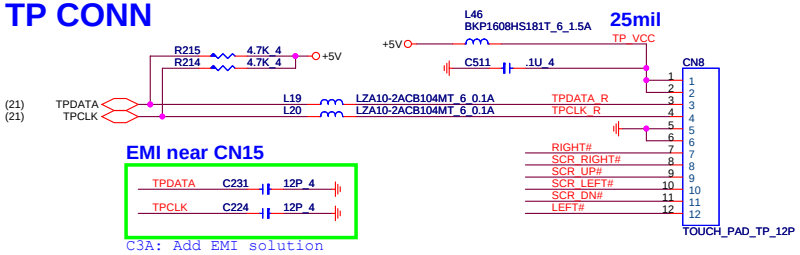
SATA HDD1



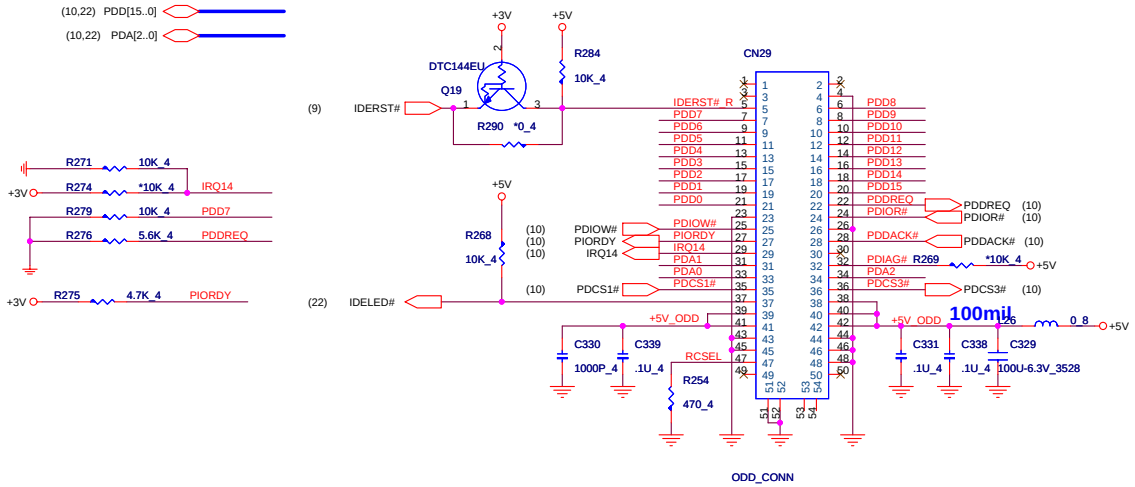
TP SWITCH



TP CONN



ODD (PATA)

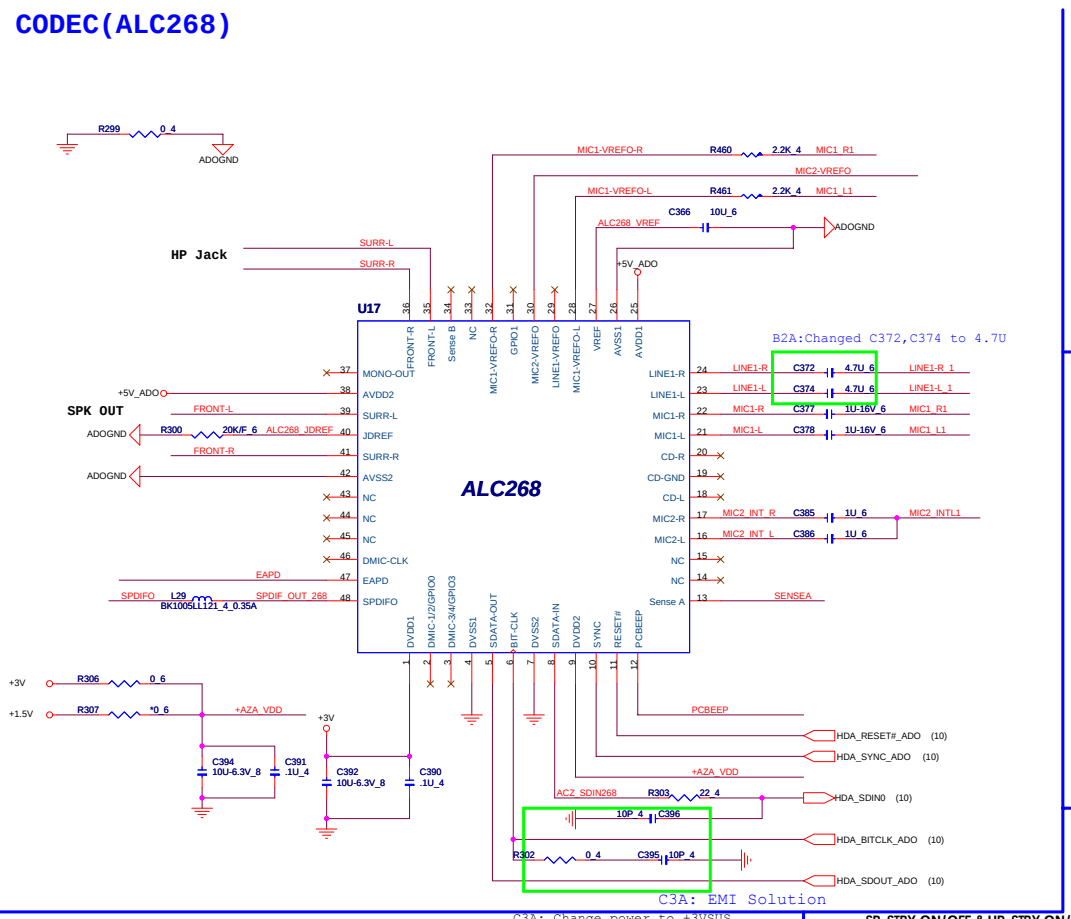


PROJECT : ZO3
Quanta Computer Inc.

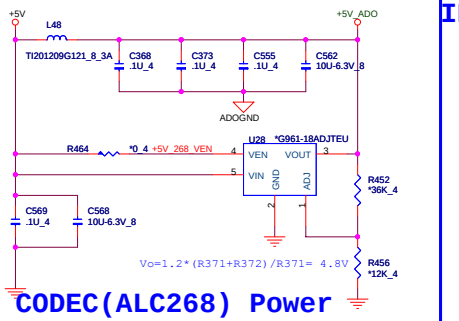
Size	Document Number	Rev
	SATA-HDD & PATA-ODD	1A

Date: Wednesday, April 25, 2007 Sheet 18 of 30

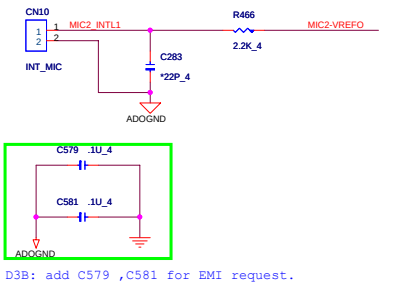
CODEC(ALC268)

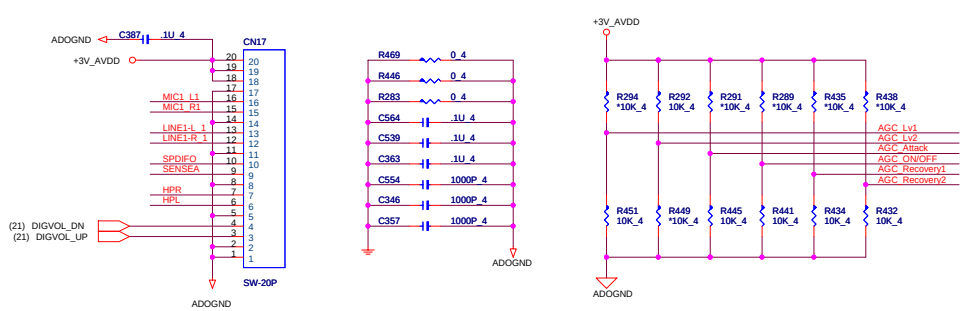


CODEC(ALC268) Power



INT MIC array





AGC-attack-time selection

AGC_Attack (4 pin)	Attack time
LOW	1 ms
Hi	2 ms

AGC ON/OFF selection

AGC_ON/OFF (6 pin)	AGC ON/OFF
LOW	ON
Hi	OFF

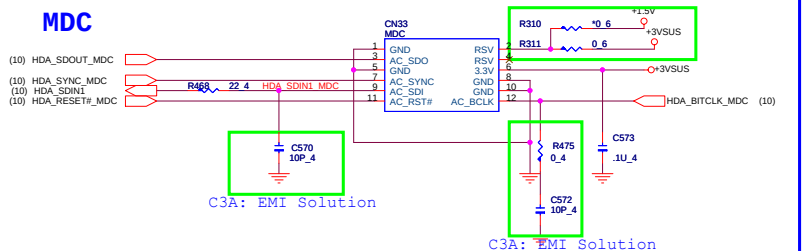
AGC-recovery-time selection

AGC_Recovery1 (10 pin)	AGC_Recovery2 (11 pin)	Recovery Time
LOW	LOW	1.0 s
LOW	Hi	2.0 s
Hi	LOW	4.0 s
Hi	Hi	8.0 s

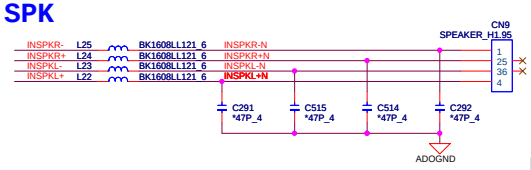
AGC-on-level selection

AGC_Lv1 (2 pin)	AGC_Lv2 (3 pin)	AGC ON Level	Output Po (RL=8 ohm)
LOW	LOW	9.8 dBV	1.2 W
LOW	Hi	9.0 dBV	1.0 W
Hi	LOW	8.1 dBV	0.8 W
Hi	Hi	6.0 dBV	0.5 W

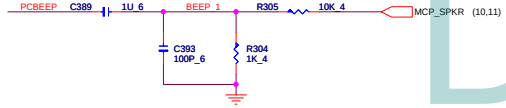
MDC



SPK



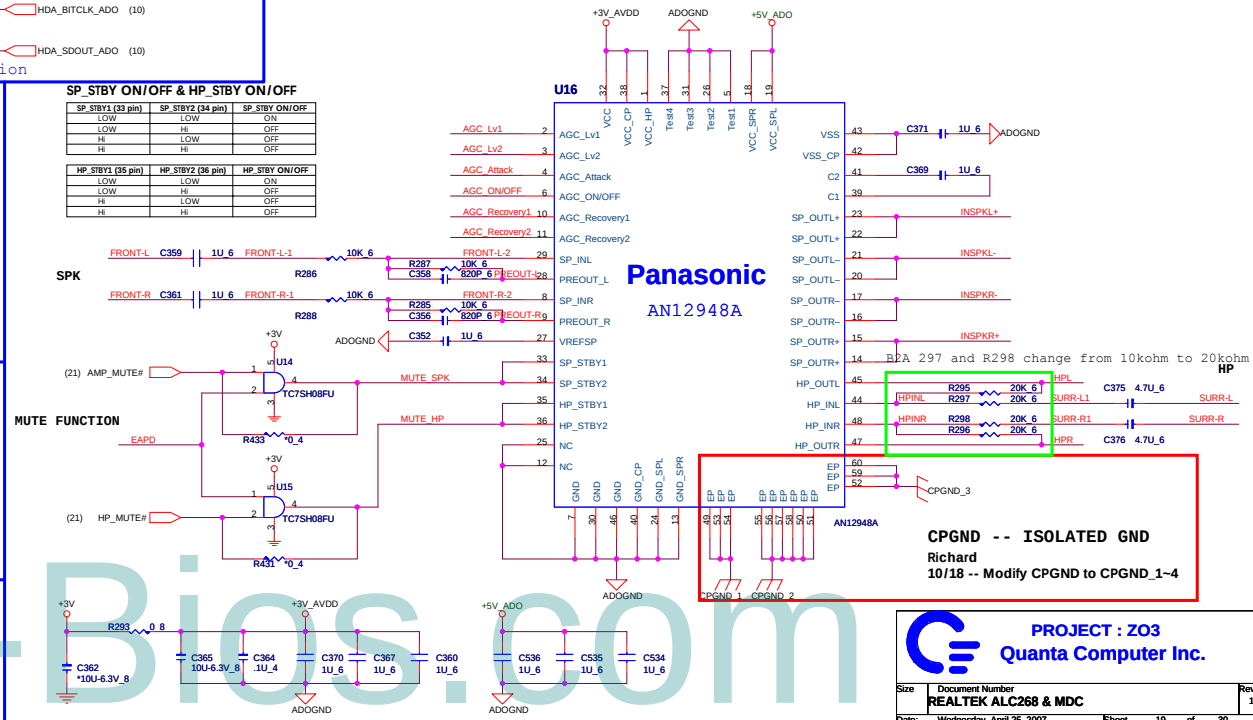
Beep



SP_STBY ON/OFF & HP_STBY ON/OFF

SP_STBY1 (33 pin)	SP_STBY2 (34 pin)	SP_STBY ON/OFF
LOW	LOW	ON
LOW	Hi	OFF
Hi	LOW	OFF
Hi	Hi	OFF

HP_STBY1 (35 pin)	HP_STBY2 (36 pin)	HP_STBY ON/OFF
LOW	LOW	ON
LOW	Hi	OFF
Hi	LOW	OFF
Hi	Hi	OFF



PROJECT : ZO3		
Quanta Computer Inc.		
Size	Document Number: REALTEK ALC268 & MDC	Rev: 1A
Date: Wednesday, April 25, 2007	Sheet 19 of 30	

R5C832 : AJ5C8320H26
R5C833 : AJ5C8330H05

U26B

PCI / OTHER

U26A

IEEE1394/SD

R5C832T_V00

R5C833T_V00

5 IN 1 CARD READER

CARD_READER_TTN_R013-B10-XX-C

CARDREADER POWER

30mil

*G5241T1U

PROCONN-MXP038-A0-4010-NB4

Reserve MS DUO card issue

1394

EEPROM

* NOT Use EEPROM :
R4063 : installed
R4064,U38,C4106 : NOT installed
* Use EEPROM :
R4064,U38,C4106 : installed
R4063 : NOT installed

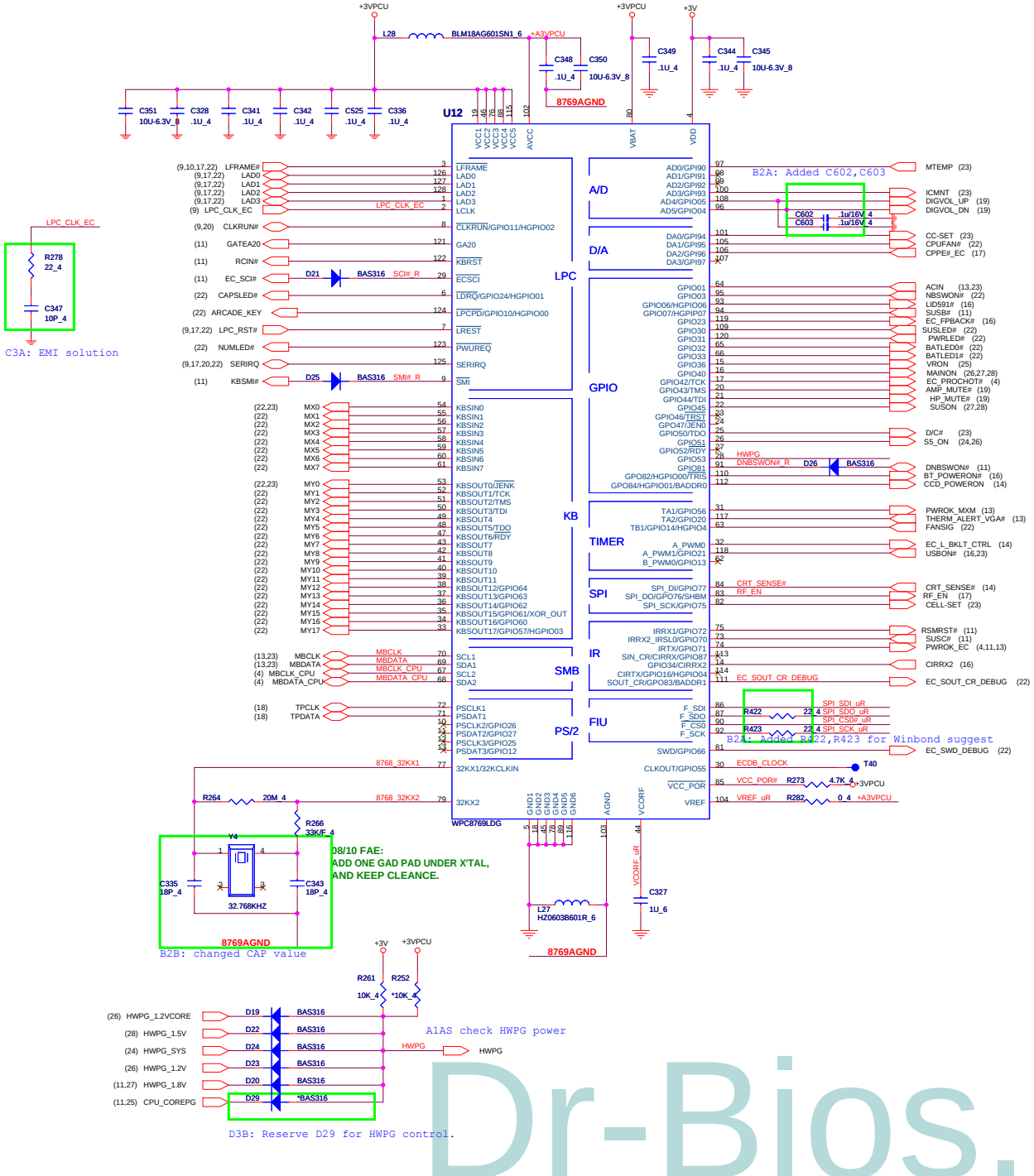
B2A: Remove U27,C594

PROJECT : Z03
Quanta Computer Inc.

Size | Document Number R5C832/833(5IN1/1394) | Rev 1A

Date: Wednesday, April 25, 2007 | Sheet 20 of 30

WPC8769LDG



I/O ADDRESS SETTING

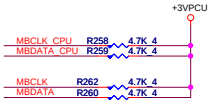
	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

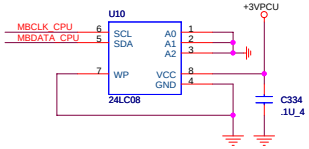
BADDR0 — CCD_POWERON — R281 10K_4
BADDR1 — EC_SOUT_CR_DEBUG — R280 *10K_4
SHBM — RF_EN — R270 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

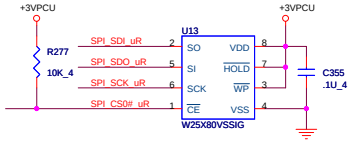
SMBUS PULL-UP



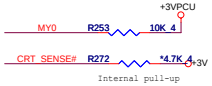
ACER ID



SPI FLASH



INTERNAL KEYBOARD STRIP SET



PROJECT : Z03			
Quanta Computer Inc.			
Size	Document Number		Rev
	PC8769L & FLASH		1A
Date:	Wednesday, April 25, 2007	Sheet 21 of 30	

INT K/B

(21,23) MY[17..0]
(21,23) MX[7..0]

CN7

FFC_26P_KB

+3VSUS

RP36
10KX8_10P8R

CA6 *220P-50V_8P4CCA7 *220P-50V_8P4C
CA3 *220P-50V_8P4CCA5 *220P-50V_8P4C
CA4 *220P-50V_8P4CCA8 *220P-50V_8P4C
CA9 *220P-50V_8P4C

LED

10/16:Changed. Follow BL3 LED

+3VPCU
R309 330_4 PWRLED#-R
R308 330_4 SUSLED#-R
LED6 LED_G/Y_LTST-C155KGJSKT
R313 330_4 BATLED0# (21)
R312 330_4 BATLED1# (21)
LED7 LED_G/Y_LTST-C155KGJSKT

(21) CAPSLED# CAPSLED# R5 330_4 +3V
LED5 LED_G_UP

(21) NUMLED# NUMLED# R4 330_4 +3V
LED4 LED_G_UP

IDE_LED# R6 330_4 +3V
LED3 LED_G_UP

Q43 2N7002E
PWRLED#-R
Q44 2N7002E
R455 10K_4
+3V
(21) PWRLED#

Q42 2N7002E
SUSLED#-R
Q46 2N7002E
R462 10K_4
+3VSUS
(21) SUSLED#

C3A: Modify LED control behavior

CPU FAN

+3V
R55 10K_4
(21) FANSIG
CN24
+5V
U6
VIN VO
/FON GND
VSET GND
G995
(4) CPUFAN#_ON
(21) CPUFAN#
TH_FAN_POWER
C410 10U-6.3V
C409 8.01U_4
C39 *.01U_4
FAN_CONN

FANPWR = 1.6*VSET

DEBUG PORT

EC Debug Port

+3VPCU
CN16
(21) EC_SOUT_CR_DEBUG
(21) EC_SWD_DEBUG
*INT_SPK

Reserved for LPC debug card

+3V
CN11
(9,17,21) LAD0
(9,17,21) LAD1
(9,17,21) LAD2
(9,17,21) LAD3
(9) PCI_CLK_DEBUG2
(9,10,17,21) LFRAME#
(9,17,21) LPC_RST#
(9,17,20,21) SERIRQ
*WTB_10P

Button

BUTTON MATRIX

	MY0
MX1	MAIL
MX2	WWW
MX4	WIRELESS
MX5	BLUETOOTH

+3VPCU +3V
CN3
(21) ARCADE_KEY
(17) RF_LED#
(16) BT_LED
(21) NBSWON#
SUSLED#-R
PWRLED#-R
SW-20P

R22 330_4 +3VPCU
LID#
MR3
MRSS23E_NEC
C578 1U_4
D3B: add C578

+3V +3V
R267 10K_4
R265 10K_4
(18) IDELED#
(10) SATA_LED#
IDE_LED#
U11
TC7SH08FU

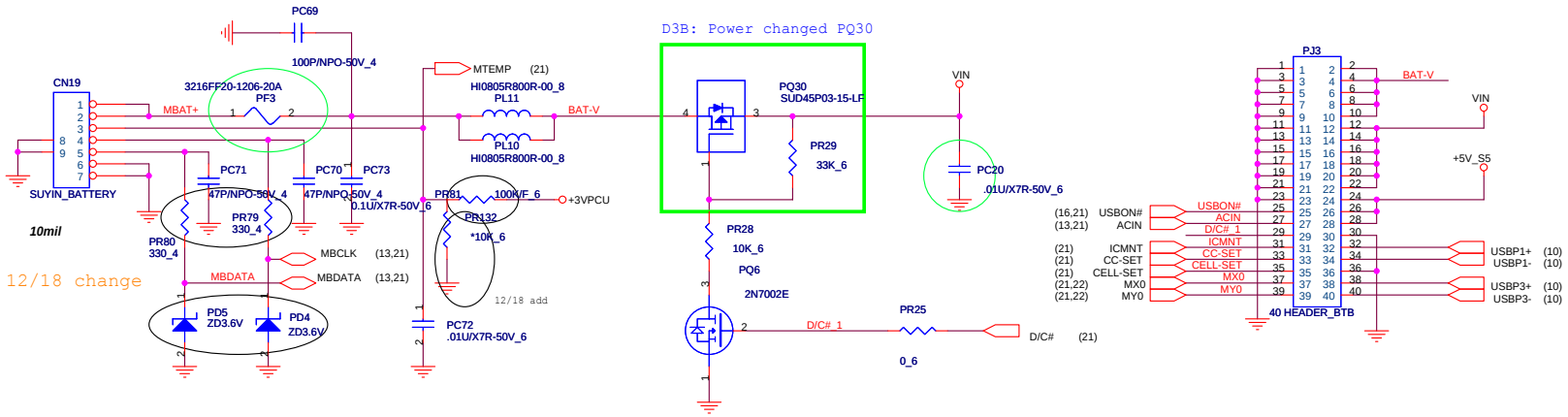
Debug

(9,20) AD[31..0]
(10,18) PDD[15..0]

CN15 *AMP_2-767004-2
(9,20) CBE0#
R420 0_4

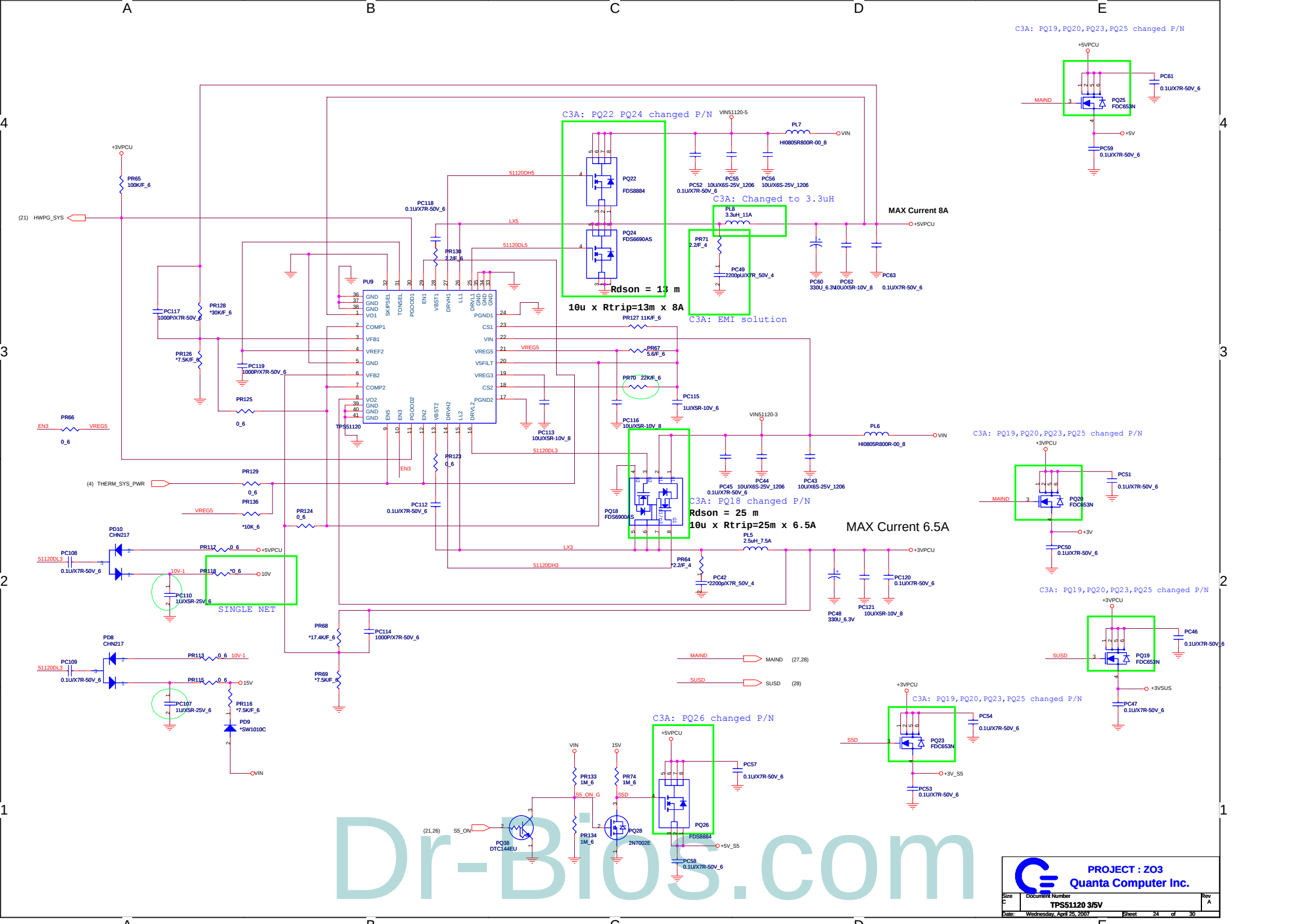
CN14 *AMP_2-767004-2
(10,18) PDA0
(16)

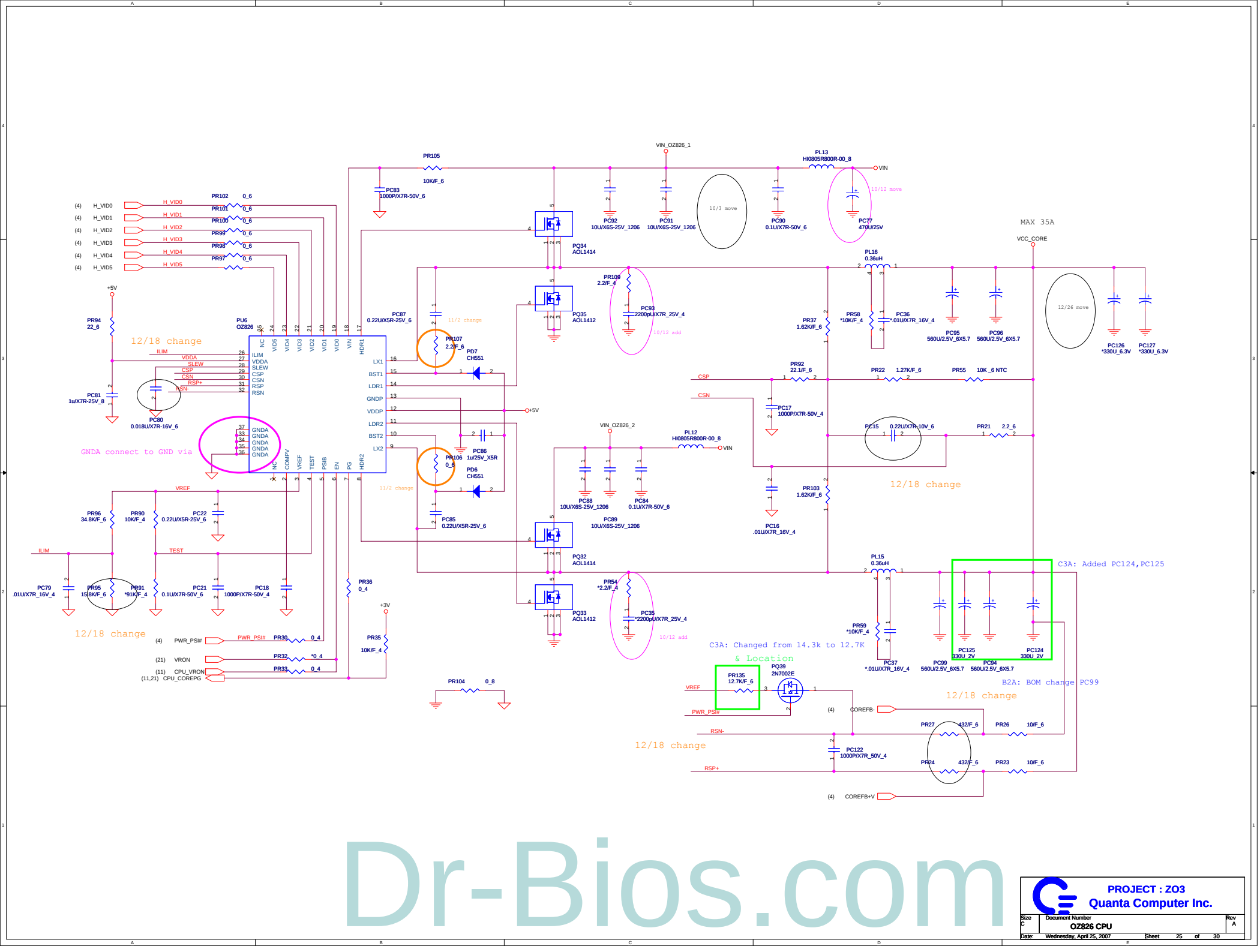
PROJECT : ZO3		
Quanta Computer Inc.		
Size	Document Number: FAN,SWITCH,LED,KB,DEBUG PORT,TP	Rev 1A
Date: Wednesday, April 25, 2007	Sheet 22 of 30	



CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S

PROJECT : ZO3		
Quanta Computer Inc.		
Size: Custom	Document Number: ISL6251 CHARGER	Rev: A
Date: Wednesday, April 25, 2007	Sheet 23 of 30	


C3A: PQ22 PQ24 changed P/N
Rdson = 13 m
10u x Rtrip=13m x 8A
C3A: Changed to 3.3uH
MAX Current 8A
C3A: EMI solution
C3A: PQ18 changed P/N
Rdson = 25 m
10u x Rtrip=25m x 6.5A
MAX Current 6.5A
SINGLE NET
C3A: PQ26 changed P/N
C3A: PQ19,PQ20,PQ23,PQ25 changed P/N
TPS51120
PROJECT : ZO3
Quanta Computer Inc.
TPS51120 3/5V
Wednesday, April 25, 2007



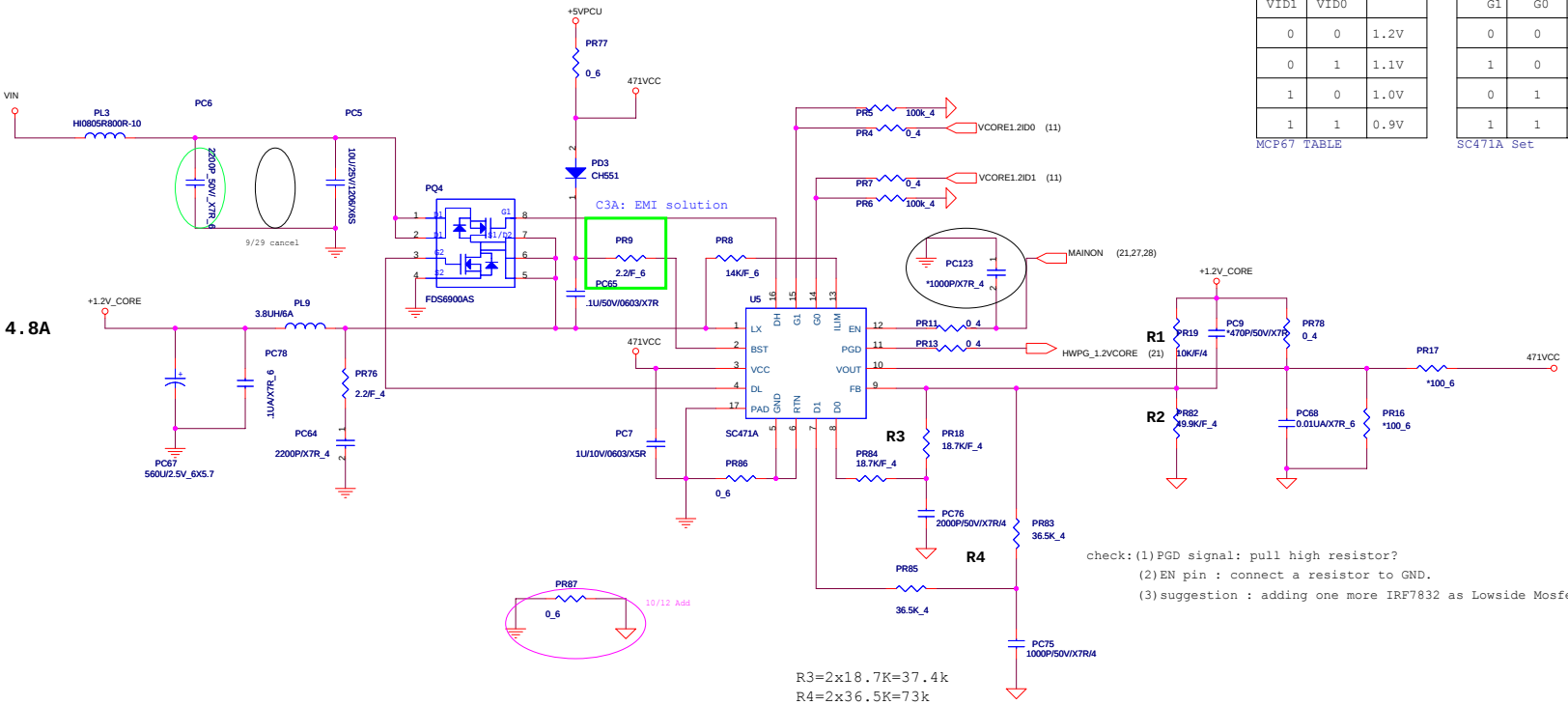
PROJECT : ZO3		
Quanta Computer Inc.		
Size: C	Document Number: OZ826 CPU	Rev: A
Date: Wednesday, April 25, 2007	Sheet 25 of 30	

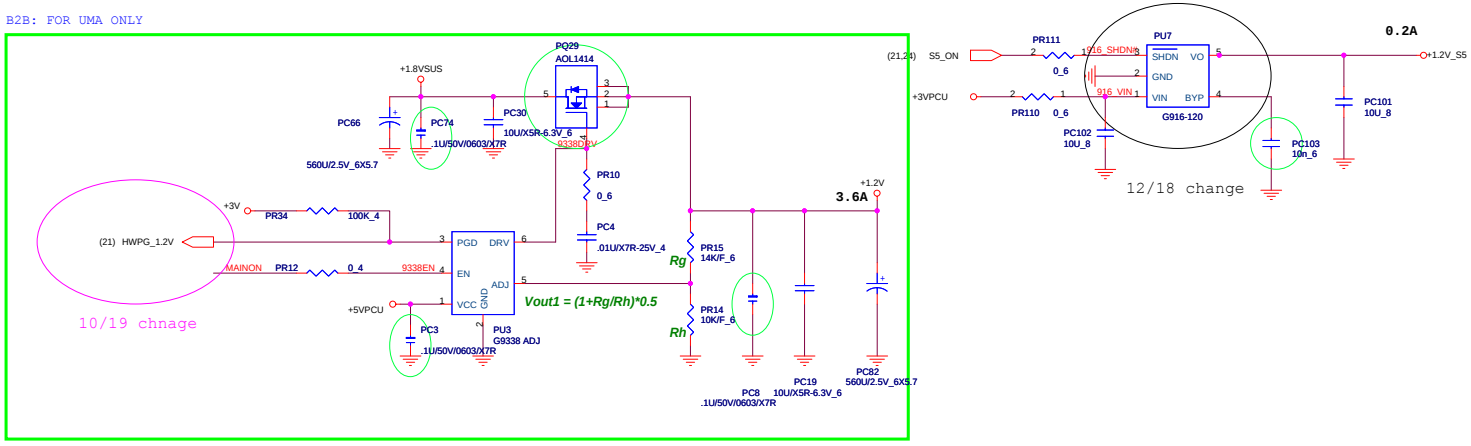
VID[1:0]		
VID1	VID0	
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

MCP67 TABLE

INPUTS		OUTPUTS	VOUT1
G1	G0	OD1 OD2 OD3	
0	0	0.75x(1+R1/R2+R1/R3+R1/R4)	1.2V
1	0	0.75x(1+R1/R2+R1/R3)	1.1V
0	1	0.75x(1+R1/R2+R1/R4)	1.0V
1	1	0.75x(1+R1/R2)	0.9V

SC471A Set

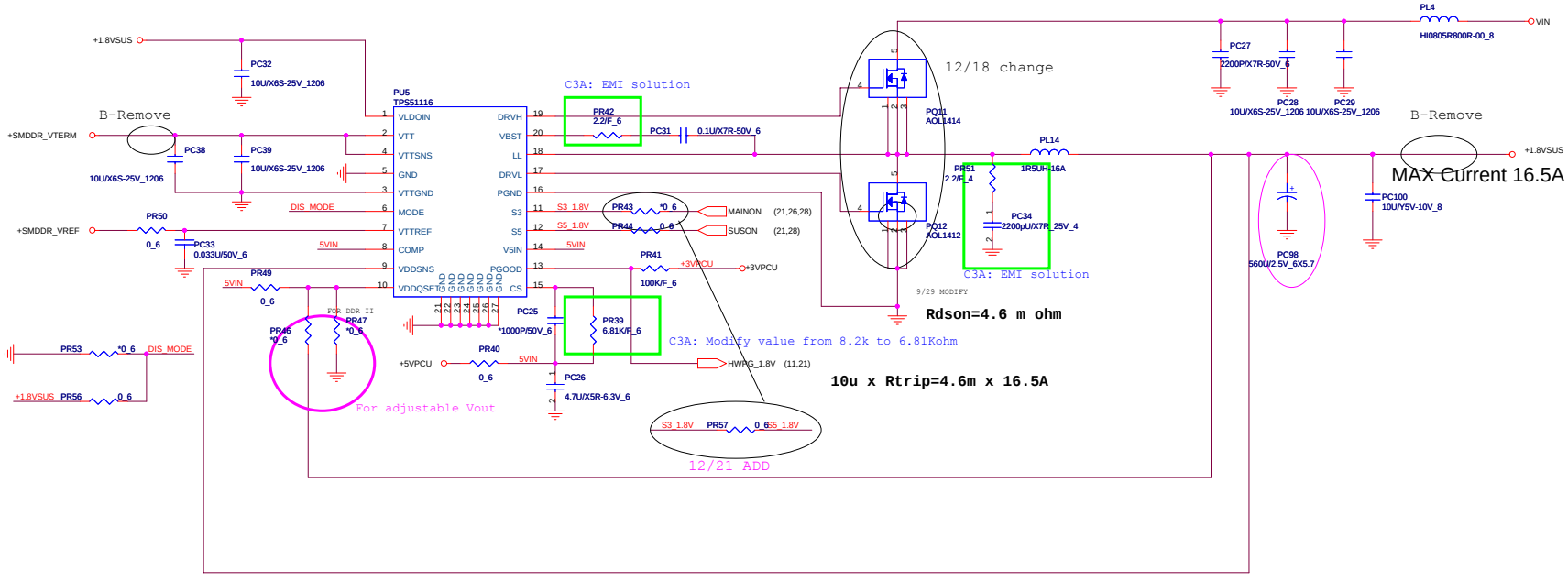


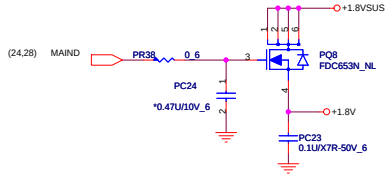


PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
C	SC471J 1.2V	A

Date: Wednesday, April 25, 2007 Sheet 26 of 30



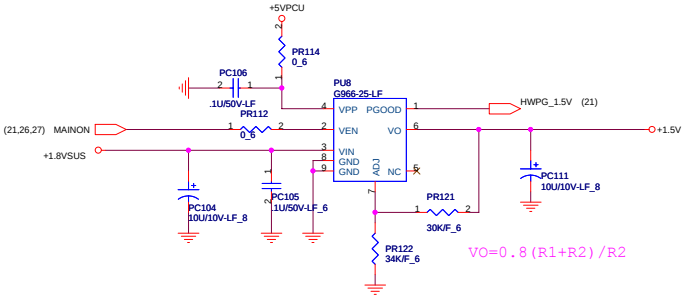


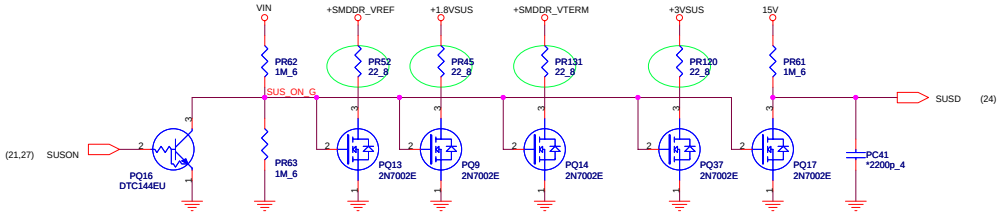
MAX Current 3.5A

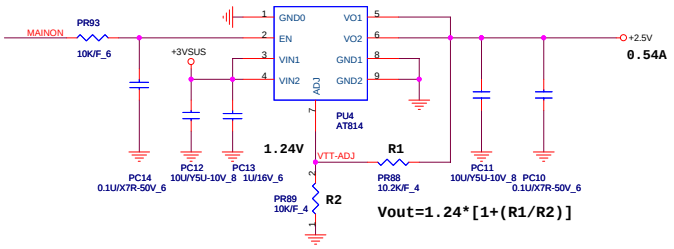
PROJECT : ZO3
Quanta Computer Inc.

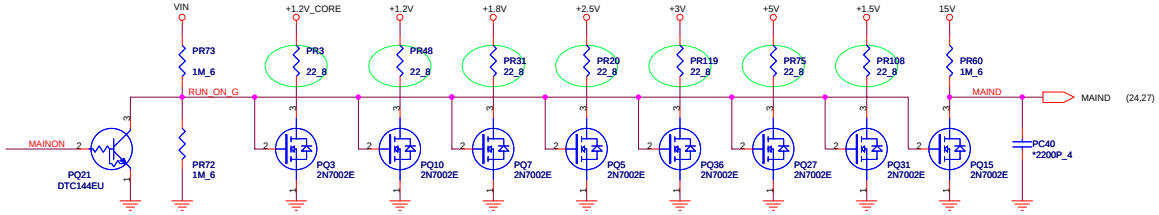
Size	Document Number	Rev
C	TPS51116 DDR	A

Date: Wednesday, April 25, 2007 Sheet 27 of 30









PROJECT : ZO3
Quanta Computer Inc.

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