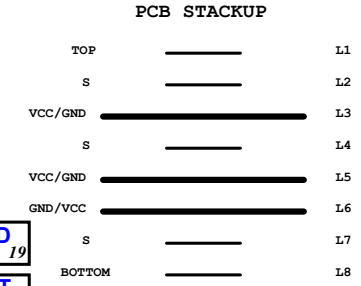
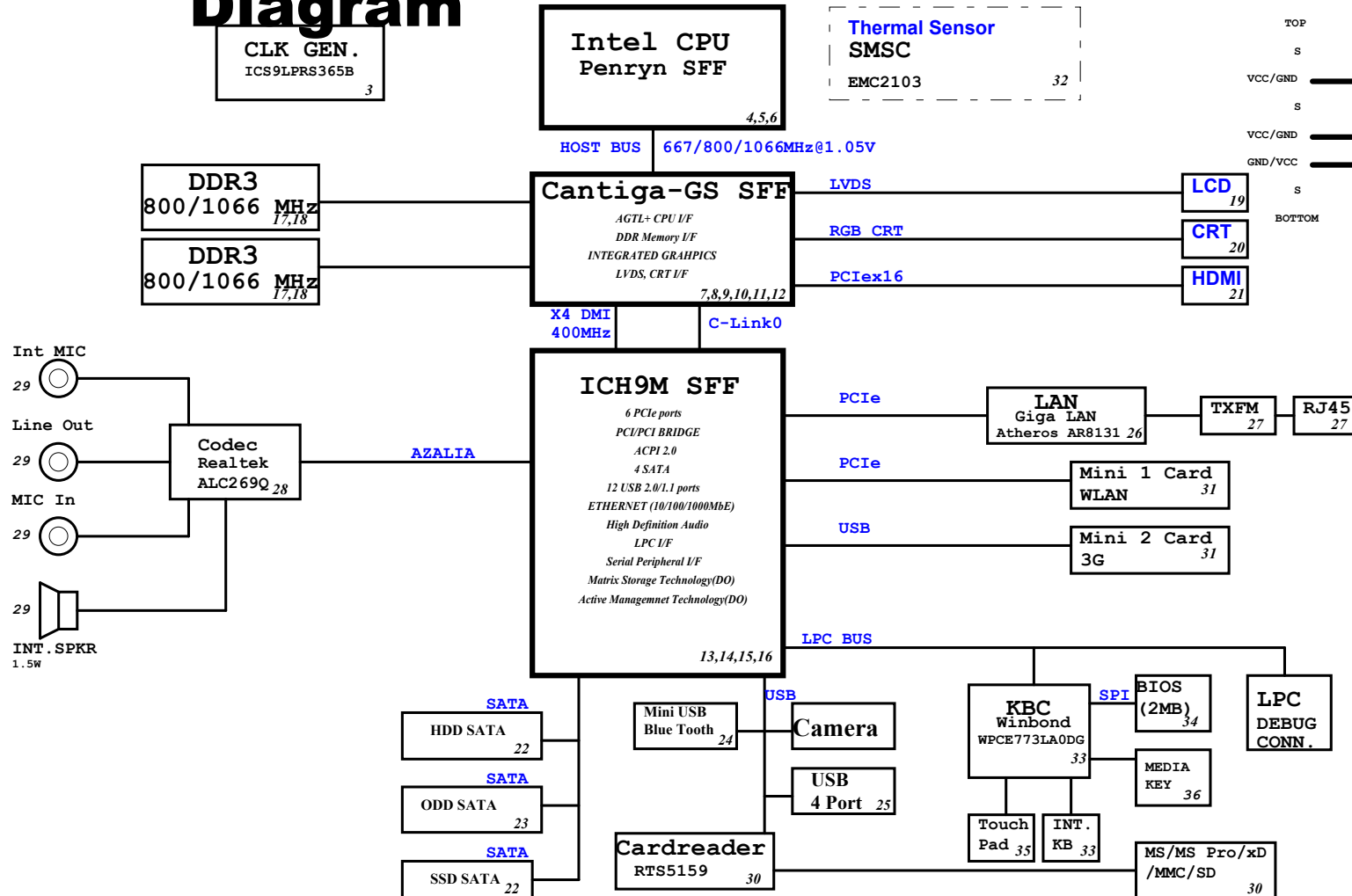


JM41 Block Diagram

Project code: 91.4CQ01.001
 PCB P/N : 48.4CQ01.011
 REVISION : 08266-1



SYSTEM DC/DC TPS51125 36	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (6A) 3D3V_S5 (5A) 5V_AUX_S5 3D3V_AUX_S5
RT8202 37	
INPUTS	OUTPUTS
DCBATOUT	LD05V_S0 (10A)
RT8202 38	
INPUTS	OUTPUTS
DCBATOUT	LD5V_S3 (11A)
RT9026 39	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 (1.2A)
CHARGER MAX8731A 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V_6.0A
CPU DC/DC ADP3207A 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 64A
VGA ISL6263A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC GFXCORE (7A)

<Core Design>

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Title	BLOCK DIAGRAM	
Size	Document Number	Rev
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Date	Monday, March 09, 2009	Sheet 1 of 40

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS_LPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled(Note2) 1 = The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]: (3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]: (3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital Display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIe disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

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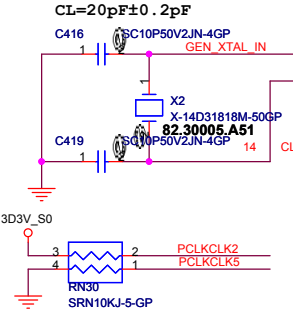
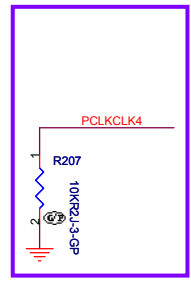
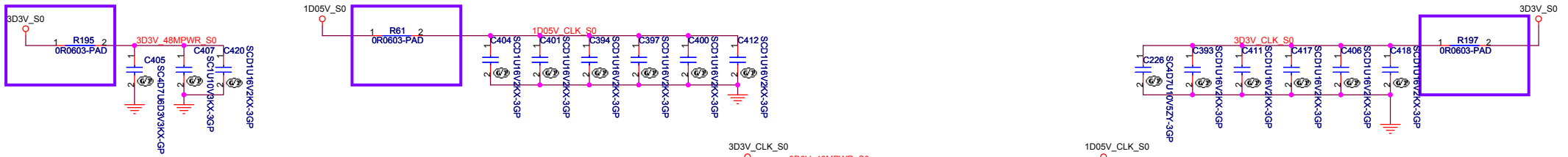
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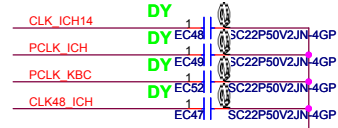
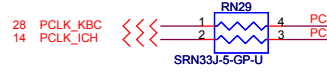
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Size A3 Document Number: **JM41 UMA** Rev: **-1**

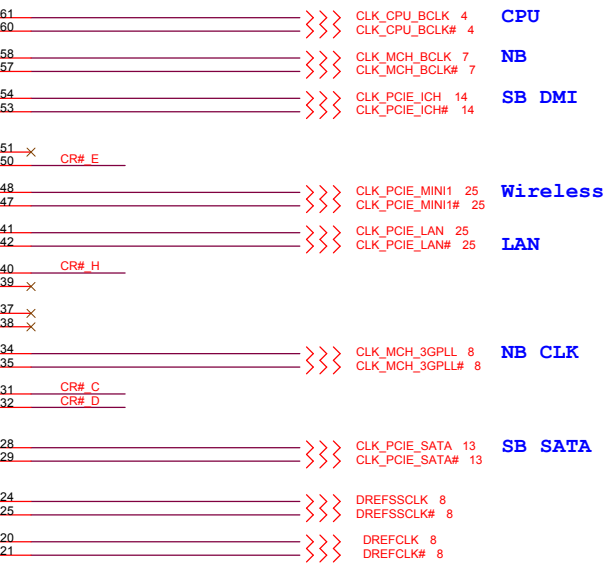
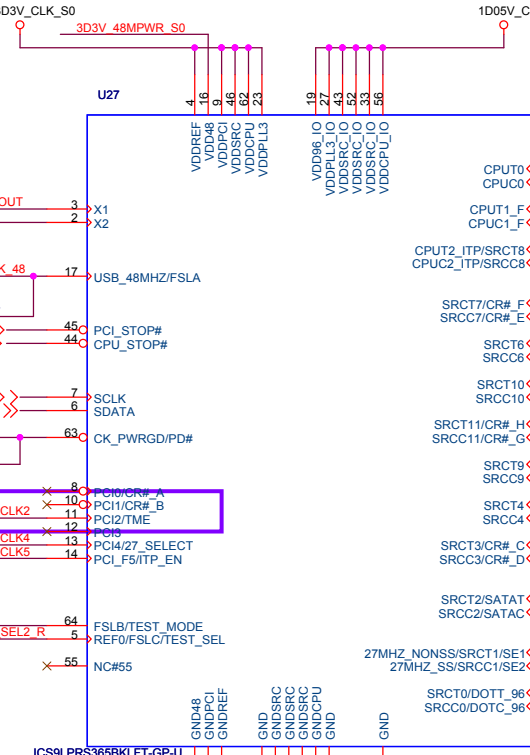
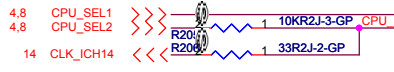
Date: Sunday, March 01, 2009 Sheet 2 of 40



SB_20090205



EMI capacitor for Antenna team suggestion



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR# A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR# A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR# B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR# B controls SRC1 pair (default) 1 = CR# B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR# C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1 = CR# C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CR# D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1 = CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1 = CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10

SEL2	SEL1	SEL0	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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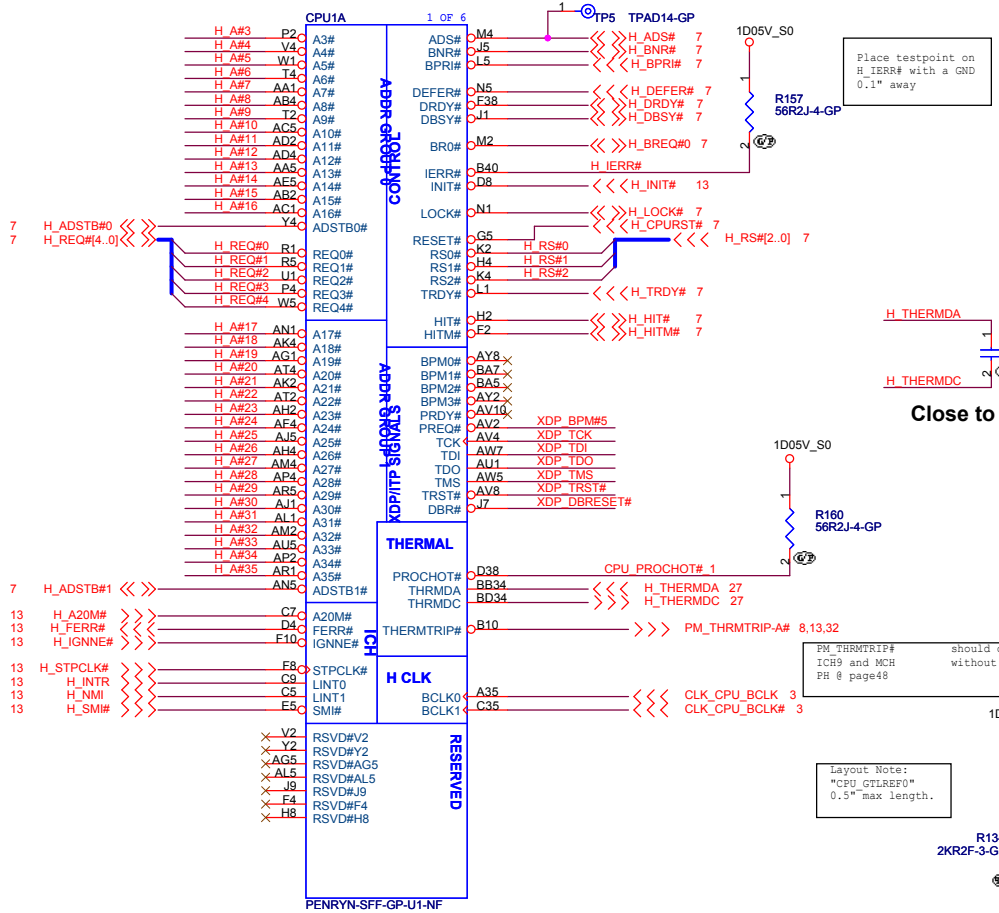
Title: **Clock Generator**

Size: Document Number **JM41_UMA** Rev **-1**

Date: Thursday, March 05, 2009 Sheet 3 of 40

7 H_A#(35..3) <<< H_A#(35..3)

H_DIN#(3..0) <<<>>H_DIN#(3..0) 7
H_DSTBN#(3..0) <<<>>H_DSTBN#(3..0) 7
H_DSTBP#(3..0) <<<>>H_DSTBP#(3..0) 7
H_DM#(63..0) <<<>>H_DM#(63..0) 7



Place testpoint on H_IERR# with a GND 0.1" away

Close to NB

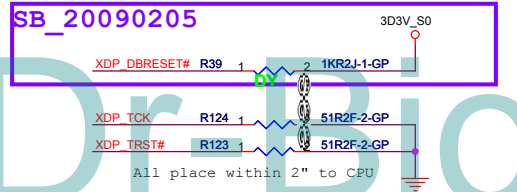
Layout Note: "CPU GTLREF0" 0.5" max length.

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"

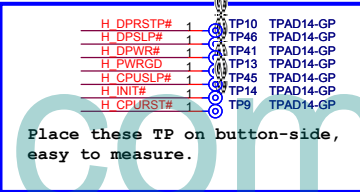
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"

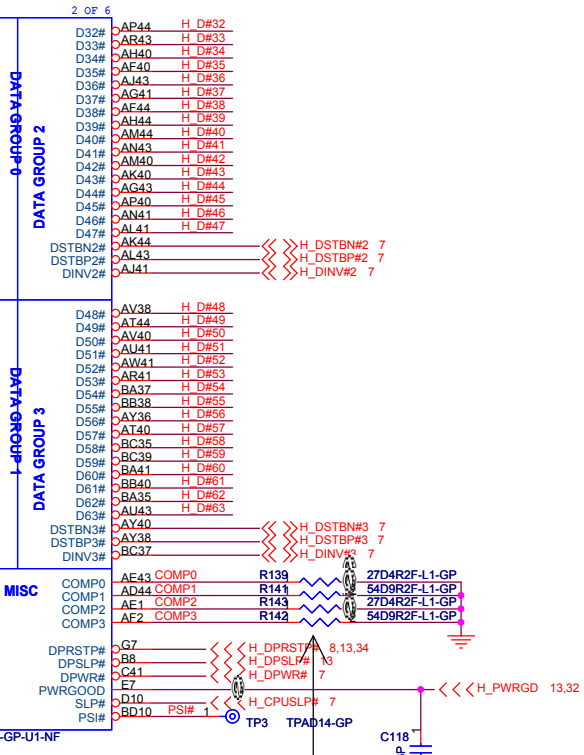
H_FERR#	C329	1	SC100P50V2JN-3GP
H_STPCLK#	C329	2	SC100P50V2JN-3GP
H_IGNNE#	C113	DY	SC100P50V2JN-3GP
H_INTR	C323	DY	SC100P50V2JN-3GP
H_DP_SLP#	C327	DY	SC100P50V2JN-3GP
H_PWRGD	C324	DY	SC100P50V2JN-3GP
H_A20M#	C92	DY	SC100P50V2JN-3GP
H_SMI#	C322	DY	SC100P50V2JN-3GP
H_NMI	C317	DY	SC100P50V2JN-3GP
H_INIT#	C318	DY	SC100P50V2JN-3GP
	C316	DY	SC100P50V2JN-3GP



All place within 2" to CPU



Place these TP on button-side, easy to measure.



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CPU (1 of 3)

JM41 UMA

File		Rev	-1
Size	Document Number		
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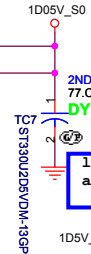
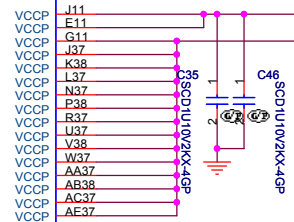
VCC_CORE

VCC_CORE

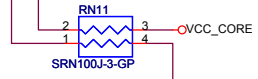
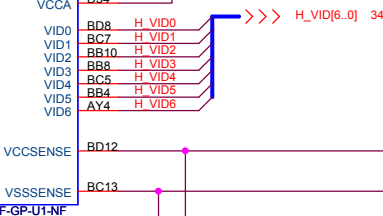
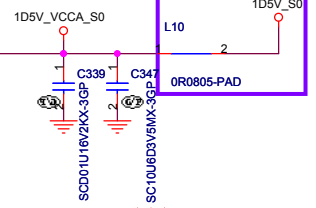
CPU1D 4 OF 6

- F32 VCC
- G33 VCC
- H32 VCC
- J33 VCC
- K32 VCC
- L33 VCC
- M32 VCC
- N33 VCC
- P32 VCC
- R33 VCC
- T32 VCC
- U33 VCC
- V32 VCC
- W33 VCC
- Y32 VCC
- AA33 VCC
- AB32 VCC
- AC33 VCC
- AD32 VCC
- AE33 VCC
- AF32 VCC
- AG33 VCC
- AH32 VCC
- AJ33 VCC
- AK32 VCC
- AL33 VCC
- AM32 VCC
- AN33 VCC
- AP32 VCC
- AR33 VCC
- AT34 VCC
- AT32 VCC
- AU33 VCC
- AV32 VCC
- AY32 VCC
- BB32 VCC
- BD32 VCC
- B28 VCC
- B30 VCC
- B26 VCC
- D28 VCC
- D30 VCC
- F30 VCC
- F28 VCC
- H30 VCC
- H28 VCC
- D26 VCC
- F26 VCC
- H26 VCC
- K30 VCC
- K28 VCC
- M30 VCC
- M28 VCC
- K26 VCC
- M26 VCC
- P30 VCC
- P28 VCC
- T30 VCC
- T28 VCC
- V30 VCC
- V28 VCC
- P26 VCC
- T26 VCC
- V26 VCC
- Y30 VCC
- Y28 VCC
- AB30 VCC

- AB28 VCC
- AD30 VCC
- AD28 VCC
- Y26 VCC
- AB26 VCC
- AD26 VCC
- AE30 VCC
- AE28 VCC
- AH30 VCC
- AH28 VCC
- AF26 VCC
- AH26 VCC
- AK30 VCC
- AK28 VCC
- AM30 VCC
- AM28 VCC
- AP30 VCC
- AP28 VCC
- AK26 VCC
- AM26 VCC
- AP26 VCC
- AT30 VCC
- AT28 VCC
- AV30 VCC
- AV28 VCC
- AY30 VCC
- AY28 VCC
- AT26 VCC
- AV26 VCC
- BB30 VCC
- BB28 VCC
- BD30 VCC



layout note: "1D5V_VCCA_S0" as short as possible



Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

- B42 VSS
- F44 VSS
- D42 VSS
- F42 VSS
- H42 VSS
- K42 VSS
- M42 VSS
- P42 VSS
- T42 VSS
- V42 VSS
- Y42 VSS
- AB42 VSS
- AD42 VSS
- AF42 VSS
- AH42 VSS
- AK42 VSS
- AM42 VSS
- AP42 VSS
- AV44 VSS
- AT42 VSS
- AV42 VSS
- AY42 VSS
- BA43 VSS
- BB42 VSS
- C39 VSS
- E39 VSS
- G37 VSS
- H38 VSS
- J39 VSS
- L39 VSS
- M38 VSS
- N39 VSS
- R39 VSS
- T38 VSS
- U39 VSS
- W39 VSS
- Y38 VSS
- AA39 VSS
- AC39 VSS
- AD38 VSS
- AE39 VSS
- AG39 VSS
- AH38 VSS
- AJ39 VSS
- AL39 VSS
- AM38 VSS
- AN39 VSS
- AR39 VSS
- AS39 VSS
- AT38 VSS
- AU39 VSS
- AU37 VSS
- AW39 VSS
- AW37 VSS
- BA39 VSS
- BC41 VSS
- BD38 VSS
- B36 VSS
- H34 VSS
- D36 VSS
- K34 VSS
- M34 VSS
- M36 VSS
- P34 VSS
- T34 VSS
- V34 VSS
- T36 VSS
- Y34 VSS
- AB34 VSS
- AD34 VSS
- Y36 VSS
- AD36 VSS
- AF34 VSS
- AH34 VSS
- AH36 VSS
- AK34 VSS
- AM34 VSS
- AM36 VSS
- AP34 VSS
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- VSS

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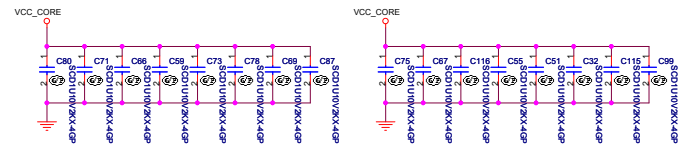
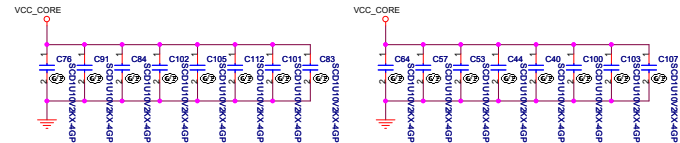
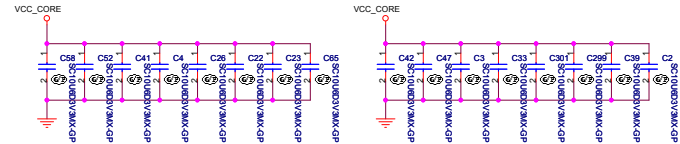
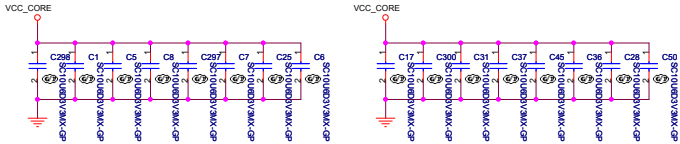
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Size: Document Number: **JM41 UMA** Rev: **-1**

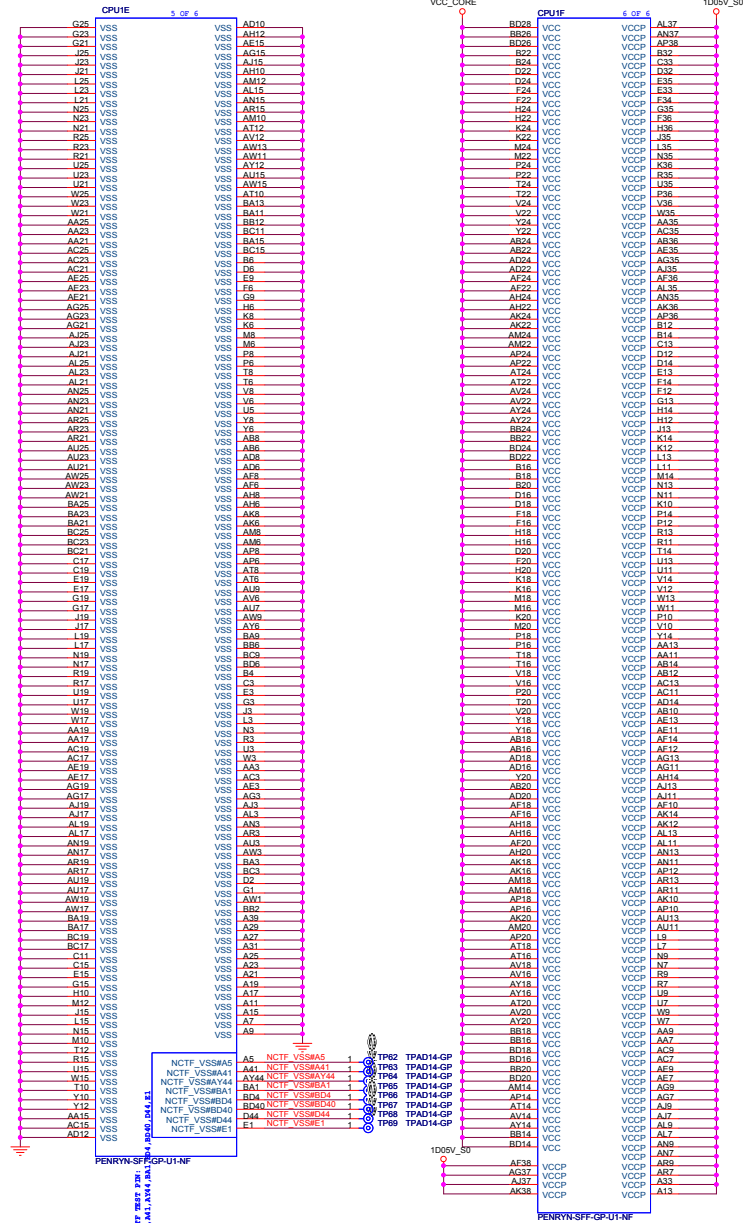
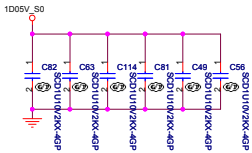
Date: Thursday, March 05, 2009 Sheet 5 of 40



Place these inside socket cavity on L8(North side Secondary)



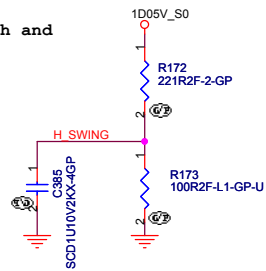
Place these inside socket cavity on L8(North side Secondary)



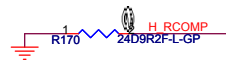
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H_SWING routing Trace width and Spacing use 10 / 20 mil

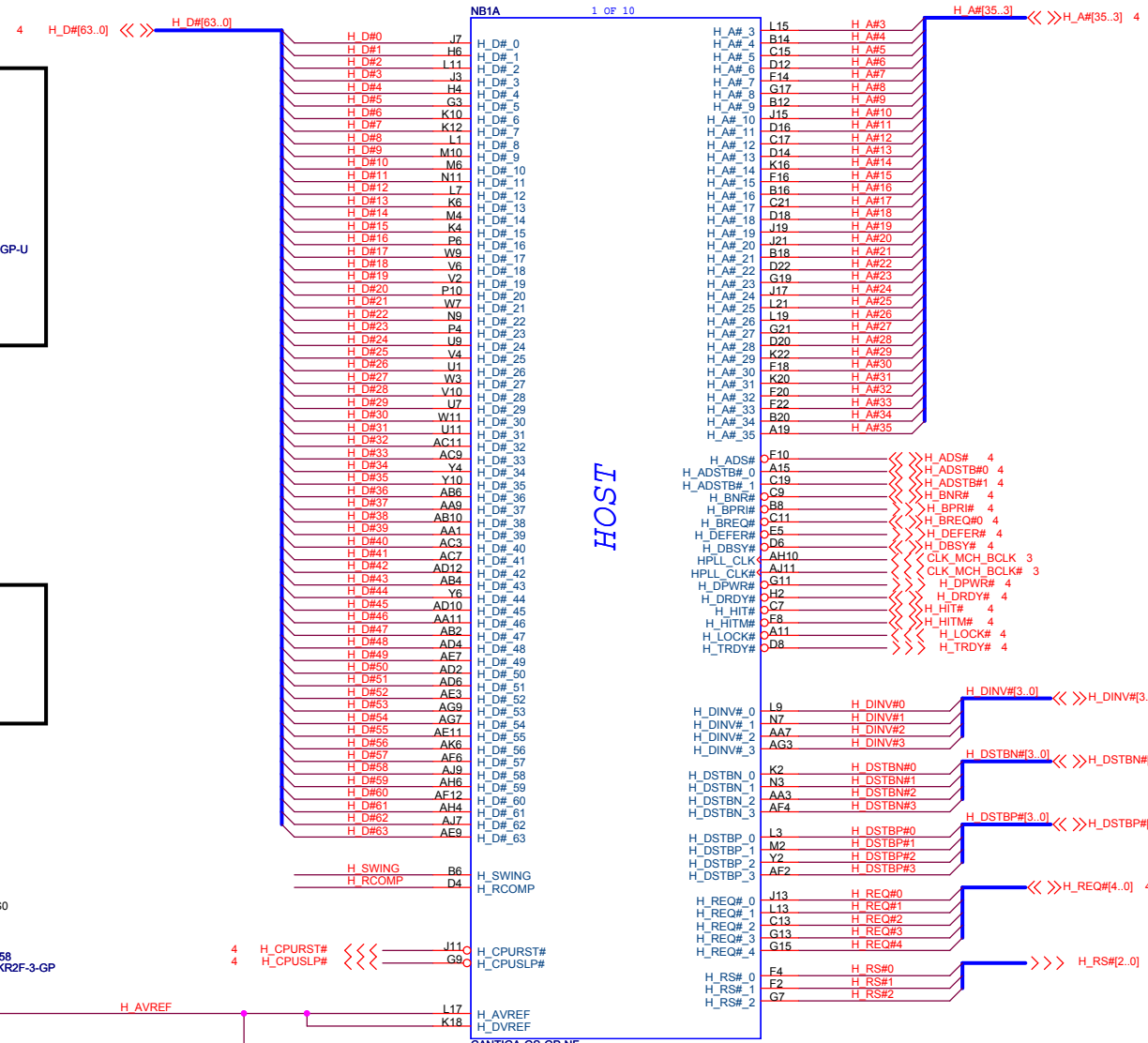
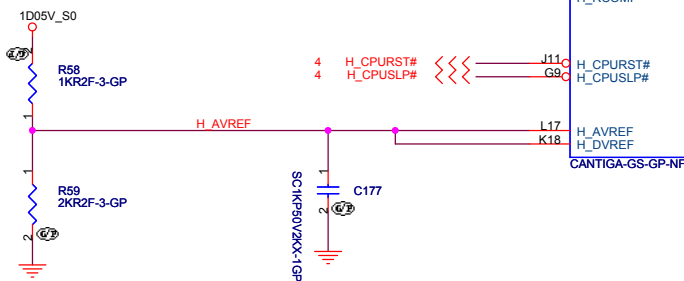
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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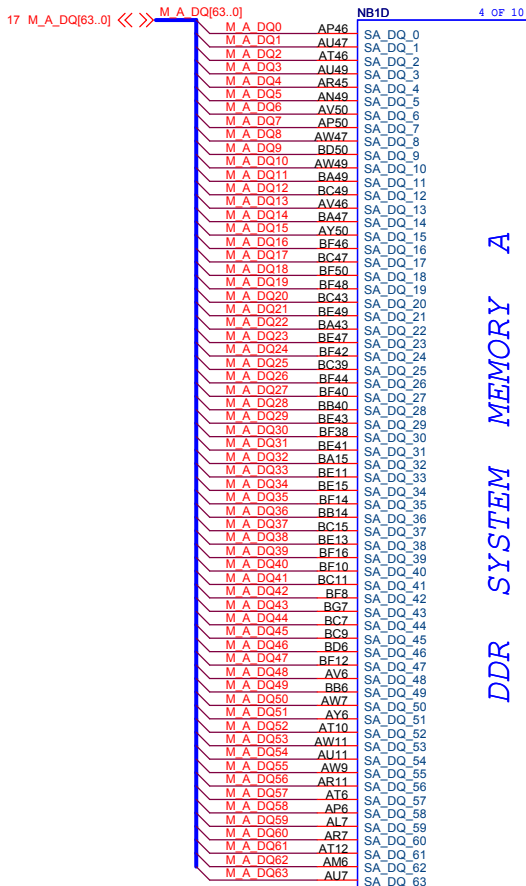
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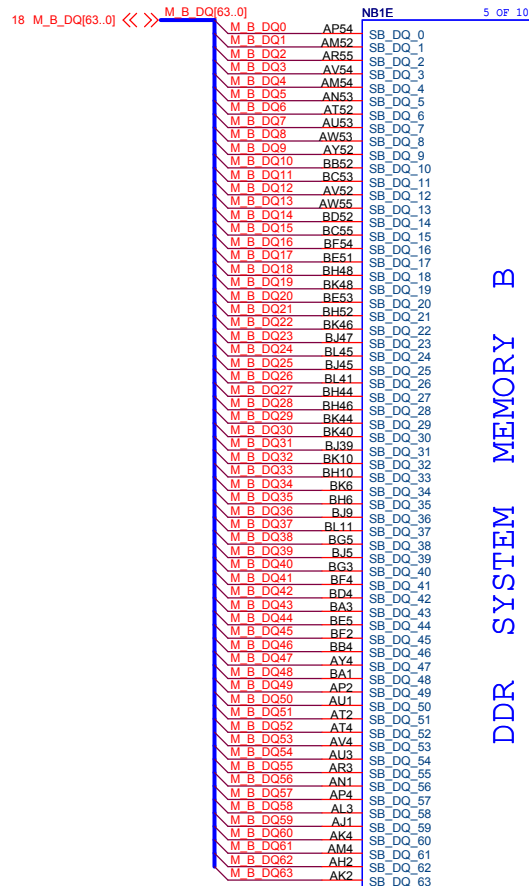
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Size: Document Number: **JM41_UMA** Rev: **-1**

Date: Thursday, March 05, 2009 Sheet 7 of 40

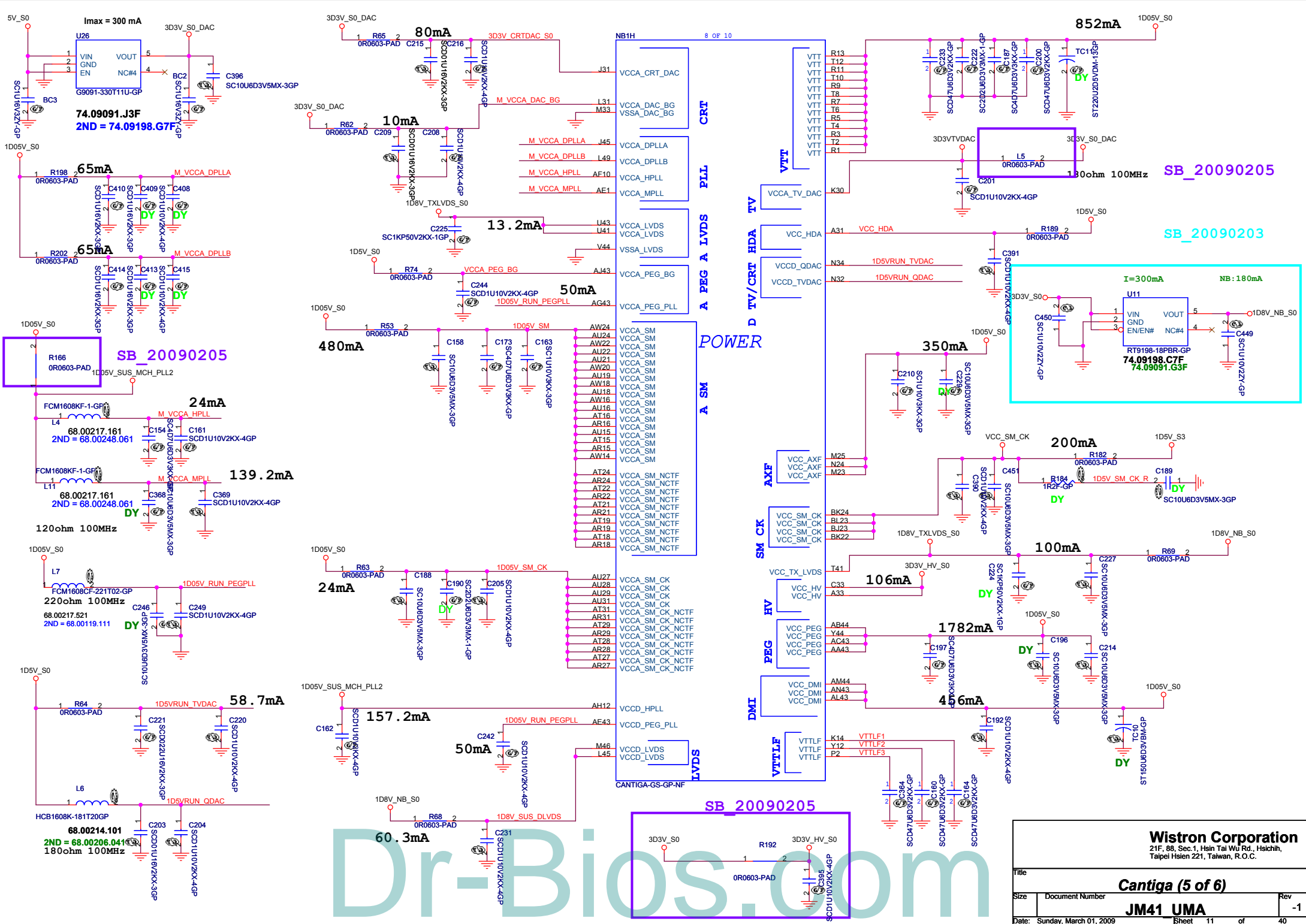


DDR SYSTEM MEMORY A



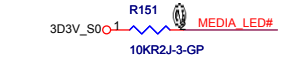
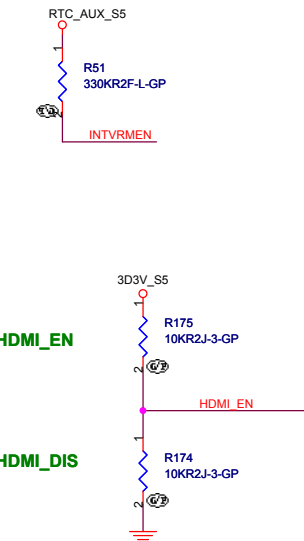
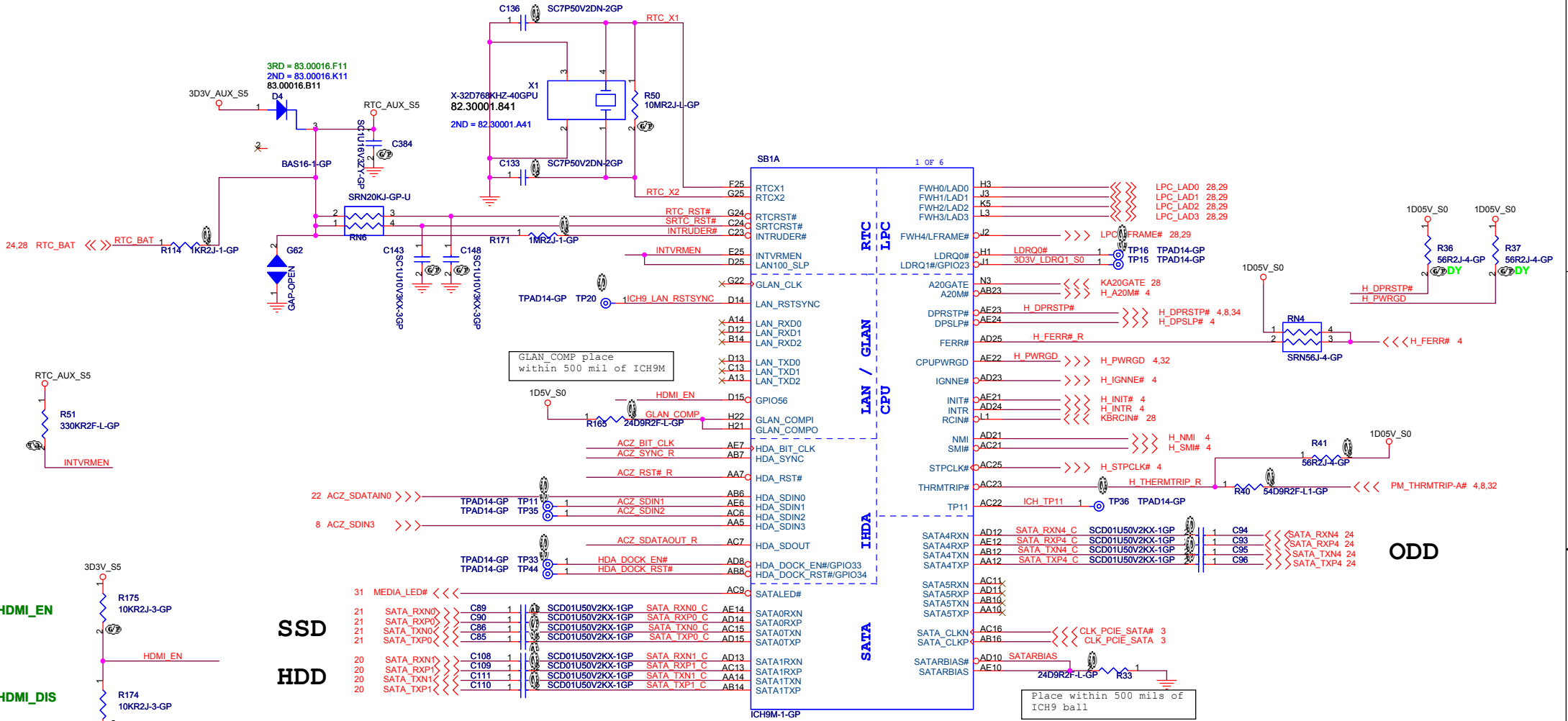
DDR SYSTEM MEMORY B





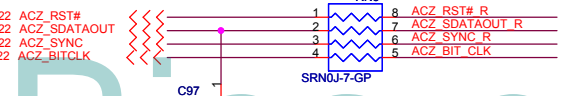
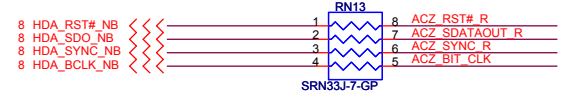
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Cantiga (5 of 6)		
Size: Document Number	Rev: -1	
Date: Sunday, March 01, 2009 Sheet 11 of 40		



SSD
HDD

31	MEDIA_LED#	<<<	AC9	
21	SATA_RXN0	>>>	C89	1
21	SATA_RXP0	>>>	C90	1
21	SATA_TXN0	>>>	C86	1
21	SATA_TXP0	>>>	C85	1
20	SATA_RXN1	>>>	C108	1
20	SATA_RXP1	>>>	C109	1
20	SATA_TXN1	>>>	C111	1
20	SATA_TXP1	>>>	C110	1



Integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
Integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

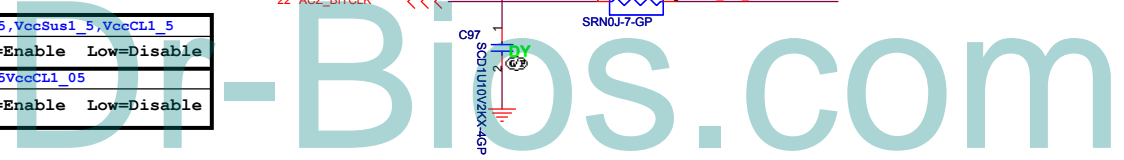
<Core Design>

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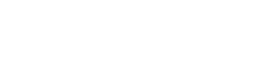
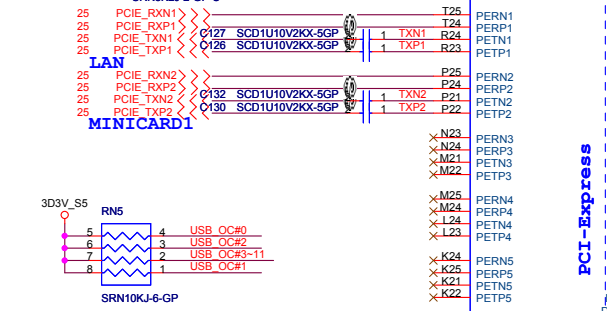
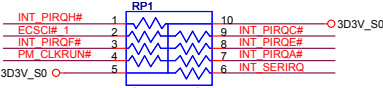
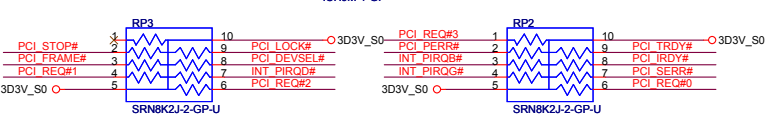
Title: **ICH9-M (1 of 4)**

Size: Document Number: **JM41_UMA** Rev: -1

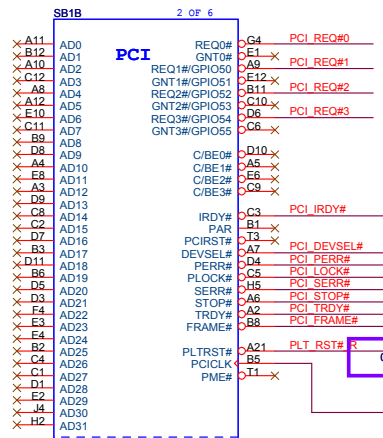
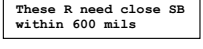
Date: Thursday, March 05, 2009 Sheet: 13 of 40



PCI_GNT#0 and SPI_CS#1
have weak internal Pull up



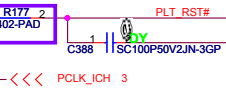
These R need close SB
within 600 mils



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PC1
1	1	LPC (Default)

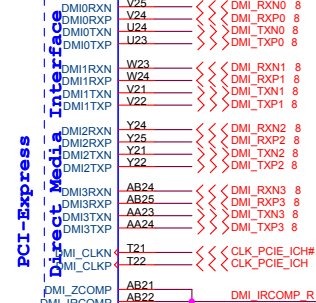
A16 swap override strap
low = A16 swap override enable
high = default

SB_20090205



GPIO49 should be pulled down to GND only when using Teناه. When using Cantiga, this ball should be left as No Connect.

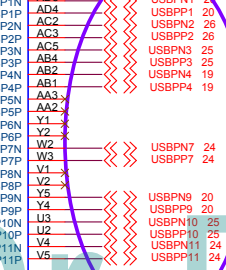
SB1D



SPI



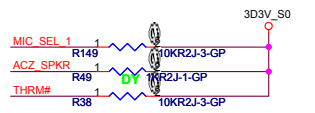
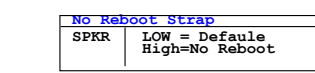
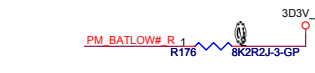
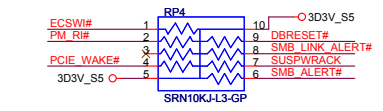
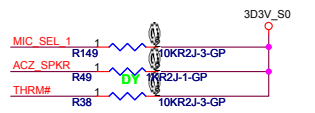
USB



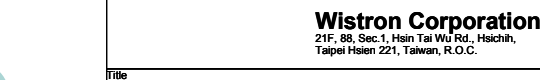
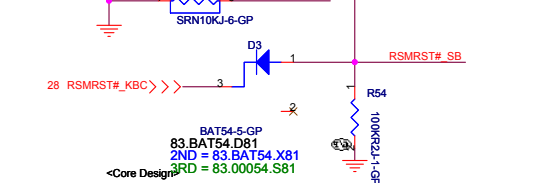
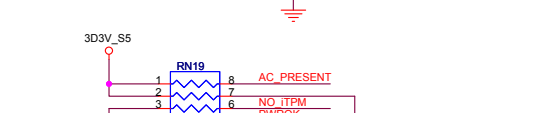
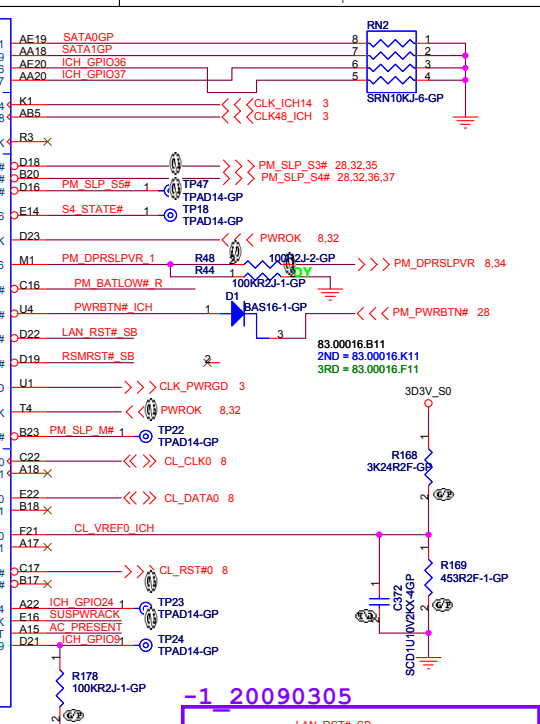
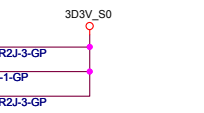
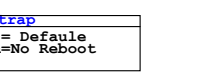
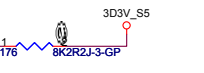
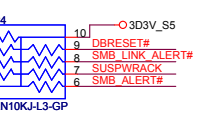
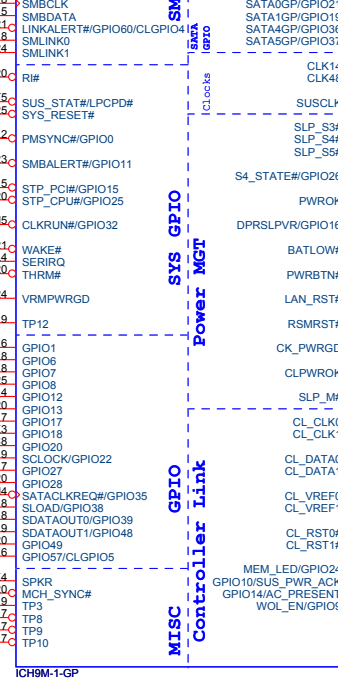
Pair	Device
0	USB2
1	USB3
2	USB4
3	WIMAX
4	WEBCAM
5	NC
6	NC
7	BLUETOOTH
8	NC
9	USB1
10	MINIC2
11	Cardreader

SB_20090205

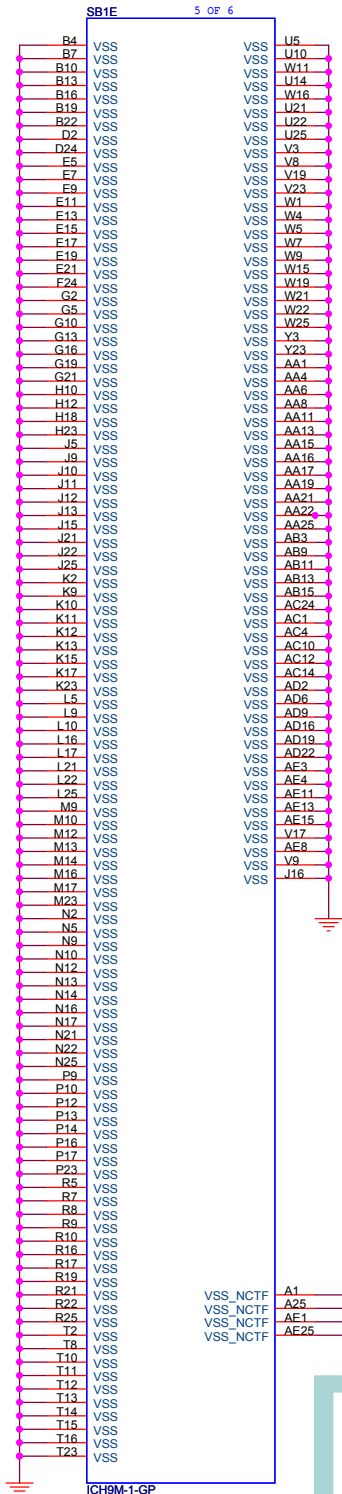
No Reboot Strap	
SPKR	LOW = Default High=No Reboot
1	ACZ_SPKR
2	ACZ_SPKR
3	ACZ_SPKR
4	ACZ_SPKR
5	ACZ_SPKR



SB1C



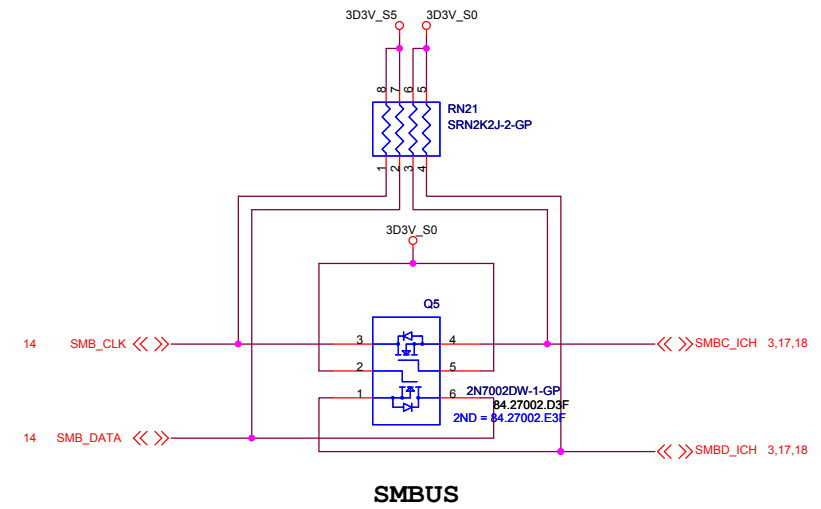
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VSS_NCTF	A1	ICH0_NCTF#A1	1	TP19	TPAD14-GP
VSS_NCTF	A25	ICH0_NCTF#A25	1	TP17	TPAD14-GP
VSS_NCTF	AE1	ICH0_NCTF#AE1	1	TP12	TPAD14-GP
VSS_NCTF	AE25	ICH0_NCTF#AE25	1	TP7	TPAD14-GP

NCTF PIN

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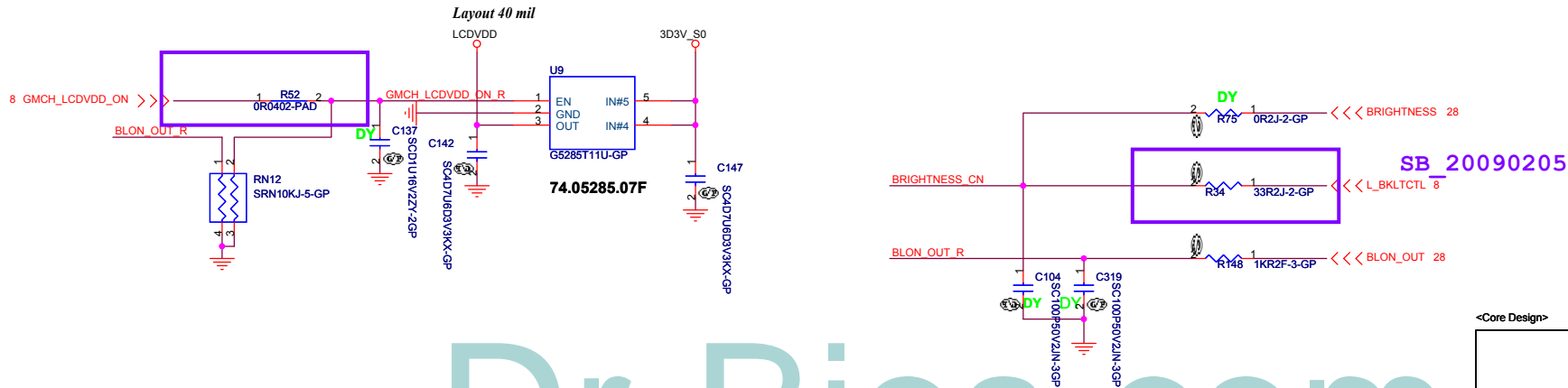
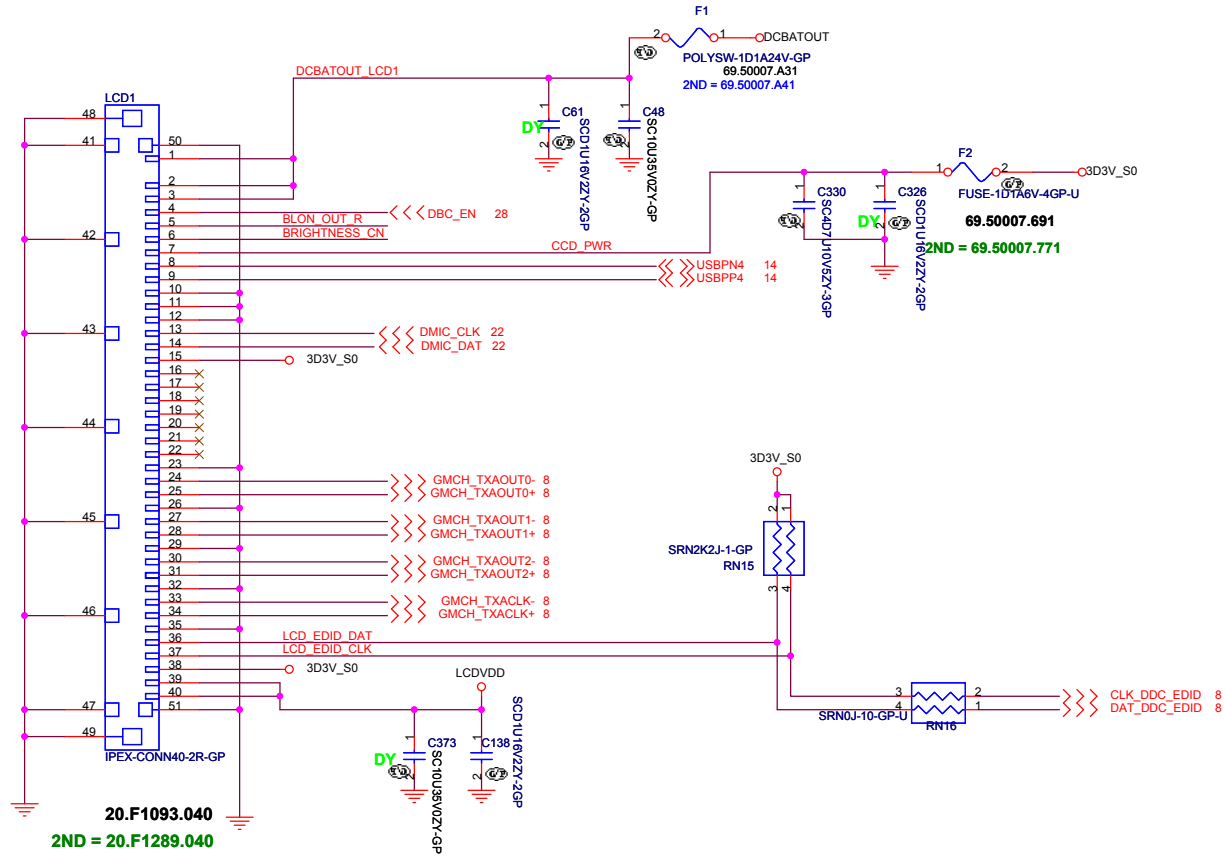


SMBUS

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ICH9-M (4 of 4)		
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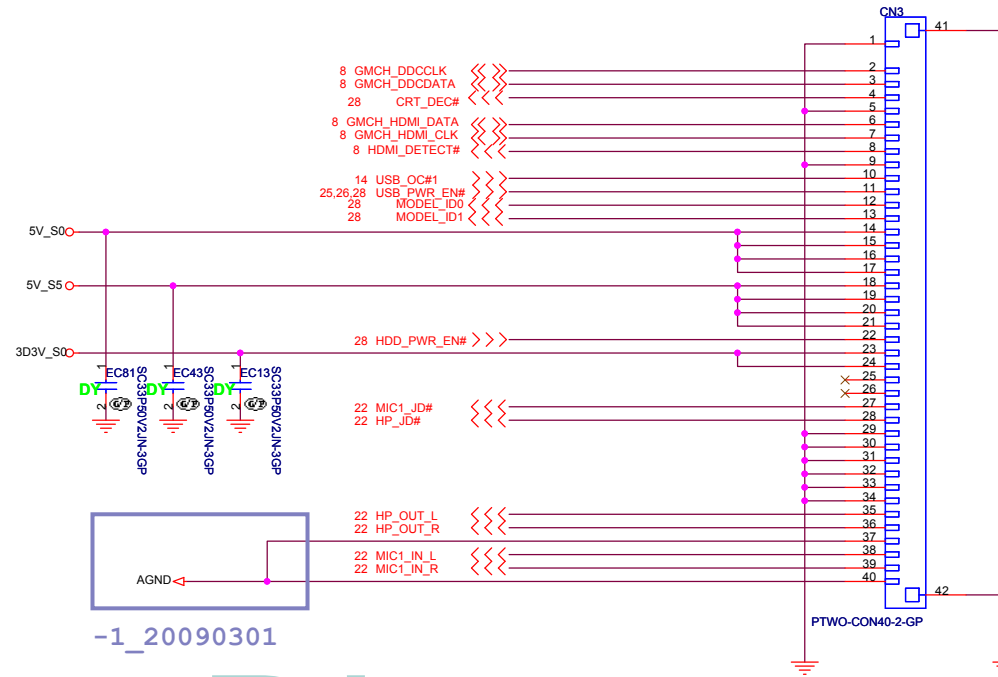
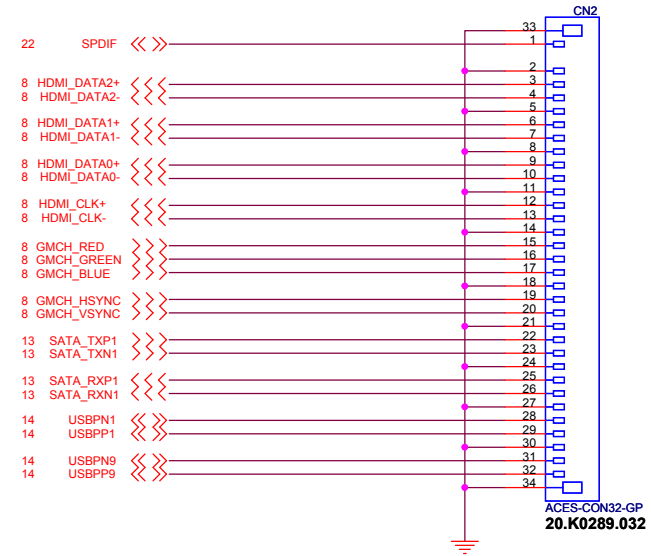
LCD/CCD CONN

Internal MIC



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<Core Design>		
Wistron Corporation 21F, 68, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title LCD CONN		
Size	Document Number	Rev
	JM41 UMA	-1
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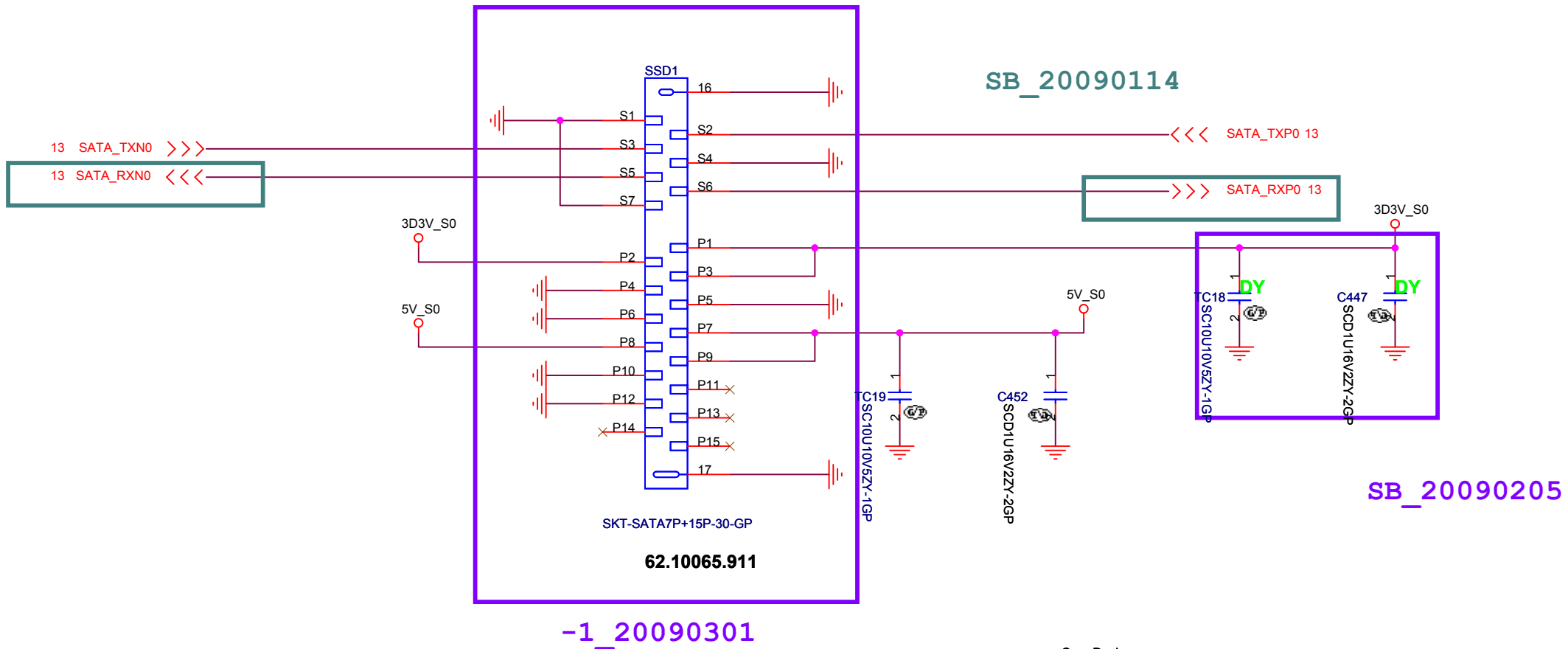


<Core Design>

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CRT BD CONN		
Size	Document Number JM41 UMA	Rev -1
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SSD SATA Connector



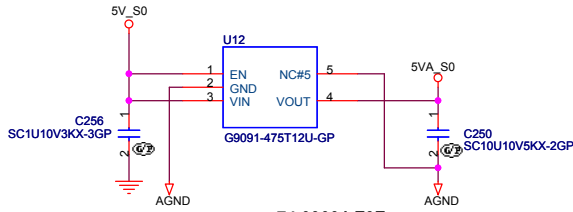
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Wistron Corporation

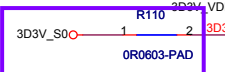
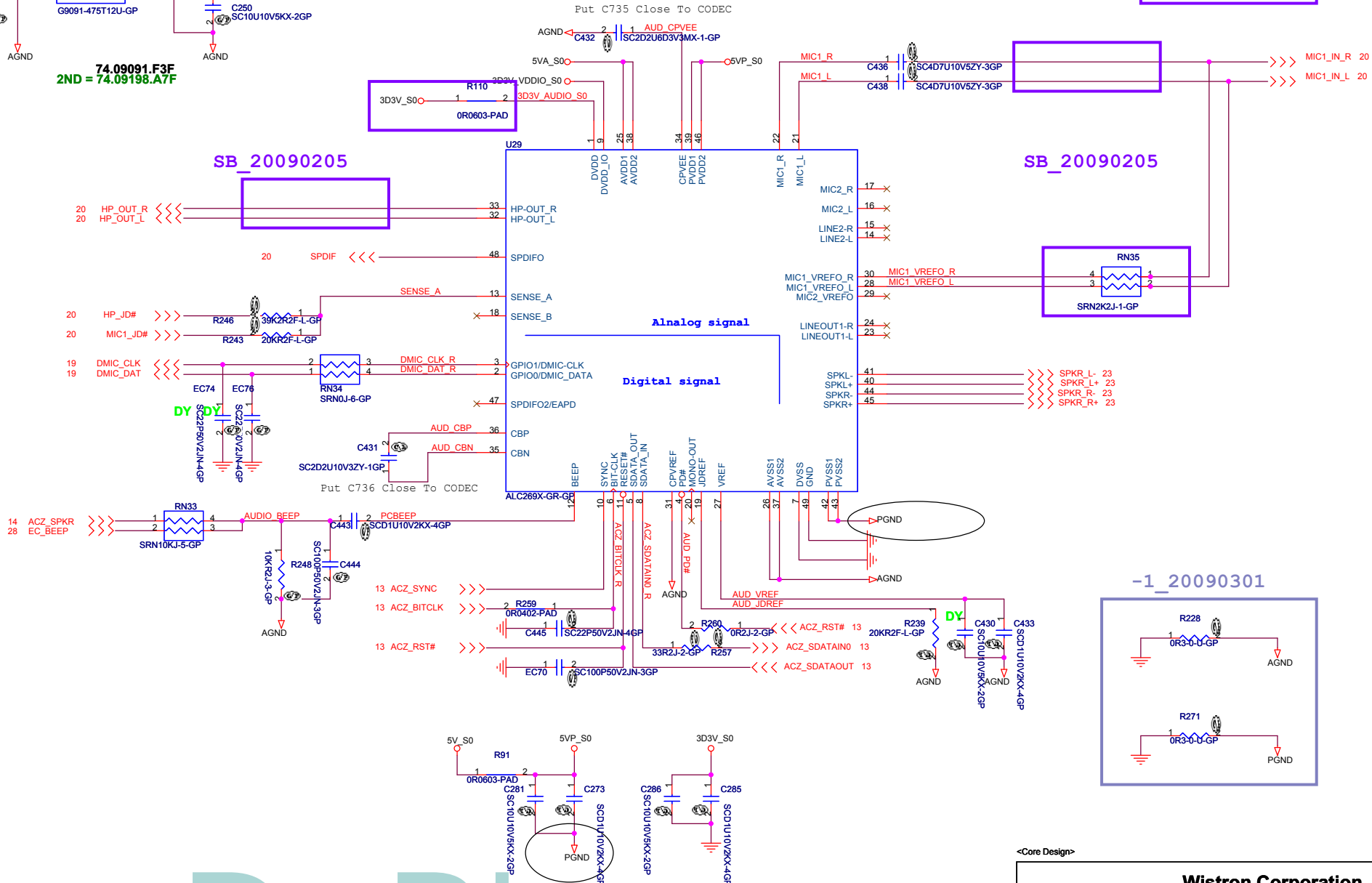
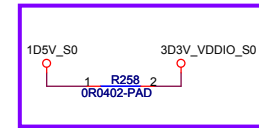
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title			HDD CONN		
Size	Document Number				Rev
	JM41 UMA				-1
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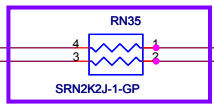
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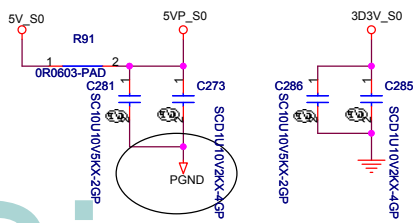
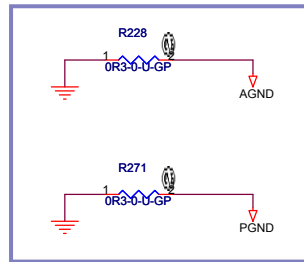
74.09091.F3F
2ND = 74.09198.A7F



SB_20090205



-1_20090301



Close Pim.39
and Pin.46

Close Pim.1
and Pin.9

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<Core Design>

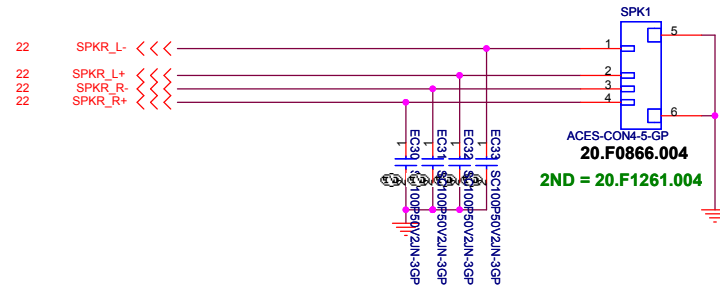
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC REALTEK ALC269**

Size: Document Number **JM41 UMA** Rev: -1

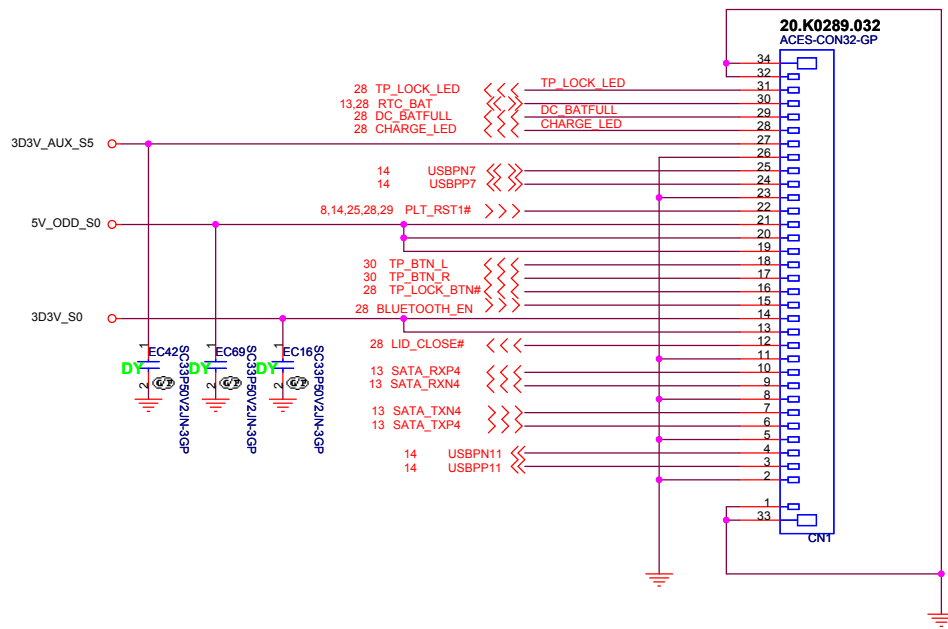
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Internal Speaker



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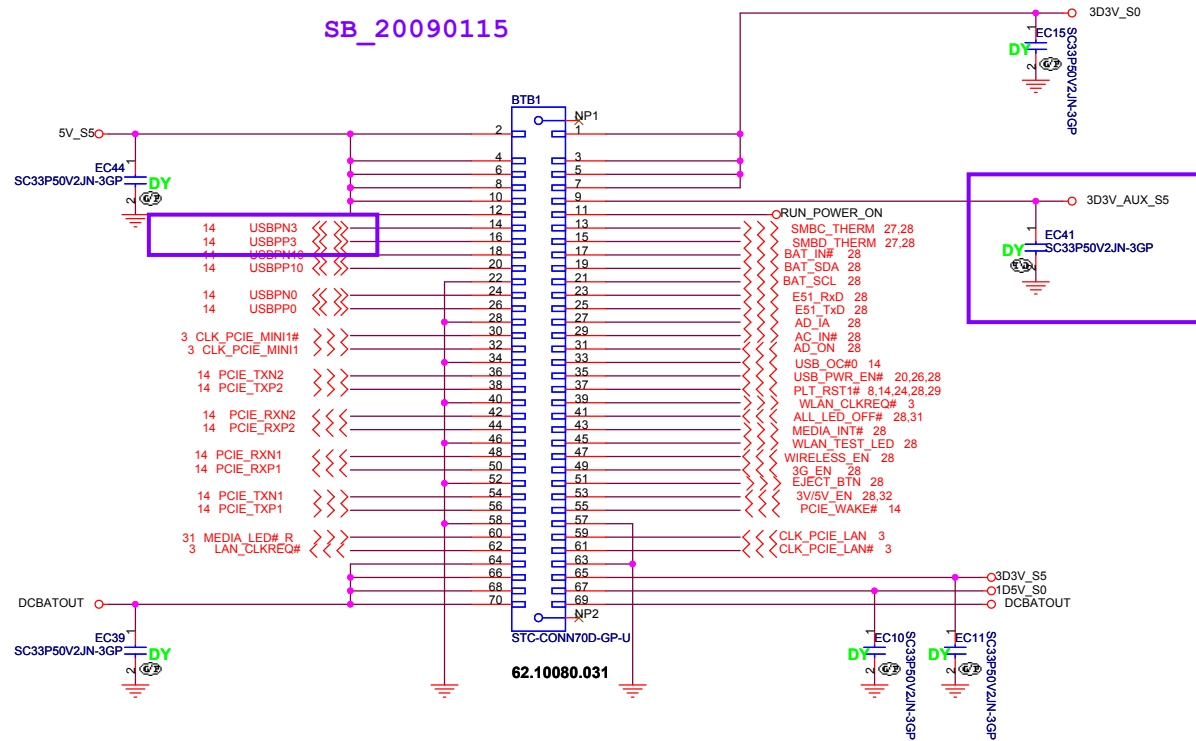
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Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title AUDIO JACK			
Size	Document Number	JM41 UMA	Rev -1
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<Core Design>

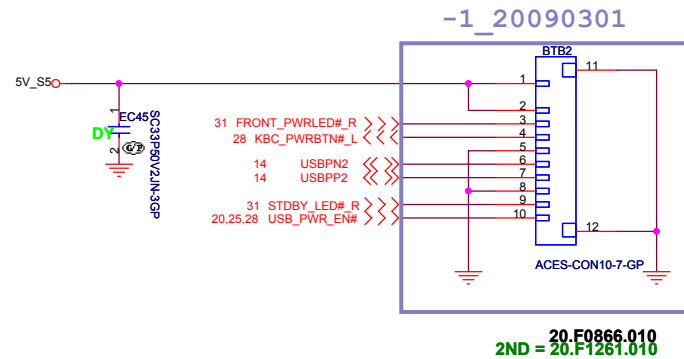
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CARDREADER BD CONN		
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<Core Design>

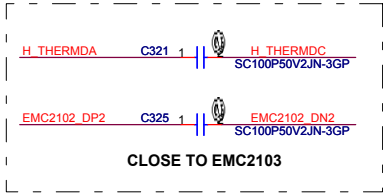
Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
MINI BD CONN		
Title		
Size	Document Number	Rev
A3	JM41_UMA	-1
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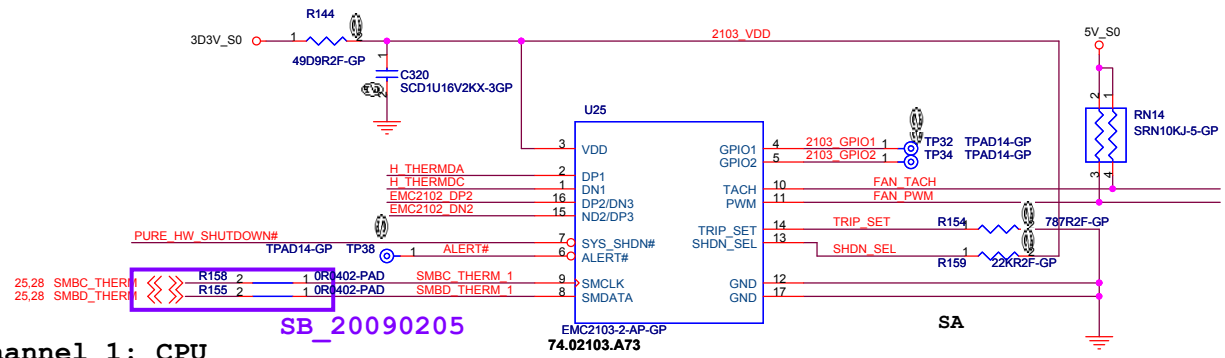
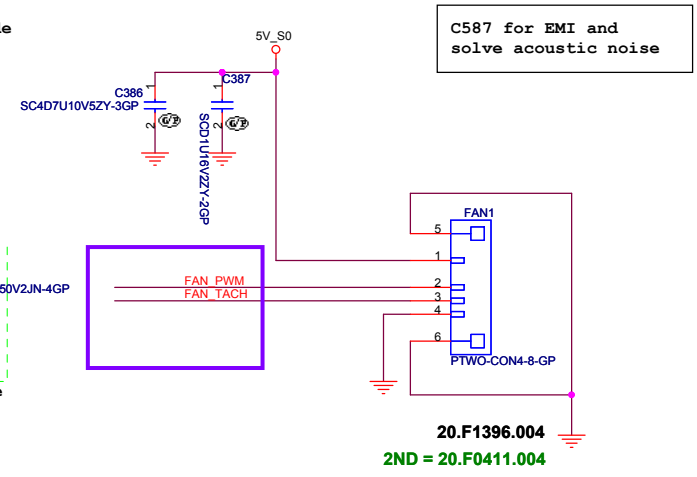
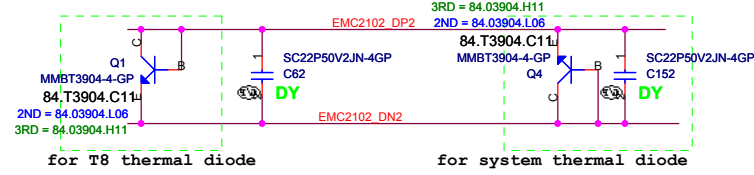
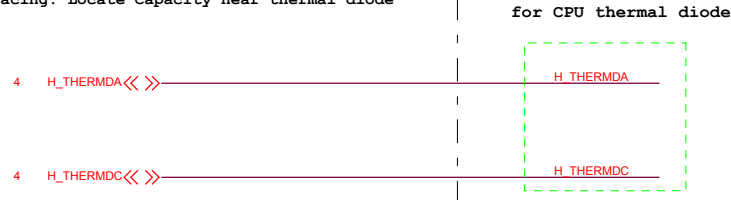
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<Core Design>

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POWER BUTTON CONN		
Size A3	Document Number JM41_UMA	Rev -1
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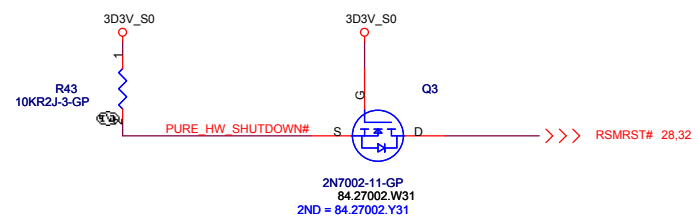
CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode



ps. FAN1 POWER TRACE WIDTH MAY BE IN 25 MIL

- Channel 1: CPU
- Channel 2: Palmrest
- Channel 3: T8

SHDN_SEL		TRIP SET	
PULL UP RESISTOR	MODE OF OPERATION	Ttrip (degree)	RSET (1%)
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED, REC DISABLED	85	562
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED, REC ENABLED	86	604
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED	87	649
15K OHM	INTERNAL DIODE	88	698
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED	89	750
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED	90	787
		91	845
		92	909
		93	953
		94	1020
		95	1100



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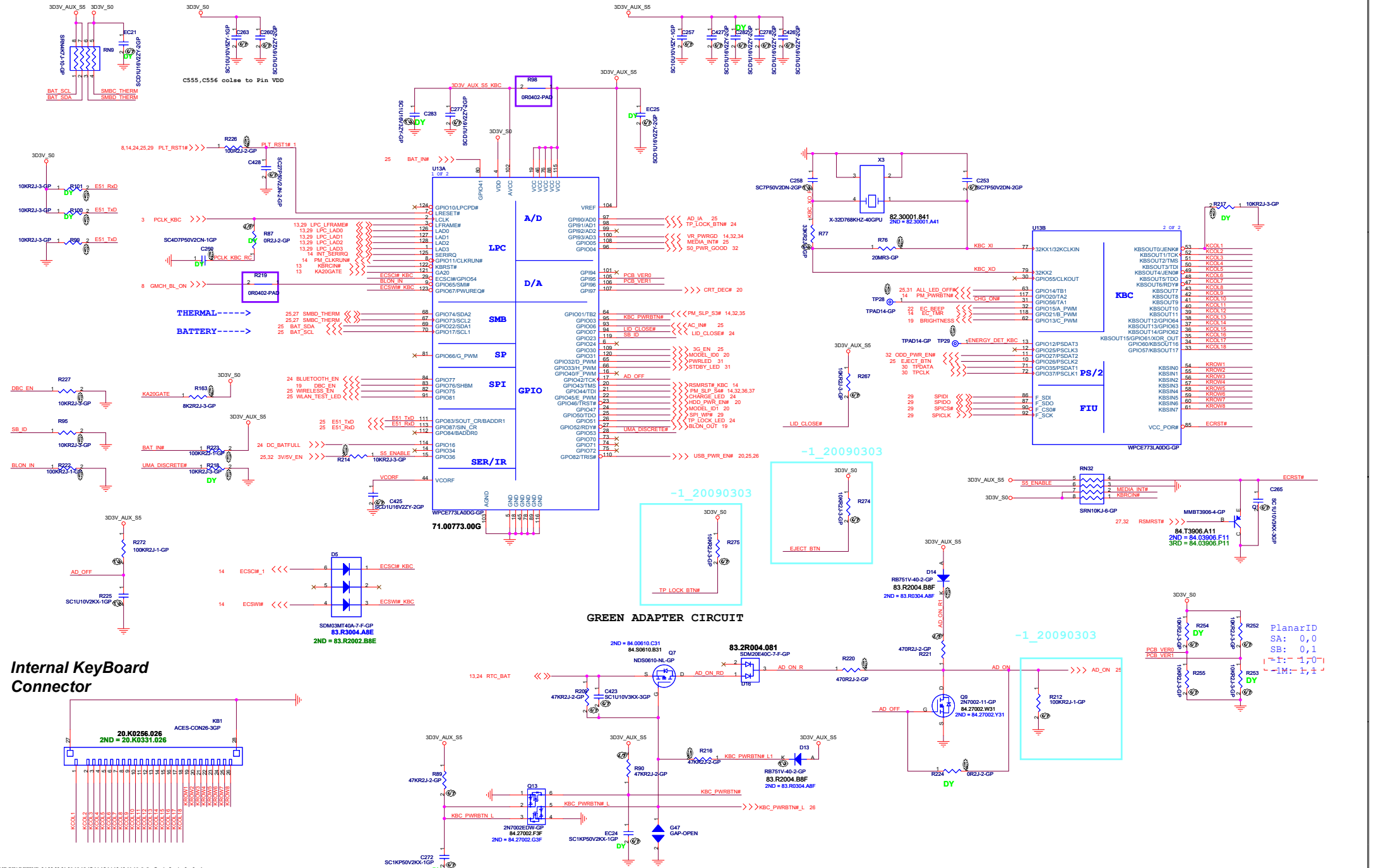
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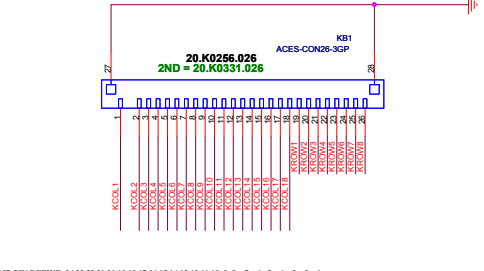
Title: **Thermal/Fan Controller**

Size: Document Number **JM41_UMA** Rev: -1

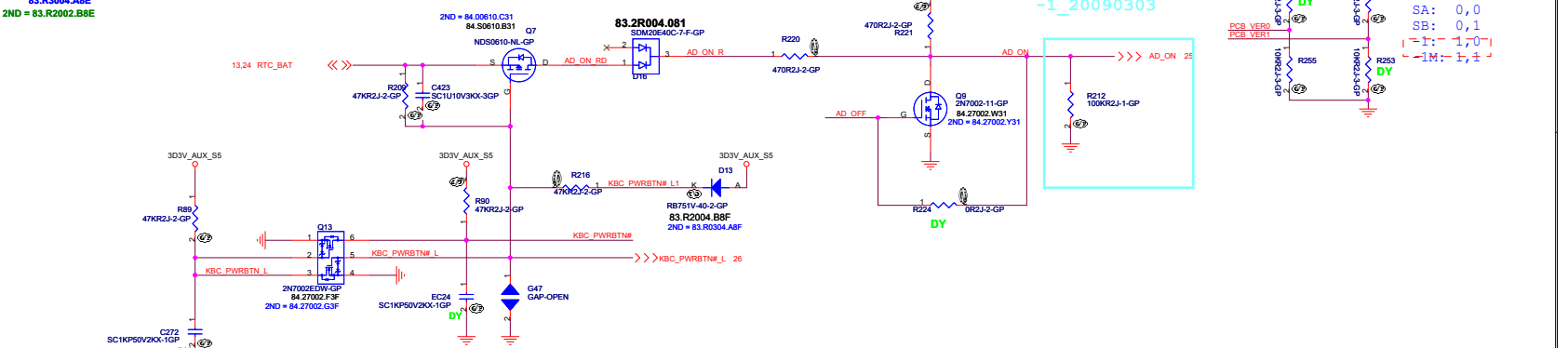
Date: Thursday, March 05, 2009 Sheet 27 of 40



Internal Keyboard Connector



GREEN ADAPTER CIRCUIT



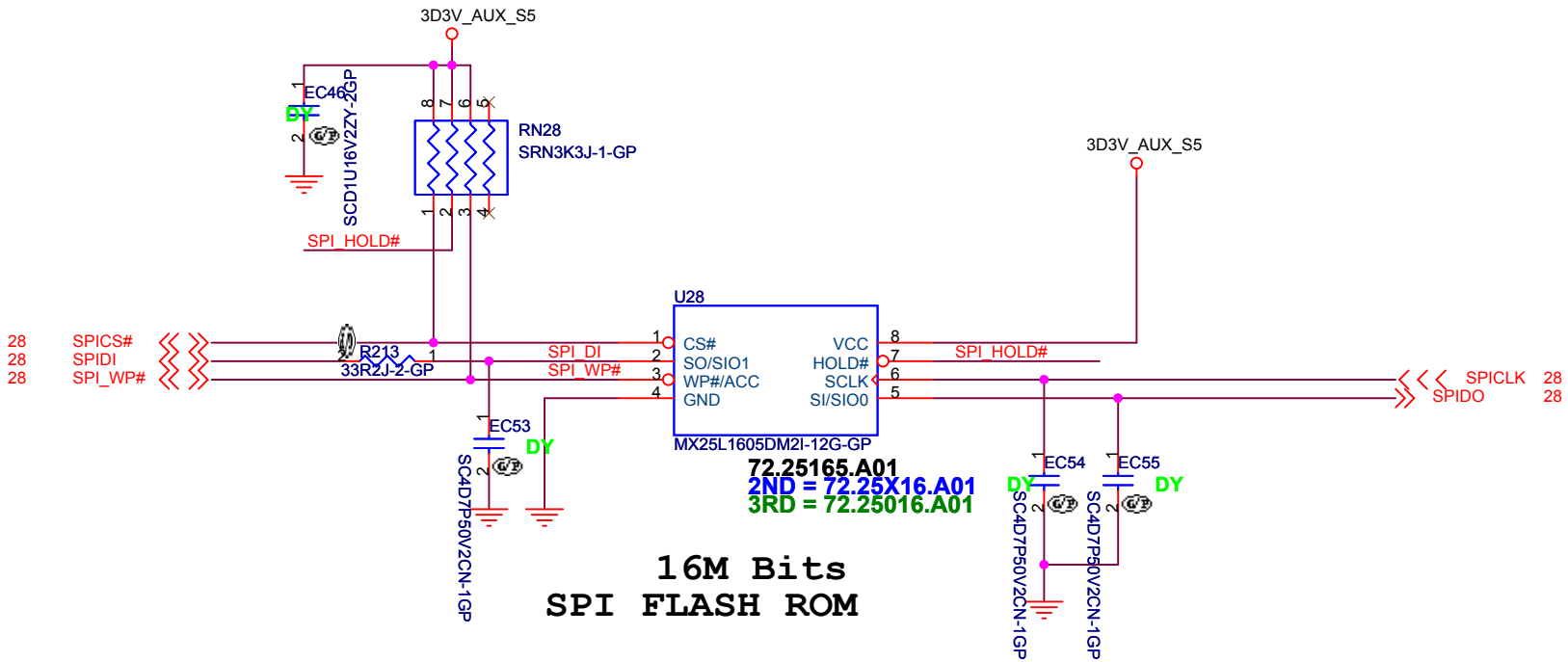
MB PIN DEFINE: 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
 KB PIN DEFINE: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

24 K/B 1

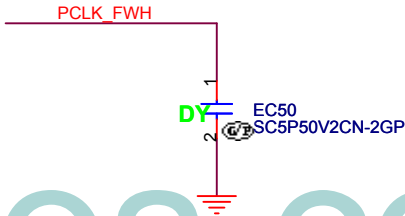
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<Core Design>

Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.		
Title: KBC WPC773		
Size: A2	Document Number: JM41 UMA	Rev: 1
Date: Monday, March 16, 2009	Sheet: 28	of: 40



GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

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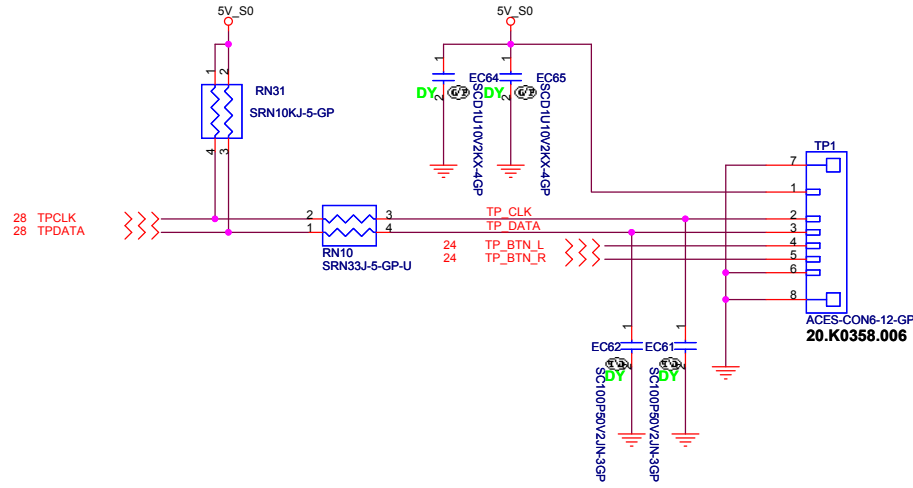
Title: **BIOS**

Size	Document Number	Rev
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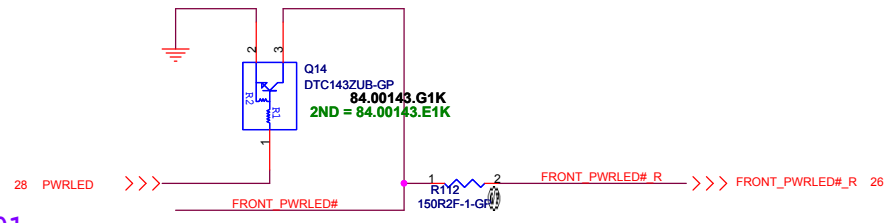
TOUCH PAD



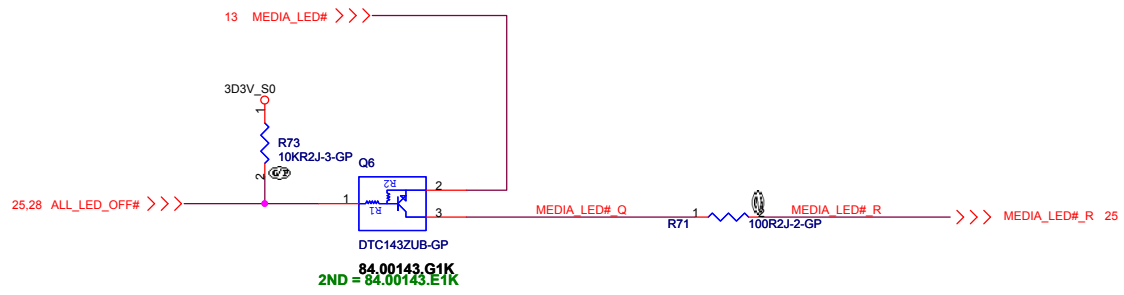
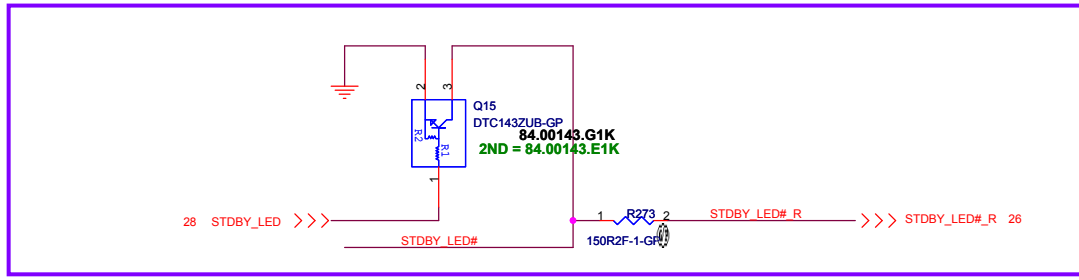
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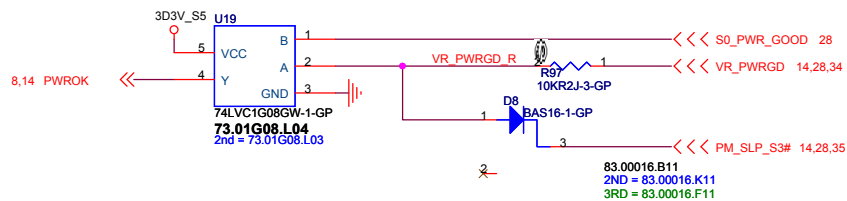
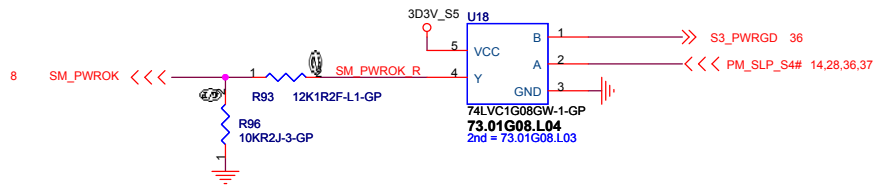
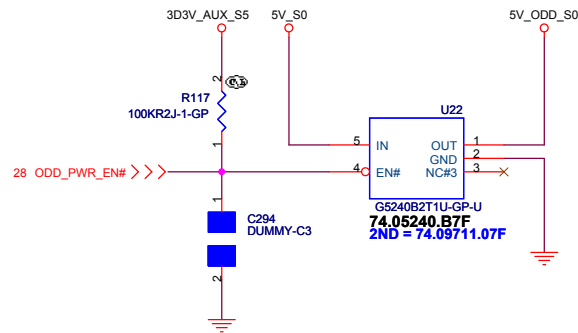


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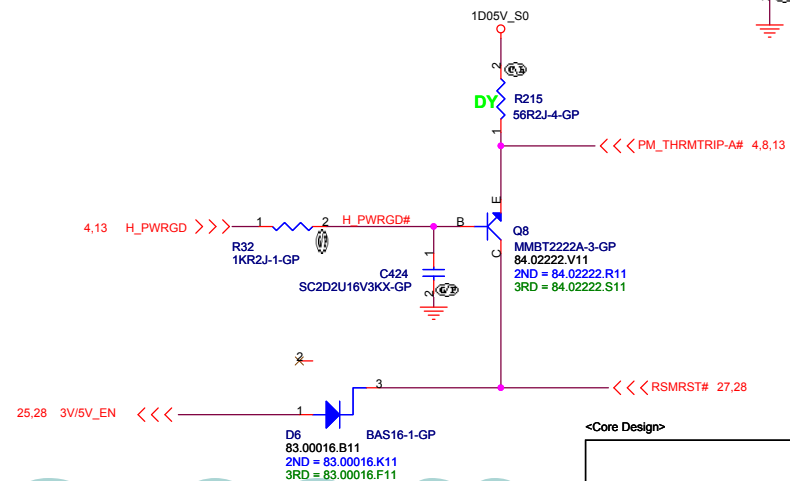
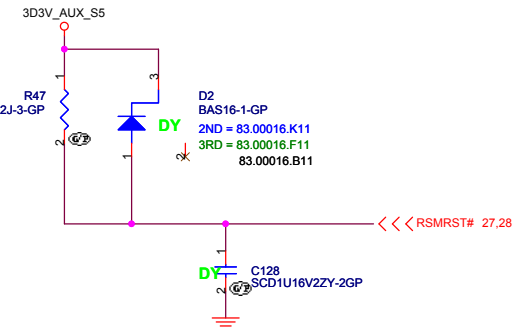
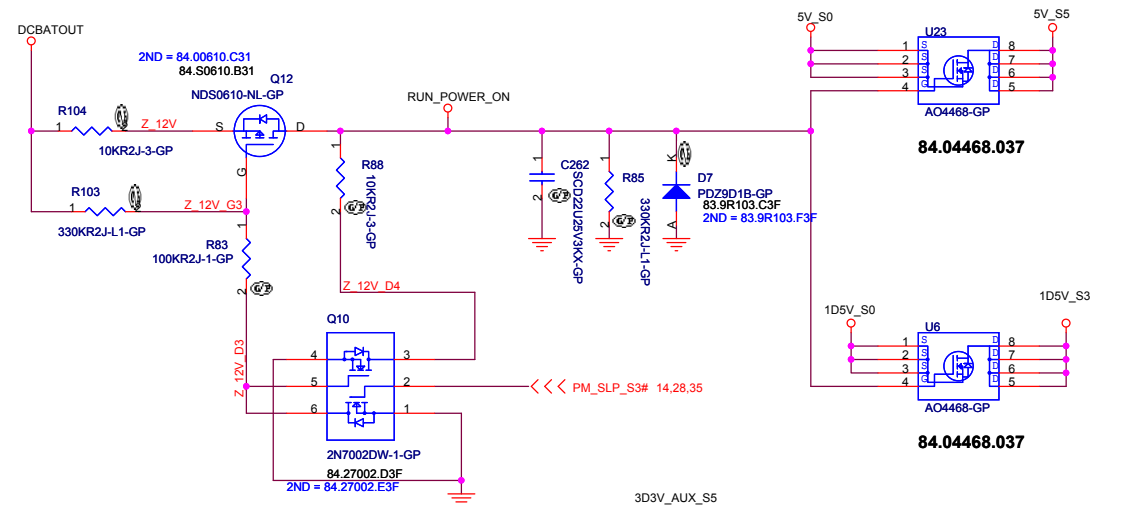
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ODD Power



Run Power



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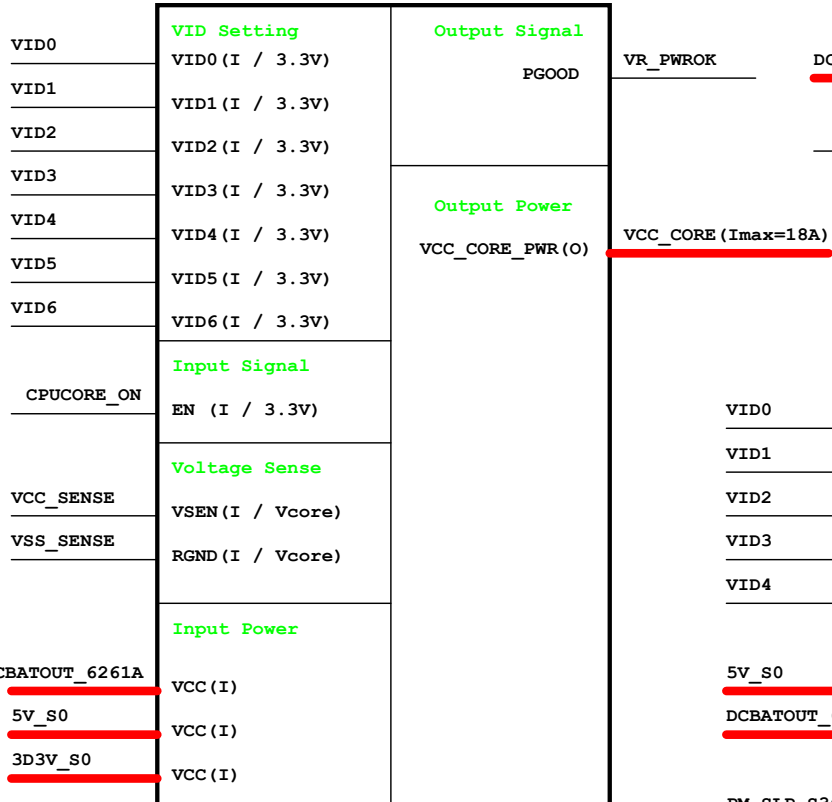
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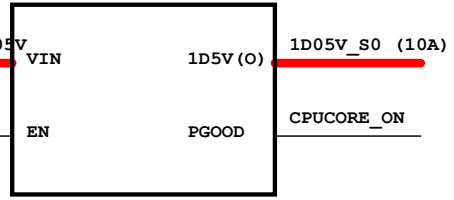
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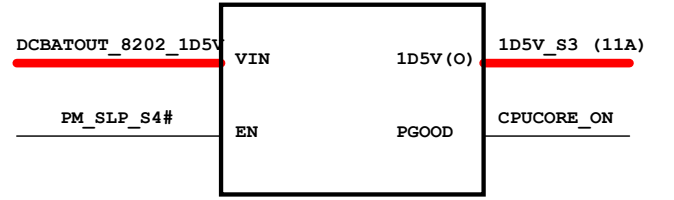
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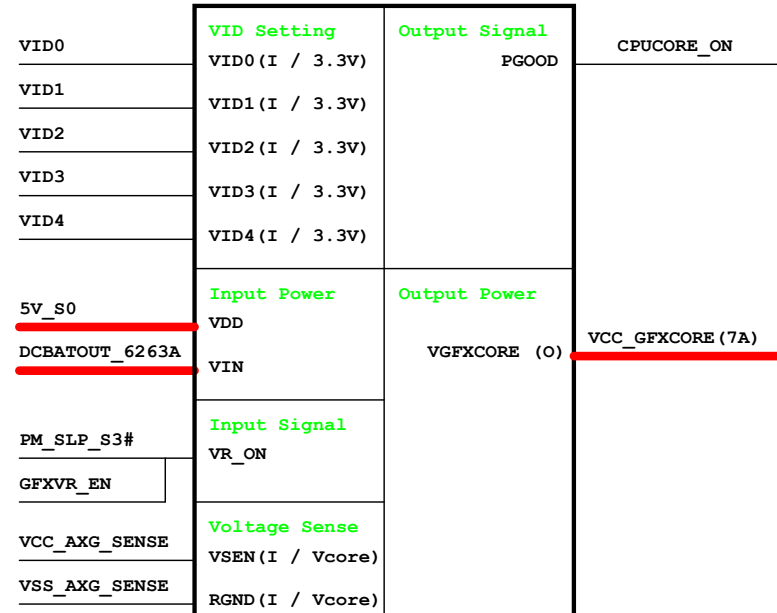
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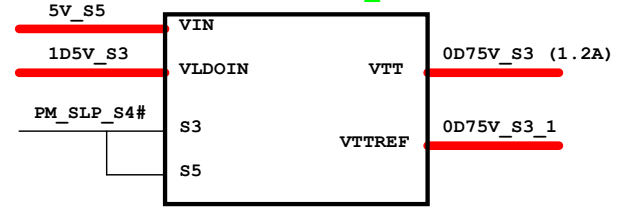
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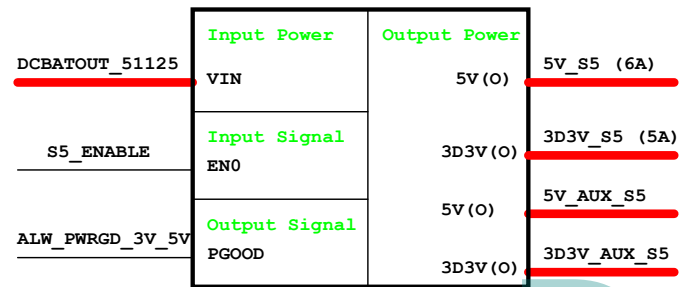
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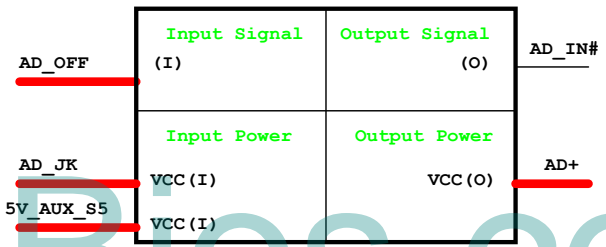
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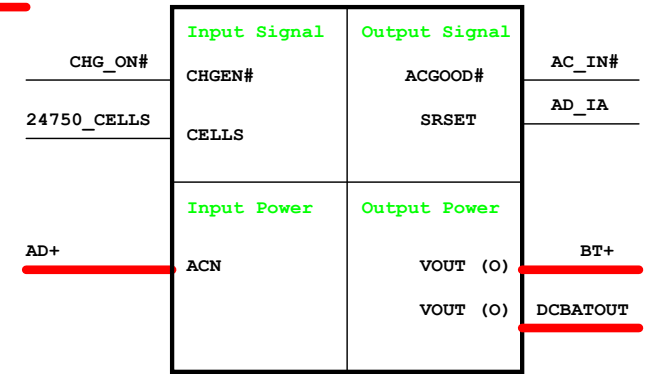
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5V/3D3V



Adapter



Charger MAX8731A



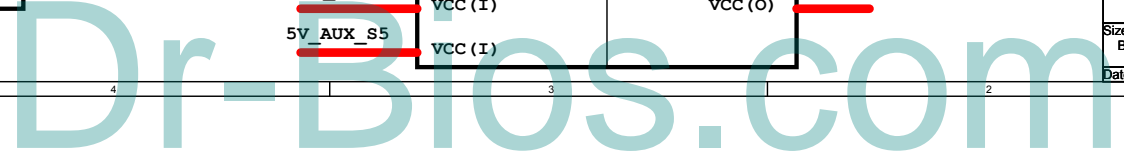
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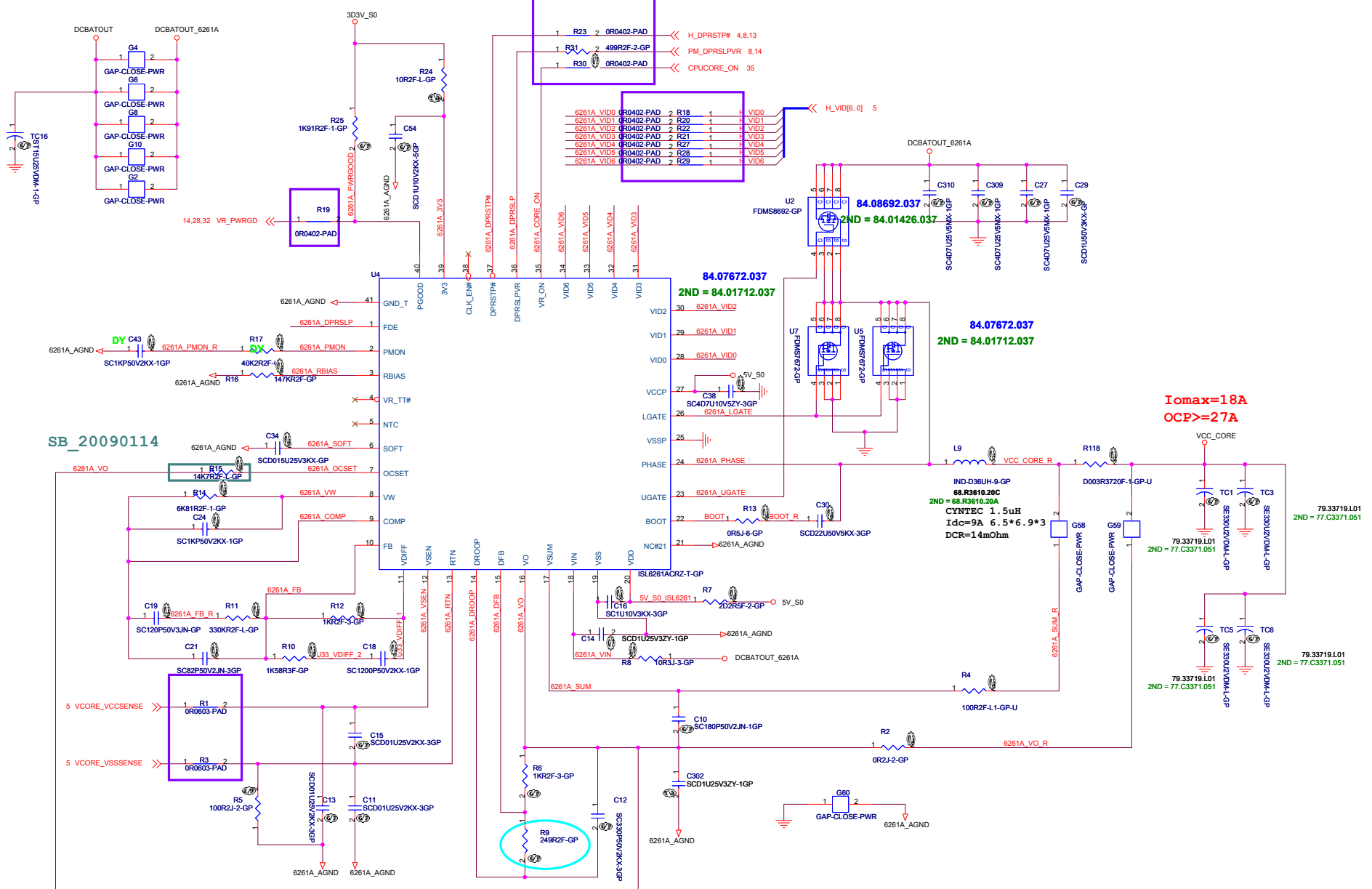
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SB_20090114

SB_20090203

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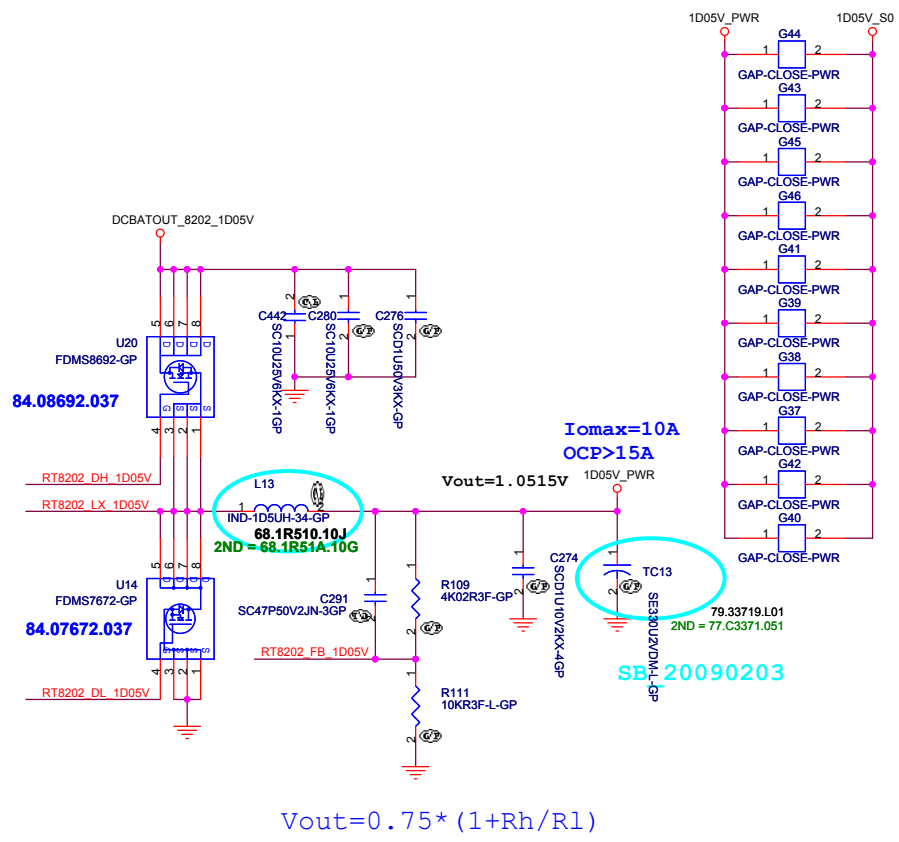
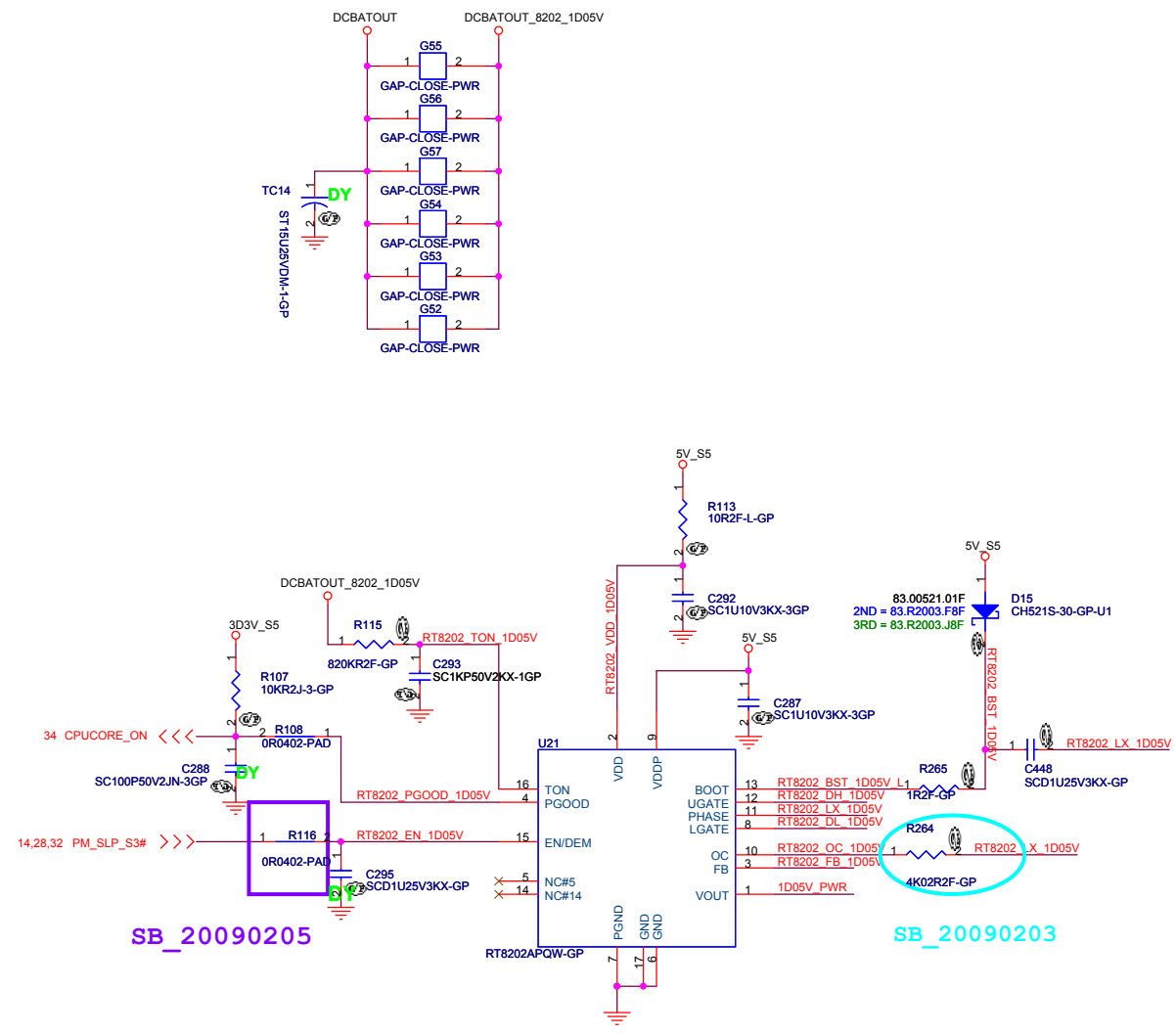
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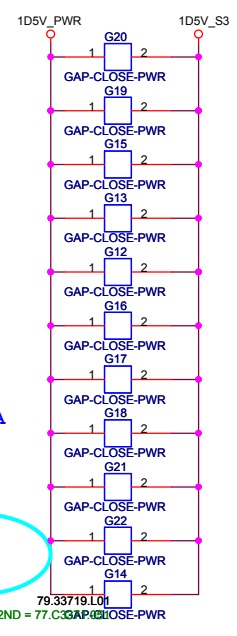
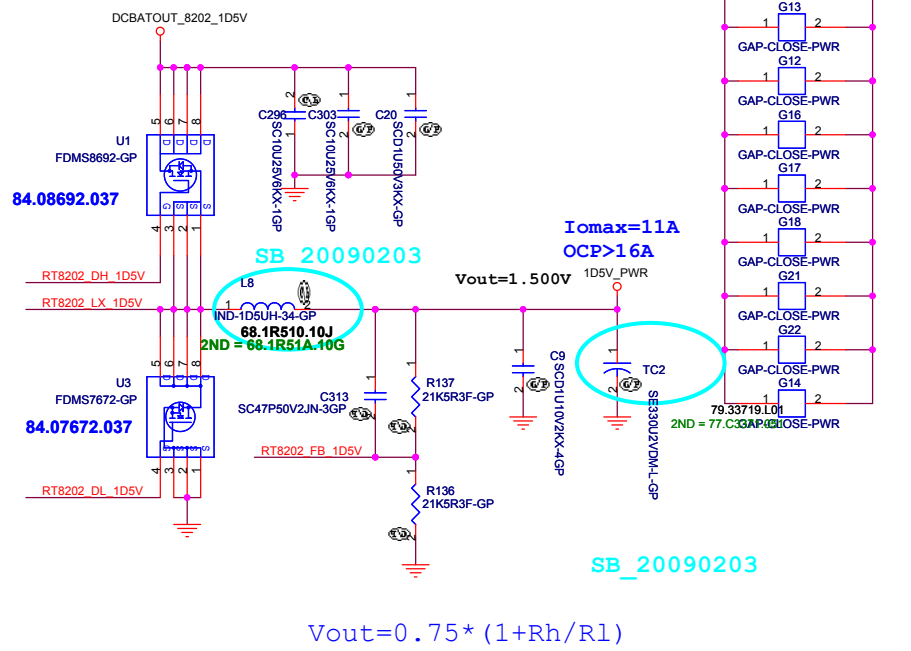
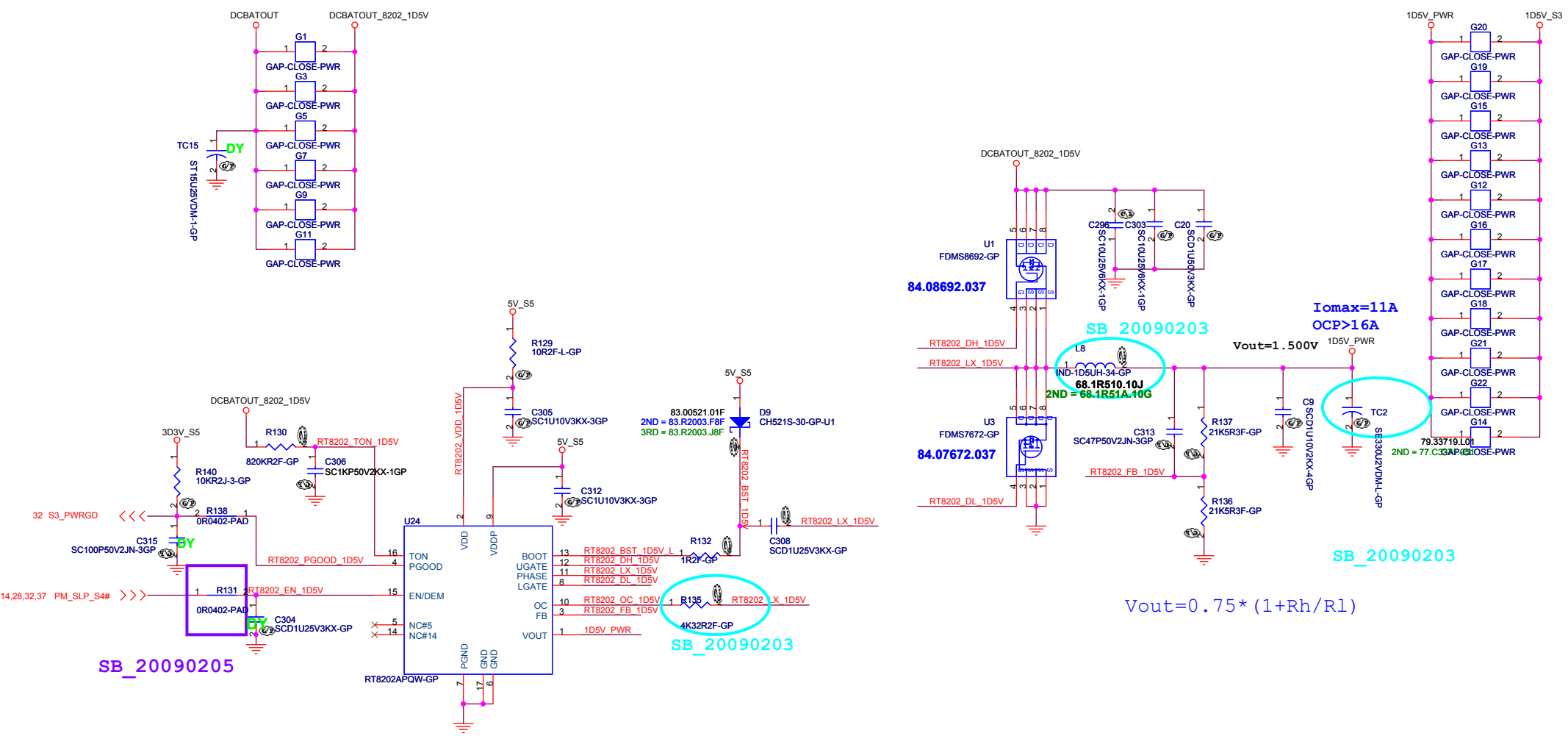
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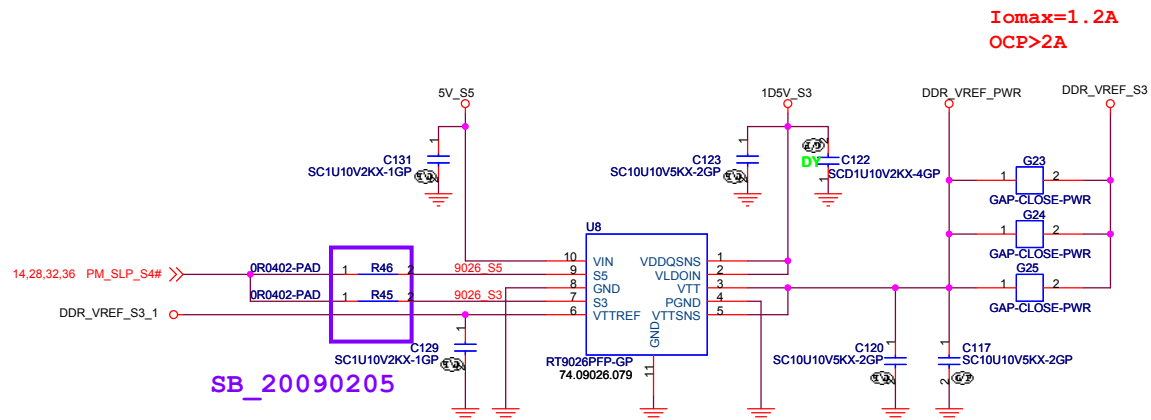
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$$V_{out} = 0.75 * (1 + R_h/R_l)$$

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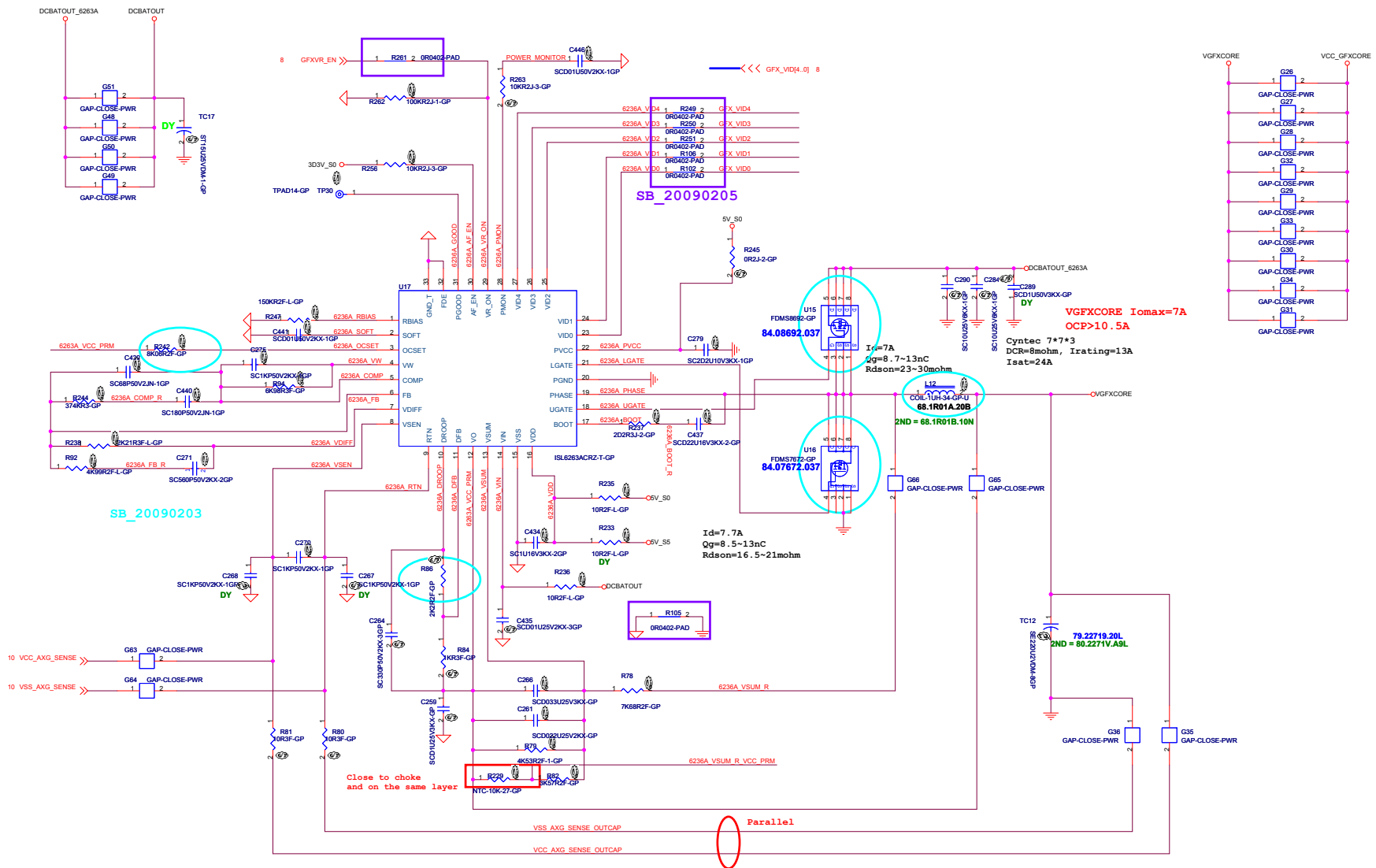
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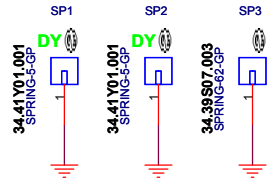
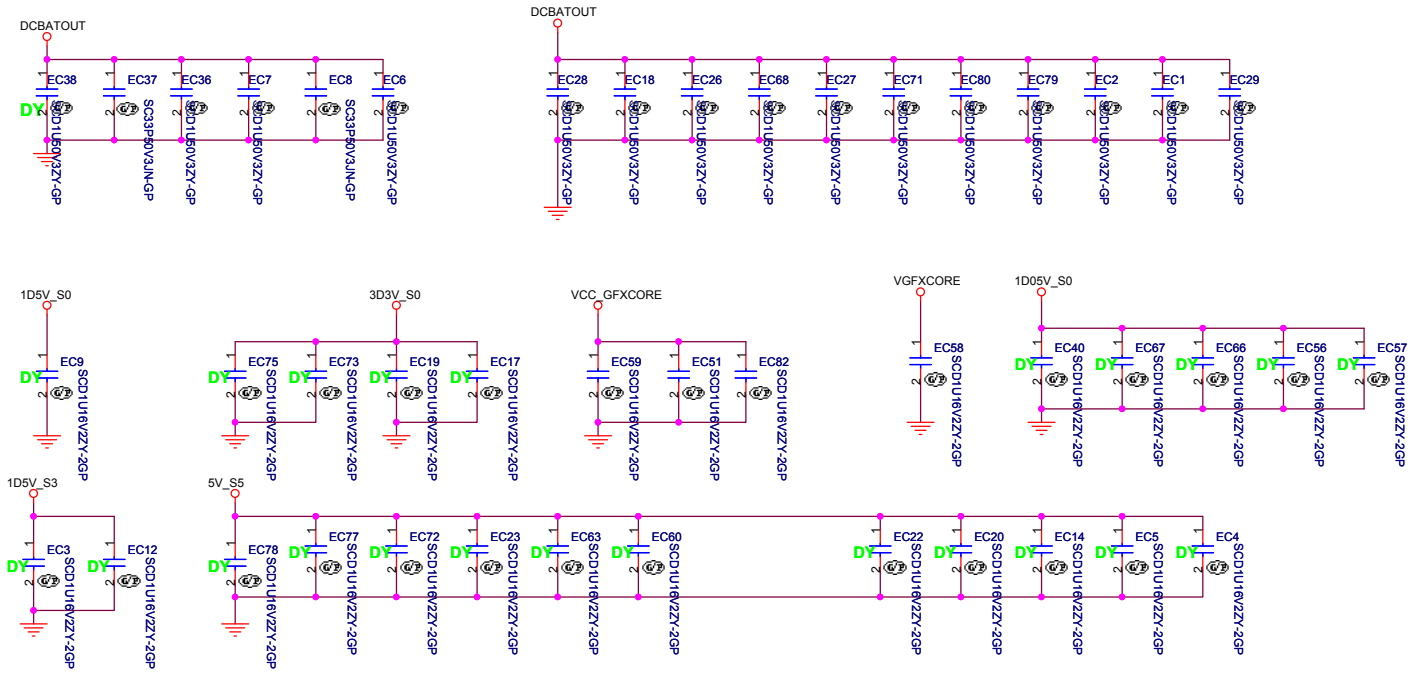
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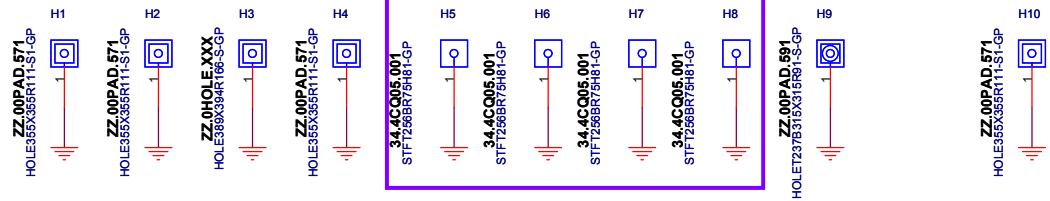
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Title: **EMI/Spring/Boss**

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Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi, Taipei Hsien 221, Taiwan, R.O.C.		
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