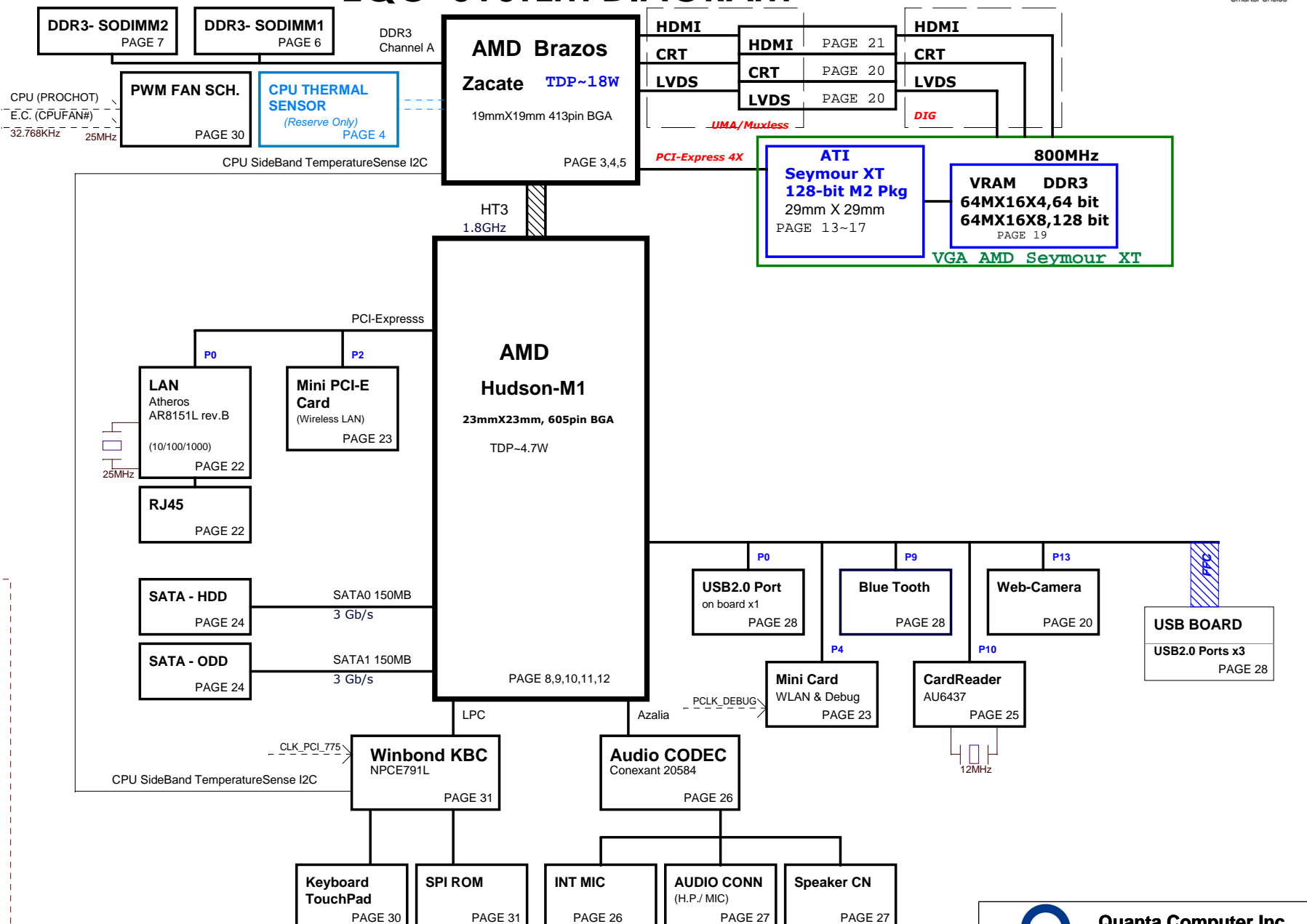


# ZQG SYSTEM DIAGRAM

**PCB STACK UP**

LAYER 1 : TOP  
 LAYER 2 : GND  
 LAYER 3 : IN1  
 LAYER 4 : IN2  
 LAYER 5 : VCC  
 LAYER 6 : BOT

IV@ ----> iGPU / PWW control  
 SW@ ----> Switchable iGPU & dGPU  
 SWS@ ----> VRAM / Strap / BACO option  
 SP@ ----> Board ID / VBIOS option / CPU



- CHARGER (ISL88731A) PAGE 32
- AMD CPU CORE (ISL6265) PAGE 34 CPU
- NB\_CORE (UP6111AQDD) PAGE 36 NB
- 0.9V/DDR 1.5V (RT8207) PAGE 37
- SYSTEM 5V/3V (RT8206) PAGE 33
- 1.1V (UP6111AQDD) PAGE 35
- Discharge / Thermal protec PAGE 40

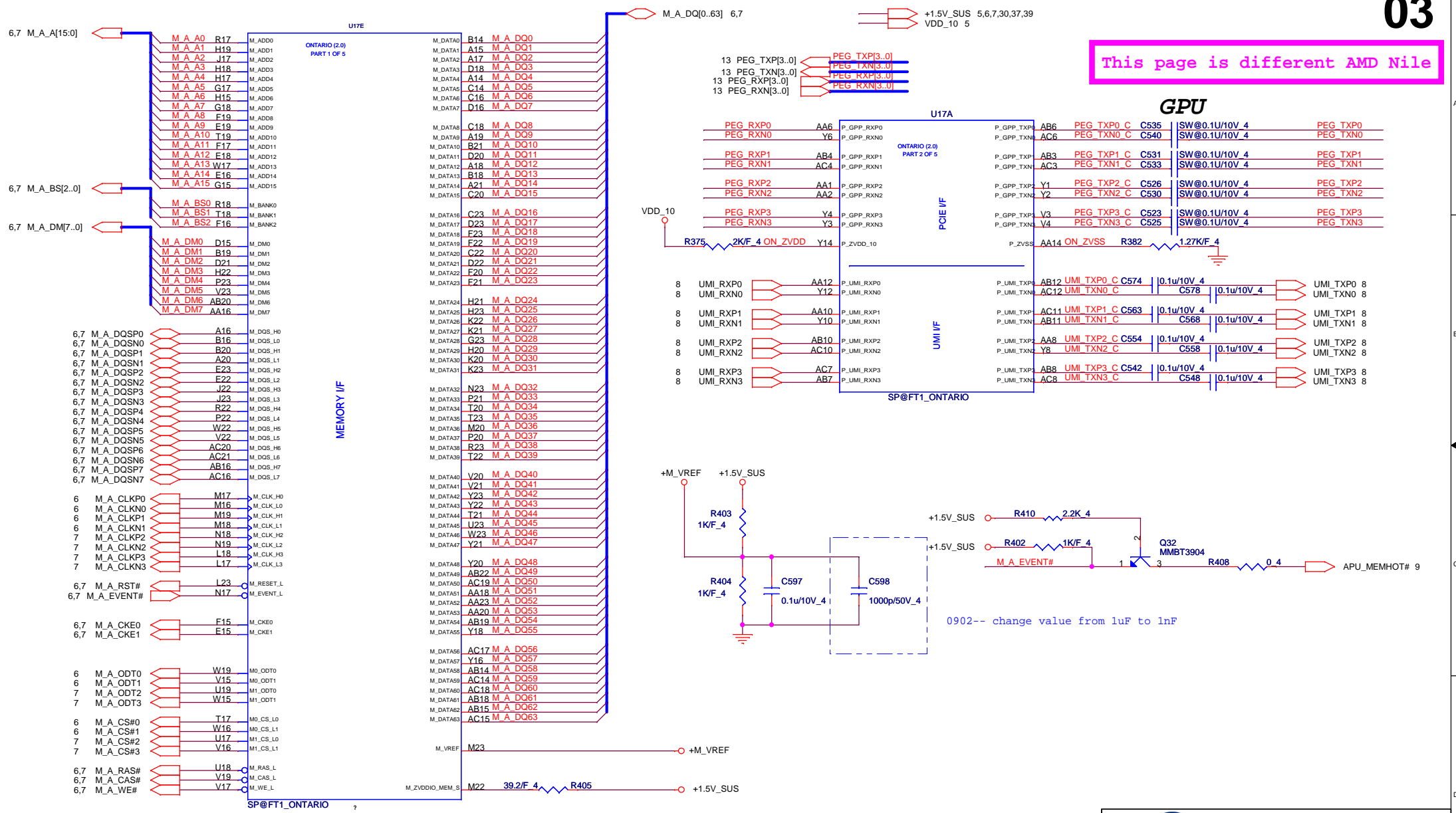
**Quanta Computer Inc.**  
 PROJECT : ZQG

Size	Document Number	Rev
	<b>Block Diagram</b>	1A
Date: Monday, November 01, 2010	Sheet	1 of 41

Dr-Bios.com

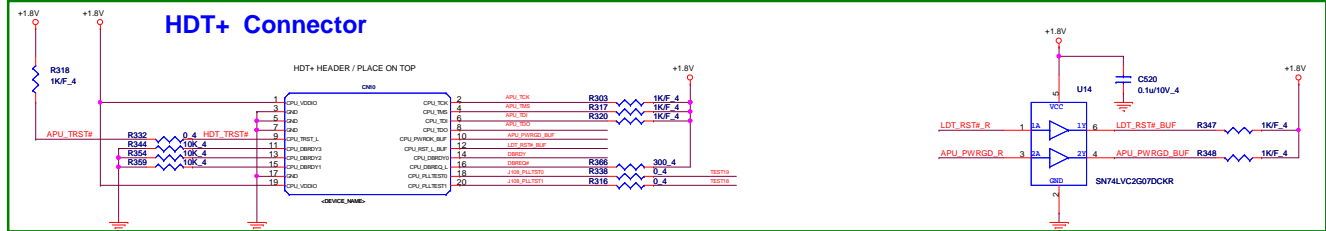
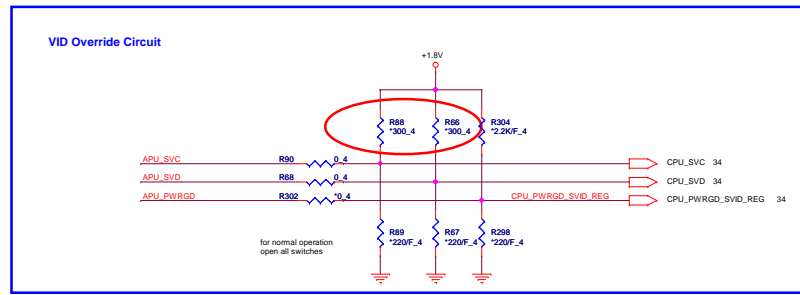
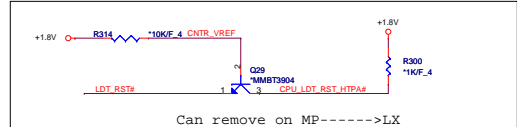
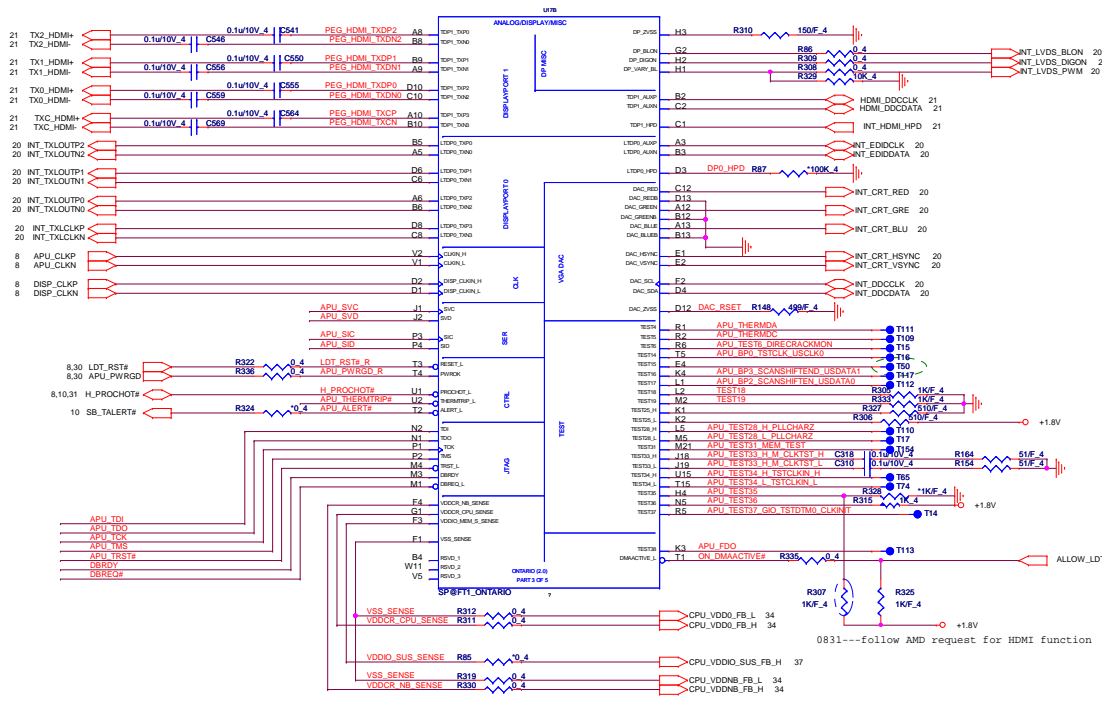
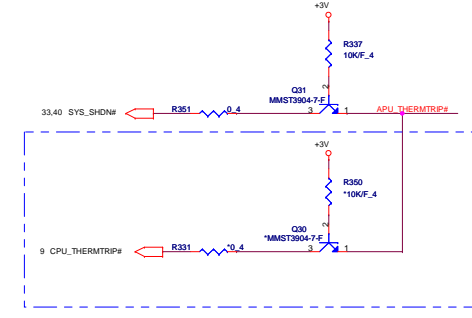
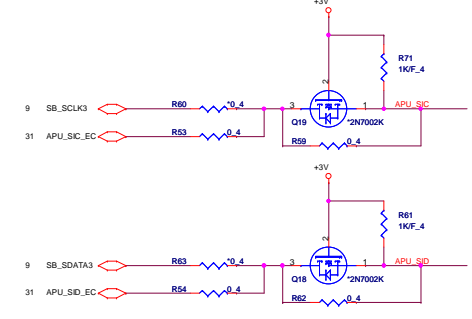
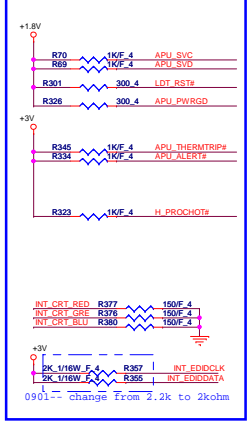


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**PROJECT : ZQG**

Size	Document Number	Rev
	<b>ONTARIO MEM &amp; PCIE I/F(1/3)</b>	1A
Date:	Monday, November 01, 2010	Sheet 3 of 41

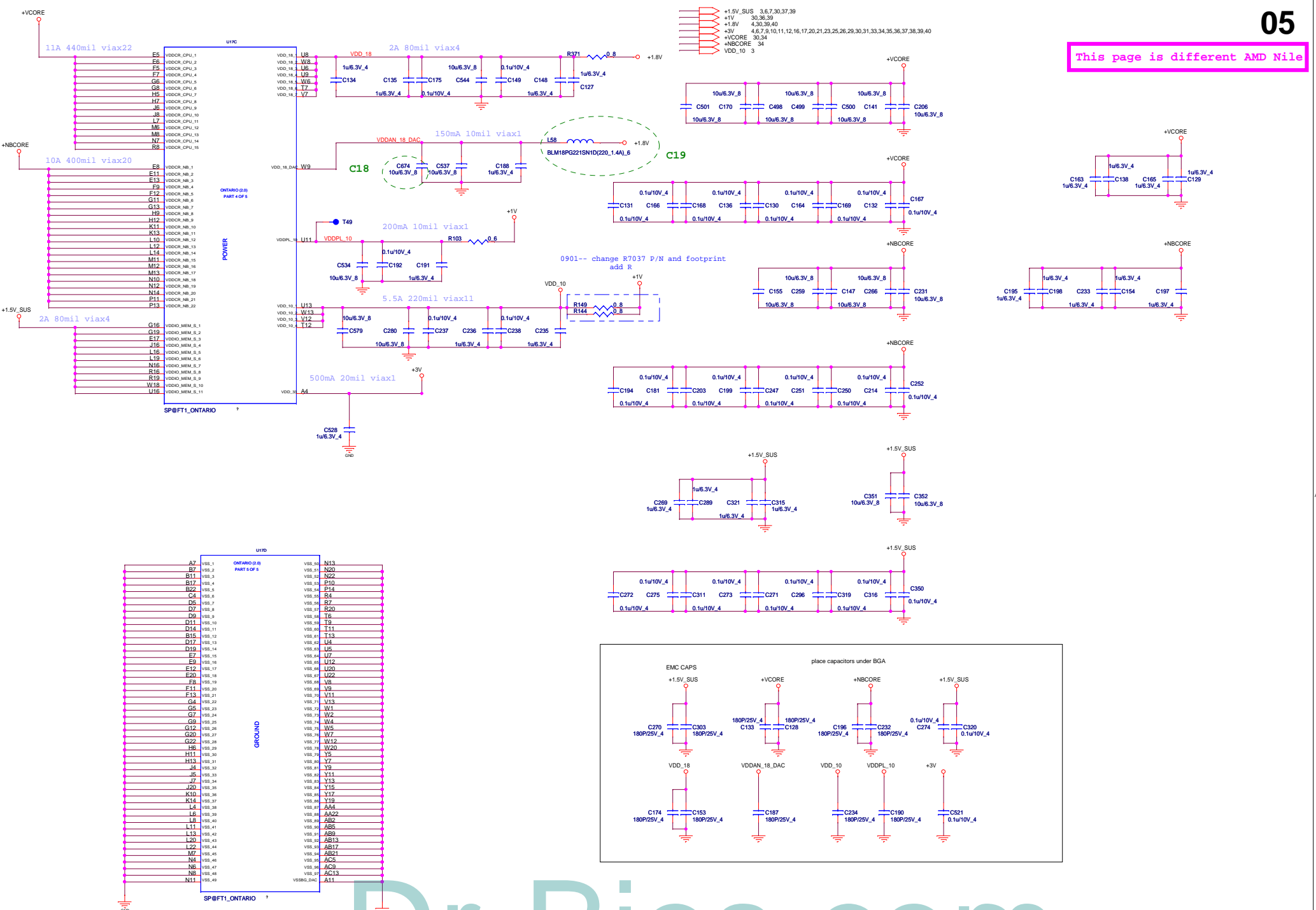


**Quanta Computer Inc.**  
PROJECT : ZQG

Size Document Number  
Date: Monday, November 01, 2010 Sheet 4 of 41

Rev  
ONTATIO DISPLAY/CLK/MI(2/3)  
1A

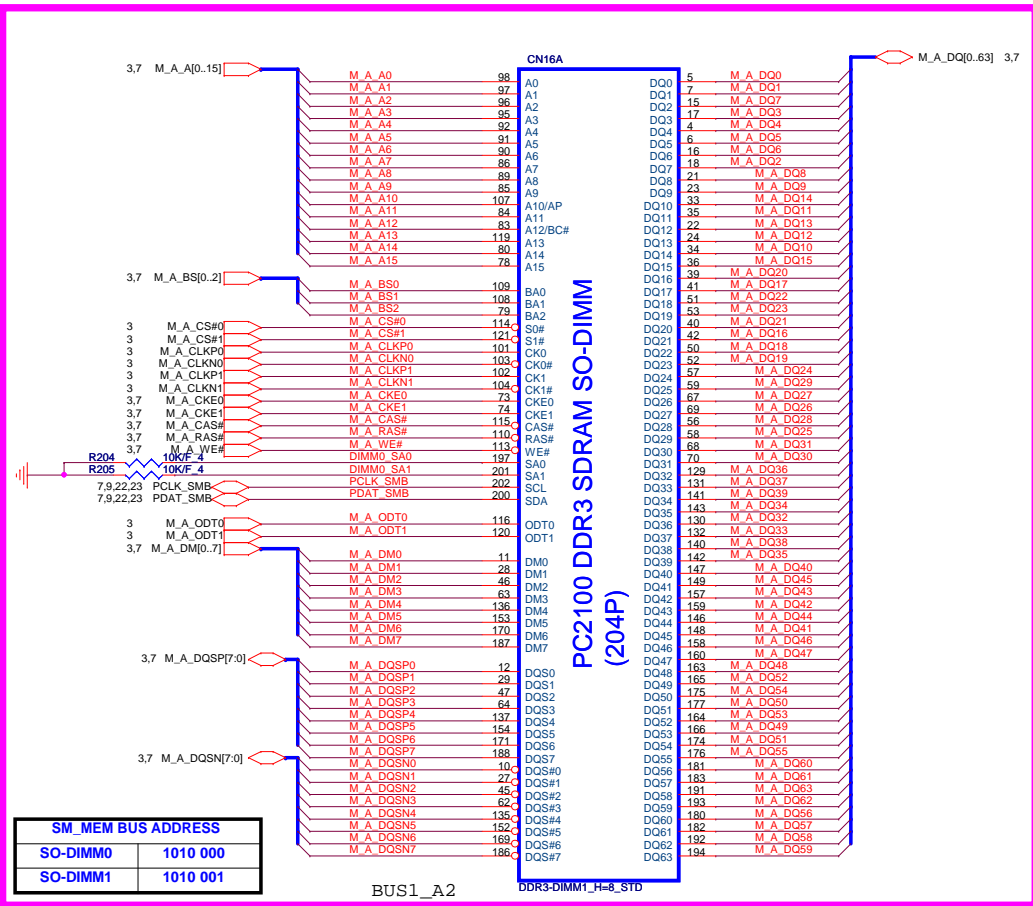
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0830--P/N and footprint are follow ZR7B

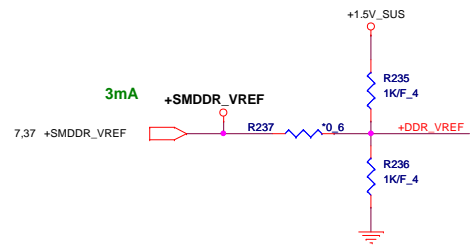
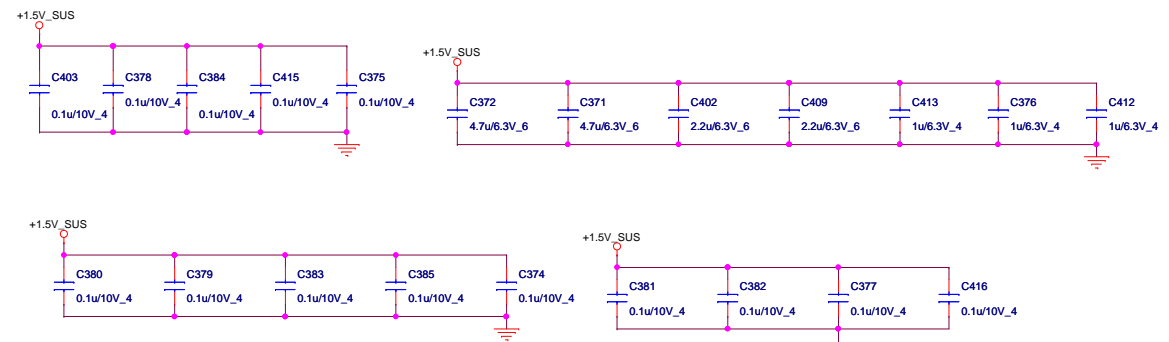
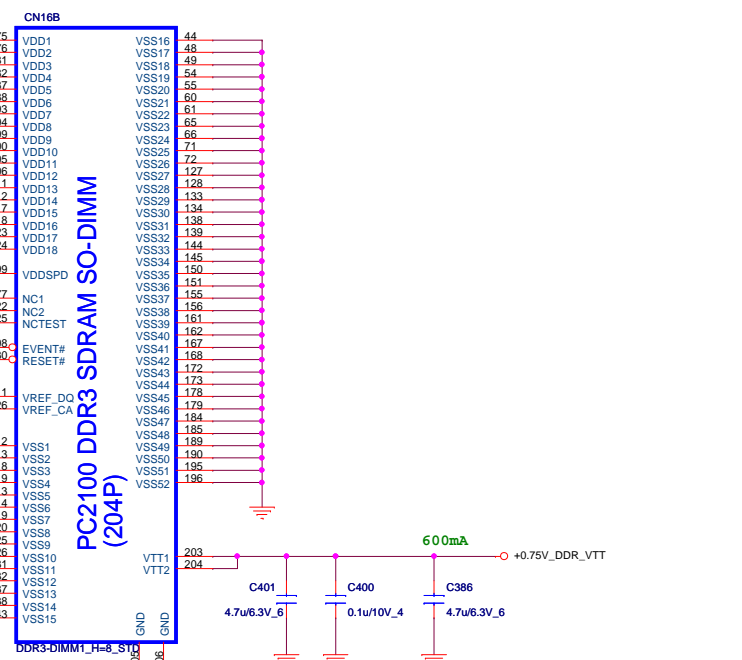
- +1.5V\_SUS 3,5,7,30,37,39
- +0.75V\_DDR\_VTT 7,37
- +3V 4,5,7,9,10,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40



SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

BUS1\_A2

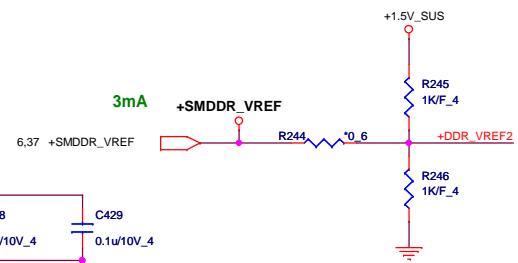
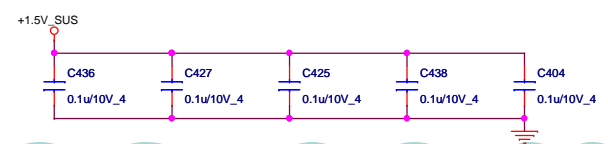
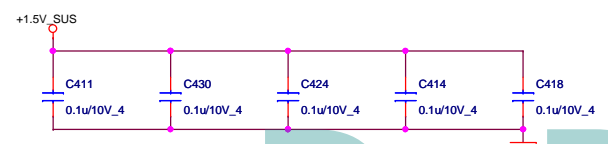
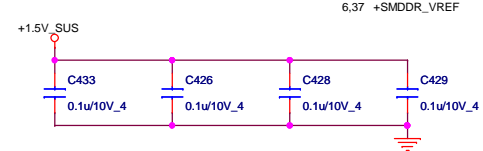
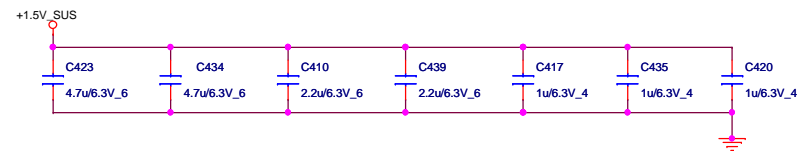
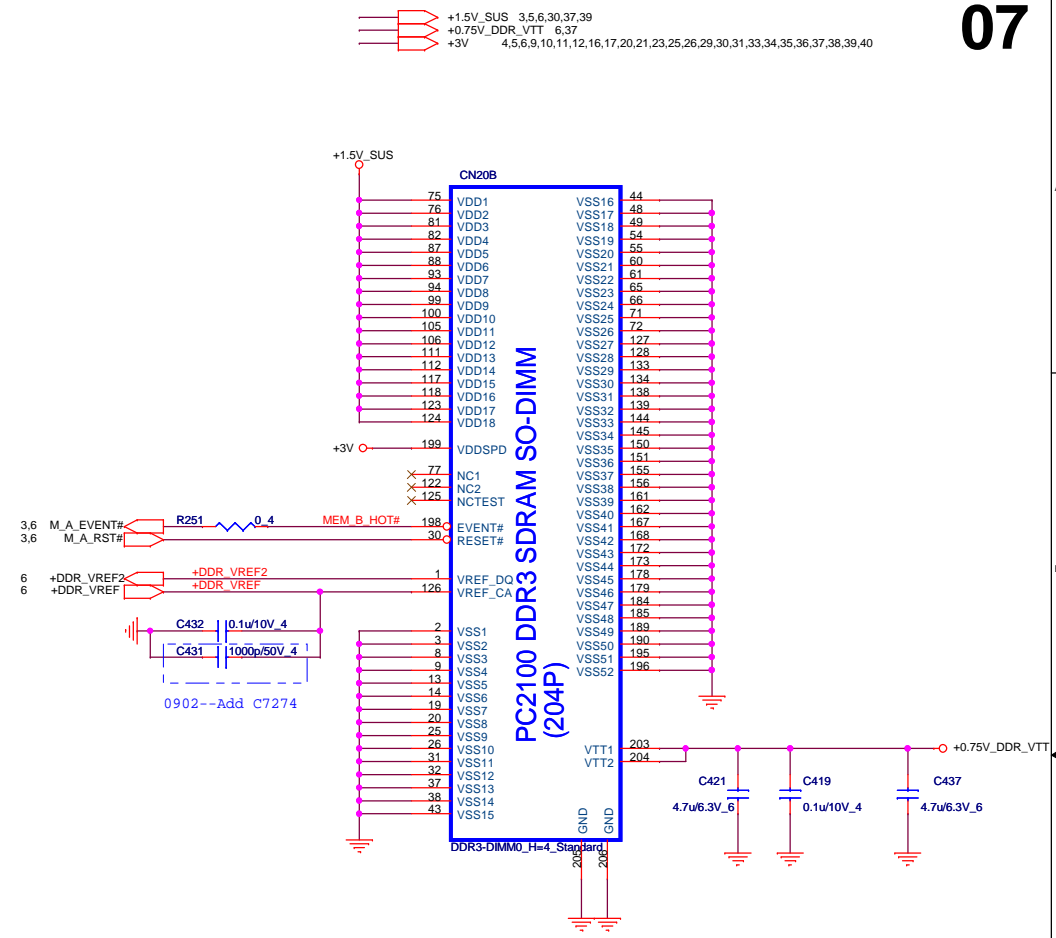
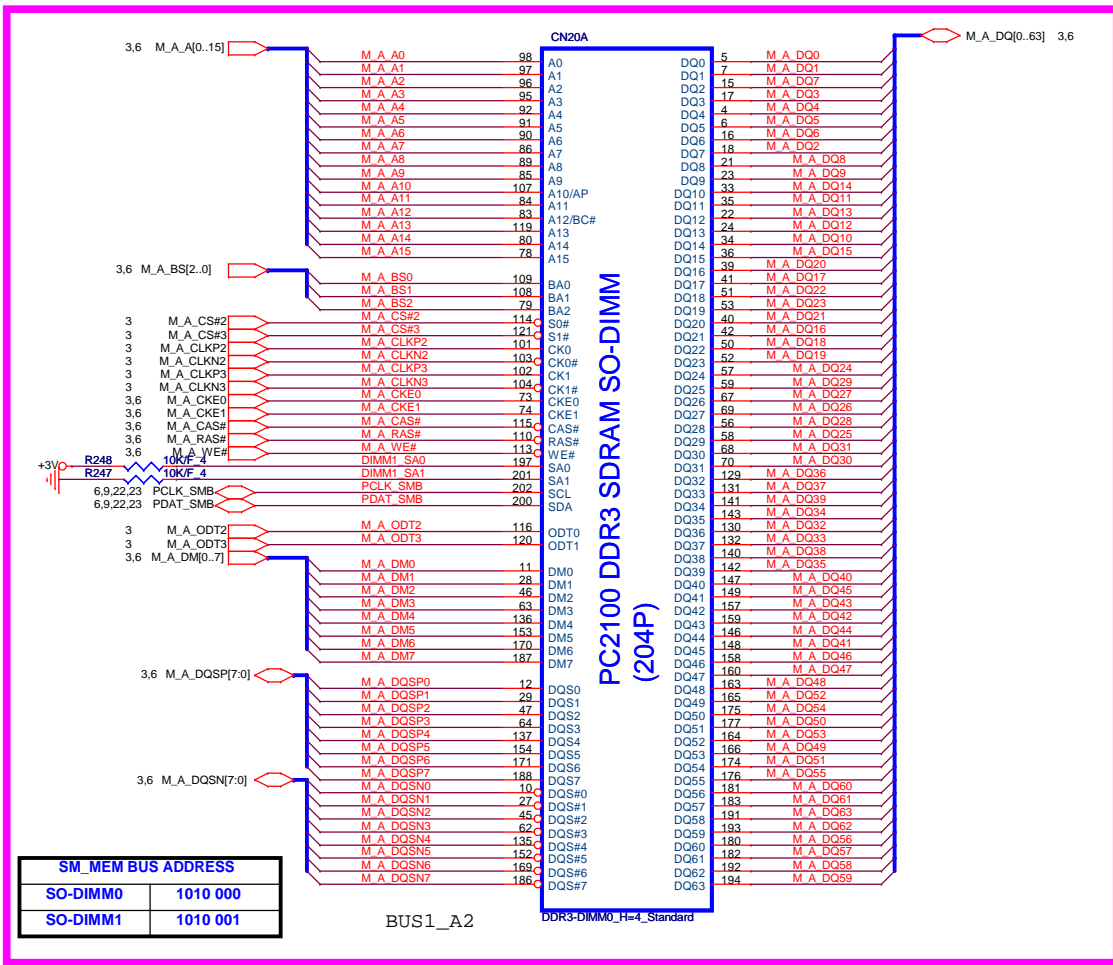
PC2100 DDR3 SDRAM SO-DIMM (204P)



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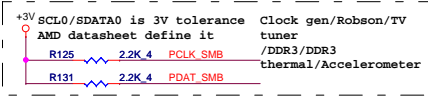
**Quanta Computer Inc.**  
PROJECT : ZQG

Size	Document Number	Rev
	<b>DDR3 SO-DIMM (STD)</b>	1A
Date:	Monday, November 01, 2010	Sheet 6 of 41

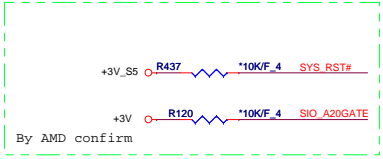




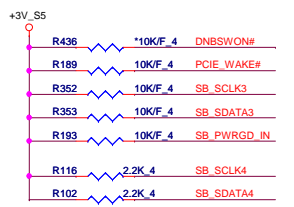




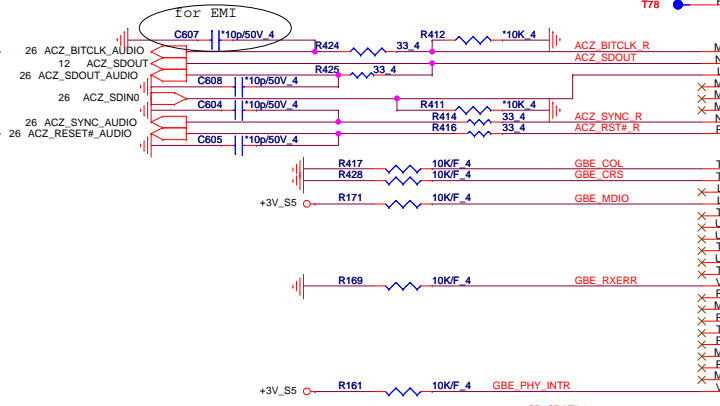
SB/ PWR\_GOOD / VDDIO\_33\_5



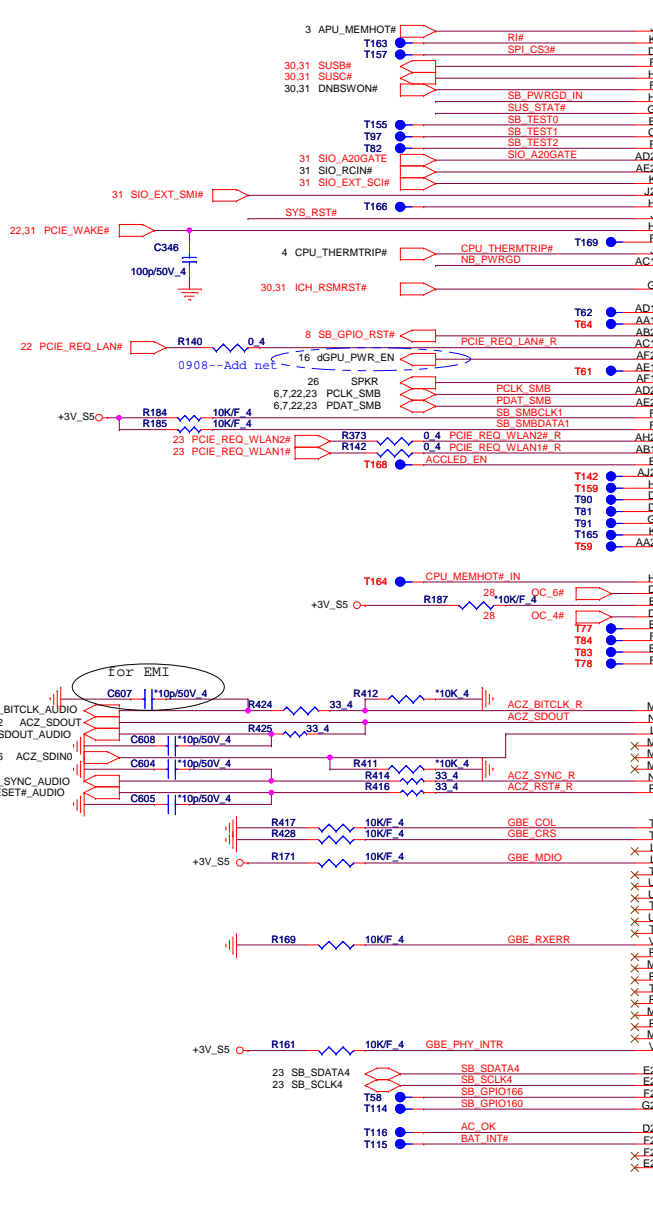
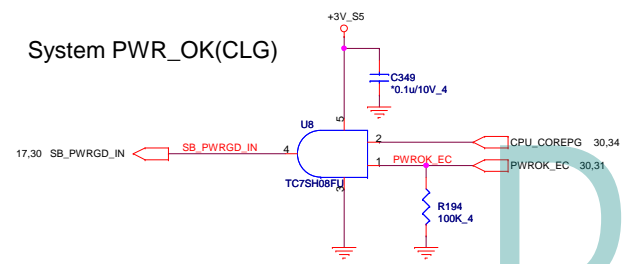
By AMD confirm



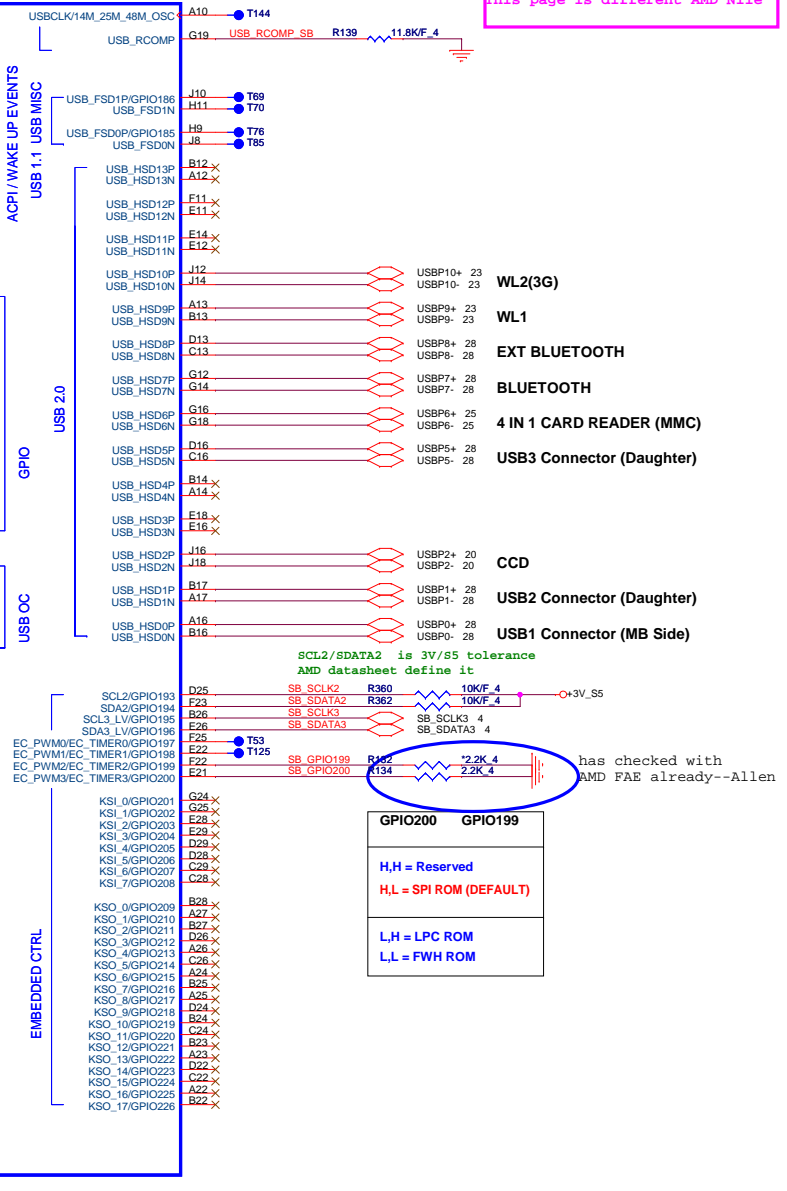
To Azalia HD audio interface is 3.3V5 voltage



System PWR\_OK(CLG)



Hudson M1 Part 4 of 5



SCL2/SDATA2 is 3V/S5 tolerance AMD datasheet define it

has checked with AMD FAE already--Allen

GPIO200	GPIO199
H,H = Reserved	H,L = SPI ROM (DEFAULT)
L,H = LPC ROM	L,L = FWX ROM



SATA PORT 0,1,2,3  
can support AHCI  
mode

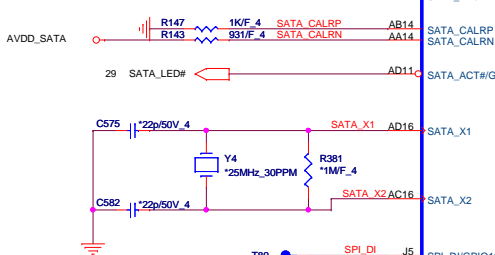
PLACE SATA AC COUPLING  
CAPS CLOSE TO HUDSON M1

**SATA HDD**  
24 SATA\_TXP0  
24 SATA\_TXN0  
24 SATA\_RXN0  
24 SATA\_RXP0

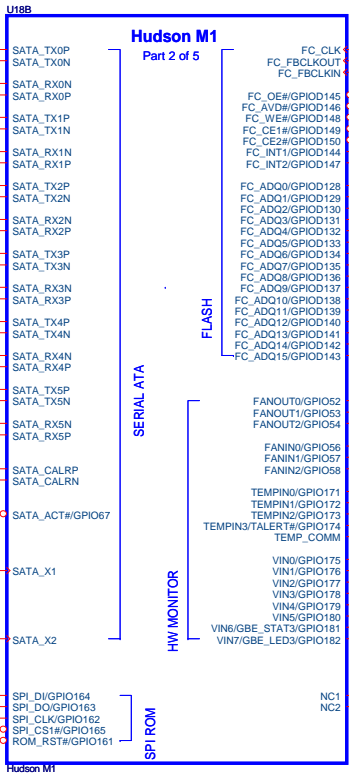
**SATA ODD**  
24 SATA\_TXP1  
24 SATA\_TXN1  
24 SATA\_RXN1  
24 SATA\_RXP1

XTLVDD\_SATA-- SATA  
crystal power  
PLVDD\_SATA--  
SATA PLL  
POWER

PLACE SATA\_CAL RES  
VERY CLOSE TO BALL  
OF HUDSON M1

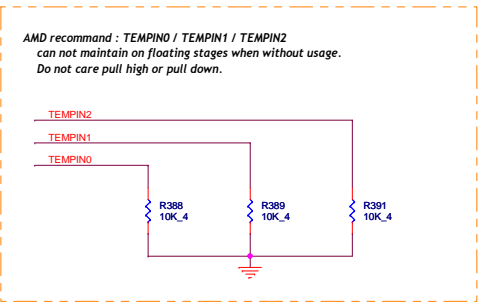


- T89 ● SPI DI J5
- T96 ● SPI DO E2
- T160 ● SPI CLK K4
- T79 ● SPI CS1# K3C
- T162 ● ROM\_RST# G2C



- AVDD\_SATA 11
- +3V 4,5,6,7,9,11,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40
- +3V\_S5 8,9,11,12,22,28,29,30,33

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AMD recommend : TEMPIN0 / TEMPIN1 / TEMPIN2  
can not maintain on floating stages when without usage.  
Do not care pull high or pull down.

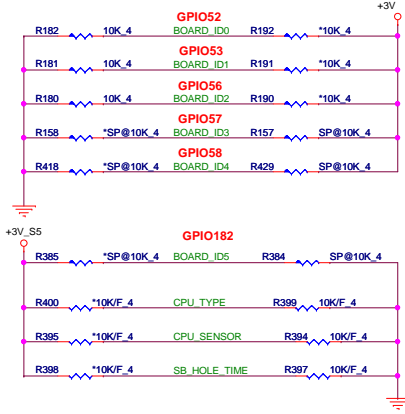
0831--modify location

MB ID

<b>CPU THERMAL</b>	<b>GPIO52</b>	<b>GPIO57</b>
External	1	( Dis ) SW 1
SB-TSI	0	UMA 0
<b>SB8XX Hold Time</b>	<b>GPIO53</b>	<b>GPIO58</b>
1.2V	1	VRAM - 800 1
1.1V	0	VRAM-900 0
<b>DU1/MK2</b>	<b>GPIO56</b>	<b>GPIO182</b>
MK2.0 AMD	1	PX4.0 1
DU1.0 AMD	0	PX3.0 0



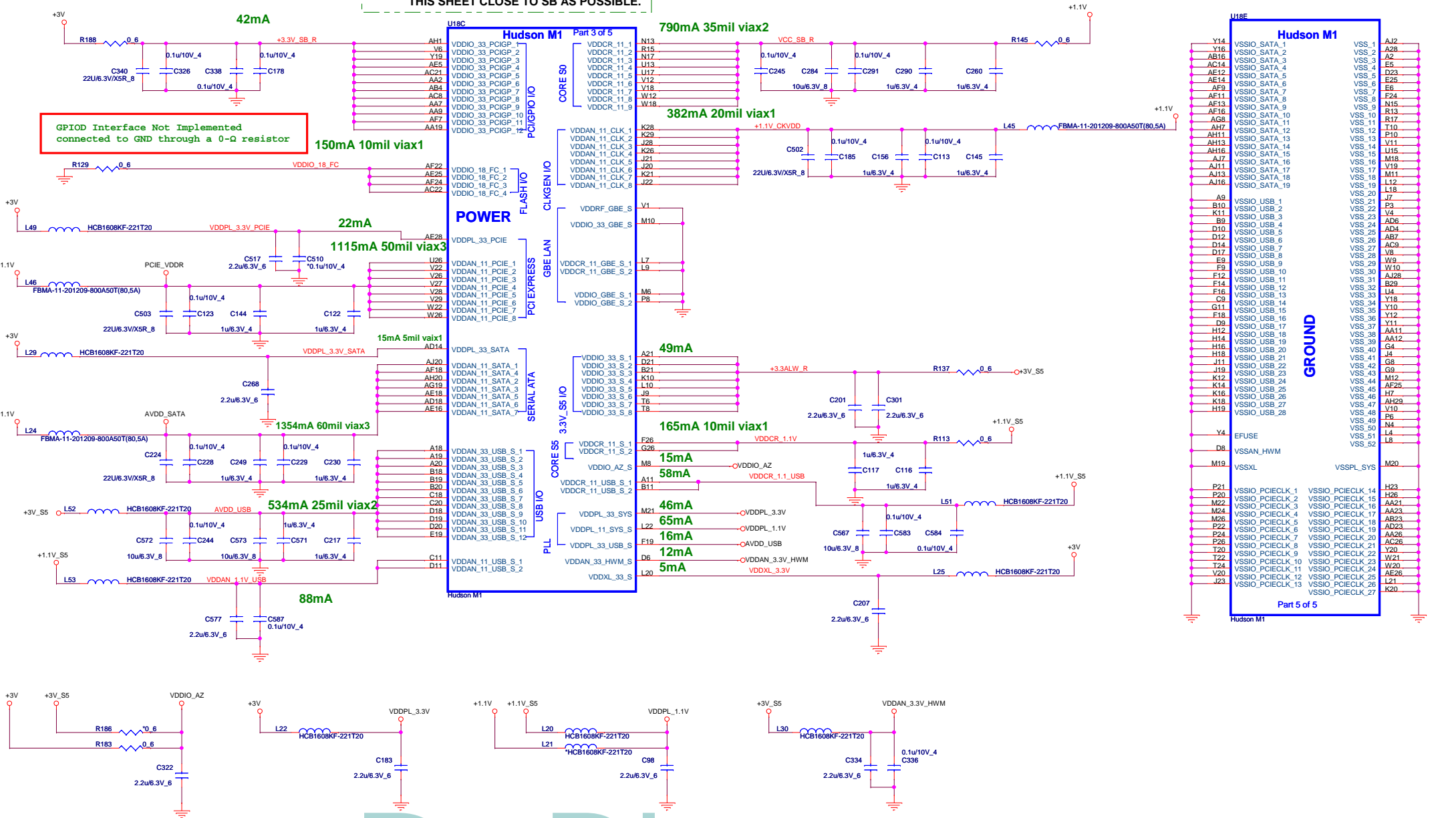
0831--add circuit



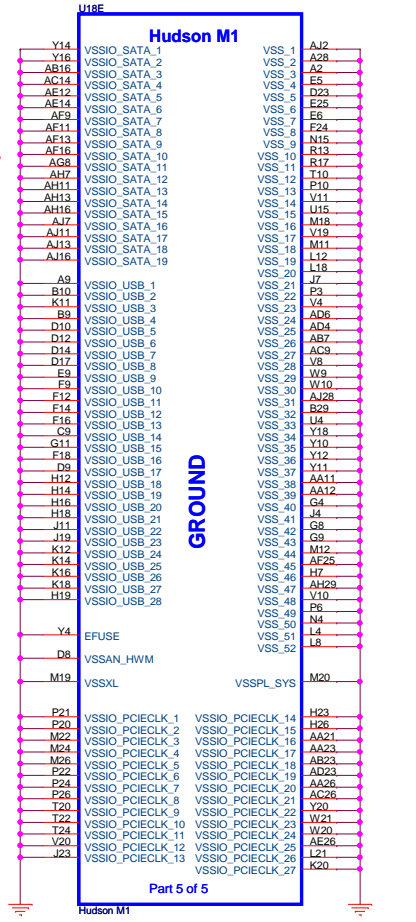
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- +3V 4,5,6,7,9,10,12,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40
- +1.1V 30,35
- +3V\_S5 8,9,10,12,22,28,29,30,33
- +1.1V\_S5 30,35
- AVDD\_SATA 10
- VDDIO\_AZ 12

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



GPIO Interface Not Implemented connected to GND through a 0-Ω resistor



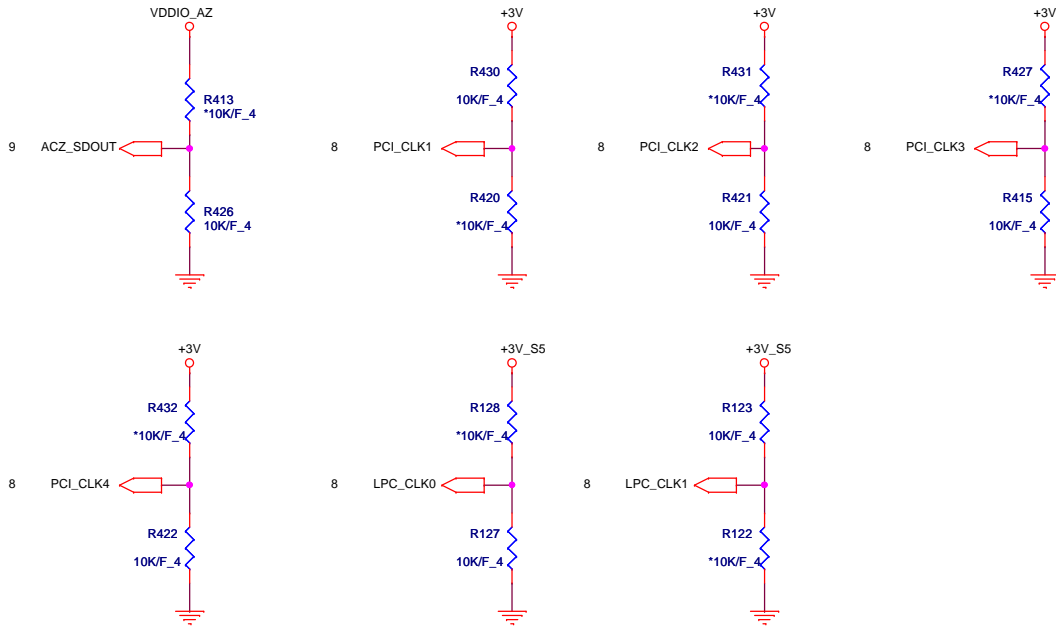
Dr-Bios.com



**OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.**

internal have pull Hi 10K , confirm AMD ward this pull Hi not need

## REQUIRED STRAPS

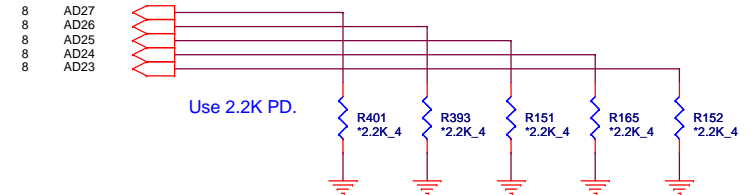


PCI\_CLK4 CPU/NB HT Clock Selection  
0 V - Reserved.  
3.3 V - Required setting for integrated clock mode.  
This strap is not used if the strap CLKGEN is configured for external clock generator mode.

VDDIO\_AZ 11  
+3V 4,5,6,7,9,10,11,16,17,20,21,23,25,26,29,30,31,33,34,35,36,37,38,39,40  
+3V\_S5 8,9,10,11,22,28,29,30,33

## DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



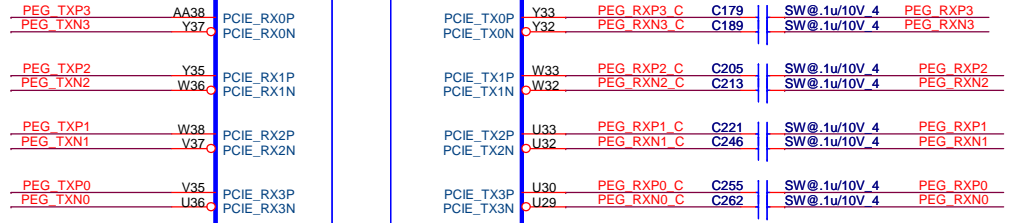
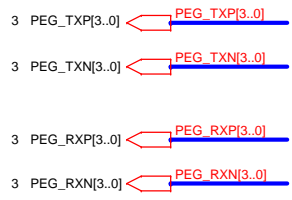
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

## REQUIRED STRAPS

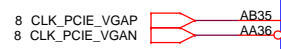
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
<b>PULL HIGH</b>	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
<b>PULL LOW</b>	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

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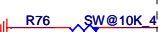
U15A



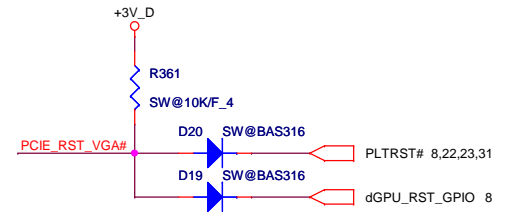
PCI EXPRESS INTERFACE



For Madison and Park the PWRGOOD ball must be connected to ground



SW@SEYMOUR\_M2



**Quanta Computer Inc.**  
 PROJECT : ZQG

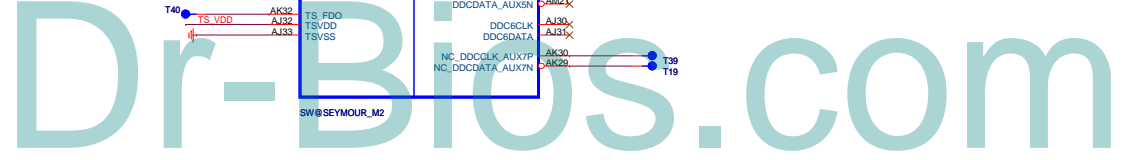
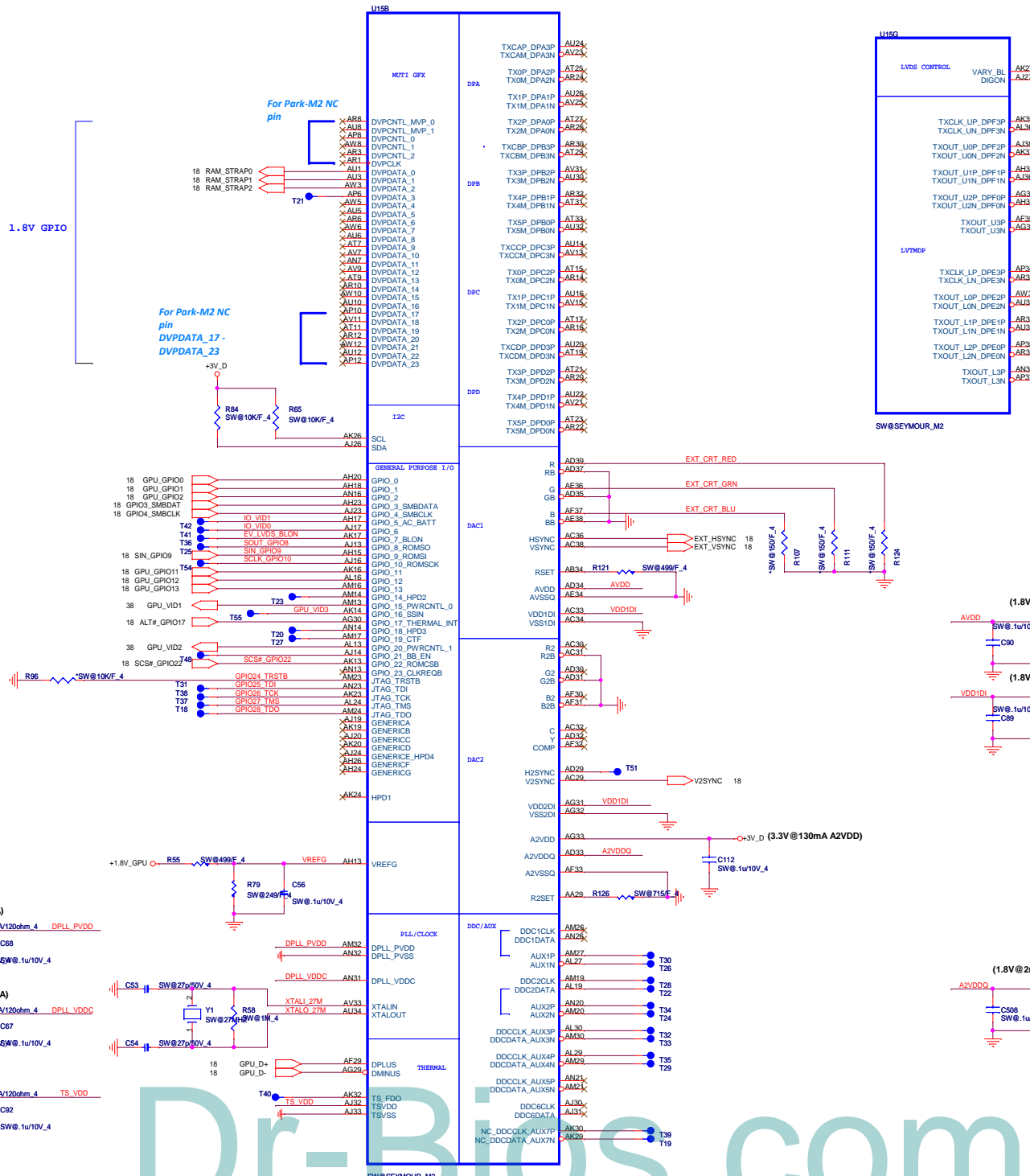
Size	Document Number	Rev
	<b>SeymourPCIE 1/6</b>	1A
Date:	Monday, November 01, 2010	Sheet 13 of 41

### GPU Power-on sequence

- 1 => +3V\_D
- 2 => +VGPU\_CORE
- 3 => +1V
- 4 => +1.5V\_GPU
- 5 => +1.8V\_GPU
- 6 => dGPU\_PWROK

1.8V GPIO

3.3V GPIO

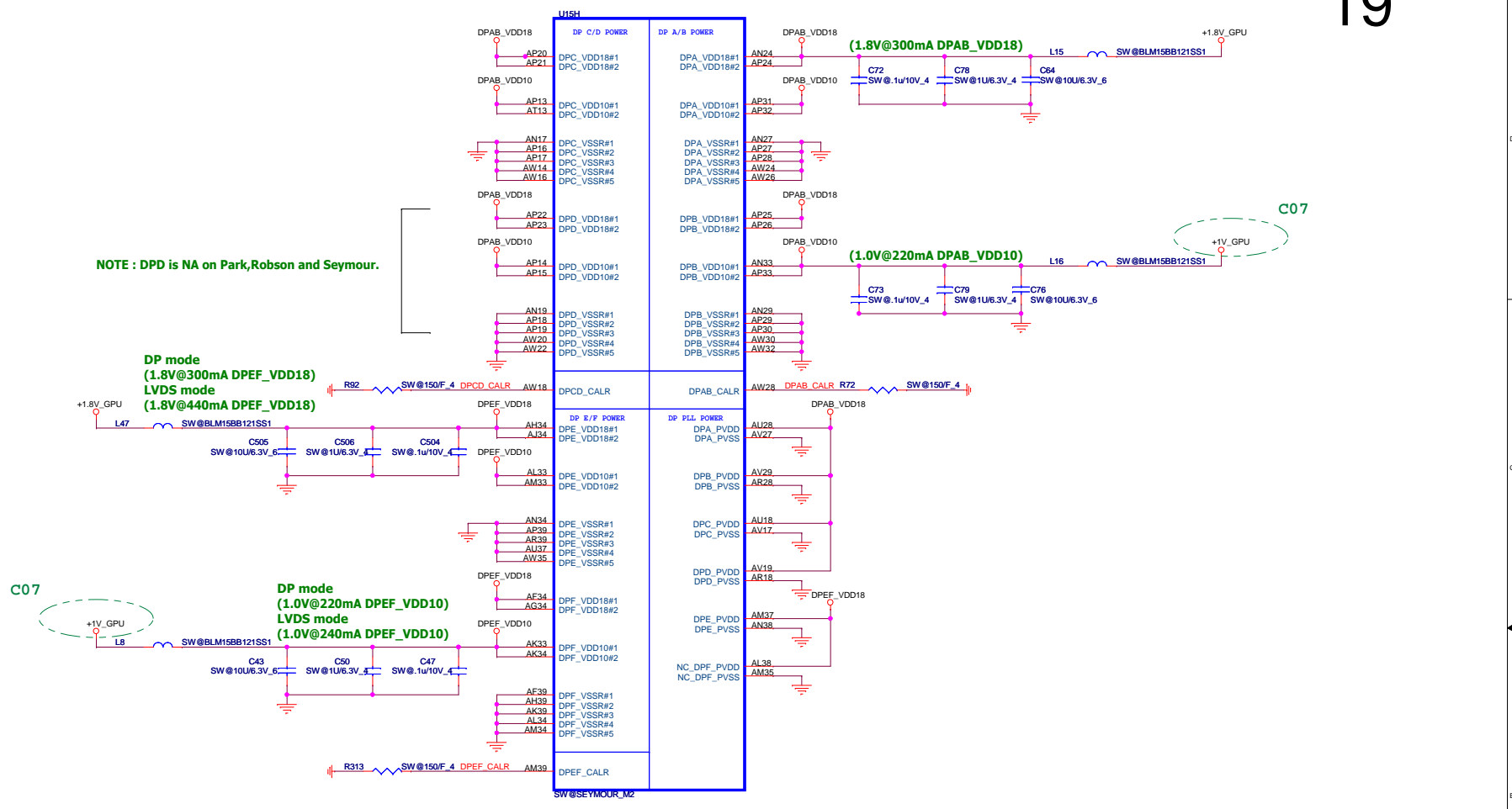






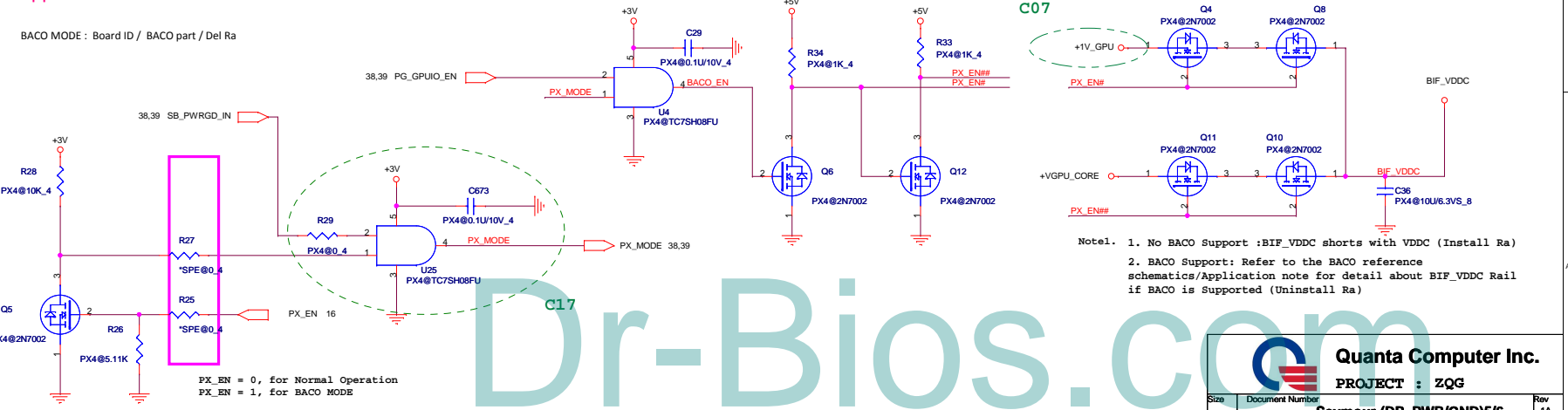


NOTE : DPD is NA on Park,Robson and Seymour.



Support BACO Mode

BACO MODE : Board ID / BACO part / Del Ra



- Notel.
1. No BACO Support :BIF\_VDDC shorts with VDDC (Install Ra)
  2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF\_VDDC Rail if BACO is Supported (Uninstall Ra)

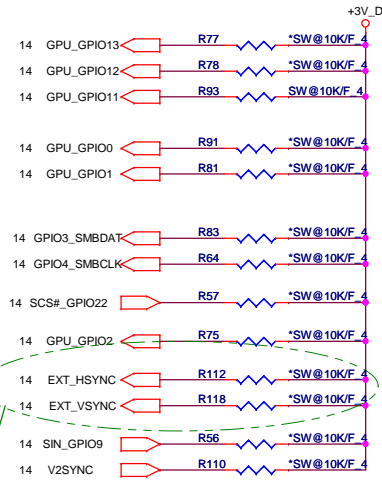
PX\_EN = 0, for Normal Operation  
PX\_EN = 1, for BACO MODE

**Quanta Computer Inc.**  
PROJECT : ZQG  
Seymour (DP\_PWR/GND)5/6

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		1A
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**PIN STRAPS**



C08 : to solve the HDMI issue , remove R112,R118 from BOMs

Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

C02 : to solve the Power DVD issue , setting size to 256MB

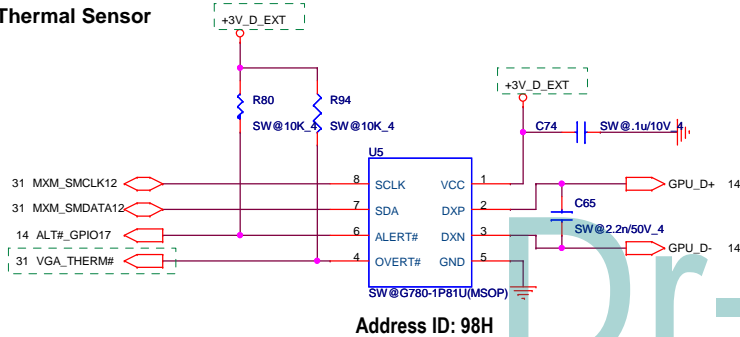
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	00	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

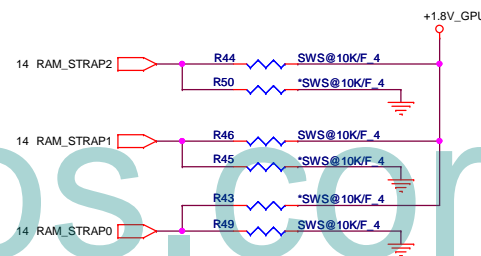
**DDR3 Memory Aperture size**

Vendor	Vendor P/N	STN B/S P/N	Total Memory Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	ZQE/JG
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW05 (64M*16)	1GB ( 900 Mhz)	1	1	0	V
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB ( 800 Mhz)	1	0	0	V
	H5TQ2G63BFR-12C	AKD5MGGT W03 (128M*16)	2GB	1	1	1	V
Samsung	K4W1G1646G-BC11	AKD5EGGT503 (64M*16)	1GB	0	1	0	
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB ( 800 Mhz)	0	0	0	V
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1	

**Thermal Sensor**



Address ID: 98H



RAM\_STRAP2 SET DDR3 Vendor  
RAM\_STRAP[1:0] SET SIZE.

**Quanta Computer Inc.**  
PROJECT : ZQG  
Seymour Strip/Thermal 6/6

Size	Document Number	Rev
		1A

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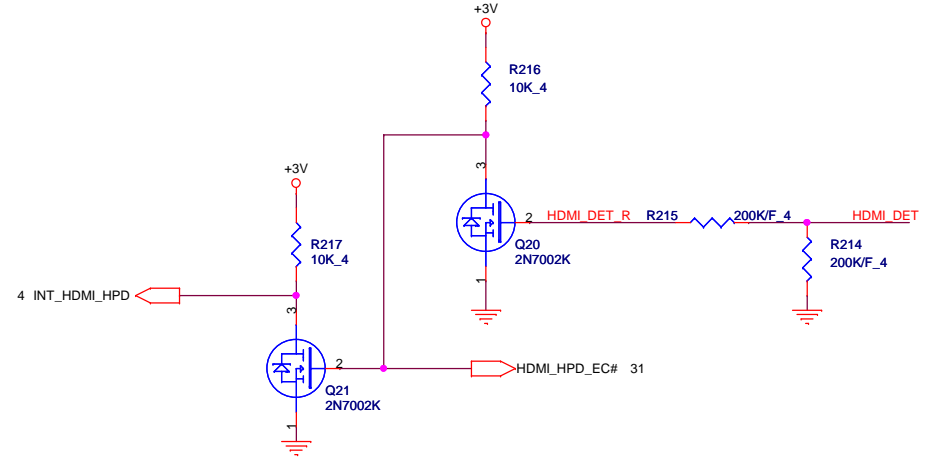


# HDMI SDVO I2C Control



# HDMI HPD SENSE (HDM)

UMA use +3V for the detect pin  
Dis use +3V\_DELAY for the detect pin

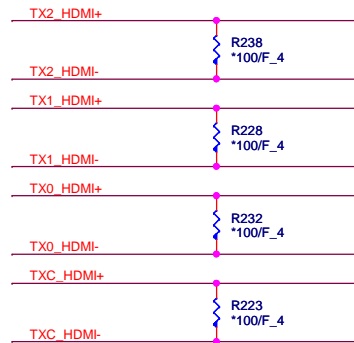
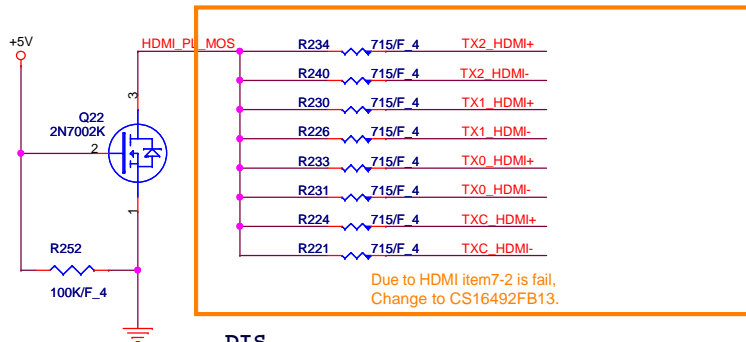


# HDMI (HDM)

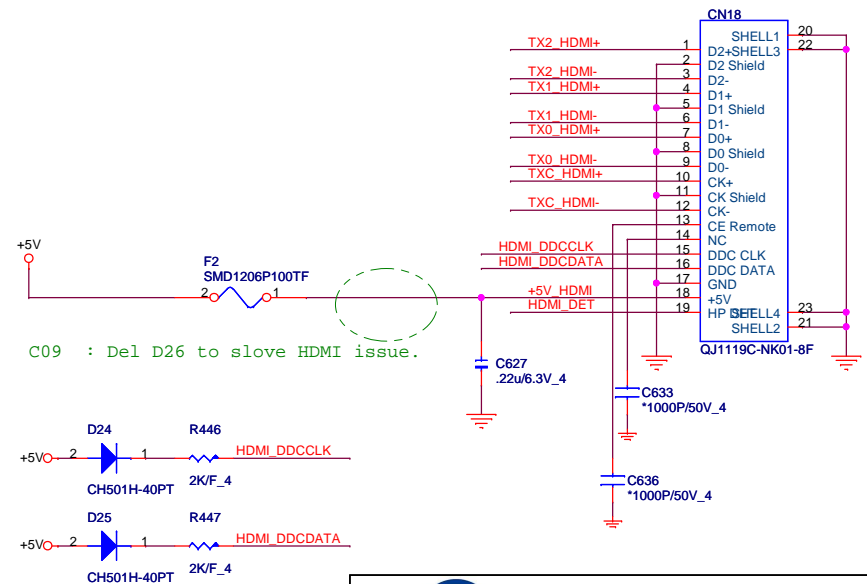
Close to HDMI Connector

EMI reserve for HDMI(EMC)

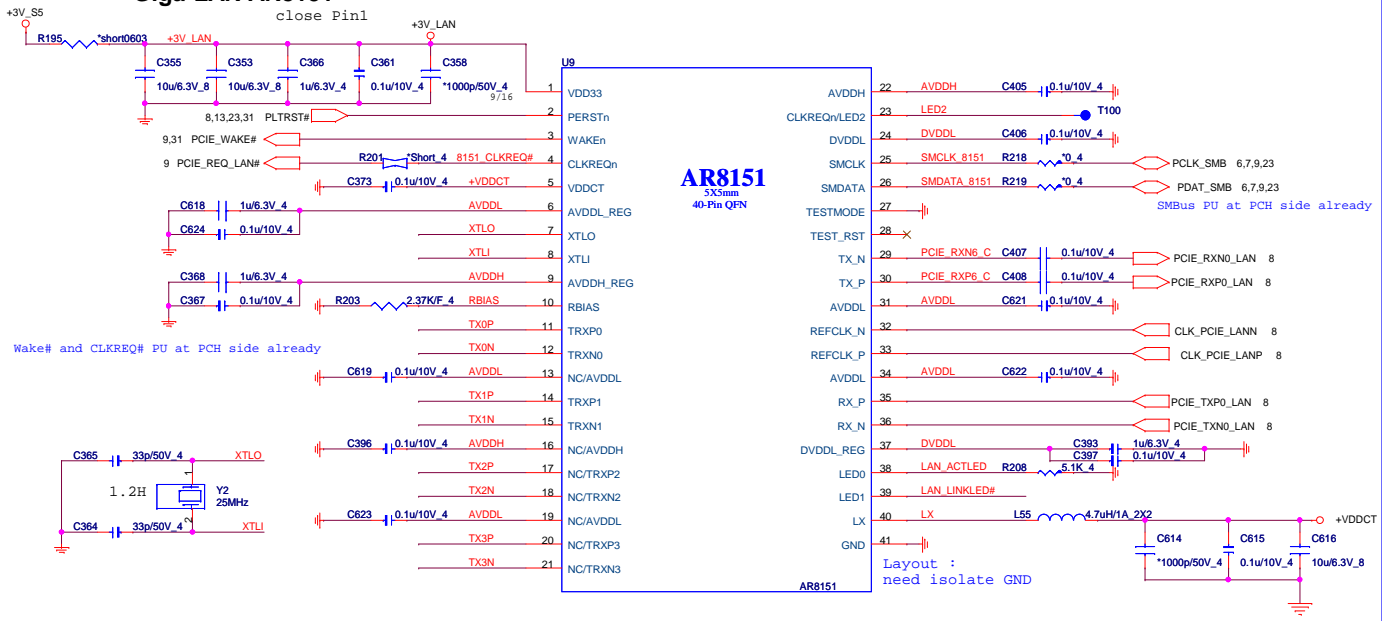
Close connector



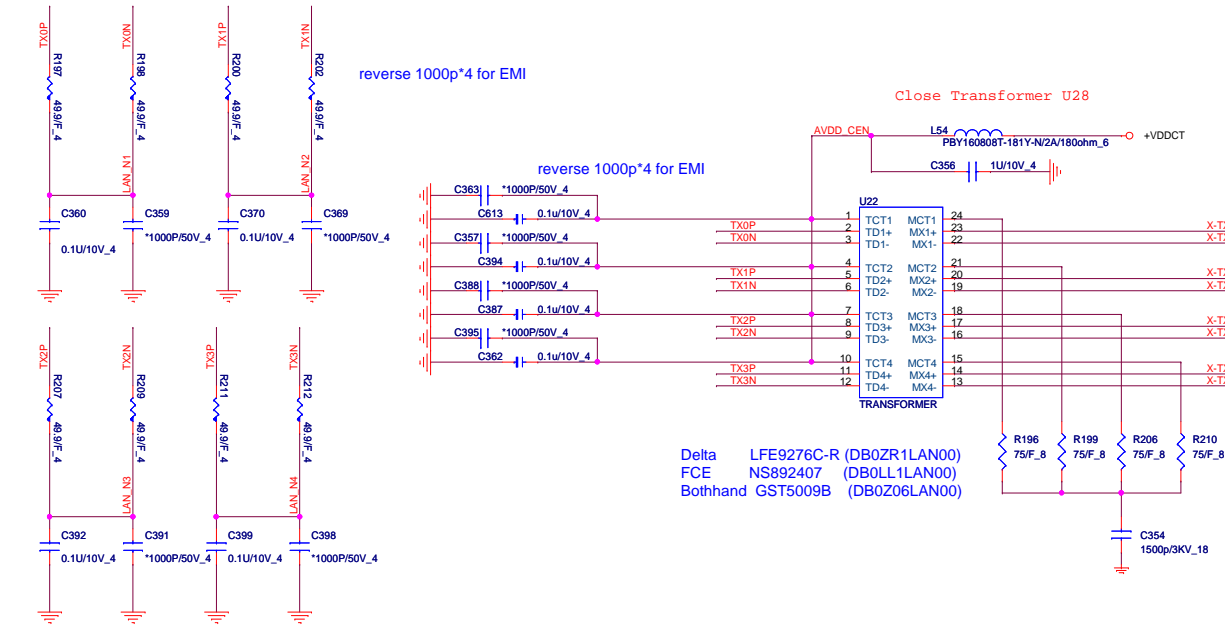
# HDMI PORT (HDM)



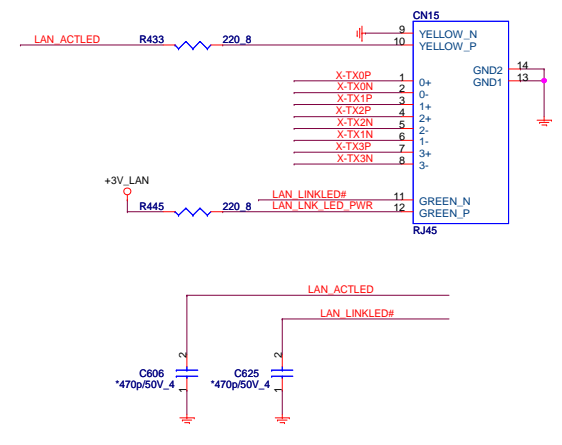
# Giga-LAN AR8151



# TRANSFORMER(LAN)



# RJ45(LAN)

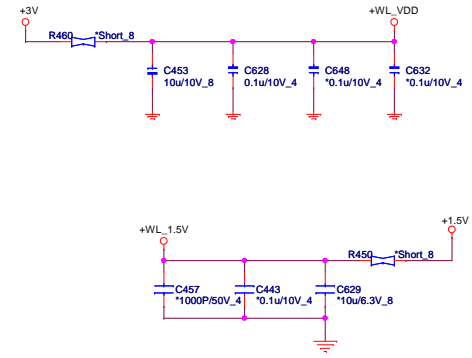
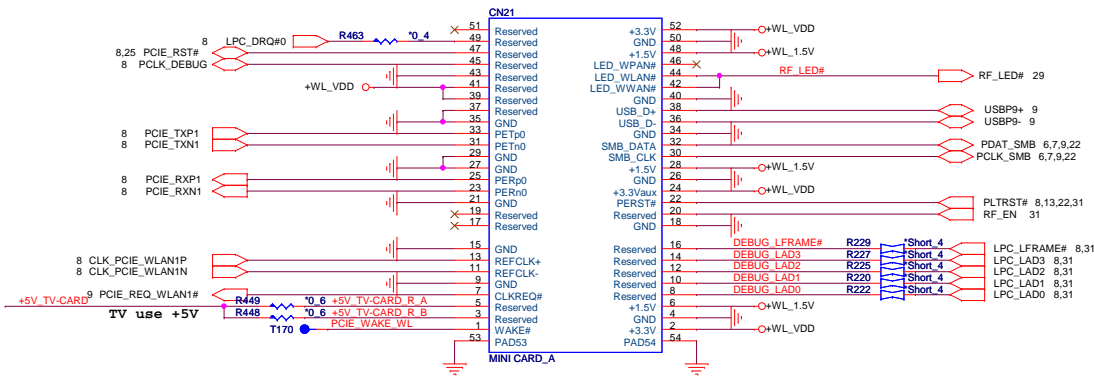


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### MINI-CARD WLAN(MPC)

+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

Check LED signal. (active high or low)

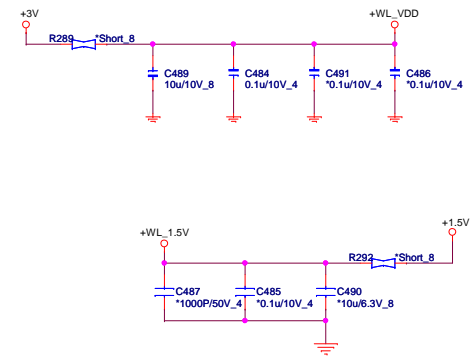
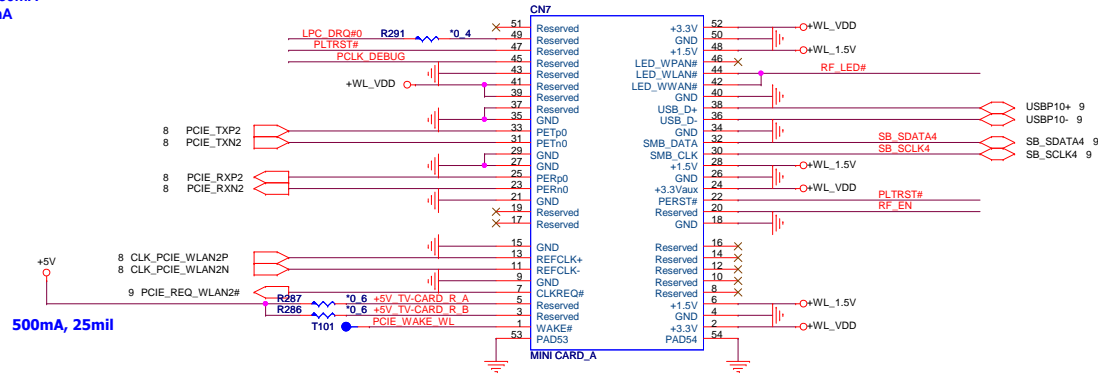


Debug

### MINI-CARD WLAN(MPC)

+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

Check LED signal. (active high or low)

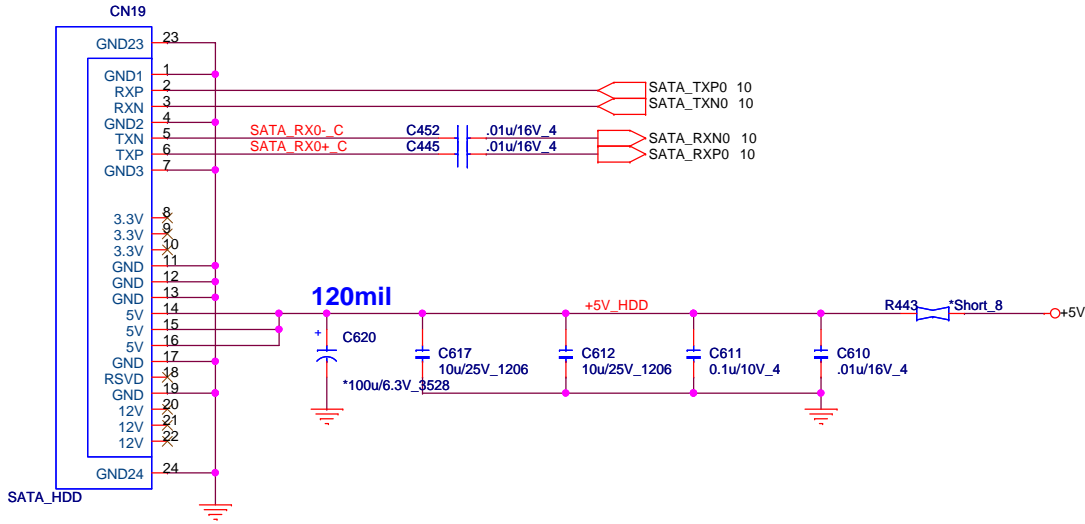


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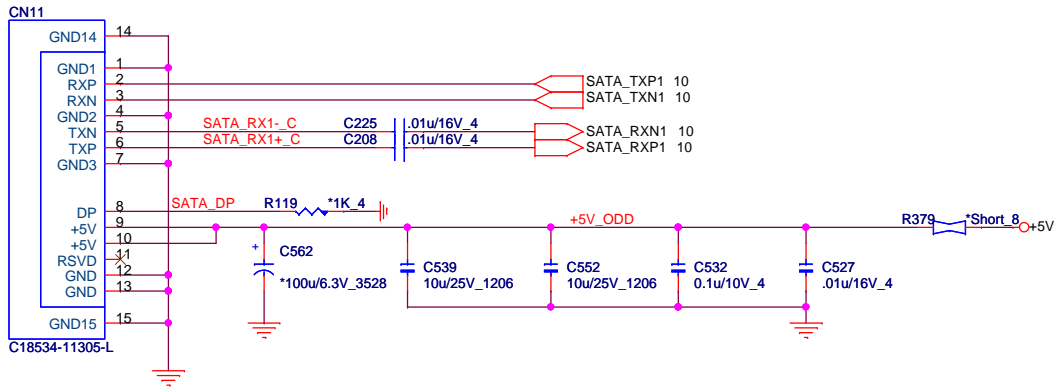
**Quanta Computer Inc.**  
PROJECT : ZQG

Size	Document Number	Rev
	<b>MINI PCI-E card</b>	1A
Date: Monday, November 01, 2010	Sheet 23 of 41	

### SATA HDD



### SATA ODD



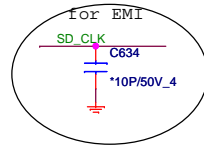
		<b>Quanta Computer Inc.</b>	
		PROJECT : ZQG	
Size	Document Number	SATA-HDD/ODD/HOLE	
Date:	Monday, November 01, 2010	Sheet	24 of 41
			Rev 1A



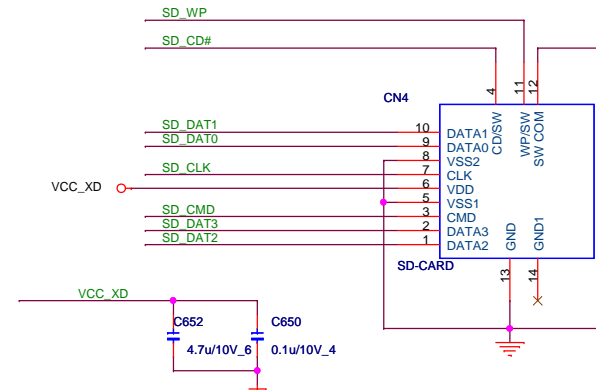
# CARD READER Controller

# 2 IN 1 CARD READER (MMC)

30

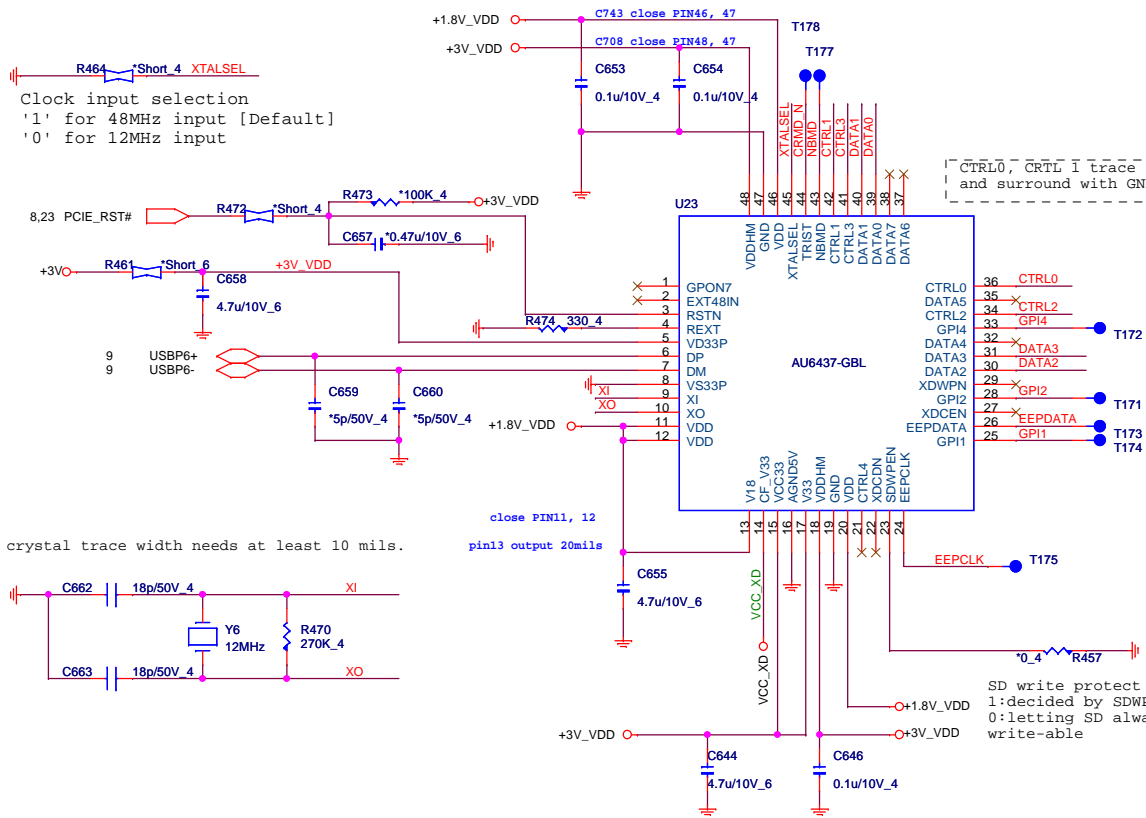


Main	DFHS11FR011
Second	DFHS11FR033

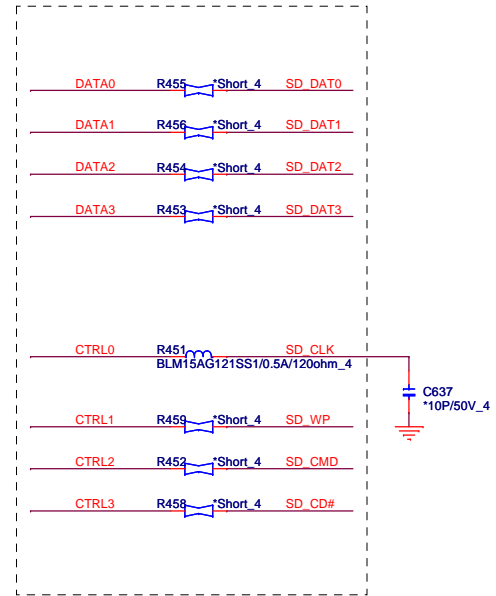


Close to CNxx pin 14 & pin23  
4.7u CAP close to pin23

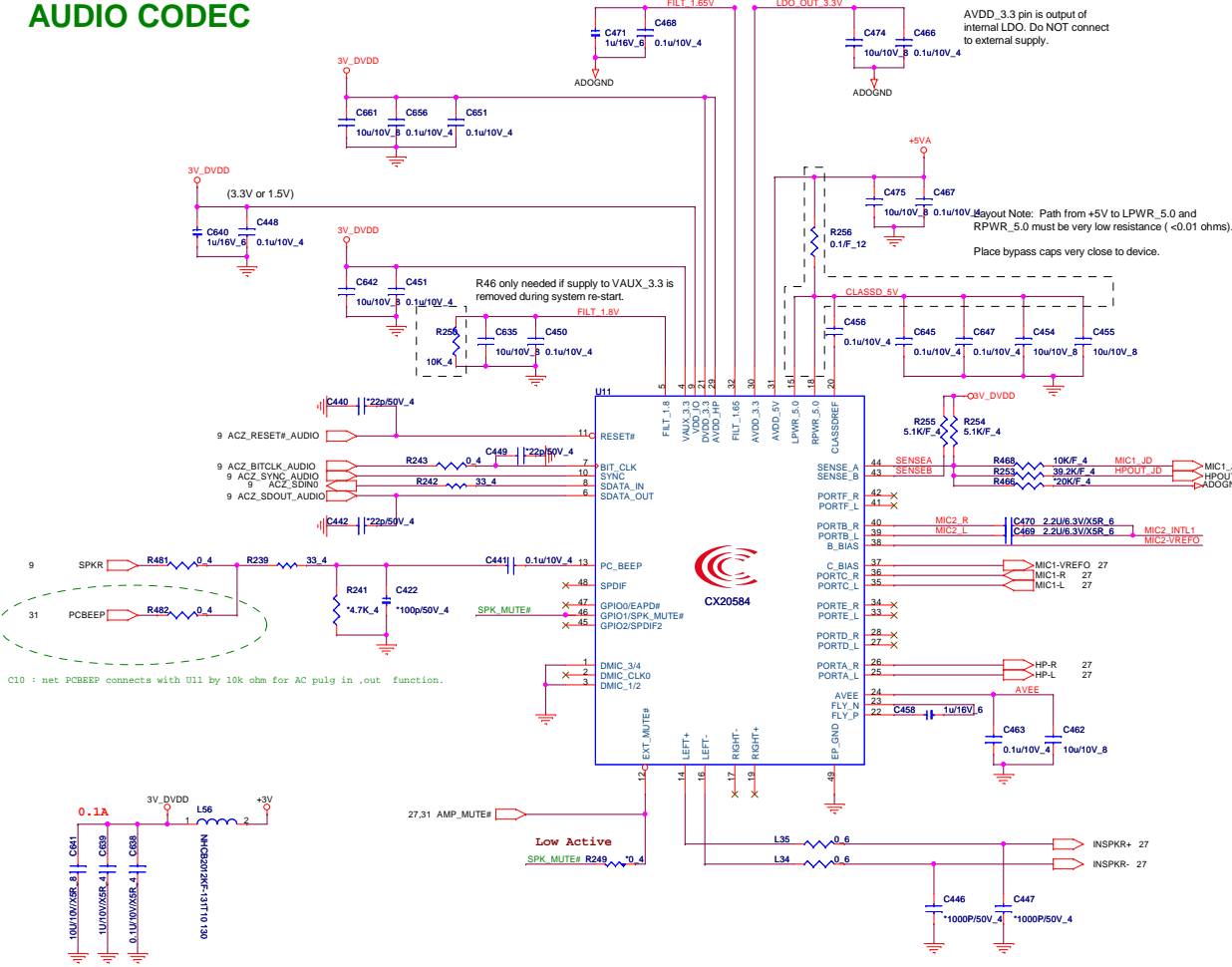
5/10 change Card Redaer conn  
footpirtnt sdcard-sdsn09-08-xa-11p-smt



CTRL0, CTRL1 trace length shorter,  
and surround with GND.



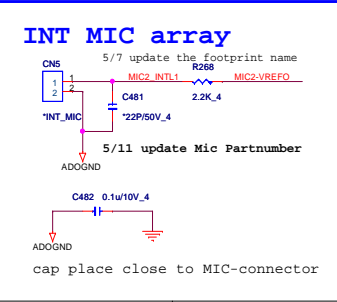
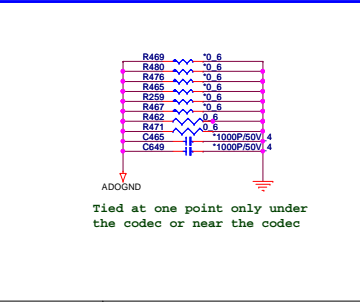
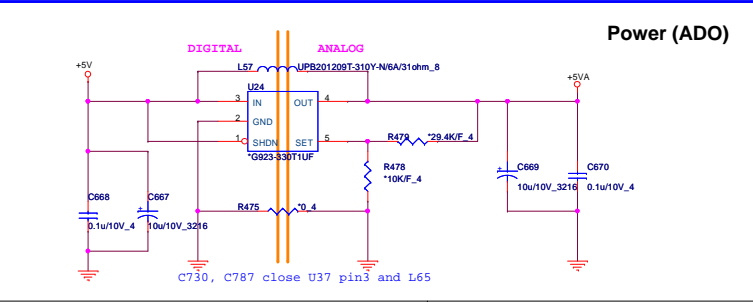
Dr-Bios.com



## Port Configuration

- Notes:
- Port A: Headphone jack (jack shared with S/PDIF)
  - Port B: Internal MIC (mono or stereo)
  - Port C: Microphone/LI/LO jack
  - Port D: Line Out Jack (Optional)
  - Port E: Line In Jack (Optional)
  - Port F: Not used.
  - Port G: Internal stereo speakers
  - Port J: Internal stereo digital mic (Optional)
  - Port H: S/PDIF (jack shared with headphone)

1. The VDD\_IO and VAUX\_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controller.
2. To support Wake-on-Jack, the codec VAUX\_3.3 pin must be powered from a Standby supply.
3. C309, C310, C311 are optional. Do not install unless needed for EM/SL.

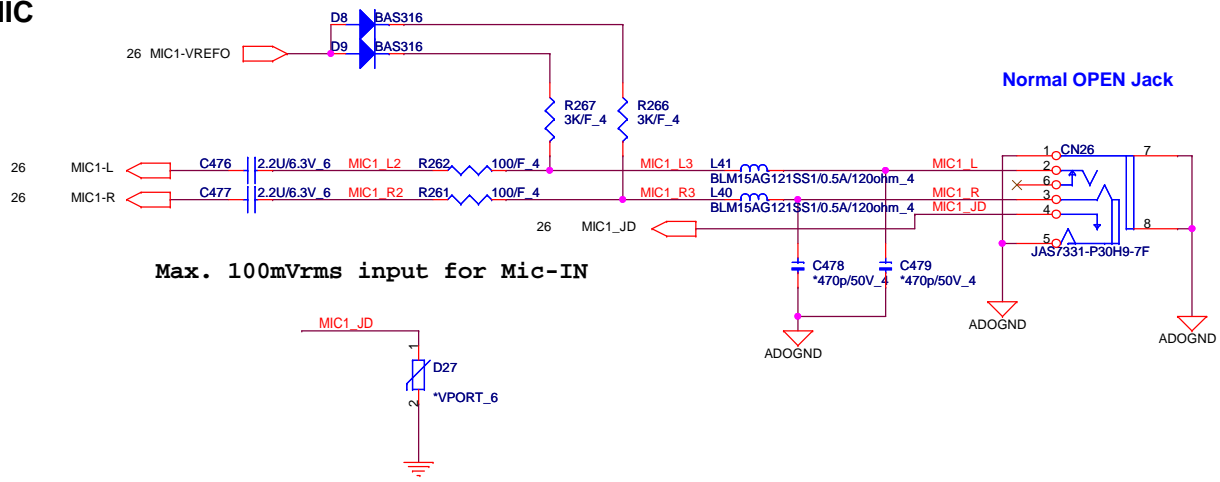


**Quanta Computer Inc.**

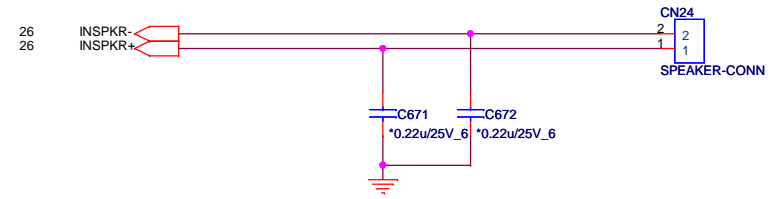
PROJECT : ZQG

Size	Document Number	Rev
Date	CONEXANT 20584	1A
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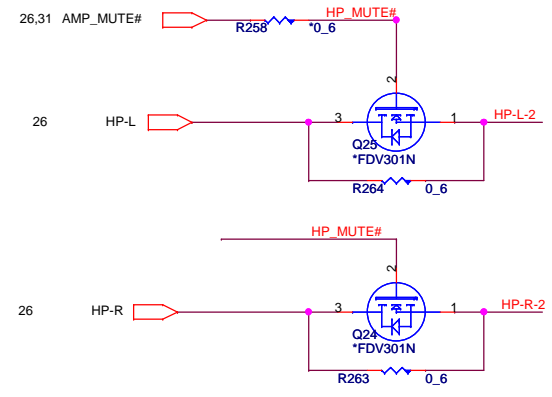
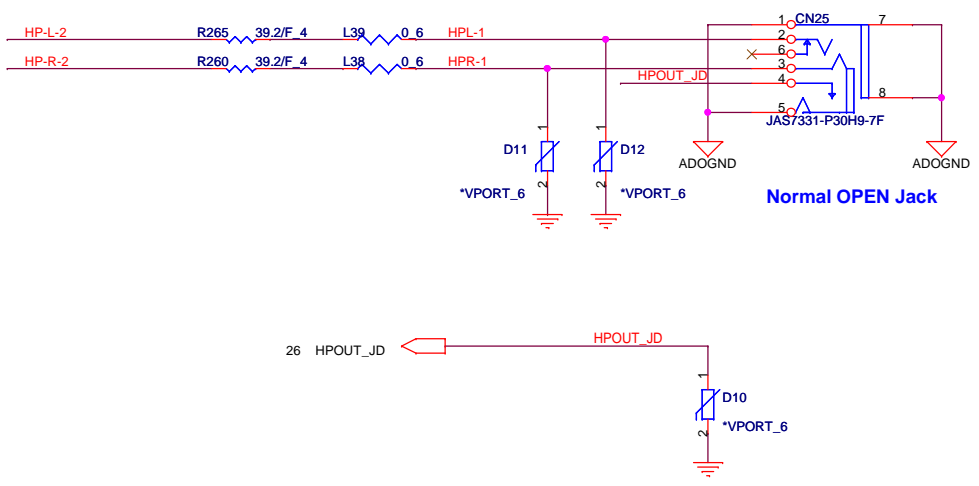
**MIC**



**Internal Speaker**



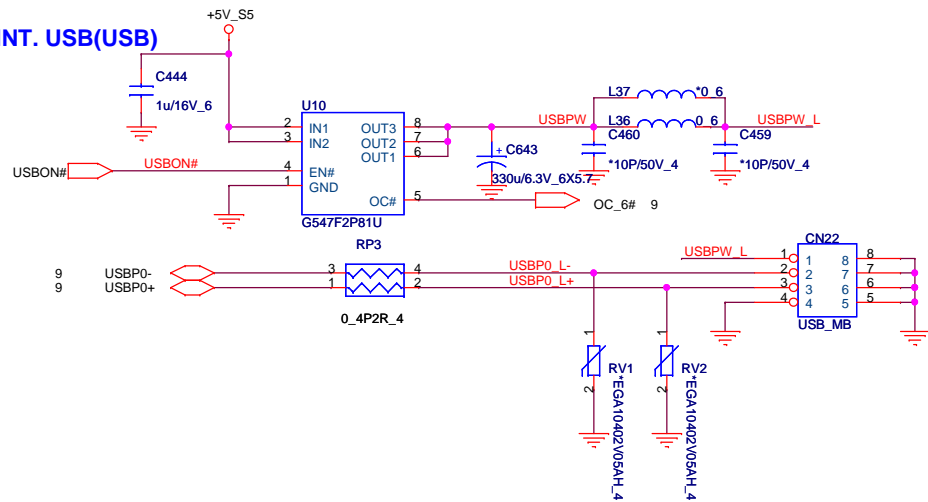
**HP**



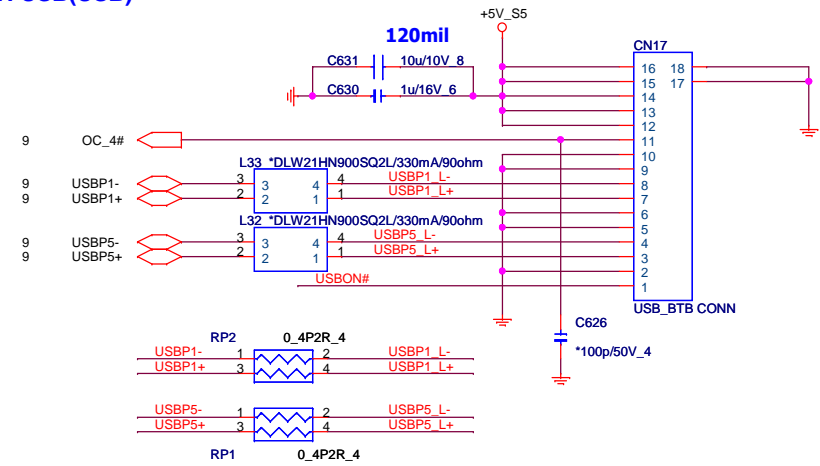
**Quanta Computer Inc.**  
**PROJECT : ZQG**

Size	Document Number	Rev
	<b>AUDIO JACK CONN</b>	1A
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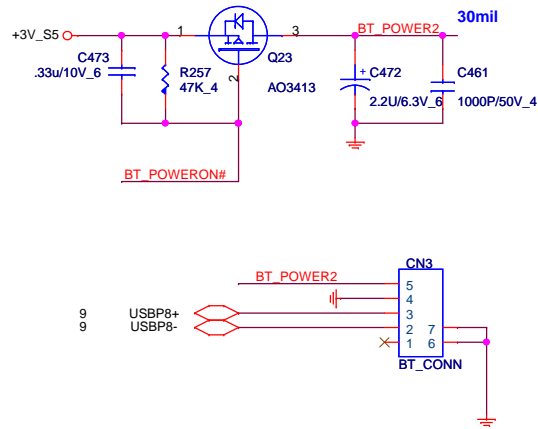
### INT. USB(USB)



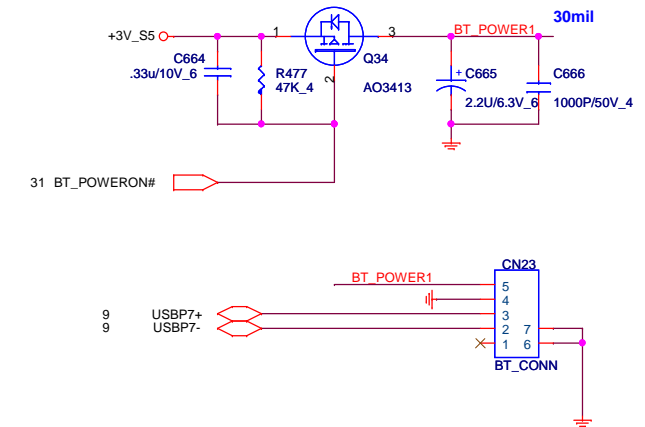
### EXT. USB(USB)




### BLUETOOTH V2.1 CONN(BTM)



### BLUETOOTH V3.0 CONN(BTM)

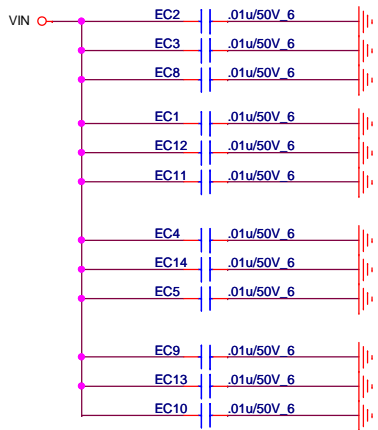




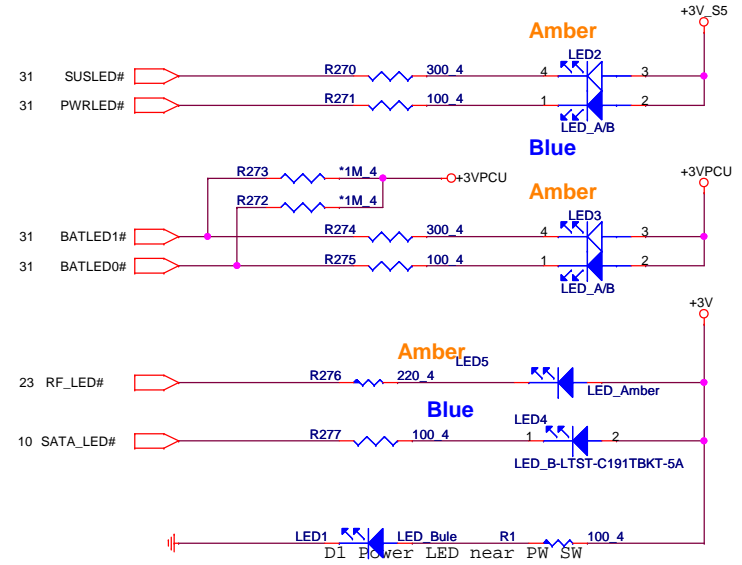
**Quanta Computer Inc.**  
PROJECT : ZQG

Size	Document Number	Rev
	<b>USB/BT</b>	1A
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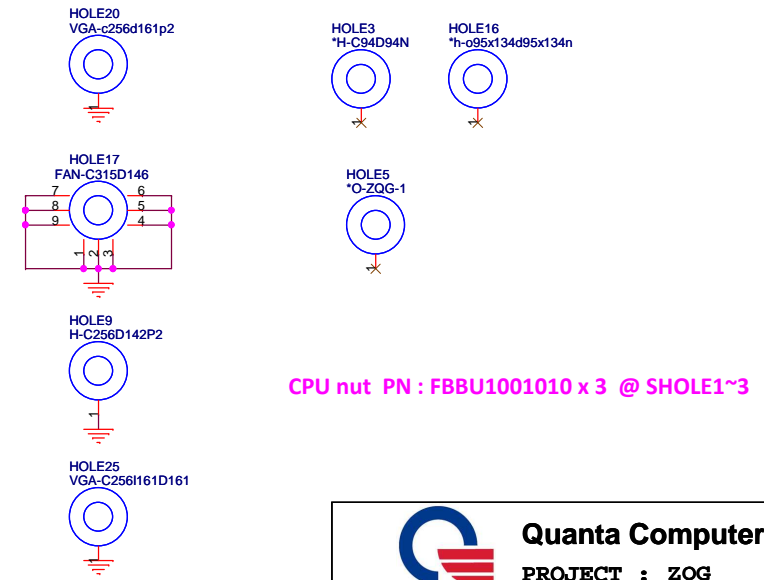
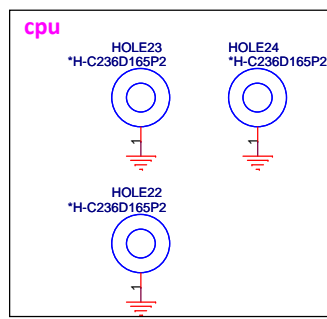
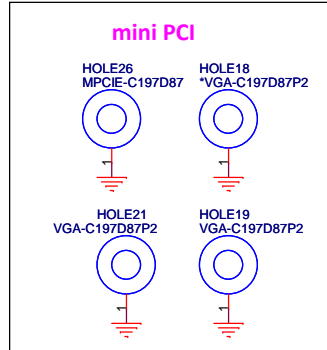
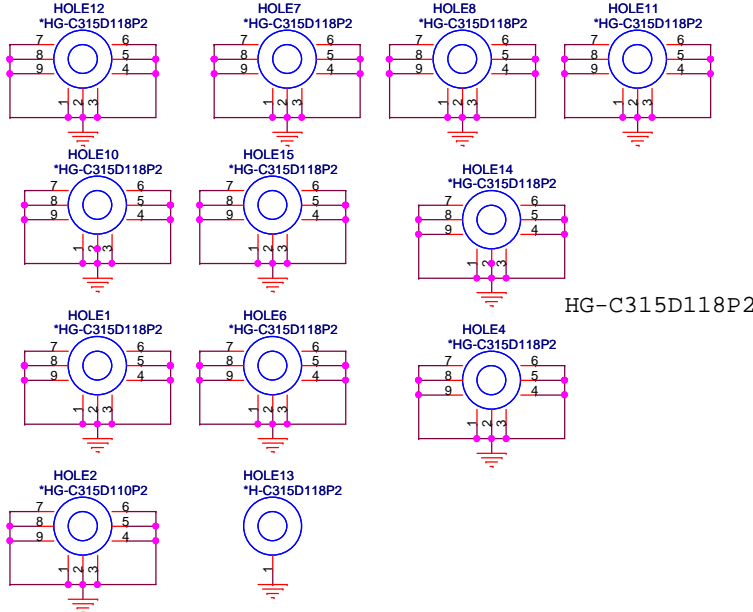
# EE RETURN-PATH CAPACITORS(EMC)



# LED(UIF)



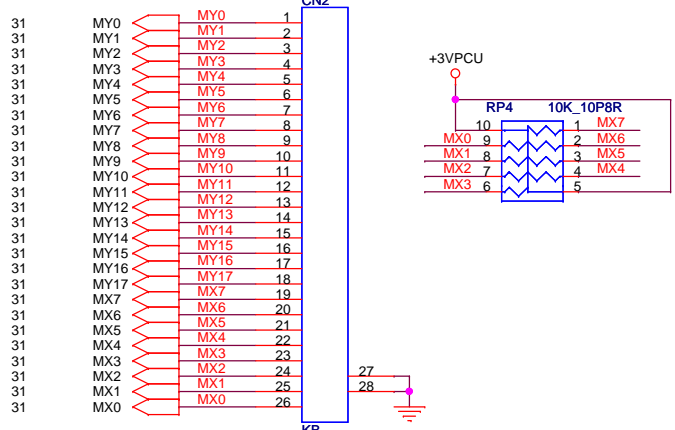
# HOLE(OTH)



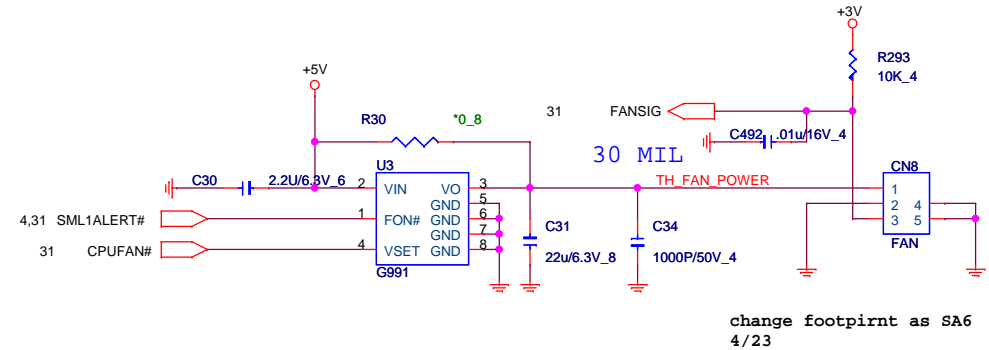
CPU nut PN : FBBU1001010 x 3 @ SHOLE1~3

<b>Quanta Computer Inc.</b> PROJECT : ZQG		Rev
		1A
Size	Document Number	
<b>29 -- LED/ EMI/ Screw Hole&amp; Nut</b>		
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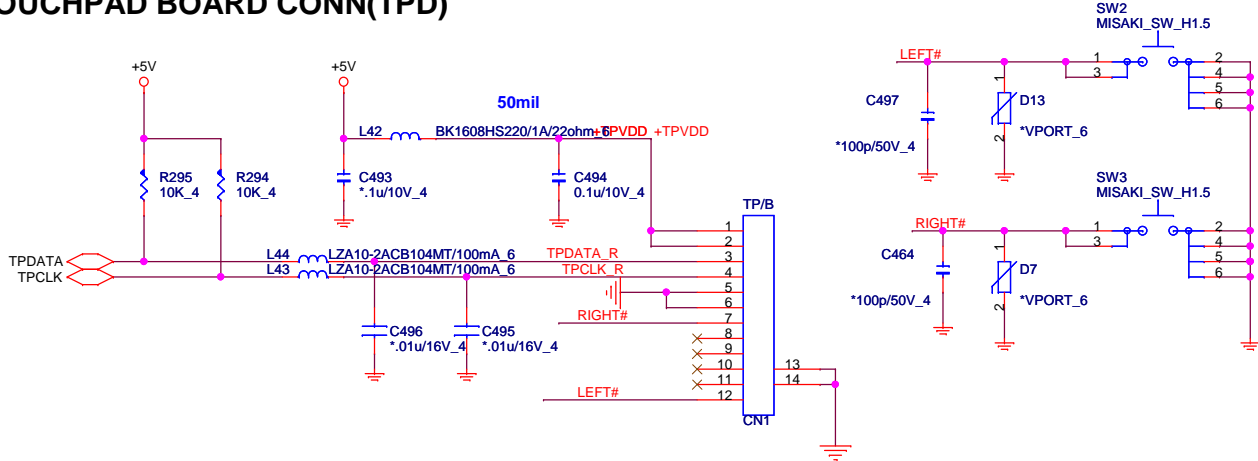
# K/B(KBC)



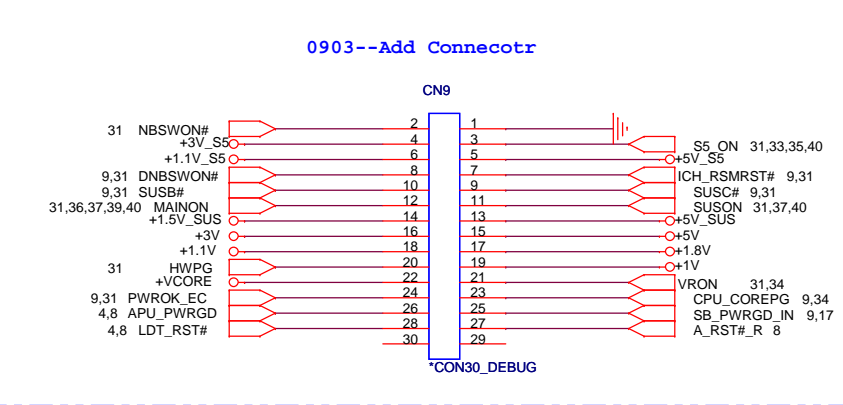
# CPU FAN(THM)



# TOUCHPAD BOARD CONN(TPD)



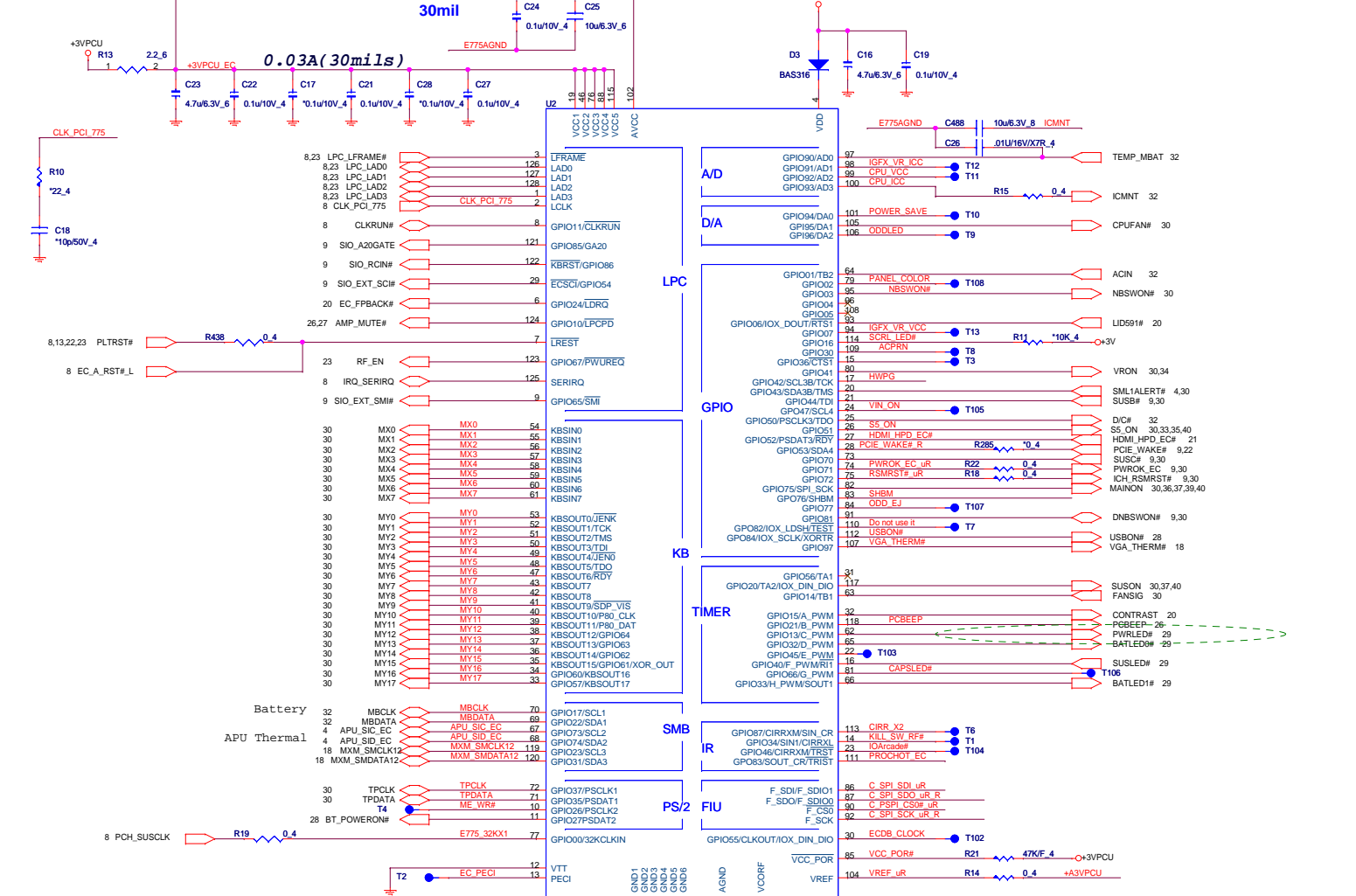
# Power Sequence



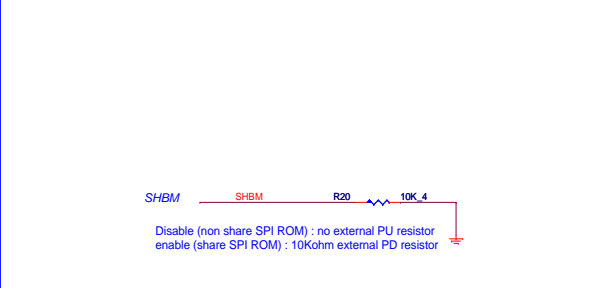
**Quanta Computer Inc.**  
PROJECT : ZQG

Size	Document Number	Rev
	<b>30 -- KB/TP/FAN</b>	1A
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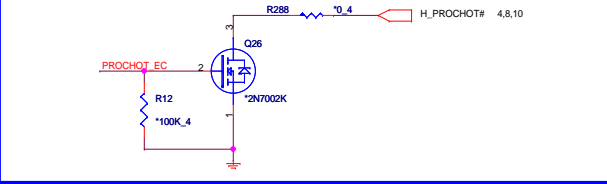
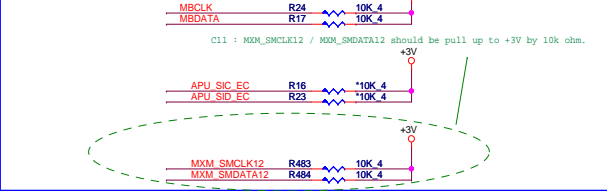
**EC(KBC)**



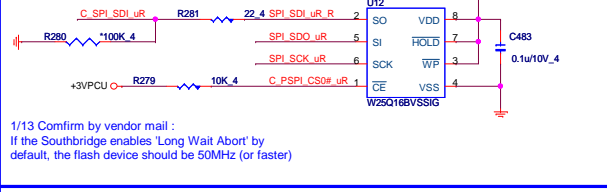
**I/O ADDRESS SETTING(KBC)**



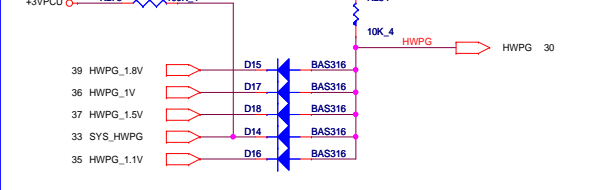
**SM BUS PU(KBC)**



**SPI FLASH(KBC)**



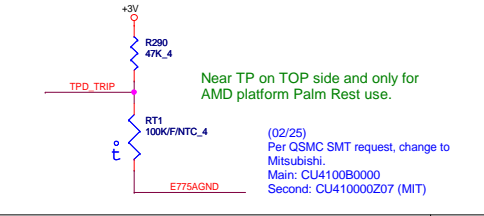
**HWPG(KBC)**



**SM BUS ARRANGEMENT TABLE**

SM Bus 1	Battery
SM Bus 2	APU Thermal
SM Bus 3	VGA

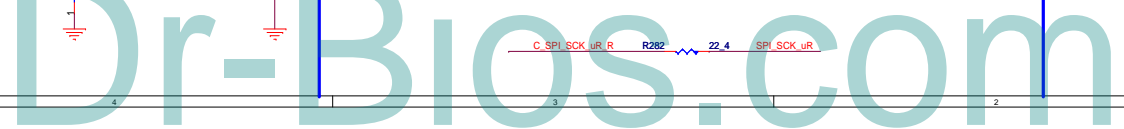
**PALM REST THERMAL SENSOR (THM)**

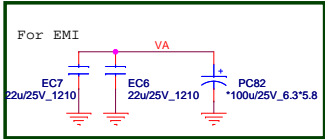
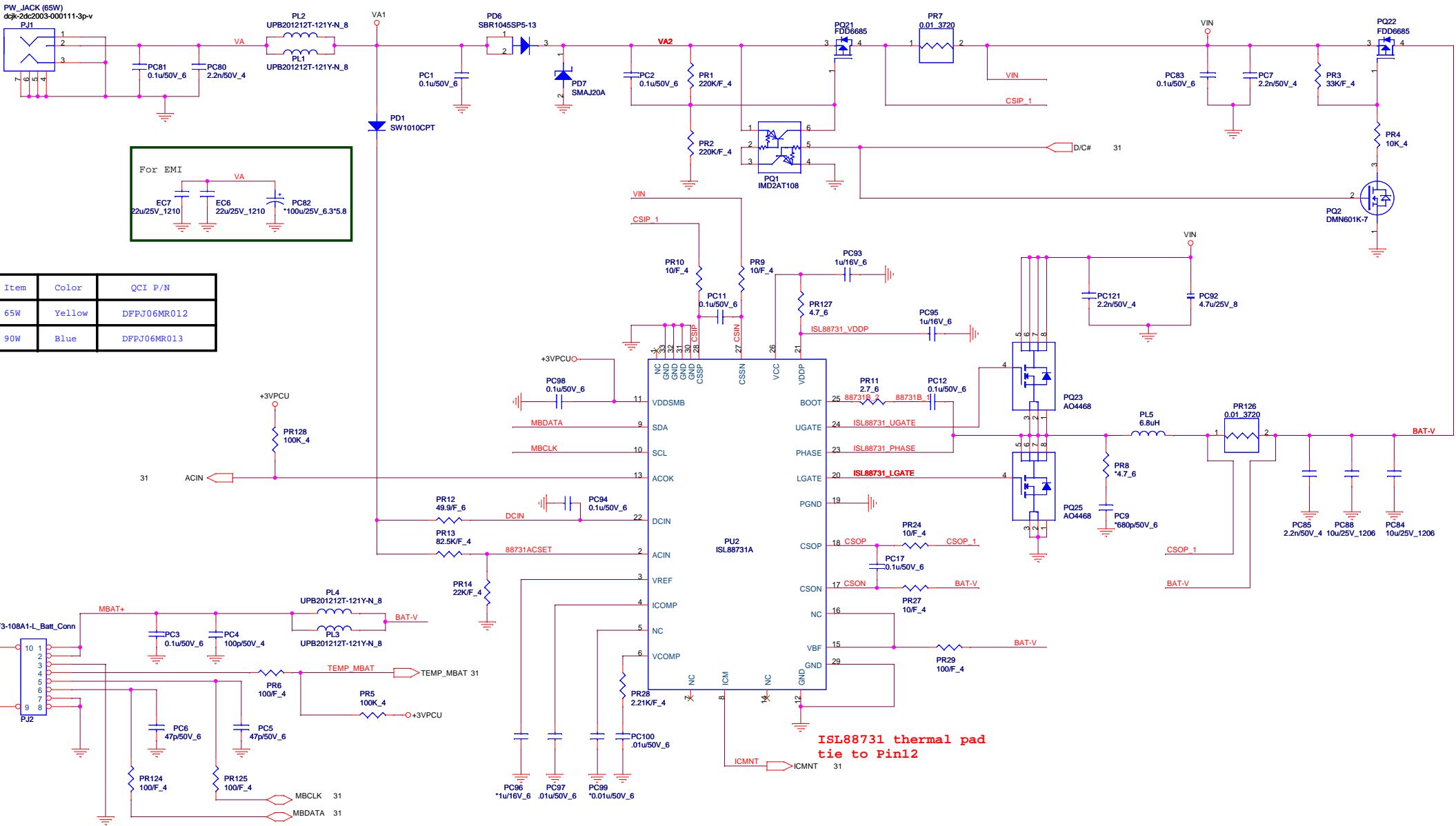


**POWER-ON SWITCH (KBC)**



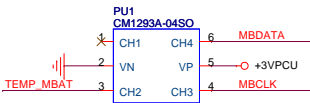
**Quanta Computer Inc.**  
**PROJECT : ZQG**  
 Size Document Number **WPCE791 & FLASH** Rev 1A  
 Date: Monday, November 01, 2010 Sheet 31 of 41





Item	Color	QCI P/N
65W	Yellow	DFPJ06MR012
90W	Blue	DFPJ06MR013

ISL88731 thermal pad tie to Pin12

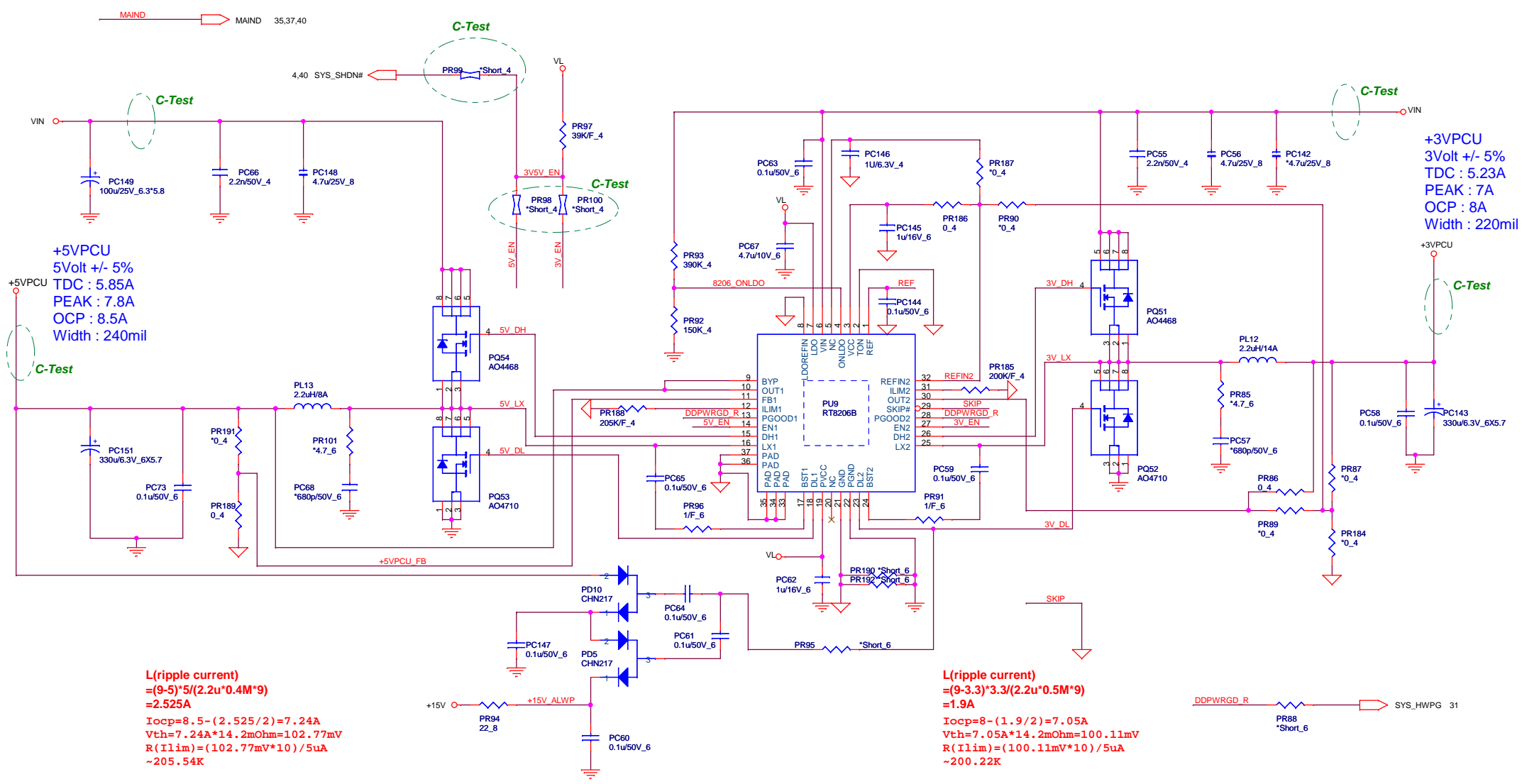


Add ESD diode base on EC FAE suggestion

**Quanta Computer Inc.**  
**PROJECT : ZQG**  
**Charger(ISL88731A)**

Size	Document Number	Rev
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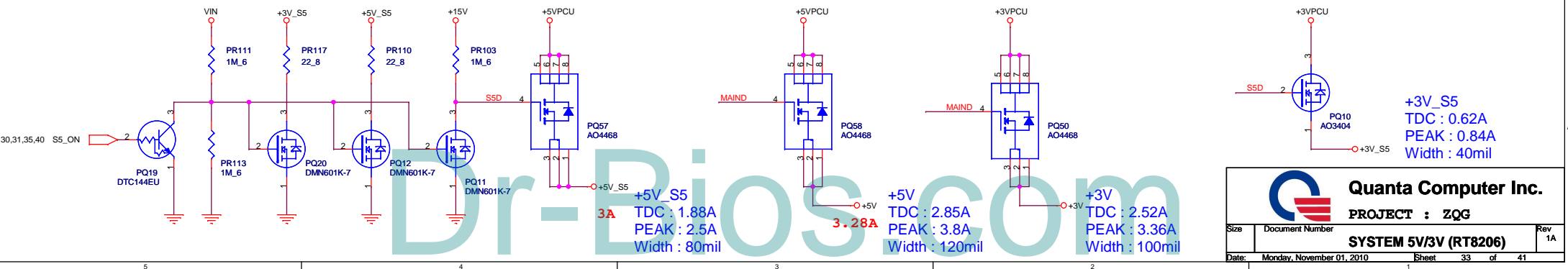


**+5VPCU**  
 5Volt +/- 5%  
 TDC : 5.85A  
 PEAK : 7.8A  
 OCP : 8.5A  
 Width : 240mil

**+3VPCU**  
 3Volt +/- 5%  
 TDC : 5.23A  
 PEAK : 7A  
 OCP : 8A  
 Width : 220mil

**L(ripple current)**  
 $= (9-5) * 5 / (2.2 * 0.4M * 9)$   
 $= 2.525A$   
 $I_{ocp} = 8.5 - (2.525 / 2) = 7.24A$   
 $V_{th} = 7.24A * 14.2m\Omega = 102.77mV$   
 $R(Ilim) = (102.77mV * 10) / 5uA$   
 $\sim 205.54K$

**L(ripple current)**  
 $= (9-3.3) * 3.3 / (2.2 * 0.5M * 9)$   
 $= 1.9A$   
 $I_{ocp} = 8 - (1.9 / 2) = 7.05A$   
 $V_{th} = 7.05A * 14.2m\Omega = 100.11mV$   
 $R(Ilim) = (100.11mV * 10) / 5uA$   
 $\sim 200.22K$



**+5V\_S5**  
 3A  
 TDC : 1.88A  
 PEAK : 2.5A  
 Width : 80mil

**+5V**  
 TDC : 2.85A  
 PEAK : 3.8A  
 Width : 120mil

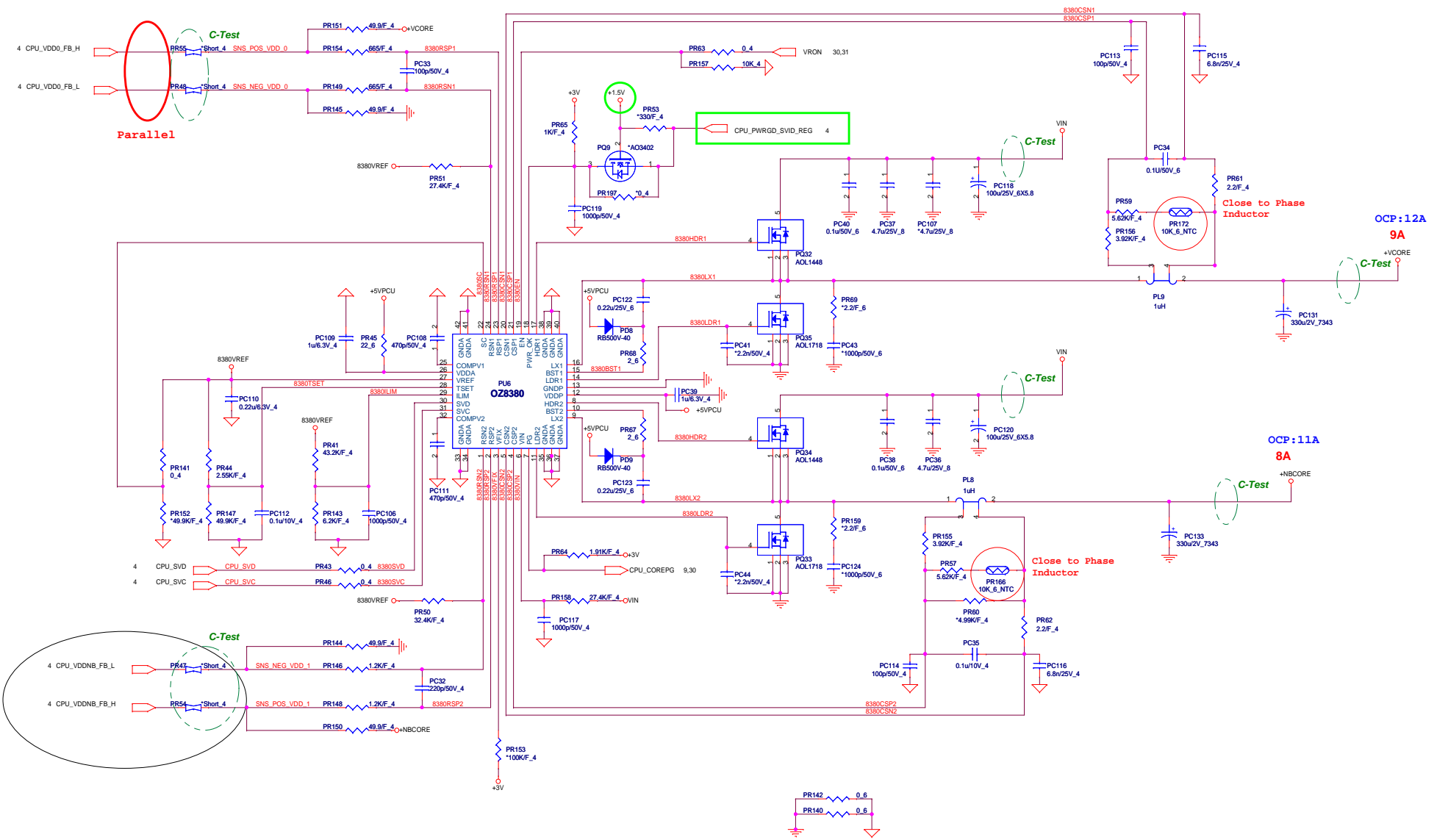
**+3V**  
 TDC : 2.52A  
 PEAK : 3.36A  
 Width : 100mil

**+3V\_S5**  
 TDC : 0.62A  
 PEAK : 0.84A  
 Width : 40mil

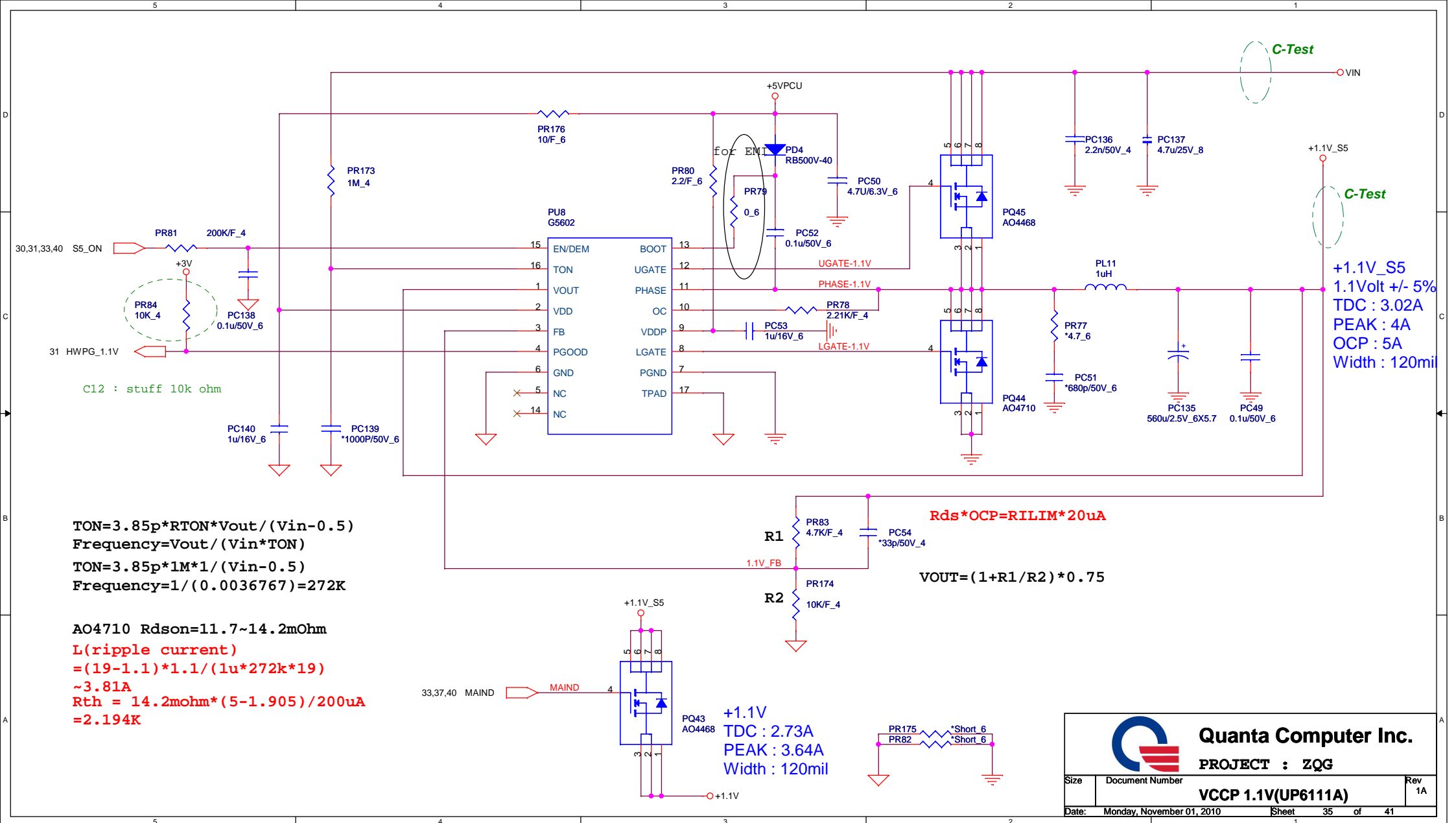
**Quanta Computer Inc.**  
**PROJECT : ZQG**  
**SYSTEM 5V/3V (RT8206)**

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		1A

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C-Test

C-Test

+1.1V\_S5  
 1.1Volt +/- 5%  
 TDC : 3.02A  
 PEAK : 4A  
 OCP : 5A  
 Width : 120mil

$TON = 3.85p * RTON * Vout / (Vin - 0.5)$   
 $Frequency = Vout / (Vin * TON)$   
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$   
 $Frequency = 1 / (0.0036767) = 272K$

AO4710  $R_{dson} = 11.7 \sim 14.2m\Omega$   
**L(ripple current)**  
 $= (19 - 1.1) * 1.1 / (1u * 272k * 19)$   
 $\sim 3.81A$   
 $R_{th} = 14.2m\Omega * (5 - 1.905) / 200uA$   
 $= 2.194K$

$R_{ds} * OCP = R_{ILIM} * 20uA$

$VOUT = (1 + R1/R2) * 0.75$

+1.1V  
 TDC : 2.73A  
 PEAK : 3.64A  
 Width : 120mil

		<b>Quanta Computer Inc.</b> <b>PROJECT : ZQG</b>	
		Size Document Number <b>VCCP 1.1V(UP6111A)</b>	Rev 1A
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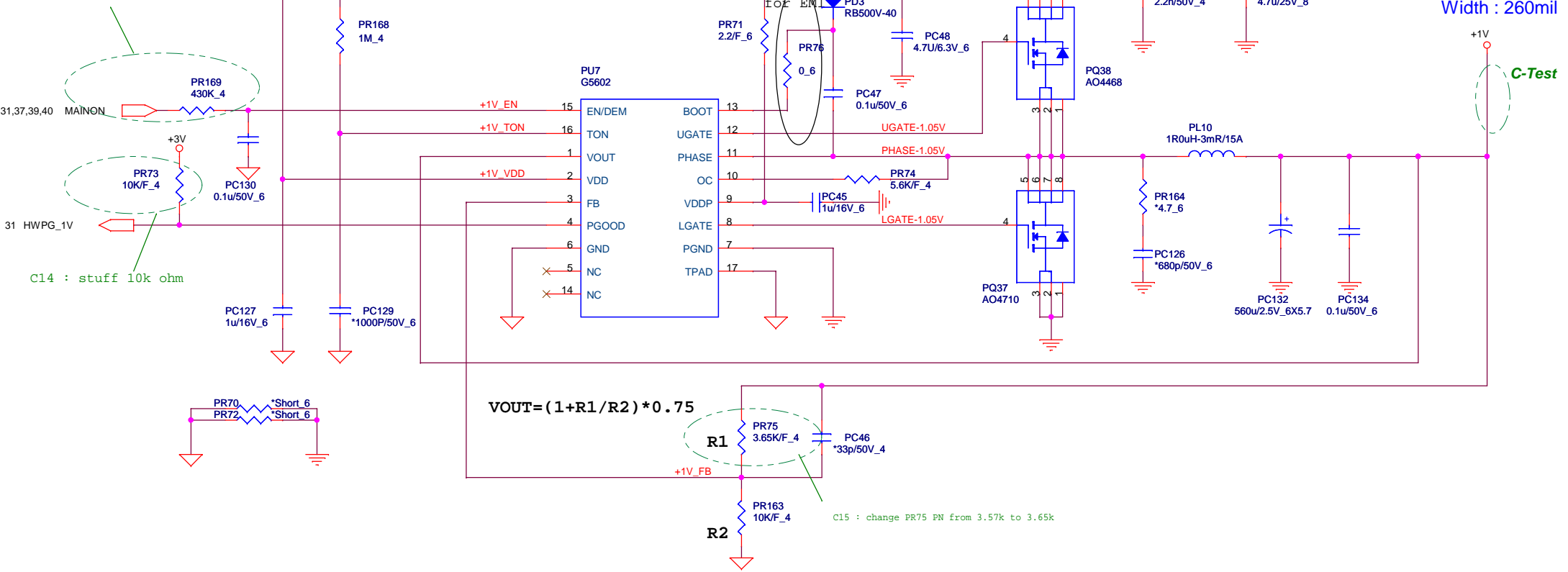
C13

change PR169 PN from 0ohm to 430kohm for timing issue

C14 : stuff 10k ohm

C15 : change PR75 PN from 3.57k to 3.65k

+1V  
 1Volt +/- 5%  
 TDC : 6.5A  
 PEAK : 8.5A  
 OCP : 10A  
 Width : 260mil



$$V_{OUT} = (1 + R1/R2) * 0.75$$

$$TON = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * TON)$$


$$TON = 3.85p * 1M * 1 / (V_{in} - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

AO4710  $R_{dson} = 11.7 \sim 14.2m\Omega$

$L(ripple\ current)$   
 $= (19-1) * 1 / (1u * 272k * 19)$   
 $\sim 3.483A$

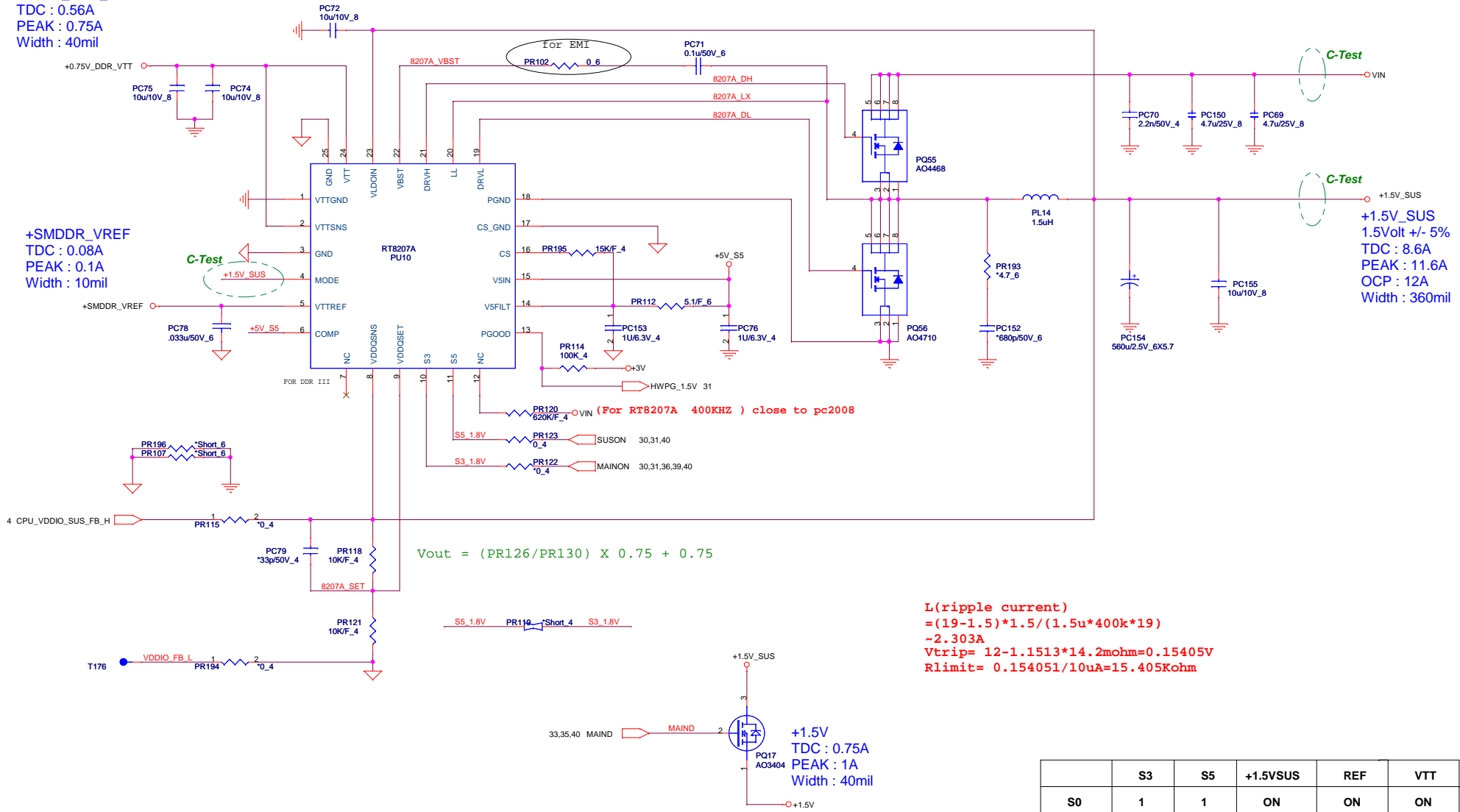
$R_{th} = 14.2m\Omega * (10 - 1.741) / 20uA$   
 $= 5.863K\Omega$

 <b>Quanta Computer Inc.</b> PROJECT : ZQG		Rev 1A
		<b>+1V(G5602)</b>
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+0.75V\_DDR\_VTT  
 TDC : 0.56A  
 PEAK : 0.75A  
 Width : 40mil

+SMDDR\_VREF  
 TDC : 0.08A  
 PEAK : 0.1A  
 Width : 10mil

+1.5V\_SUS  
 1.5Volt +/- 5%  
 TDC : 8.6A  
 PEAK : 11.6A  
 OCP : 12A  
 Width : 360mil

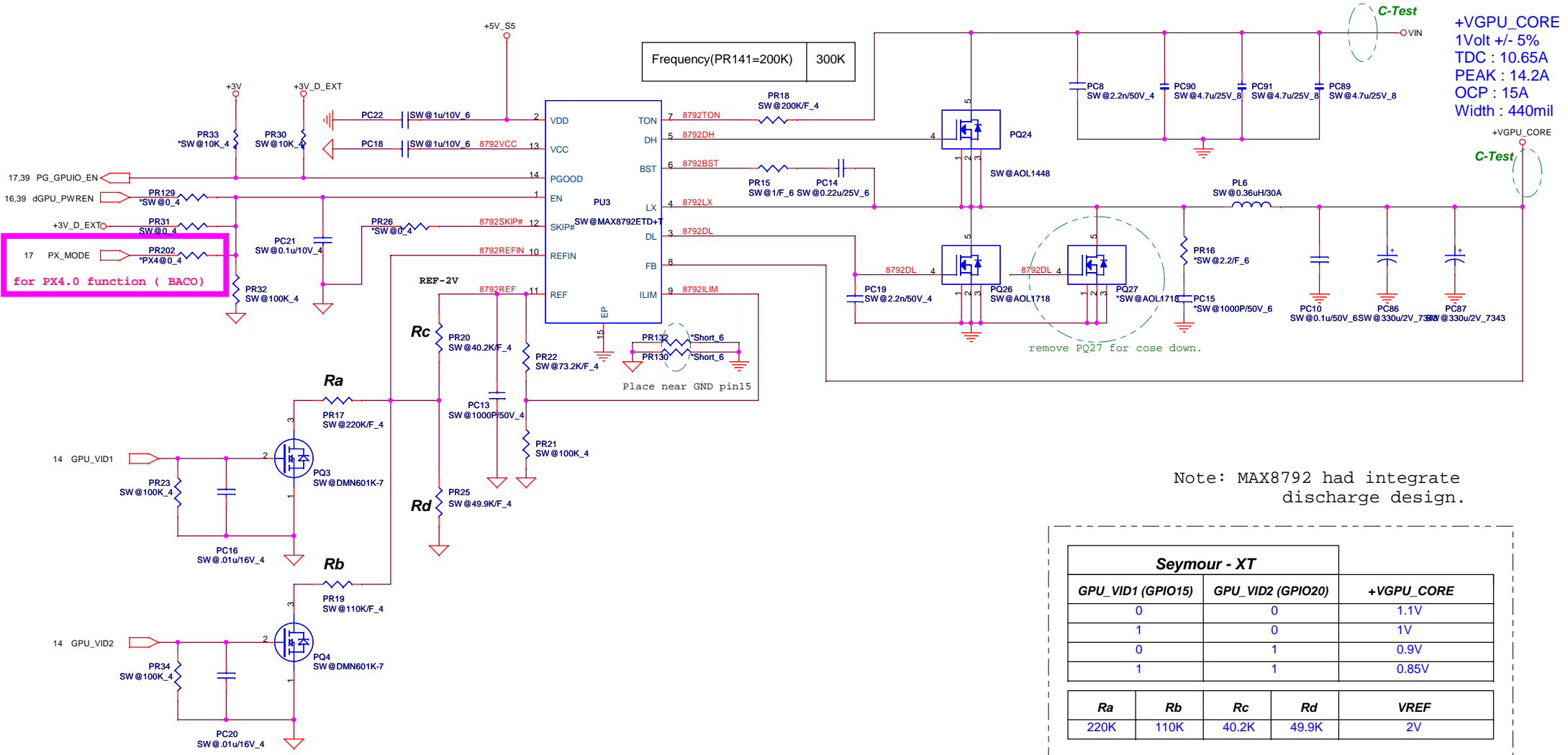


L(ripple current)  
 $= (19-1.5) * 1.5 / (1.5u * 400k * 19)$   
 $\sim 2.303A$   
 $V_{trip} = 12 - 1.1513 * 14.2mohm = 0.15405V$   
 $R_{limit} = 0.154051 / 10uA = 15.405Kohm$

$V_{out} = (PR126/PR130) \times 0.75 + 0.75$

+1.5V  
 TDC : 0.75A  
 PEAK : 1A  
 Width : 40mil

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



+VGPU\_CORE  
 1Volt +/- 5%  
 TDC : 10.65A  
 PEAK : 14.2A  
 OCP : 15A  
 Width : 440mil

17 PX\_MODE  
 for PX4.0 function ( BACO)

Note: MAX8792 had integrate discharge design.

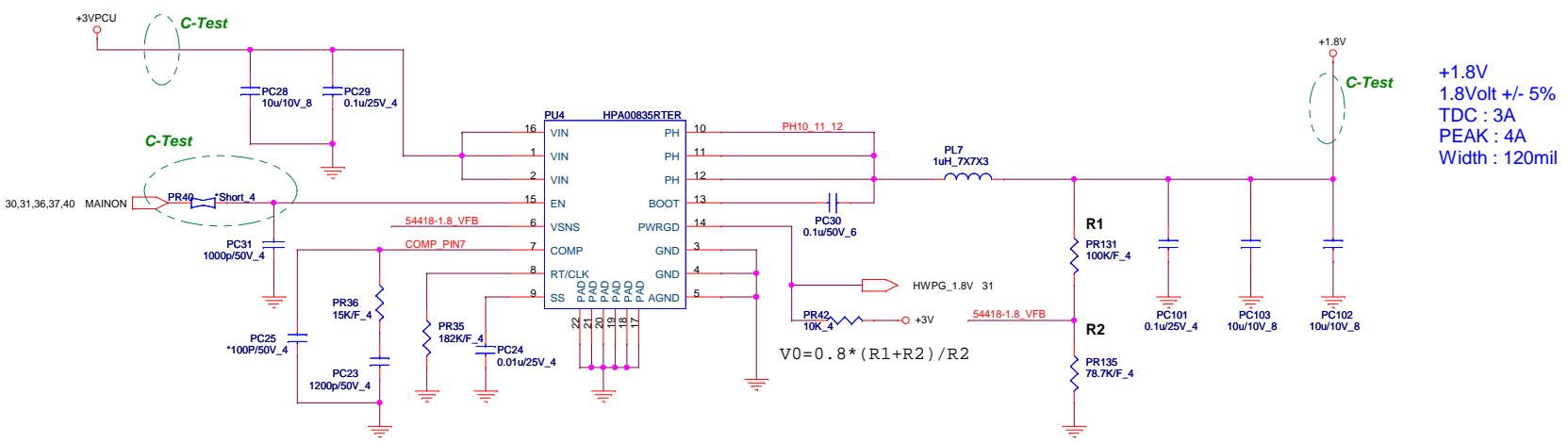
Seymour - XT		
GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.1V
1	0	1V
0	1	0.9V
1	1	0.85V

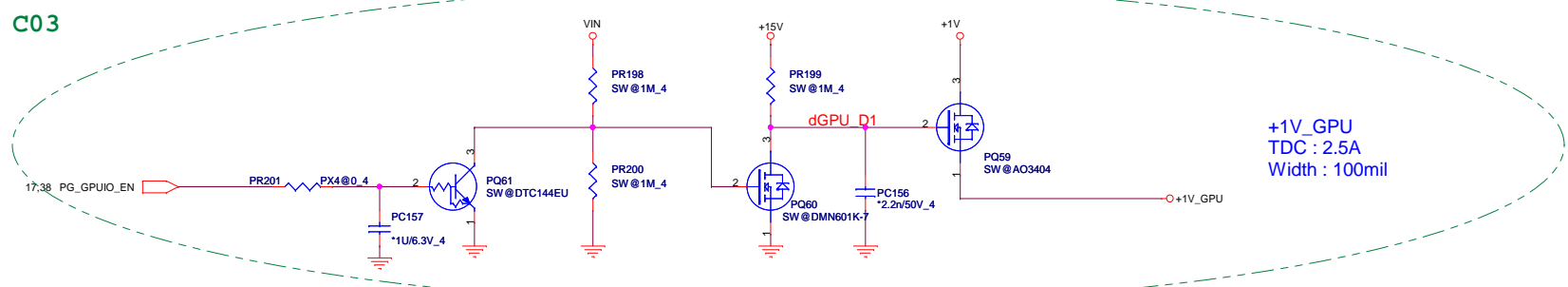
Ra	Rb	Rc	Rd	VREF
220K	110K	40.2K	49.9K	2V

Ra --> 220K/F\_4 (CS42202FB01) Rb --> 110K/F\_4 (CS41102FB13)  
 Rc --> 40.2K/F\_4 (CS34022FB15) Rd --> 49.9K/F\_4 (CS34992FB10)

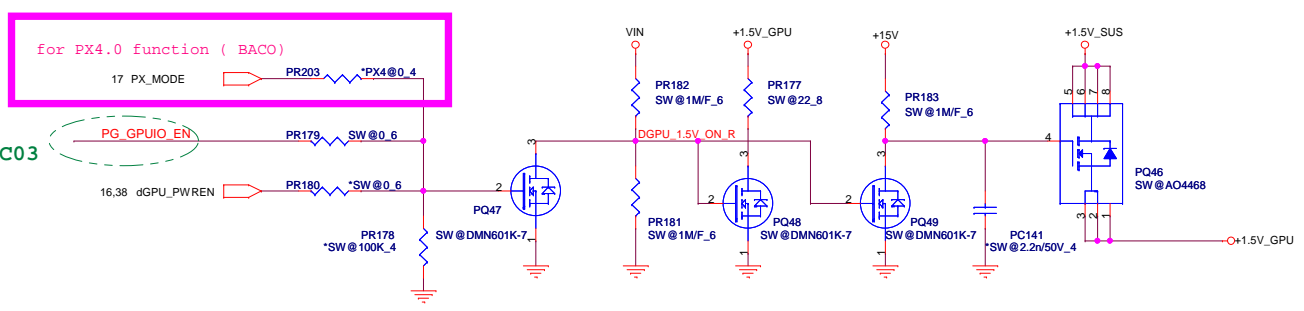
**Quanta Computer Inc.**  
 PROJECT : ZQG  
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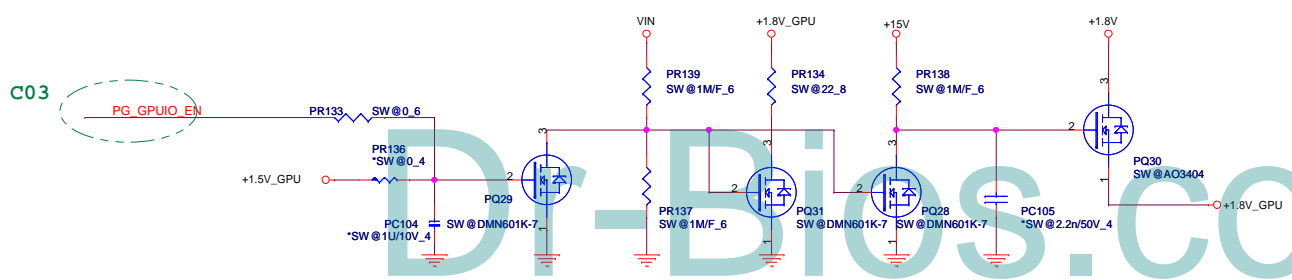
+1.8V  
1.8V +/- 5%  
TDC : 3A  
PEAK : 4A  
Width : 120mil



+1V\_GPU  
TDC : 2.5A  
Width : 100mil



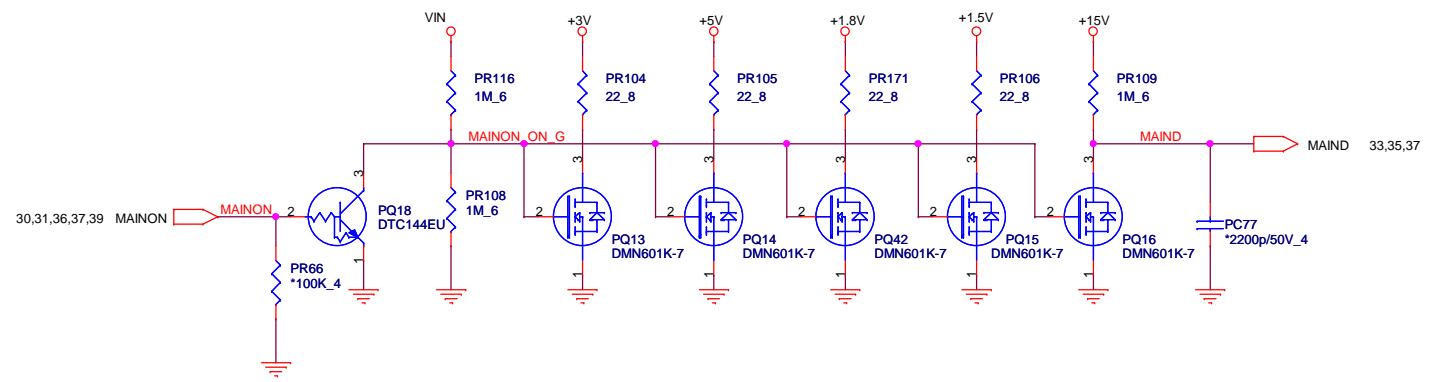
+1.5V\_GPU  
TDC : 2.1A  
PEAK : 2.8A  
Width : 90mil



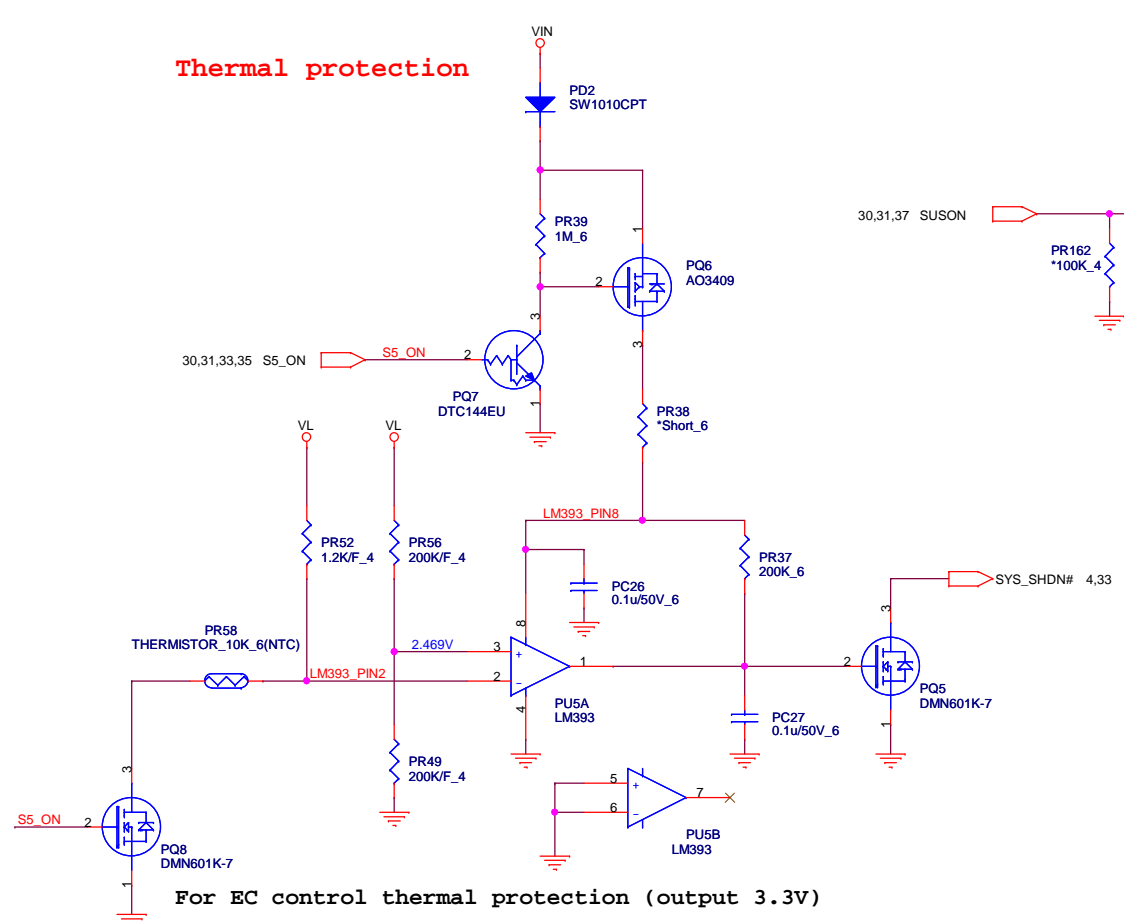
+1.8V\_GPU  
TDC : 1.41A  
PEAK : 1.88A  
Width : 60mil

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PROJECT : ZQG

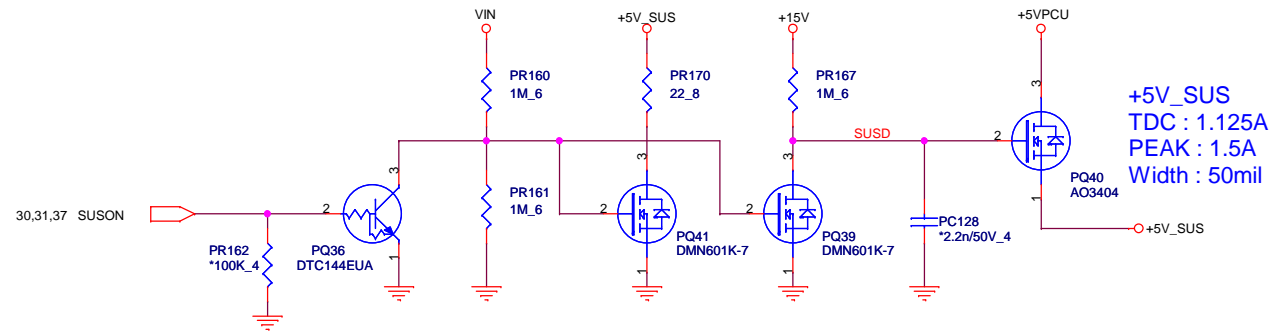
Size	Document Number	Rev
	<b>+1.8V / +1V_GPU / +1.5V_GPU / +1.8V_GPU</b>	1A
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**Thermal protection**



For EC control thermal protection (output 3.3V)



+5V\_SUS  
TDC : 1.125A  
PEAK : 1.5A  
Width : 50mil

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		1A
Size	Document Number	<b>Discharge /Thermal protection</b>
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ZQE/G M/B	3A	<p>C01</p> <p>C02 PAGE18 : to slove the Power DVD issue , setting size to 256MB</p> <p>C03 PAGE39 : add PR210,PC157,PQ61,PR198,PR200,PR199,PQ60,PC156,PQ69 for GPU +1V power source . changed control net from HWPG_1V to PG_GPUIO_EN</p> <p>C04 PAGE13 : change the power source from +1V to +1V_GPU</p> <p>C05 PAGE14 : change the power source from +1V to +1V_GPU</p> <p>C06 PAGE16 : change the power source from +1V to +1V_GPU</p> <p>C07 PAGE17 : change the power source from +1V to +1V_GPU</p> <p>C08 PAGE18 : to solve the HDMI issue , remove R112,R118 from BOMs</p> <p>C09 PAGE21 : Del D26 to slove HDMI issue.</p> <p>C10 PAGE26 : net PCBEEP connects with U11 by 10k ohm for AC pulg in /out function.</p> <p>C11 PAGE31 : Both MXM_SMCLK12 / MXM_SMDATA12 should be pull up to +3V by 10k ohm.</p> <p>C12 PAGE35 : stuff 10k ohm</p> <p>C13 PAGE36 : change PR169 PN from 0 ohm to 430K ohm for timing issue.</p> <p>C14 PAGE36 : stuff 10k ohm</p> <p>C15 PAGE36 : change PR75 PN from 3.57k to 3.65k</p> <p>C16 PAGE38 : remove PQ27 for cose down.</p> <p>C17 PAGE38 : remove PQ27 for cose down.</p> <p>C18 PAGE5 : Add C674 to reduce CRT noise.</p> <p>C19 PAGE5 : del R100 , add L58 to reduce CRT noise.</p>	1	1A	3A
			2	1A	3A
			3	1A	3A
			4	1A	3A
			5	1A	3A
			6	1A	3A
			7	1A	3A
			8	1A	3A
			9	1A	3A
			10	1A	3A
			11	1A	3A
			12	1A	3A
			13	1A	3A
			14	1A	3A
			15	1A	3A
			16	1A	3A
			17	1A	3A
			18	1A	3A
			19	1A	3A
			20	1A	3A
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			30	1A	3A
			31	1A	3A
			32	1A	3A
			33	1A	3A
			34	1A	3A
			35	1A	3A
			36	1A	3A
			37	1A	3A
			38	1A	3A
			39	1A	3A
			40	1A	3A
			41	1A	3A

Note :  
1. Remove Jumper : JP7,JP11,JP1,JP2,JP3,JP4,JP5,JP6,JP8,JP9,JP10,JP12,JP13,JP14,JP15,JP16,JP17,JP18



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