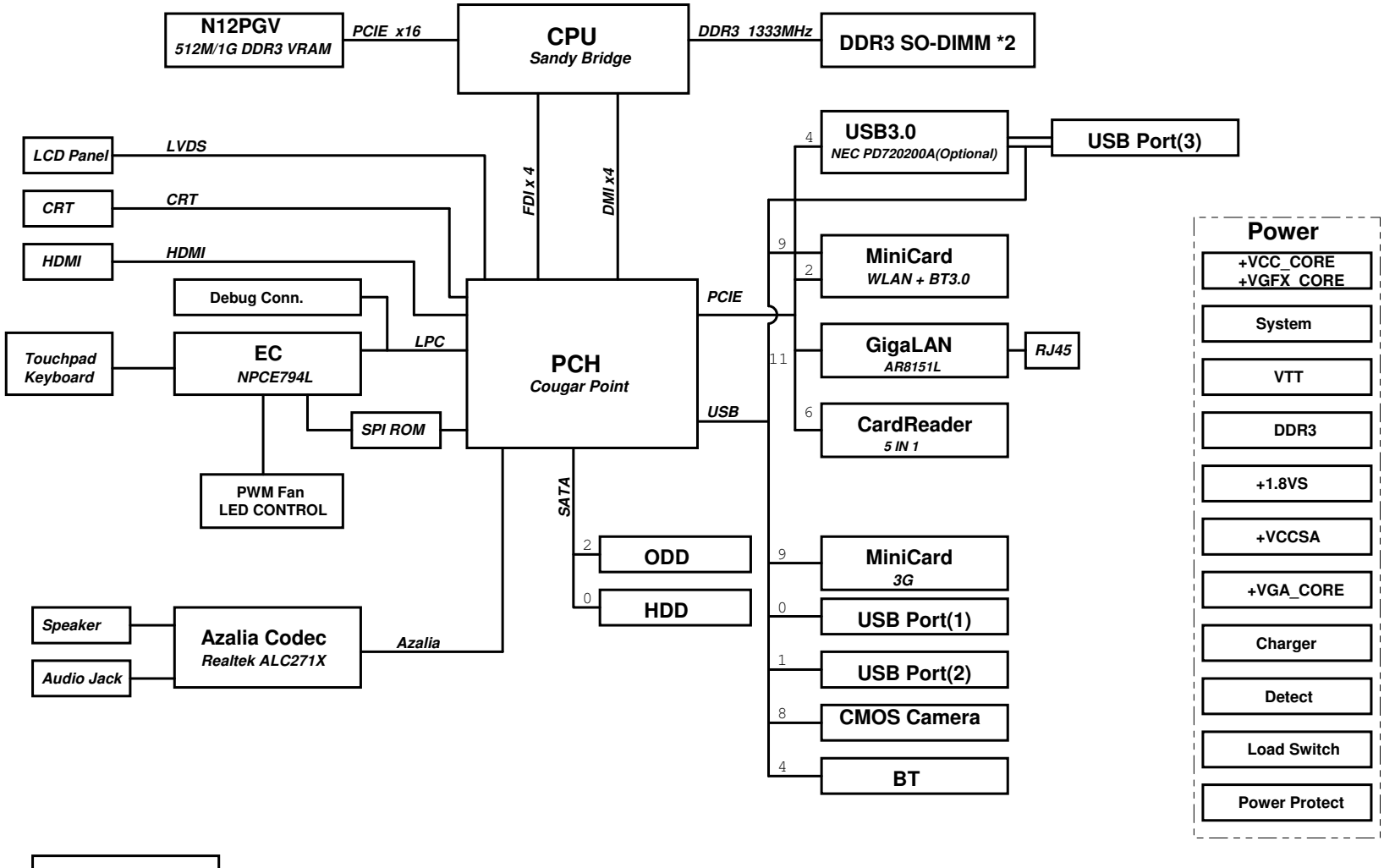
Huron River Platform Rev 2.1

BLOCK DIAGRAM



PEGATRON Title : System Setting
Engineer: JAY TSAI
Size: Custom | Project Name: EIH31 | Rev: 1.3
Date: Sunday, February 06, 2011 | Sheet 1 of 99

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)
PlamRest Thermal Sensor (G781)	1001100x (98h)

PCIE 1	CardReader
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

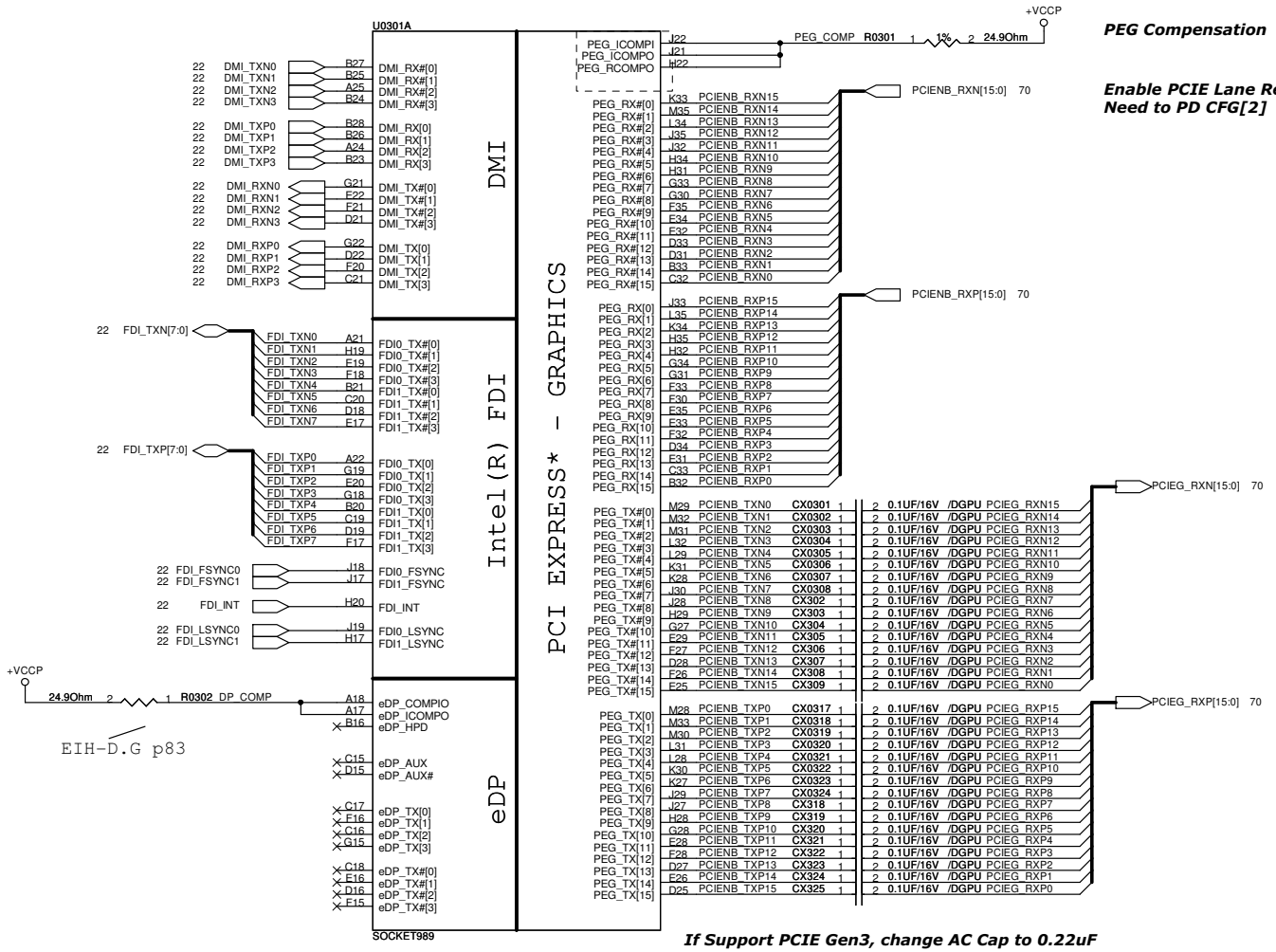
USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	N/A
USB 4	Bluetooth
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	SIM Card
USB 11	3G
USB 12	N/A
USB 13	N/A

PEGATRON Title : System Setting

Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

Date: Tuesday, January 04, 2011 Sheet 2 of 99



EIH31 : 1201-006D000 MOBILE rPGA CPU SOCKET 988B

PEGATRON	Title : CPU(1)_DMI,PEG,FDI,		
	Engineer: JAY TSAI		
Size: Custom	Project Name: EIH31		Rev: 1.0
Date: Friday, January 07, 2011	Sheet 3 of 99		

+1.5V_VCCDDQ +1.5V_VCCDDQ 7
+3VS +3VS 16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+3VSUS +3VSUS 22,24,27,28,30,59,81,82,84,92
+VCCP +VCCP 3,6,25,26,27,30,32,55,82
+3V +3V 24,52,53,55,59,91

U0301B

C26 will change to PROC_SELECT#

MISC
24 H_SNB_IVB# C26 SNB_IVB#
T0401 TP_SKTOCC# R AN34 SKTOCC#
T0402 TP_CATERR# R AL33 CATERR#

THERMAL
25 H_PECI AN33 PECI
+VCCP 75Ohm R0404 H_PROCHOT# 44.2Ohm R0403 H_PROCHOT# D AL32 PROCHOT#
25,32 H_THRMTRIP# SP0401 R0402 H_THRMTRIP# R AN32 THERMTRIP#

PWR MANAGEMENT
22 H_PM_SYNC SP0402 H_PM_SYNC_R AM34 PM_SYNC
10KOhm R0408
25 H_CPUPWRGD SP0403 H_CPUPWRGD_R AP33 UNCOREPWRGOOD
22 PM_DRAM_PWRGD 130Ohm R0409 VDDPWRGOOD_R R1.3 V8 SM_DRAMPWROK
24,30,32,40,53,59,70 BUF_PLT_RST# R0416 1.5KOhm BUF_CPU_RST# AR33 RESET#
R0417 750Ohm

SOCKET989
12V013ASM000

CLOCKS
BCLK A28 BCLK_CPU_P 0Ohm RN0401A CLK_EXP_P 21
BCLK# A27 BCLK_CPU_N 0Ohm RN0401B CLK_EXP_N 21
R0429 1KOhm
DPLL_REF_SSCLK A16 CLK_DP_P_R 0Ohm RN0402A CLK_DP_P 21
DPLL_REF_SSCLK# A15 CLK_DP_N_R 0Ohm RN0402B CLK_DP_N 21
@@
R0430 1KOhm +VCCP

EIH- D.G p83

DDR3 MISC
SM_DRAMRST# R8 CPUDRAMRST# 5
SM_RCOMP[0] AK1 SM_RCOMP_0 R0418 1% 140Ohm
SM_RCOMP[1] A5 SM_RCOMP_1 R0419 1% 25.5Ohm
SM_RCOMP[2] A4 SM_RCOMP_2 R0420 1% 200Ohm

Huron River platform Design Guide Update 440484
SM_RCOMP_1 use 26ohm 1%

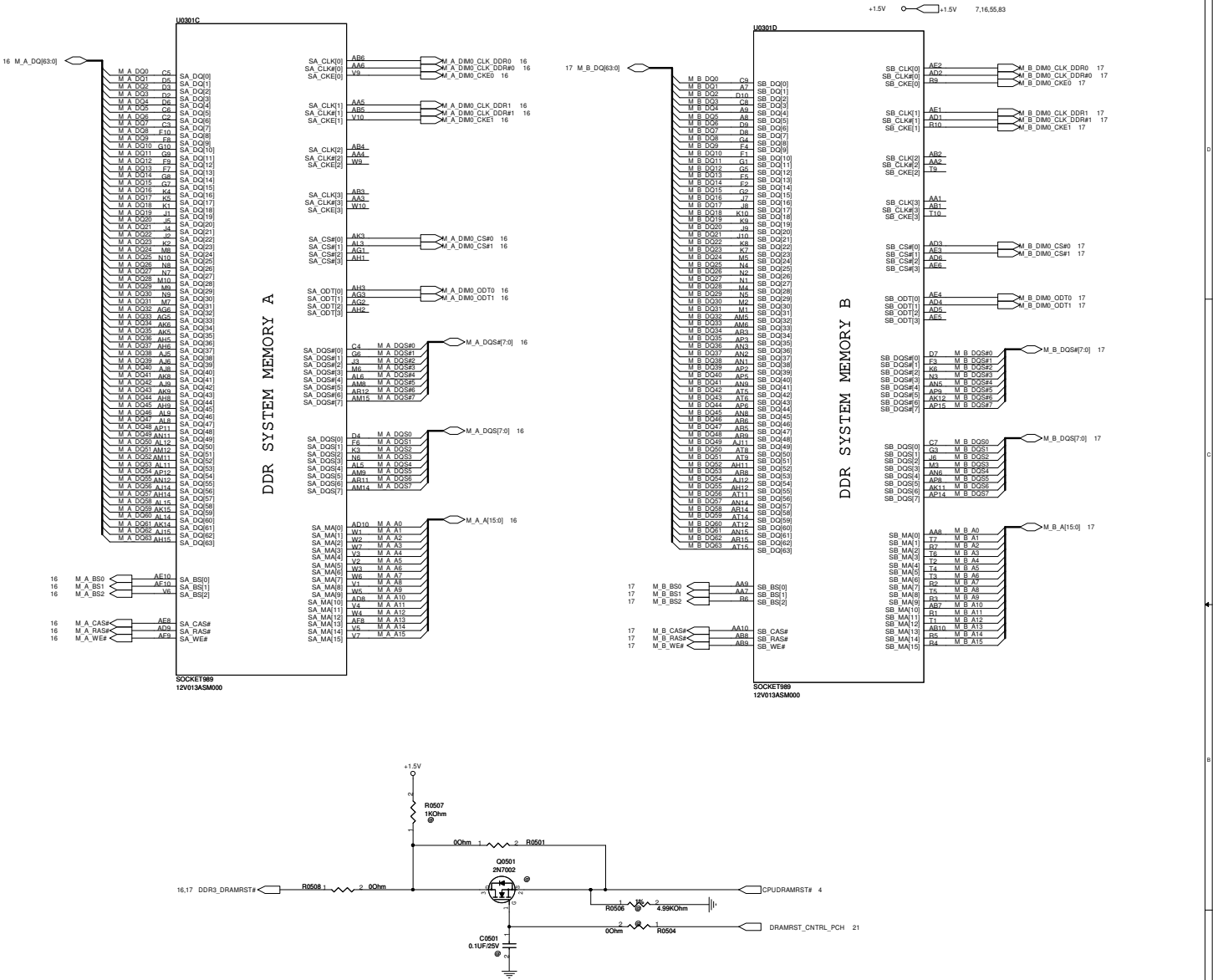
JTAG & BPM
PRDY# AP29 XDP_PRDY# T0403
PREQ# AP27 XDP_PREQ#
TCK AR26 XDP_TCK
TMS AR27 XDP_TMS
TRST# AP30 XDP_TRST#
TDI AR28 XDP_TDI
TDO AP26 XDP_TDO
DBR# AL35 H_DBR#
BPM#[0] AT28 XDP_BPM#0 T0411
BPM#[1] AR29 XDP_BPM#1
BPM#[2] AR30 XDP_BPM#2 T0413
BPM#[3] AT30 XDP_BPM#3 T0414
BPM#[4] AP32 XDP_BPM#4 T0415
BPM#[5] AR31 XDP_BPM#5 T0416
BPM#[6] AT31 XDP_BPM#6 T0417
BPM#[7] AR32 XDP_BPM#7 T0418

+VCCP
XDP_BPM#1 R0428 51Ohm @
XDP_PREQ# R0421 51Ohm
XDP_TDI R0422 51Ohm @
XDP_TDO R0423 51Ohm
XDP_TMS R0424 51Ohm @
H_DBR# R0425 1KOhm @ +3VS
XDP_TCK R0426 51Ohm @
XDP_TRST# R0427 51Ohm

R1.3 Add VR_HOT#
80 VR_HOT# 0Ohm @ R0462
H_PROCHOT#
Q0401 2N7002
THRO_CPU THRO_CPU 30

PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ
+1.5V_VCCDDQ +3VSUS +3V
R0449 200Ohm 1%
1.57 Volt
U0404 Vcc=1.65~5.5 @
PM_DRAM_PWRGD 0Ohm R0451
R0452 1.1KOhm 1% @
C0405 0.22UF/10V @
R0450 1KOhm 1% @
R0453 10KOhm @
Q0403 PMBS3904 @
R0454 24.3KOhm 1% @
+1.5V_VCCDDQ
C0404 0.22UF/10V @
R0455 47KOhm 1% @

PEGATRON Title : CPU(2)_CLK,MISC,JTA
Engineer: JAY TSAI
Size Custom | Project Name EIH31 | Rev 1.0
Date: Friday, January 07, 2011 | Sheet 4 of 99



PEGATRON	Title : CPU(3)_DDR3		
	Engineer: JAY TSAI		
Size: Custom	Project Name: EIH31		Rev: 1.0
Date: Friday, January 07, 2011		Sheet 5 of 99	

POWER

U0301F

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

+VCC_CORE

+VCCP

SV-DC
0.8V ~ 1.35V

53A

8.5A

+VCCP +VCCP 3,4,25,26,27,30,32,55,82

+VCC_CORE +VCC_CORE 80

ER1.16

CE0601 CE0602 A14 at Power side

VR_SVID_ALERT# 80

VR_SVID_CLK 80

VR_SVID_DATA 80

VCCSENSE 80

VSSSENSE 80

SOCKET989

12V013ASM000

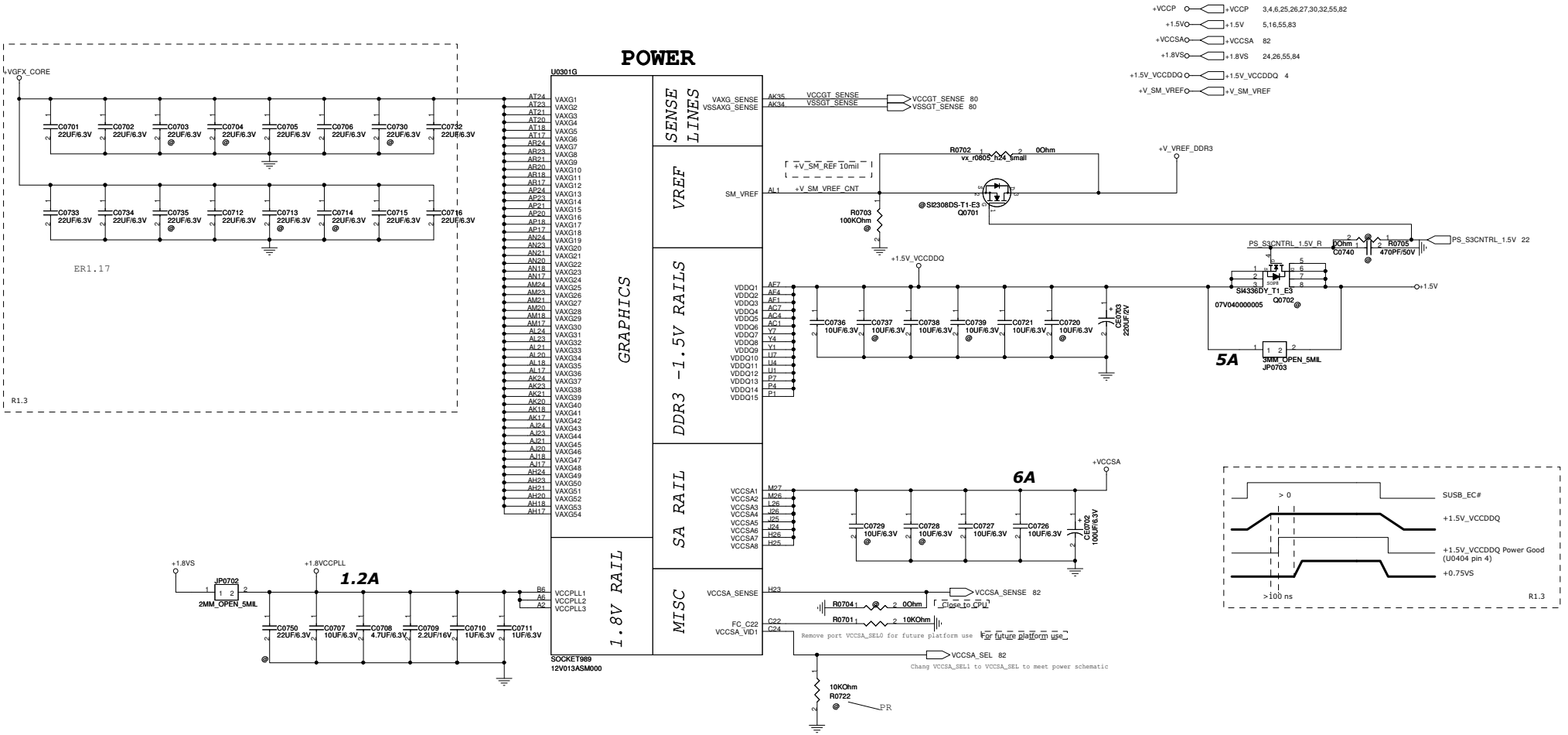
PEGATRON Title : CPU(4)_PWR

Engineer: JAY TSAI

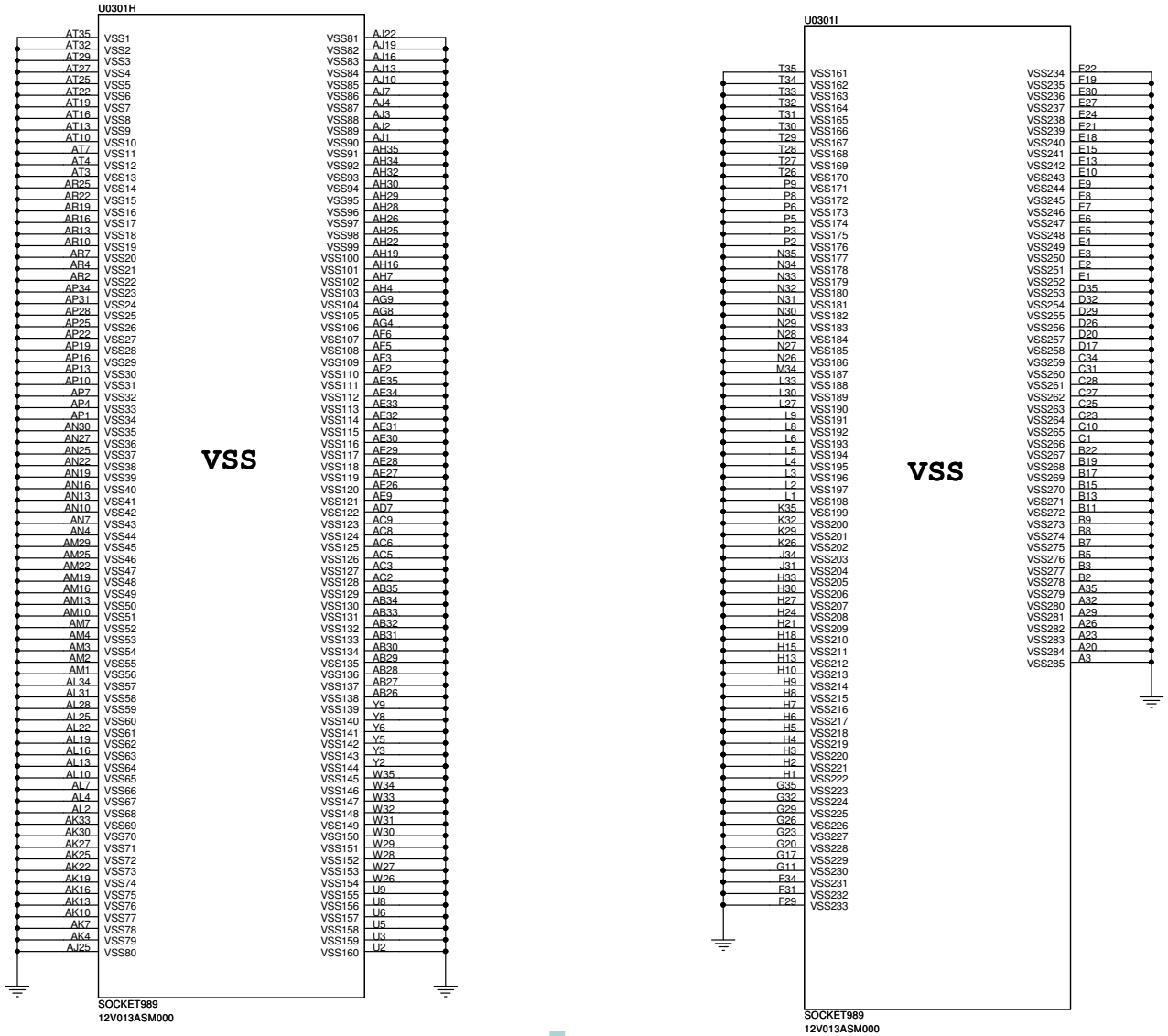
Size: Custom | Project Name: EIH31 | Rev: 1.0

Date: Thursday, January 13, 2011 | Sheet 6 of 99

POWER



PEGATRON	Title : CPU(5)_PWR	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Thursday, January 13, 2011	Sheet 7 of 99	



PEGATRON Title : CPU(6)_CFG,RSVD,GI

Engineer: JAY TSAI

Size	Project Name	Rev
Custom	EIH31	1.0

Date: Tuesday, January 04, 2011 Sheet 8 of 99

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection

- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

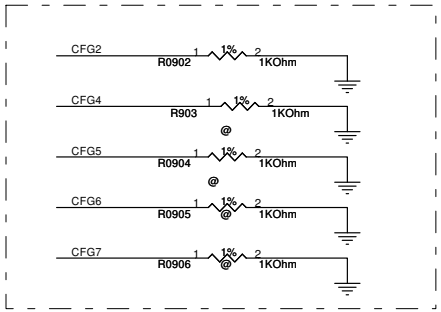
CFG[6:5]: PCI Express Port Bifurcation Straps

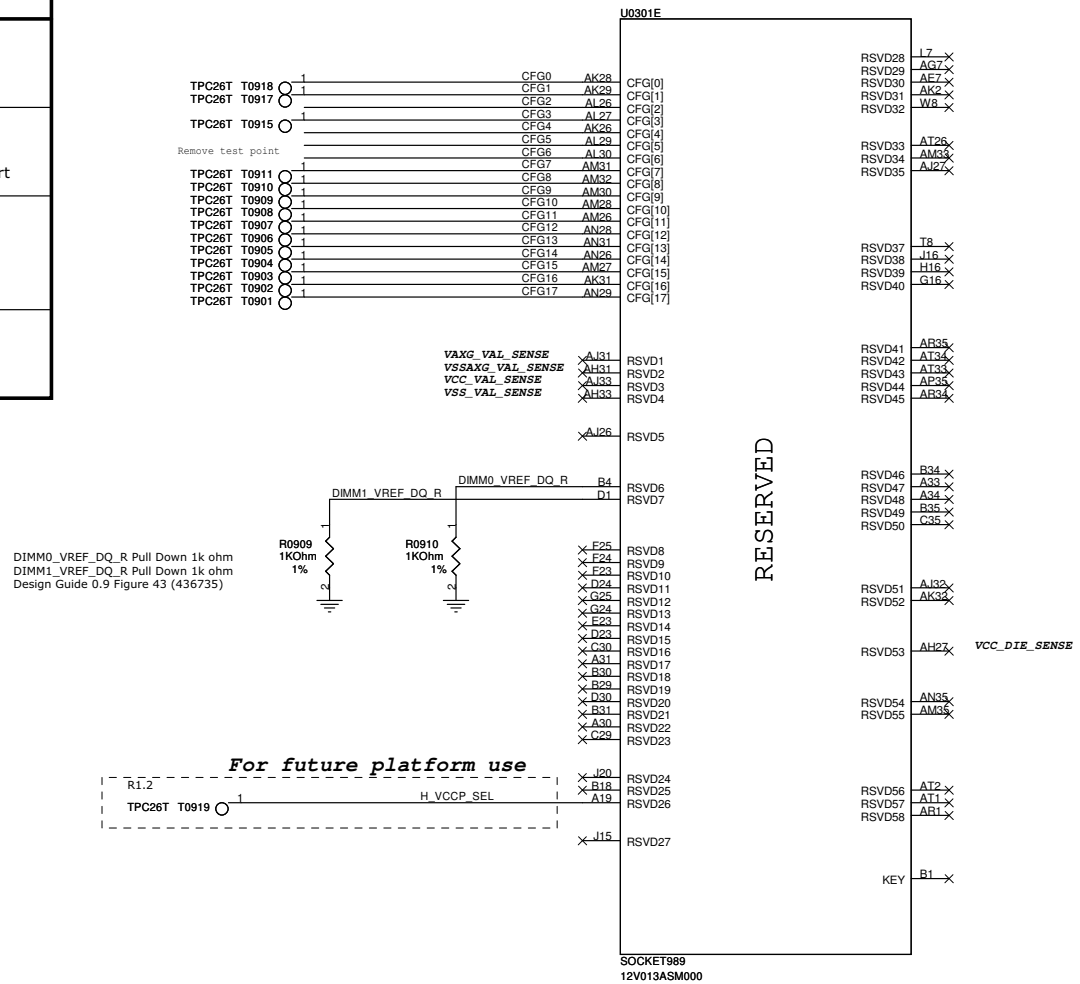
- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training

CFG2 : Check H34 layout request





PEGATRON Title : CPU(7)_CFG,RSVD,GH
Engineer: JAY TSAI
Size: Custom | Project Name: EIH31 | Rev: 1.0
Date: Tuesday, January 04, 2011 | Sheet 9 of 99

PEGATRON

Title : NB(7)_****

Engineer: *JAY TSAI*

Size	Project Name	Rev
A	EIH31	1.3

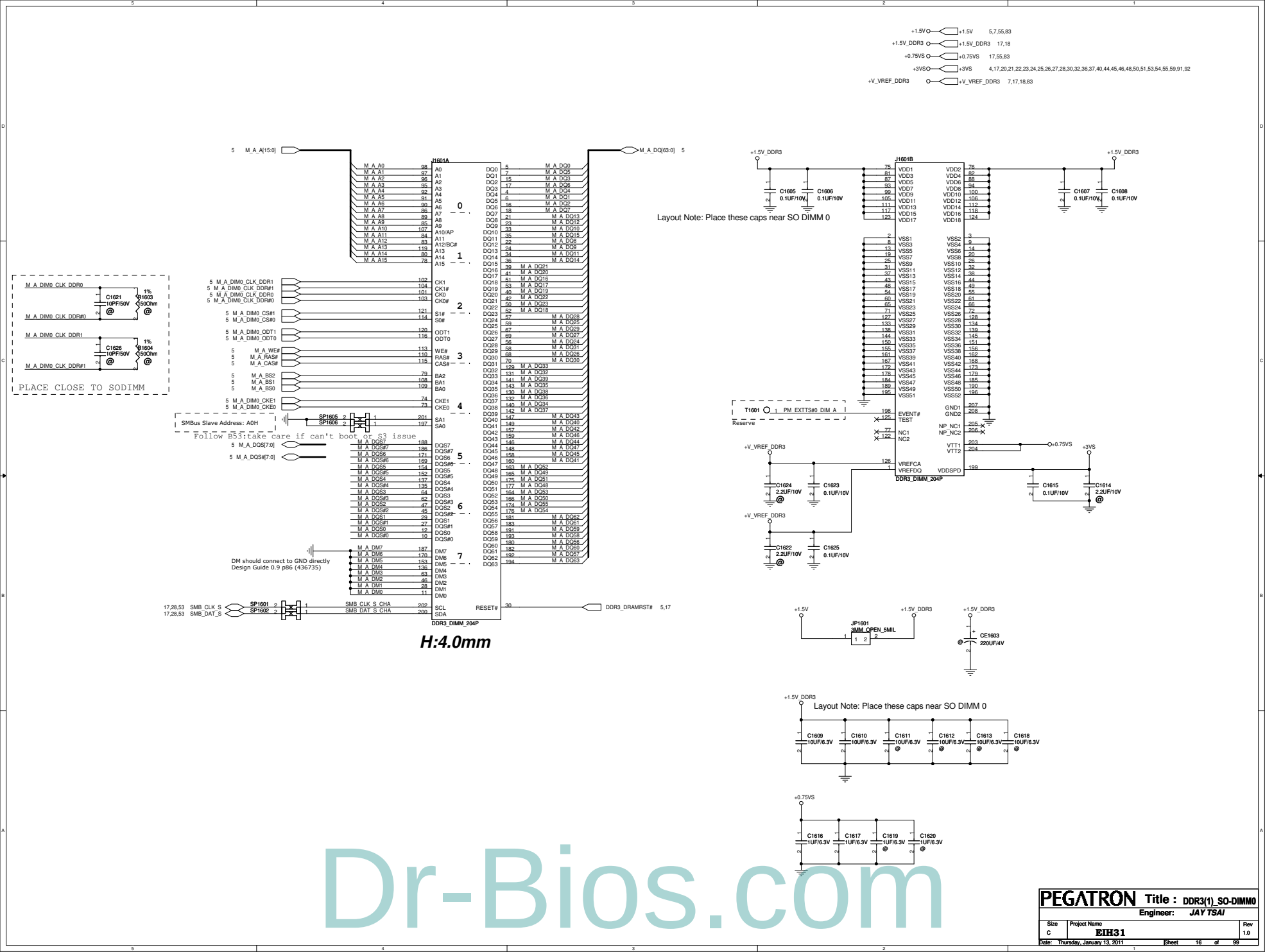
Date: Tuesday, January 04, 2011 Sheet 14 of 99

PEGATRON Title : NB(8)_****

Engineer: *JAY TSAI*

Size	Project Name	Rev
A	EIH31	1.3

Date: Tuesday, January 04, 2011 Sheet 15 of 99



PEGATRON	Title : DDR3(1)_SO-DIMM0	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.0
Date: Thursday, January 13, 2011	Sheet 16 of 99	

+1.5V → +1.5V 5,7,16,55,83
+1.5V_DDR3 → +1.5V_DDR3 16,18
+0.75VS → +0.75VS 16,55,83
+3VS → +3VS 4,16,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+V_VREF_DDR3 → +V_VREF_DDR3 7,16,18,83

5 M_B_A[15:0]

M_B_DQ[63:0] 5

J1701A

M_B_A0	98	A0	DQ0	5	M_B_DQ4
M_B_A1	97	A1	DQ1	7	M_B_DQ5
M_B_A2	96	A2	DQ2	15	M_B_DQ3
M_B_A3	95	A3	DQ3	17	M_B_DQ6
M_B_A4	92	A4	DQ4	4	M_B_DQ0
M_B_A5	91	A5	DQ5	6	M_B_DQ1
M_B_A6	90	A6	DQ6	16	M_B_DQ2
M_B_A7	86	A7	DQ7	18	M_B_DQ7
M_B_A8	89	A8	DQ8	21	M_B_DQ13
M_B_A9	85	A9	DQ9	23	M_B_DQ12
M_B_A10	107	A10/AP	DQ10	33	M_B_DQ14
M_B_A11	84	A11	DQ11	35	M_B_DQ15
M_B_A12	83	A12/BC#	DQ12	22	M_B_DQ8
M_B_A13	119	A13	DQ13	24	M_B_DQ9
M_B_A14	80	A14	DQ14	34	M_B_DQ11
M_B_A15	78	A15	DQ15	36	M_B_DQ10
			DQ16	39	M_B_DQ16
			DQ17	41	M_B_DQ17
			DQ18	51	M_B_DQ19
			DQ19	53	M_B_DQ22
			DQ20	40	M_B_DQ20
			DQ21	42	M_B_DQ21
			DQ22	50	M_B_DQ23
			DQ23	52	M_B_DQ18
			DQ24	57	M_B_DQ31
			DQ25	59	M_B_DQ27
			DQ26	67	M_B_DQ26
			DQ27	69	M_B_DQ30
			DQ28	56	M_B_DQ24
			DQ29	58	M_B_DQ28
			DQ30	68	M_B_DQ25
			DQ31	70	M_B_DQ29
			DQ32	129	M_B_DQ37
			DQ33	131	M_B_DQ36
			DQ34	141	M_B_DQ39
			DQ35	143	M_B_DQ38
			DQ36	130	M_B_DQ33
			DQ37	132	M_B_DQ32
			DQ38	140	M_B_DQ35
			DQ39	142	M_B_DQ34
			DQ40	147	M_B_DQ45
			DQ41	149	M_B_DQ40
			DQ42	157	M_B_DQ46
			DQ43	159	M_B_DQ47
			DQ44	146	M_B_DQ41
			DQ45	148	M_B_DQ44
			DQ46	158	M_B_DQ42
			DQ47	160	M_B_DQ43
			DQ48	163	M_B_DQ48
			DQ49	165	M_B_DQ53
			DQ50	175	M_B_DQ52
			DQ51	177	M_B_DQ49
			DQ52	164	M_B_DQ50
			DQ53	166	M_B_DQ51
			DQ54	174	M_B_DQ54
			DQ55	176	M_B_DQ55
			DQ56	181	M_B_DQ58
			DQ57	183	M_B_DQ60
			DQ58	191	M_B_DQ63
			DQ59	193	M_B_DQ61
			DQ60	180	M_B_DQ56
			DQ61	182	M_B_DQ57
			DQ62	192	M_B_DQ59
			DQ63	194	M_B_DQ62
M_B_DM7	187	DM7			
M_B_DM6	170	DM6			
M_B_DM5	153	DM5			
M_B_DM4	136	DM4			
M_B_DM3	63	DM3			
M_B_DM2	46	DM2			
M_B_DM1	28	DM1			
M_B_DM0	11	DM0			
		SCL	RESET#	30	DDR3_DRAMRST# 5,16
		SDA			

DDR3_DIMM_204P
12V02GISM000

H:8.0mm

5 M_B_DIM0_CLK_DDR1 → CK1 102
5 M_B_DIM0_CLK_DDR#1 → CK1# 104
5 M_B_DIM0_CLK_DDR0 → CK0 101
5 M_B_DIM0_CLK_DDR#0 → CK0# 103

5 M_B_DIM0_CS#1 → S1# 121
5 M_B_DIM0_CS#0 → S0# 114

5 M_B_DIM0_ODT1 → ODT1 120
5 M_B_DIM0_ODT0 → ODT0 116

5 M_B_WE# → WE# 113
5 M_B_RAS# → RAS# 110
5 M_B_CAS# → CAS# 115

5 M_B_BS2 → BA2 79
5 M_B_BS1 → BA1 108
5 M_B_BS0 → BA0 109

5 M_B_DIM0_CKE1 → CKE1 74
5 M_B_DIM0_CKE0 → CKE0 73

SMBus Slave Address: A4H

+3VS — R1709 1 — 2 30K0hm — SP1703 2 — 1 — SA1 201, SA0 197

take care if can't boot or S3 issue

5 M_B_DQS[7:0] → DQS7 188, DQS#7 186, DQS6 171, DQS#6 169, DQS5 154, DQS#5 152, DQS4 137, DQS#4 135, DQS3 64, DQS#3 62, DQS2 47, DQS#2 45, DQS1 29, DQS#1 27, DQS0 12, DQS#0 10
5 M_B_DQS#[7:0]

DM should connect to GND directly
Design Guide 0.9 p86 (436735)

16,28,53 SMB_CLK_S — SP1701 2 — 1 — SMB_CLK_S_CHB 202
16,28,53 SMB_DAT_S — SP1702 2 — 1 — SMB_DAT_S_CHB 200

M_B_DIM0_CLK_DDR0 — C1720 10PF/50V — 150Ohm R1707 — M_B_DIM0_CLK_DDR#0
M_B_DIM0_CLK_DDR1 — C1721 10PF/50V — 150Ohm R1708 — M_B_DIM0_CLK_DDR#1
PLACE CLOSE TO SODIMM

+1.5V_DDR3
C1705 0.1UF/10V
C1706 0.1UF/10V
C1707 0.1UF/10V
C1708 0.1UF/10V
Layout Note: Place these caps near SO DIMM 1

J1701B

		VDD1	VDD2	75	76
		VDD3	VDD4	81	82
		VDD5	VDD6	87	88
		VDD7	VDD8	93	94
		VDD9	VDD10	99	100
		VDD11	VDD12	105	106
		VDD13	VDD14	111	112
		VDD15	VDD16	117	118
		VDD17	VDD18	123	124
		VSS1	VSS2	2	3
		VSS3	VSS4	8	9
		VSS5	VSS6	13	14
		VSS7	VSS8	19	20
		VSS9	VSS10	25	26
		VSS11	VSS12	31	32
		VSS13	VSS14	37	38
		VSS15	VSS16	43	44
		VSS17	VSS18	48	49
		VSS19	VSS20	54	55
		VSS21	VSS22	60	61
		VSS23	VSS24	65	66
		VSS25	VSS26	71	72
		VSS27	VSS28	127	128
		VSS29	VSS30	133	134
		VSS31	VSS32	138	139
		VSS33	VSS34	144	145
		VSS35	VSS36	150	151
		VSS37	VSS38	155	156
		VSS39	VSS40	161	162
		VSS41	VSS42	167	168
		VSS43	VSS44	172	173
		VSS45	VSS46	178	179
		VSS47	VSS48	184	185
		VSS49	VSS50	189	190
		VSS51	VSS52	195	196
		GND1	GND2		207, 208
		EVENT#		198	
		TEST		125	
		NC1	NP_NC1	77	205
		NC2	NP_NC2	122	206
		VTT1			203
		VTT2			204
		VREFCA		126	
		VREFDQ	VDDSPD	1	199

T1701 1 PM_EXTTS#0_DIM_B
Reserve

DDR3_DIMM_204P
12V02GISM000

+0.75VS
+3VS
+V_VREF_DDR3
C1724 2.2UF/10V
C1723 0.1UF/10V
C1722 2.2UF/10V
C1725 0.1UF/10V
C1715 0.1UF/10V
C1714 2.2UF/10V

+1.5V_DDR3
CE1703 220UF/4V

+1.5V_DDR3
Layout Note: Place these caps near SO DIMM 1
C1709 10UF/6.3V
C1710 10UF/6.3V
C1711 10UF/6.3V
C1712 10UF/6.3V
C1713 10UF/6.3V
C1718 10UF/6.3V

+0.75VS
C1716 1UF/6.3V
C1717 1UF/6.3V
C1630 1UF/6.3V
C1631 1UF/6.3V

PEGATRON Title : DDR3(2)_SO-DIMM1
Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.0
Date: Thursday, January 13, 2011 | Sheet 17 of 99

+1.5V_DDR3 +1.5V_DDR3 16,17

+V_VREF +V_VREF
+V_VREF_DDR3 +V_VREF_DDR3 7,16,17,83
+V_SM_VREF +V_SM_VREF

+3V +3V 4,24,52,53,55,59,91
+5VSUS +5VSUS 22,27,81,82,83,84,87,91
+5VA +5VA 59,81,88

DDR3 Vref

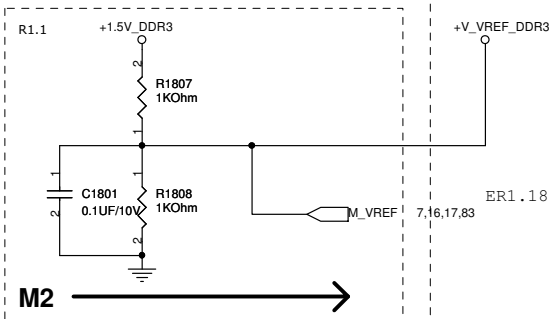
Default M1

R1.1

Power remove M_REF function.

M1: Fixed SO-DIMM VREF_DQ

M2: Programmable SO-DIMM VREFDQ on motherboard– New Requirement



PEGATRON	Title DDR3(3)_CA/DQ Voltage	
	Engineer: JAY TSAI	
Size B	Project Name EIH31	Rev 1.0
Date: Thursday, January 13, 2011	Sheet 18 of 99	

R1.4--2

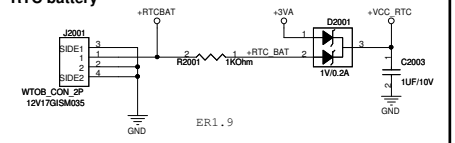
PEGATRON Title : VID Controller

Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

Date: Tuesday, January 04, 2011 Sheet 19 of 99

RTC battery



Connector Type 1217-001L000

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

+VCC_RTC RTCRST# RC delay should be 18ms~25ms

R2003 20KOhm, C2004 1UF/10V, JRST2001 SGL_JUMP @, R2004 20KOhm, R2005 1MOhm, C2005 1UF/10V, JRST2002 SGL_JUMP @

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs

PCH_INTVRMEN R2030 200KOhm 1% R1_3

+VCC_RTC R2006 200KOhm 1% R1_3

C2001 15PF/50V, C2002 15PF/50V, X2001 32.768KHZ, R2002 10MOhm, R0402, SP2005

RTC_X1 A20, RTC_X2 C20, RTC_RST# D20, SRTC_RST# G22, SM_INTRUDER# K22, PCH_INTVRMEN C17

Remove 3 Test point

U2001A

RTC: RTCX1 A20, RTCX2 C20, RTCRST# D20, SRTCRST# G22, INTRUDER# K22, INTVRMEN C17

LPC: FWH0/LAD0 C38, FWH1/LAD1 A38, FWH2/LAD2 B37, FWH3/LAD3 C37, FWH4/LFRAME# D36, LDRQ0# F36, LDRQ1#/GPIO23 K36, SERIRQ V5

IHDA: HDA_BCLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN#/GPIO33 C36, HDA_DOCK_RST#/GPIO13 N32

JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO

SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3

SATA: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5, SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10, SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4, SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1, SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1, SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO Y11, SATAICOMPI Y10, SATA3RCOMPO AB12, SATA3COMPI AB13, SATA3RBIAS AH1, SATALED# P3, SATA0GP/GPIO21 V14, SATA1GP/GPIO19 P1

SATA 6G: SATA_RXN0 51, SATA_RXP0 51, SATA_TXN0 51, SATA_TXP0 51, SATA_RXN1 51, SATA_RXP1 51, SATA_TXN1 51, SATA_TXP1 51

HDD1

SATA_RXN2 51, SATA_RXP2 51, SATA_TXN2 51, SATA_TXP2 51

ODD

SATA_COMP R2007 37.4Ohm, SATA3_COMP R2047 49.9Ohm, RBIAS_SATA3 R2048 750Ohm, R2025 10KOhm, SATA_LED# 54, SATA0GP, BBS_BIT0 24

COUGAR_POINT_ES1

0200-00HU000 C.S 907552 A1 QMVY BGA942 INTEL/COUGAR POINT PCH

Remove SATA_DET#0_R, BBS_BIT0_R for xDP Connector

HDA_BCLK ← ACZ_BCLK_AUD (36) SP2006 R0402
HDA_SYNC ← ACZ_SYNC_AUD (36) SP2007 R0402
SPKR ← SB_SPKR (36)
HDA_RST# ← ACZ_RST#_AUD (36,37) SP2008 R0402
HDA_SDIN0 ← ACZ_SDIN0_AUD (36)
Remove TP
HDA_SDO ← ACZ_SDOUT_AUD (36) SP2009 R0402
R2050 near SP2009
PCH_FLASH_DESCRIPTOR (30) R2050 0Ohm

T2013 R1.2 Pull Down at CardReader
Remove CARDREADER_RESET#

T2024 PCH_JTAG_TCK_BUF, T2025 PCH_JTAG_TMS, T2026 PCH_JTAG_TDI, T2027 PCH_JTAG_TDO

SPI_CLK (28), SPI_CS#0 (28)
No Support 64Mb BIOS ROM T2028
SPI_SI (28), SPI_SO (28)

Remove xDP component

Strap information:

SB_SPKR: No reboot strap
Low: Disable (Default)
High:Enable
SB_SPKR R2020 1KOhm +3VS

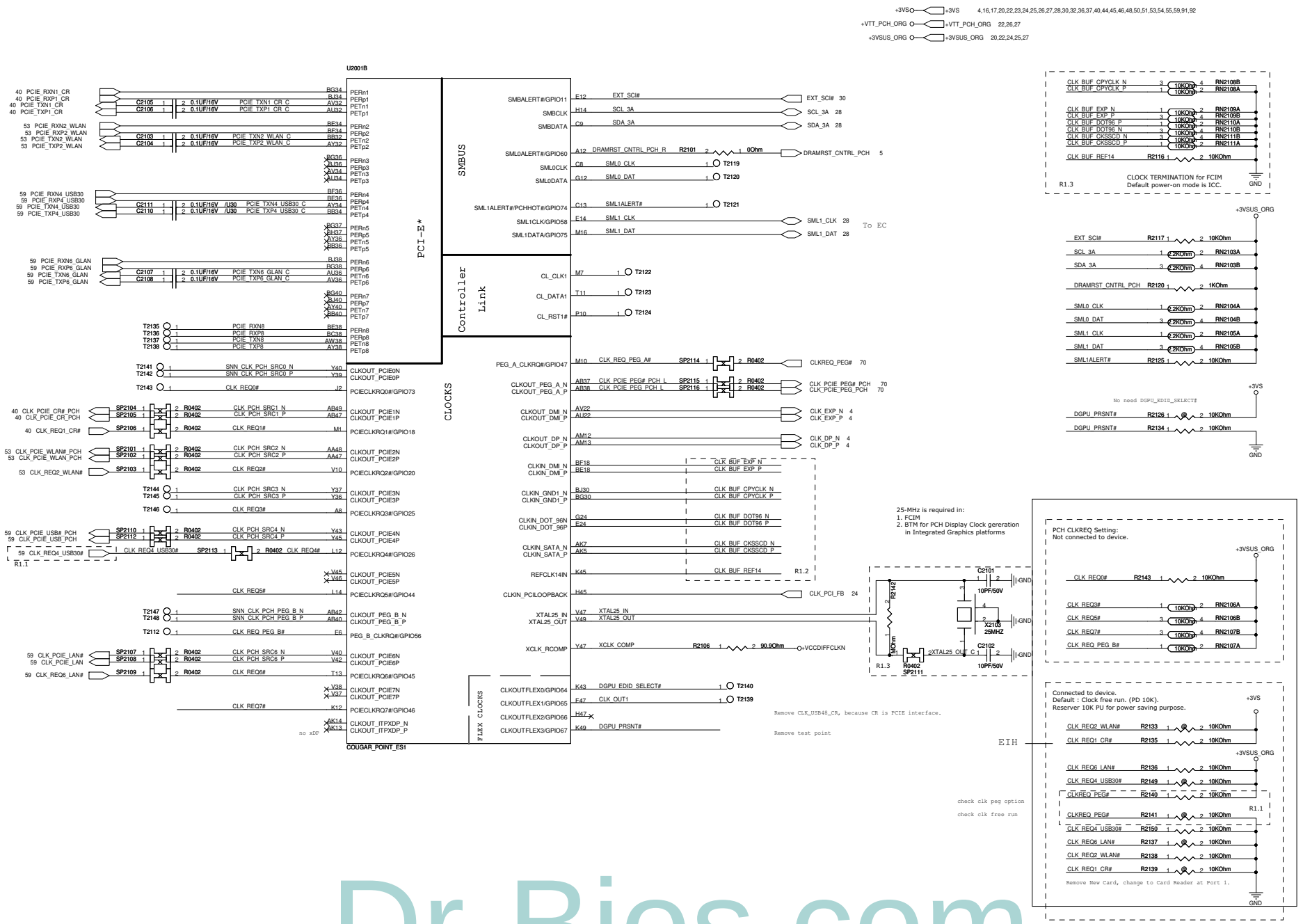
ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.ACZ_SDOUTwhich sample high on the rising edge of PWROK
Will also disable Intel ME.
ACZ_SDOUT R2034 1KOhm +3VSUS_ORG

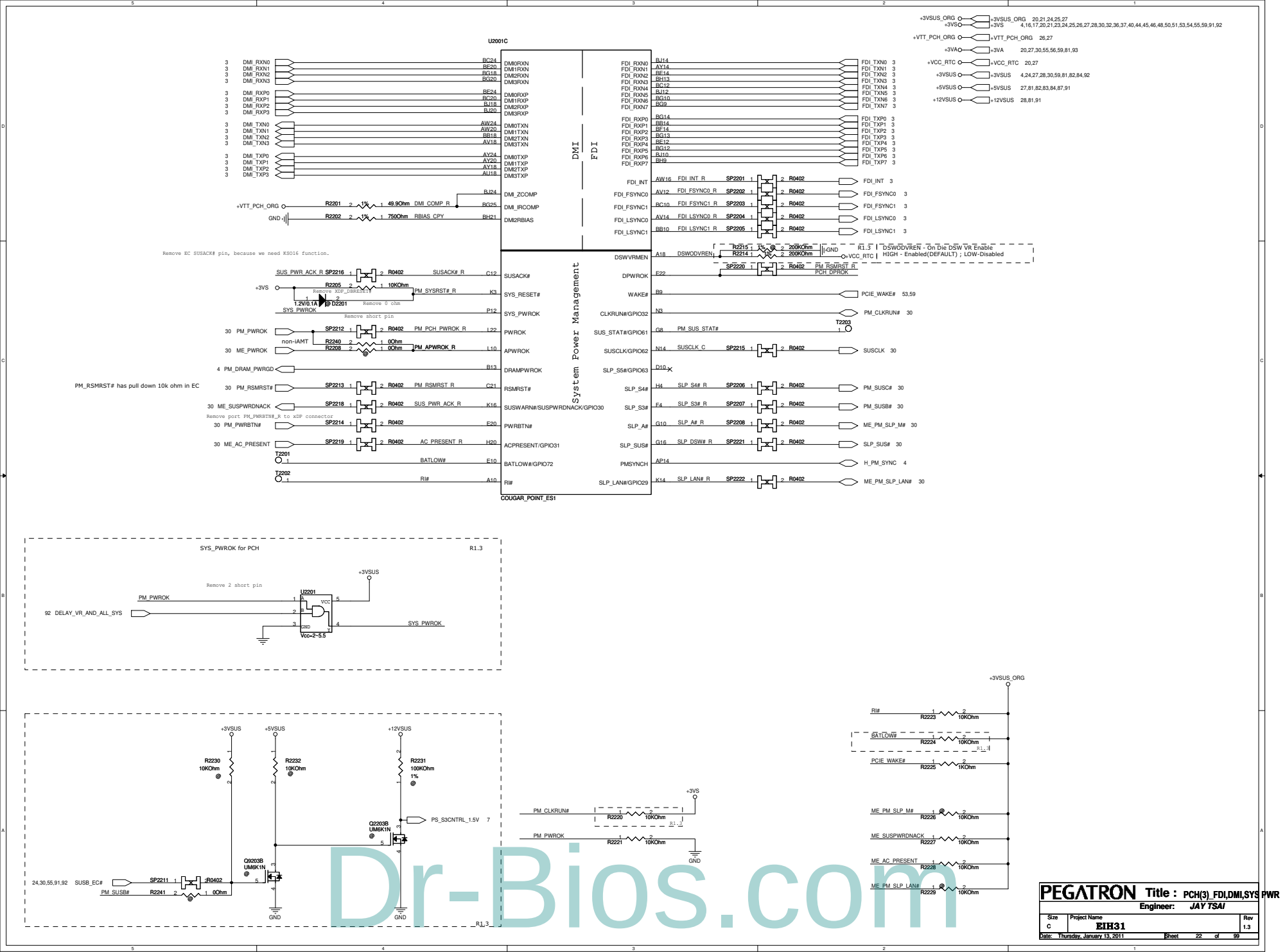
ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hrron River Platform Schematic Design Checklist (438390 page 48)
ACZ_SYNC R2036 1KOhm +3VSUS_ORG
VCCVRAM use +1.5VS in mobile

Pull High +3VS
INT_SERIRQ R2026 10KOhm
SATA0GP R2027 10KOhm

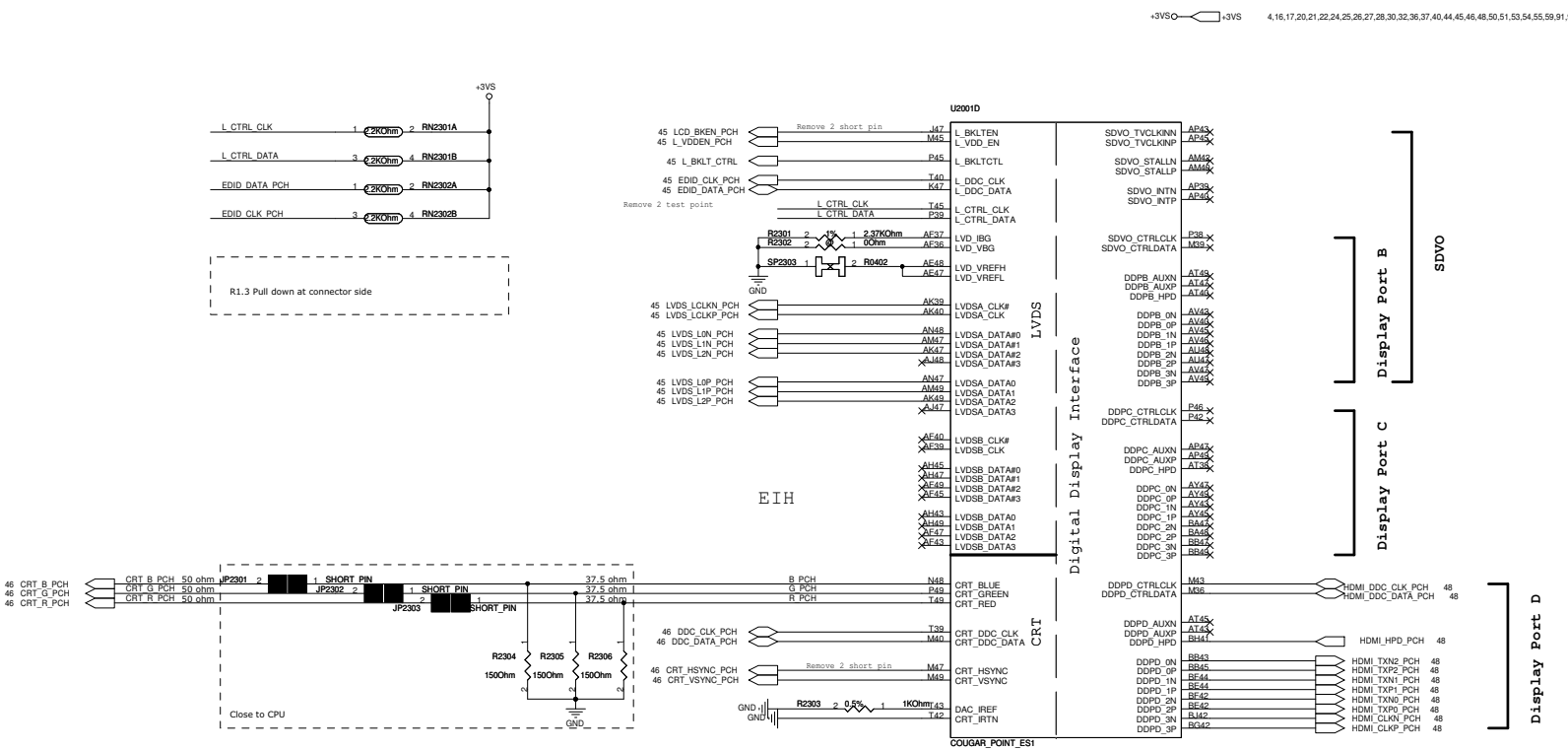
+VCC_RTC +VCC_RTC 22,27
+RTCBAT +RTCBAT
+3VA +3VA 27,30,55,56,59,81,93
+3VS +3VS 4,16,17,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+3VSUS_ORG +3VSUS_ORG 21,22,24,25,27
+1.05VM_ORG +1.05VM_ORG 27
+VTT_PCH_VCCIO +VTT_PCH_VCCIO 26,27

PEGATRON Title : PCH(1)_SATA,IHDA,RTC,LPC
Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.3
Date: Thursday, January 13, 2011 | Sheet 20 of 99


+3VS +3VS 4,16,17,20,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27
+3VSUS_ORG +3VSUS_ORG 20,22,24,25,27
U2001B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR_POINT_ES1
CLOCK TERMINATION for FCIM
Default power-on mode is ICC.
To EC
25-MHz is required in:
1. FCIM
2. BTM for PCH Display Clock gereration in Integrated Graphics platforms
PCH CLKREQ Setting:
Not connected to device.
Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.
EIH
check clk peg option
check clk free run
Remove CLK_USB48_CR, because CR is PCIE interface.
Remove test point
Remove New Card, change to Card Reader at Port 1.
No need DGPU_EDID_SELECT#
PEGATRON
Title : PCH(2)_PCIE,CLK,SMB,PEG
Engineer: JAY TSAI
Size C
Project Name EIH31
Rev 1.3
Date: Friday, January 07, 2011
Sheet 21 of 99



PEGATRON	Title : PCH(3) FDI,DMI,SYS PWR
	Engineer: JAY TSAI
Size: C	Project Name: EIH31
Rev: 1.3	
Date: Thursday, January 13, 2011	Sheet 22 of 99



CRT Disable: (For discrete graphic)

1. **NC:**
   CRT_RED,CRT_GREEN,CRT_BLUE
   CRT_HSYCN,CRT_VSYNC
2. **1-kΩ ±0.5% pull-down to GND:**
   DAC_IREF
3. **Connected to GND:**
   CRT_ITRN
4. **Connect to +V3.3:**
   VCCADAC

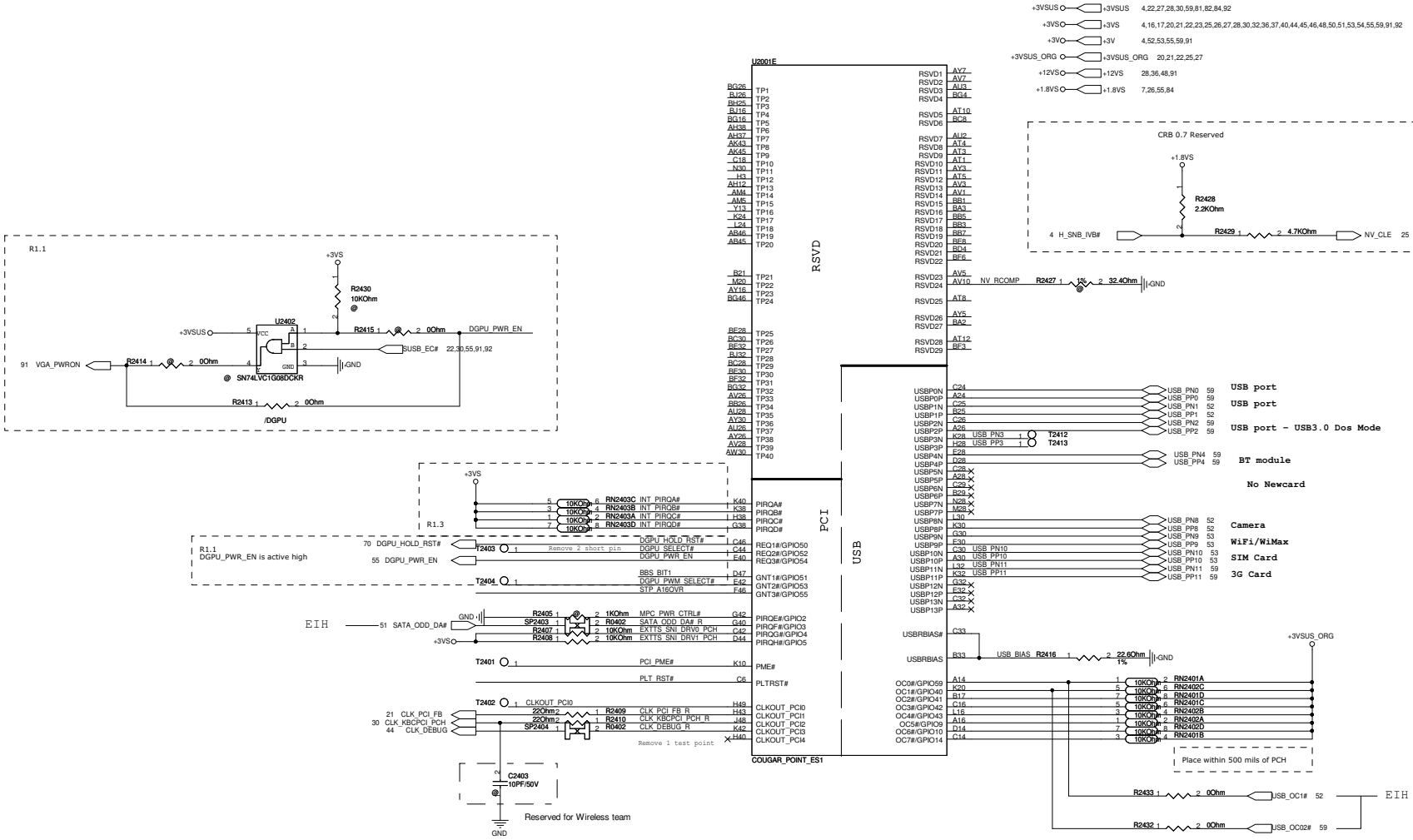
DisPlay Port Disable: (For discrete graphic)

1. **NC:**
   ALL

LVDS Disable: (For discrete graphic)

1. **NC:**
   LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
   LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
   LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
   L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
   LVD_VREFL, LVD_IBG, LVD_VBG
2. **Connected to GND:**
   VccALVDS,VccTX_LVDS

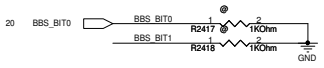
PEGATRON	Title : PCH(4)_DP,LVDS,CRT	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, January 07, 2011	Sheet 23 of 99	



BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

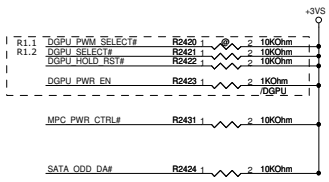
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI **(PCH)**

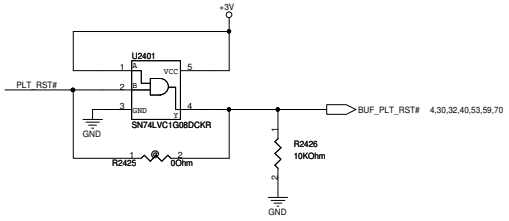
Sampled on rising edge of PWROK.



STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper

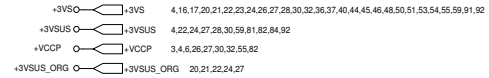
Low=Enabled A16 swap override/ Top-Block swap override
High=Default

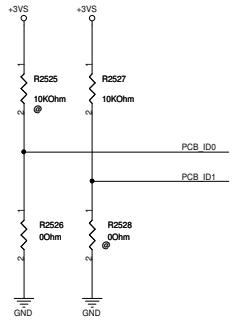




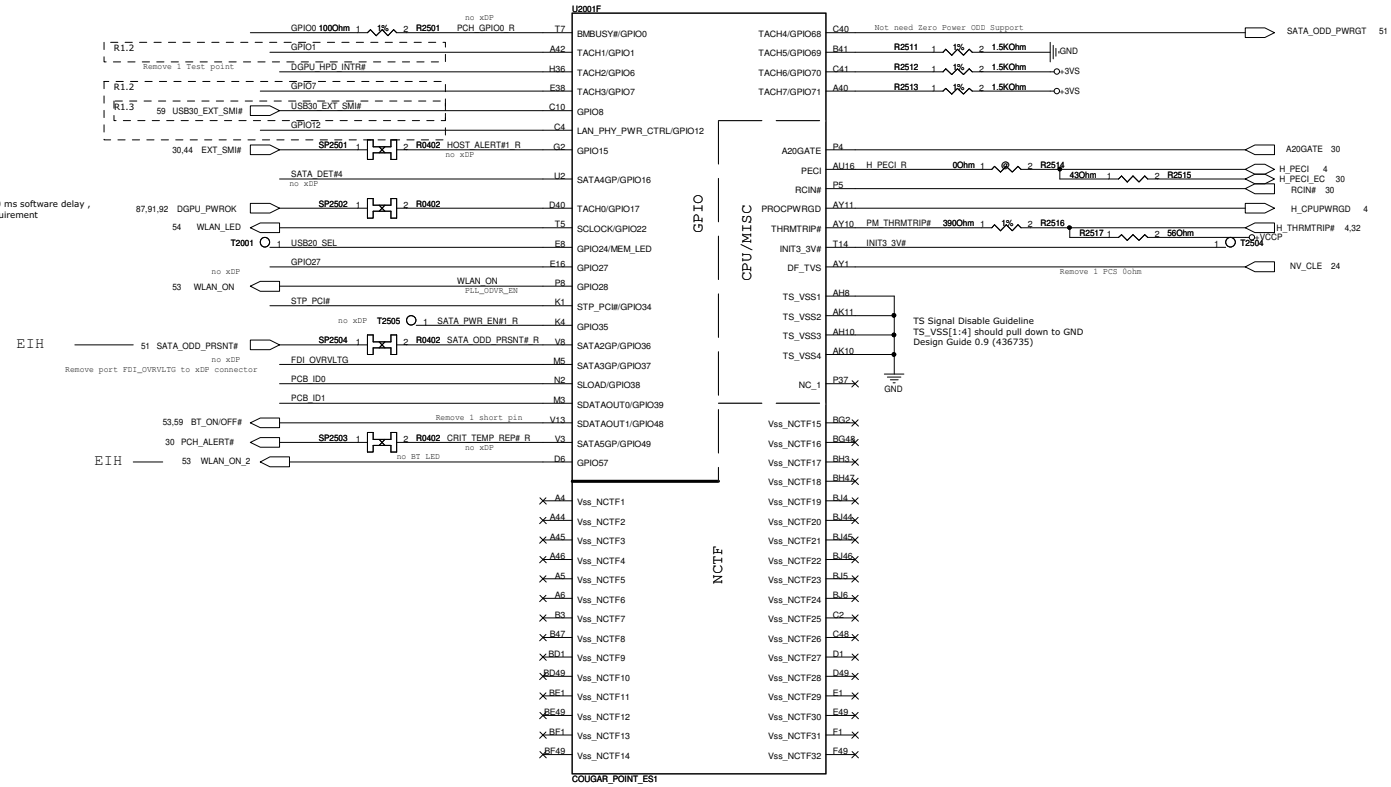
PEGATRON	Title : PCH(5)_PCI,NVRAM,USB	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, January 07, 2011	Sheet 24 of 99	

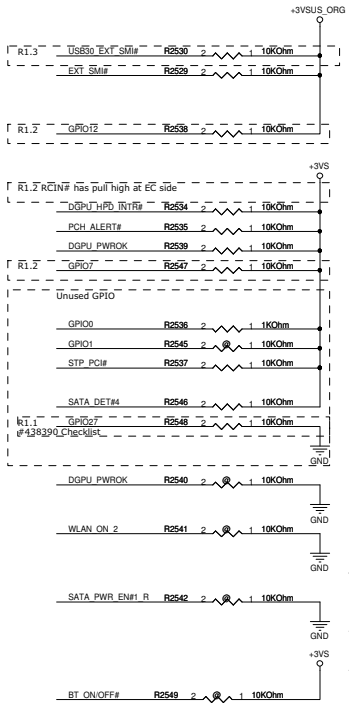
	PCB_ID1	PCB_ID0
SR	L	L
ER	L	H
PR	H	L
MP		

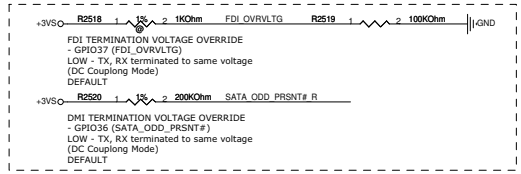


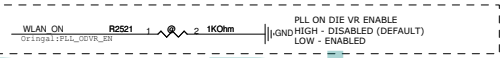


DGPU_PWROK has 100 ms software delay , no hardware delay requirement

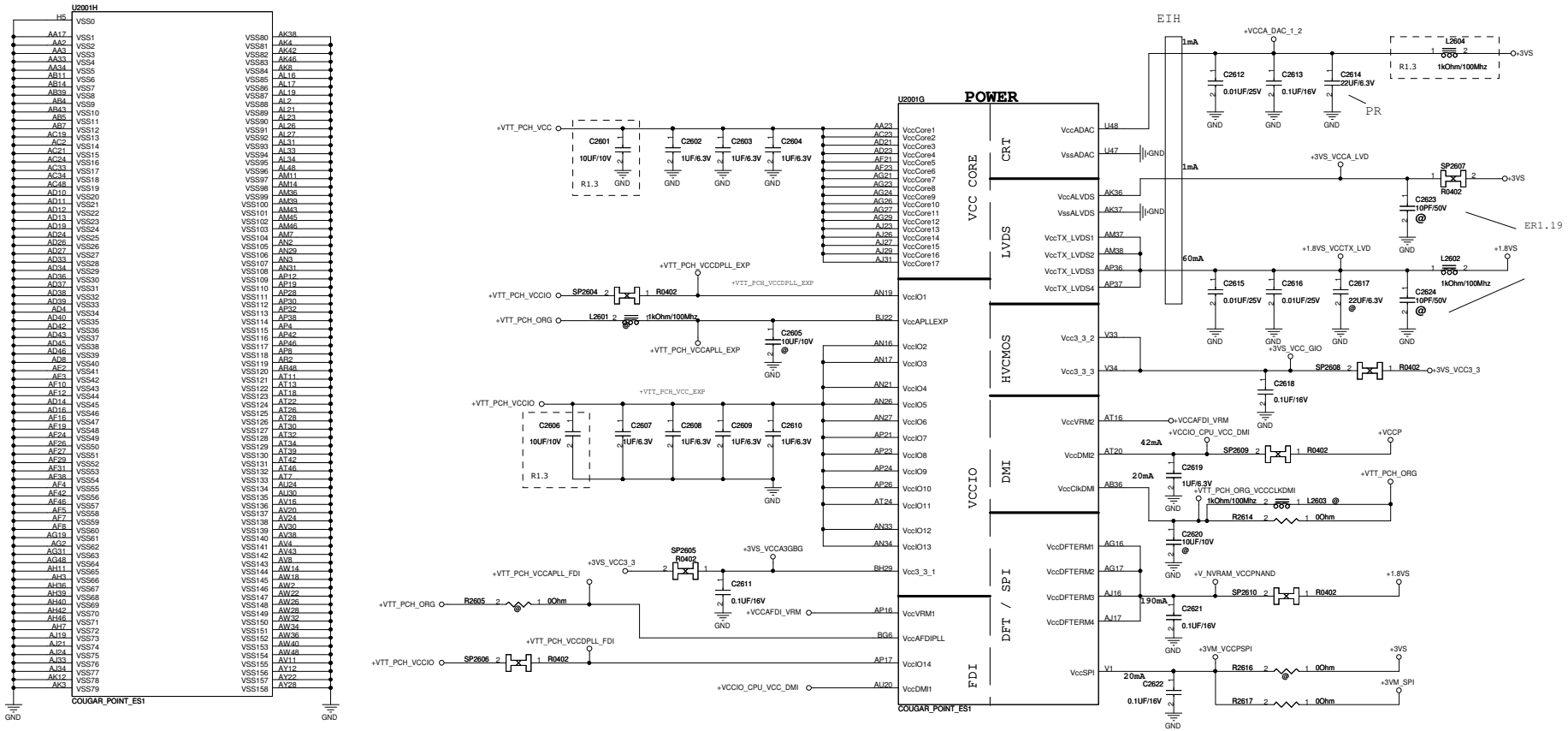


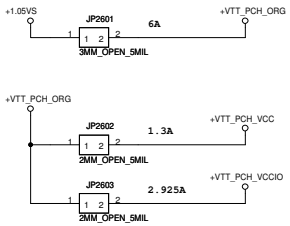


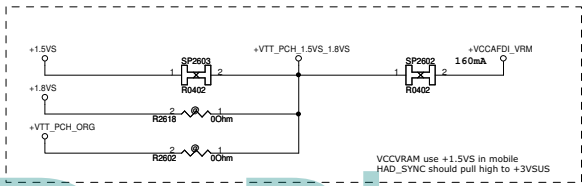


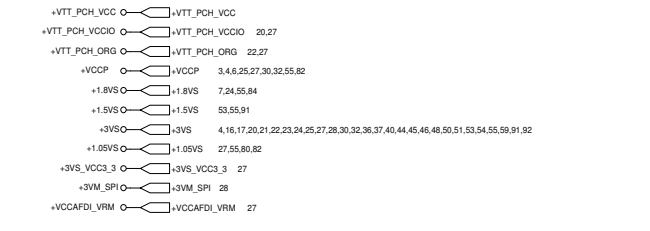


PEGATRON Title : PCH(6)_CPU,GPIO,MISC
Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.3
Date: Thursday, January 13, 2011 | Sheet 25 of 99

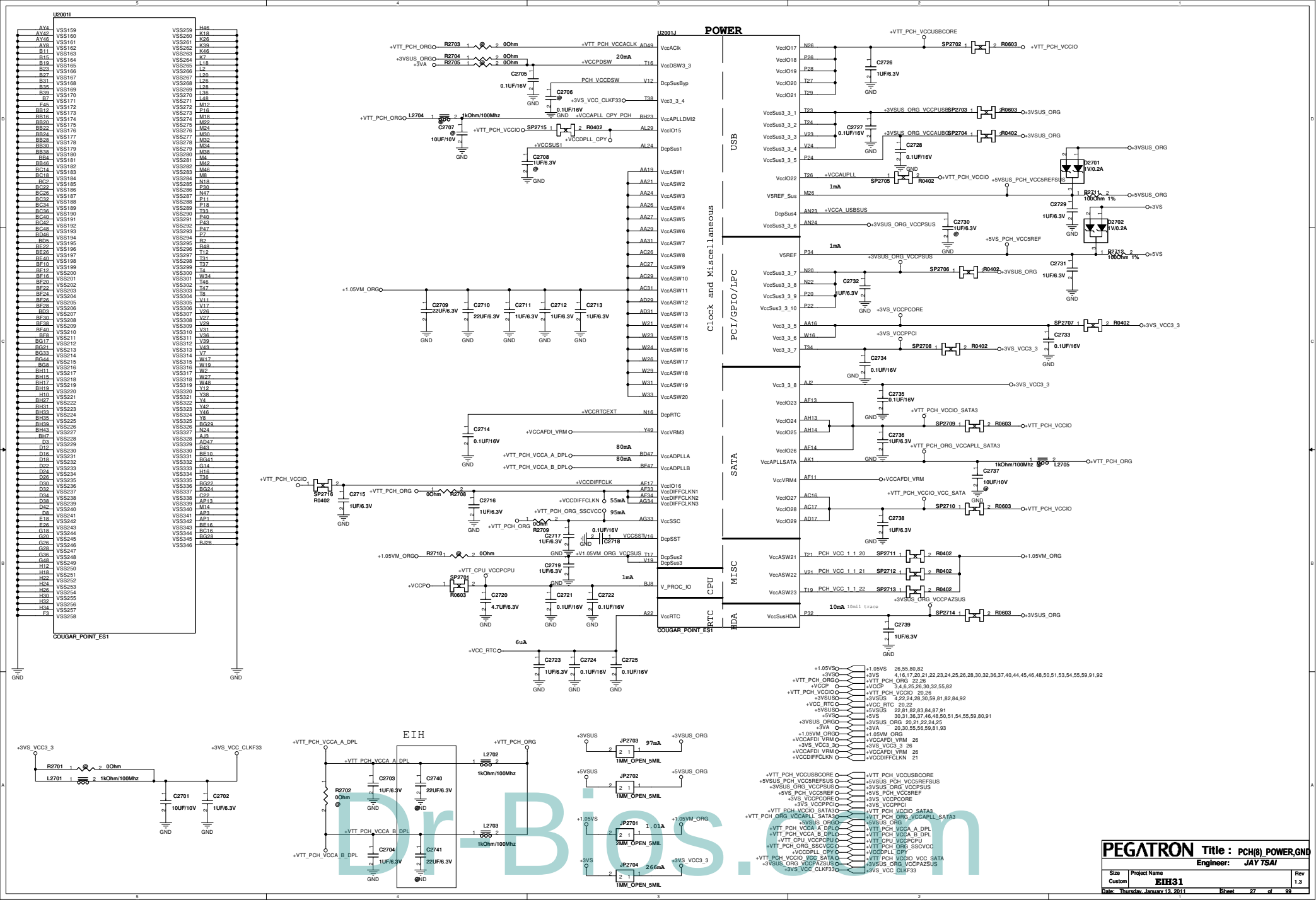




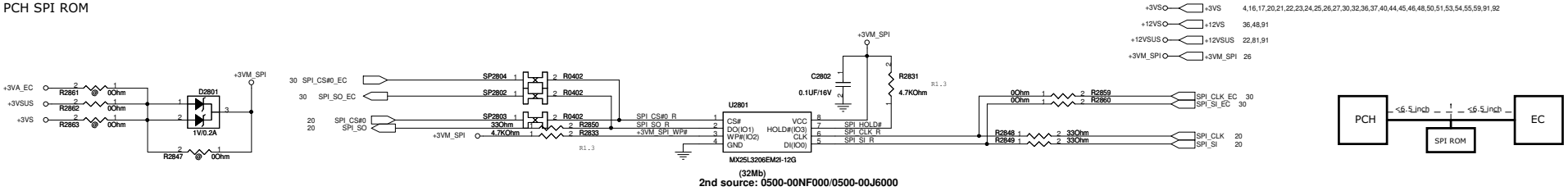




PEGATRON	Title : PCH(7)_POWER,GND		
	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 26 of 99		

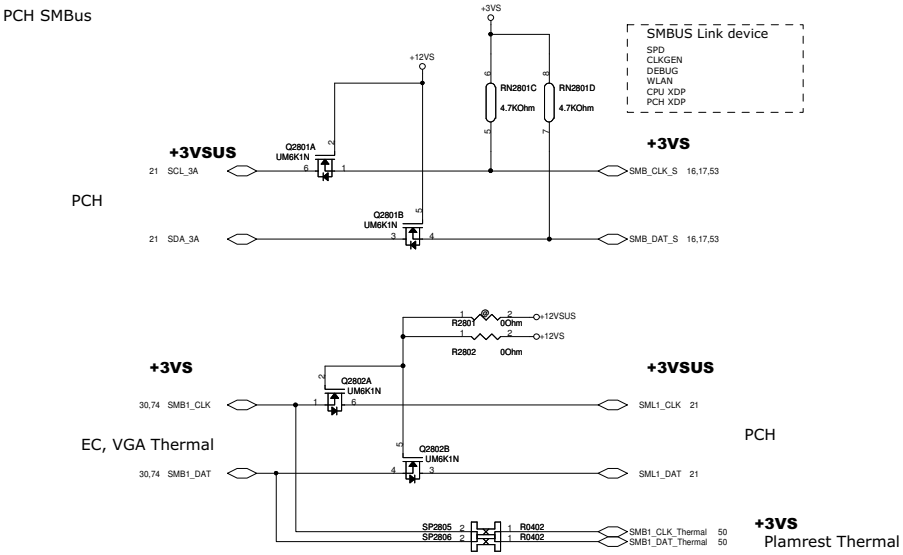

POWER
U2001I
COUGAR_POINT_ES1
U2001J
COUGAR_POINT_ES1
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
EIH
PEGATRON
Title : PCH(8)_POWER,GND
Engineer: JAY TSAI
Size: Custom
Project Name: EIH31
Rev: 1.3
Date: Thursday, January 13, 2011
Sheet 27 of 99
Dr-Bios.com

PCH SPI ROM



2nd source: 0500-00NF000/0500-00J6000

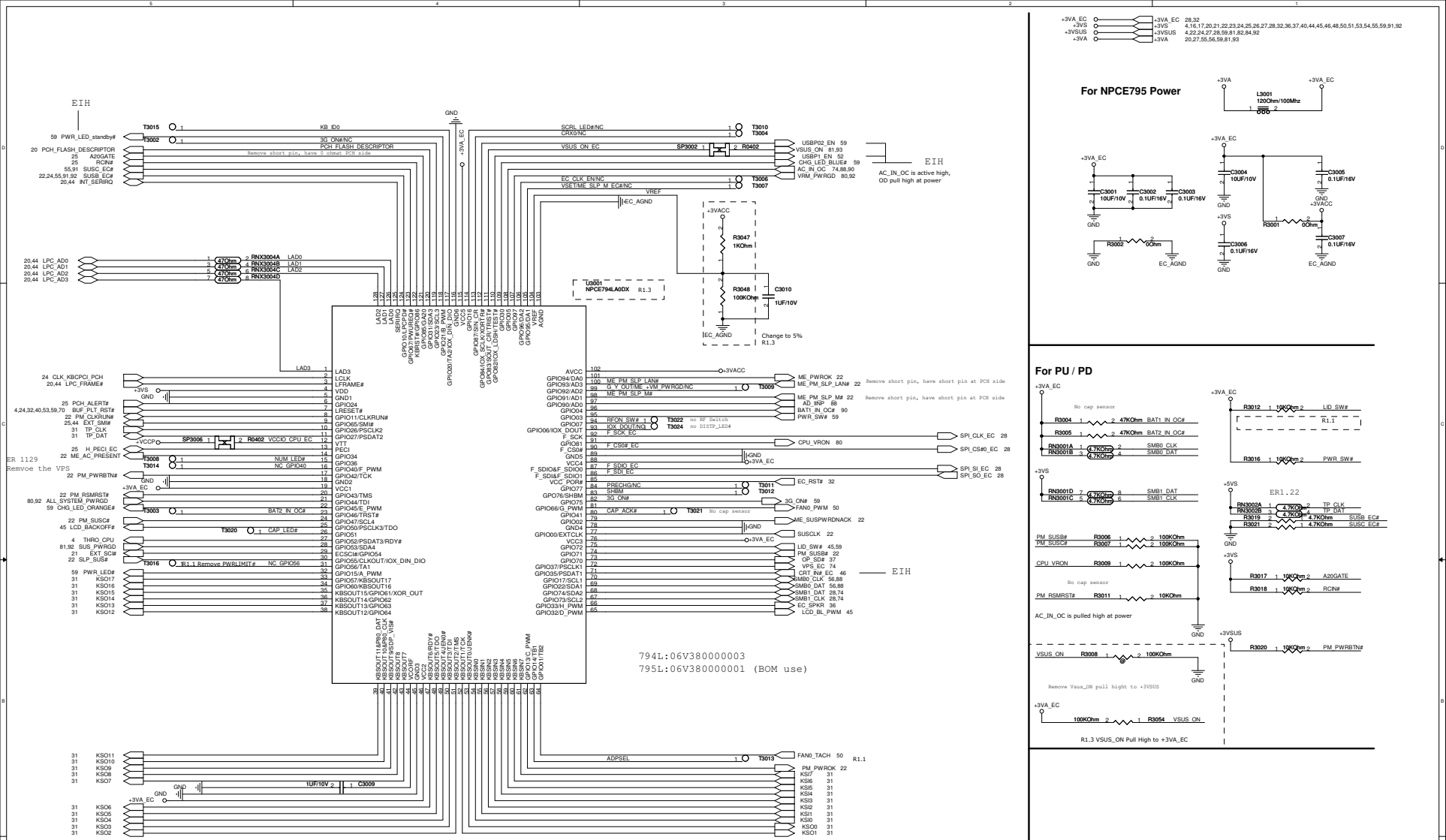
PCH SMBus



remove MOS & pull-hige resitor, because there is the function at page 74

PEGATRON	Title : PCH(9)_SPI,SMB	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, January 07, 2011	Sheet 28 of 99	

PEGATRON	Title : CLK_ICS9LRS3197	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 29 of 99	

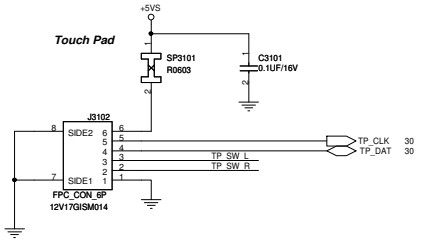


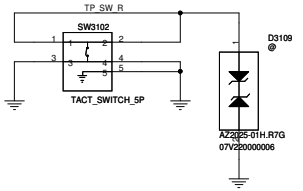
For NPCE795 Power

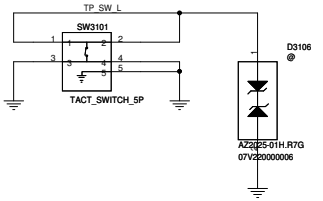
For PU / PD

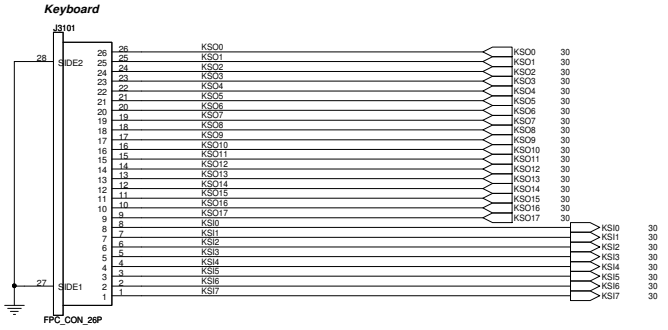
PEGATRON	Title : NPCE794L		
	Engineer: JAY TSAI		
Size: Custom	Project Name: EIH31		Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 30 of 99		

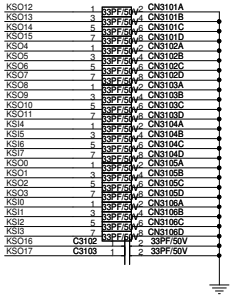
+5VSO +5VS 27,30,36,37,46,48,50,51,54,55,59,80,91











The pin define is checked to keyboard spec. R is KSO, C is KSI. The connector pin define is the same the KB.

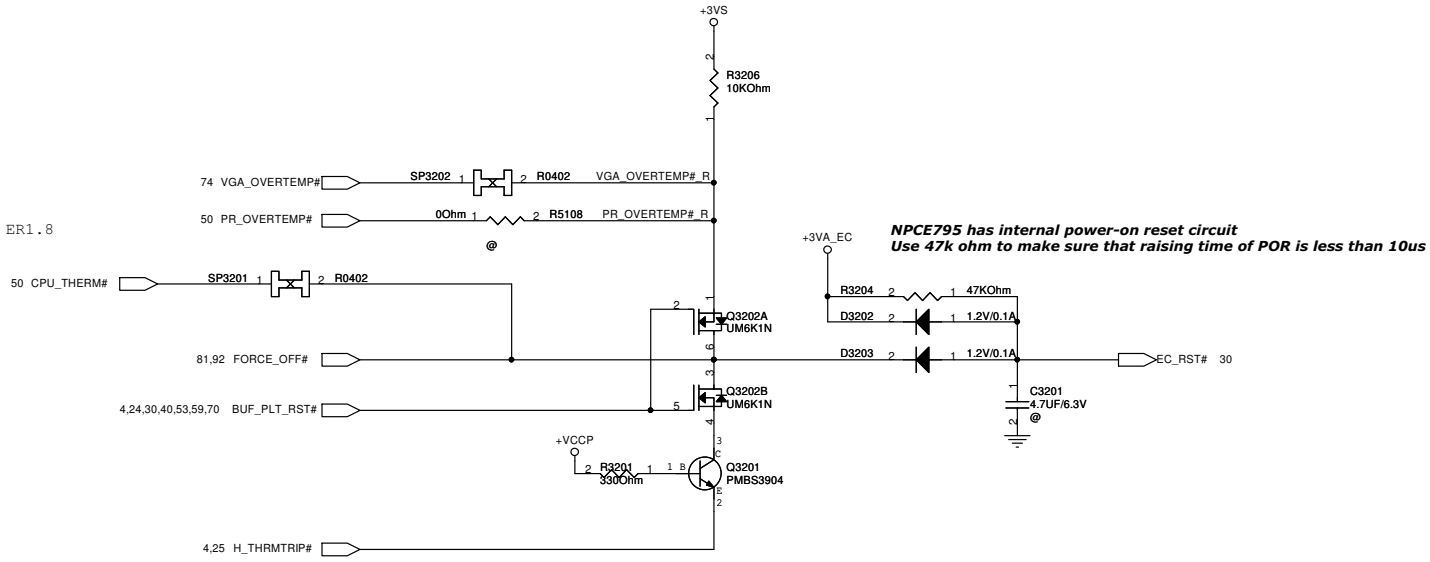
PEGATRON	Title : EC_IT8512(2)KB, TP,FP		
	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 31 of 99		

+VCCP +VCCP 3,4,6,25,26,27,30,55,82

+3VA_EC +3VA_EC 28,30

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92

Thermal Policy



PEGATRON	Title : RST_Reset Circuit	
<OrgName>	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Thursday, January 13, 2011	Sheet 32 of 99	

PEGATRON	Title : MDC CONN	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 35 of 99	

Audio Codec

DIGITAL

ANALOG

Intel 1.01 Design Guide update #440484
R1.3 use dual mosfet

+12VS
SP3603
R0402
UM6K1N
Q3604B
R3618 0Ohm
20 ACZ_SDOUT_AUD

+12VS
SP3604
R0402
UM6K1N
Q3604A
20 ACZ_SYNC_AUD
R3603 0Ohm
ACZ_SYNC_AUD_R
ACZ SDOUT AUD R

+5VS
+3VS
+5VS_AUDIO
+5VS 27,30,31,37,46,48,50,51,54,55,59,80,91
+3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+5VS_AUDIO 37

+5VS_AMP
+5VS
SP3606
R0805

H_SPKR+ 37
H_SPKR- 37
H_SPKL- 37
H_SPKL+ 37

+5VS_AMP
R3610 0Ohm
C3634 10UF/10V @
C3615 10UF/10V
C3609 0.1UF/16V
C3628 0.1UF/16V @

Short 0 ohm
+5VS_AMP
C3623 0.1UF/16V
C3620 10UF/10V
C3636 0.1UF/16V @
C3638 10UF/10V @

+5VS_AUDIO
C3608 0.1UF/16V
C3610 10UF/10V
GND_AUDIO

R3609 0Ohm @
R3608 0Ohm @
R3607 0Ohm @
R3604 0Ohm @
GND_AUDIO
add R3607&R3606&R3605 c3499 for EMI

+5VS
+5VS_AUDIO
L3603 >30 mil or shape
80Ohm/100Mhz
vx_l0805_h43_small
Irat=2A

37 EAPD
C3639 10UF/10V @
T3602

ER 1.8
SPDIF OUT

+3VS
+3VS_DVDD
L3602
120Ohm/100Mhz
C3616 10UF/10V
C3617 0.1UF/16V @
C3618 0.1UF/16V

U3601A
GND
SPDIFO
AVDD1
PVDD2
SPK-OUT-R+
SPK-OUT-R-
PVSS2
PVSS1
SPK-OUT-L-
SPK-OUT-L+
PVDD1
AVDD2
AVSS2

T3603
T3604
37 MUTE_AMP#
20 ACZ_BCLK_AUD
20 ACZ_SDIN0_AUD
20,37 ACZ_RST#_AUD
ACZ_SDOUT_AUD_R
ACZ_BCLK_AUD
R3625 33Ohm
ACZ_SYNC_AUD_R
PC_BEEP

DVDD
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
PD#
SDATA-OUT
BCLK
DVSS2
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP

CBP
CBN
CPVEE
HPOUT-R(PORT-I-R)
HPOUT-L(PORT-I-L)
MIC1-VREFO-L
MIC1-VREFO-R
MIC2-VREFO
LDO-CAP
VREF
AVSS1
AVDD1

C3626 2.2UF/10V
C3627 2.2UF/10V
GND_AUDIO
AC_HP_R 37
AC_HP_L 37
MIC1_VREFO 37
MIC_VREFO 37
MIC2_VREFO 37
AUD_LDO_CAP
VREF_CODEC
+5VS_AUDIO
C3614 0.1UF/16V
C3632 10UF/10V
C3613 0.1UF/16V
C3611 2.2UF/10V
GND_AUDIO

+3VS
C3633 0.1UF/16V
Check R3625 resistor value
ACZ_BCLK_AUD
C3629 22PF/50V

ALC271X-VB3-GR
02V0J0000004

SenseA
LINE2-R(PORT-E-R)
LINE2-L(PORT-E-L)
MIC2-L(PORT-F-L)
MIC2-R(PORT-F-R)
VREF
MONO_OUT
MIC1-L(PORT-B-L)
MIC1-R(PORT-B-R)
LINE1-L(PORT-C-L)
LINE1-R(PORT-C-R)

ER 1129
Change the PART & SYMBOL (8VIA)

HeadPhone Out
EXT MIC Vref.
EXT MIC Vref.
COMBO MIC Vref.
INT MIC Vref.

MIC1_VREFO
MIC_VREFO
MIC2_VREFO
AUD_LDO_CAP
C3612 10UF/10V
C3624 10UF/10V @
C3619 10UF/10V @
C3625 10UF/10V @
GND_AUDIO

HP Jack Detect
EXT MIC Detect
37 HPOUT_JD#
37 MIC1_JD#
R3619 1% 39.2KOhm
R3613 1% 20KOhm

INT MIC IN
AUD_LDO_CAP
R3628 4.7KOhm
52 INT_MIC_AC_IN
R3629 1KOhm
1UF/10V C3630 INT_MIC_AC_IN_L
1UF/10V C3631 INT_MIC_AC_IN_R

C3635 2.2UF/10V
EXT_MIC_AC_IN_R
EXT_MIC_AC_IN_L
C3637 2.2UF/10V
R3630 1KOhm
R3631 1KOhm
EXT_MIC_R 37
EXT_MIC_L 37

EXT MIC IN

37 MIC2_L
37 MIC2_R
37 MIC2_JD#
R3620 1% 20KOhm
R3616 20KOhm 1%
GND_AUDIO

R3605 0Ohm
D3601
20 SB_SPKR
30 EC_SPKR
1V/0.2A
R3614 47KOhm
R3615 4.7KOhm
R3611 @ 0Ohm
PC_BEEP_C
C3622 0.1UF/16V
C3621 100PF/50V @
PC_BEEP

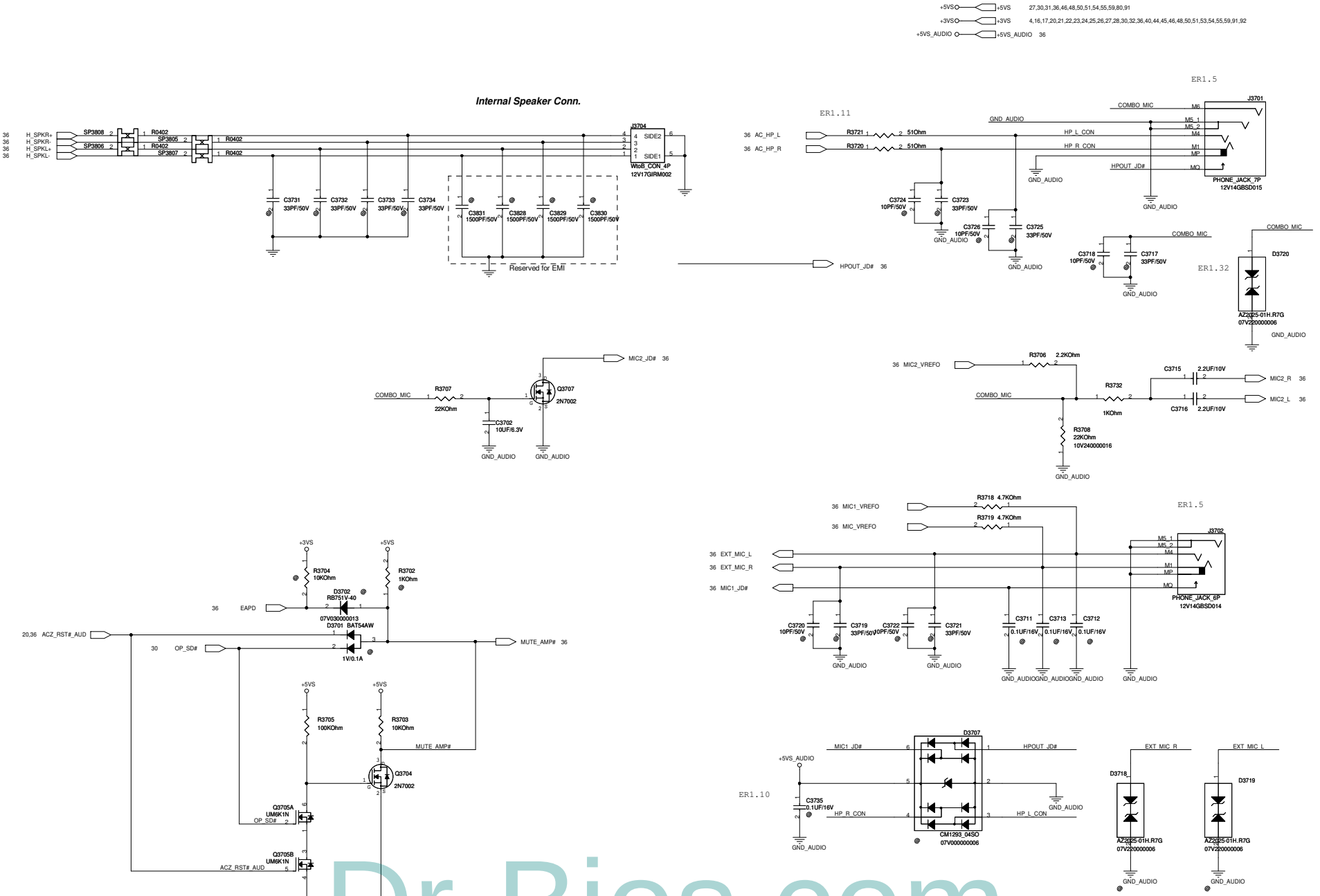
ER1.2

U3601B
GND1 GND8
GND2 GND7
GND3 GND6
GND4 GND5
ALC271X-VB3-GR
02V0J0000004

ER 1129
Change the PART & SYMBOL (8VIA)

R3606 0Ohm
R3626 0Ohm @
GND_AUDIO
R3602 0Ohm
R3627 0Ohm @
GND_AUDIO

PEGATRON Title : AUD(1)_ALC269
<OrgName> Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.1
Date: Thursday, January 13, 2011 | Sheet 36 of 99

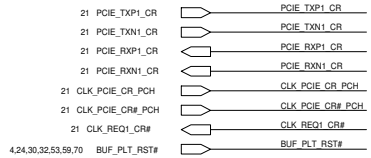


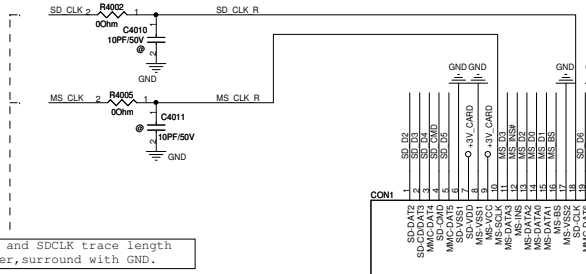
PEGATRON	Title : AUD(2)_AMP,JACK		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 37 of 99		

PEGATRON	Title : AUD(3)_FM2010	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 38 of 99	

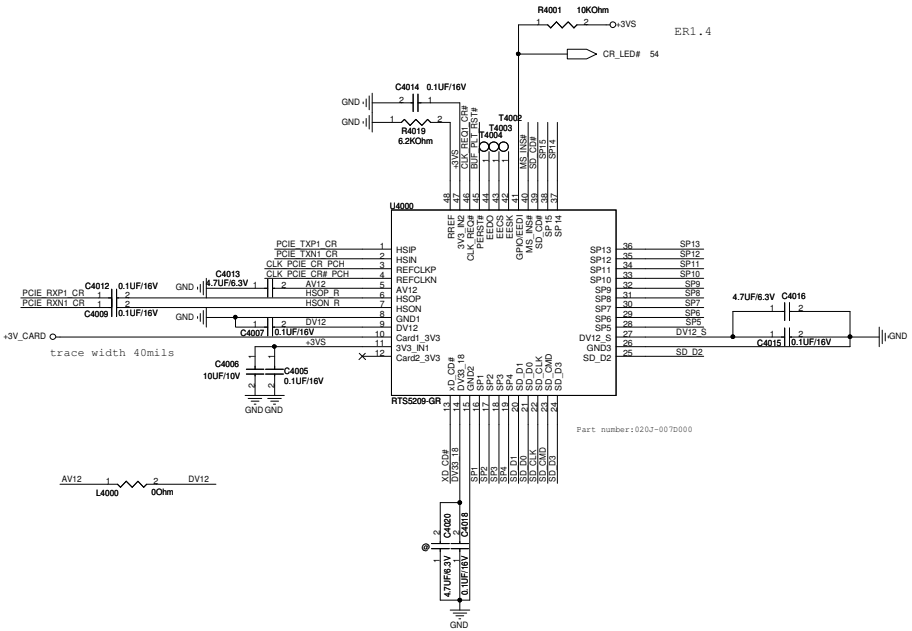
PEGATRON	Title : AUD(4)_****	
<OrgName>	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 39 of 99	

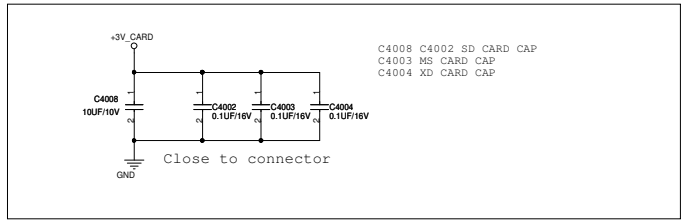
From System's PCIE interface





MSCLK and SDCLK trace length shorter,surround with GND.





Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

Share Pin

Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

PEGATRON Title : RTS5209

<OrgName> Engineer:

Size	Project Name	Rev
C	EIH31	0.1

Date: Thursday, January 13, 2011 Sheet 40 of 99

PEGATRON	Title : CB(2)_R5C833	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 41 of 99	

4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92

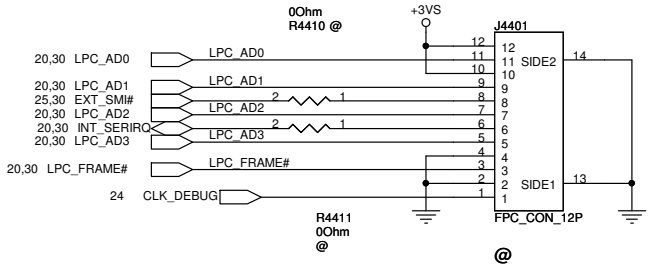
91

PEGATRON	Title : CB(3)_4in1 CardReader	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, January 07, 2011	Sheet 42 of 99	

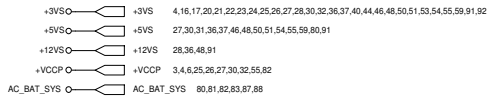
PEGATRON	Title : CB(4)_NewCard	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 43 of 99	

+3VSO +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,45,46,48,50,51,53,54,55,59,91,92

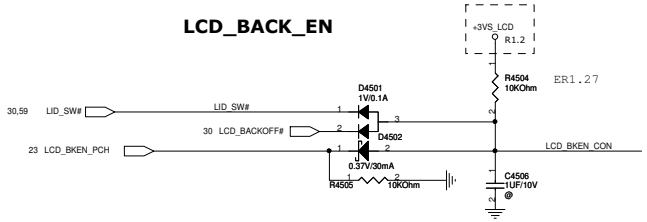
LPC Debug Port



PEGATRON	Title : BUG_Debug	
<OrgName>	Engineer: JAY TSAI	
Size: B	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 44 of 99	

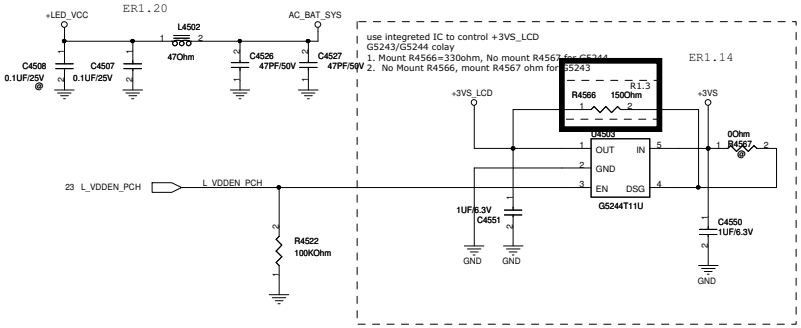


LCD_BACK_EN

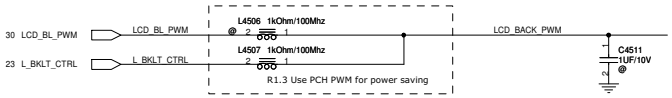


Remove MOS solution.

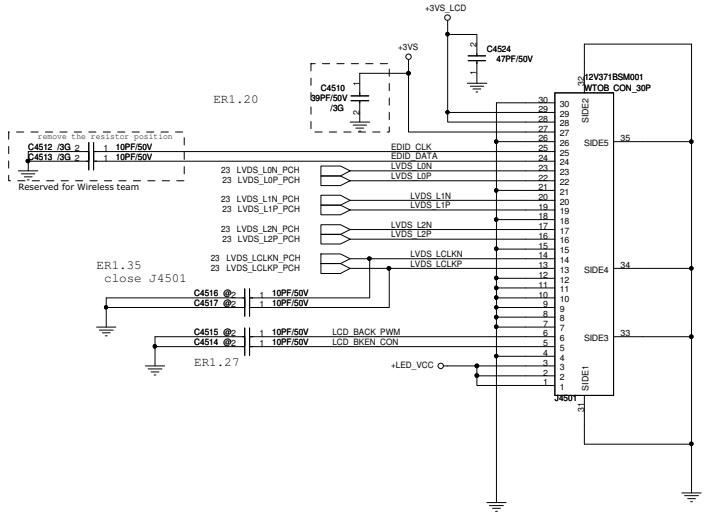
LCD VDDEN / +LED_VCC



LCD_BL_PWM

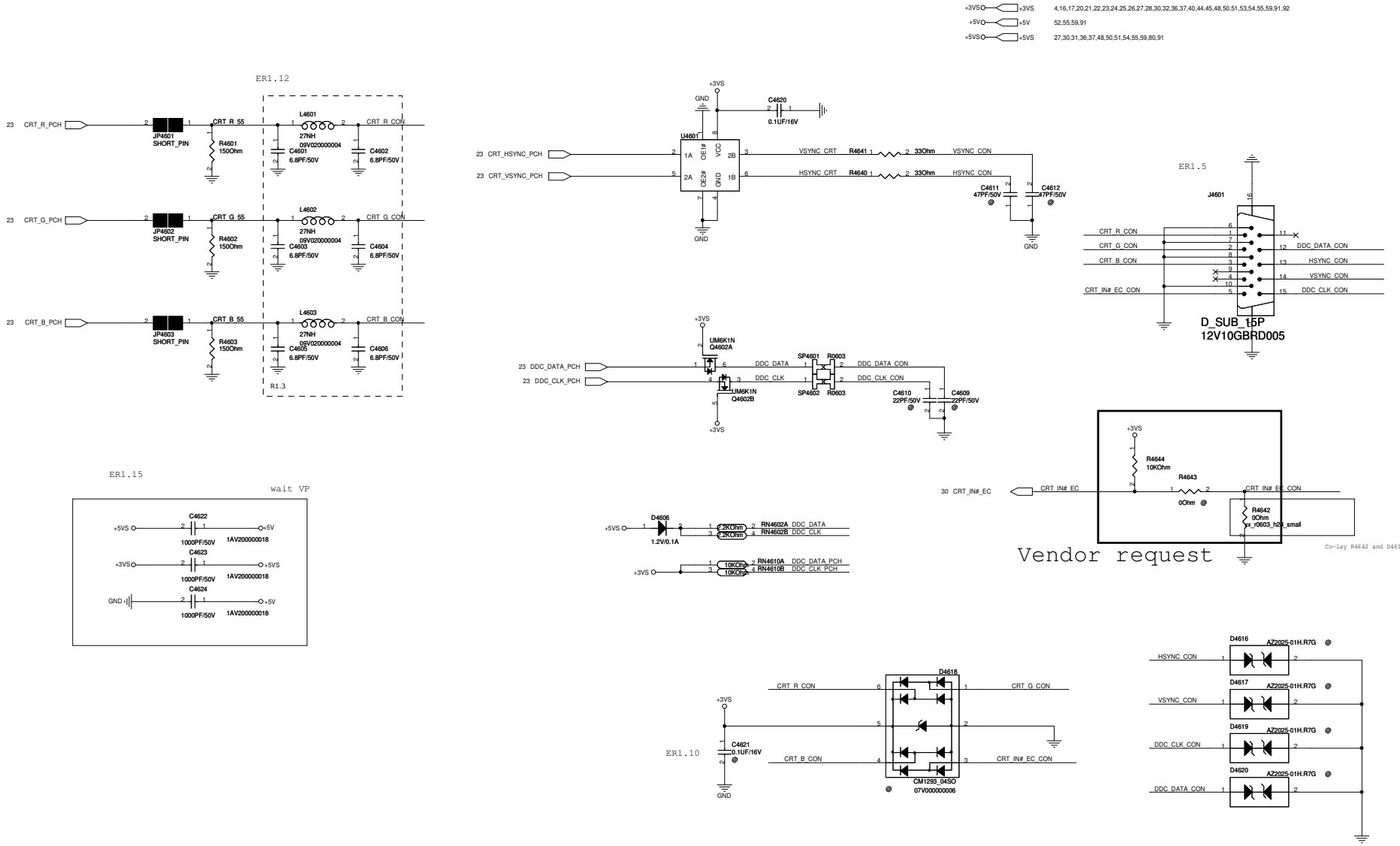


LVDS Connector



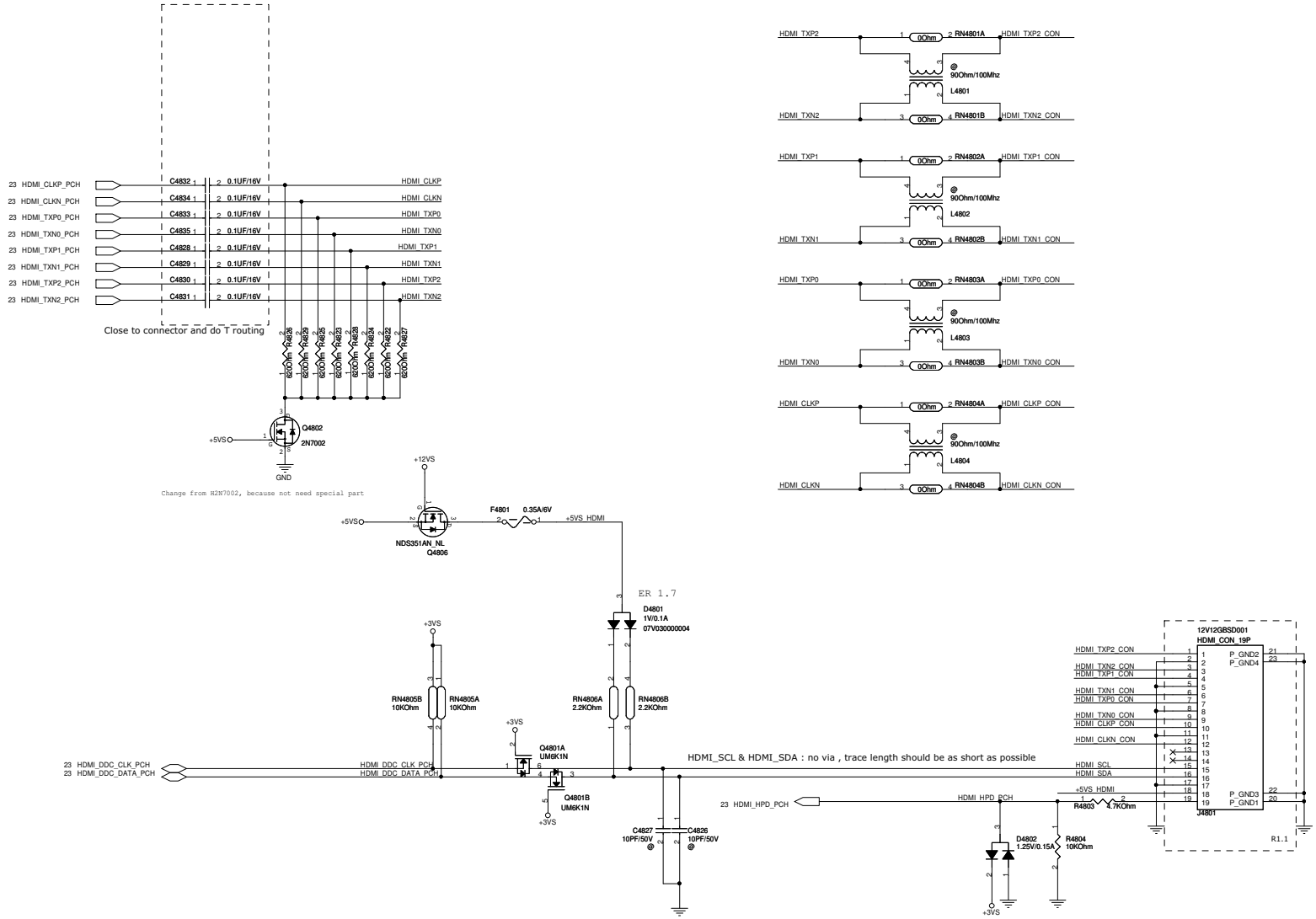
EDID Switch

PEGATRON	Title : CRT(1)_LVDS		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 45 of 99		



PEGATRON	Title : CRT(2)_D-Sub		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 46 of 99		

PEGATRON	Title : CRT(3)_Display Port	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 47 of 99	



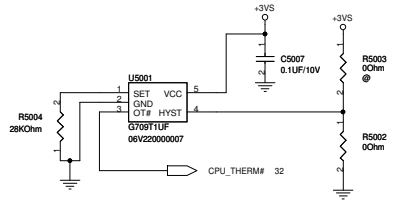
PEGATRON	Title : TV(1)_HDMI	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, January 07, 2011	Sheet 48 of 99	

PEGATRON	Title : TV(2)_****	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 49 of 99	

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,51,53,54,55,59,91,92

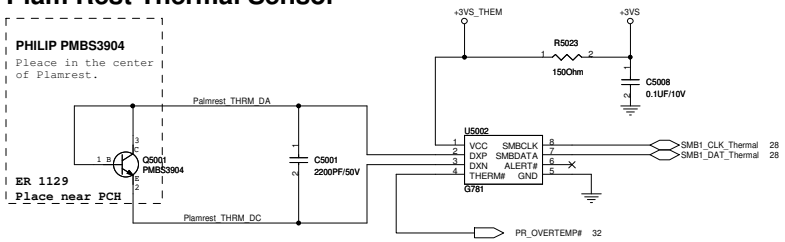
+5VS +5VS 27,30,31,36,37,46,48,51,54,55,59,80,91

CPU Thermal Sensor



(10°C for HYST =VCC)
(2°C for HYST = GND)
Hysteresis prevents the output from oscillating when the temperature is near the trip point.

Plam Rest Thermal Sensor

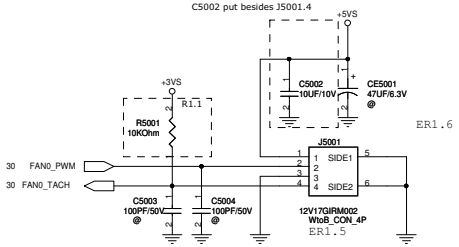


U5002 under palmrest

SMBUS addr=1001100x (98)

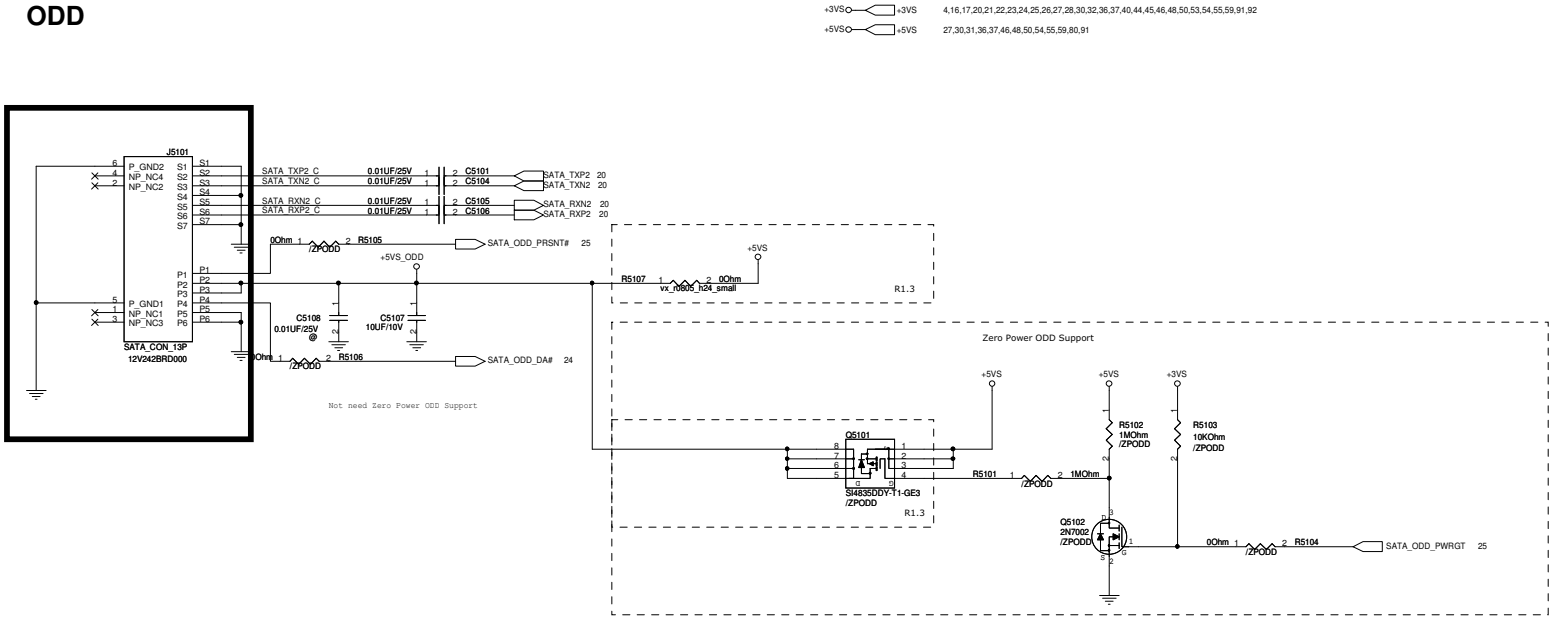
U5002: Remote(Local) thermal sensor,use remote mode.

PWM Fan

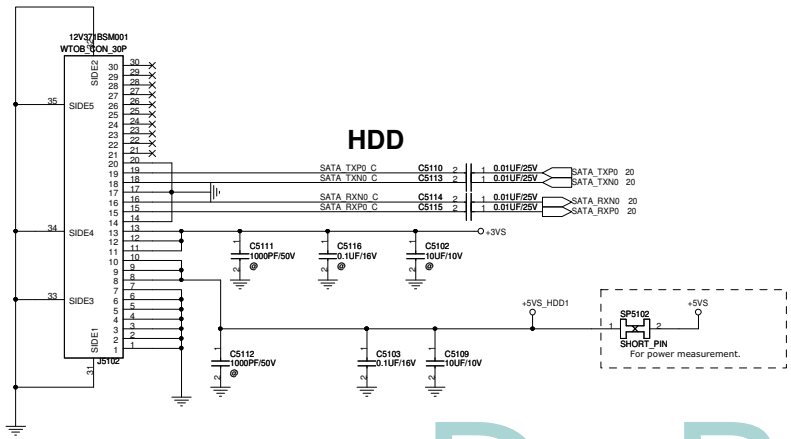


PEGATRON	Title : FAN_Fan,Sensor	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 2.0
Date: Thursday, January 13, 2011	Sheet 50 of 99	

ODD

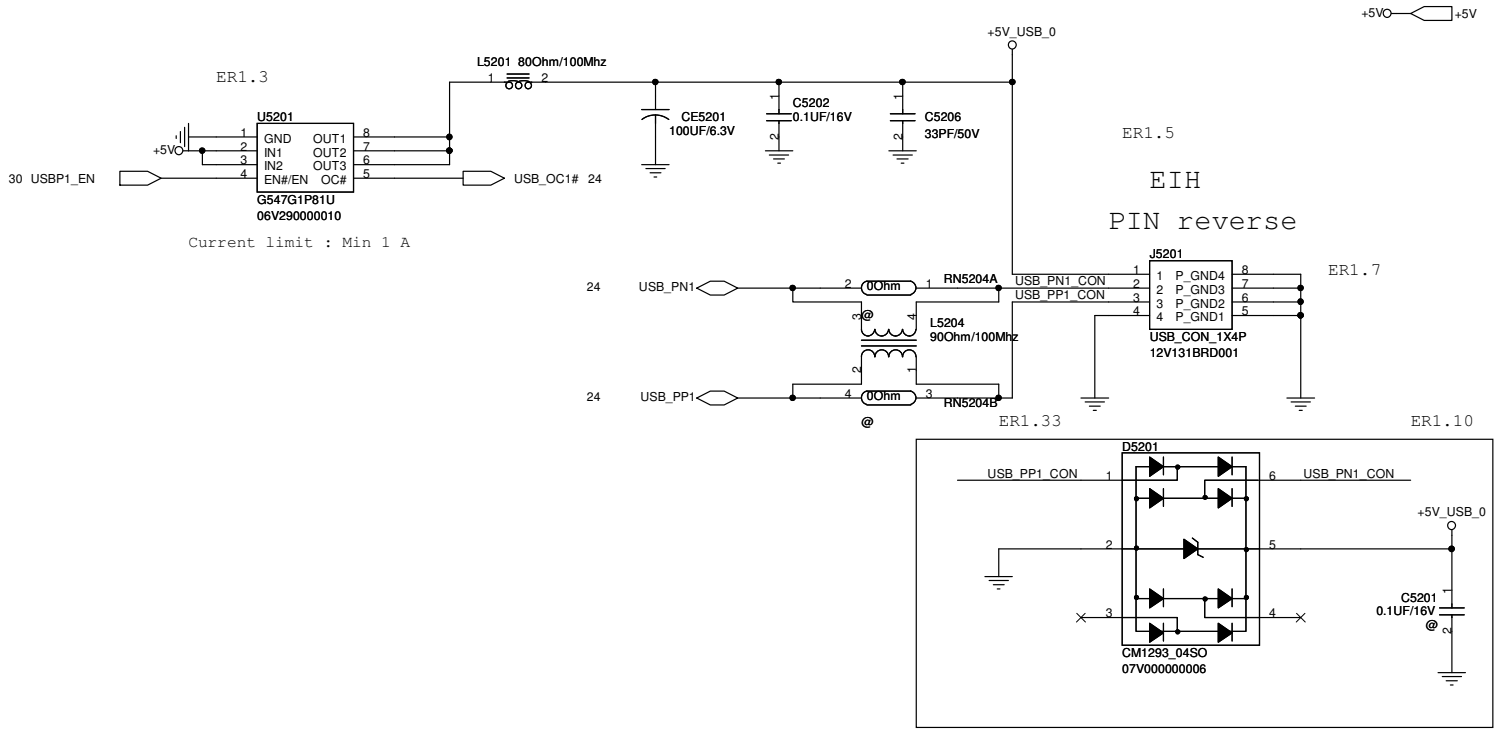


HDD

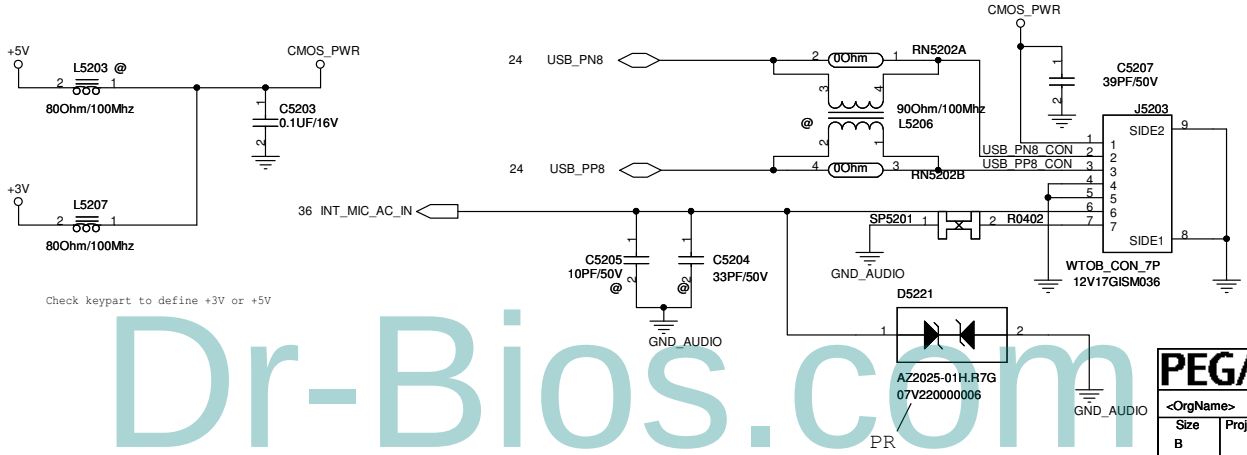


PEGATRON	Title : XDD_HDD,ODD		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Friday, January 07, 2011	Sheet 51 of 99		

USB ports



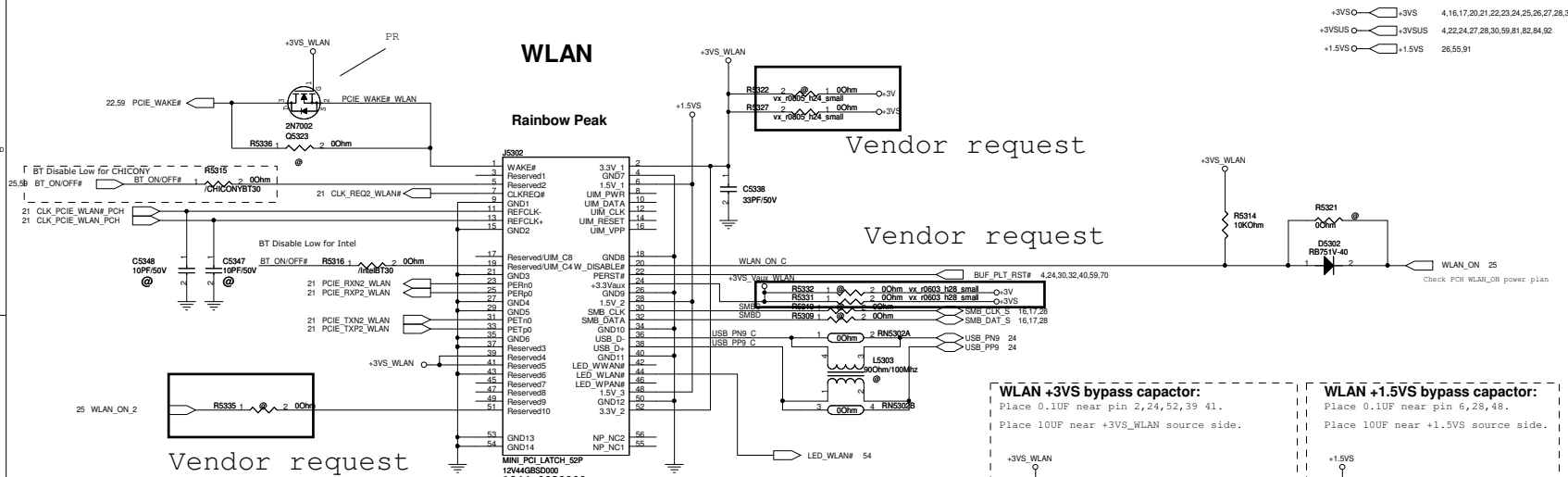
Camera



PEGATRON	Title : USB_USB Port	
<OrgName>	Engineer: JAY TSAI	
Size: B	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 52 of 99	

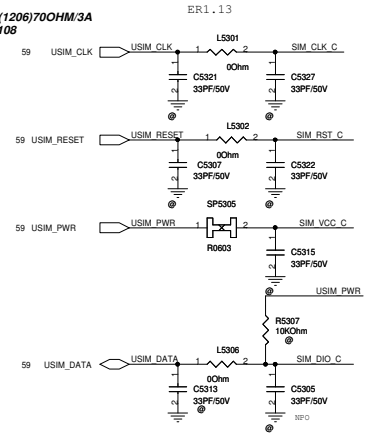
WLAN

Rainbow Peak

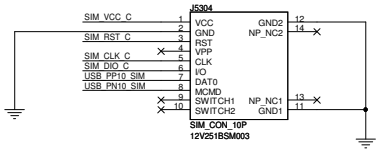


Remove Bead
Option :
BEAD SMD(1206)70OHM/3A
09G010070108

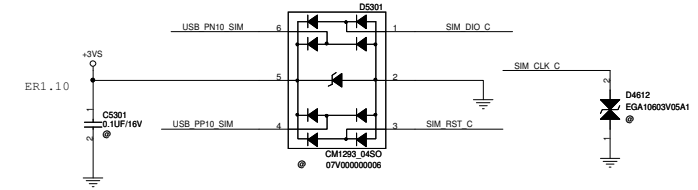
ER1.13

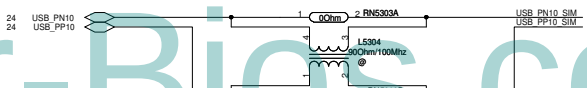


ER1.5

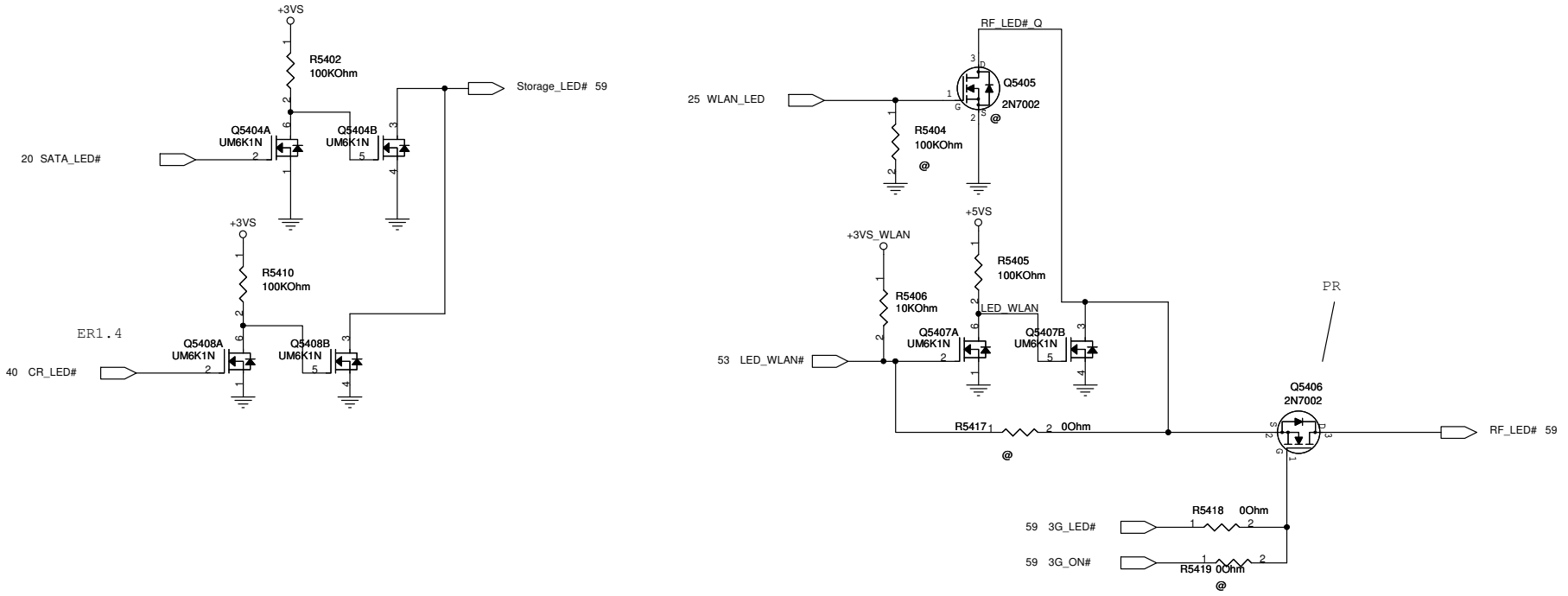


ER1.10



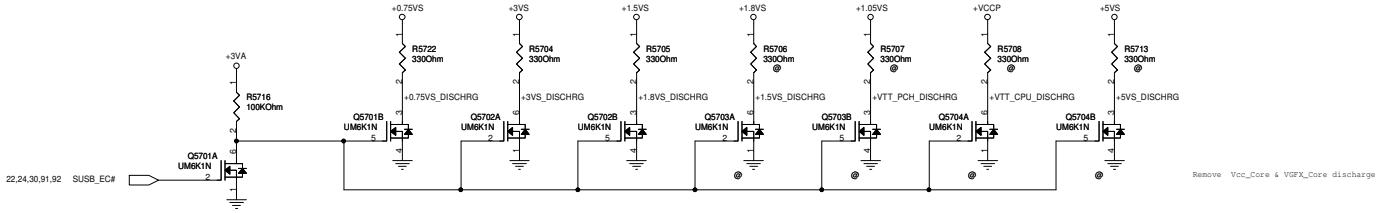


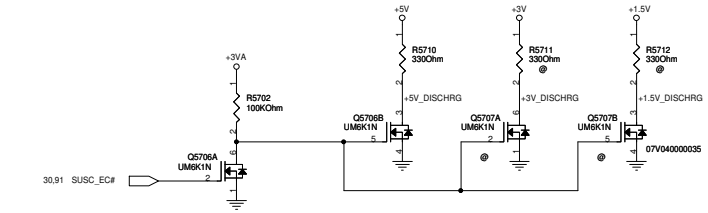
PEGATRON	Title : WLAN/ 3G	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 53 of 99	



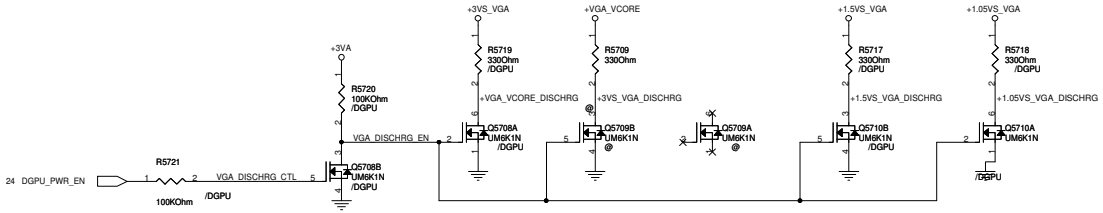
PEGATRON	Title : USB3.0	
<OrgName>	Engineer: JAY TSAI	
Size: B	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 54 of 99	

+3VA +3VA 20,27,30,56,59,81,93
+VCC_CORE +VCC_CORE 6,80
+VGFX_CORE +VGFX_CORE 7,80
+VCCP +VCCP 3,4,6,25,26,27,30,32,82
+0.75VS +0.75VS 16,17,83
+1.05VS +1.05VS 26,27,80,82
+1.5VS +1.5VS 26,53,91
+1.8VS +1.8VS 7,24,26,84
+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,59,91,92
+5VS +5VS 27,30,31,36,37,46,48,50,51,54,59,80,91
+1.5V +1.5V 5,7,16,83
+3V +3V 4,24,52,53,59,91
+5V +5V 46,52,59,91
+VGA_VCORE +VGA_VCORE 75,87
+3VS_VGA +3VS_VGA 70,72,74,91
+1.5VS_VGA +1.5VS_VGA 71,76,91
+1.05VS_VGA +1.05VS_VGA 70,71,72,91





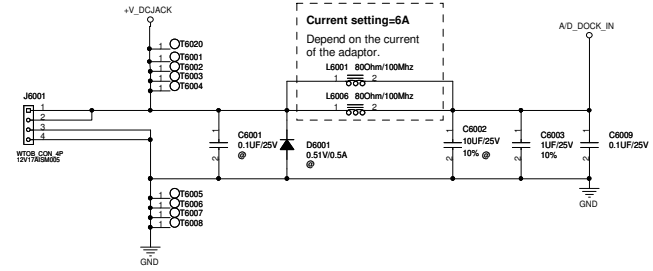
R1.1



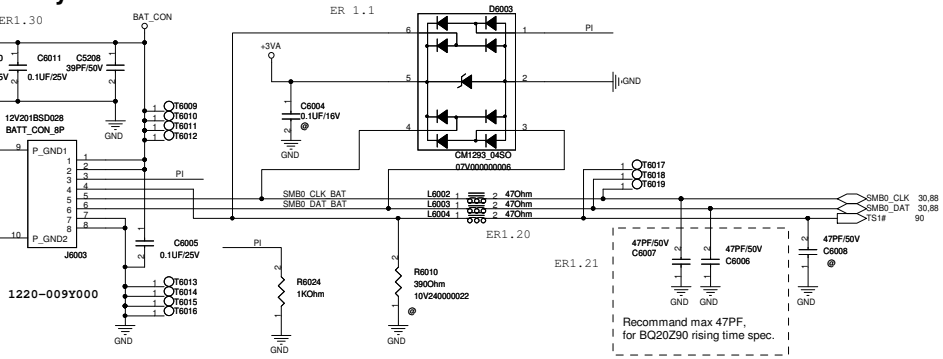
Unmount +VGA_Vcore discharg

PEGATRON Title : DSG_Discharge
<OrgName> Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.3
Date: Thursday, January 13, 2011 Sheet 55 of 99

DC Jack WtoB CONN



Battery Connector



+VCC_RTC — +VCC_RTC 20,22,27
+3VA_EC — +3VA_EC 28,30,32
+3VA — +3VA 20,27,30,55,59,81,93
+5VA — +5VA 59,81,88

+3VSUS — +3VSUS 4,22,24,27,28,30,59,81,82,84,92
+5VSUS — +5VSUS 22,27,81,82,83,84,87,91
+12VSUS — +12VSUS 22,28,81,91

+1.5V — +1.5V 5,7,16,55,83
+3V — +3V 4,24,52,53,55,59,91
+5V — +5V 46,52,55,59,91
+12V — +12V 91

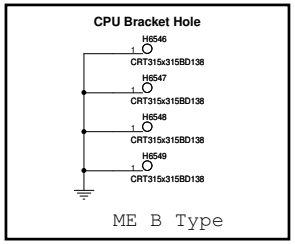
+0.75VS — +0.75VS 16,17,55,83
+1.05VS — +1.05VS 26,27,55,80,82
+1.5VS — +1.5VS 26,53,55,91
+1.8VS — +1.8VS 7,24,26,55,84
+3VS — +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+5VS — +5VS 27,30,31,36,37,46,48,50,51,54,55,59,80,91
+12VS — +12VS 28,36,48,91

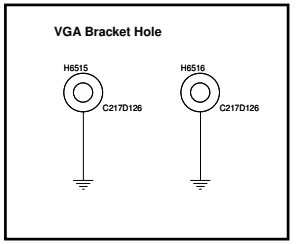
AC_BAT_SYS — AC_BAT_SYS 45,80,81,82,83,87,88
A/D_DOCK_IN — A/D_DOCK_IN 88
BAT_CON — BAT_CON 88

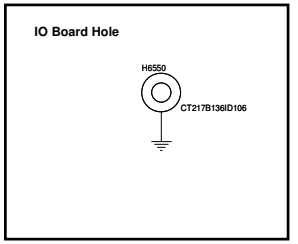
+1.5V_DDR3 — +1.5V_DDR3 16,17,18
+VCCP — +VCCP 3,4,6,25,26,27,30,32,55,82
+VCC_CORE — +VCC_CORE 6,80
+VGFX_CORE — +VGFX_CORE 7,80
+VTT_PCH_ORG — +VTT_PCH_ORG 22,26,27
+VTT_PCH_VCCIO — +VTT_PCH_VCCIO 20,26,27
+1.05VM_ORG — +1.05VM_ORG 27

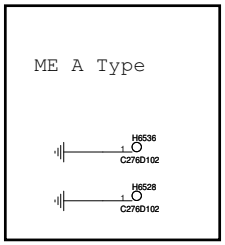
+V_VREF — +V_VREF
+V_VREF_DDR3 — +V_VREF_DDR3 7,16,17,18,83
+V_SM_VREF — +V_SM_VREF

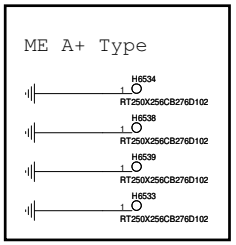
PEGATRON	Title : DC_DC/BAT CONN		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 56 of 99		

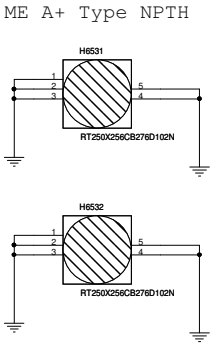


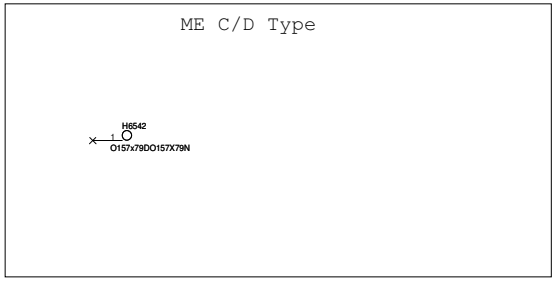


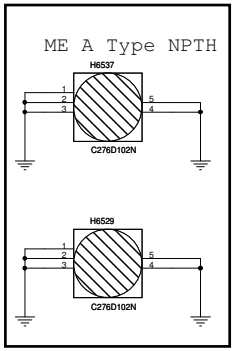


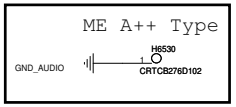












PEGATRON Title : ME_CONN,Skew Hole

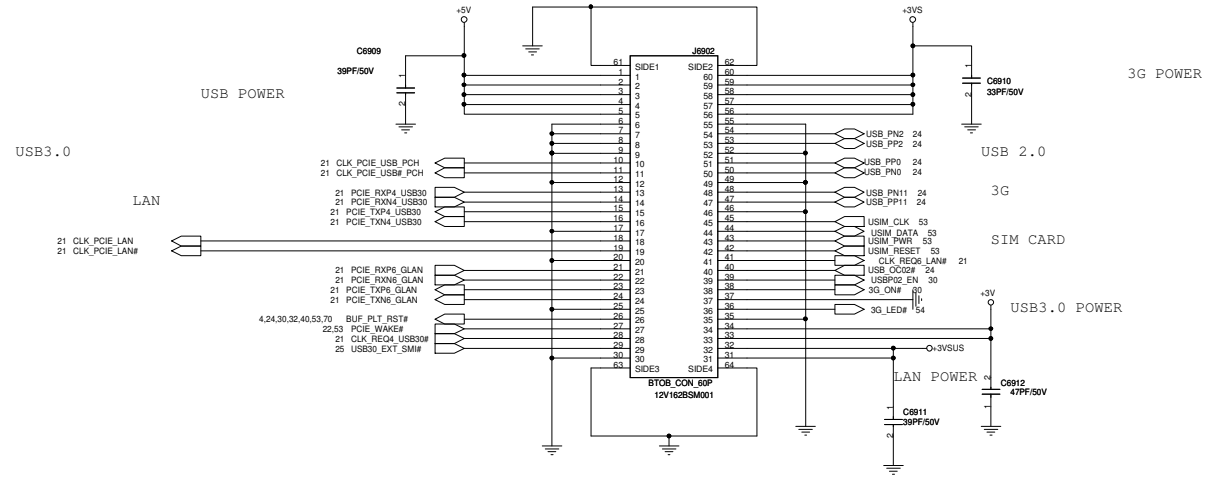
<OrgName> Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

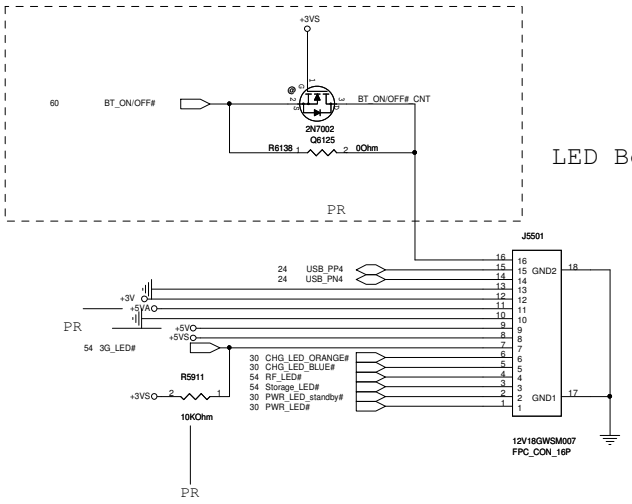
Date: Thursday, January 13, 2011 Sheet 57 of 99

PEGATRON	Title : System Setting	
<OrgName>	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 06, 2011	Sheet 58 of 99	

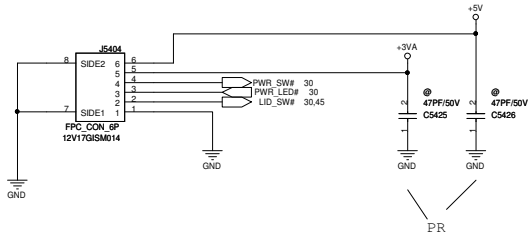
USB IO Board CNT



LED Board CNT



POWER Board CNT



PEGATRON Title : B to B

<OrgName> Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

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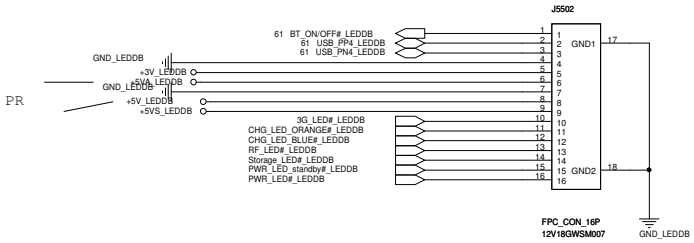
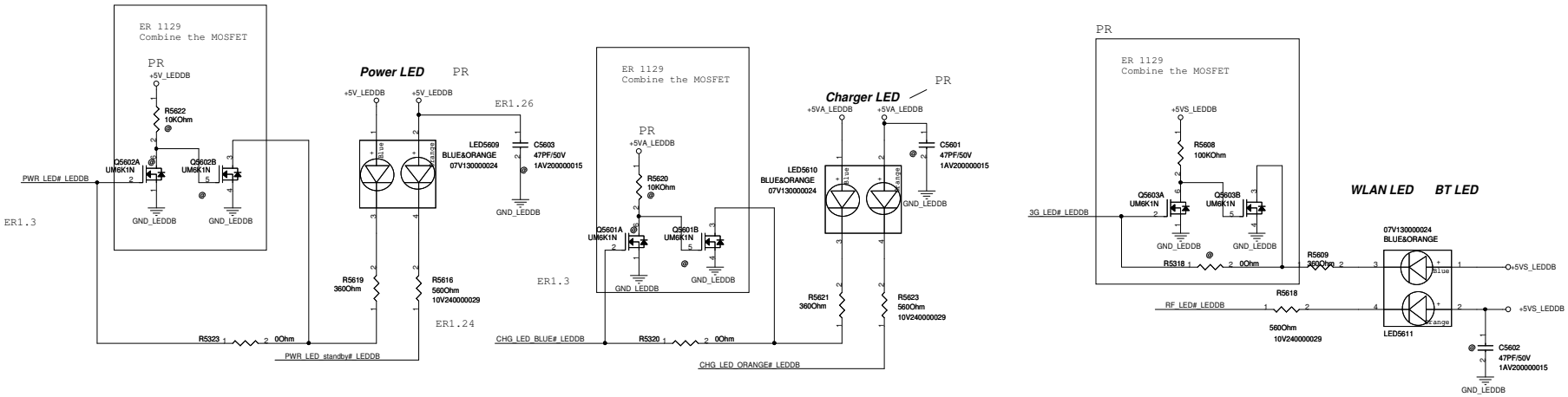
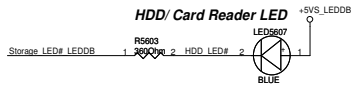
+3VA	+3VA	20,27,30,55,56,59,81,93
+3VS	+3VS	4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,59,91,92
+5VSUS	+5VSUS	22,27,81,82,83,84,87,91
+5VA	+5VA	59,81,88
+5V	+5V	46,52,55,59,91
+5VS	+5VS	27,30,31,36,37,46,48,50,51,54,55,59,80,91
AC_BAT_SYS	AC_BAT_SYS	45,80,81,82,83,87,88
+3V	+3V	4,24,52,53,55,59,91

LED DB

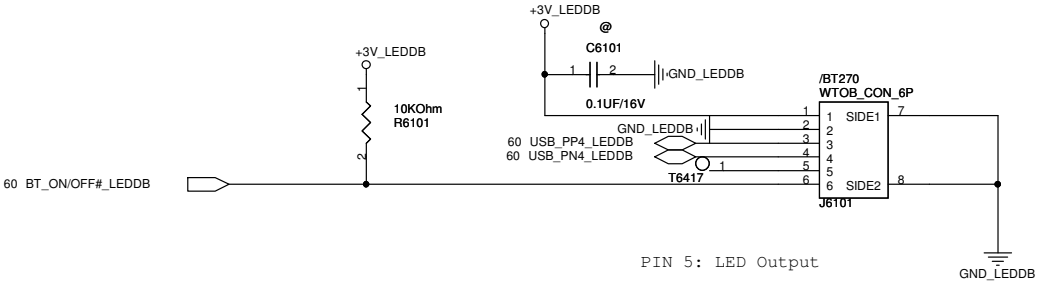




Dual Color

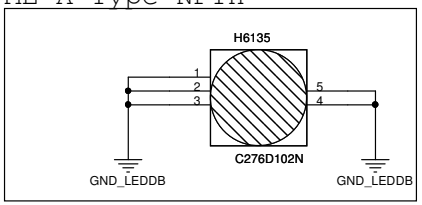


PEGATRON	Title : LED_Indicator		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 60 of 99		



PIN 5: LED Output

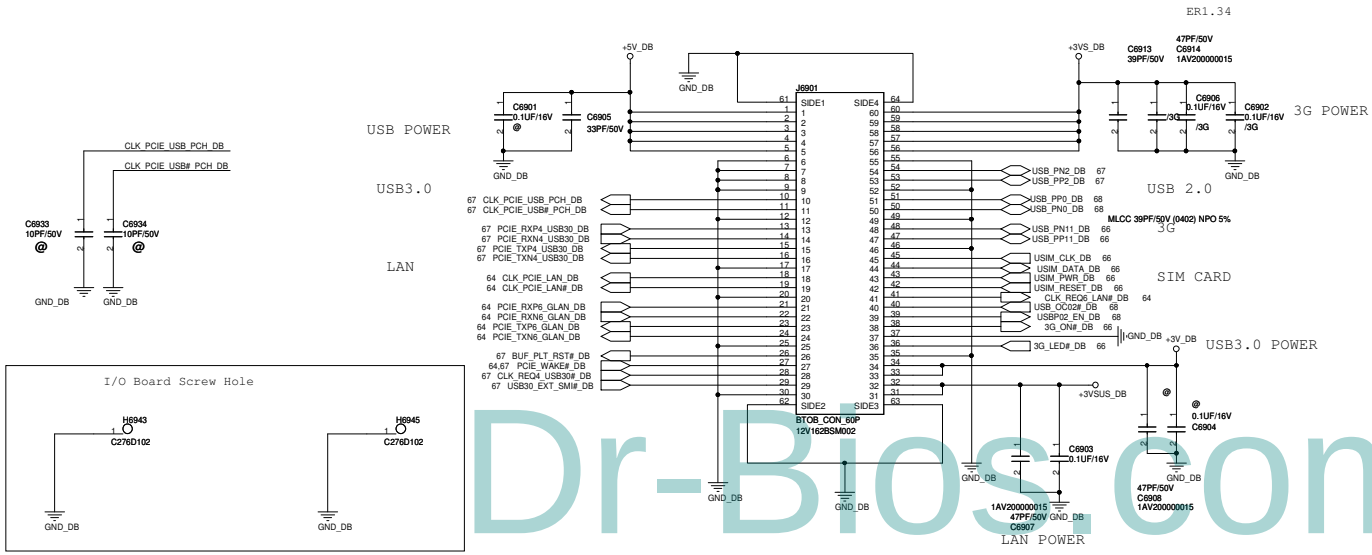
ME A Type NPTH



PEGATRON	Title : BT_Bluetooth	
<OrgName>	Engineer: JAY TSAI	
Size: B	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 61 of 99	

PEGATRON	Title : System Setting	
<OrgName>	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 06, 2011	Sheet 62 of 99	

DB



PEGATRON	Title : B to B	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 63 of 99	

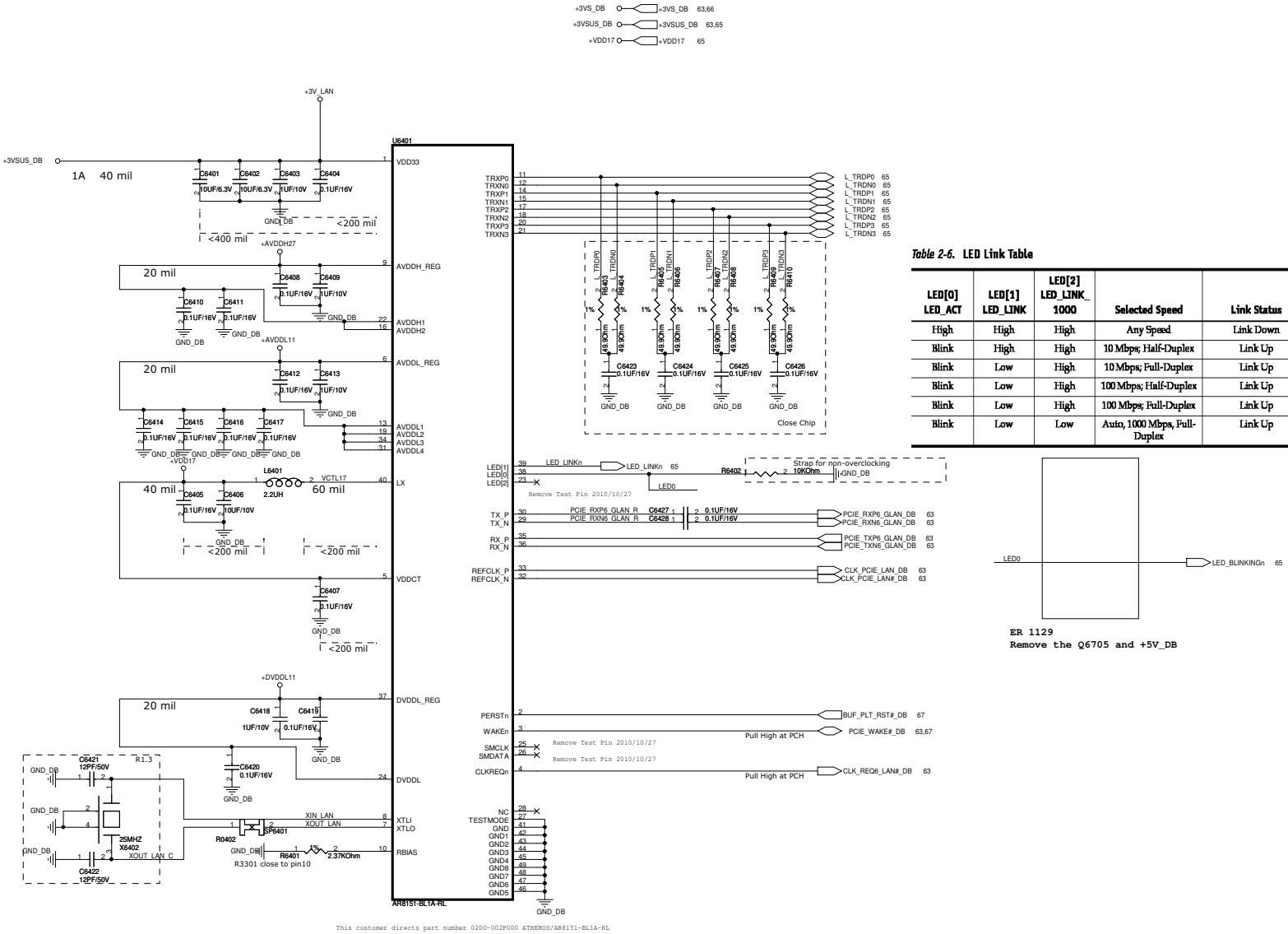
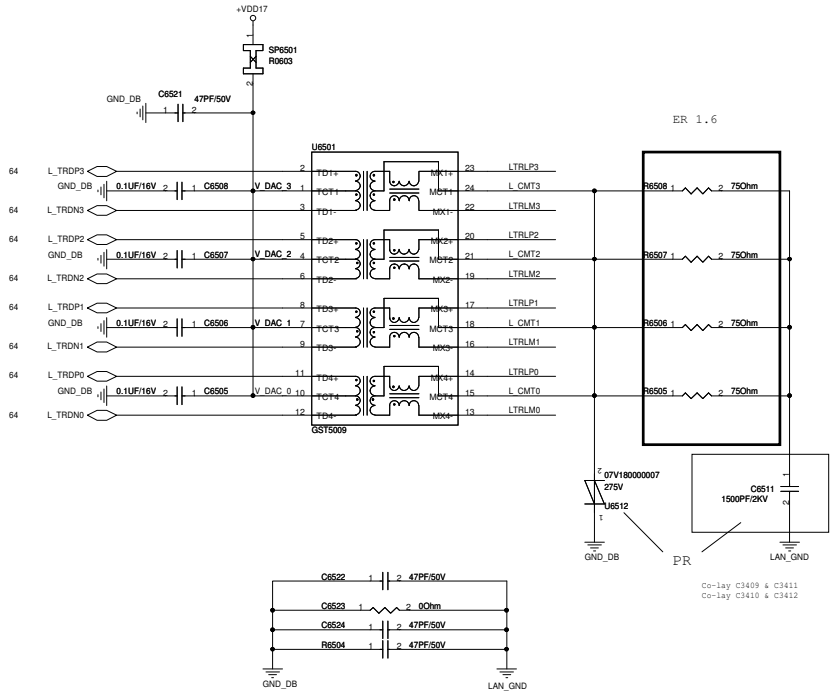
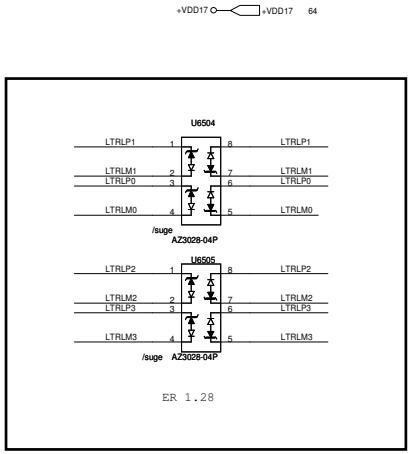


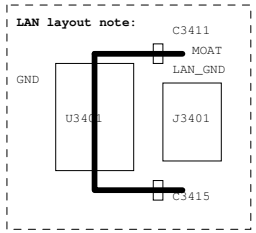
Table 2-6. **LED Link Table**

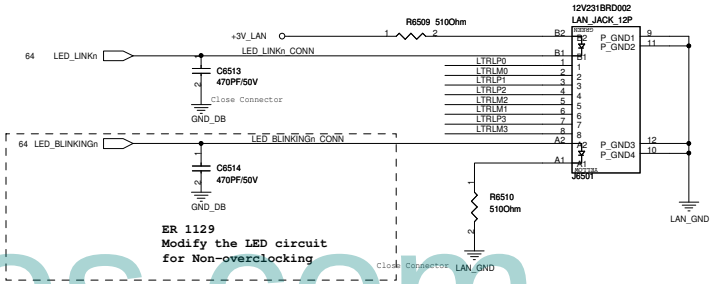
LED[0] LED_ACT	LED[1] LED_LINK	LED[2] LED_LINK_ 1000	Selected Speed	Link Status
High	High	High	Any Speed	Link Down
Blink	High	High	10 Mbps; Half-Duplex	Link Up
Blink	Low	High	10 Mbps; Full-Duplex	Link Up
Blink	Low	High	100 Mbps; Half-Duplex	Link Up
Blink	Low	High	100 Mbps; Full-Duplex	Link Up
Blink	Low	Low	Auto, 1000 Mbps, Full-Duplex	Link Up

PEGATRON	Title : LAN_AR8151		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31	Rev: 1.3	
Date: Thursday, January 13, 2011	Sheet 64 of 99		









PEGATRON Title : RJ45/ RJ11

<OrgName> Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

Date: Thursday, January 13, 2011 Sheet 65 of 99

+3VS_DB +3VS_DB 63
+3VSUS_DB +3VSUS_DB 63,64,65

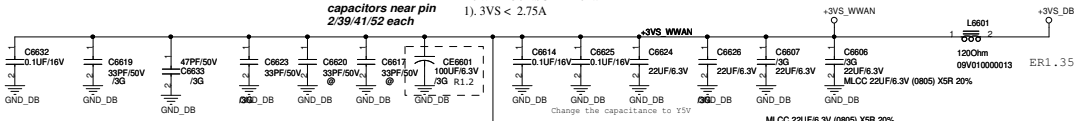
3G

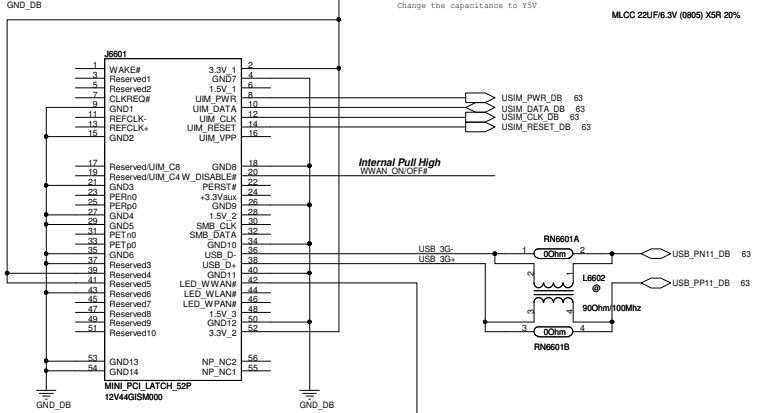
Place one 22uF capacitor near pin2, another near 39/41, the other near pin52.

Place 0.1uF & 33PF capacitors near pin 2/39/41/52 each

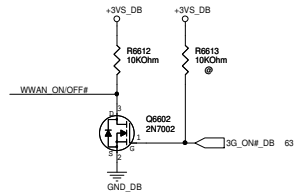
POWER CONSUMPTION:
1). 3VS < 2.75A

ER1.34

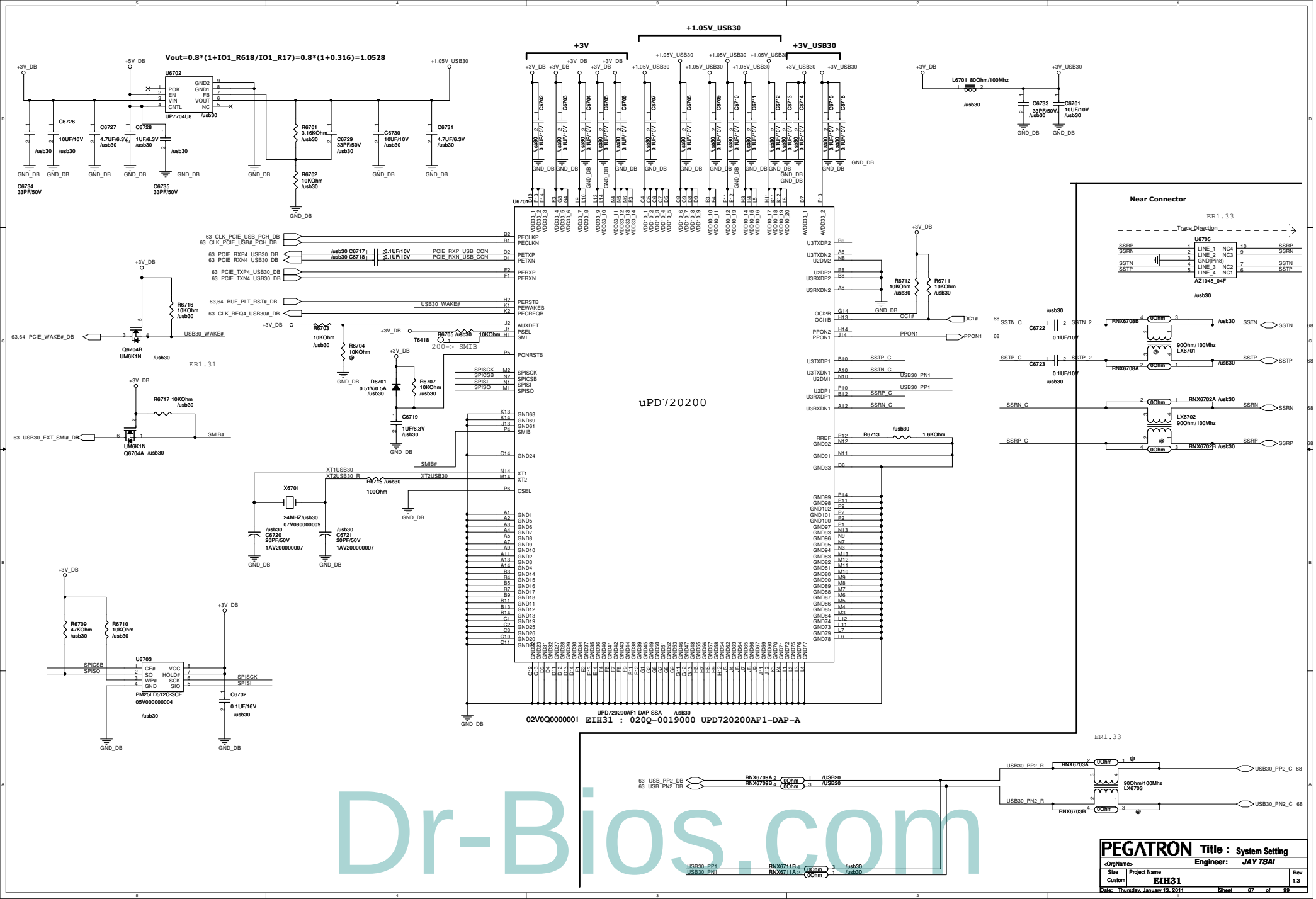




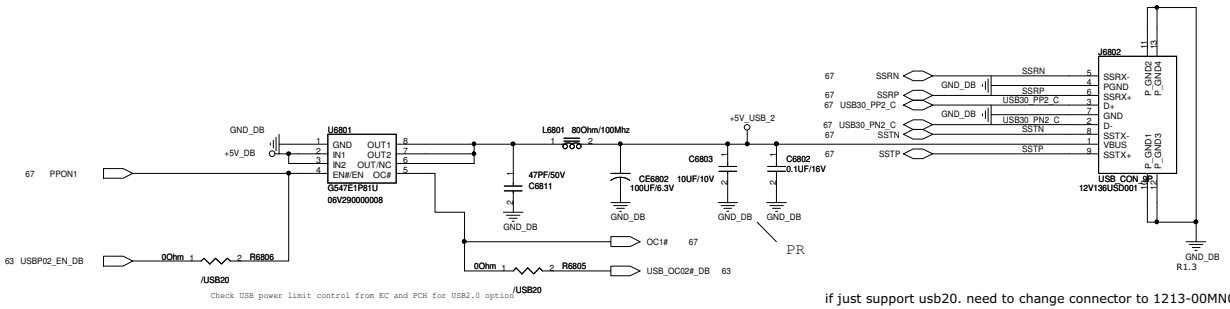
H=6.8mm



PEGATRON	Title : WLAN/ 3G	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 66 of 99	


Vout=0.8*(1+IO1_R618/IO1_R17)=0.8*(1+0.316)=1.0528
+1.05V_USB30
+3V
+3V_USB30
U6702
UP7704U8
uPD720200
Near Connector
ER1.33
ER1.31
Trace Direction
U6705
AZ1045_04F
U6703
PM25LD512C-SCE
05V000000004
X6701
24MHZ/usb30
07V080000009
Q6704B
UM6K1N
Q6704A
T6418
200-> SMIB
UPD720200AF1-DAP-SSA /usb30
02V0Q0000001 EIH31 : 020Q-0019000 UPD720200AF1-DAP-A
Dr-Bios.com
PEGATRON
Title : System Setting
Engineer: JAY TSAI
EIH31
Thursday, January 13, 2011
Sheet 67 of 99

USB ports



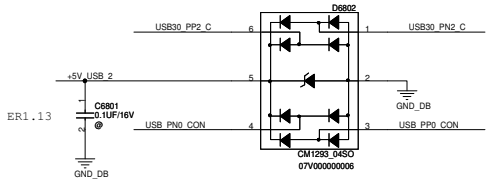
Check USB power limit control from EC and PCH for USB2.0 option

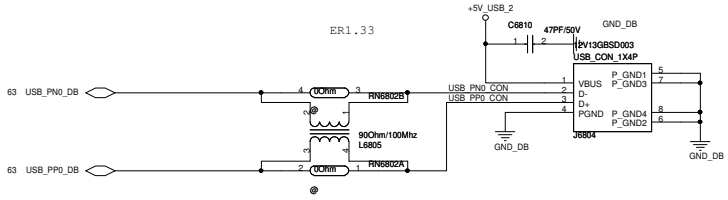
Boston:GPIO82:USBSLP_EN#,check KBID0

Boston:GPIO14:USB_OC2#_EC

BOM by USB 3.0 must change the U5201 for active HI solution.

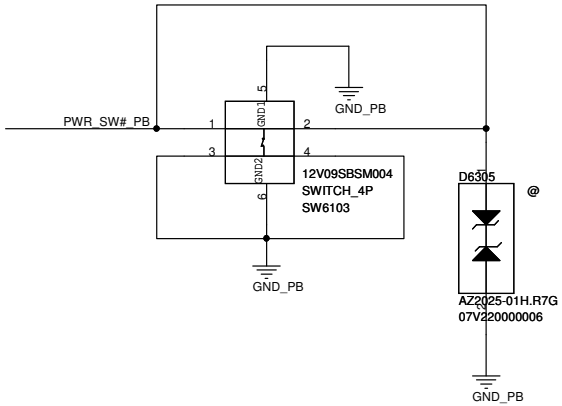
if just support usb20. need to change connector to 1213-00MN000 and unmount /usb30 and mount /usb20 in page 54



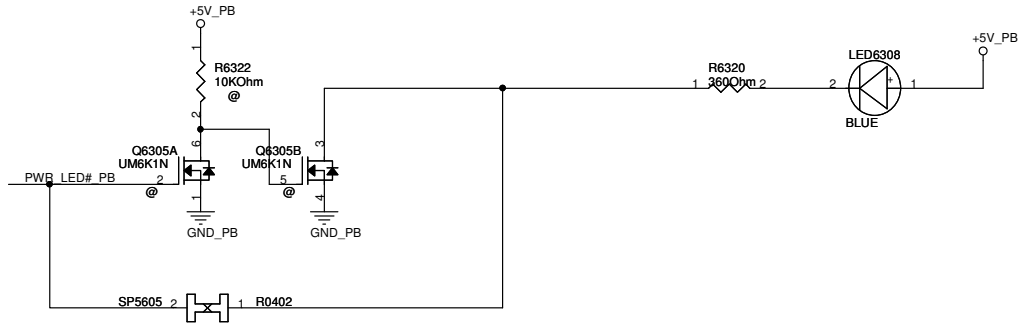


PEGATRON	Title : USB_USB Port		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 68 of 99		

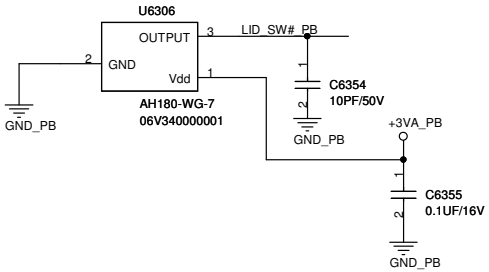
Power Button



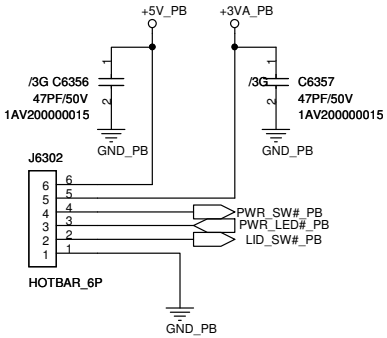
Power Button LED-Power



Hall Sensor



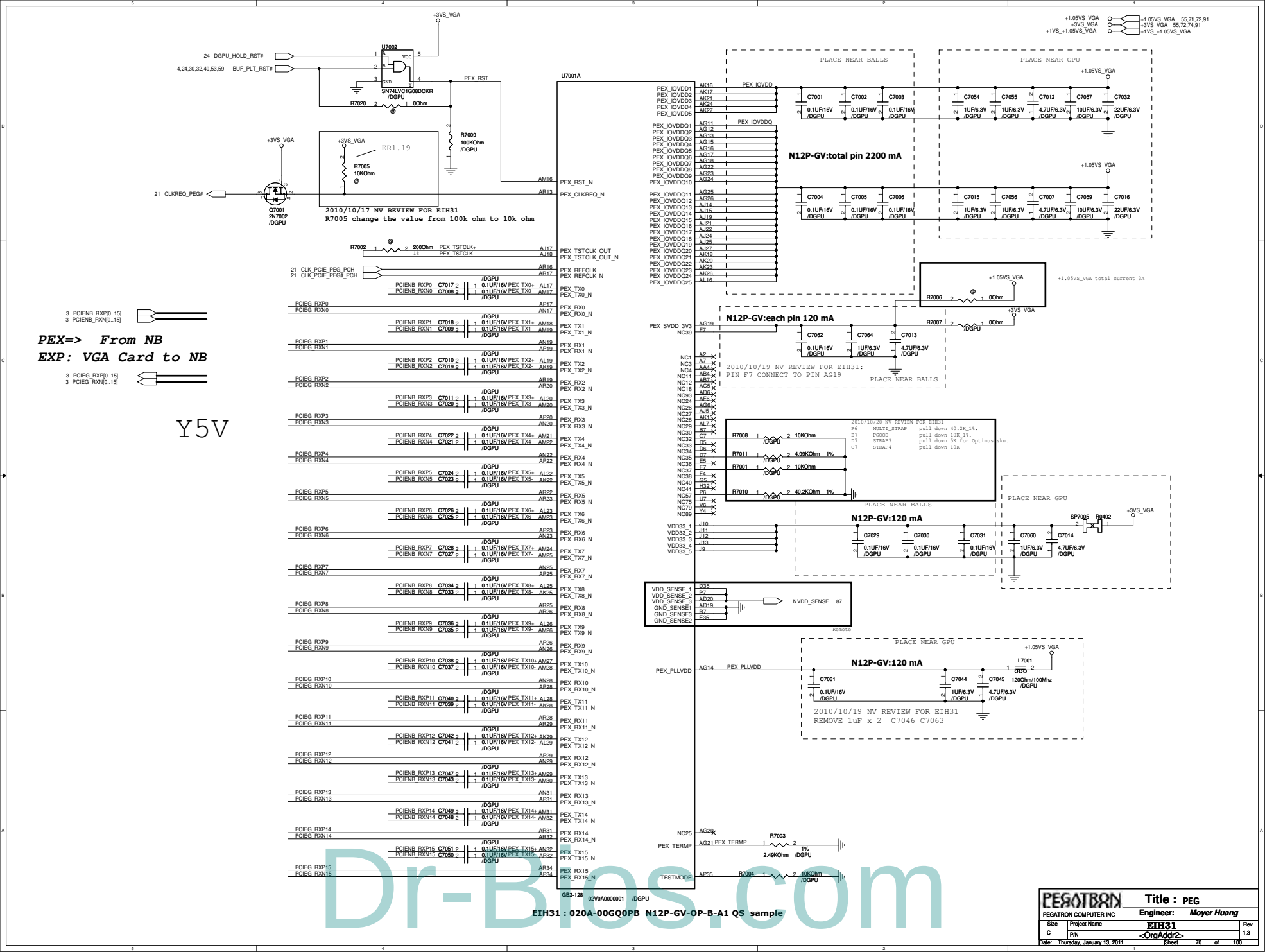
ER1.34



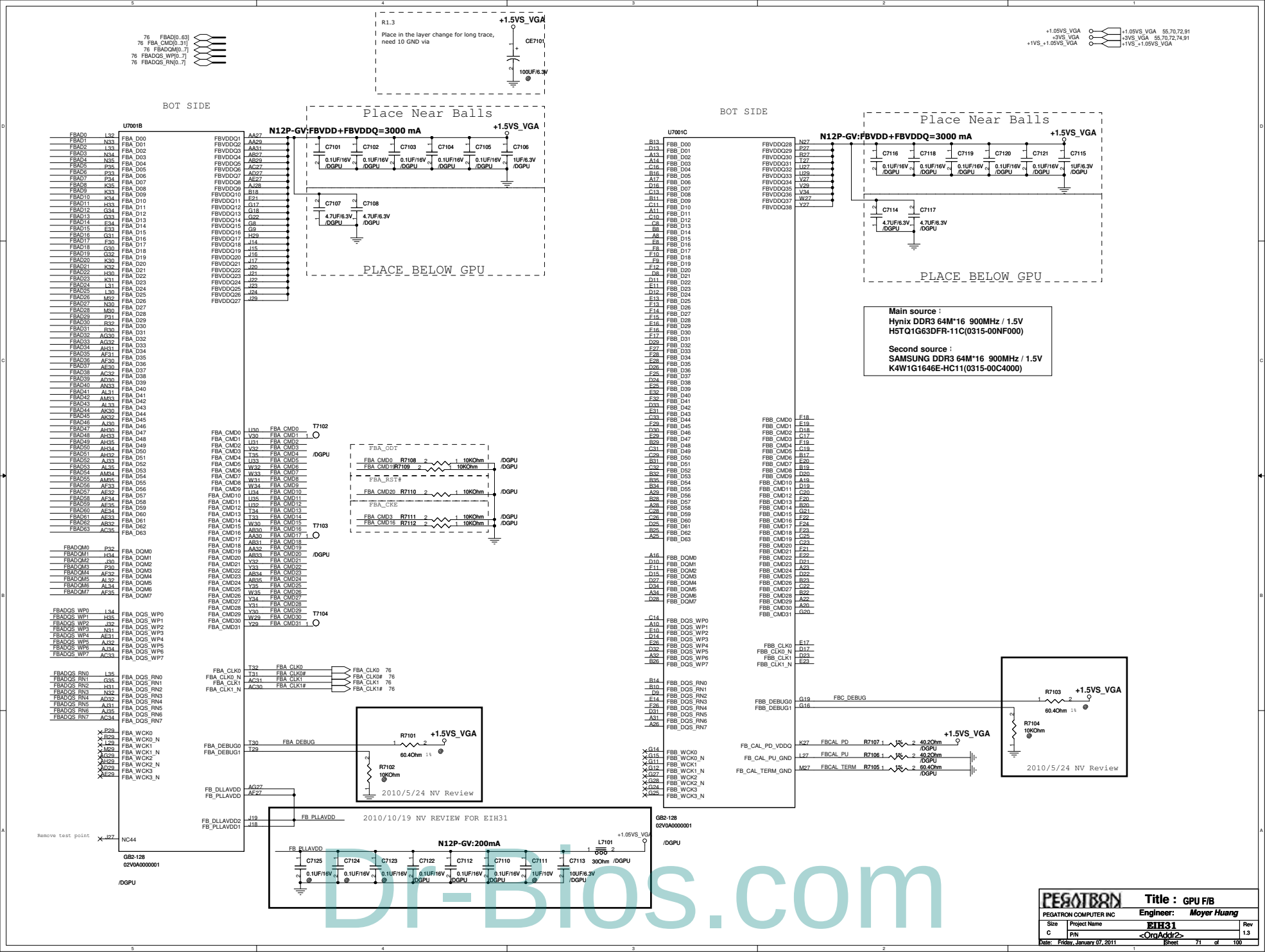
HOT bar

SKREW HOLE MAKING BY LAYOUT

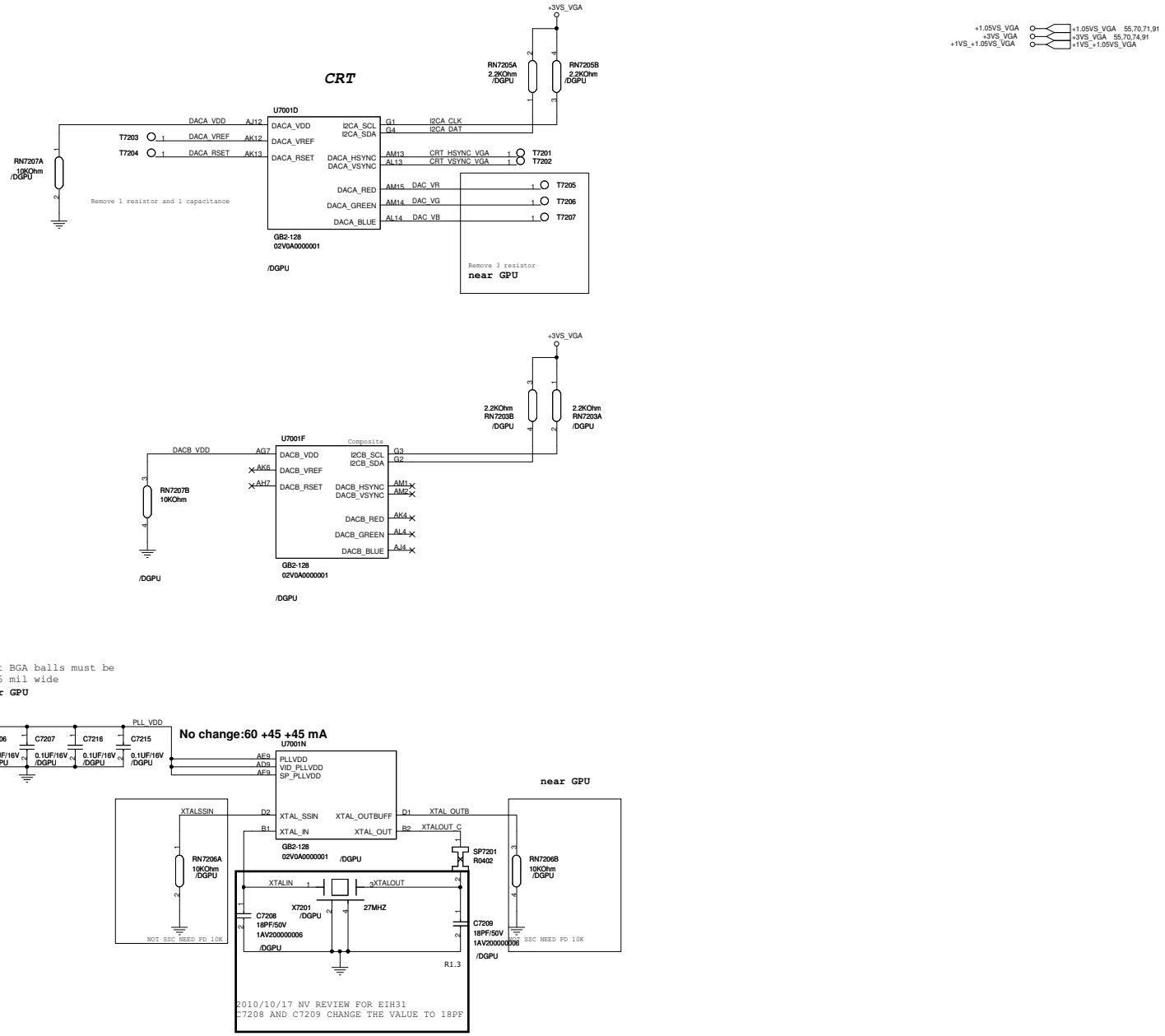
PEGATRON	Title : TPM_****	
<OrgName>	Engineer: JAY TSAI	
Size: B	Project Name: EIH31	Rev: 1.3
Date: Friday, January 07, 2011	Sheet 69 of 99	



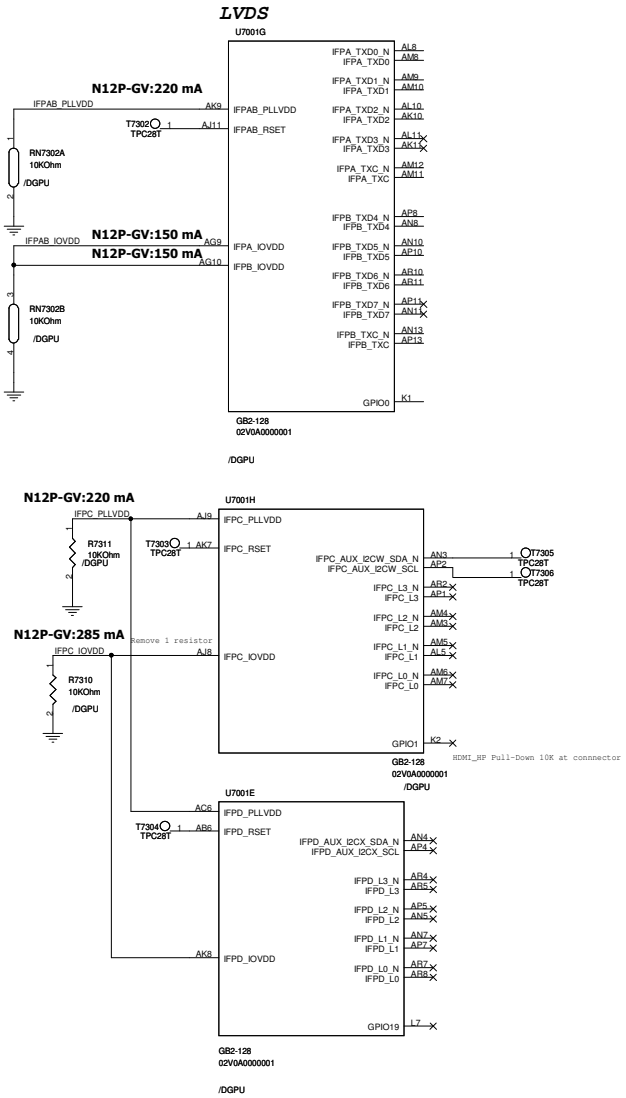
PEGATRON	Title : PEG		
PEGATRON COMPUTER INC	Engineer: Moyer Huang		
Size C	Project Name EIH31		Rev 1.3
	P/N <OrgAddr2>		
Date: Thursday, January 13, 2011	Sheet 70	of 100	



PEGATRON COMPUTER INC	Title : GPU F/B		
	Engineer: Moyer Huang		
Size: C	Project Name: EIH31		Rev: 1.3
	P/N: <OrgAddr2>		
Date: Friday, January 07, 2011	Sheet 71 of 100		



PEGATRON COMPUTER INC	Title : Connector, LED		
	Engineer: Moyer Huang		
Size: C	Project Name: EIH31		Rev: 1.3
	P/N: <OrgAddr2>		
Date: Friday, January 07, 2011	Sheet 72 of 100		



+1.05VS_VGA
+3VS_VGA
+1.05VS_VGA

+1.05VS_VGA 55,70,71,72,91
+3VS_VGA 55,70,72,74,91
+1.05VS_VGA 55,70,71,72,91

IFPx	A	B	C	D	E	F
MASERATI						

PEGATRON COMPUTER INC

Title : Connector, LED

Engineer: Moyer Huang

Size	Project Name	Rev
C	EIH31	1.3
	P/N <OrgAddr2>	

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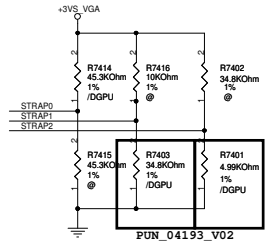
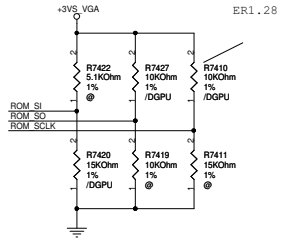
+1.05VS_VGA
+3VS_VGA
+1.05VS_VGA

+1.05VS_VGA 55,70,71,72,91
+3VS_VGA 55,70,72,91
+1.05VS_VGA 55,70,71,72,91





ER1.28

STRAP0

USER[3:0]

3	2	1	0	PANEL	VS/HS
0	0	0	0	XGA	-/-
0	0	0	1	XGA	+/+
0	0	1	0	SXGA	+/+
0	0	1	1	SXGA+	-/-
0	1	0	0	UXGA	+/+
1	1	1	1	EDID	N/A

STRAP1

3GIO_PAD_CFG_ADR[3:0]

3	2	1	0	PANEL
0	0	0	0	RESERVED
0	1	1	0	NOTEBOOK
.				
.				
1	1	1	1	RESERVED

STRAP2

LOGICAL BIT	
0	PCI_DEVID[0]
1	PCI_DEVID[1]
2	PCI_DEVID[2]
3	PCI_DEVID[3]

ROM_SI_RAMCONFIG

MONO RANK

Hynix 64Mx16 -> ram_cfg = 0x2
Samsung 64Mx16 -> ram_cfg = 0x3
Hynix 128Mx16 -> ram_cfg = 0x6
Samsung 128Mx16 -> ram_cfg = 0x7

ROM_SO

LOGICAL BIT	
3	XCLK_417
2	FB_0_BAR_SIZE
1	SMB_ALT_ADDR
0	VGA_DEVICE

ROM_SCLK

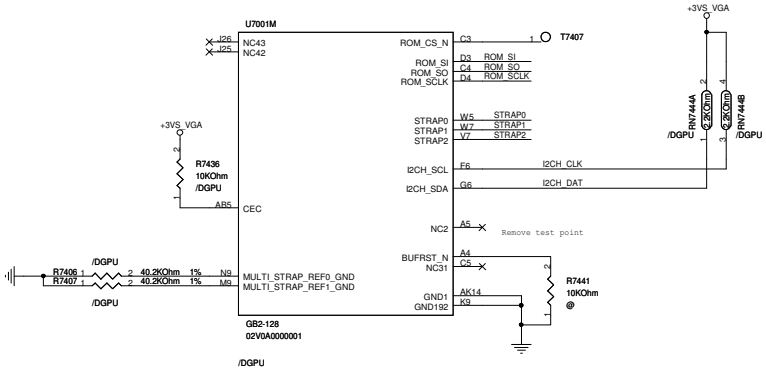
LOGICAL BIT	
3	PCI_DEVID[4]
2	SUB_VENDER
1	SLOT_CLK_CFG
0	PEX_PLL_EN_TERM

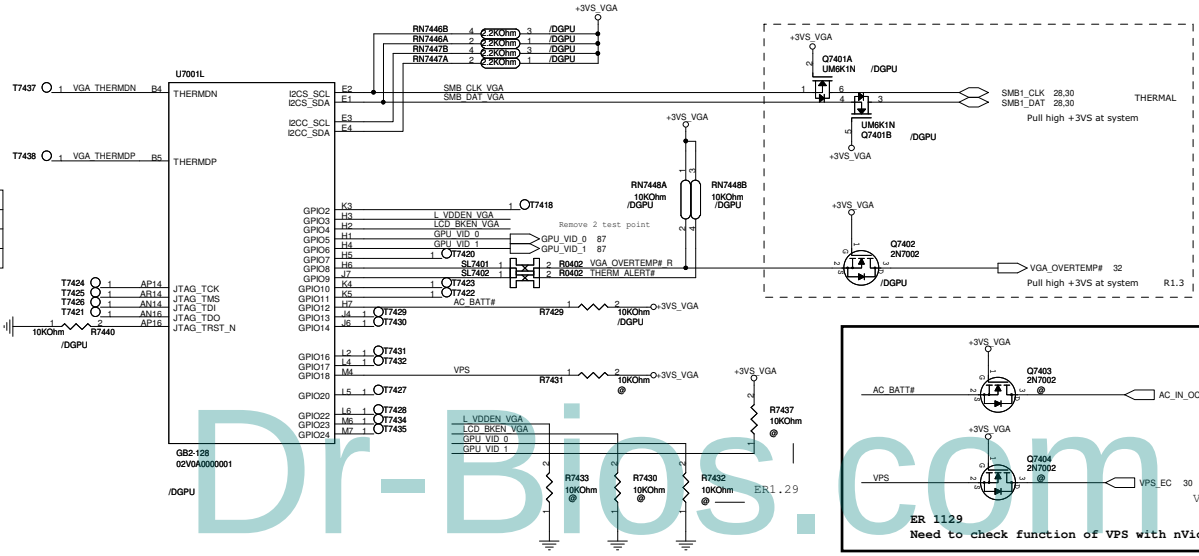
5K PU 1000 PD 0000
10K PU 1001 PD 0001
15K PU 1010 PD 0010
20K PU 1011 PD 0011
25K PU 1100 PD 0100
30K PU 1101 PD 0101
35K PU 1110 PD 0110
45K PU 1111 PD 0111

N12P-GS : 0x0DF4
~10100
= PCI_DEVICE[4][3][2][1][0]

GPIO USAGE

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	IFPAB HOTPLUG DETECT
1	IN	N/A	IFPC HOTPLUG DETECT
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD ALTV0
6	OUT	HIGH	NVVDD ALTV1
7	OUT	HIGH	FBVDDQ ALTV
8	IN/OUT	LOW	OVERTEMP ALERT
9	OUT	LOW	THERMAL ALERT
10	OUT	HIGH	FB_VREF CONTROL
11	OUT	HIGH	RESERVED
12	IN	N/A	AC DETECT
13	OUT	LOW	LOAD STEP DOWN
14	OUT	HIGH	LOAD STEP UP
15	IN	N/A	IFPE HOTPLUG DETECT
16	IN	N/A	FAN PWM OUT
17	IN	N/A	FAN TACH IN
18	IN	N/A	RESERVED
19	IN	N/A	IFPD HOTPLUG DETECT
20	IN	N/A	RESERVED
21	IN	N/A	IFPF HOTPLUG DETECT
22	IN	N/A	RESERVED
23	IN	N/A	RESERVED
24	IN	N/A	RESERVED





GPU_VID	VID1	VID0	+VGA_VCORE
Low	0	0	0.85V
Med	0	1	1V
High	1	0	1.025V

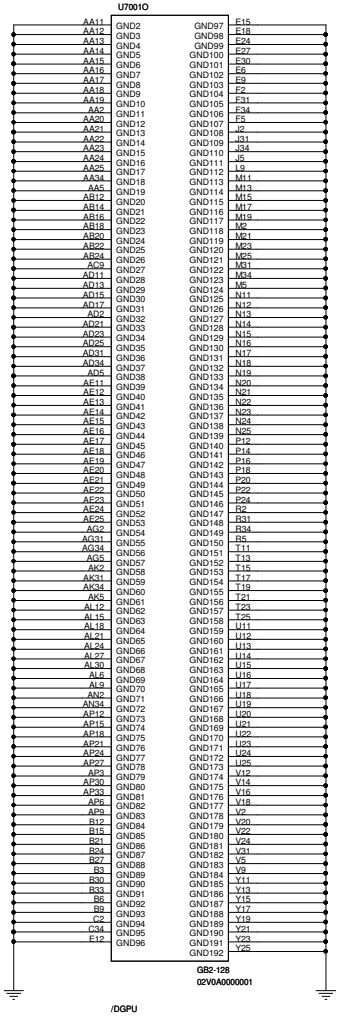
PEGATRON COMPUTER INC

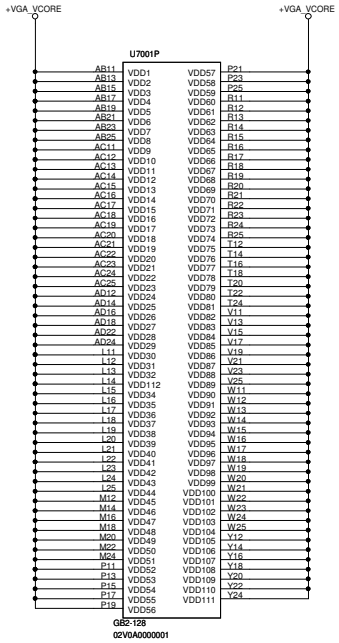
Title : Connector, LED

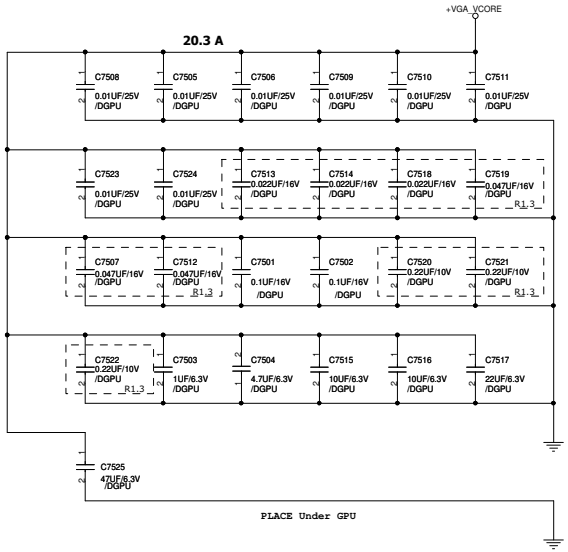
Engineer: Moyer Huang

Size	Project Name	Rev
C	EIH31	1.3
	P/N <OrgAddr2>	

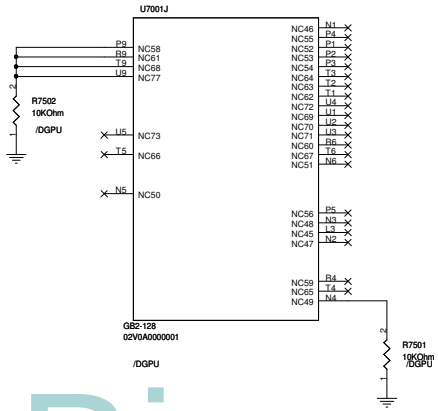
Date: Thursday, January 13, 2011 Sheet 74 of 100

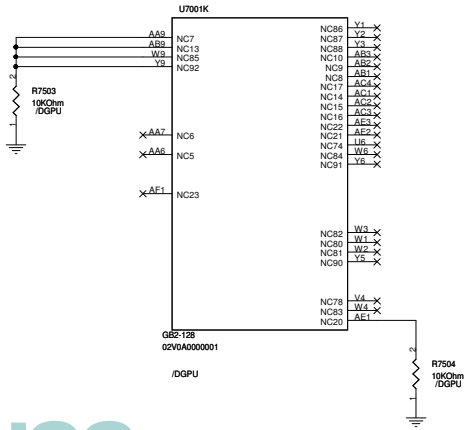






NV Design Guide	Maserati
0.01U x 8	0.01U x 8
0.022U x 3	0.022U x 3
0.047U x 3	0.047U x 3
0.1U x 2	0.1U x 2
0.22U x 3	0.22U x 3
1U x 1	1U x 1
4.7U x 1	4.7U x 1
10U x 2	10U x 2
22U x 1	22U x 1
47U x 1	47U x 1

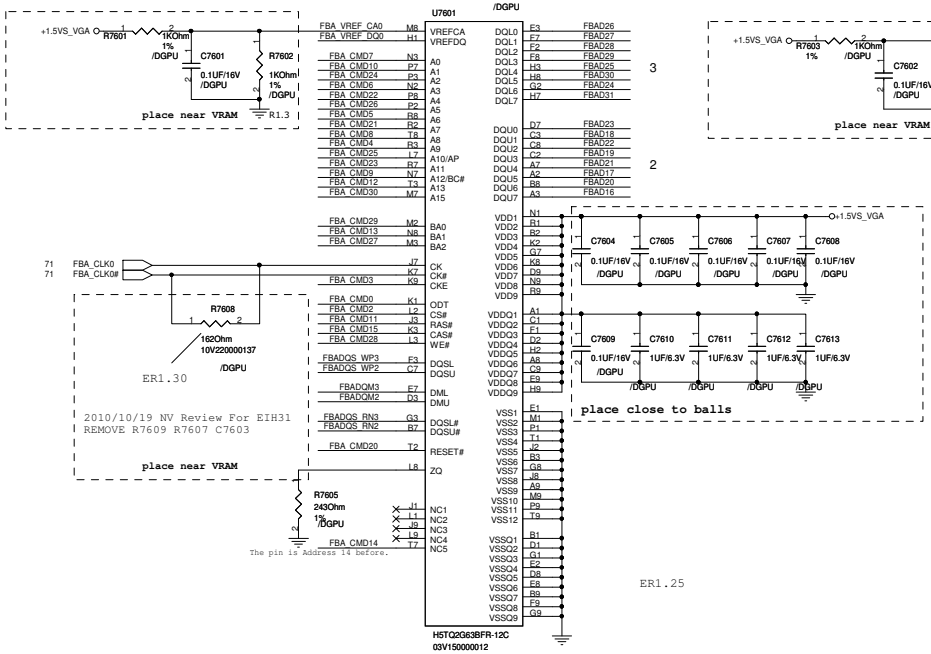




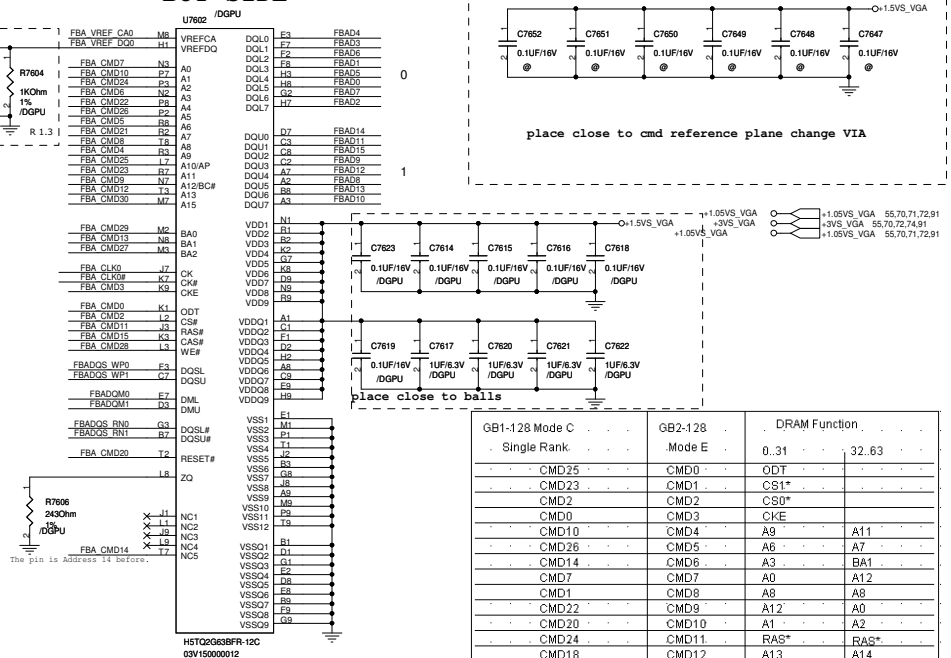
PEGATRON COMPUTER INC	Title : GPU PWR/GND		
	Engineer: Moyer Huang		
Size: C	Project Name: EIH31		Rev: 1.3
	P/N: <OrgAddr2>		
Date: Friday, January 07, 2011	Sheet 75 of 100		

VRAM CH A

TOP SIDE

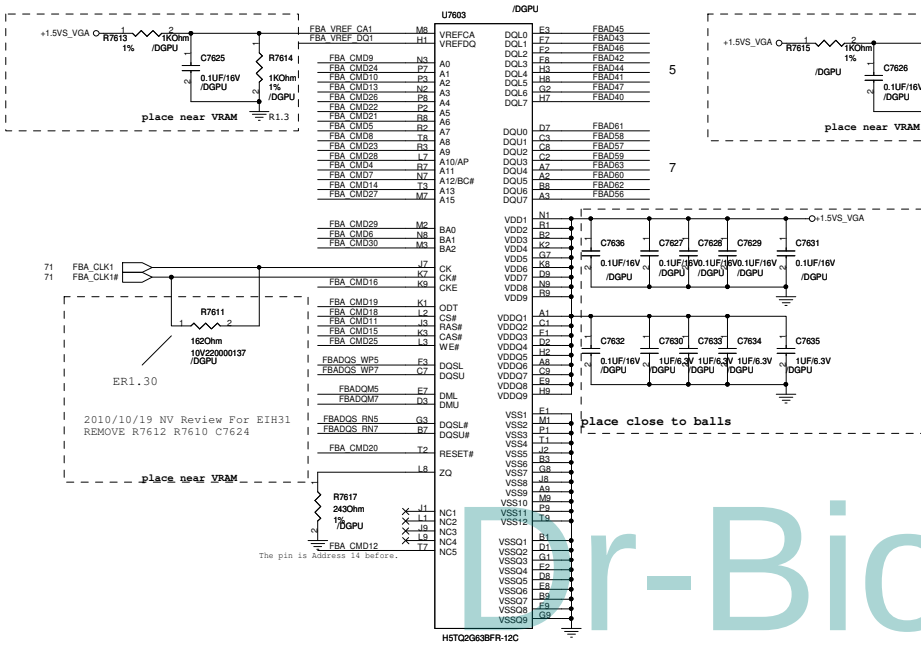


BOT SIDE

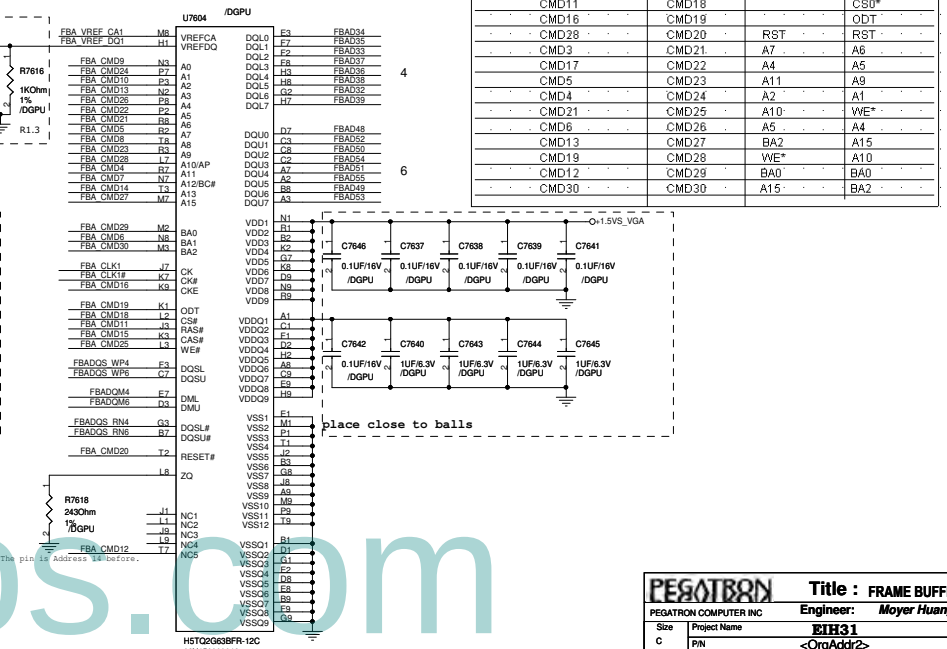


GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function 0..31	32..63
CMD25	CMD0	ODT	
CMD23	CMD1	CS1*	
CMD2	CMD2	CS0*	
CMD0	CMD3	CKE	
CMD10	CMD4	A9	A11
CMD26	CMD5	A6	A7
CMD14	CMD6	A3	BA1
CMD7	CMD7	A0	A12
CMD1	CMD8	A8	A8
CMD22	CMD9	A12	A0
CMD20	CMD10	A1	A2
CMD24	CMD11	RAS*	RAS*
CMD18	CMD12	A13	A14
CMD9	CMD13	BA1	A3
CMD29	CMD14	A14	A13
CMD8	CMD15	CAS*	CAS*
CMD27	CMD16		CKE
CMD15	CMD17		CS1*
CMD11	CMD18		CS0*
CMD16	CMD19		ODT
CMD28	CMD20	RST	RST
CMD3	CMD21	A7	A6
CMD17	CMD22	A4	A5
CMD5	CMD23	A11	A9
CMD4	CMD24	A2	A1
CMD21	CMD25	A10	WE*
CMD6	CMD26	A5	A4
CMD13	CMD27	BA2	A15
CMD19	CMD28	WE*	A10
CMD12	CMD29	BA0	BA0
CMD30	CMD30	A15	BA2

TOP SIDE



BOT SIDE



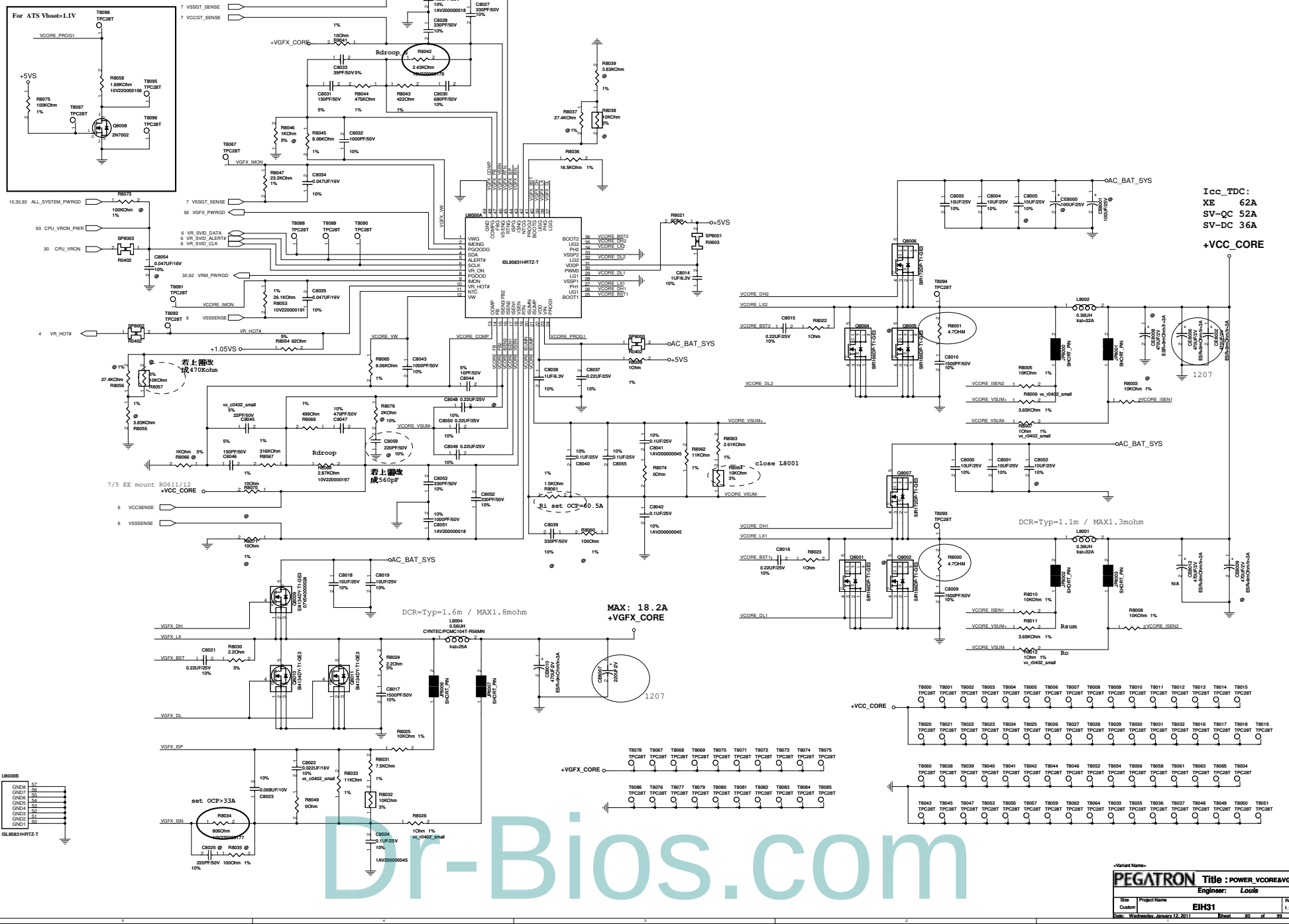
PEGATRON	Title :	FRAME BUFFER A	
PEGATRON COMPUTER INC	Engineer:	Moyer Huang	
Size: C	Project Name: EIH31		Rev: 1.3
	P/N: <OrgAddr2>		
Date: Thursday, January 13, 2011	Sheet 76 of 100		

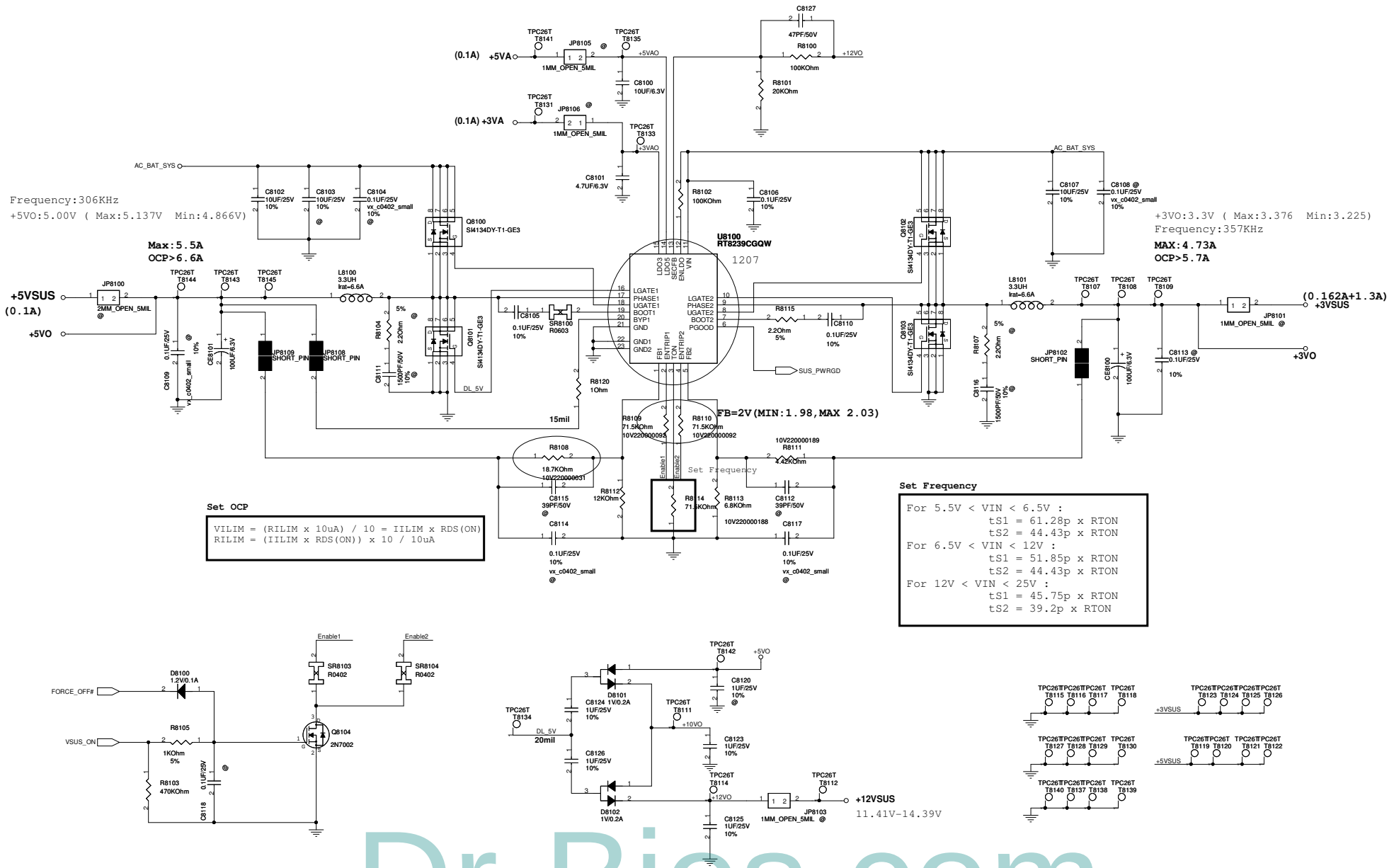
PEGATRON COMPUTER INC	Title : FRAME BUFFER C		
	Engineer: *Moyer Huang*		
Size: C	Project Name: EIH31		Rev: 1.3
	P/N: <OrgAddr2>		
Date: Tuesday, January 04, 2011	Sheet 77 of 100		

PEGATRON	Title :	FRAME BUFFER C	
PEGATRON COMPUTER INC	Engineer:	*Moyer Huang*	
Size: A	Project Name:	EIH31	Rev: 1.3
	P/N:	<OrgAddr2>	
Date: Tuesday, January 04, 2011	Sheet 78 of 100		

PEGATRON		Title :	FRAME BUFFER C	
PEGATRON COMPUTER INC		Engineer:	*Moyer Huang*	
Size	Project Name	EIH31		Rev
A	P/N	<OrgAddr2>		1.3
Date: Tuesday, January 04, 2011		Sheet 79 of 100		

HURON RIVER





<variant_name>

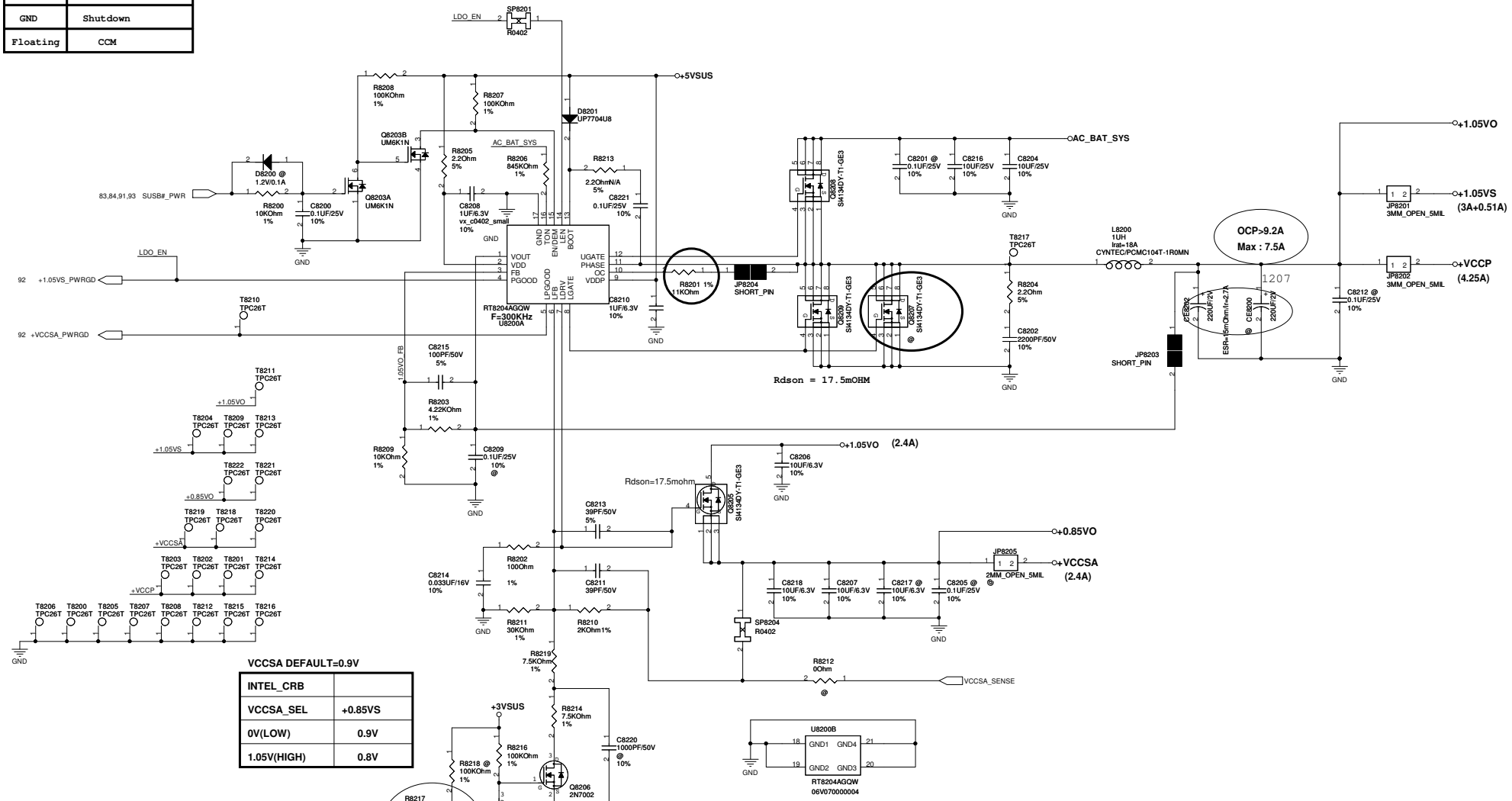
PEGATRON Title : POWER_SYSTEM
Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Wednesday, January 12, 2011 Sheet 81 of 94

VCCP & VCCSA POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation'
GND	Shutdown
Floating	CCM



<Variant Name>

PEGATRON Title : POWER_VCCP

Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Thursday, January 13, 2011 Sheet 82 of 94

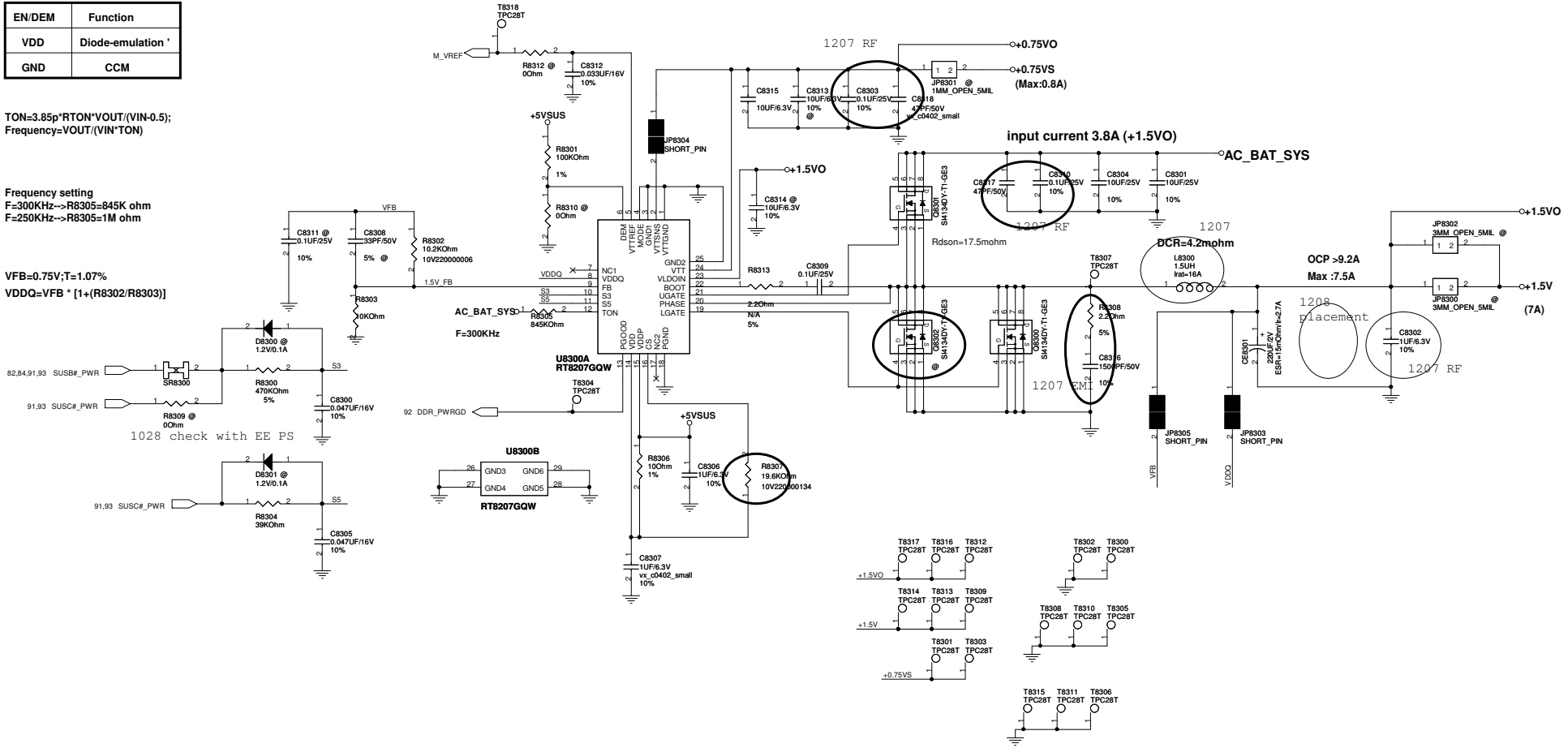
DDR & VTT POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation '
GND	CCM

TON=3.85p*RTON*VOUT/(VIN-0.5);
Frequency=VOUT/(VIN*TON)

Frequency setting
F=300KHz-->R8305=845K ohm
F=250KHz-->R8305=1M ohm

VFB=0.75V;T=1.07%
VDDQ=VFB * [1+(R8302/R8303)]



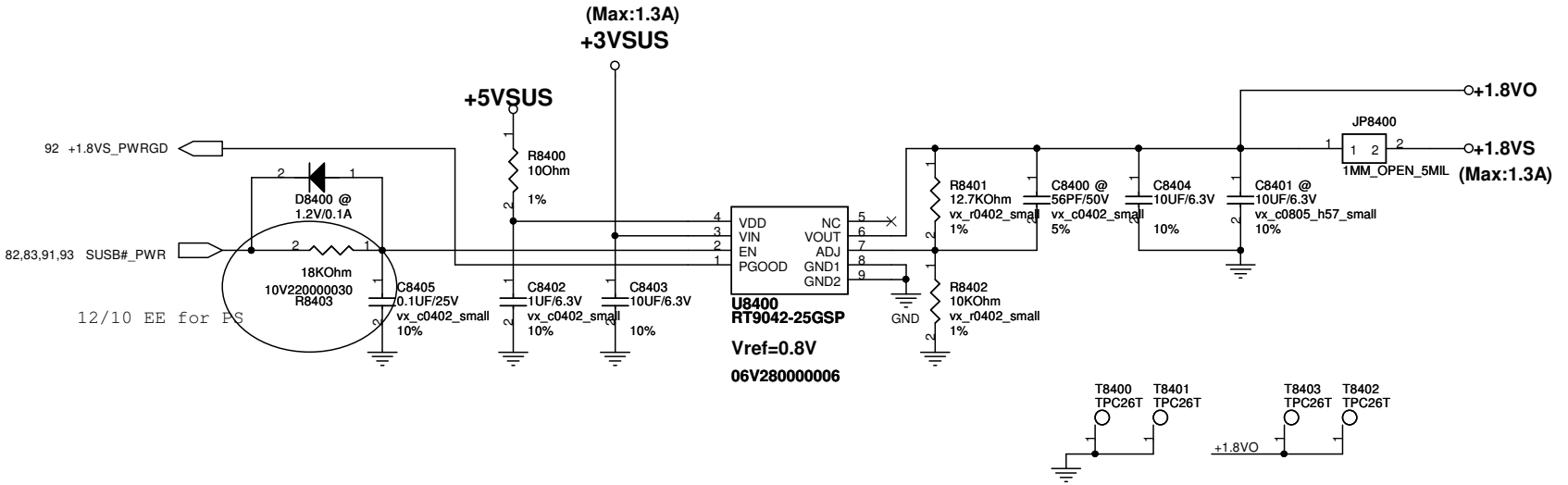
<Variant Name>

PEGATRON Title : POWER_DDR & VTT
Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Thursday, January 13, 2011 Sheet 83 of 94

1.8VS POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_1.8VS

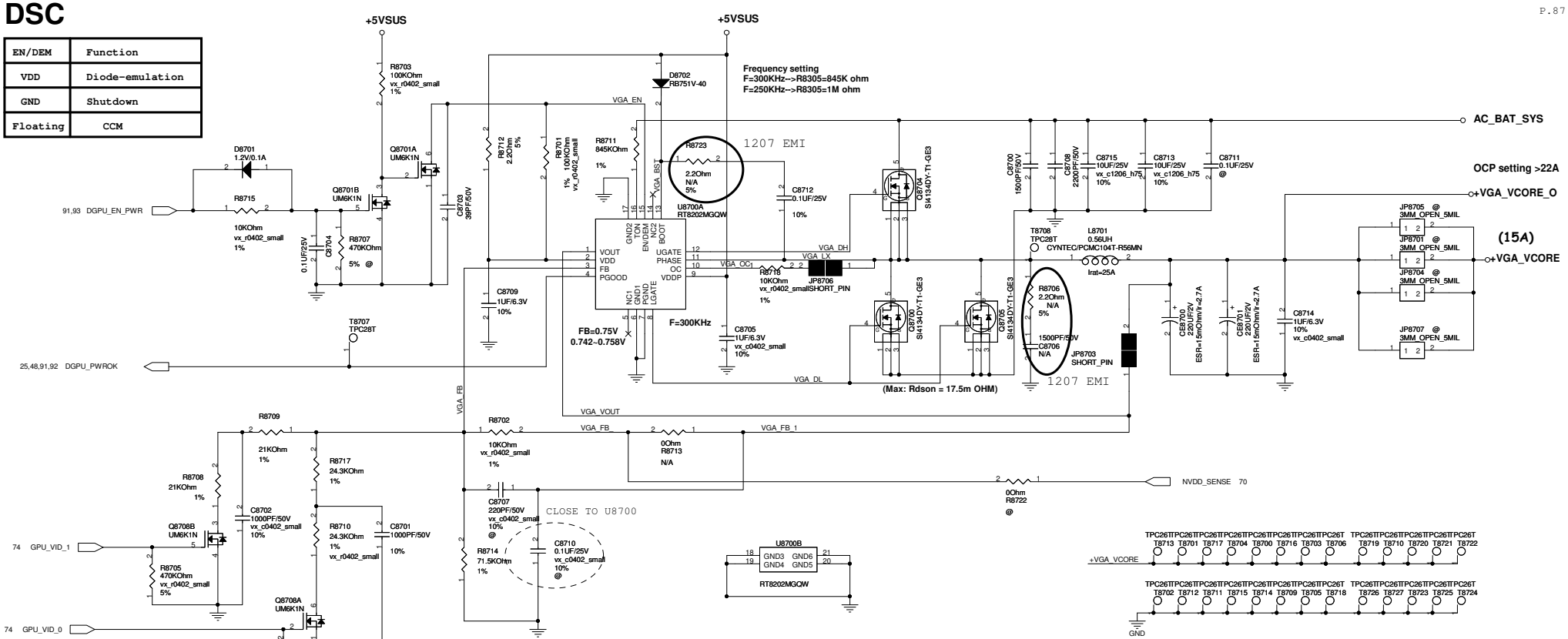
Engineer: *Louis*

Size	Project Name	Rev
Custom	EIH31	1.1

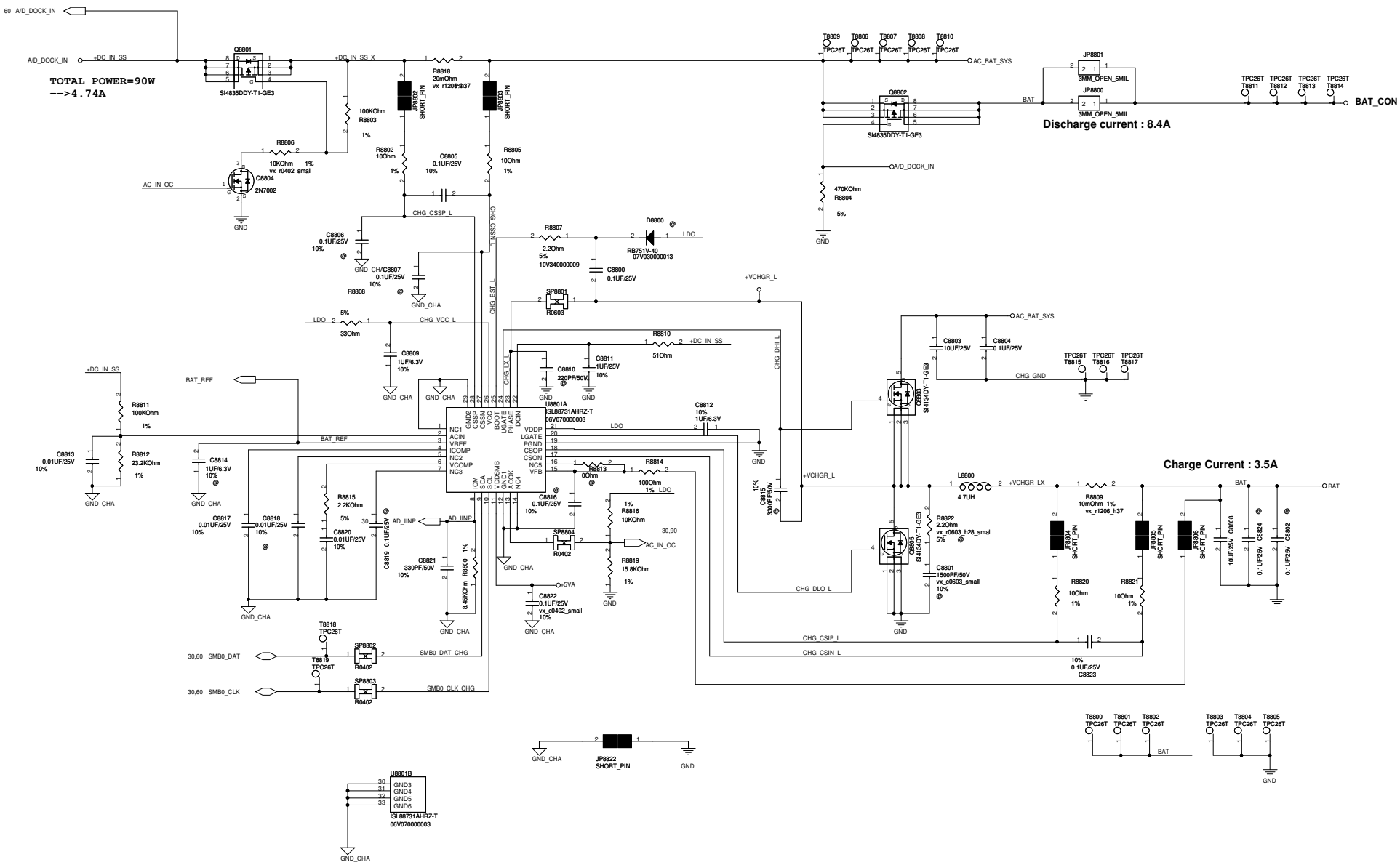
Date: Wednesday, January 12, 2011 Sheet 84 of 94

DSC

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM

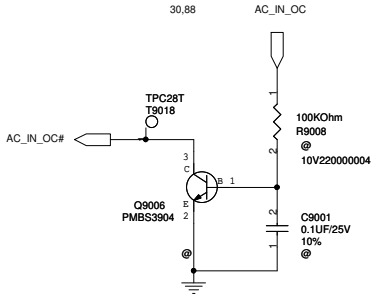


GPU_VID_1	GPU_VID_0	+VGA_VCORE_O(N12p-GS)	+VGA_VCORE_O(N12P-GV)
L	L	0.825V	0.85V
L	H	0.975V	1V
H	L	1V	1.025V
H	H	X	


60 A/D_DOCK_IN
A/D_DOCK_IN
+DC_IN_SS
TOTAL POWER=90W
-->4.74A
Q8801
SI4835DDY-T1-GE3
+DC_IN_SS_X
R8818
20mOhm
vx_r1206_h37
JP8802
SHORT_PIN
JP8803
SHORT_PIN
100KOhm
R8803
1%
R8806
10KOhm 1%
vx_r0402_small
Q8804
2N7002
AC_IN_OC
R8802
10Ohm
1%
C8805
0.1UF/25V
10%
R8805
10Ohm
1%
CHG_CSSP_L
CHG_CSSN_L
C8806
0.1UF/25V
10%
GND_CHA
C8807
0.1UF/25V
10%
R8808
@
R8807
2.2Ohm
5%
10V340000009
D8800
@
LDO
RB751V-40
07V030000013
C8800
0.1UF/25V
SP8801
R0603
+VCHGR_L
LDO
5%
33Ohm
CHG_VCC_L
C8809
1UF/6.3V
10%
CHG_BST_L
R8810
51Ohm
+DC_IN_SS
C8811
1UF/25V
10%
C8810
220PF/50V
@
CHG_LX_L
CHG_DHI_L
U8801A
ISL88731AHRZ-T
06V070000003
C8812
10%
1UF/6.3V
BAT_REF
R8811
100KOhm
1%
R8812
23.2KOhm
1%
C8813
0.01UF/25V
10%
C8814
1UF/6.3V
10%
@
R8813
0Ohm
@
R8814
100Ohm
1% LDO
C8816
0.1UF/25V
10%
C8817
0.01UF/25V
10%
C8818
0.01UF/25V
10%
@
R8815
2.2KOhm
5%
C8820
0.01UF/25V
10%
C8819
0.1UF/25V
AD_IINP
C8821
330PF/50V
10%
R8800
1%
8.45KOhm
SP8804
R0402
30,90
AC_IN_OC
R8816
10KOhm
1%
R8819
15.8KOhm
1%
+5VA
C8822
0.1UF/25V
vx_c0402_small
10%
T8818
TPC26T
T8819
TPC26T
30,60 SMB0_DAT
30,60 SMB0_CLK
SP8802
SP8803
R0402
SMB0_DAT_CHG
SMB0_CLK_CHG
U8801B
ISL88731AHRZ-T
06V070000003
JP8822
SHORT_PIN
T8809
T8806
T8807
T8808
T8810
TPC26T
AC_BAT_SYS
JP8801
3MM_OPEN_5MIL
JP8800
3MM_OPEN_5MIL
BAT
BAT_CON
Discharge current : 8.4A
Q8802
SI4835DDY-T1-GE3
A/D_DOCK_IN
470KOhm
R8804
5%
TPC26T
T8811
T8812
T8813
T8814
Q8803
SI4134DY-T1-GE3
C8803
10UF/25V
C8804
0.1UF/25V
CHG_GND
TPC26T
T8815
T8816
T8817
Charge Current : 3.5A
L8800
4.7UH
+VCHGR_LX
C8815
10%
330PF/50V
R8809
10mOhm 1%
vx_r1206_h37
Q8805
SI4134DY-T1-GE3
R8822
2.2Ohm
vx_r0603_h28_small
5%
C8801
1500PF/50V
vx_c0603_small
10%
JP8804
SHORT_PIN
JP8805
SHORT_PIN
JP8806
SHORT_PIN
R8820
10Ohm
1%
R8821
10Ohm
1%
C8808
10UF/25V
C8824
0.1UF/25V
C8802
0.1UF/25V
CHG_DLO_L
CHG_CSIP_L
CHG_CSIN_L
C8823
10%
0.1UF/25V
T8800
T8801
T8802
TPC26T
T8803
T8804
T8805
TPC26T
BAT
GND

BATTERY IN DETECT

ADAPTER IN DETECT



<Variant Name>

PEGATRON Title : POWER_DETECT

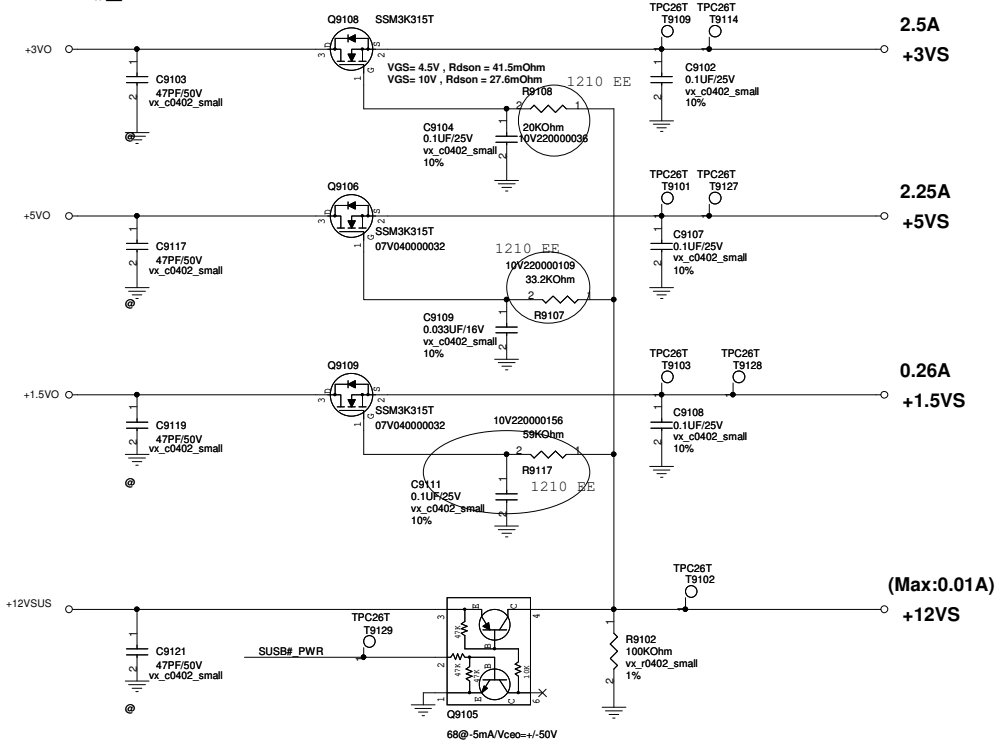
Engineer: *Louis*

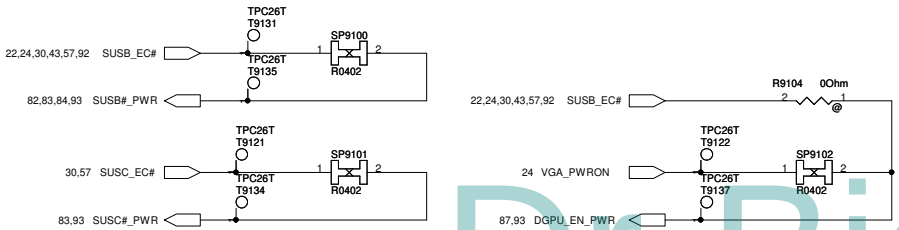
Size	Project Name	Rev
Custom	EIH31	1.1

Date: Thursday, January 13, 2011 Sheet 90 of 99

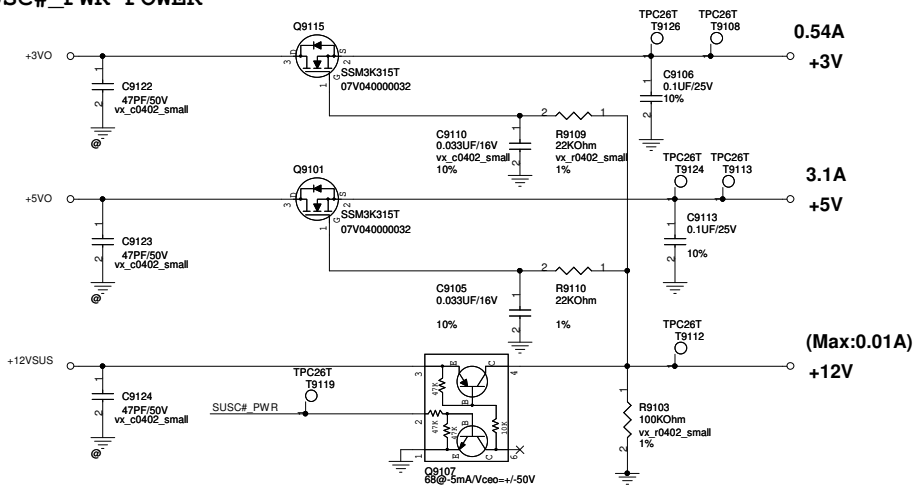
Ron = 41.5 mΩ (max) (@VGS = 4.5 V)
Ron = 27.6 mΩ (max) (@VGS = 10 V)

SUSB#_PWR POWER



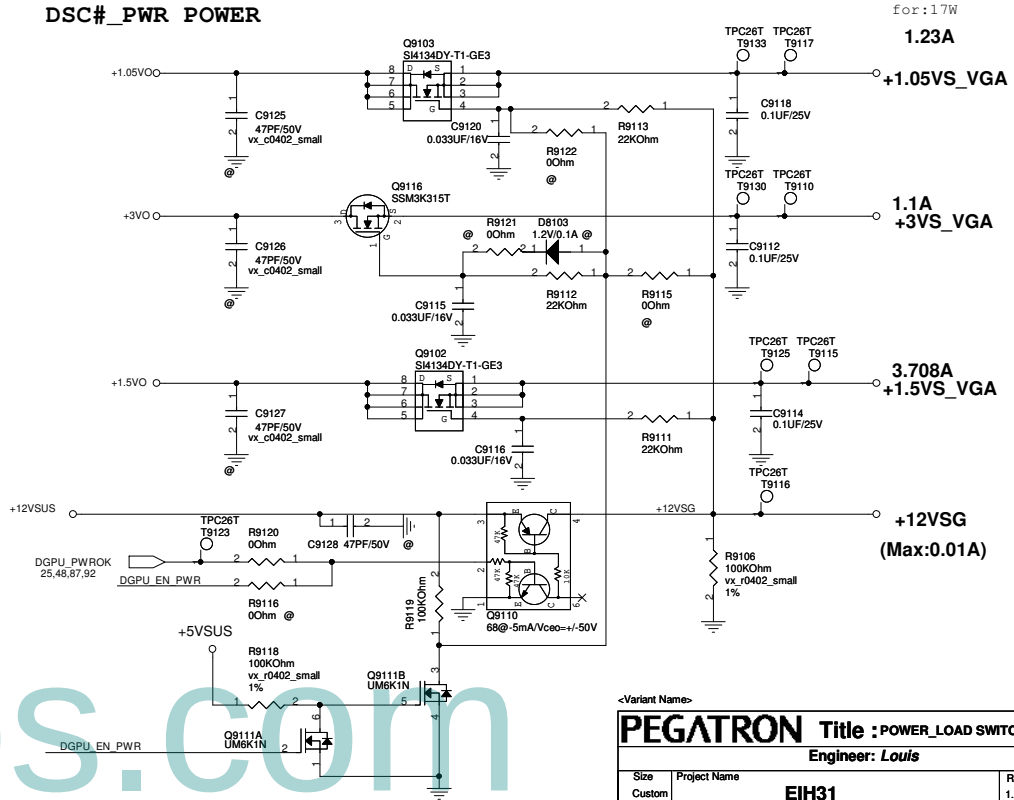


SUSC#_PWR POWER



DSC#_PWR POWER

for:17W



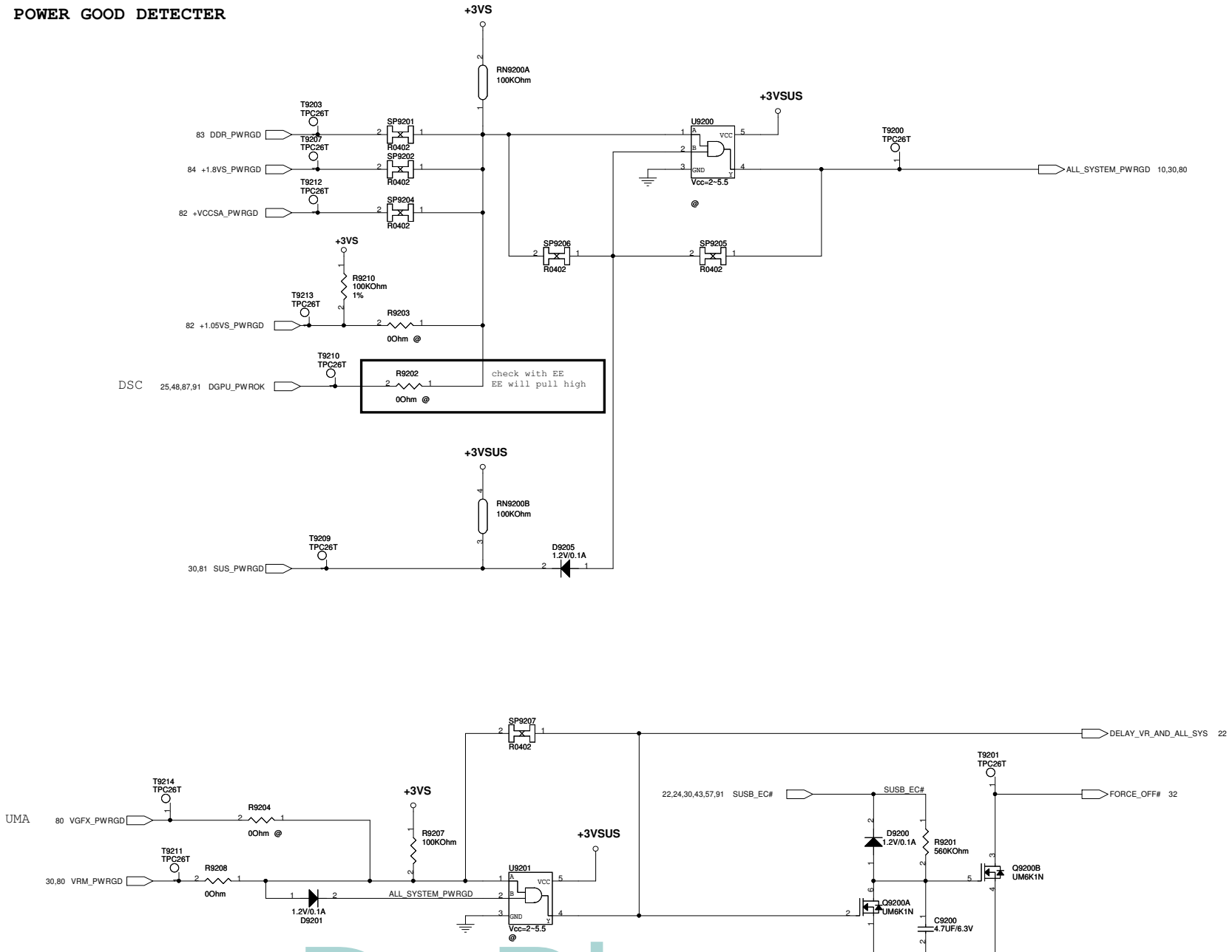
<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH
Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Thursday, January 13, 2011 Sheet 91 of 99

POWER GOOD DETECTER



<Variant Name>

PEGATRON Title :POWER_PROTECT

Engineer: *Louis*

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Thursday, January 13, 2011 Sheet 92 of 99

AC_BAT_SYS → AC_BAT_SYS 45,80,81,82,83,87,88
BAT → BAT 88
BAT_CON → BAT_CON 60,88

+3VA → +3VA 20,27,30,37,56,57,81
+3VAO → +3VAO 20,27,30,37,56,57,81
+5VAO → +5VAO 81
+5VA → +5VA 56,81,88

+5VO → +5VO 81,91
+3VO → +3VO 81,91
+1.05VO → +1.05VO 82,91
+0.75VO → +0.75VO 83
+1.5VO → +1.5VO 83,91
+1.8VO → +1.8VO 84
+0.85VO → +0.85VO 82

+5VSUS → +5VSUS 22,27,81,82,83,84,87,91
+3VSUS → +3VSUS 4,10,22,24,27,28,30,33,34,81,82,84,92
+12VSUS → +12VSUS 22,28,81,91

+5V → +5V 44,52,56,57,84,91
+3V → +3V 4,24,40,43,45,53,55,56,57,61,91
+12V → +12V 40,91
+1.5V → +1.5V 5,7,16,57,83

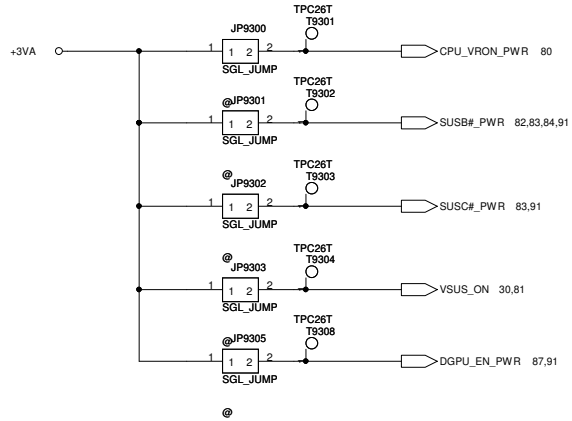
+5VS → +5VS 27,30,31,36,46,48,50,51,56,57,80,91
+3VS → +3VS 4,10,16,17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,43,44,45,46,48,50,51,53,56,57,66,80,91,92
+12VS → +12VS 28,36,45,48,91
+1.05VS → +1.05VS 26,27,57,80,82
+0.75VS → +0.75VS 16,17,57,83
+1.5VS → +1.5VS 26,43,53,57,91
+1.8VS → +1.8VS 7,24,26,57,84
+VCCSA → +VCCSA 7,82

+VCC_CORE → +VCC_CORE 6,57,80
+VGFX_CORE → +VGFX_CORE 7,57,80
+VGA_VCORE → +VGA_VCORE 57,75,87

+1.05VS_VGA → +1.05VS_VGA 57,70,71,72,73,91
+1.5VS_VGA → +1.5VS_VGA 57,71,76,77,91

+3VS_VGA → +3VS_VGA 57,70,72,73,74,91
+12VSG → +12VSG 91

FOR POWER TEST

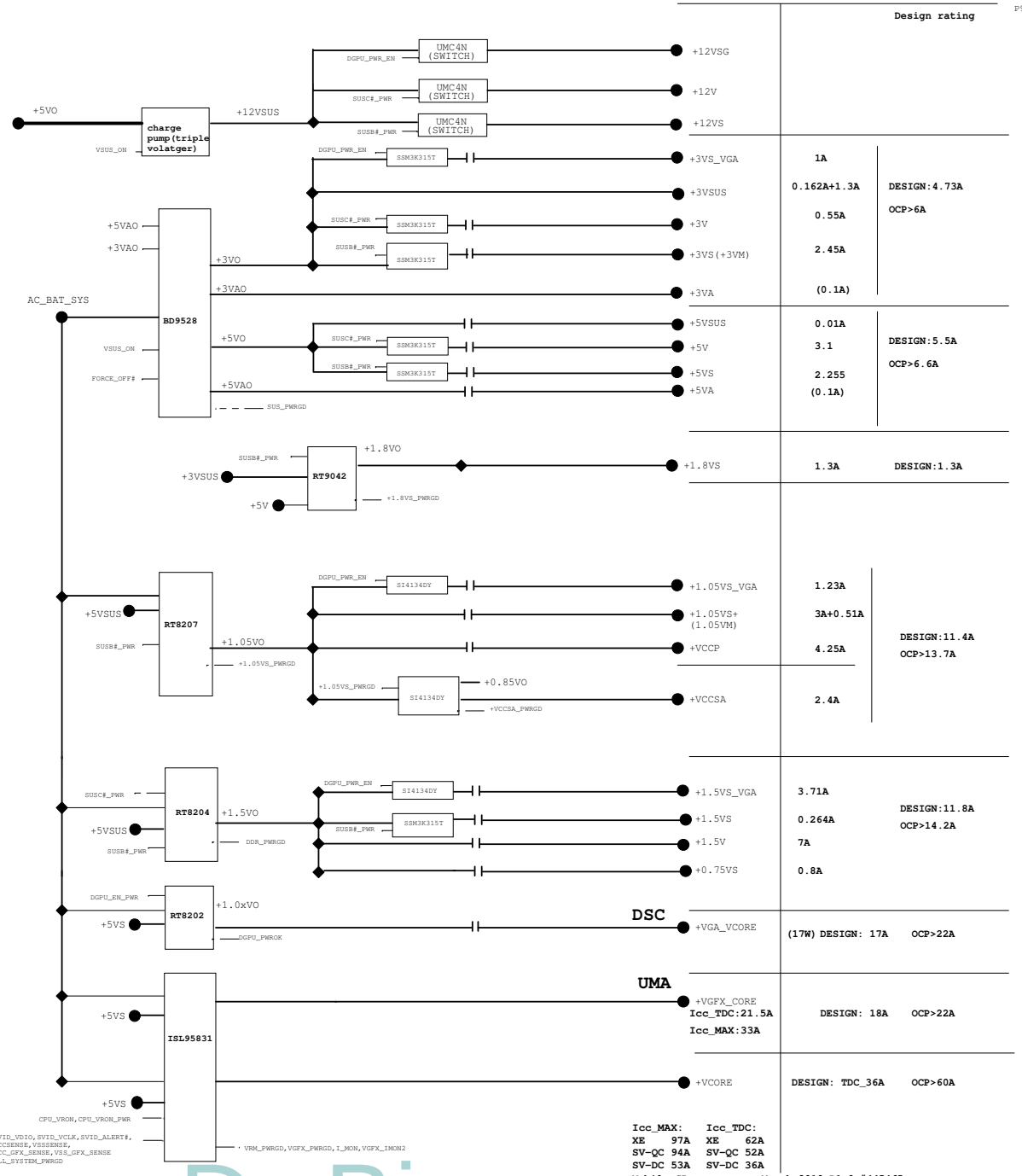


<Variant Name>

PEGATRON Title : POWER_SIGNAL
Engineer: *Louos*

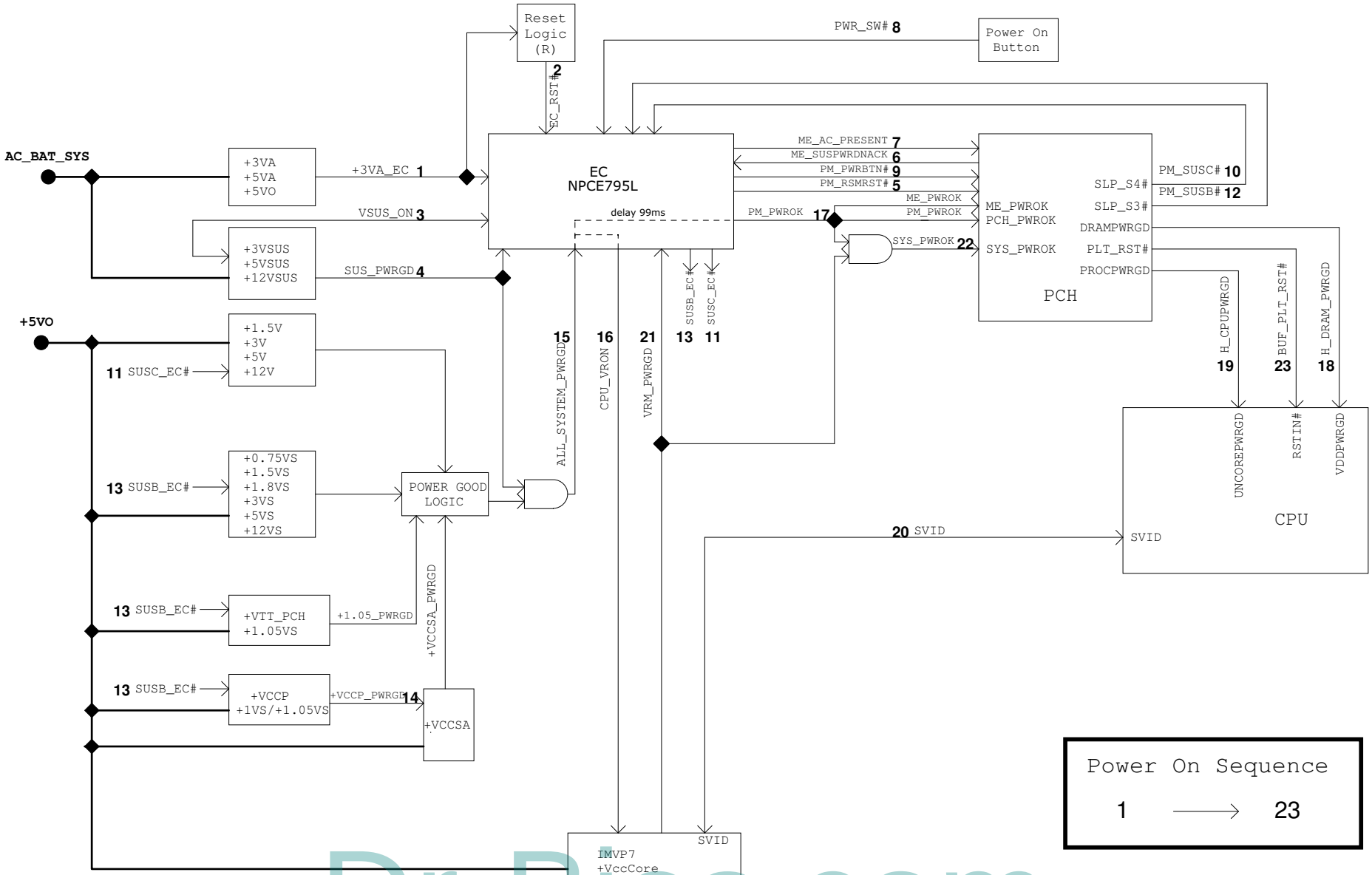
Size	Project Name	Rev
Custom	EIH31	1.1

Date: Thursday, January 13, 2011 Sheet 93 of 99


Design rating
+5VO
charge pump(triple volatger)
+12VSUS
VSUS_ON
DGPU_PWR_EN
UMC4N (SWITCH)
+12VSG
SUSC#_PWR
UMC4N (SWITCH)
+12V
SUSB#_PWR
UMC4N (SWITCH)
+12VS
DGPU_PWR_EN
SSM3K315T
+3VS_VGA
1A
+3VSUS
0.162A+1.3A
DESIGN:4.73A
OCP>6A
SUSC#_PWR
SSM3K315T
+3V
0.55A
SUSB#_PWR
SSM3K315T
+3VS(+3VM)
2.45A
+5VAO
+3VAO
+3VO
+3VAO
+3VA
(0.1A)
AC_BAT_SYS
BD9528
+5VSUS
0.01A
+5VO
SUSC#_PWR
SSM3K315T
+5V
3.1
DESIGN:5.5A
OCP>6.6A
VSUS_ON
FORCE_OFF#
SUSB#_PWR
SSM3K315T
+5VS
2.255
+5VAO
+5VA
(0.1A)
SUS_PWRGD
SUSB#_PWR
RT9042
+1.8VO
+1.8VS
1.3A
DESIGN:1.3A
+3VSUS
+5V
+1.8VS_PWRGD
DGPU_PWR_EN
SI4134DY
+1.05VS_VGA
1.23A
+5VSUS
RT8207
+1.05VS+ (1.05VM)
3A+0.51A
SUSB#_PWR
+1.05VO
+VCCP
4.25A
DESIGN:11.4A
OCP>13.7A
+1.05VS_PWRGD
+1.05VS_PWRGD
SI4134DY
+0.85VO
+VCCSA
2.4A
+VCCSA_PWRGD
SUSC#_PWR
RT8204
+1.5VO
DGPU_PWR_EN
SI4134DY
+1.5VS_VGA
3.71A
DESIGN:11.8A
OCP>14.2A
+5VSUS
SUSB#_PWR
DDR_PWRGD
SUSB#_PWR
SSM3K315T
+1.5VS
0.264A
+1.5V
7A
+0.75VS
0.8A
DGPU_EN_PWR
RT8202
+1.0xVO
DSC
+5VS
+VGA_VCORE
(17W) DESIGN: 17A
OCP>22A
DGPU_PWROK
UMA
+5VS
ISL95831
+VGFX_CORE
Icc_TDC:21.5A
DESIGN: 18A
OCP>22A
Icc_MAX:33A
+5VS
+VCORE
DESIGN: TDC_36A
OCP>60A
CPU_VRON,CPU_VRON_PWR
SVID_VDIO,SVID_VCLK,SVID_ALERT#,
VCCSENSE,VSSSENSE,
VCC_GFX_SENSE,VSS_GFX_SENSE
ALL_SYSTEM_PWRGD
VRM_PWRGD,VGFX_PWRGD,I_MON,VGFX_IMON2
Icc_MAX: Icc_TDC:
XE 97A XE 62A
SV-QC 94A SV-QC 52A
SV-DC 53A SV-DC 36A
Mobile SB processor March 2010 R1.0 #445465

PEGATRON	Title : ****	
BG1\HW1	Engineer: *Ivan Liu*	
Size: A	Project Name: **H36HC**	Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 96 of 99	

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



Power On Sequence

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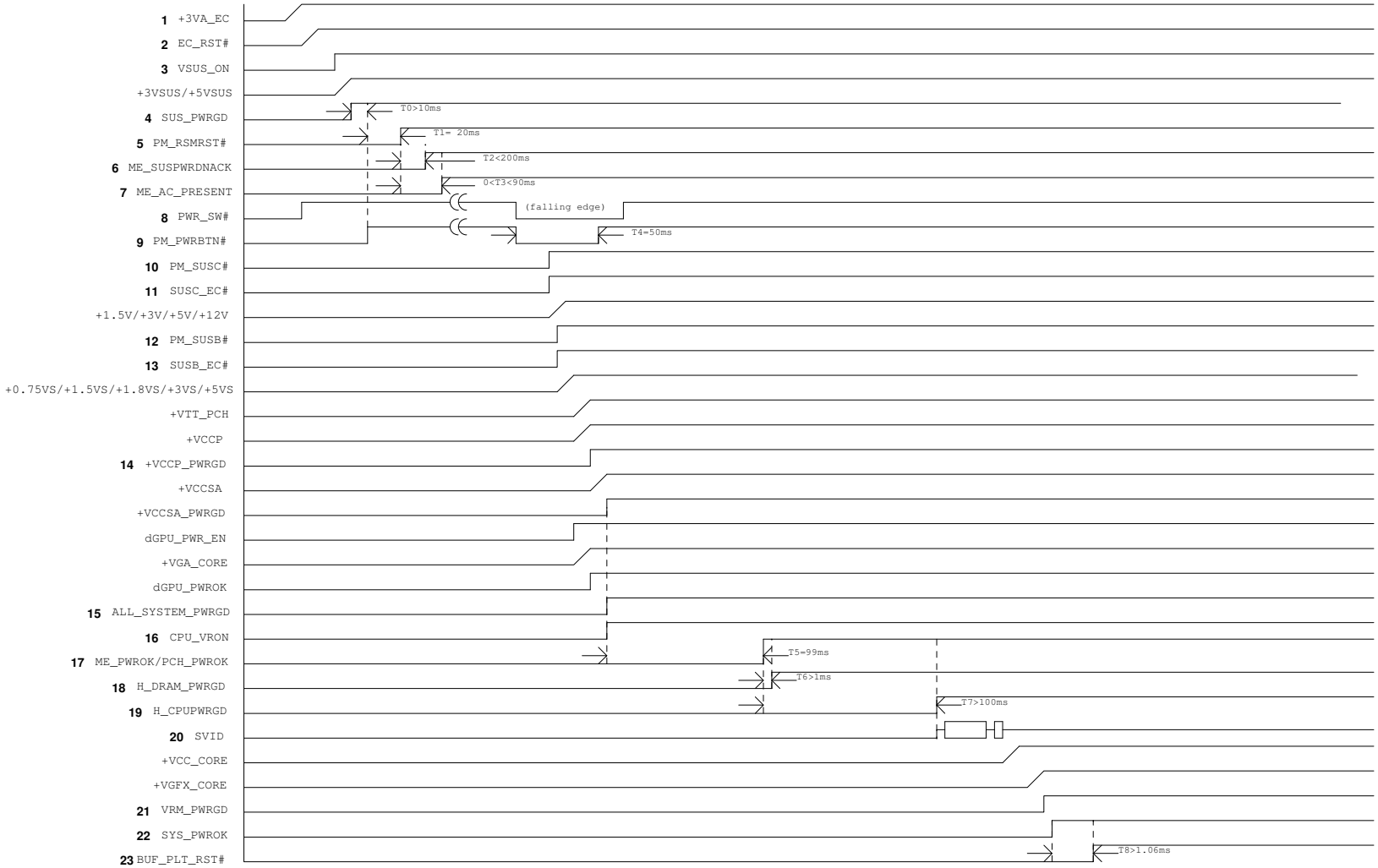
PEGATRON	Title : Power On Sequence		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Thursday, January 13, 2011	Sheet 98 of 99		

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



PEGATRON	Title : Power On Timing		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Tuesday, January 04, 2011	Sheet 99 of 99		