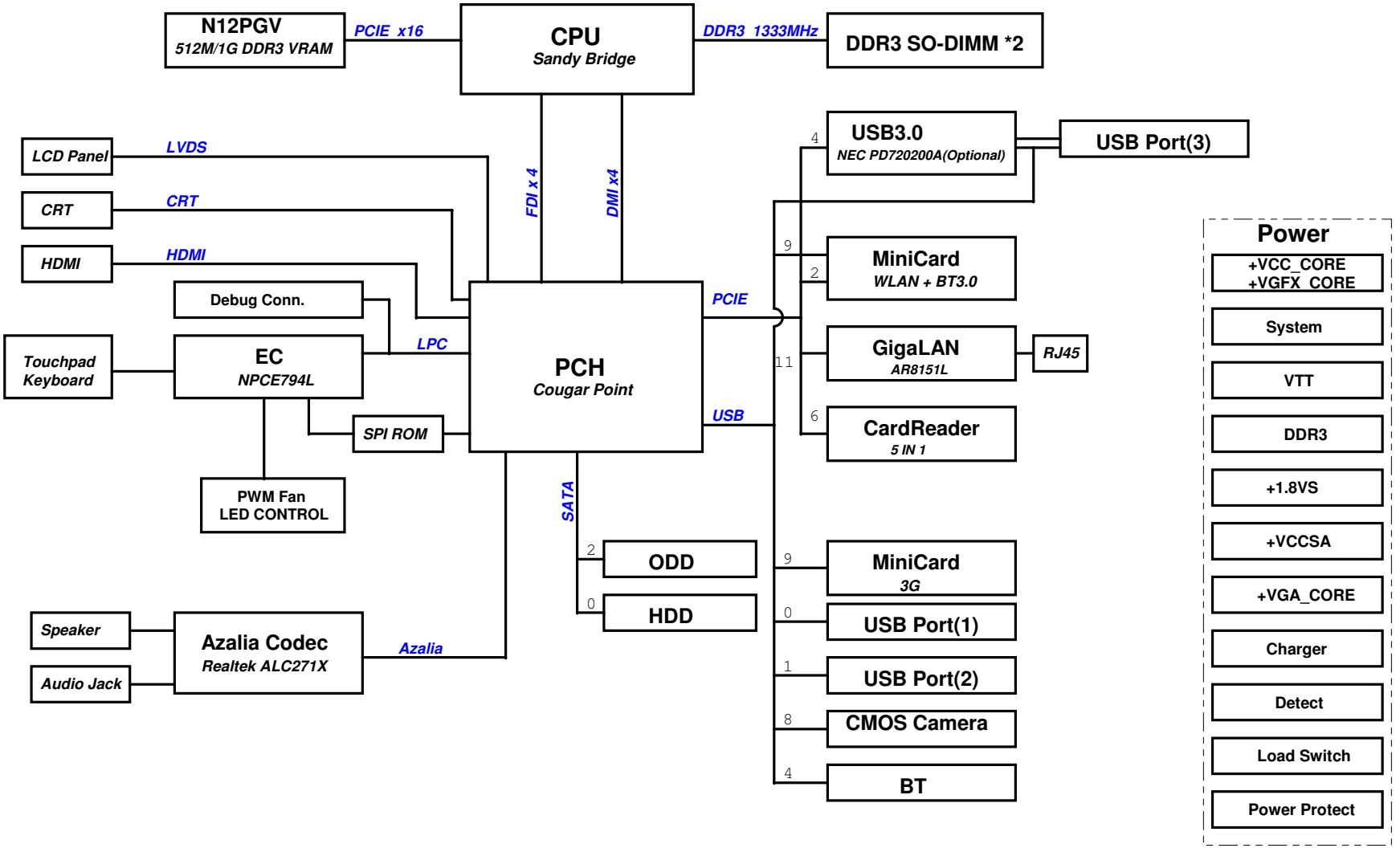
Huron River Platform Rev 1.0

BLOCK DIAGRAM



PEGATRON Title : System Setting
Engineer: JAY TSAI
Size: Custom | Project Name: EIH31 | Rev: 1.3
Date: Friday, December 17, 2010 | Sheet 1 of 99

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)
PlamRest Thermal Sensor (G781)	1001100x (98h)

PCIE 1	CardReader
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

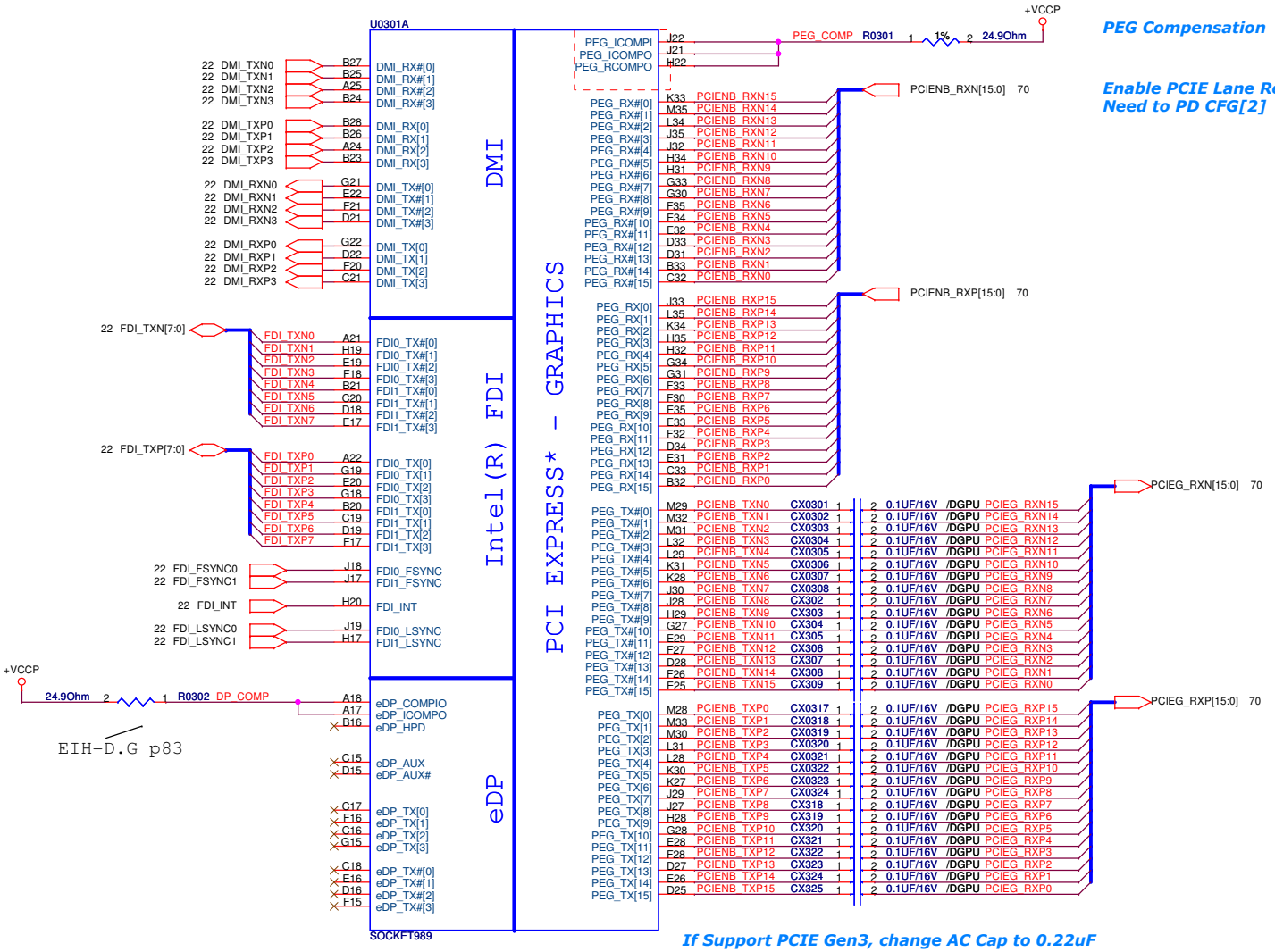
USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	N/A
USB 4	Bluetooth
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	SIM Card
USB 11	3G
USB 12	N/A
USB 13	N/A

PEGATRON Title : System Setting

Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

Date: Friday, December 17, 2010 Sheet 2 of 99



EIH31 : 1201-006D000 MOBILE rPGA CPU SOCKET 988B

PEGATRON	Title :	CPU(1)_DMI,PEG,FDI,
	Engineer:	JAY TSAI
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Friday, December 17, 2010	Sheet 3 of 99	

+1.5V_VCCDDQ +1.5V_VCCDDQ 7
+3VS +3VS 16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92
+3VSUS +3VSUS 22,24,27,28,30,69,81,82,84,92
+VCCP +VCCP 6,25,26,27,30,32,57,82
+3V +3V 24,52,53,55,57,69,91

U0301B

C26 will change to PROC_SELECT#

MISC
24 H_SNB_IVB# C26 SNB_IVB#
T0401 TP_SKTOCC# AN34 SKTOCC#

THERMAL
T0402 TP_CATERR# AL33 CATERR#
25 H_PECI AN33 PECI
+VCCP 75Ohm R0404 H_PROHOT# 44.2Ohm R0403 H_PROHOT# AL32 PROCHOT#
25,32 H_THRMTRIP# SP0401 R0402 H_THRMTRIP# AN32 THERMTRIP#

PWR MANAGEMENT
22 H_PM_SYNC SP0402 H_PM_SYNC AM34 PM_SYNC
10KOhm R0408
25 H_CPUPWRGD SP0403 H_CPUPWRGD AP33 UNCOREPWRGOOD
22 PM_DRAM_PWRGD 130Ohm R0409 VDDPWRGOOD R1.3 V8 SM_DRAMPWROK
R0416
24,30,32,40,53,69,70 BUF_PLT_RST# 1.5KOhm BUF_CPU_RST# AR33 RESET#
R0417 750Ohm

SOCKET989
12V013ASM000

CLOCKS
BCLK A28 BCLK_CPU_P 0Ohm RN0401A CLK_EXP_P 21
BCLK# A27 BCLK_CPU_N 0Ohm RN0401B CLK_EXP_N 21
R0429 1KOhm
DPLL_REF_SSCLK A16 CLK_DP_P_R 0Ohm RN0402A CLK_DP_P 21
DPLL_REF_SSCLK# A15 CLK_DP_N_R 0Ohm RN0402B CLK_DP_N 21
@@
R0430 1KOhm +VCCP

EIH- D.G p83

DDR3 MISC
SM_DRAMRST# R8 CPUDRAMRST# 5
SM_RCOMP[0] AK1 SM_RCOMP_0 R0418 1% 140Ohm
SM_RCOMP[1] A5 SM_RCOMP_1 R0419 1% 25.5Ohm
SM_RCOMP[2] A4 SM_RCOMP_2 R0420 1% 200Ohm

Huron River platform Design Guide Update 440484
SM_RCOMP_1 use 26ohm 1%

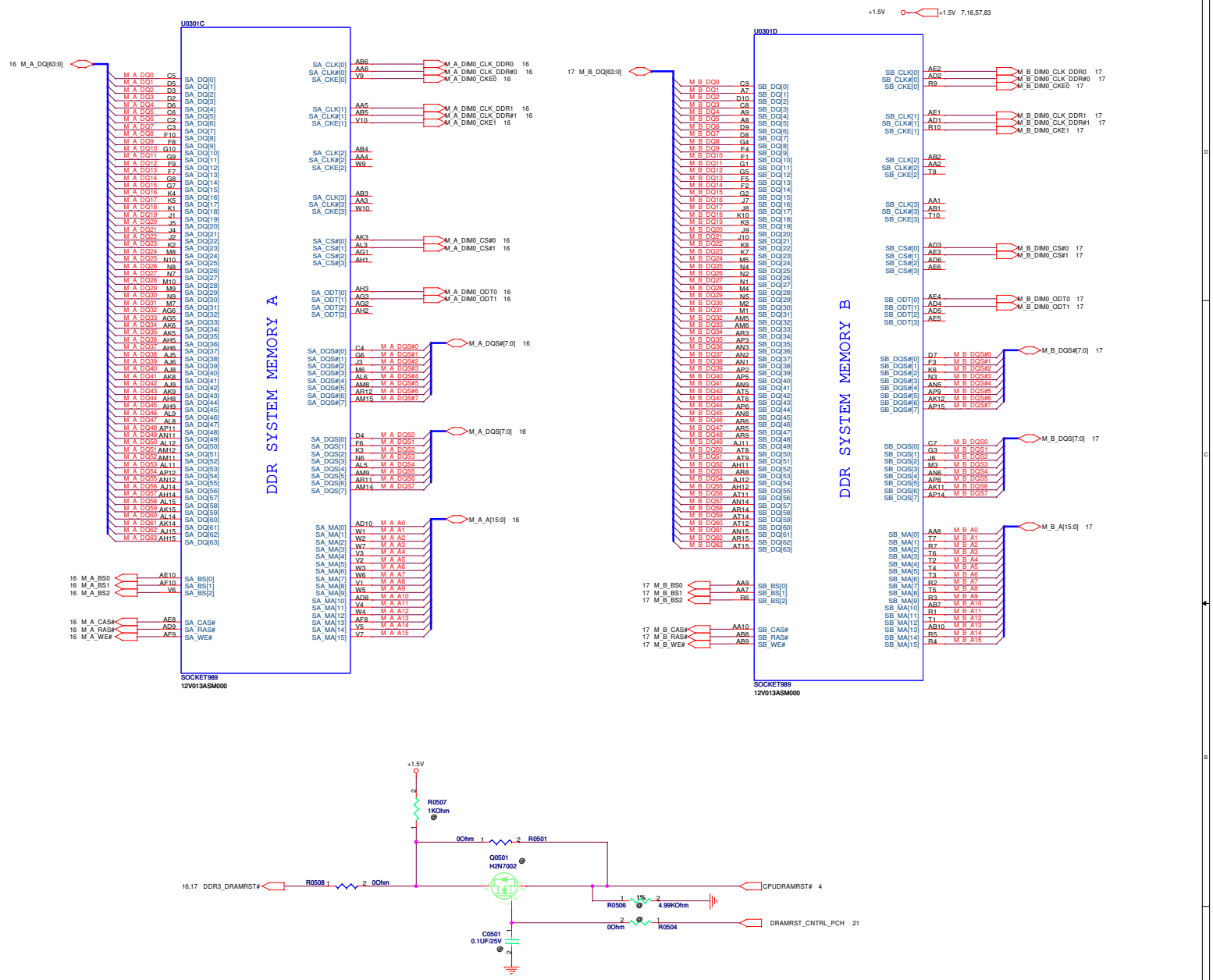
JTAG & BPM
PRDY# AP29 XDP_PRDY# T0403
PREQ# AP27 XDP_PREQ#
TCK AR26 XDP_TCK
TMS AR27 XDP_TMS
TRST# AP30 XDP_TRST#
TDI AR28 XDP_TDI
TDO AP26 XDP_TDO
DBR# AL35 H_DBR#
BPM#[0] AT28 XDP_BPM#0 T0411
BPM#[1] AR29 XDP_BPM#1
BPM#[2] AR30 XDP_BPM#2 T0413
BPM#[3] AT30 XDP_BPM#3 T0414
BPM#[4] AP32 XDP_BPM#4 T0415
BPM#[5] AR31 XDP_BPM#5 T0416
BPM#[6] AT31 XDP_BPM#6 T0417
BPM#[7] AR32 XDP_BPM#7 T0418

+VCCP
XDP_BPM#1 R0428 51Ohm @
XDP_PREQ# R0421 51Ohm
XDP_TDI R0422 51Ohm @
XDP_TDO R0423 51Ohm
XDP_TMS R0424 51Ohm @
H_DBR# R0425 1KOhm @ +3VS
XDP_TCK R0426 51Ohm @
XDP_TRST# R0427 51Ohm

R1.3 Add VR_HOT#
80 VR_HOT# 0Ohm @ R0462
H_PROCHOT#
Q0401 2N7002
THRO_CPU THRO_CPU 30

PM_SYS_PWRGD is the power good for +1.5V_VCCDDQ
+1.5V_VCCDDQ +3VSUS +3V
R0449 200Ohm 1%
1.57 Volt
U0404 Vcc=1.65~5.5 @
R0453 10KOhm @
PM_DRAM_PWRGD 0Ohm R0451
R0452 1.1KOhm 1% @
R0450 1KOhm 1% @
C0405 0.22UF/10V @
Q0403 PMBS3904 @
R0454 24.3KOhm 1% @
+1.5V_VCCDDQ
C0404 0.22UF/10V @
R0455 47KOhm 1% @

PEGATRON Title : CPU(2)_CLK,MISC,JTA
Engineer: JAY TSAI
Size Custom | Project Name EIH31 | Rev 1.0
Date: Friday, December 17, 2010 | Sheet 4 of 99



PEGATRON	Title : CPU(3)_DDR3		
	Engineer: JAY TSAI		
Size: Custom	Project Name: EIH31		Rev: 1.0
Date: Friday, December 17, 2010	Sheet 5 of 99		

POWER

U0301F

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

SOCKET989

12V013ASM000

+VCC_CORE

+VCCP

+VCCP +VCCP 25,26,27,30,32,57,82

+VCC_CORE +VCC_CORE 80

SV-DC
0.8V ~ 1.35V

53A

C0632 22UF/6.3V
C0633 22UF/6.3V @
C0634 22UF/6.3V
C0638 22UF/6.3V
C0639 22UF/6.3V
C0645 22UF/6.3V
C0655 22UF/6.3V
C0658 22UF/6.3V
C0659 22UF/6.3V @
C0662 22UF/6.3V

C0640 10UF/6.3V @
C0657 10UF/6.3V
C0660 10UF/6.3V
C0661 10UF/6.3V
C0647 10UF/6.3V @
C0648 10UF/6.3V
C0649 10UF/6.3V
C0651 10UF/6.3V
C0652 10UF/6.3V
C0653 10UF/6.3V

C0637 10UF/6.3V
C0641 10UF/6.3V @
C0642 10UF/6.3V @
C0650 10UF/6.3V
C0656 10UF/6.3V
C0689 10UF/6.3V
C0690 22UF/6.3V @
C0691 22UF/6.3V @
C0692 22UF/6.3V @
C0693 22UF/6.3V @

ER1.16

Decoupling guide from Intel (POWER + EE)
+VCC_CORE 22uF * 19pcs (3 no stuff)
10uF * 11pcs (1 no stuff)
470uF * 6pcs (2 no stuff)

H36HC 1.3
+VCC_CORE 22uF * 14pcs(6pcs unmount)
10uF * 16pcs (4pcs unmount)
470uF * 2pcs

A14 (EE)
+VCC_CORE 22uF * 10pcs(1PCS unmount)
10uF * 15pcs (4PCS unmount)
470uF total at power page

CE0601 CE0602 A14 at Power side

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

R0612 1% 44.2Ohm → VR_SVID_ALERT# 80

Close to CPU R0611 75Ohm 1%

SP0601 R0402 → VR_SVID_CLK 80

Close to VR R0605 54.9Ohm 1%

Close to CPU R0607 130Ohm 1%

SP0602 R0402 → VR_SVID_DATA 80

Close to VR R0608 130Ohm 1%

8.5A

C0601 10UF/6.3V
C0602 10UF/6.3V
C0603 10UF/6.3V
C0604 10UF/6.3V
C0605 10UF/6.3V
C0606 10UF/6.3V
C0607 10UF/6.3V
C0608 10UF/6.3V
C0609 10UF/6.3V
C0687 10UF/6.3V

C0688 10UF/6.3V
C0610 10UF/6.3V
C0611 10UF/6.3V @
C0644 10UF/6.3V @
C0612 10UF/6.3V
C0613 10UF/6.3V
C0614 10UF/6.3V
C0615 10UF/6.3V
C0616 10UF/6.3V

C0617 22UF/6.3V @
C0618 22UF/6.3V @
C0619 22UF/6.3V @
C0620 22UF/6.3V @
C0621 22UF/6.3V @
C0622 22UF/6.3V @
C0623 22UF/6.3V @
C0624 22UF/6.3V @
C0625 22UF/6.3V @
CE0603 330UF/2V

VCC_SENSE AJ35 VCC_SENSE_R SP0603 1
VSS_SENSE AJ34 VSS_SENSE_R SP0604 1
2 R0402 VCCSENSE
2 R0402 VSSSENSE
VCCSENSE 80
VSSSENSE 80

R0602 100Ohm 1%
R0603 100Ohm 1%

VCCIO_SENSE B10 TP_VCCIO_SENSE T0601
VSSIO_SENSE A10 TP_VSSIO_SENSE T0602

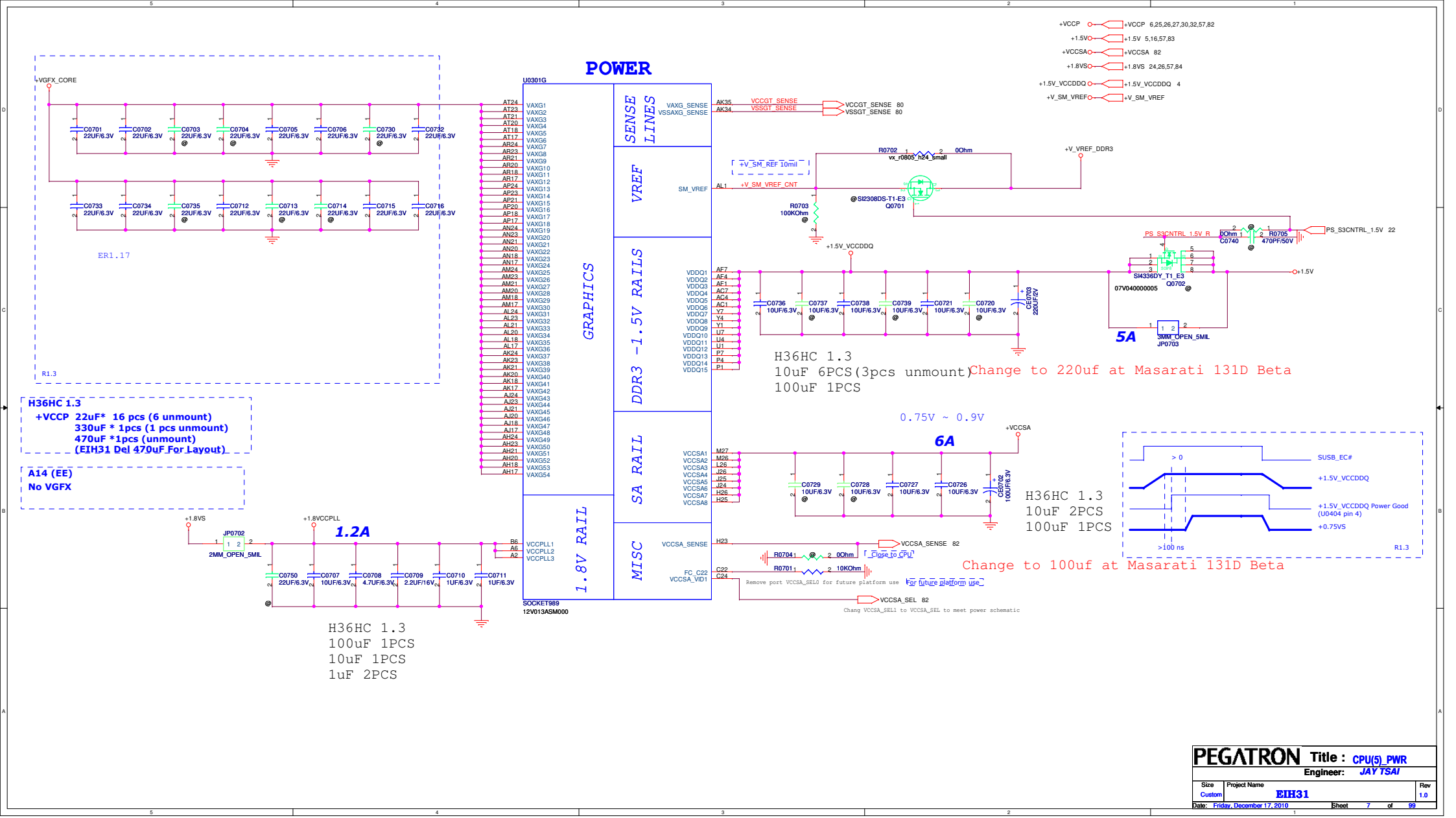
Decoupling guide from Intel (POWER + EE)
+VCCP 22uF * 29pcs
330uF * 6pcs (3 no stuff)

Maserati (EE)
+VCCP 10uF * 19pcs (6pcs no stuff)
22uF* 9 pcs (total unmount)
330 uF *1pcs (unmount)

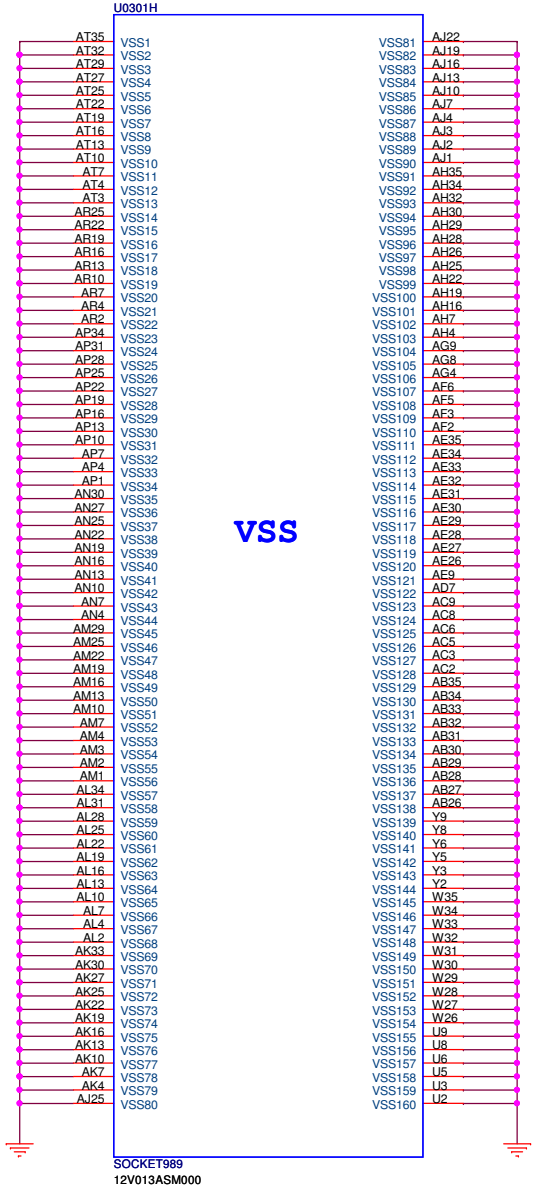
A14 (EE)
+VCCP 10uF * 14pcs(2pcs unmount)

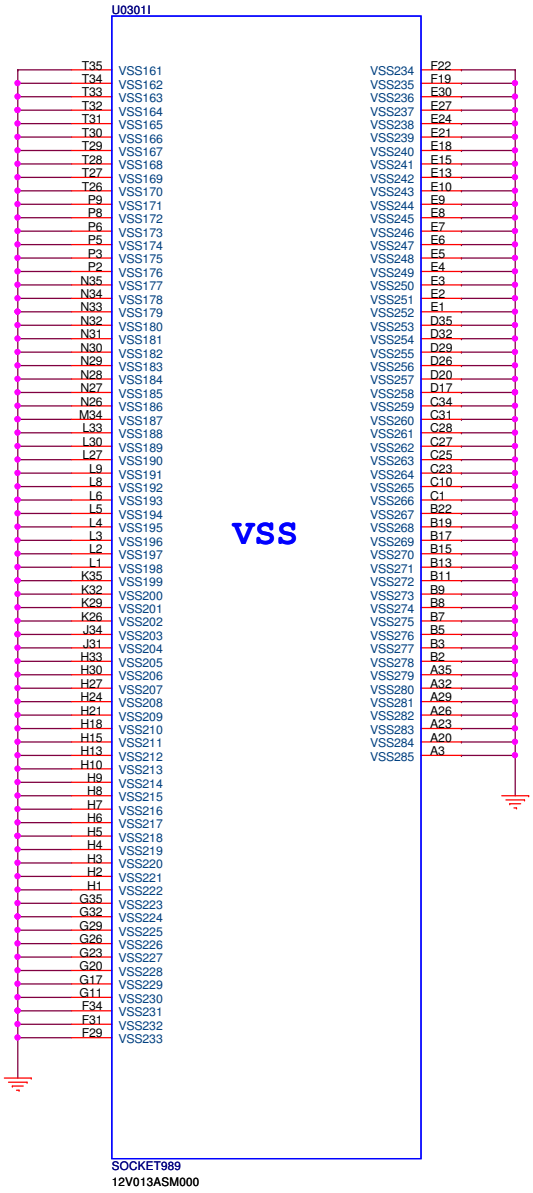
H36HC 1.3
10uF 13PCS

PEGATRON Title : CPU(4)_PWR
Engineer: JAY TSAI
Size: Custom | Project Name: EIH31 | Rev: 1.0
Date: Friday, December 17, 2010 | Sheet 6 of 99



PEGATRON	Title : CPU(5)_PWR	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Friday, December 17, 2010	Sheet 7 of 99	





PEGATRON Title : CPU(6)_CFG,RSVD,GN

Engineer: JAY TSAI

Size	Project Name	Rev
Custom	EIH31	1.0

Date: Friday, December 17, 2010 Sheet 8 of 99

CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection

- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

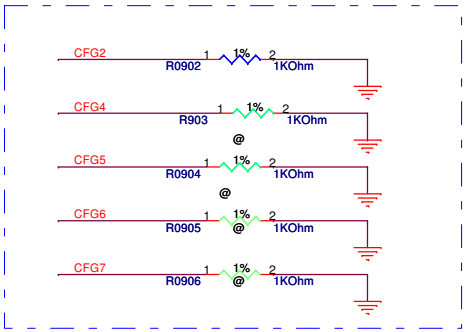
CFG[6:5]: PCI Express Port Bifurcation Straps

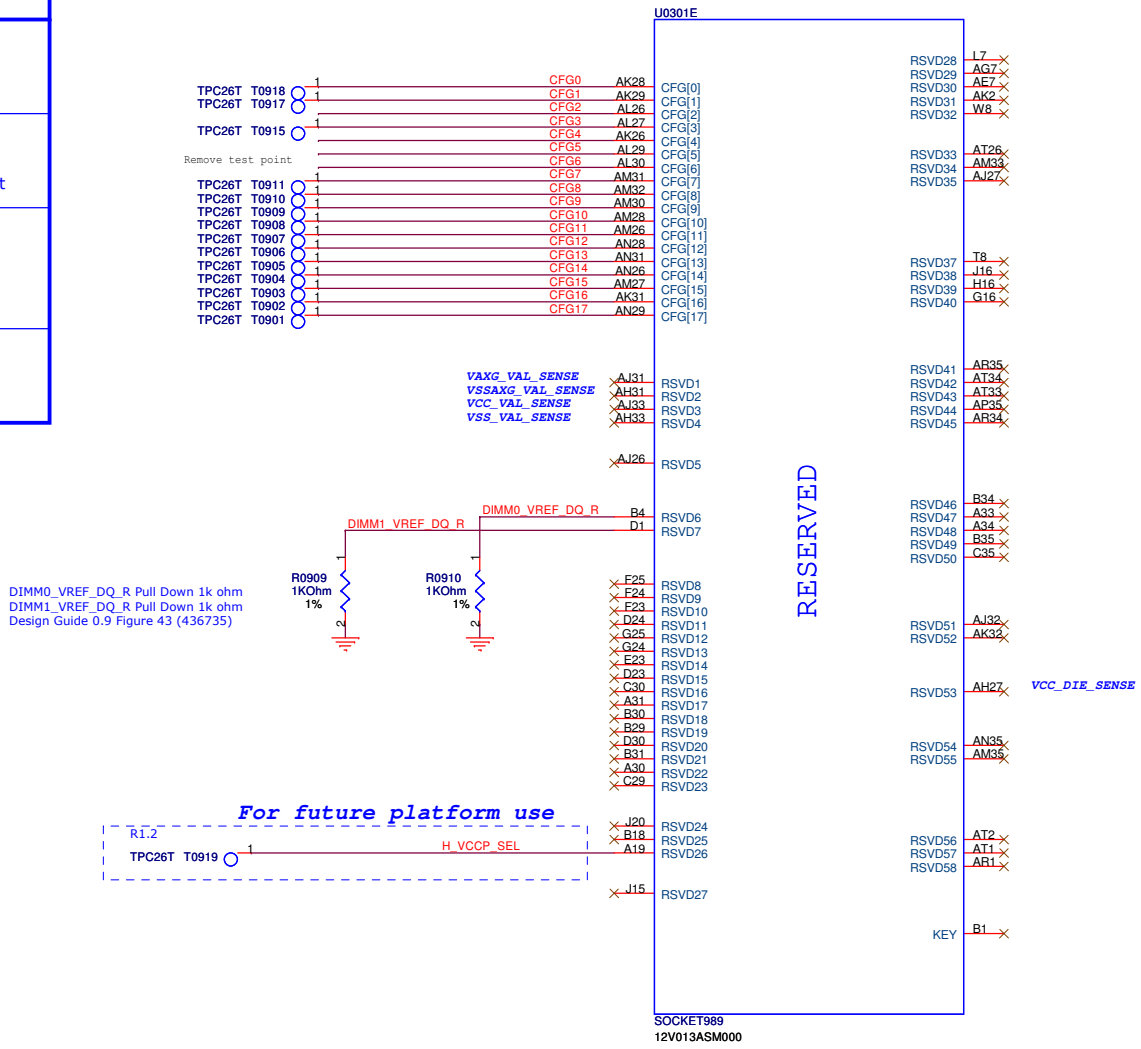
- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training

CFG2 : Check H34 layout request





PEGATRON Title : CPU(7)_CFG,RSVD,GN

Engineer: JAY TSAI

Size	Project Name	Rev
Custom	EIH31	1.0

Date: Friday, December 17, 2010 Sheet 9 of 99

PEGATRON	Title : NB(3)_****	
	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 10 of 99	

PEGATRON	Title : NB(8)_****			
	Engineer: JAY TSAI			
Size: A	Project Name: EIH31			Rev: 1.3
Date: Friday, December 17, 2010		Sheet 15 of 99		

+1.5V +1.5V 5,7,57,83
+1.5V_DDR3 +1.5V_DDR3 17,18
+0.75VS +0.75VS 17,57,83
+3VS +3VS 4,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92
+V_VREF_DDR3 +V_VREF_DDR3 7,17,18,83

5 M_A_A[15:0]
M_A_DQ[63:0] 5

J1601A
DDR3_DIMM_204P

M_A_A0 98 M_A_A1 97 M_A_A2 96 M_A_A3 95 M_A_A4 92 M_A_A5 91 M_A_A6 90 M_A_A7 86 M_A_A8 89 M_A_A9 85 M_A_A10 107 M_A_A11 84 M_A_A12 83 M_A_A13 119 M_A_A14 80 M_A_A15 78

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15

0 1

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

5 M_A_DIM0_CLK_DDR1 102 M_A_DIM0_CLK_DDR#1 104 M_A_DIM0_CLK_DDR0 101 M_A_DIM0_CLK_DDR#0 103

CK1 CK1# CK0 CK0#

5 M_A_DIM0_CS#1 121 5 M_A_DIM0_CS#0 114

S1# S0#

2

5 M_A_DIM0_ODT1 120 5 M_A_DIM0_ODT0 116

ODT1 ODT0

5 M_A_WE# 113 5 M_A_RAS# 110 5 M_A_CAS# 115

WE# RAS# CAS#

3

5 M_A_BS2 79 5 M_A_BS1 108 5 M_A_BS0 109

BA2 BA1 BA0

5 M_A_DIM0_CKE1 74 5 M_A_DIM0_CKE0 73

CKE1 CKE0

4

SA1 SA0

SP1605 SP1606 201 197

SMBus Slave Address: A0H

Follow B53:take care if can't boot or S3 issue

5 M_A_DQS[7:0] 5 M_A_DQS#[7:0]

M_A_DQS7 188 M_A_DQS#7 186 M_A_DQS6 171 M_A_DQS#6 169 M_A_DQS5 154 M_A_DQS#5 152 M_A_DQS4 137 M_A_DQS#4 135 M_A_DQS3 64 M_A_DQS#3 62 M_A_DQS2 47 M_A_DQS#2 45 M_A_DQS1 29 M_A_DQS#1 27 M_A_DQS0 12 M_A_DQS#0 10

DQS7 DQS#7 DQS6 DQS#6 DQS5 DQS#5 DQS4 DQS#4 DQS3 DQS#3 DQS2 DQS#2 DQS1 DQS#1 DQS0 DQS#0

5 6

M_A_DM7 187 M_A_DM6 170 M_A_DM5 153 M_A_DM4 136 M_A_DM3 63 M_A_DM2 46 M_A_DM1 28 M_A_DM0 11

DM7 DM6 DM5 DM4 DM3 DM2 DM1 DM0

7

DM should connect to GND directly
Design Guide 0.9 p86 (436735)

17,28,53 SMB_CLK_S SP1601 SMB_CLK_S_CHA 202
17,28,53 SMB_DAT_S SP1602 SMB_DAT_S_CHA 200

SCL SDA

RESET# 30 DDR3_DRAMRST# 5,17

PLACE CLOSE TO SODIMM

M_A_DIM0_CLK_DDR0 C1621 10PF/50V @ 1% R1603 150Ohm @ M_A_DIM0_CLK_DDR#0
M_A_DIM0_CLK_DDR1 C1626 10PF/50V @ 1% R1604 150Ohm @ M_A_DIM0_CLK_DDR#1

H:4.0mm

+1.5V_DDR3
C1605 0.1UF/10V C1606 0.1UF/10V
C1607 0.1UF/10V C1608 0.1UF/10V

Layout Note: Place these caps near SO DIMM 0

J1601B

VDD1 VDD3 VDD5 VDD7 VDD9 VDD11 VDD13 VDD15 VDD17
VDD2 VDD4 VDD6 VDD8 VDD10 VDD12 VDD14 VDD16 VDD18

75 81 87 93 99 105 111 117 123
76 82 88 94 100 106 112 118 124

VSS1 VSS3 VSS5 VSS7 VSS9 VSS11 VSS13 VSS15 VSS17 VSS19 VSS21 VSS23 VSS25 VSS27 VSS29 VSS31 VSS33 VSS35 VSS37 VSS39 VSS41 VSS43 VSS45 VSS47 VSS49 VSS51
VSS2 VSS4 VSS6 VSS8 VSS10 VSS12 VSS14 VSS16 VSS18 VSS20 VSS22 VSS24 VSS26 VSS28 VSS30 VSS32 VSS34 VSS36 VSS38 VSS40 VSS42 VSS44 VSS46 VSS48 VSS50 VSS52

2 8 13 19 25 31 37 43 48 54 60 65 71 127 133 138 144 150 155 161 167 172 178 184 189 195
3 9 14 20 26 32 38 44 49 55 61 66 72 128 134 139 145 151 156 162 168 173 179 185 190 196

GND1 GND2
207 208

T1601 1 PM_EXTTS#0_DIM_A
Reserve

EVENT# TEST
198 125

NC1 NC2
77 122

NP_NC1 NP_NC2
205 206

VTT1 VTT2
203 204

+0.75VS +3VS

VREFCA VREFDQ
126 1

VDDSPD
199

DDR3_DIMM_204P

+V_VREF_DDR3
C1624 2.2UF/10V @ C1623 0.1UF/10V
C1622 2.2UF/10V @ C1625 0.1UF/10V

C1615 0.1UF/10V
C1614 2.2UF/10V @

+1.5V +1.5V_DDR3 +1.5V_DDR3
JP1601 3MM_OPEN_5MIL
CE1603 220UF/4V

+1.5V_DDR3
Layout Note: Place these caps near SO DIMM 0
C1609 10UF/6.3V C1610 10UF/6.3V C1611 10UF/6.3V @ C1612 10UF/6.3V @ C1613 10UF/6.3V @ C1618 10UF/6.3V @

+0.75VS
C1616 1UF/6.3V C1617 1UF/6.3V C1619 1UF/6.3V @ C1620 1UF/6.3V @

PEGATRON Title : DDR3(1)_SO-DIMM0
Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.0
Date: Friday, December 17, 2010 | Sheet 16 of 99

+1.5V +1.5V 5,7,16,57,83
+1.5V_DDR3 +1.5V_DDR3 16,18
+0.75VS +0.75VS 16,57,83
+3VS +3VS 4,16,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92
+V_VREF_DDR3 +V_VREF_DDR3 7,16,18,83

5 M_B_A[15:0]

J1701A

M_B_A0 98 A0
M_B_A1 97 A1
M_B_A2 96 A2
M_B_A3 95 A3
M_B_A4 92 A4
M_B_A5 91 A5
M_B_A6 90 A6
M_B_A7 86 A7
M_B_A8 89 A8
M_B_A9 85 A9
M_B_A10 107 A10/AP
M_B_A11 84 A11
M_B_A12 83 A12/BC#
M_B_A13 119 A13
M_B_A14 80 A14
M_B_A15 78 A15

5 M_B_DIM0_CLK_DDR1 102 CK1
5 M_B_DIM0_CLK_DDR#1 104 CK1#
5 M_B_DIM0_CLK_DDR0 101 CK0
5 M_B_DIM0_CLK_DDR#0 103 CK0#

5 M_B_DIM0_CS#1 121 S1#
5 M_B_DIM0_CS#0 114 S0#

5 M_B_DIM0_ODT1 120 ODT1
5 M_B_DIM0_ODT0 116 ODT0

5 M_B_WE# 113 WE#
5 M_B_RAS# 110 RAS#
5 M_B_CAS# 115 CAS#

5 M_B_BS2 79 BA2
5 M_B_BS1 108 BA1
5 M_B_BS0 109 BA0

5 M_B_DIM0_CKE1 74 CKE1
5 M_B_DIM0_CKE0 73 CKE0

201 SA1
197 SA0

5 M_B_DQS[7:0]
5 M_B_DQS#[7:0]

M_B_DQS7 188 DQS7
M_B_DQS#7 186 DQS#7
M_B_DQS6 171 DQS6
M_B_DQS#6 169 DQS#6
M_B_DQS5 154 DQS5
M_B_DQS#5 152 DQS#5
M_B_DQS4 137 DQS4
M_B_DQS#4 135 DQS#4
M_B_DQS3 64 DQS3
M_B_DQS#3 62 DQS#3
M_B_DQS2 47 DQS2
M_B_DQS#2 45 DQS#2
M_B_DQS1 29 DQS1
M_B_DQS#1 27 DQS#1
M_B_DQS0 12 DQS0
M_B_DQS#0 10 DQS#0

M_B_DM7 187 DM7
M_B_DM6 170 DM6
M_B_DM5 153 DM5
M_B_DM4 136 DM4
M_B_DM3 63 DM3
M_B_DM2 46 DM2
M_B_DM1 28 DM1
M_B_DM0 11 DM0

16,28,53 SMB_CLK_S SP1701 SMB_CLK_S_CHB 202 SCL
16,28,53 SMB_DAT_S SP1702 SMB_DAT_S_CHB 200 SDA

RESET# 30 DDR3_DRAMRST# 5,16

DDR3_DIMM_204P
12V02GISM000

M_B_DQ[63:0] 5

M_B_DQ0 5 DQ0
M_B_DQ1 6 DQ1
M_B_DQ2 15 DQ2
M_B_DQ3 17 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 7 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 18 DQ7
M_B_DQ8 21 DQ8
M_B_DQ9 23 DQ9
M_B_DQ10 33 DQ10
M_B_DQ11 35 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 24 DQ13
M_B_DQ14 34 DQ14
M_B_DQ15 36 DQ15
M_B_DQ16 39 DQ16
M_B_DQ17 41 DQ17
M_B_DQ18 51 DQ18
M_B_DQ19 53 DQ19
M_B_DQ20 40 DQ20
M_B_DQ21 42 DQ21
M_B_DQ22 50 DQ22
M_B_DQ23 52 DQ23
M_B_DQ24 57 DQ24
M_B_DQ25 59 DQ25
M_B_DQ26 67 DQ26
M_B_DQ27 69 DQ27
M_B_DQ28 56 DQ28
M_B_DQ29 58 DQ29
M_B_DQ30 68 DQ30
M_B_DQ31 70 DQ31
M_B_DQ32 129 DQ32
M_B_DQ33 131 DQ33
M_B_DQ34 141 DQ34
M_B_DQ35 143 DQ35
M_B_DQ36 130 DQ36
M_B_DQ37 132 DQ37
M_B_DQ38 140 DQ38
M_B_DQ39 142 DQ39
M_B_DQ40 147 DQ40
M_B_DQ41 149 DQ41
M_B_DQ42 157 DQ42
M_B_DQ43 159 DQ43
M_B_DQ44 146 DQ44
M_B_DQ45 148 DQ45
M_B_DQ46 158 DQ46
M_B_DQ47 160 DQ47
M_B_DQ48 163 DQ48
M_B_DQ49 165 DQ49
M_B_DQ50 175 DQ50
M_B_DQ51 177 DQ51
M_B_DQ52 164 DQ52
M_B_DQ53 166 DQ53
M_B_DQ54 174 DQ54
M_B_DQ55 176 DQ55
M_B_DQ56 181 DQ56
M_B_DQ57 183 DQ57
M_B_DQ58 191 DQ58
M_B_DQ59 193 DQ59
M_B_DQ60 180 DQ60
M_B_DQ61 182 DQ61
M_B_DQ62 192 DQ62
M_B_DQ63 194 DQ63

0 1 2 3 4 5 6 7

M_B_DIM0_CLK_DDR0 — C1720 10PF/50V @ — 150Ohm R1707 — M_B_DIM0_CLK_DDR#0
M_B_DIM0_CLK_DDR1 — C1721 10PF/50V @ — 150Ohm R1708 — M_B_DIM0_CLK_DDR#1
PLACE CLOSE TO SODIMM

SMBus Slave Address: A4H
+3VS R1709 10KOhm SP1703
take care if can't boot or S3 issue

DM should connect to GND directly
Design Guide 0.9 p86 (436735)

H:8.0mm

+1.5V_DDR3 C1705 0.1UF/10V C1706 0.1UF/10V
Layout Note: Place these caps near SO DIMM 1
+1.5V_DDR3 C1707 0.1UF/10V C1708 0.1UF/10V

J1701B

VDD1 75 VDD2 76
VDD3 81 VDD4 82
VDD5 87 VDD6 88
VDD7 93 VDD8 94
VDD9 99 VDD10 100
VDD11 105 VDD12 106
VDD13 111 VDD14 112
VDD15 117 VDD16 118
VDD17 123 VDD18 124

VSS1 2 VSS2 3
VSS3 8 VSS4 9
VSS5 13 VSS6 14
VSS7 19 VSS8 20
VSS9 25 VSS10 26
VSS11 31 VSS12 32
VSS13 37 VSS14 38
VSS15 43 VSS16 44
VSS17 48 VSS18 49
VSS19 54 VSS20 55
VSS21 60 VSS22 61
VSS23 65 VSS24 66
VSS25 71 VSS26 72
VSS27 127 VSS28 128
VSS29 133 VSS30 134
VSS31 138 VSS32 139
VSS33 144 VSS34 145
VSS35 150 VSS36 151
VSS37 155 VSS38 156
VSS39 161 VSS40 162
VSS41 167 VSS42 168
VSS43 172 VSS44 173
VSS45 178 VSS46 179
VSS47 184 VSS48 185
VSS49 189 VSS50 190
VSS51 195 VSS52 196

GND1 207 GND2 208

T1701 1 PM_EXTTS#0_DIM_B
Reserve
EVENT# 198
TEST 125
NC1 77
NC2 122
NP_NC1 205
NP_NC2 206
VTT1 203 +0.75VS
VTT2 204
VREFCA 126
VREFDQ 1
VDDSPD 199

DDR3_DIMM_204P
12V02GISM000

+V_VREF_DDR3 C1724 2.2UF/10V C1723 0.1UF/10V
+V_VREF_DDR3 C1722 2.2UF/10V C1725 0.1UF/10V
+3VS C1715 0.1UF/10V C1714 2.2UF/10V @

+1.5V_DDR3 CE1703 220UF/4V

+1.5V_DDR3
Layout Note: Place these caps near SO DIMM 1
C1709 10UF/6.3V C1710 10UF/6.3V C1711 10UF/6.3V C1712 10UF/6.3V C1713 10UF/6.3V C1718 10UF/6.3V

+0.75VS C1716 1UF/6.3V C1717 1UF/6.3V C1630 1UF/6.3V C1631 1UF/6.3V

PEGATRON Title : DDR3(2)_SO-DIMM1
Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.0
Date: Friday, December 17, 2010 | Sheet 17 of 99

+1.5V_DDR3 +1.5V_DDR3 16,17

+V_VREF +V_VREF
+V_VREF_DDR3 +V_VREF_DDR3 7,16,17,83
+V_SM_VREF +V_SM_VREF

+3V +3V 4,24,52,53,55,57,69,91
+5VSUS +5VSUS 22,27,55,81,82,83,84,87,91
+5VA +5VA 81,88

DDR3 Vref

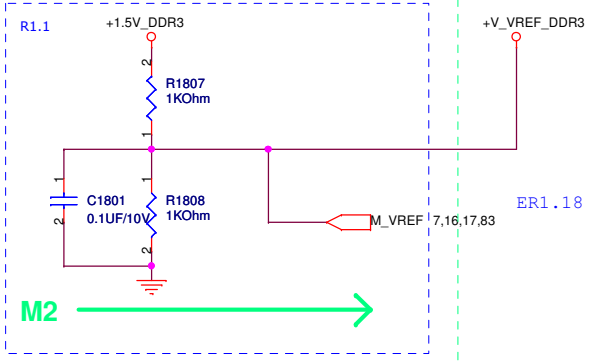
Default M1

R1.1

Power remove M_REF function.

M1: Fixed SO-DIMM VREF_DQ

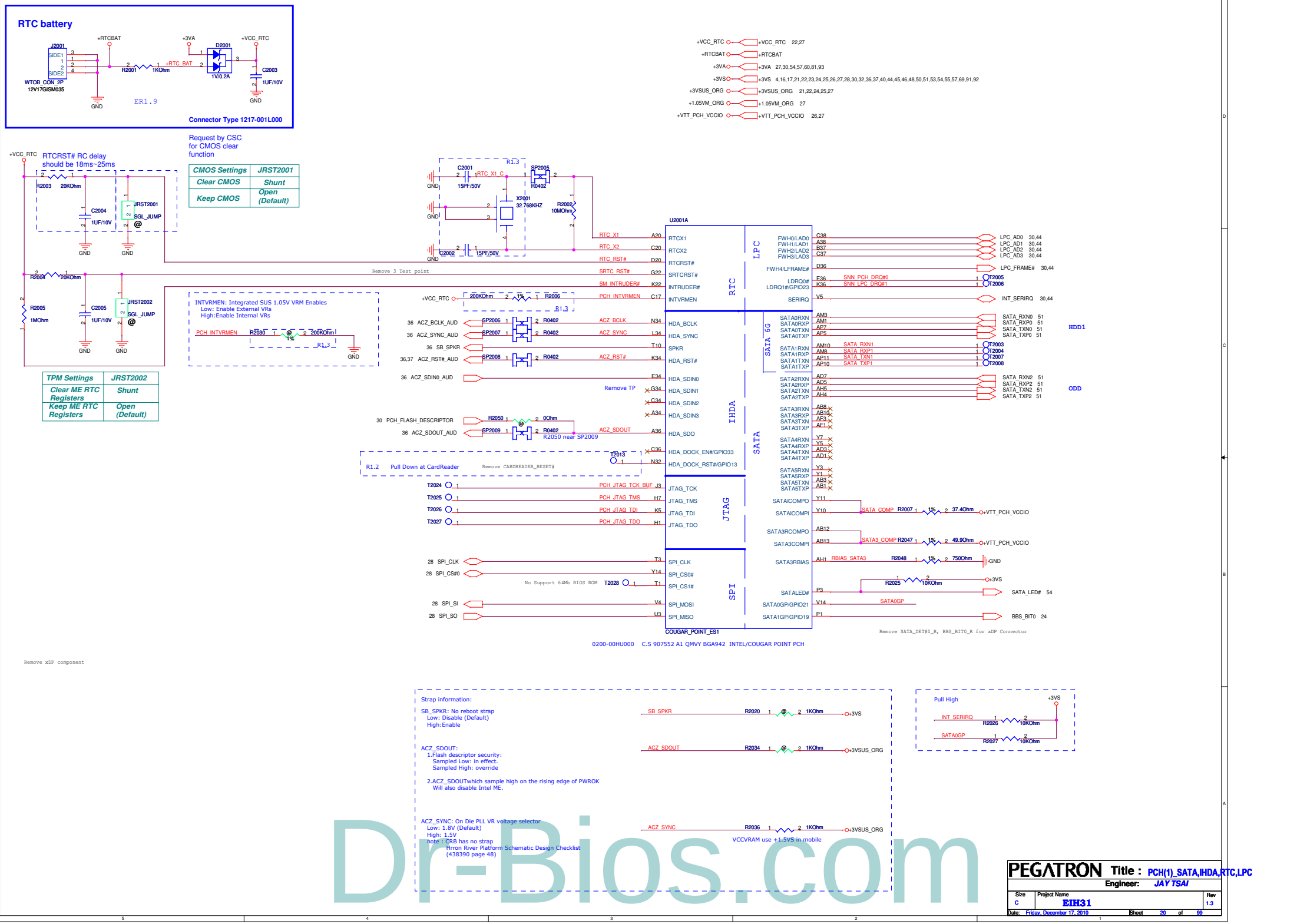
M2: Programmable SO-DIMM VREFDQ on motherboard– New Requirement

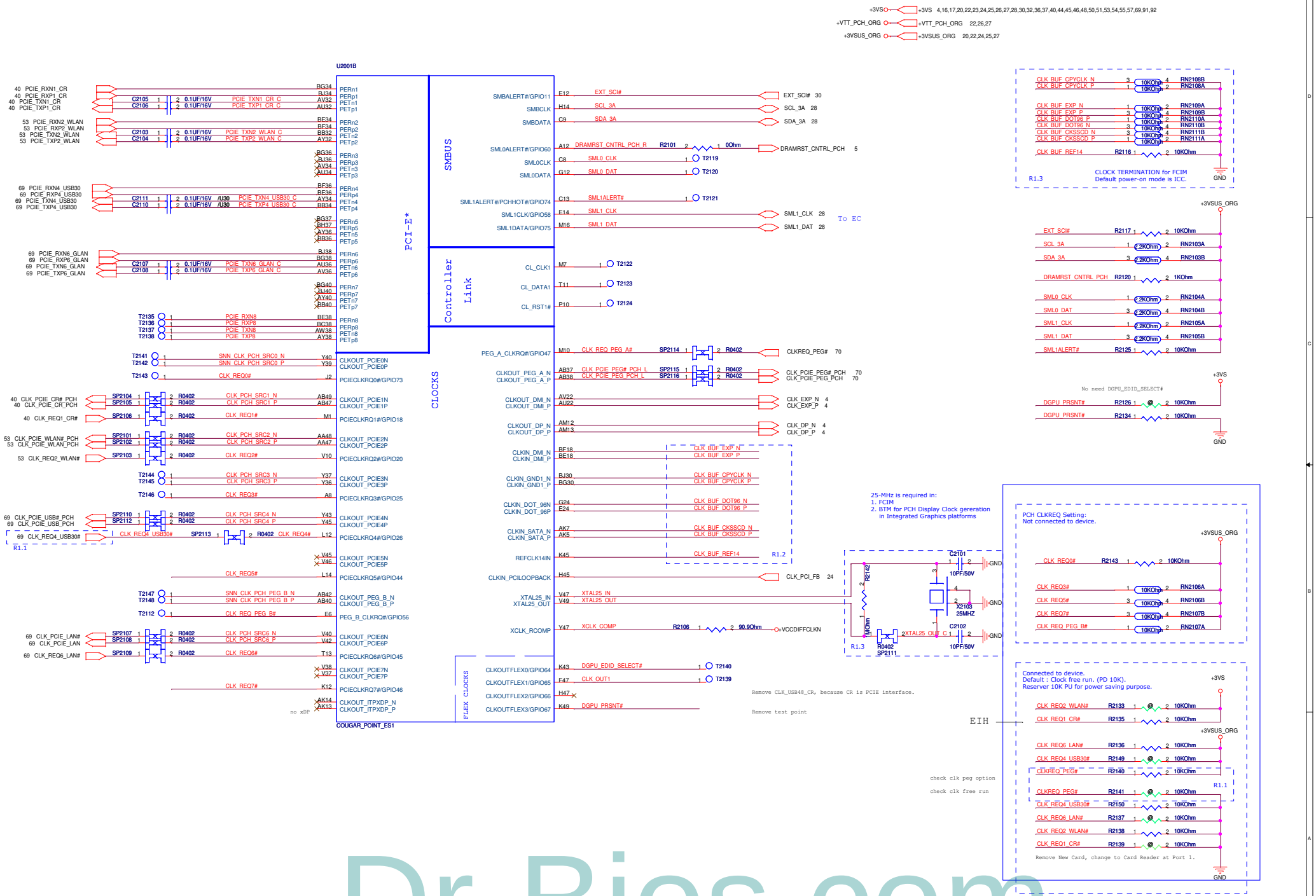


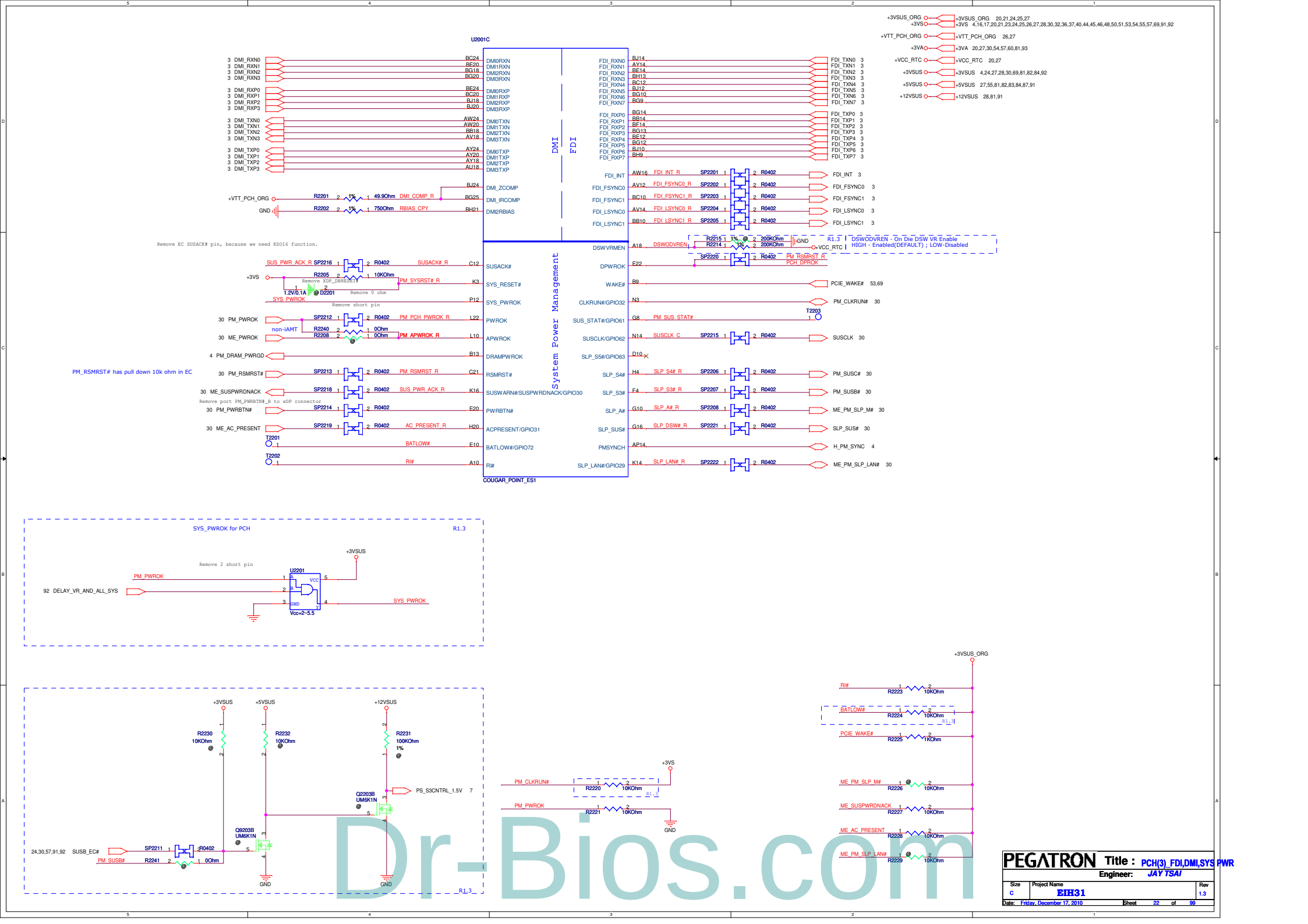
PEGATRON	Title: DDR3(3)_CA/DQ Voltage	
	Engineer: JAY TSAI	
Size: B	Project Name: EIH31	Rev: 1.0
Date: Friday, December 17, 2010	Sheet 18 of 99	

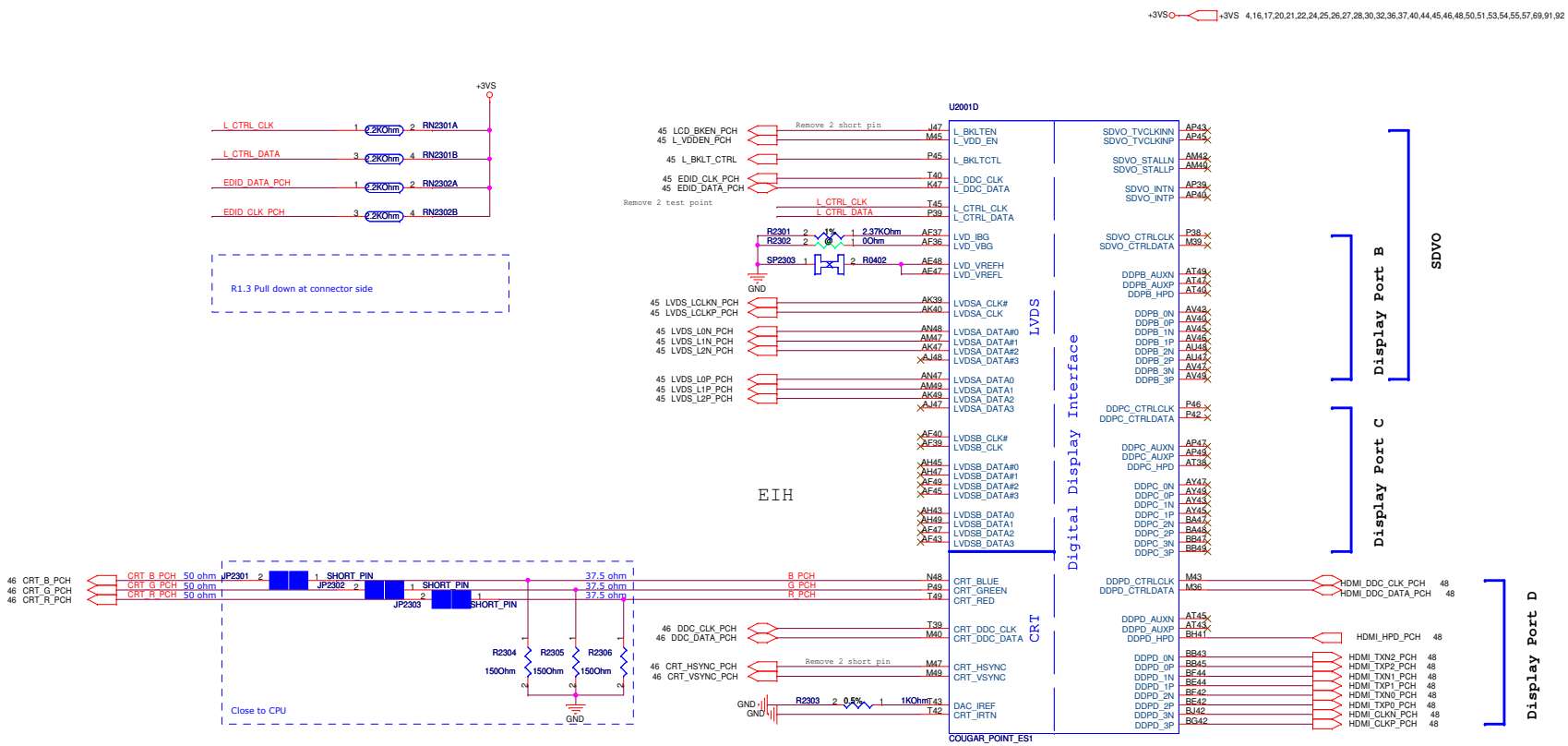
R1.4--2

PEGATRON	Title : VID Controller	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 19 of 99	


RTC battery
+RTCBAT
+3VA
+VCC_RTC
J2001
SIDE1
SIDE2
WTOB_CON_2P
12V17GISM035
R2001
1KOhm
+RTC_BAT
D2001
1V/0.2A
C2003
1UF/10V
GND
ER1.9
Connector Type 1217-001L000
+VCC_RTC +VCC_RTC 22,27
+RTCBAT +RTCBAT
+3VA +3VA 27,30,54,57,60,81,93
+3VS +3VS 4,16,17,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92
+3VSUS_ORG +3VSUS_ORG 21,22,24,25,27
+1.05VM_ORG +1.05VM_ORG 27
+VTT_PCH_VCCIO +VTT_PCH_VCCIO 26,27
Request by CSC for CMOS clear function
CMOS Settings JRST2001
Clear CMOS Shunt
Keep CMOS Open (Default)
RTCRST# RC delay should be 18ms~25ms
R2003 20KOhm
C2004 1UF/10V
JRST2001
SGL_JUMP
R2004 20KOhm
R2005 1MOhm
C2005 1UF/10V
JRST2002
SGL_JUMP
TPM Settings JRST2002
Clear ME RTC Registers Shunt
Keep ME RTC Registers Open (Default)
INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs
PCH_INTVRMEN R2030 200KOhm
C2001 15PF/50V
C2002 15PF/50V
X2001 32.768KHZ
R2002 10MOhm
R1.3
SP2005
R0402
Remove 3 Test point
U2001A
RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC
LPC
FWH0/LAD0 C38
FWH1/LAD1 A38
FWH2/LAD2 B37
FWH3/LAD3 C37
FWH4/LFRAME# D36
LDRQ0# F36
LDRQ1#/GPIO23 K36
SERIRQ V5
LPC_AD0 30,44
LPC_AD1 30,44
LPC_AD2 30,44
LPC_AD3 30,44
LPC_FRAME# 30,44
SNN_PCH_DRQ#0
SNN_LPC_DRQ#1
T2005
T2006
INT_SERIRQ 30,44
200KOhm 1% R2006
36 ACZ_BCLK_AUD SP2006 R0402 ACZ_BCLK N34 HDA_BCLK
36 ACZ_SYNC_AUD SP2007 R0402 ACZ_SYNC L34 HDA_SYNC
36 SB_SPKR T10 SPKR
36,37 ACZ_RST#_AUD SP2008 R0402 ACZ_RST# K34 HDA_RST#
36 ACZ_SDIN0_AUD E34 HDA_SDIN0
Remove TP G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
30 PCH_FLASH_DESCRIPTOR R2050 0Ohm
36 ACZ_SDOUT_AUD SP2009 R0402 ACZ_SDOUT A36 HDA_SDO
R2050 near SP2009
C36 HDA_DOCK_EN#/GPIO33
T2013 N32 HDA_DOCK_RST#/GPIO13
R1.2 Pull Down at CardReader
Remove CARDREADER_RESET#
IHDA
SATA 6G
SATA
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7
SATA0TXP AP5
SATA_RXN0 51
SATA_RXP0 51
SATA_TXN0 51
SATA_TXP0 51
HDD1
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
T2003
T2004
T2007
T2008
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA_RXN2 51
SATA_RXP2 51
SATA_TXN2 51
SATA_TXP2 51
ODD
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11
SATAICOMPI Y10
SATA_COMP R2007 37.4Ohm +VTT_PCH_VCCIO
SATA3RCOMPO AB12
SATA3COMPI AB13
SATA3_COMP R2047 49.9Ohm +VTT_PCH_VCCIO
SATA3RBIAS AH1
RBIAS_SATA3 R2048 750Ohm GND
R2025 10KOhm +3VS
SATALED# P3
SATA_LED# 54
SATA0GP/GPIO21 V14
SATA0GP
SATA1GP/GPIO19 P1
BBS_BIT0 24
Remove SATA_DET#0_R, BBS_BIT0_R for xDP Connector
JTAG
T2024 PCH_JTAG_TCK_BUF J3 JTAG_TCK
T2025 PCH_JTAG_TMS H7 JTAG_TMS
T2026 PCH_JTAG_TDI K5 JTAG_TDI
T2027 PCH_JTAG_TDO H1 JTAG_TDO
SPI
28 SPI_CLK T3 SPI_CLK
28 SPI_CS#0 Y14 SPI_CS0#
No Support 64Mb BIOS ROM T2028 T1 SPI_CS1#
28 SPI_SI V4 SPI_MOSI
28 SPI_SO U3 SPI_MISO
COUGAR_POINT_ES1
0200-00HU000 C.S 907552 A1 QMVY BGA942 INTEL/COUGAR POINT PCH
Remove xDP component
Strap information:
SB_SPKR: No reboot strap
Low: Disable (Default)
High:Enable
SB_SPKR R2020 1KOhm +3VS
ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.ACZ_SDOUTwhich sample high on the rising edge of PWROK
Will also disable Intel ME.
ACZ_SDOUT R2034 1KOhm +3VSUS_ORG
ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : ER8 has no strap
Hrron River Platform Schematic Design Checklist
(438390 page 48)
ACZ_SYNC R2036 1KOhm +3VSUS_ORG
VCCVRAM use +1.5VS in mobile
Pull High
+3VS
INT_SERIRQ R2026 10KOhm
SATA0GP R2027 10KOhm
PEGATRON
Title : PCH(1)_SATA,IHDA,RTC,LPC
Engineer: JAY TSAI
Size C
Project Name EIH31
Rev 1.3
Date: Friday, December 17, 2010
Sheet 20 of 99


+3VS 4,16,17,20,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92
+VTT_PCH_ORG 22,26,27
+3VSUS_ORG 20,22,24,25,27
U2001B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGAR_POINT_ES1
To EC
CLOCK TERMINATION for FCIM
Default power-on mode is ICC.
R1.3
No need DGPU_EDID_SELECT#
25-MHz is required in:
1. FCIM
2. BTM for PCH Display Clock gereration
in Integrated Graphics platforms
PCH CLKREQ Setting:
Not connected to device.
Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.
Remove New Card, change to Card Reader at Port 1.
check clk peg option
check clk free run
Remove CLK_USB48_CR, because CR is PCIE interface.
Remove test point
EIH
no xDP
PEGATRON
Title : PCH(2)_PCIE,CLK,SMB,PEG
Engineer: JAY TSAI
Size C
Project Name EIH31
Rev 1.3
Date: Friday, December 17, 2010
Sheet 21 of 99


U2001C
DMI
FDI
System Power Management
COUGAR_POINT_ES1
Remove EC SUSACK# pin, because we need KS016 function.
PM_RSMRST# has pull down 10k ohm in EC
SYS_PWROK for PCH
R1.3
Remove 2 short pin
Vcc=2~5.5
Remove short pin
Remove XDP_DBRESET#
Remove 0 ohm
Remove port PM_PWRBTN#_R to xDP connector
non-iAMT
DSWODVREN - On Die DSW VR Enable
HIGH - Enabled(DEFAULT) ; LOW-Disabled
+3VSUS_ORG 20,21,24,25,27
+3VS 4,16,17,20,21,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92
+VTT_PCH_ORG 26,27
+3VA 20,27,30,54,57,60,81,93
+VCC_RTC 20,27
+3VSUS 4,24,27,28,30,69,81,82,84,92
+5VSUS 27,55,81,82,83,84,87,91
+12VSUS 28,81,91
PEGATRON
Title : PCH(3)_FDI,DMI,SYS PWR
Engineer: JAY TSAI
Size C
Project Name EIH31
Rev 1.3
Date: Friday, December 17, 2010
Sheet 22 of 99



CRT Disable: (For discrete graphic)

1. NC:
   - CRT_RED,CRT_GREEN,CRT_BLUE
   - CRT_HSYCN,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
   - DAC_IREF
3. Connected to GND:
   - CRT_ITRN
4. Connect to +V3.3:
   - VCCADAC

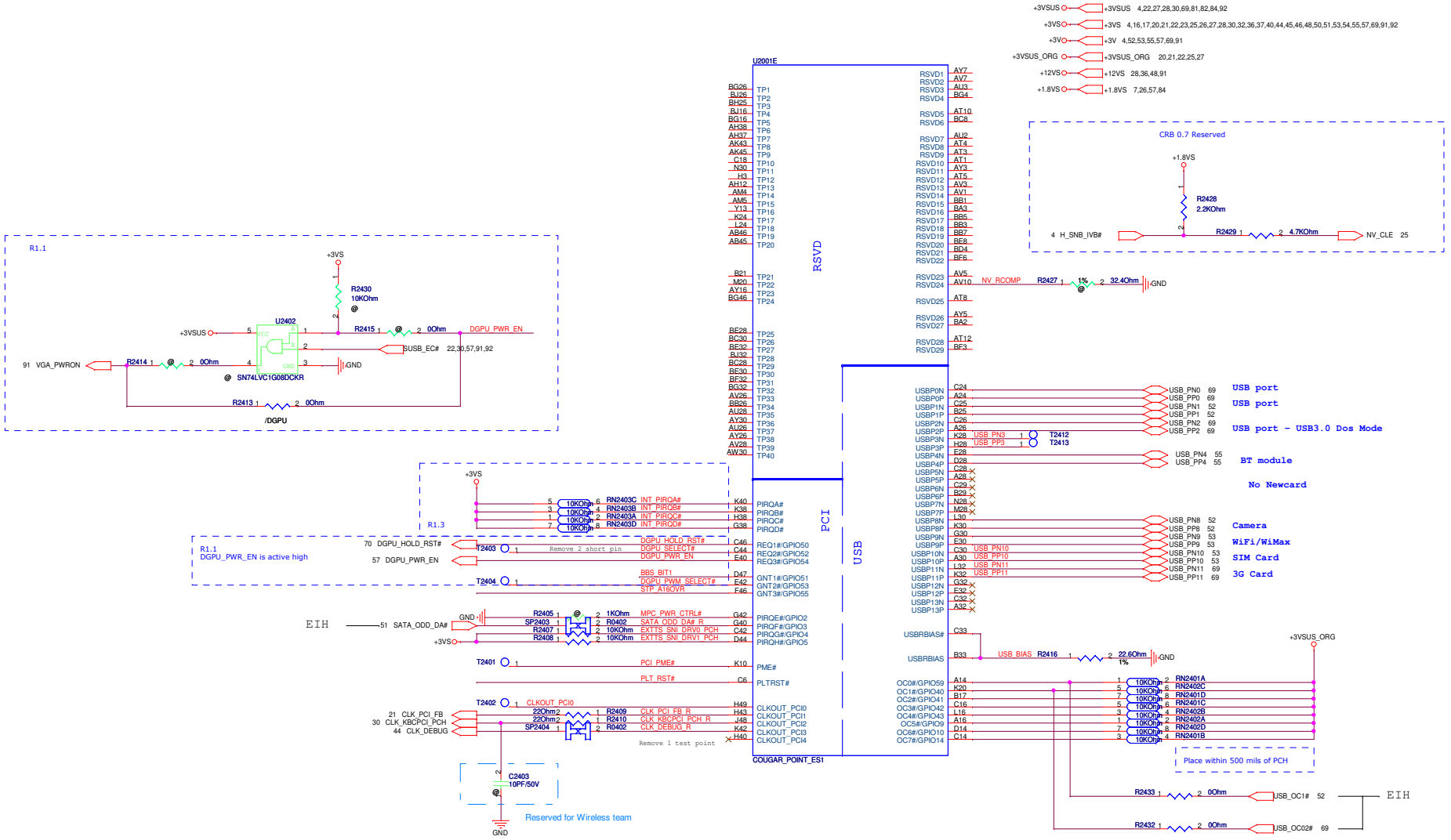
DisPlay Port Disable: (For discrete graphic)

1. NC:
   - ALL

LVDS Disable: (For discrete graphic)

1. NC:
   - LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
   - LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
   - LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
   - L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
   - LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
   - VccALVDS,VccTX_LVDS

PEGATRON	Title : PCH(4)_DP,LVDS,CRT	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 23 of 99	



BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI **(PCH)**

Sampled on rising edge of PWROK.

20 BBS_BIT0 — BBS_BIT0 R2417 @ 1KOhm — BBS_BIT1 R2418 1KOhm — GND

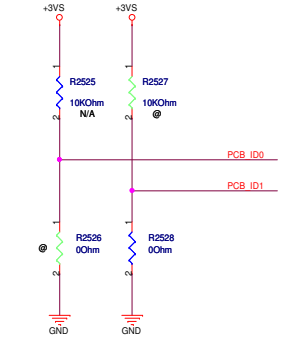
STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default

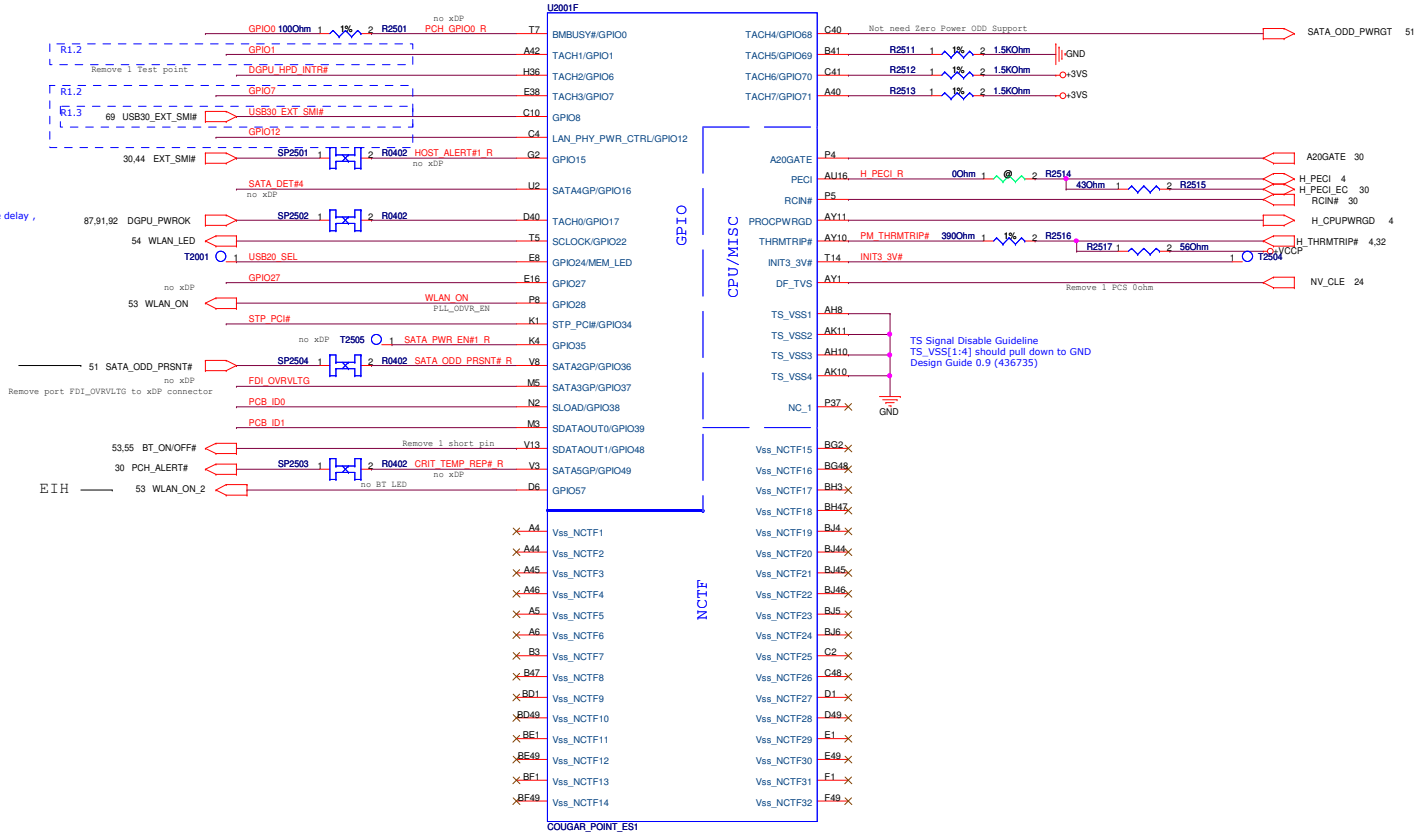
STP_A16OVR R2419 @ 1KOhm — GND

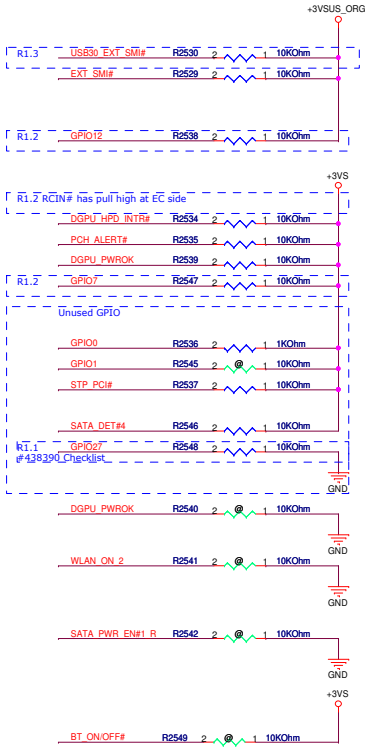
PEGATRON	Title : PCH(5)_PCI,NVRAM,USB		
	Engineer: JAY TSAI		
Size C	Project Name EIH31		Rev 1.3
Date: Friday, December 17, 2010	Sheet 24	of 99	

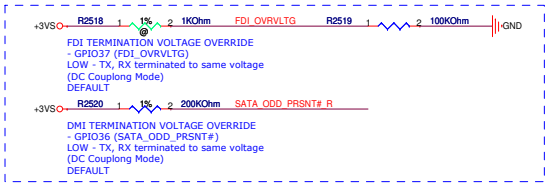
	PCB_ID1	PCB_ID0
SR	L	L
ER	L	H
PR		
MP		

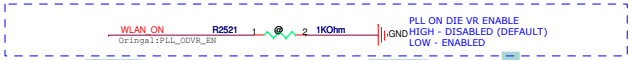


DGPU_PWROK has 100 ms software delay , no hardware delay requirement

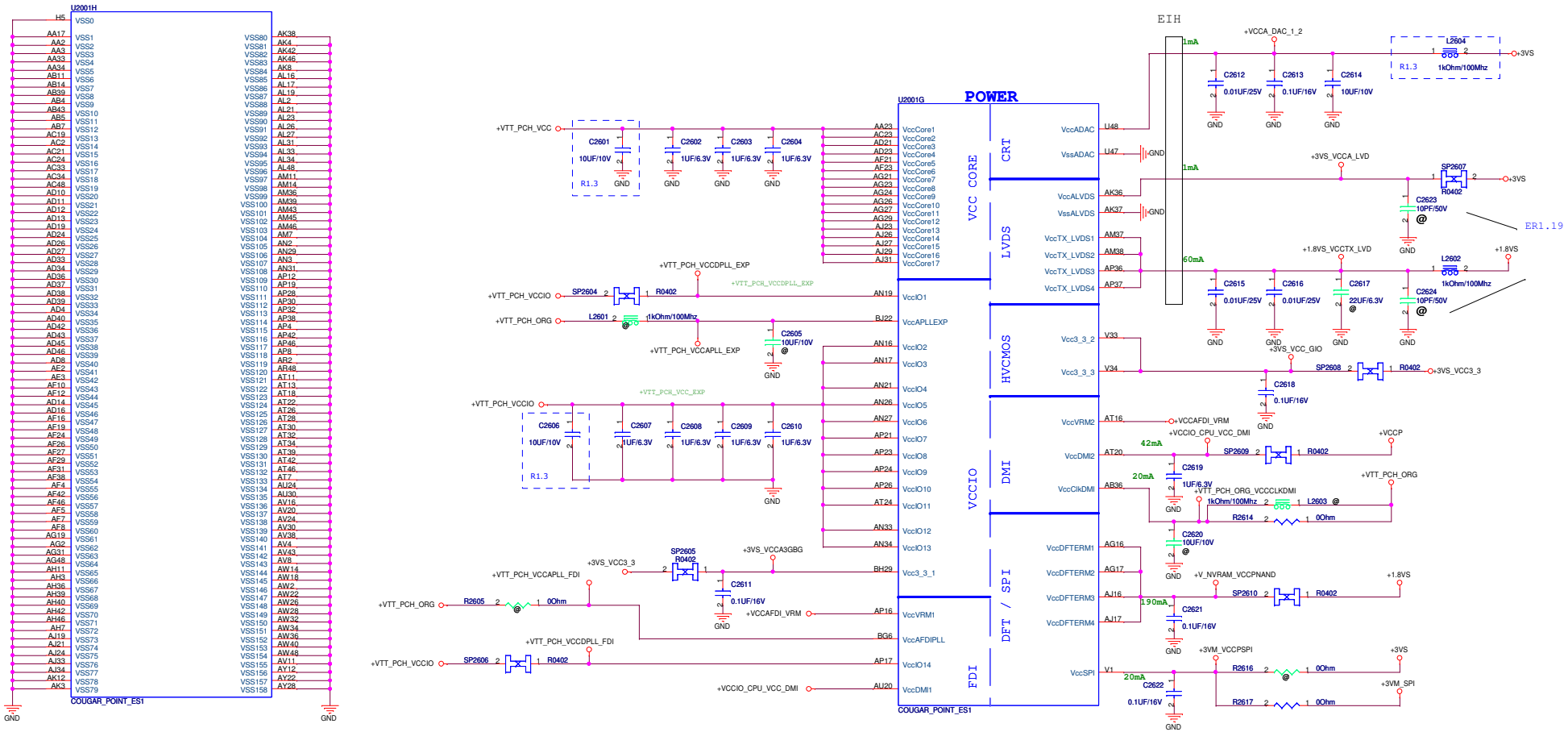




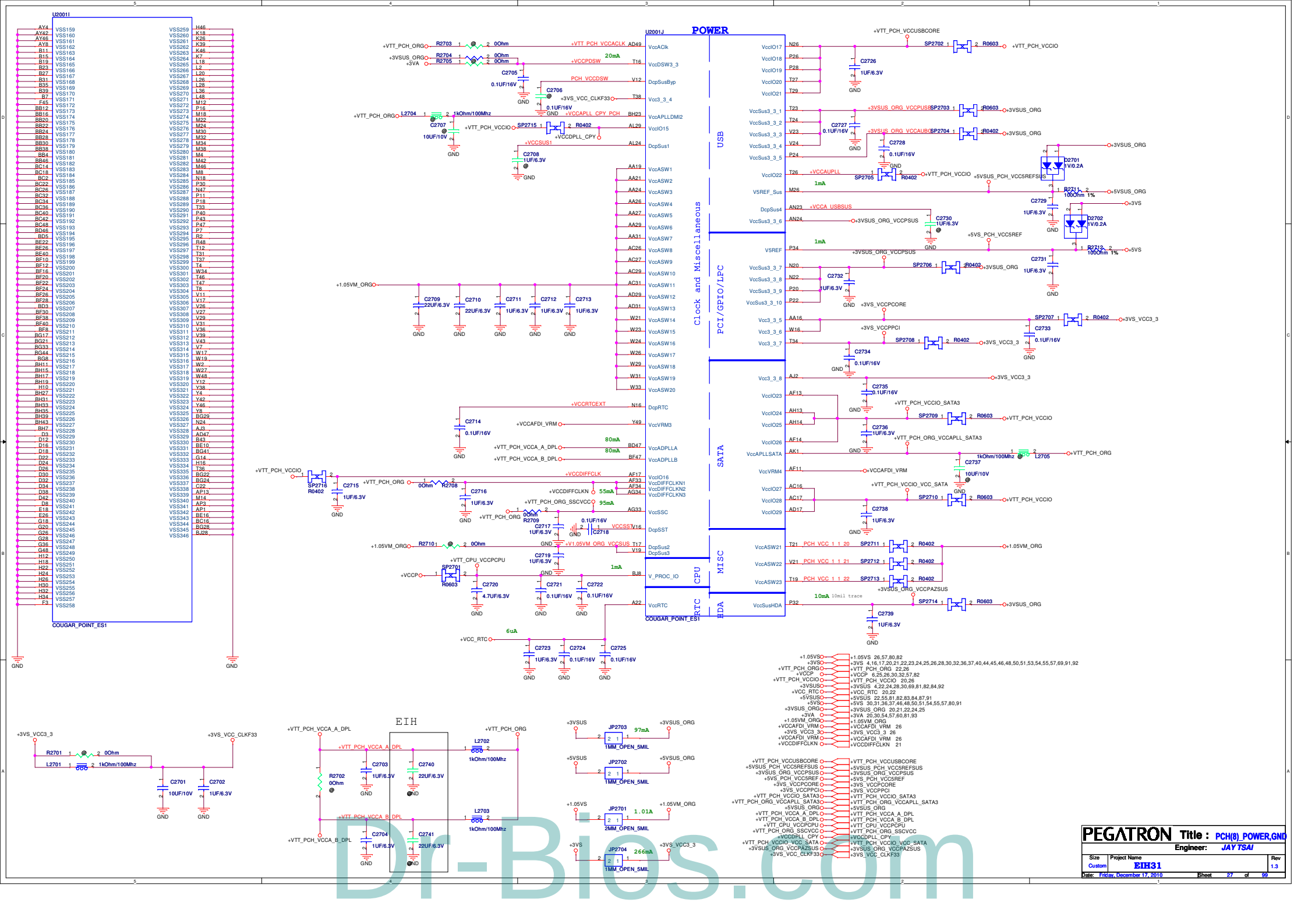




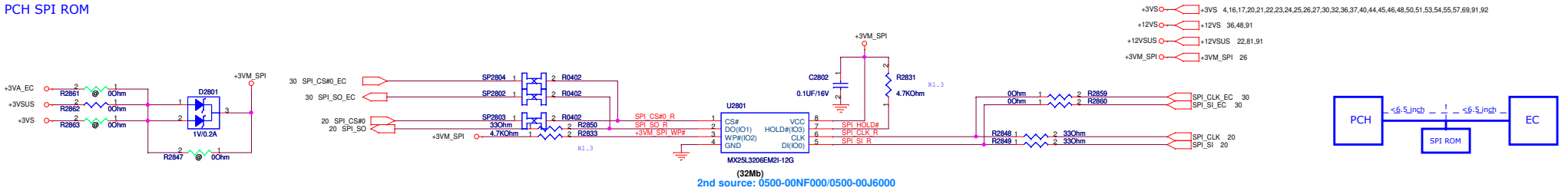
PEGATRON Title : PCH(6)_CPU,GPIO,MISC
Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.3
Date: Friday, December 17, 2010 | Sheet 25 of 99



PEGATRON	Title : PCH(7)_POWER,GND
	Engineer: JAY TSAI
Size: C	Project Name: EIH31
Rev: 1.3	
Date: Friday, December 17, 2010	Sheet 26 of 99

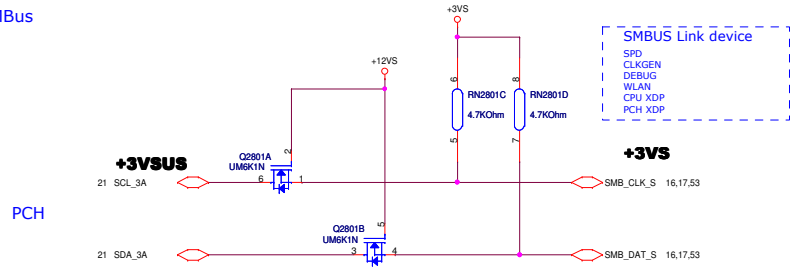

U2001I
COUGAR_POINT_ES1
U2001J
POWER
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA
COUGAR_POINT_ES1
EIH
PEGATRON
Title : PCH(8)_POWER,GND
Engineer: JAY TSAI
Size: Custom
Project Name: EIH31
Rev: 1.3
Date: Friday, December 17, 2010
Sheet 27 of 99

PCH SPI ROM

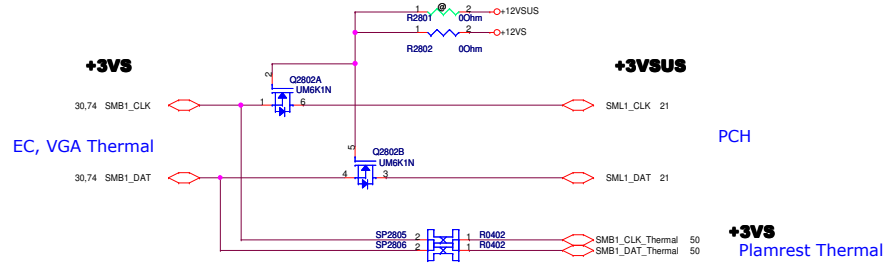


2nd source: 0500-00NF000/0500-00J6000

PCH SMBus



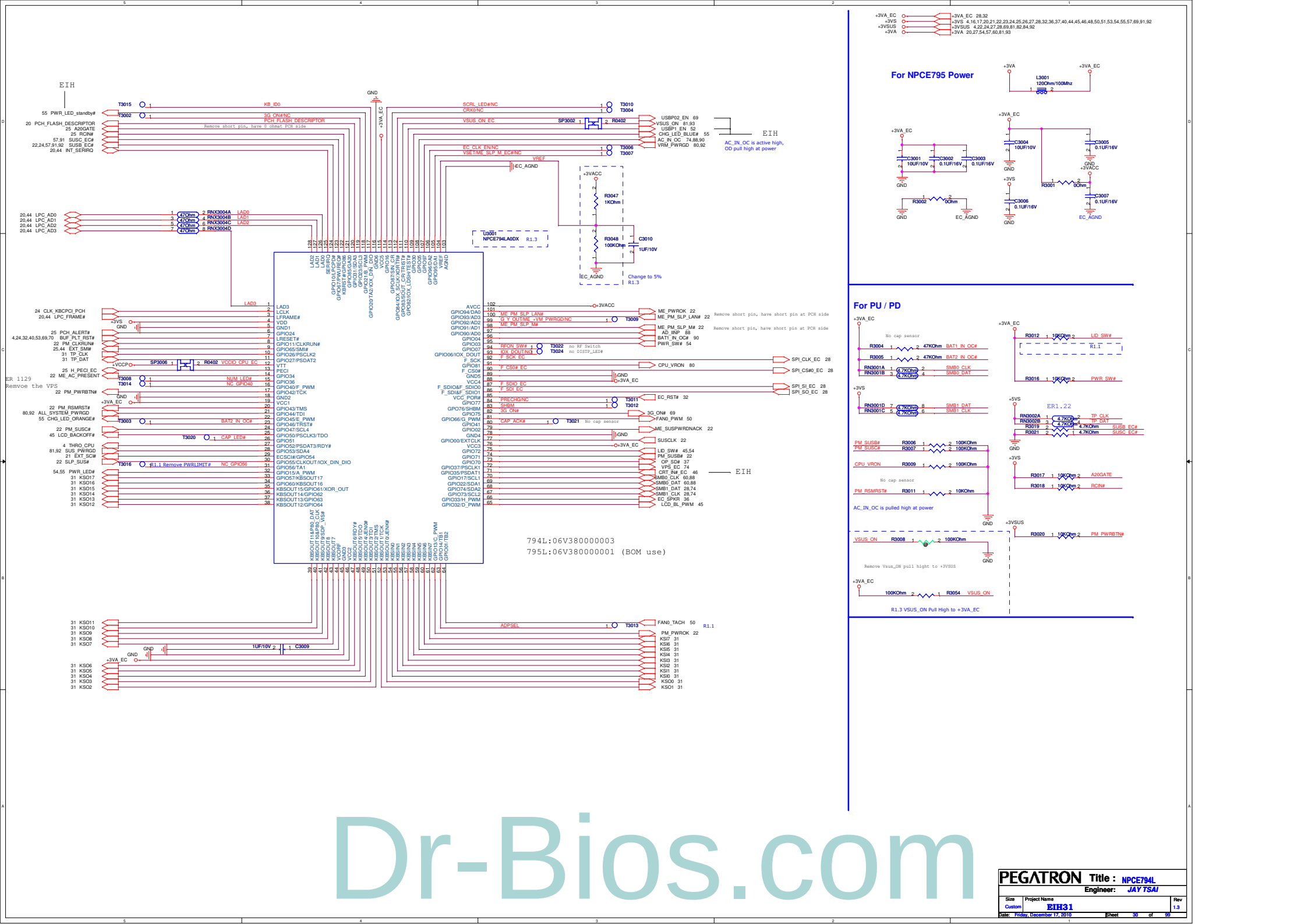
EC, VGA Thermal



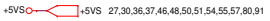
remove MOS & pull-hige resitor, because there is the function at page 74

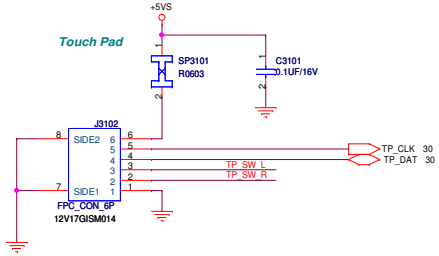
PEGATRON	Title : PCH(9)_SPI,SMB	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 28 of 99	

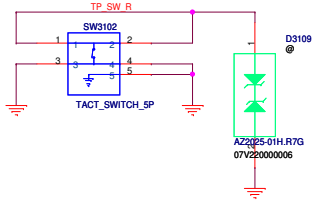
PEGATRON	Title : CLK_ICS9LRS3197	
	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 29 of 99	

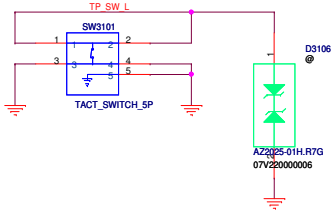


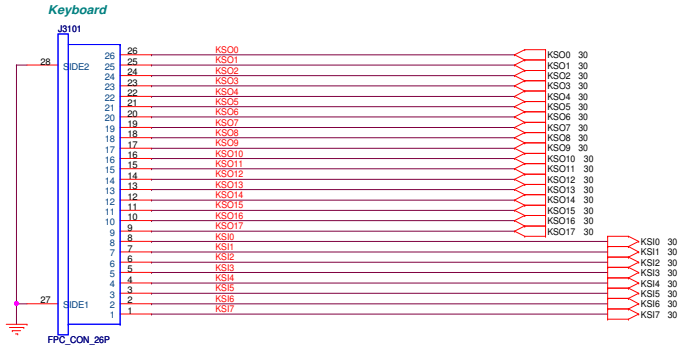
PEGATRON Title : NPCE794L
Engineer: JAY TSAI
Size: Custom | Project Name: EIH31 | Rev: 1.3
Date: Friday, December 17, 2010 | Sheet 30 of 99

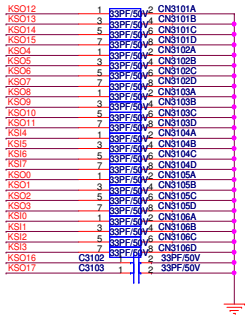












The pin define is checked to keyboard spec. R is KSO, C is KSI. The connector pin define is the same the KB.

PEGATRON Title : EC_IT8512(2)KB, TP,FP

Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

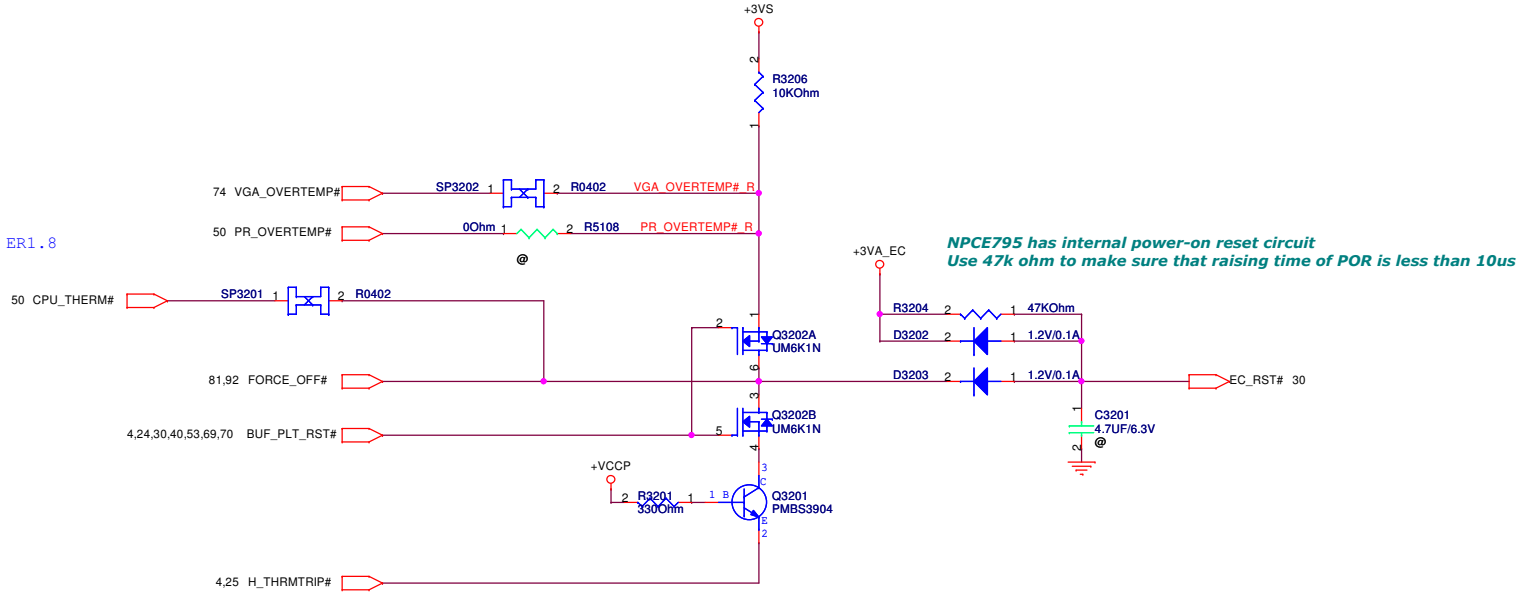
Date: Friday, December 17, 2010 Sheet 31 of 99

+VCCP +VCCP 6,25,26,27,30,57,82

+3VA_EC +3VA_EC 28,30

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,36,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92

Thermal Policy



PEGATRON	Title : RST_Reset Circuit	
<OrgName>	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.0
Date: Friday, December 17, 2010	Sheet 32 of 99	

PEGATRON	Title : MDC CONN	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 35 of 99	

Audio Codec

DIGITAL

ANALOG

Intel 1.01 Design Guide update #440484
R1.3 use dual mosfet

+12VS
SP3603
R0402
UM6K1N
Q3604B
20 ACZ_SDOUT_AUD
R3618 @ 0Ohm
+12VS
SP3604
R0402
UM6K1N
Q3604A
20 ACZ_SYNC_AUD
R3603 @ 0Ohm
ACZ_SYNC_AUD_R
ACZ_SDOUT_AUD_R

+5VS
+5VS_AMP
SP3606
R0805

+5VS 27,30,31,37,46,48,50,51,54,55,57,80,91
+3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92
+5VS_AUDIO 37

H_SPKR+ 37
H_SPKR- 37
H_SPKL- 37
H_SPKL+ 37

+5VS_AMP
R3610 0Ohm
C3634 10UF/10V @
C3628 0.1UF/16V @
C3615 10UF/10V
C3609 0.1UF/16V
Short 0 ohm
C3623 0.1UF/16V
C3620 10UF/10V
C3636 0.1UF/16V
C3638 10UF/10V @

R3609 @ 0Ohm
R3608 @ 0Ohm
R3607 @ 0Ohm
R3604 @ 0Ohm
GND_AUDIO
add R3607&R3606&R3605 c3499 for EMI

+5VS
+5VS_AUDIO
L3603
>30 mil or shape
80Ohm/100Mhz
vx_l0805_h43_small
Irat=2A

37 EAPD
C3639 10UF/10V @
T3602
ER 1.8
SPDIF OUT

+5VS_AUDIO
C3608 0.1UF/16V
C3610 10UF/10V
GND_AUDIO

+3VS
+3VS_DVDD
L3602
120Ohm/100Mhz
C3616 10UF/10V
C3617 0.1UF/16V @
C3618 0.1UF/16V

+3VS
DVDD_IO_CODEC
C3633 0.1UF/16V

U3601A
GND SPDIFO EAPD PVDD SPK-OUT-R+ SPK-OUT-R- PVSS1 SPK-OUT-L- SPK-OUT-L+ AVDD2 AVSS2
DVDD GPIO0/DMIC-DATA GPIO1/DMIC-CLK PD# SDATA-OUT BCLK DVSS2 SDATA-IN DVDD-IO SYNC RESET# PCBEEP
CBP CBN CPVEE HPOUT-R(PORT-I-R) HPOUT-L(PORT-I-L) MIC1-VREFO-L MIC1-VREFO-R MIC2-VREFO LDO-CAP VREF AVSS1 AVDD1
SenseA MIC1-L(PORT-E-L) LINE2-R(PORT-E-R) MIC2-L(PORT-F-L) MIC2-R(PORT-F-R) VREF JDREF MONO-OUT MIC1-L(PORT-B-L) MIC1-R(PORT-B-R) LINE1-L(PORT-C-L) LINE1-R(PORT-C-R)
ALC271X-VB3-GR
02V0J0000004

T3603
T3604
37 MUTE_AMP#
ACZ_SDOUT_AUD_R
20 ACZ_BCLK_AUD
20 ACZ_SDIN0_AUD
R3625 @ 33Ohm
Check R3625 resistor value
DVDD_IO_CODEC
ACZ_SYNC_AUD_R
20,37 ACZ_RST#_AUD
PC_BEEP
ACZ_BCLK_AUD
C3629 @ 22PF/50V

C3626 2.2UF/10V
C3627 2.2UF/10V
GND_AUDIO
AC_HP_R
AC_HP_L
AUD_LDO_CAP
VREF_CODEC
+5VS_AUDIO
C3614 0.1UF/16V
C3632 10UF/10V
C3613 0.1UF/16V
C3611 2.2UF/10V
GND_AUDIO

AC_HP_R 37
AC_HP_L 37
MIC1_VREFO 37
MIC_VREFO 37
MIC2_VREFO 37

HeadPhone Out
EXT MIC Vref.
EXT MIC Vref.
COMBO MIC Vref.
INT MIC Vref.

MIC1_VREFO
MIC_VREFO
MIC2_VREFO
AUD_LDO_CAP
C3612 10UF/10V
C3624 10UF/10V @
C3619 10UF/10V @
C3625 10UF/10V @
GND_AUDIO GND_AUDIO GND_AUDIO GND_AUDIO

ER 1129
Change the PART & SYMBOL (8VIA)

HP Jack Detect
EXT MIC Detect
37 HPOUT_JD#
37 MIC1_JD#
R3619 1% 39.2KOhm
R3613 1% 20KOhm

INT MIC IN
AUD_LDO_CAP
R3628 4.7KOhm
52 INT_MIC_AC_IN
R3629 1KOhm
1UF/10V C3630 INT_MIC_AC_IN_L
1UF/10V C3631 INT_MIC_AC_IN_R

C3635 2.2UF/10V
EXT_MIC_AC_IN_R
EXT_MIC_AC_IN_L
C3637 2.2UF/10V
R3630 1KOhm
R3631 1KOhm
EXT_MIC_R 37
EXT_MIC_L 37
EXT MIC IN

37 MIC2_L
37 MIC2_R
37 MIC2_JD#
R3620 1% 20KOhm
R3616 20KOhm 1%
GND_AUDIO

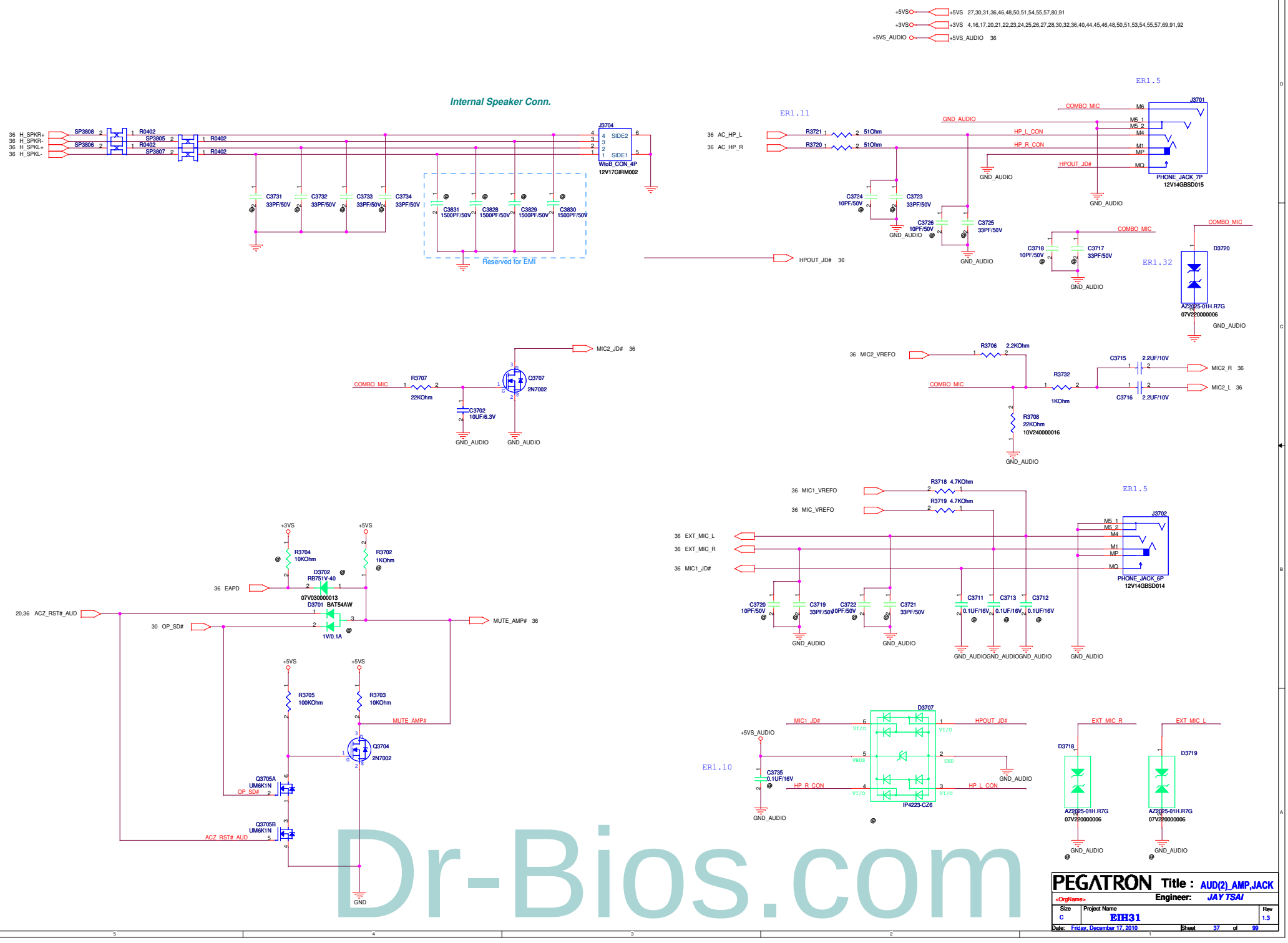
R3605 @ 0Ohm
D3601
20 SB_SPKR
30 EC_SPKR
1V/0.2A
R3611 @ 0Ohm
R3614 47KOhm
R3615 4.7KOhm
PC_BEEP_C
C3622 0.1UF/16V
PC_BEEP
C3621 @ 100PF/50V
ER1.2

U3601B
GND1 GND2 GND3 GND4 GND8 GND7 GND6 GND5
ALC271X-VB3-GR
02V0J0000004

ER 1129
Change the PART & SYMBOL (8VIA)

R3606 @ 0Ohm
R3626 @ 0Ohm
GND_AUDIO
R3602 @ 0Ohm
R3627 @ 0Ohm
GND_AUDIO

PEGATRON Title : AUD(1)_ALC269
<OrgName> Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.1
Date: Friday, December 17, 2010 | Sheet 36 of 99



PEGATRON Title : AUD(2)_AMP,JACK

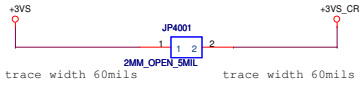
<OrgName> Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

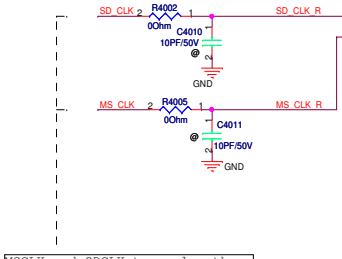
Date: Friday, December 17, 2010 Sheet 37 of 99

PEGATRON	Title : AUD(3)_FM2010	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 38 of 99	

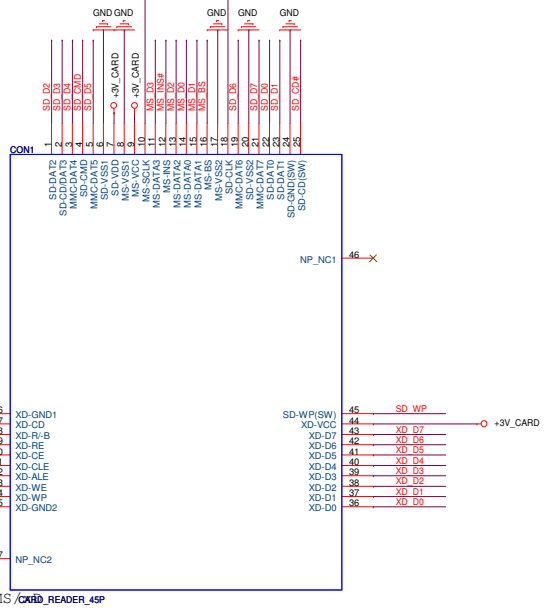
PEGATRON	Title : AUD(4)_****	
<OrgName>	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 39 of 99	

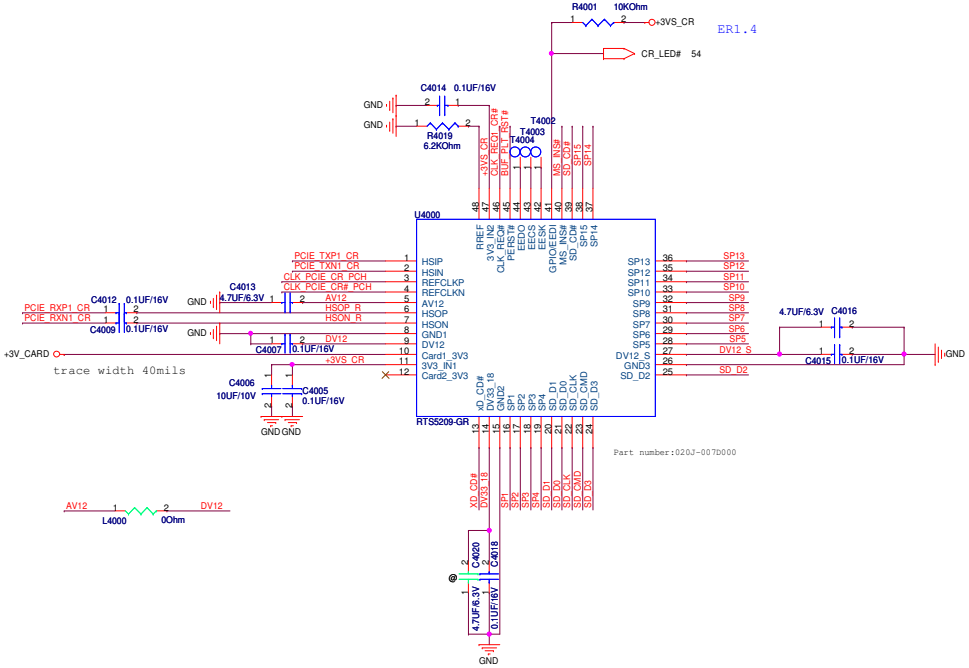


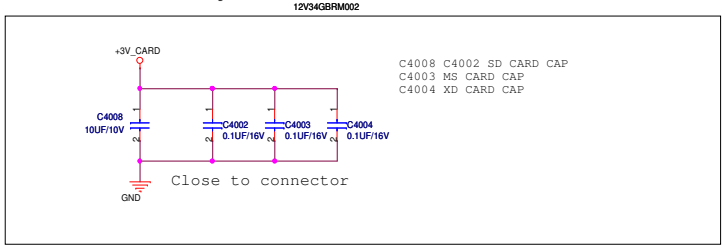
From System's PCIE interface



MSCLK and SDCLK trace length shorter,surround with GND.







Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

Share Pin

Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

PEGATRON Title : RTS5209
<OrgName> Engineer:
Size C | Project Name EIH31 | Rev 0.1
Date: Friday, December 17, 2010 Sheet 40 of 99

PEGATRON	Title : CB(2)_R5C833	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 41 of 99	

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92

+12V +12V 91

PEGATRON Title : CB(3)_4in1 CardReader

<OrgName> Engineer: JAY TSAI

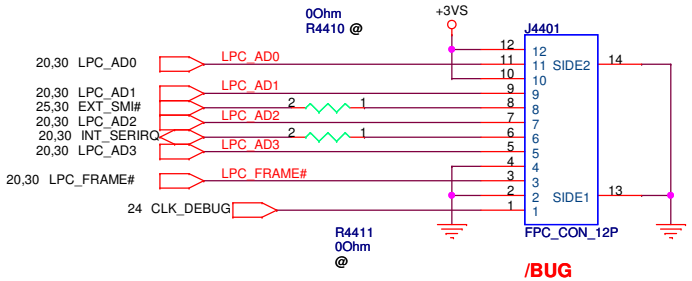
Size	Project Name	Rev
C	EIH31	1.3

Date: Friday, December 17, 2010 Sheet 42 of 99

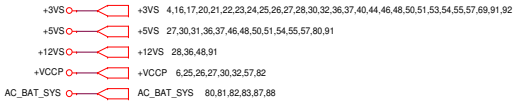
PEGATRON	Title : CB(4)_NewCard	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 43 of 99	

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,45,46,48,50,51,53,54,55,57,69,91,92

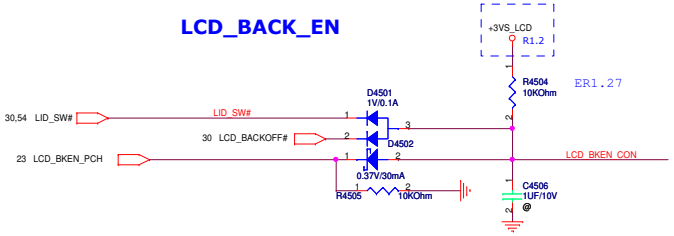
LPC Debug Port



PEGATRON	Title : BUG_Debug	
<OrgName>	Engineer: JAY TSAI	
Size: B	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 44 of 99	

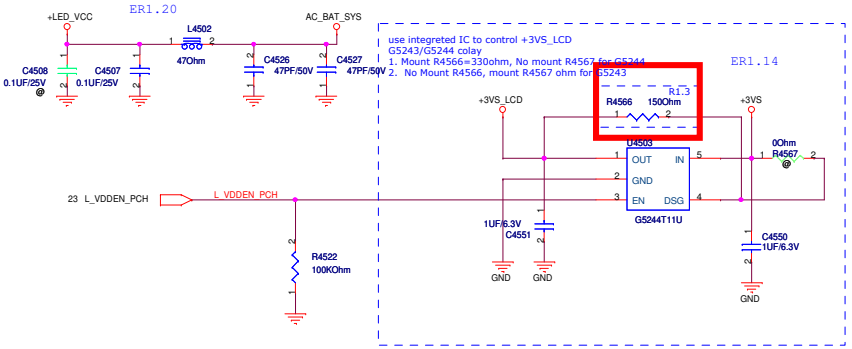


LCD_BACK_EN

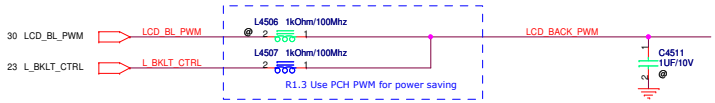


Remove MOS solution.

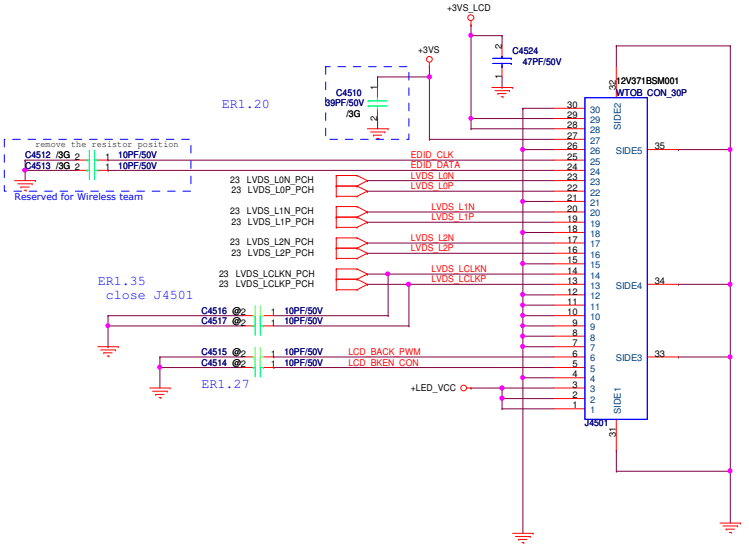
LCD VDDEN / +LED_VCC



LCD_BL_PWM

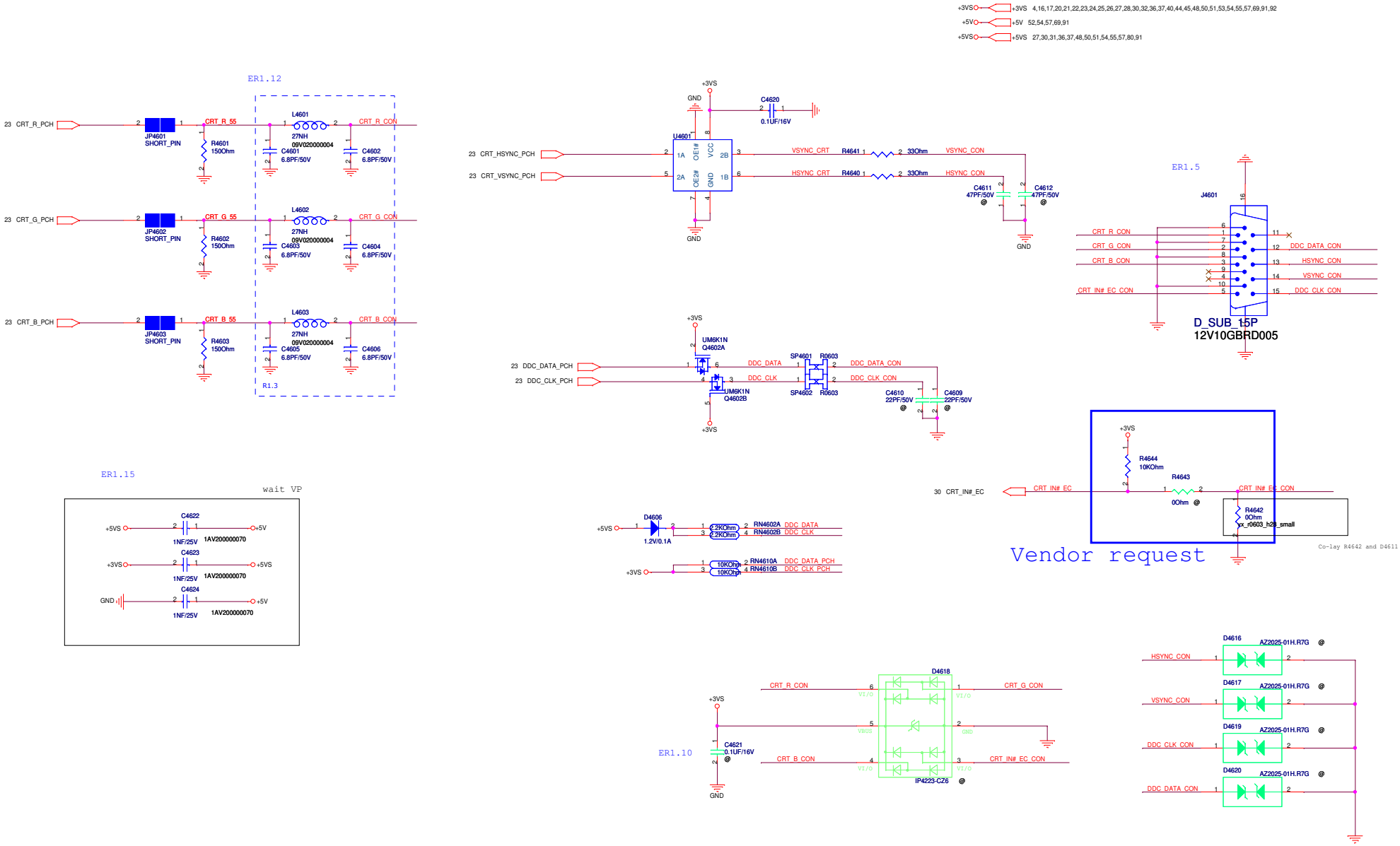


LVDS Connector



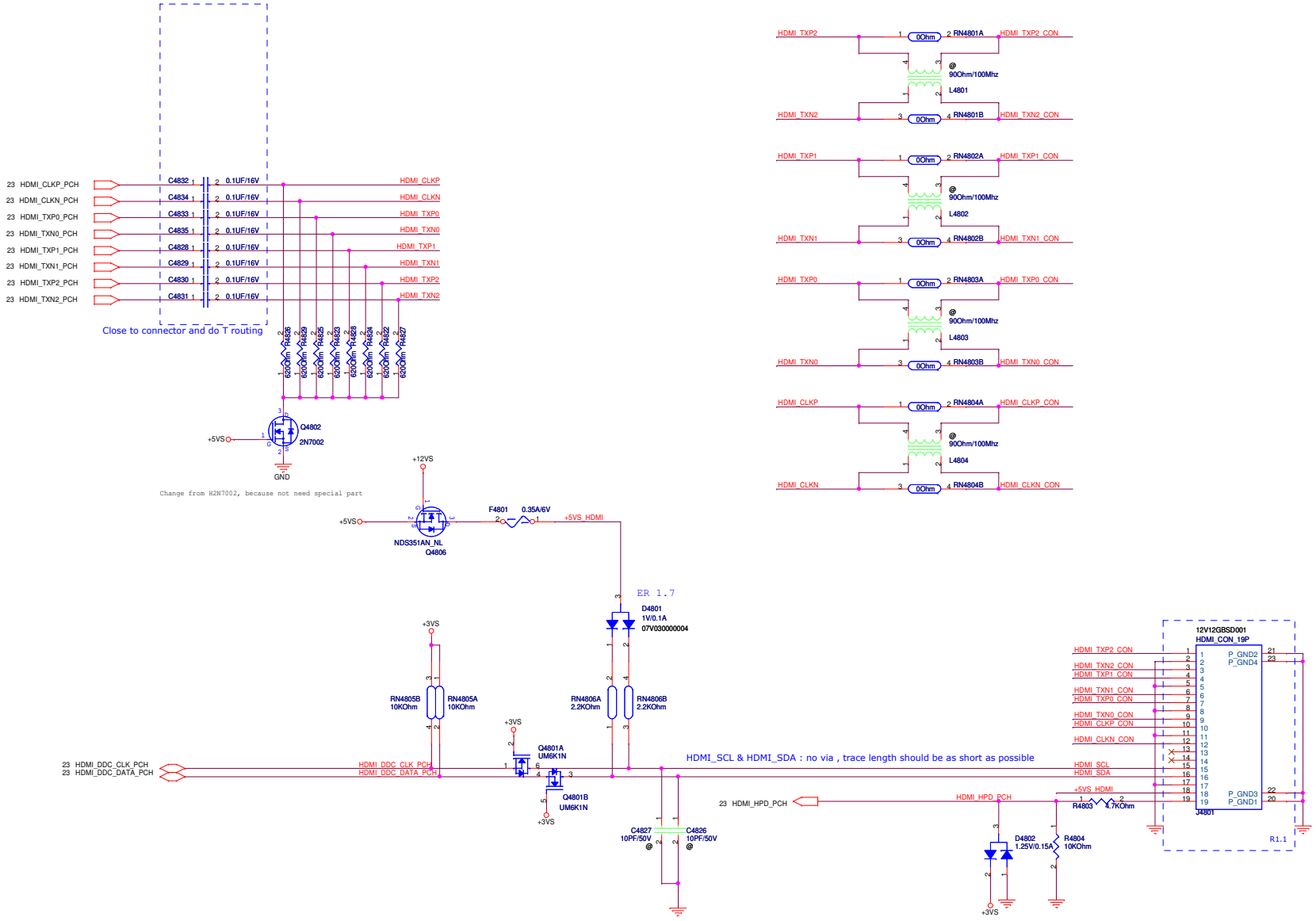
EDID Switch

PEGATRON	Title : CRT(1)_LVDS	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 45 of 99	



PEGATRON	Title : CRT(2)_D-Sub	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 46 of 99	

PEGATRON	Title : CRT(3)_Display Port		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Friday, December 17, 2010	Sheet 47 of 99		



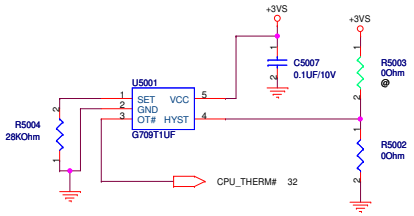
PEGATRON	Title : TV(1)_HDMI	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 48 of 99	

PEGATRON	Title : TV(2)_****	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 49 of 99	

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,51,53,54,55,57,69,91,92

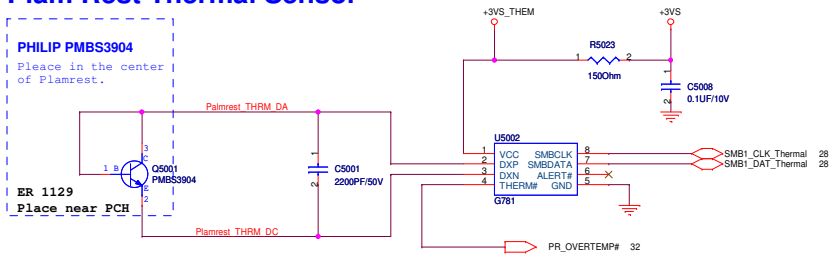
+5VS +5VS 27,30,31,36,37,46,48,51,54,55,57,80,91

CPU Thermal Sensor



(10°C for HYST =VCC)
(2°C for HYST = GND)
Hysteresis prevents the output from oscillating when the temperature is near the trip point.

Plam Rest Thermal Sensor

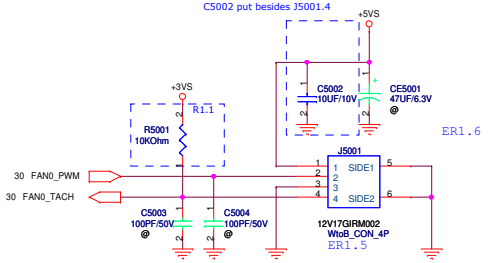


U5002 under palmrest

SMBUS addr=1001100x (98)

U5002: Remote(Local) thermal sensor,use remote mode.

PWM Fan



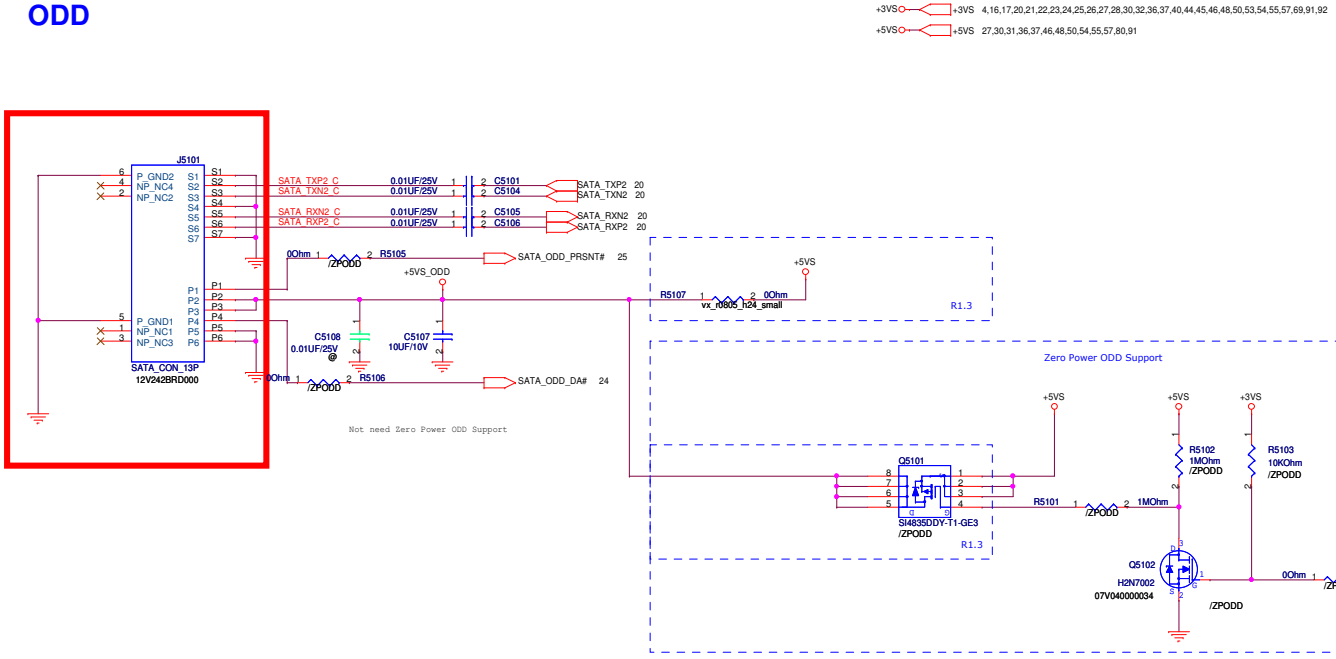
PEGATRON Title : FAN_Fan,Sensor

<OrgName> Engineer: JAY TSAI

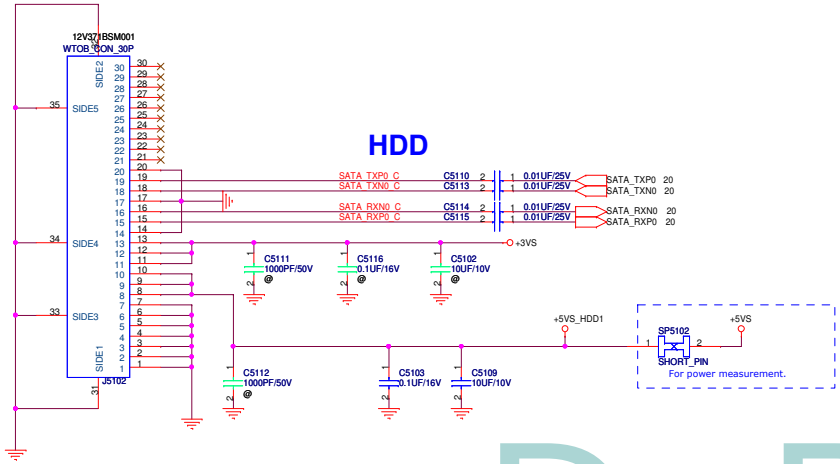
Size	Project Name	Rev
C	EIH31	2.0

Date: Friday, December 17, 2010 Sheet 50 of 99

ODD

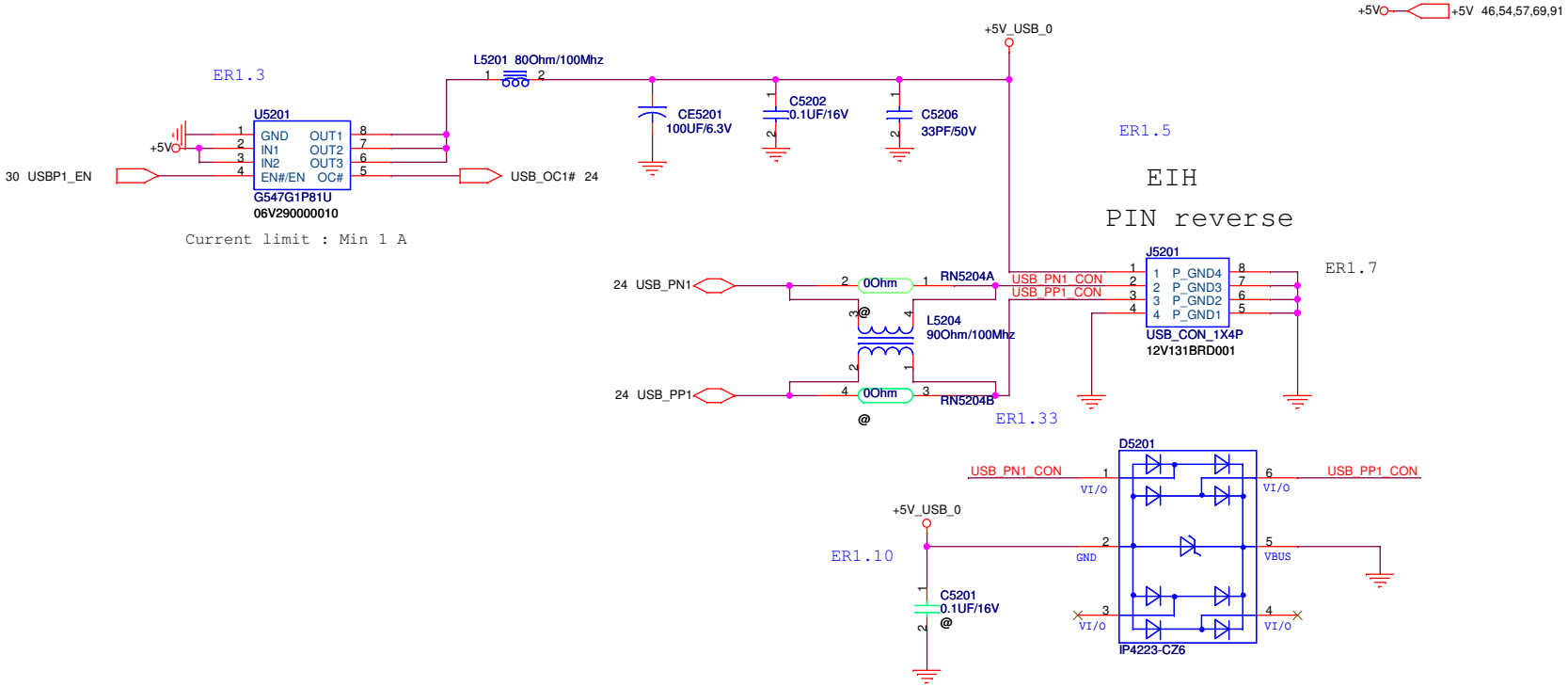


HDD

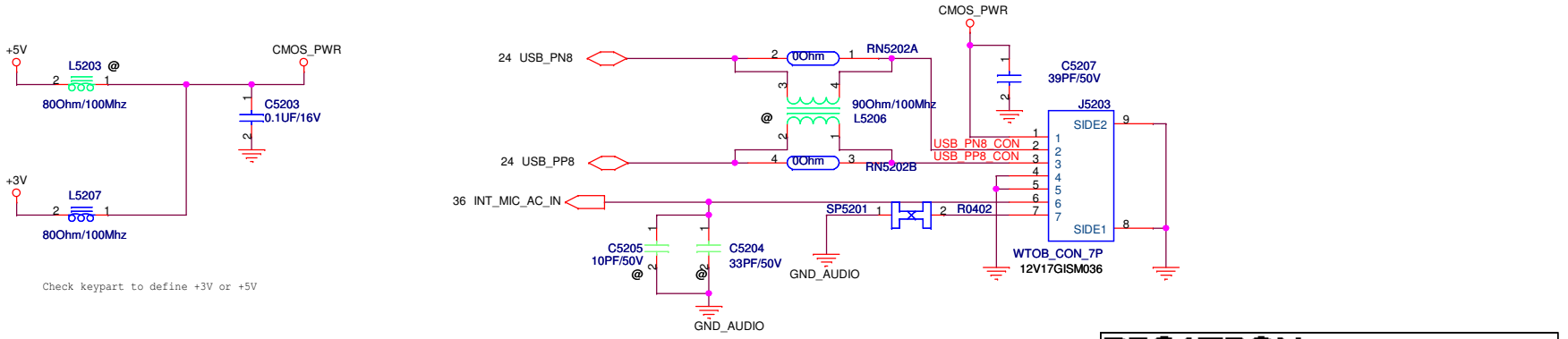


PEGATRON	Title : XDD_HDD,ODD	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 51 of 99	

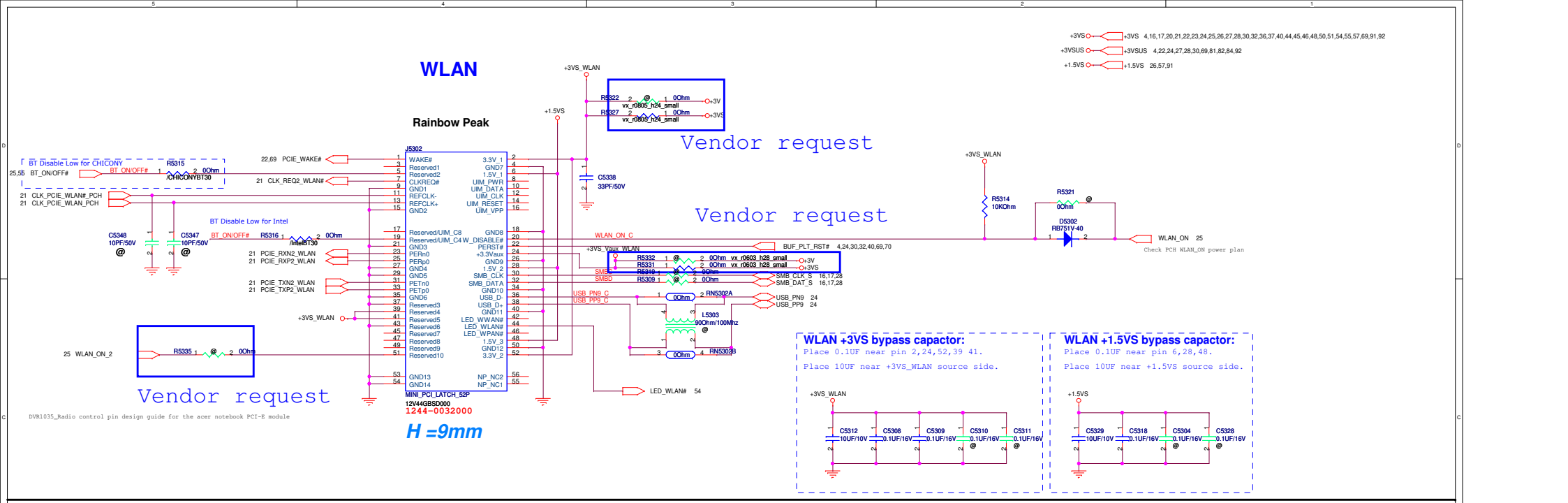
USB ports

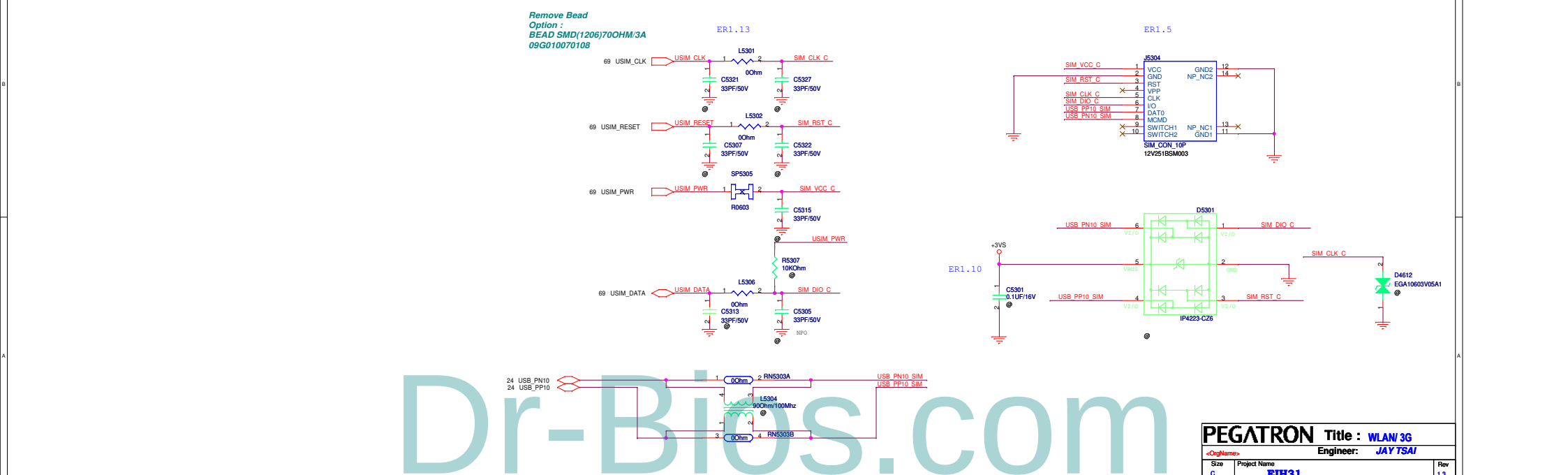


Camera

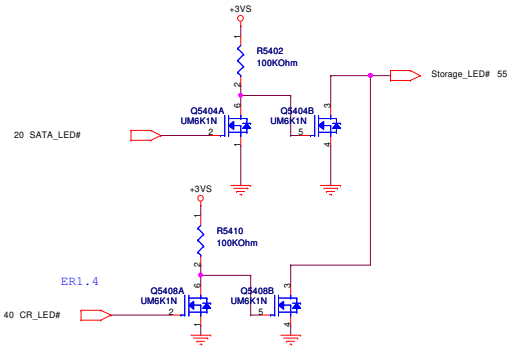


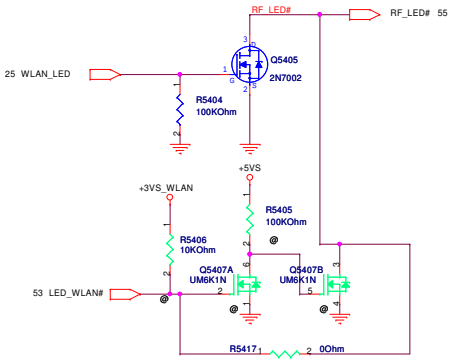
PEGATRON	Title : USB_USB Port	
<OrgName>	Engineer: JAY TSAI	
Size: B	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 52 of 99	



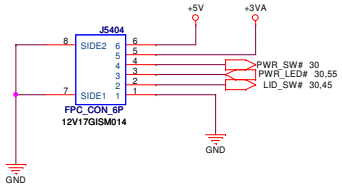


PEGATRON	Title : WLAN/ 3G		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Friday, December 17, 2010	Sheet 53 of 99		





POWER Board



PEGATRON	Title : USB3.0	
<OrgName>	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 54 of 99	

+3VA +3VA 20,27,30,54,57,60,81,93

+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,57,69,91,92

+5VSUS +5VSUS 22,27,81,82,83,84,87,91

+5VA +5VA 81,88

+5V +5V 46,52,54,57,69,91

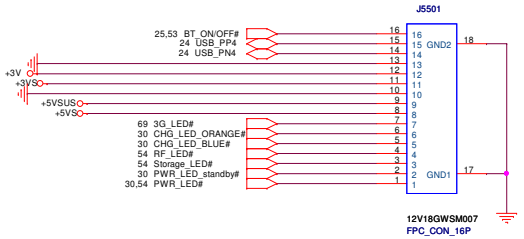
+5VS +5VS 27,30,31,36,37,46,48,50,51,54,57,80,91

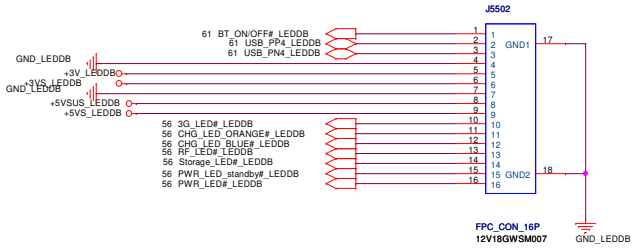
AC_BAT_SYS AC_BAT_SYS 45,80,81,82,83,87,88

+3V +3V 4,24,52,53,57,69,91

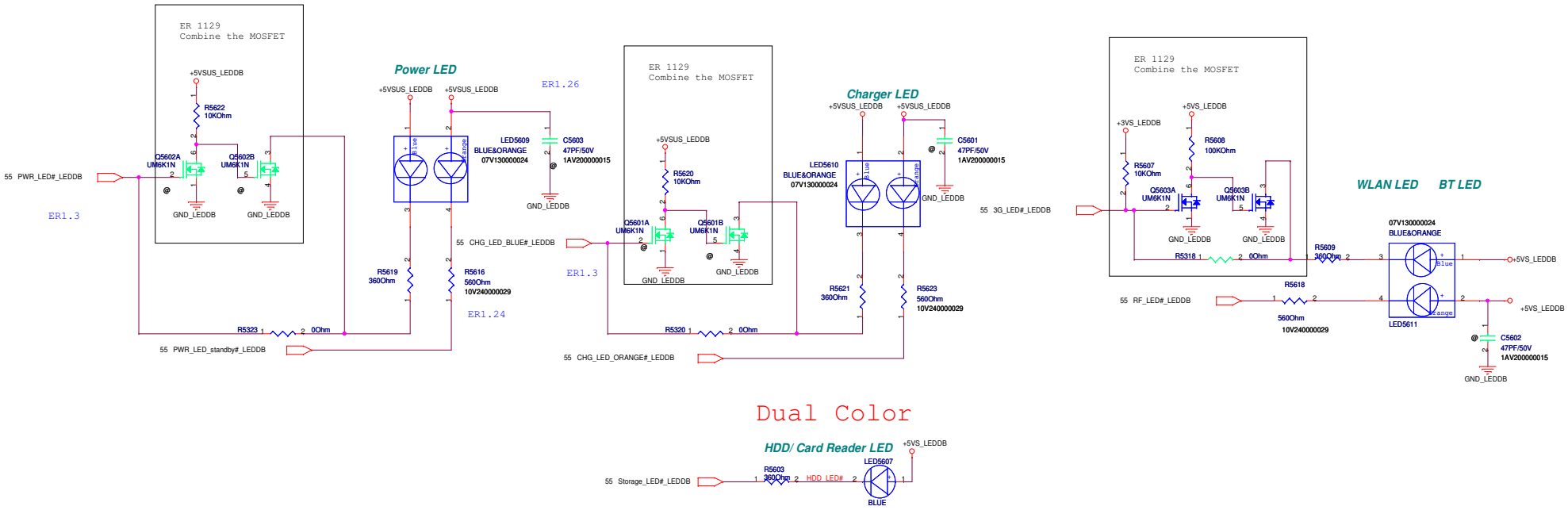
MB

LED DB



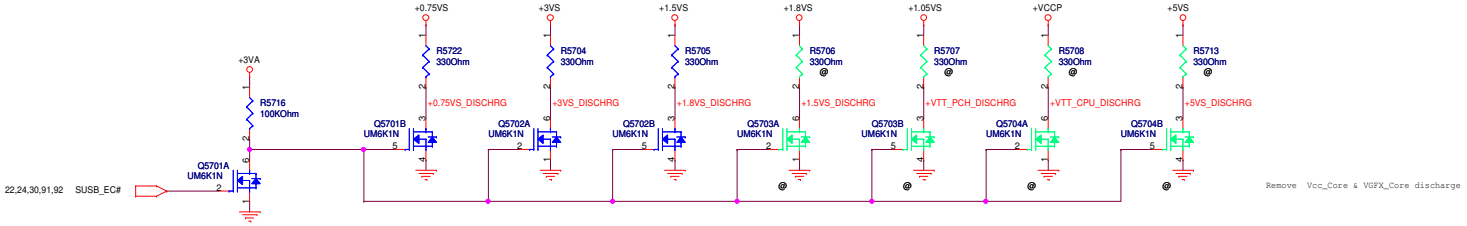


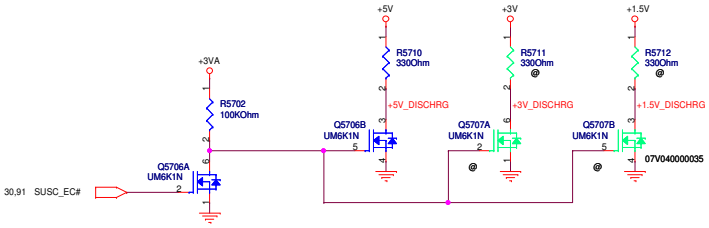
PEGATRON	Title : System Setting	
<OrgName>	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 55 of 99	



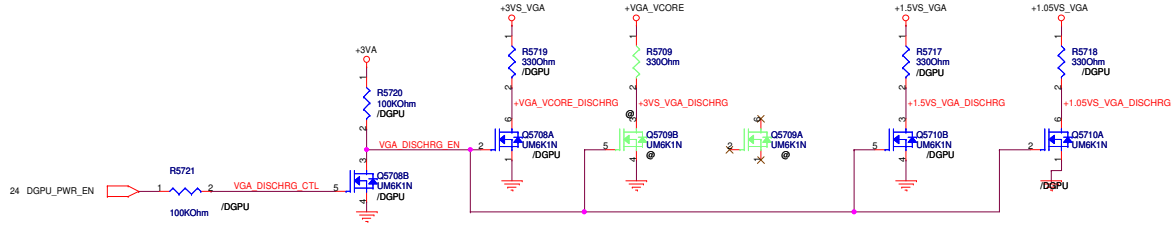
PEGATRON	Title : LED_Indicator	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 56 of 99	

+3VA +3VA 20,27,30,54,60,81,93
+VCC_CORE +VCC_CORE 6,80
+VGFX_CORE +VGFX_CORE 7,80
+VCCP +VCCP 6,25,26,27,30,32,82
+0.75VS +0.75VS 16,17,83
+1.05VS +1.05VS 26,27,80,82
+1.5VS +1.5VS 26,53,91
+1.8VS +1.8VS 7,24,26,84
+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,69,91,92
+5VS +5VS 27,30,31,36,37,46,48,50,51,54,55,80,91
+1.5V +1.5V 5,7,16,83
+3V +3V 4,24,52,53,55,69,91
+5V +5V 46,52,54,69,91
+VGA_VCORE +VGA_VCORE 75,87
+3VS_VGA +3VS_VGA 70,72,74,91
+1.5VS_VGA +1.5VS_VGA 71,76,91
+1.05VS_VGA +1.05VS_VGA 70,71,72,91





R1.1



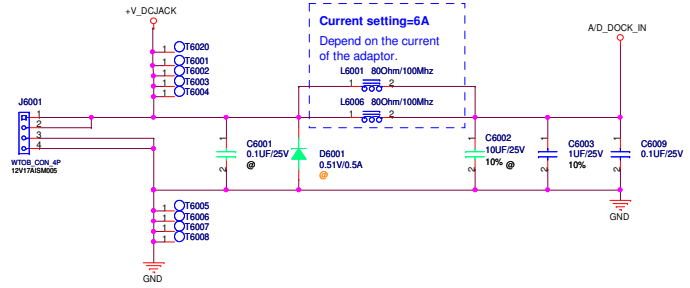
Unmount +VGA_Vcore discharg

PEGATRON	Title : DSG_Discharge	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 57 of 99	

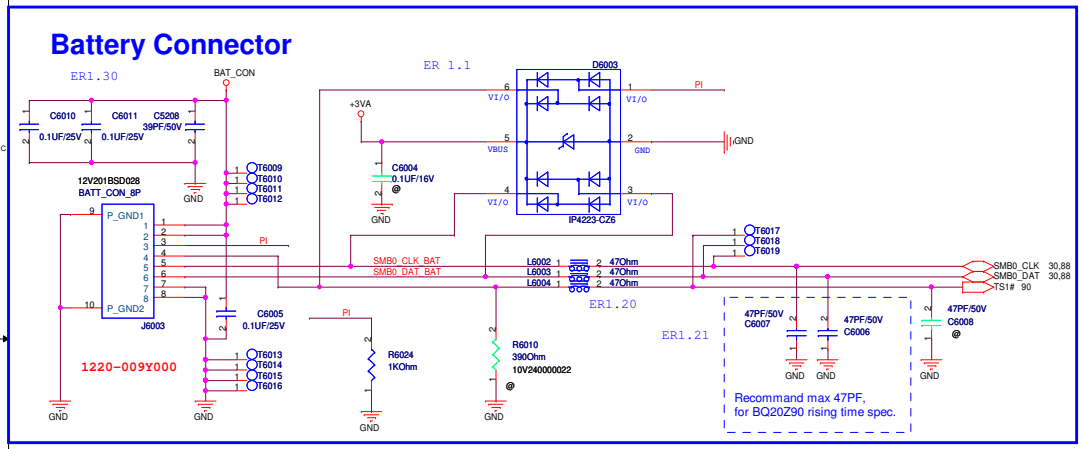
PEGATRON	Title : PCI_****	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 58 of 99	

PEGATRON	Title : DJ_****	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 59 of 99	

DC Jack WtoB CONN



Battery Connector



+VCC_RTC +VCC_RTC 20,22,27
+3VA_EC +3VA_EC 28,30,32
+3VA +3VA 20,27,30,54,57,81,93
+5VA +5VA 81,88

+3VSUS +3VSUS 4,22,24,27,28,30,69,81,82,84,92
+5VSUS +5VSUS 22,27,55,81,82,83,84,87,91
+12VSUS +12VSUS 22,28,81,91

+1.5V +1.5V 5,7,16,57,83
+3V +3V 4,24,52,53,55,57,69,91
+5V +5V 46,52,54,57,69,91
+12V +12V 91

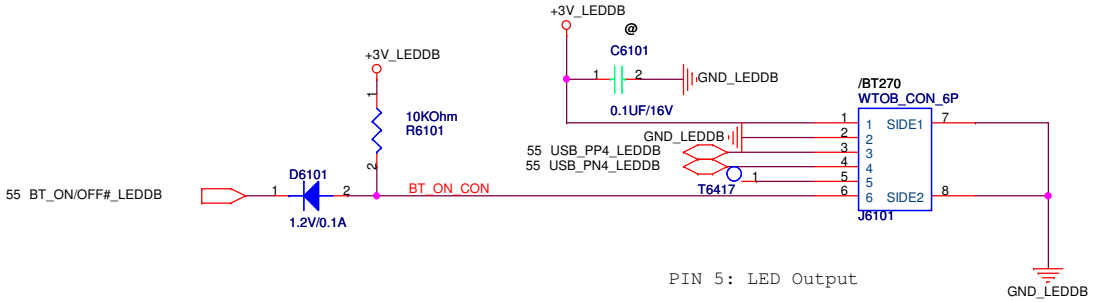
+0.75VS +0.75VS 16,17,57,83
+1.05VS +1.05VS 26,27,57,80,82
+1.5VS +1.5VS 26,53,57,91
+1.8VS +1.8VS 7,24,26,57,84
+3VS +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92
+5VS +5VS 27,30,31,36,37,46,48,50,51,54,55,57,80,91
+12VS +12VS 28,36,48,91

AC_BAT_SYS AC_BAT_SYS 45,80,81,82,83,87,88
A/D_DOCK_IN A/D_DOCK_IN 88
BAT_CON BAT_CON 88

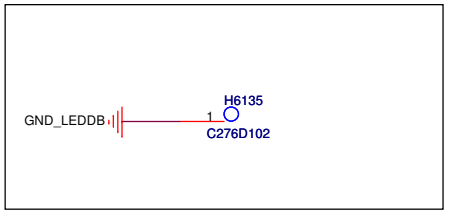
+1.5V_DDR3 +1.5V_DDR3 16,17,18
+VCCP +VCCP 6,25,26,27,30,32,57,82
+VCC_CORE +VCC_CORE 6,80
+VGFX_CORE +VGFX_CORE 7,80
+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27
+VTT_PCH_VCCIO +VTT_PCH_VCCIO 20,26,27
+1.05VM_ORG +1.05VM_ORG 27

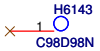
+V_VREF +V_VREF
+V_VREF_DDR3 +V_VREF_DDR3 7,16,17,18,83
+V_SM_VREF +V_SM_VREF

PEGATRON	Title : DC_DC/BAT CONN	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 60 of 99	



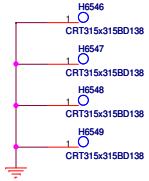
PIN 5: LED Output





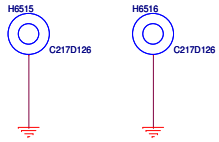
PEGATRON	Title : BT_Bluetooth	
<OrgName>	Engineer: JAY TSAI	
Size: B	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 61 of 99	

CPU Bracket Hole

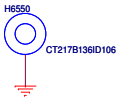


ME B Type

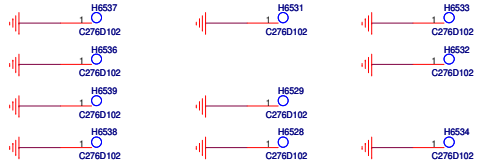
VGA Bracket Hole



IO Board Hole



ME A Type



ME C/D Type

PEGATRON Title : ME_CONN,Skew Hole

<OrgName> Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

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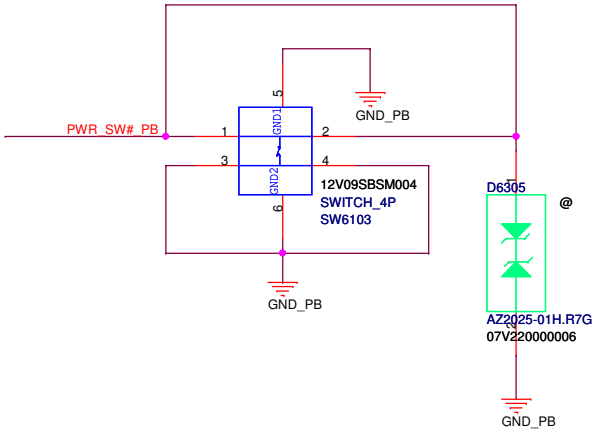
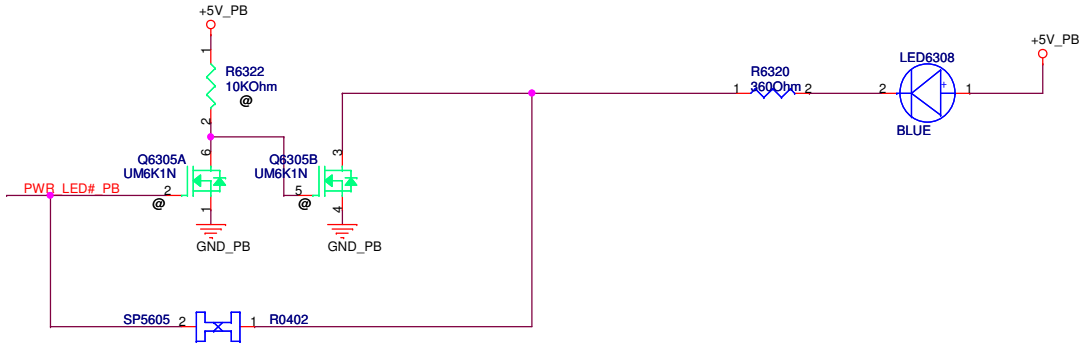
Power Button

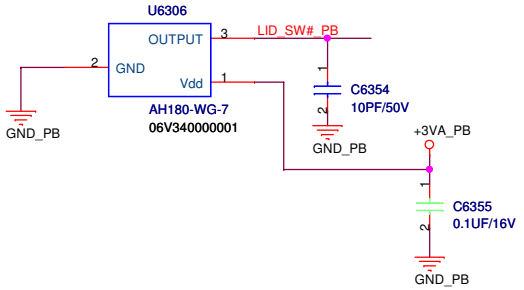


Power Button LED-Power

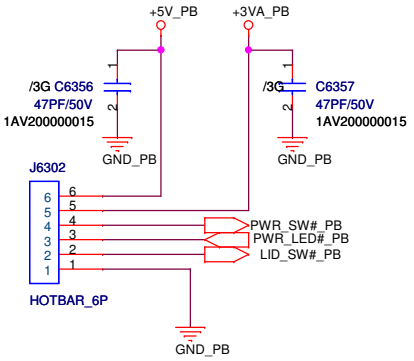
Power LED



Hall Sensor



ER1.34



HOT bar

SKREW HOLE MAKING BY LAYOUT

PEGATRON Title : TPM_****

<OrgName> Engineer: JAY TSAI

Size	Project Name	Rev
B	EIH31	1.3

Date: Friday, December 17, 2010 Sheet 63 of 99

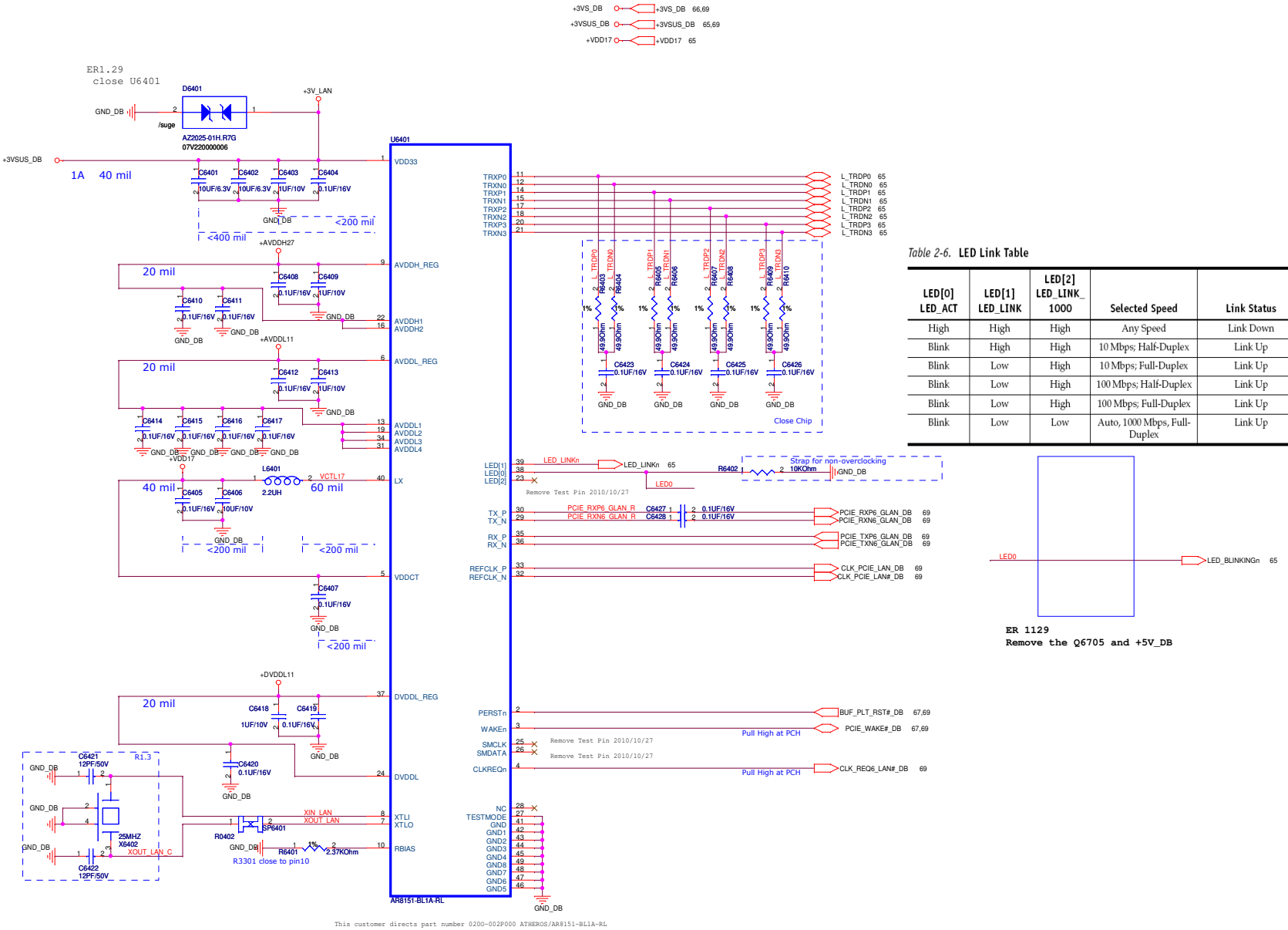
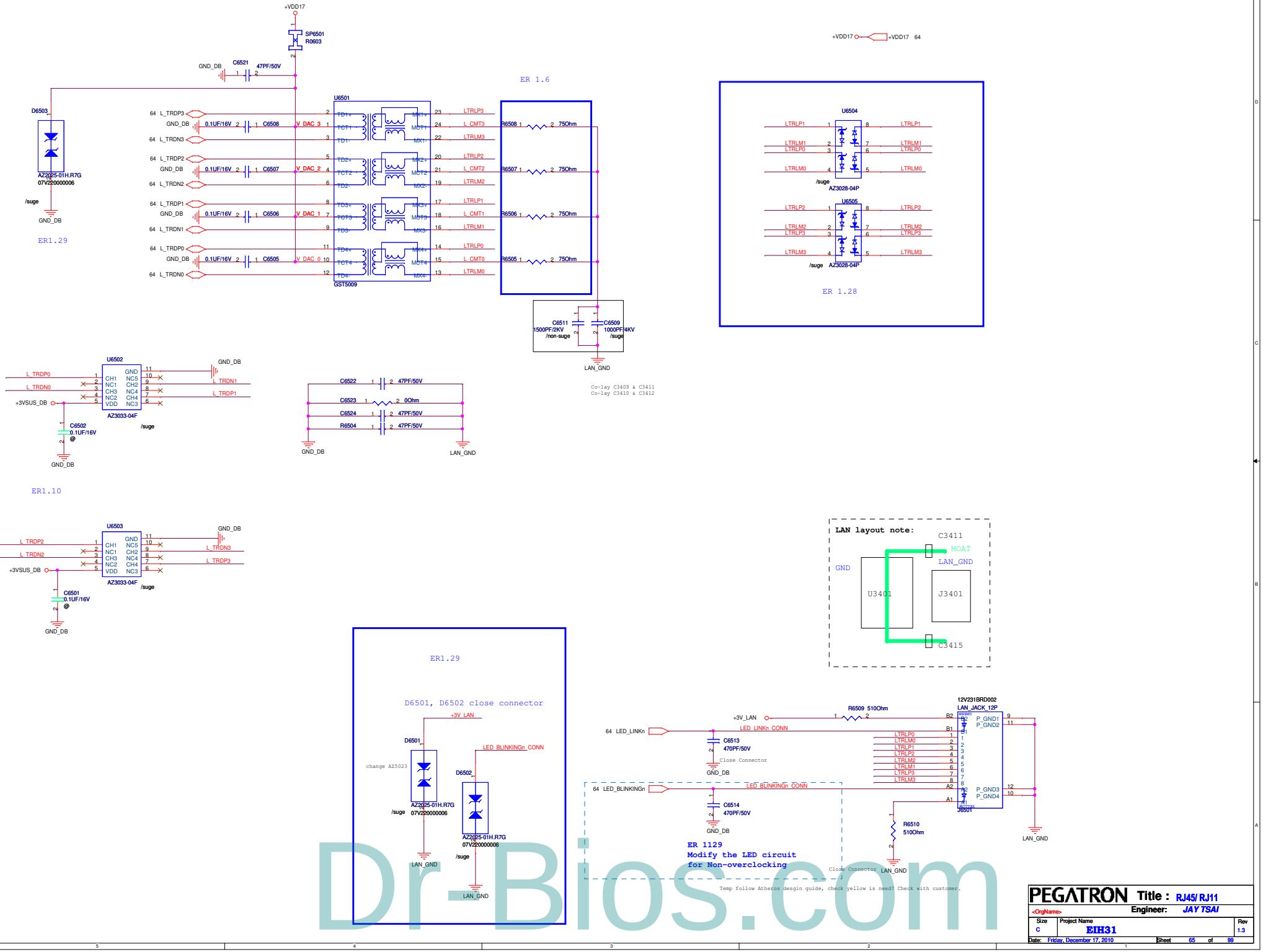


Table 2-6. **LED Link Table**

LED[0] LED_ACT	LED[1] LED_LINK	LED[2] LED_LINK_ 1000	Selected Speed	Link Status
High	High	High	Any Speed	Link Down
Blink	High	High	10 Mbps; Half-Duplex	Link Up
Blink	Low	High	10 Mbps; Full-Duplex	Link Up
Blink	Low	High	100 Mbps; Half-Duplex	Link Up
Blink	Low	High	100 Mbps; Full-Duplex	Link Up
Blink	Low	Low	Auto, 1000 Mbps, Full-Duplex	Link Up

This customer directs part number 0200-002P000 ATHEROS/AR8151-BL1A-RL

PEGATRON Title : LAN_AR8151
<OrgName> Engineer: JAY TSAI
Size C | Project Name EIH31 | Rev 1.3
Date: Friday, December 17, 2010 | Sheet 64 of 99



PEGATRON Title : RJ45/ RJ11

<OrgName> Engineer: JAY TSAI

Size	Project Name	Rev
C	EIH31	1.3

Date: Friday, December 17, 2010 Sheet 65 of 99

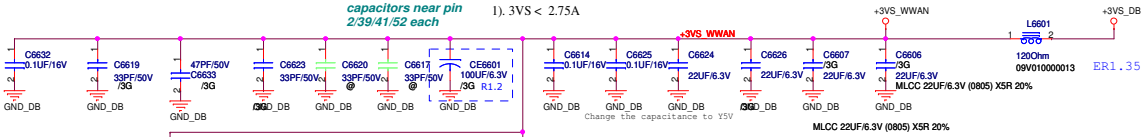
3G

Place one 22uF capacitor near pin2, another near 39/41, the other near pin52.

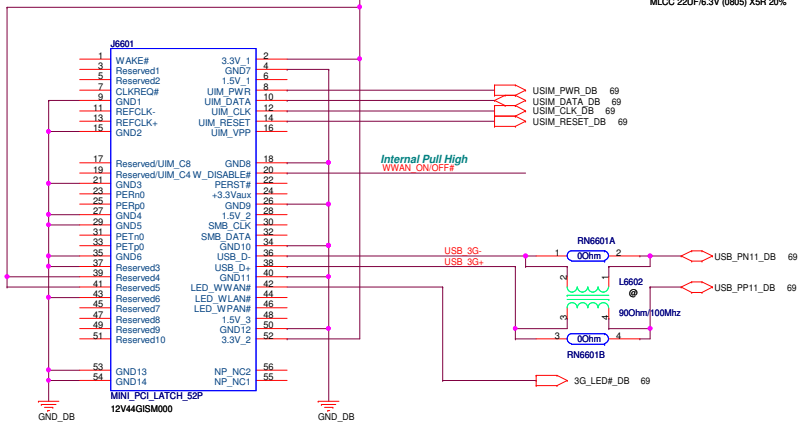
Place 0.1uF & 33PF capacitors near pin 2/39/41/52 each

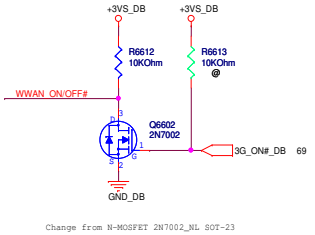
POWER CONSUMPTION:
1). 3VS < 2.75A

ER1.34



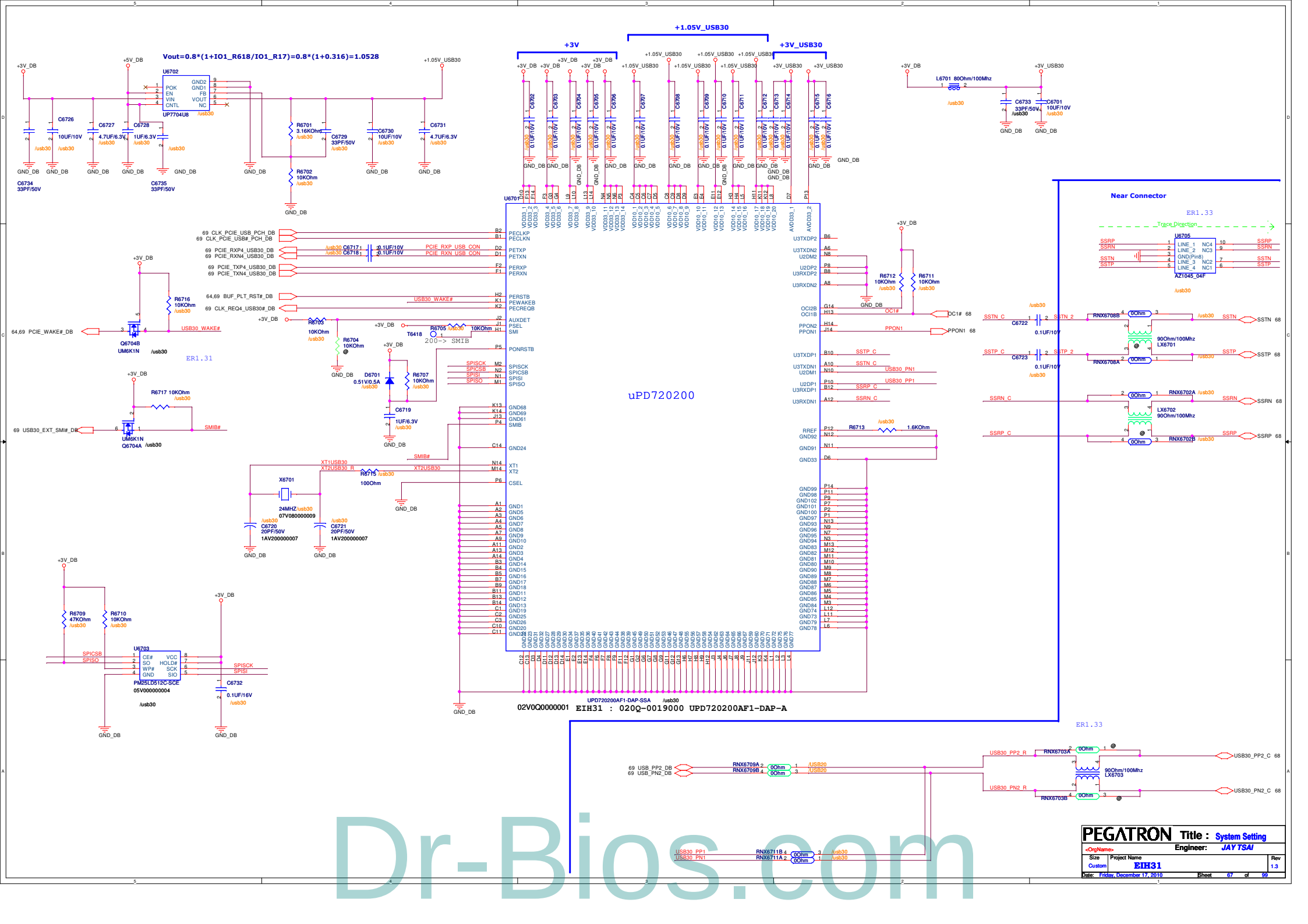
ER1.35



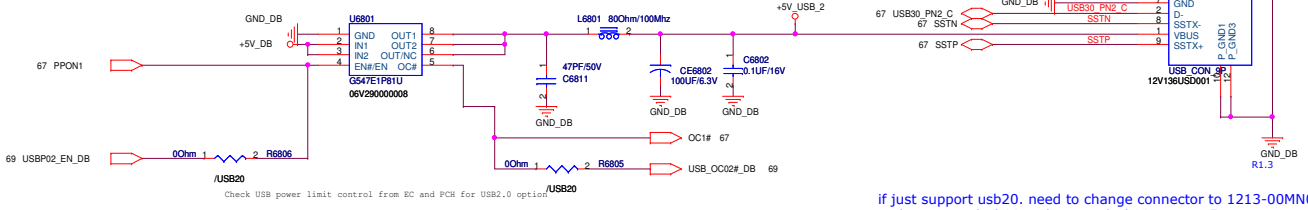


H=6.8mm

PEGATRON	Title : WLAN/ 3G	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 66 of 99	


Vout=0.8*(1+IO1_R618/IO1_R17)=0.8*(1+0.316)=1.0528
+1.05V_USB30
+3V
+3V_USB30
U6702
UP7704U8
uPD720200
Near Connector
ER1.33
ER1.31
U6705
AZ1045_04F
U6701
UPD720200AF1-DAP-SSA
02V0Q0000001 EIH31 : 020Q-0019000 UPD720200AF1-DAP-A
U6703
PM25LD512C-SCE
05V000000004
X6701
24MHZ
07V080000009
T6418
200-> SMIB
Q6704B
UM6K1N
Q6704A
Trace Direction
PEGATRON
Title : System Setting
Engineer: JAY TSAI
<OrgName>
Size: Custom
Project Name: EIH31
Rev: 1.3
Date: Friday, December 17, 2010
Sheet 67 of 99

USB ports



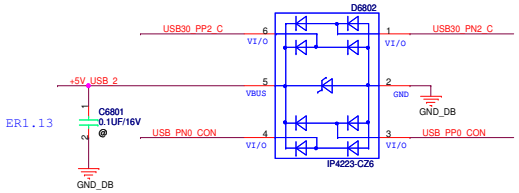
Check USB power limit control from EC and PCH for USB2.0 option

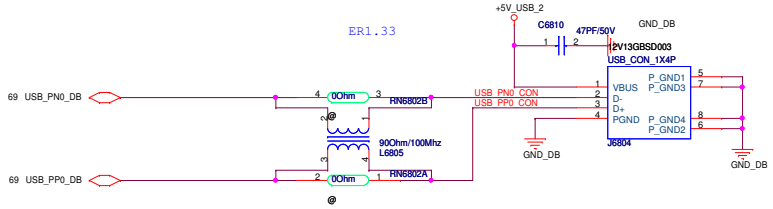
Boston:GPIO82:USBSLP_EN#,check KBID0

Boston:GPIO14:USB_OC2#_EC

BOM by USB 3.0 must change the U5201 for active HI solution.

if just support usb20. need to change connector to 1213-00MN000 and unmount /usb30 and mount /usb20 in page 54

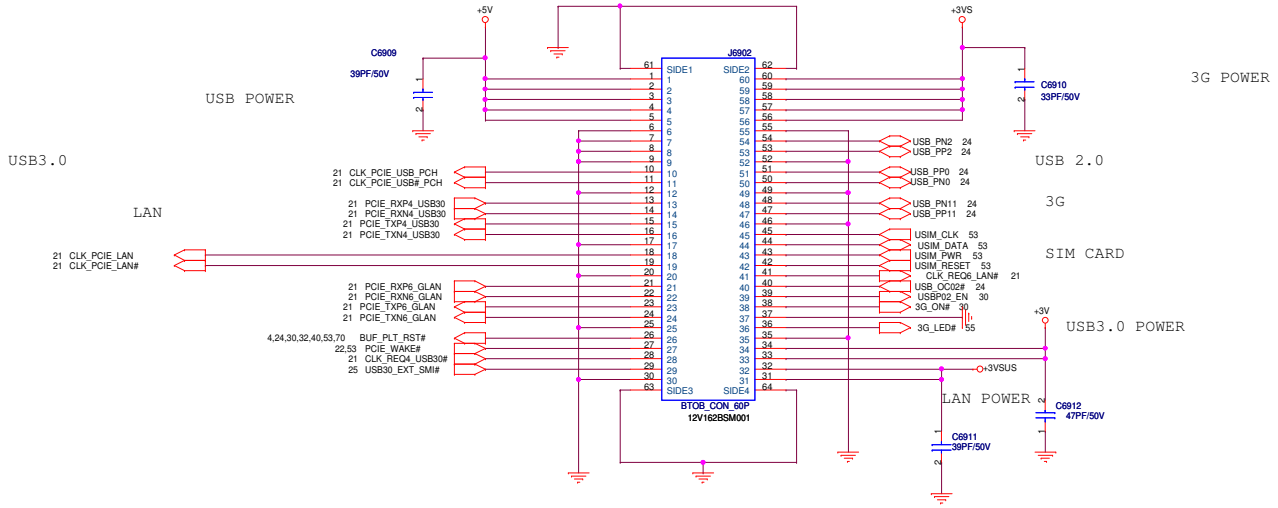




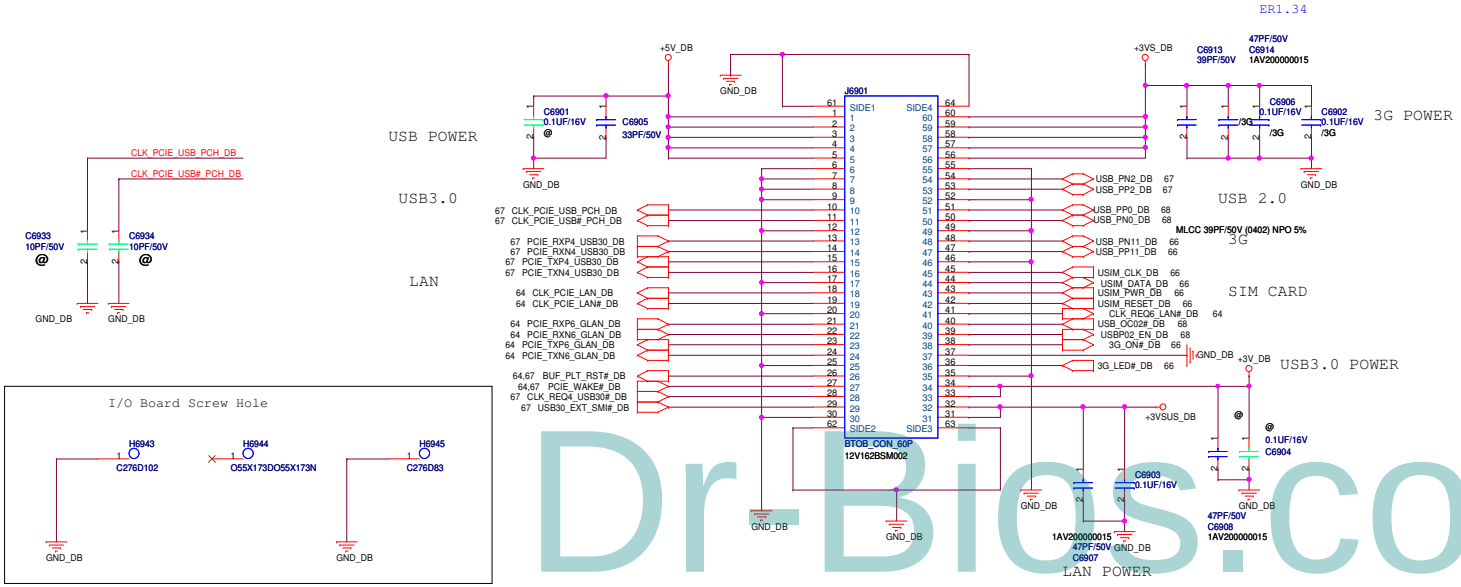
+5V_DB +5V_DB 67,69

PEGATRON	Title : USB_USB Port	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 68 of 99	

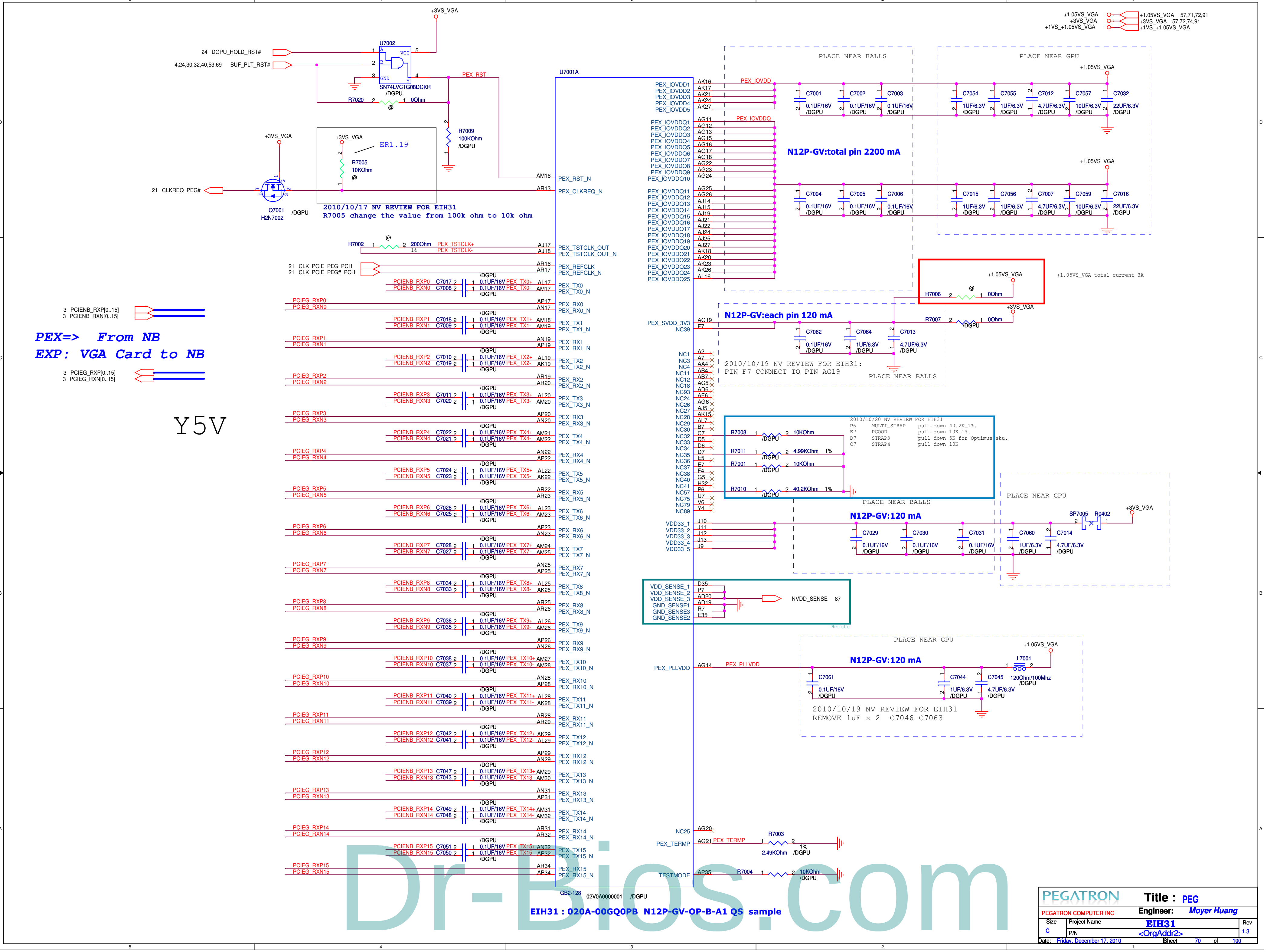
MB



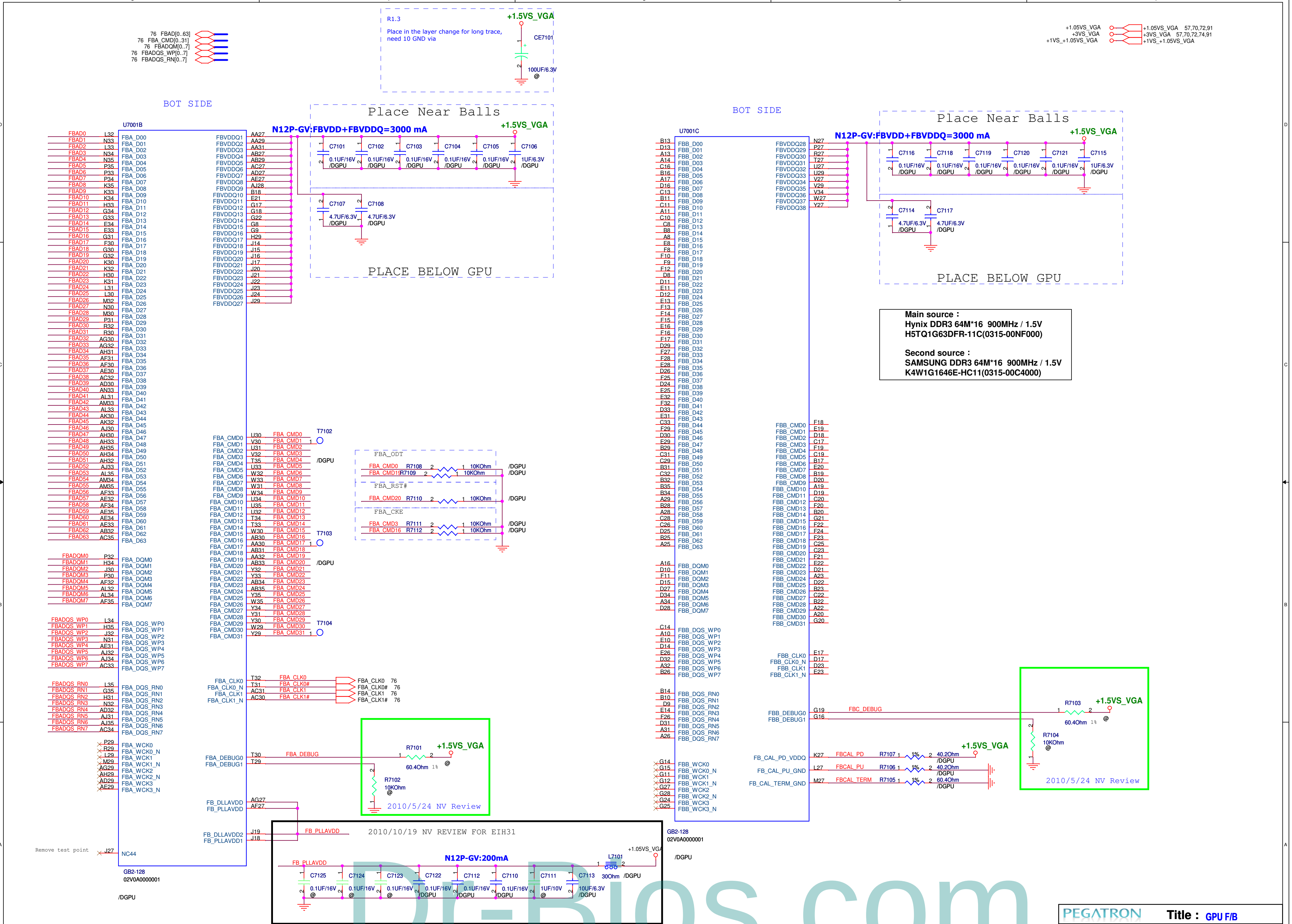
DB



PEGATRON	Title : B to B	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 69 of 99	



+1.05VS_VGA
+3VS_VGA
+1VS_+1.05VS_VGA
+1.05VS_VGA 57,71,72,91
+3VS_VGA 57,72,74,91
+1VS_+1.05VS_VGA
24 DGPU_HOLD_RST#
4,24,30,32,40,53,69 BUF_PLT_RST#
U7002
SN74LVC1G08DCKR
/DGPU
PEX_RST
R7020 0Ohm
R7009 100KOhm /DGPU
ER1.19
R7005 10KOhm
21 CLKREQ_PEG#
Q7001 H2N7002 /DGPU
2010/10/17 NV REVIEW FOR EIH31
R7005 change the value from 100k ohm to 10k ohm
U7001A
PEX_RST_N
PEX_CLKREQ_N
PLACE NEAR BALLS
PLACE NEAR GPU
PEX_IOVDD
PEX_IOVDDQ
N12P-GV:total pin 2200 mA
R7002 200Ohm 1%
PEX_TSTCLK+
PEX_TSTCLK-
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
21 CLK_PCIE_PEG_PCH
21 CLK_PCIE_PEG#_PCH
PEX_REFCLK
PEX_REFCLK_N
3 PCIENB_RXP[0..15]
3 PCIENB_RXN[0..15]
PEX=> From NB
EXP: VGA Card to NB
3 PCIEG_RXP[0..15]
3 PCIEG_RXN[0..15]
Y5V
R7006 0Ohm
+1.05VS_VGA total current 3A
N12P-GV:each pin 120 mA
PEX_SVDD_3V3
R7007 0Ohm
2010/10/19 NV REVIEW FOR EIH31:
PIN F7 CONNECT TO PIN AG19
2010/10/20 NV REVIEW FOR EIH31
P6 MULTI_STRAP pull down 40.2K_1%.
E7 PGOOD pull down 10K_1%.
D7 STRAP3 pull down 5K for Optimus sku.
C7 STRAP4 pull down 10K
R7008 10KOhm
R7011 4.99KOhm 1%
R7001 10KOhm
R7010 40.2KOhm 1%
N12P-GV:120 mA
SP7005 R0402
VDD_SENSE_1
VDD_SENSE_2
VDD_SENSE_3
GND_SENSE1
GND_SENSE3
GND_SENSE2
NVDD_SENSE 87
Remote
PEX_PLLVDD
L7001 120Ohm/100Mhz /DGPU
2010/10/19 NV REVIEW FOR EIH31
REMOVE 1uF x 2 C7046 C7063
PEX_TERMP
R7003 2.49KOhm 1% /DGPU
TESTMODE
R7004 10KOhm /DGPU
GB2-128 02V0A000001 /DGPU
EIH31 : 020A-00GQ0PB N12P-GV-OP-B-A1 QS sample
PEGATRON
PEGATRON COMPUTER INC
Title : PEG
Engineer: Moyer Huang
Size C
Project Name EIH31
P/N <OrgAddr2>
Rev 1.3
Date: Friday, December 17, 2010 Sheet 70 of 100


R1.3
Place in the layer change for long trace, need 10 GND via
+1.5VS_VGA
CE7101
100UF/6.3V
BOT SIDE
Place Near Balls
U7001B
N12P-GV:FBVDD+FBVDDQ=3000 mA
PLACE BELOW GPU
FBA_ODT
FBA_RST#
FBA_CKE
T7102
T7103
T7104
/DGPU
2010/5/24 NV Review
2010/10/19 NV REVIEW FOR EIH31
N12P-GV:200mA
+1.05VS_VGA
L7101
30Ohm
Remove test point
GB2-128
02V0A0000001
U7001C
Main source：
Hynix DDR3 64M*16 900MHz / 1.5V
H5TQ1G63DFR-11C(0315-00NF000)
Second source：
SAMSUNG DDR3 64M*16 900MHz / 1.5V
K4W1G1646E-HC11(0315-00C4000)
+1.05VS_VGA 57,70,72,91
+3VS_VGA 57,70,72,74,91
+1VS_+1.05VS_VGA

PEGATRON

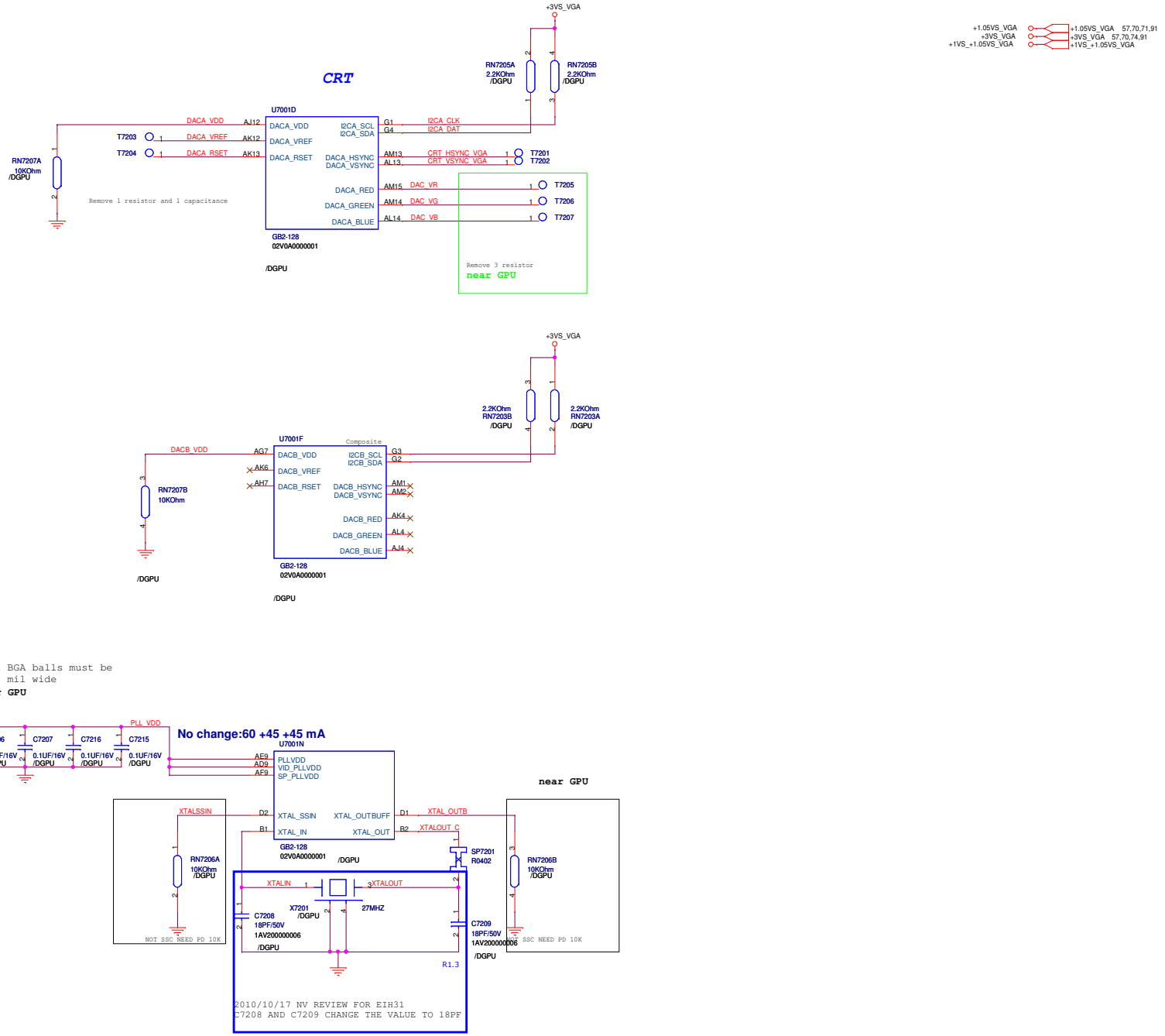
PEGATRON COMPUTER INC

Title： GPU F/B

Engineer: Moyer Huang

Size	Project Name	Rev
C	EIH31	1.3
	P/N <OrgAddr2>	

Date: Friday, December 17, 2010 Sheet 71 of 100



PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Moyer Huang		
Size: C	Project Name: EIH31		Rev: 1.3
	P/N: <OrgAddr2>		
Date: Friday, December 17, 2010	Sheet 72 of 100		

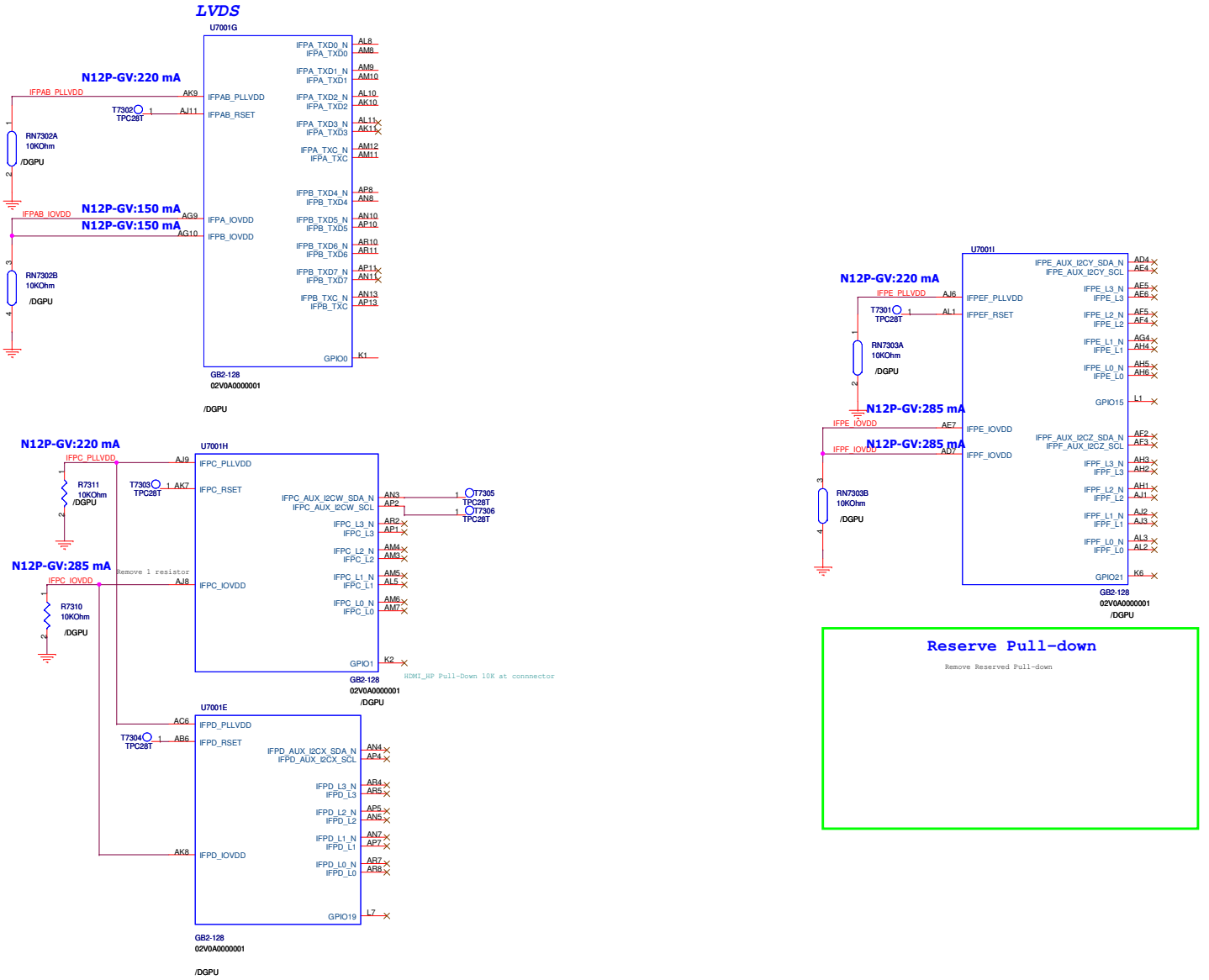


Table 7.1 N11x Fermi Family Display Link Summary

Link A	Link B	Link C	Link D	Link E	Link F
LVDS (Single Link or Dual Link with IFPB)	LVDS (Dual Link with IFPA)	DisplayPort, HDMI	DisplayPort, eDP	DisplayPort, DVI (Single Link or Dual Link with IFPF), HDMI	DisplayPort, DVI (Dual Link with IFPE)

IFPx	A	B	C	D	E	F
MASERATI						

PEGATRON
PEGATRON COMPUTER INC
Title : Connector, LED
Engineer: Moyer Huang
Size C | Project Name EIH31 | Rev 1.3
P/N <OrgAddr2>
Date: Friday, December 17, 2010 | Sheet 73 of 100

+1.05VS_VGA
+3VS_VGA
+1.05VS_VGA

+1.05VS_VGA +1.05VS_VGA 57,70,71,72,91
+3VS_VGA +3VS_VGA 57,70,72,91
+1.05VS_VGA +1.05VS_VGA 57,70,71,72,91

GPIO USAGE

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	IFPAB HOTPLUG DETECT
1	IN	N/A	IFPC HOTPLUG DETECT
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD ALTV0
6	OUT	HIGH	NVVDD ALTV1
7	OUT	HIGH	FBVDDQ ALTV
8	IN/OUT	LOW	OVERTEMP ALERT
9	OUT	LOW	THERMAL ALERT
10	OUT	HIGH	FB_VREF CONTROL
11	OUT	HIGH	RESERVED
12	IN	N/A	AC DETECT
13	OUT	LOW	LOAD STEP DOWN
14	OUT	HIGH	LOAD STEP UP
15	IN	N/A	IFPE HOTPLUG DETECT
16	IN	N/A	FAN PWM OUT
17	IN	N/A	FAN TACH IN
18	IN	N/A	RESERVED
19	IN	N/A	IFPD HOTPLUG DETECT
20	IN	N/A	RESERVED
21	IN	N/A	IFPF HOTPLUG DETECT
22	IN	N/A	RESERVED
23	IN	N/A	RESERVED
24	IN	N/A	RESERVED

ER1.28

+3VS_VGA
R7414 45.3KOhm 1% /DGPU
R7416 10KOhm 1% @
R7402 34.8KOhm 1% @
R7415 45.3KOhm 1% @
R7403 34.8KOhm 1% /DGPU
R7401 4.99KOhm 1% /DGPU
STRAP0
STRAP1
STRAP2
PUN_04193_V02

+3VS_VGA
R7422 5.1KOhm 1% @
R7427 10KOhm 1% /DGPU
R7410 10KOhm 1% /DGPU
R7420 15KOhm 1% /DGPU
R7419 10KOhm 1% @
R7411 15KOhm 1% @
ROM_SI
ROM_SO
ROM_SCLK

STRAP0

USER[3:0] 3 2 1 0 PANEL VS/HS

0	0	0	0 XGA +/-
0	0	0	1 XGA +/+
0	0	1	0 SXGA +/+
0	0	1	1 SXGA+ -/-
0	1	0	0 UXGA +/+
1	1	1	1 EDID N/A

STRAP1

3GIO_PAD_CFG_ADR[3:0] 3 2 1 0 PANEL

0	0	0	0 RESERVED
0	1	1	0 NOTEBOOK
.			
.			
1	1	1	1 RESERVED

STRAP2

LOGICAL BIT	
0	PCI_DEVID[0]
1	PCI_DEVID[1]
2	PCI_DEVID[2]
3	PCI_DEVID[3]

ROM_SI_RAMCONFIG (MONO RANK)

Hynix 64Mx16 -> ram_cfg = 0x2
Samsung 64Mx16 -> ram_cfg = 0x3
Hynix 128Mx16 -> ram_cfg = 0x6
Samsung 128Mx16 -> ram_cfg = 0x7

ROM_SO

LOGICAL BIT	
3	XCLK_417
2	FB_0_BAR_SIZE
1	SMB_ALT_ADDR
0	VGA_DEVICE

ROM_SCLK

LOGICAL BIT	
3	PCI_DEVID[4]
2	SUB_VENDER
1	SLOT_CLK_CFG
0	PEX_PLL_EN_TERM

5K PU 1000 PD 0000
10K PU 1001 PD 0001
15K PU 1010 PD 0010
20K PU 1011 PD 0011
25K PU 1100 PD 0100
30K PU 1101 PD 0101
35K PU 1110 PD 0110
45K PU 1111 PD 0111

N12P-GS : 0x0DF4
~10100
= PCI_DEVICE[4][3][2][1][0]

U7001M
GB2-128
02V0A0000001
/DGPU

+3VS_VGA
R7436 10KOhm /DGPU
CEC
ROM_CS_N C3 T7407
ROM_SI D3
ROM_SO C4
ROM_SCLK D4
STRAP0 W5
STRAP1 W7
STRAP2 V7
I2CH_SCL F6 I2CH_CLK
I2CH_SDA G6 I2CH_DAT
RN7444A 2.2KOhm /DGPU
RN7444B 2.2KOhm /DGPU
NC2 A5 Remove test point
BUFRST_N A4
NC31 C5
GND1 AK14
GND192 K9
R7441 10KOhm @
R7406 40.2KOhm 1% N9 /DGPU
R7407 40.2KOhm 1% M9 /DGPU
MULTI_STRAP_REF0_GND
MULTI_STRAP_REF1_GND

U7001L
GB2-128
02V0A0000001
/DGPU

T7437 VGA_THERMDN B4 THERMDN
T7438 VGA_THERMDP B5 THERMDP
I2CS_SCL E2
I2CS_SDA E1
I2CC_SCL E3
I2CC_SDA E4
SMB_CLK_VGA
SMB_DAT_VGA
RN7446B 2.2KOhm /DGPU
RN7446A 2.2KOhm /DGPU
RN7447B 2.2KOhm /DGPU
RN7447A 2.2KOhm /DGPU

Q7401A UM6K1N /DGPU
UM6K1N Q7401B /DGPU
SMB1_CLK 28,30
SMB1_DAT 28,30
THERMAL
Pull high +3VS at system

RN7448A 10KOhm /DGPU
RN7448B 10KOhm /DGPU
GPIO2 K3 T7418
GPIO3 H3 L_VDDEN_VGA
GPIO4 H2 LCD_BKEN_VGA
GPIO5 H1 GPU_VID_0
GPIO6 H4 GPU_VID_1
GPIO7 H5 T7420
GPIO8 H6 SL7401 SL7402 R6402 VGA_OVERTEMP# R
GPIO9 J7 R6402 THERM_ALERT#
GPIO10 K4 T7423
GPIO11 K5 T7422
GPIO12 H7 AC_BATT#
GPIO13 J4 T7429
GPIO14 J6 T7430
R7429 10KOhm /DGPU
Remove 2 test point
GPU_VID_0 87
GPU_VID_1 87
VGA_OVERTEMP# 32
Pull high +3VS at system R1.3
Q7402 H2N7002 /DGPU

T7424 AP14 JTAG_TCK
T7425 AR14 JTAG_TMS
T7426 AN14 JTAG_TDI
T7421 AN16 JTAG_TDO
AP16 JTAG_TRST_N
R7440 10KOhm /DGPU

GPIO16 L2 T7431
GPIO17 L4 T7432
GPIO18 M4 VPS
R7431 10KOhm @
GPIO20 L5 T7427
GPIO22 L6 T7428
GPIO23 M6 T7434
GPIO24 M7 T7435
L_VDDEN_VGA
LCD_BKEN_VGA
GPU_VID_0
GPU_VID_1
R7433 10KOhm @
R7430 10KOhm @
R7432 10KOhm @
R7437 10KOhm @
ER1.29

GPU_VID	VID1	VID0	+VGA_VCORE
Low	0	0	0.85V
Med	0	1	1V
High	1	0	1.025V

Q7403 H2N7002 @
AC_BATT#
AC_IN_OC 30,88,90
Q7404 H2N7002 @
VPS
VPS_EC 30

ER 1129
Need to check function of VPS with nVidia

Vendor REQUEST

PEGATRON
PEGATRON COMPUTER INC
Title : Connector, LED
Engineer: Moyer Huang
Size C
Project Name EIH31
P/N <OrgAddr2>
Rev 1.3
Date: Friday, December 17, 2010
Sheet 74 of 100

+1.05VS_VGA
+3VS_VGA
+1.05VS_VGA

+1.05VS_VGA 57,70,71,72,91
+3VS_VGA 57,70,72,74,91
+1.05VS_VGA 57,70,71,72,91

U7001O

GB2-128
02V0A0000001

/DGPU

+VGA_VCORE

U7001P

GB2-128
02V0A0000001

/DGPU

+VGA_VCORE

20.3 A

C7508 0.01UF/25V /DGPU
C7505 0.01UF/25V /DGPU
C7506 0.01UF/25V /DGPU
C7509 0.01UF/25V /DGPU
C7510 0.01UF/25V /DGPU
C7511 0.01UF/25V /DGPU
C7523 0.01UF/25V /DGPU
C7524 0.01UF/25V /DGPU
C7513 0.022UF/16V /DGPU
C7514 0.022UF/16V /DGPU
C7518 0.022UF/16V /DGPU
C7519 0.047UF/16V /DGPU
C7507 0.047UF/16V /DGPU
C7512 0.047UF/16V /DGPU
C7501 0.1UF/16V /DGPU
C7502 0.1UF/16V /DGPU
C7520 0.22UF/10V /DGPU
C7521 0.22UF/10V /DGPU
C7522 0.22UF/10V /DGPU
C7503 1UF/6.3V /DGPU
C7504 4.7UF/6.3V /DGPU
C7515 10UF/6.3V /DGPU
C7516 10UF/6.3V /DGPU
C7517 22UF/6.3V /DGPU
C7525 47UF/6.3V /DGPU

PLACE Under GPU

NV Design Guide	Maserati
0.01U x 8	0.01U x 8
0.022U x 3	0.022U x 3
0.047U x 3	0.047U x 3
0.1U x 2	0.1U x 2
0.22U x 3	0.22U x 3
1U x 1	1U x 1
4.7U x 1	4.7U x 1
10U x 2	10U x 2
22U x 1	22U x 1
47U x 1	47U x 1

U7001J

R7502 10KOhm /DGPU

R7501 10KOhm /DGPU

GB2-128
02V0A0000001

/DGPU

U7001K

R7503 10KOhm /DGPU

R7504 10KOhm /DGPU

GB2-128
02V0A0000001

/DGPU

PEGATRON
PEGATRON COMPUTER INC

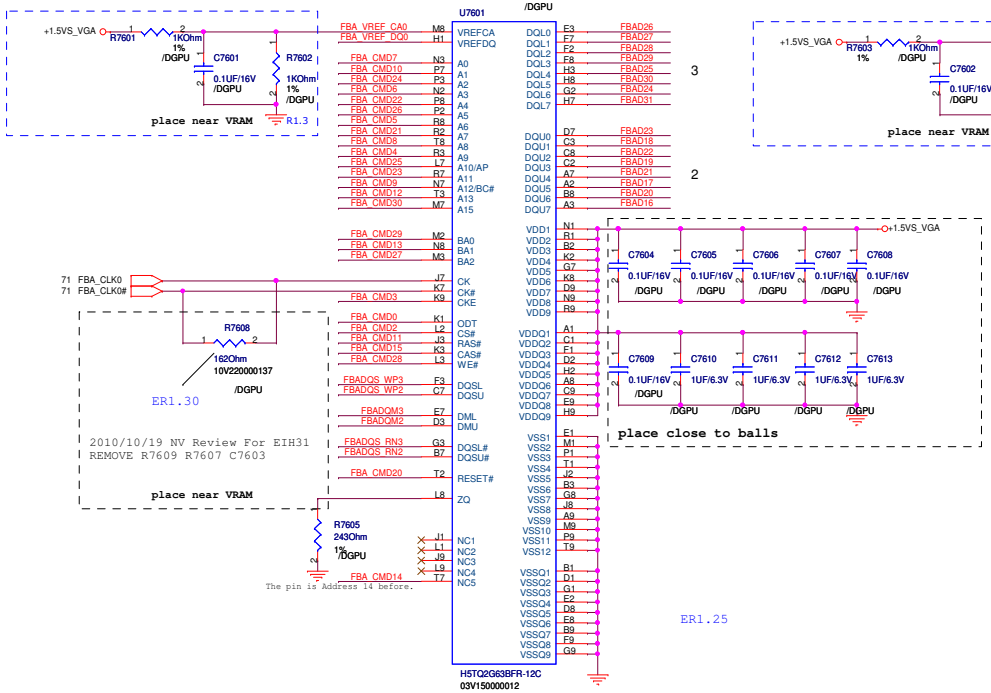
Title : GPU PWR/GND
Engineer: Moyer Huang

Size	Project Name	Rev
C	EIH31	1.3
	P/N <OrgAddr2>	

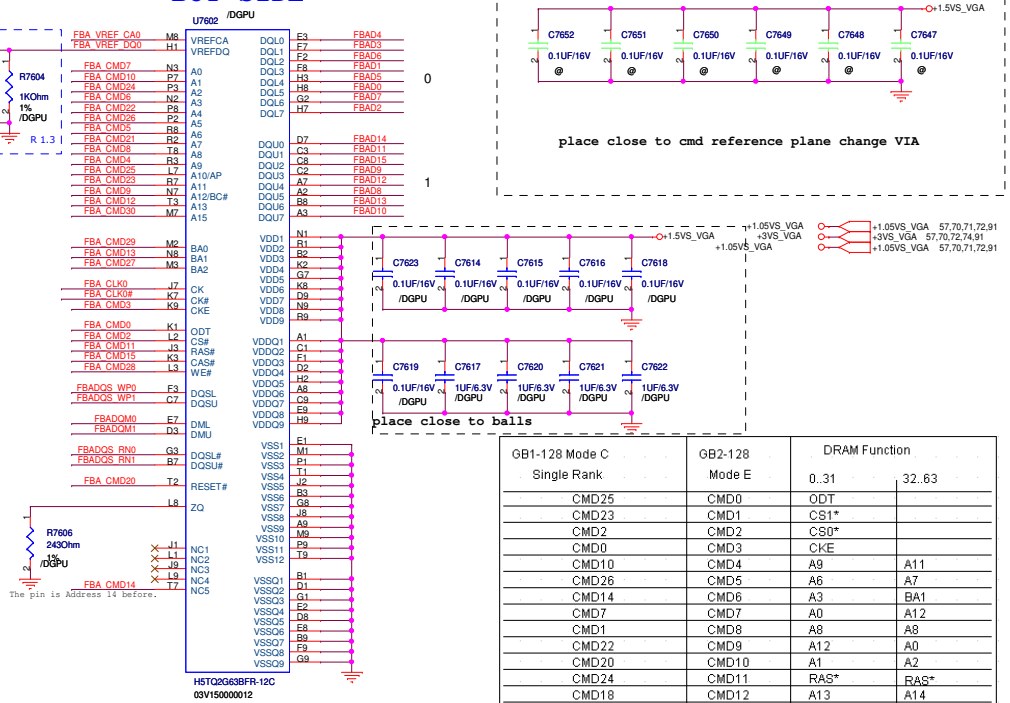
Date: Friday, December 17, 2010 Sheet 75 of 100

VRAM CH A

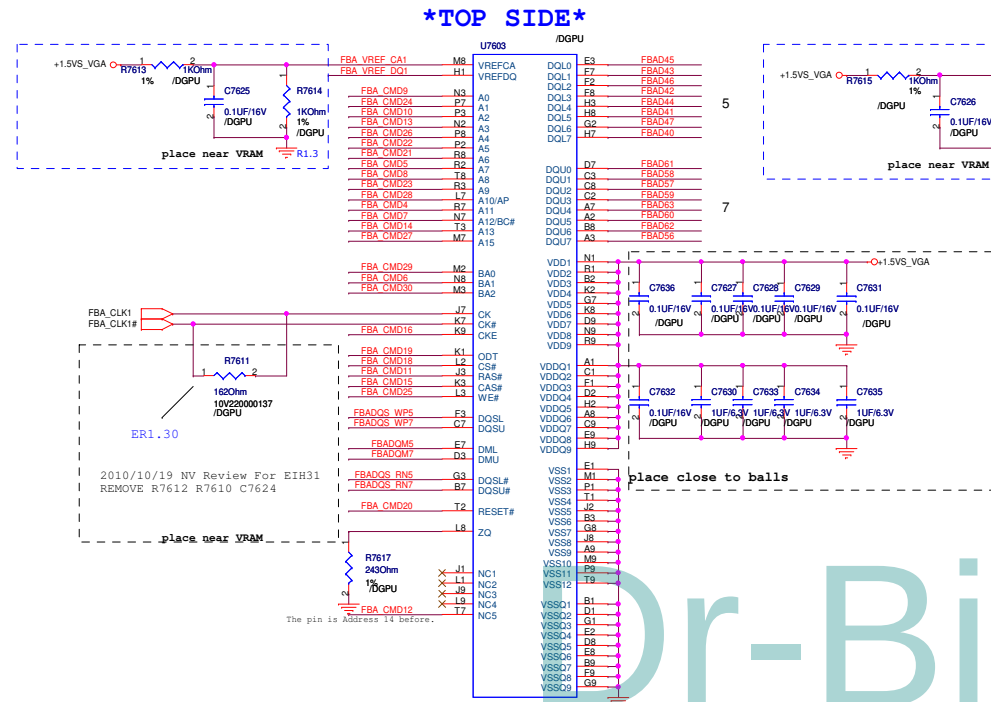
TOP SIDE



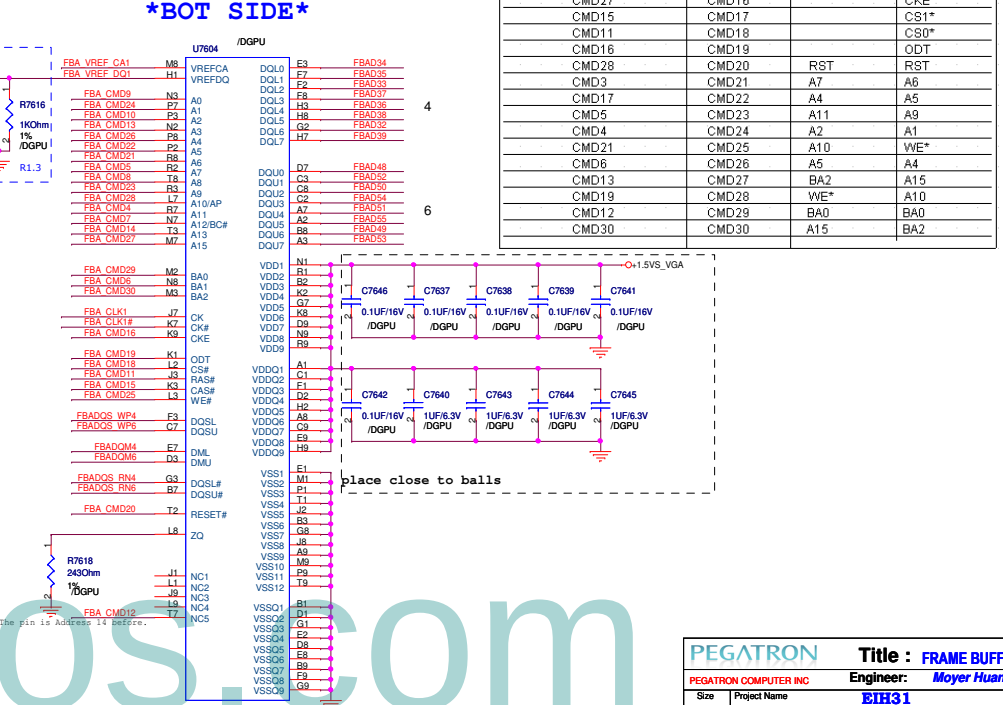
BOT SIDE



TOP SIDE



BOT SIDE



GB1-128 Mode C Single Rank	GB2-128 Mode E	DRAM Function 0..31	32..63
CMD25	CMD0	ODT	
CMD23	CMD1	CS1*	
CMD2	CMD2	CS0*	
CMD0	CMD3	CKE	
CMD10	CMD4	A9	A11
CMD26	CMD5	A6	A7
CMD14	CMD6	A3	BA1
CMD7	CMD7	A0	A12
CMD1	CMD8	A8	A8
CMD22	CMD9	A12	A0
CMD20	CMD10	A1	A2
CMD24	CMD11	RAS*	RAS*
CMD18	CMD12	A13	A14
CMD9	CMD13	BA1	A3
CMD29	CMD14	A14	A13
CMD8	CMD15	CAS*	CAS*
CMD27	CMD16		CKE
CMD15	CMD17		CS1*
CMD11	CMD18		CS0*
CMD16	CMD19		ODT
CMD28	CMD20	RST	RST
CMD3	CMD21	A7	A6
CMD17	CMD22	A4	A5
CMD5	CMD23	A11	A9
CMD4	CMD24	A2	A1
CMD21	CMD25	A10	WE*
CMD6	CMD26	A5	A4
CMD13	CMD27	BA2	A15
CMD19	CMD28	WE*	A10
CMD12	CMD29	BA0	BA0
CMD30	CMD30	A15	BA2

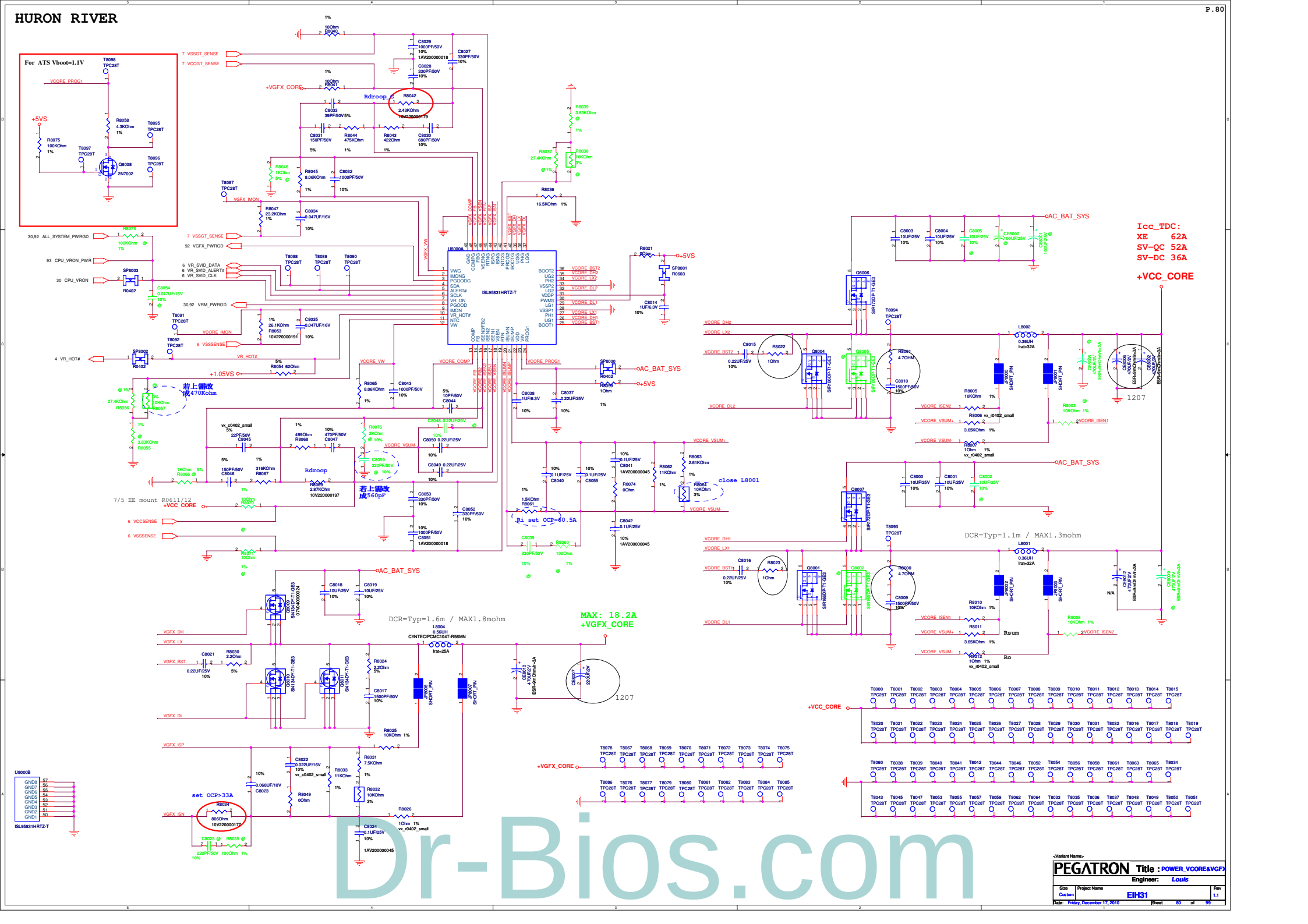
PEGATRON	Title :	FRAME BUFFER A	
PEGATRON COMPUTER INC	Engineer:	Moyer Huang	
Size: C	Project Name: EIH31		Rev: 1.3
	P/N: <OrgAddr2>		
Date: Friday, December 17, 2010	Sheet 76 of 100		

PEGATRON	Title : FRAME BUFFER C		
PEGATRON COMPUTER INC	Engineer: Moyer Huang		
Size: C	Project Name: EIH31		Rev: 1.3
	P/N: <OrgAddr2>		
Date: Friday, December 17, 2010	Sheet 77 of 100		

PEGATRON	Title : FRAME BUFFER C
PEGATRON COMPUTER INC	Engineer: Moyer Huang
Size: A	Project Name: EIH31
	P/N: <OrgAddr2>
Rev: 1.3	
Date: Friday, December 17, 2010	Sheet 78 of 100

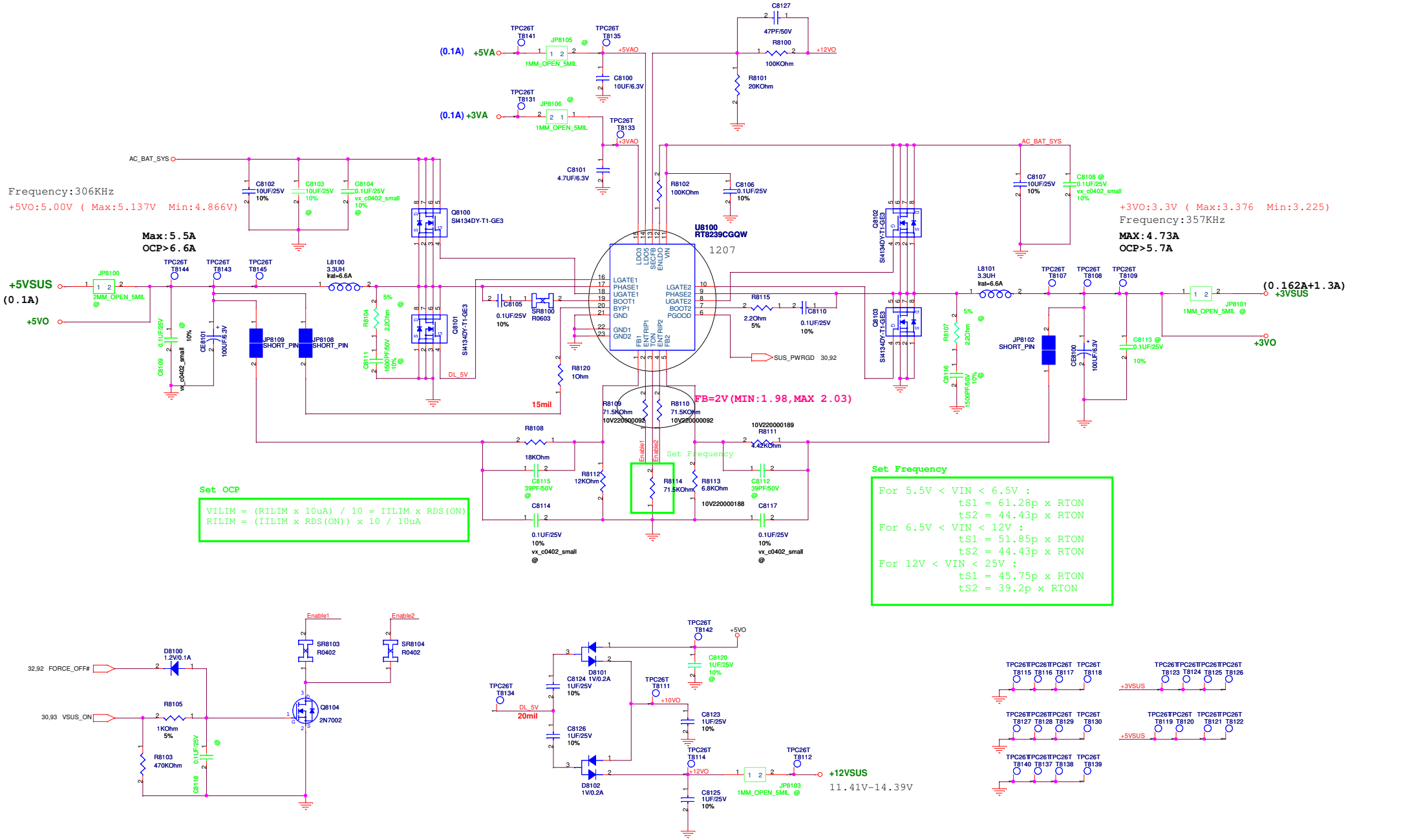
PEGATRON	Title : FRAME BUFFER C
PEGATRON COMPUTER INC	Engineer: Moyer Huang
Size: A	Project Name: EIH31
	P/N: <OrgAddr2>
Rev: 1.3	
Date: Friday, December 17, 2010	Sheet 79 of 100

HURON RIVER



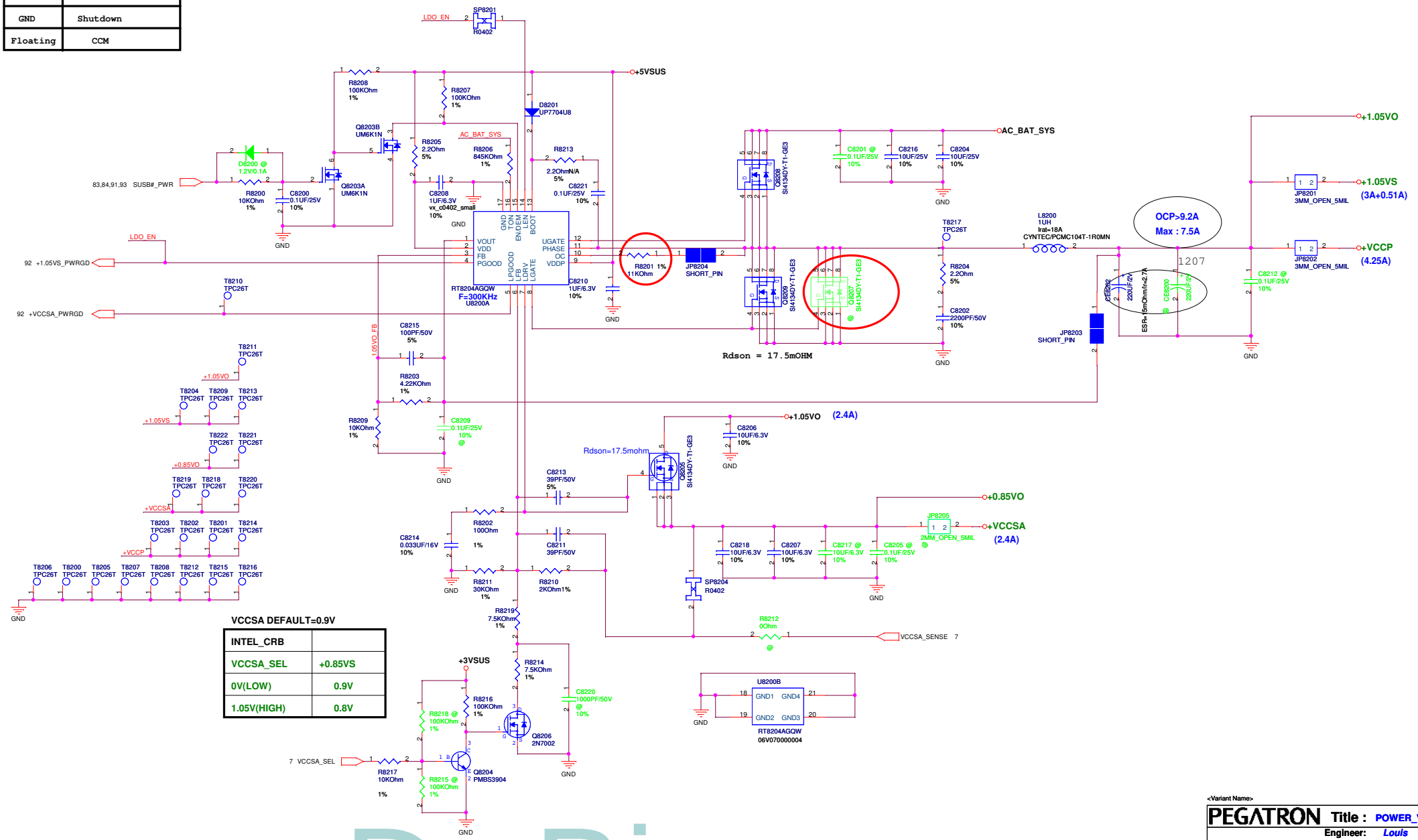
Title	POWER_VCORE&VGFX
Engineer	Louis
Size	Custom
Project Name	EIH31
Rev	1.1
Date	Friday, December 17, 2010
Sheet	80 of 99

PEGATRON


Frequency:306KHz
+5VO:5.00V (Max:5.137V Min:4.866V)
Max:5.5A
OCP>6.6A
+3VO:3.3V (Max:3.376 Min:3.225)
Frequency:357KHz
MAX:4.73A
OCP>5.7A
U8100
RT8239CGQW
1207
+5VSUS
(0.1A)
+5VO
(0.1A) +5VA
(0.1A) +3VA
AC_BAT_SYS
(0.162A+1.3A)
+3VSUS
+3VO
SUS_PWRGD 30,92
FB=2V(MIN:1.98,MAX 2.03)
15mil
20mil
Set Frequency
Set OCP
VILIM = (RILIM x 10uA) / 10 = IILIM x RDS(ON)
RILIM = (IILIM x RDS(ON)) x 10 / 10uA
For 5.5V < VIN < 6.5V :
tS1 = 61.28p x RTON
tS2 = 44.43p x RTON
For 6.5V < VIN < 12V :
tS1 = 51.85p x RTON
tS2 = 44.43p x RTON
For 12V < VIN < 25V :
tS1 = 45.75p x RTON
tS2 = 39.2p x RTON
32,92 FORCE_OFF#
30,93 VSUS_ON
+12VSUS
11.41V~14.39V

VCCP & VCCSA POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation'
GND	Shutdown
Floating	CCM



<Variant Name>

PEGATRON Title : POWER_VCCP

Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Friday, December 17, 2010 Sheet 82 of 94

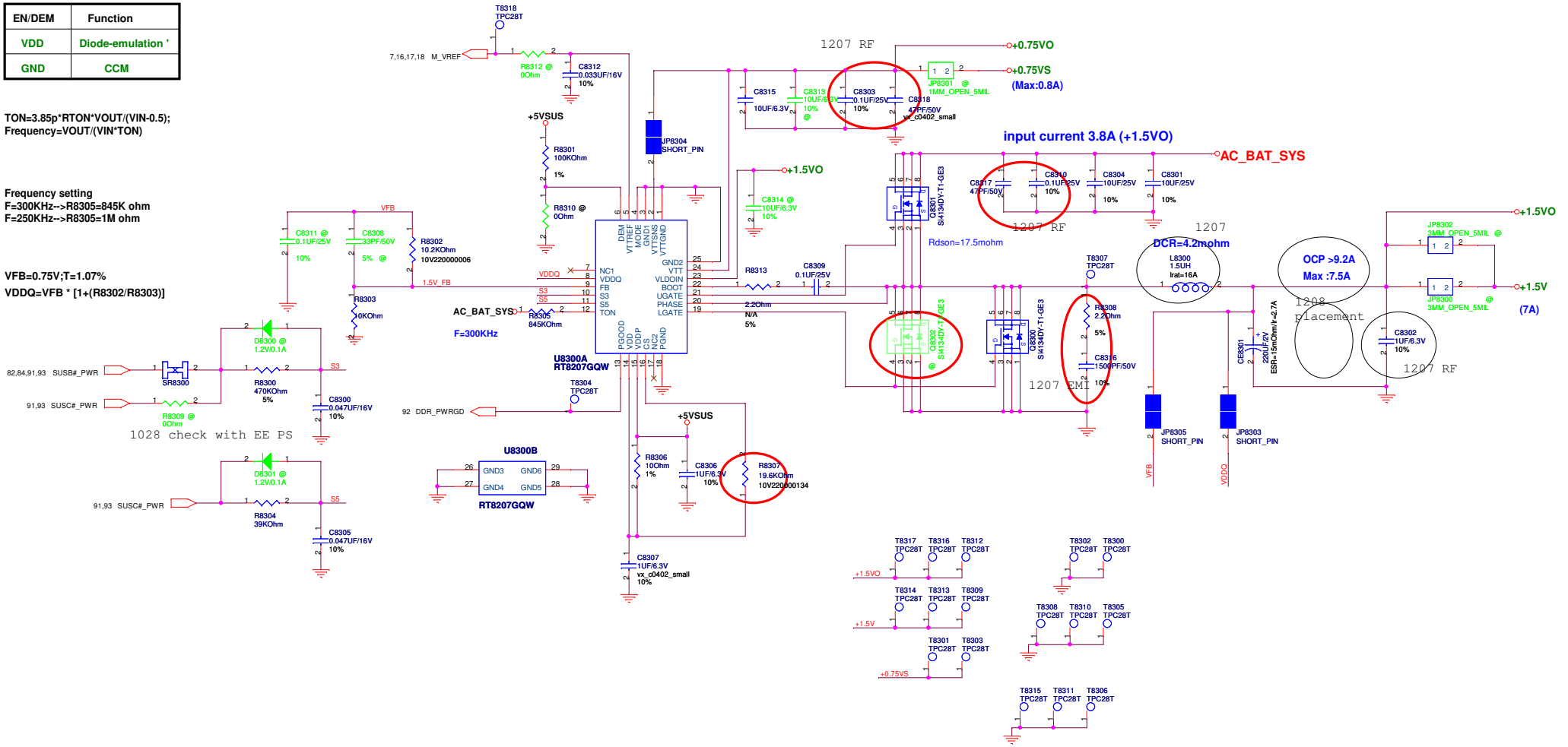
DDR & VTT POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation '
GND	CCM

TON=3.85p*RTON*VOUT/(VIN-0.5);
Frequency=VOUT/(VIN*TON)

Frequency setting
F=300KHz-->R8305=845K ohm
F=250KHz-->R8305=1M ohm

VFB=0.75V;T=1.07%
VDDQ=VFB * [1+(R8302/R8303)]



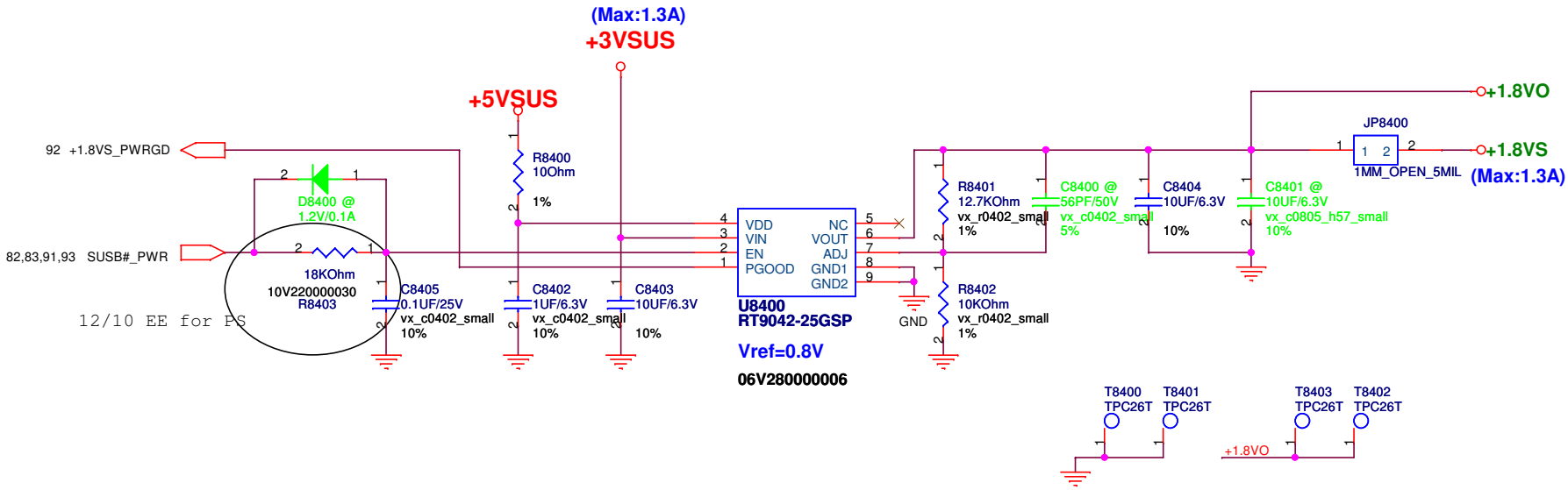
<Variant Name>

PEGATRON Title : POWER_DDR & VTT
Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Friday, December 17, 2010 Sheet 83 of 94

1.8VS POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_1.8VS

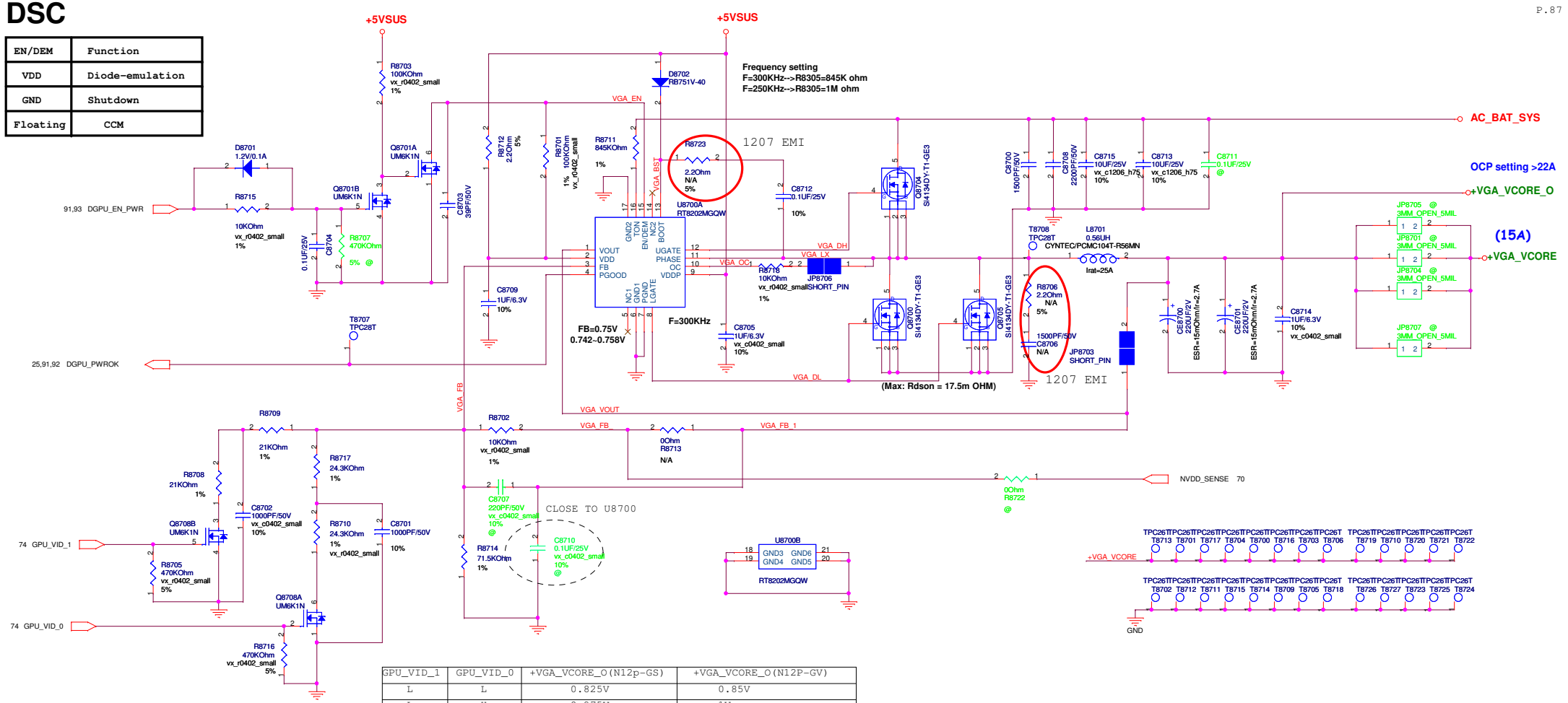
Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Friday, December 17, 2010 Sheet 84 of 94

DSC

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



GPU_VID_1	GPU_VID_0	+VGA_VCORE_O(N12p-GS)	+VGA_VCORE_O(N12P-GV)
L	L	0.825V	0.85V
L	H	0.975V	1V
H	L	1V	1.025V
H	H	X	

<Variant Name>

PEGATRON Title : POWER_VGA_CORE

Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

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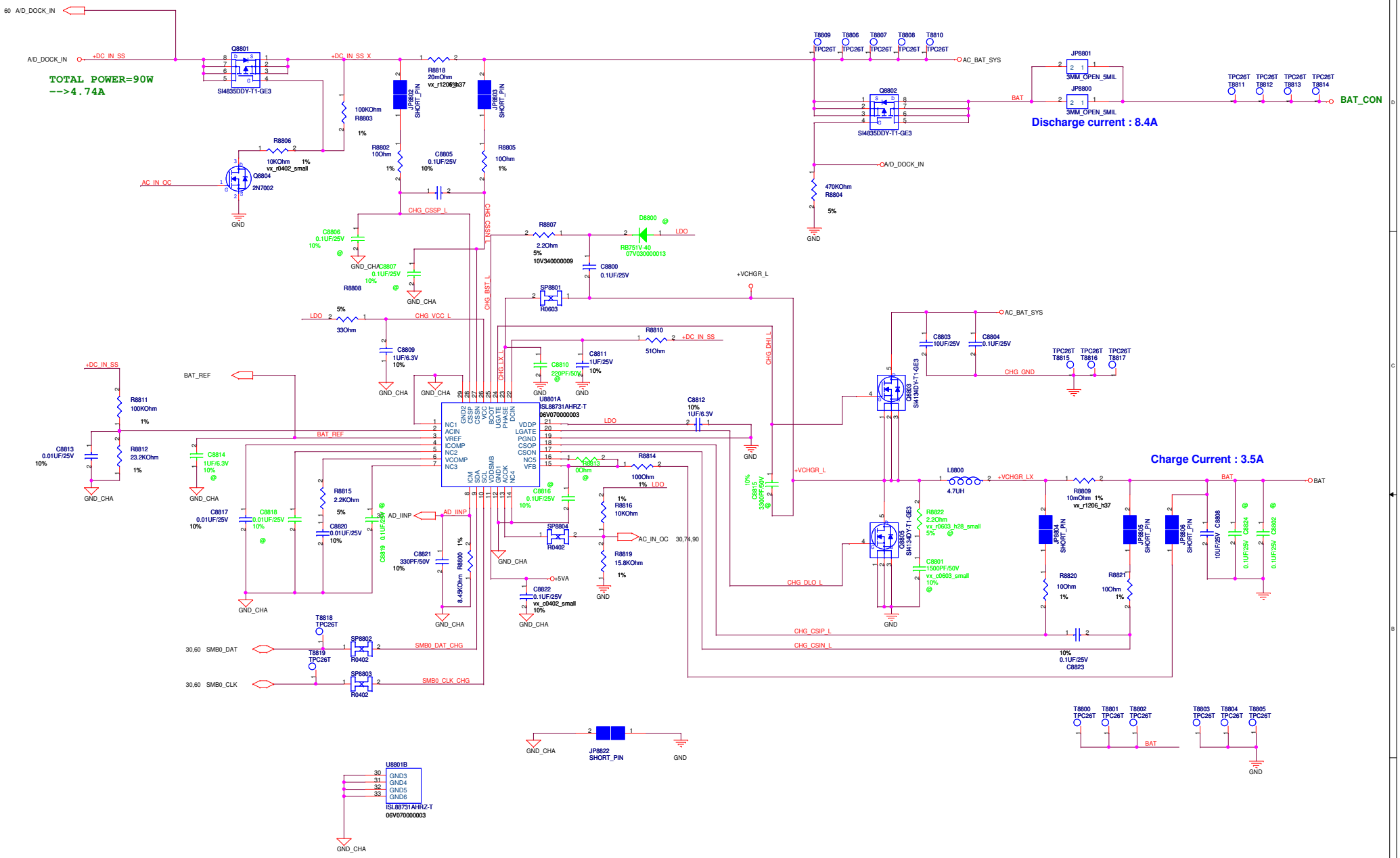
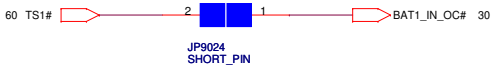
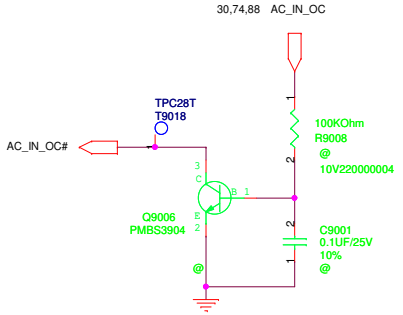

60 A/D_DOCK_IN
A/D_DOCK_IN
+DC_IN_SS
+DC_IN_SS_X
TOTAL POWER=90W
-->4.74A
Q8801
SI4835DDY-T1-GE3
R8818
20mOhm
vx_r1206_h37
JP8802
SHORT_PIN
JP8803
SHORT_PIN
100KOhm
R8803
1%
R8806
10KOhm
vx_r0402_small
Q8804
2N7002
AC_IN_OC
R8802
10Ohm
C8805
0.1UF/25V
R8805
10Ohm
CHG_CSSP_L
C8806
0.1UF/25V
C8807
0.1UF/25V
R8808
GND_CHA
CHG_CSSN_L
R8807
2.2Ohm
10V340000009
D8800
RB751V-40
07V030000013
LDO
C8800
0.1UF/25V
SP8801
R0603
+VCHGR_L
CHG_BST_L
LDO
33Ohm
CHG_VCC_L
C8809
1UF/6.3V
C8810
220PF/50V
C8811
1UF/25V
R8810
51Ohm
U8801A
ISL88731AHRZ-T
06V070000003
C8812
1UF/6.3V
CHG_DHI_L
CHG_LX_L
BAT_REF
R8811
100KOhm
R8812
23.2KOhm
C8813
0.01UF/25V
C8814
1UF/6.3V
C8817
0.01UF/25V
C8818
0.01UF/25V
R8815
2.2KOhm
C8820
0.01UF/25V
C8819
0.1UF/25V
AD_IINP
C8821
330PF/50V
R8800
8.45KOhm
C8816
0.1UF/25V
R8813
0Ohm
R8814
100Ohm
R8816
10KOhm
R8819
15.8KOhm
SP8804
R0402
AC_IN_OC
30,74,90
+5VA
C8822
0.1UF/25V
vx_c0402_small
T8818
TPC26T
T8819
TPC26T
30,60 SMB0_DAT
30,60 SMB0_CLK
SP8802
SP8803
R0402
SMB0_DAT_CHG
SMB0_CLK_CHG
U8801B
GND3
GND4
GND5
GND6
ISL88731AHRZ-T
06V070000003
JP8822
SHORT_PIN
T8809
T8806
T8807
T8808
T8810
TPC26T
AC_BAT_SYS
Q8802
SI4835DDY-T1-GE3
JP8801
3MM_OPEN_5MIL
JP8800
3MM_OPEN_5MIL
BAT
BAT_CON
Discharge current : 8.4A
470KOhm
R8804
5%
A/D_DOCK_IN
C8803
10UF/25V
C8804
0.1UF/25V
CHG_GND
TPC26T
T8811
T8812
T8813
T8814
TPC26T
T8815
T8816
T8817
Q8803
SI4134DY-T1-GE3
Charge Current : 3.5A
L8800
4.7UH
+VCHGR_LX
R8809
10mOhm
vx_r1206_h37
R8822
2.2Ohm
vx_r0603_h28_small
5%
Q8805
SI4134DY-T1-GE3
C8801
1500PF/50V
vx_c0603_small
10%
JP8804
SHORT_PIN
JP8805
SHORT_PIN
JP8806
SHORT_PIN
R8820
10Ohm
R8821
10Ohm
C8808
10UF/25V
C8824
0.1UF/25V
C8802
0.1UF/25V
C8823
0.1UF/25V
CHG_CSIP_L
CHG_CSIN_L
CHG_DLO_L
T8800
T8801
T8802
T8803
T8804
T8805
TPC26T
GND
GND_CHA

BATTERY IN DETECT



ADAPTER IN DETECT



<Variant Name>

PEGATRON Title : POWER_DETECT

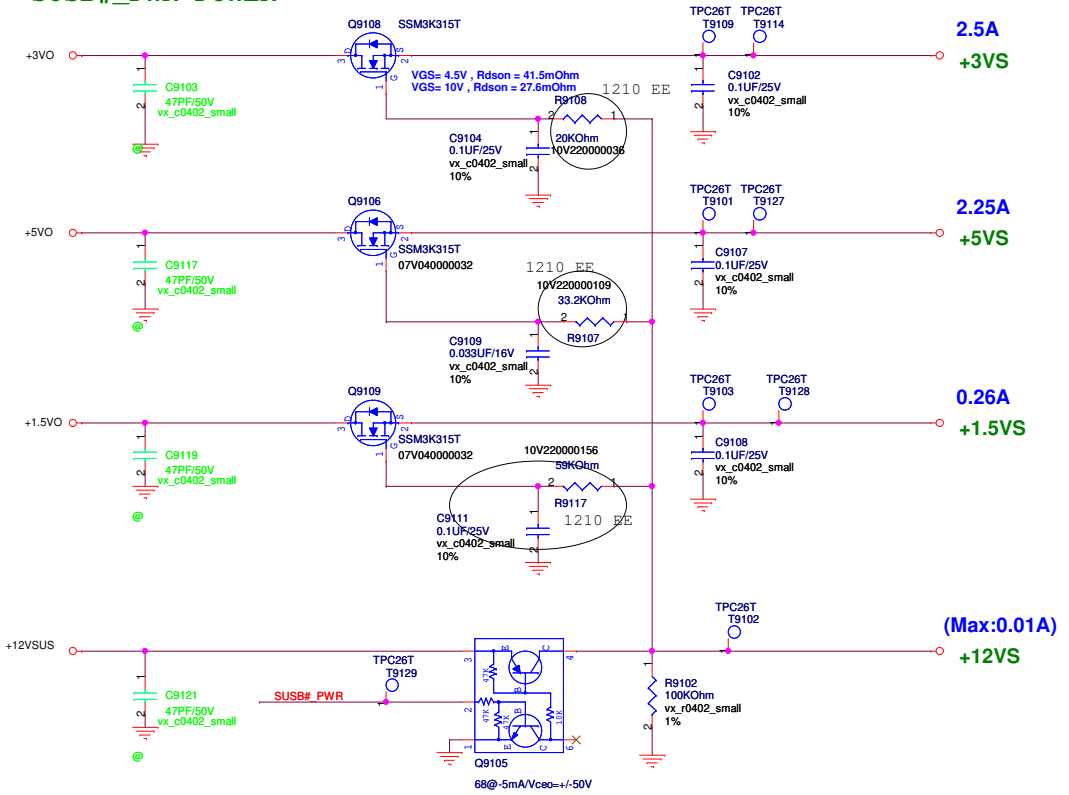
Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

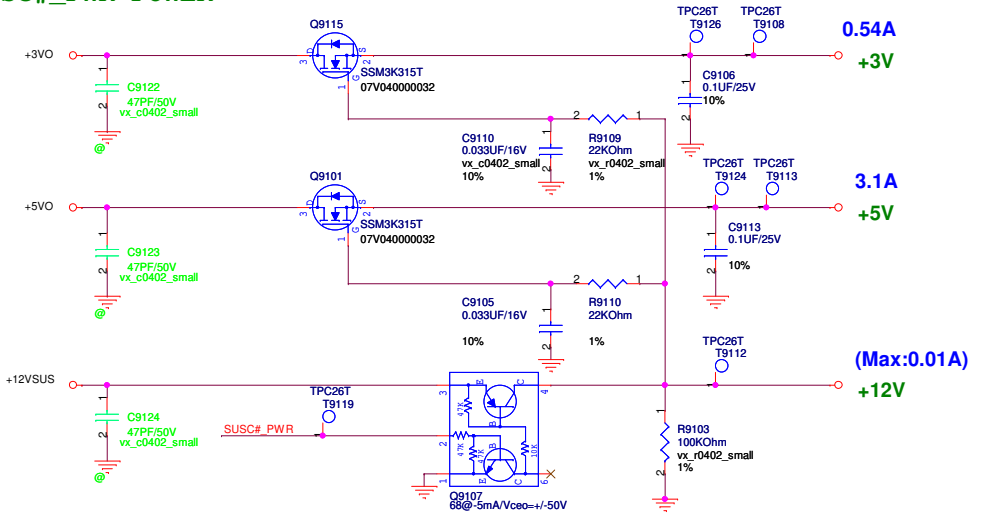
Date: Friday, December 17, 2010 Sheet 90 of 99

Ron = 41.5 mΩ (max) (@VGS = 4.5 V)
Ron = 27.6 mΩ (max) (@VGS = 10 V)

SUSB#_PWR POWER

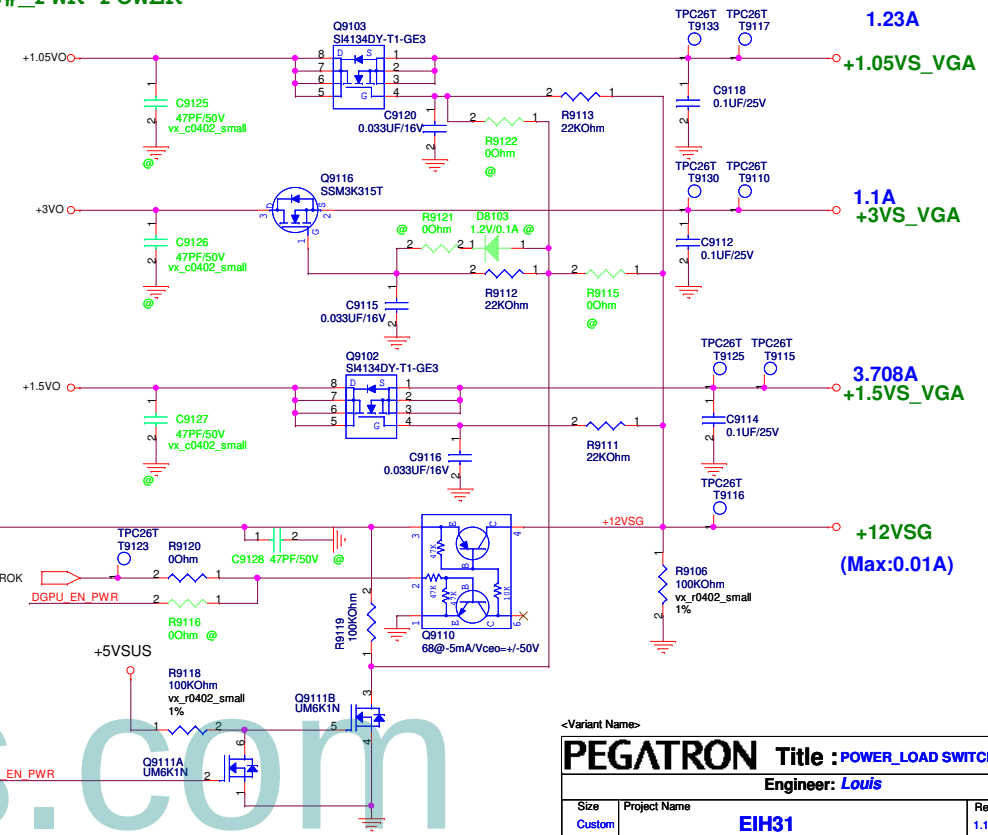


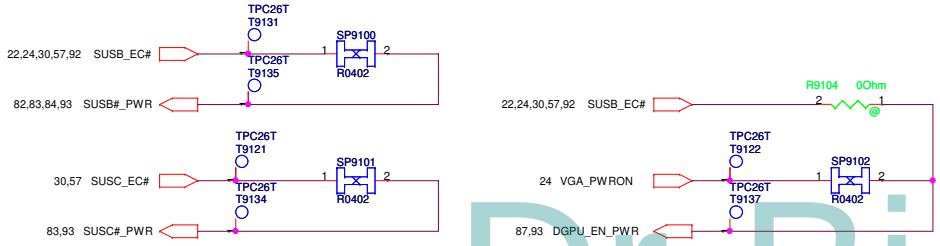
SUSC#_PWR POWER



DSC#_PWR POWER

for:17W





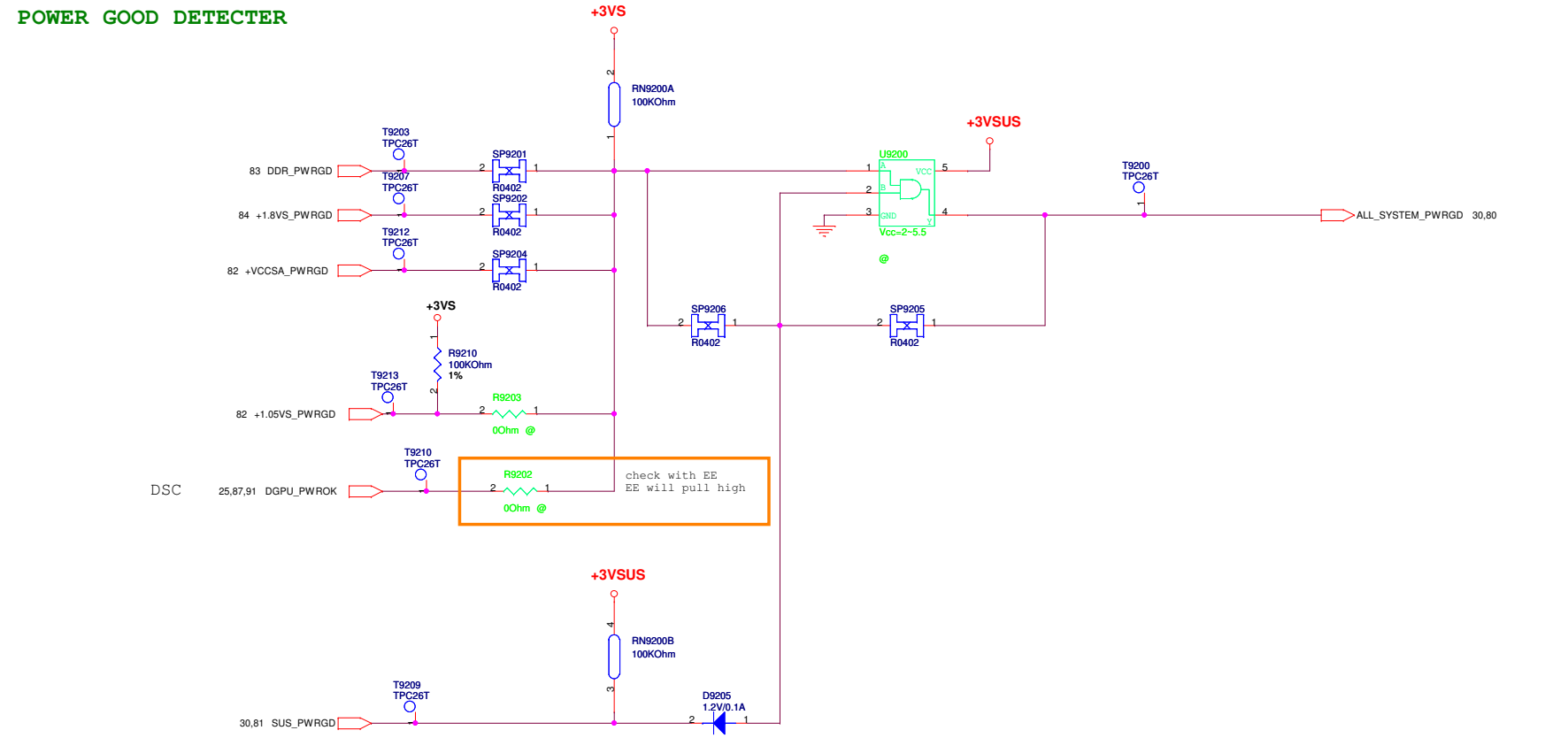
<Variant Name>

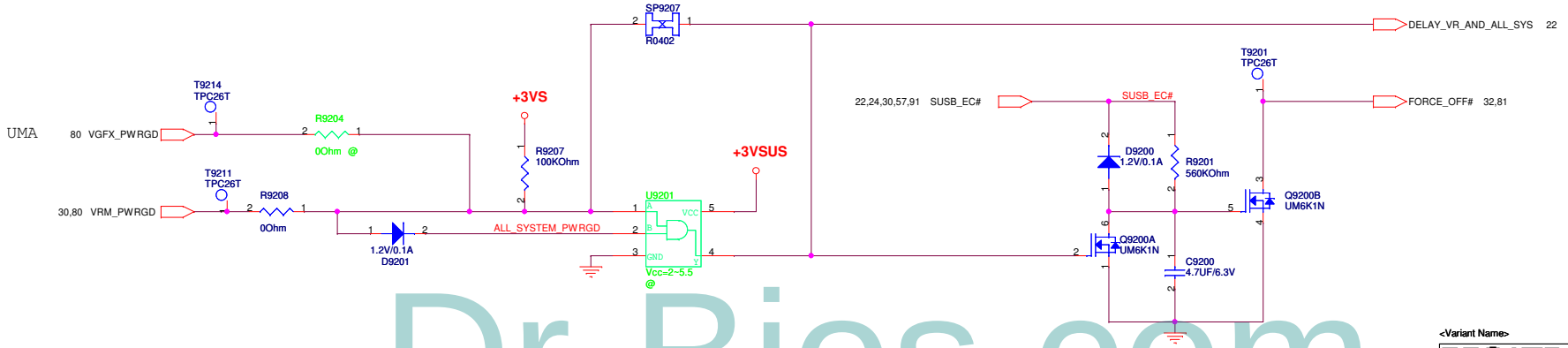
PEGATRON Title : POWER_LOAD SWITCH
Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Friday, December 17, 2010 Sheet 91 of 99

POWER GOOD DETECTER





<Variant Name>

PEGATRON Title :POWER_PROTECT

Engineer: Louis

Size	Project Name	Rev
Custom	EIH31	1.1

Date: Friday, December 17, 2010 Sheet 92 of 99

AC_BAT_SYS → AC_BAT_SYS 45,80,81,82,83,87,88
BAT → BAT 88
BAT_CON → BAT_CON 60,88

+3VA → +3VA 20,27,30,54,57,60,81
+3VAO → +3VAO
+5VAO → +5VAO
+5VA → +5VA 81,88

+5VO → +5VO 81,91
+3VO → +3VO 81,91
+1.05VO → +1.05VO 82,91
+0.75VO → +0.75VO 83
+1.5VO → +1.5VO 83,91
+1.8VO → +1.8VO 84
+0.85VO → +0.85VO 82

+5VSUS → +5VSUS 22,27,55,81,82,83,84,87,91
+3VSUS → +3VSUS 4,22,24,27,28,30,69,81,82,84,92
+12VSUS → +12VSUS 22,28,81,91

+5V → +5V 46,52,54,57,69,91
+3V → +3V 4,24,52,53,55,57,69,91
+12V → +12V 91
+1.5V → +1.5V 5,7,16,57,83

+5VS → +5VS 27,30,31,36,37,46,48,50,51,54,55,57,80,91
+3VS → +3VS 4,16,17,20,21,22,23,24,25,26,27,28,30,32,36,37,40,44,45,46,48,50,51,53,54,55,57,69,91,92
+12VS → +12VS 28,36,48,91
+1.05VS → +1.05VS 26,27,57,80,82
+0.75VS → +0.75VS 16,17,57,83
+1.5VS → +1.5VS 26,53,57,91
+1.8VS → +1.8VS 7,24,26,57,84
+VCCSA → +VCCSA 7,82

+VCC_CORE → +VCC_CORE 6,80
+VGFX_CORE → +VGFX_CORE 7,80
+VGA_VCORE → +VGA_VCORE 57,75,87

+1.05VS_VGA → +1.05VS_VGA 57,70,71,72,91
+1.5VS_VGA → +1.5VS_VGA 57,71,76,91

+3VS_VGA → +3VS_VGA 57,70,72,74,91
+12VSG → +12VSG 91

FOR POWER TEST

+3VA → JP9300 (SGL_JUMP) → TPC26T T9301 → CPU_VRON_PWR 80
+3VA → @JP9301 (SGL_JUMP) → TPC26T T9302 → SUSB#_PWR 82,83,84,91
+3VA → @JP9302 (SGL_JUMP) → TPC26T T9303 → SUSC#_PWR 83,91
+3VA → @JP9303 (SGL_JUMP) → TPC26T T9304 → VSUS_ON 30,81
+3VA → @JP9305 (SGL_JUMP) → TPC26T T9308 → DGPU_EN_PWR 87,91

@

<Variant Name>

PEGATRON Title : POWER_SIGNAL
Engineer: Louos

Size	Project Name	Rev
Custom	EIH31	1.1

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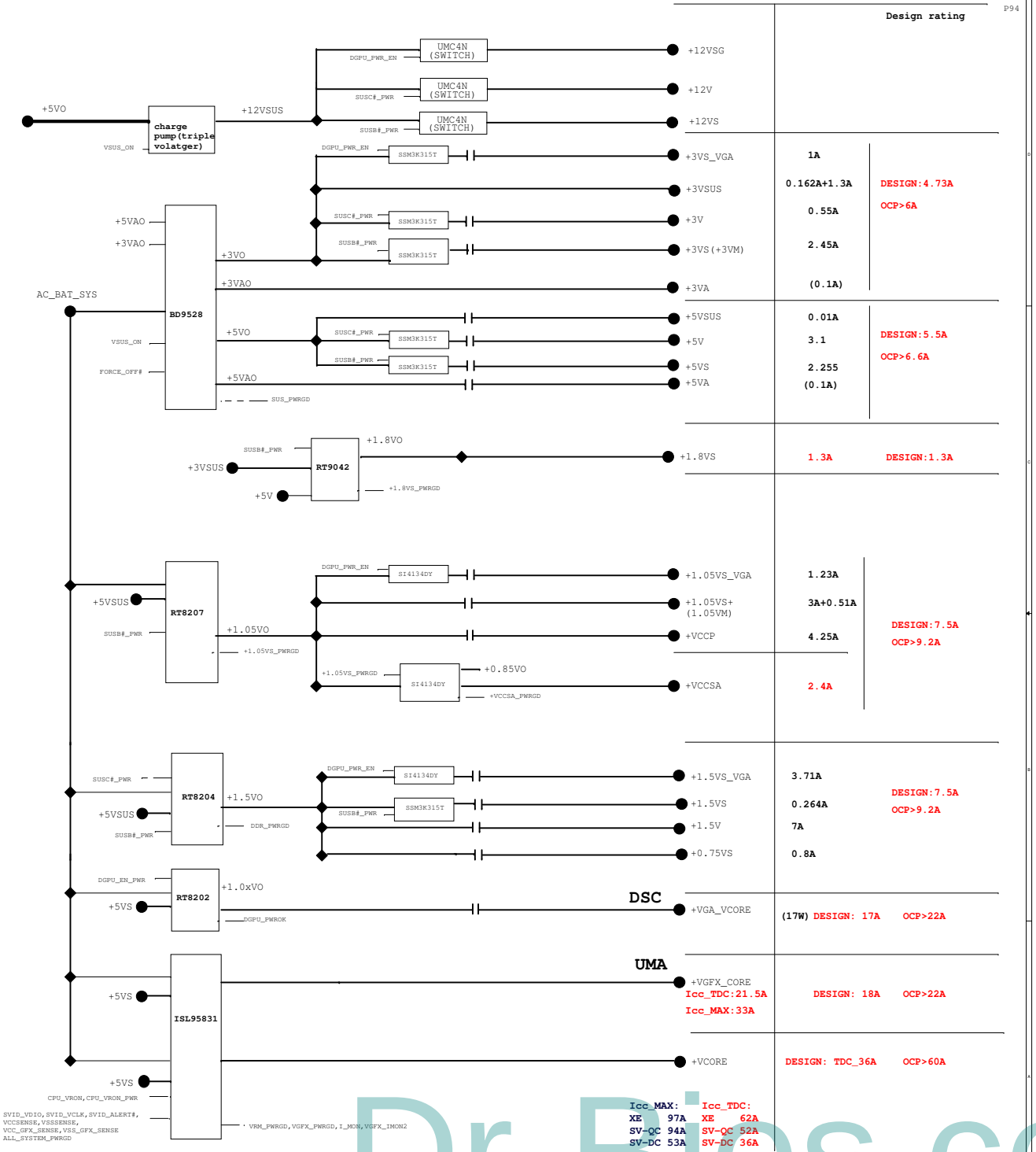

Design rating
+5VO
charge pump(triple volatger)
VSUS_ON
+12VSUS
DGPU_PWR_EN
UMC4N (SWITCH)
SUSC#_PWR
SUSB#_PWR
+12VSG
+12V
+12VS
SSM3K315T
+3VS_VGA
+3VSUS
+3V
+3VS(+3VM)
+3VA
1A
0.162A+1.3A
0.55A
2.45A
(0.1A)
DESIGN:4.73A
OCP>6A
+5VAO
+3VAO
+3VO
AC_BAT_SYS
BD9528
FORCE_OFF#
SUS_PWRGD
+5VSUS
+5V
+5VS
+5VA
0.01A
3.1
2.255
(0.1A)
DESIGN:5.5A
OCP>6.6A
RT9042
+1.8VO
+1.8VS
1.3A
DESIGN:1.3A
+1.8VS_PWRGD
RT8207
SUSB#_PWR
+1.05VO
+1.05VS_PWRGD
SI4134DY
+0.85VO
+VCCSA_PWRGD
+1.05VS_VGA
+1.05VS+ (1.05VM)
+VCCP
+VCCSA
1.23A
3A+0.51A
4.25A
2.4A
DESIGN:7.5A
OCP>9.2A
RT8204
+1.5VO
DDR_PWRGD
+1.5VS_VGA
+1.5VS
+1.5V
+0.75VS
3.71A
0.264A
7A
0.8A
DESIGN:7.5A
OCP>9.2A
RT8202
DGPU_EN_PWR
+1.0xVO
DGPU_PWROK
DSC
+VGA_VCORE
(17W) DESIGN: 17A OCP>22A
UMA
ISL95831
+VGFX_CORE
Icc_TDC:21.5A
Icc_MAX:33A
DESIGN: 18A OCP>22A
+VCORE
DESIGN: TDC_36A OCP>60A
CPU_VRON,CPU_VRON_PWR
SVID_VDIO,SVID_VCLK,SVID_ALERT#,
VCCSENSE,VSSSENSE,
VCC_GFX_SENSE,VSS_GFX_SENSE
ALL_SYSTEM_PWRGD
VRM_PWRGD,VGFX_PWRGD,I_MON,VGFX_IMON2
Icc_MAX: Icc_TDC:
XE 97A XE 62A
SV-QC 94A SV-QC 52A
SV-DC 53A SV-DC 36A
Mobile SB processor March 2010 R1.0 #445465
PEGATRON
Title : POWER_FLOWCHART
Engineer: Louis
EIH31

PEGATRON	Title : ****
BG1\HW1	Engineer: *Ivan Liu*
Size: A	Project Name: **H36HC**
Rev: 1.3	
Date: Friday, December 17, 2010	Sheet 96 of 99

SR BOM change

SR1.1 Un-mount Q5602, Q5601 and mount R5323 and R5310

SR1.2 CE5001 un-mount

SR1.3 L3602 mount

SR1.4 R7005 un-mount

SR1.5 R7410 change 10K ohm

SR1.6 R4504 change 10K ohm for LVDS backlight

SR1.7 R7430, R7432, R7433 un-mount

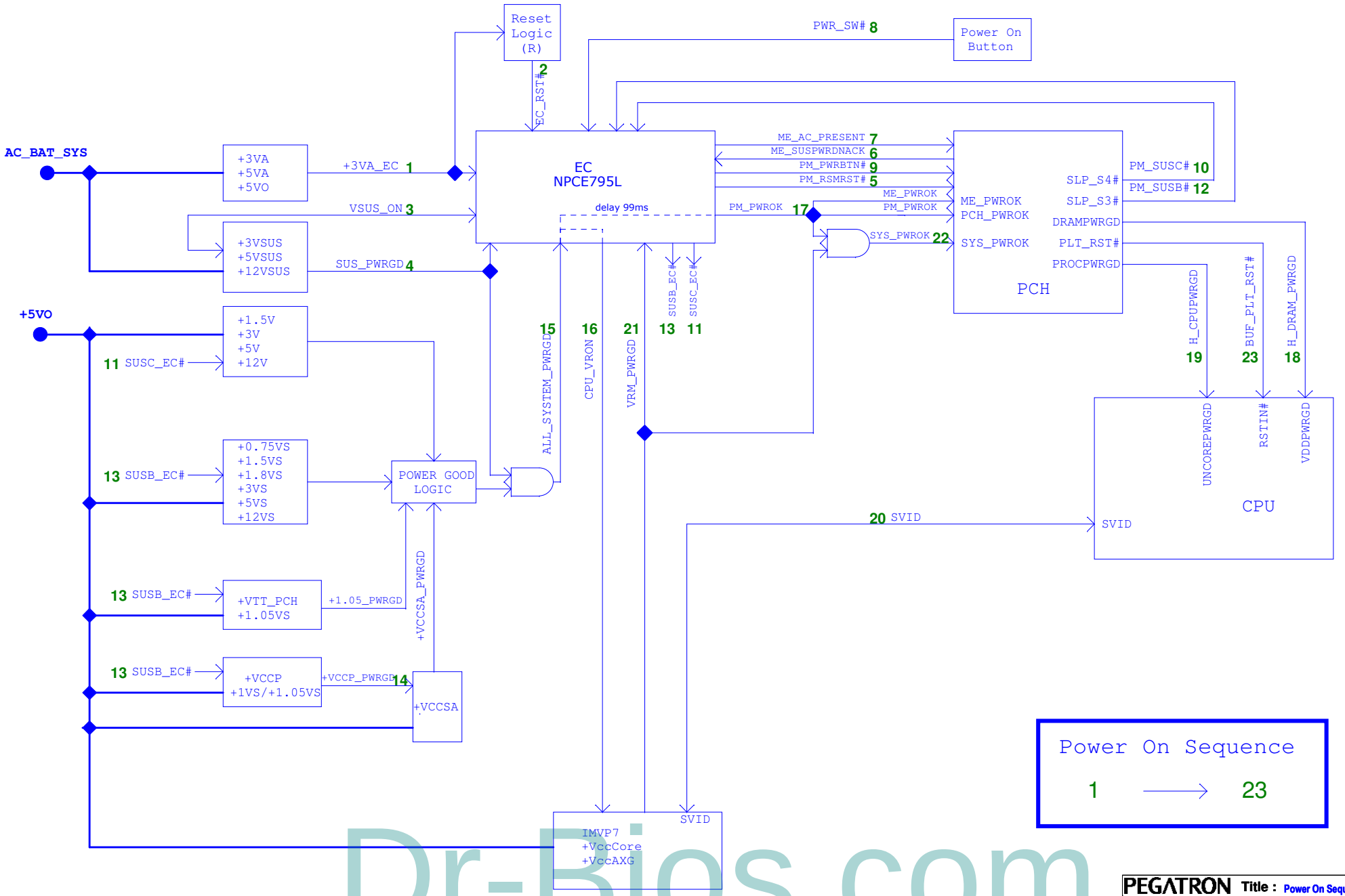
SR1.8 R7608, R7611 change 162 ohm

ER

ER1.1 PI pin connect to ESD and VDD pin reserve 0.1 uF cap
ER1.2 Add diode and reserve 0 ohm for AC adapter plug in /out voice
ER1.3 U5201 change G547G1P81U for Desing IP
ER1.4 Add Card Reader LED
ER1.5 J3701, J3702, J4601, J5201, J5304,J5001 chang connector
ER1.6 R6505~R6508 change 0603 size
ER1.7 D4801 contact to 2.2K ohm for EA solution in HDMI issue
ER1.8 CPU_THERM# contact to FORCE_OFF#
ER1.9 RTC battery connector (J2001)Pin1, Pin2 swap
ER1.10 D3707, D4618, D5201, D5301, D6502, D6503, D6802 VDD pin reserve 0.1 uF cap
ER1.11 R3720 R3721 change 51ohm for consumer spec in HP
ER1.12 L4601, L4602, L4603 change 27nH and add C4622, C4623, C4624 for EA solution in CRT
ER1.13 L5301, L5302, L5306 change 0 ohm and L5305 change short pin,
C5321, C5327,C5307, C5322, C5315, C5305, C5313 change umount
ER1.14 Change R4566 from 300(0603) to 150(0402) for LVDS power sequence solution
ER1.15 USB port 0 and port 1 swap
ER1.16 Vcore_add CE8002&CE8006 to replace CE0601&CE0602
ER1.17 VGFX_CORE(IGPU) add CE8007 to replace CE0705
ER1.18 reserve M_VREF schematic
ER1.19 Reserve C2623, C2624, C4514, C4515 for WLAN solution
ER1.20 Reserve C4510, C4512, C4513 for 3G and L6002~L6004, L4502 change 47 ohm Bead
ER1.21 C6007, C6006 mount for WLAN
ER1.22 RN3002 change 2R4P
ER1.23 LED and BT schematic change to LED board
ER1.24 LED power change 5VSUS, so R5618, R5616, R5623 change 560 ohm
ER1.25 VRAM change co-lay footprint
ER1.26 Reserve C5601, C5602, C5603, C6356, C6357 to 47pF for RF request
ER1.27 Reserve C4516, C4517 to 10pF for RF request
ER1.28 U6504,U6505 change AZ3028 for EMI request
ER1.29 D6401, D6501, D6502 change ESD AZ5023 in for EMI request in LAN function
ER1.30 Add C6010 C6011 for EMI request
ER1.31 Merge Q6704 and remove U6704
ER1.32 D3720 change to mount for EMI request
ER1.34 Reserve C6913(47PF), C6902(0.1uF), C6623(47PF), C6606(22uF) for 3G
ER1.35 L6601=>0901-00HI000 FERRITE BEAD(1206)390 OHM/2A

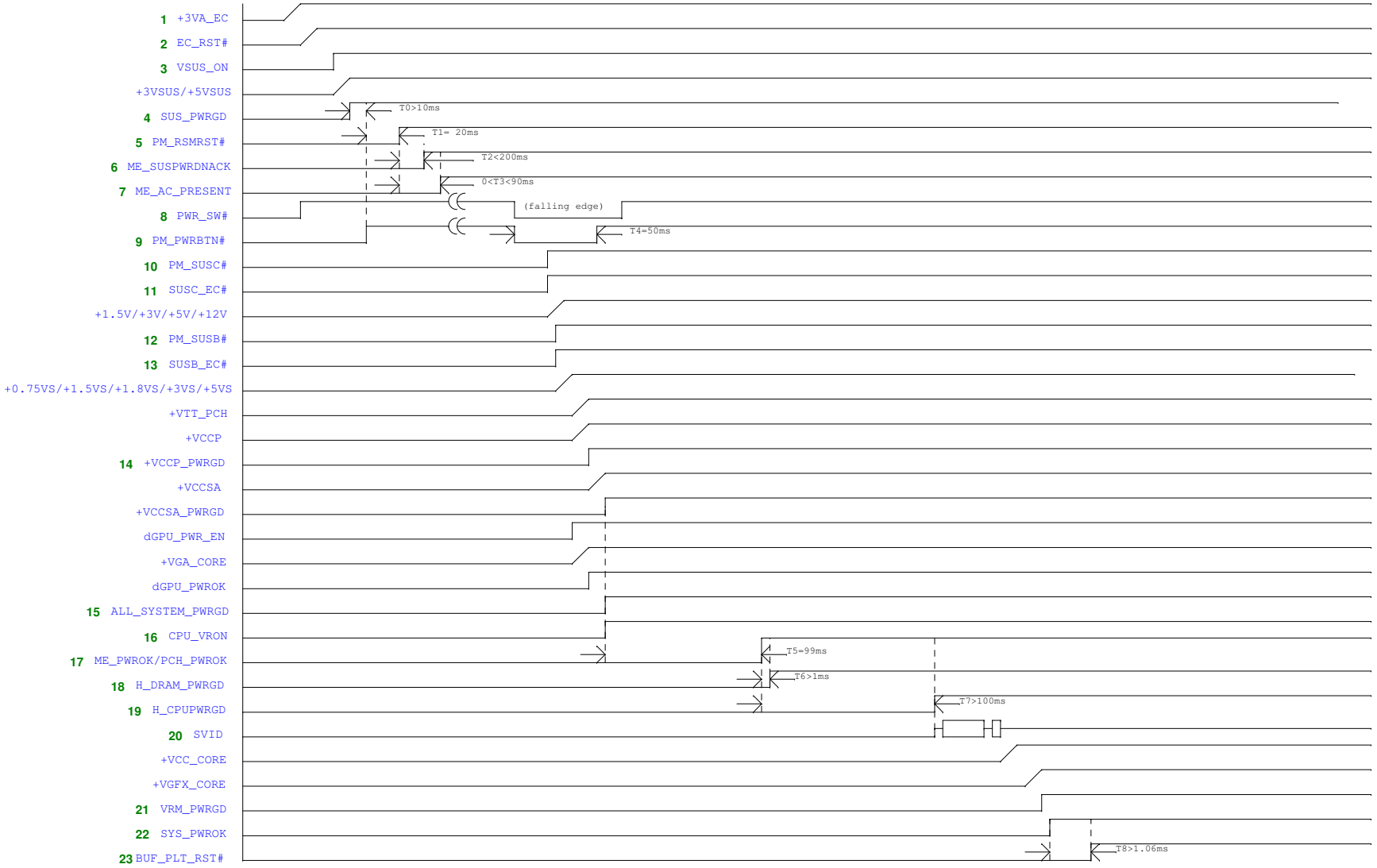
PEGATRON	Title : ****	
<OrgName>	Engineer: JAY TSAI	
Size: Custom	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 97 of 99	

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



PEGATRON	Title : Power On Sequence		
<OrgName>	Engineer: JAY TSAI		
Size: C	Project Name: EIH31		Rev: 1.3
Date: Friday, December 17, 2010	Sheet 98 of 99		

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



PEGATRON	Title : Power On Timing	
<OrgName>	Engineer: JAY TSAI	
Size: C	Project Name: EIH31	Rev: 1.3
Date: Friday, December 17, 2010	Sheet 99 of 99	