

CLK-GEN
ICS 952801
Page 2

HOST 200MHz
ZCLK 133MHz
AGP 66MHz
PCI 33MHz
USB 48MHz
REF 14.318MHz

3V/5V
Page 22

3V_ALWAYS
5VPCU
3V_S5
1.8V_S5
3VSUS
5VSUS
+3V
+5V
15V

2.5V/1.25V
Page 23

2.5VSUS
1.25VREF
+2.5V
DDR_VTT

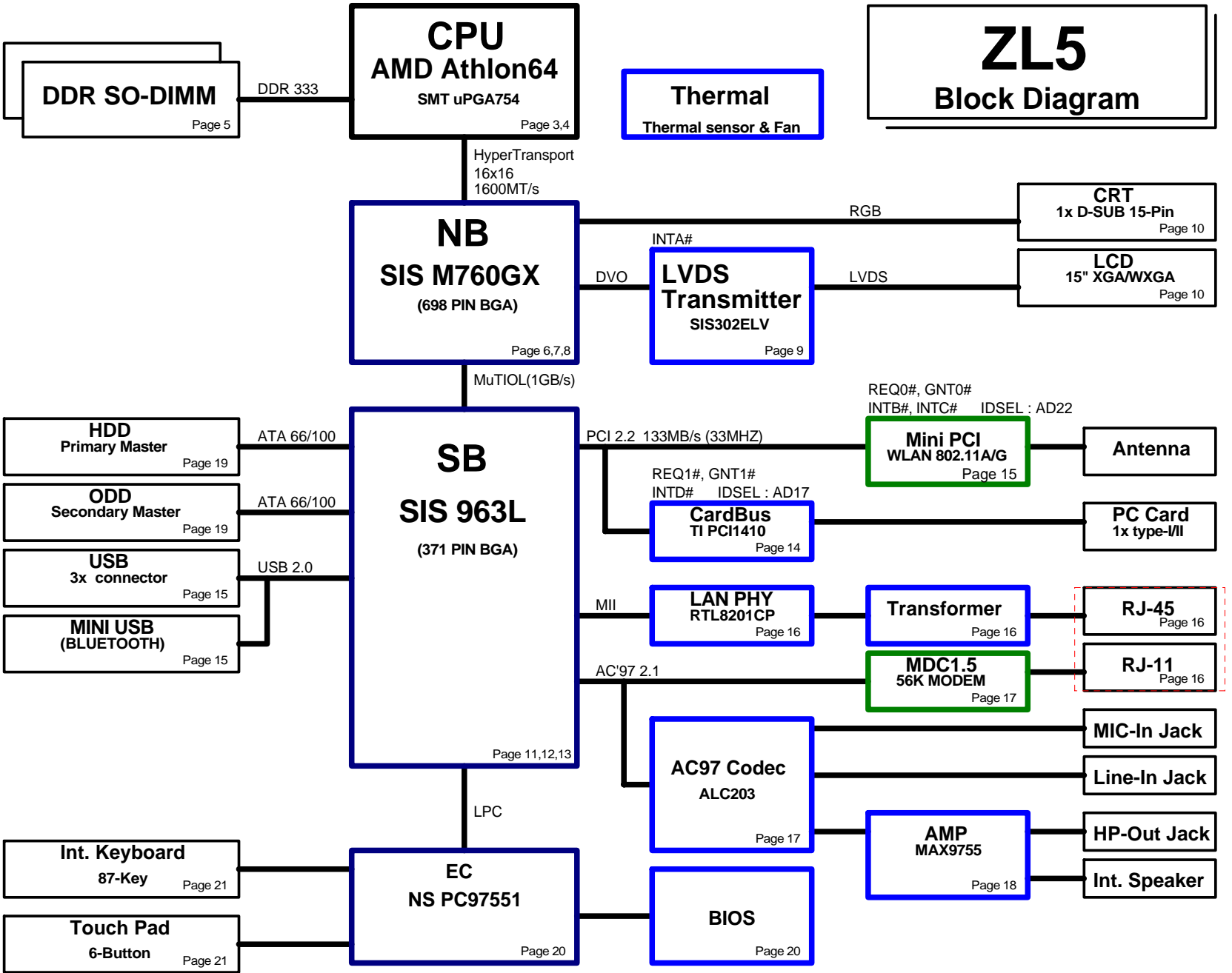
**1.2V/1.5V
1.8V**
Page 24

+1.2V_HT
+1.5V
+1.8V

CPU CORE
Page 25

VCC_CORE

BATTERY CHARGER
Page 26

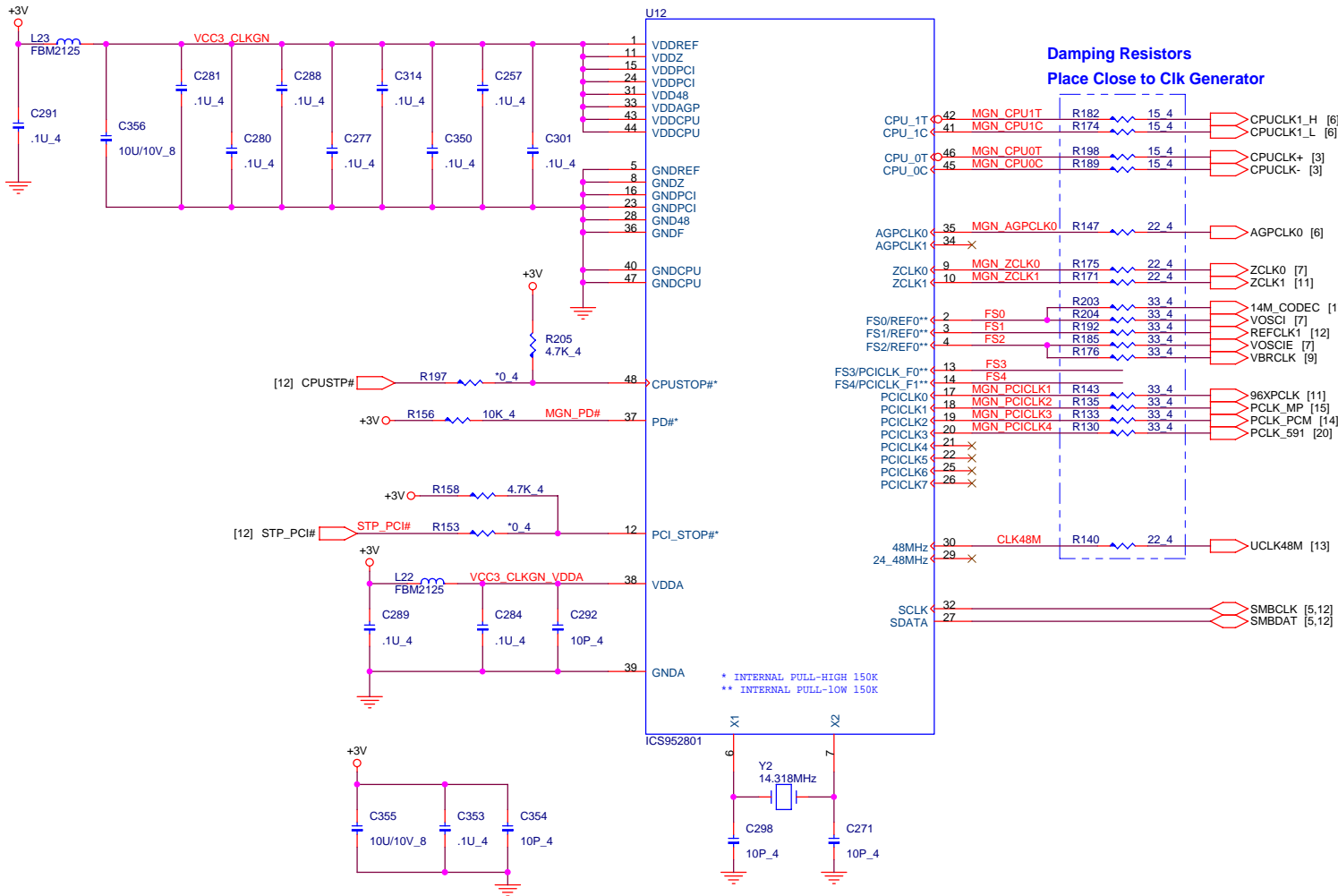


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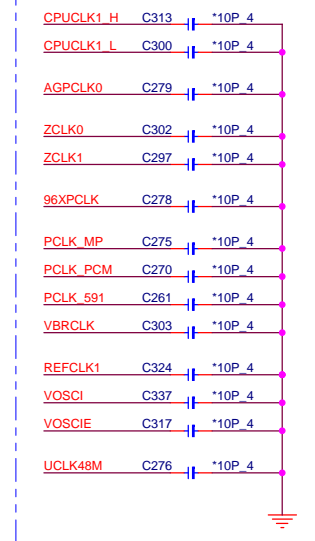
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Size: Document Number: **BLOCK DIAGRAM** Rev: 3B

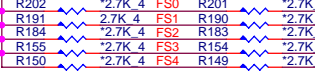
Date: Thursday, March 10, 2005 Sheet: 1 of 26



By-Pass Capacitors
Place Close to Clock Generator



Frequency Selection



CLK Table for SiS M760 (Not For ICS ICS-952801)

SiS 755/M760 CLOCK					CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	VCO (MHz)
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)					
0	0	0	0	0	200	66.66	66.66	33.33	400
0	0	0	0	1	200	100	66.66	33.33	400
0	0	0	1	0	200	133.33	66.66	33.33	400
0	0	0	1	1	200	166.66	66.66	33.33	1000
0	0	1	0	0	233	66.66	66.66	33.33	466
0	0	1	0	1	233	93.2	66.66	33.33	466
0	0	1	1	0	233	133.28	66.66	33.33	933
0	0	1	1	1	233	139.8	69.9	33.33	699
0	1	0	0	0	266	66.66	66.66	33.33	266
0	1	0	0	1	266	106.4	66.5	33.33	532
0	1	0	1	0	266	133	66.5	33.33	532
0	1	0	1	1	266	159.6	66.5	33.33	798
0	1	1	0	0	200	133	50	33.33	400
0	1	1	0	1	200	114	66.66	33.33	800
0	1	1	1	0	200	142	66.66	33.33	1000
0	1	1	1	1	200	160	66.66	33.33	800

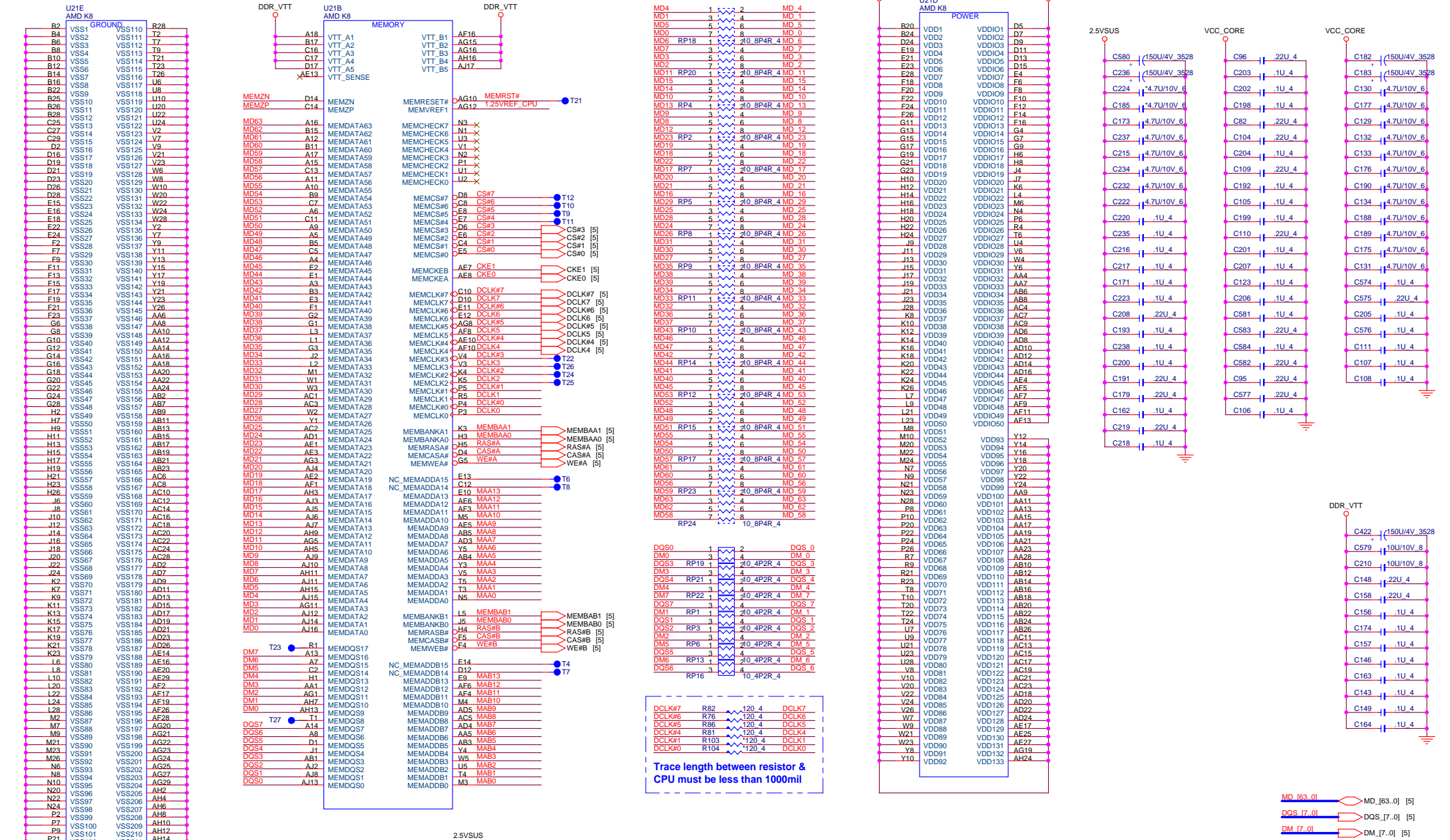
SiS 755/M760 CLOCK					CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)				
1	0	0	0	0	180	135	67.5	33.75
1	0	0	0	1	185	132.14	66.07	33.04
1	0	0	1	0	190	135.71	67.08	33.93
1	0	0	1	1	195	130	65	32.5
1	0	1	0	0	205	136.66	68.33	34.17
1	0	1	0	1	210	140	70	35
1	0	1	1	0	215	129	64.5	32.25
1	0	1	1	1	220	132	66	33
1	1	0	0	0	66.66	66.66	66.66	33.33
1	1	0	0	1	66.66	100	66.66	33.33
1	1	0	1	0	100	100	66.66	33.33
1	1	0	1	1	100	133.33	66.66	33.33
1	1	1	0	0	133	100	66.66	33.33
1	1	1	0	1	133	133.33	66.66	33.33
1	1	1	1	0	166	100	66.66	33.33
1	1	1	1	1	166	133.33	66.66	33.33

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CLOCK GENERATOR Rev 3B

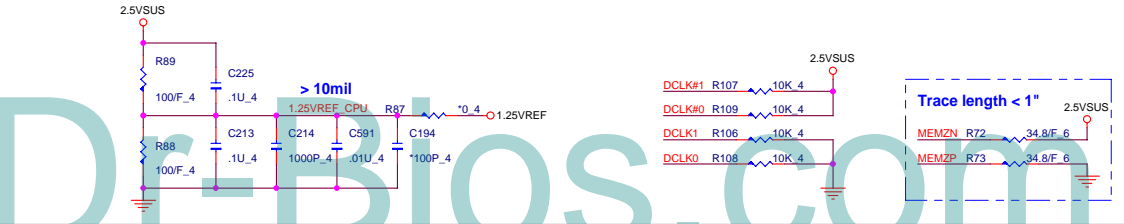
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CPU DDR/POWER I/F

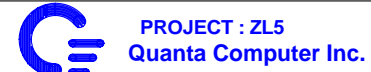


Trace length between resistor & CPU must be less than 1000mil

- MD [63..0] [5]
- DQS [7..0] [5]
- DM [7..0] [5]
- MAA[13..0] [5]
- MAB[13..0] [5]



Trace length < 1"



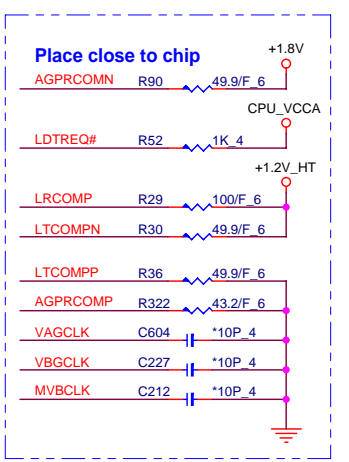
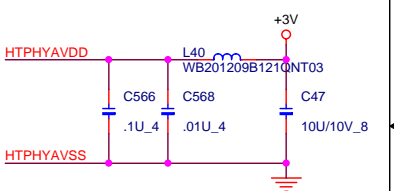
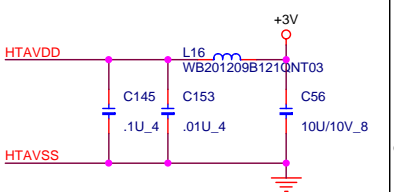
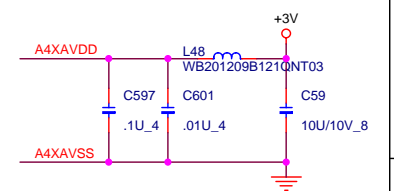
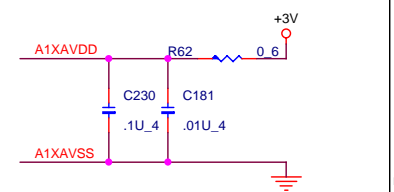
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 [3] CADIN[15..0] ← CADIN[15..0]
 [3] CADOP[15..0] ← CADOP[15..0]
 [3] CADON[15..0] ← CADON[15..0]

CADIP15 D24
 CADIN15 D25
 CADIP14 E23
 CADIN14 E24
 CADIP13 F22
 CADIN13 F23
 CADIP12 G21
 CADIN12 G22
 CADIP11 H20
 CADIN11 H21
 CADIP10 I19
 CADIN10 I20
 CADIP9 J18
 CADIN9 J19
 CADIP8 K17
 CADIN8 K18
 CADIP7 L16
 CADIN7 L17
 CADIP6 M15
 CADIN6 M16
 CADIP5 N14
 CADIN5 N15
 CADIP4 O13
 CADIN4 O14
 CADIP3 P12
 CADIN3 P13
 CADIP2 Q11
 CADIN2 Q12
 CADIP1 R10
 CADIN1 R11
 CADIP0 S9
 CADIN0 S10

CLKINO [3]
 CLKIPO [3]
 CLKIN1 [3]
 CLKIP1 [3]
 CTLINO [3]
 CTLIPO [3]

[9] VAD[11..0]
 [9] VAGCLK
 [9] VAHSYNC
 [9] VAVSYNC
 [9] VADE
 [9] VBD[11..0]

[9] VBGCLK
 [9] VBHSYNC
 [9] VBSYNC
 [9] VBDE
 [9] VBCTL1
 [9] VBCTL0



CADON0 N27
 CADOP0 P27
 CADON1 M29
 CADOP1 N29
 CADON2 L27
 CADOP2 M27
 CADON3 K29
 CADOP3 L29
 CADON4 H29
 CADOP4 J29
 CADON5 G27
 CADOP5 H27
 CADON6 F29
 CADOP6 G29
 CADON7 E27
 CADOP7 F27
 CADON8 N24
 CADOP8 P24
 CADON9 M25
 CADOP9 N25
 CADON10 L26
 CADOP10 M26
 CADON11 K24
 CADOP11 L24
 CADON12 H26
 CADOP12 J26
 CADON13 G24
 CADOP13 H24
 CADON14 F25
 CADOP14 G25
 CADON15 E26
 CADOP15 F26

HOST_TX
 HOST_RX
 M760-1

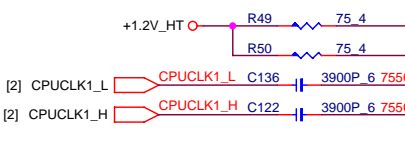
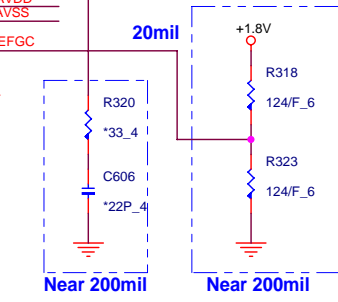
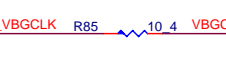
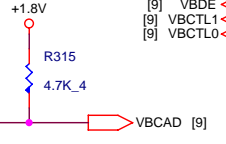
LRCOMP C28
 LRCAD_N0
 LRCAD_P0
 LRCAD_N1
 LRCAD_P1
 LRCAD_N2
 LRCAD_P2
 LRCAD_N3
 LRCAD_P3
 LRCAD_N4
 LRCAD_P4
 LRCAD_N5
 LRCAD_P5
 LRCAD_N6
 LRCAD_P6
 LRCAD_N7
 LRCAD_P7
 LRCAD_N8
 LRCAD_P8
 LRCAD_N9
 LRCAD_P9
 LRCAD_N10
 LRCAD_P10
 LRCAD_N11
 LRCAD_P11
 LRCAD_N12
 LRCAD_P12
 LRCAD_N13
 LRCAD_P13
 LRCAD_N14
 LRCAD_P14
 LRCAD_N15
 LRCAD_P15

[3] CLKON1 J25
 [3] CLKOP1 K25
 [3] CLKON0 J27
 [3] CLKOP0 K27
 [3] CTLO0 D29
 [3] CTLOP0 E29
 755CLK- A11
 755CLK+ A12
 HTAVDD C11
 HTAVSS B11
 HTPHYAVDD C12
 HTPHYAVSS B12

[3] LDTSTOP# E11
 [12] LDTRREQ# D12
 [3] LDTREST# D11

M760GX
 SBA7 D2
 SBA6 C6
 SBA5 D3
 SBA4 E4
 SBA3 F5
 SBA2 G6
 SBA1 H7
 SBA0 I8
 ST0 C5
 ST1 A5
 ST2 B4
 AAD0 U6
 AAD1 U1
 AAD2 U3
 AAD3 U4
 AAD4 U5
 AAD5 T3
 AAD6 T4
 AAD7 T6
 AAD8 R2
 AAD9 R5
 AAD10 R6
 AAD11 R7
 AAD12 N2
 AAD13 N3
 AAD14 N4
 AAD15 K2
 AAD16 K3
 AAD17 J5
 AAD18 J6
 AAD19 I6
 AAD20 I4
 AAD21 J1
 AAD22 J5
 AAD23 J6
 AAD24 G4
 AAD25 G3
 AAD26 F1
 AAD27 F2
 AAD28 H6
 AAD29 H7
 AAD30 G3
 AAD31 E3

AC/BE#3 OH3
 AC/BE#2 OL4
 AC/BE#1 ON5
 AC/BE#0 OR4
 AREQ# OA6
 AGNT# OB6
 AFRAME# OL6
 AIRDY# OL1
 ATRDY# OM4
 ADEVSEL# OM5
 ASERR# OM1
 ASTOP# OM2
 APAR N6
 RBF# C4
 WBF# A3
 GC_DET# D6
 PIPE#/ADBIH G6
 ADBIL E6
 SB_STB C1
 SB_STB# C2
 AD_STB0 T2
 AD_STB#0 R1
 AD_STB1 J2
 AD_STB#1 H1
 AGPCLK AA1
 AGPCOMP_P V2
 AGPCOMP_N V3
 AGPCOMM V3
 A1XAVDD AA4
 A1XAVSS AA5
 A4XAVDD AA2
 A4XAVSS AA3
 AGPVPREF V1
 AVREFGC V1
 AGPVSSREF V4



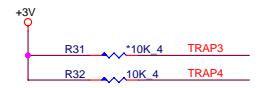
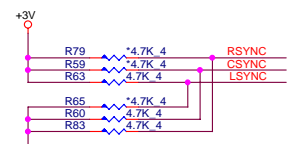
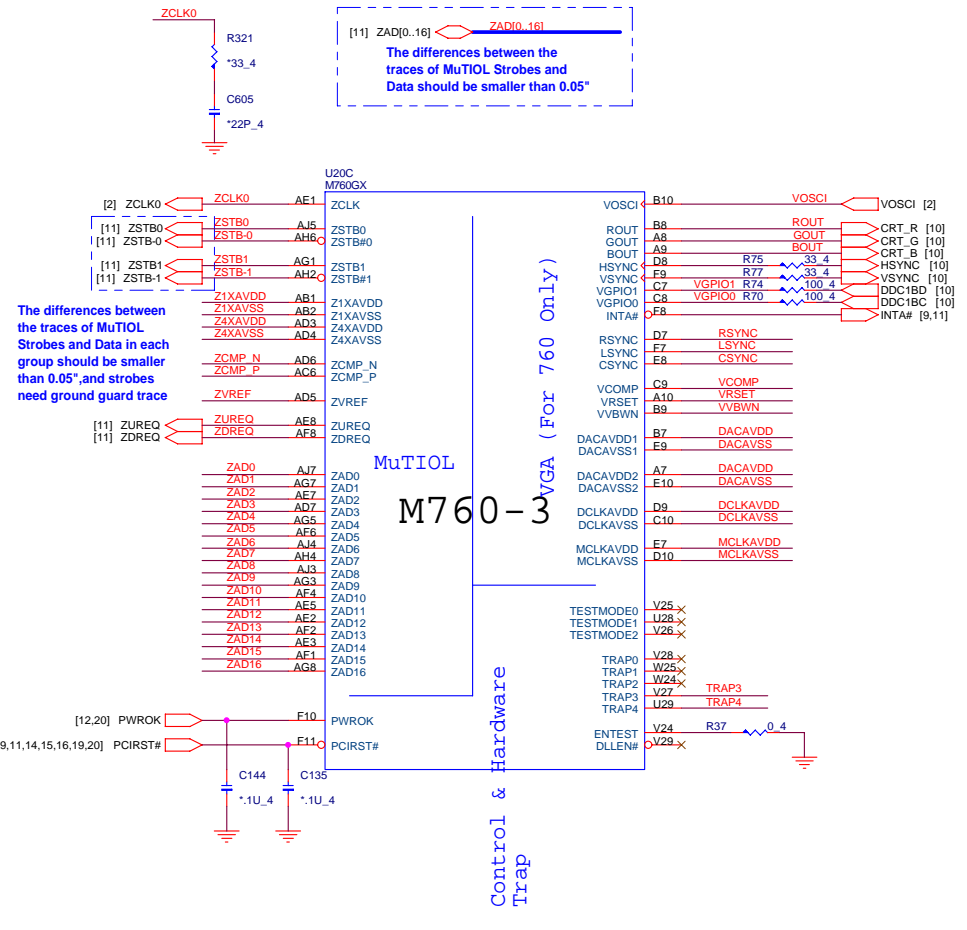
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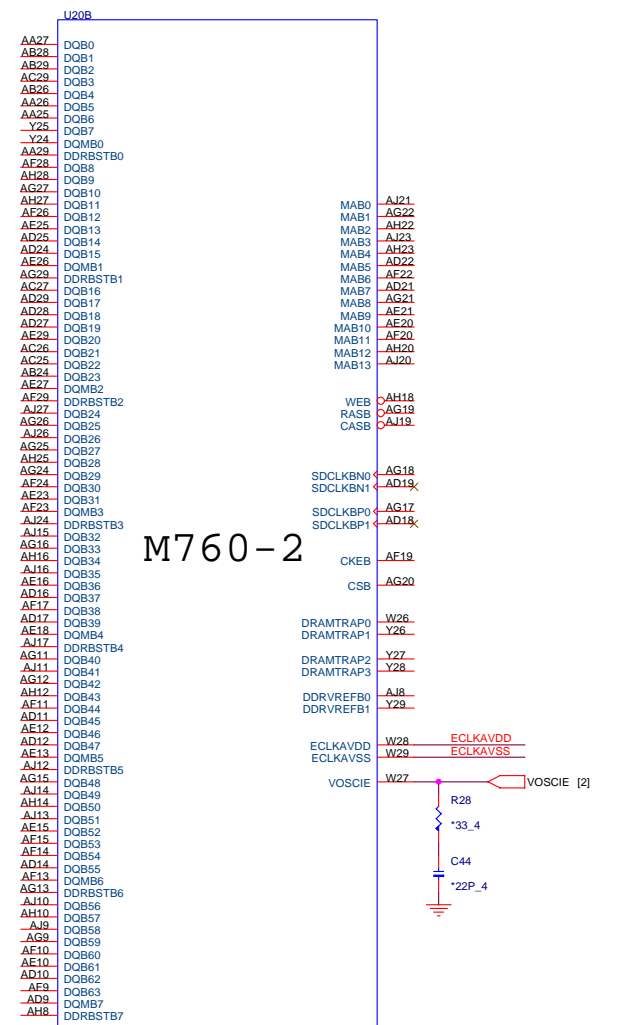
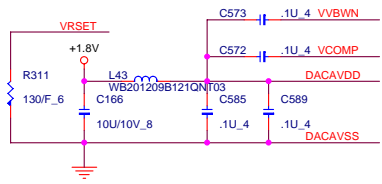
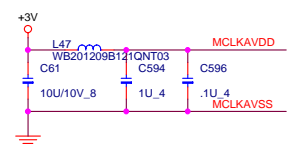
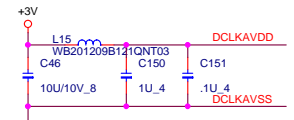
Size	Document Number	Rev
	M760GX(HT LINK/AGP)	3B
Date:	Thursday, March 10, 2005	Sheet 6 of 26

[11] ZAD[0..16] \leftrightarrow ZAD[0..16]

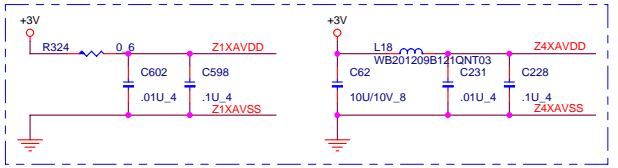
The differences between the traces of MuTIOL Strobes and Data should be smaller than 0.05"



NB Hardware Trap has internal pull-low in SiS M760 chip

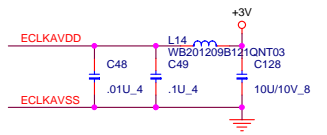
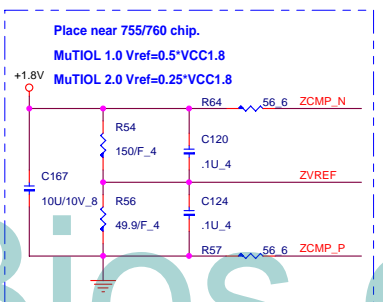


M760-2



SiS755/760 NB Hardware Trap Table

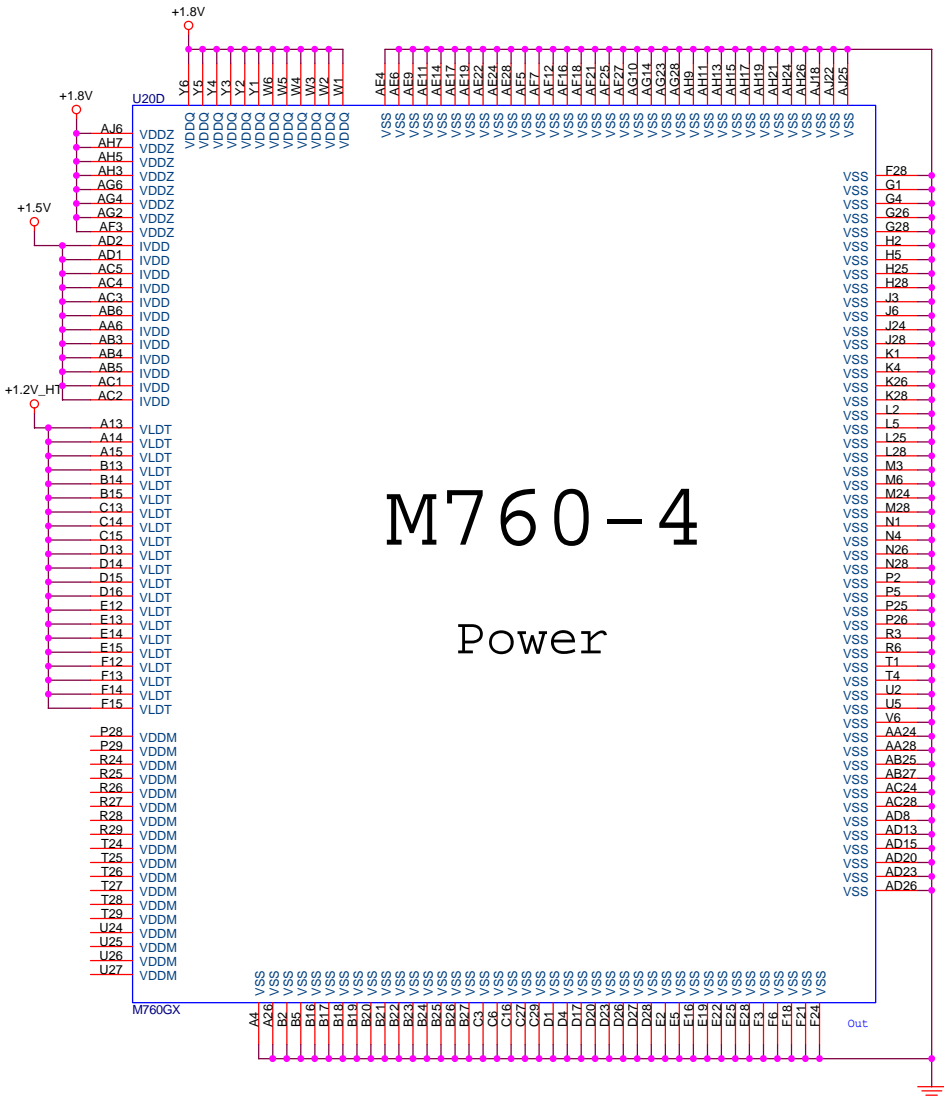
	755/760	ON/1	OFF/0	Internal	Default
DLLEN#	CPULCLK/ZCLK/AGPCLK PLL/DLL Circuit Enable	DISABLE	ENABLE	Pull Low	Low/0
TESTMODE0				Pull Low	
TESTMODE1	755 Test Mode Selection	1: Mode1	0: Mode0	Pull Low	
TESTMODE2	755 Test Mode Enable	ENABLE	DISABLE	Pull Low	Low/0
TRAP0	MuTIOL Verision 1, 2	Ver. 1	Ver. 2	Pull Low	Low/0
TRAP1	MuTIOL DBI Mode	DISABLE	ENABLE	Pull Low	Low/0
TRAP2	MuTIOLInitial Packet Series Mode	DISABLE	ENABLE	Pull Low	Low/0
TRAP3	Reserve			Pull Low	High/1
TRAP4	Reserve			Pull Low	High/1



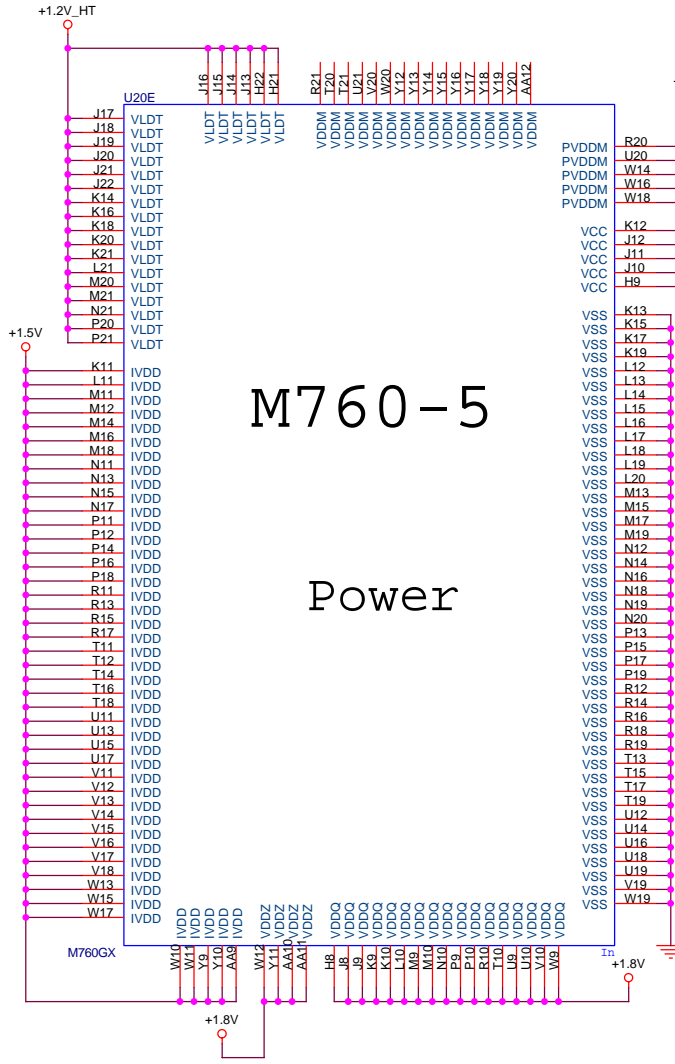
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	M760GX(MuTIOL/VGA)	3B
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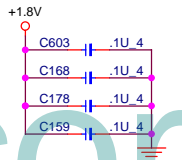
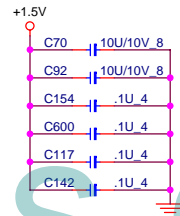
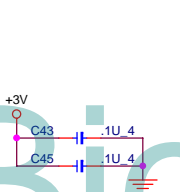
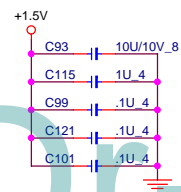
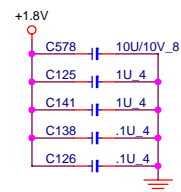
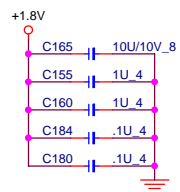
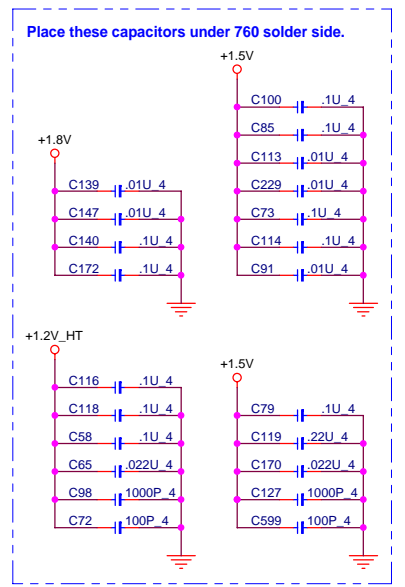
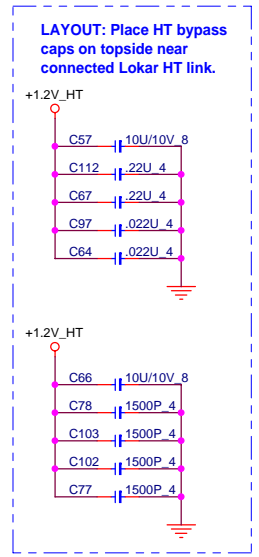
If Support Sis M760LV IVDD=1.5V



M760-4
Power



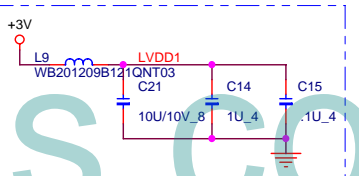
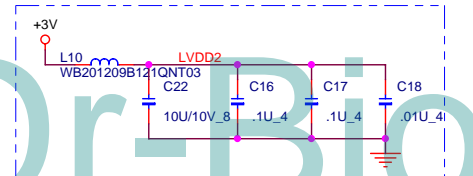
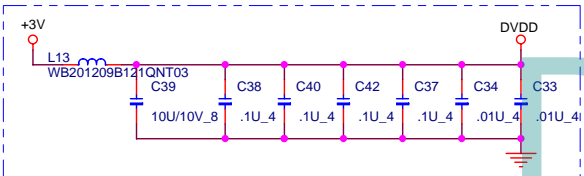
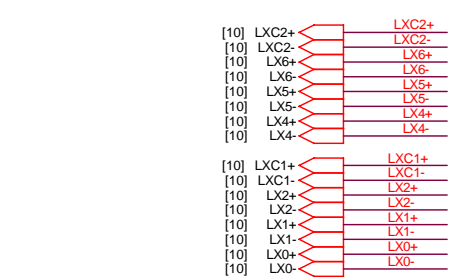
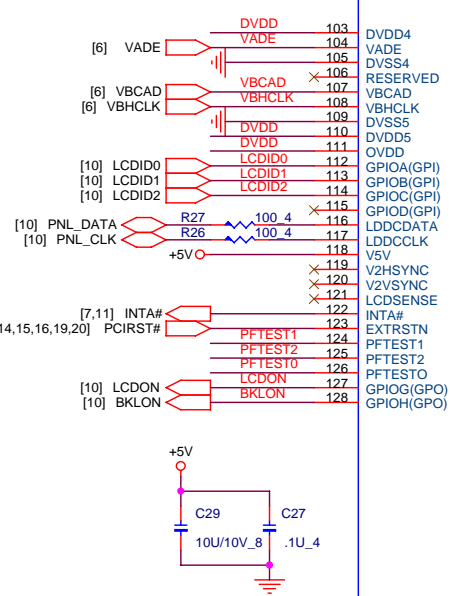
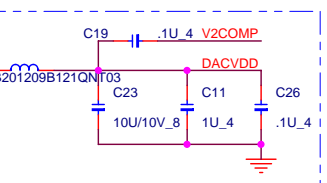
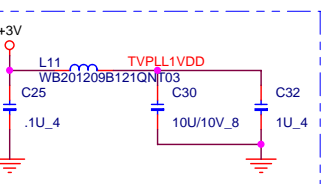
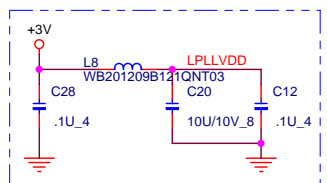
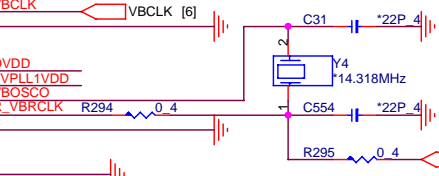
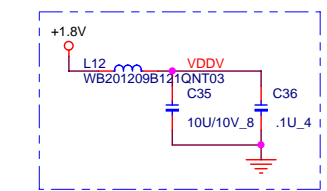
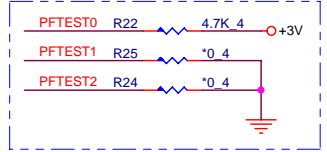
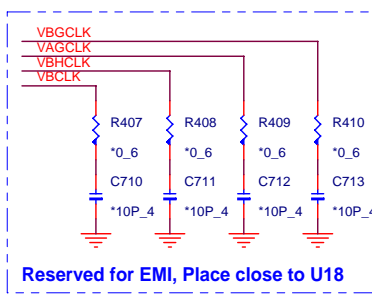
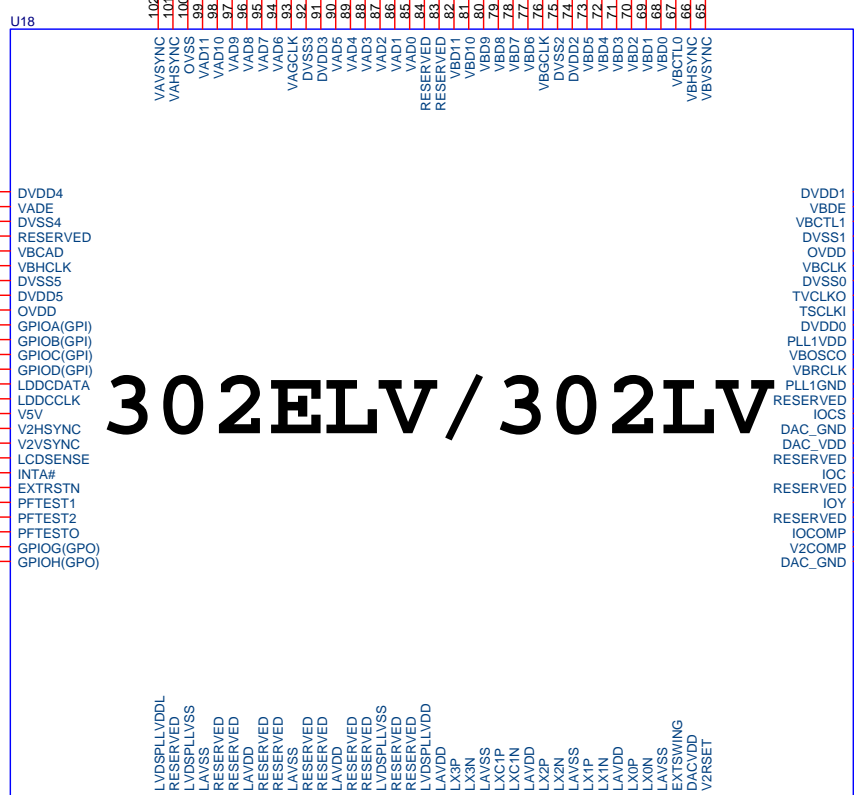
M760-5
Power



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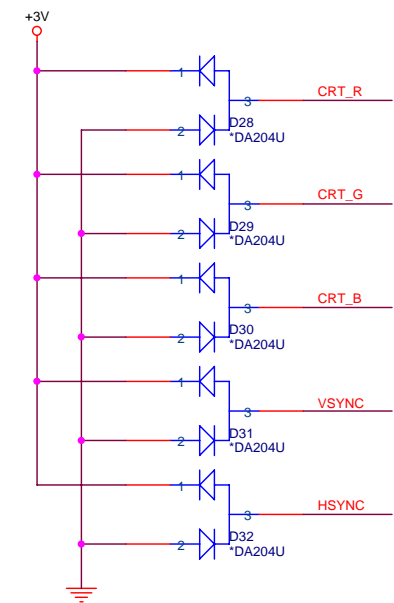
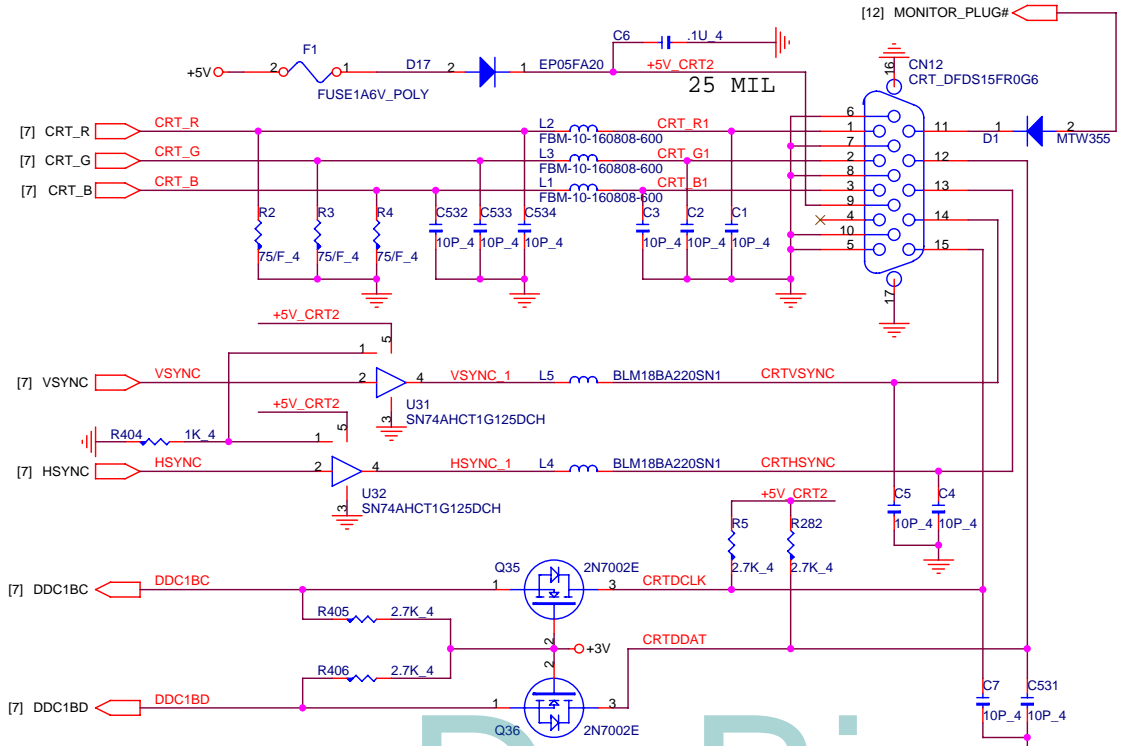
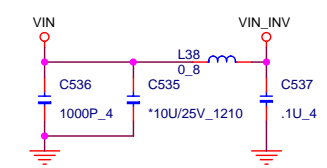
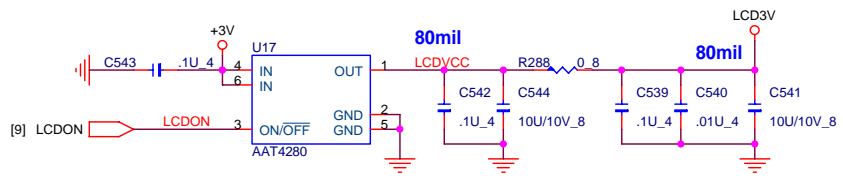
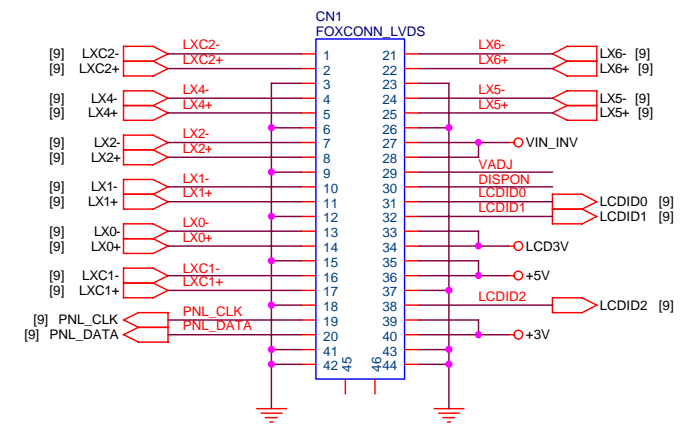
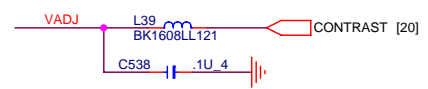
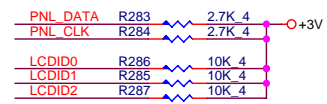
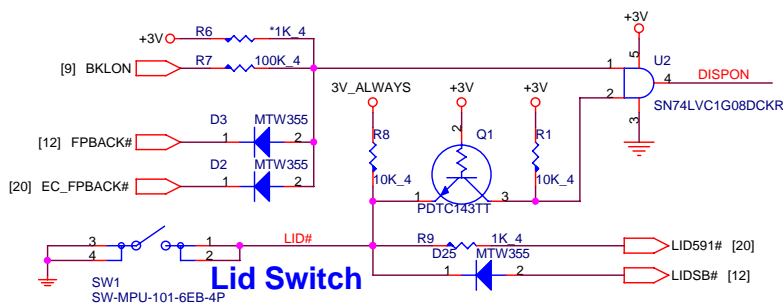
302ELV/302LV



PROJECT : ZL5
Quanta Computer Inc.

Size: Document Number
302ELV(LVDS)

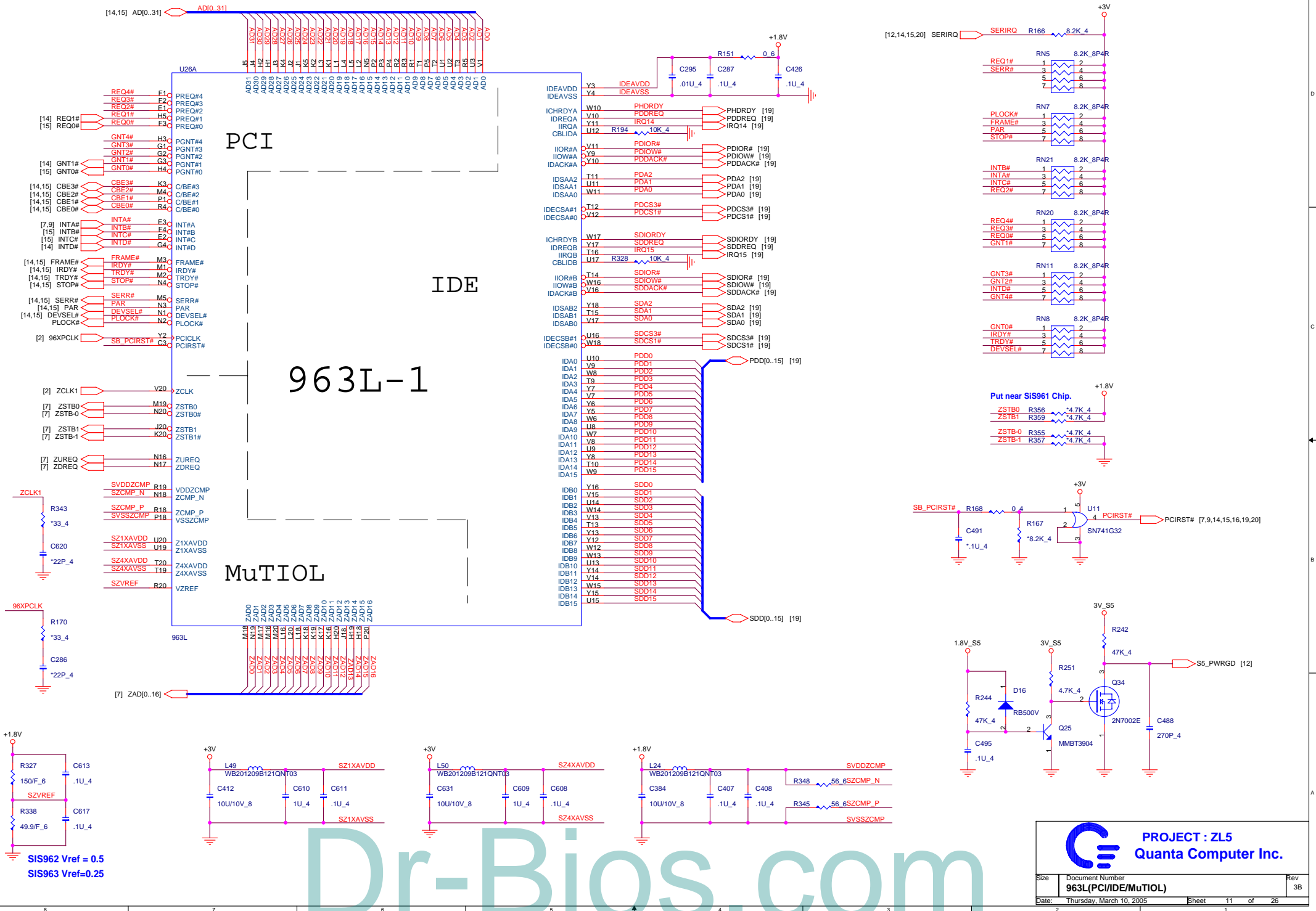
Date: Thursday, March 10, 2005 Sheet 9 of 26 Rev 3B



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PROJECT : ZL5
Quanta Computer Inc.

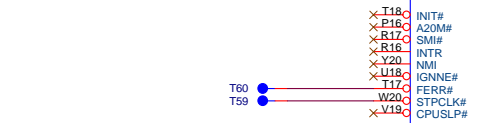
Size	Document Number	Rev
	CRT/LVDS	3B
Date:	Thursday, March 10, 2005	Sheet 10 of 26



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PROJECT : ZL5
Quanta Computer Inc.

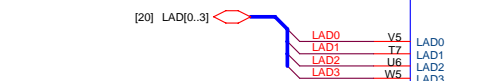
Size	Document Number	Rev
	963L(PCI/IDE/MuTIOL)	3B
Date:	Thursday, March 10, 2005	Sheet 11 of 26



CPU_S



APIC



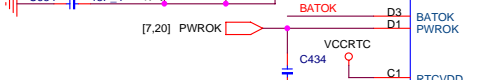
LPC



MII



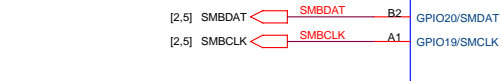
RTC



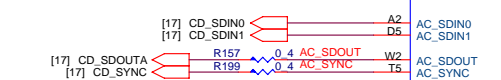
GPIO



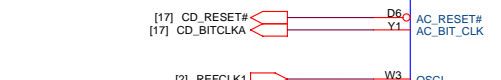
AC97



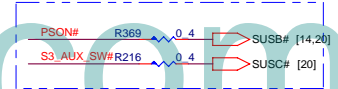
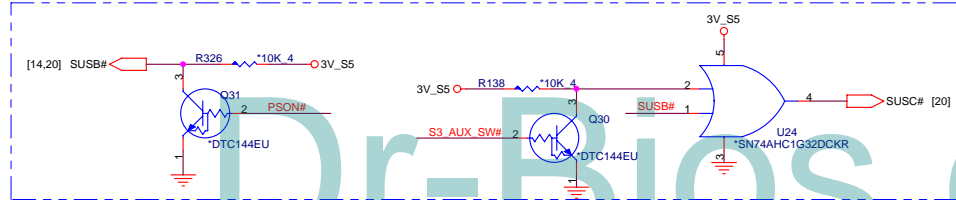
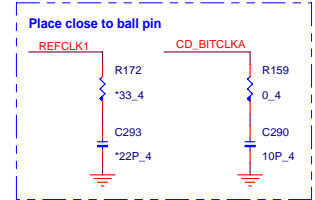
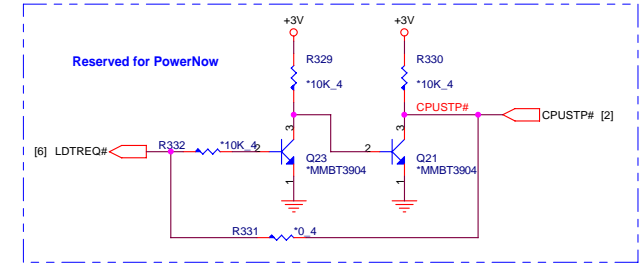
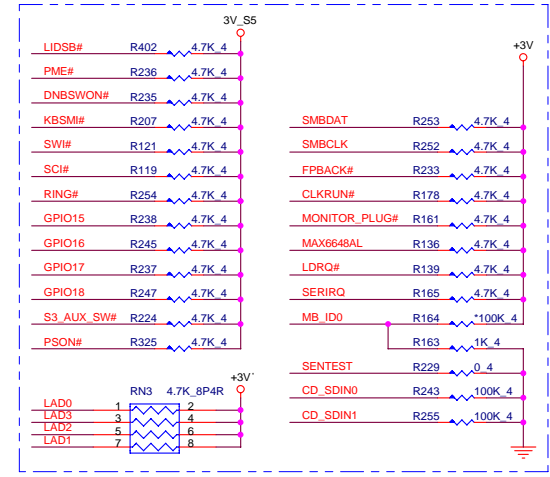
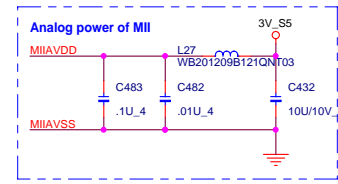
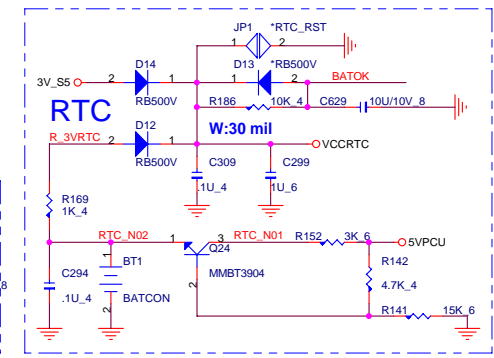
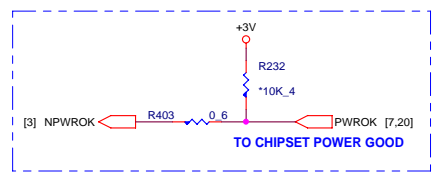
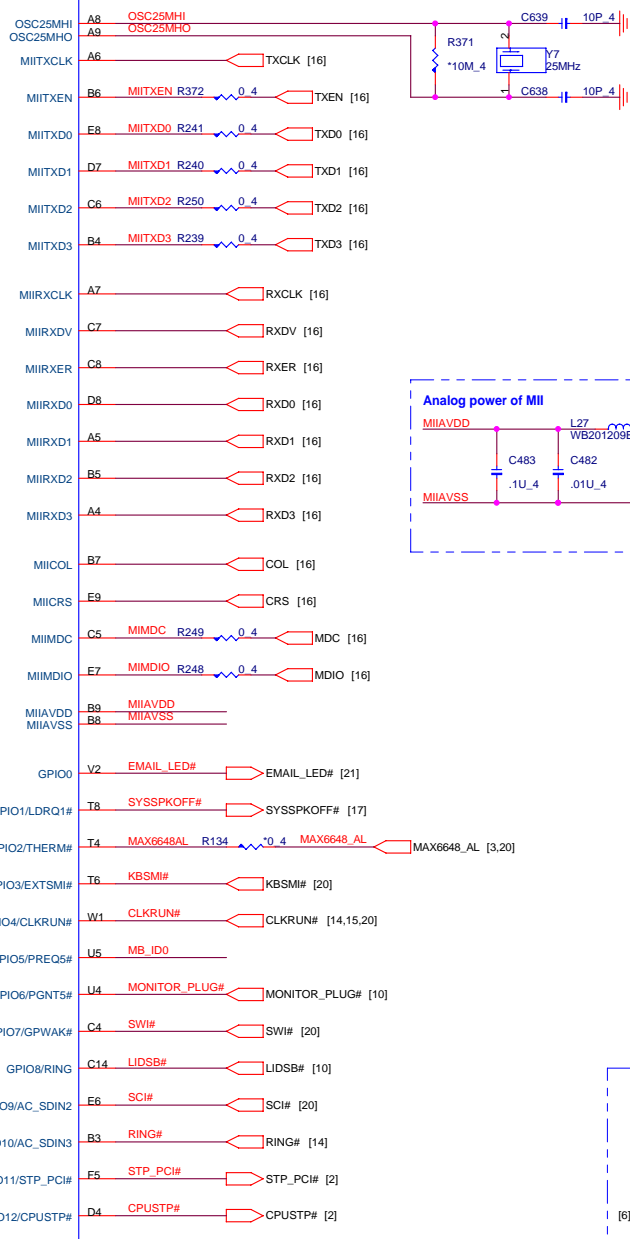
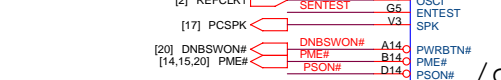
ACPI /others



KBC SPEEDSTEP



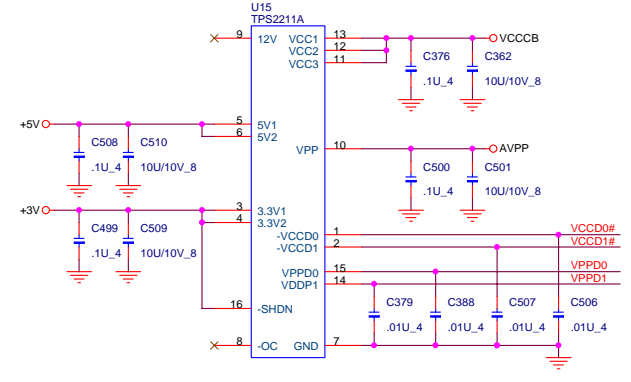
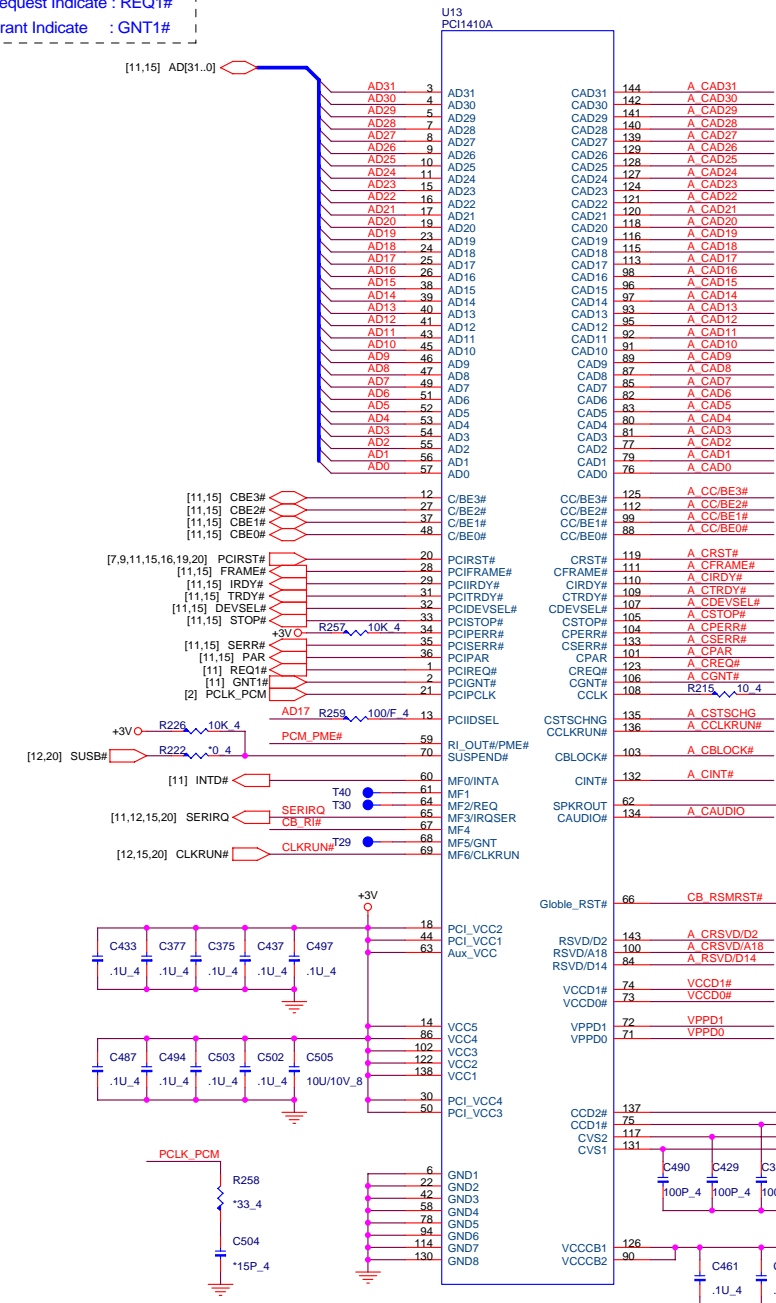
GPIO



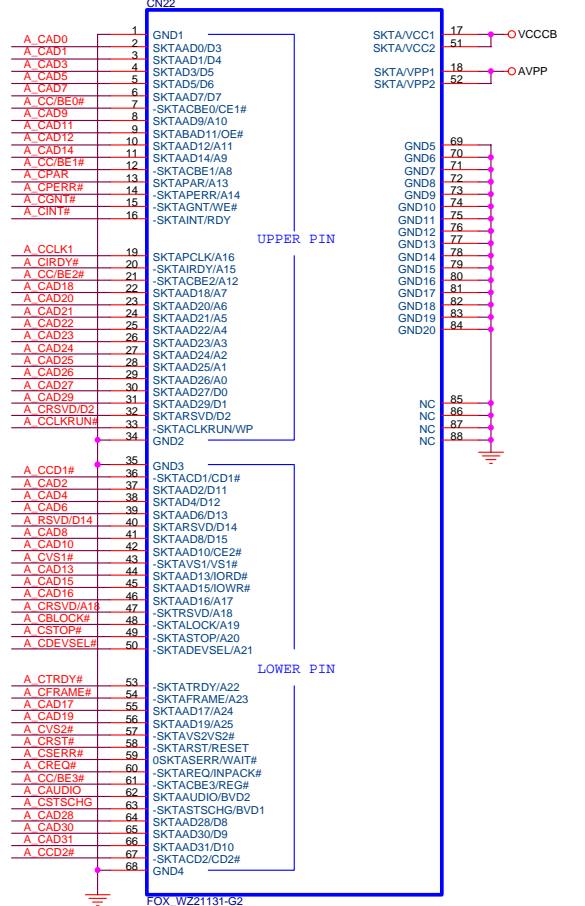
Dr-BIOS.COM

PROJECT : ZL5
Quanta Computer Inc.
 Size Document Number
963L(MISC SIGNAL)
 Date: Thursday, March 10, 2005 Sheet 12 of 26 Rev 3B

ID Select : AD17
 Interrupt Pin : INTD#
 Request Indicate : REQ1#
 Grant Indicate : GNT1#



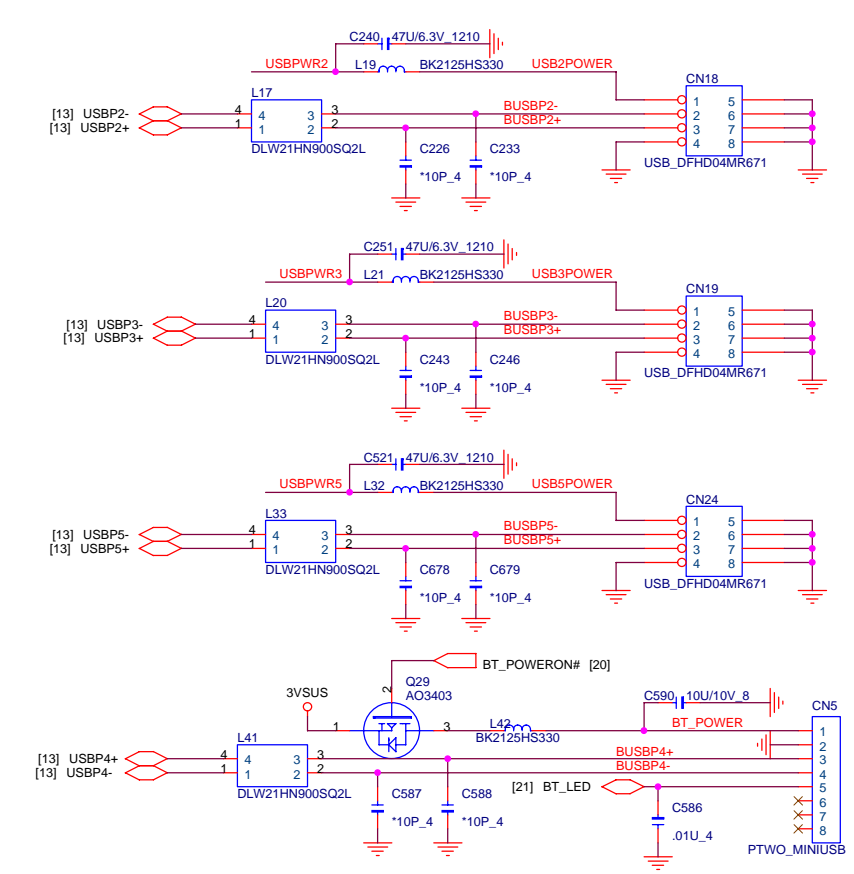
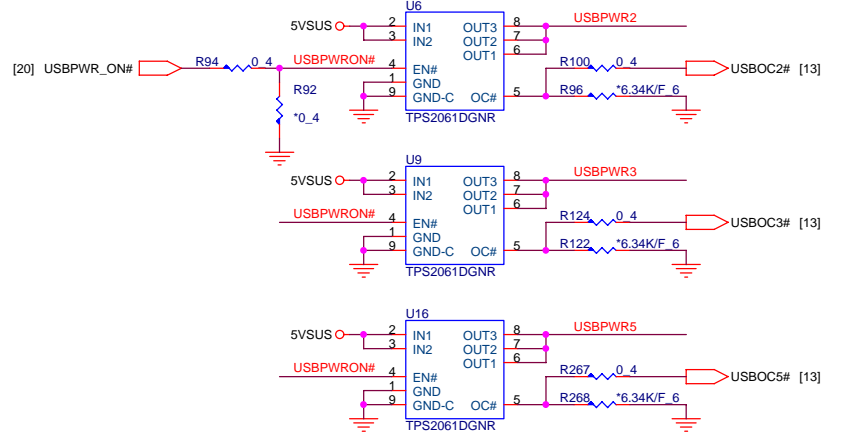
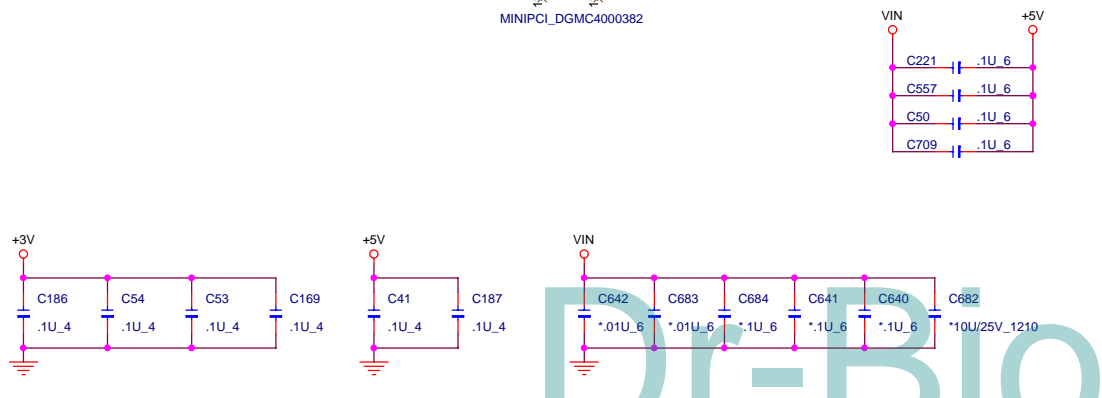
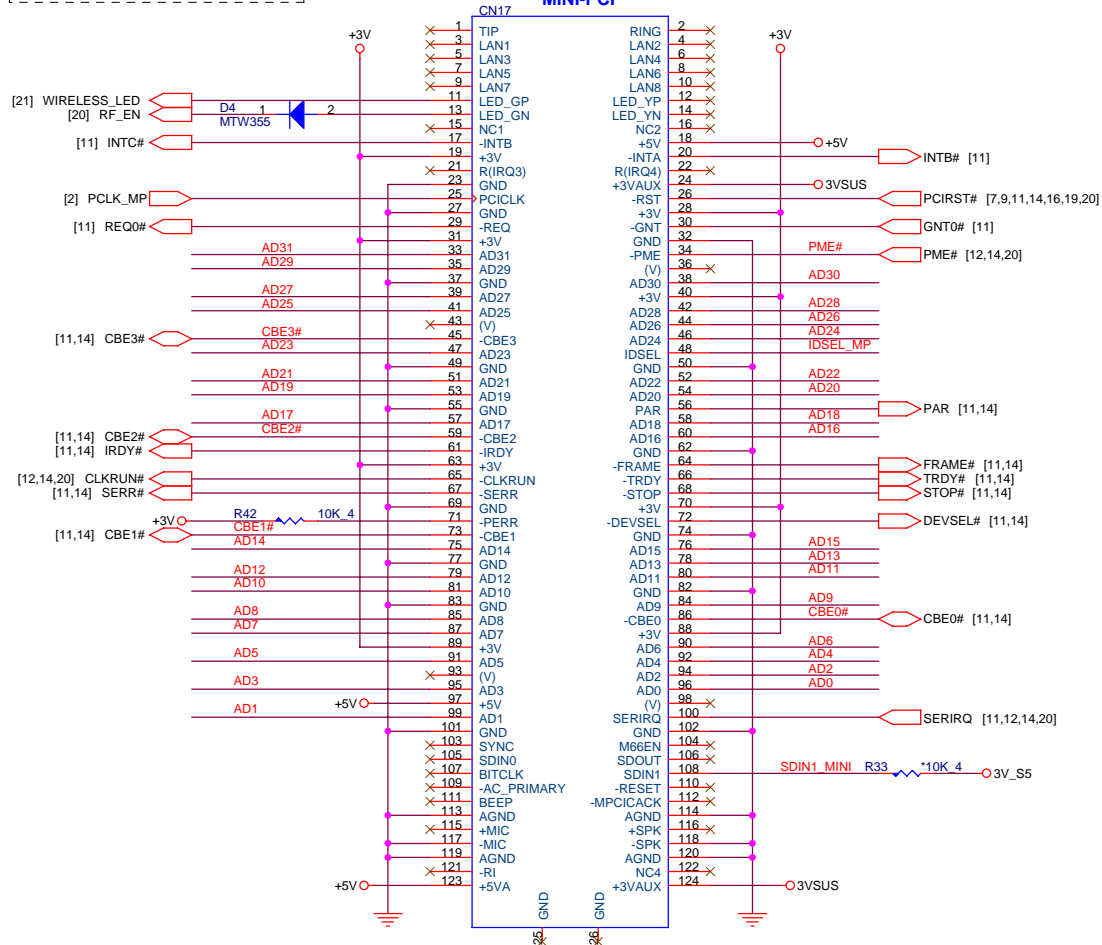
CARBUS SLOT



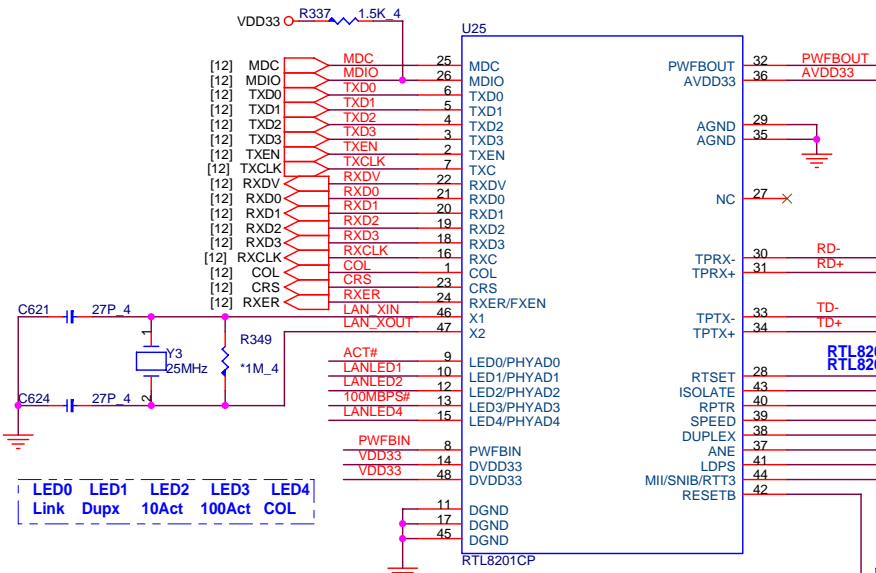
PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	PCMCIA(PCI1410)	3B
Date:	Thursday, March 10, 2005	Sheet 14 of 26

ID Select : AD22
 Interrupt Pin : INTB# , INTC#
 Request Indicate : REQ0#
 Grant Indicate : GNT0#



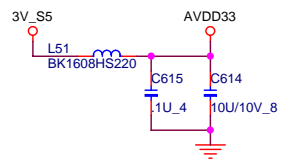
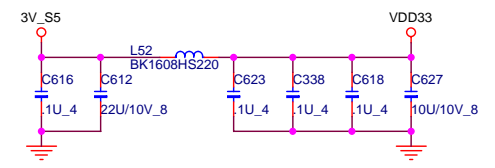
PROJECT : ZL5
Quanta Computer Inc.
 Size Document Number
MINI PCI/USB
 Date: Thursday, March 10, 2005 Sheet 15 of 26 Rev 3B



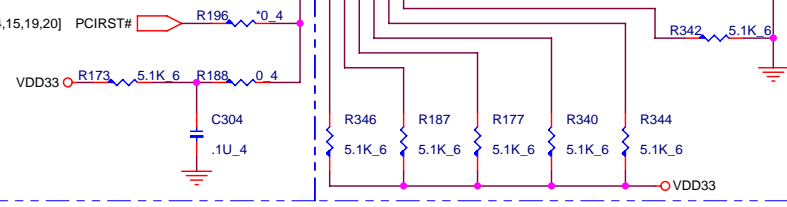
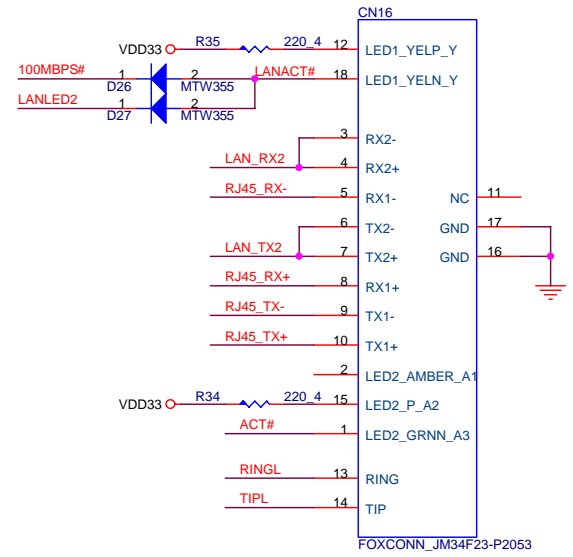
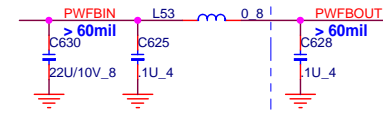
LED0 Link
LED1 Dupx
LED2 10Act
LED3 100Act
LED4 COL

1. You could simply connect RESETB to PCI Reset. And just discard R30, R28, C20.
2. If Wake on Lan feature is needed, you have to supply power from auxiliary power for all LAN-related circuit including RTL8201BL/CL/CP and MAC. In this kind of application, discard R29 and retain other components for one resetting upon power up.

RTL8201BL : R5 (5.9K 1%)
RTL8201CL/RTL8201CP : R5 (2K 1%)



Place close to PWFBIN | Place close to PWFBOUT

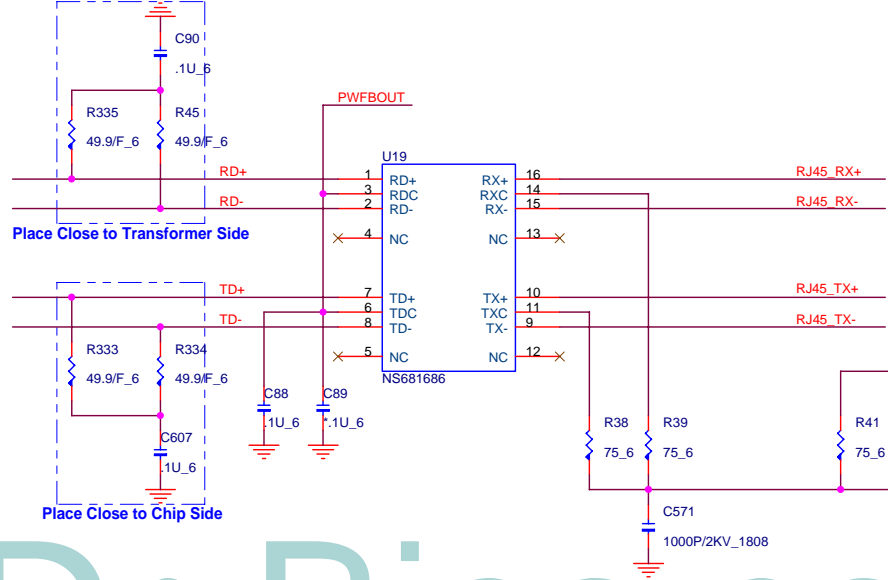


Reserved for 8201CL/CP LED Mode
Change to compatible with BL
COL R354 5.1K 4 VDD33

Reserved for ensuring
8201BL/CL/CP latch to UTP Mode.
RXER R339 5.1K 4

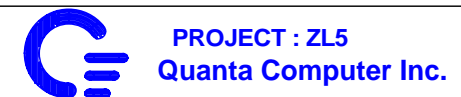
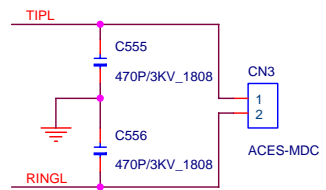
Reserved for ensuring 8201CL/CP
latch to normal operation mode.
CRS R341 5.1K 4

ACT# R351 5.1K 4 VDD33
100MBPS# R350 5.1K 4
LANLED2 R353 5.1K 4
LANLED1 R352 5.1K 4
LANLED4 R347 5.1K 4



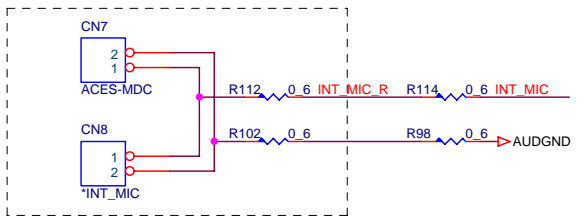
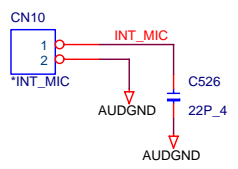
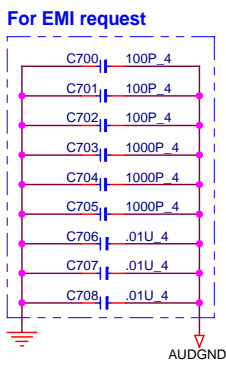
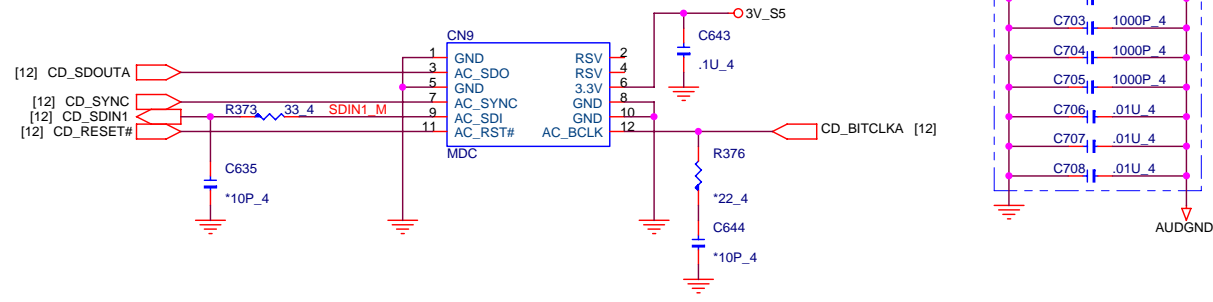
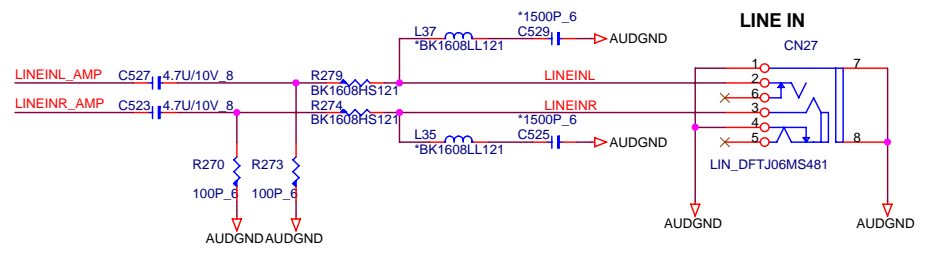
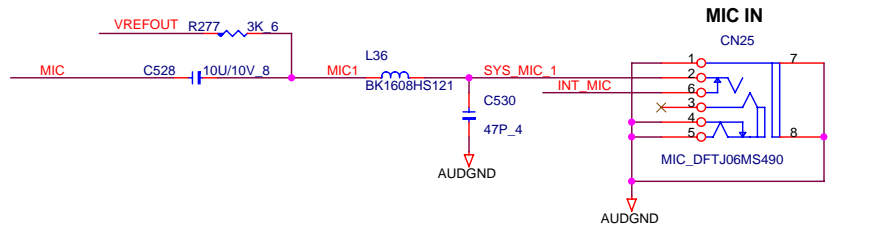
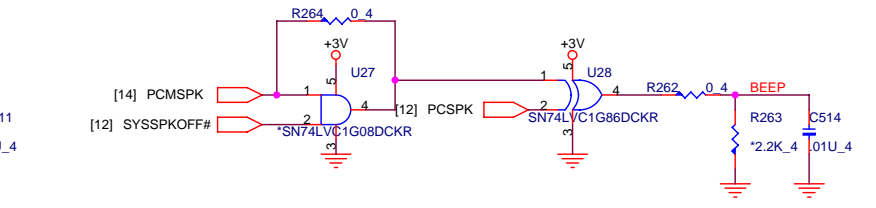
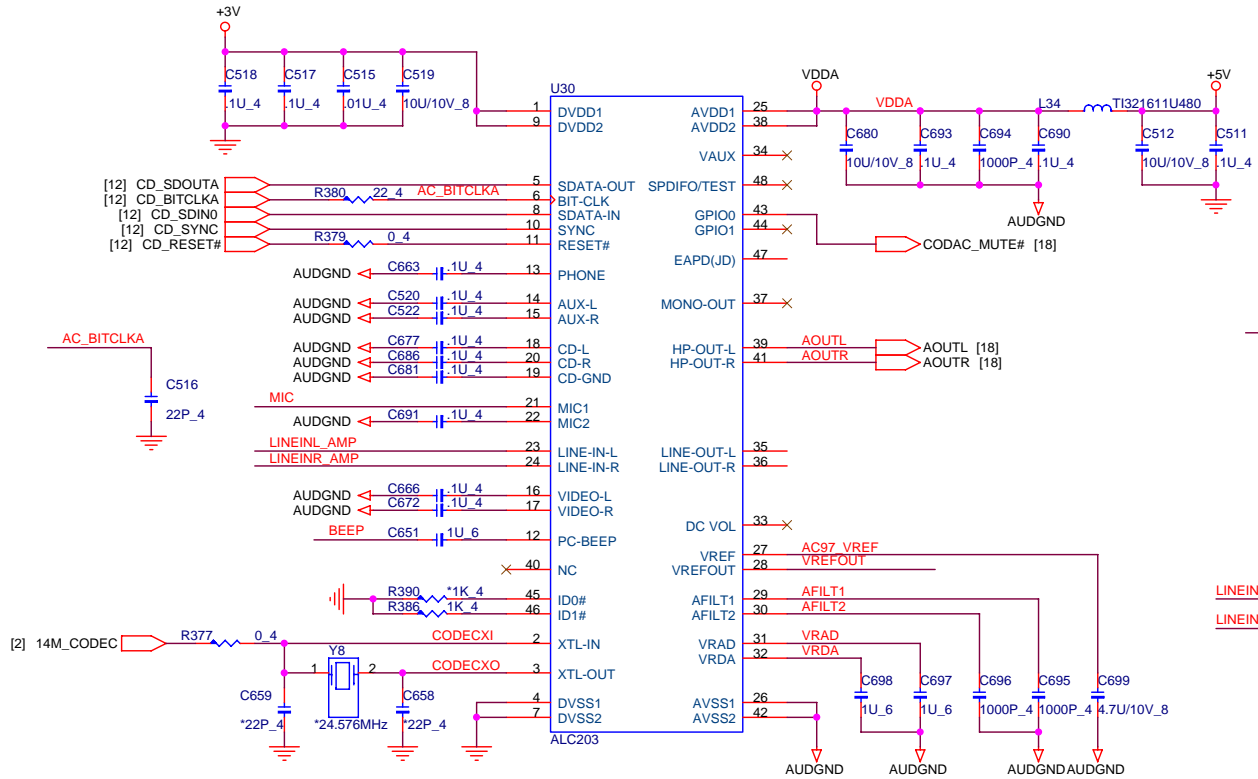
Place Close to Transformer Side


Place Close to Chip Side



Size	Document Number	Rev
	LAN RTL8201CP	3B
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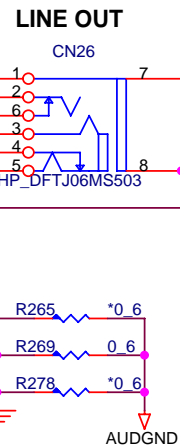
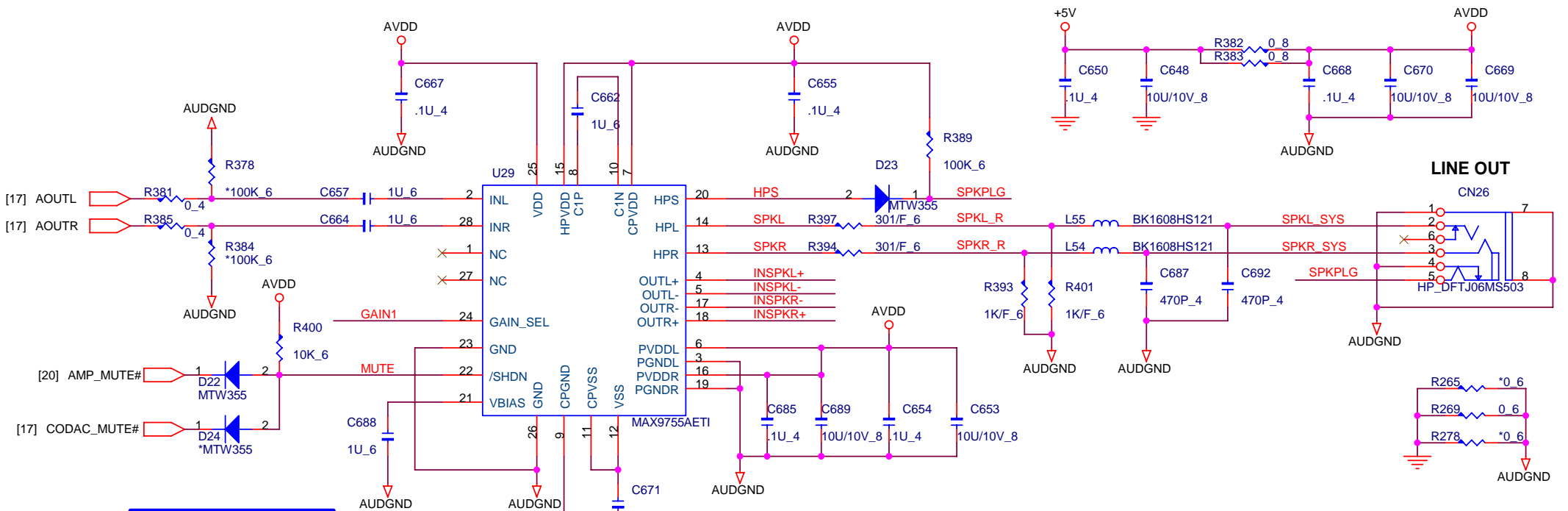
Dr-Bios.com



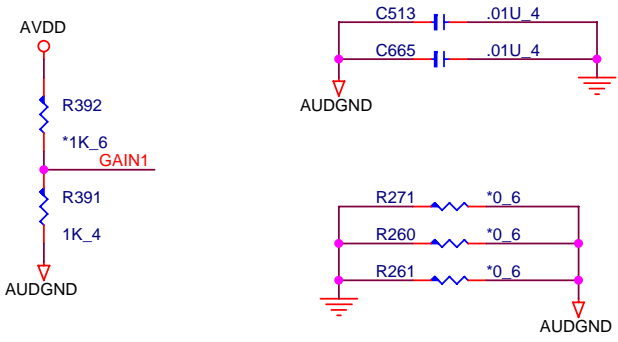
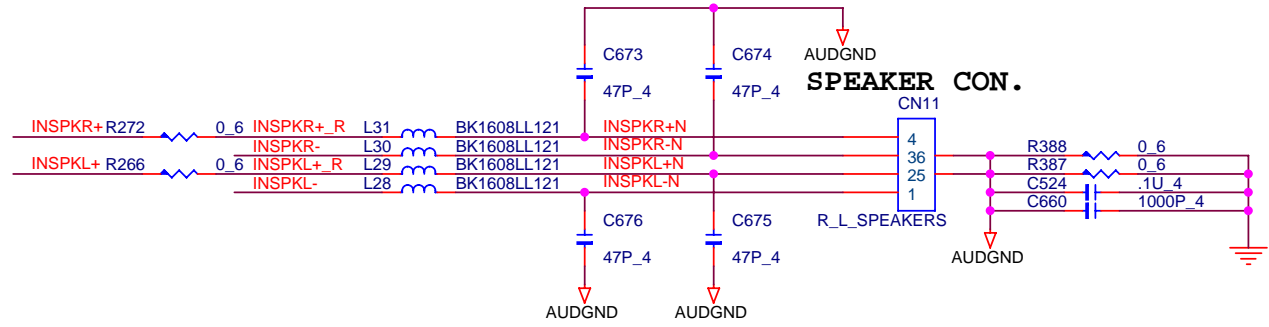


PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	CODEC(ALC203)/MDC1.5	3B
Date:	Thursday, March 10, 2005	Sheet 17 of 26



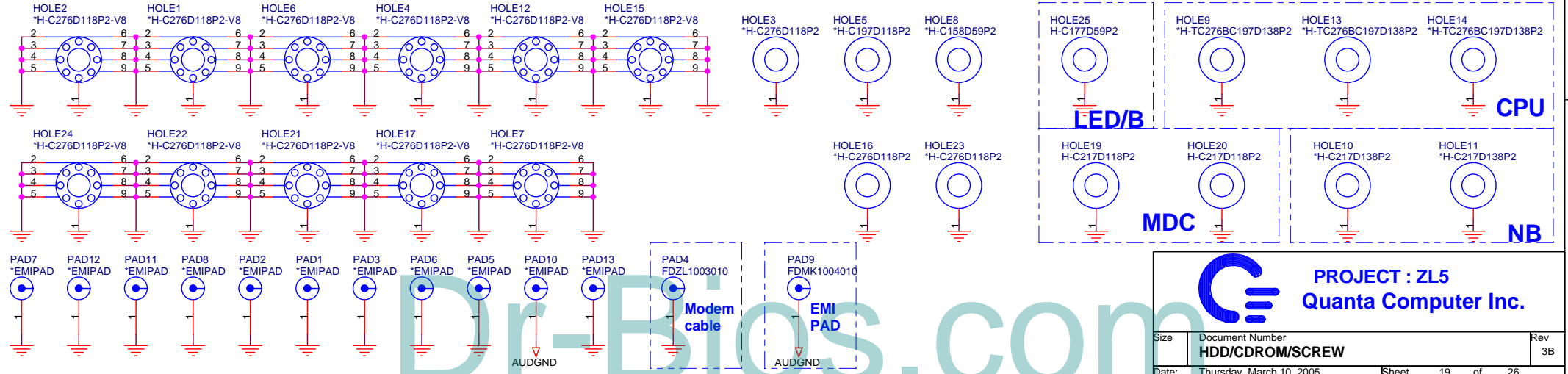
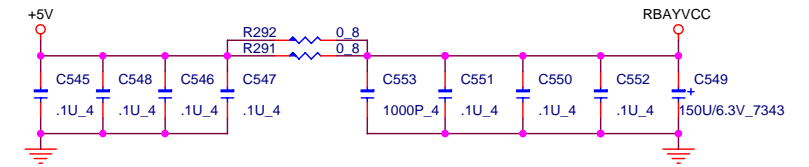
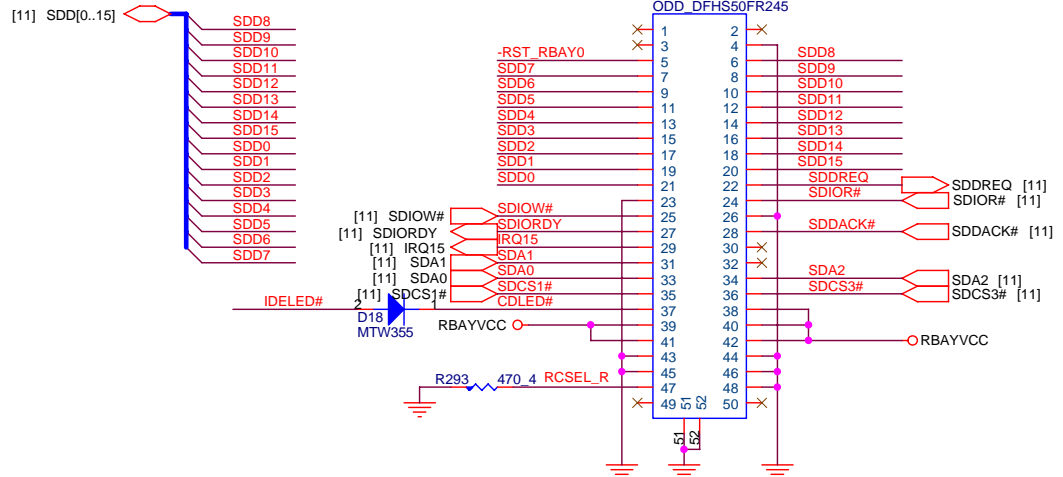
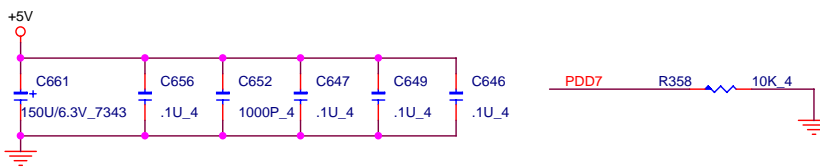
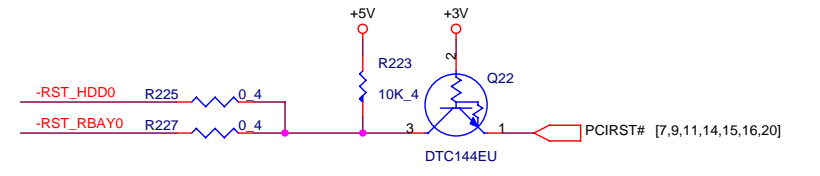
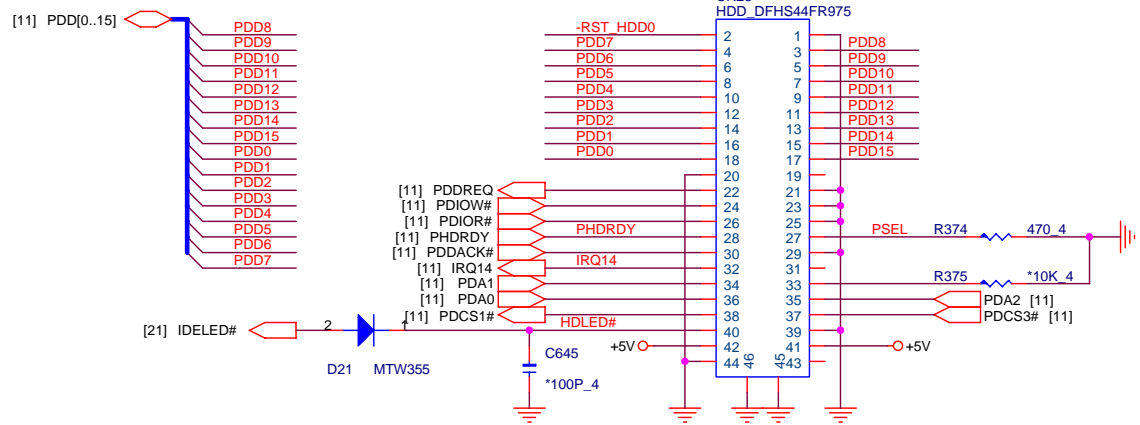
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



PROJECT : ZL5
Quanta Computer Inc.

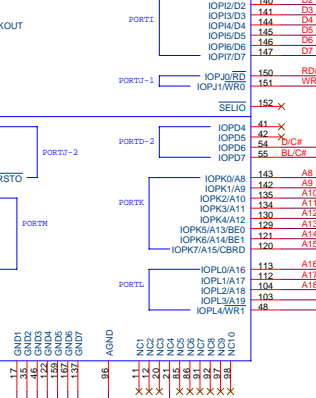
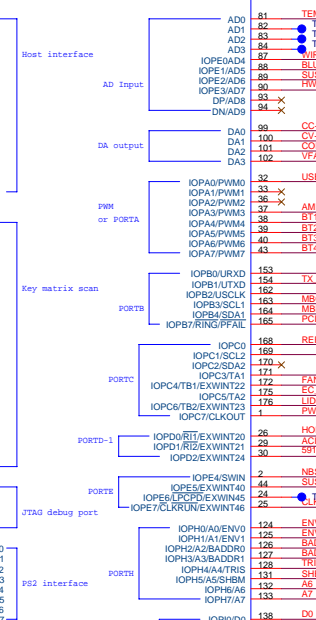
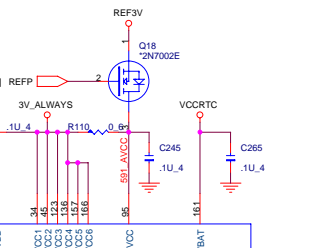
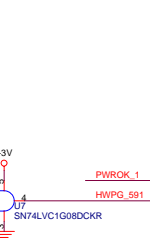
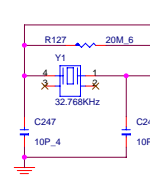
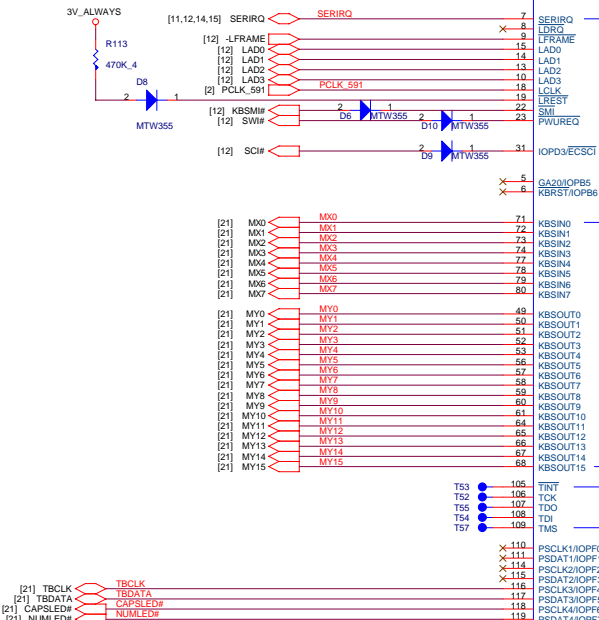
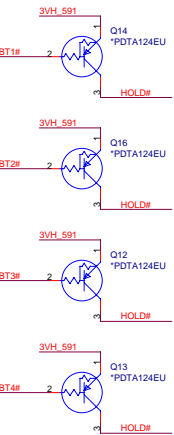
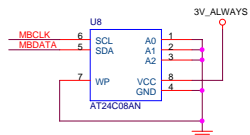
Size	Document Number	Rev
	AUDIO AMP	3B
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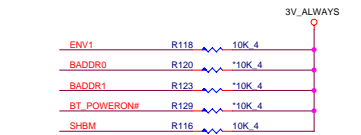
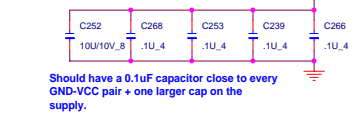
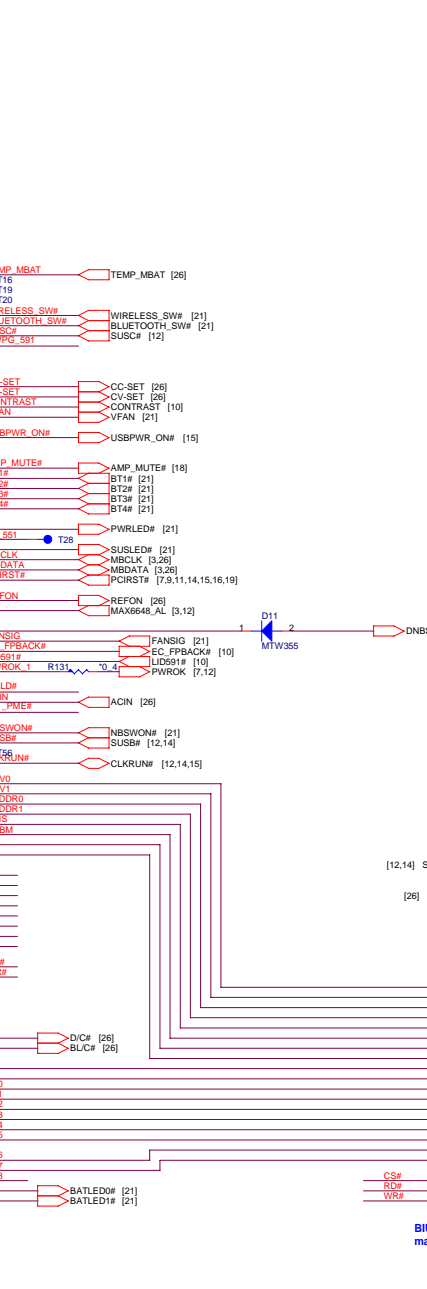


PROJECT : ZL5
Quanta Computer Inc.
 Size Document Number
HDD/CDROM/SCREW
 Date: Thursday, March 10, 2005 Sheet 19 of 26 Rev 3B

LDRQ#(pin 8) internal is no use

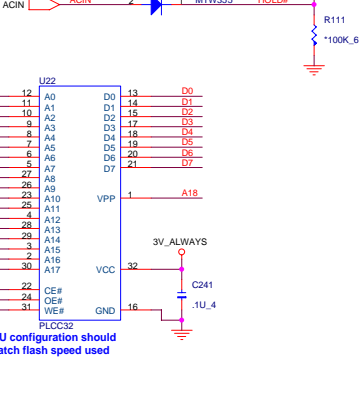
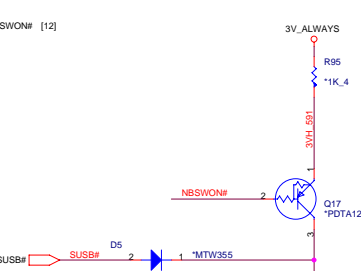
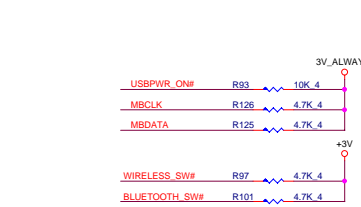


FOR 97551 ONLY



SHBM=1: Enable shared memory with host BIOS

BADDR0-1	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGGBAH, HCFGGBAL)+1
1 1	Reserved	



BIU configuration should match flash speed used

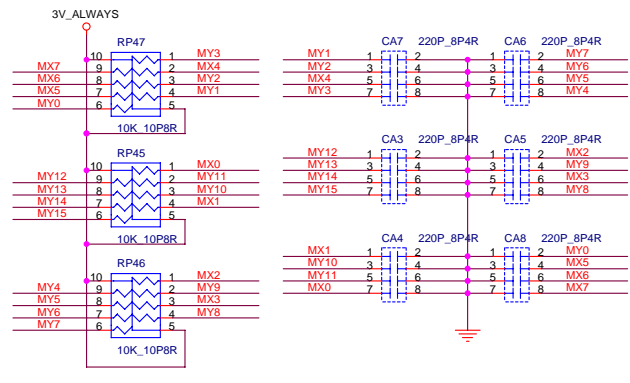
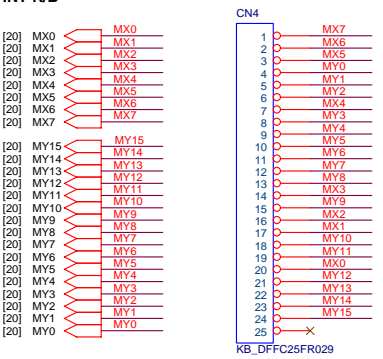


PROJECT : ZL5
Quanta Computer Inc.

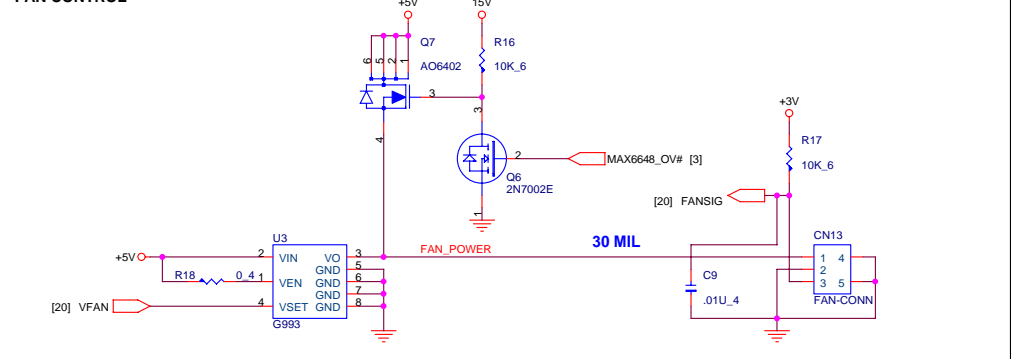
Size: Document Number
PC97551/FLASH

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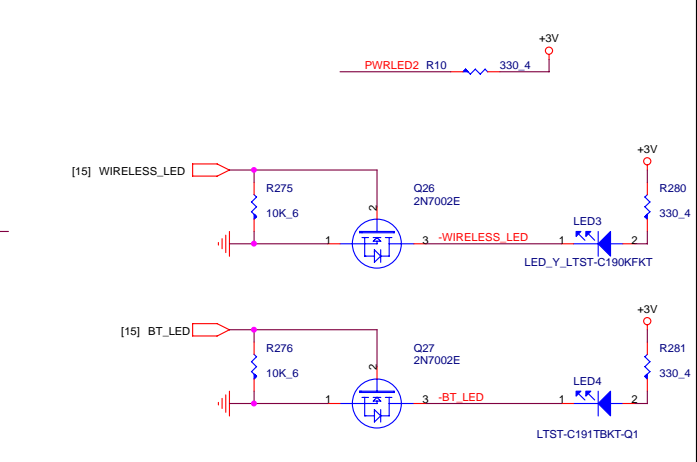
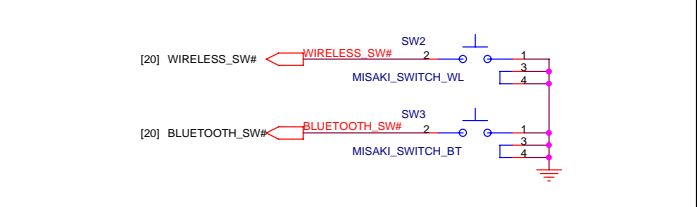
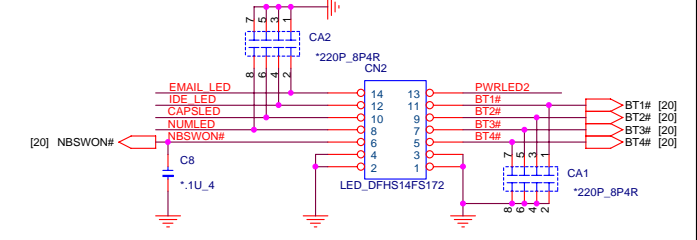
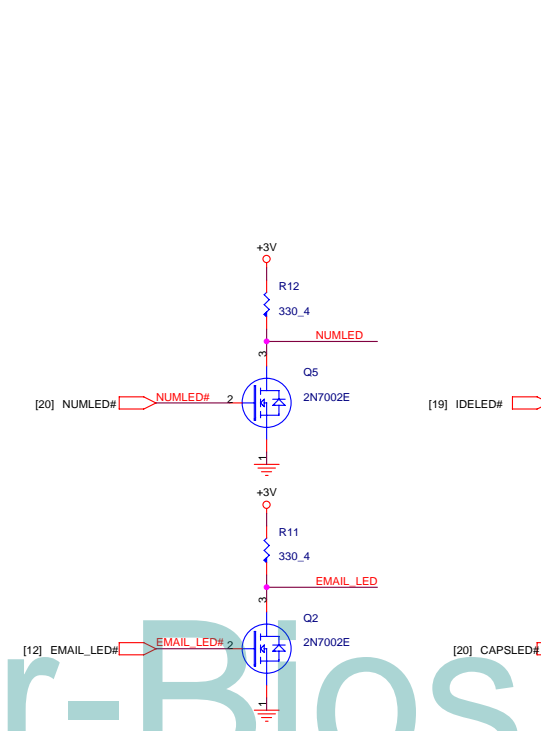
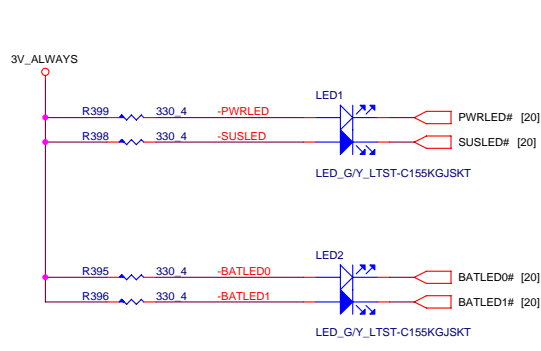
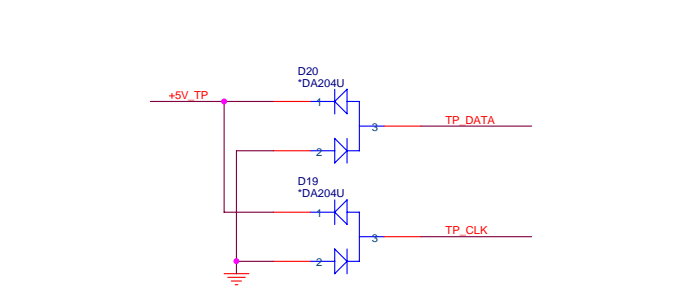
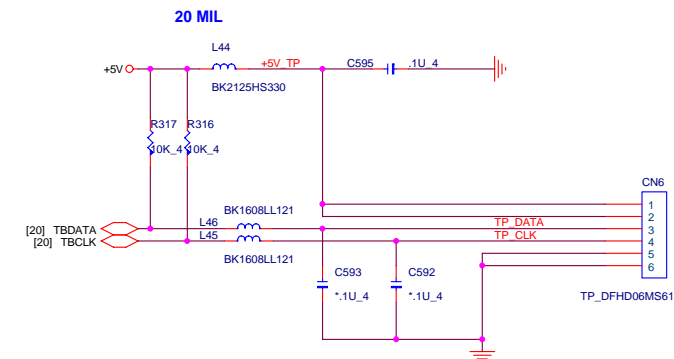
INT K/B



FAN CONTROL



TOUCH PAD

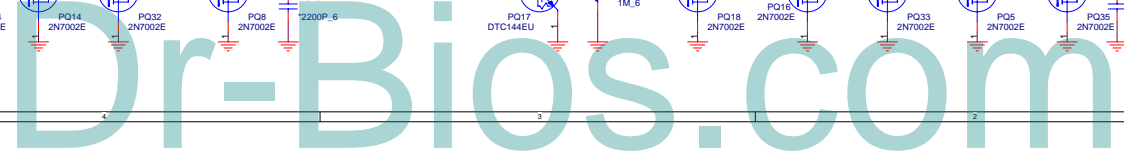
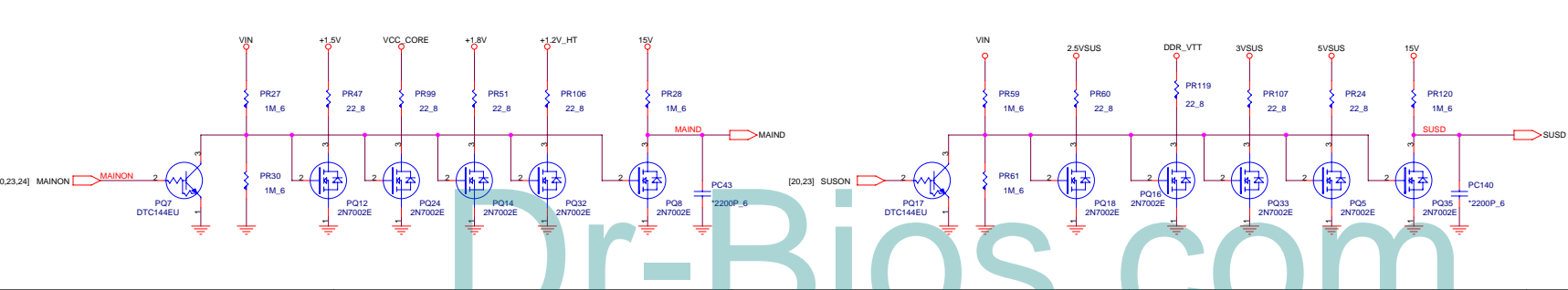
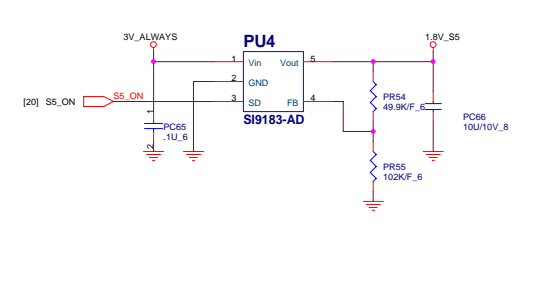
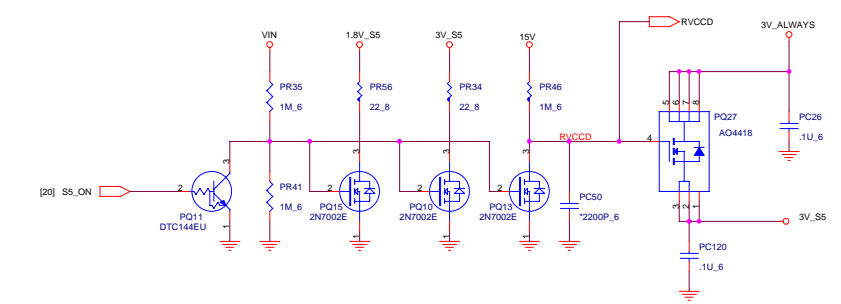
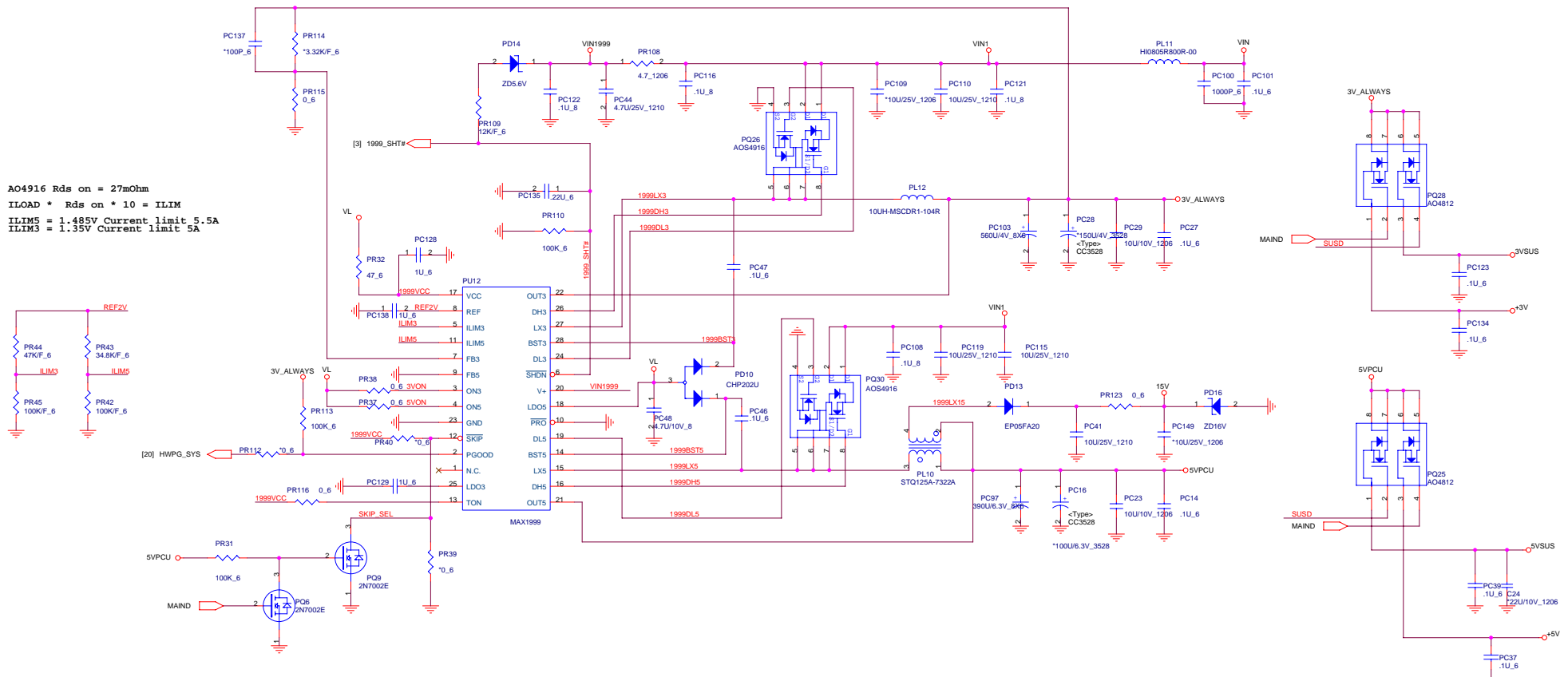


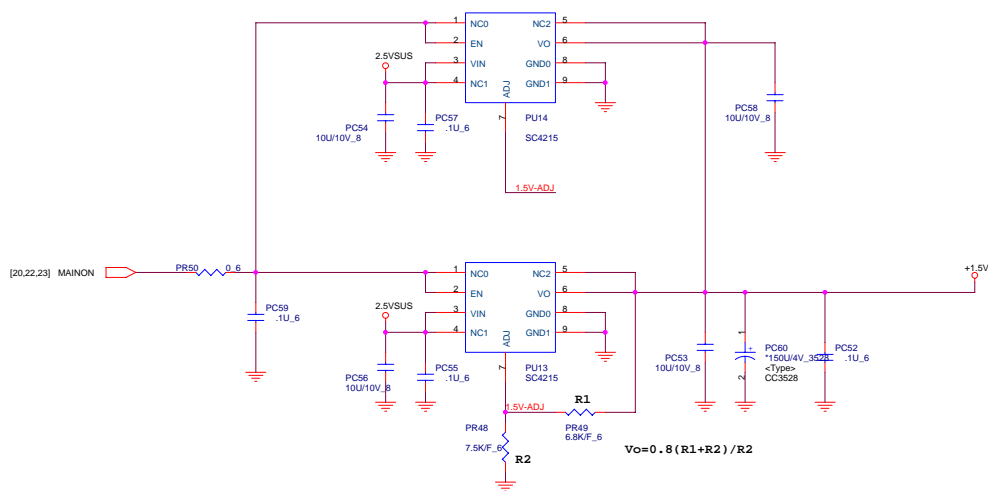
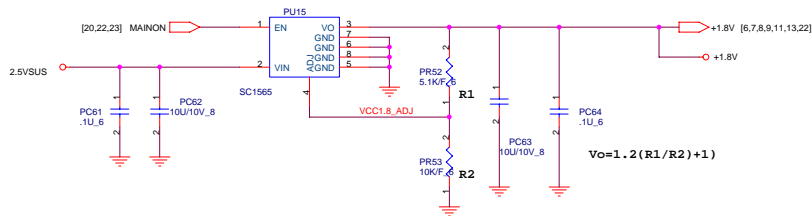
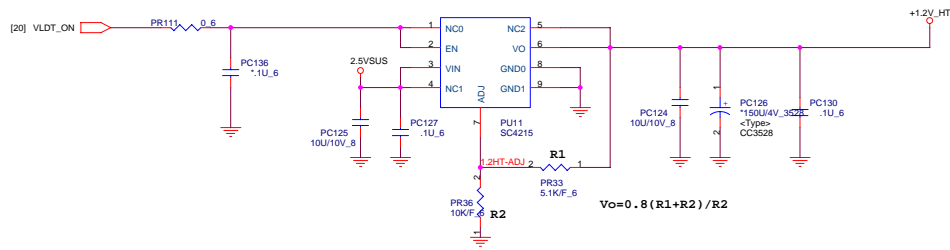
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Quanta Computer Inc.

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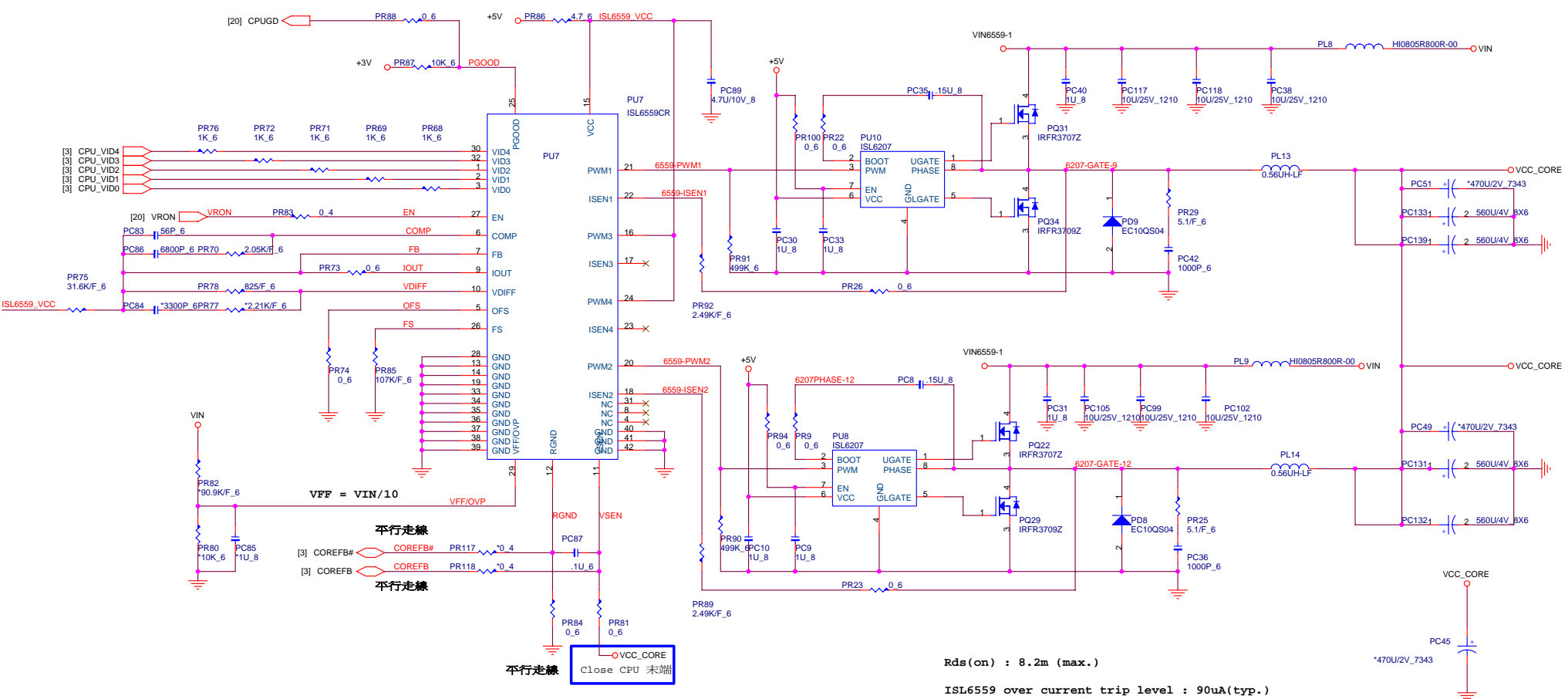
AO4916 Rds on = 27mOhm
 ILOAD * Rds on * 10 = ILIM
 ILIM5 = 1.485V Current limit 5.5A
 ILIM3 = 1.35V Current limit 5A



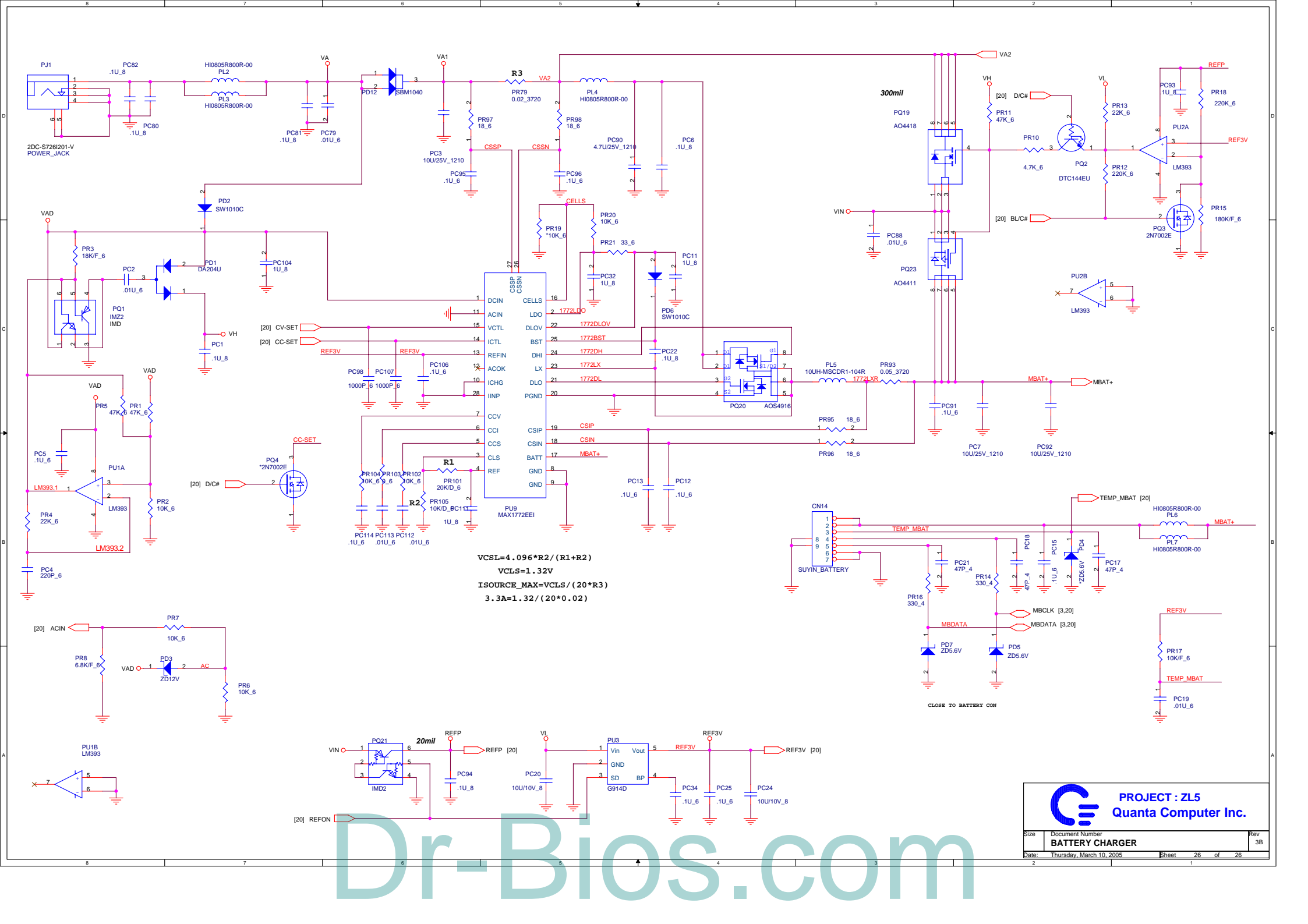


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Vcore



Rds(on) : 8.2m (max.)
ISL6559 over current trip level : 90uA(typ.)
Full load Isen current : 90uA/1.5 ~ 60uA
AMD LPM 35W CORE current 28A
 $Rds(on) * Io(phase) = Rsen * Isen$
 $8.2m * 1.3 * (28A/2) = Rsen * 60uA$
Rsen = 2.48K ~ 2.49K
OCP : 28A * 1.5 = 42A



$$VCSL = 4.096 * R2 / (R1 + R2)$$

$$VCLS = 1.32V$$

$$ISOURCE_MAX = VCLS / (20 * R3)$$

$$3.3A = 1.32 / (20 * 0.02)$$

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