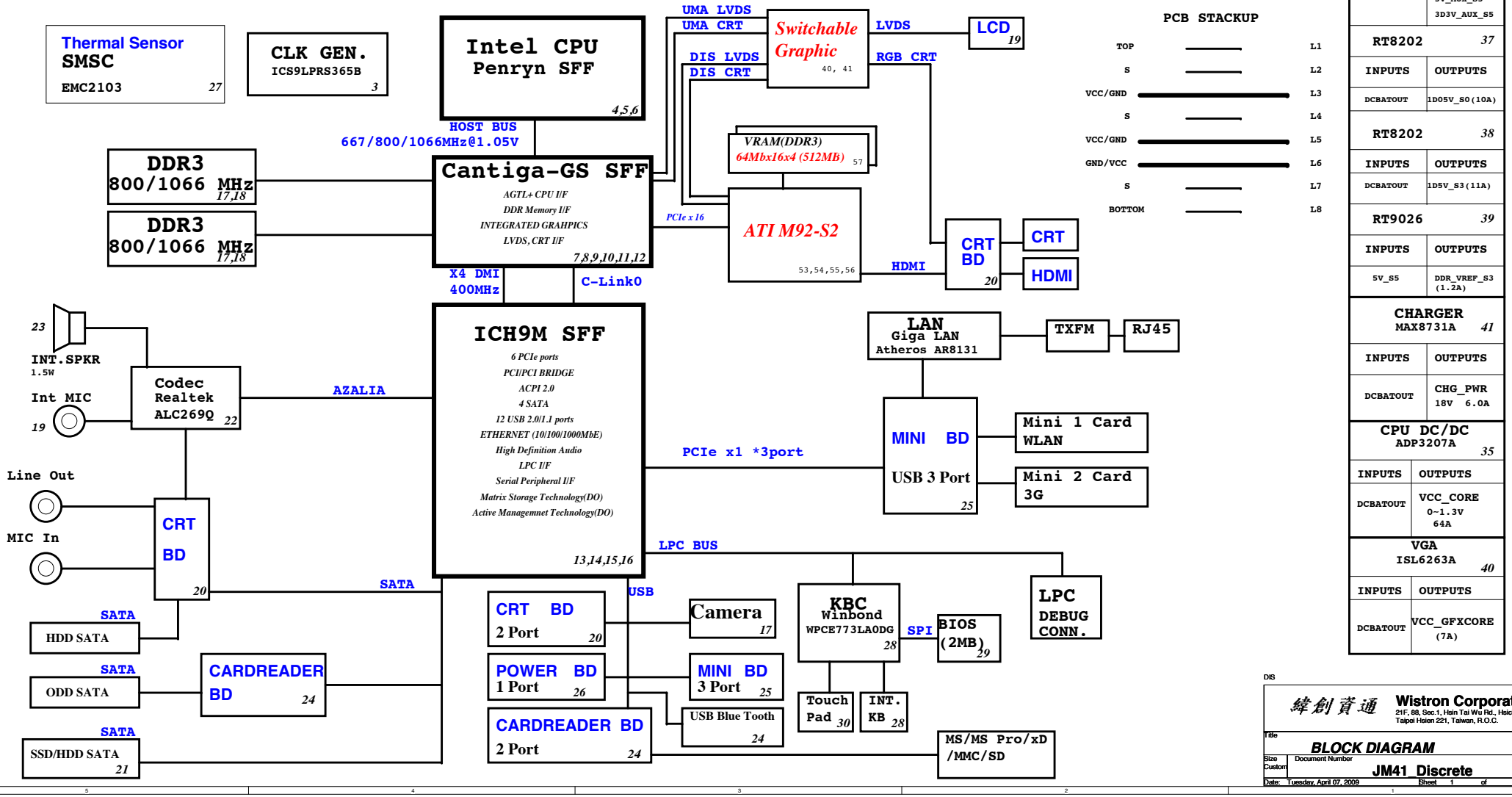
JM41/JM51 Discrete Block Diagram

Project code: 91.4CQ01.001
PCB P/N : 48.4CQ01.0SB
REVISION : 08274-1



PCB STACKUP

TOP	L1
S	L2
VCC/GND	L3
S	L4
VCC/GND	L5
GND/VCC	L6
S	L7
BOTTOM	L8

SYSTEM DC/DC TPS51125 36

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5

RT8202 37

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A)

RT8202 38

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(11A)

RT9026 39

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 (1.2A)

CHARGER MAX8731A 41

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ADP3207A 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 64A

VGA ISL6263A 40

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

DIS

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Title: BLOCK DIAGRAM
Size: Custom | Document Number: JM41_Discrete | Rev: -1
Date: Tuesday, April 07, 2009 | Sheet 1 of 48

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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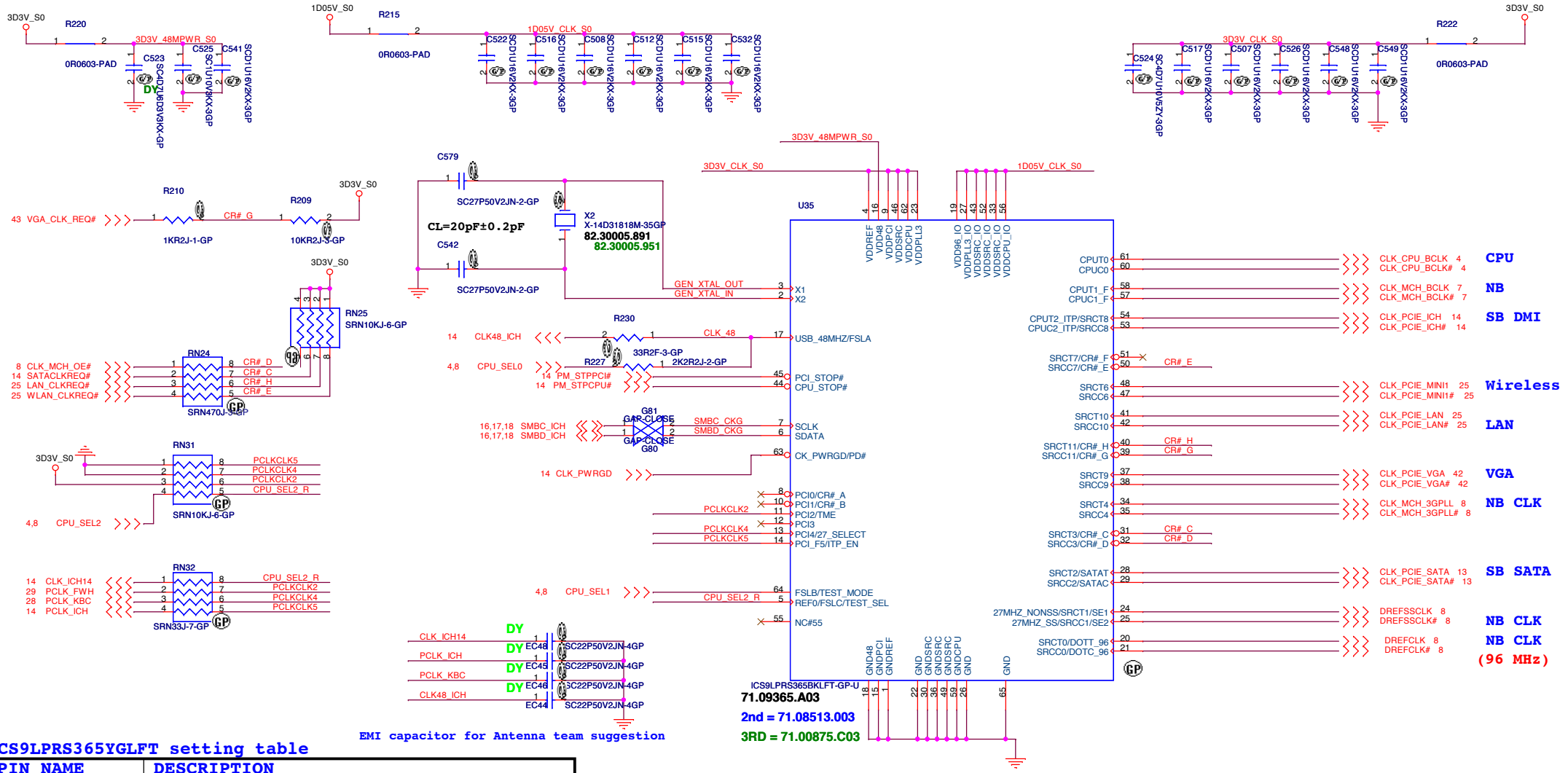
Title: Reference
Size: A3 | Document Number: JM41 Discrete | Rev: -1
Date: Monday, April 06, 2009 | Sheet 2 of 48



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: *Clock Generator*

Size	Document Number	Rev
	JM41_Discrete	-1

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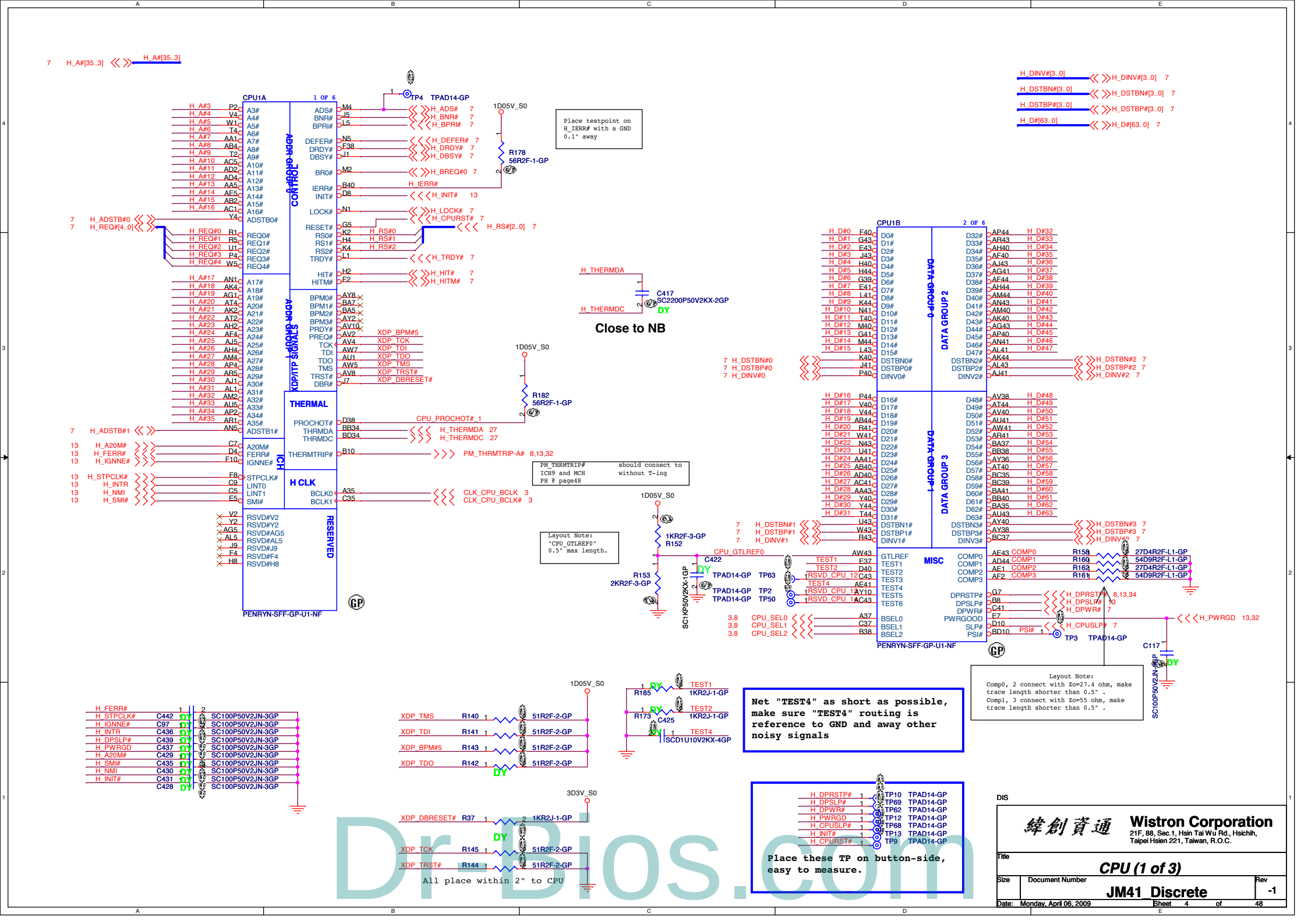
CPU1A
1 OF 6
CONTROL
ADDR GROUP 0
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
PENRYN-SFF-GP-U1-NF
CPU1B
2 OF 6
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
MISC
PENRYN-SFF-GP-U1-NF
TP4 TPAD14-GP
Place testpoint on H_IERR# with a GND 0.1" away
R178 56R2F-1-GP
R182 56R2F-1-GP
Close to NB
C417 SC2200P50V2KX-2GP
R152 1KR2F-3-GP
R153 2KR2F-3-GP
SC1KP50V2KX-1GP
C422
Layout Note: "CPU_GTLREF0" 0.5" max length.
PM_THRMTRIP# should connect to ICH9 and MCH PH @ page48
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
SC100P50V2JN-GP
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
R185 1KR2J-1-GP
R173 1KR2J-1-GP
C425 SCD1U10V2KX-4GP
R140 51R2F-2-GP
R141 51R2F-2-GP
R143 51R2F-2-GP
R142 51R2F-2-GP
R37 1KR2J-1-GP
R145 51R2F-2-GP
R144 51R2F-2-GP
All place within 2" to CPU
SC100P50V2JN-3GP
Place these TP on button-side, easy to measure.
TP10 TPAD14-GP
TP69 TPAD14-GP
TP62 TPAD14-GP
TP12 TPAD14-GP
TP68 TPAD14-GP
TP13 TPAD14-GP
TP9 TPAD14-GP
TP3 TPAD14-GP
TP63 TPAD14-GP
TP2 TPAD14-GP
TP50 TPAD14-GP
R158 27D4R2F-L1-GP
R160 54D9R2F-L1-GP
R162 27D4R2F-L1-GP
R161 54D9R2F-L1-GP
C117
DIS
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Title
CPU (1 of 3)
Size
Document Number
JM41_Discrete
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-1
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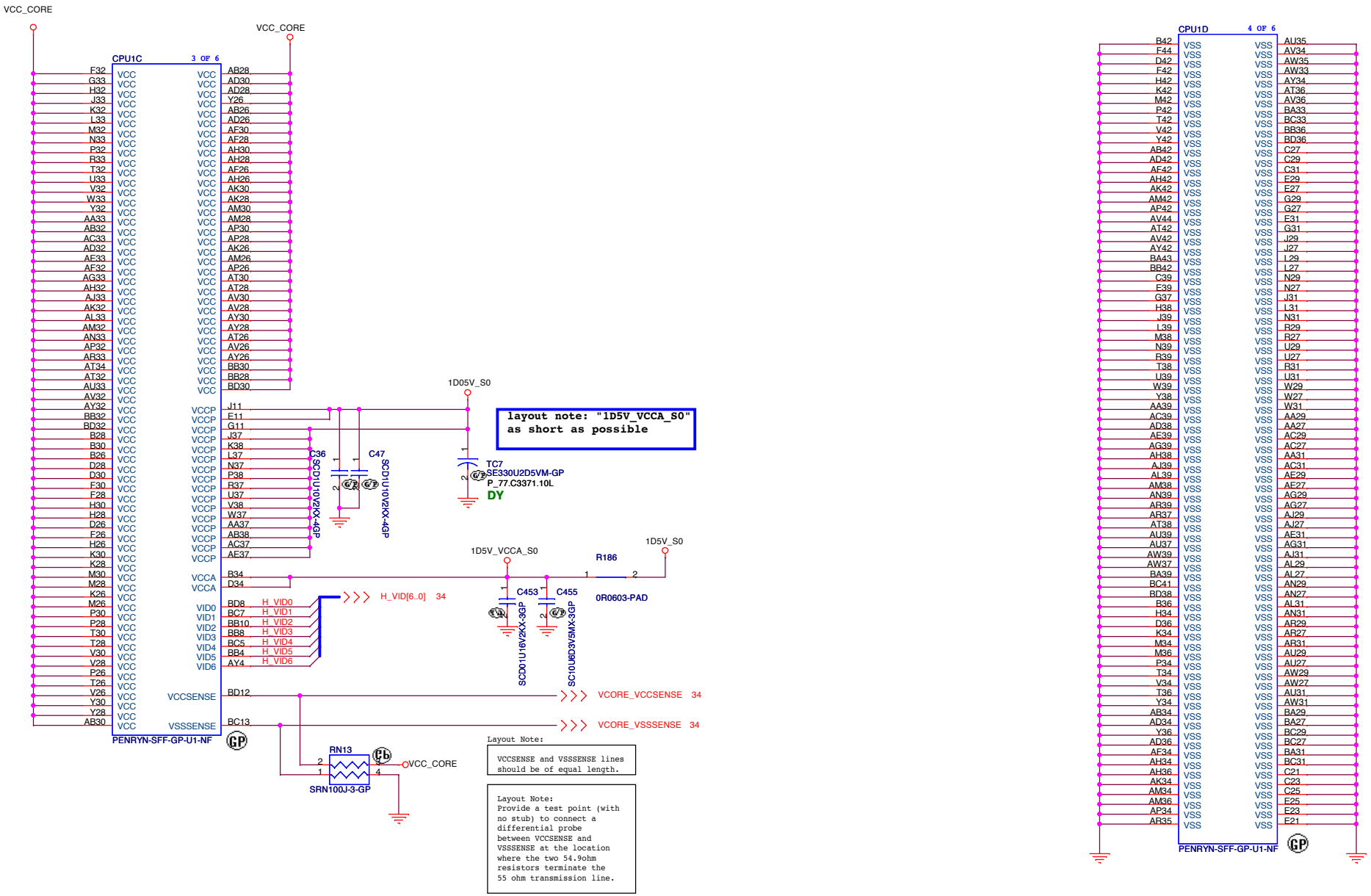

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Title	CPU (2 of 3)	
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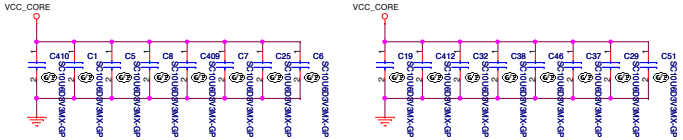
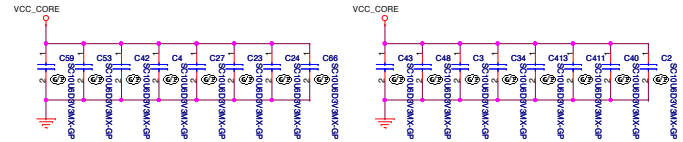
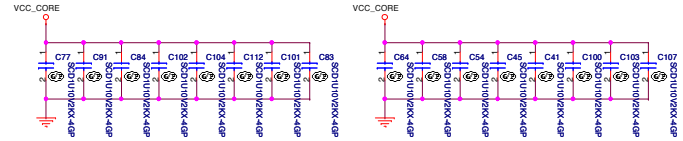
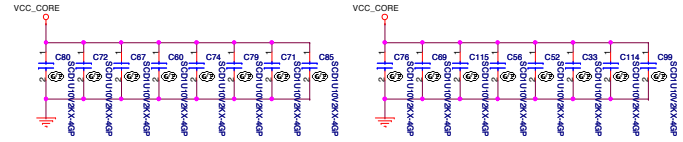
Place these inside socket
cavity on L8(North side Secondary)

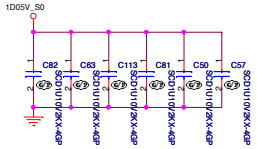


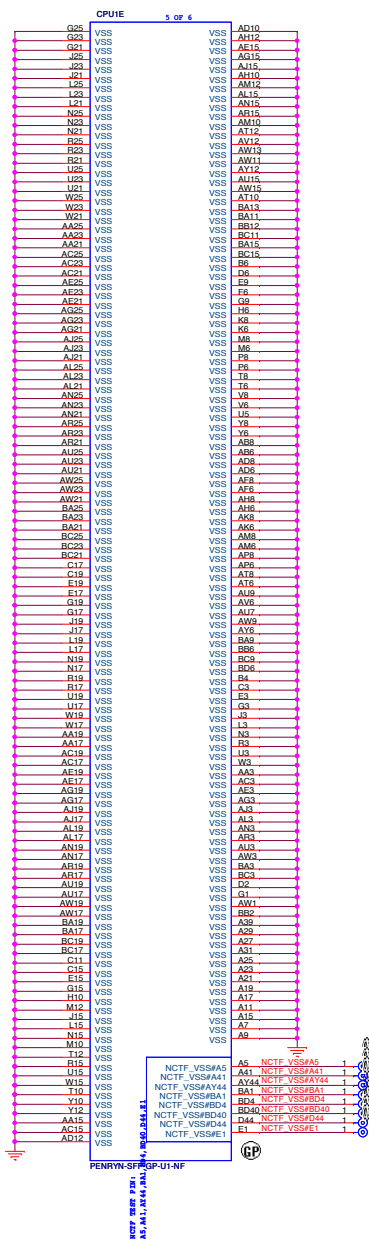


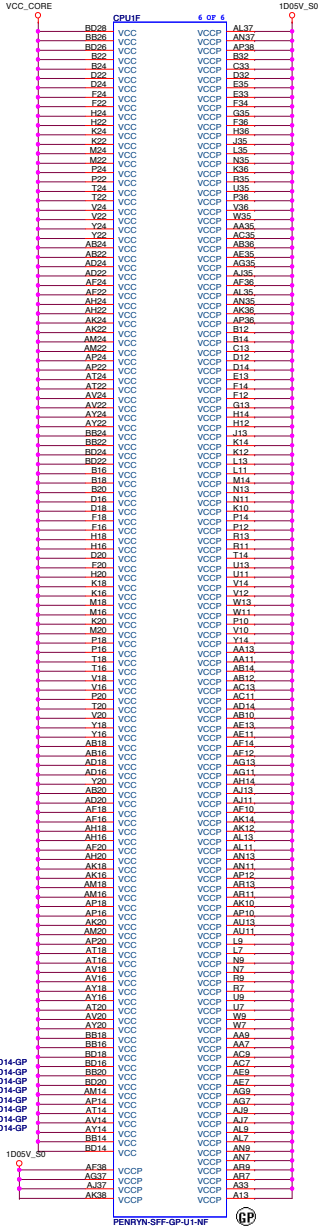




Place these inside socket
cavity on L8(North side Secondary)







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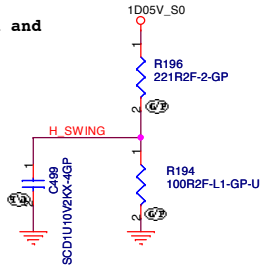
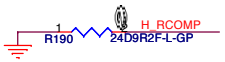
H_SWING routing Trace width and Spacing use 10 / 20 mil

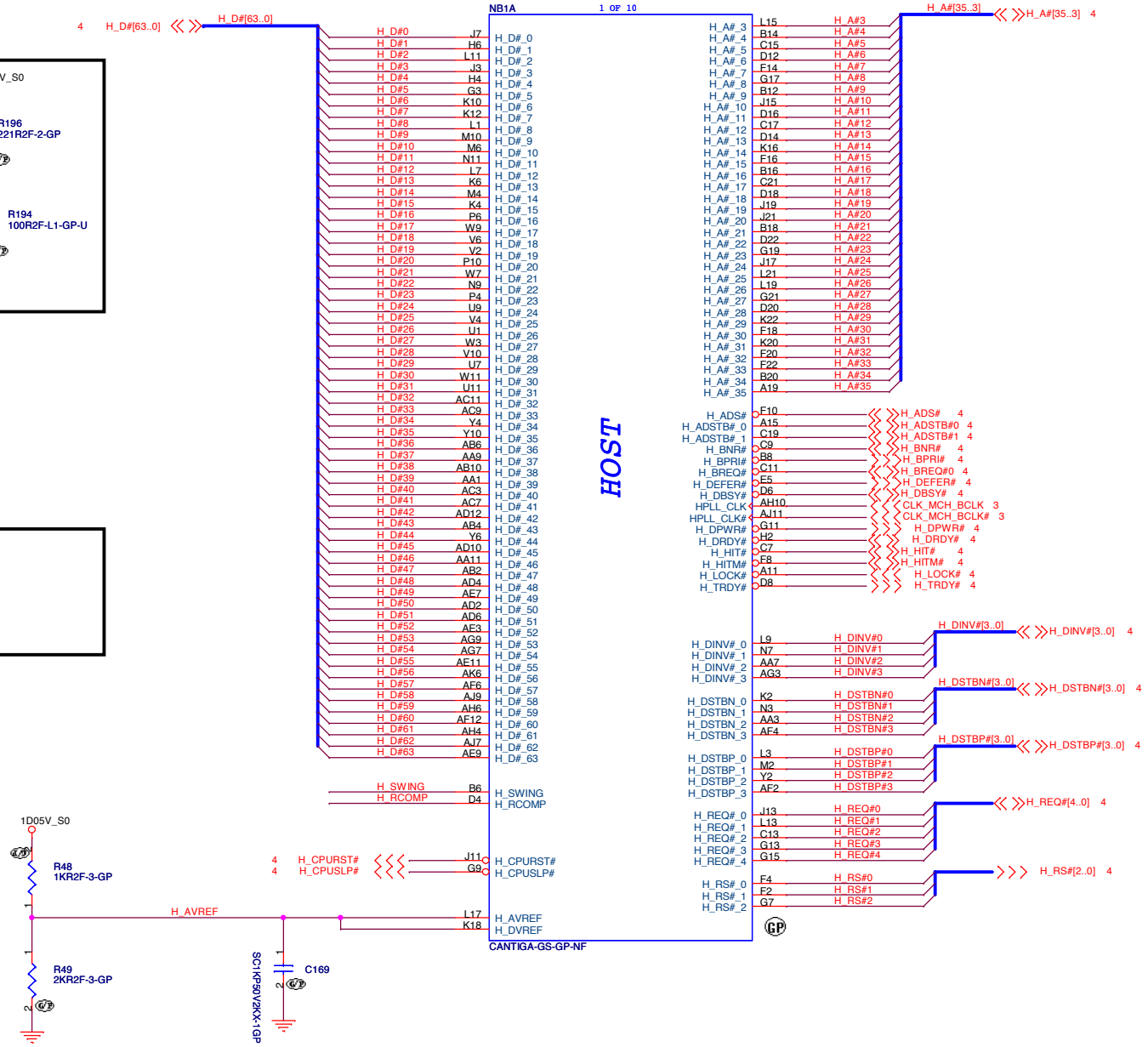
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Title: ***Cantiga (1 of 6)***

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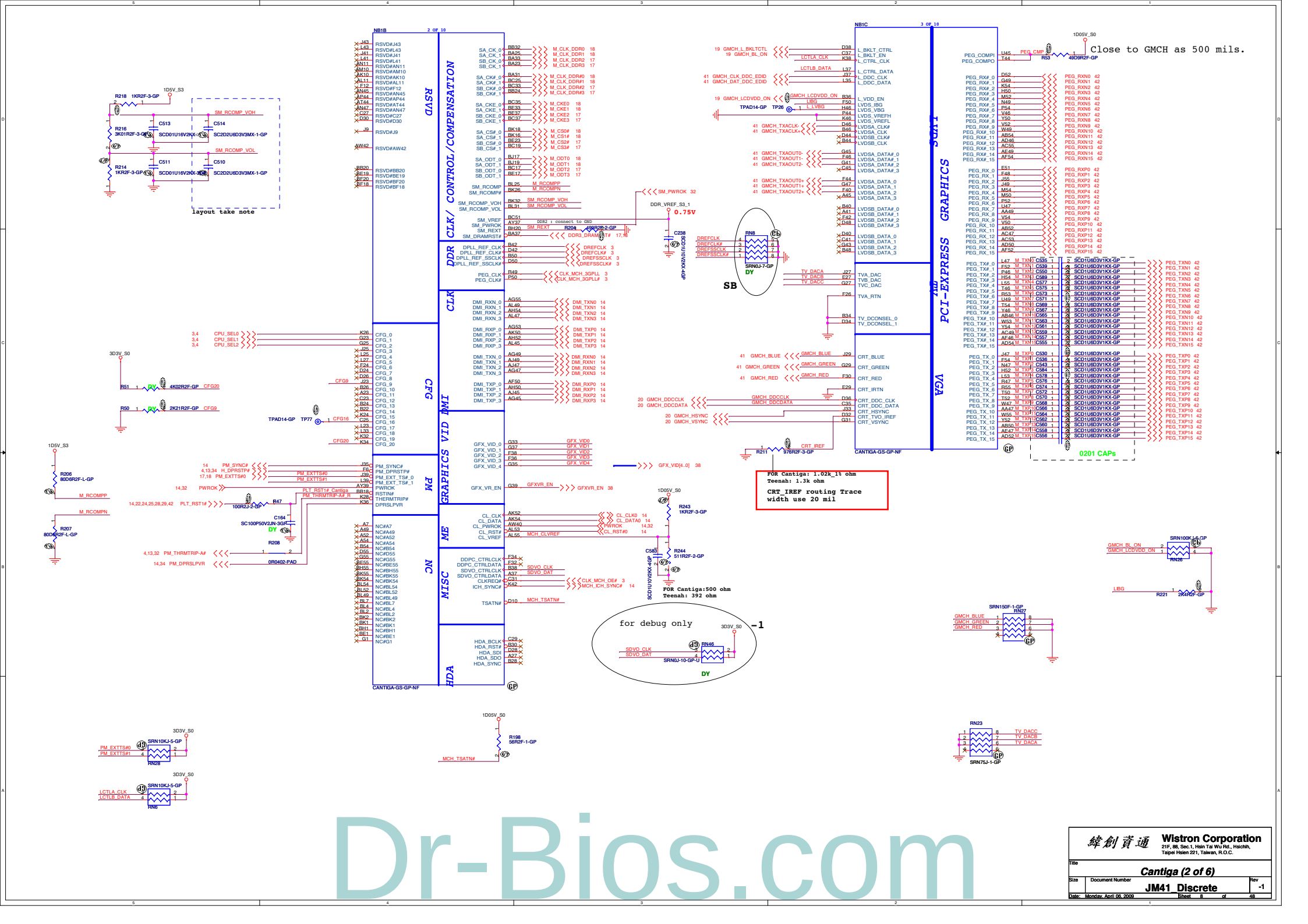
NB1B
2 OF 10
RSVD
CLK/ CONTROL/COMPENSATION
DDR
CLK
CFG
DMI
GRAPHICS VID
PM
ME
NC
MISC
HDA
CANTIGA-GS-GP-NF
NB1C
3 OF 10
LVDS
PCI-EXPRESS
GRAPHICS
DMI
VGA
CANTIGA-GS-GP-NF
Close to GMCH as 500 mils.
layout take note
SB
DY
0201 CAPs
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
FOR Cantiga:500 ohm
Teenah: 392 ohm
for debug only
-1
0.75V
Dr-Bios.com
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Cantiga (2 of 6)
JM41_Discrete
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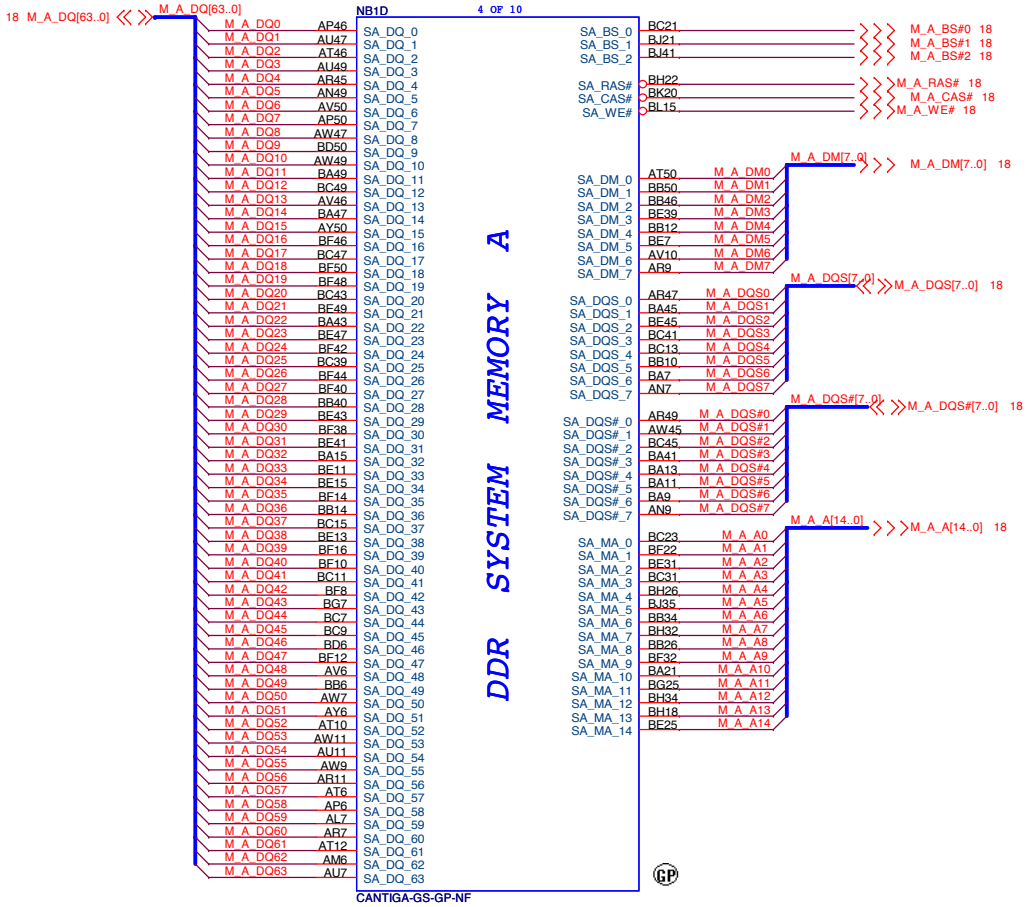

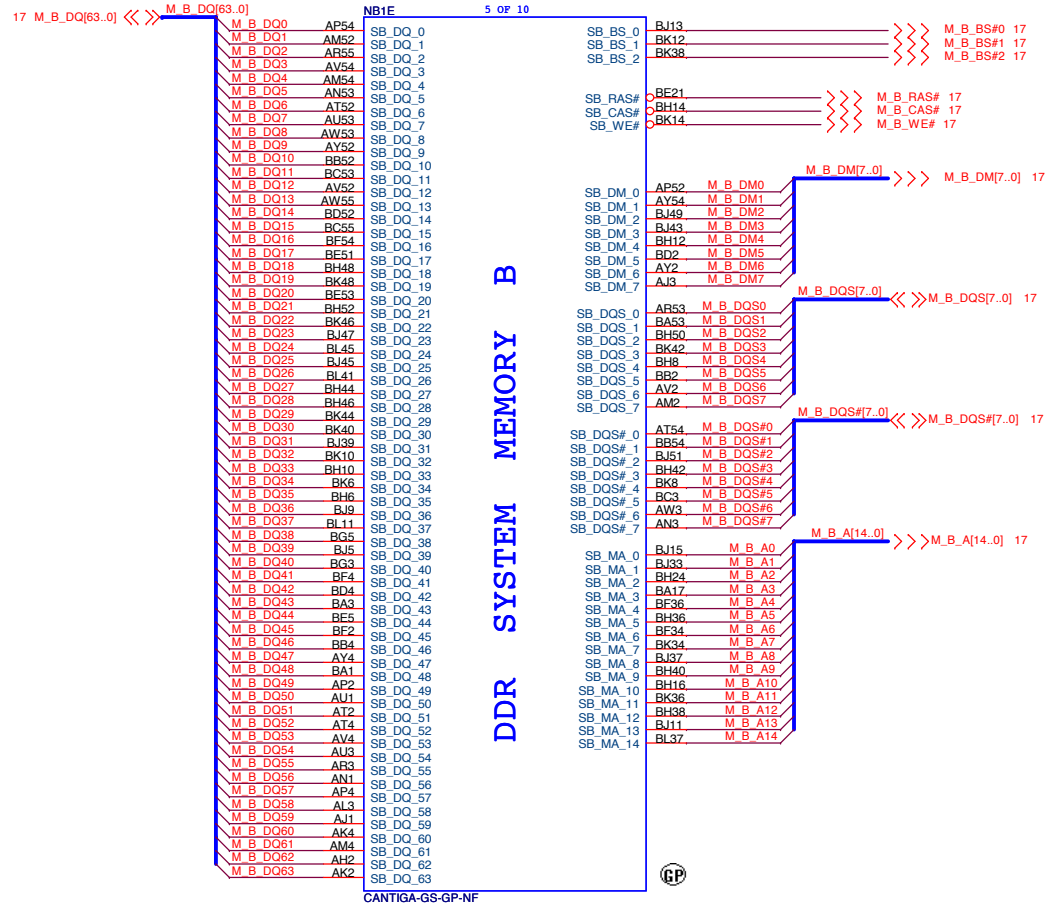

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Title: Cantiga (3 of 6)

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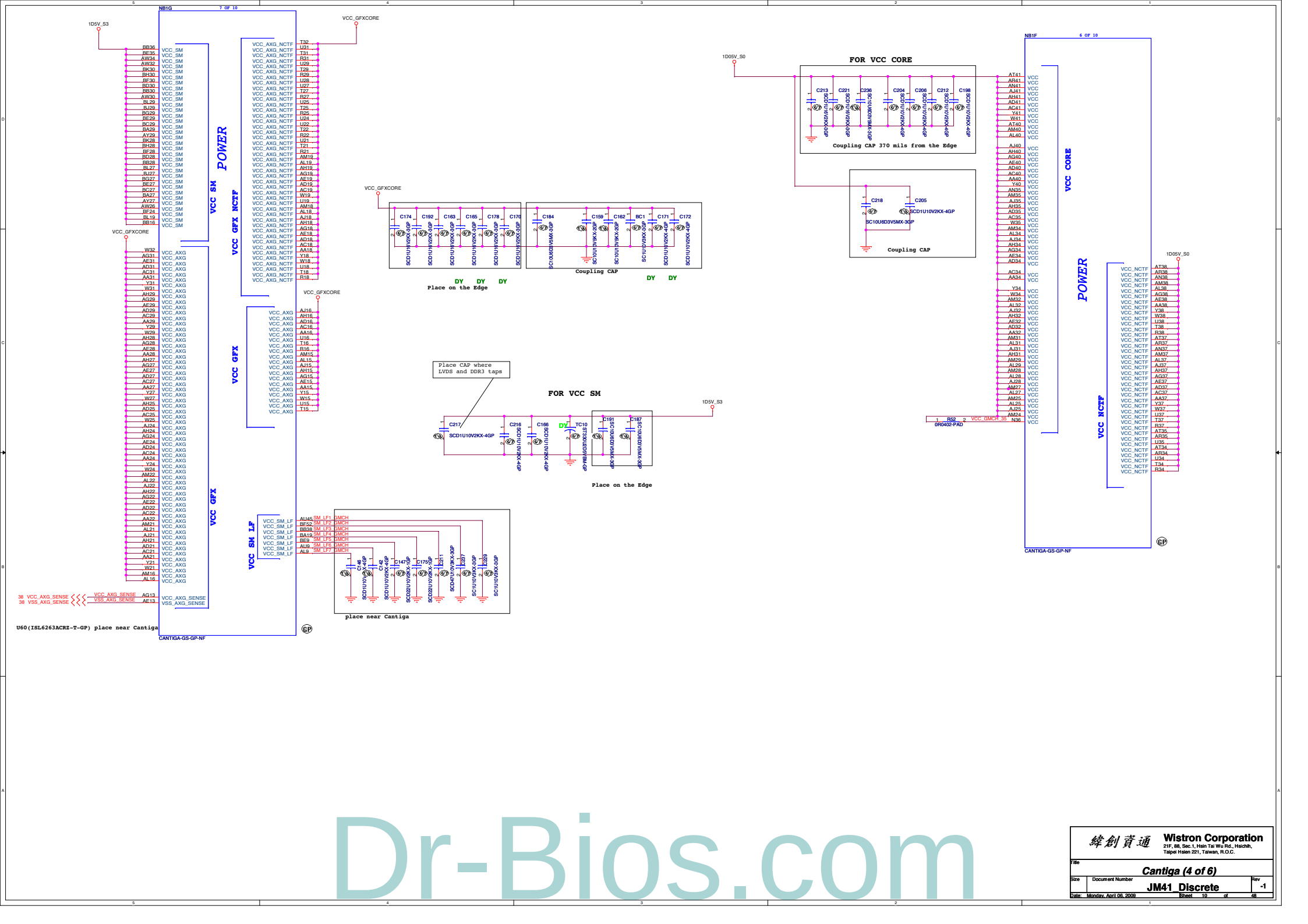

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Title: Cantiga (4 of 6)	
Size:	Document Number: JM41_Discrete
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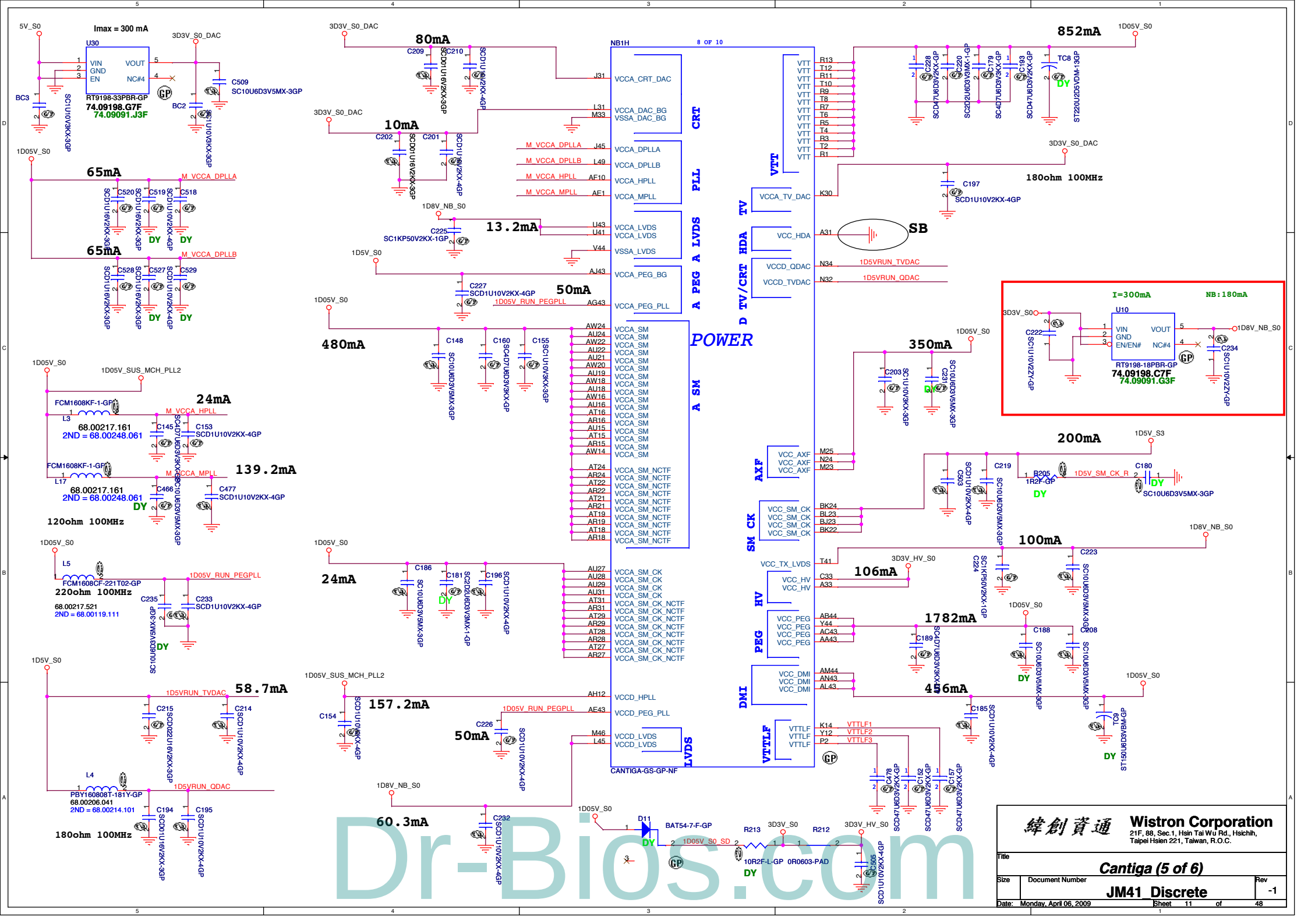

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Title	Cantiga (5 of 6)
Size	Document Number: JM41_Discrete
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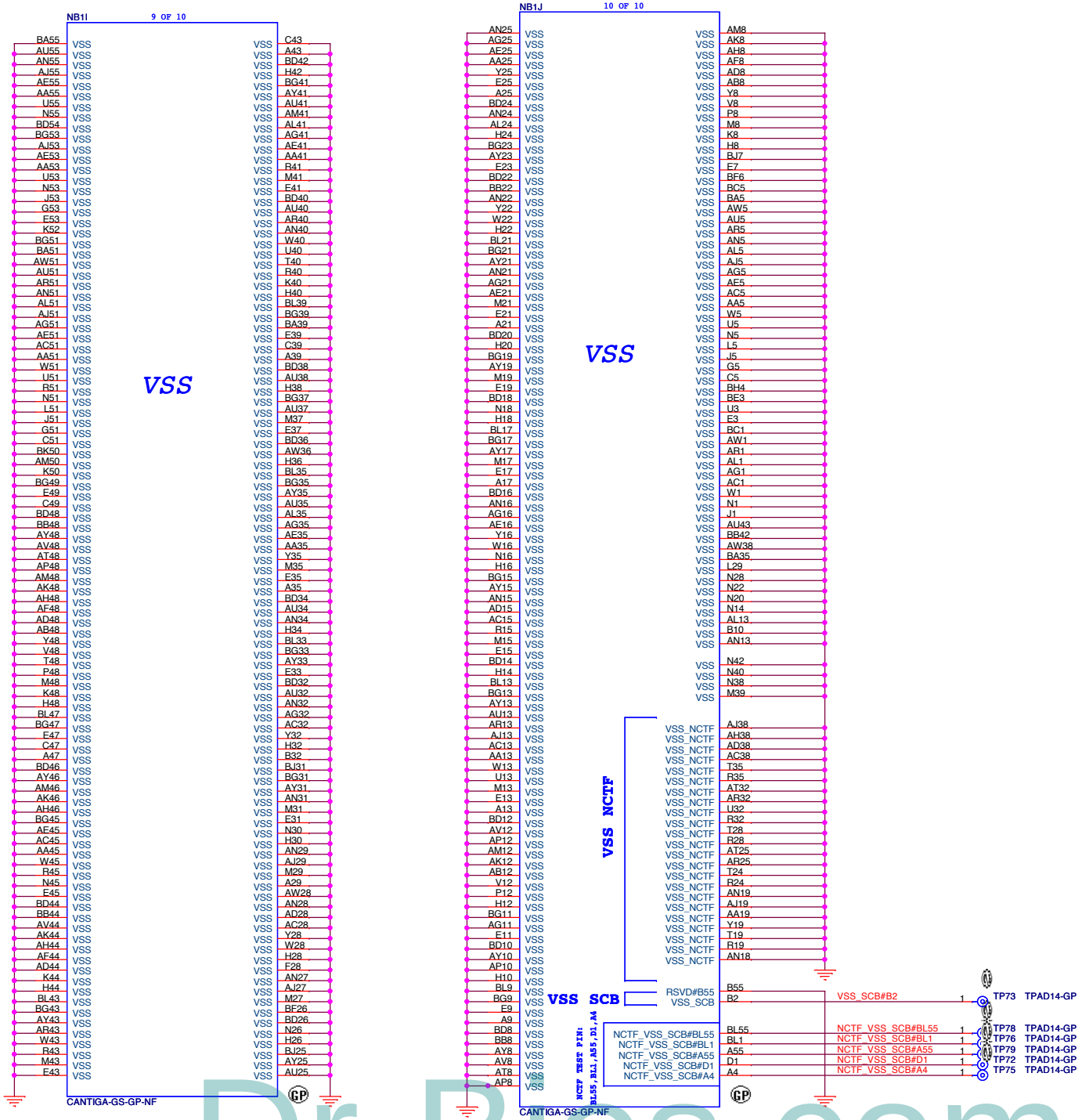

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Title: Cantiga (6 of 6)

Size | Document Number: JM41_Discrete | Rev: -1

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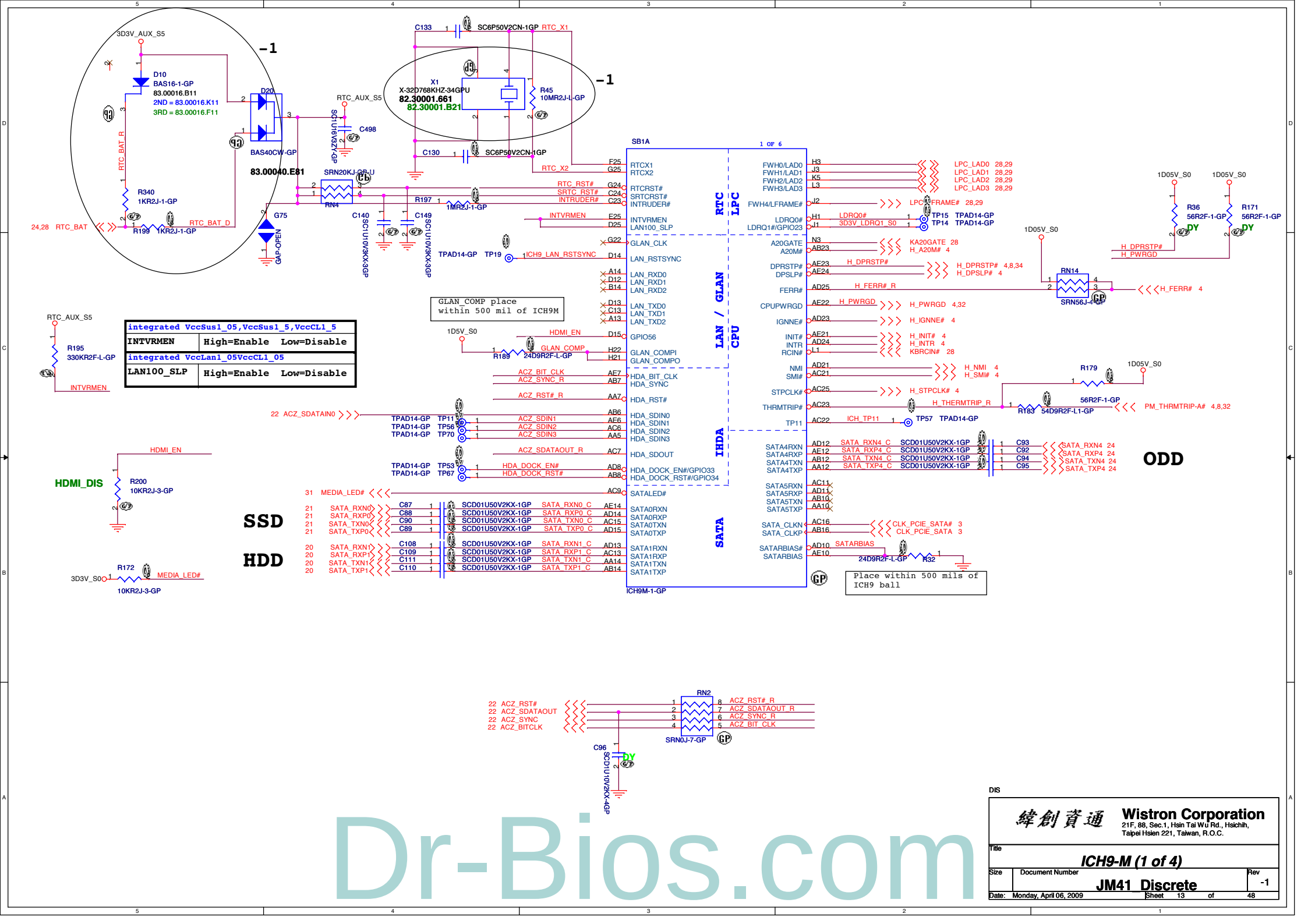
3D3V_AUX_S5
D10
BAS16-1-GP
83.00016.B11
2ND = 83.00016.K11
3RD = 83.00016.F11
D20
BAS40CW-GP
83.00040.E81
RTC_BAT_R
R340
1KR2J-1-GP
R199
1KR2J-1-GP
24,28 RTC_BAT
RTC_BAT_D
G75
GAP-OPEN
RTC_AUX_S5
C498
SCD1U16V2ZY-2GP
SRN20KJ-8B-U
RN4
C140
C149
SCD1U10V3KX-3GP
C133
SC6P50V2CN-1GP
RTC_X1
X1
X-32D768KHZ-34GPU
82.30001.661
82.30001.B21
R45
10MR2J-L-GP
C130
SC6P50V2CN-1GP
RTC_X2
R197
1MR2J-1-GP
TPAD14-GP TP19
ICH9_LAN_RSTSYNC
INTVRMEN
RTC_RST#
SRTC_RST#
INTRUDER#
SB1A
1 OF 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
RTC
LPC
GLAN
LAN / CPU
HDA
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP11
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
LPC_LAD0 28,29
LPC_LAD1 28,29
LPC_LAD2 28,29
LPC_LAD3 28,29
LPC_FRAME# 28,29
TP15 TPAD14-GP
TP14 TPAD14-GP
KA20GATE 28
H_A20M# 4
H_DPRSTP# 4,8,34
H_DPSLP# 4
H_FERR# 4
H_PWRGD 4,32
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRCIN# 28
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R
TP57 TPAD14-GP
SATA_RXN4 24
SATA_RXP4 24
SATA_TXN4 24
SATA_TXP4 24
CLK_PCIE_SATA# 3
CLK_PCIE_SATA 3
SATARBIAS
24D9R2F-L-GP
R32
ICH9M-1-GP
Place within 500 mils of ICH9 ball
GLAN_COMP place within 500 mil of ICH9M
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
RTC_AUX_S5
R195
330KR2F-L-GP
INTVRMEN
1D5V_S0
HDMI_EN
R189
24D9R2F-L-GP
GLAN_COMP
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
22 ACZ_SDATAIN0
TPAD14-GP TP11
TPAD14-GP TP56
TPAD14-GP TP70
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDATAOUT_R
TPAD14-GP TP53
TPAD14-GP TP67
HDA_DOCK_EN#
HDA_DOCK_RST#
HDMI_EN
HDMI_DIS
R200
10KR2J-3-GP
R172
10KR2J-3-GP
3D3V_S0
MEDIA_LED#
31 MEDIA_LED#
SSD
HDD
21 SATA_RXN0
21 SATA_RXP0
21 SATA_TXN0
21 SATA_TXP0
20 SATA_RXN1
20 SATA_RXP1
20 SATA_TXN1
20 SATA_TXP1
C87
C88
C90
C89
C108
C109
C111
C110
SCD01U50V2KX-1GP
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1_C
SATA_TXP1_C
AE14
AD14
AC15
AD15
AD13
AC13
AA14
AB14
RN14
SRN56J-4-GP
H_FERR# 4
R36
56R2F-1-GP
DY
R171
56R2F-1-GP
DY
H_DPRSTP#
H_PWRGD
R179
56R2F-1-GP
R183
54D9R2F-L1-GP
PM_THRMTRIP-A# 4,8,32
ODD
C93
C92
C94
C95
RN2
SRN0J-7-GP
22 ACZ_RST#
22 ACZ_SDATAOUT
22 ACZ_SYNC
22 ACZ_BITCLK
ACZ_RST#_R
ACZ_SDATAOUT_R
ACZ_SYNC_R
ACZ_BIT_CLK
C96
SCD1U10V2KX-4GP
DIS
緯創資通
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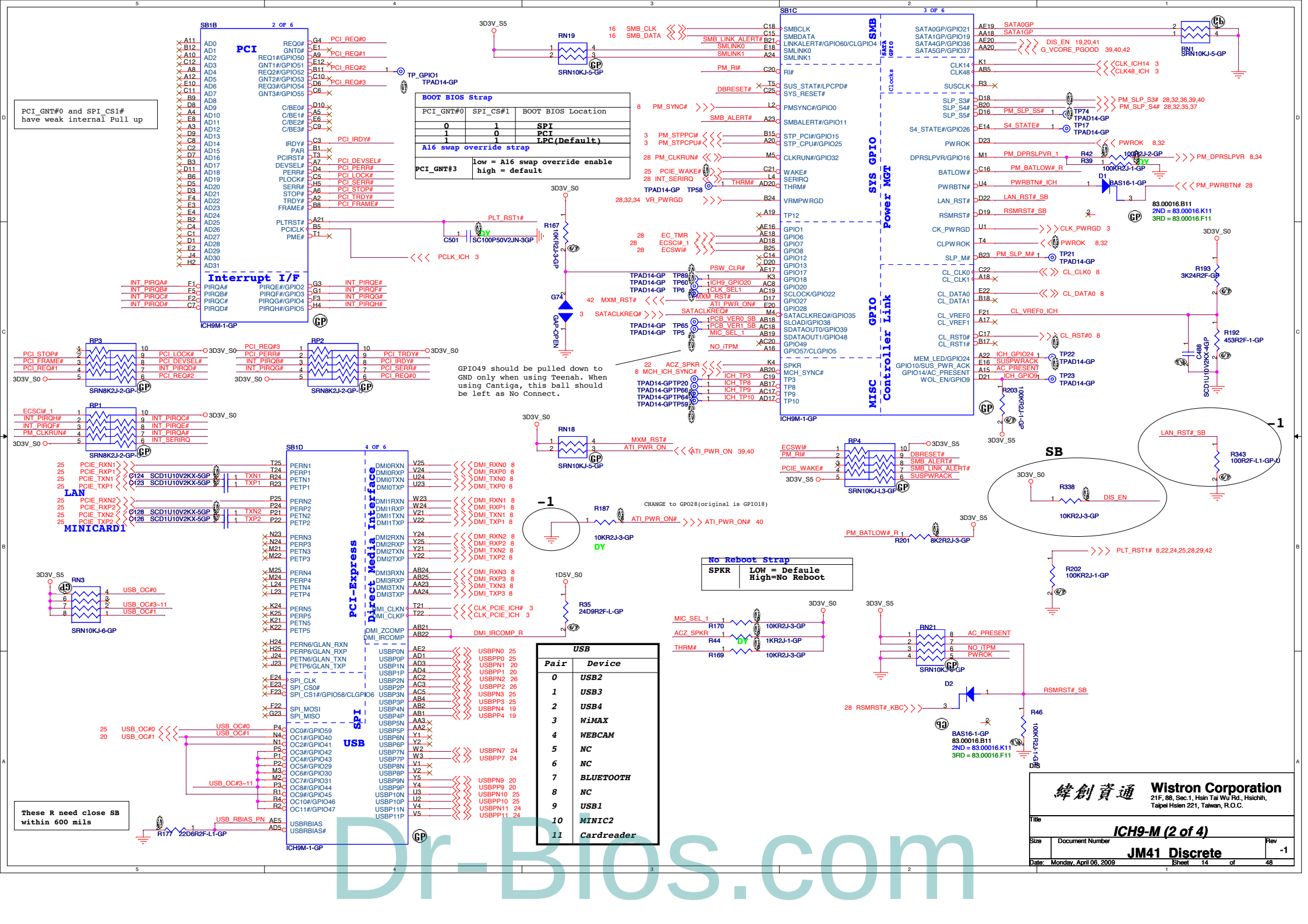
Title
ICH9-M (1 of 4)
Size
Document Number
JM41_Discrete
Rev
-1
Date: Monday, April 06, 2009
Sheet 13 of 48


PCI_GNT#0 and SPI_CS1# have weak internal Pull up
BOOT BIOS Strap
PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC(Default)
A16 swap override strap
PCI_GNT#3 | low = A16 swap override enable high = default
GPIO049 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
No Reboot Strap
SPKR | LOW = Defaule High=No Reboot
USB
Pair | Device
0 | USB2
1 | USB3
2 | USB4
3 | WiMAX
4 | WEBCAM
5 | NC
6 | NC
7 | BLUETOOTH
8 | NC
9 | USB1
10 | MINIC2
11 | Cardreader
These R need close SB within 600 mils
SB
LAN
MINICARD1
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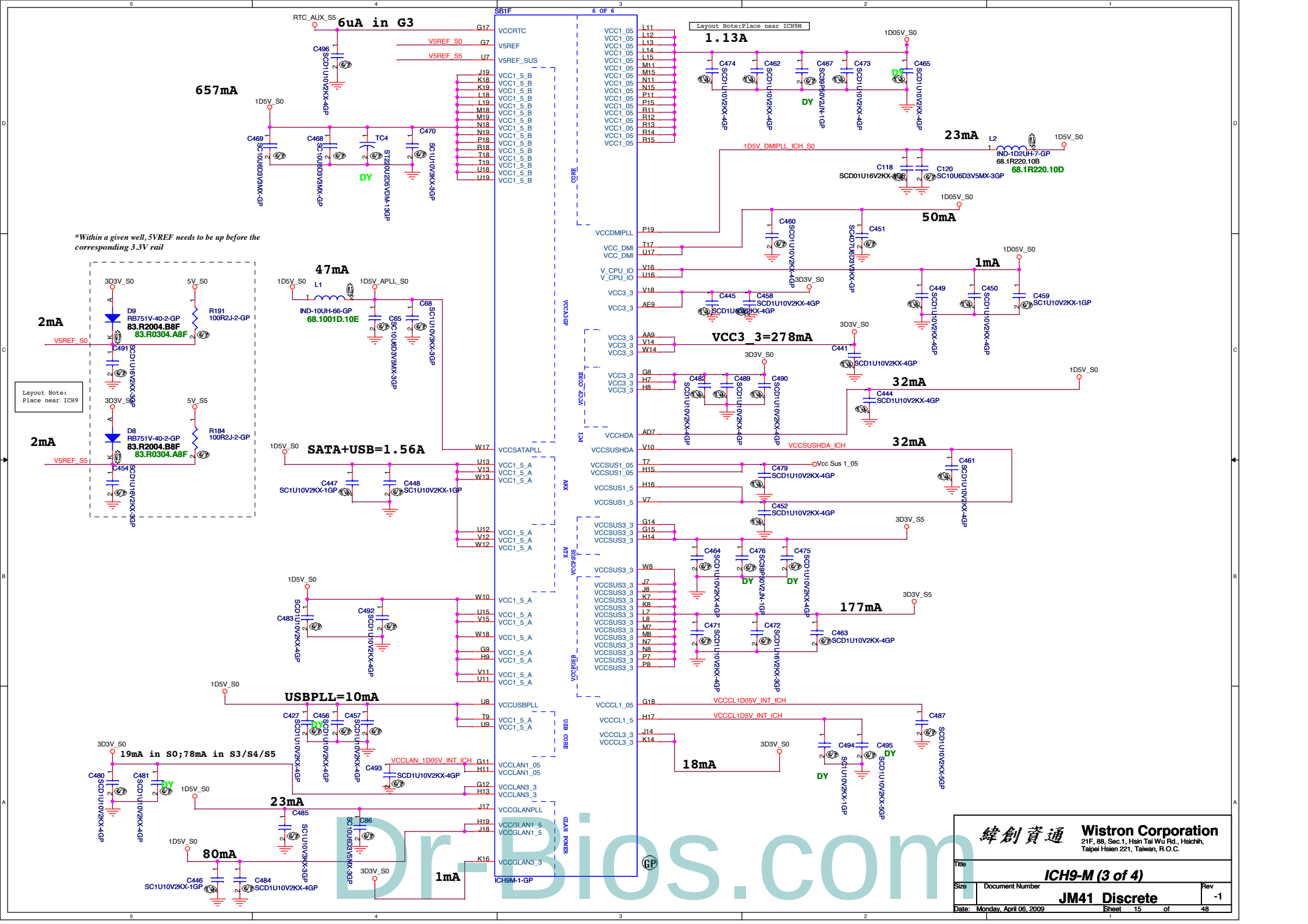
ICH9-M (2 of 4)
JM41 Discrete
Monday, April 06, 2009
Sheet 14 of 48


6uA in G3
657mA
1.13A
23mA
50mA
1mA
2mA
2mA
47mA
SATA+USB=1.56A
VCC3_3=278mA
32mA
32mA
177mA
USBPLL=10mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH9
Layout Note:Place near ICH9M
SB1F
6 OF 6
ICH9M-1-GP
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ICH9-M (3 of 4)
JM41 Discrete
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Date: Monday, April 06, 2009
Sheet 15 of 48
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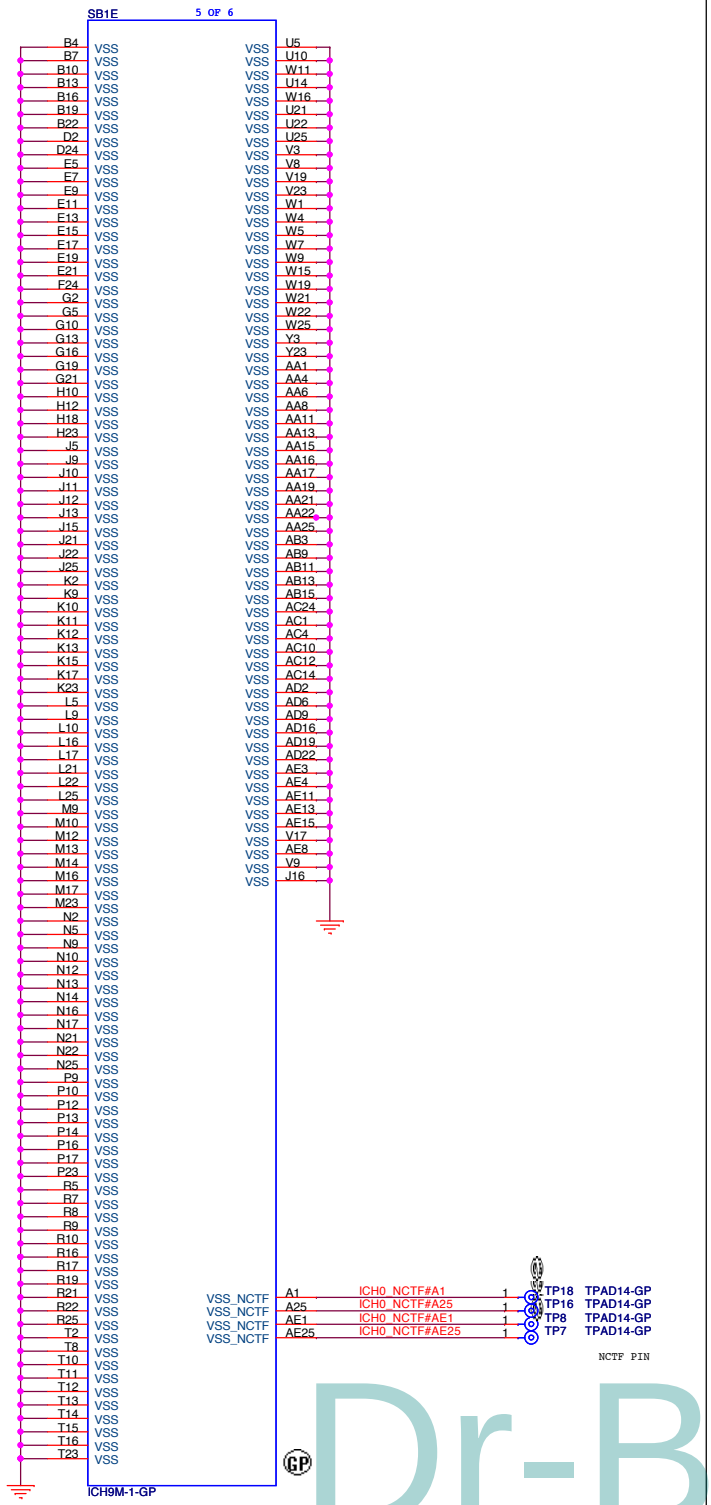

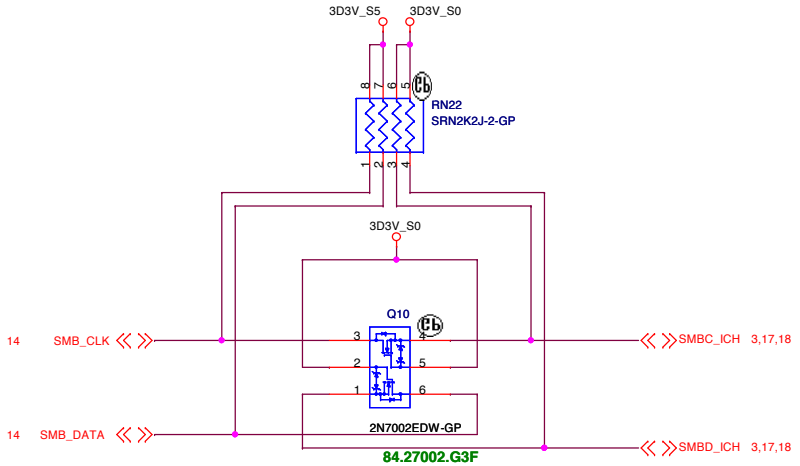

SMBUS

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Title: ***ICH9-M (4 of 4)***

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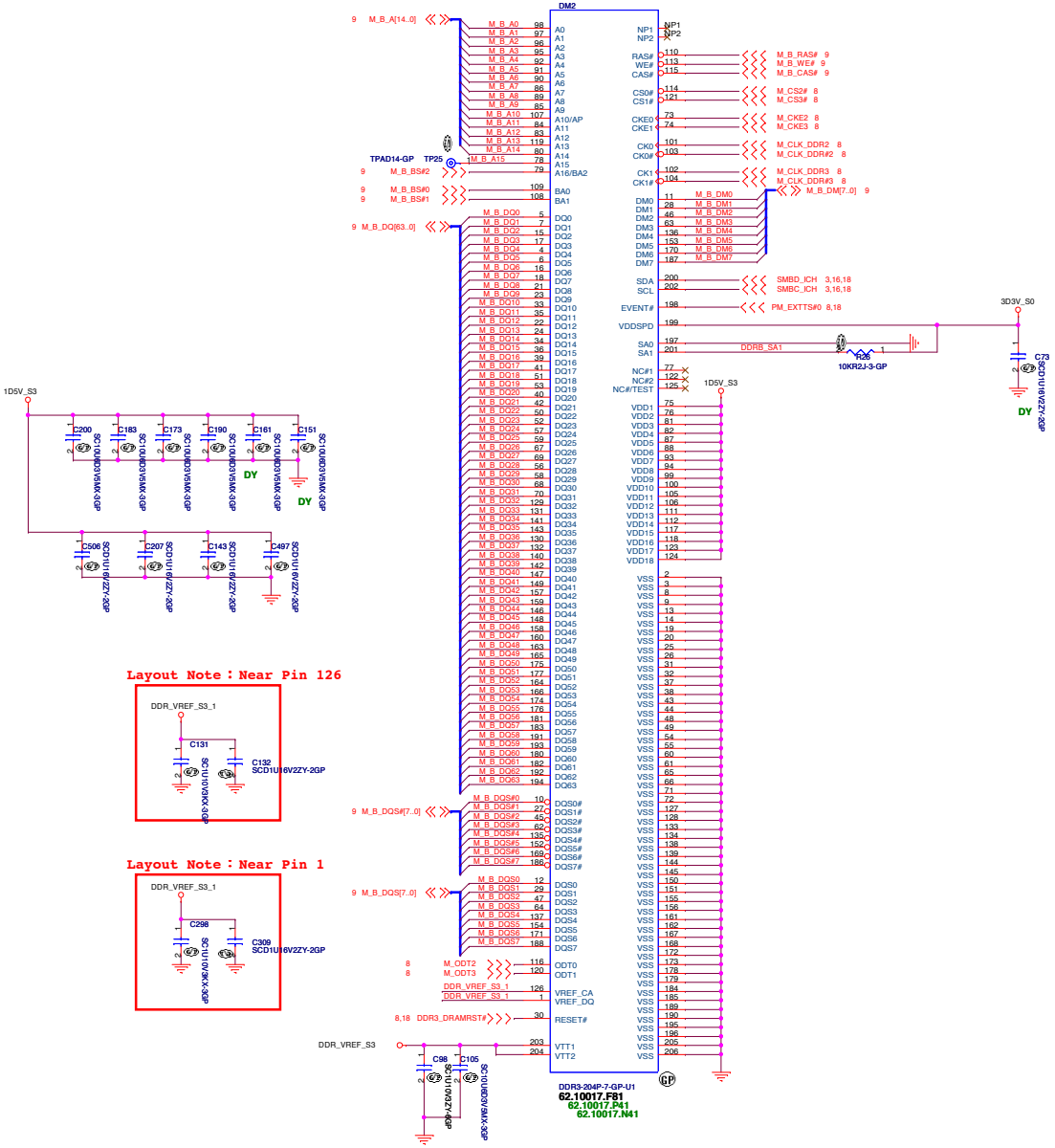
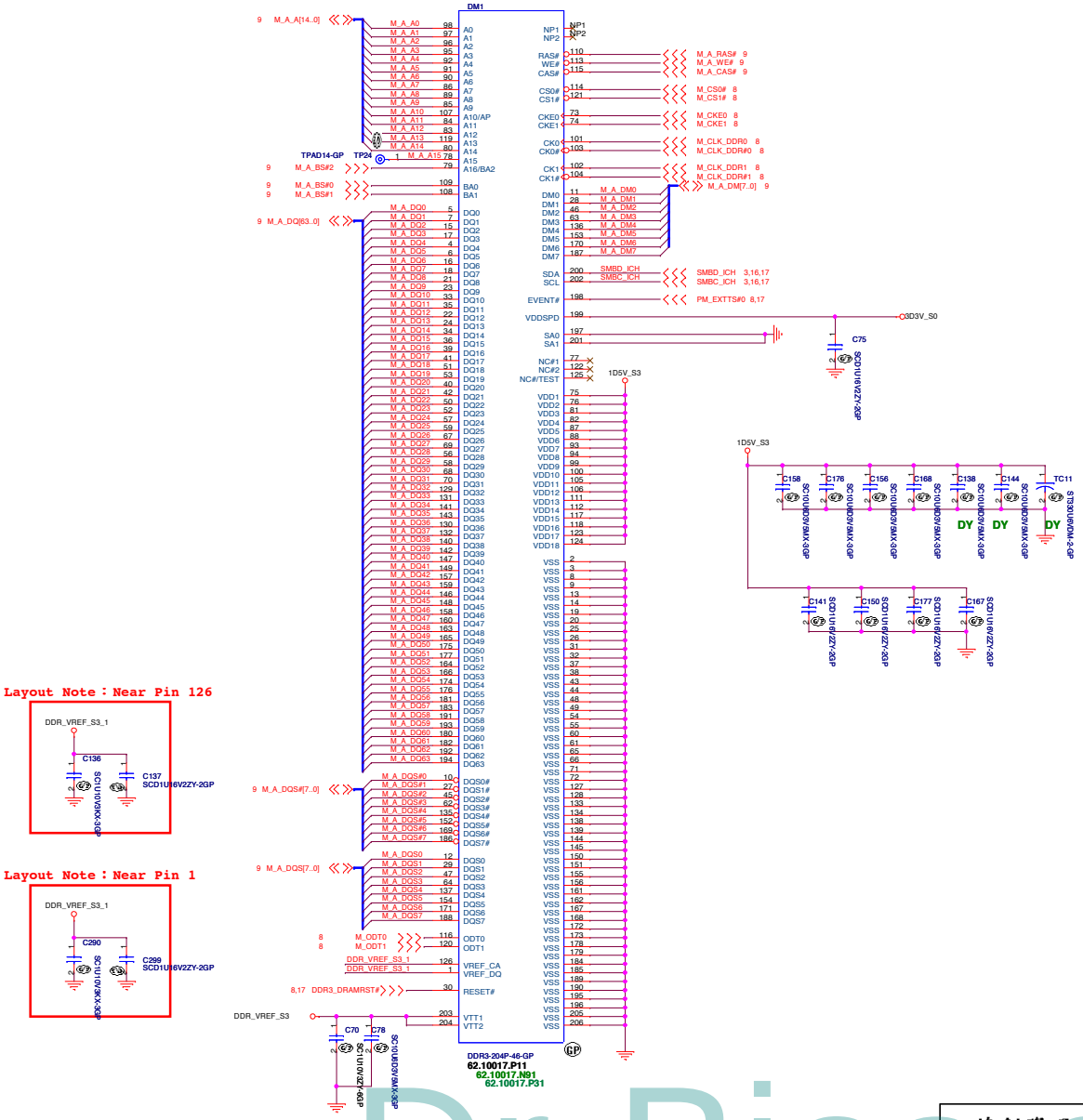
DDR3 SOCKET_1



緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR3 Socket1		
Size	Document Number: JM41 Discrete	Rev: -1
Date: Monday, April 06, 2009	Sheet 17 of 48	

DDR3 SOCKET_2



Layout Note : Near Pin 126

Layout Note : Near Pin 1

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Title	DDR3 Socket2	
Size	Document Number	Rev
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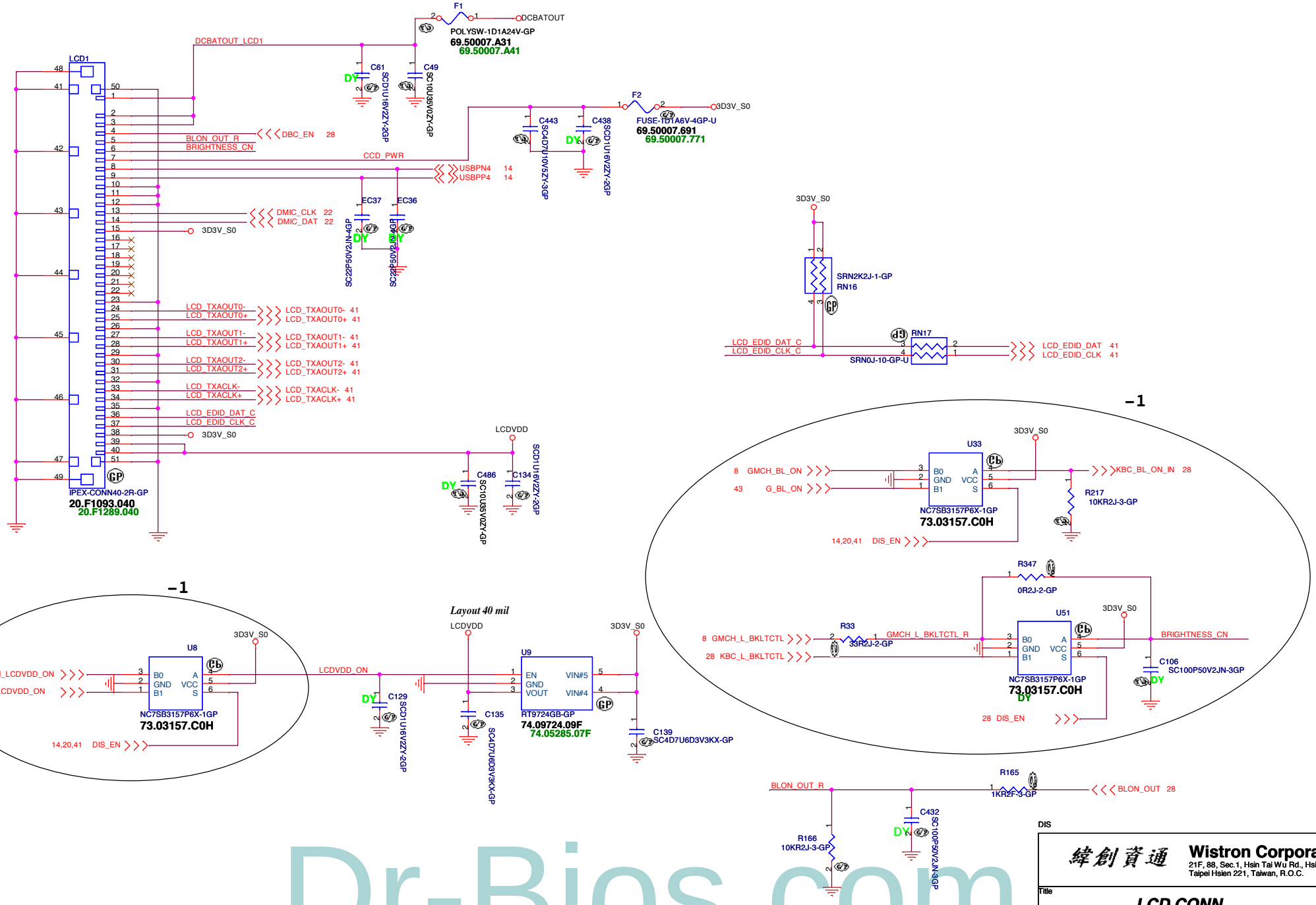
LCD/CCD CONN

Internal MIC



DIS

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Title	**LCD CONN**
Size	Document Number: **JM41_Discrete** — Rev: -1
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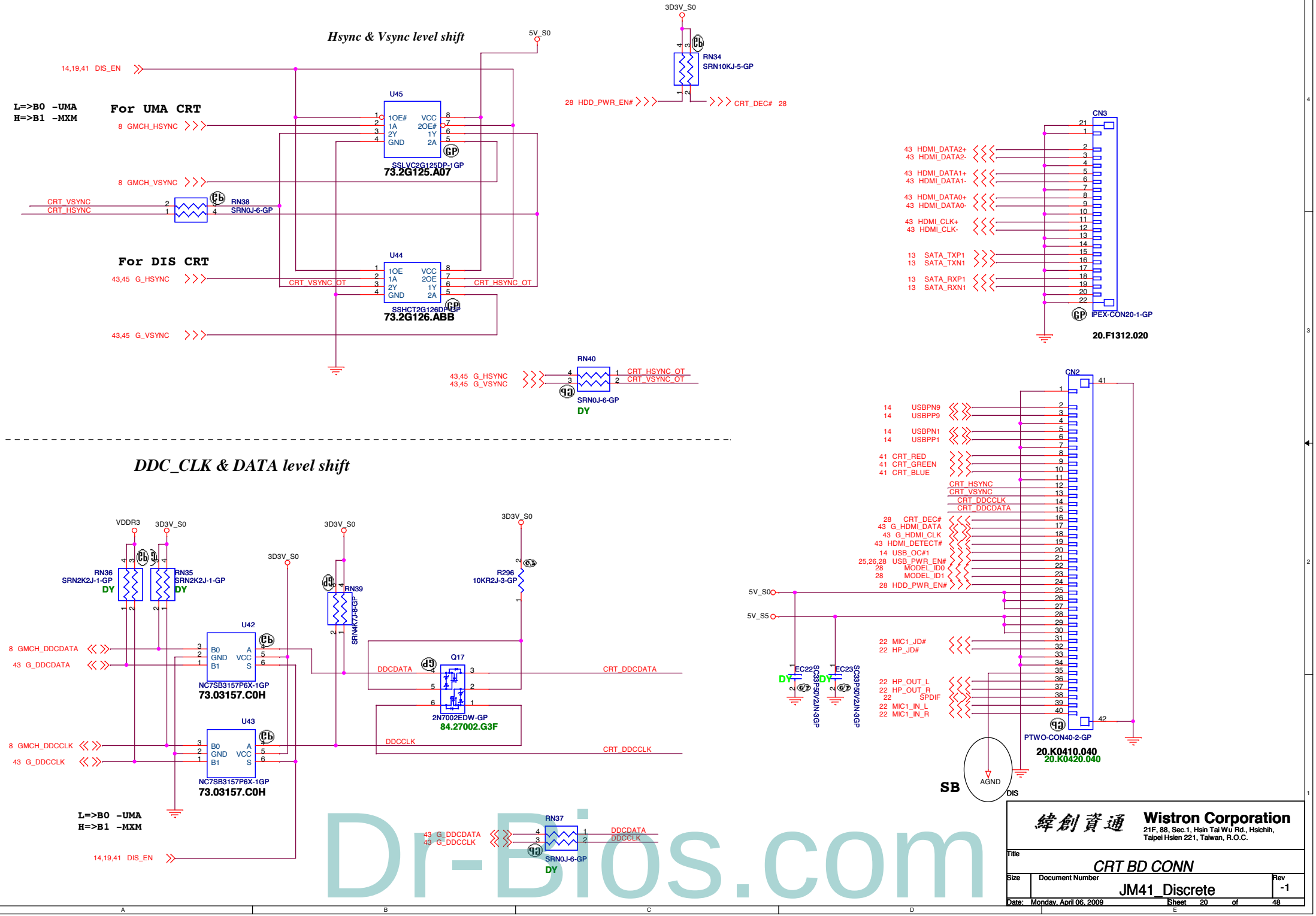

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT BD CONN

Size | Document Number: JM41_Discrete | Rev: -1

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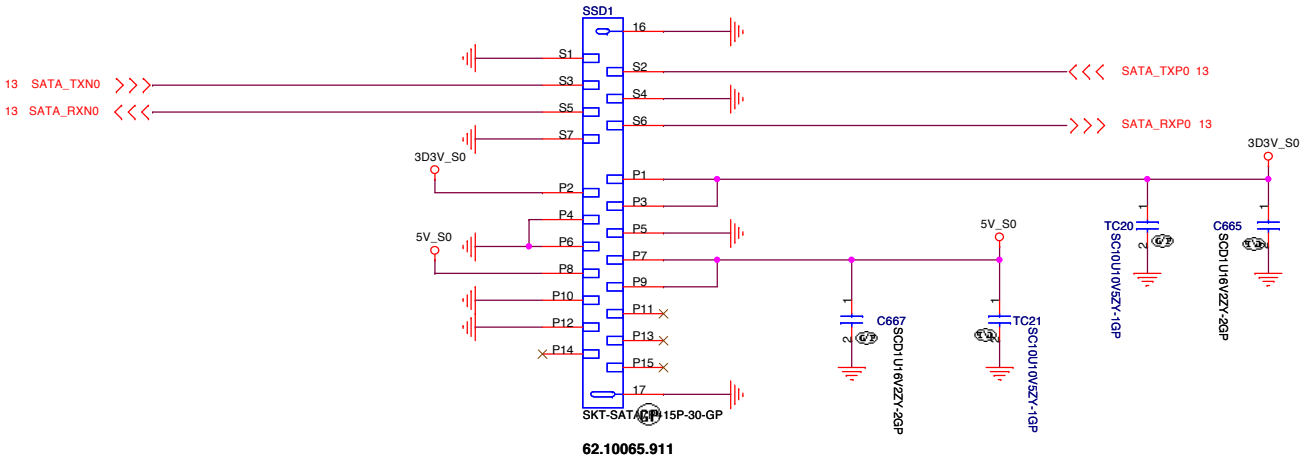
SSD SATA Connector



DIS

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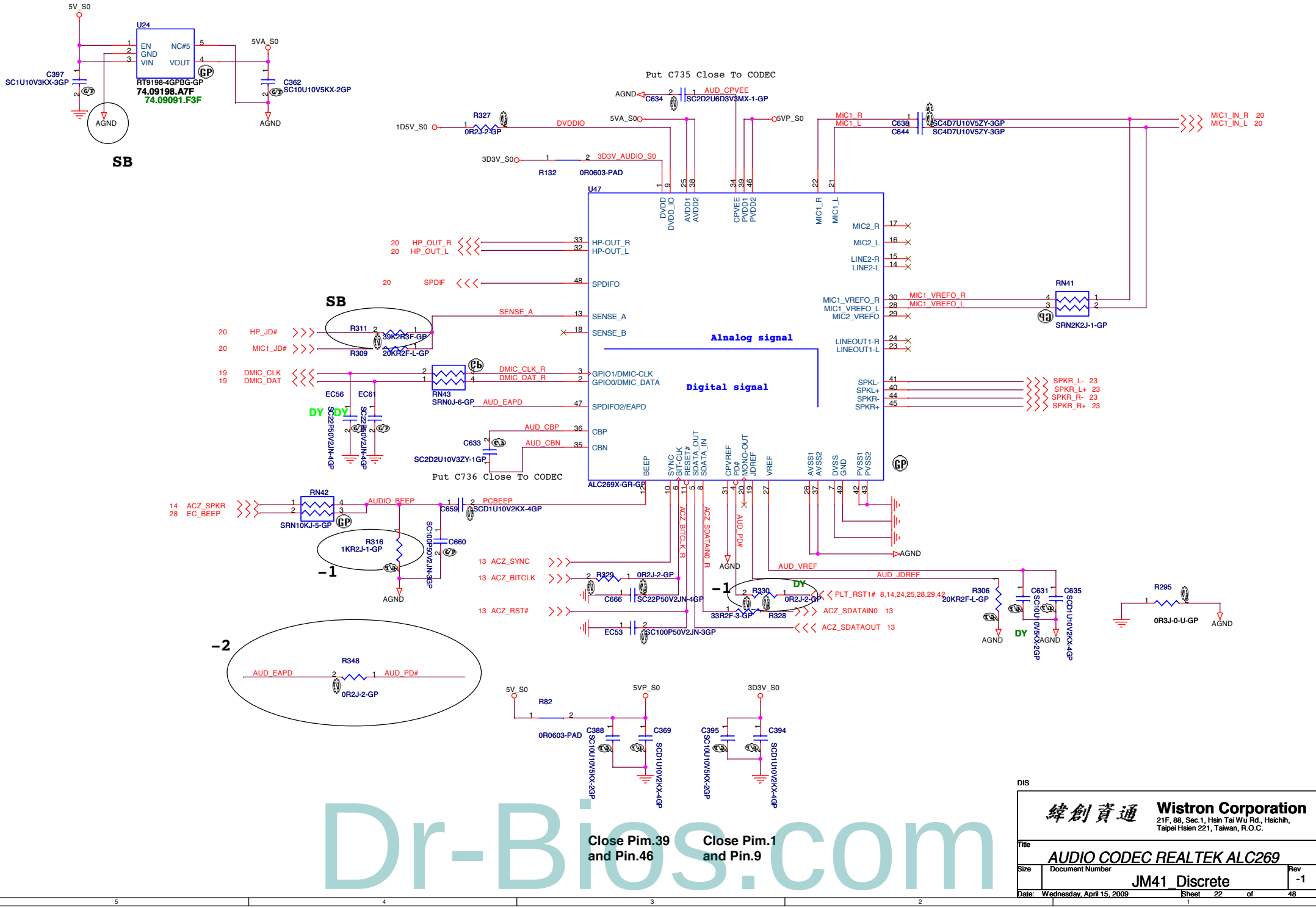
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD CONN***

Size	Document Number	Rev
	JM41 Discrete	-1

Date: Monday, April 06, 2009 Sheet 21 of 48



DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC REALTEK ALC269

Size	Document Number	Rev
	JM41_Discrete	-1

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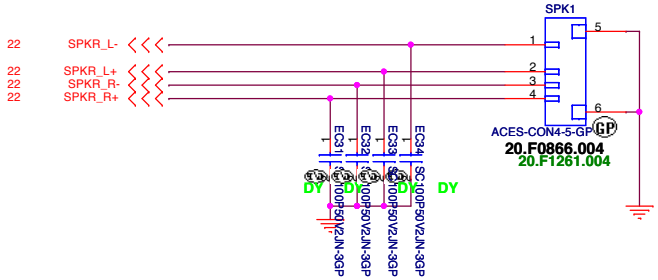
Internal Speaker



DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO JACK*

Size | Document Number: JM41_Discrete | Rev: -1

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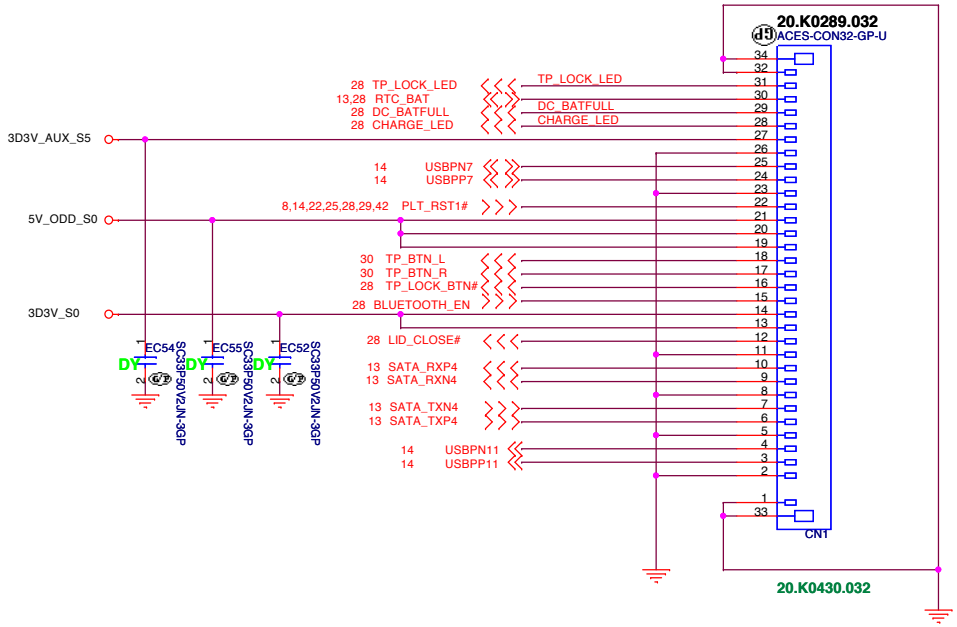

DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *CARDREADER BD CONN*

Size	Document Number	Rev
	JM41_Discrete	-1

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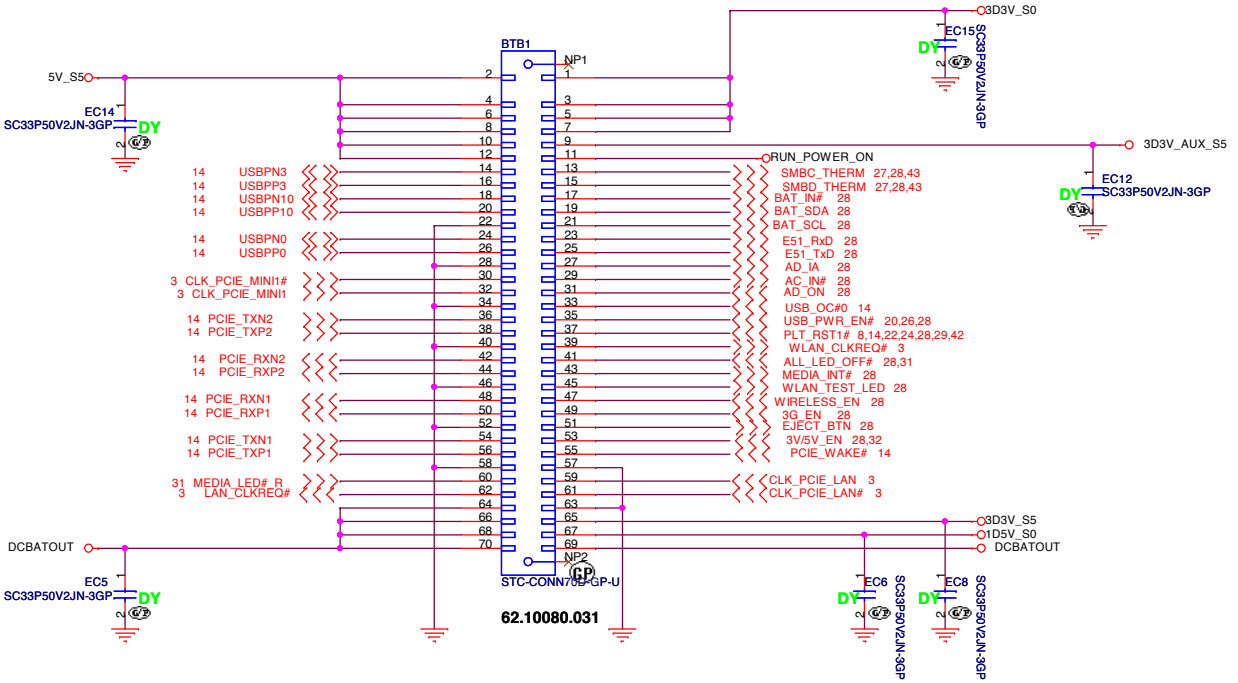

DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINI BD CONN***

Size	Document Number	Rev
A3	JM41_Discrete	-1

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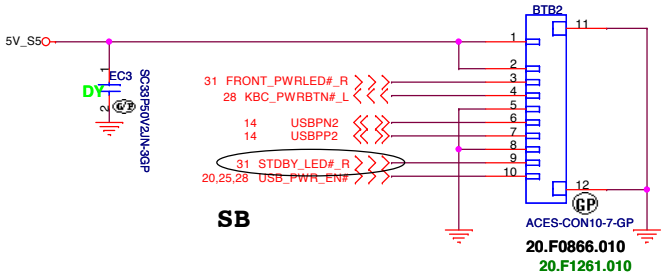

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER BUTTON CONN***

Size	Document Number	Rev
A3	JM41_Discrete	-1

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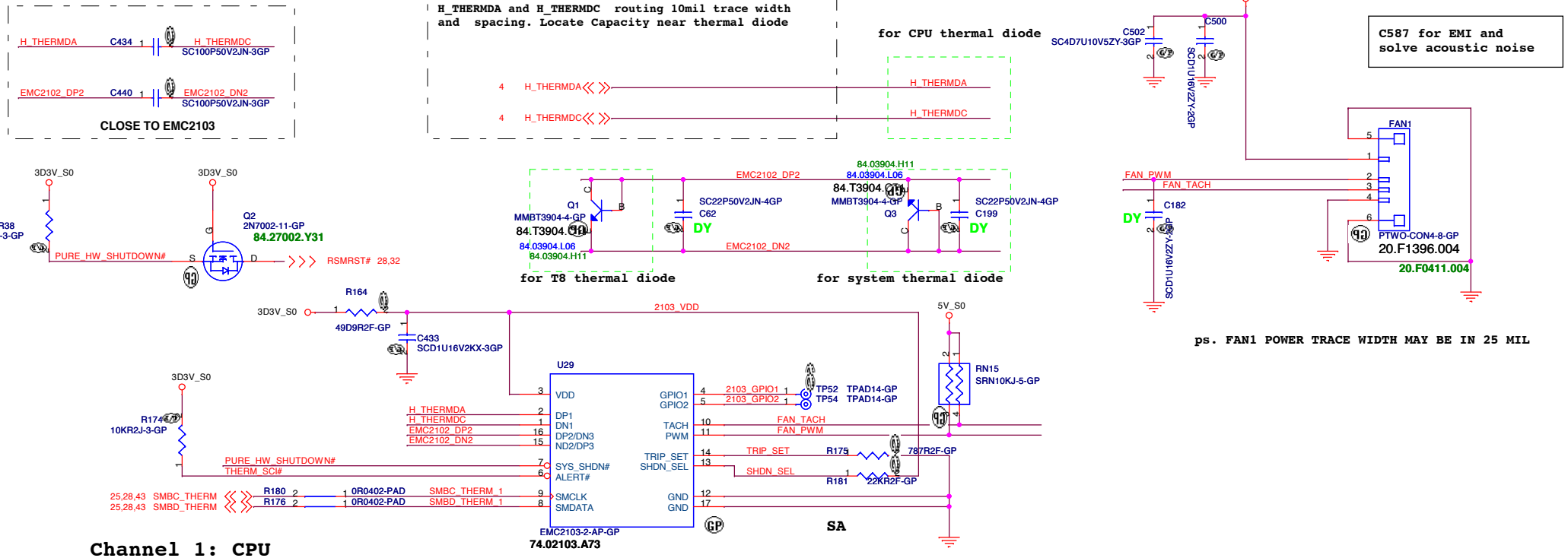

Channel 1: CPU
Channel 2: Palmrest
Channel 3: T8

SHDN_SEL

PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED,REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED,REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED

TRIP_SET

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

DIS

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Title: Thermal/Fan Controllor

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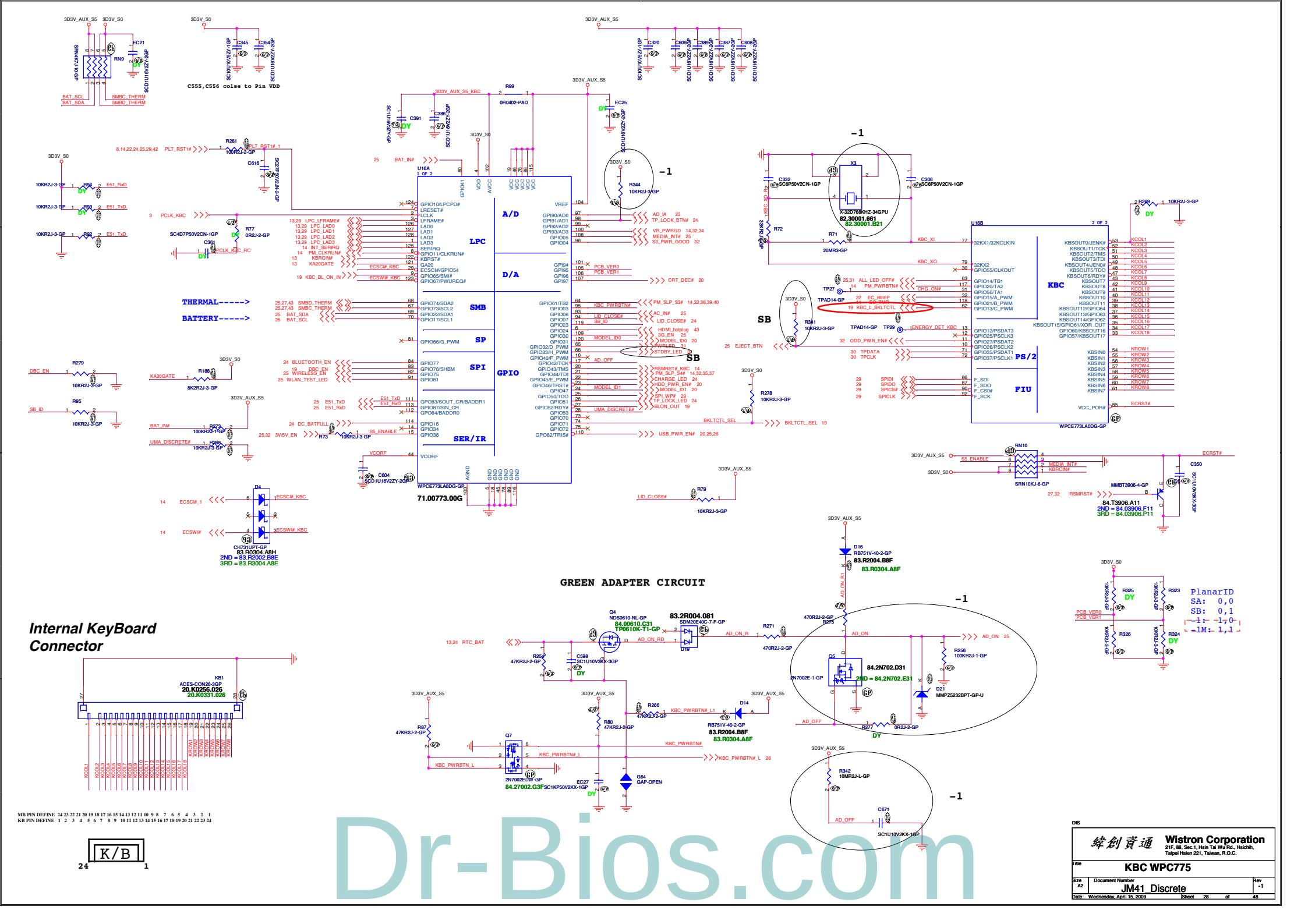
C555,C556 colse to Pin VDD
THERMAL------>
BATTERY------>
U16A
WPCE773LA0DG-GP
71.00773.00G
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
SB
KBC
PS/2
FIU
WPCE773LA0DG-GP
GREEN ADAPTER CIRCUIT
Internal KeyBoard Connector
KB1
ACES-CON26-3GP
20.K0256.026
20.K0331.026
MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
K/B
24 1
PlanarID
SA: 0,0
SB: 0,1
-1: -1,0
-1M: 1,1
Wistron Corporation
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KBC WPC775
Size A2
Document Number JM41_Discrete
Rev -1
Date: Wednesday, April 15, 2009
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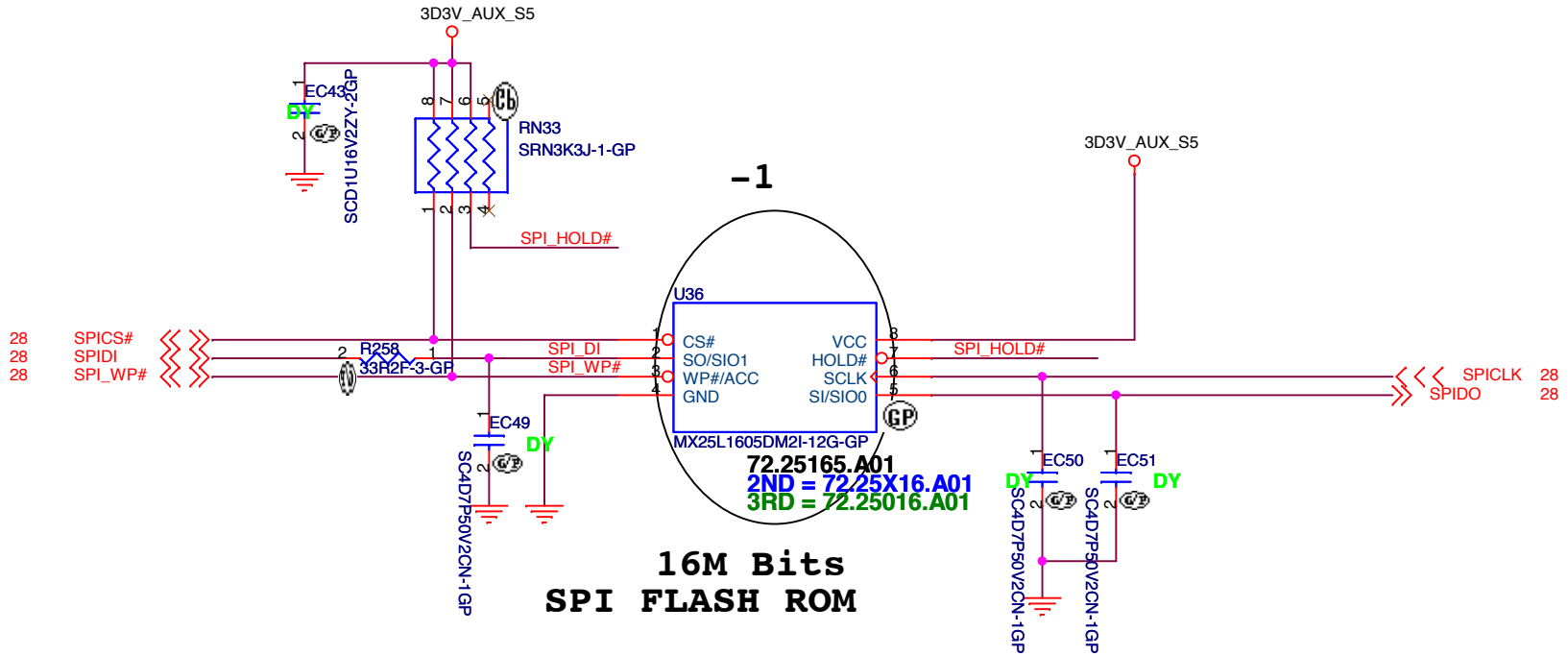
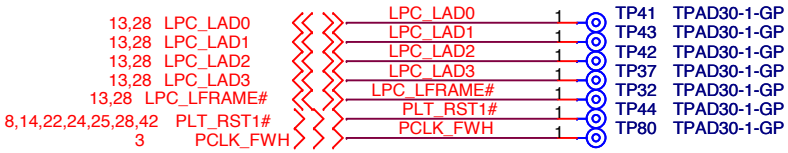
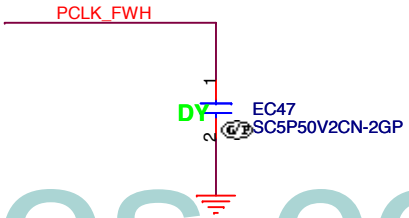


GOLDEN FINGER FOR DEBUG BOARD





DIS

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Title: BIOS

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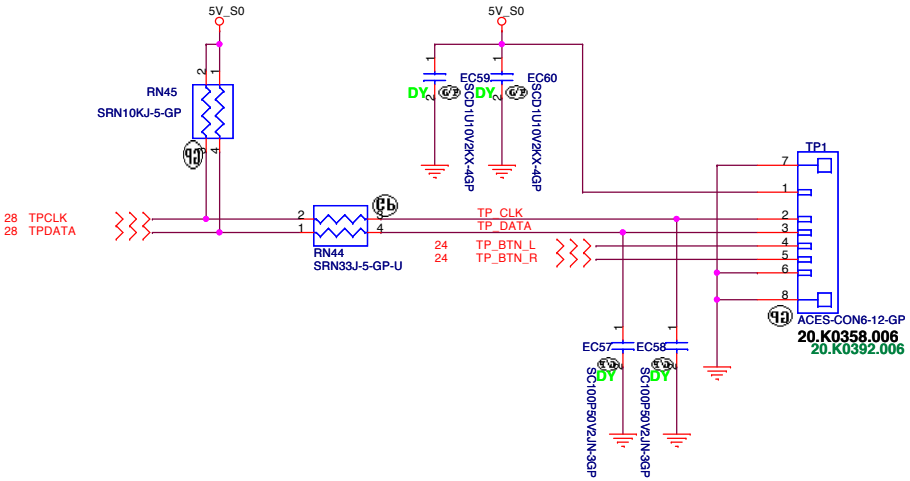
TOUCH PAD



DIS

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Title	*Touch PAD*	
Size	Document Number: JM41_Discrete	Rev: -1
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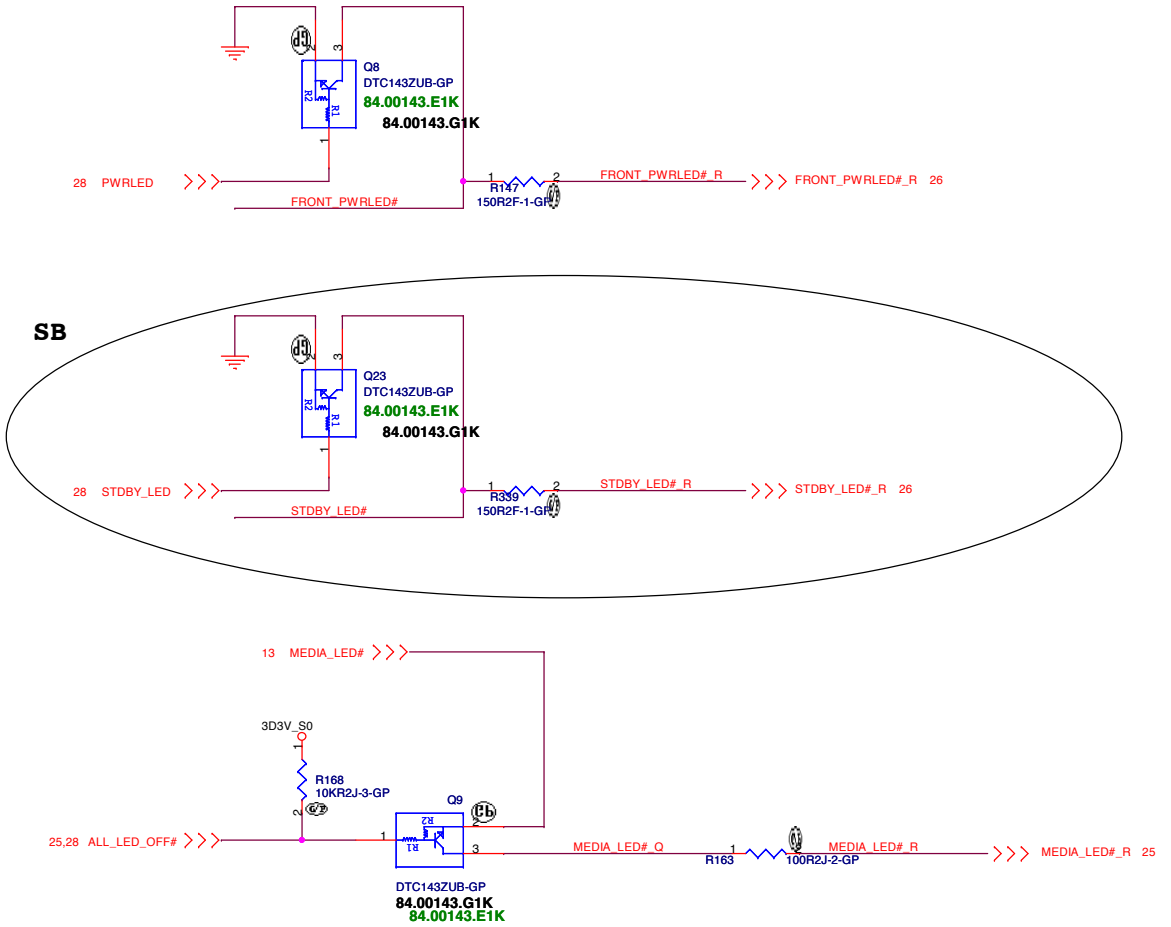

DIS

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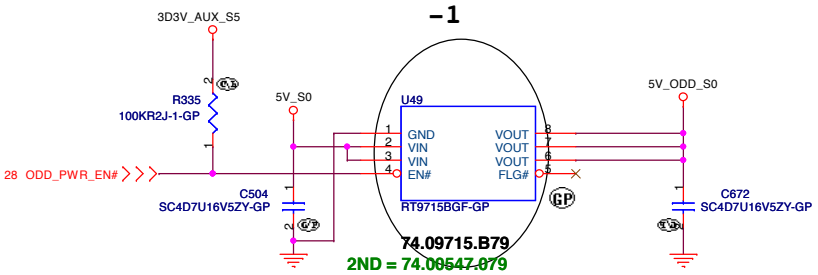
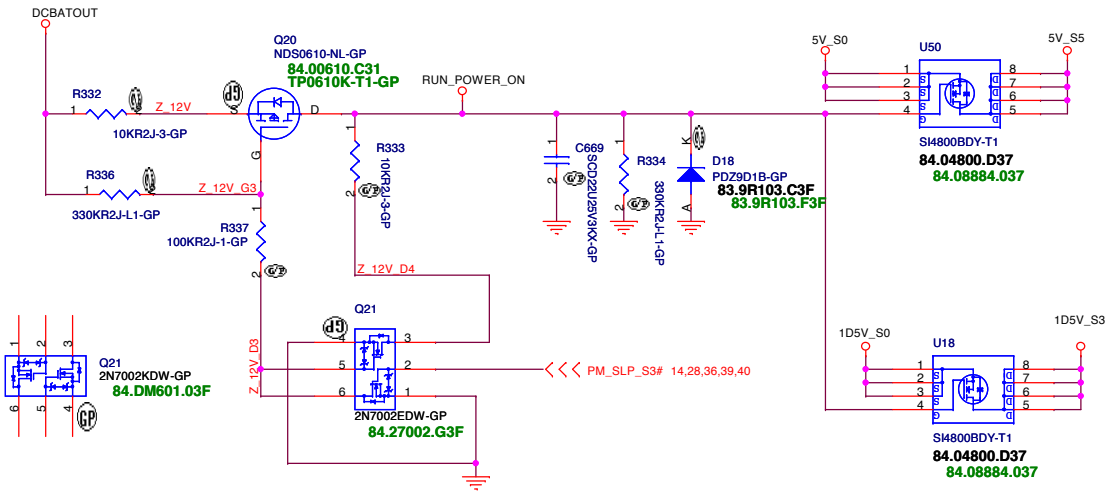
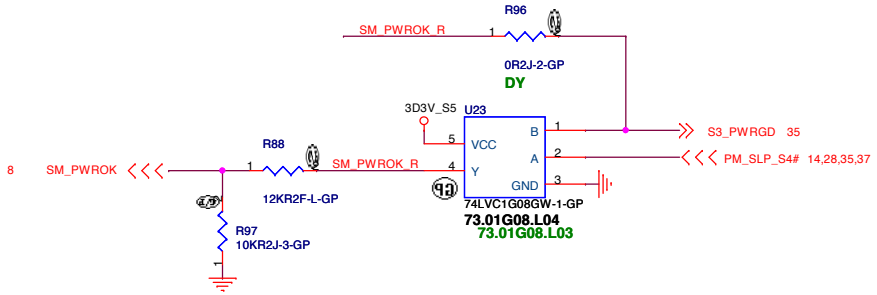
Title	**LED**	
Size	Document Number **JM41_Discrete**	Rev **-1**
Date: Monday, April 06, 2009	Sheet 31 of 48	

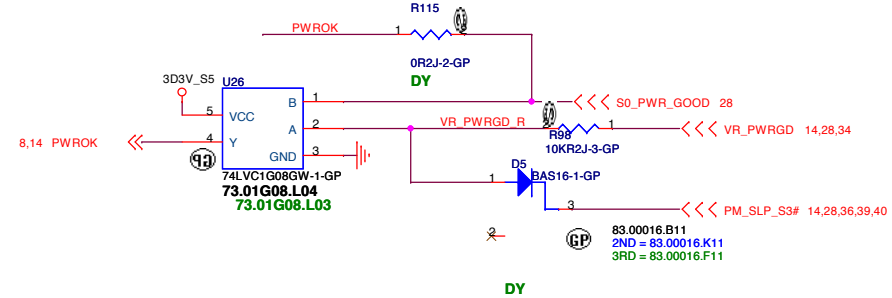
ODD Power

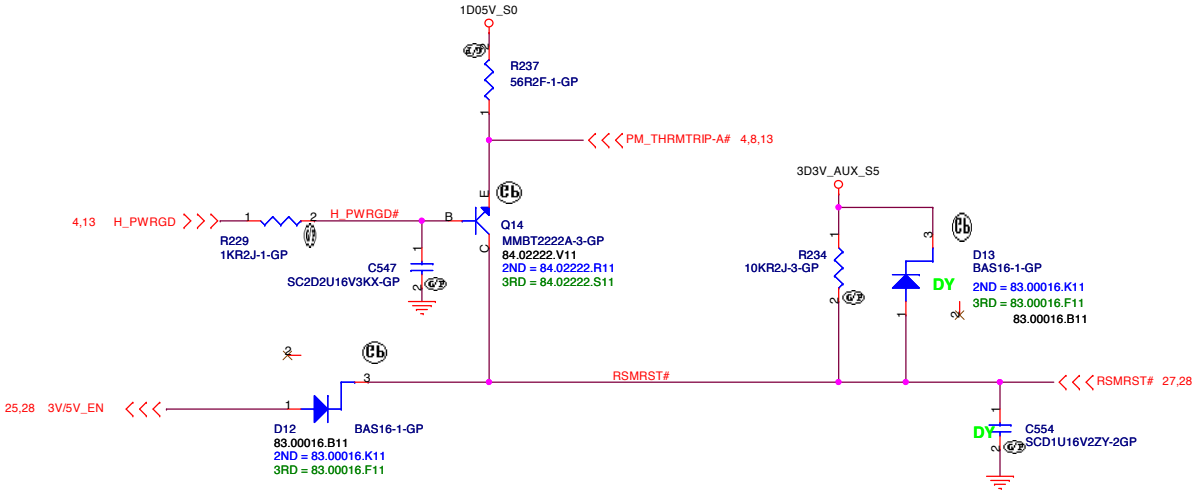


Run Power









DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN & ODD POWER

Size	Document Number	Rev
	JM41_Discrete	-1

Date: Wednesday, April 15, 2009 Sheet 32 of 48

CPU_CORE
ISL6261A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6261A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

Output Power
VCC_CORE_PWR(O)

VR_PWROK
VCC_CORE(Imax=18A)

RT8202 1D05V_S0

DCBATOUT_8202_1D05V
PM_SLP_S3#

VIN
EN
1D5V(O)
PGOOD

1D05V_S0 (10A)
CPUCORE_ON

RT8202 1D5V_S3

DCBATOUT_8202_1D5V
PM_SLP_S4#

VIN
EN
1D5V(O)
PGOOD

1D5V_S3 (11A)
CPUCORE_ON

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT_6263A

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

Output Power
VGFXCORE (O)

CPUCORE_ON
VCC_GFXCORE(7A)

RT9026 0D9V_S0

5V_S5
1D5V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D75V_S3 (1.2A)
0D75V_S3_1

Charger MAX8731A

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA
BT+
DCBATOUT

TPS51125
5V/3D3V

DCBATOUT_51125
S5_ENABLE
ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (5A)
5V_AUX_S5
3D3V_AUX_S5

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

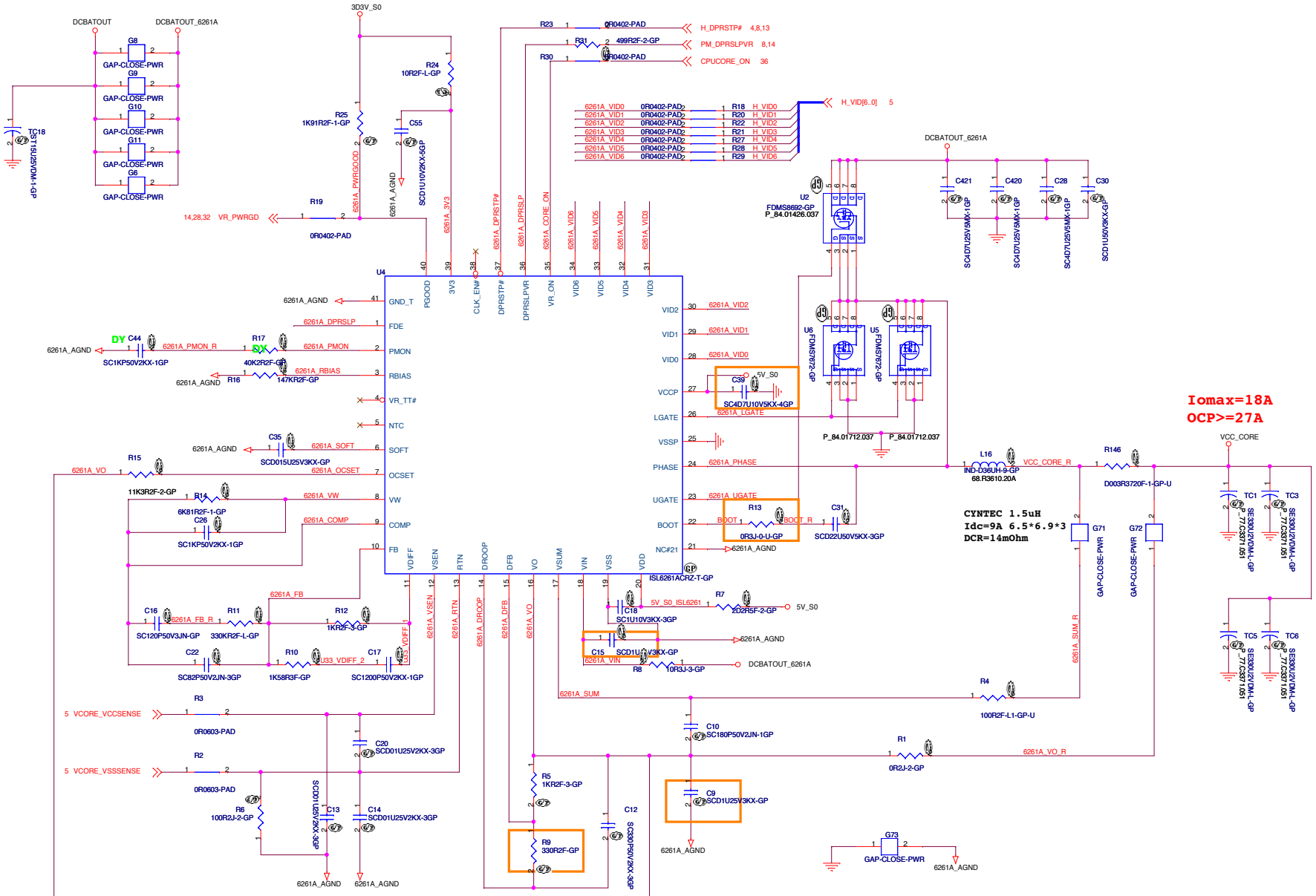
DIS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Sequence Logic**

Size	Document Number	Rev
B	JM41_Discrete	-1

Date: Monday, April 06, 2009 Sheet 33 of 48



DIS

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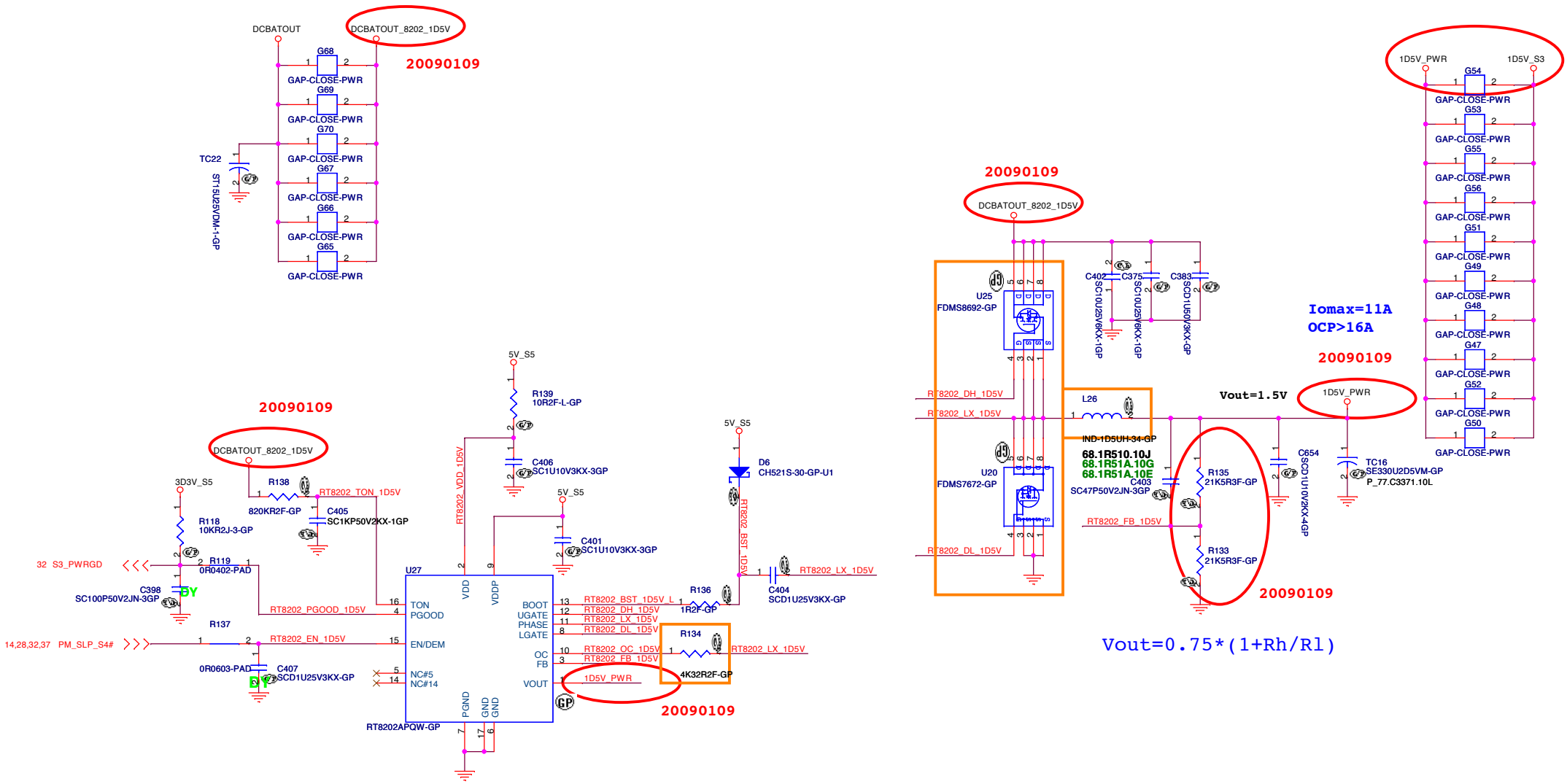
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL6261A_CPU CORE**

Size	Document Number	Rev
Custom	JM41_Discrete	-1

Date: Monday, April 06, 2009 Sheet 34 of 48



DIS

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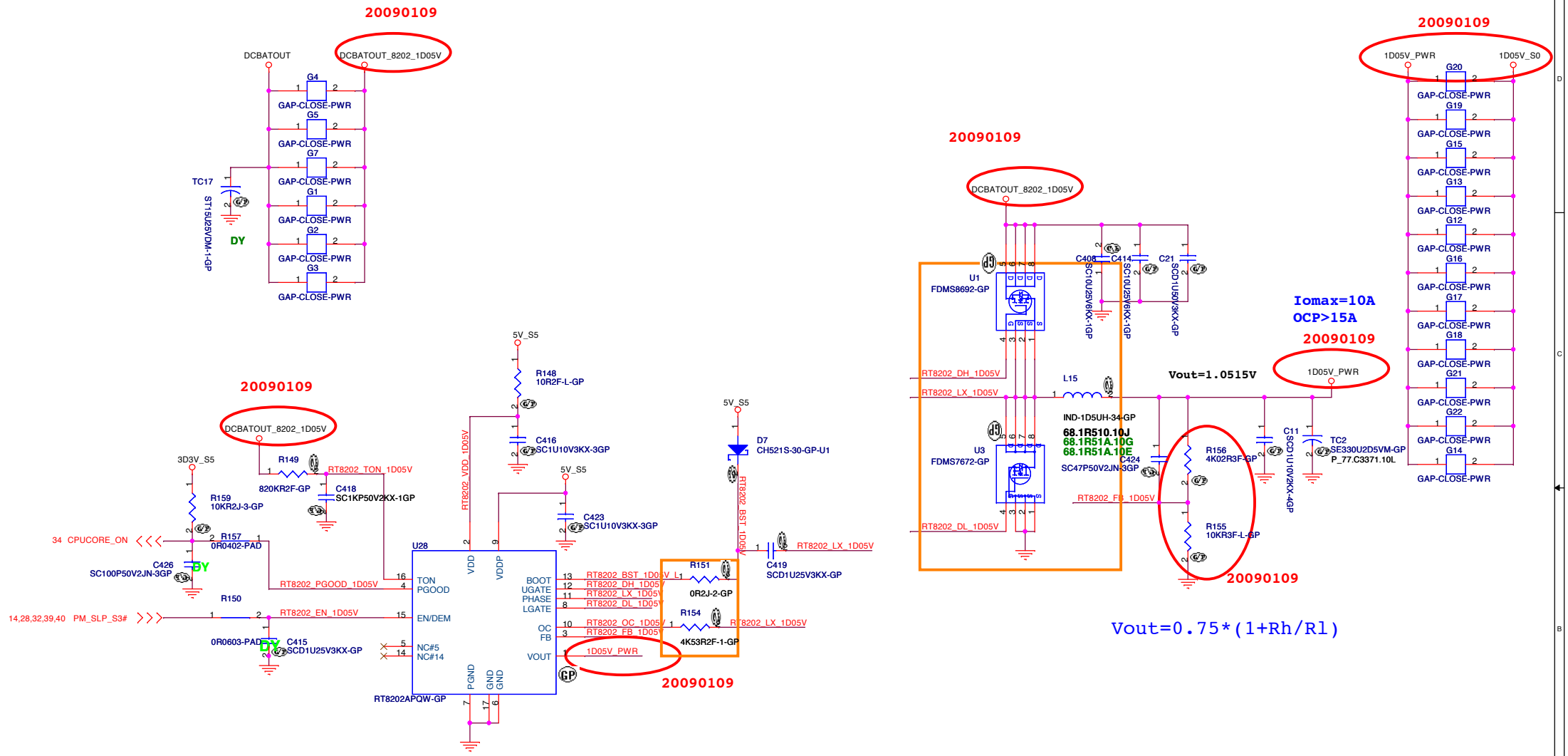
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8202_1D5V

Size: A3 | Document Number: JM41_Discrete | Rev: -1

Date: Monday, April 13, 2009 | Sheet 35 of 48



DIS

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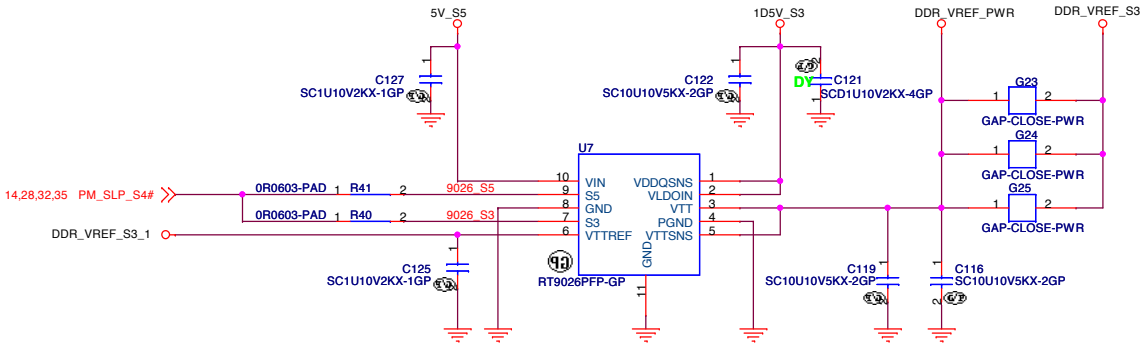
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8202_1D05V

Size: A3 | Document Number: JM41_Discrete | Rev: -1

Date: Monday, April 13, 2009 | Sheet 36 of 48

Iomax=1.2A
OCP>2A



DIS

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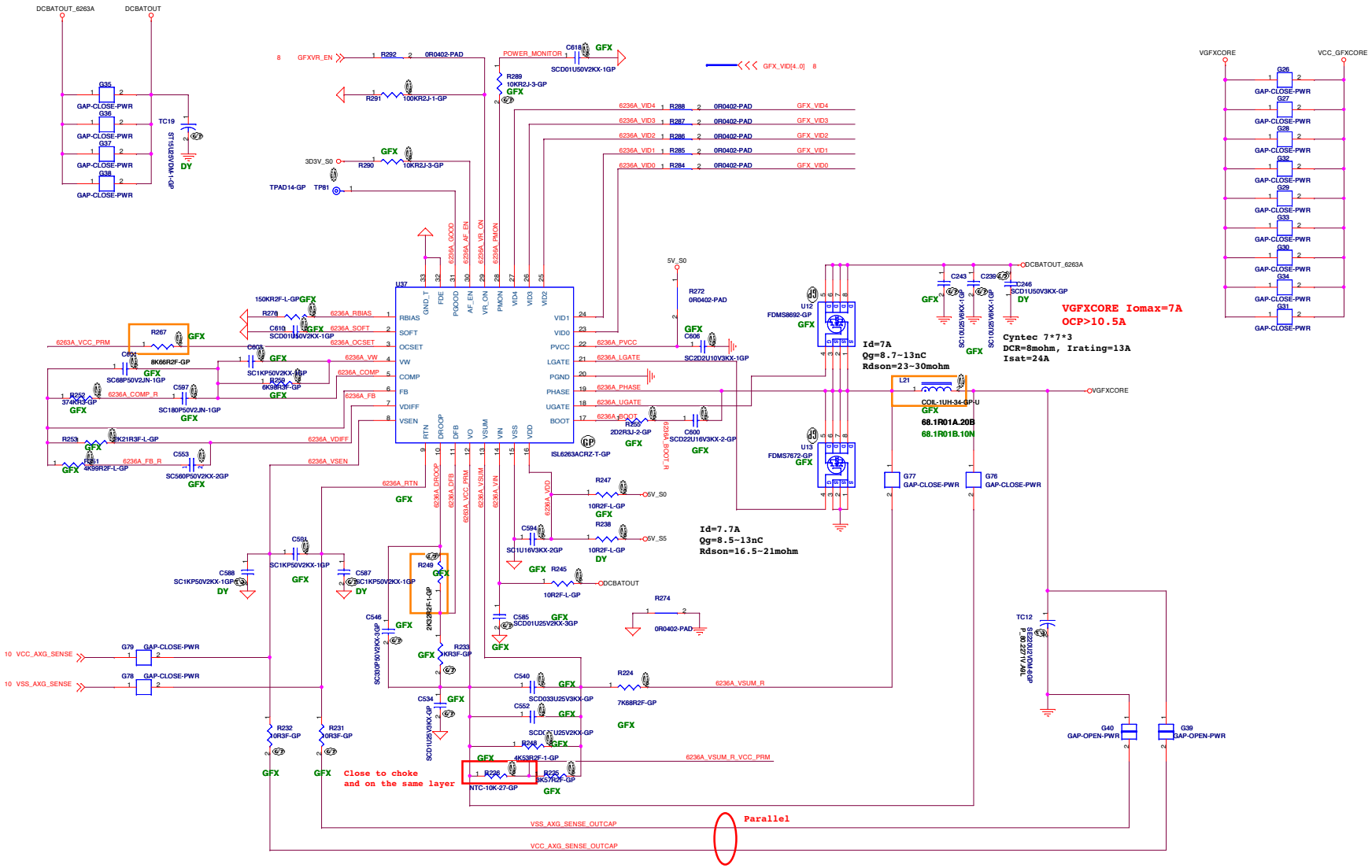
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT9026_0D75V	
Size A3	Document Number JM41_Discrete	Rev -1
Date: Monday, April 06, 2009	Sheet 37 of 48	



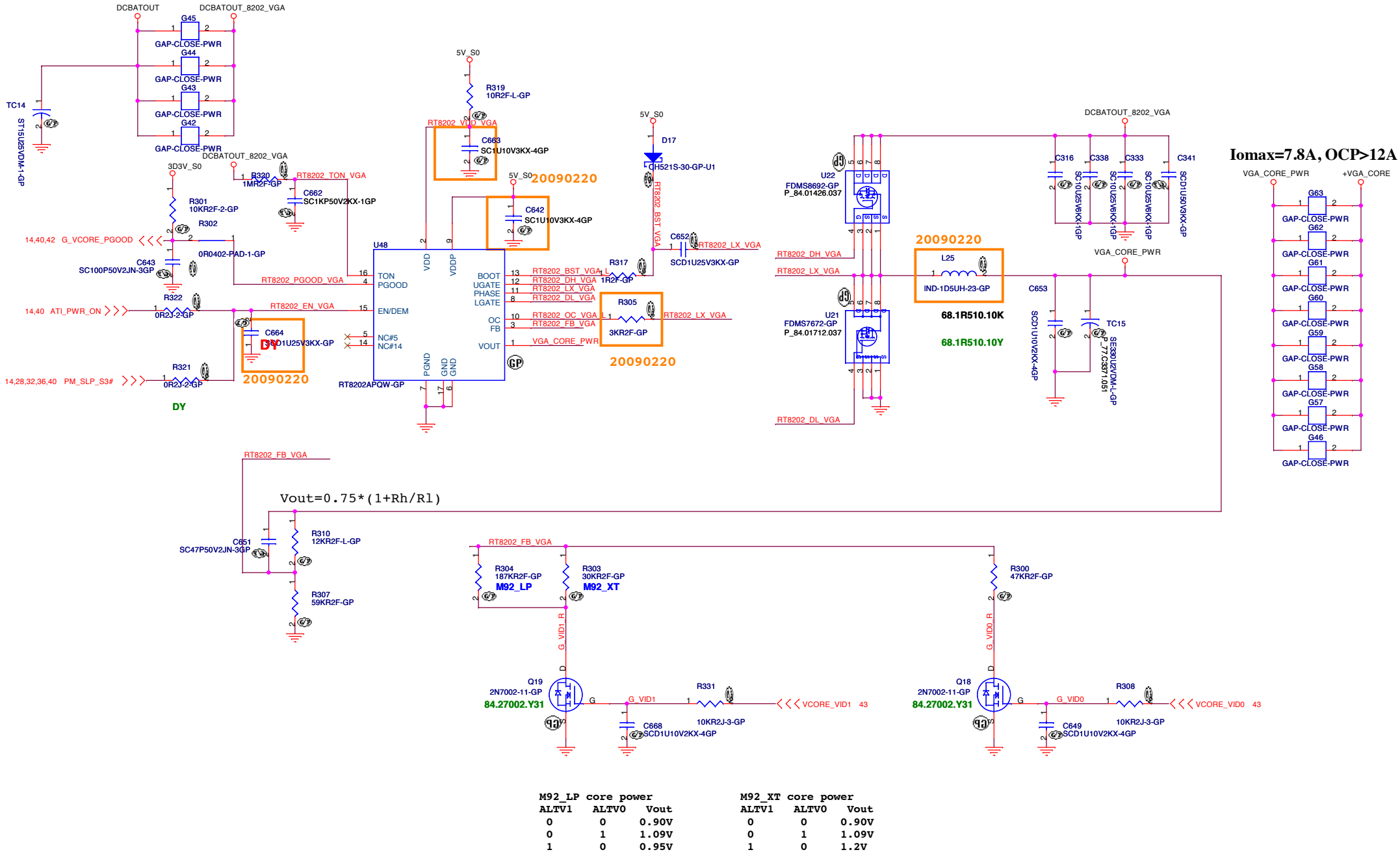
DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6263A_GFX CORE

Size: A2 | Document Number: JM41_Discrete | Rev: -1

Date: Monday, April 06, 2009 | Sheet 38 of 48



M92_LP core power		
ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	0.95V

M92_XT core power		
ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	1.2V

DIS

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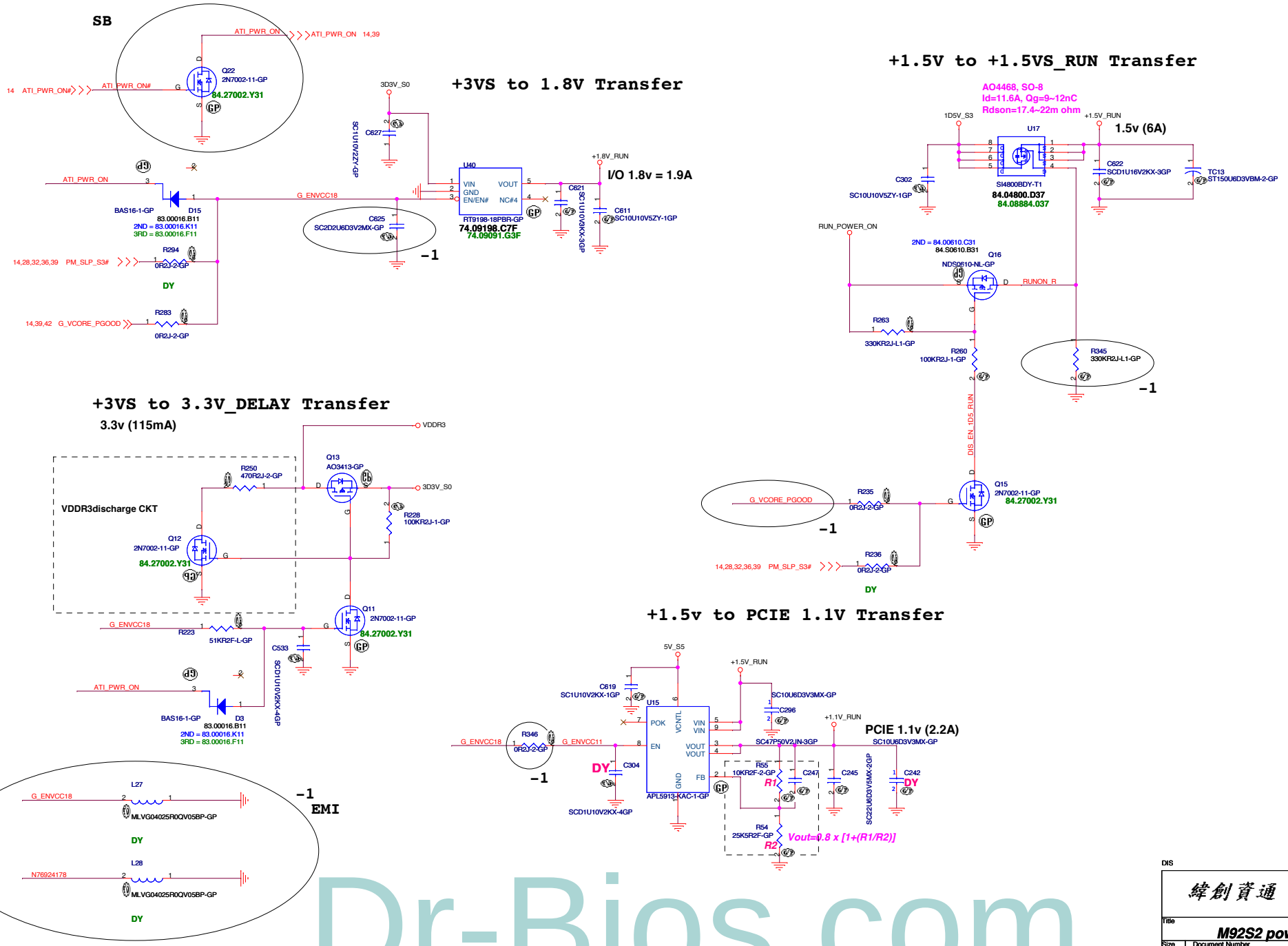
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8202A_VGA CORE

Size: A3 | Document Number: JM41_Discrete | Rev: -1

Date: Monday, April 06, 2009 | Sheet 39 of 48



DIS

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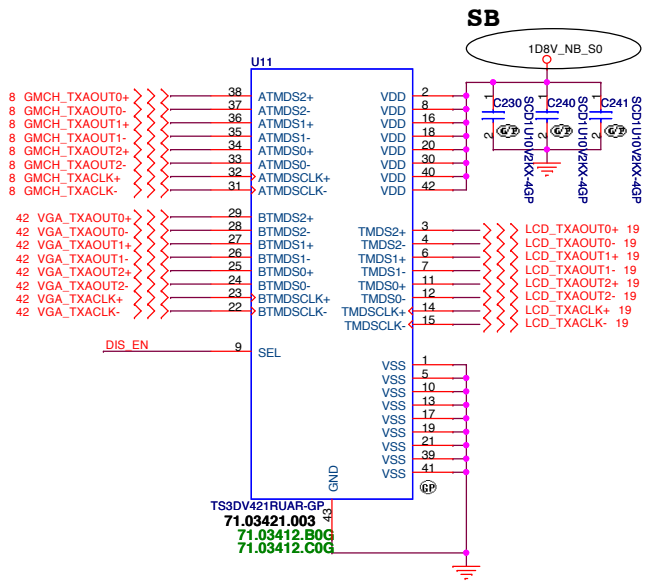
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M92S2 power

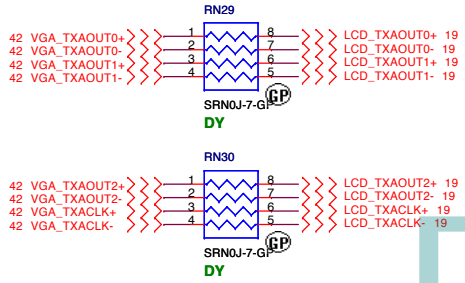
Size	Document Number	Rev
Custom	JM41_Discrete	-1

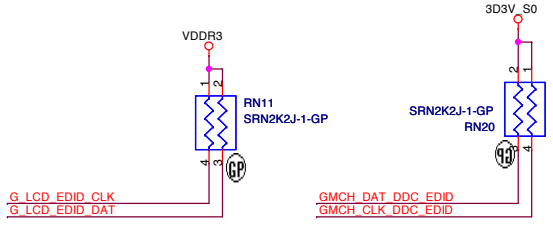
Date: Monday, April 13, 2009 Sheet 40 of 48

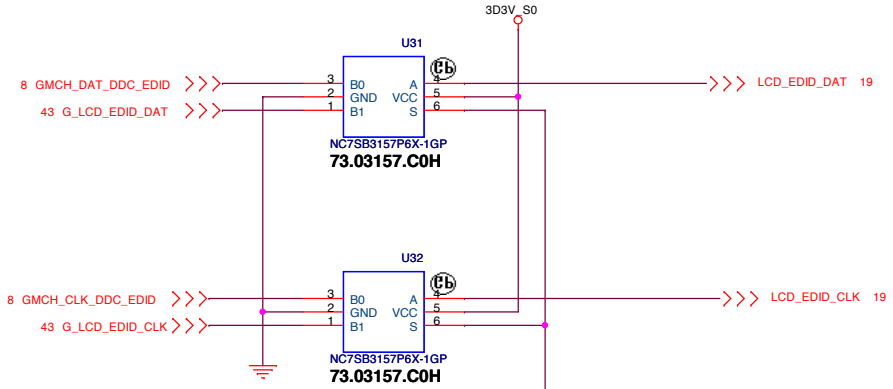


FUNCTION TABLE

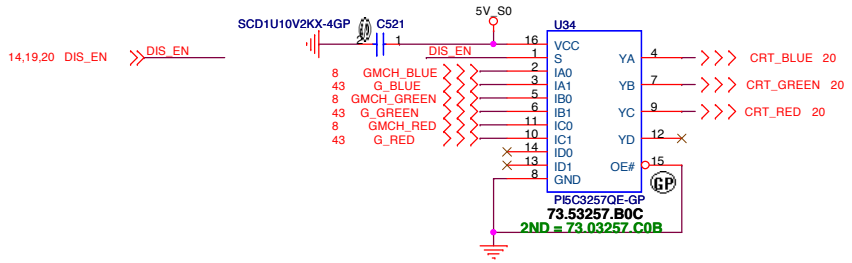
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-







$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



DIS

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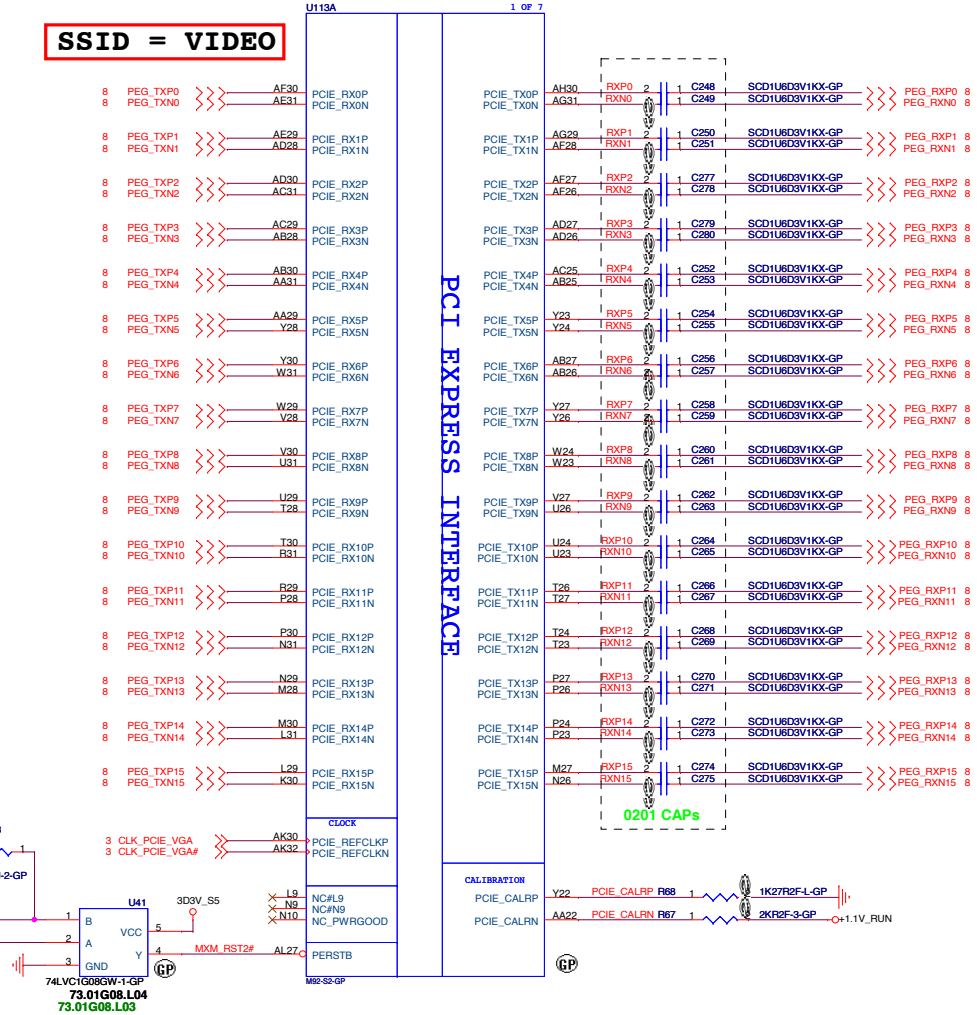
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

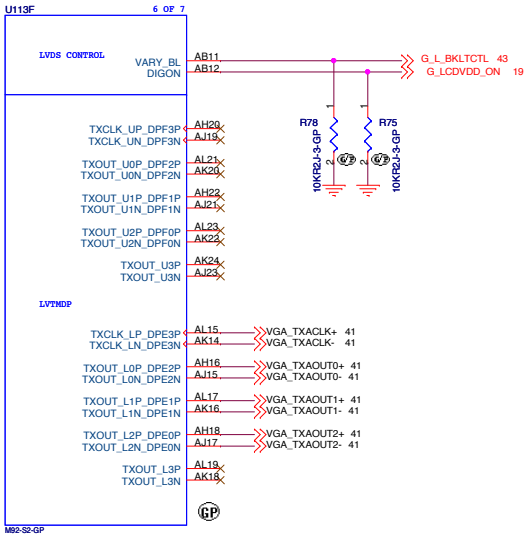
Title: PX_SWITCH

Size	Document Number	Rev
A3		-1

Date: Monday, April 06, 2009 Sheet 41 of 48

SSID = VIDEO





DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA-PCIE/LVDS(1/4)**

Size	Document Number	Rev
Custom	JM41_Discrete	-1

Date: Monday, April 06, 2009 Sheet 42 of 48

SSID = VIDEO

DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung

+1.8V_RUN

R120 10KR2J-3-GP Samsung — DVPDATA23
R101 10KR2J-3-GP Hynix — DVPDATA22
R121 10KR2J-3-GP DY — DVPDATA21
R100 10KR2J-3-GP DY — DVPDATA20
R116 10KR2J-3-GP Hynix — DVPDATA20
R102 10KR2J-3-GP Samsung — DVPDATA21
R117 10KR2J-3-GP — DVPDATA22
R86 10KR2J-3-GP — DVPDATA23

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO 0000 - GDDR3 16Mx32 Qimonda 0001 - GDDR3 32Mx32 Hynix 0010 - GDDR3 32Mx32 Qimonda 0011 - GDDR3 32Mx32 Samsung

U113B 2 OF 7

MUTI GPX

DVPCNTL_MVP_0 AA1
DVPCNTL_MVP_1 Y4
DVPCNTL_0 AC7
DVPCNTL_1 Y2
DVPCNTL_2 U5
DVPCLK U1
DVPDATA_0 Y7
DVPDATA_1 V2
DVPDATA_2 Y6
DVPDATA_3 V4
DVPDATA_4 AB7
DVPDATA_5 W1
DVPDATA_6 AB8
DVPDATA_7 W3
DVPDATA_8 AB9
DVPDATA_9 W5
DVPDATA_10 AC6
DVPDATA_11 W6
DVPDATA_12 AD7
DVPDATA_13 AA3
DVPDATA_14 AC8
DVPDATA_15 AA5
DVPDATA_16 AE8
DVPDATA_17 AA6
DVPDATA_18 AE9
DVPDATA_19 AB4
DVPDATA_20 AD9
DVPDATA_21 AB2
DVPDATA_22 AC10
DVPDATA_23 AC5

DPA
TXCAP_DPA3P AF2
TXCAM_DPA3N AF4
TX0P_DPA2P AG3
TX0M_DPA2N AG5
TX1P_DPA1P AH3
TX1M_DPA1N AH1
TX2P_DPA0P AK3
TX2M_DPA0N AK1

DPB
TXCBP_DPB3P AK5
TXCBM_DPB3N AM3
TX3P_DPB2P AK6
TX3M_DPB2N AM5
TX4P_DPB1P AJ7
TX4M_DPB1N AH6
TX5P_DPB0P AK8
TX5M_DPB0N AL7

PLACE THESE CAPACITOR CLOSE TO CONNECTOR

HDMI (DPA)

G_HDMI_D_CLK+ C376 SCD1U10V2KX-4GP — HDMI_CLK+ 20
G_HDMI_D_CLK- C372 SCD1U10V2KX-4GP — HDMI_CLK- 20
G_HDMI_TX2+ C390 SCD1U10V2KX-4GP — HDMI_DATA0+ 20
G_HDMI_TX2- C384 SCD1U10V2KX-4GP — HDMI_DATA0- 20
G_HDMI_TX1+ C396 SCD1U10V2KX-4GP — HDMI_DATA1+ 20
G_HDMI_TX1- C392 SCD1U10V2KX-4GP — HDMI_DATA1- 20
G_HDMI_TX0+ C400 SCD1U10V2KX-4GP — HDMI_DATA2+ 20
G_HDMI_TX0- C399 SCD1U10V2KX-4GP — HDMI_DATA2- 20

PLACE THESE RESISTORS CLOSE TO DIFF. PAIRS AND AVOID STUBS TO ALL DIFF. TRACES.

MINIMIZE THE DISTANCE BETWEEN THESE RES. AND 100nF AC CAPS

I2C
41 G_LCD_EDID_CLK — R1 — SCL
41 G_LCD_EDID_DAT — R3 — SDA

GENERAL PURPOSE I/O

42 G_L_BKLTCTL — R89 0R2J-2-GP — GPIO_0 U6
GPIO_1 U10
GPIO_2 T10
GPIO_3_SMBDATA U8
GPIO_4_SMBCLK U7
GPIO_5_AC_BATT T8
GPIO_6 T9
19 G_BL_ON — R90 0R2J-2-GP DY — GPIO_7_BLON T7
GPIO_8_ROMSO P10
GPIO_9_ROMSI P4
GPIO_10_ROMSCK P2
GPIO_11 N6
GPIO_12 N5
GPIO_13 N3
GPIO_14_HPD2 Y9
GPIO_15_PWRCNTL_0 N1
GPIO_16_SSIN M4
GPIO_17_THERMAL_INT R6
GPIO_18_HPD3 W10
GPIO_19_CTF M2
GPIO_20_PWRCNTL_1 P8
GPIO_21_BB_EN P7
GPIO_22_ROMCSB N8
GPIO_23_CLKREQB N7
GPIO_29_DRM_0 T11
GPIO_30_DRM_1 R11

TP86 G_TEMP_FAIL — R124 10KR2J-3-GP
TP45 VGA_THERM# — 10KR2J-3-GP R128 — VGA_CLK_REQ# 3
39 VCORE_VID0 — TP87 — CLK_VID_27M_SS
TP33 — G_TEMP_FAIL
39 VCORE_VID1 — R109 10KR2J-3-GP — VGA_CLK_REQ#
20 HDMI_DETECT# — R81 4K99R2F-L-GP — G_HDMI_DETECT# — R84 10KR2J-3-GP

JTAG_TRSTB L6
JTAG_TDI L5
JTAG_TCK L3
JTAG_TMS L1
JTAG_TDO K4
TESTEN AF24
JTAG_TESTEN — R131 1KR2J-1-GP
TP85 TP83 TP84 TP82
GENERICA AB13
GENERICB W8
GENERICC W9
GENERICD W7
GENERICE_HPD4 AD10
TP30 TP40 TP35 TP39
R66 1KR2J-1-GP
TP34 — G_HDMI_DETECT# — HPD1 AC14

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = .6V)
VREFG AC16
+1.8V_RUN — R299 499R2F-2-GP — VGA_VREFG — R74 249R2F-GP — C331 SCD1U16V2KX-3GP

PLL/CLOCK

DPLL_PVDD 120mA AF14 AE14
DPLL_VDDC 300mA AD14
XTALIN AM28
XTALOUT AK28
C612 SC22P50V2JN-4GP — X4 XTAL-27MHZ-74-GP — C624 SC27P50V2JN-2GP
82.30034.611
2ND = 82.30034.421
G_27M_XTALIN — G_27M_XTALOUT — 1MR2F-GP R282

THERMAL

DPLUS T4
DMINUS T2
GPU_TEMP+ — GPU_TEMP-
TS_FDO R5
TSVDD 20mA AD17
TSVSS AC17
+TSVDD — TP88 — L22 BLM15BD121SN1D-GP — +1.8V_RUN
68.00217.611
C329 SC1U10V2KX-1GP — C330 SCD1U16V2KX-3GP

M92-S2-GP

CRT

R AM26 AK26 — G_RED — R63 150R2F-1-GP — G_RED 41
G AL25 AJ25 — G_GREEN — R64 150R2F-1-GP — G_GREEN 41
B AH24 AG25 — G_BLUE — R69 150R2F-1-GP — G_BLUE 41
HSYNC AH26 — G_HSYNC 20,45
VSYNC AJ27 — G_VSYNC 20,45
RSET AD22 — VGA_RSET — R70 499R2F-2-GP (Placed between this pin and AVSSQ)
70mA AVDD AG24 — +DAC1_AVDD — M92_AVSSQ — GAP-CLOSE G41
AVSSQ AE22
45mA VDD1DI AE23 — +DAC1_VDD1DI
VSS1DI AD23

DAC1

DAC2

R2 AM12 AK12
R2B AL11 AJ11
G2 AK10 AL9
G2B AH12 AM10
B2 AJ9
B2B AL13 AJ13
C
Y
COMP
H2SYNC
V2SYNC
40mA VDD2DI AD19 — +1.8V_RUN
VSS2DI AC19
65mA A2VDD AE20 — VDDR3
2mA A2VDDQ AE17 — +1.8V_RUN
A2VSSQ AE19
R2SET AG13 — VGA_R2SET — R76 715R2F-GP

DDC/AUX

DDC1CLK AE6 — G_DDCCLK 20
DDC1DATA AE5 — G_DDCDATA 20
AUX1P AD2
AUX1N AD4
DDC2CLK AC11 — G_HDMI_CLK 20
DDC2DATA AC13 — G_HDMI_DATA 20
AUX2P AD13
AUX2N AD11
NC#AB22 AB23
NC#AC22 AC23
DDCAUX5P AE16
DDCAUX5N AD16
DDC6CLK AC1
DDC6DATA AC3
NC_DDCAUX7P AD20
NC_DDCAUX7N AC20

VDDR3 — RN12 SRN1K5J-GP — G_HDMI_CLK — G_HDMI_DATA

+DAC1_AVDD — C297 SCD1U16V2KX-3GP — C545 SCD1U16V2KX-3GP — C538 SC1U10V2KX-1GP — C551 SC-D71MD3/3MX-3GP — L18 BLM15BD121SN1D-GP — +1.8V_RUN
68.00217.611
+DAC1_VDD1DI — C544 SCD1U16V2KX-3GP — C303 SCD1U16V2KX-3GP — C537 SC1U10V2KX-1GP — L19 BLM15BD121SN1D-GP — +1.8V_RUN
68.00217.611

VDDR3 — C614 SCD1U16V2KX-3GP
25,27,28 SMBC_THERM — G83 G781_CLOSE — KBC_THERM_G781_CLK
25,27,28 SMBD_THERM — G82 — KBC_THERM_G781_DAT
U38 G781P8F-GP
SMBCLK SMBDATA ALERT# GND — VCC DXP DXN THERM#
G781_ALERT#
GPU_TEMP+ — C607 SC2200P50V2KX-2GP — GPU_TEMP-
GPU_THERM# — R262 2K2R2F-GP — R264 2K2R2F-GP — VDDR3

GPU DIE TEMP:
REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing.

-1
3D3V_S0 — R219 10KR2J-3-GP — HDMI_hotplug 28
HDMI_DETECT# — Q24 2N7002-11-GP
84.27002.Y31

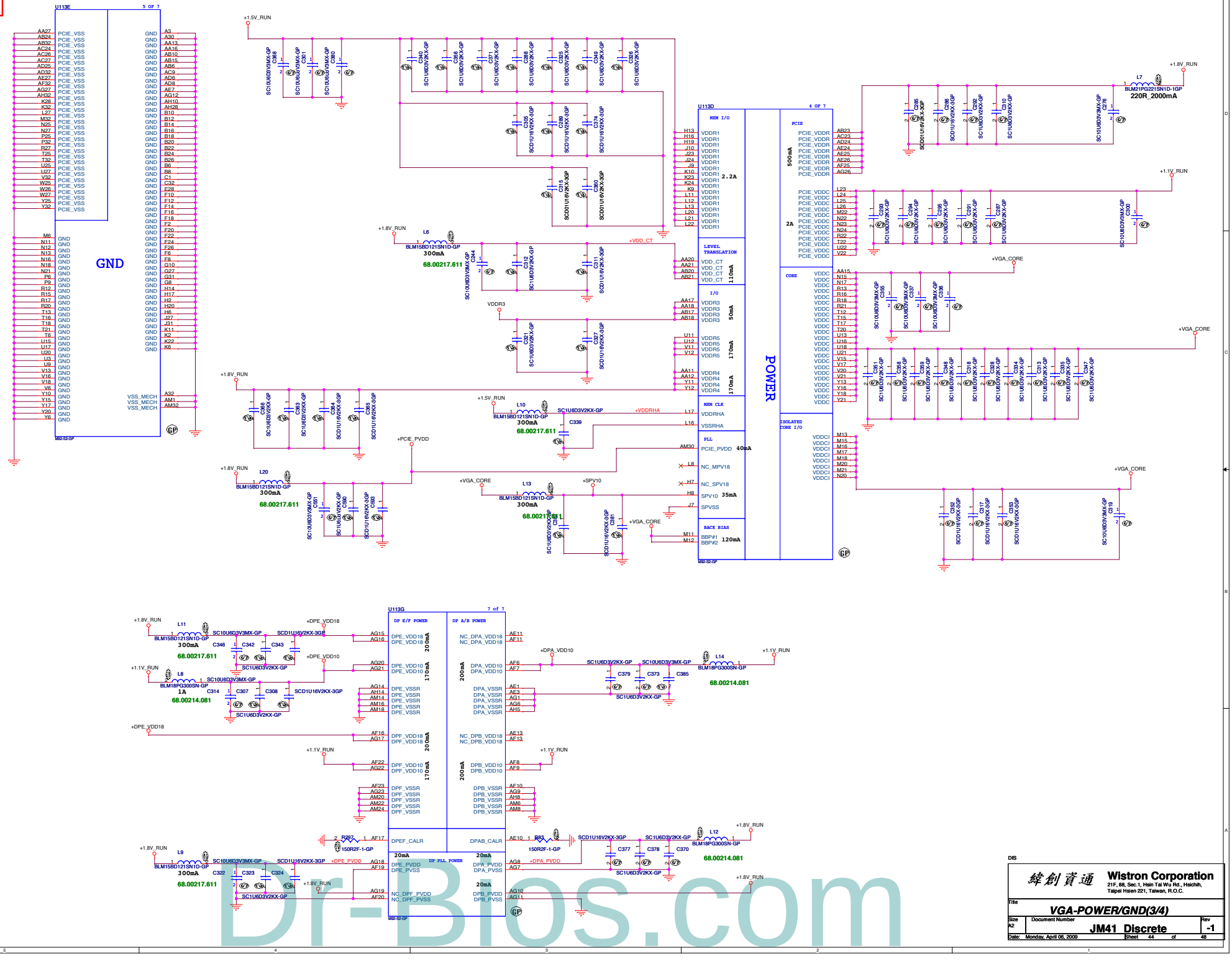
H:UMA MODE HDMI PLUG_OUT
L:UMA MODE HDMI PLUG_IN

DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-TV/CRT/DP PORT(2/4)
Size: C
Document Number: JM41_Discrete
Rev: -1
Date: Monday, April 06, 2009
Sheet 43 of 48

SSID = VIDEO



DIS

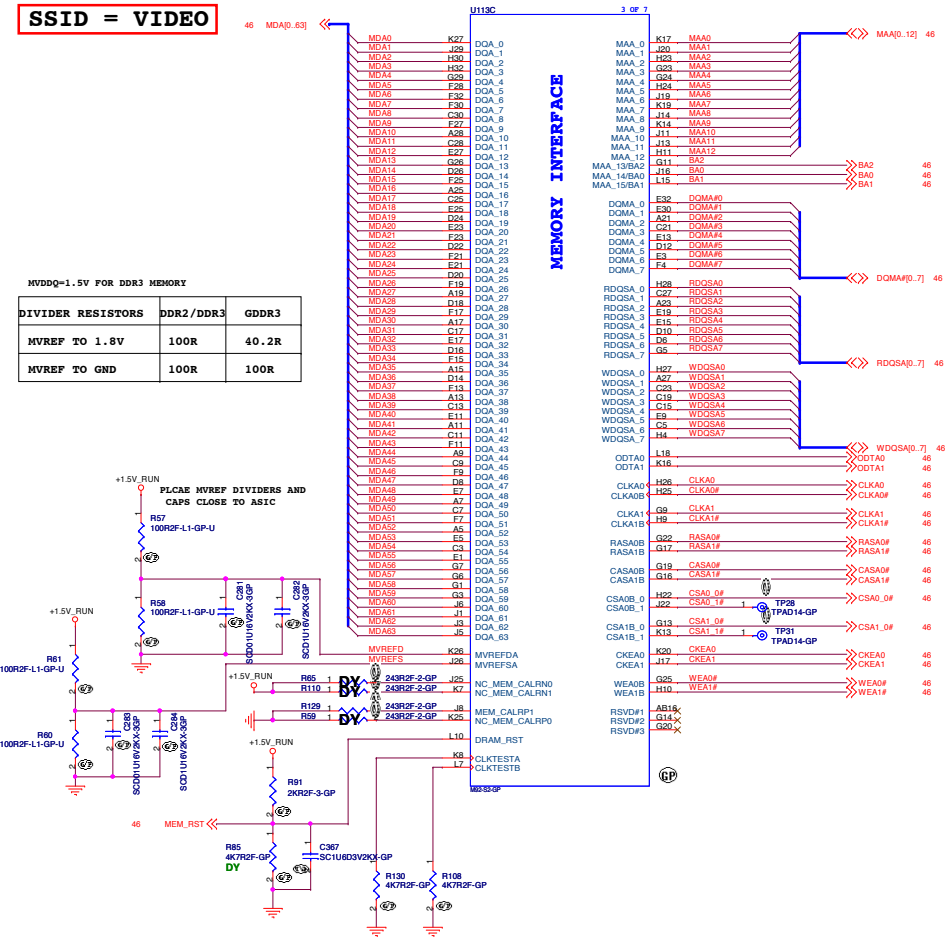
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-POWER/GND(3/4)

Size: A2 | Document Number: JM41 Discrete | Rev: -1

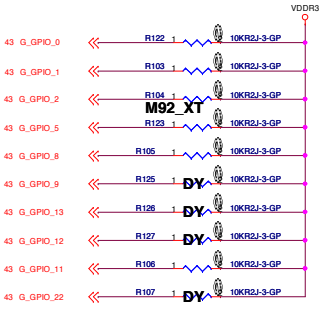
Date: Monday, April 06, 2009 | Sheet 44 of 48

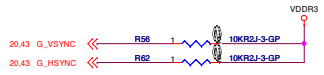
SSID = VIDEO



MVDDQ=1.5V FOR DDR3 MEMORY

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R





ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[9,13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
V 64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing V
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled V
BIF_GEN2_EN_A	GPIO2	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	0= Disable CLKREQ#power management capability 1= Enable CLKREQ# power management capability V
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI V

DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-MEMORY/STRAPS(4/4)

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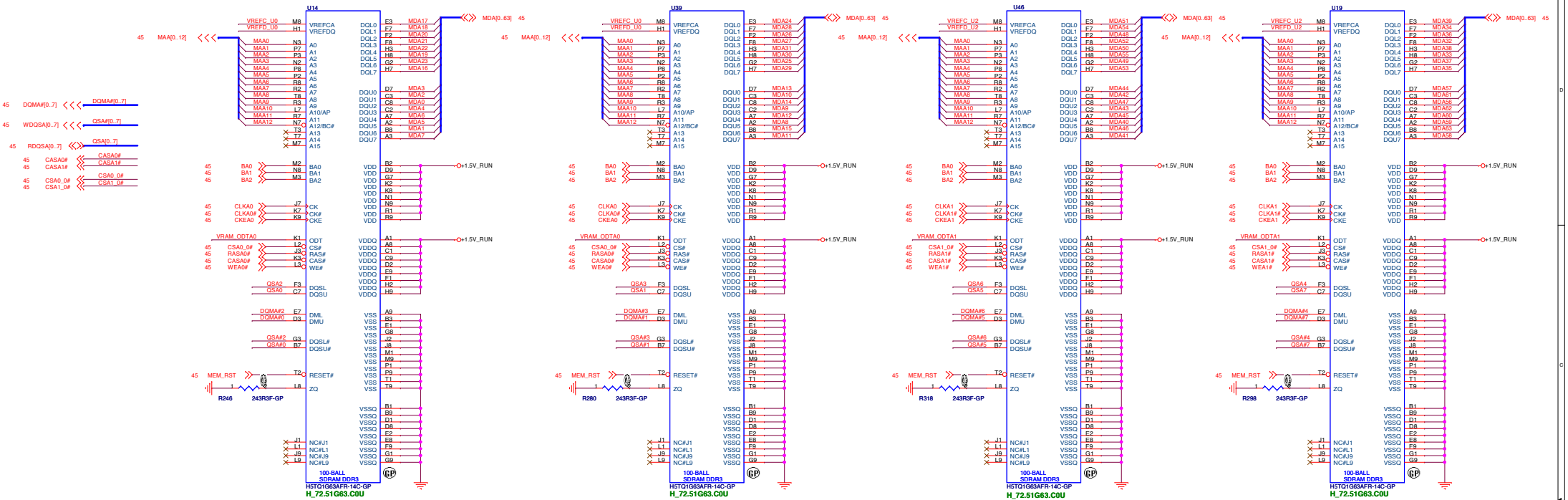
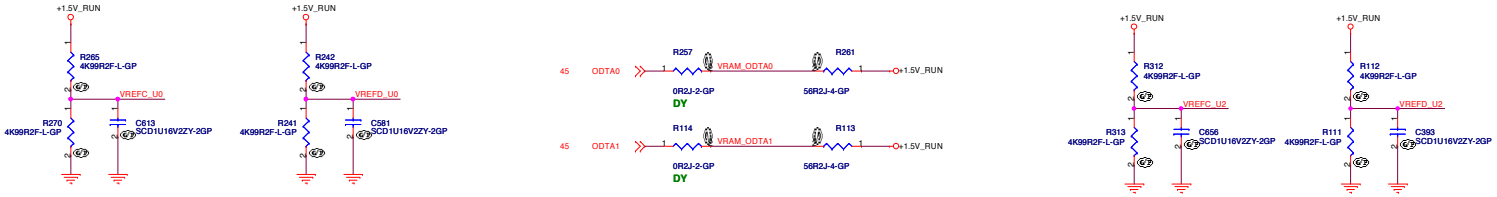
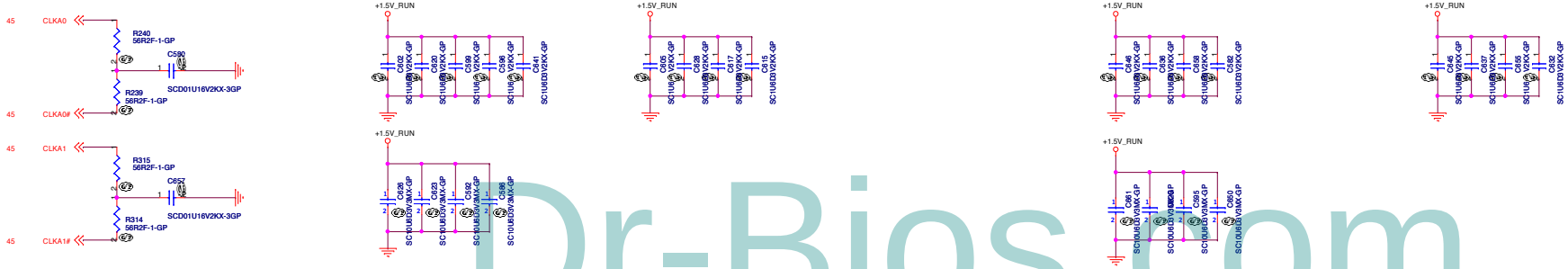
512MB DDR3





Samsung : K4W1G1646E-EC12

Hynix : H5TQ1G63BFR-12C



DIS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VRAM	
Size: A2	Document Number: JM41 Discrete	Rev: -1
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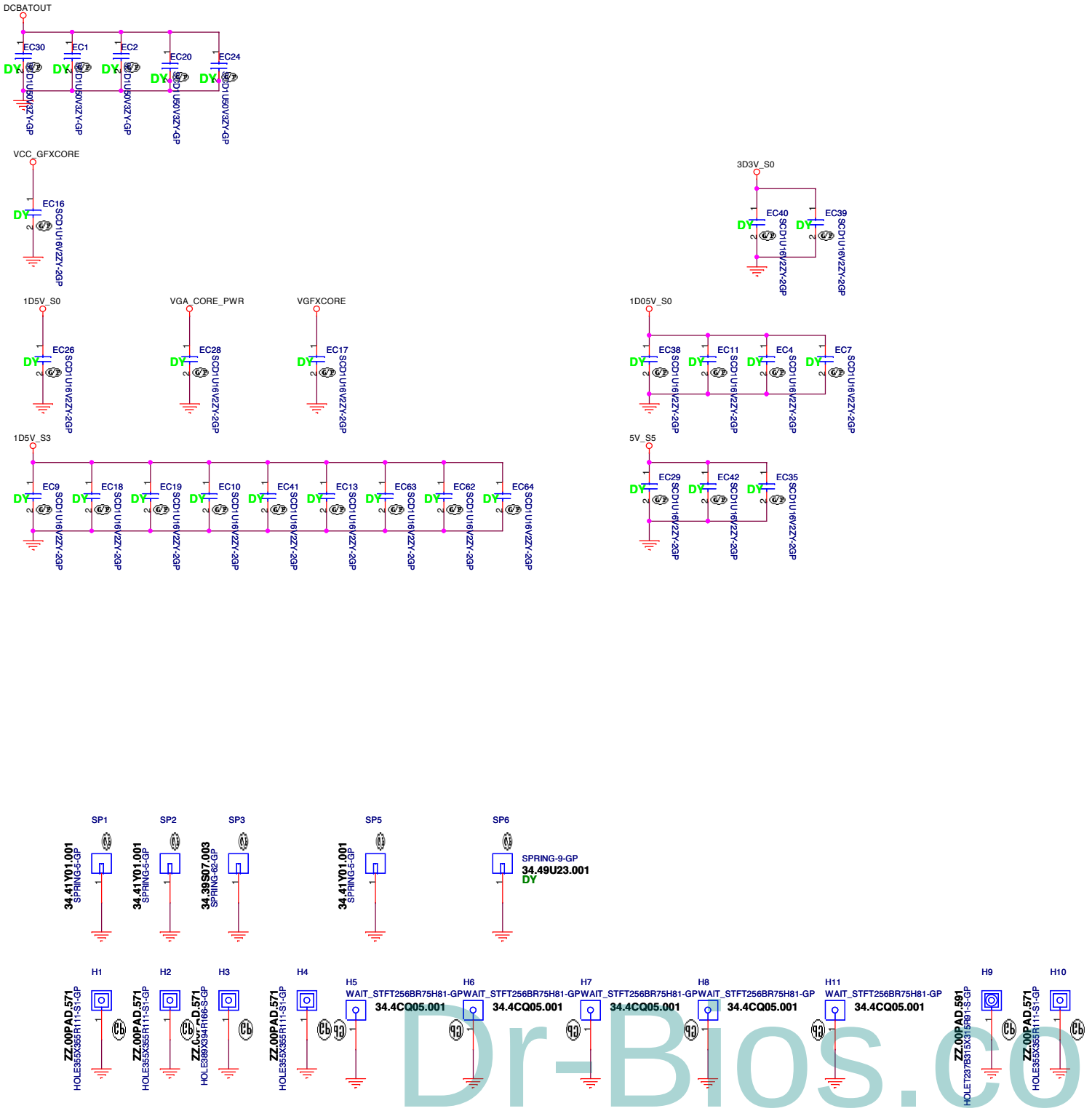

DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

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JM41/JM51 DIS Schematic EC Tracking Record
EC #/ Page / Description / Part Affected

EC SC01/11/connect NB1.A31 to GND(For power save)
EC SC02/14/net DIS_EN pull high 10K to 3D3V_S0
EC SC03/20/CN2.pin35 change to AGND
EC SC04/22/R311 change to 39.2K
EC SC05/22/U24.pin2 change to AGND
EC SC06/26/BTB2.pin9 add stand by led control signal
EC SC07/28/U16.pin66 add stand by led control signal
EC SC08/28/add circuit to support green adapter
EC SC09/28/net EJECT_BTN pull high 10K to 3D3V_S0
EC SC10/31/add circuit to stand by led control
EC SC11/40/change GPU power enable signal to ATI_PWR_ON#(low active)
EC SC12/41/change U11 power plane to 1D8V_NB_S0

DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY

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A2	JM41_Discrete	-1

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