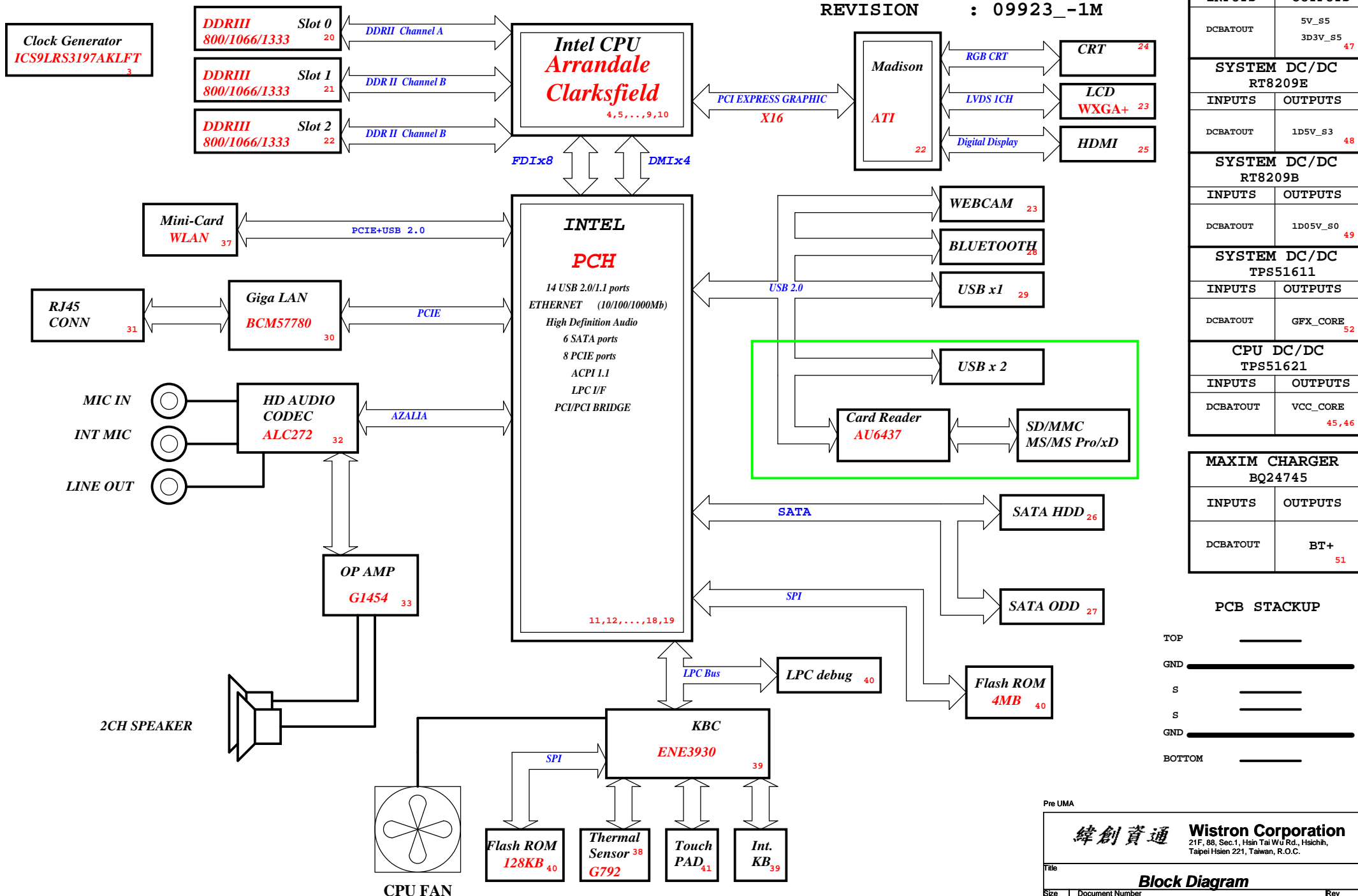


JE70-CP Block Diagram

Project code: 91.4HN01.001
 PCB P/N : 48.4HN01.0SD
 REVISION : 09923_-1M



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 47
SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 48
SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 49
SYSTEM DC/DC TPS51611	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE 52
CPU DC/DC TPS51621	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 45, 46
MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
DCBATOUT	BT+ 51

PCB STACKUP

TOP	_____
GND	_____
S	_____
S	_____
GND	_____
BOTTOM	_____

Pre UMA

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Title: **Block Diagram**

Size A3 Document Number **JE70-CP** Rev **-1M**

Date: Tuesday, February 02, 2010 Sheet 1 of 67

PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

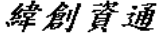
USB Table

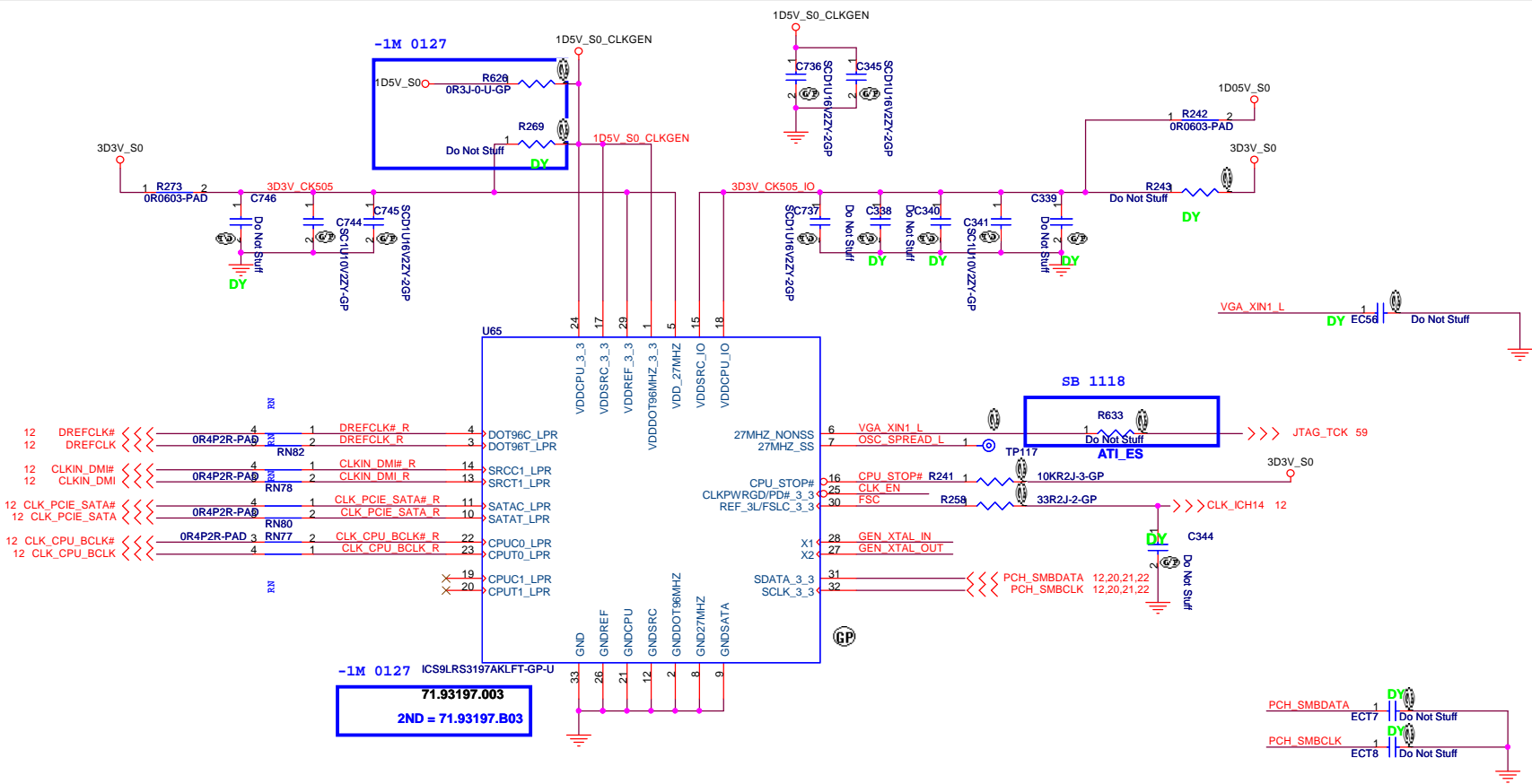
Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

Pre UMA

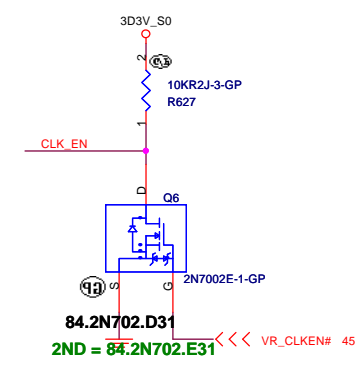
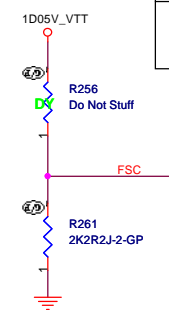
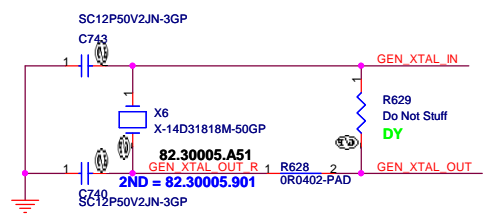
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Table of Content	
Size A3	Document Number JE70-CP
Date: Tuesday, February 02, 2010	Rev -1M
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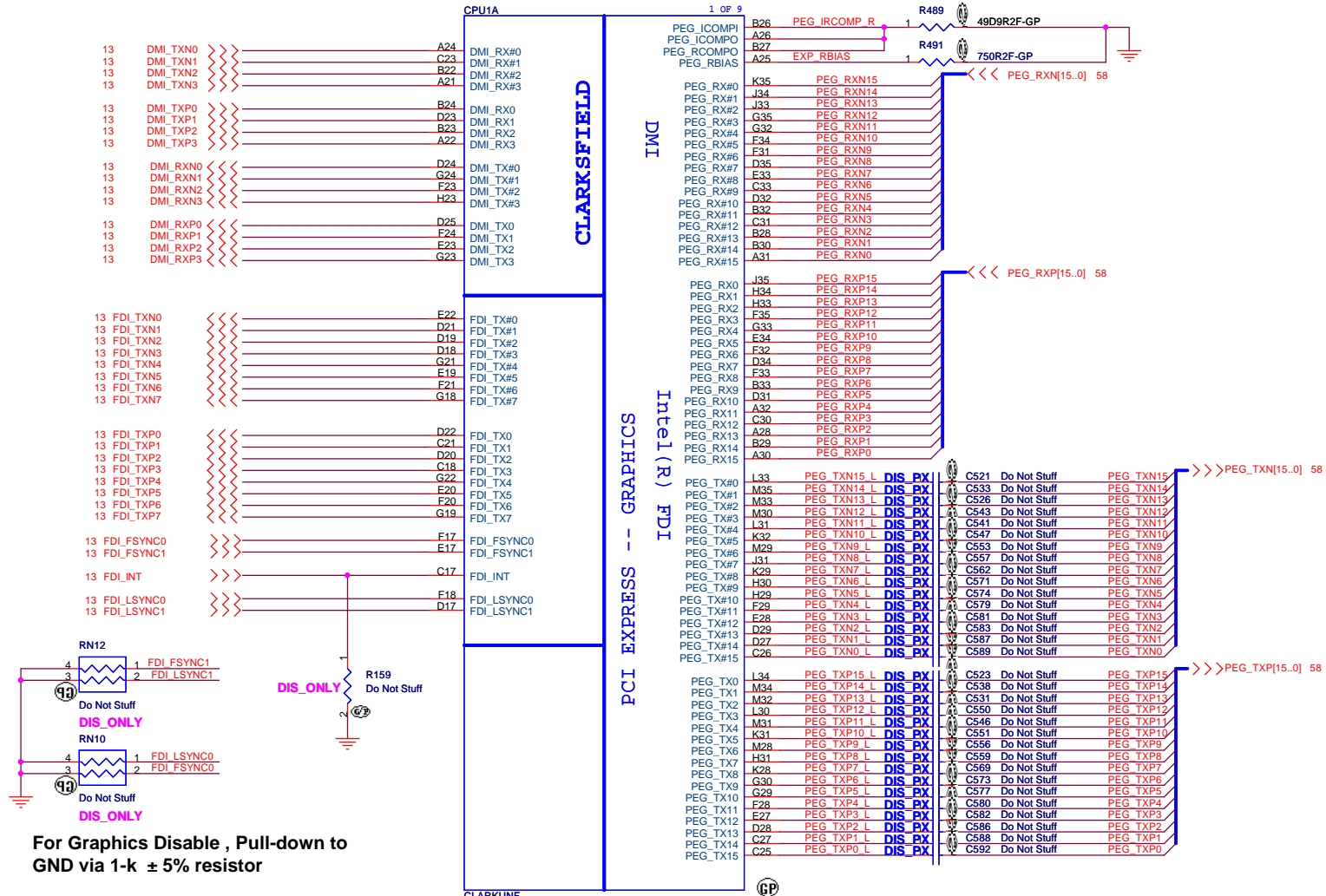


- 12 DREFCLK# <<< 0R4P2R-PA0 4 1 DREFCLK# R 4 DOT96C_LPR
- 12 DREFCLK <<< 0R4P2R-PA0 2 2 DREFCLK R 4 DOT96T_LPR
- 12 CLKIN_DMII# <<< 0R4P2R-PA0 4 1 CLKIN_DMII# R 14 SRCC1_LPR
- 12 CLKIN_DMI <<< 0R4P2R-PA0 2 2 CLKIN_DMI R 13 SRCT1_LPR
- 12 CLK_PCIE_SATA# <<< 0R4P2R-PA0 4 1 CLK_PCIE_SATA# R 11 SATAC_LPR
- 12 CLK_PCIE_SATA <<< 0R4P2R-PA0 2 2 CLK_PCIE_SATA R 10 SATAT_LPR
- 12 CLK_CPU_BCLK# <<< 0R4P2R-PAD 3 RN77 2 CLK_CPU_BCLK# R 22 CPUC0_LPR
- 12 CLK_CPU_BCLK <<< 0R4P2R-PAD 4 1 CLK_CPU_BCLK R 23 CPUT0_LPR

-1M 0127 ICS9LRS3197AKLFT-GP-U
71.93197.003
2ND = 71.93197.B03

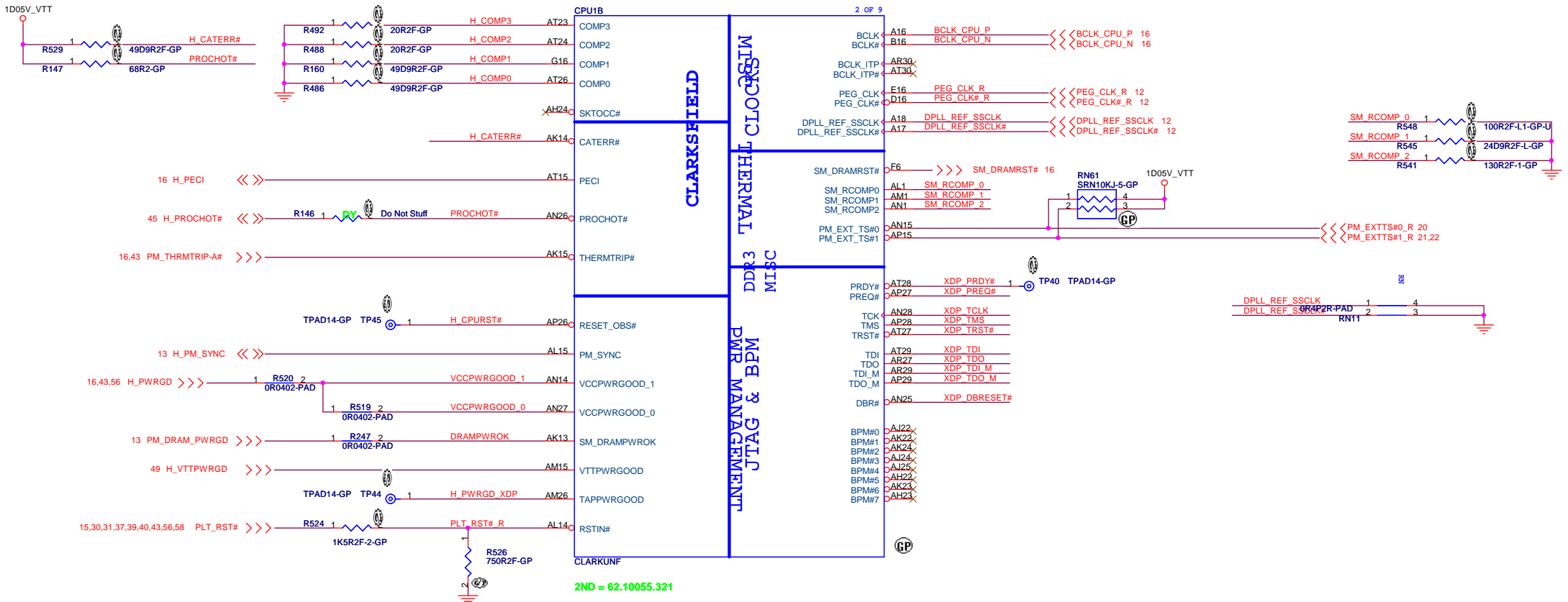
FSC	0	1
SPEED	133MHz (Default)	100MHz

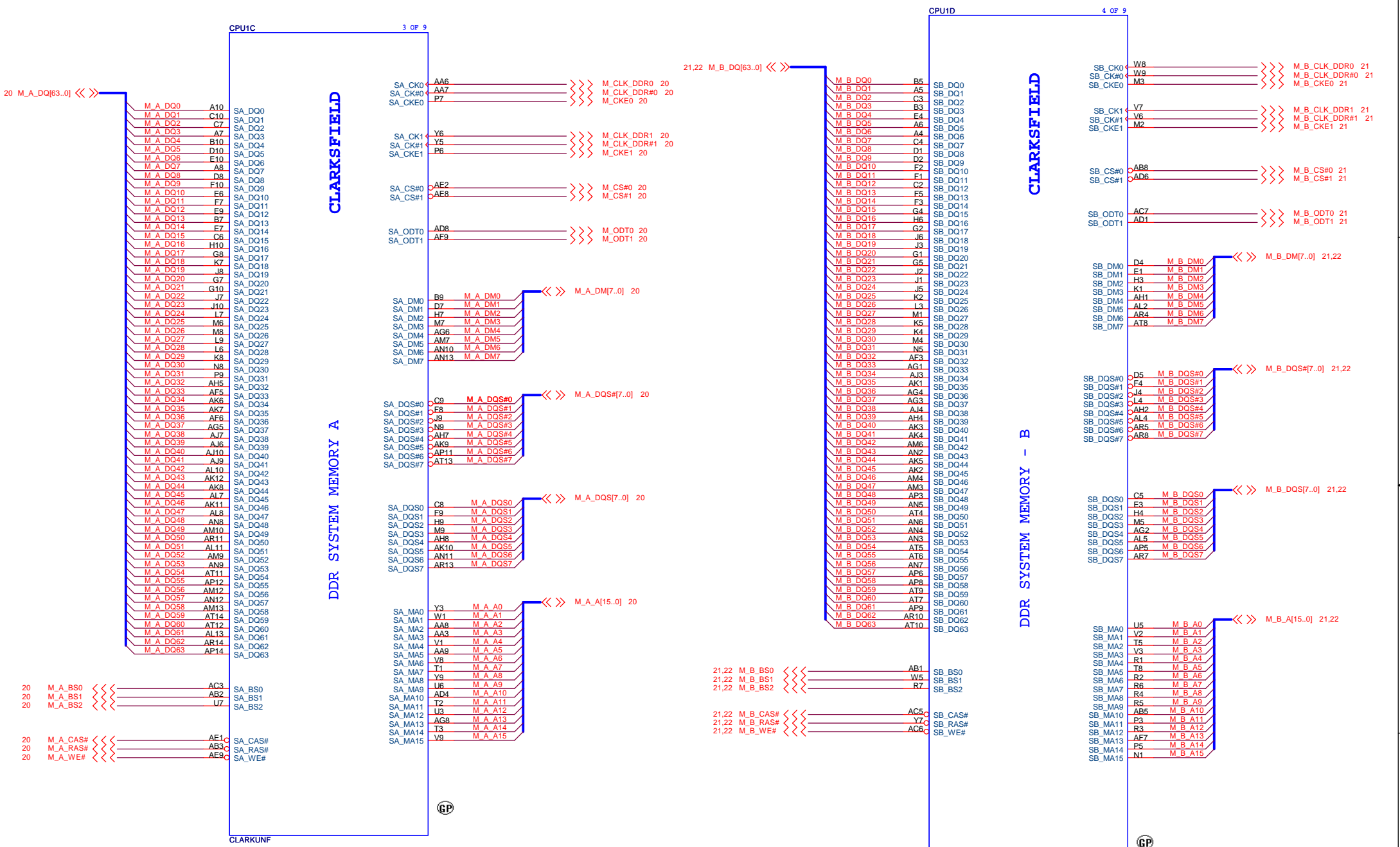




For Graphics Disable, Pull-down to GND via 1-k ± 5% resistor

2ND = 62.10055.321
62.10053.561





62.10053.561

2ND = 62.10055.321

62.10053.561

2ND = 62.10055.321

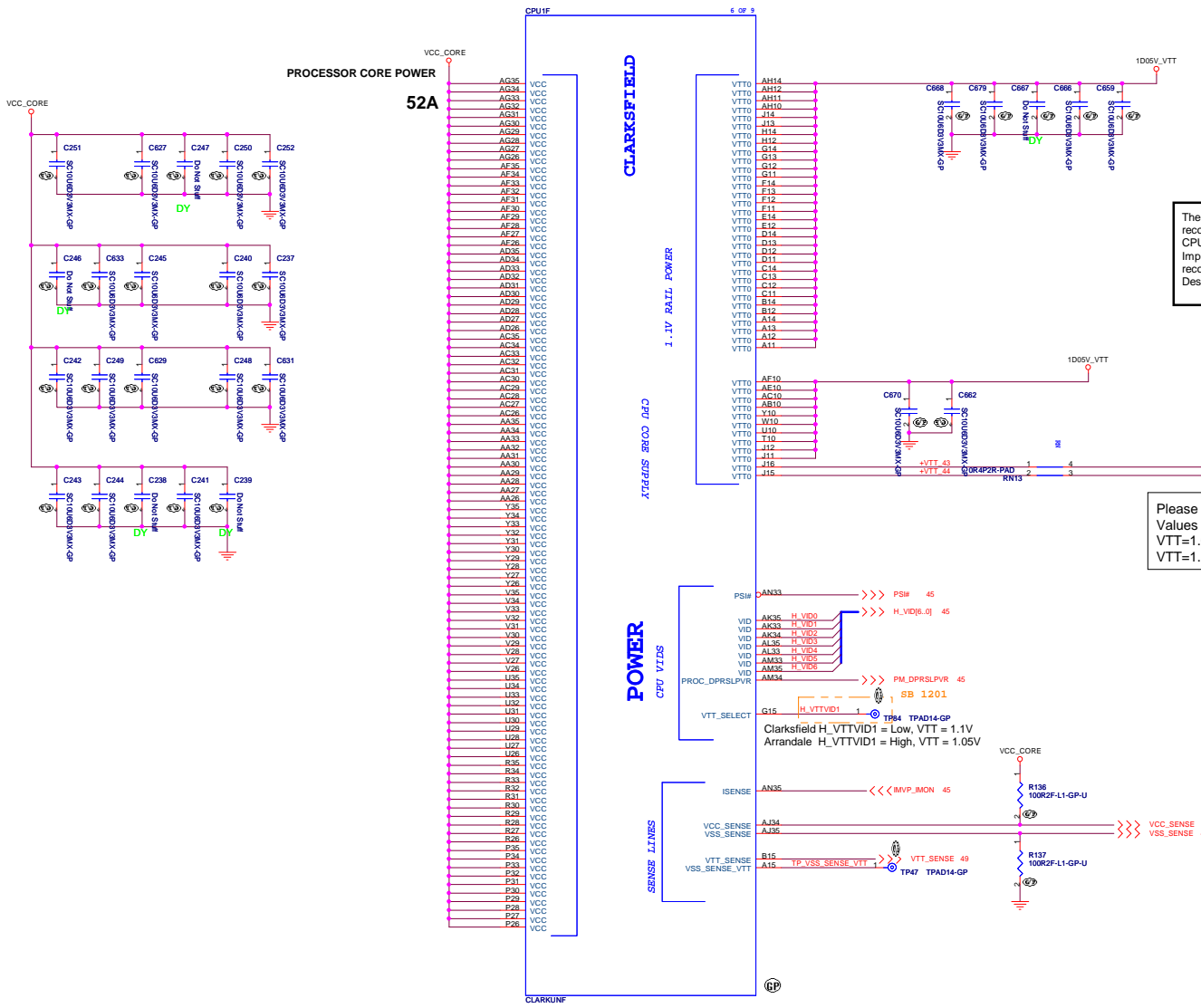
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Title: CPU (3/7)

Size A3 Document Number JE70-CP Rev -1M

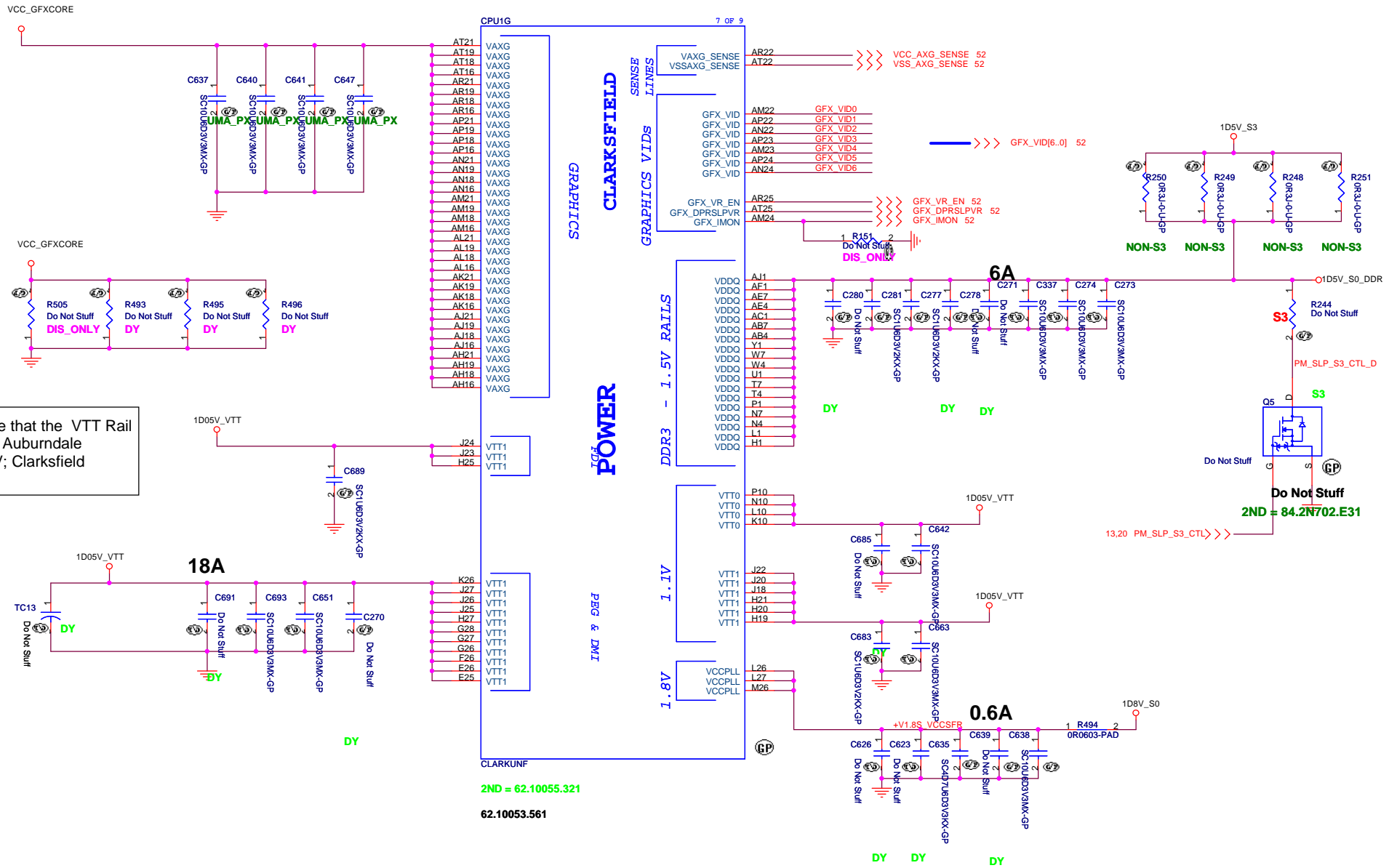
Date: Tuesday, February 02, 2010 Sheet 6 of 67



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

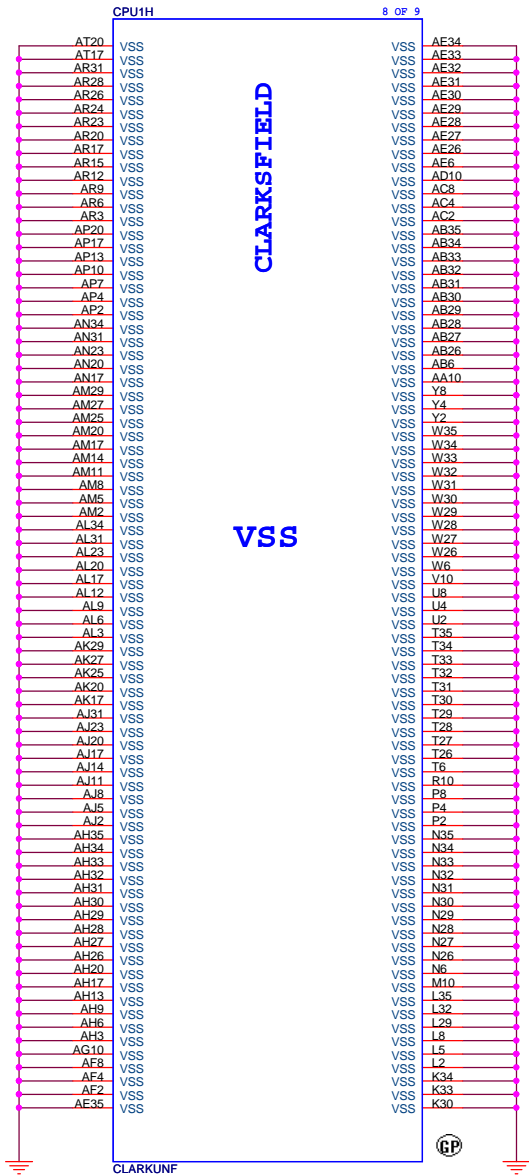
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksville VTT=1.1V

2ND = 62.10055.321
62.10053.561



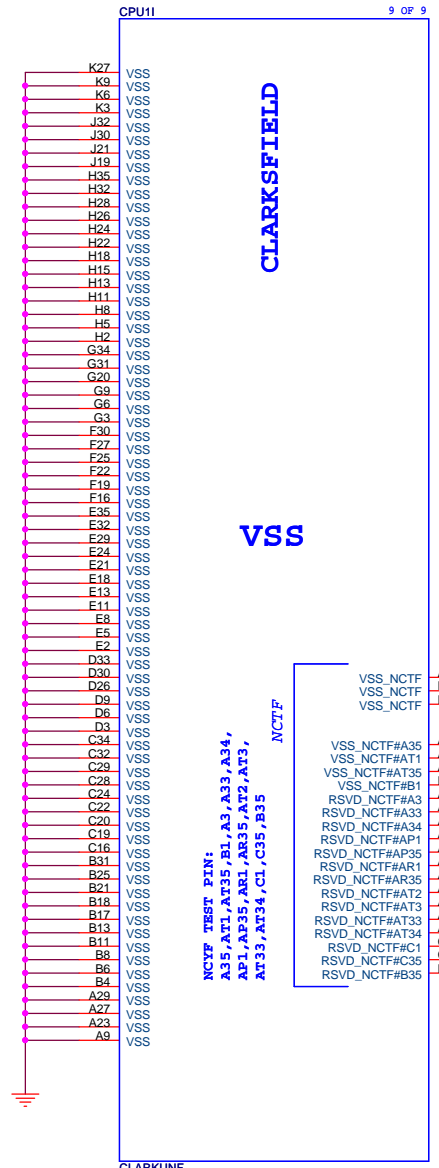
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

2ND = 62.10055.321
62.10053.561



2ND = 62.10055.321

62.10053.561



2ND = 62.10055.321

62.10053.61

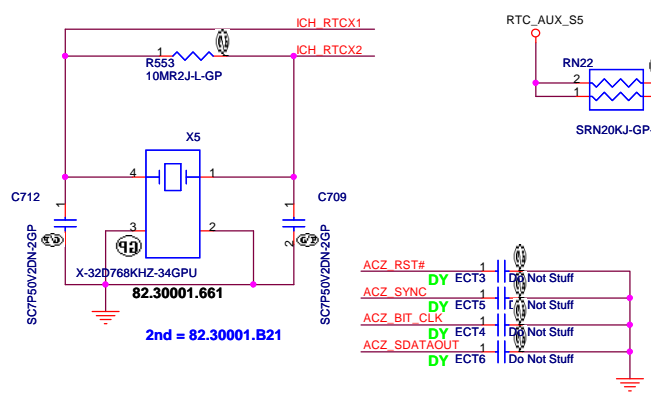
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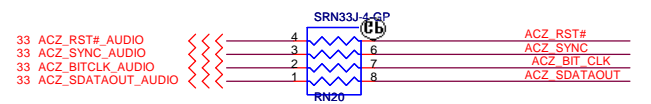
Title: **CPU (6/7)**

Size A3	Document Number JE70-CP	Rev -1M
Date: Tuesday, February 02, 2010	Sheet 9 of 67	

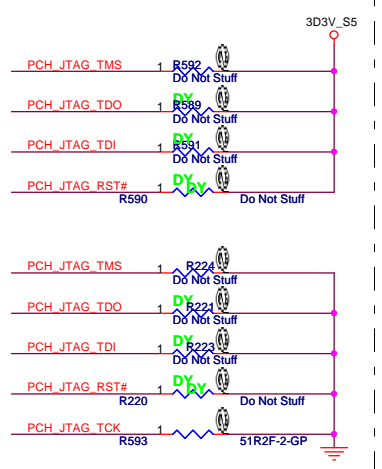
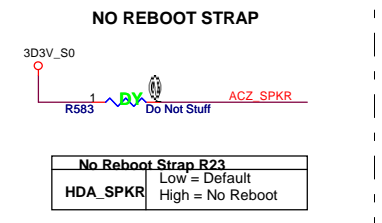


INTVRMEN- Integrated SUS
1.1V VRM Enable
High - Enable internal VRs

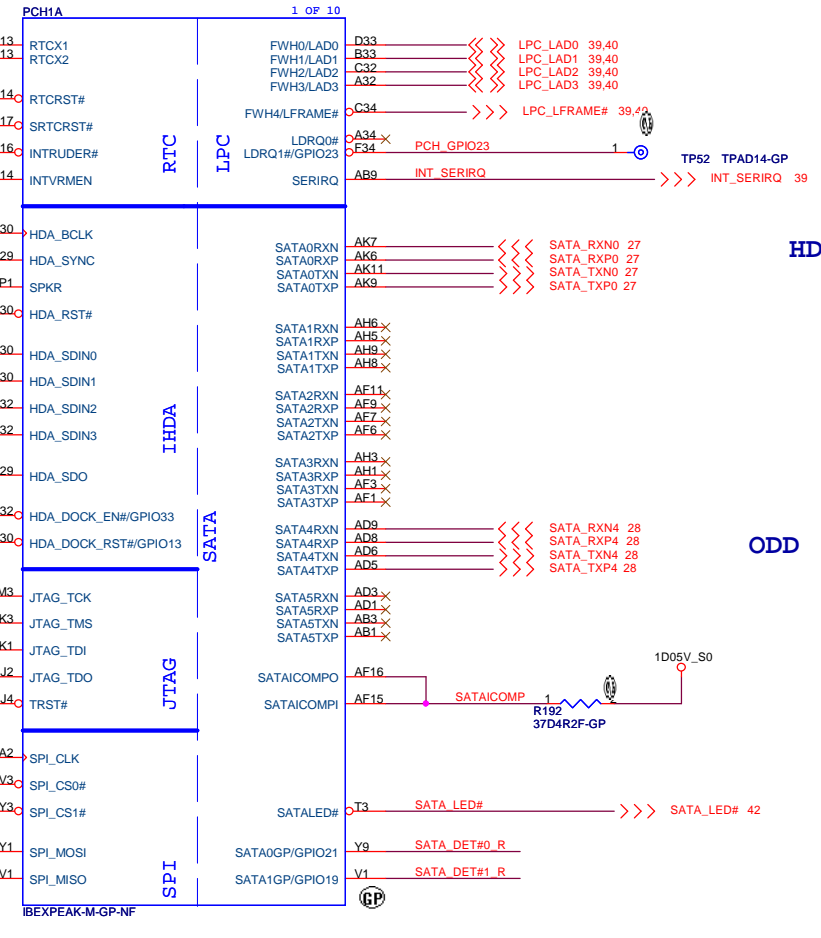
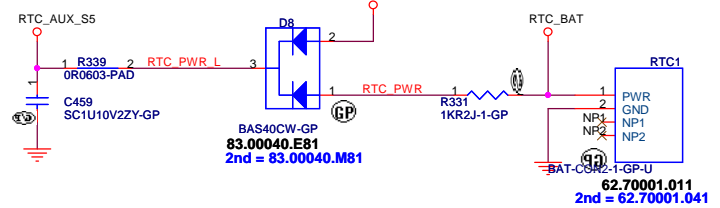
Integrated VccSusi_05, VccSusi_5, VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable



1D5V_S00 1 R549 ACZ_SYNC
Do Not Stuff
This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.

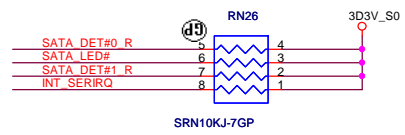


SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required



HDD

ODD



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Title: **PCH (1/9)**

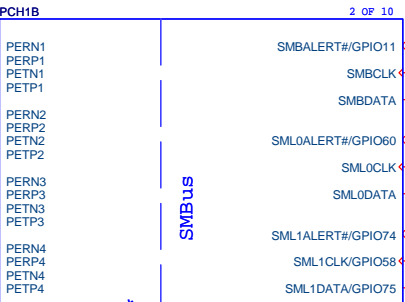
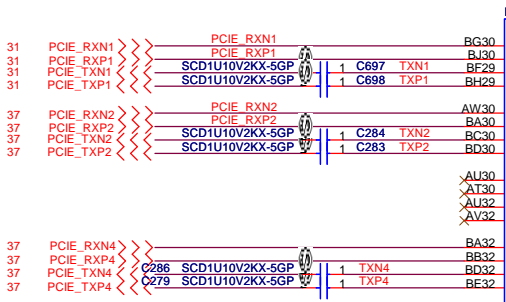
Size A3 Document Number: **JE70-CP** Rev: **-1M**

Date: Tuesday, February 02, 2010 Sheet 11 of 67

LAN

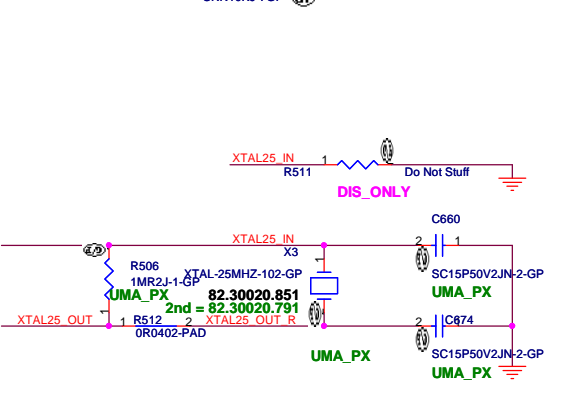
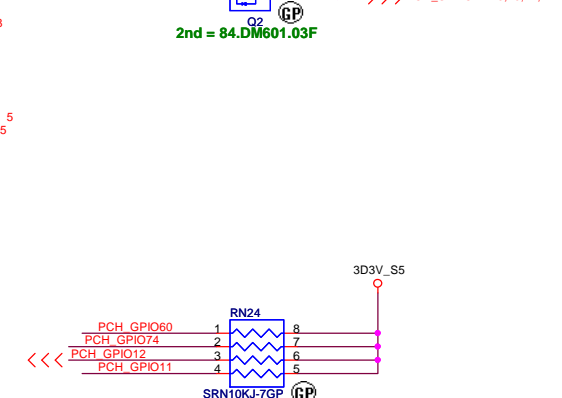
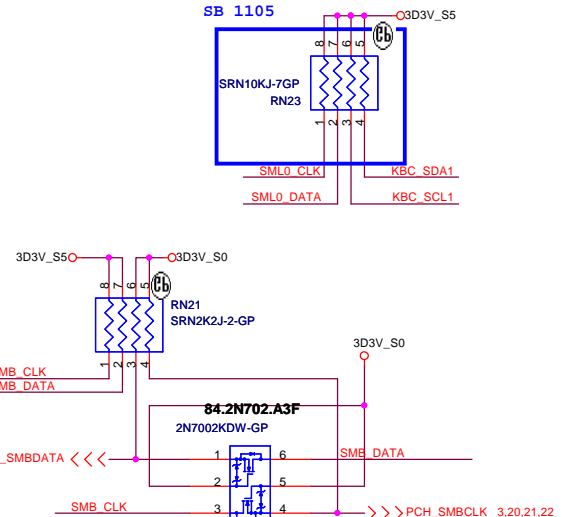
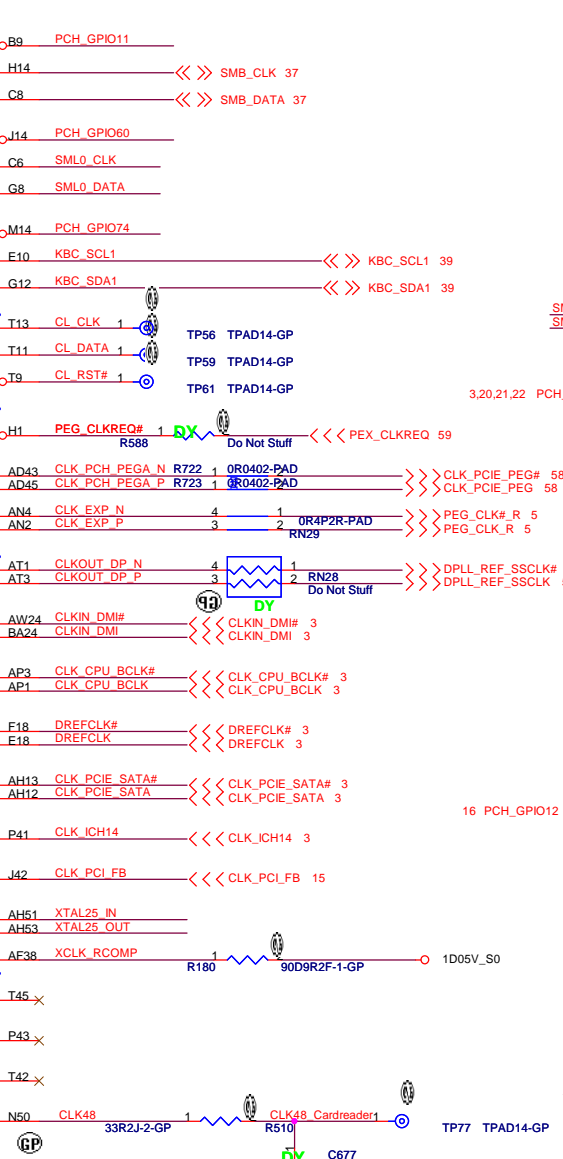
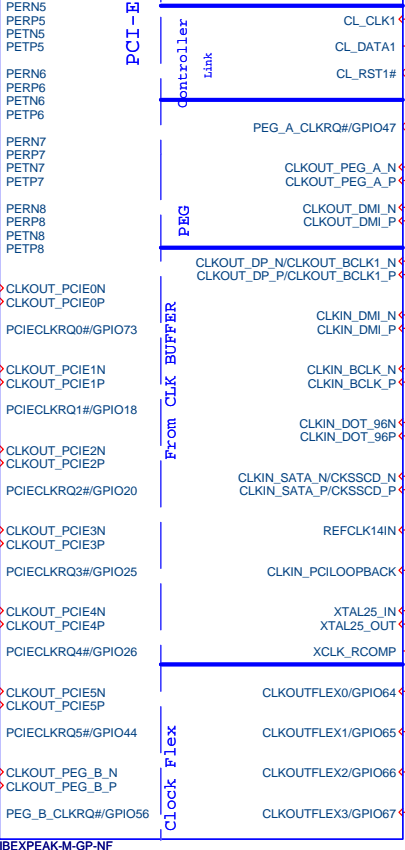
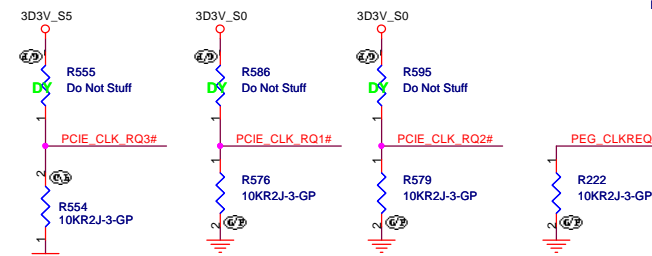
MINICARD1

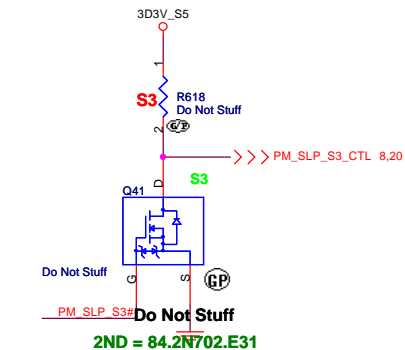
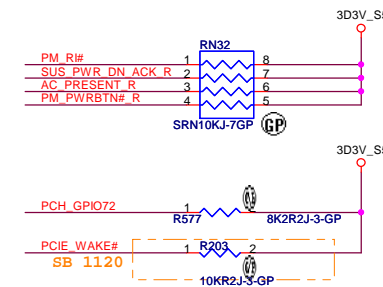
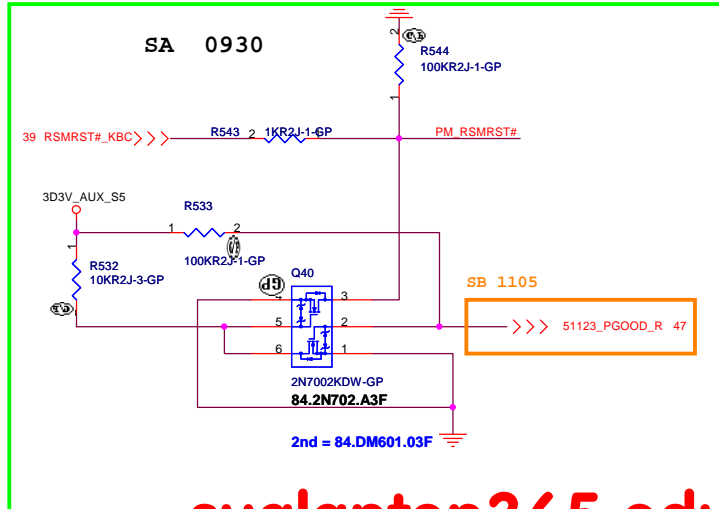
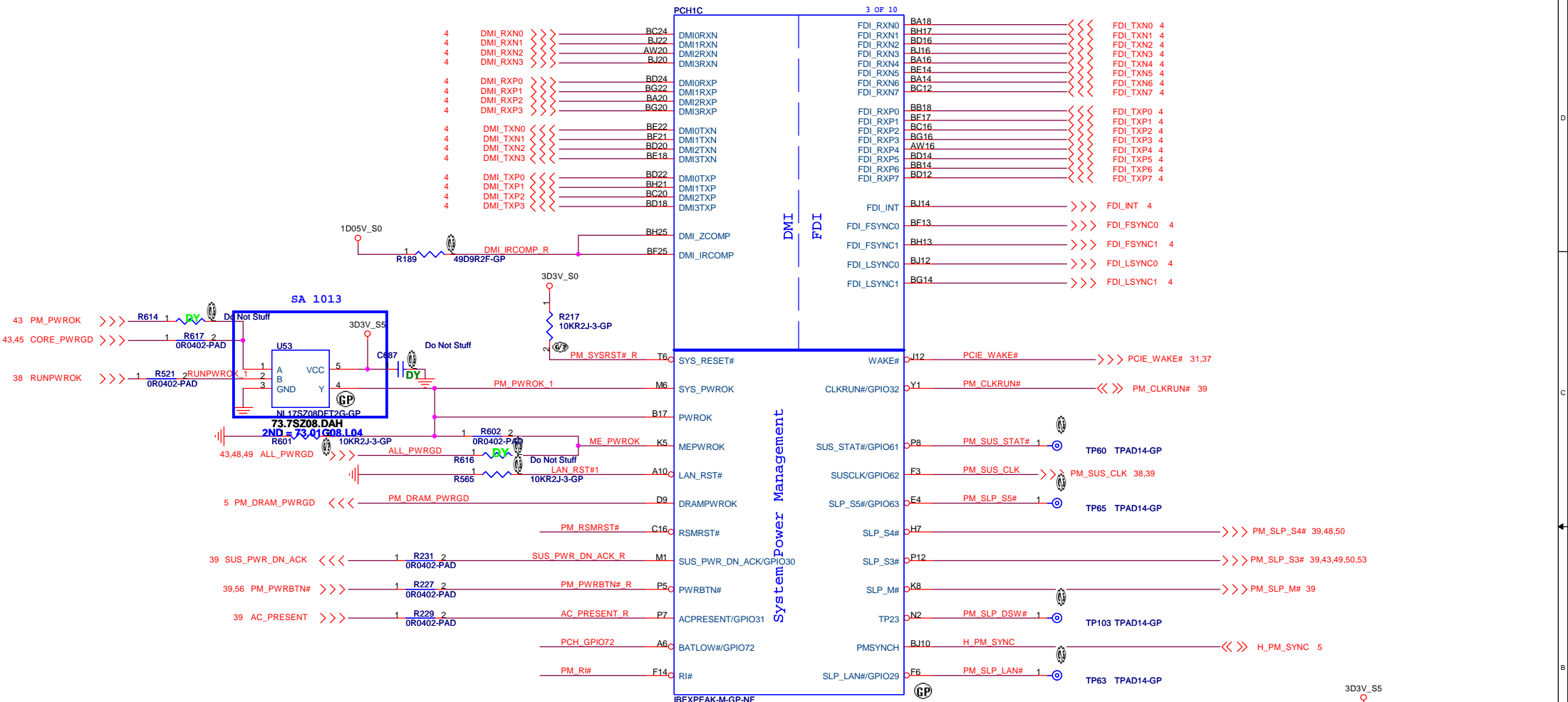
MINICARD2



PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).





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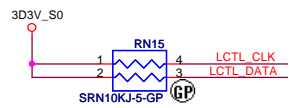
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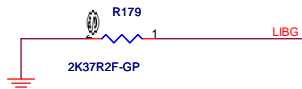
Title: **PCH (3/9)**

Size A3 Document Number **JE70-CP** Rev **-1M**

Date: Tuesday, February 02, 2010 Sheet 13 of 67



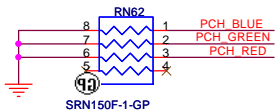
UMA_PX



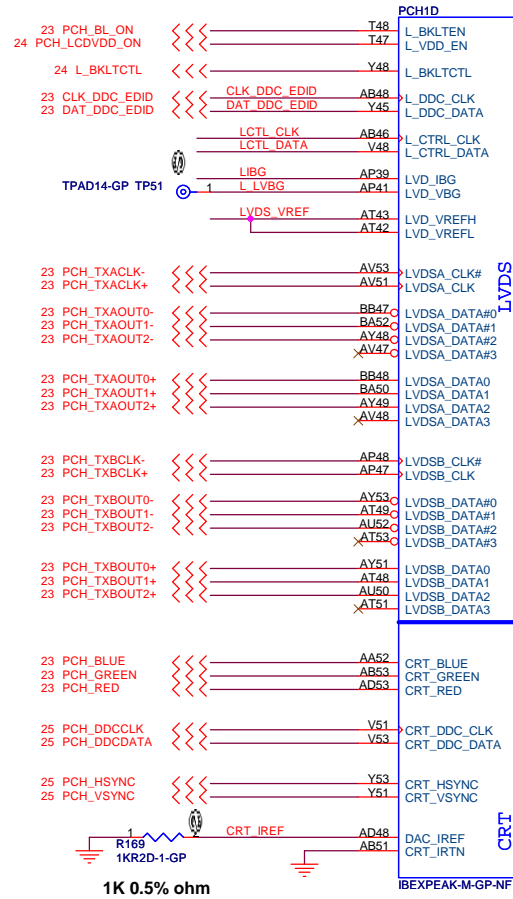
UMA_PX



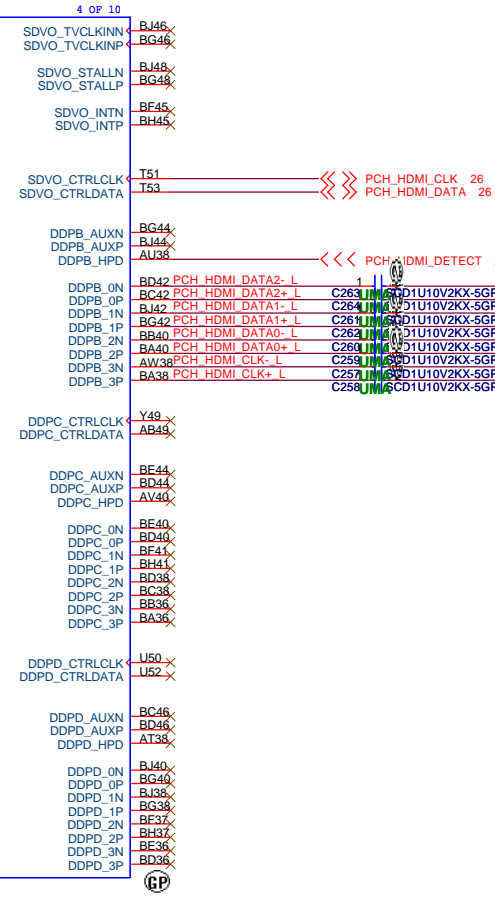
UMA_PX

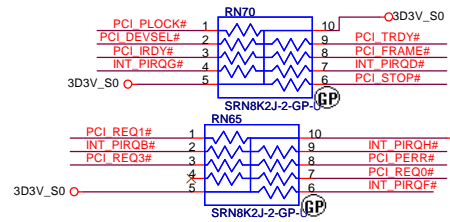


UMA_PX

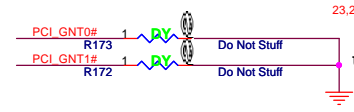
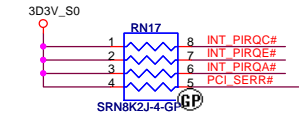


Digital Display Interface

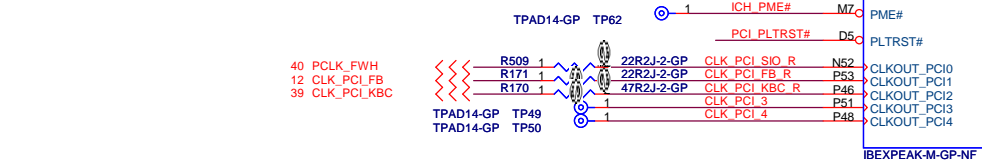




These pins are left as NC, because the function is disable.



PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI



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- H40 AD0
- N34 AD1
- C44 AD2
- A38 AD3
- C36 AD4
- J34 AD5
- A40 AD6
- D45 AD7
- E36 AD8
- H48 AD9
- E40 AD10
- C40 AD11
- M48 AD12
- M45 AD13
- M40 AD14
- M43 AD15
- J36 AD16
- K48 AD17
- F40 AD18
- C42 AD19
- K46 AD20
- M51 AD21
- J52 AD22
- K51 AD23
- L34 AD24
- E42 AD25
- J40 AD26
- G46 AD27
- F44 AD28
- M47 AD29
- H36 AD30
- AD31
- J50 C/BE0#
- G42 C/BE1#
- H47 C/BE2#
- G34 C/BE3#
- G38 PIRQA#
- H51 PIRQB#
- B37 PIRQC#
- A44 PIRQD#
- F51 REQ0#
- A46 REQ1#/GPIO50
- M53 REQ2#/GPIO52
- M53 REQ3#/GPIO54
- F48 GNT0#
- K46 GNT1#/GPIO51
- F36 GNT2#/GPIO53
- H53 GNT3#/GPIO55
- B41 PIRQE#/GPIO2
- K53 PIRQF#/GPIO3
- A36 PIRQG#/GPIO4
- A48 PIRQH#/GPIO5
- K6 PCIRST#
- E44 SERR#
- E50 PERR#
- A42 PCI_IRDY#
- H44 PCI_DEVSEL#
- F46 PCI_FRAME#
- C46 PCI_PLOCK#
- D49 PCI_STOP#
- C48 PCI_TRDY#
- M7 ICH_PME#
- D5 PCI_PLTRST#
- N52 CLKOUT_PCI0
- P53 CLKOUT_PCI1
- P46 CLKOUT_PCI2
- P51 CLKOUT_PCI3
- P48 CLKOUT_PCI4

- 5 OF 10 NV_CE#0 AY9
- NV_CE#1 BD1
- NV_CE#2 AP15
- NV_CE#3 BDE
- NV_DQ#0 AV9
- NV_DQ#1 BGS
- NV_DQ0/NV_IO0 AP7
- NV_DQ1/NV_IO1 AP6
- NV_DQ2/NV_IO2 AT6
- NV_DQ3/NV_IO3 AT9
- NV_DQ4/NV_IO4 AV6
- NV_DQ5/NV_IO5 BB3
- NV_DQ6/NV_IO6 BA4
- NV_DQ7/NV_IO7 BE4
- NV_DQ8/NV_IO8 BE4
- NV_DQ9/NV_IO9 BB6
- NV_DQ10/NV_IO10 BD6
- NV_DQ11/NV_IO11 BB7
- NV_DQ12/NV_IO12 BC8
- NV_DQ13/NV_IO13 BJ8
- NV_DQ14/NV_IO14 BJ6
- NV_DQ15/NV_IO15 BG6
- NV_ALE BD3
- NV_CLE AY6
- NV_RCOMP AU2
- NV_RB# AV7
- NV_WR#0_RE# AY8
- NV_WR#1_RE# AY5
- NV_WE#_CK0 AV11
- NV_WE#_CK1 BE5
- H18 USBP#0
- J18 USBP#1
- A18 USBP#2
- C18 USBP#3
- M20 USBP#4
- F20 USBP#5
- J20 USBP#6
- L20 USBP#7
- F20 USBP#8
- G20 USBP#9
- A20 USBP#10
- C20 USBP#11
- M22 USBP#12
- N22 USBP#13
- B21 USBP#14
- D21 USBP#15
- H22 USBP#16
- J22 USBP#17
- F22 USBP#18
- A22 USBP#19
- C22 USBP#20
- G24 USBP#21
- H24 USBP#22
- L24 USBP#23
- M24 USBP#24
- A24 USBP#25
- C24 USBP#26
- B25 USBRBIAS#
- D25 USBRBIAS
- N16 USB_OC#0
- J16 USB_OC#1
- F16 USB_OC#2
- E16 USB_OC#3
- G16 USB_OC#4
- F12 USB_OC#4
- T15

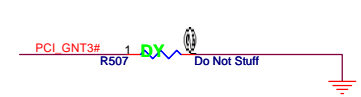
These pins are left as NC, because the function is disable.

DMI Termination Voltage
 NV_CLE Set to Vss when low.
 Set to Vcc when high.

Danbury Technology:
 Disabled when Low.
 Enable when High.

USB

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	NC
6	NC
7	NC
8	NC
9	USB1(HS)
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader



A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default
-----------	---

Pre UMA

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Title: **PCH (5/9)**

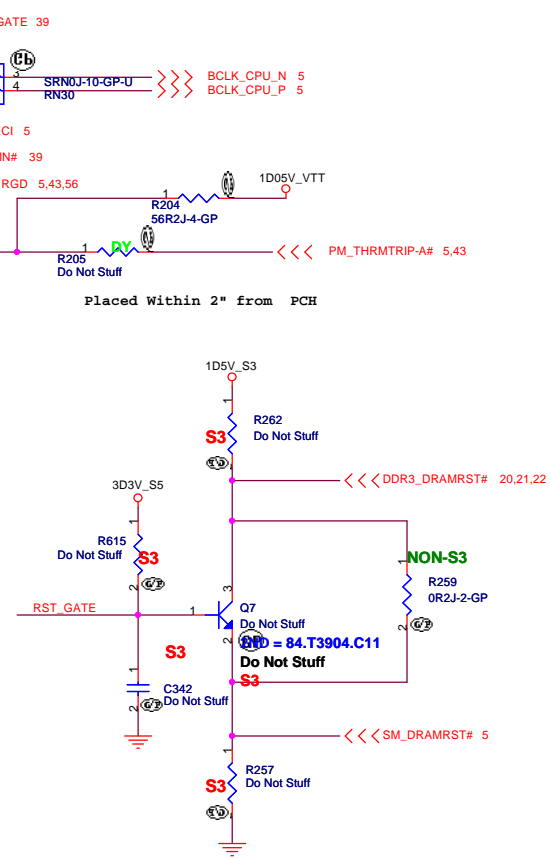
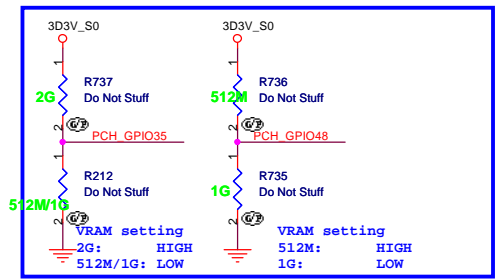
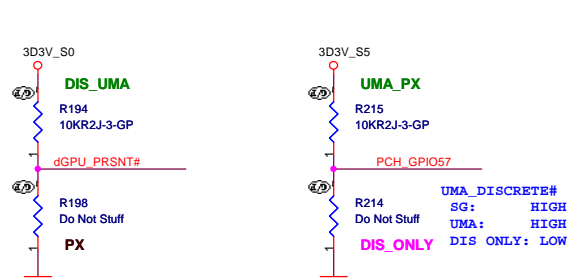
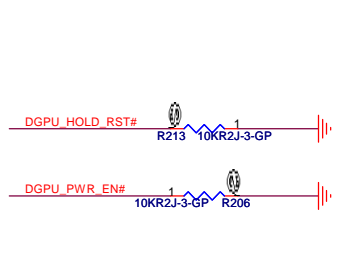
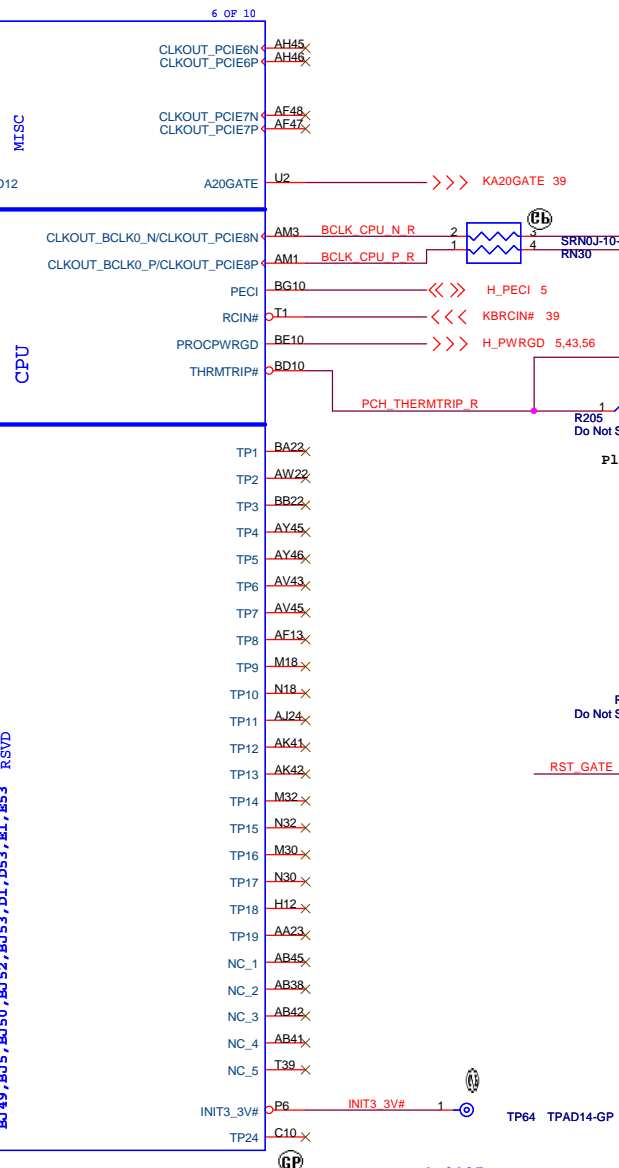
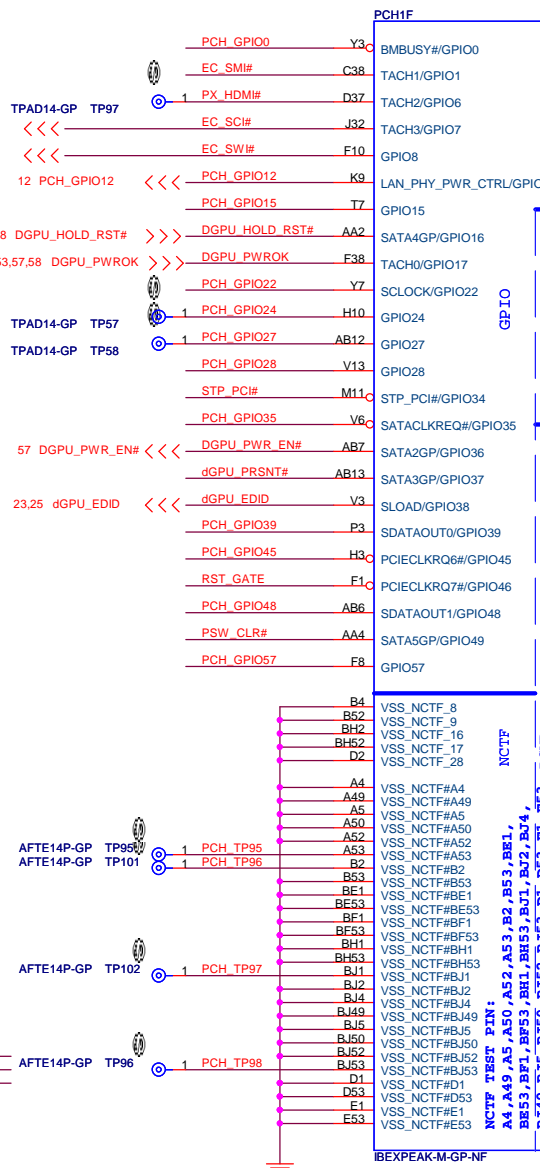
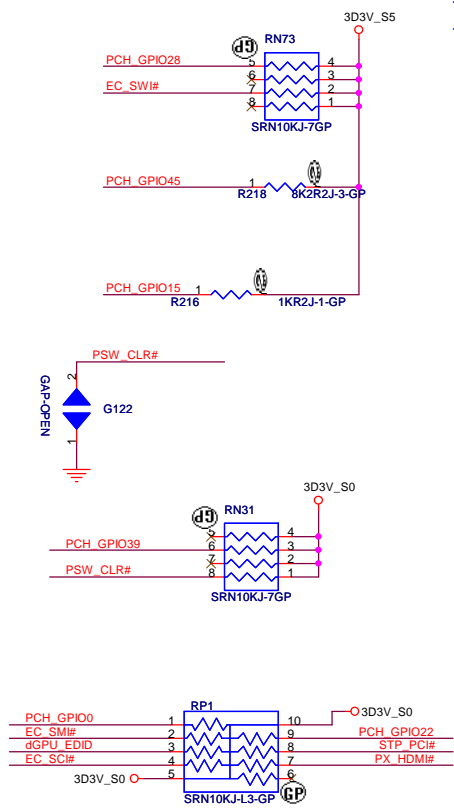
Size A3 | Document Number: **JE70-CP** | Rev: **-1M**

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GPIO8 has a weak[20K] internal pull up.
No need to have external pull up/down.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



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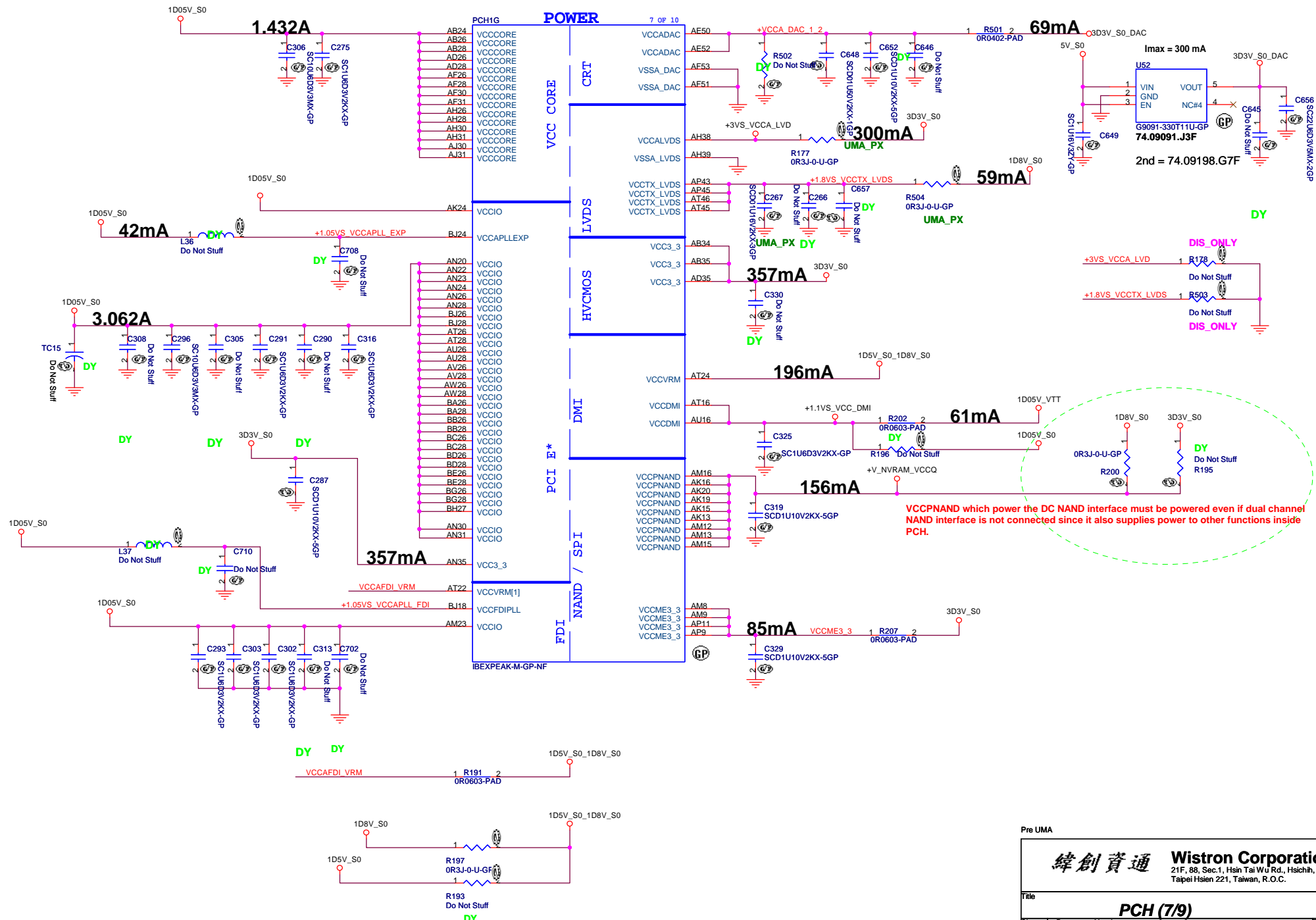
Pre UMA

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Title: **PCH (6/9)**

Size A3 Document Number **JE70-CP** Rev **-1M**

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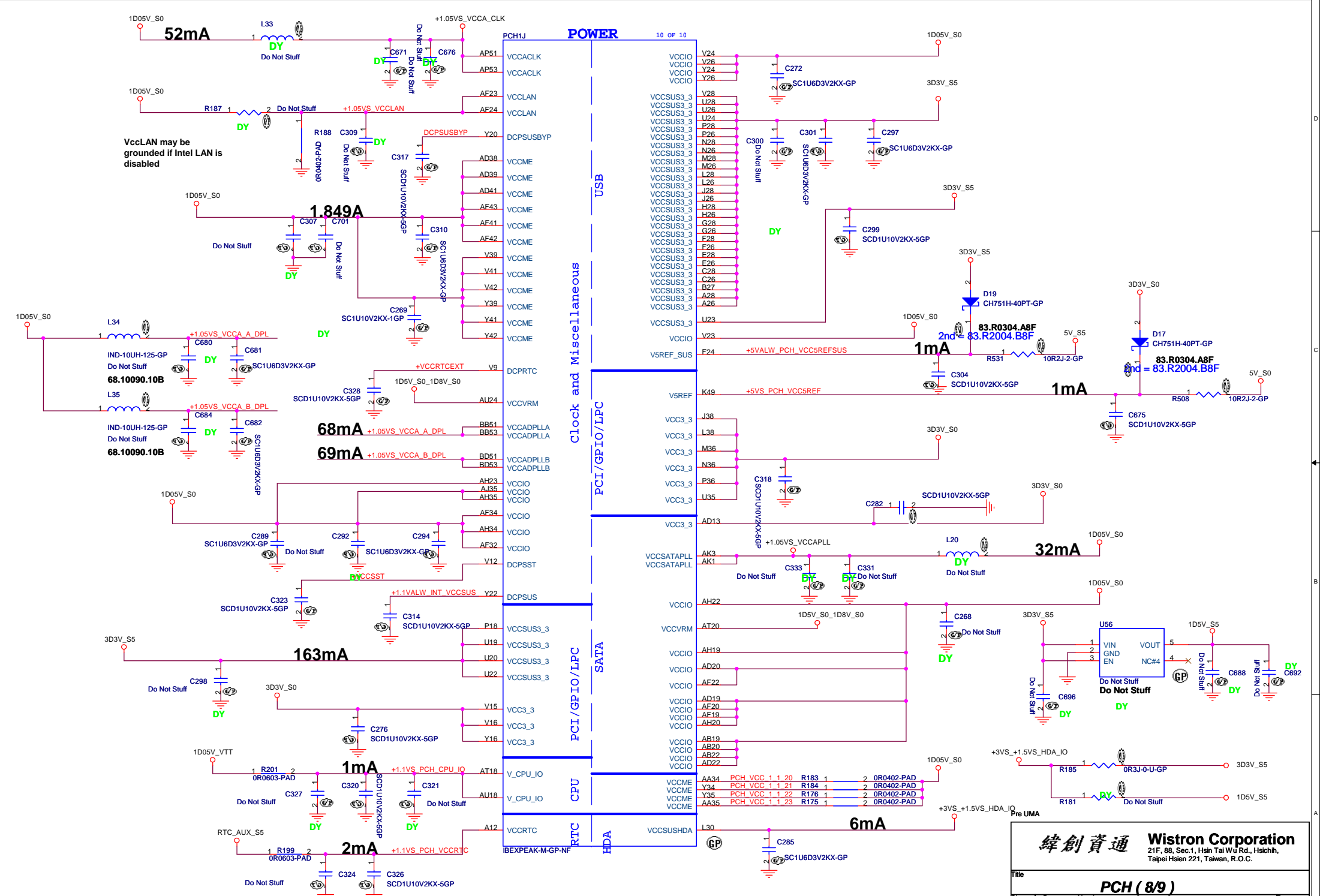
Pre UMA

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Title: **PCH (7/9)**

Size A3 Document Number **JE70-CP** Rev **-1M**

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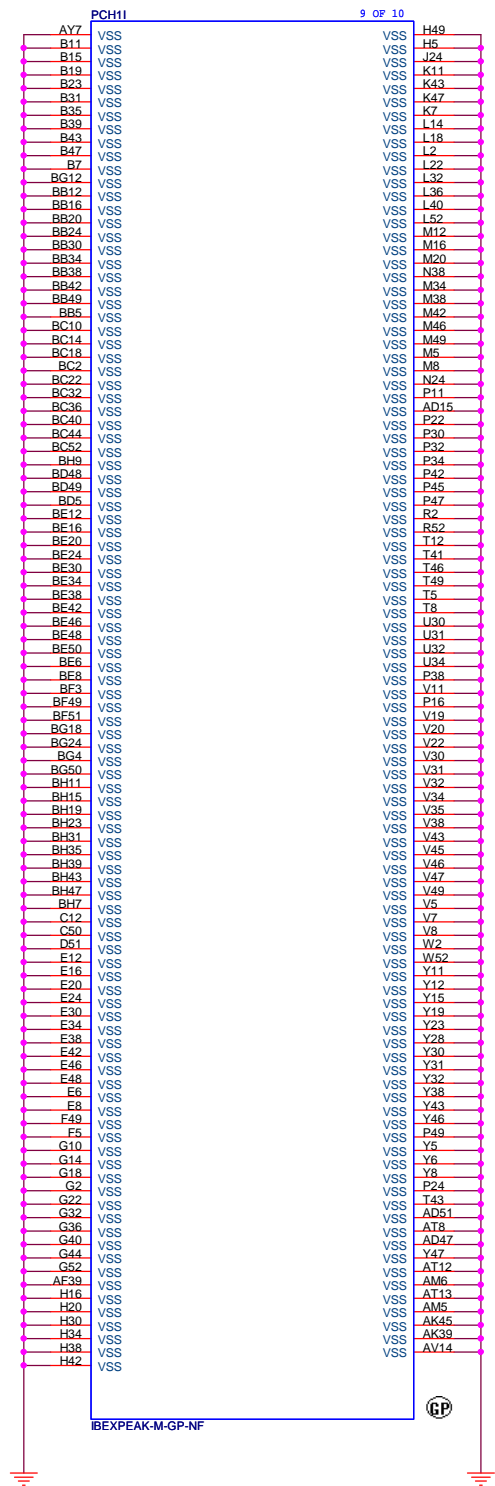
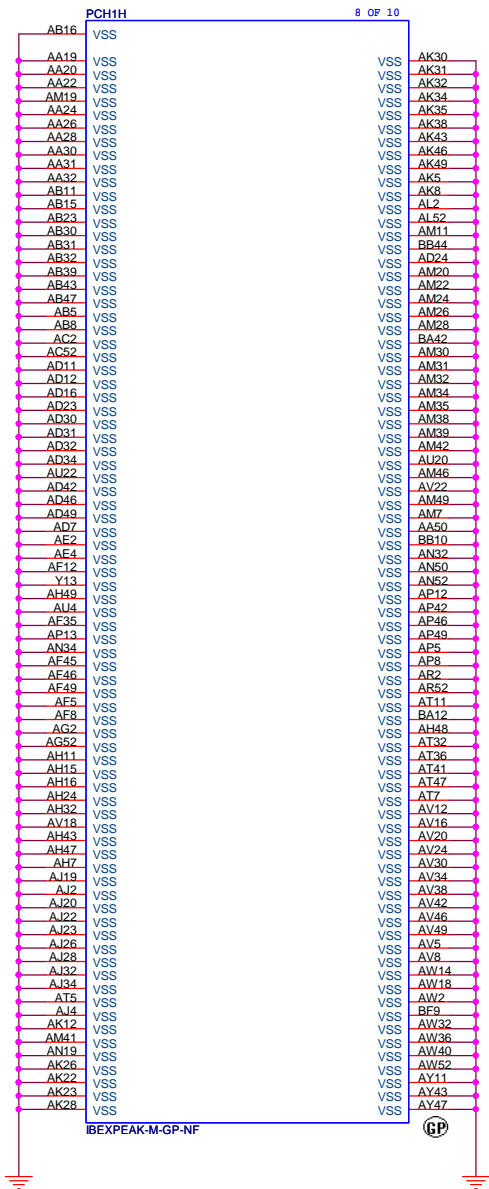
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Title: **PCH (8/9)**

Size A3 Document Number **JE70-CP** Rev **-1M**

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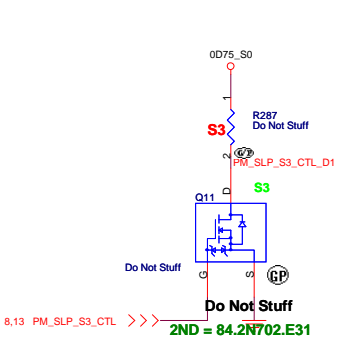
Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

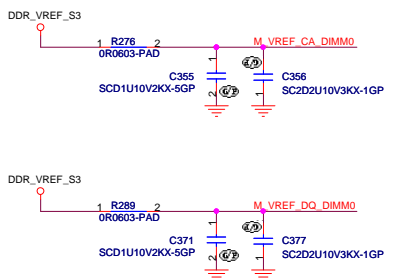
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Size A3 Document Number **JE70-CP** Rev **-1M**

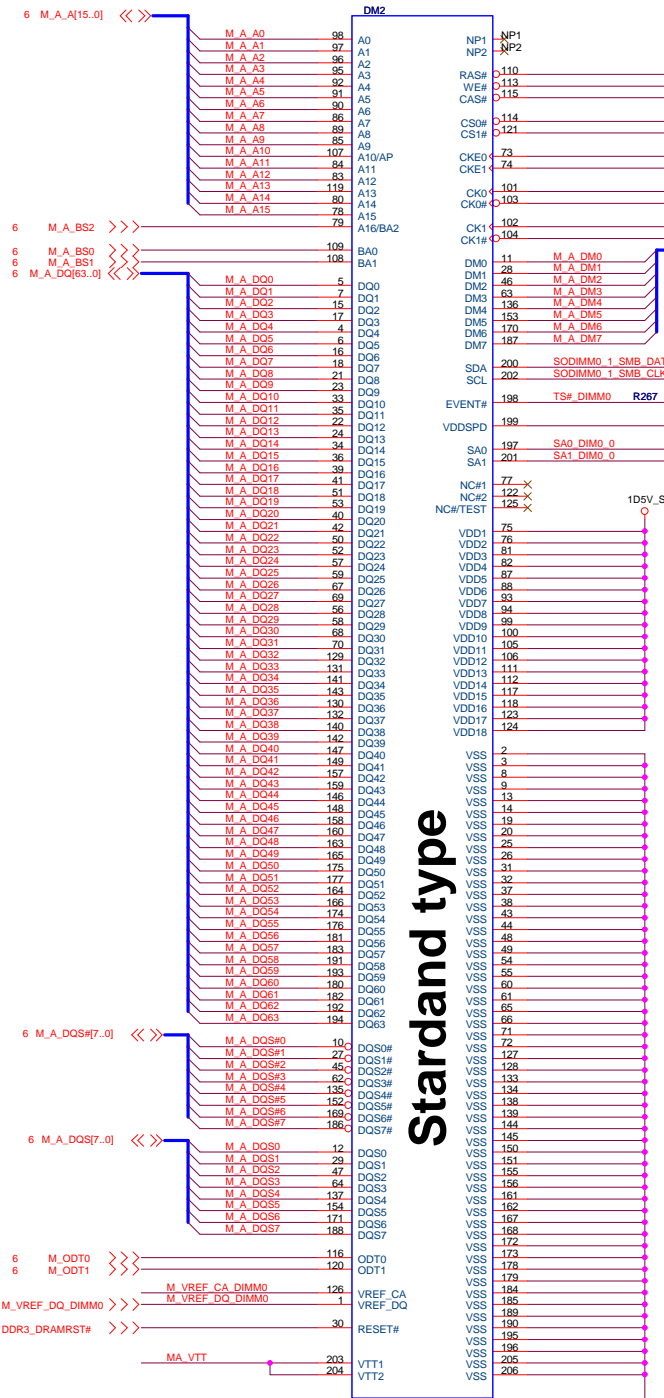
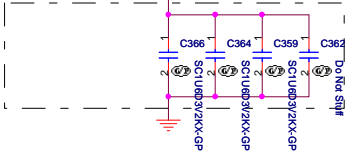
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8.13 PM_SLP_S3_CTL >>> 2ND = 84.2N702.E31

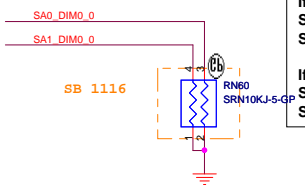


Place these caps close to VTT1 and VTT2.



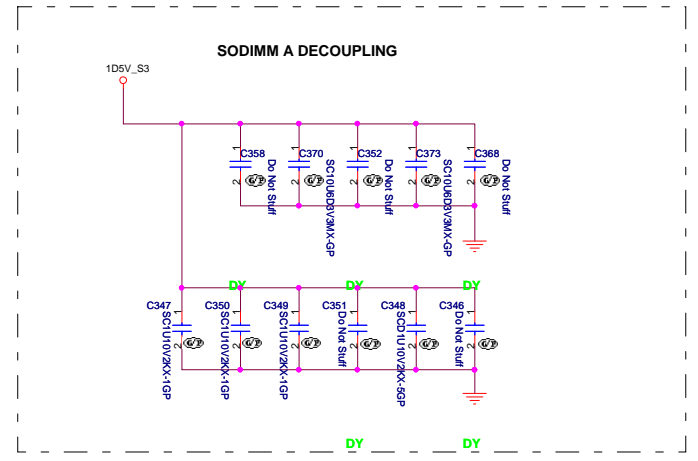
H = 4mm
DDR3-204P-99-GP
62.10017.W01
2nd = 62.10017.V31

Layout Note:
Place these Caps near SO-DIMMA.



Note:
If SA0_DIMM0 = 0, SA1_DIMM0 = 0
SO-DIMMA SPD Address is 0x0A0
SO-DIMMA TS Address is 0x30

If SA0_DIMM0 = 1, SA1_DIMM0 = 0
SO-DIMMA SPD Address is 0x0A2
SO-DIMMA TS Address is 0x32



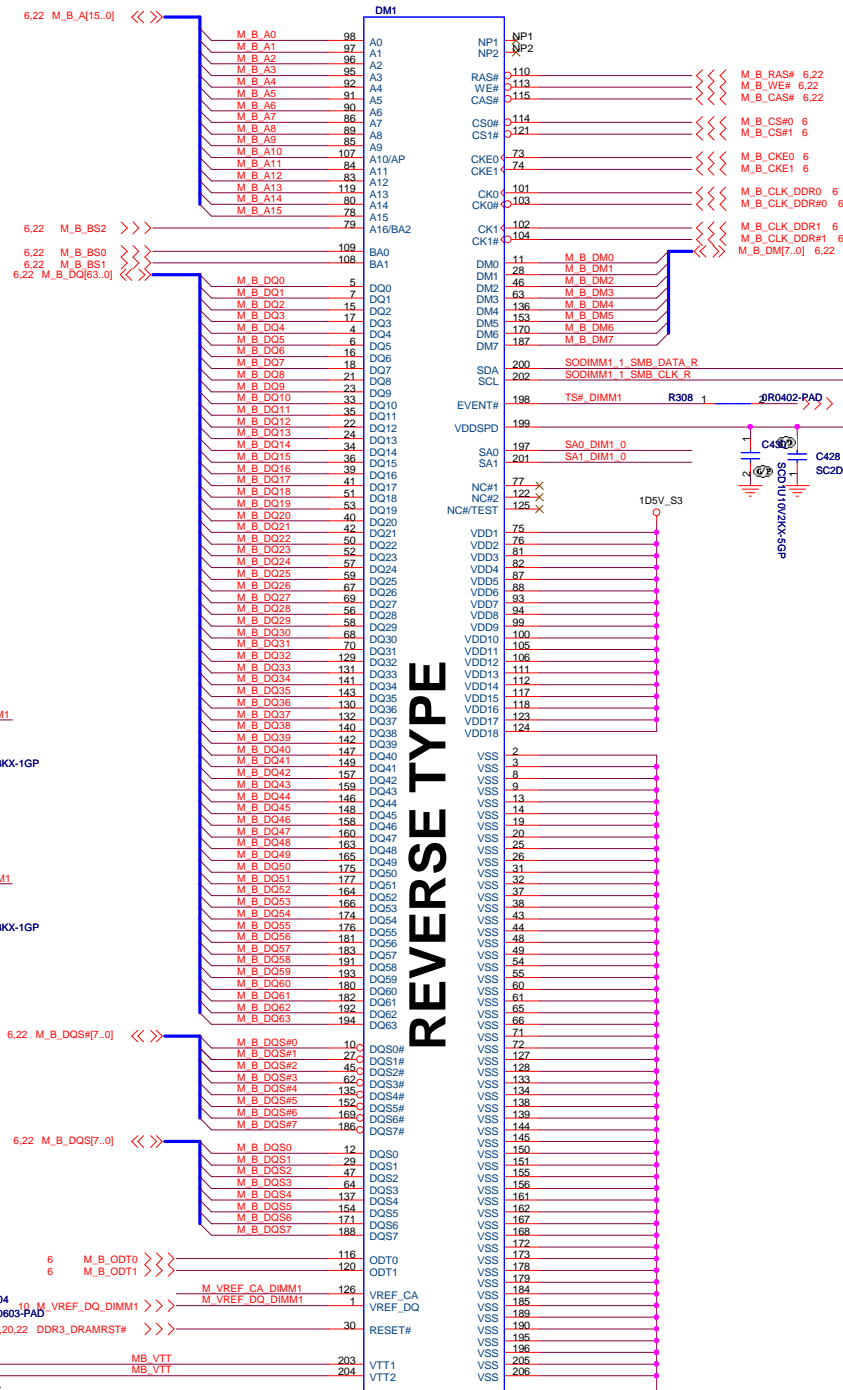
Pro UMA

緯創資通 Wistron Corporation
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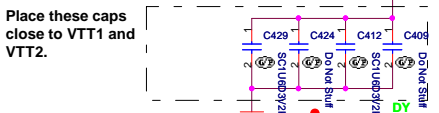
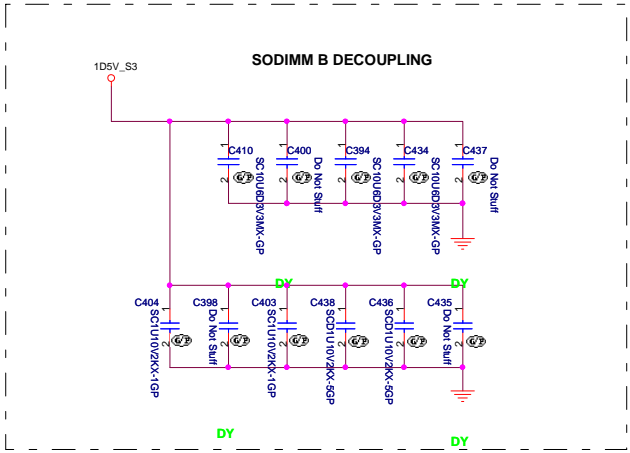
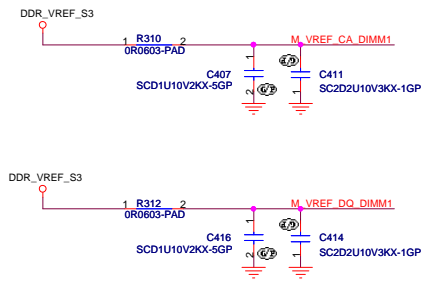
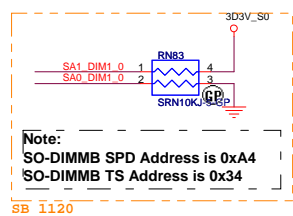
Title: **DDRIII Socket DM1**

Size: Custom Document Number: **JE70-CP** Rev: **-1M**

Date: Tuesday, February 02, 2010 Sheet 20 of 67



REVERSE TYPE



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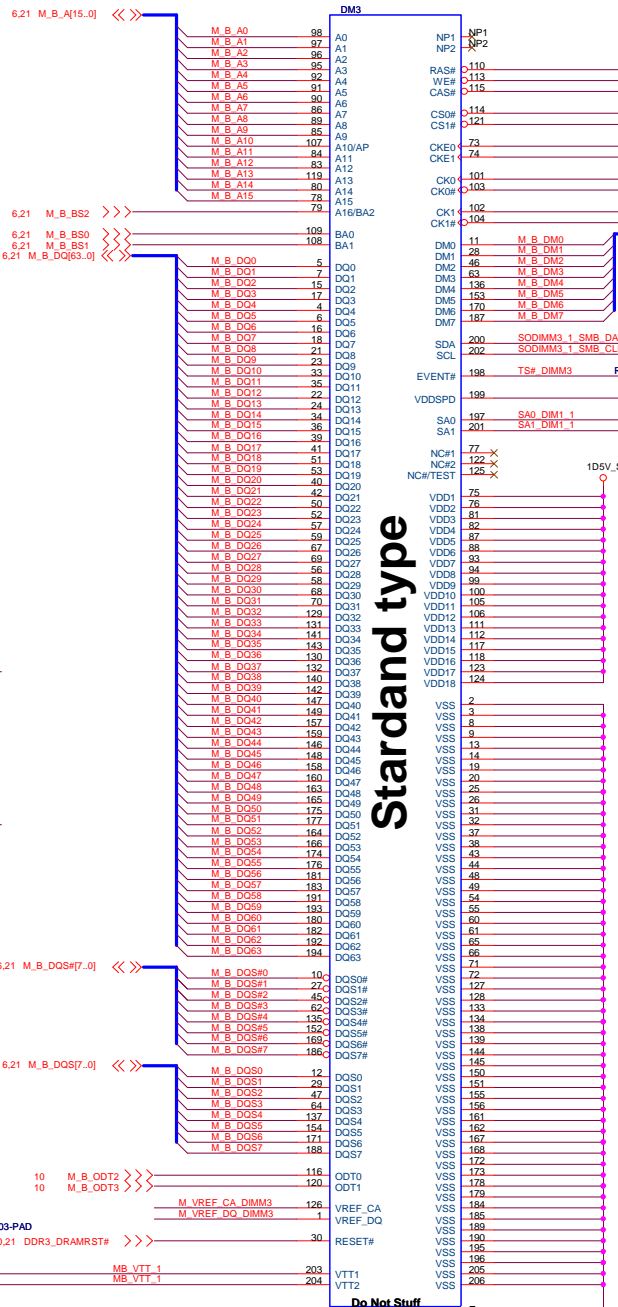
Pre UMA

緯創資通 Wistron Corporation
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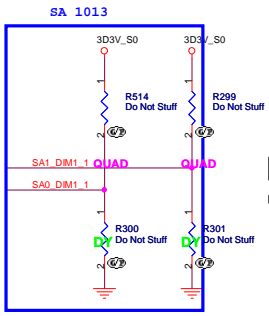
Title: **DDRIII Socket DM2**

Size: Custom Document Number: **JE70-CP** Rev: **-1M**

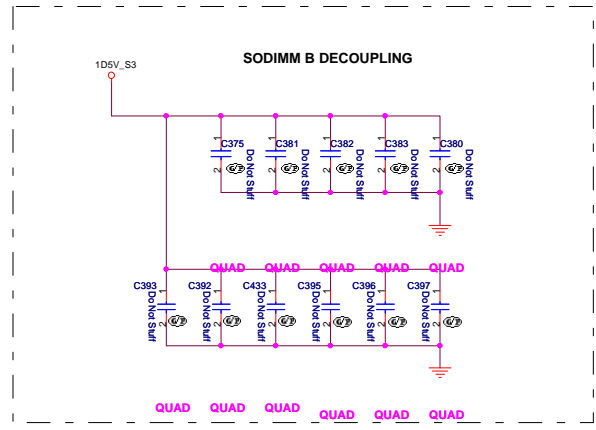
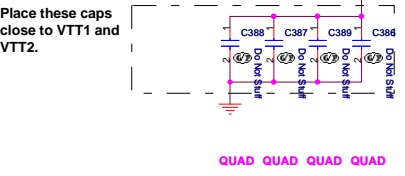
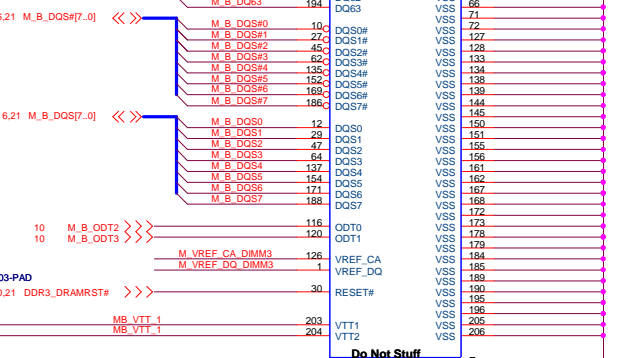
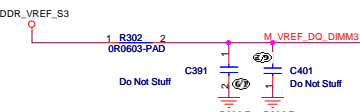
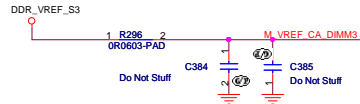
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Stardand type



Note:
SO-DIMMB SPD Address is 0xA6
SO-DIMMB TS Address is 0x36

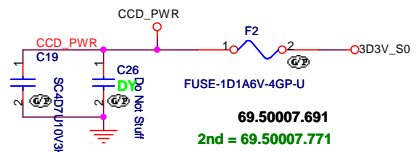
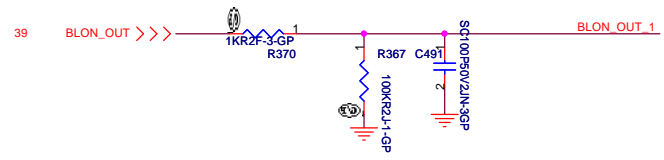
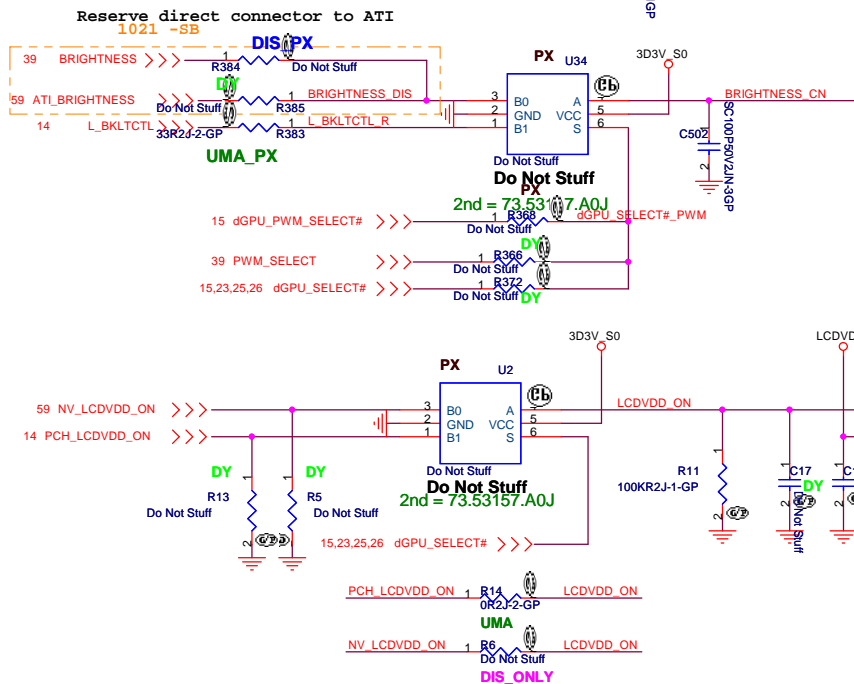
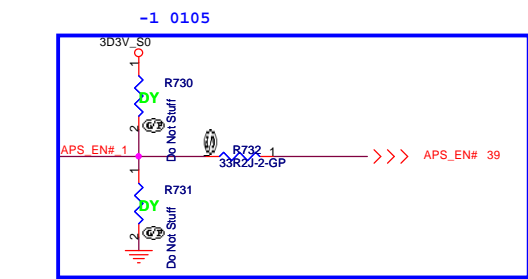
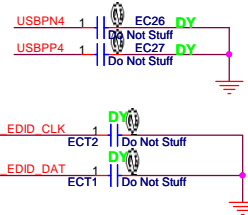
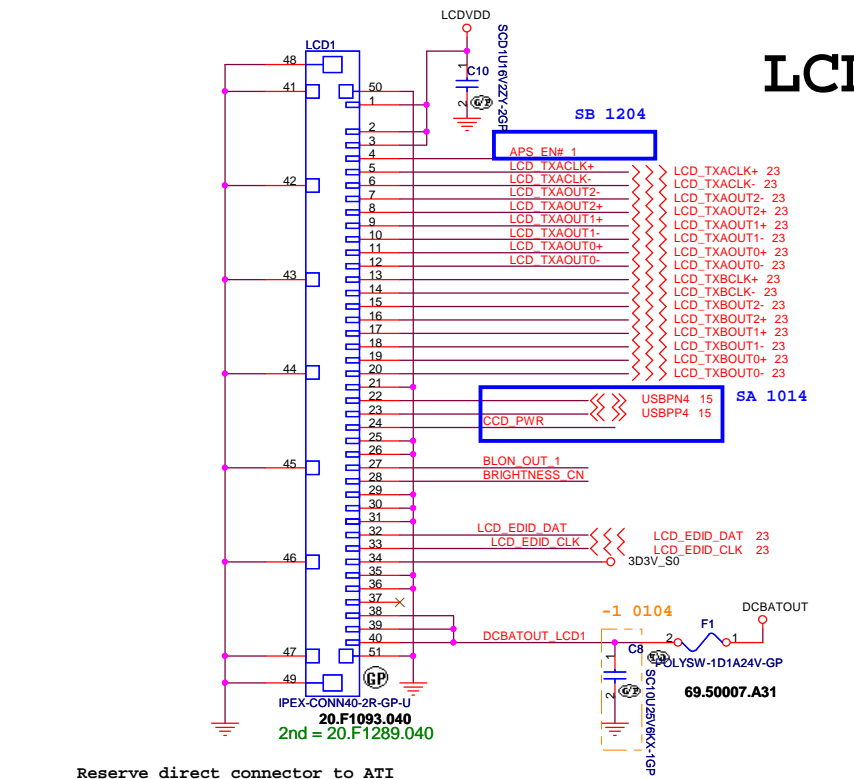


H = 8mm

Do Not Stuff
2nd =

QUAD

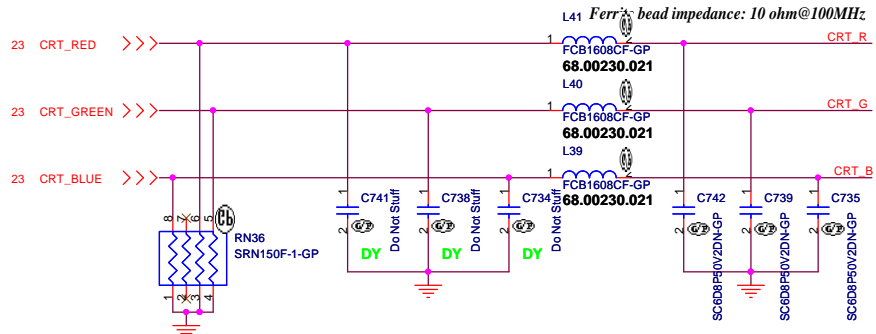
LCD/INVERTER/CCD CONN



Pre UMA

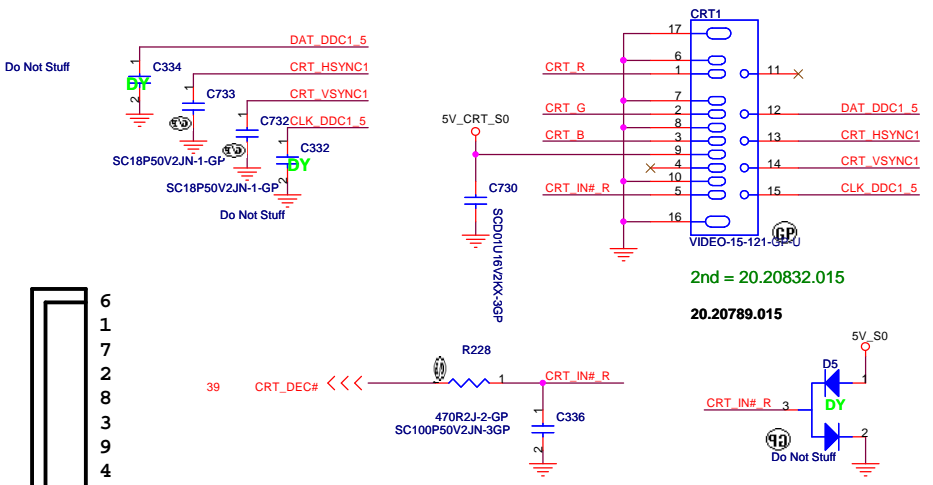
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
LCD CONN			
File			
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		Rev	-1M

Layout Note:
Place these resistors close to the CRT-out connector



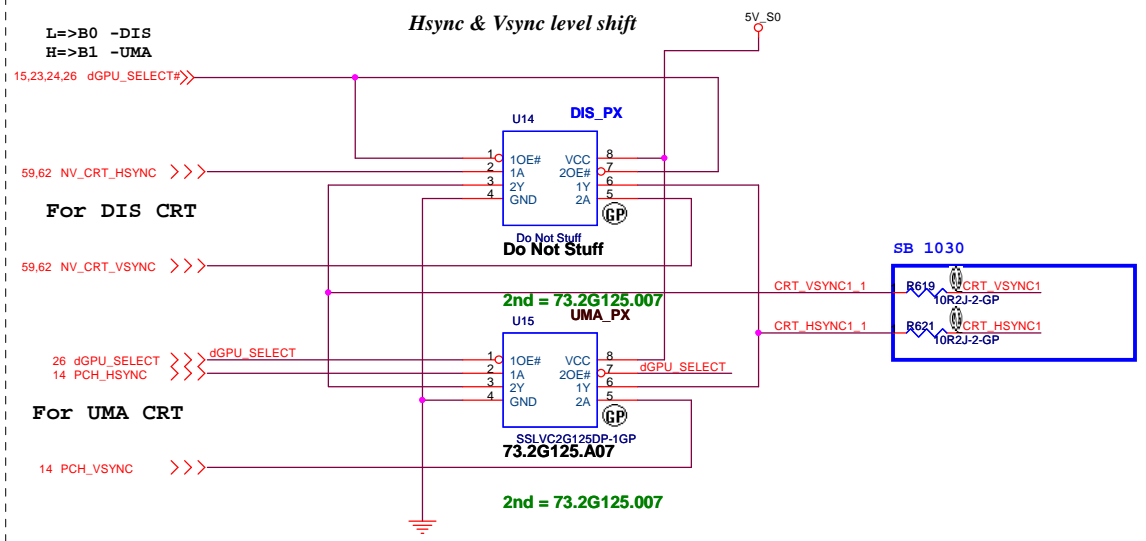
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

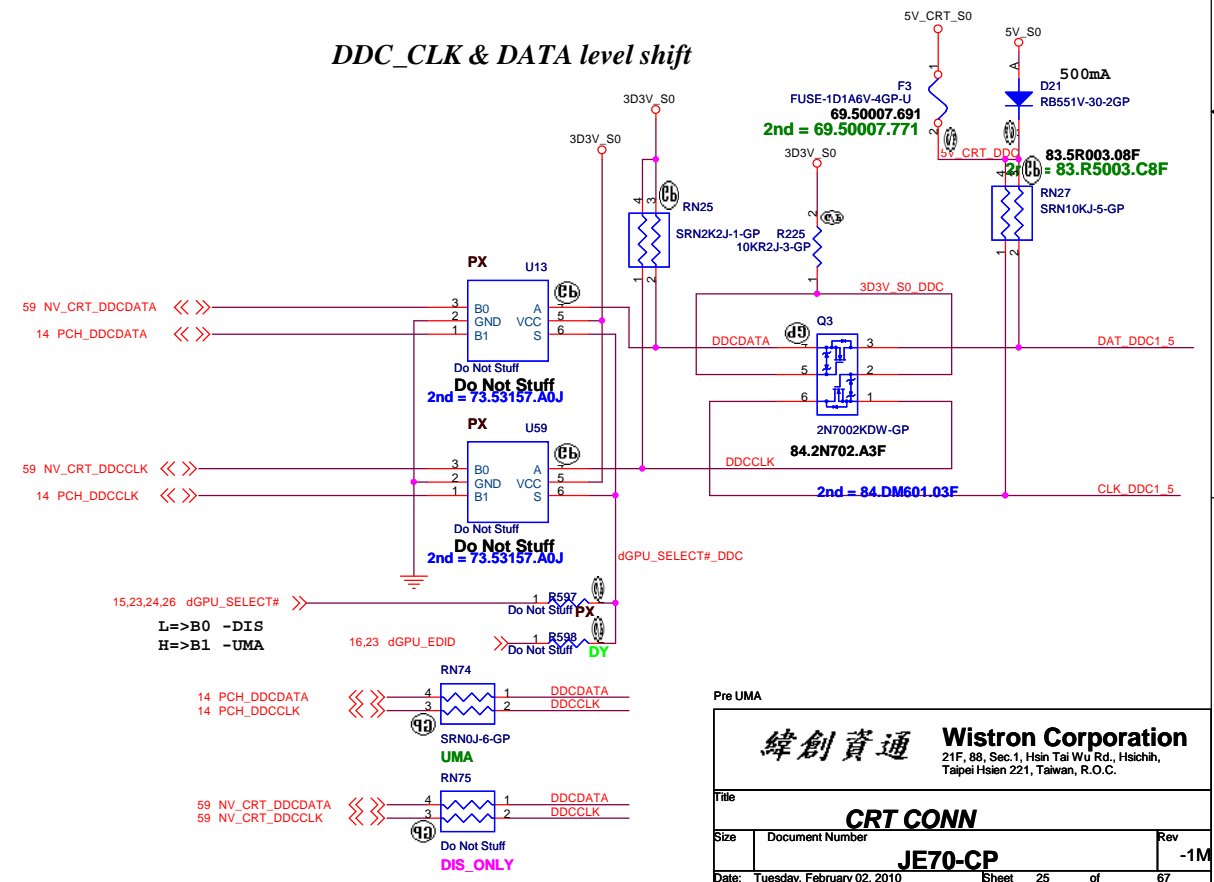


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Hsync & Vsync level shift



DDC_CLK & DATA level shift



Pre UMA

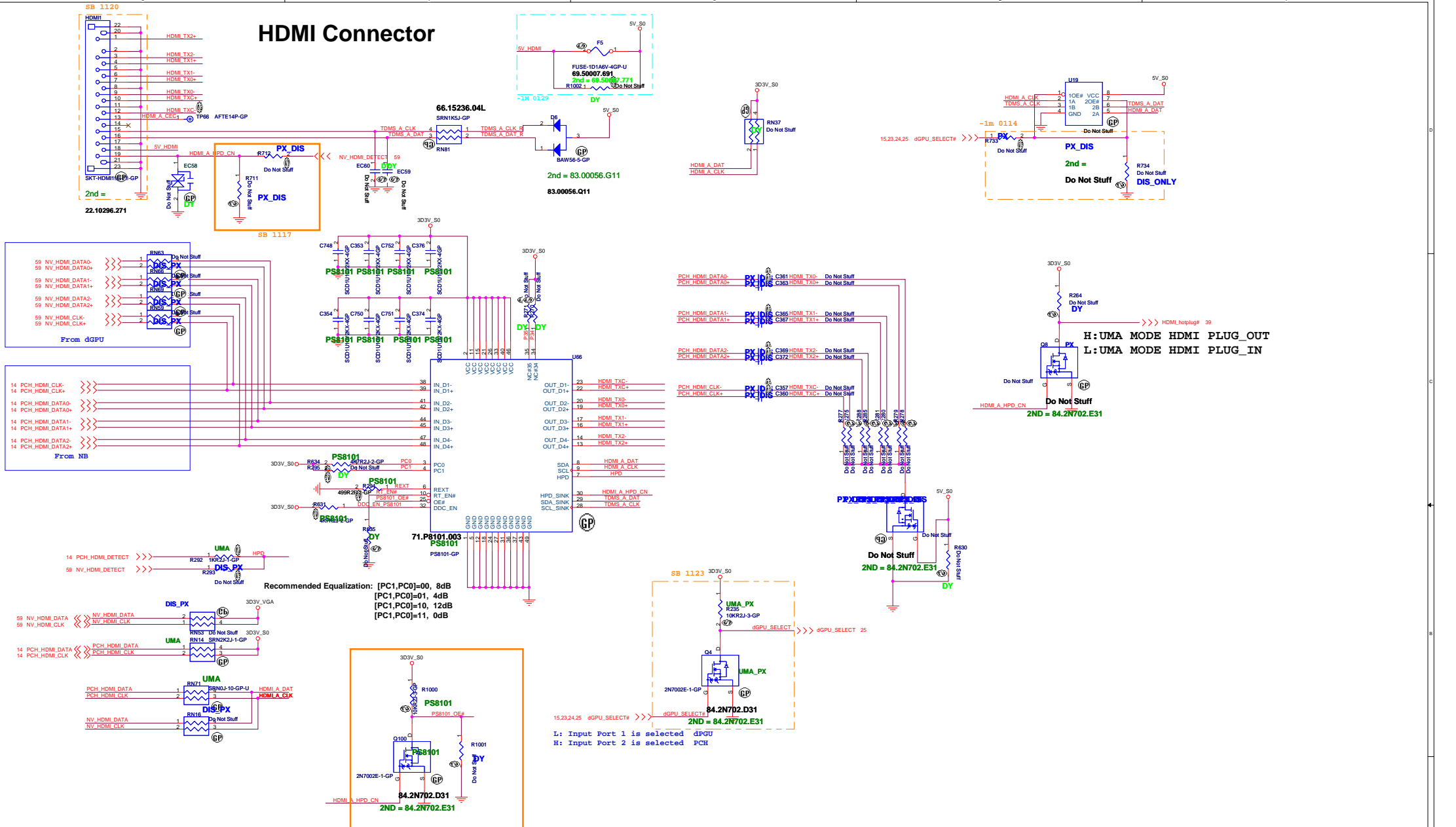
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT CONN**

Size: Document Number: **JE70-CP** Rev: **-1M**

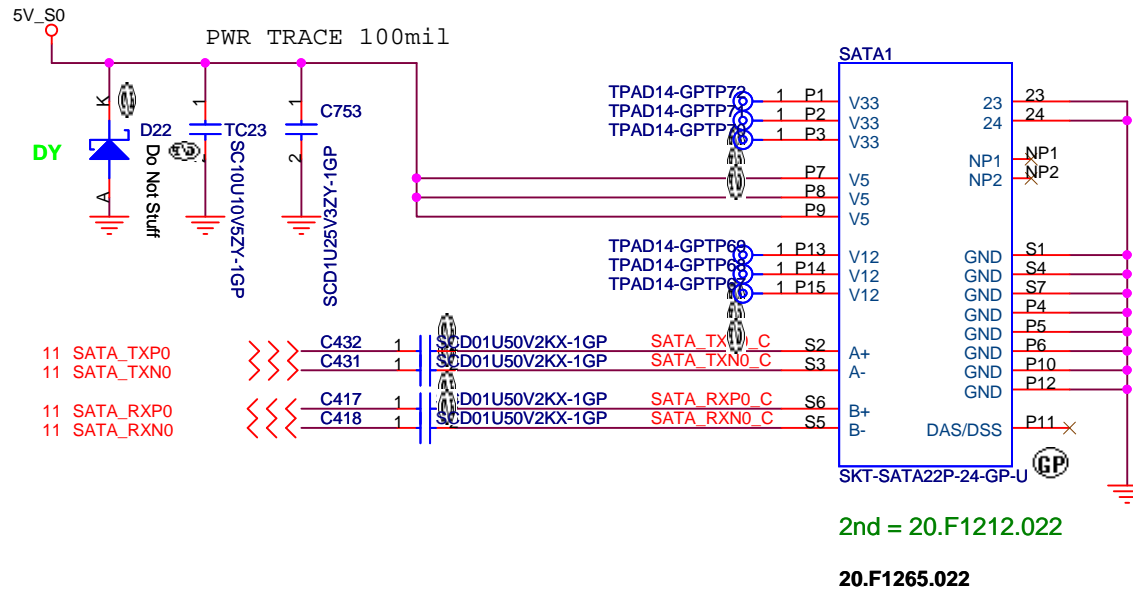
Date: Tuesday, February 02, 2010 Sheet 25 of 67

HDMI Connector

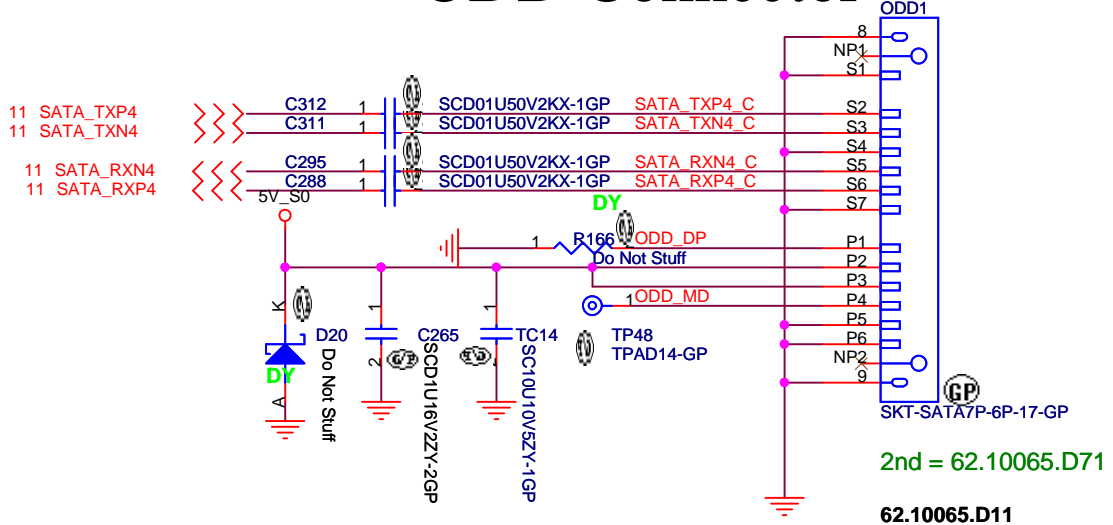


Recommended Equalization: [PC1,PC0]=0, 8dB
 [PC1,PC0]=01, 4dB
 [PC1,PC0]=10, 12dB
 [PC1,PC0]=11, 0dB

SATA Connector

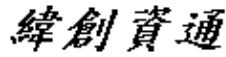


ODD Connector

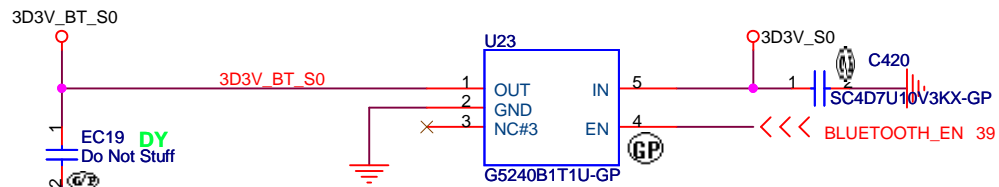


2nd = 62.10065.D71
62.10065.D11

Pre UMA

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
ODD	
Size	Document Number
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Date:	Tuesday, February 02, 2010
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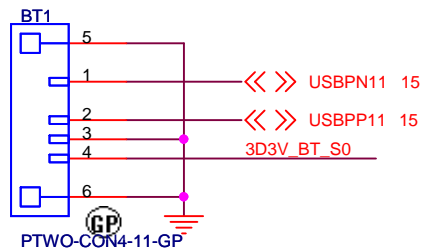
BLUETOOTH MODULE



74.05240.A7F

2nd = 74.09711.A7F

EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



20.F1561.004

2nd = 20.F1621.004

Pre UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

BLUETOOTH

Size

Document Number

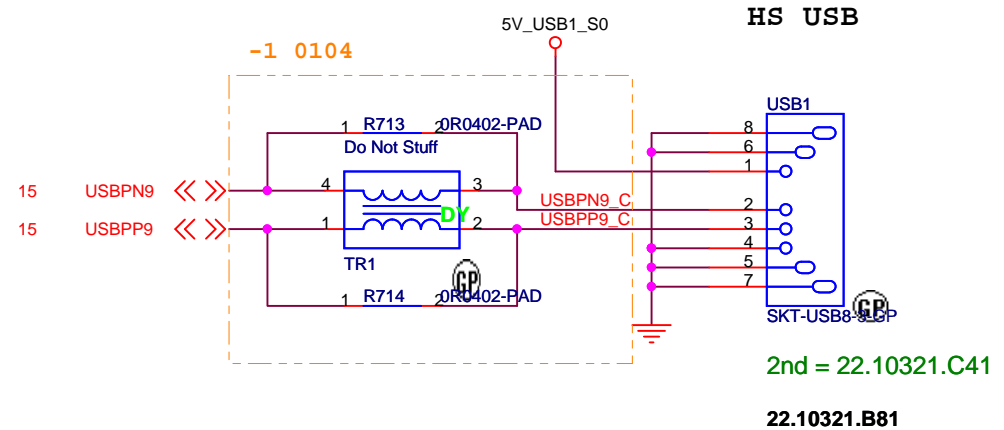
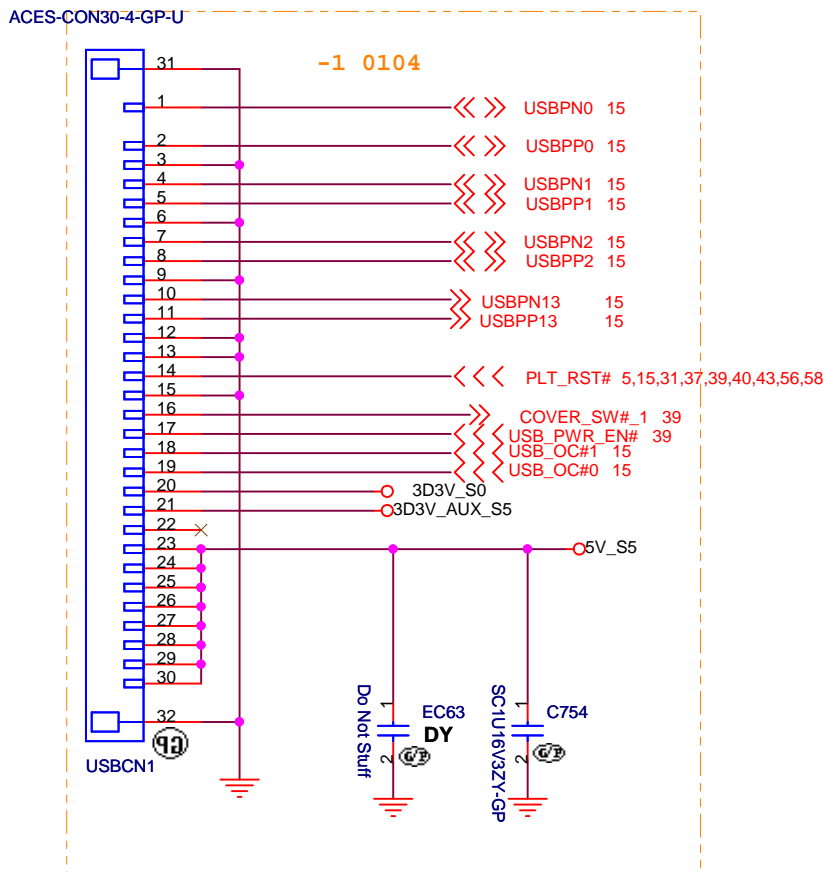
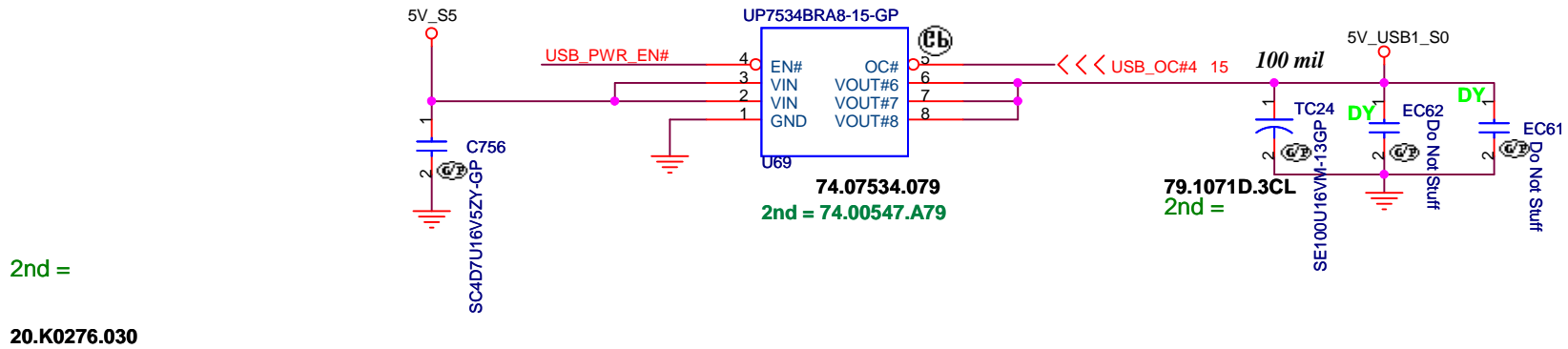
JE70-CP

Rev

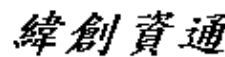
-1M

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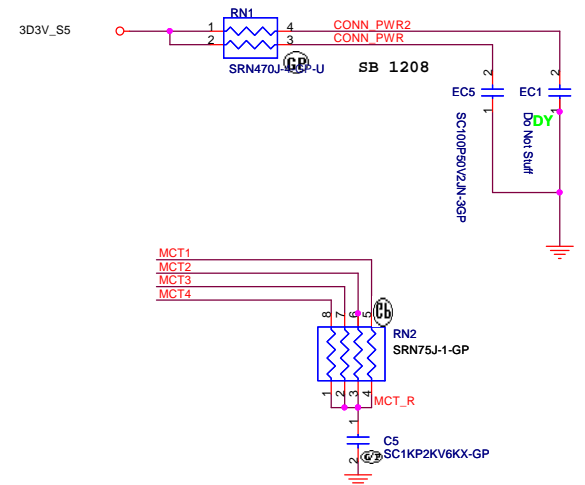
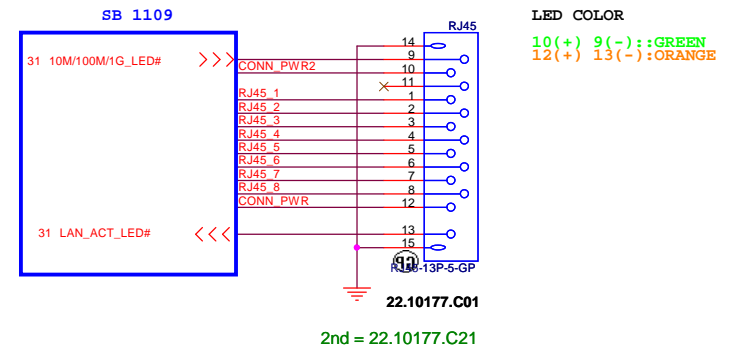
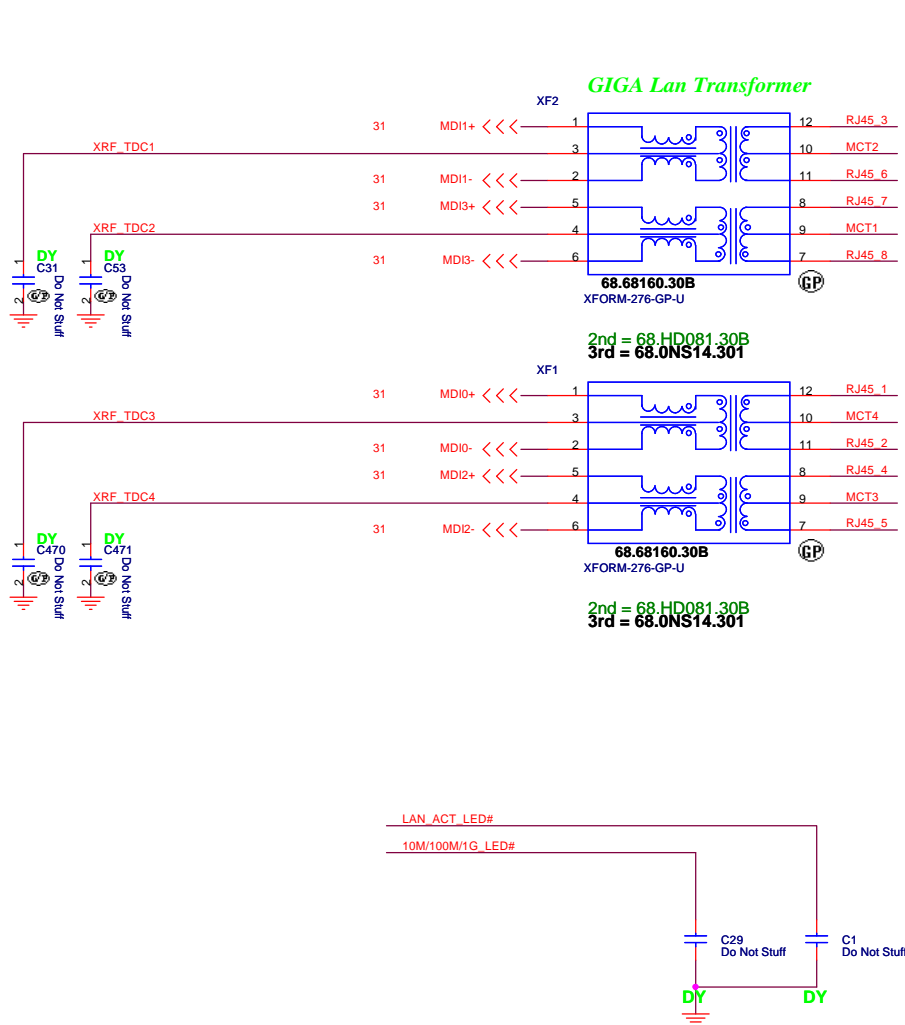
Pre UMA

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
USB CONN		
Size	Document Number	Rev
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LAN Connector

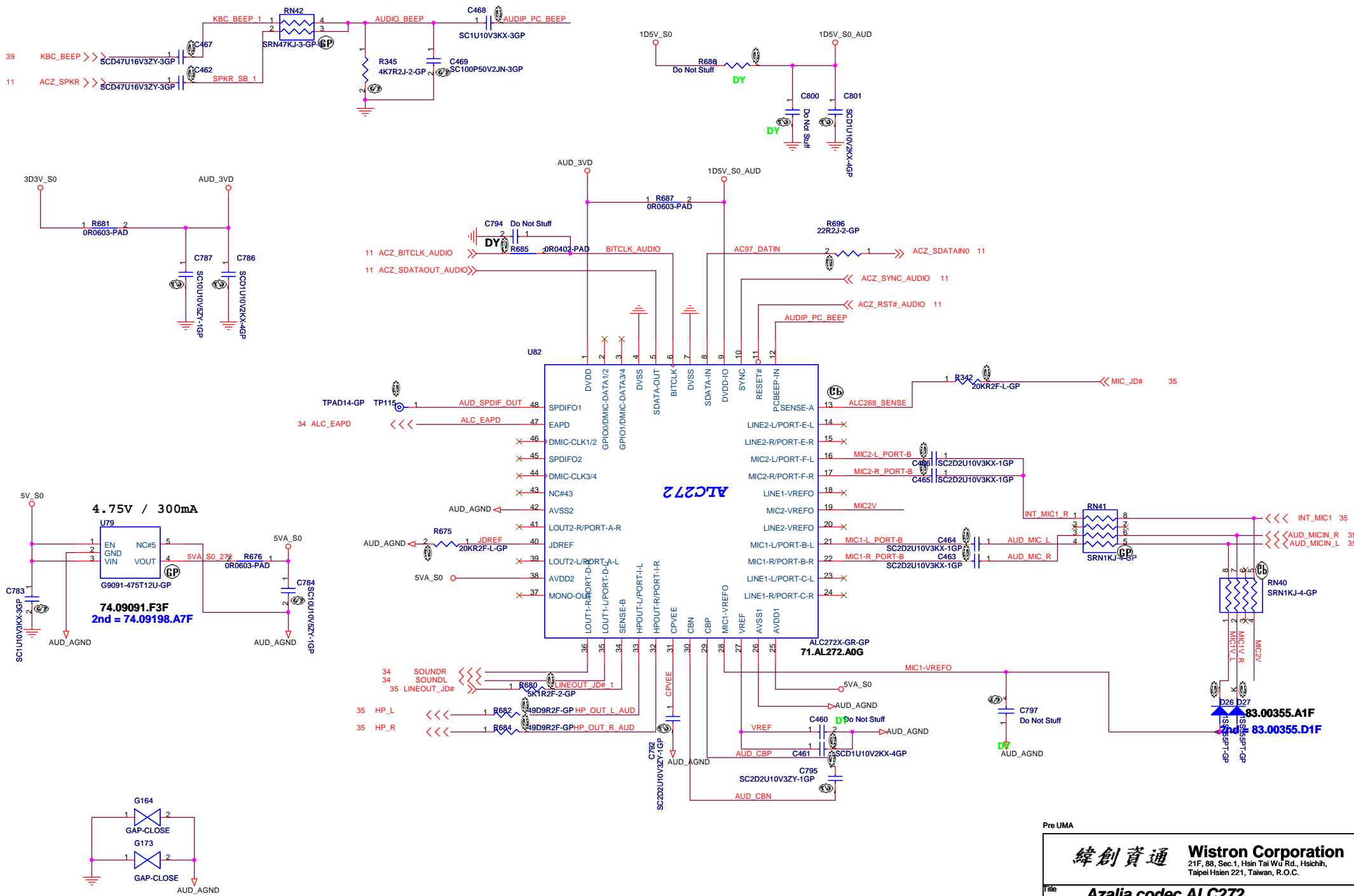
LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



Pre UMA

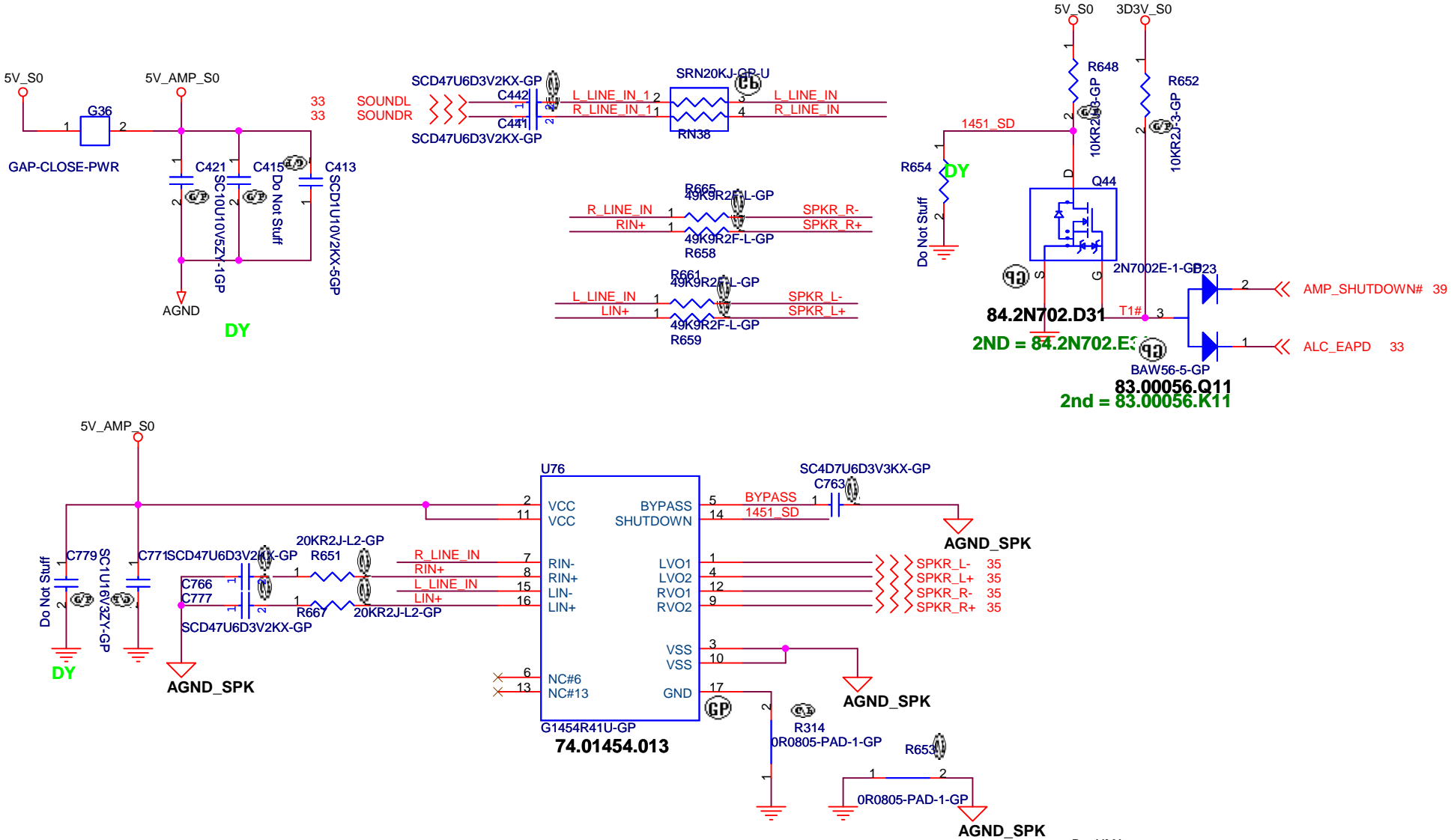
Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
LAN CONN	
Title	
Size A3	Document Number JE70-CP
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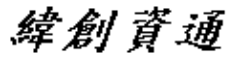
Pre UMA		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Azalia codec ALC272		
Size A3	Document Number JE70-CP	Rev -1M
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AUDIO OP AMPLIFIER

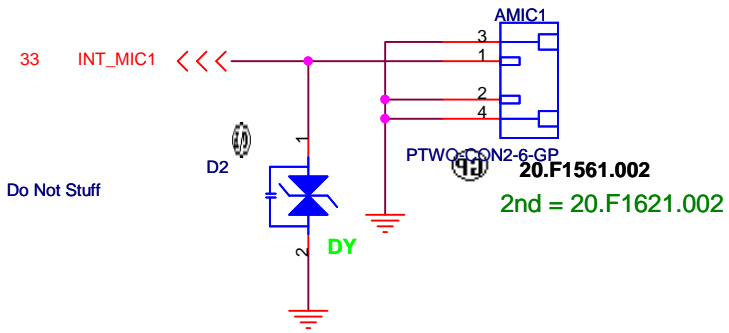


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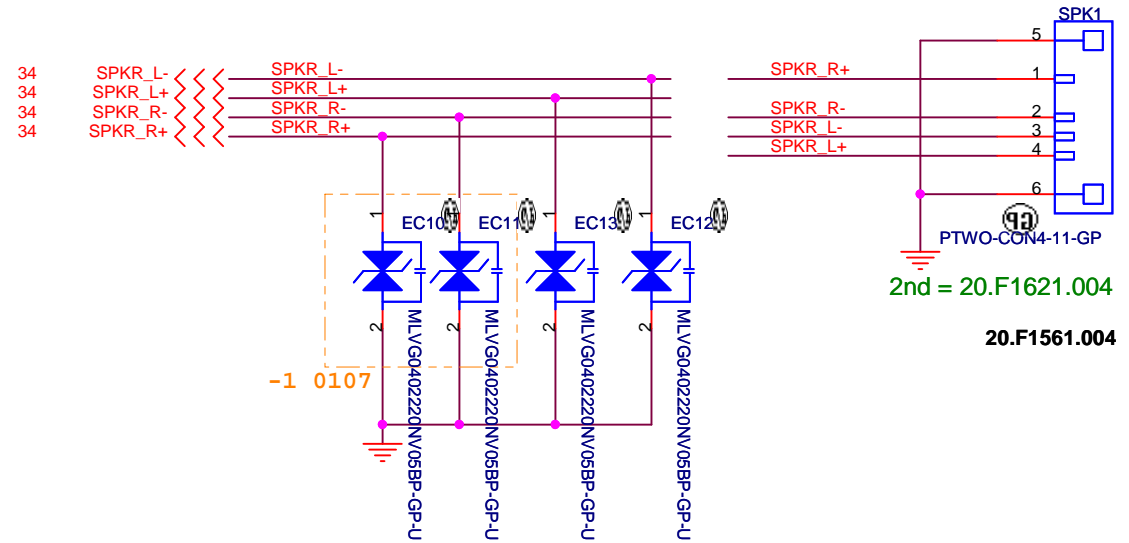
Pre UMA

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title AUDIO AMP	
Size	Document Number JE70-CP
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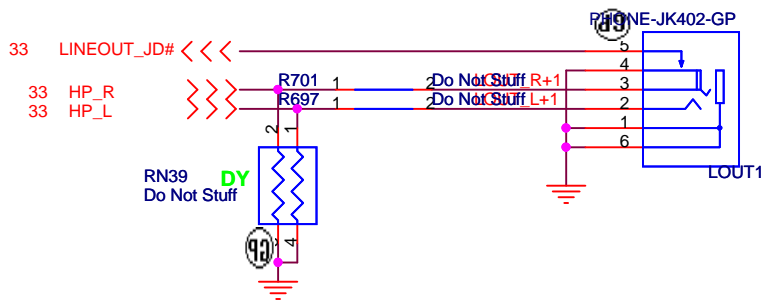
Internal Mic



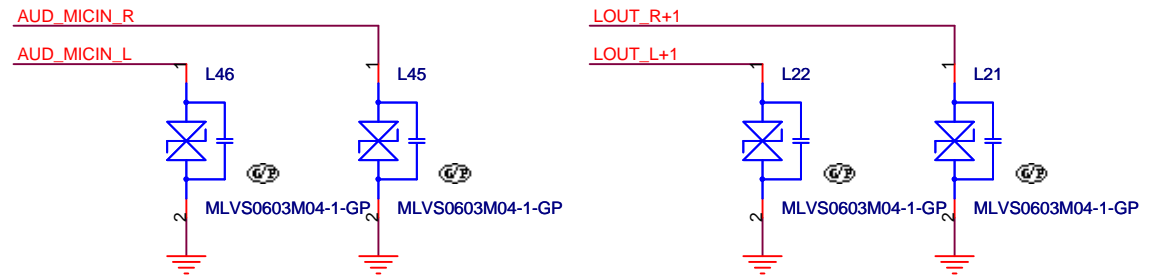
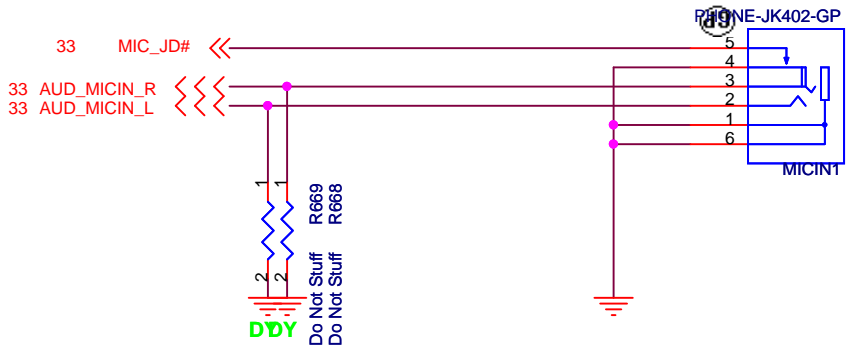
Internal Speaker



LINE OUT



MIC IN



Pre UMA

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Title		
AUDIO jack		
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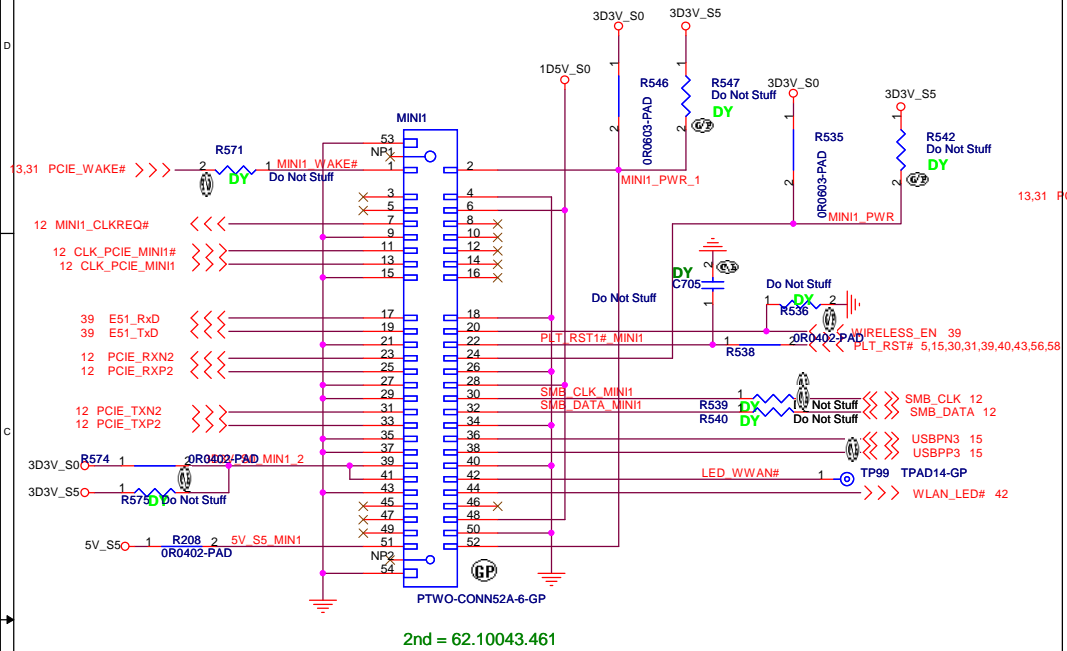
Pre UMA

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Title			
Cardreader			
Size	Document Number	JE70-CP	Rev
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Mini Card Connector(WLAN)

Support debug-card

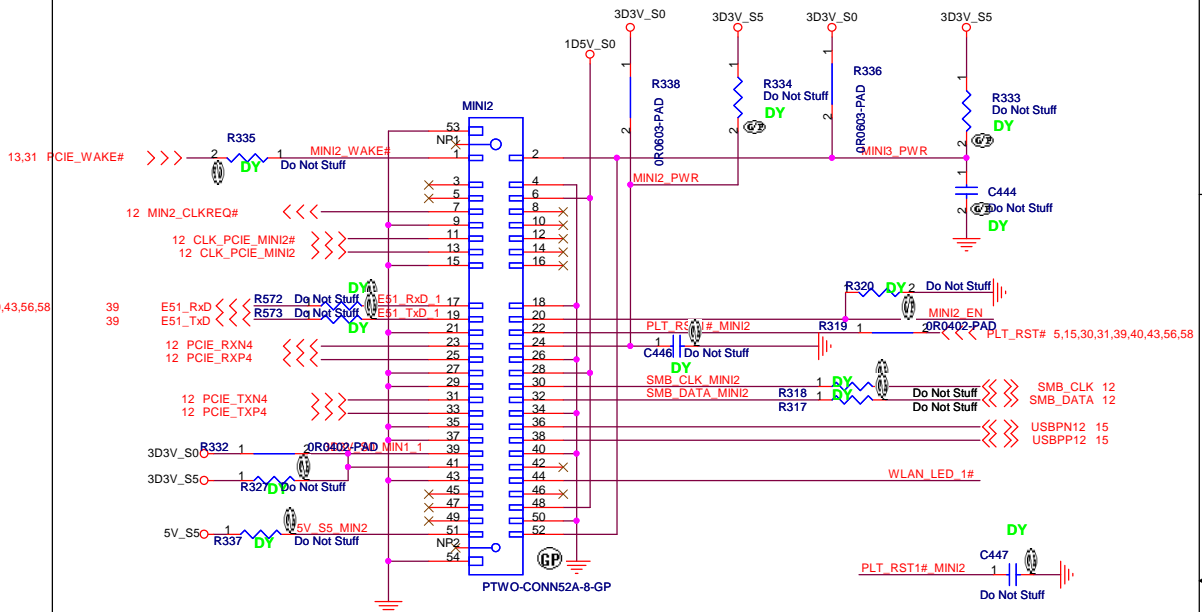
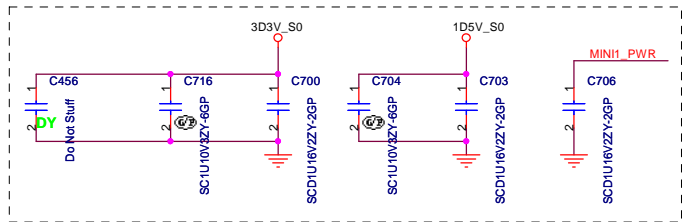
Mini Card Connector(Robson2 and 3G)



2nd = 62.10043.461

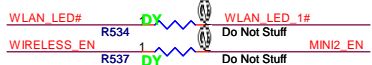
20.F1517.052

Place near MINI1

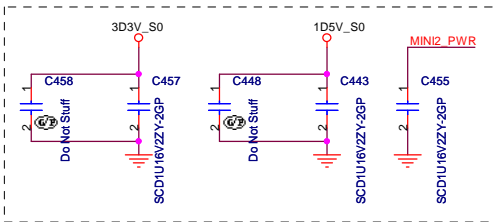


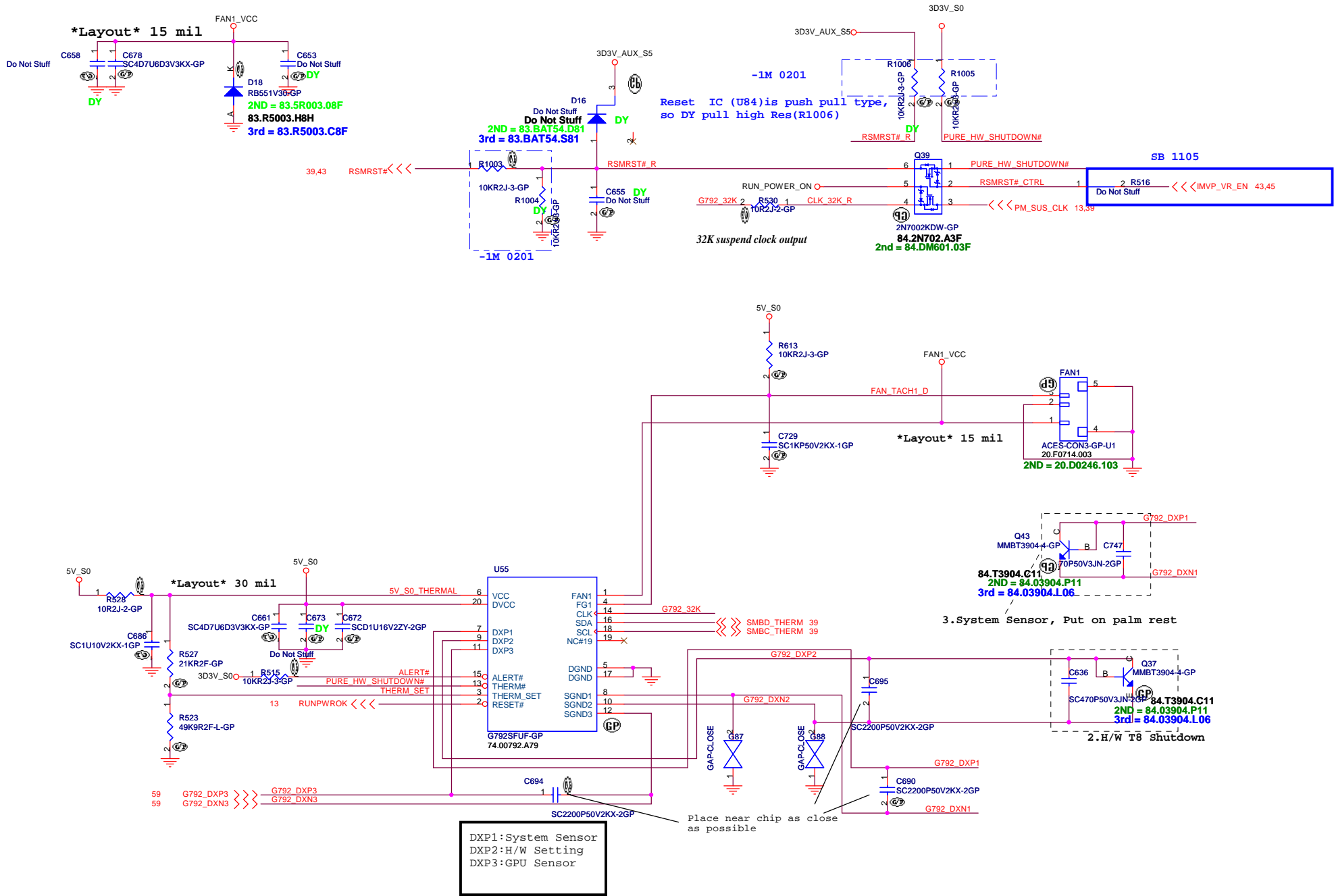
2nd =

20.F1518.052



Place near MINIC2





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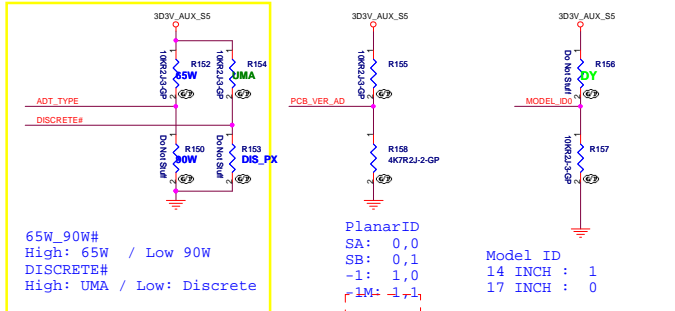
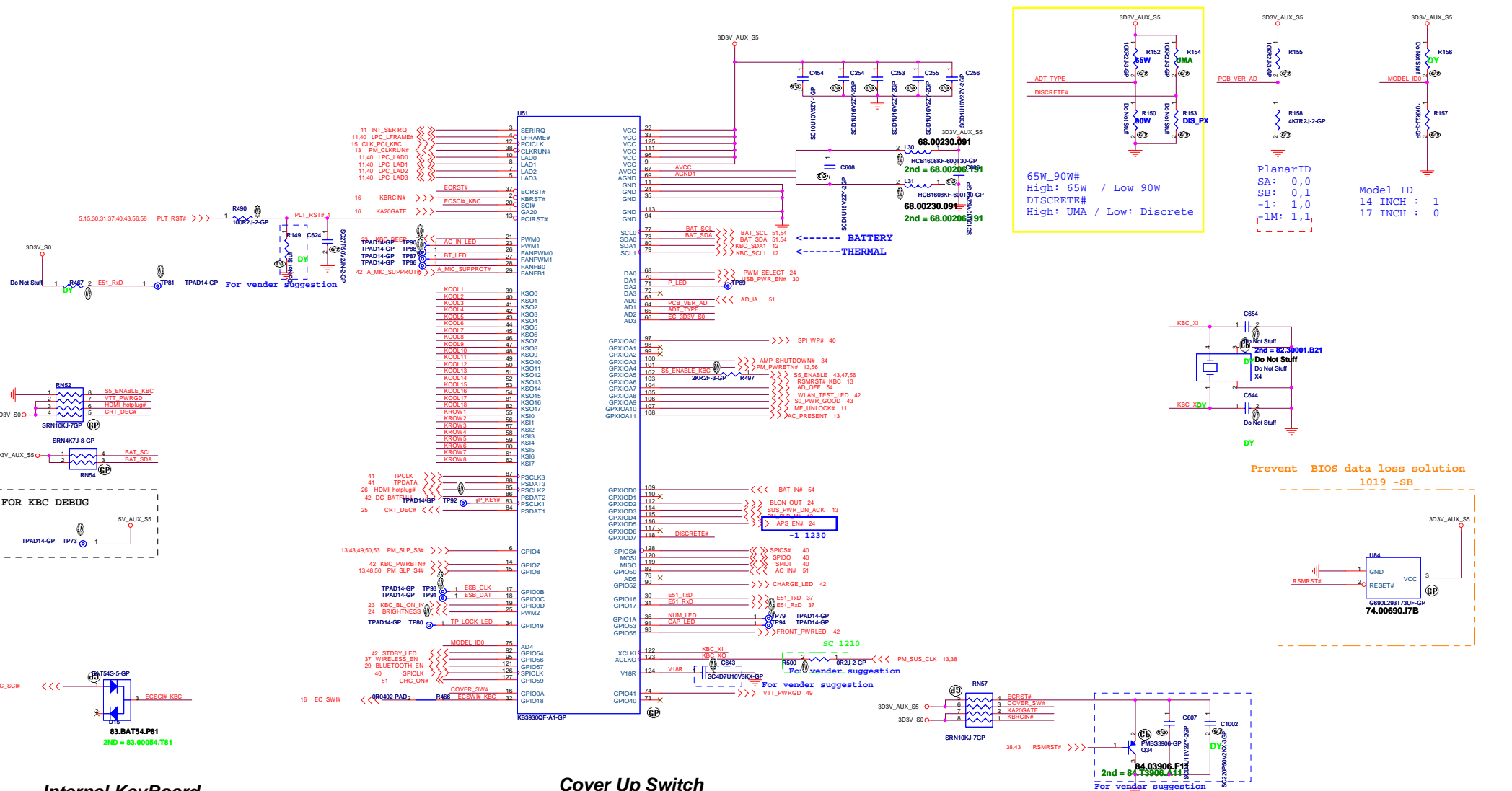
Pre UMA

緯創資通 **Wistron Corporation**
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Title: **Thermal/Fan Connector**

Size: Document Number **JE70-CP** Rev **-1M**

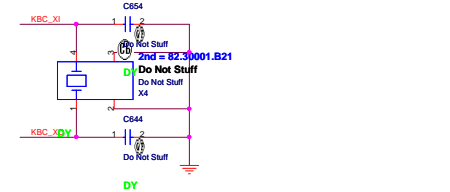
Date: Wednesday, February 03, 2010 Sheet 38 of 67



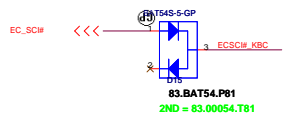
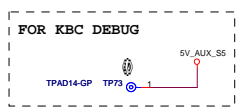
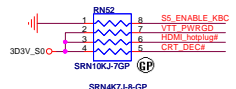
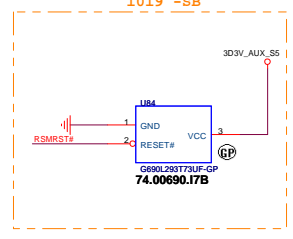
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete

PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
LM: -1,-1

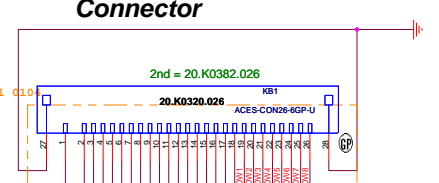
Model ID
14 INCH : 1
17 INCH : 0



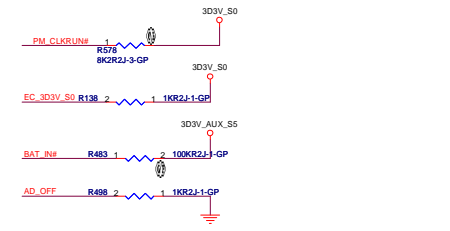
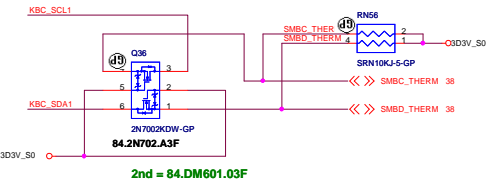
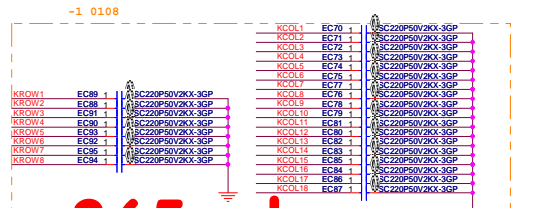
Prevent BIOS data loss solution
1019 -SB



Cover Up Switch



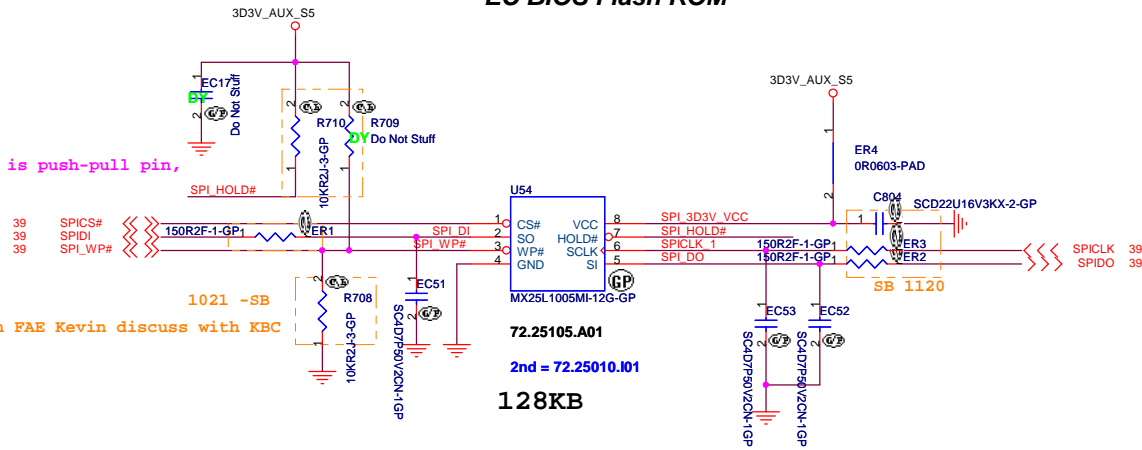
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26



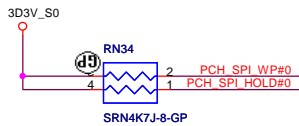
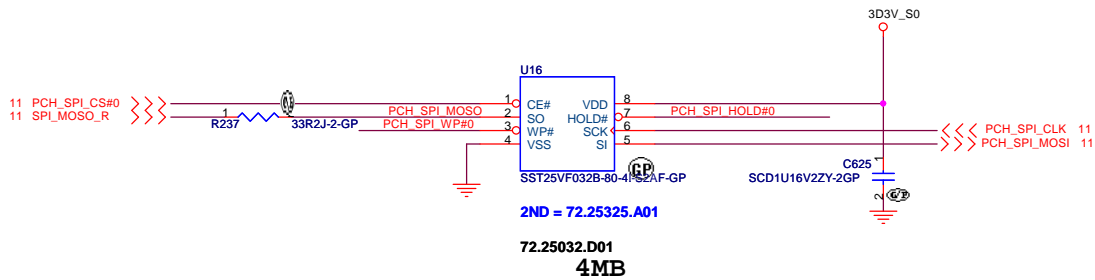
EC BIOS Flash ROM

for ENE FAE suggest, SPICS# is push-pull pin, don't need to pull high

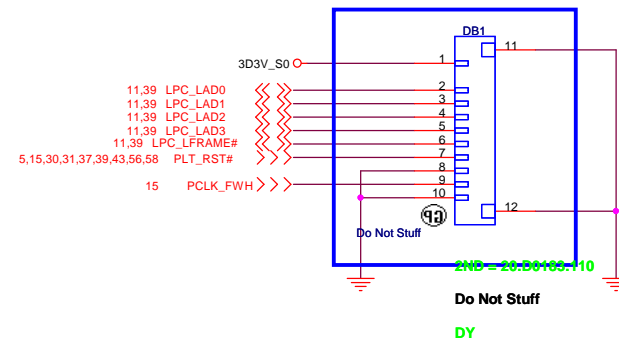
base on FAE Kevin discuss with KBC



System BIOS Flash ROM



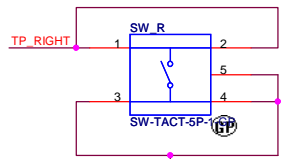
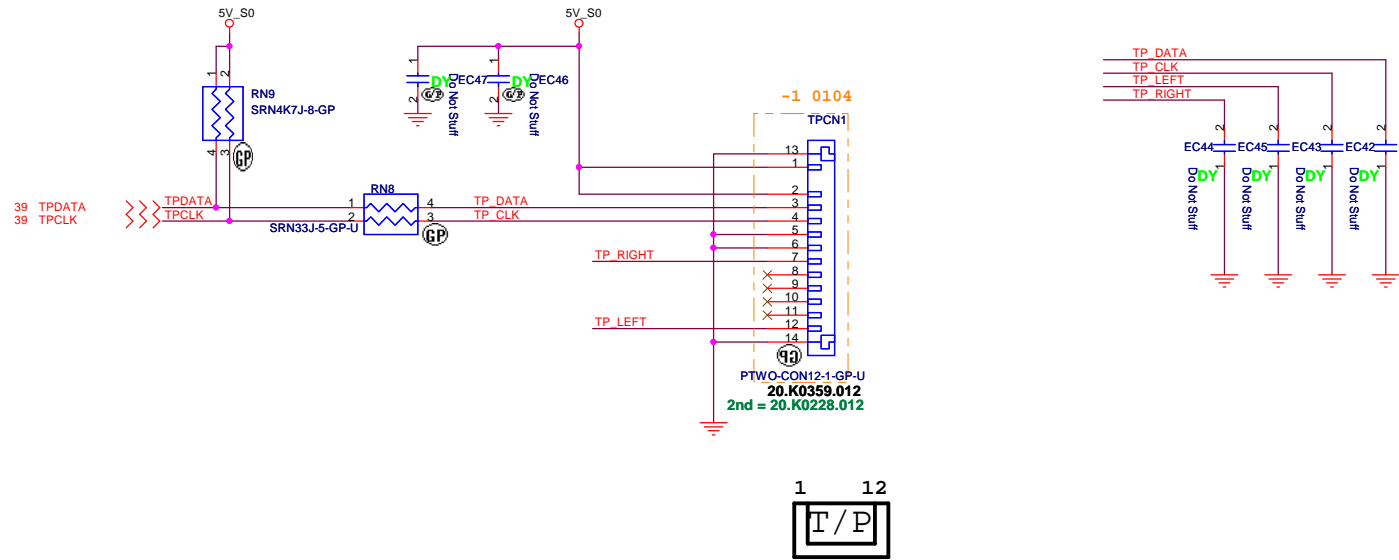
GOLDEN FINGER FOR DEBUG BOARD



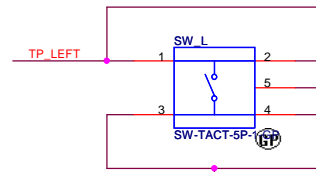
Pre UMA

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Title	
BIOS	
Size	Document Number
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Date: Tuesday, February 02, 2010	Sheet 40 of 67
Rev	-1M

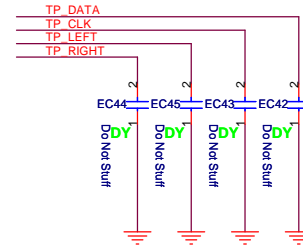
TOUCH PAD



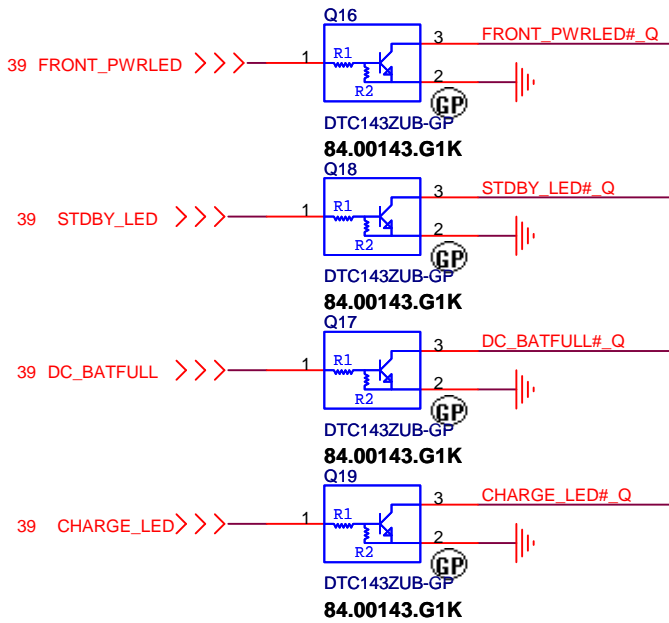
62.40009.A61
2nd = 62.40009.B21



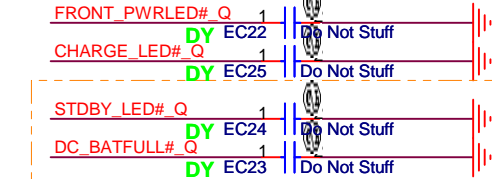
62.40009.A61
2nd = 62.40009.B21



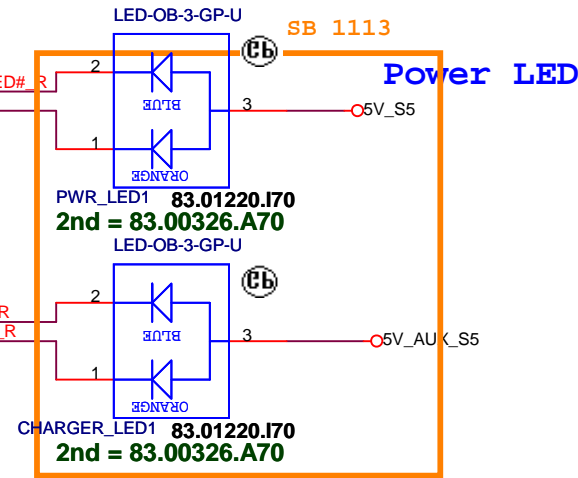
LED



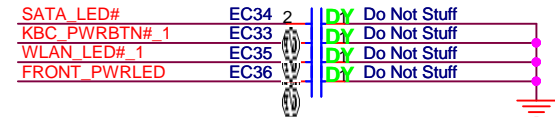
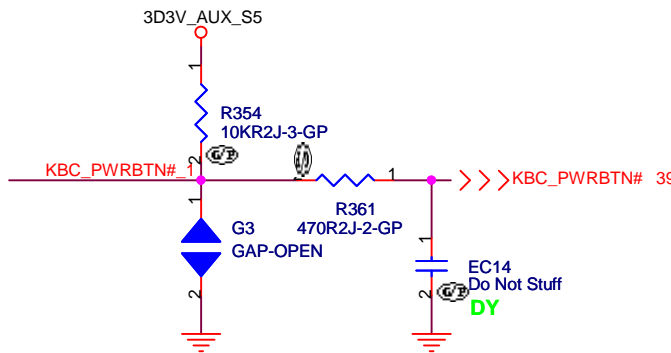
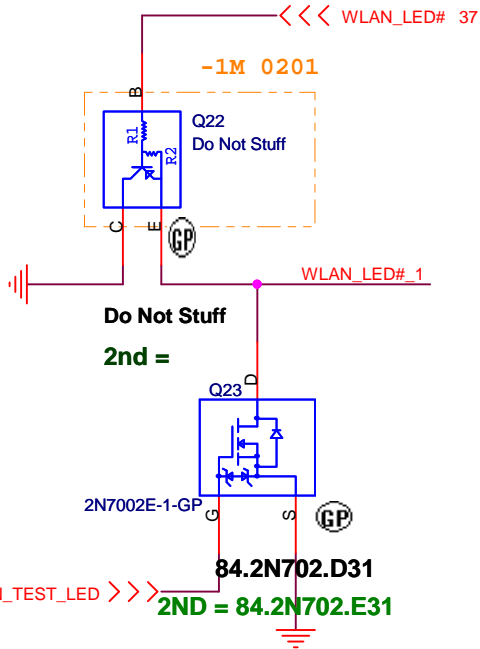
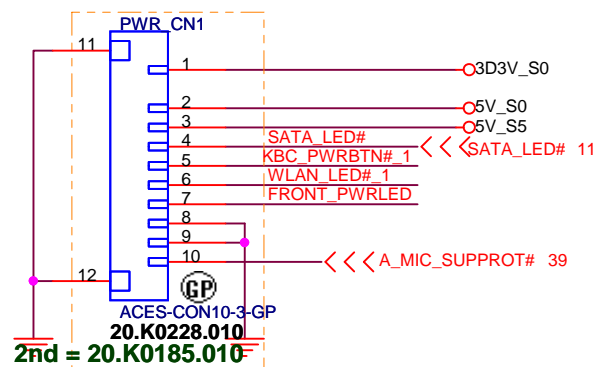
- FRONT_PWRLED#_Q 1 R340 330R2F-GP
- STDBY_LED#_Q 1 R343 330R2F-GP
- DC_BATFULL#_Q 1 R341 330R2F-GP
- CHARGE_LED#_Q 1 R344 330R2F-GP



-1 0107



-1 0104



Pre UMA

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Title LED&POWERBD CONN

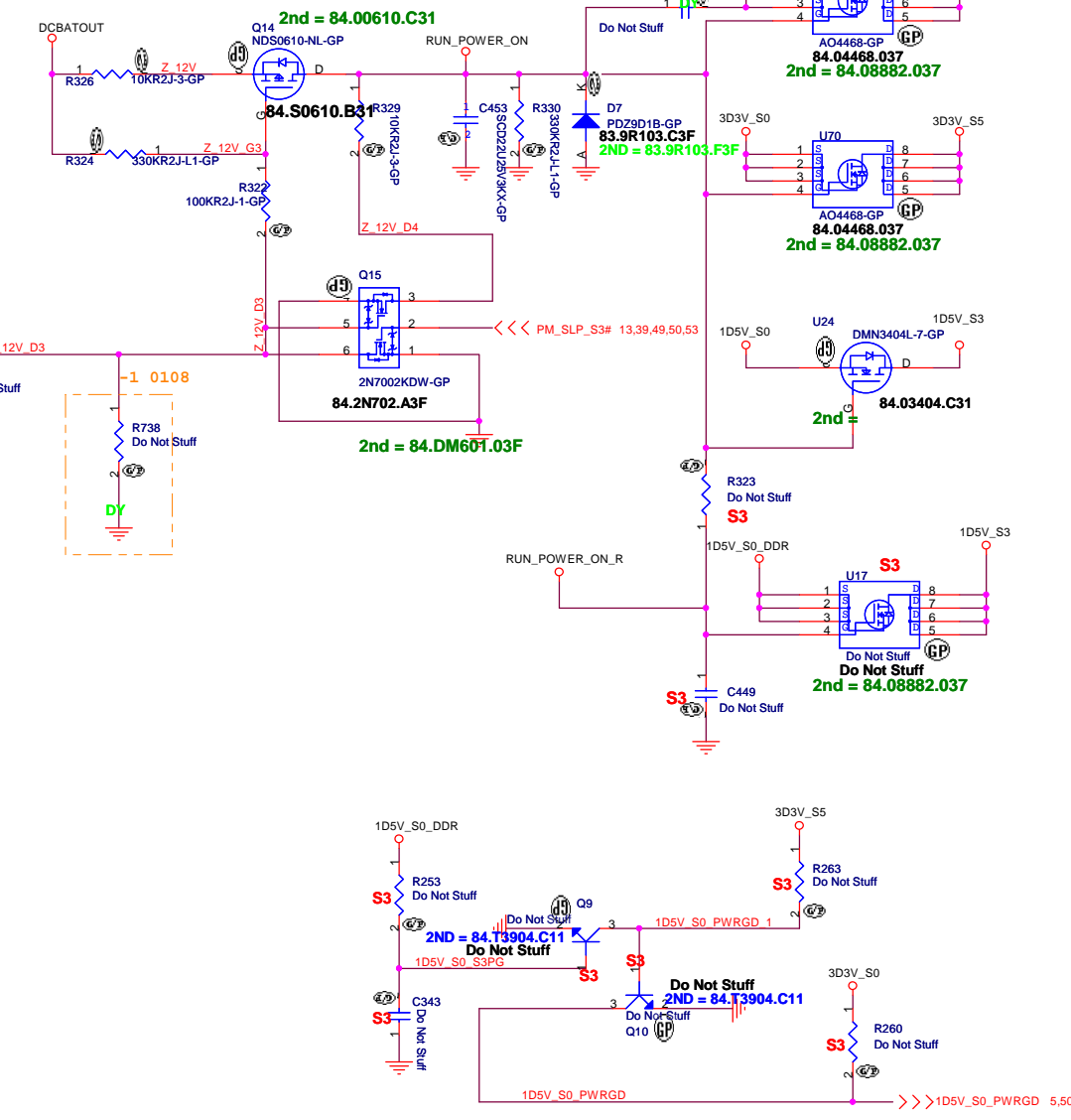
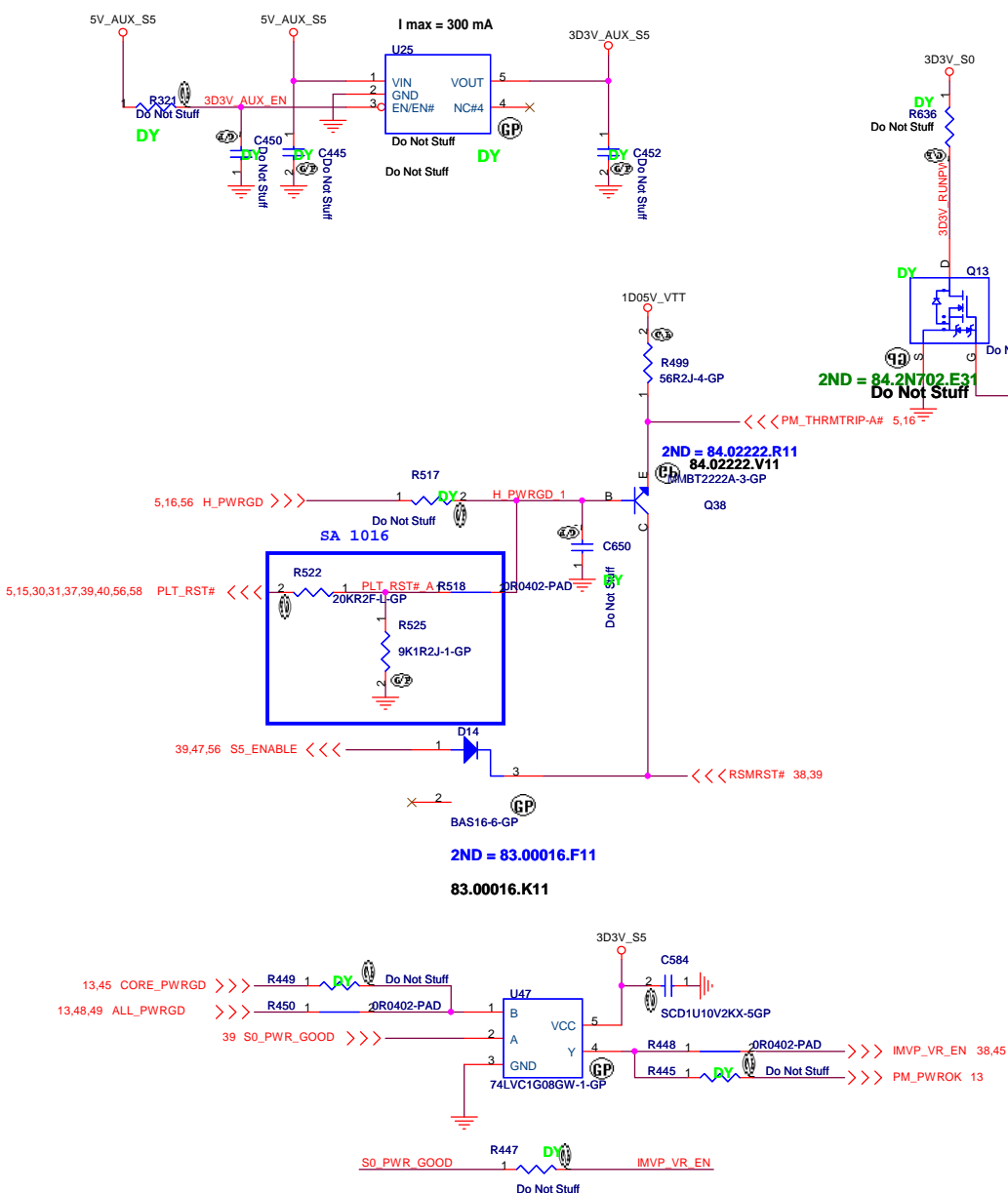
Size Document Number JE70-CP Rev -1M

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Run Power

Aux Power

3D3V_AUX_S5



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Pre UMA

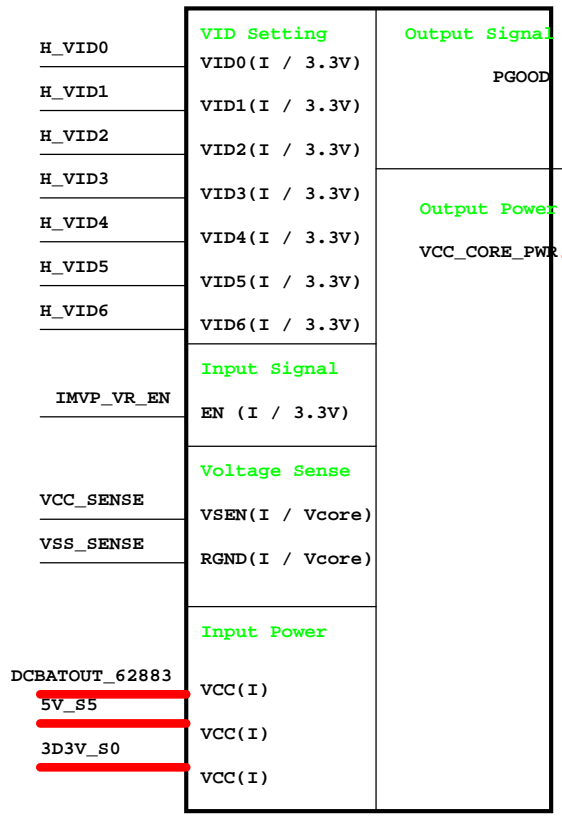
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and 3D3V AUX S5**

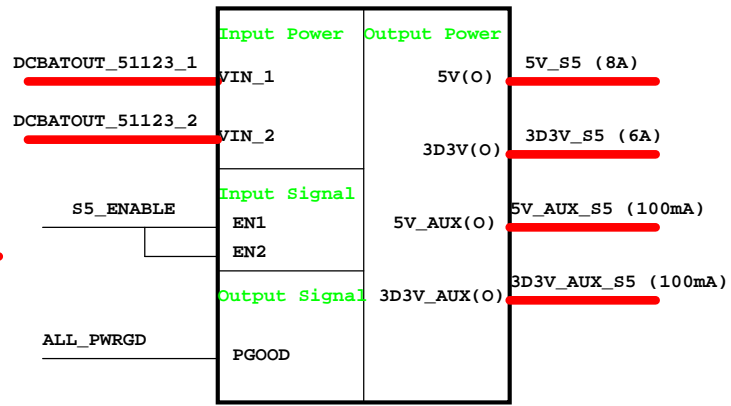
Size	Document Number	Rev
	JE70-CP	-1M

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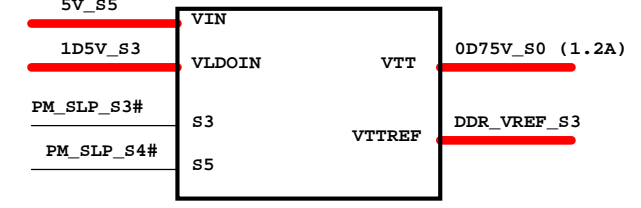
ISL62883 VCC_CORE



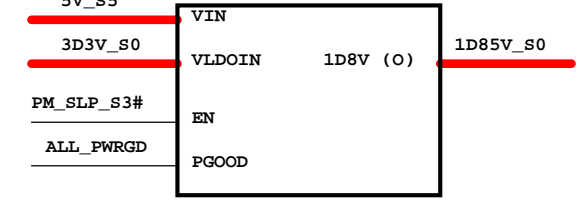
TPS51123 5V/3D3V



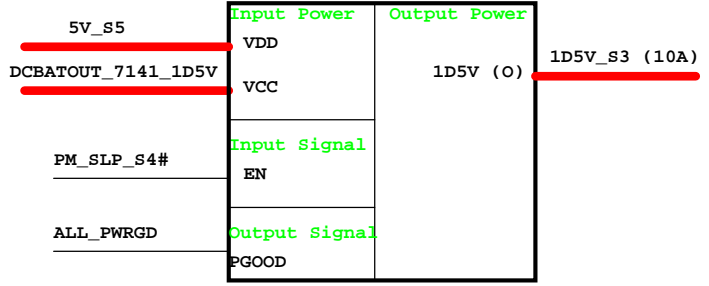
RT9026 0D75V_S0



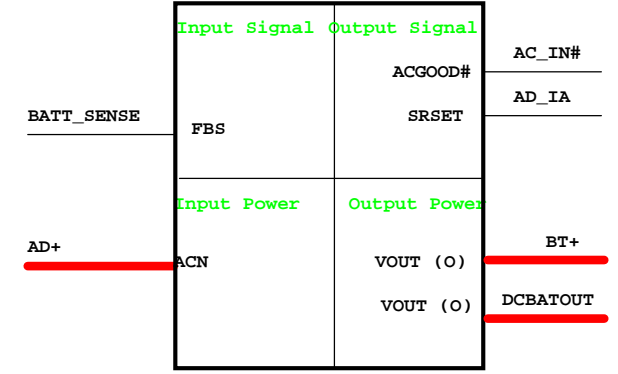
RT9025 1D8V



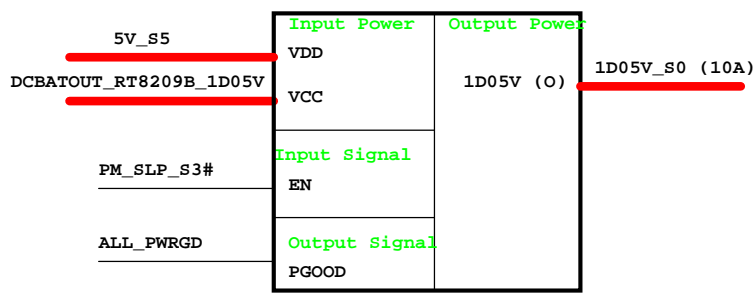
RT9025 1D5V



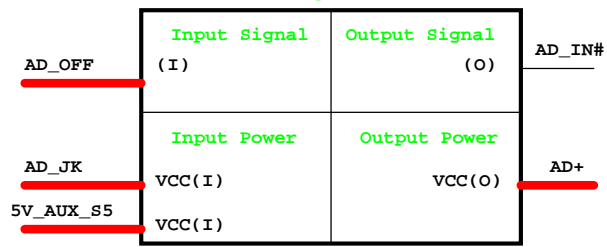
Charger BQ24745



RT8209B 1D05V



Adapter



Pre UMA

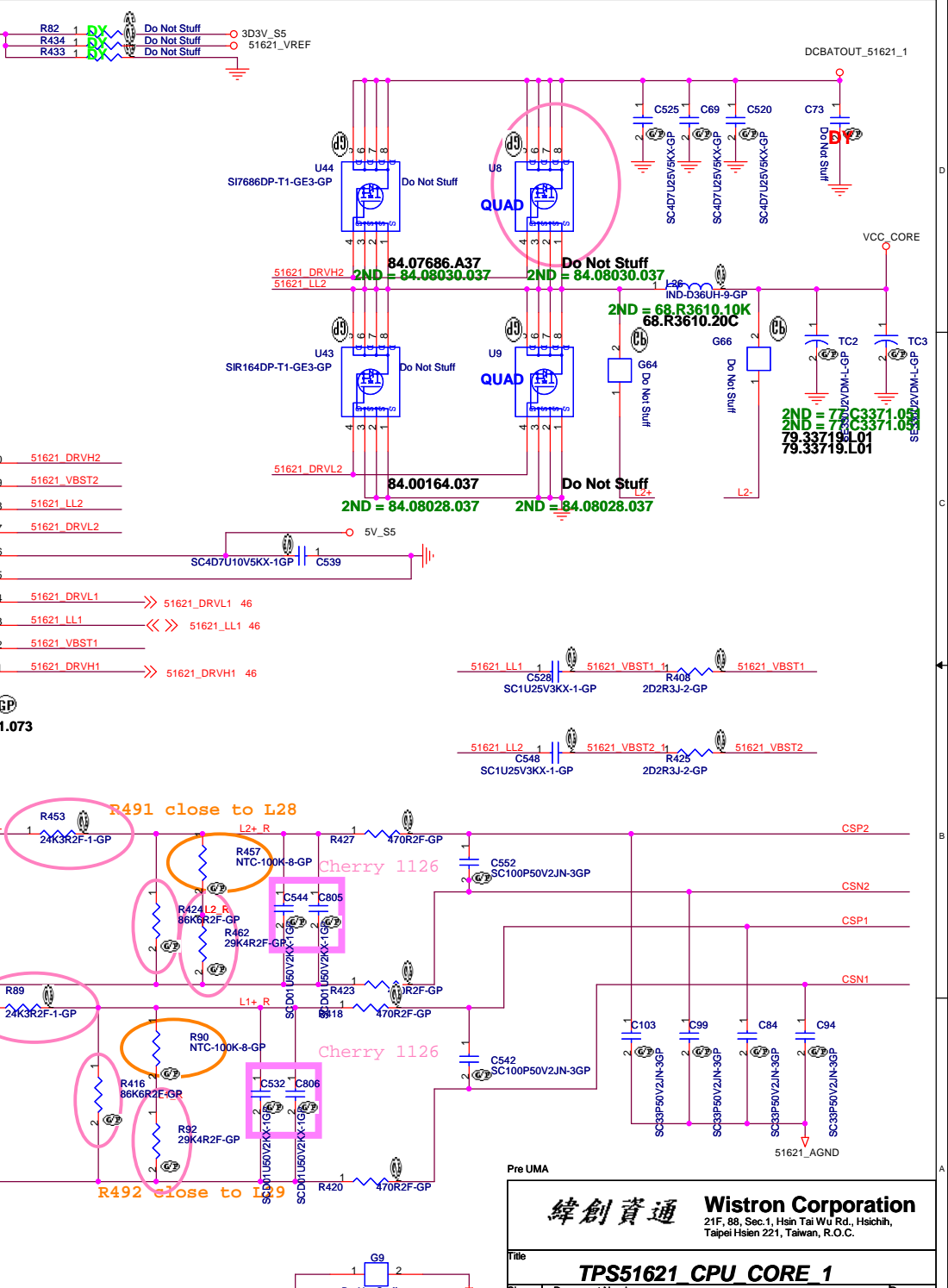
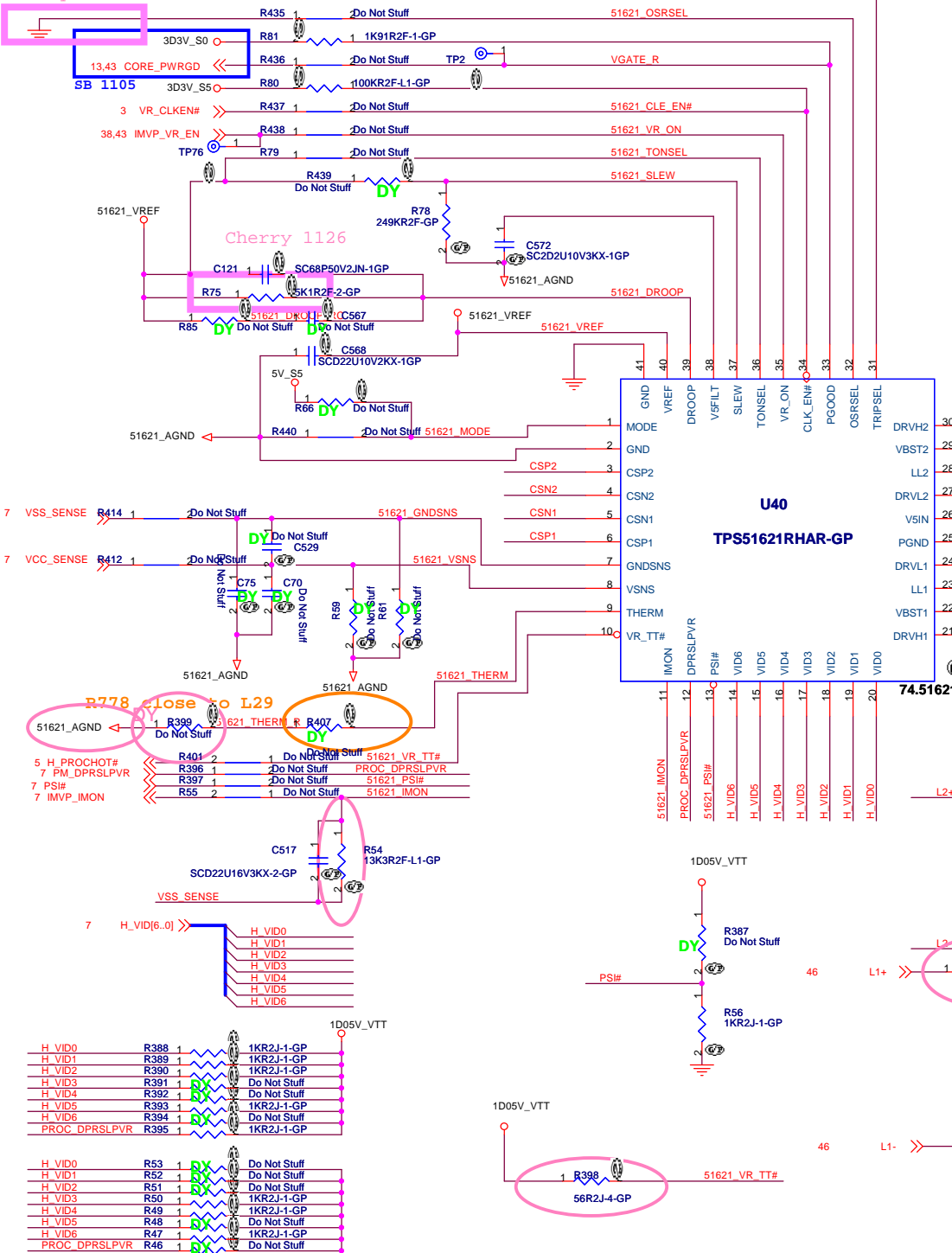
緯創資通 Wistron Corporation
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Title **Power Block Diagram**

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Cherry 1204



- 7 VSS_SENSE R414 1 Do Not Stuff
- 7 VCC_SENSE R412 1 Do Not Stuff
- 5 H_PROCHOT# R401 2 Do Not Stuff
- 7 PM_DPRSPLV R396 1 Do Not Stuff
- 7 PS1# R397 1 Do Not Stuff
- 7 IMVP_IMON R55 2 Do Not Stuff

- H_VID0 R388 1 1K R2J-1-GP
- H_VID1 R389 1 1K R2J-1-GP
- H_VID2 R390 1 1K R2J-1-GP
- H_VID3 R391 1 Do Not Stuff
- H_VID4 R392 1 Do Not Stuff
- H_VID5 R393 1 1K R2J-1-GP
- H_VID6 R394 1 Do Not Stuff
- PROC_DPRSPLV R395 1 1K R2J-1-GP

- H_VID0 R53 1 Do Not Stuff
- H_VID1 R52 1 Do Not Stuff
- H_VID2 R51 1 Do Not Stuff
- H_VID3 R50 1 1K R2J-1-GP
- H_VID4 R49 1 1K R2J-1-GP
- H_VID5 R48 1 Do Not Stuff
- H_VID6 R47 1 1K R2J-1-GP
- PROC_DPRSPLV R46 1 Do Not Stuff

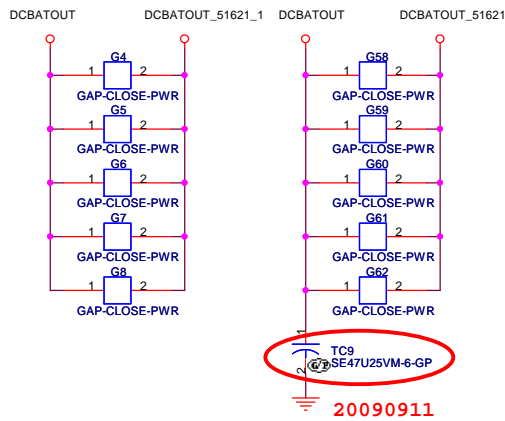
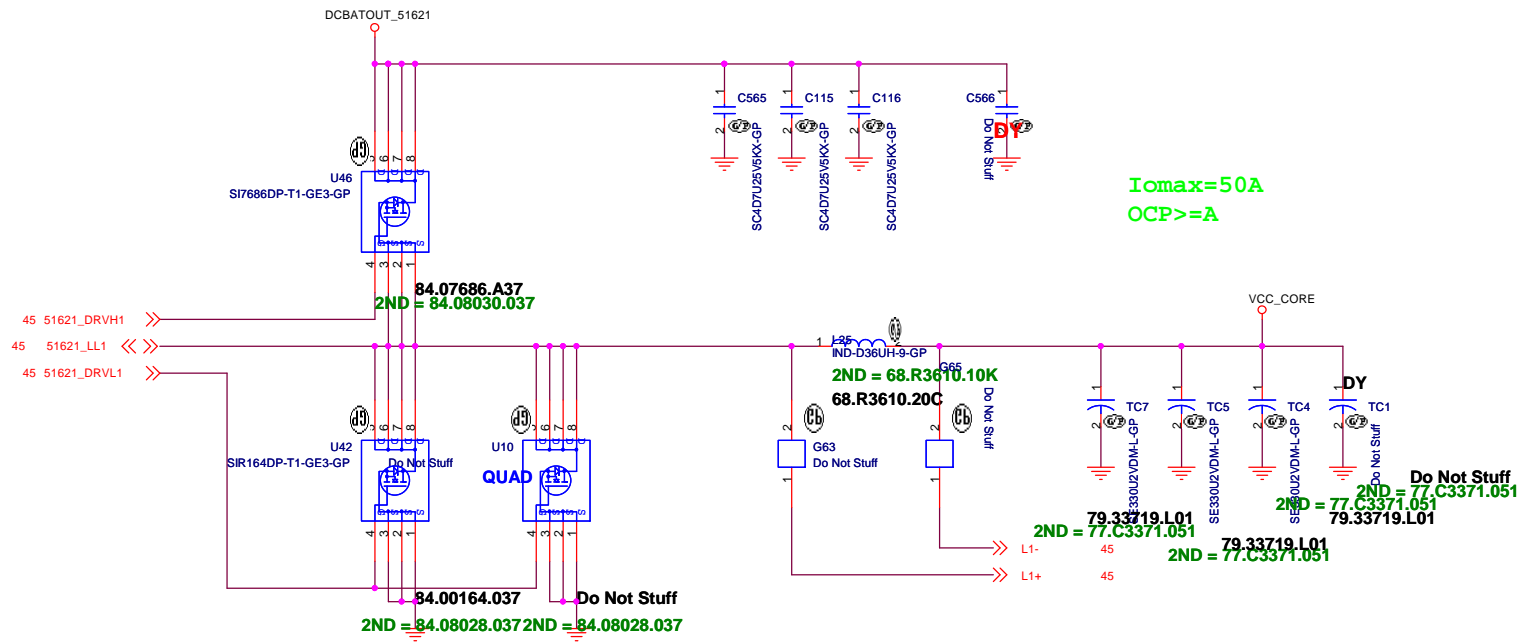
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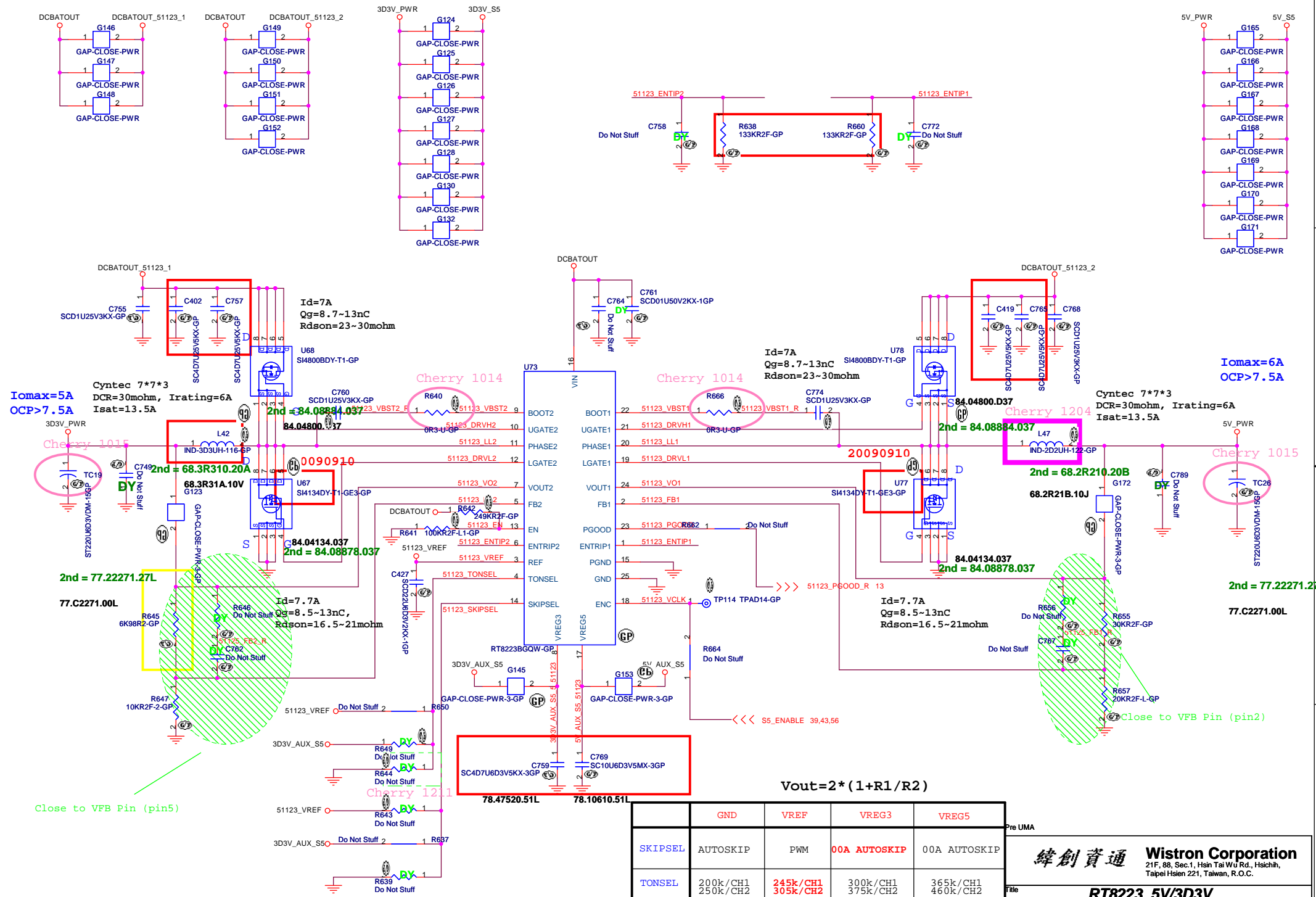
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Size	A3	Document Number	JE70-CP
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Pre UMA

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ISL62882 CPU CORE (1/2)		
Title		
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$$V_{out} = 2 * (1 + R1/R2)$$

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

Pre UMA

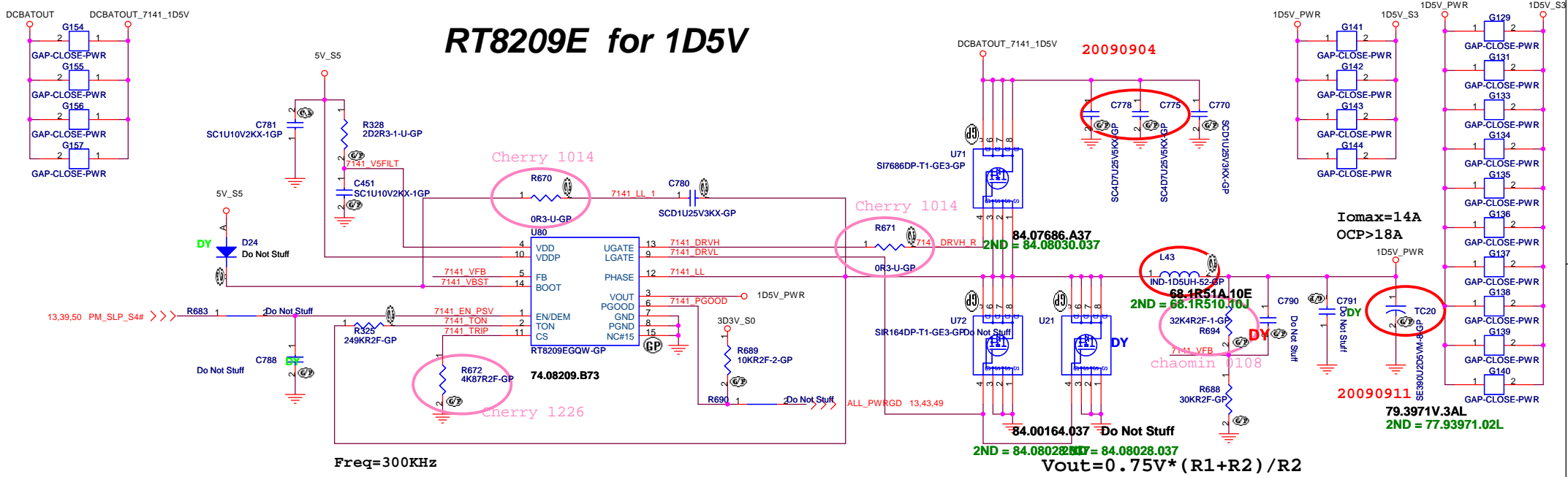
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: **RT8223_5V/3D3V**

Size: Document Number **JE70-CP** Rev: **-1M**

Date: Tuesday, February 02, 2010 Sheet: 47 of 67

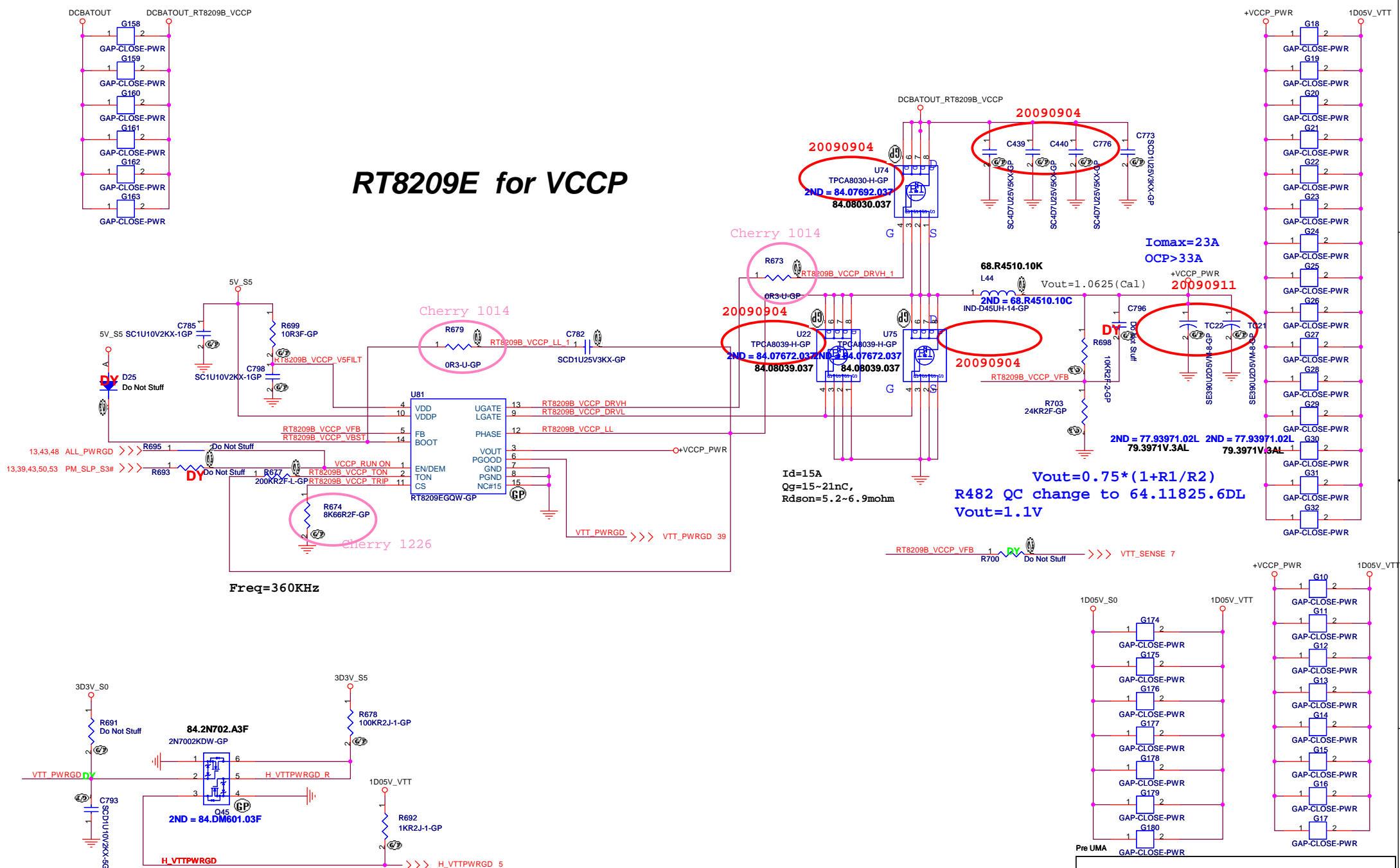
RT8209E for 1D5V



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Pre UMA	
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
RT8209E 1D5V	
Size	Document Number
	JE70-CP
Date:	Rev
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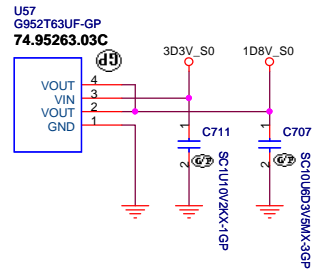
RT8209E for VCCP




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 Taipei Hsien 221, Taiwan, R.O.C.

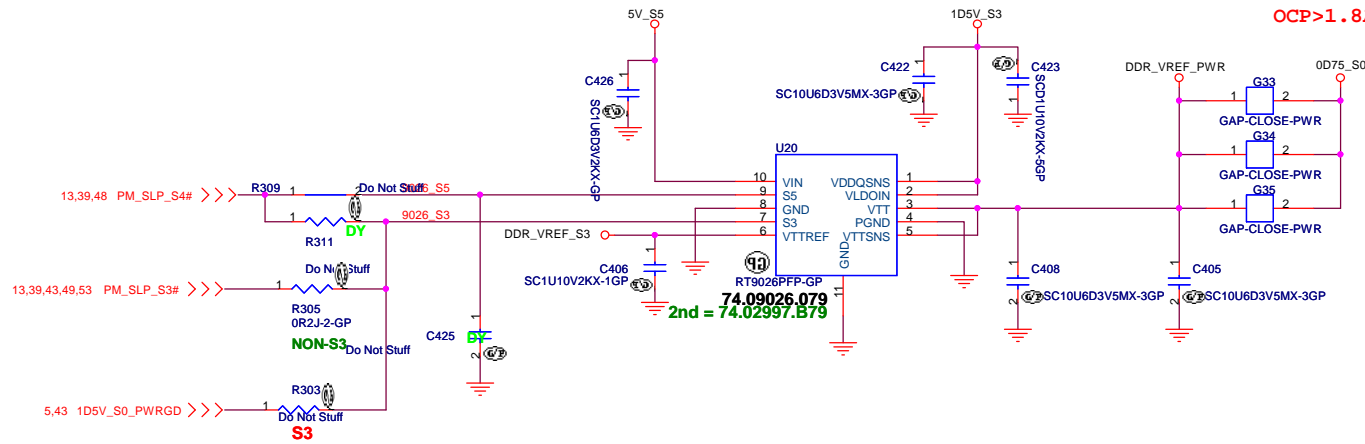
Title: **RT8209B_+VCCP**
 Size: Document Number **JE70-CP** Rev: **-1M**
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1.8V_S0 1.8V 1A Regulator

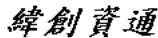


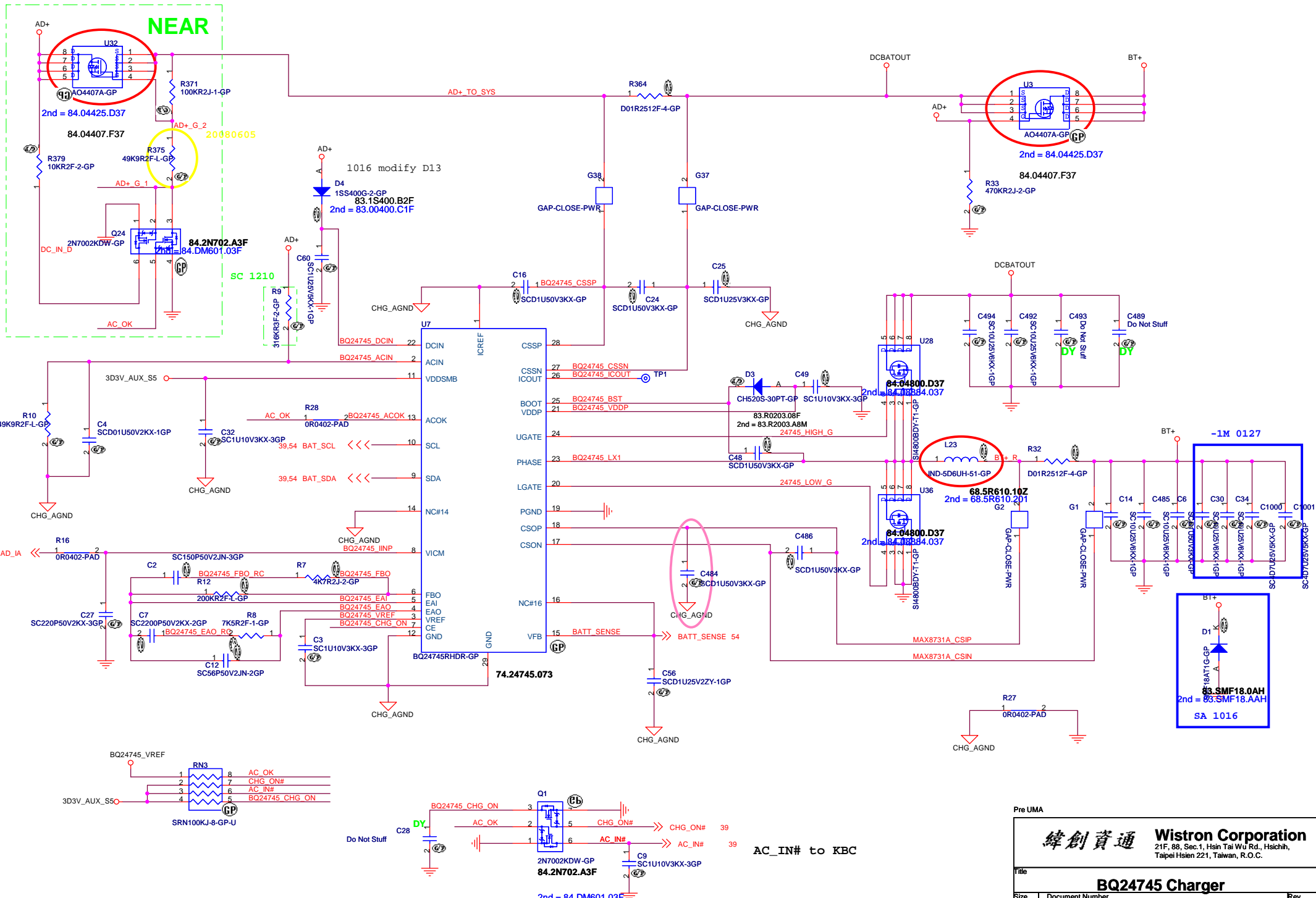
RT9026 for 0D75V_S3

I_{omax}=1.2A
OCP>1.8A



Pre UMA

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RT8015A for 1D8V/RT9026 0D75	
File	Rev
Size	Document Number
JE70-CP	
Date: Tuesday, February 02, 2010	Sheet 50 of 67

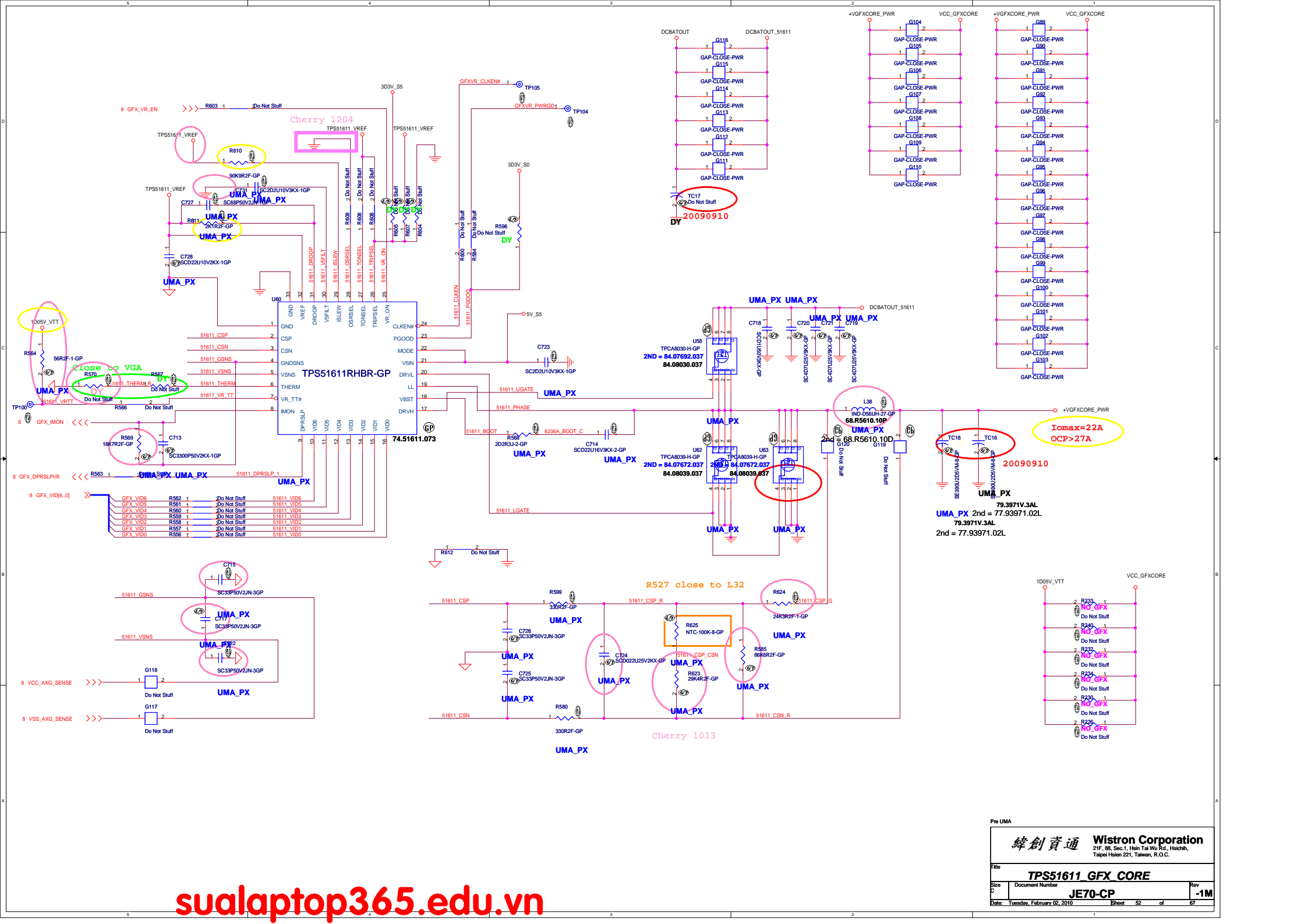


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Pre UMA

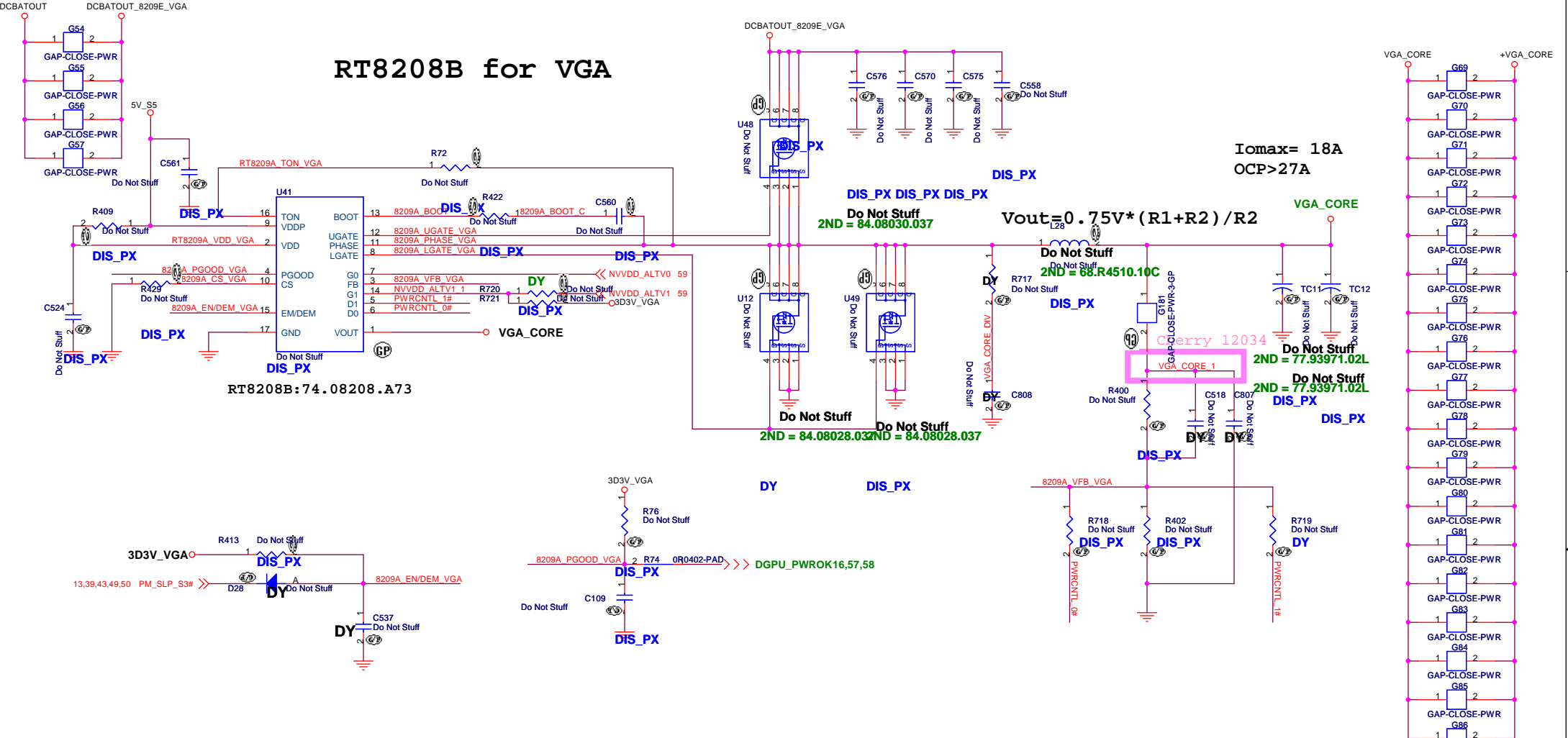
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
BQ24745 Charger		
Size	Document Number	Rev
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RT8208B for VGA



RT8208B: 74.08208.A73

Iomax = 18A
OCP > 27A

$$V_{out} = 0.75V * (R1 + R2) / R2$$

MADSIION PRO

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALT*0	O	YES	GPU VOLTAGE L: 1.00V GPU VOLTAGE H: 0.90V

PARK XT

	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALT*0	O	YES	GPU VOLTAGE L: 1.12V GPU VOLTAGE H: 0.90V

Park ==> R718 = 33K (64.33025.6DL)
Madison ==> R718 = 71.5K (64.71525.6DL)

NVVDD_ALT*1	NVVDD_ALT*0	+VGA_CORE
H	L	1.12V or 1V OUT = [R400 + (R402 // R718)] / (R402 // R718)
H	H	0.9V OUT = (R400 + R402) / R402

Pre UMA

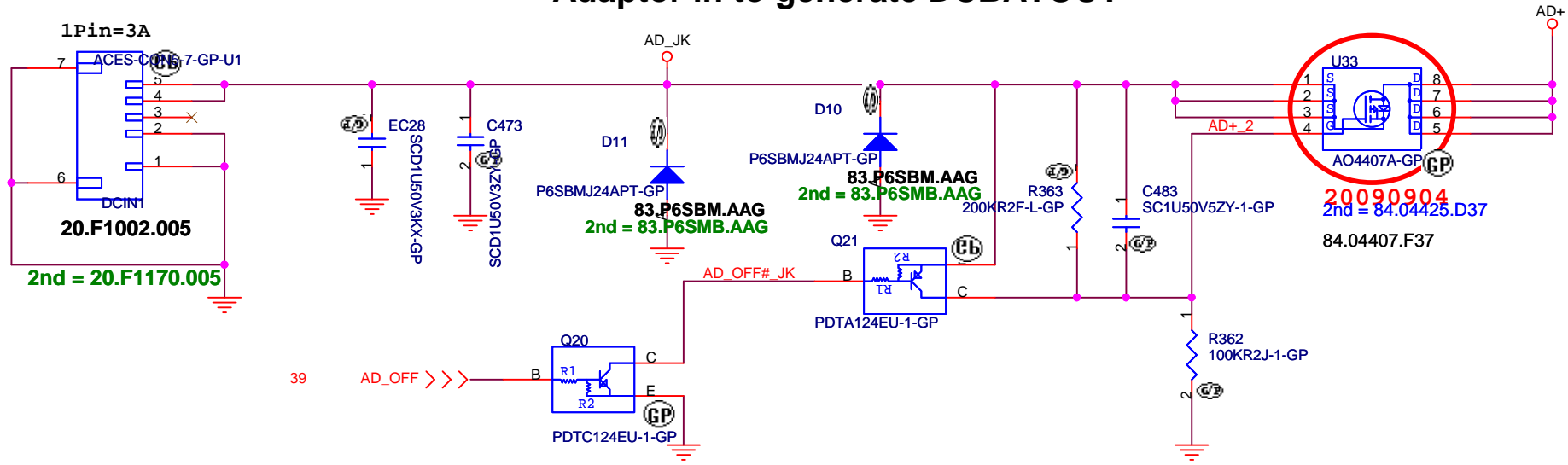
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8209E VGA CORE**

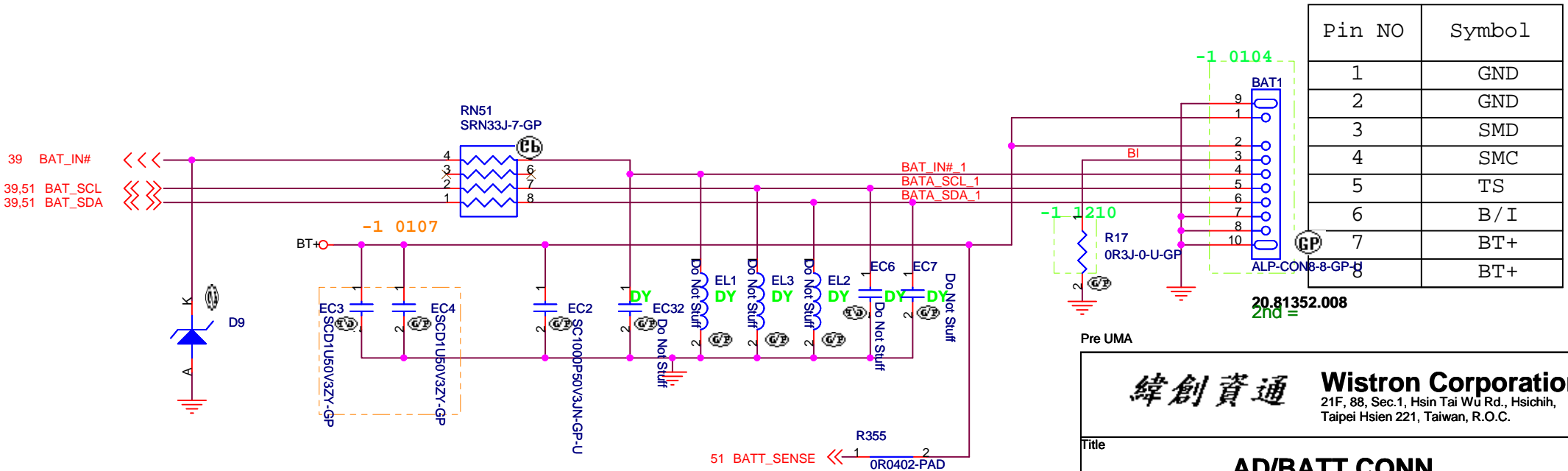
Size A3 Document Number: **JE70-CP** Rev

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Adaptor in to generate DCBATOUT



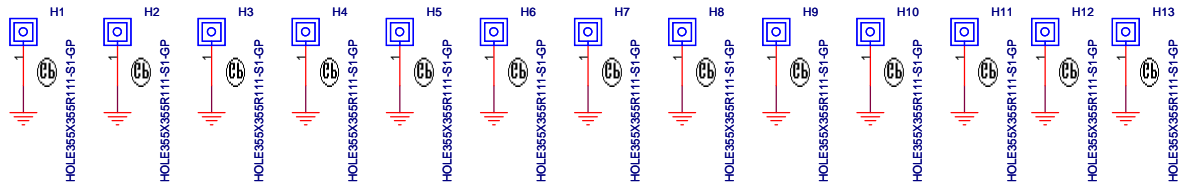
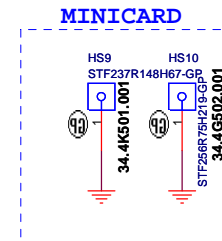
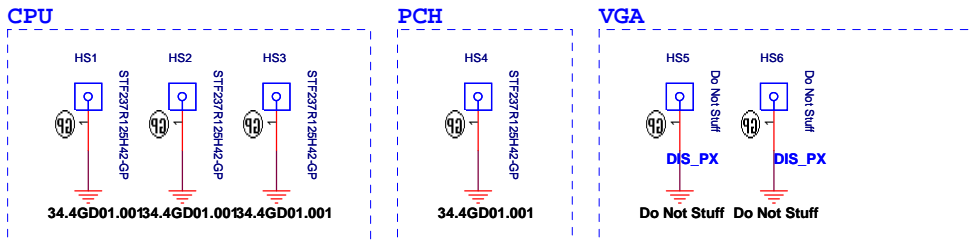
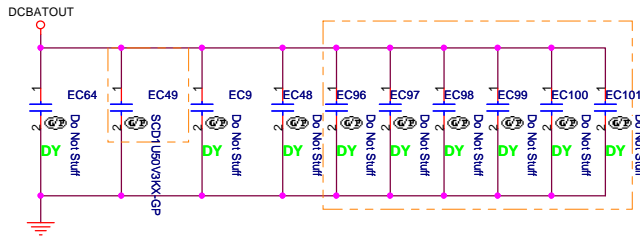
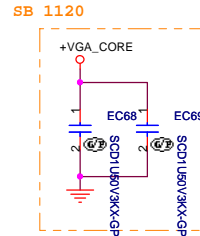
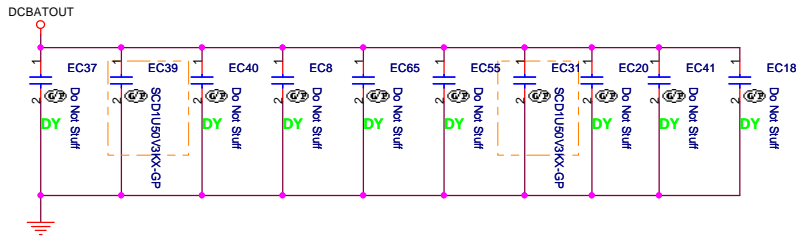
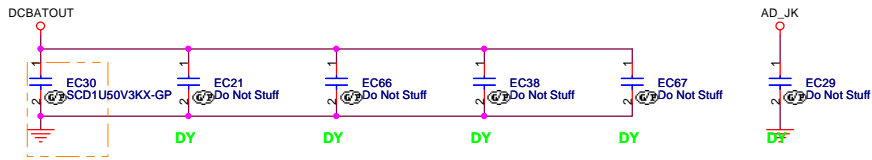
BATTERY CONNECTOR



Pre UMA

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
AD/BATT CONN		
Size	Document Number	Rev
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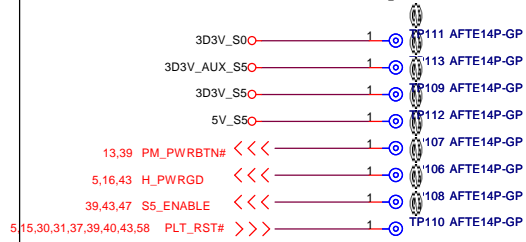


Pre UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

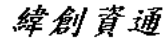
Title		
EMI/Spring/Boss		
Size	Document Number	Rev
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Check test point

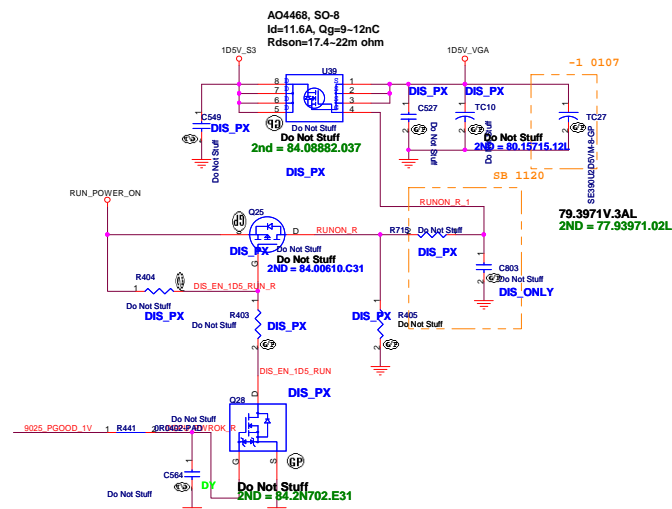
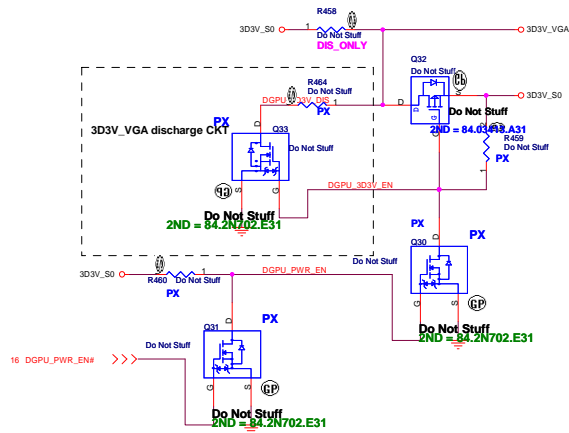


Test Point放在Dimm Door打開可量測處

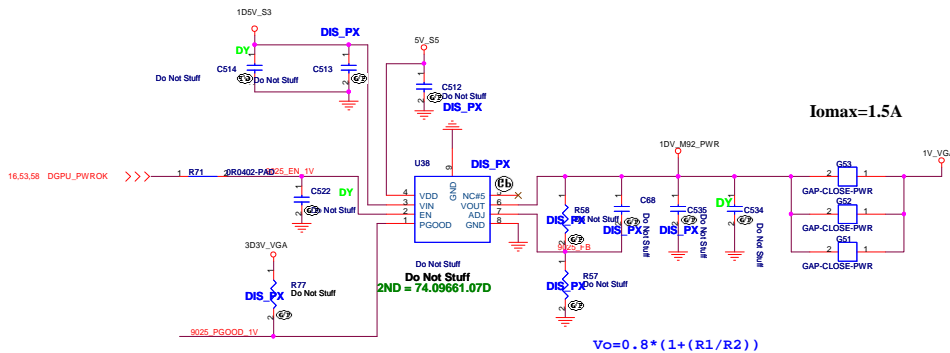
Pre UMA

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Title	
AFTE TP	
Size	Document Number
	JE70-CP
Date: Tuesday, February 02, 2010	Sheet 56 of 67
Rev	-1M

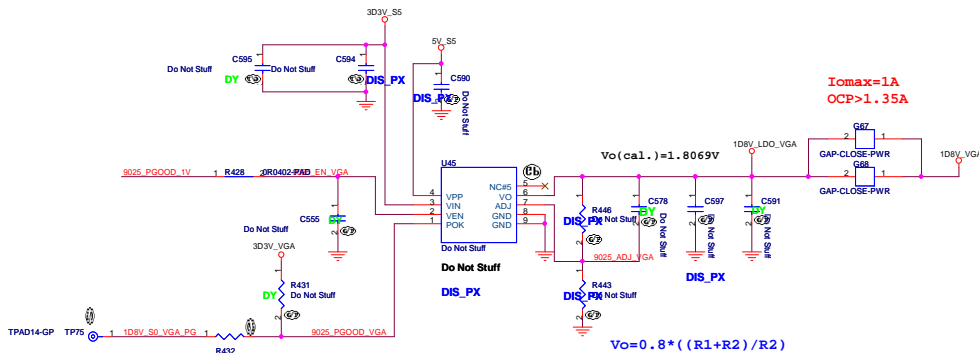
+3VS to 3.3V_DELAY Transfer



RT9025 for 1V_VGA

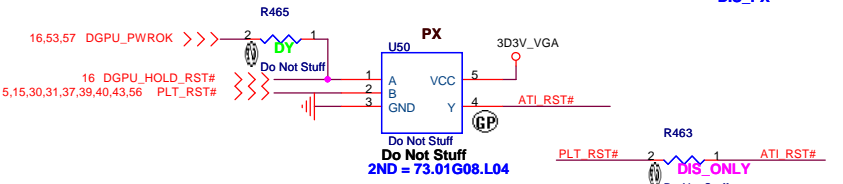
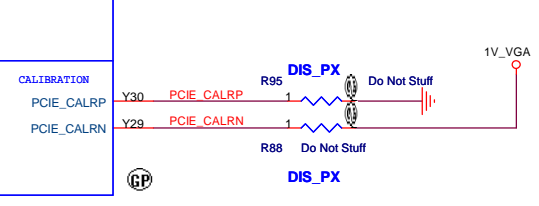
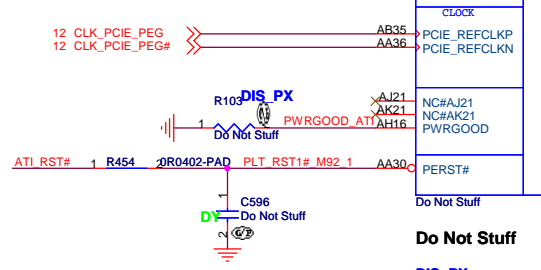
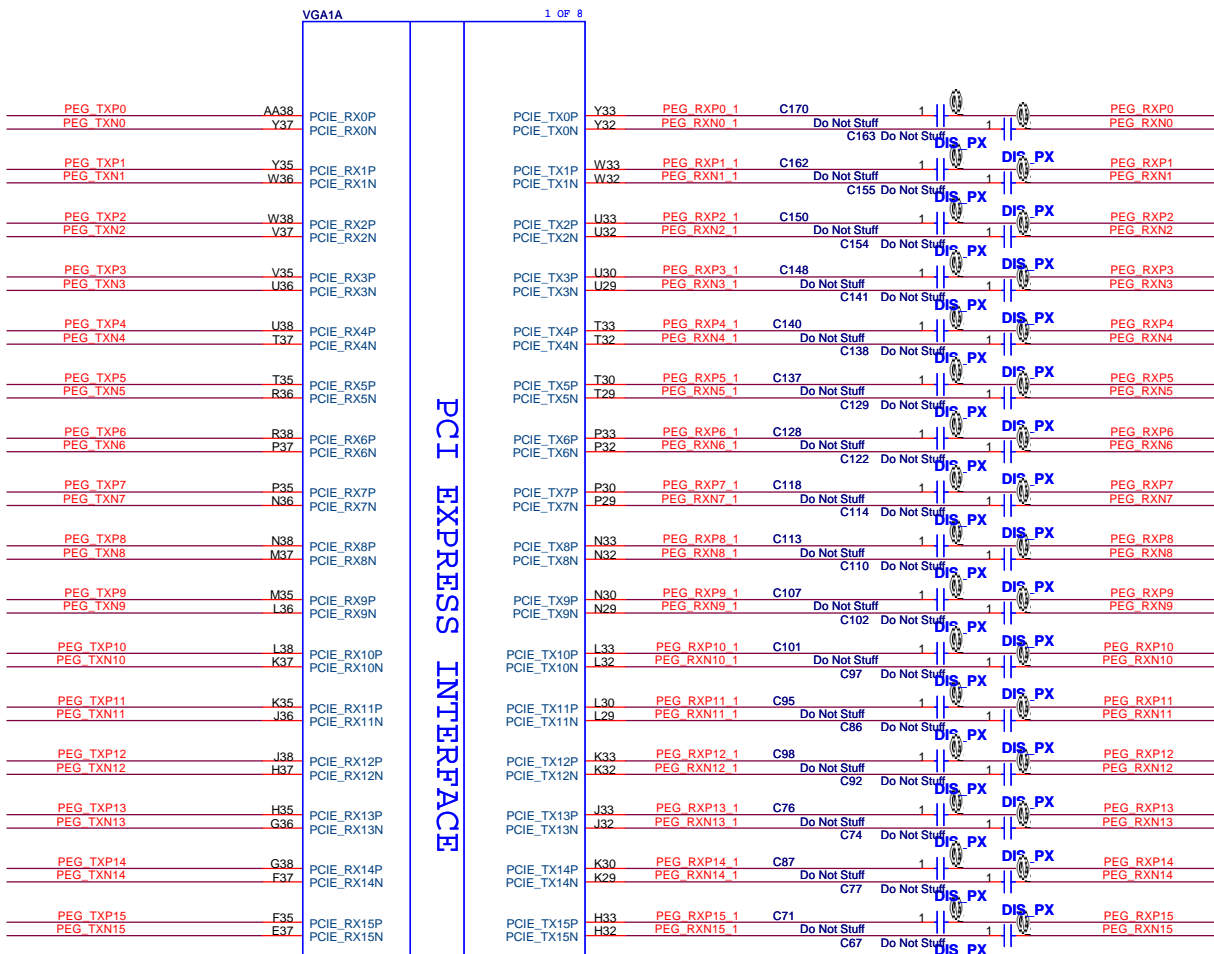


G9661 for 1D8V_VGA



4 PEG_TXP[15..0] << PEG_TXP[15..0]
 4 PEG_TXN[15..0] << PEG_TXN[15..0]

4 PEG_RXP[15..0] << PEG_RXP[15..0]
 4 PEG_RXN[15..0] << PEG_RXN[15..0]



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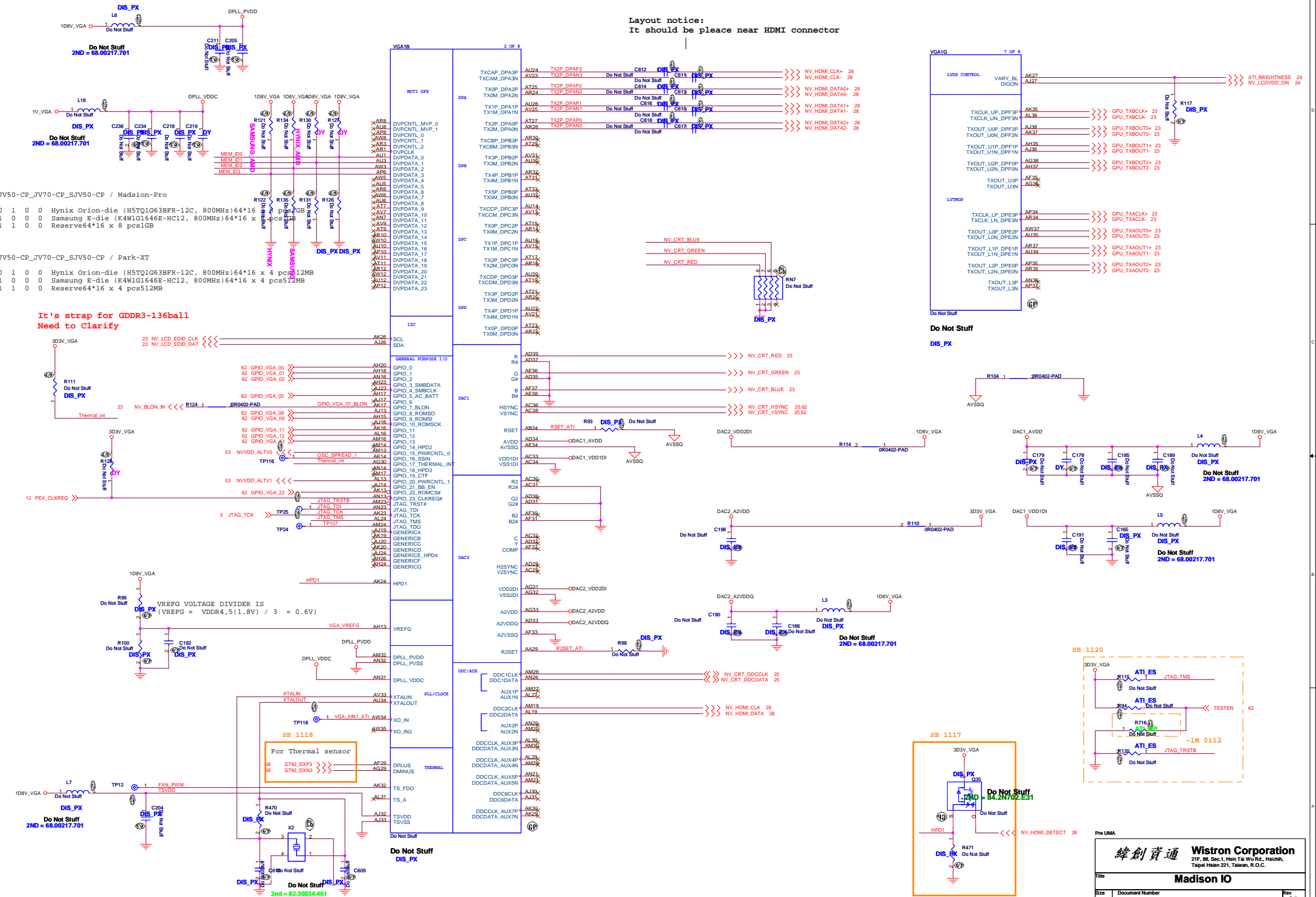
Pre UMA

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 Taipei Hsien 221, Taiwan, R.O.C.

File: **Madison PCIE**

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Layout notice:
It should be please near HDMI connector



Do Not Stuff
2ND = 68.00217.701

Do Not Stuff
2ND = 68.00217.701

JV50-CP_JV70-CP_SJV50-CP / Madsion-Pro

0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 4 pcs512MB
1 1 0 0 Reserve64*16 x 8 pcs1GB

JV50-CP_JV70-CP_SJV50-CP / Park-XT

0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16 x 4 pcs12MB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 4 pcs512MB
1 1 0 0 Reserve64*16 x 4 pcs512MB

It's strap for GDDR3-136ball
Need to Clarify

DIS_PX

12 PEK_CLKREQ

DIS_PX

DIS_PX

DIS_PX
Do Not Stuff
2ND = 68.00217.701

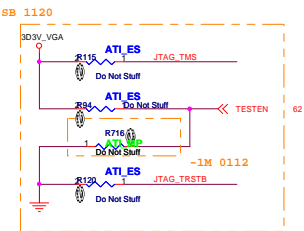
For Thermal sensor
G782_DXP3
G782_DWN3

Do Not Stuff
DIS_PX

2nd = 82.30034.461

Do Not Stuff
2ND = 84.21702.E31

DIS_PX
Do Not Stuff

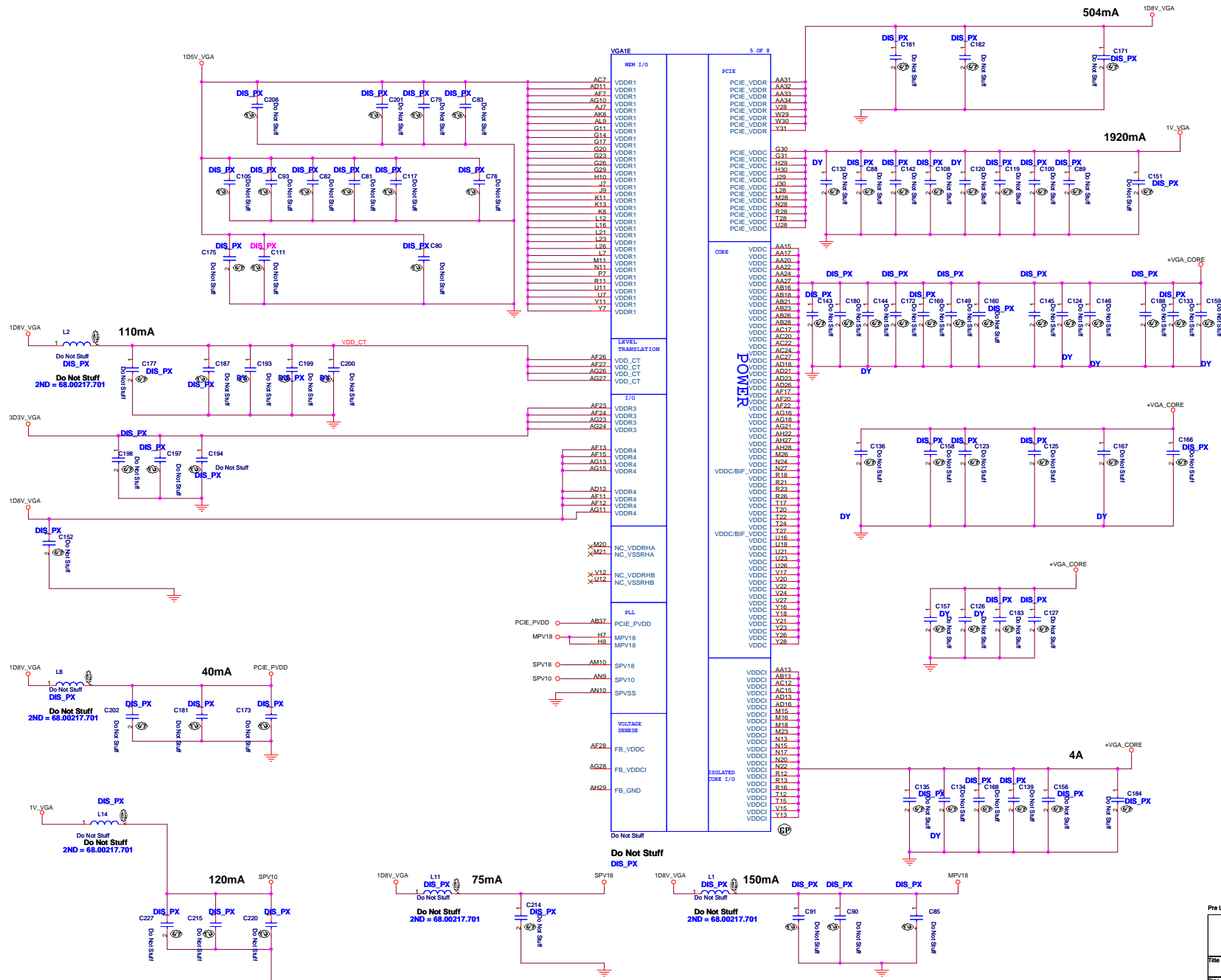


Pre UMA

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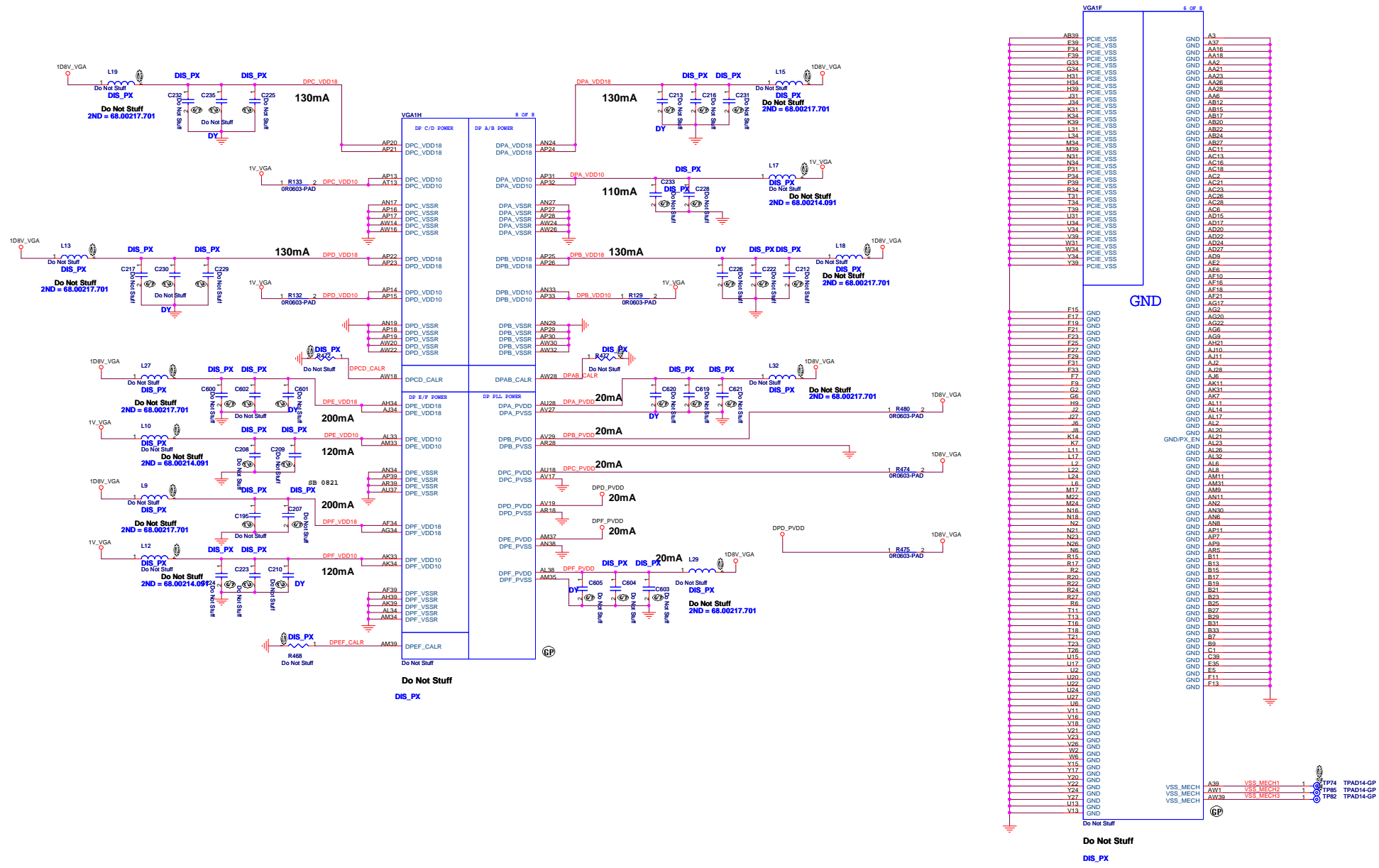
Madison IO

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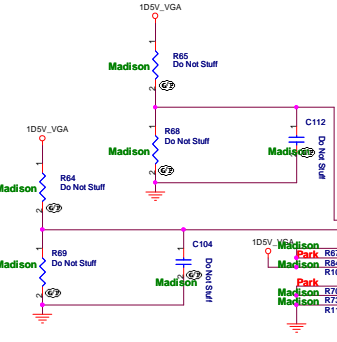
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<p>File: Madison POWER</p>		
Size	Document Number	Rev
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For SSTL-1.8/SSTL-2/DDRI/GDDR1: 0.5 * VDDRL1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDRL1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used

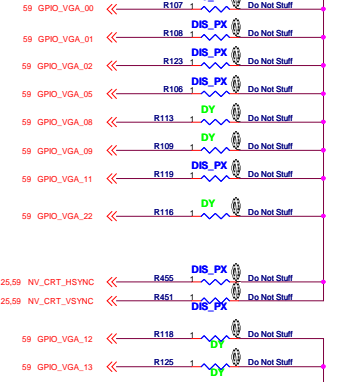
Do Not Stuff

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS
TX_PWRS_ENB (Internal PD)	GPIO0	PCIe Full Tx Output Swing Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR FULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number
128MB	x000	ST Microelectronics	M25P05A 0100
256MB	x001		M25P10A 0101
64MB	x010		M25P20 0101
32MB	x		M25P40 0101
512MB	x		M25P80 0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A 0100
2GB	x		Pm25LV010A 0101
4GB	x		



Do Not Stuff

Designator	For M97-M2	For Mannheim
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

Designator	For M97-M2	For Mannheim
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

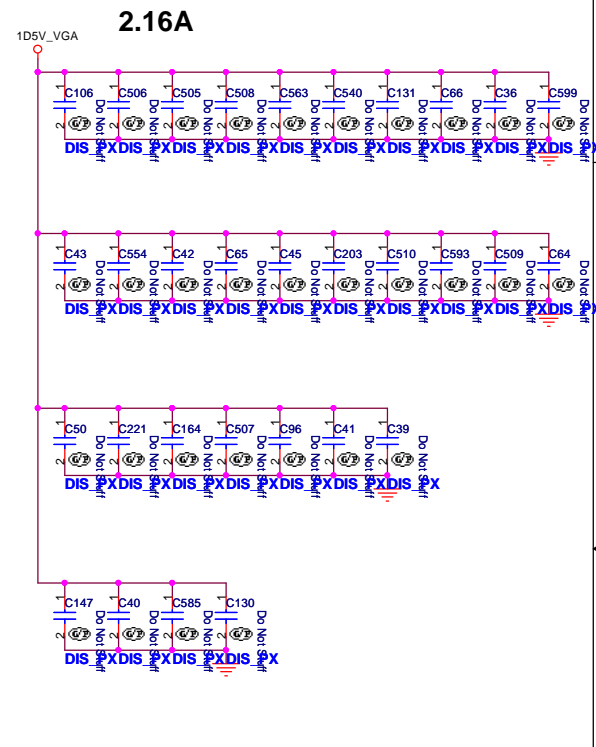
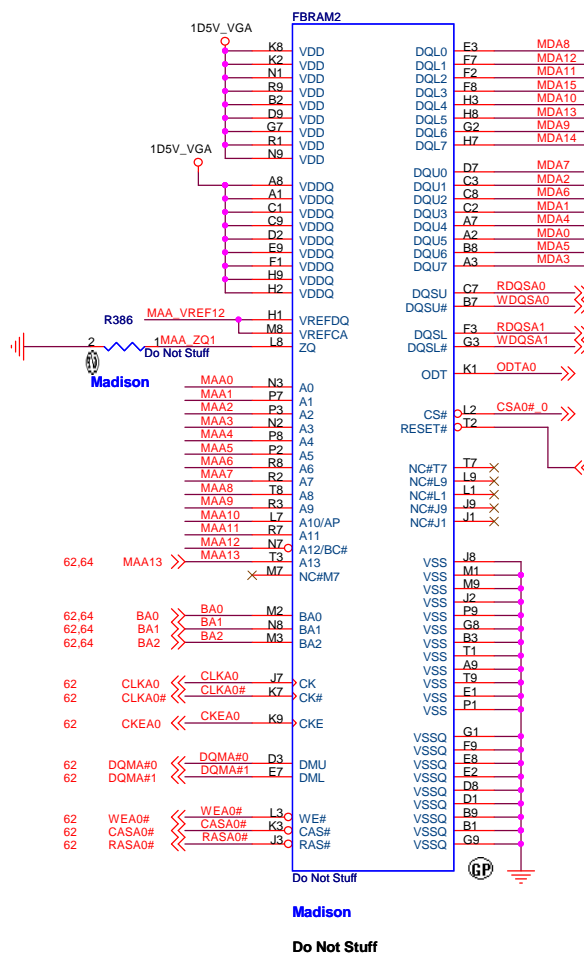
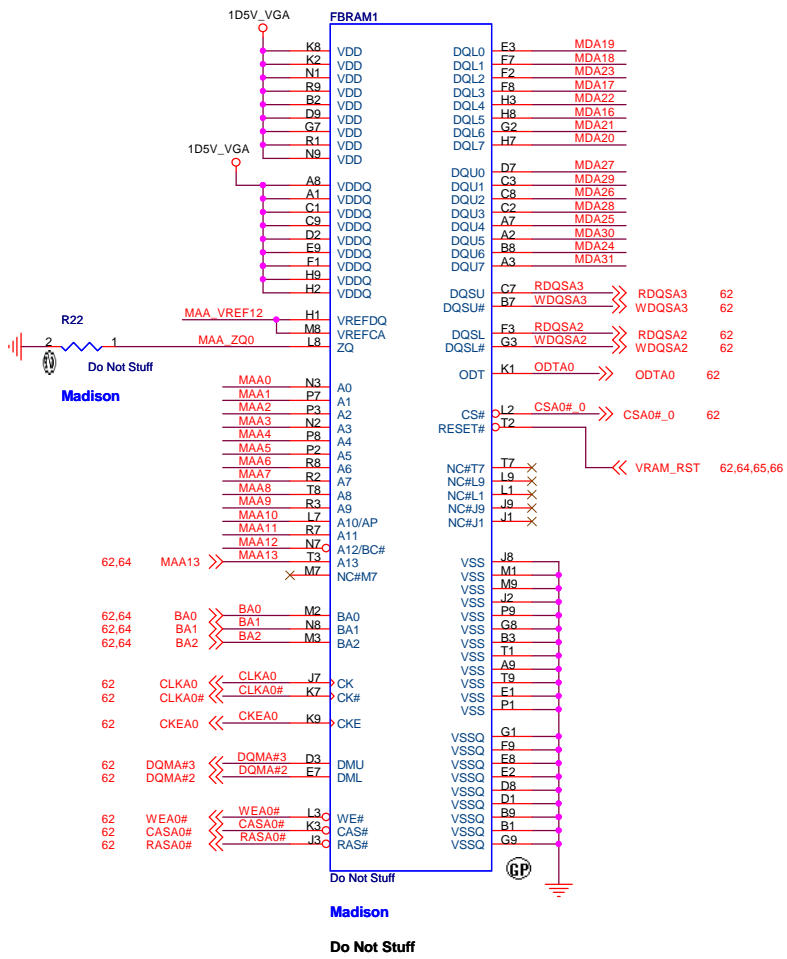
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Madison Memory / Straps

JE70-CP

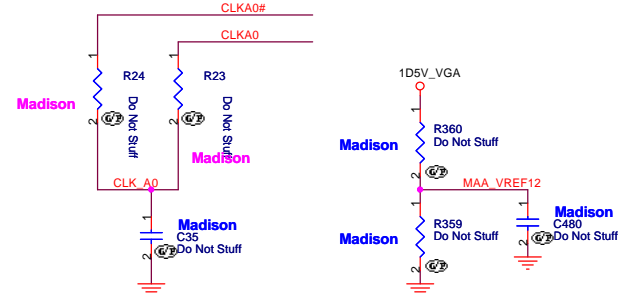
Rev 1M

DDR3



SAMSUNG: 72.41164.H0U
 HYNIX: 72.51G63.C0U

- 62,64 DQMA#[0..7] <<>
- 62,64 RDQSA#[0..7] <<>
- 62,64 WDOQA#[0..7] <<>
- 62,64 MAA[0..12] <<
- 62,64 MDA[0..63] <<>



Pre UMA

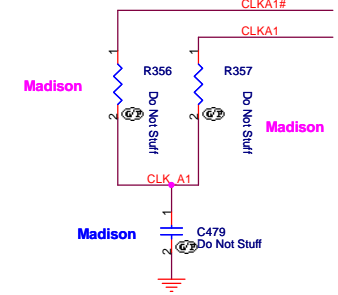
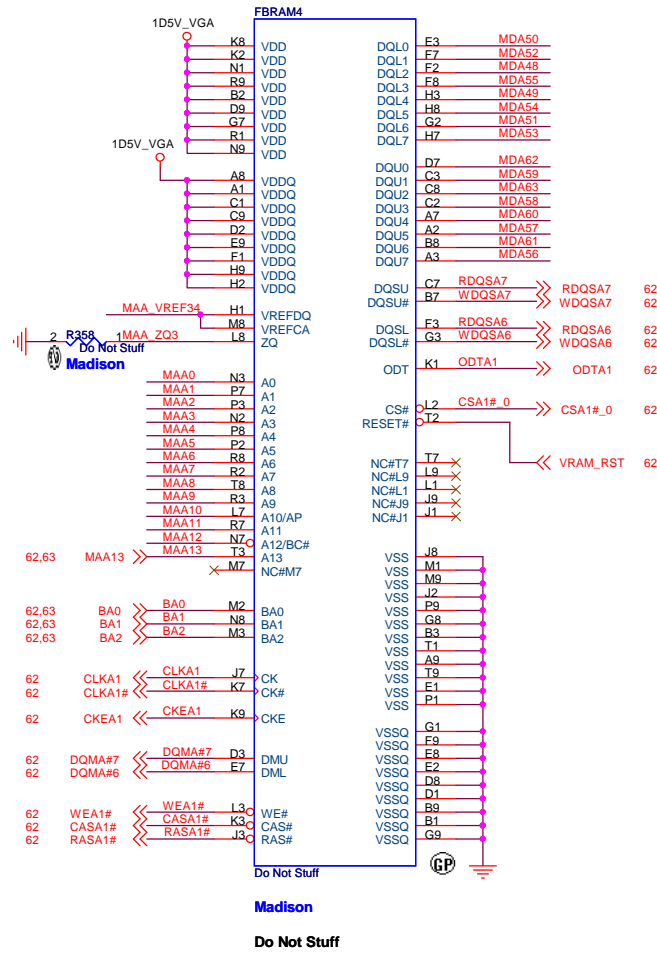
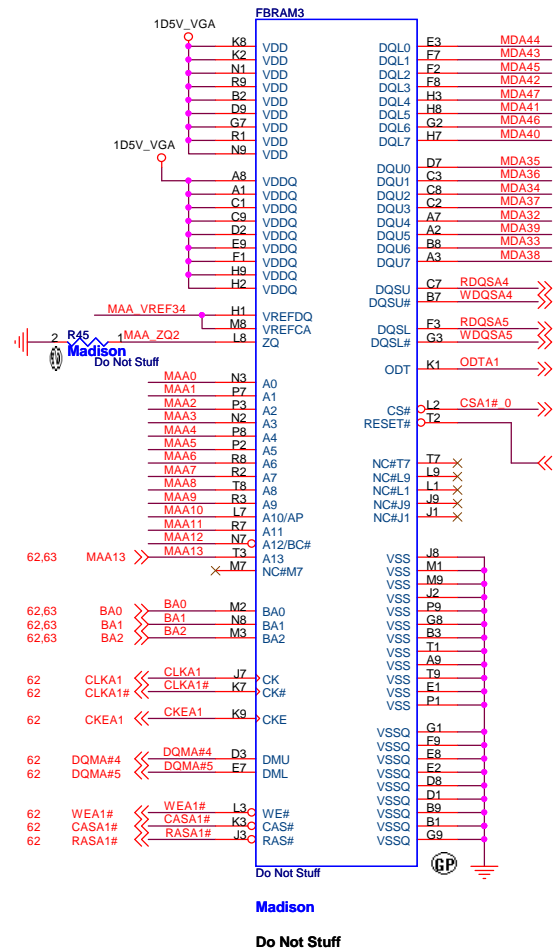
緯創資通 Wistron Corporation
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Title: **VRAM(1/4)**

Size: A3 Document Number: **JE70-CP** Rev: **-1M**

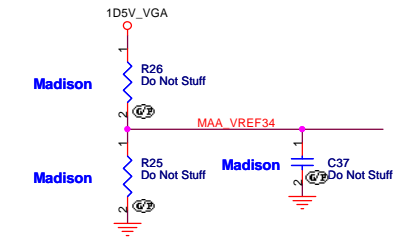
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DDR3



SAMSUNG: 72.41164.H0U
 HYNIX: 72.51G63.C0U

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- 62,63 RDQSA#[0..7] <<>
- 62,63 WDQSA#[0..7] <<>
- 62,63 MAA#[0..12] <<
- 62,63 MDA#[0..63] <<>



Pre UMA

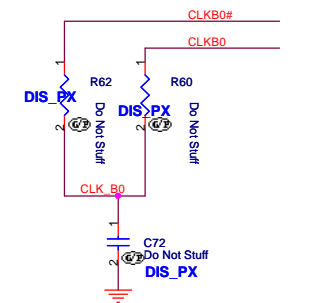
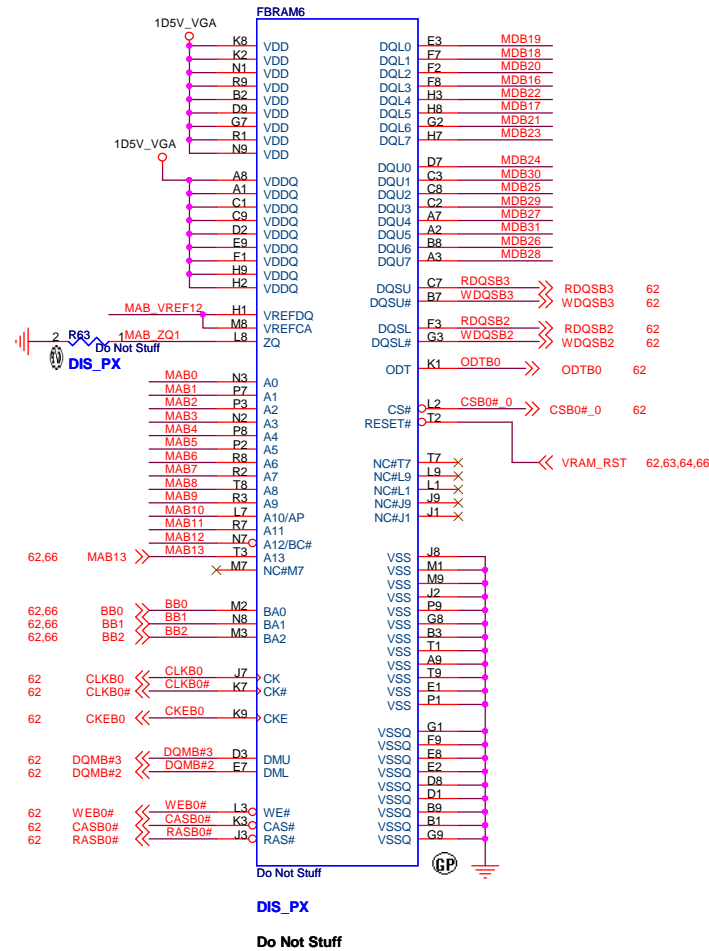
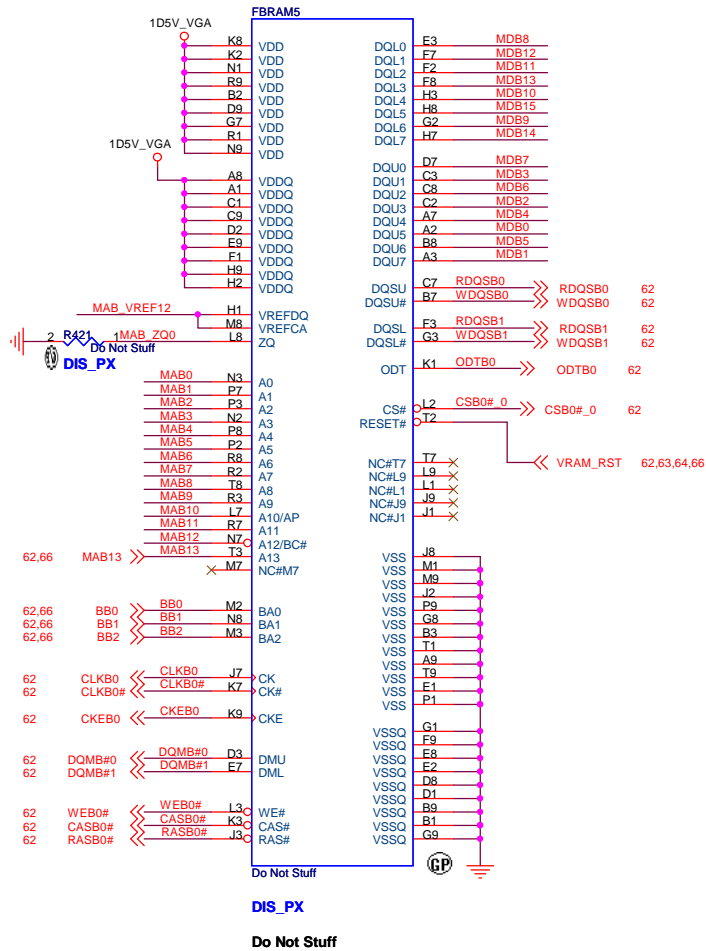
緯創資通 Wistron Corporation
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Title: **VRAM(2/4)**

Size: A3 Document Number: **JE70-CP** Rev: -1M

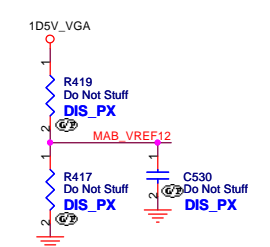
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DDR3



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

- 62,66 DQMB#0..7] <<>
- 62,66 RDQSB#0..7] <<>
- 62,66 WDQSB#0..7] <<>
- 62,66 MAB#0..12] <<>
- 62,66 MDB#0..63] <<>



Pre UMA

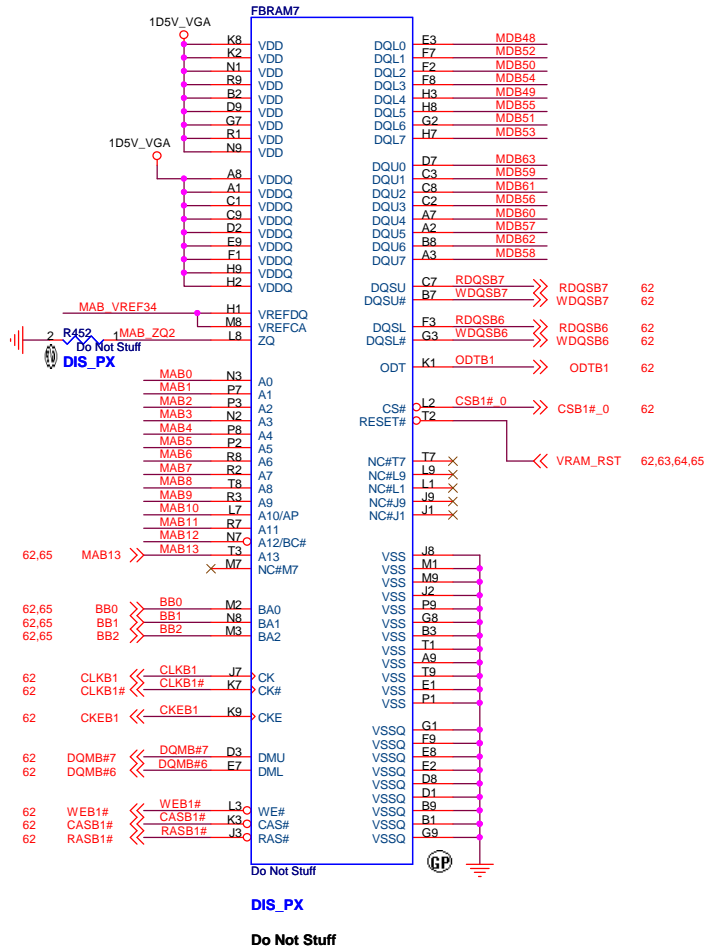
緯創資通 Wistron Corporation
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Title: **VRAM(3/4)**

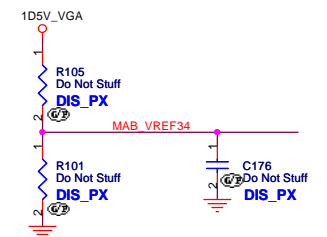
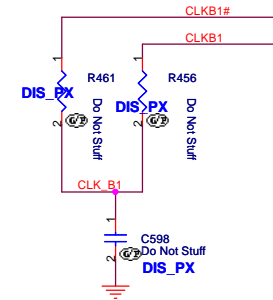
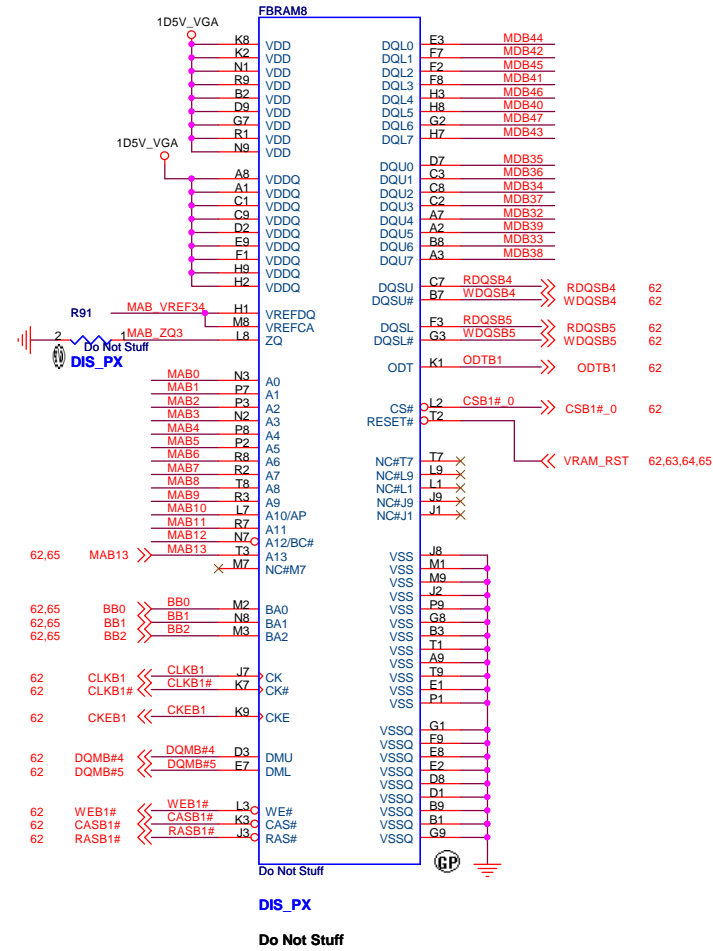
Size: A3 Document Number: **JE70-CP** Rev: **-1M**

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DDR3



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



- 62,65 DQMB#[0..7] <<>
- 62,65 RDQSB#[0..7] <<>
- 62,65 WDQSB#[0..7] <<>
- 62,65 MAB#[0..12] << MAB#[0..12]
- 62,65 MDB#[0..63] <<> MDB#[0..63]

Pre UMA

緯創資通		Wistron Corporation	
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VRAM(4/4)			
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Title			
Modify History			
Size	Document Number	Rev	
	JE70-CP	-1M	
Date: Tuesday, February 02, 2010		Sheet 67	of 67