Intel Huron River Platform – N53SV

- Huron River Platform Block Diagram
- Cougar Point Overview
- N53SV Architecture
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- [Repair reference] - Vcore Problems
- [Repair reference] - Battery Charging problems
- [Repair reference] - LAN problems
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- Q & A

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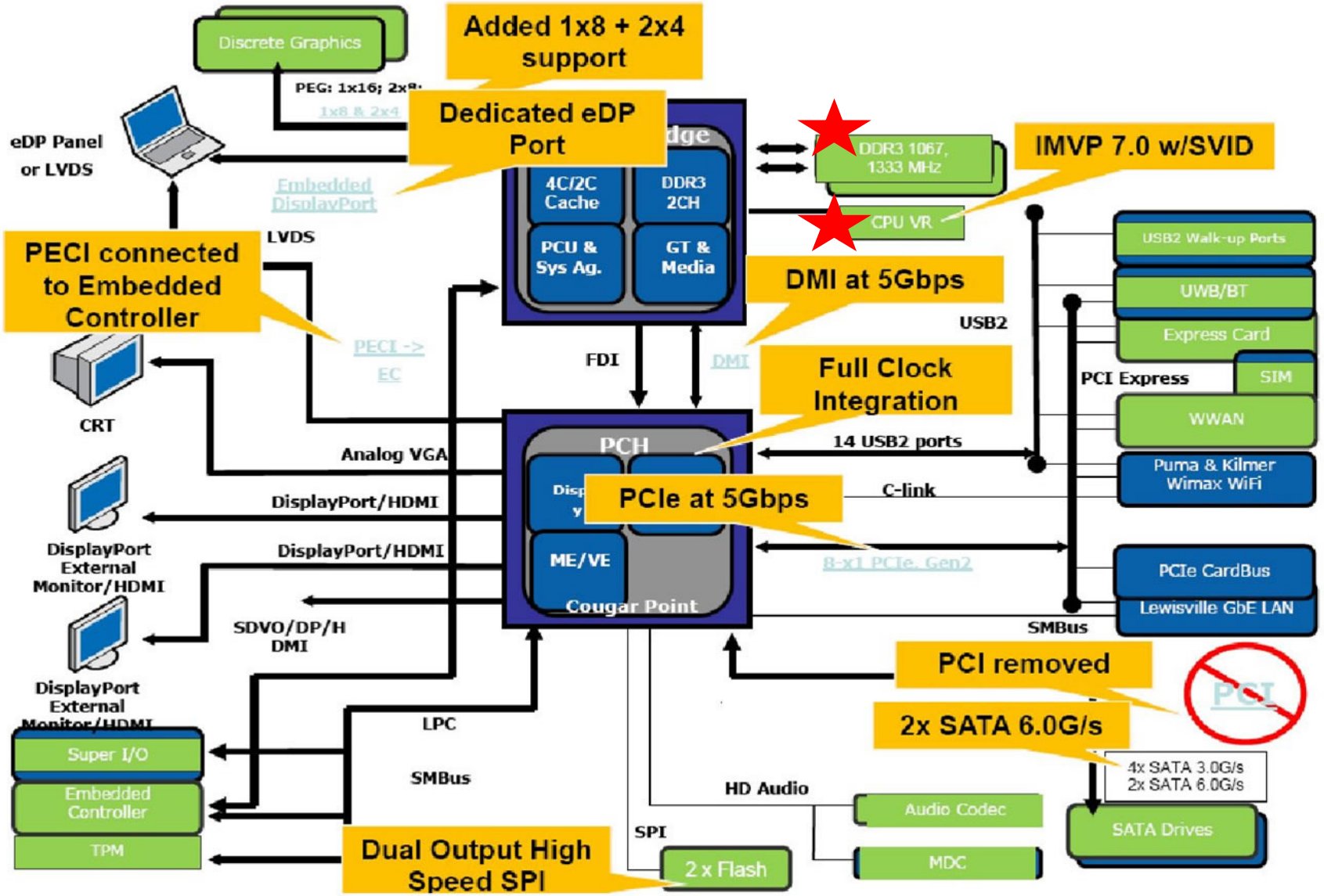
Huron River platform



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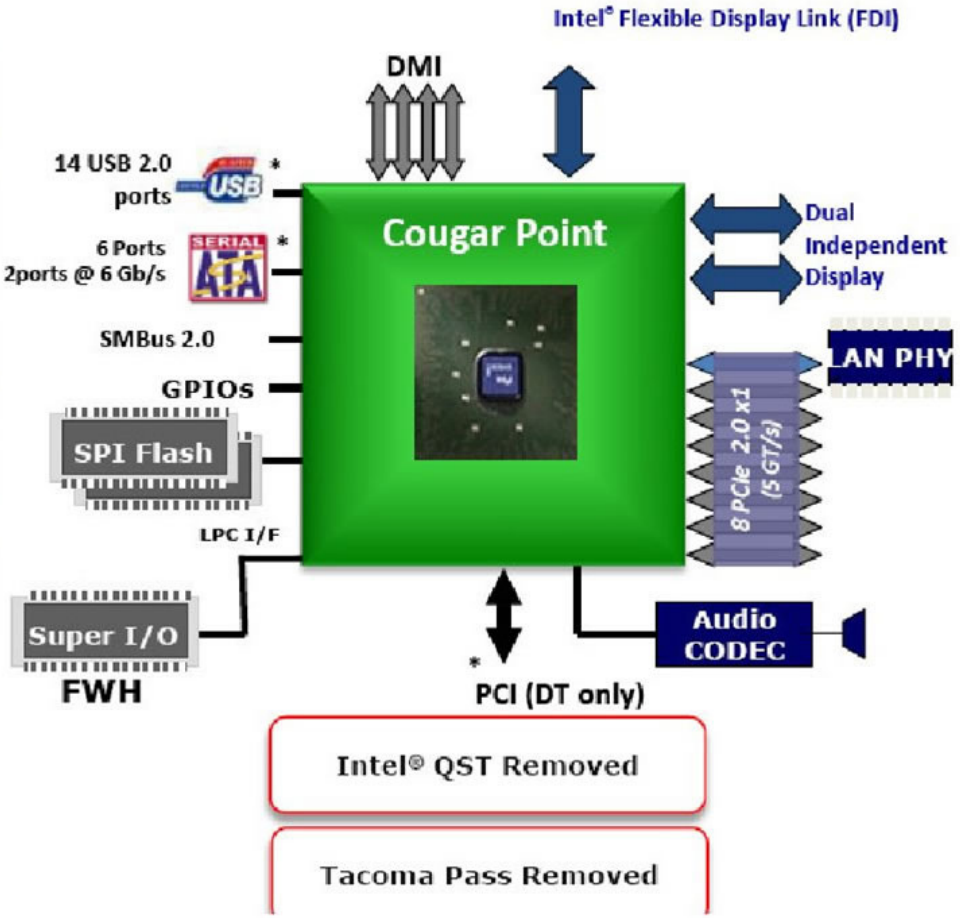
Cougar Point PCH

New Features

- 6 SATA ports (Ports 0 & 1 6Gb/s Support)
- Supports Intel® Rapid Storage Technology 10.0
- Full Clock Integration
- 8 PCIe 2.0 x1 (5Gb/s) Ports
- Cost Reduced HDMI Level Shifter



Continuing Features

- Digital & Analog Display Interfaces
- Intel® Virtualization Technology for Directed I/O
- Intel® Rapid Recover Technology, eSATA Port Disable
- Flexible LAN PCIe Attach
- Intel® High Definition Audio
- Hardware- Based KVM
- PAVP HD Content Protection

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Intel Huron River Platform – N53SV

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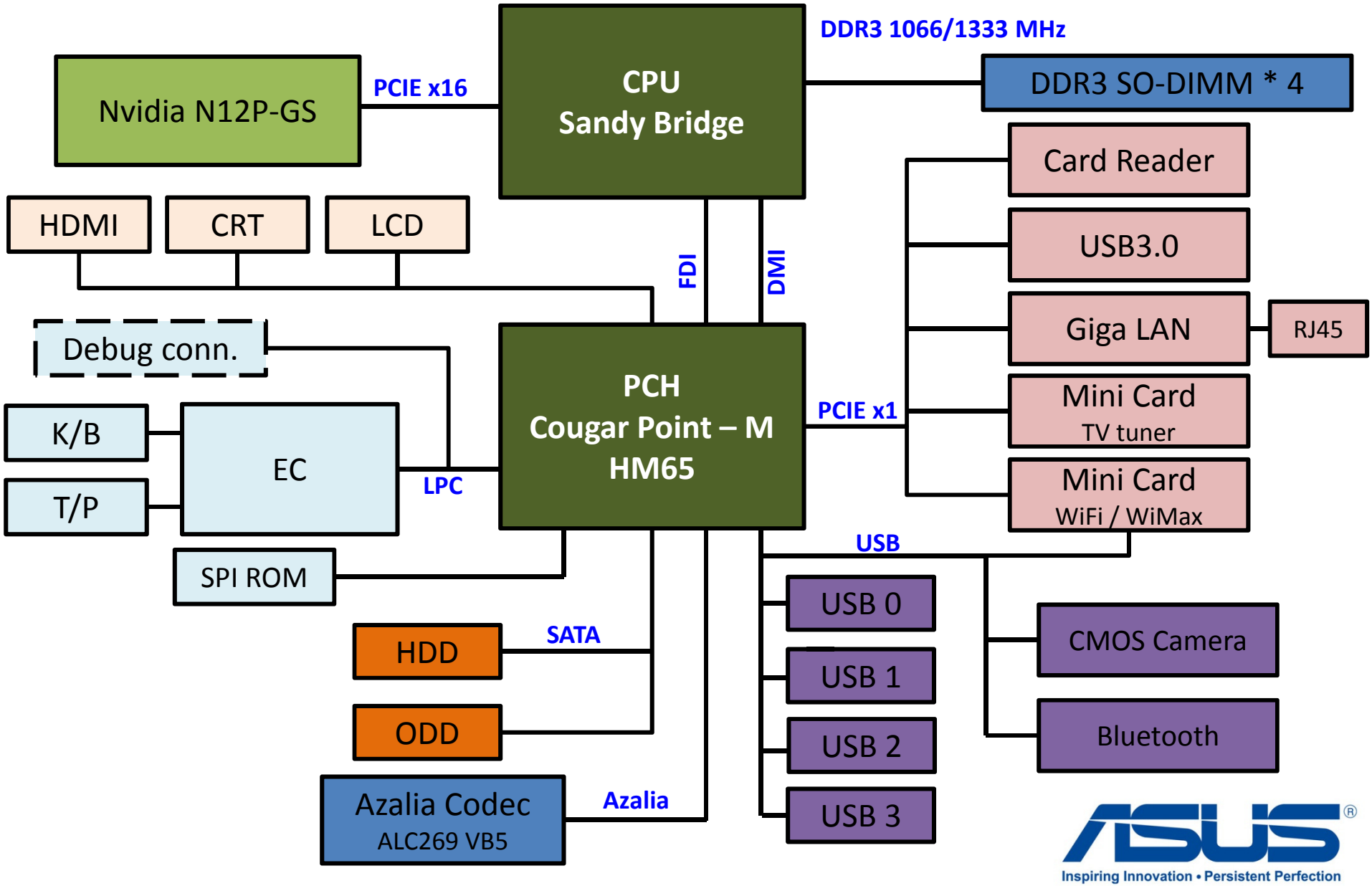
Huron River Platform – N53SV Architecture



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Intel Huron River Platform – N53SV

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No power

- Power on sequence (*AC-In mode*)
- Power on sequence analysis

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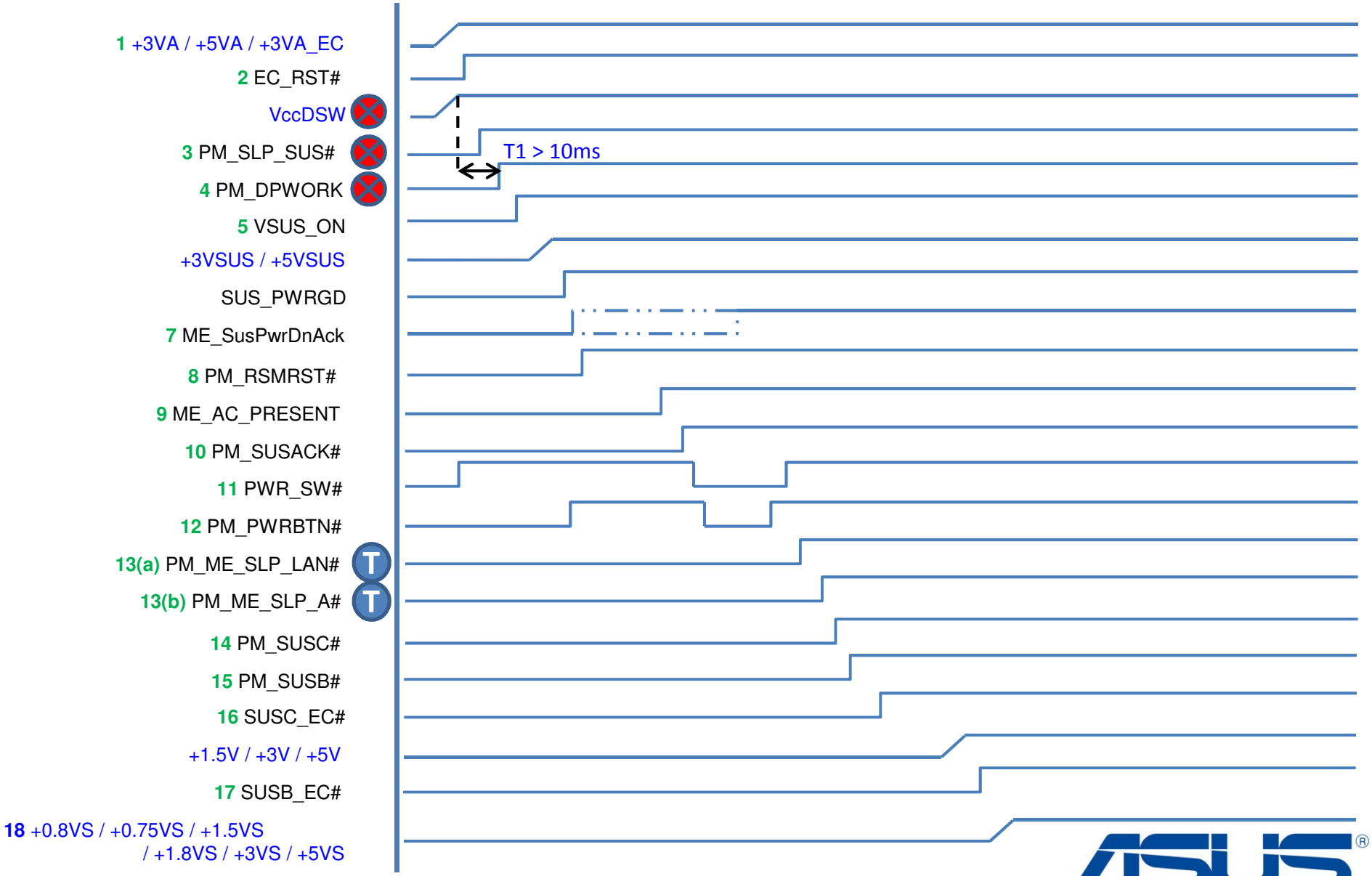
➢ Power on sequence



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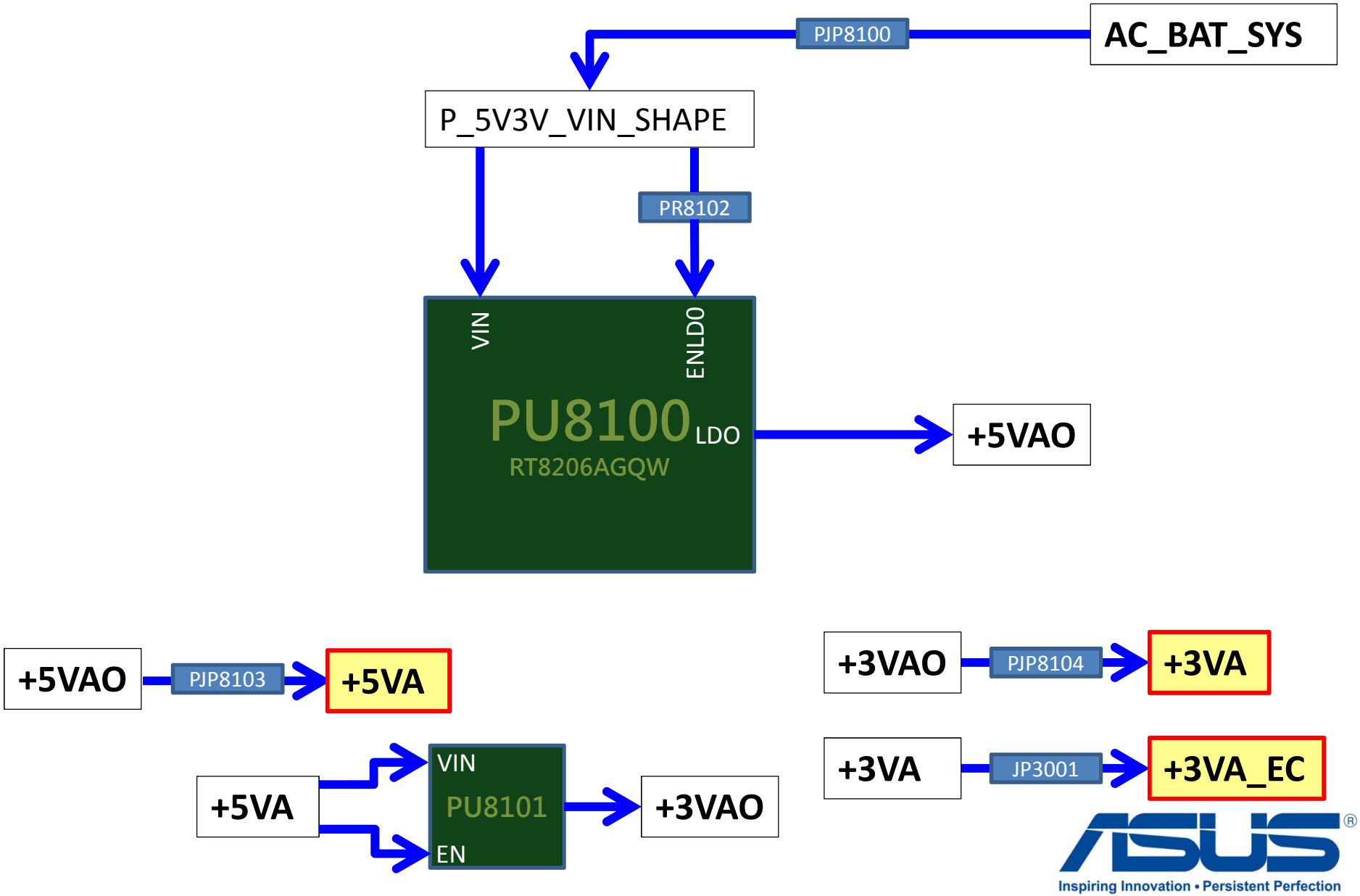
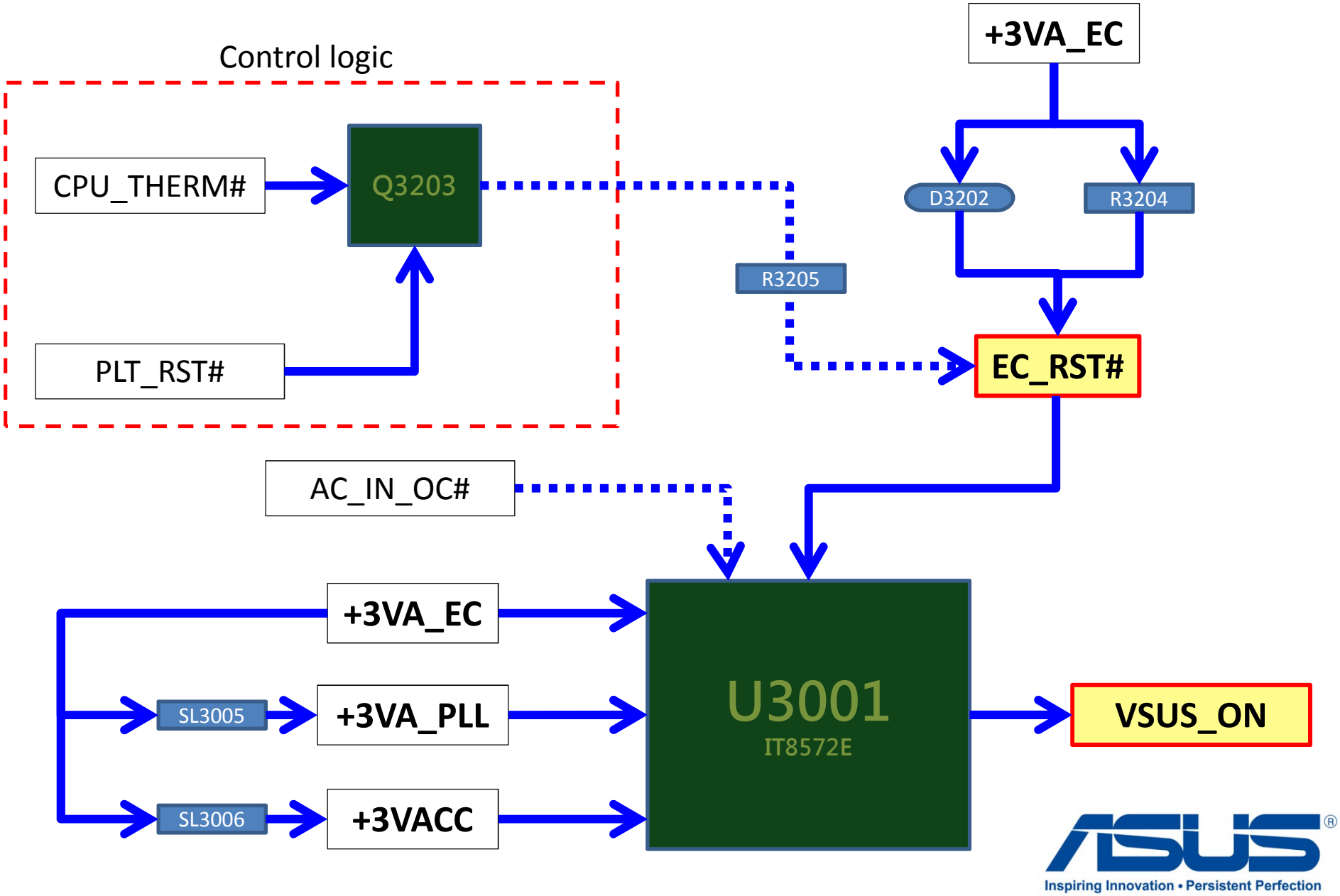
➢ Power on sequence analysis *+3VA, +5VA, +3VA_EC*



➢ Power on sequence analysis

EC_RST#, VSUS_ON



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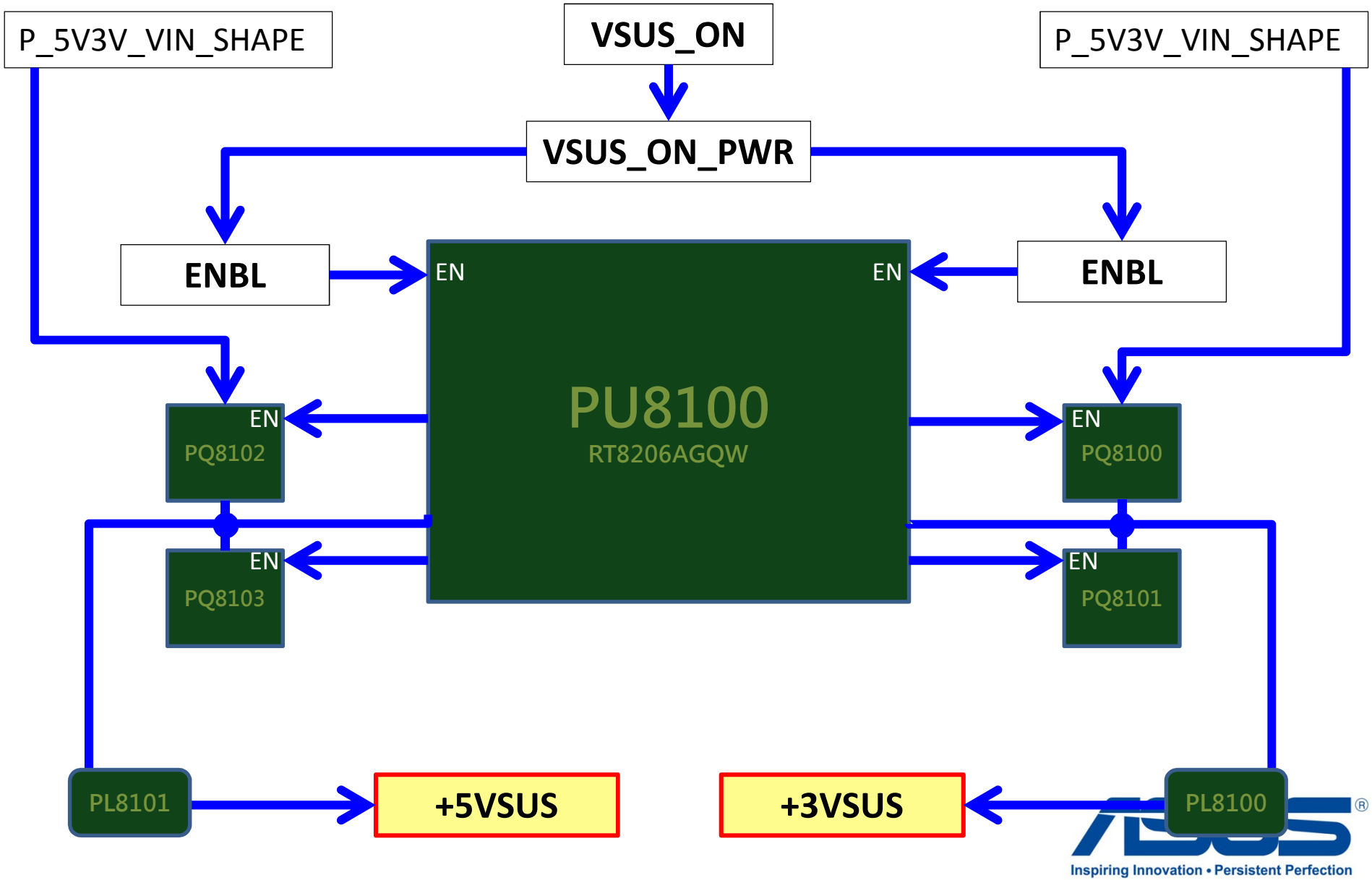
➢ Power on sequence analysis

+3VSUS, +5VSUS



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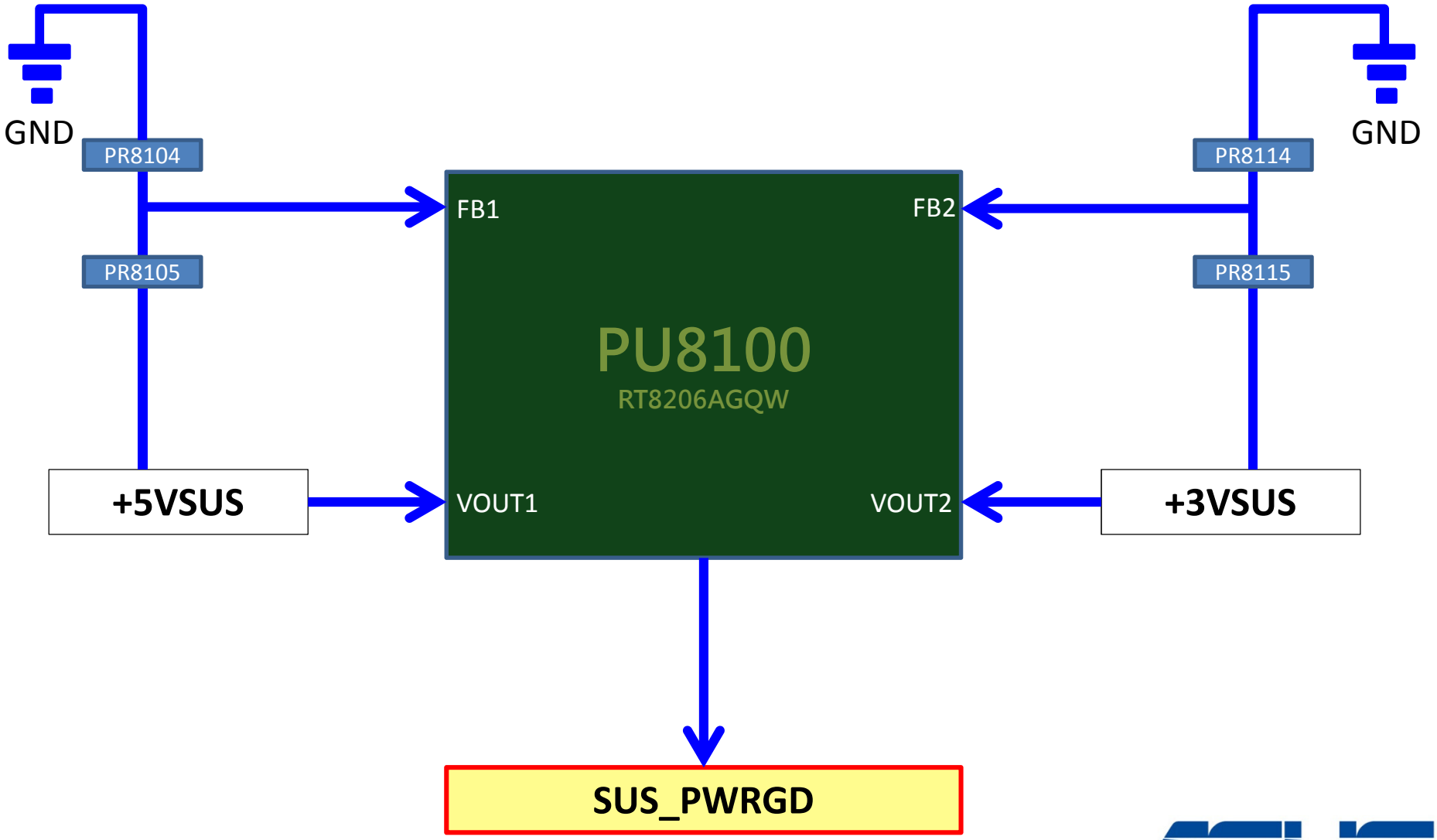
➢ Power on sequence analysis

SUS_PWRGD



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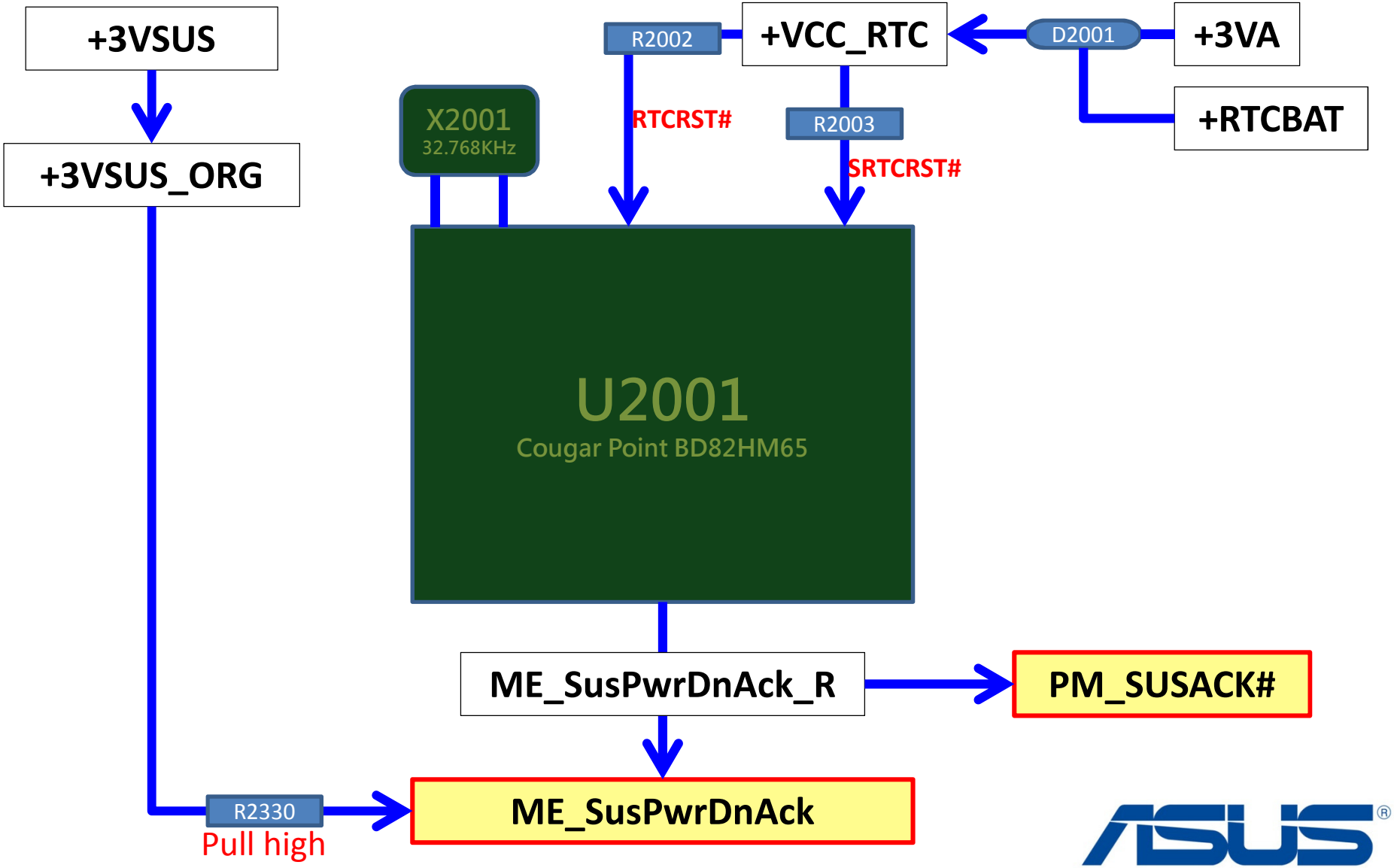
➢ Power on sequence analysis

ME_SusPwrDnAck, PMSUSACK#



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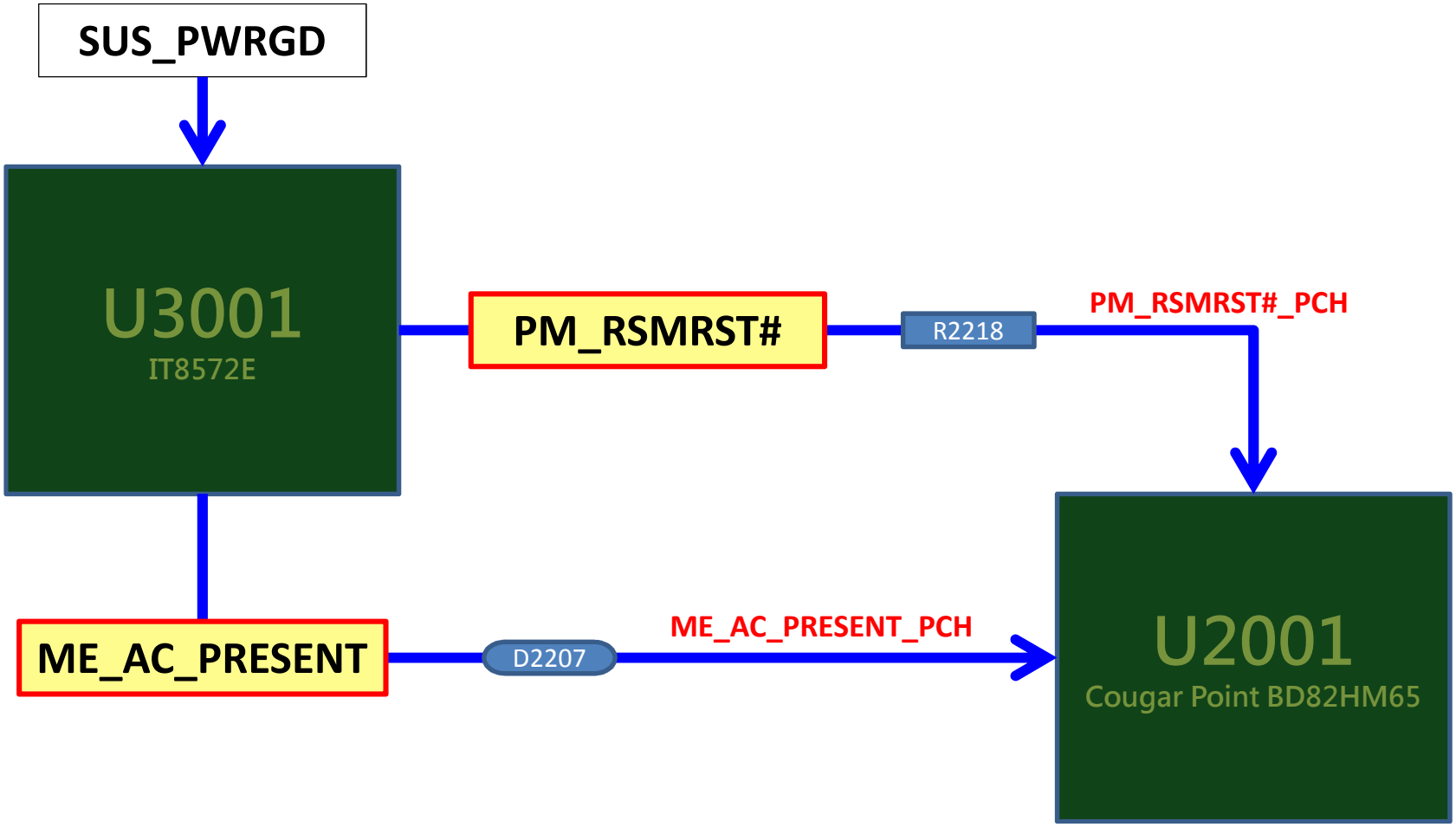
➢ Power on sequence analysis

PM_RSMRST#, ME_AC_PRESENT



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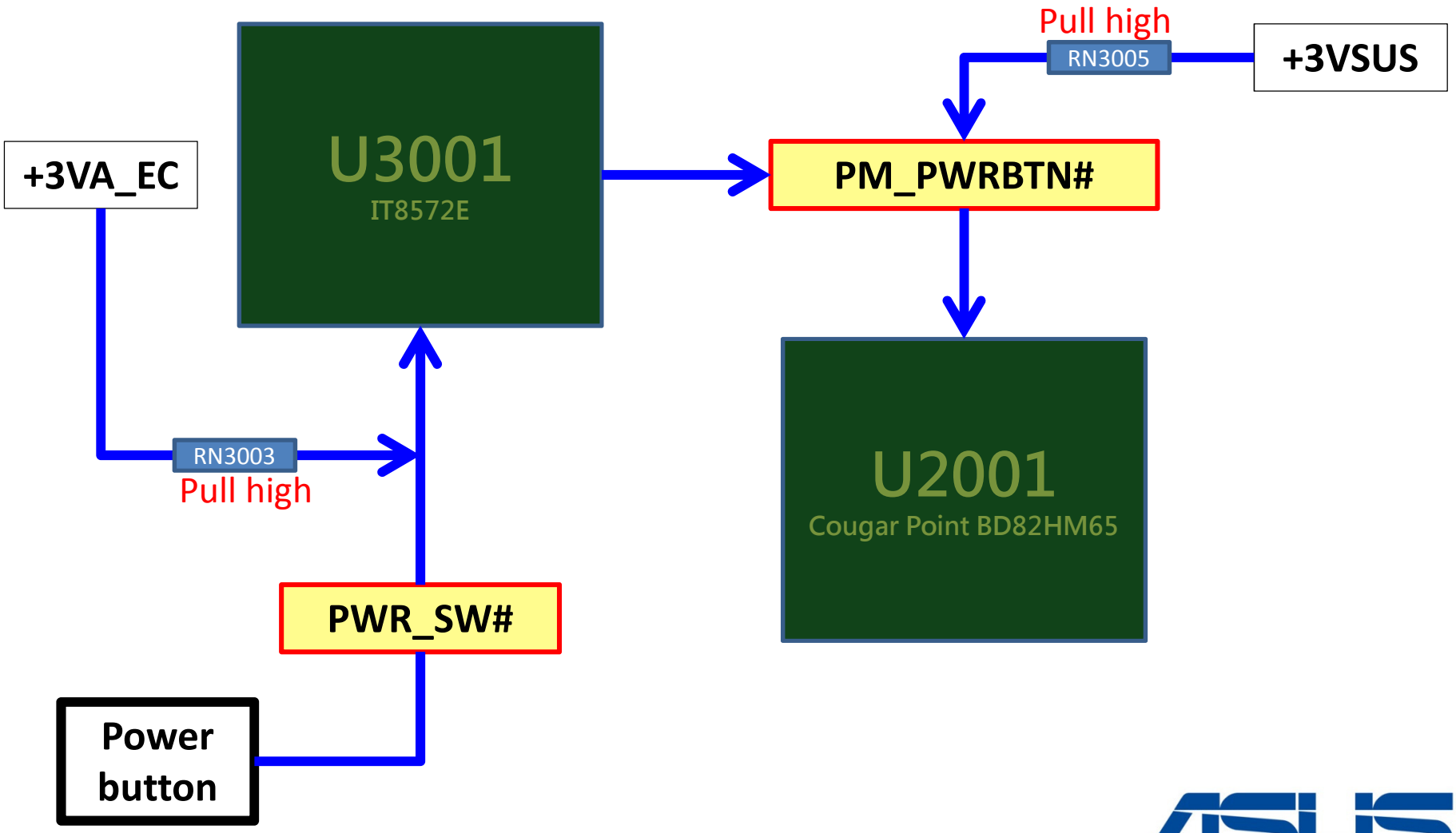
➢ Power on sequence analysis

PWR_SW#, PM_PWRBTN#



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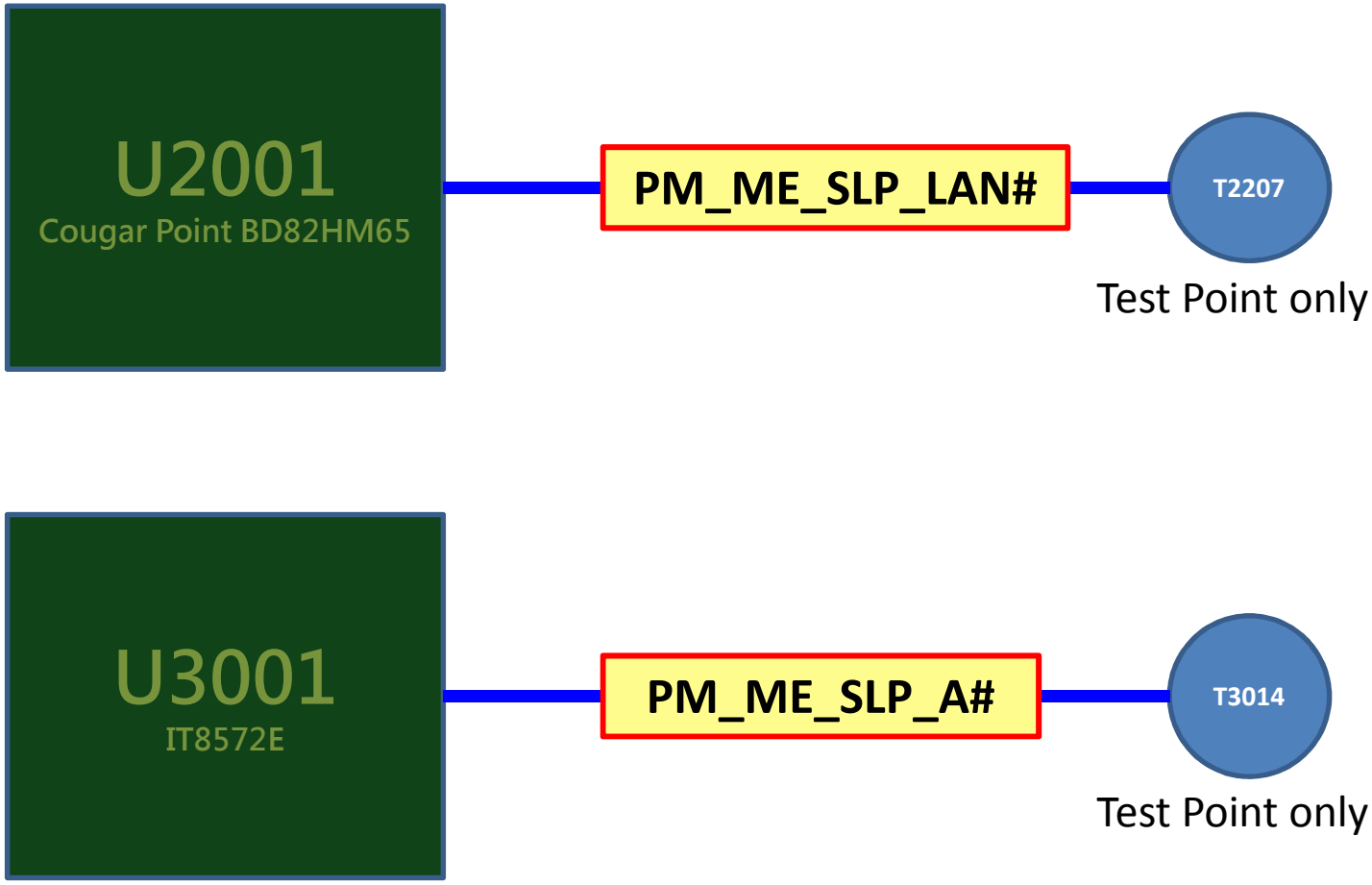
➢ Power on sequence analysis

PM_ME_SLP_LAN#, PM_ME_SLP_A#



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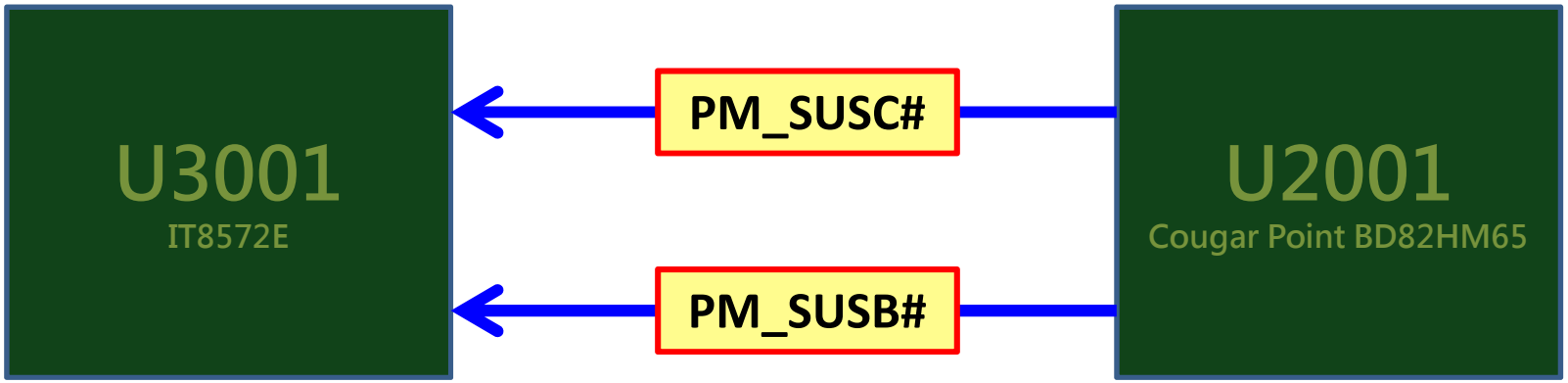
➢ Power on sequence analysis

PM_SUSC#, PM_SUSB#



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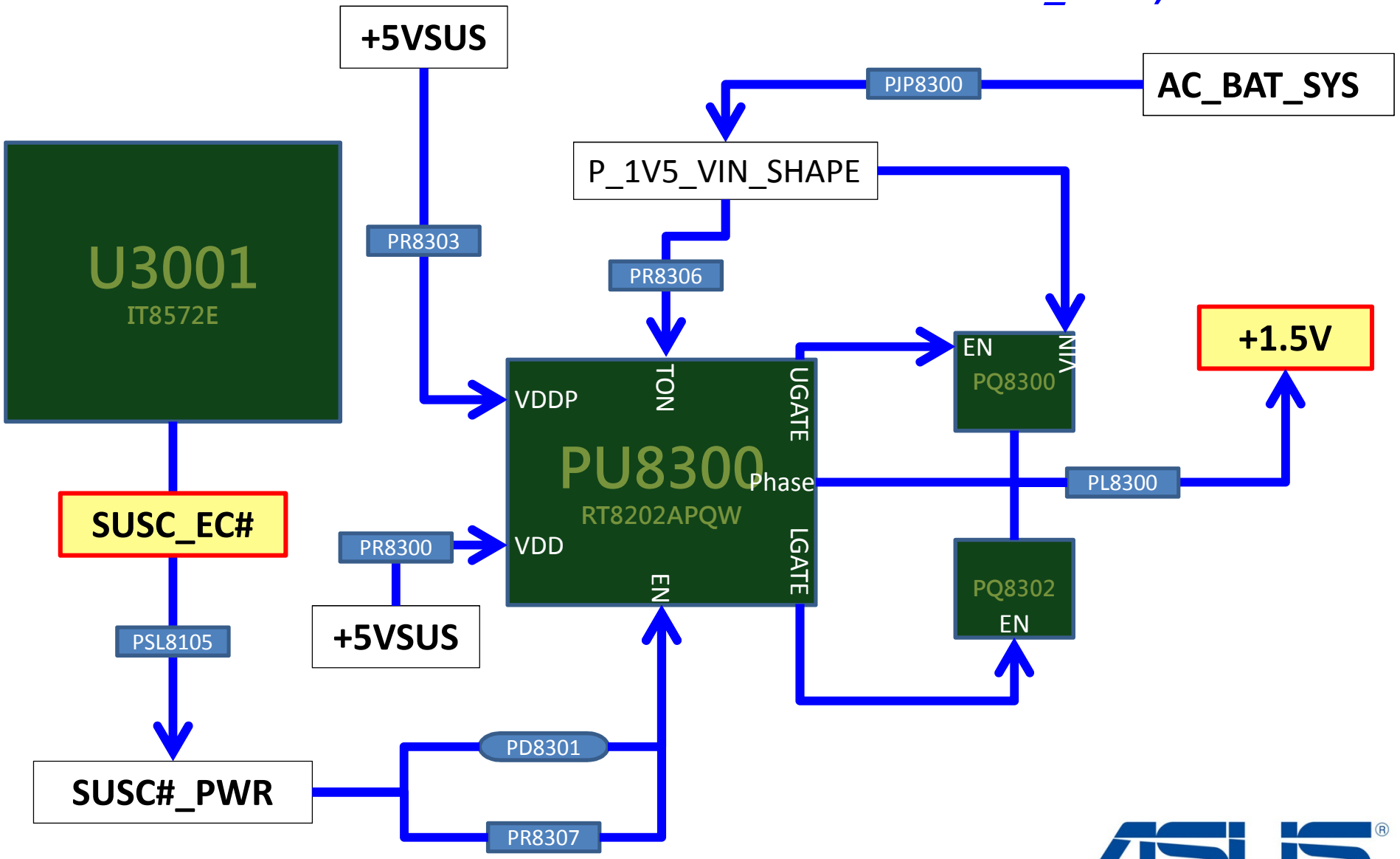
➢ Power on sequence analysis

SUSC_EC#, +1.5V



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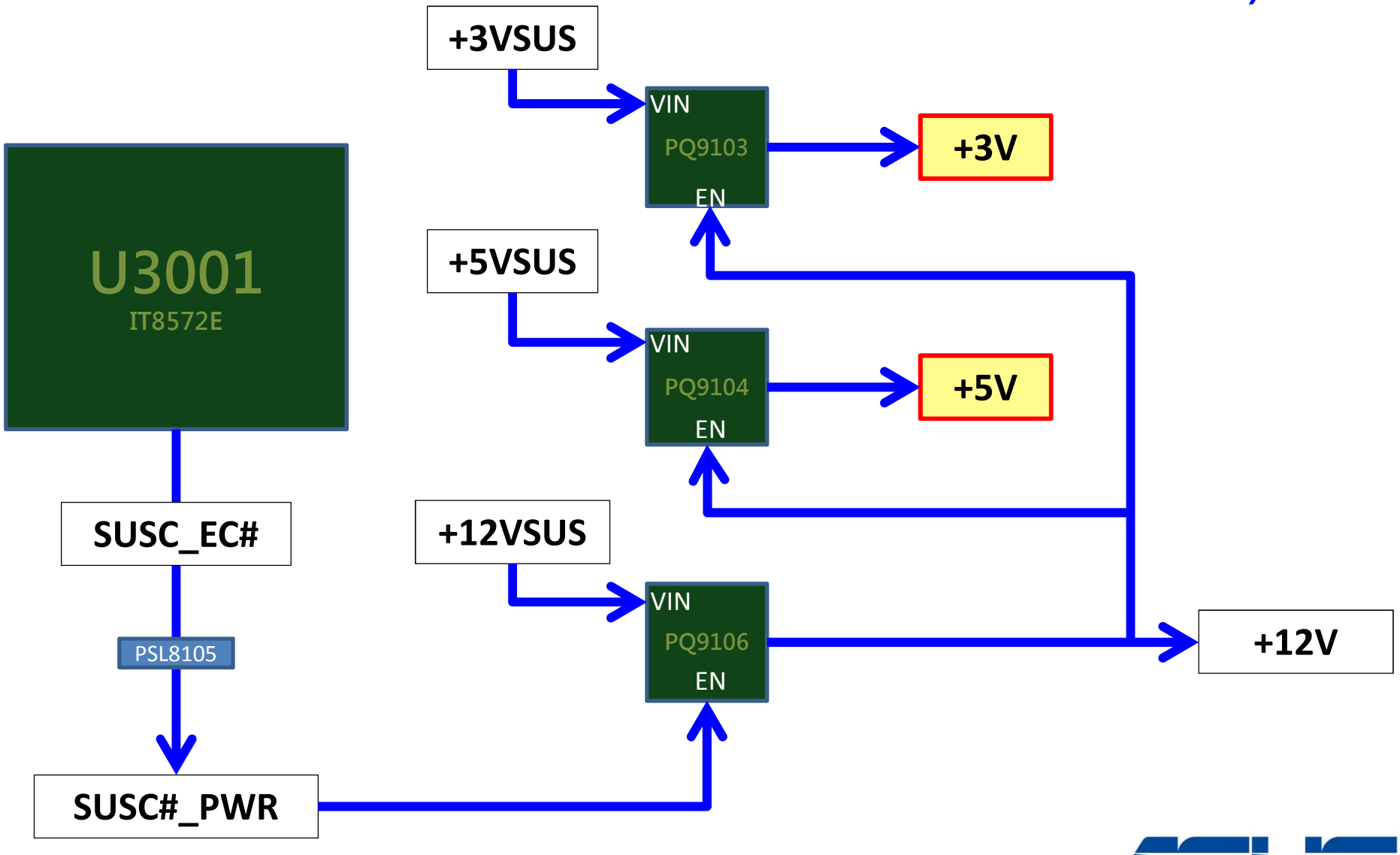
➢ Power on sequence analysis

+3V, +5V



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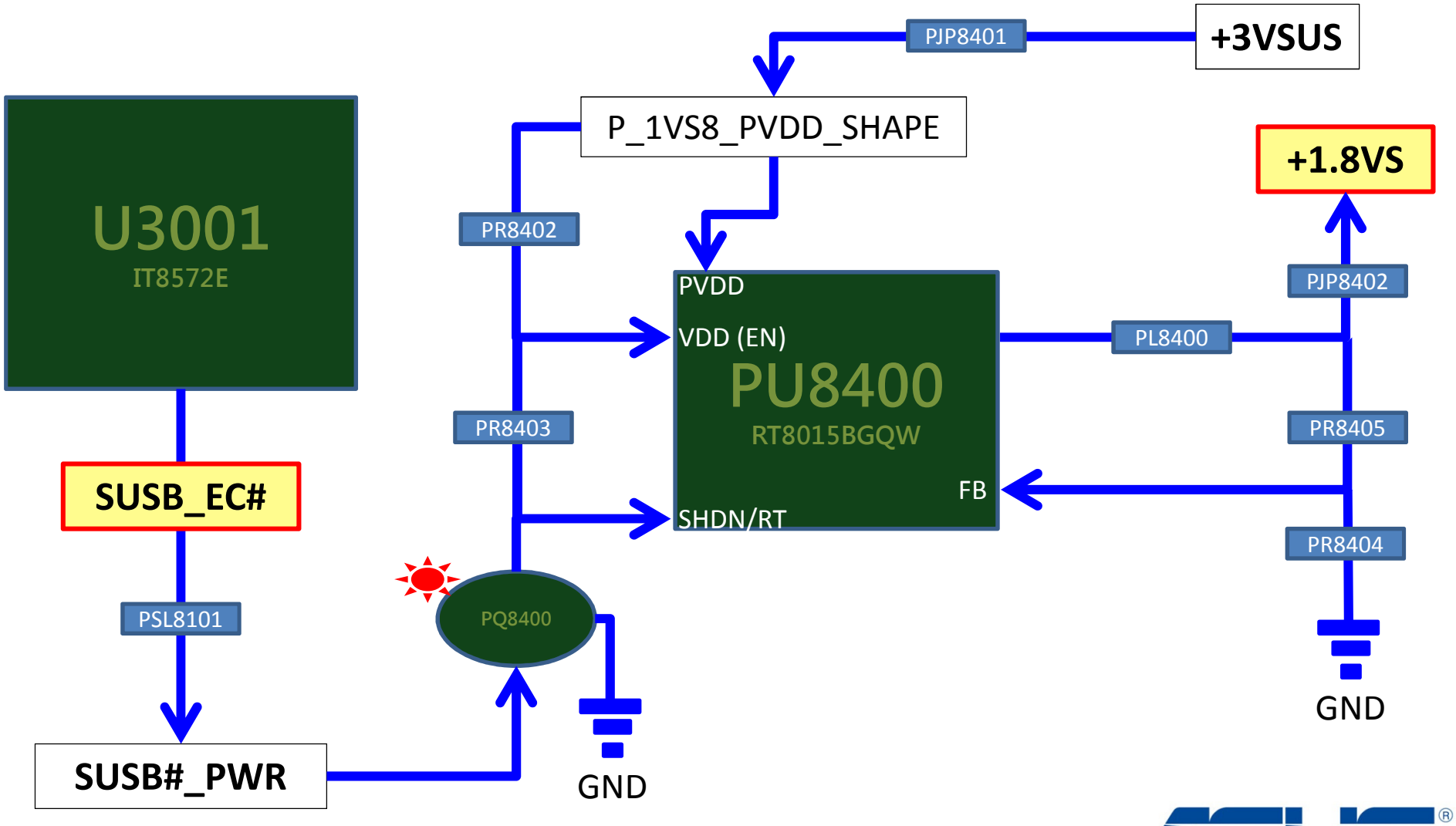
➢ Power on sequence analysis

SUSB_EC#, +1.8VS



Q8401: A transistor to be the inverter.

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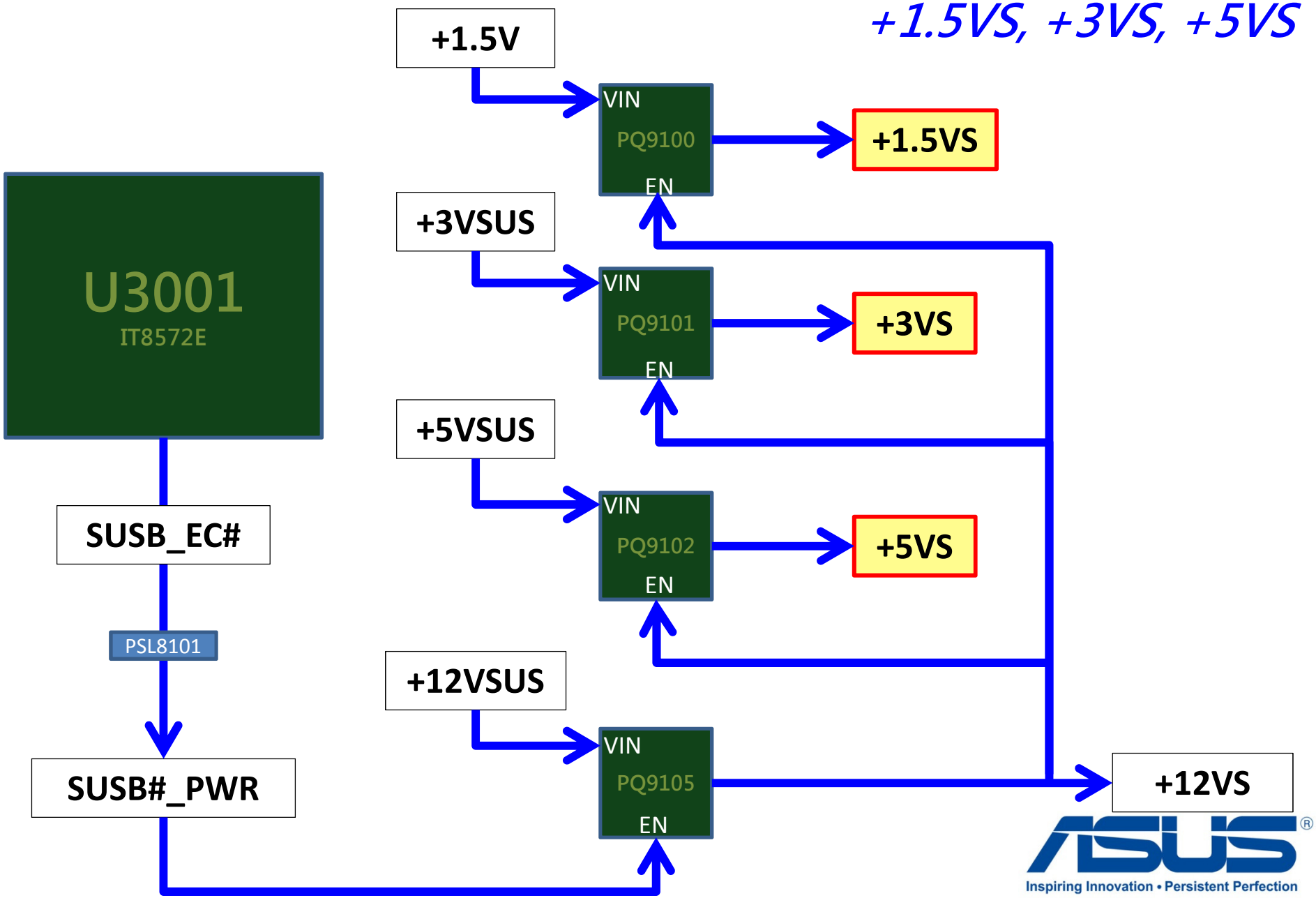
➢ Power on sequence analysis

+1.5VS, +3VS, +5VS



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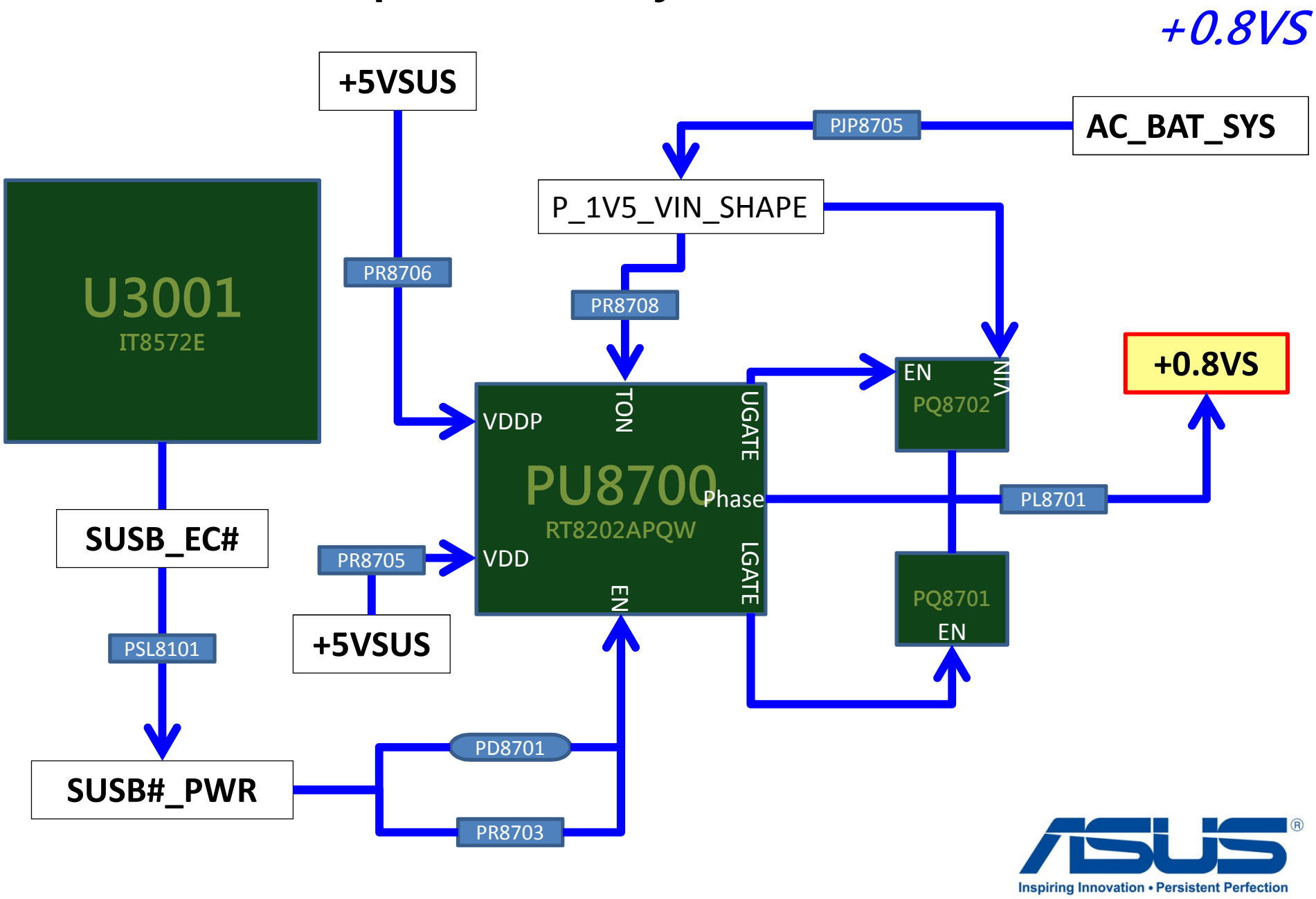
➢ Power on sequence analysis



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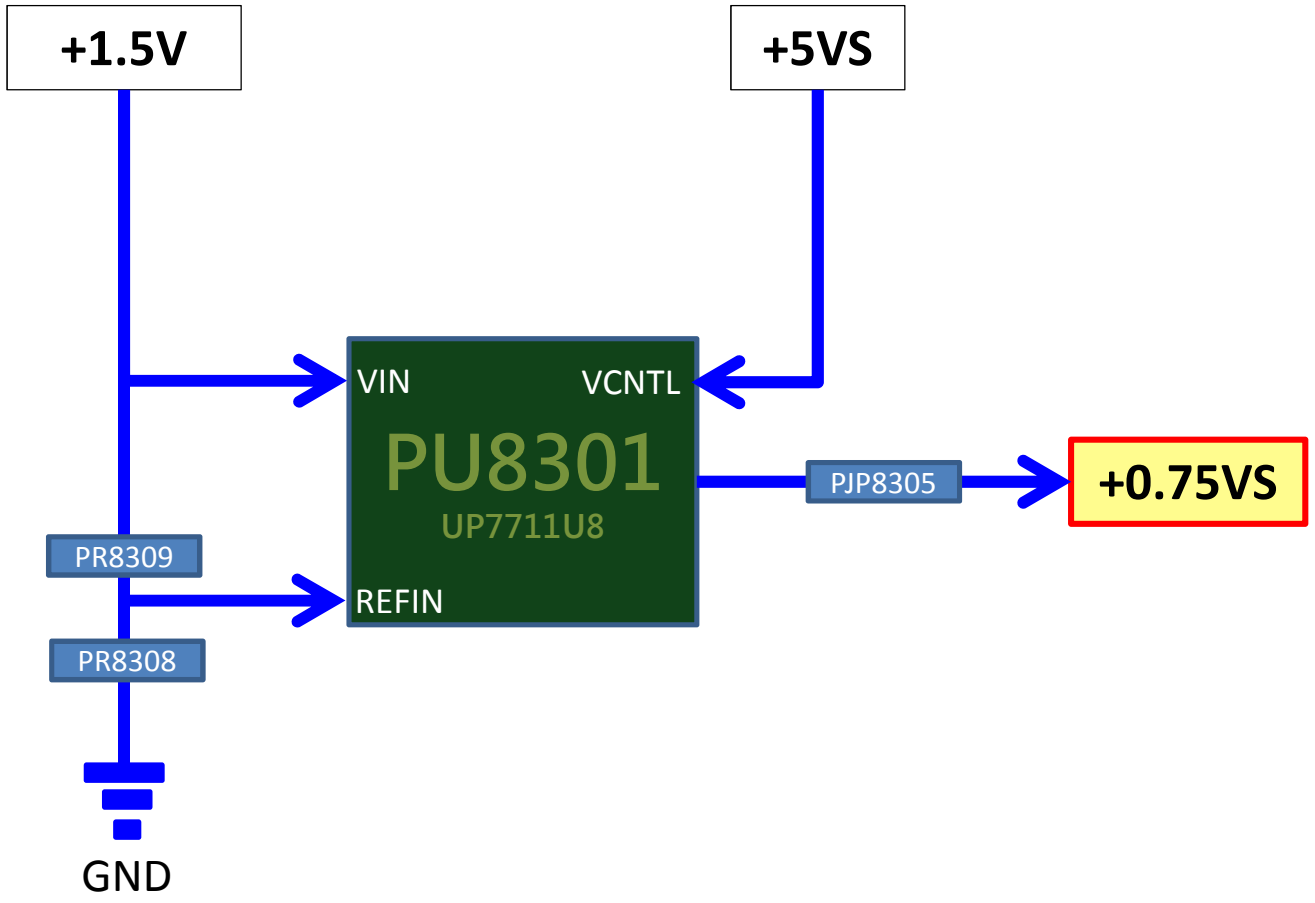
➢ Power on sequence analysis

+0.75VS



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Intel Calpella Platform – K52JT

- Calpella Platform Block Diagram
- Ibex Peak-M Overview
- K52JT Architecture
- [Repair reference] - No power
- **[Repair reference] - No display with power is on**
- [Repair reference] - Vcore Problems
- [Repair reference] - Battery Charging problems
- [Repair reference] - LAN problems
- [Repair reference] - Audio problems
- Q & A

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No display with power is on

- View angle : Architecture
- Connection problems between PCH and EC
- Connection problems between PCH and BIOS
- Connection problems between CPU and PCH
- Connection problems between CPU and RAM(s)
- Connection problems between CPU and GPU chipset
- Connection problems between PCH and Display devices

No display with power is on

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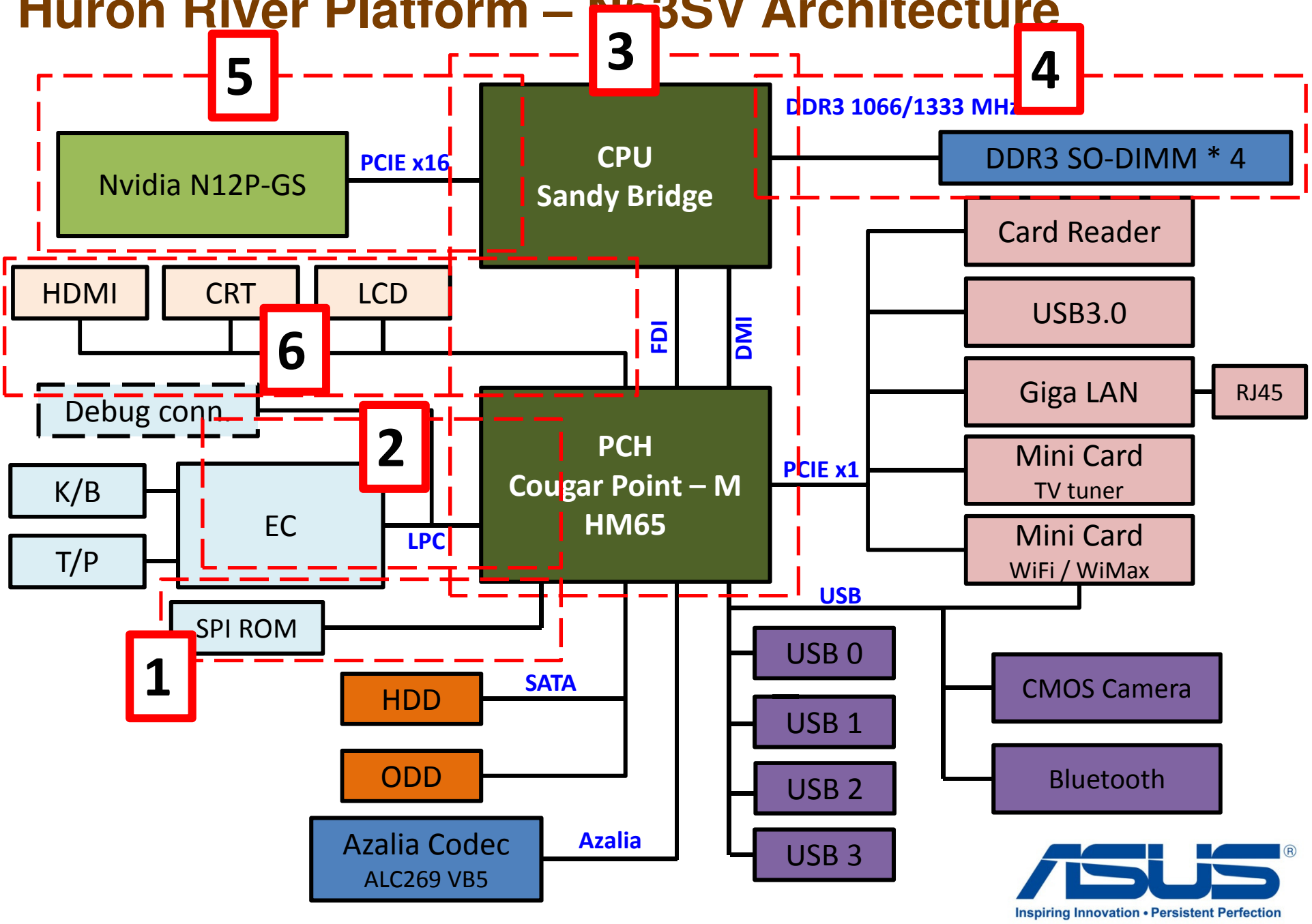
Huron River Platform – N53SV Architecture



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No display with power is on

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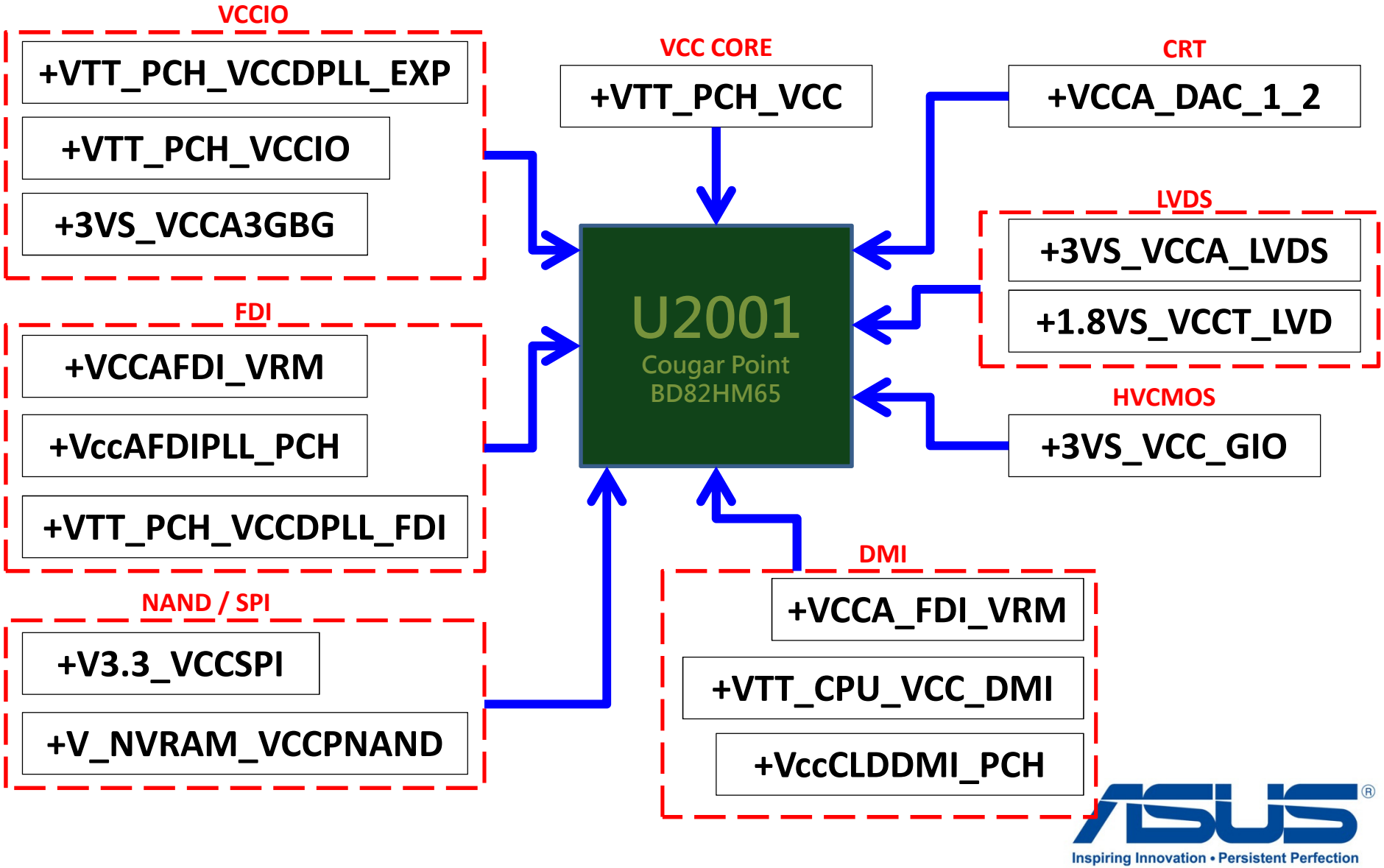
➢ Connection problems between PCH and BIOS

Critical Power sources to PCH (1)



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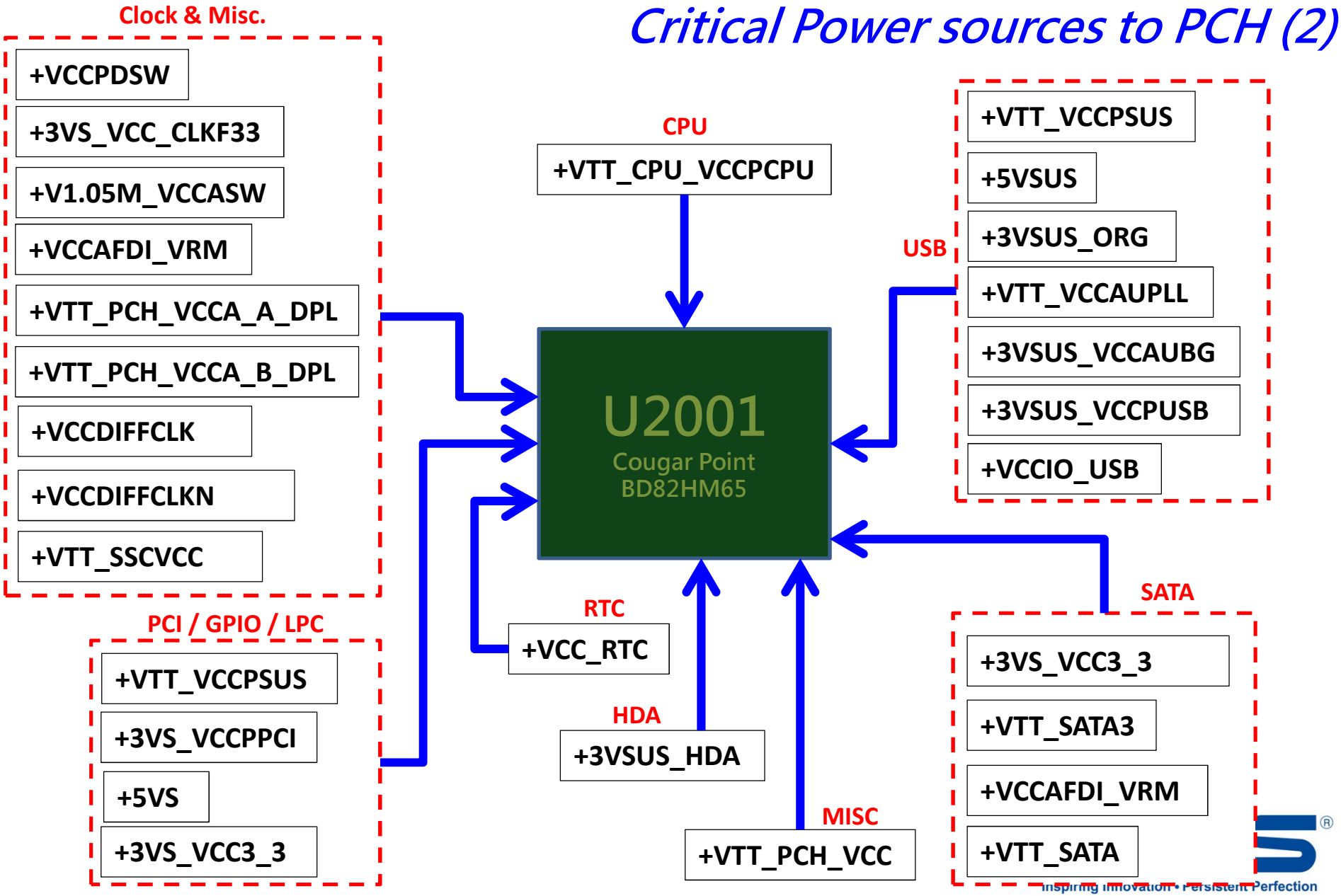
➢ Connection problems between PCH and BIOS

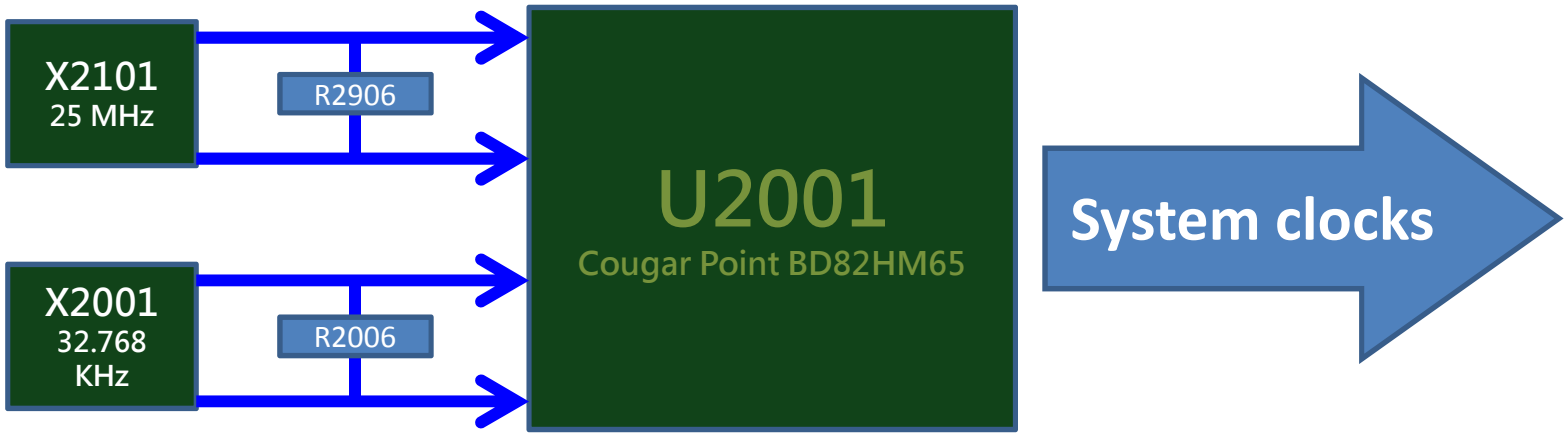
Critical Power sources to PCH (2)



➢ Connection problems between PCH and BIOS

Critical Clocks to PCH

Cougar Point Integrated the clock generator. Most of clock signals on N53SV MB are generated from Cougar Point.
In N53SV, all system clock signals are provided by PCH except GPU and LAN.



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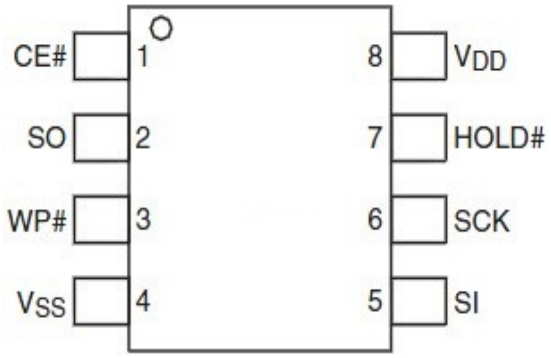
➢ Connection problems between PCH and BIOS

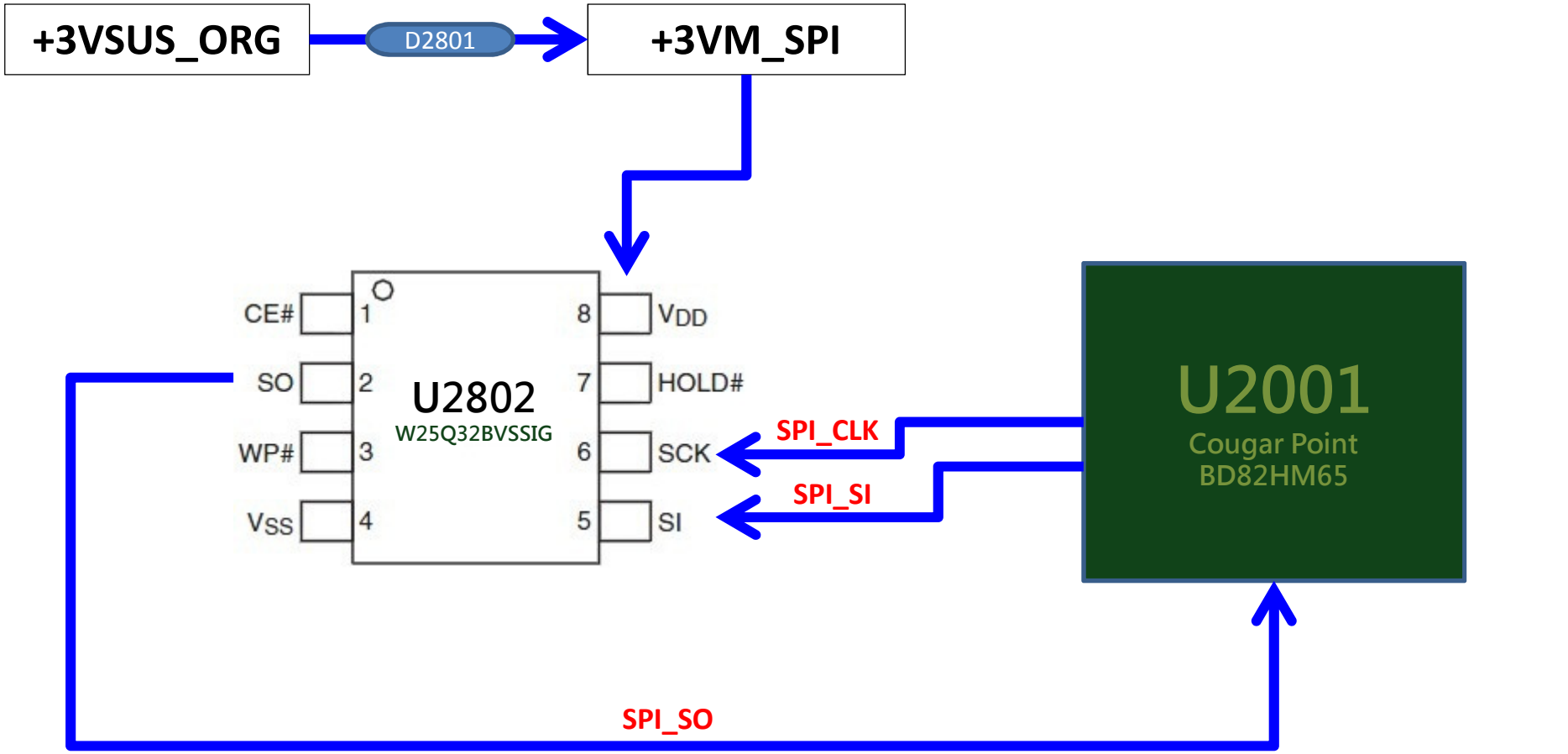
Winbond W25Q32BVSSIG Pin Descriptions



Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable/disable BPL bit in the status register.
HOLD#	Hold	To temporarily stop serial communication with SPI flash memory without resetting the device.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V
V_{SS}	Ground	

➢ Connection problems between PCH and BIOS

How BIOS works in N53SV



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No display with power is on

- View angle : Architecture
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- Connection problems between CPU and GPU chipset
- Connection problems between PCH and Display devices

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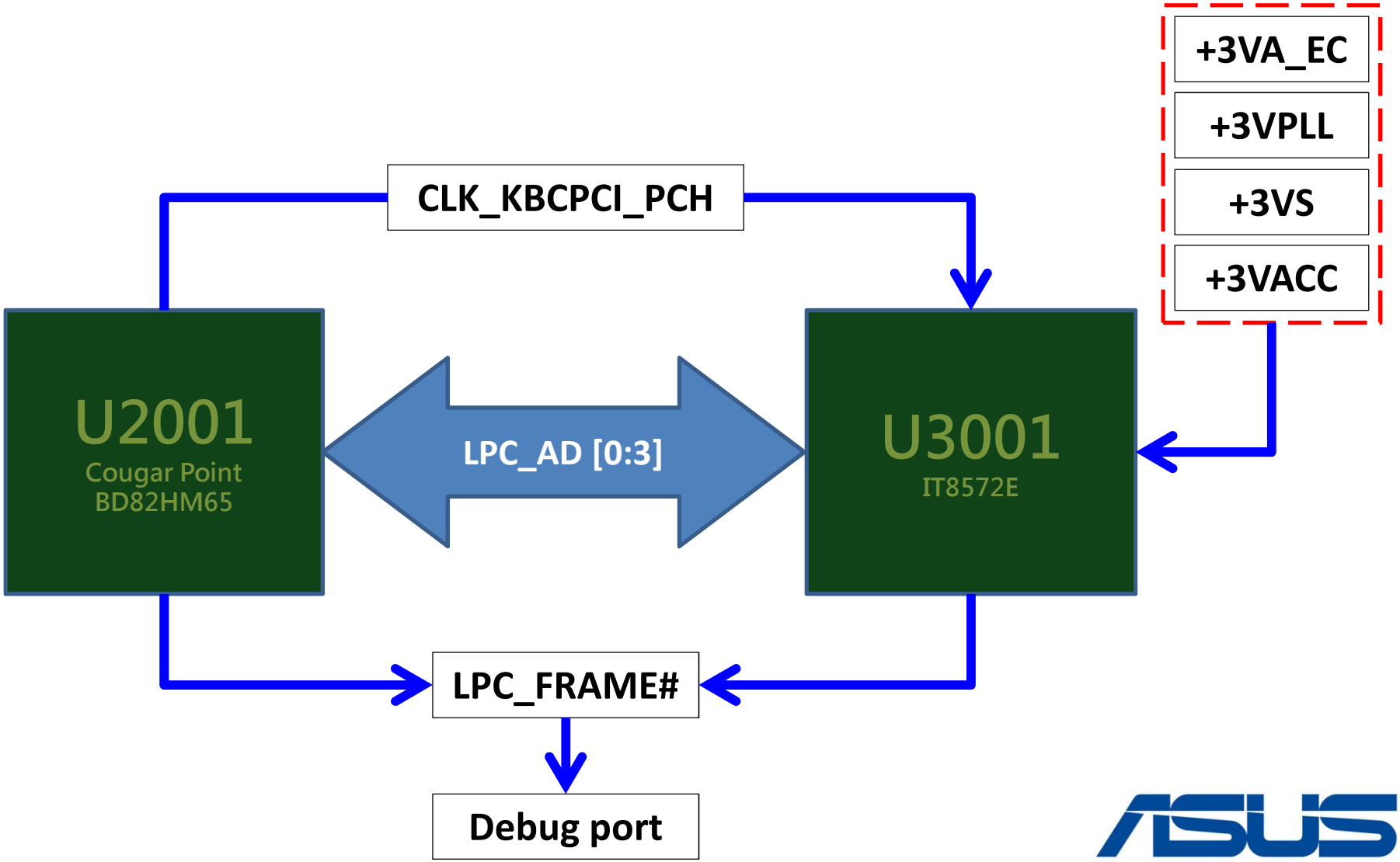
- Connection problems between PCH and EC

Critical communication pins between PCH to EC



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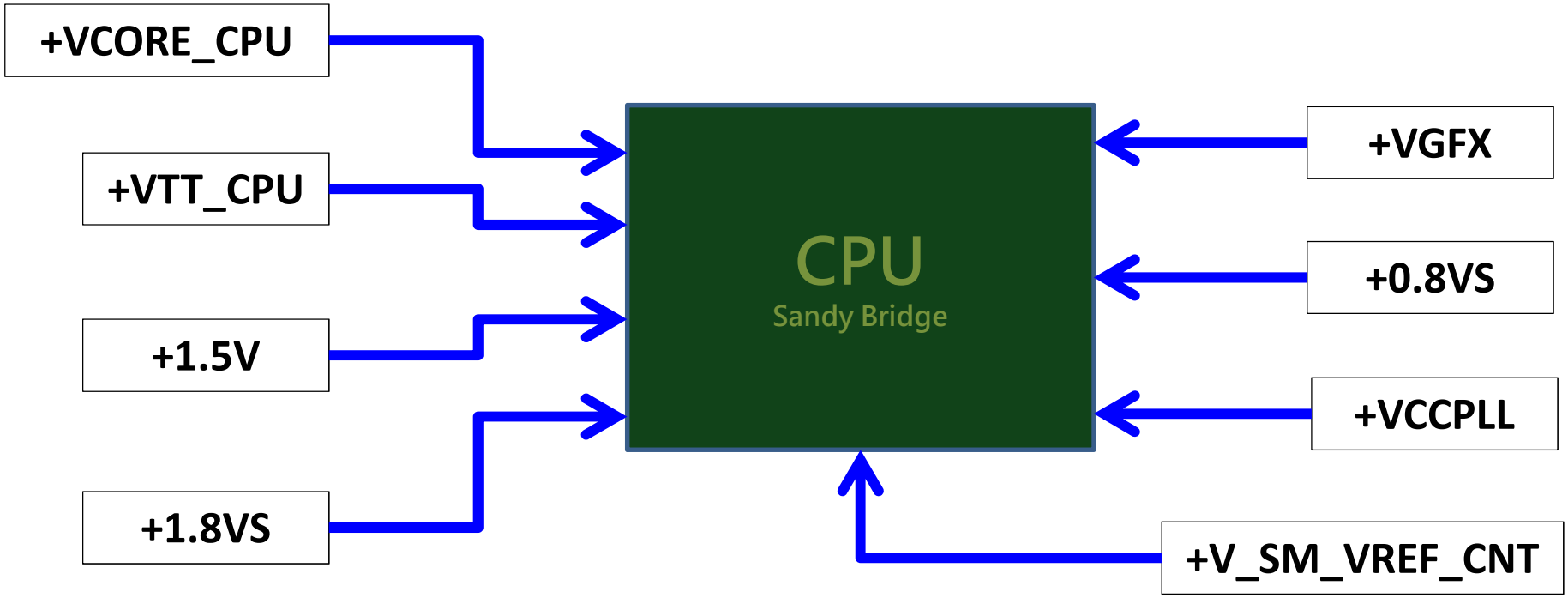
➢ Connection problems between CPU and PCH

Critical Power sources to CPU



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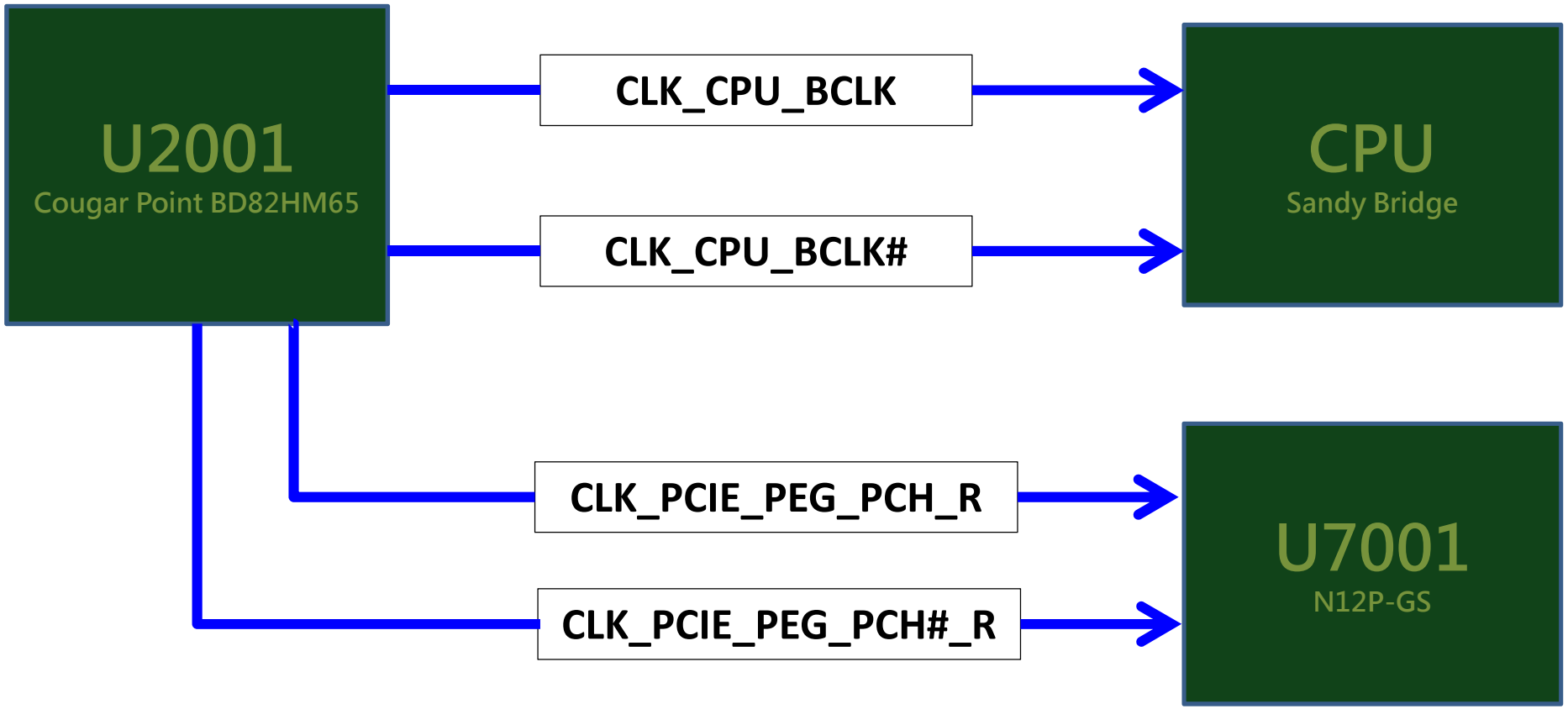
➢ Connection problems between CPU and PCH

Critical Clocks from PCH to CPU and GPU



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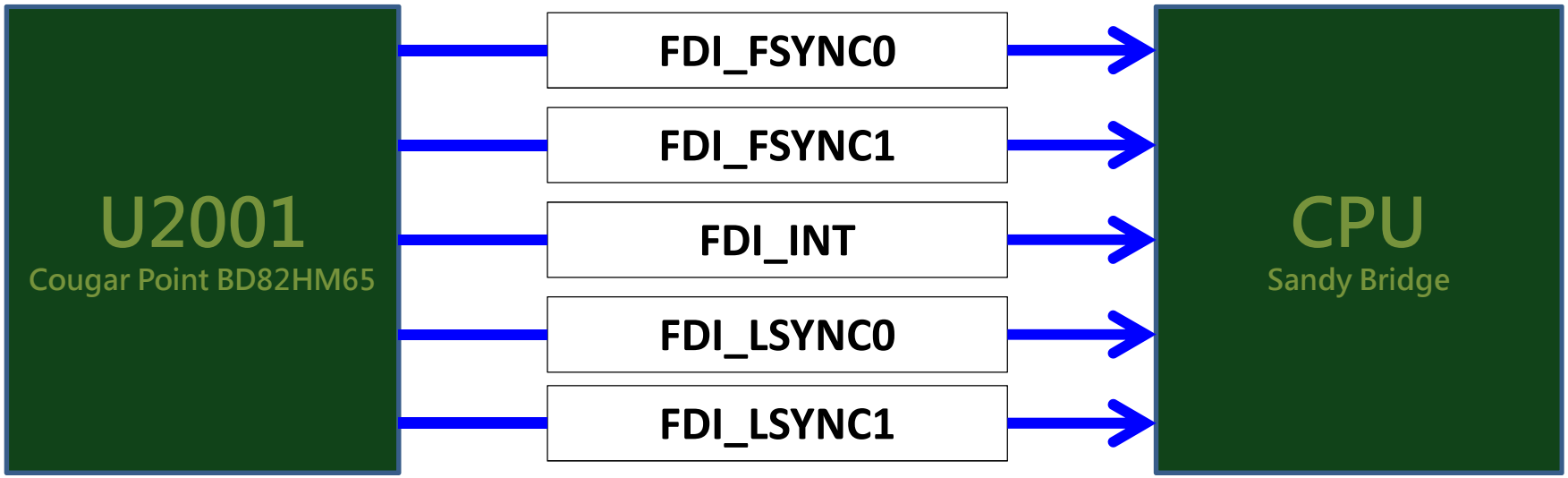
➢ Connection problems between CPU and PCH

FDI control signal between PCH & CPU



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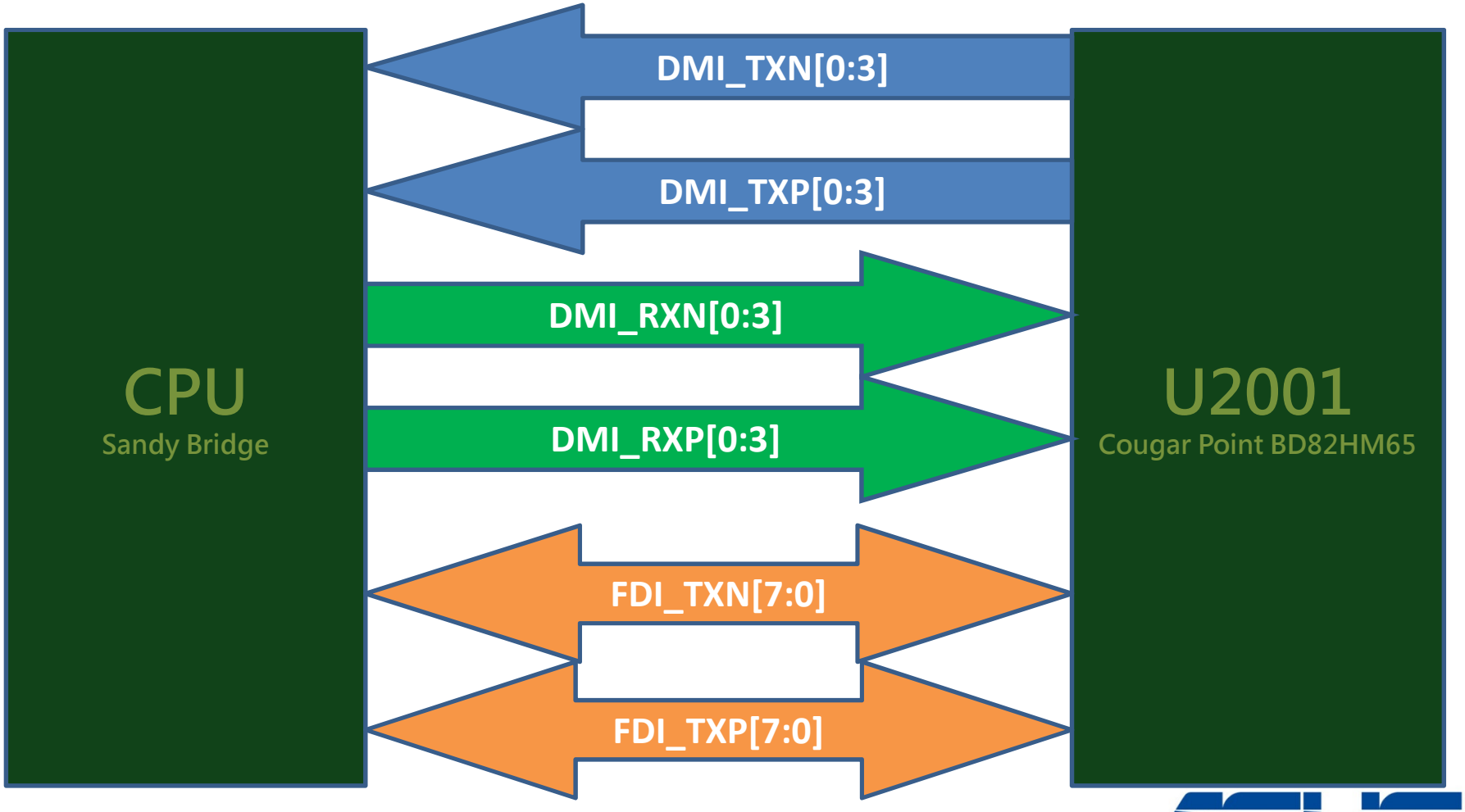
➢ Connection problems between CPU and PCH

Data Transmission pins between PCH & CPU



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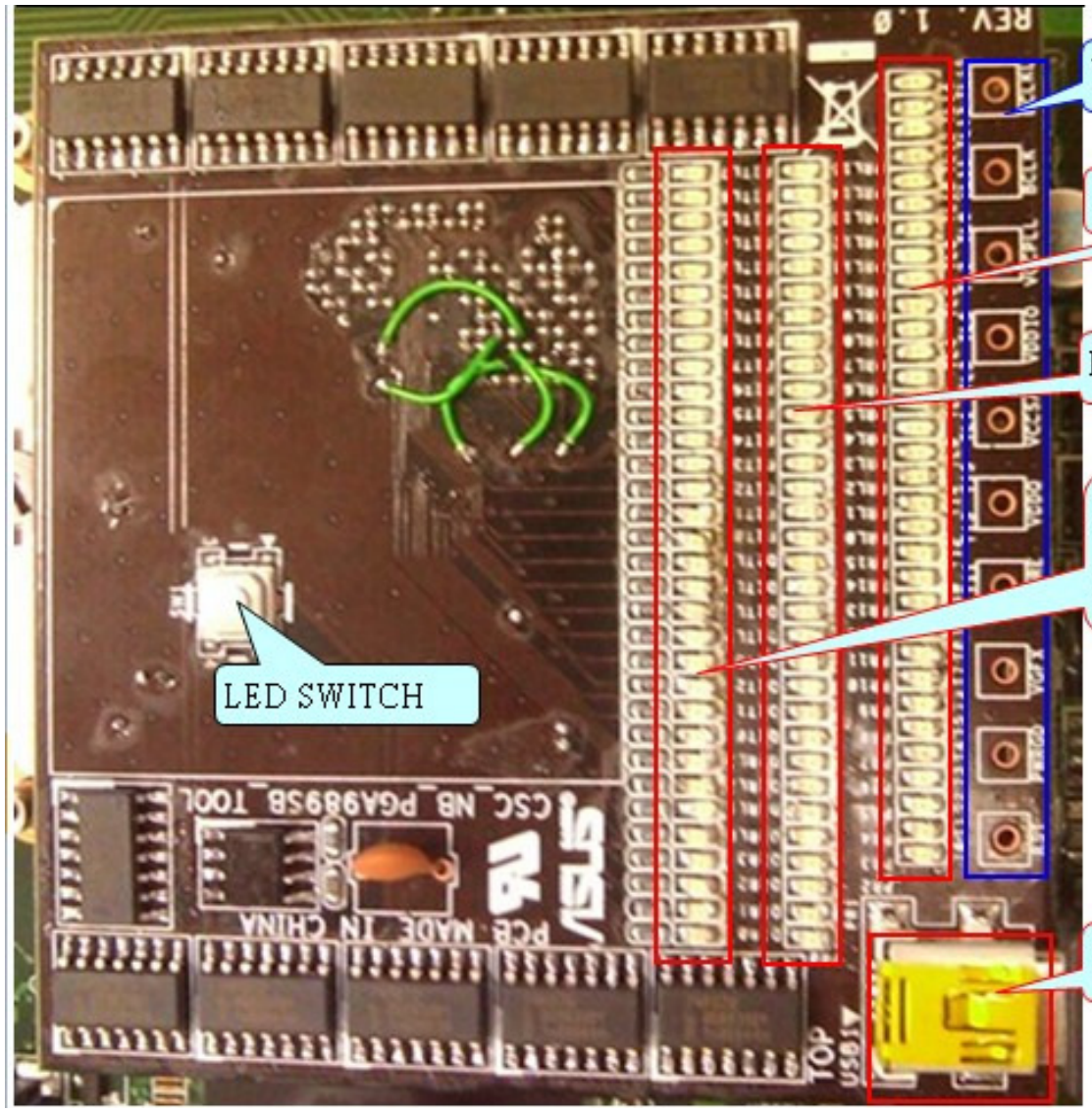
➢ Connection problems between CPU, PCH, RAM and GPU

Sandy Bridge CPU inspection Tool



No display with power is on

- View angle : Architecture
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- Connection problems between PCH and Display devices

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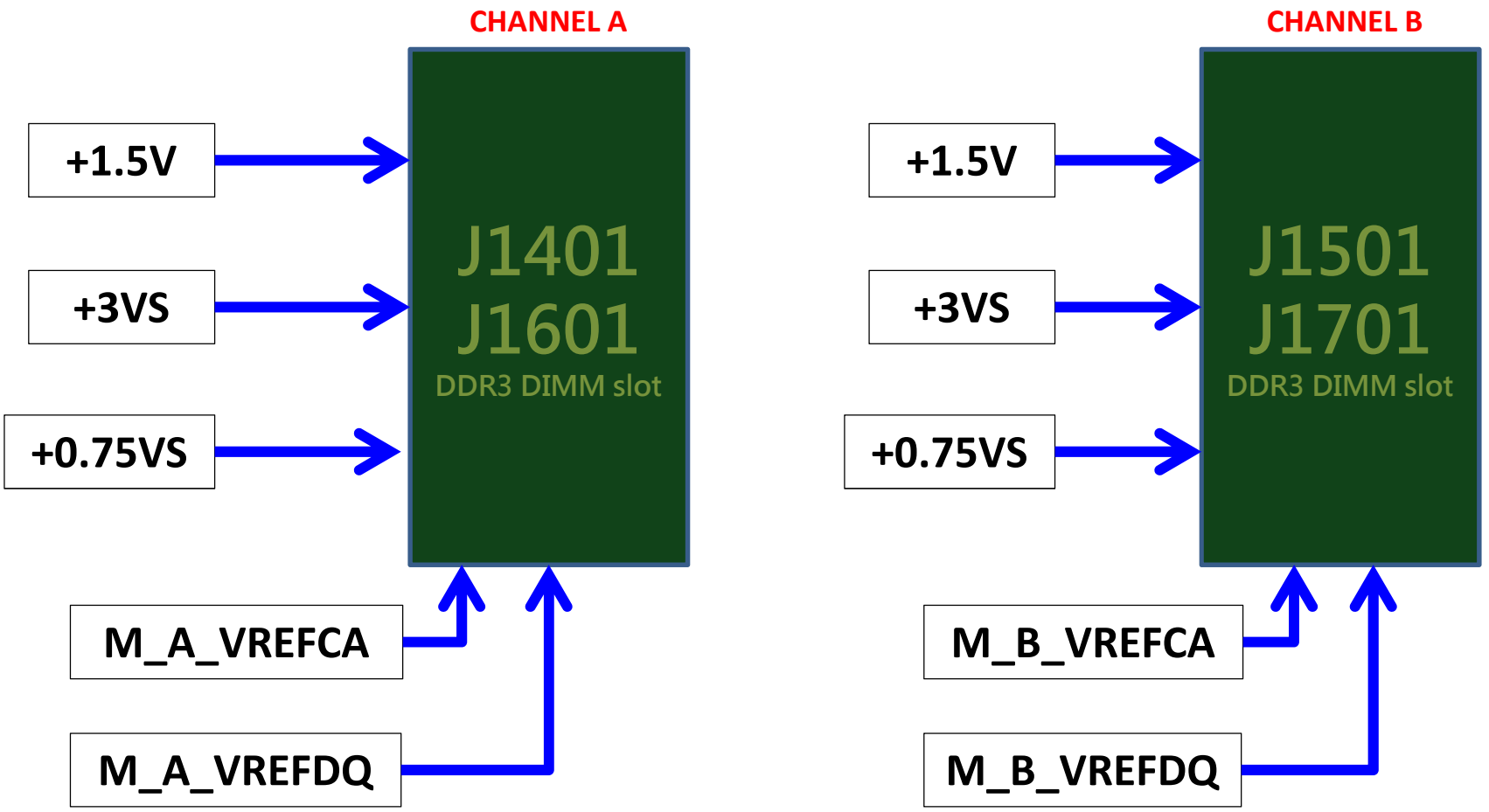
➢ Connection problems between CPU and RAM(s)

Critical Power sources to DDR3



The function 2-DIMM per channel is only available with Core i7.

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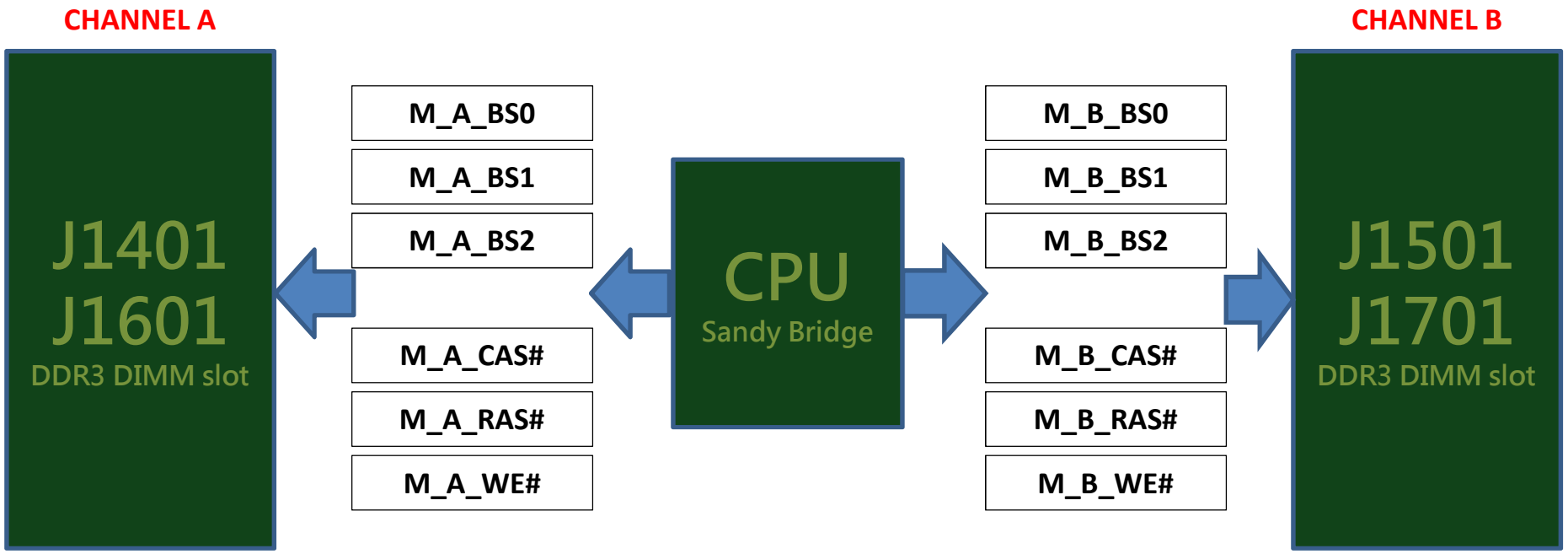
➢ Connection problems between CPU and RAM(s)

Critical Clocks and Control signals to DDR3 (1)



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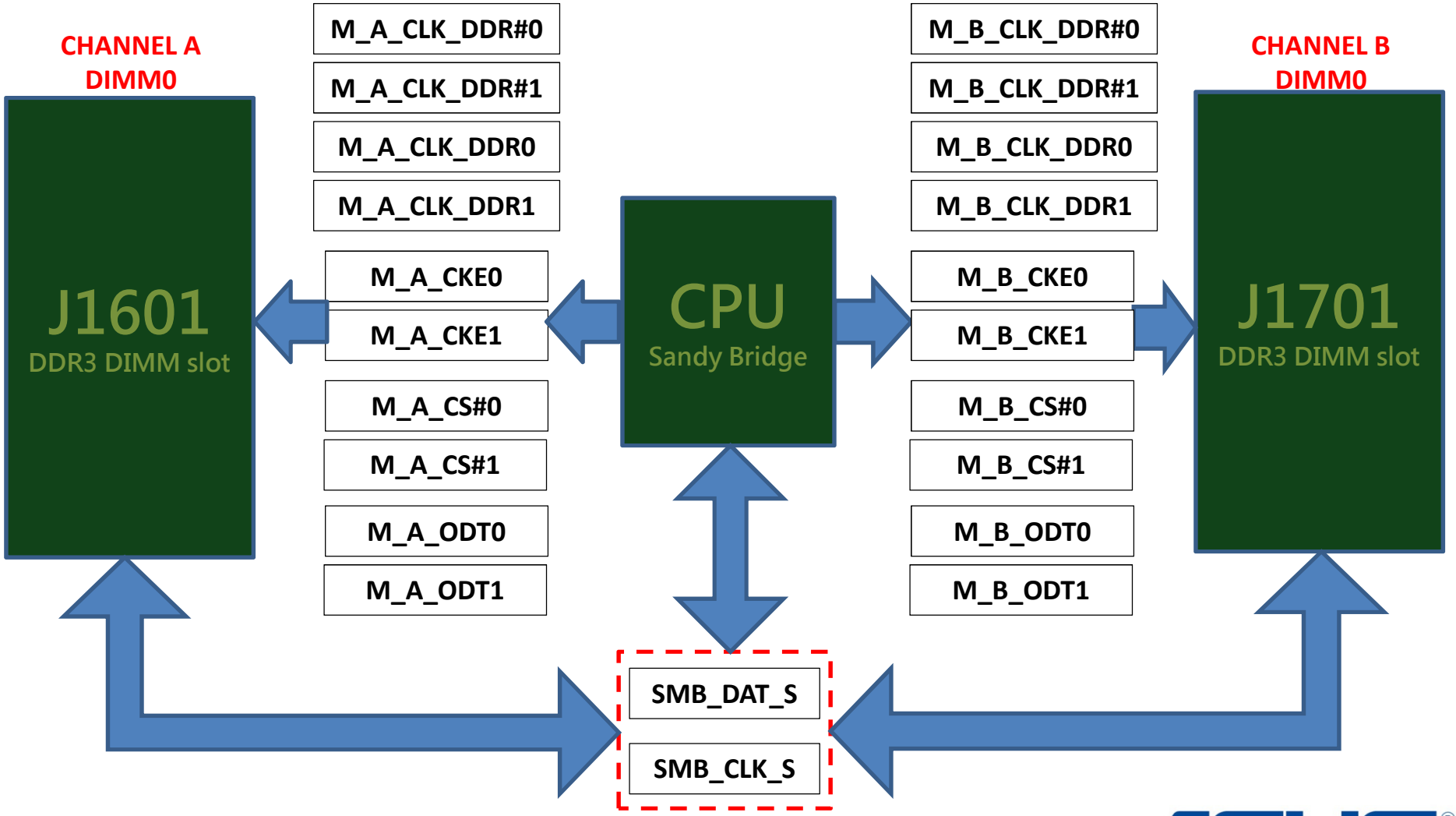
➢ Connection problems between CPU and RAM(s)

Critical Clocks and Control signals to DDR3 (2)



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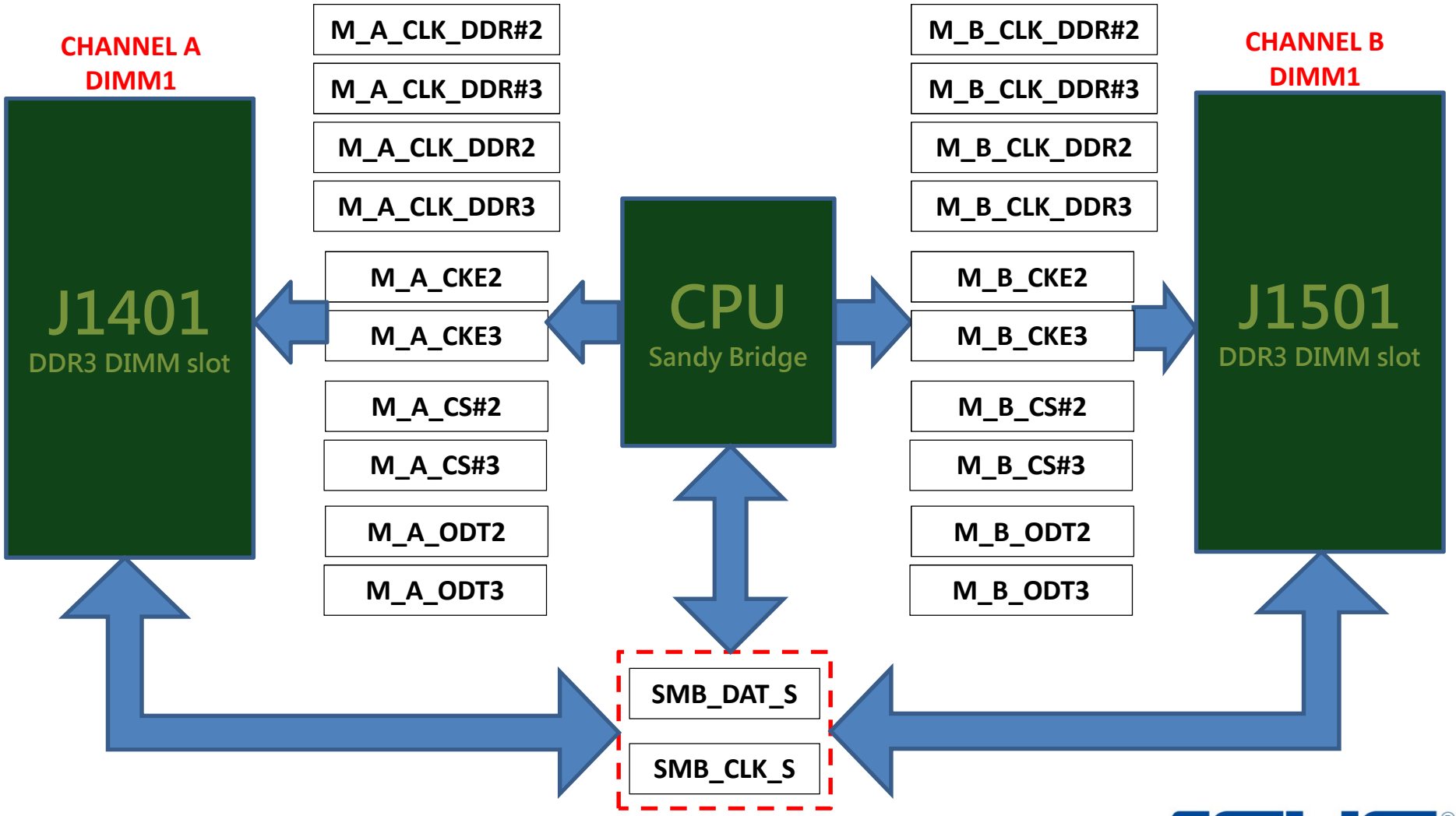
➢ Connection problems between CPU and RAM(s)

Critical Clocks and Control signals to DDR3 (3)



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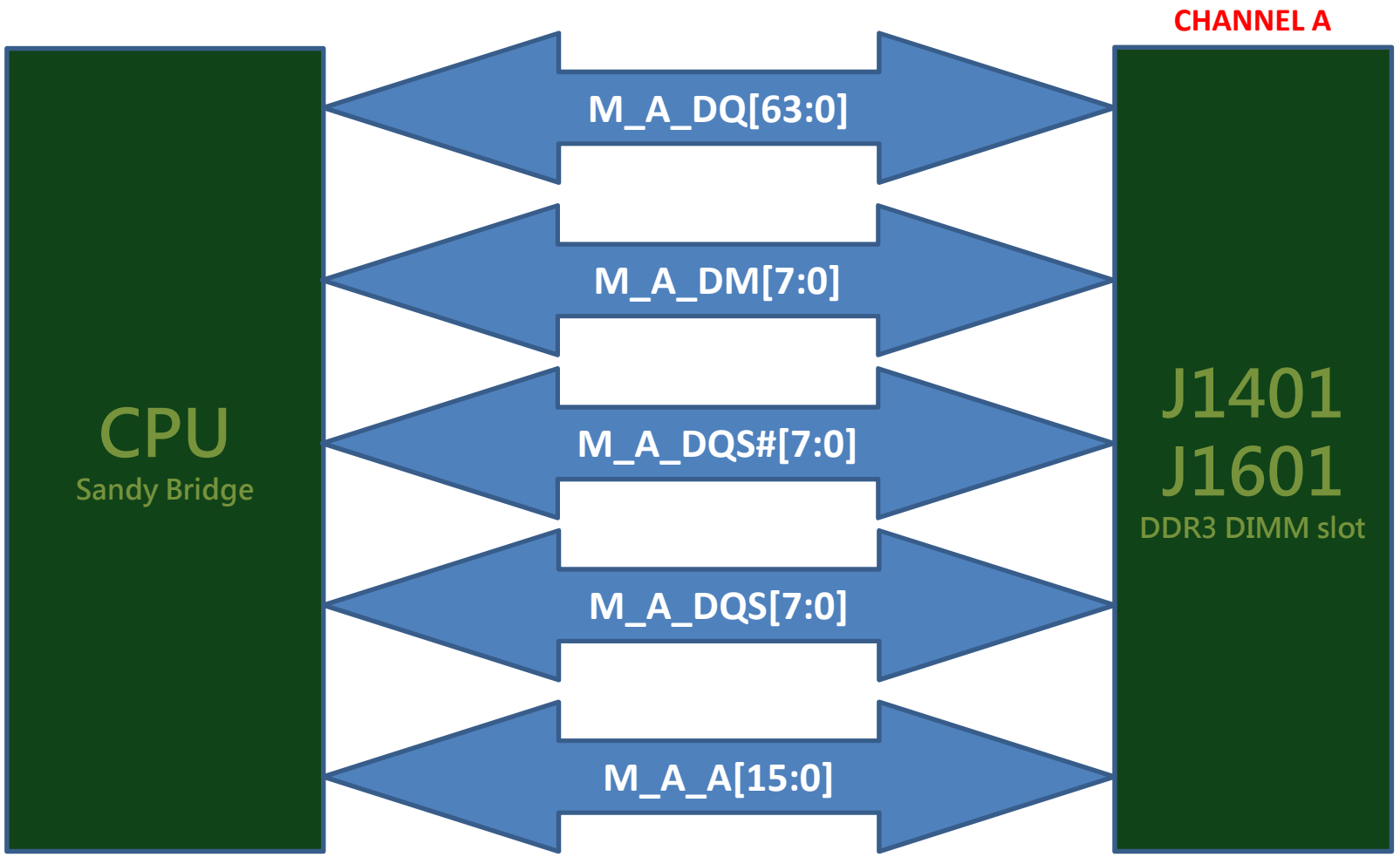
➢ Connection problems between CPU and RAM(s)

Data Transmission pins between CPU and DIMM0



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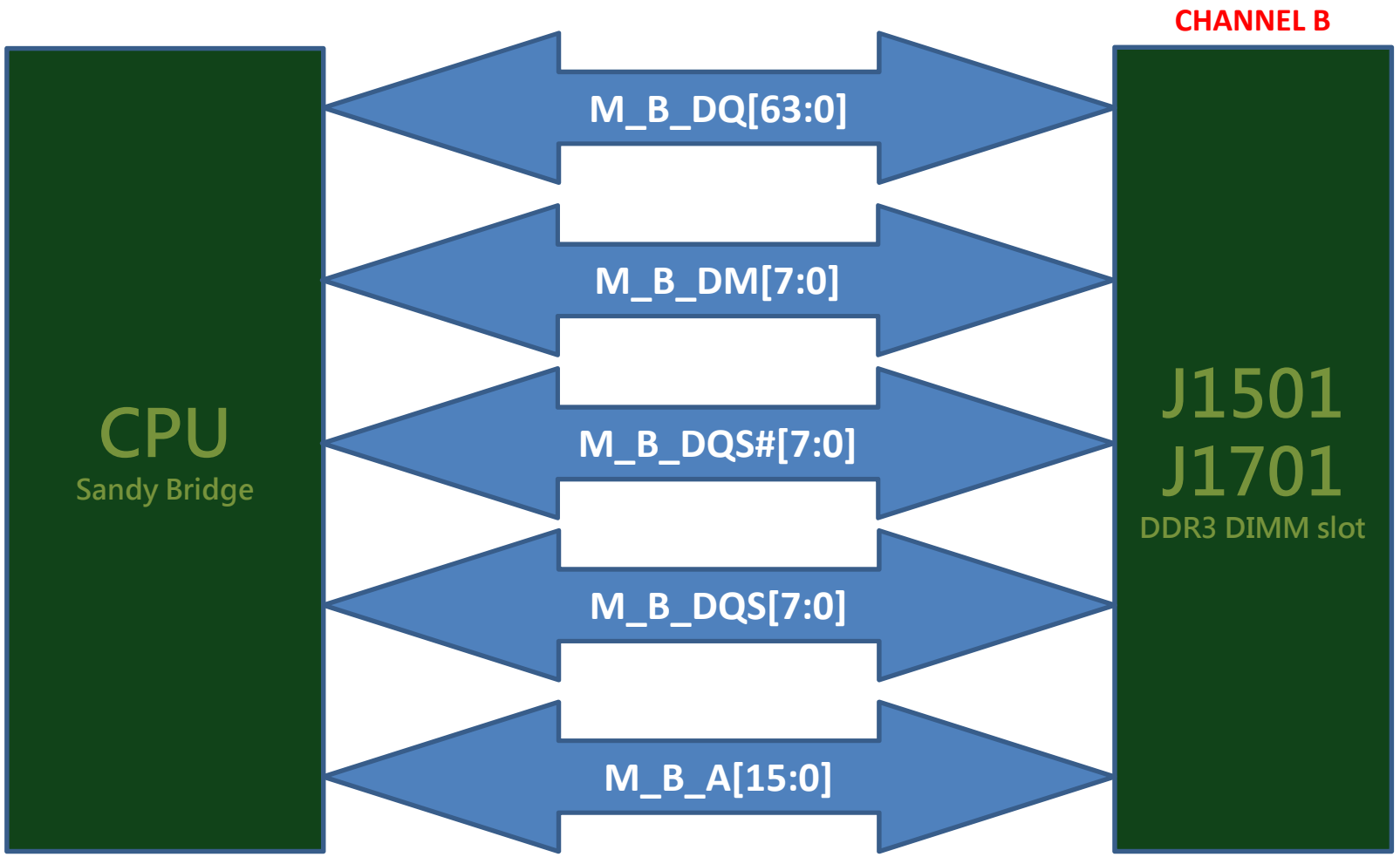
➢ Connection problems between CPU and RAM(s)

Data Transmission pins between CPU and DIMM1



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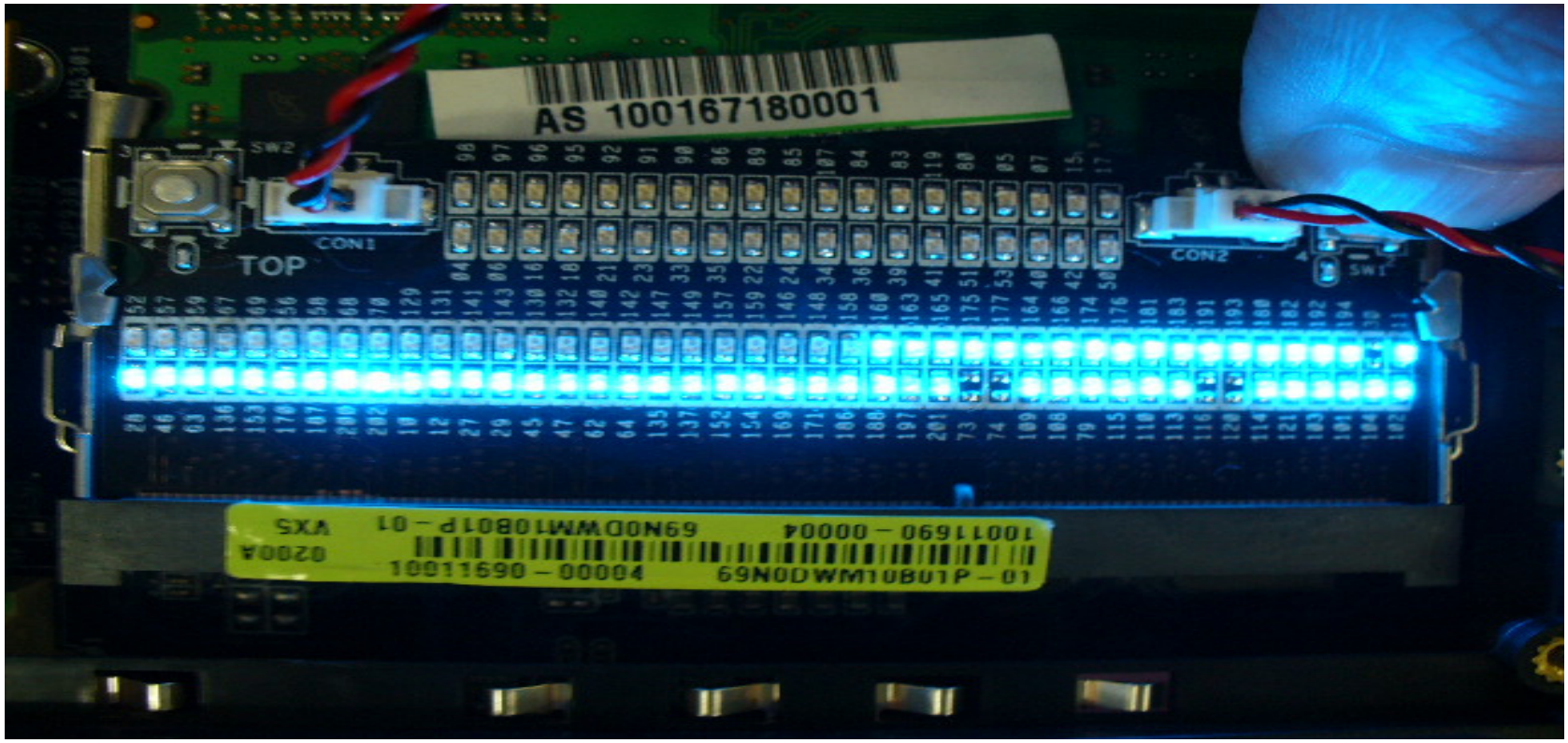
- Connection problems between CPU and RAM(s)

DDR3 inspection Tool



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No display with power is on

- View angle : Architecture
- Connection problems between PCH and BIOS
- Connection problems between PCH and EC
- Connection problems between CPU and PCH
- Connection problems between CPU and RAM(s)
- **Connection problems between CPU and GPU chipset**
- Connection problems between PCH and Display devices

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➢ Connection problems between GPU and display devices

Critical Power sources to Nvidia N12P-GT(1)

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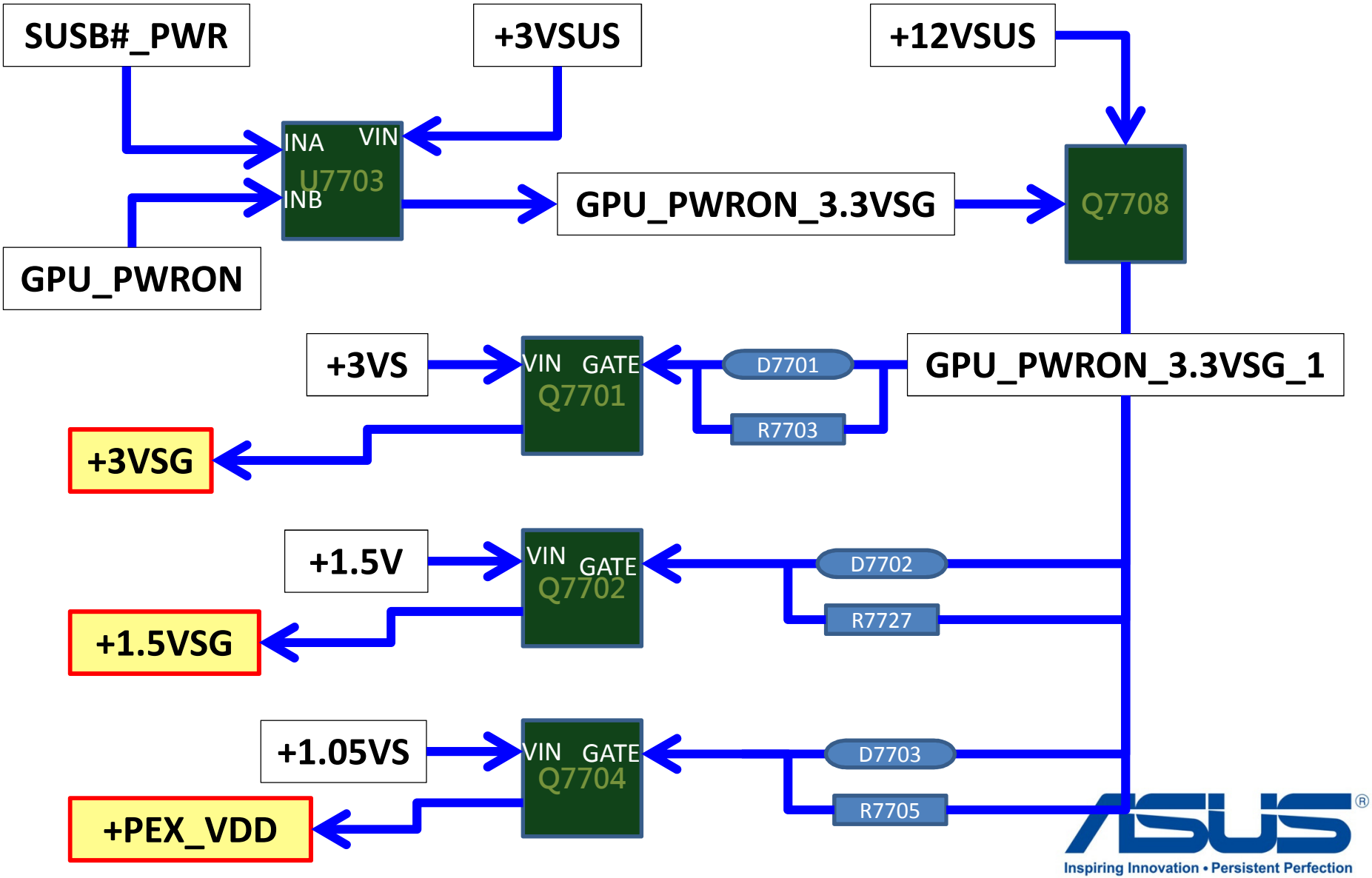
➢ Connection problems between GPU and display devices

Critical Power sources to Nvidia N12P-GT(2)



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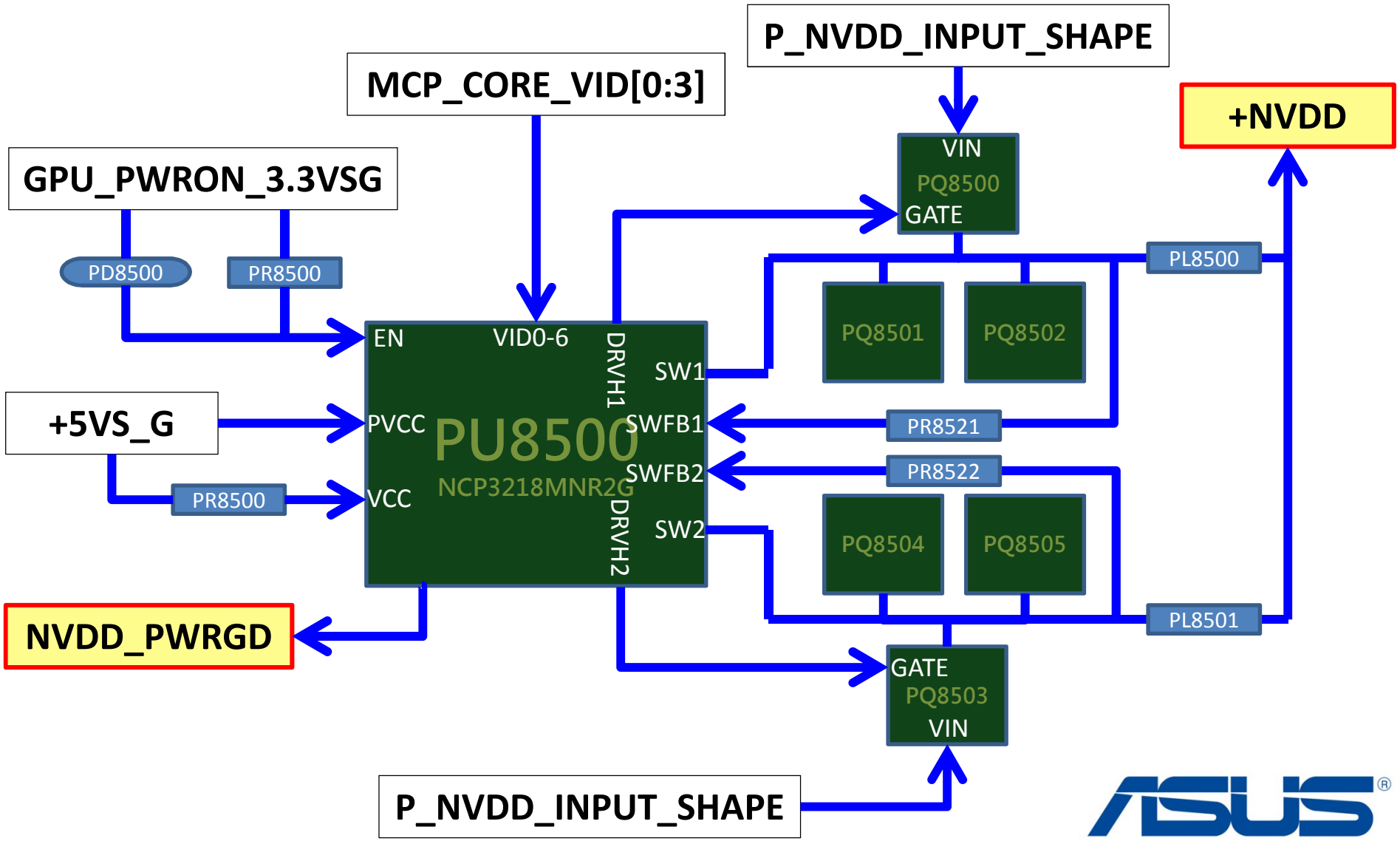
➢ Connection problems between GPU and display devices

Critical Power sources to Nvidia N12P-GT(3)



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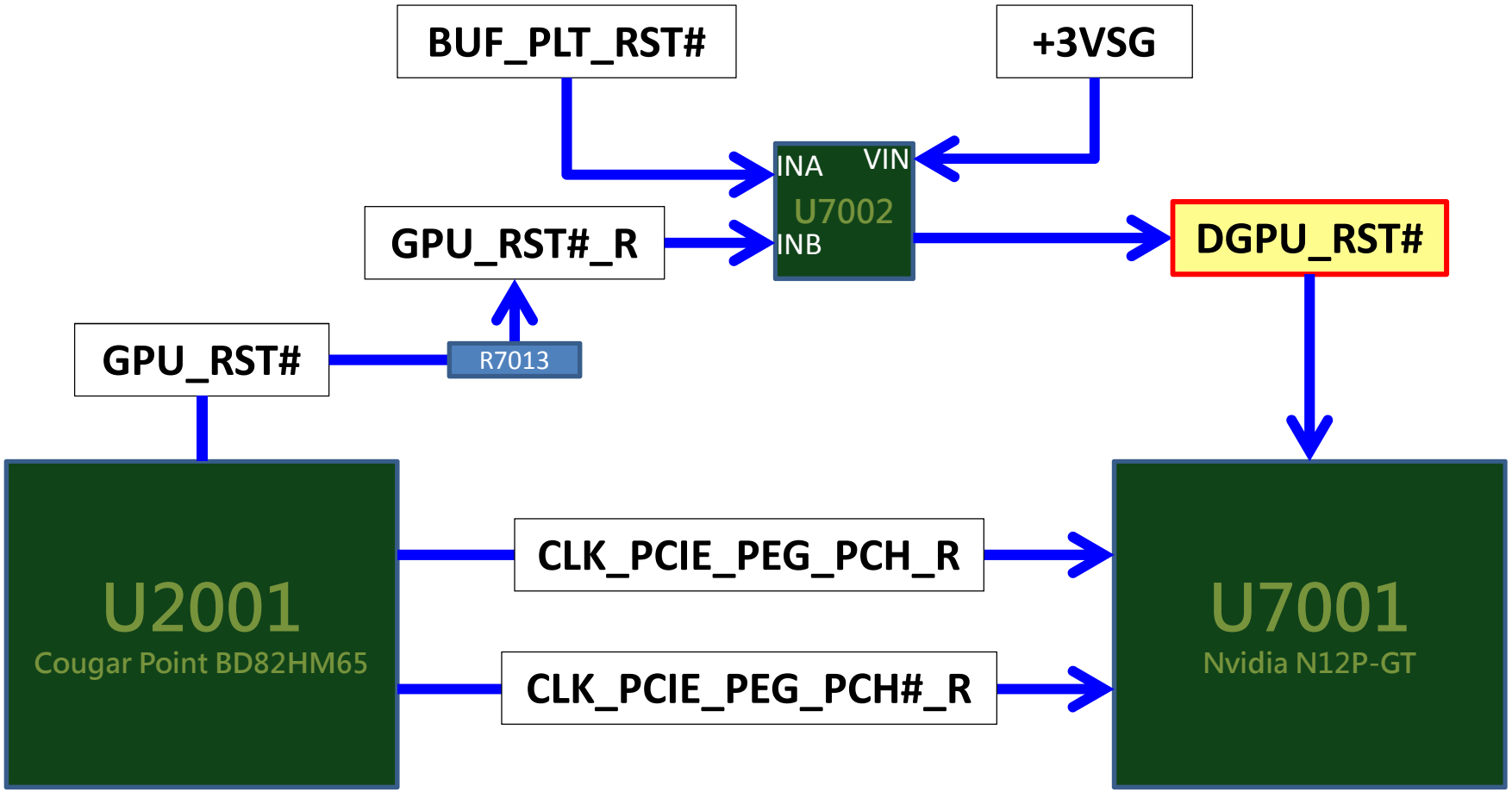
➢ Connection problems between GPU and display devices

Critical Clocks to Nvidia N12P-GT GPU chipset



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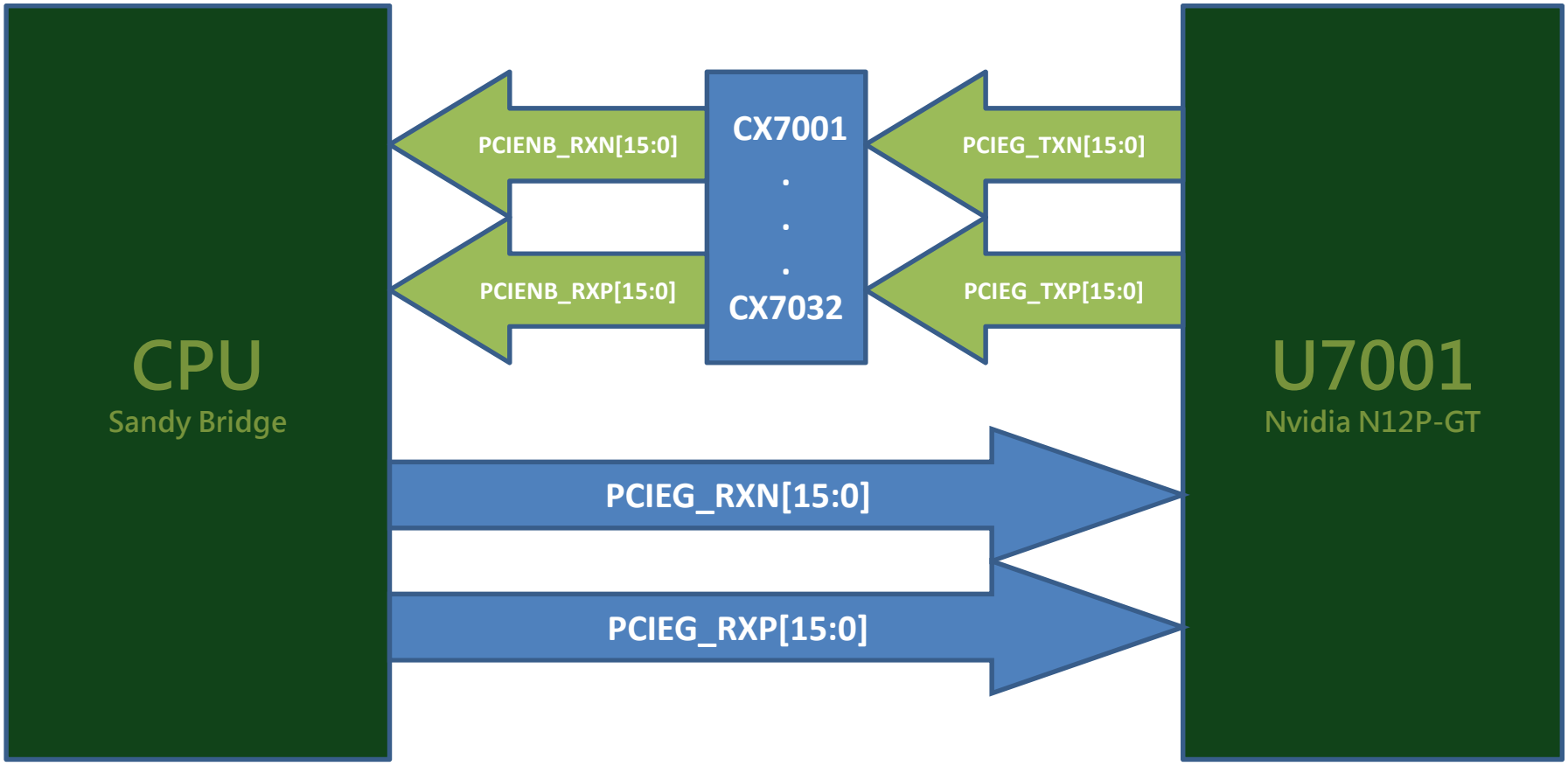
➢ Connection problems between CPU and GPU

Data Transmission pins between CPU & GPU



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No display with power is on

- View angle : Architecture
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- Connection problems between CPU and RAM(s)
- Connection problems between CPU and GPU chipset
- **Connection problems between PCH and Display devices**

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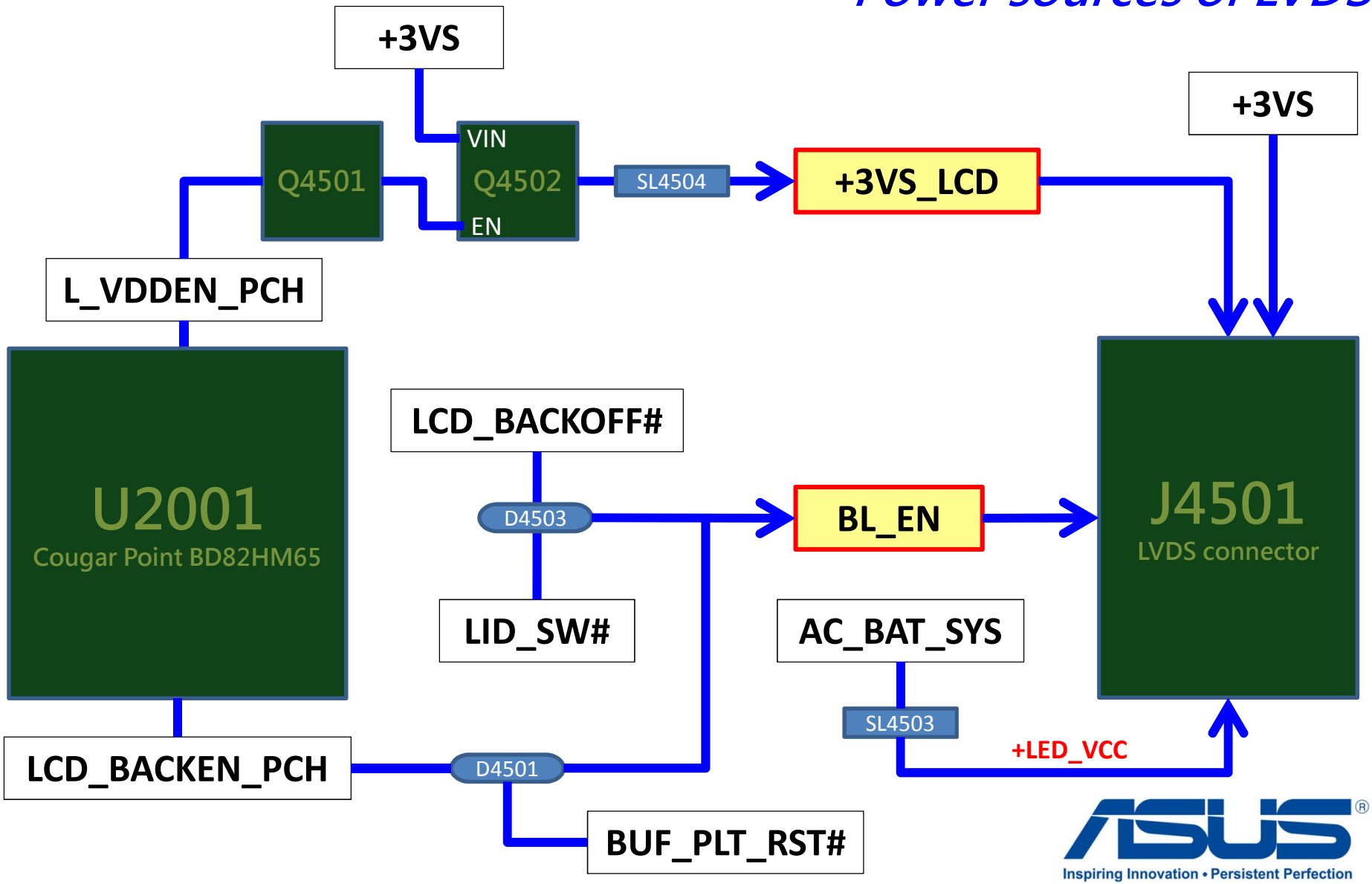
➢ Connection problems between PCH and display devices

Power sources of LVDS



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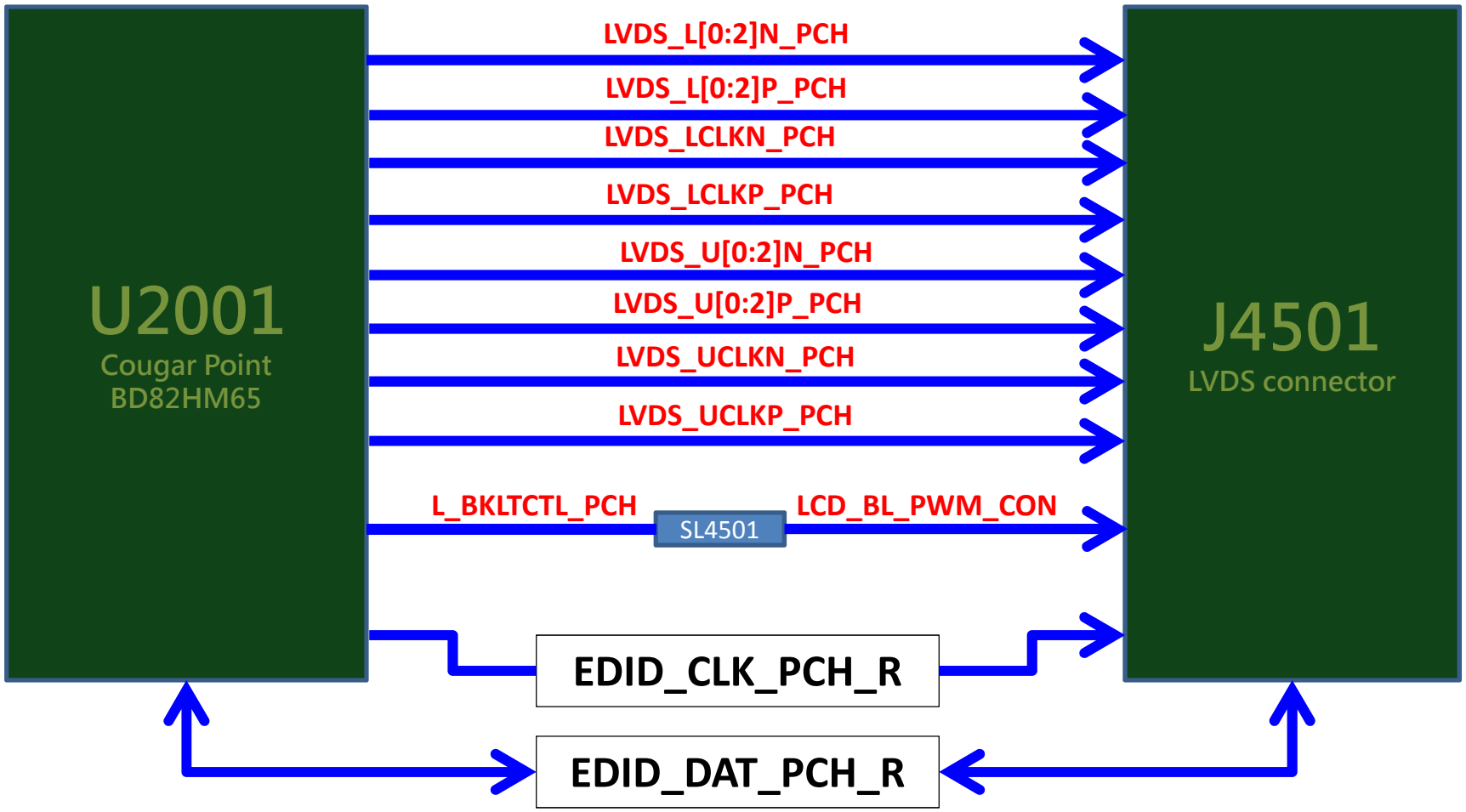
➢ Connection problems between PCH and display devices

Signals from PCH to LVDS



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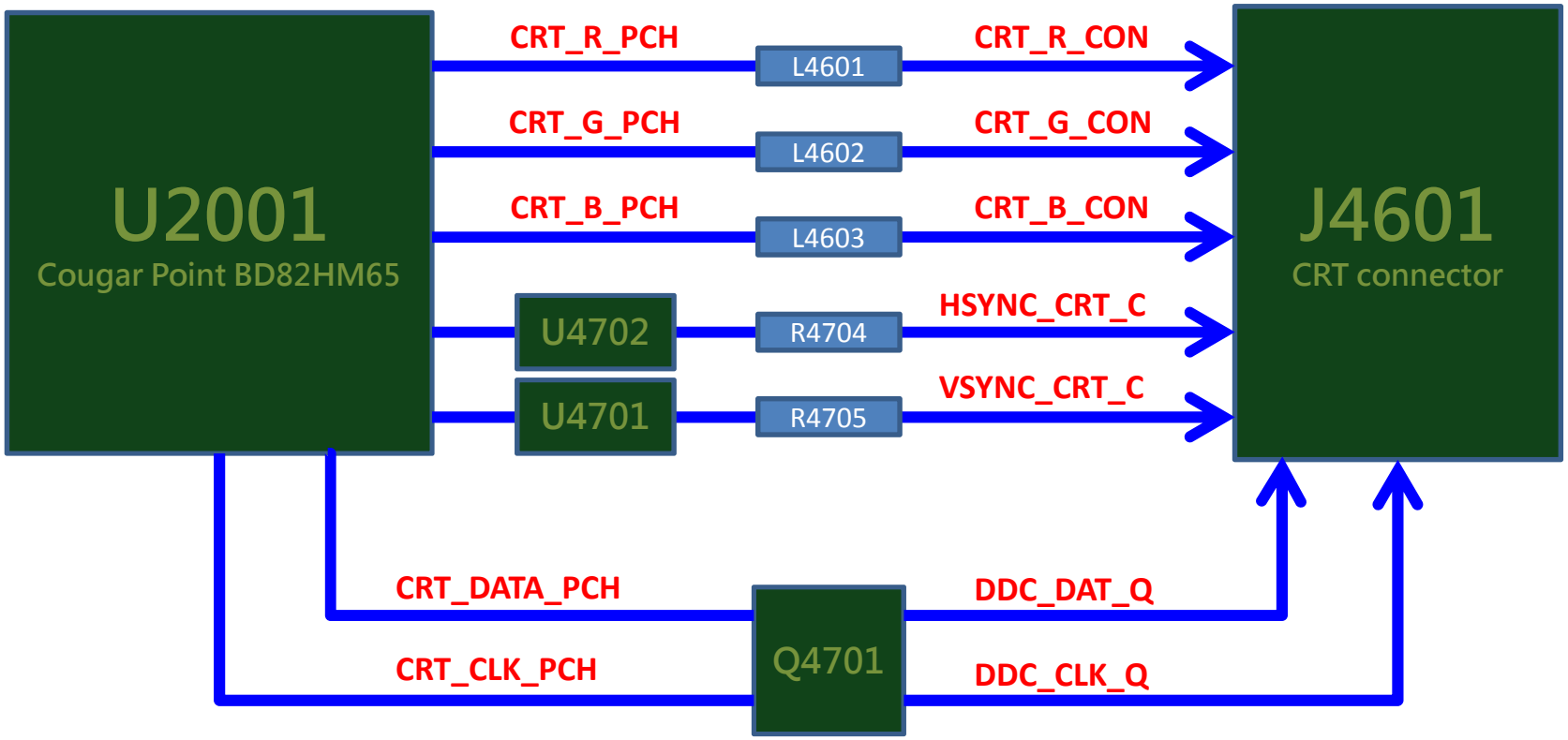
➢ Connection problems between PCH and display devices

Signals from PCH to CRT out



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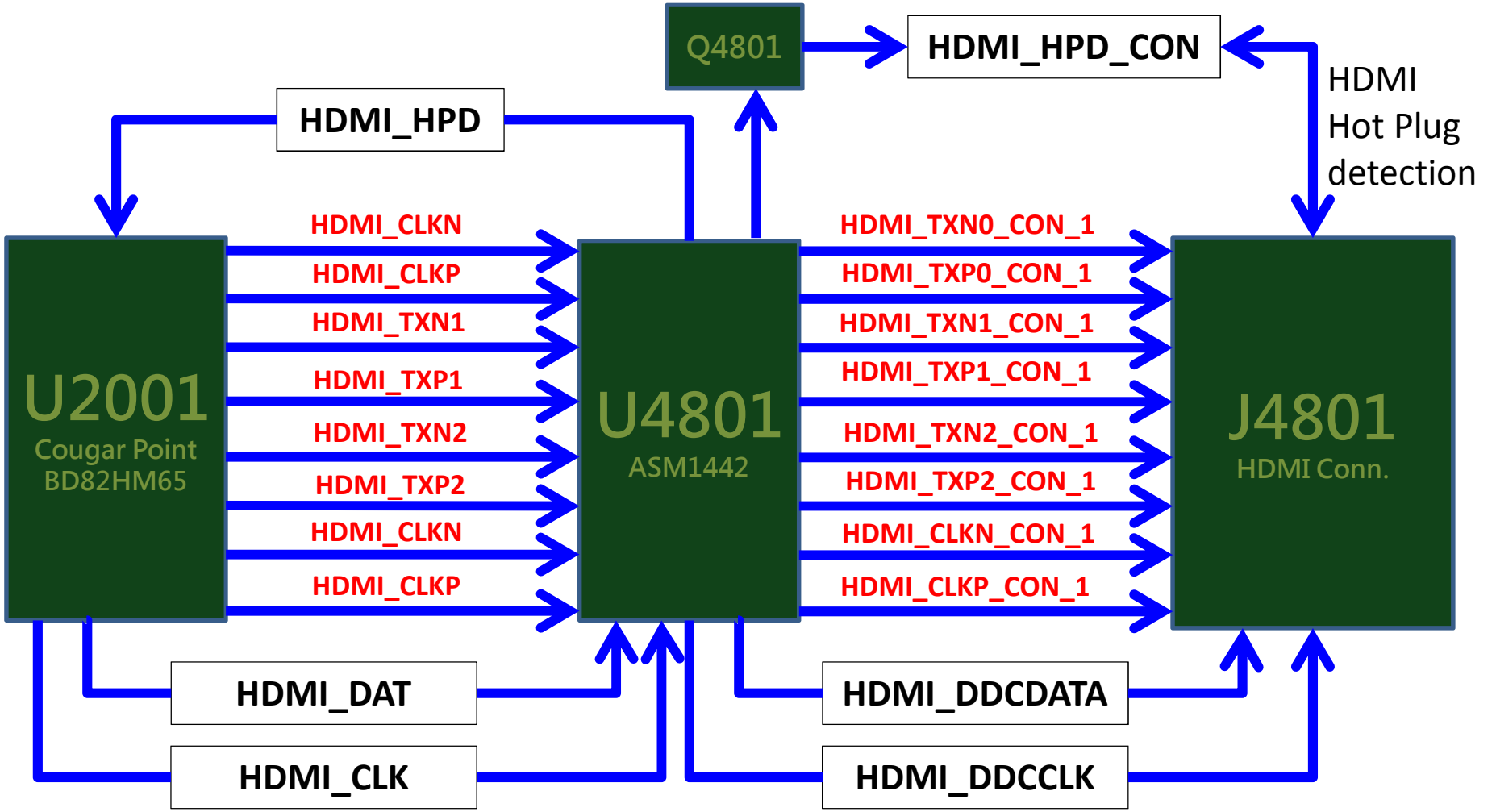
➢ Connection problems between PCH and display devices

Signals from PCH to HDMI out



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Intel Huron River Platform – N53SV

- Huron River Platform Block Diagram
- Cougar Point Overview
- N53SV Architecture
- [Repair reference] - No power
- [Repair reference] - No display with power is on
- **[Repair reference] - Vcore Problems**
- [Repair reference] - Battery Charging problems
- [Repair reference] - LAN problems
- [Repair reference] - Audio problems
- Q & A

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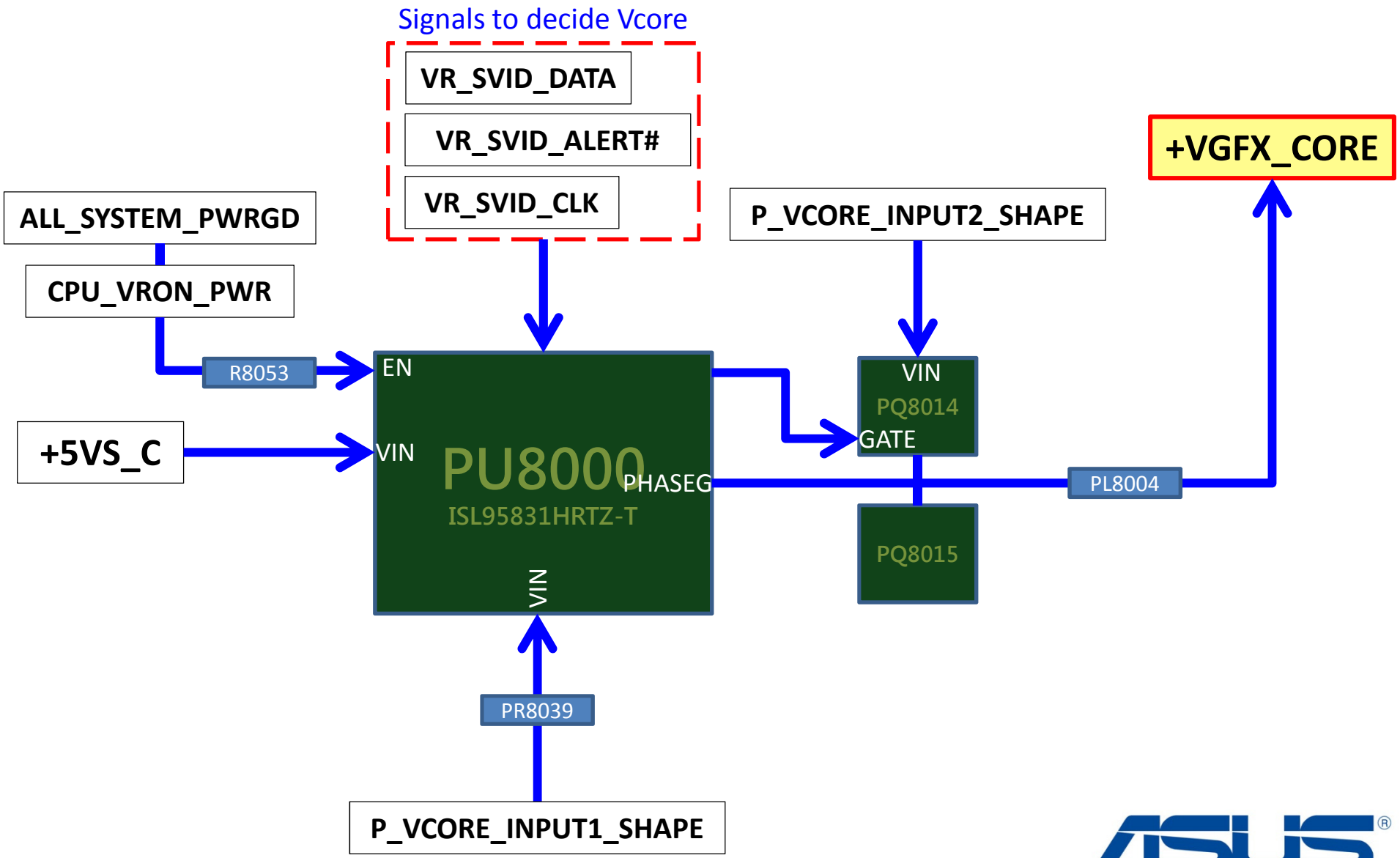
➢ VCORE Problems

+VGFX_CORE



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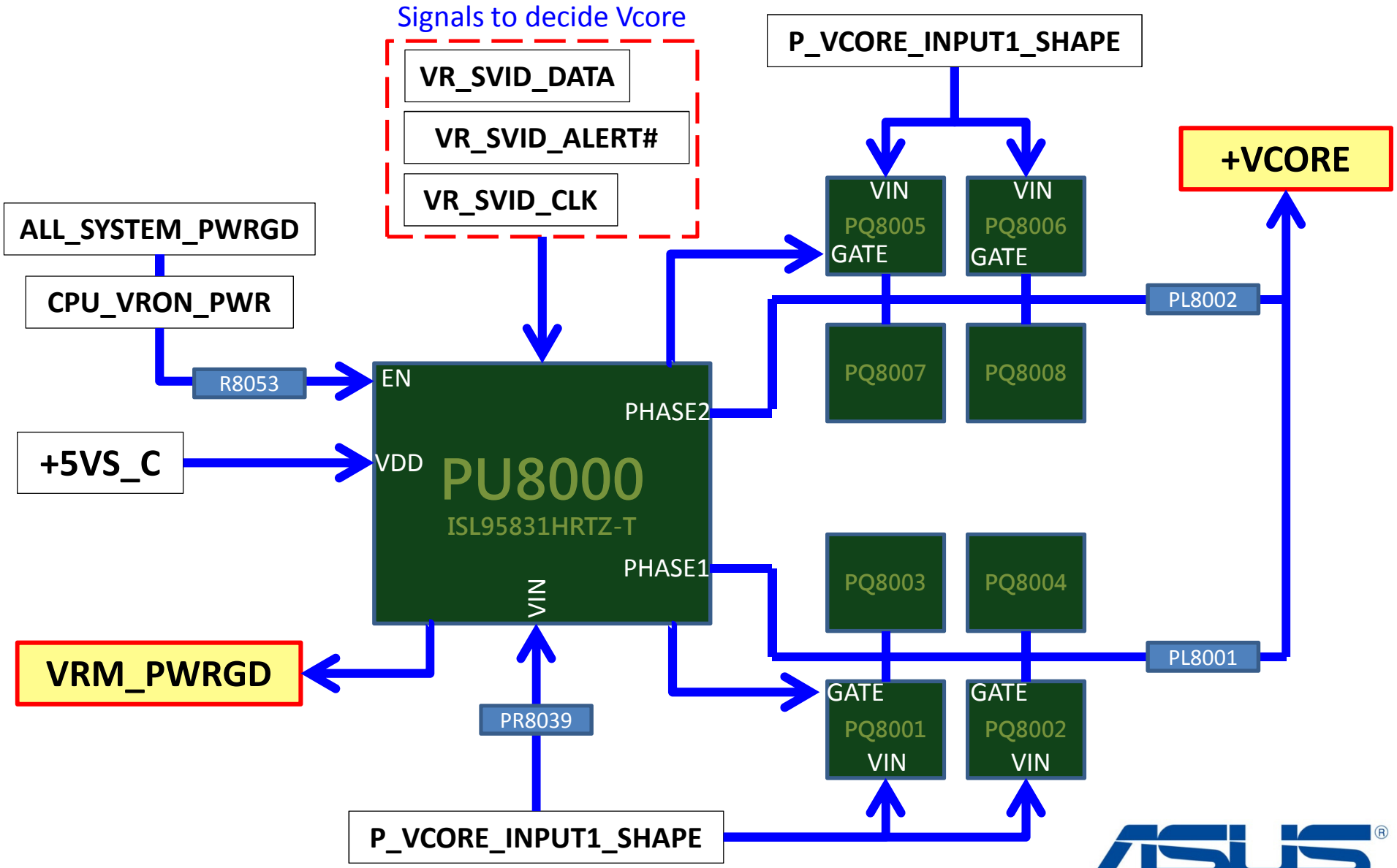
➢ VCORE Problems

+VCORE



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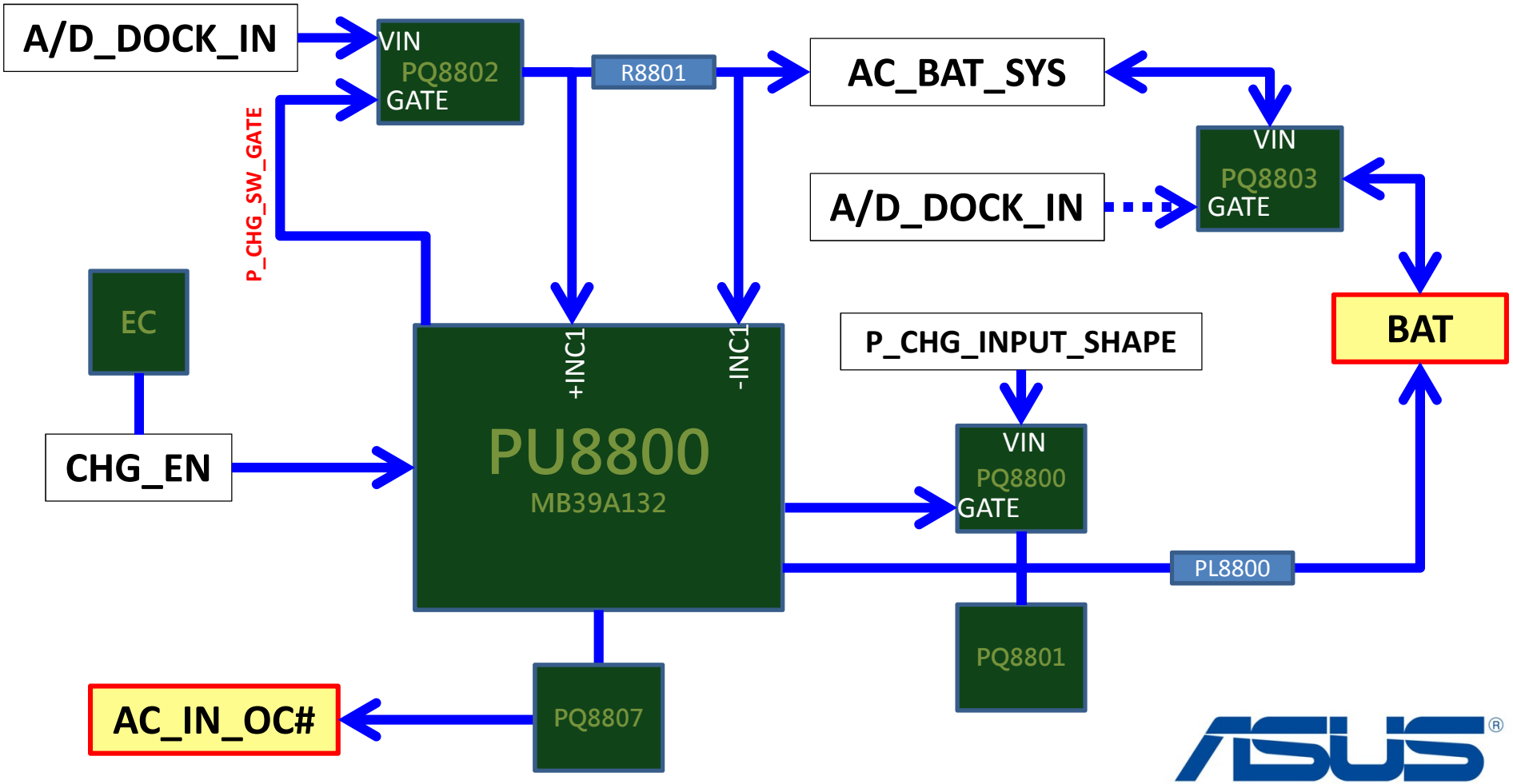
➢ Battery Charging Problems

Battery cannot be charged due to Power (BAT) problems



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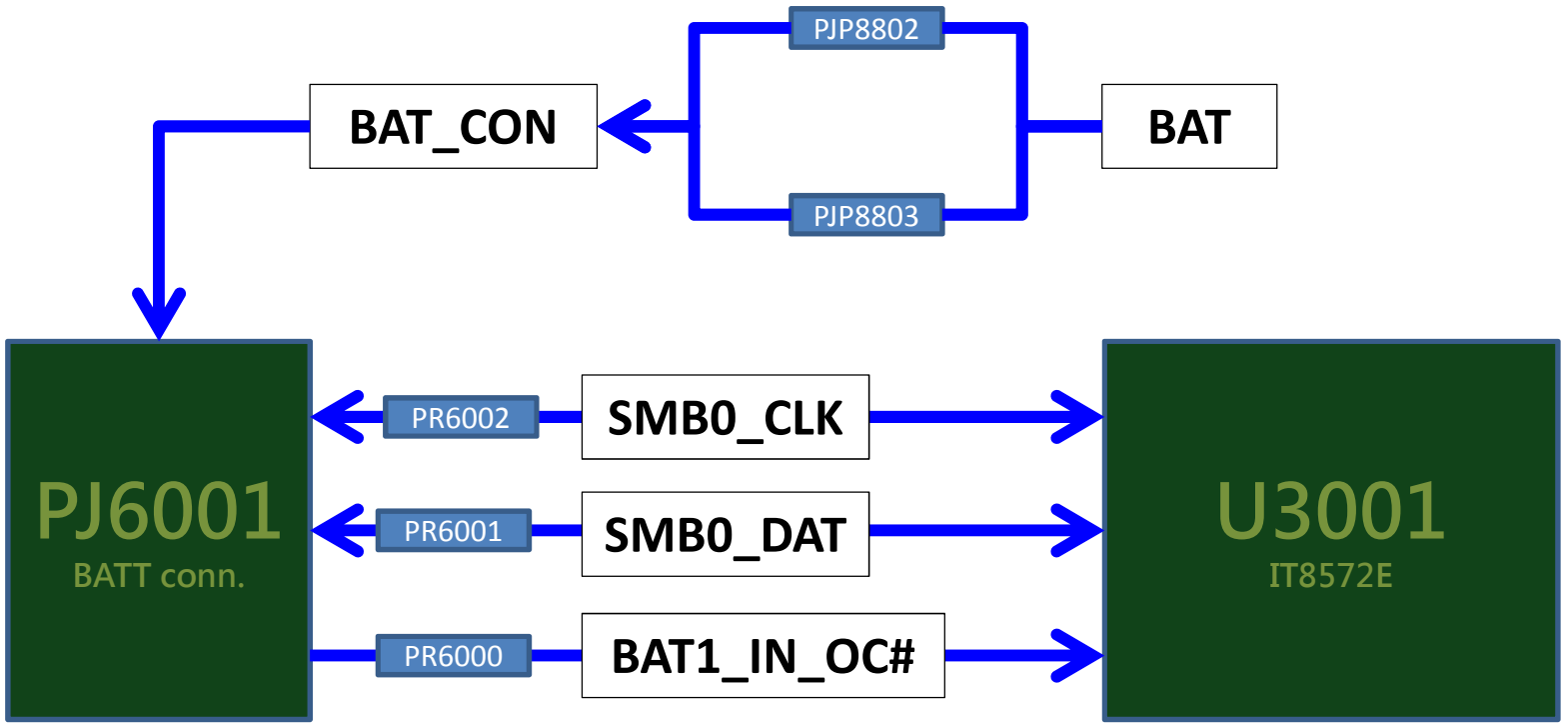
➢ Battery Charging Problems

Battery cannot be charged due to Signal detection problems



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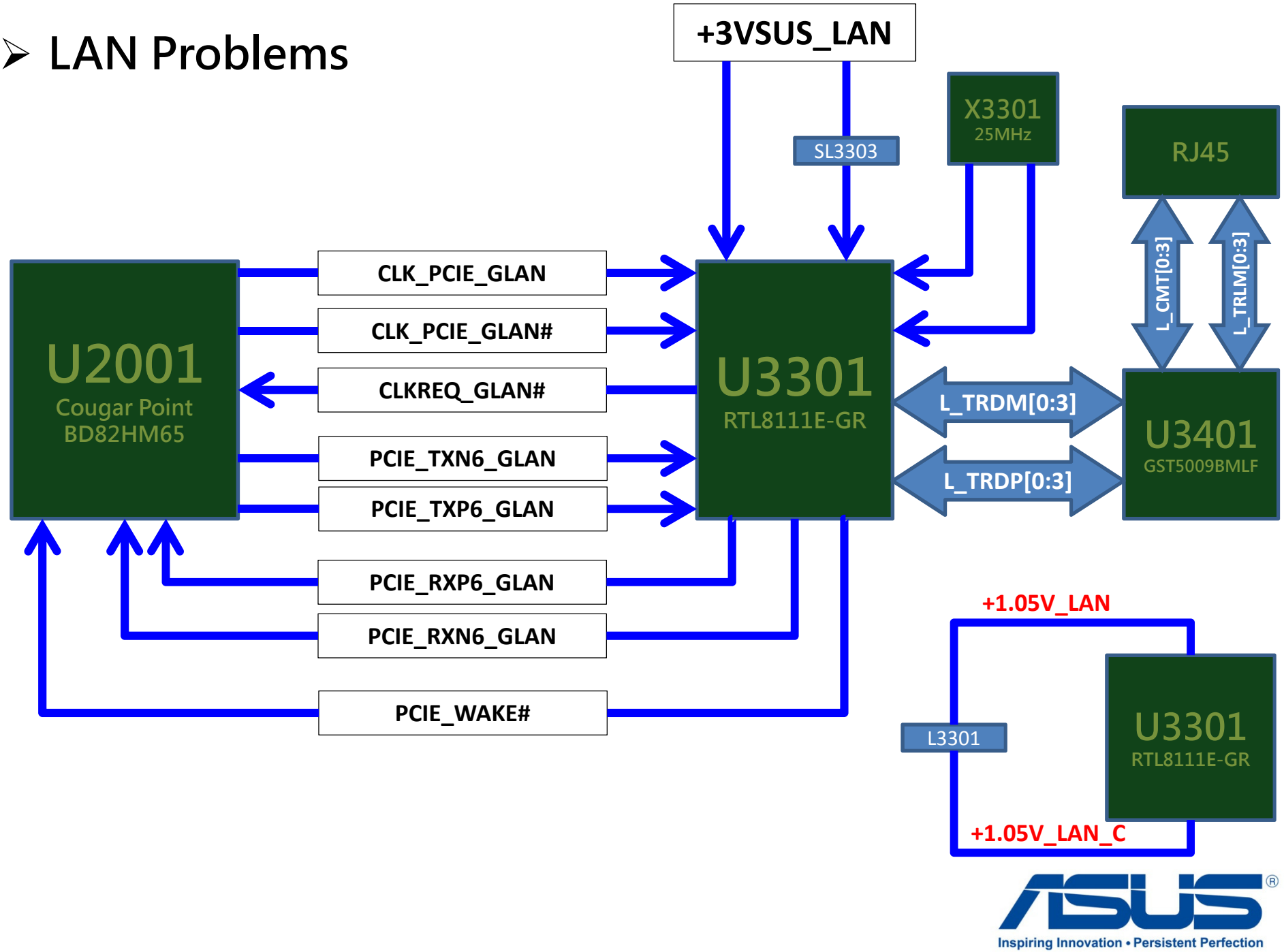
➢ LAN Problems



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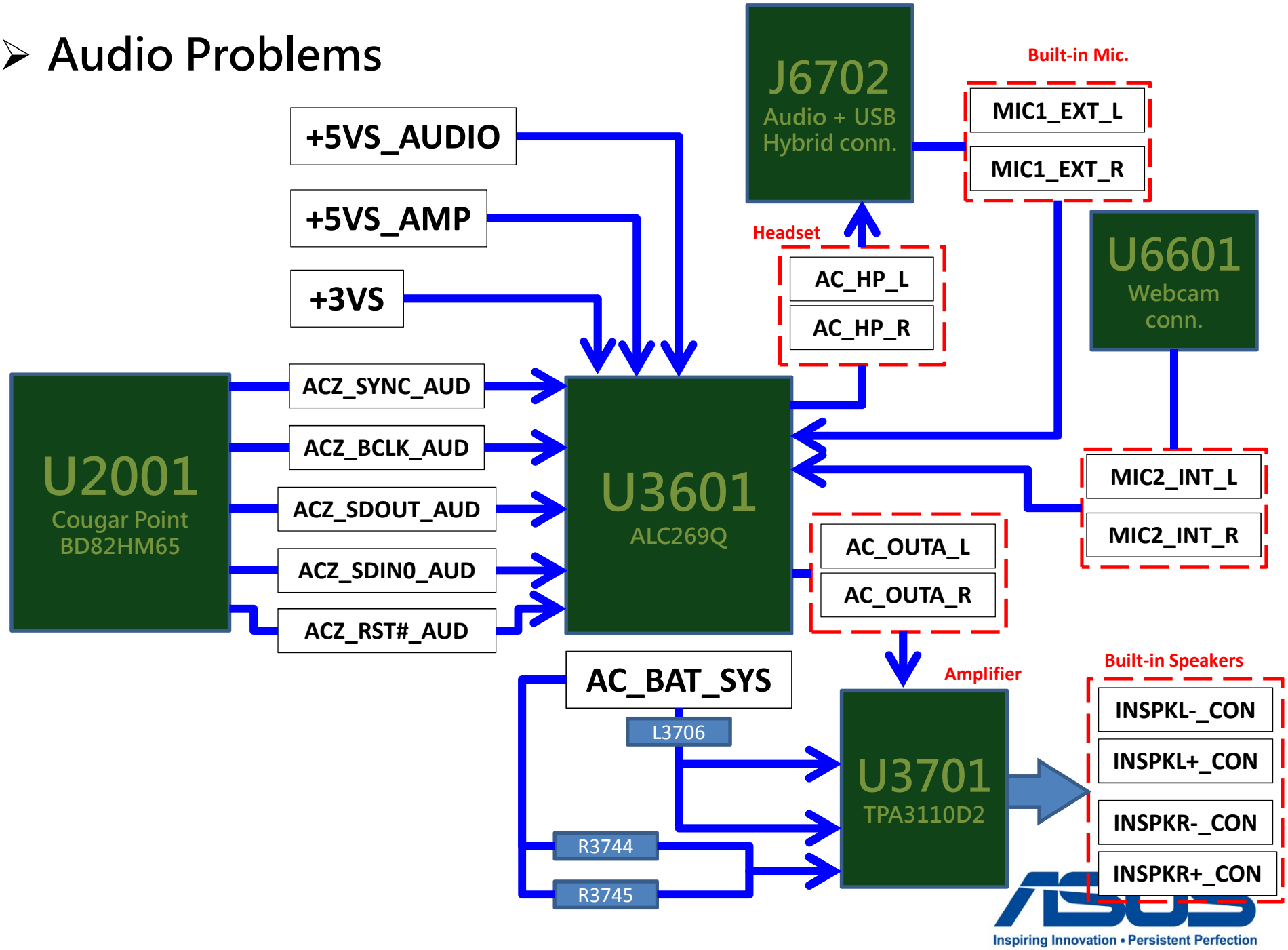
➢ Audio Problems



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THANK YOU

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