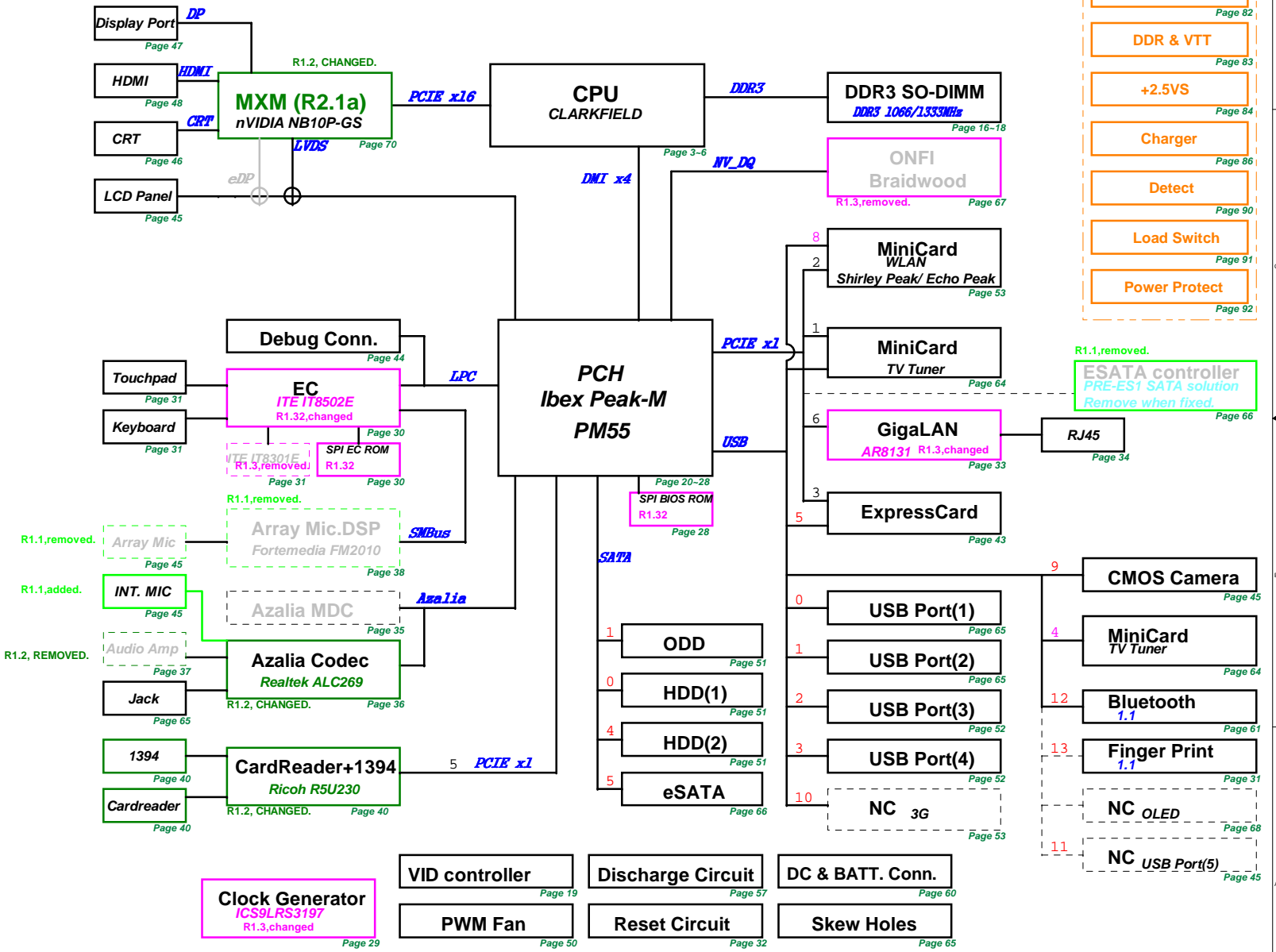


M60J SCHEMATIC Revision 2.00

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BLOCK DIAGRAM



Power

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R1.1, removed.
ESATA controller
 PRE-ES1 SATA solution
 Remove when fixed. Page 66

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	NC_TP	-	+3VS
GPIO 01	GPO	NC_TP	INT TBD	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	EXT PU	+5VS
GPIO 06	GPO	NC_TP	INT TBD	+3VS
GPIO 07	GPO	NC_TP	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	NC_PU	EXT PU	+3VSUS
GPIO 10	Native	NC_PU	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	NC_TP	-	+3VSUS
GPIO 13	GPO	NC_TP	-	+3VSUS
GPIO 14	GPO	NC_PU	EXT PU	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	+3VSUS
GPIO 16	GPI	DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 17	GPI	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	GPI	CLKREQ1#_TV	EXT PD	+3VS
GPIO 19	GPI	SATA1GP	EXT PU	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PD	+3VS
GPIO 21	GPI	SATA0GP	EXT PU	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	NC_TP	INT PU	+3VS
GPIO 24	GPO	NC_TP	-	+3VSUS
GPIO 25	GPI	CLKREQ3#_NEWCARD	EXT PD	+3VSUS
GPIO 26	GPI	CLK_REQ4#_CB	EXT PD	+3VSUS
GPIO 27	GPO	NC_TP	INT WEAK PU	+3VSUS
GPIO 28	GPO	WLAN_ON#	EXT PD	+3VSUS
GPIO 29	Native	NC_TP	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	GPO	ME_SusPwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	GPIO	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	HDA_DOCK_EN#	-	+3VS
GPIO 34	Native	NC_TP	-	+3VS
GPIO 35	GPO	SATA_CLK_REQ#	EXT PD	+3VS
GPIO 36	GPI	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	NC_PU	EXT PU	+3VSUS
GPIO 41	Native	NC_PU	EXT PU	+3VSUS
GPIO 42	Native	NC_PU	EXT PU	+3VSUS
GPIO 43	Native	NC_PU	EXT PU	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU	+3VSUS
GPIO 45	Native	NC_TP	EXT PU	+3VSUS
GPIO 46	Native	NC_TP	EXT PU	+3VSUS
GPIO 47	GPI	CLKREQ_PEG#	EXT PU	+3VSUS
GPIO 48	GPO	NC_TP	-	+3VS
GPIO 49	GPIO	PCH_TEMP_ALERT#	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	Native	DGPU_SELECT#_R	EXT PU	+5VS
GPIO 53	GPO	NC_TP	INT PU	+3VS
GPIO 54	Native	PCI_REQ3#	EXT PU	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	GPI	CLKREQ_GLAN#	EXT PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	GPIO	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	NC_PU	EXT PU	+3VSUS
GPIO 60	Native	SML0ALERT#	EXT PU	+3VSUS
GPIO 61	Native	NC_TP	-	+3VSUS
GPIO 62	Native	NC_TP	-	+3VSUS
GPIO 63	Native	NC_TP	-	+3VSUS
GPIO 64	Native	NC_TP	INT TBD	+3VS
GPIO 65	Native	NC_TP	INT TBD	+3VS
GPIO 66	Native	NC_TP	INT TBD	+3VS
GPIO 67	Native	NC_TP	INT TBD	+3VS
GPIO 72	Native	PM_BATLOW#	EXT PU	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU	+3VSUS
GPIO 74	Native	SML1ALERT#	EXT PU	+3VSUS
GPIO 75	GPIO	SML1_DATA	EXT PU	+3VSUS

EC GPIO	Use As	Signal Name
GPA0	0	PWR_LED#
GPA1	0	CHG_LED#
GPA2	-	-
GPA3	-	-
GPA4	0	LCD_BL_PWM
GPA5	0	FAN0_PWM
GPA6	-	-
GPA7	-	-
GPB0	0	BATSEL_0
GPB1	0	BATSEL_1
GPB2	0	ME_AC_PRESENT_EC
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	0	A20GATE
GPB6	0	RCIN#
GPB7	0	PM_RSMRST#
GPC0	-	-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	0	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	0	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	0	EXT_SCI#
GPD4	0	EXT_SMI#
GPD5	0	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	-	-
GPE0	0	VSUS_ON
GPE1	0	EGAD (IT8301 Address/Data connect)
GPE2	0	EGCS (IT8301 Cycle Start connect)
GPE3	0	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5	-	-
GPE6	I	LID_SW#
GPE7	-	-
GPF0	0	-
GPF1	-	-
GPF2	I	EXP_GATE#
GPF3	-	-
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	0	THRO_CPU
GPF7	0	PCH_SPI_OV
GPG0	I	ME_SusPwrDnAck_EC
GPG1	I	PM_SUSB#
GPG2	-	-
GPG6	-	-
GPH0	IO	PM_CLKRUN#
GPH1	0	GFX_VR_ON
GPH2	0	CHG_EN
GPH3	0	SUSC_EC#
GPH4	0	SUSB_EC#
GPH5	0	NUM_LED#
GPH6	0	CAP_LED#
GPI0	-	-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ALERT#
GPI5	I	ALS_AD
GPI6	I	CAP_ACK_A#
GPI7	I	CAP_ACK_B#
GPJ0	0	CPU_VRON
GPJ1	0	PM_PWROK
GPJ2	0	VSET_EC
GPJ3	0	ISET_EC
GPJ4	0	TP_LED
GPJ5	-	-

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SusPwrDnAck
GPIO2	-	-
GPIO3	-	-
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	0	ME_AC_PRESENT
GPIO7	-	-
GPIO8	-	-
GPIO9	-	-
GPIO10	-	-
GPIO11	-	-
GPIO12	0	ME_PWROK
GPIO13	-	-
GPIO14	0	ME_SLP_M_ECH#
GPIO15	-	-
GPIO16	-	-
GPIO17	-	-
GPIO18	-	-
GPIO19	-	-
GPIO20	-	-
GPIO21	-	-
GPIO22	-	-
GPIO23	-	-
GPIO24	-	-
GPIO25	-	-
GPIO26	-	-
GPIO27	-	-
GPIO28	-	-
GPIO29	-	-
GPIO30	-	-
GPIO31	-	-
GPIO32	-	-
GPIO33	-	-
GPIO34	-	-
GPIO35	-	-
GPIO36	-	-
GPIO37	-	-

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	SM-Bus Address
Clock Generator(IC59LRS3197)	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
VID Controller(ASM8272)	0011011x (36)
WiFi/WiMax	N/A
EC Master (SMB1)	
SM-Bus Device	SM-Bus Address
CPU Thermal Sensor	-
VGA Thermal IC(G781-1)	1001101x (9A)

Device Identification

CPU Thermal Sensor P/N:		component name
1st		
S		
S		
S		

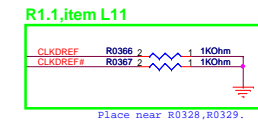
Clock Gen P/N:		component name
1st	06G011604010	ICS9LRS3197
S		
S		

VGA Thermal Sensor		component name
1st	06G023048020	G781-1
S		
S		

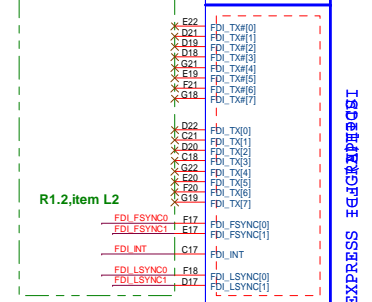
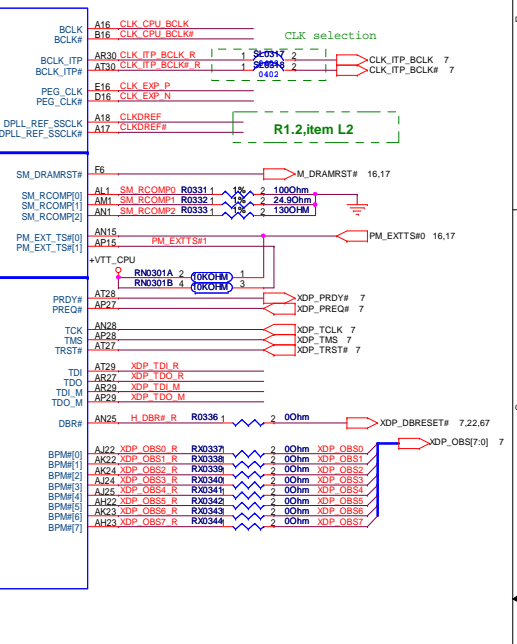
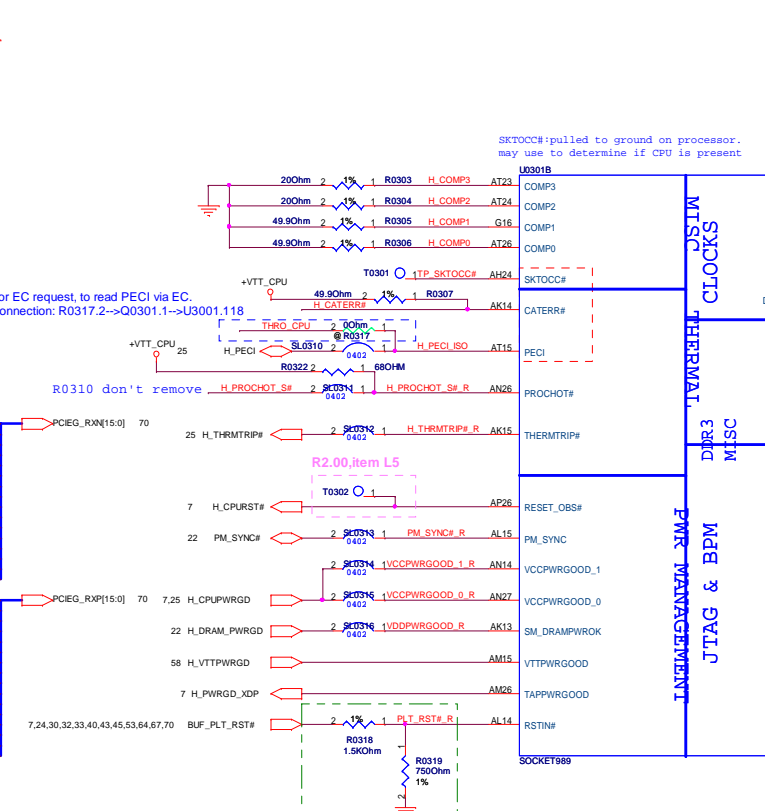
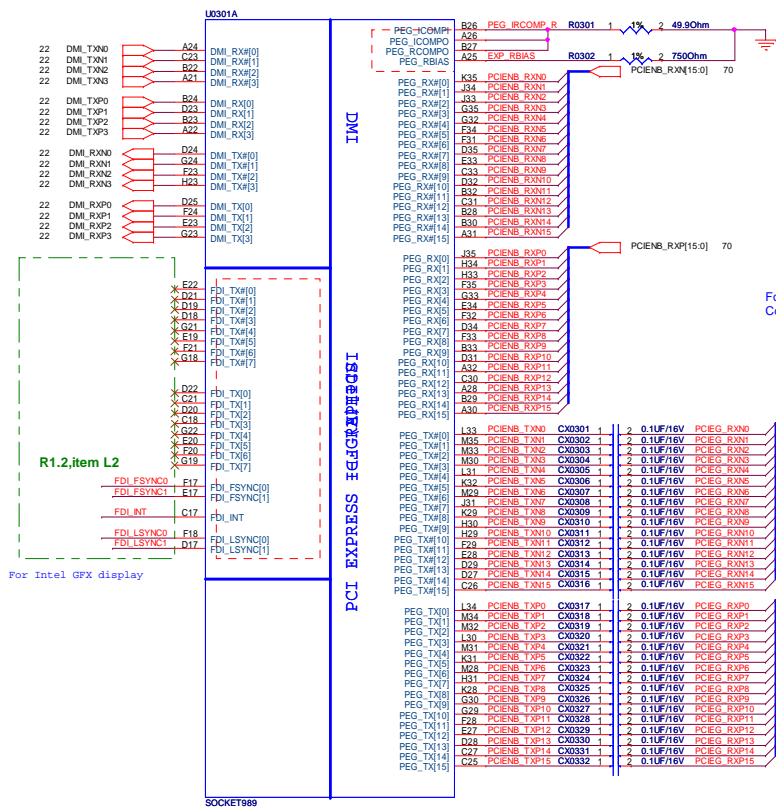
PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	Card reader
PCIE 6	GLAN
PCIE 7	
PCIE 8	

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

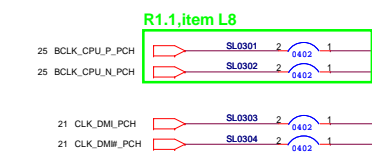
USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	Minicard TV Tuner
USB 5	NewCard
USB 6	
USB 7	
USB 8	WLAN
USB 9	CMOS Camera
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	Finger Printer



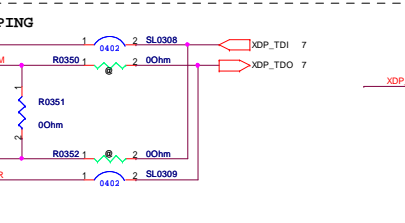
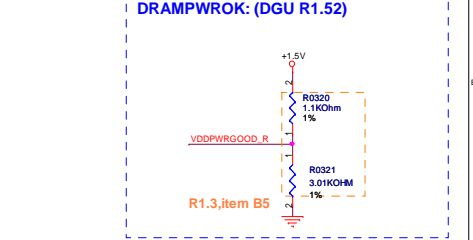
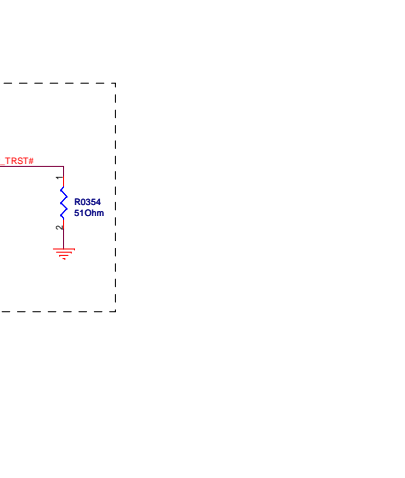
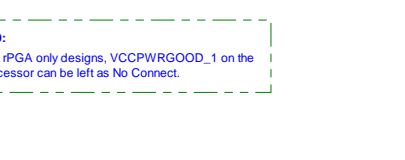
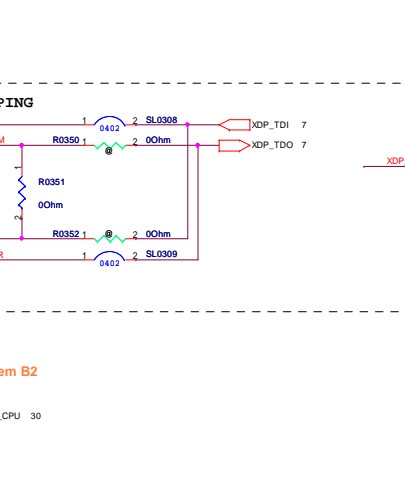
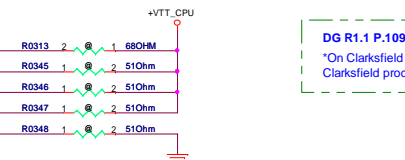
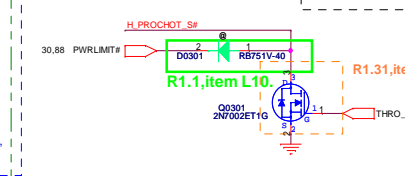
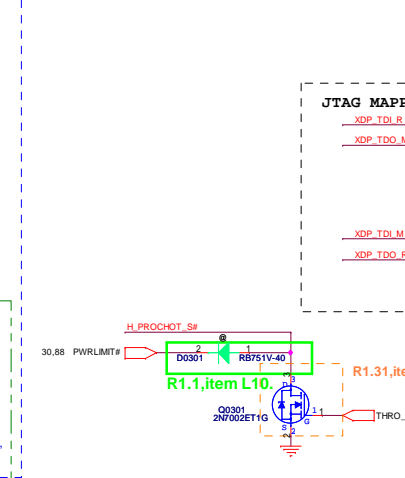
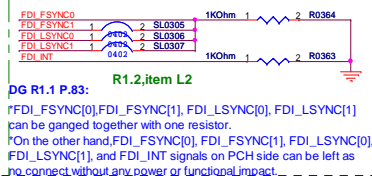
Place near R0328, R0329.



For Intel GFX display

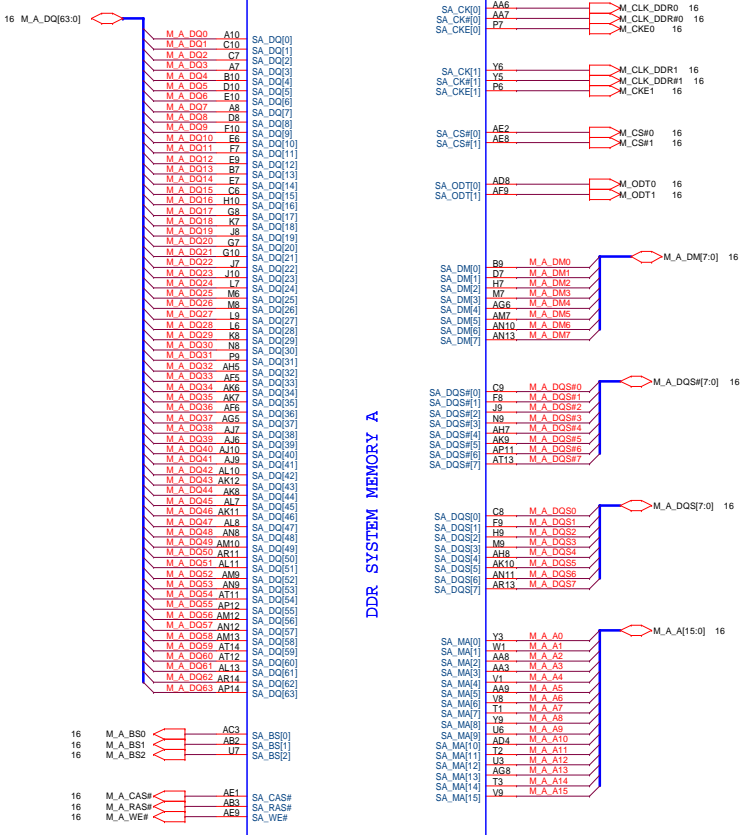


FDI disable: (For discrete graphic)
1. NC: FDI_TX#(0:7), FDI_RX#(0:7), FDI_RX#(0:7), FDI_RX#(0:7)
VCC_AXGSENSE, VSS_AXGSENSE
2. Pull-down to GND via 1KΩ ± 5% resistor: FDI_FSYNC(0:1), FDI_FSYNC(0:1), FDI_INT, GFX_IMON
~15mW power saving: (DG R0.8 P.70)
3. Connected to GND: VCCAXG,
4. Can be connected to GND directly: DPLL_REF_CLK, DPLL_REF_CLK#
5. Connect to +V1.05S rail: VCCFDIPLL



ASUS Logo, Title: CPU(1)_DMI,PEG,FDI,CLK,MISC, Engineer: James1_Wu, Project Name: M60J, Date: Friday, July 10, 2009, Sheet 3 of 99

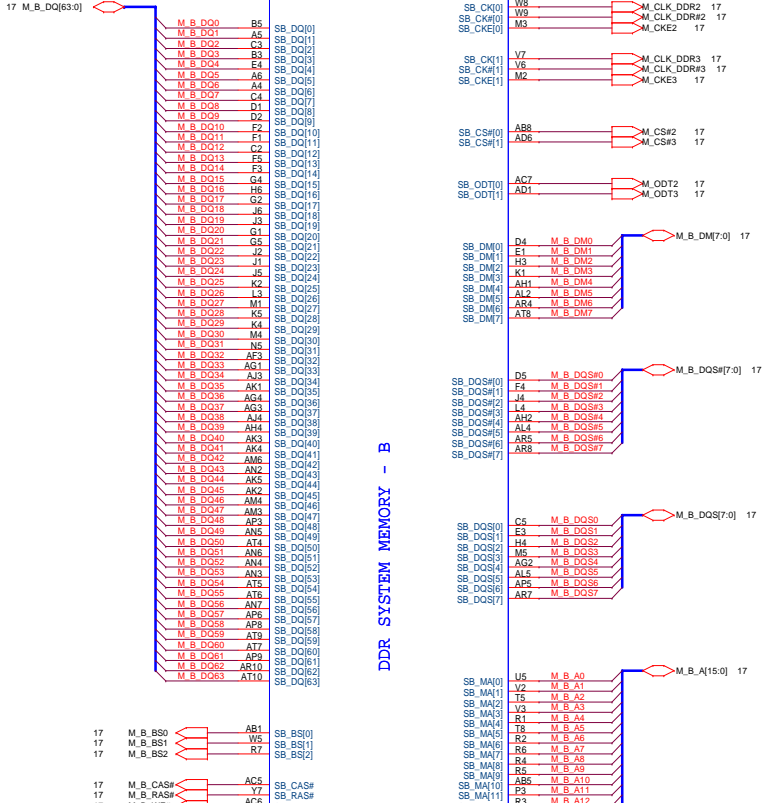
U301C



DDR SYSTEM MEMORY A

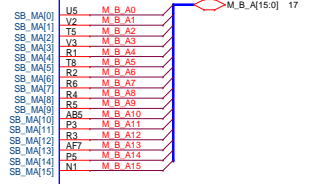
SOCKET989

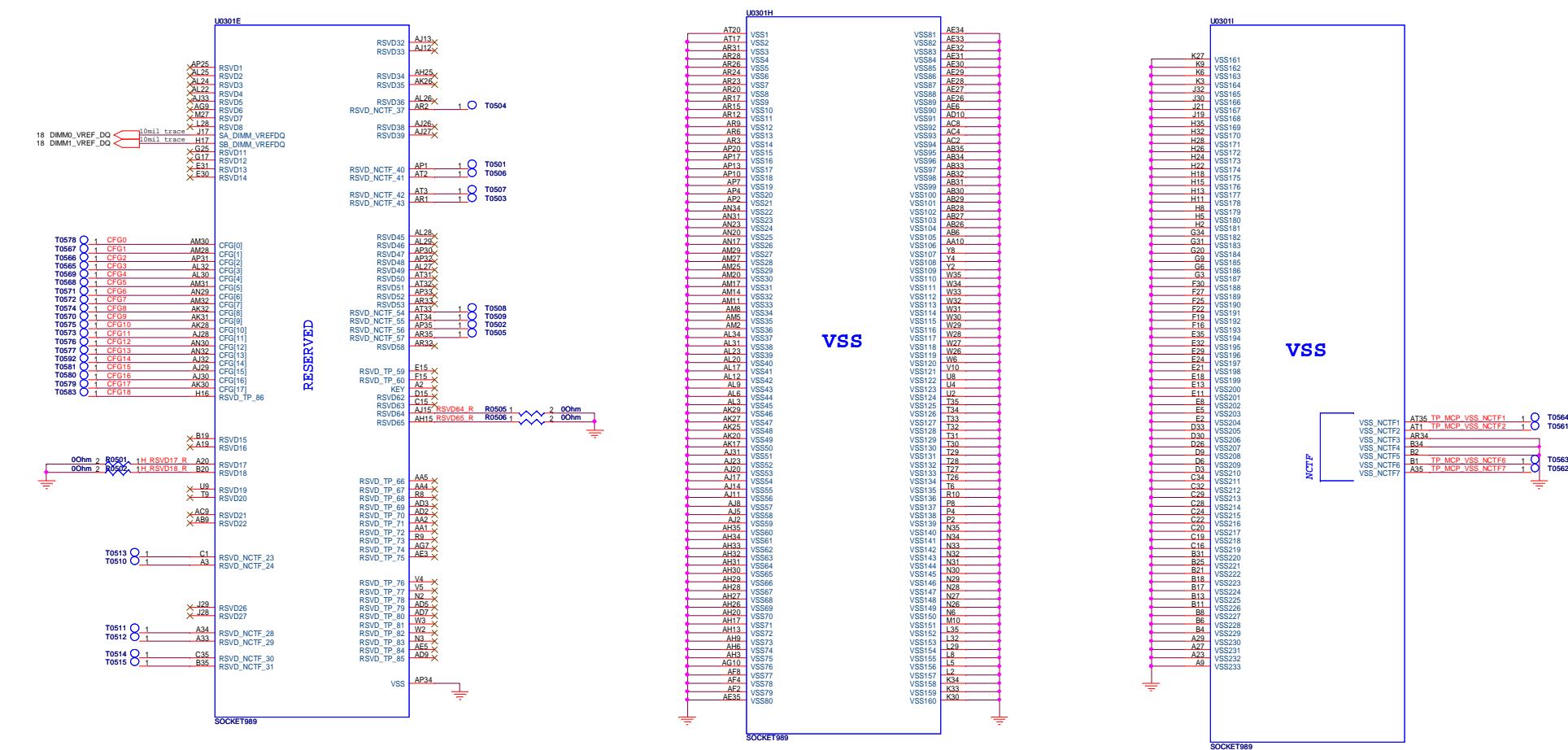
U301D



DDR SYSTEM MEMORY - B

SOCKET989

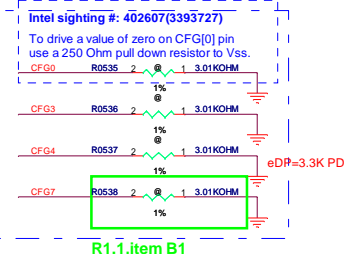




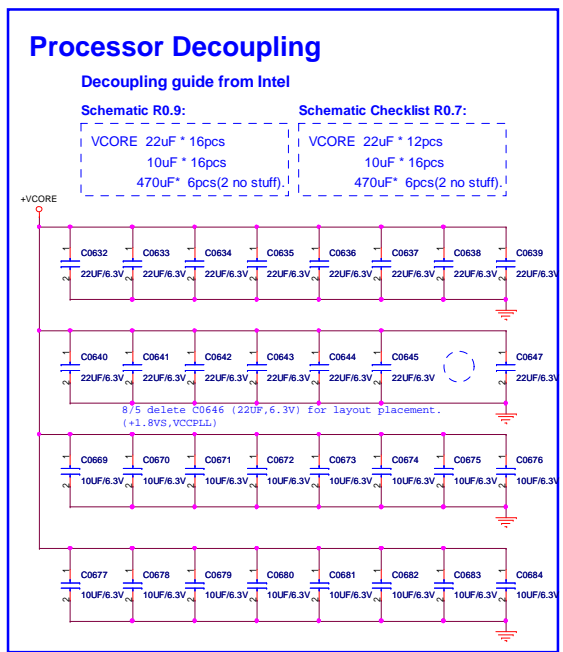
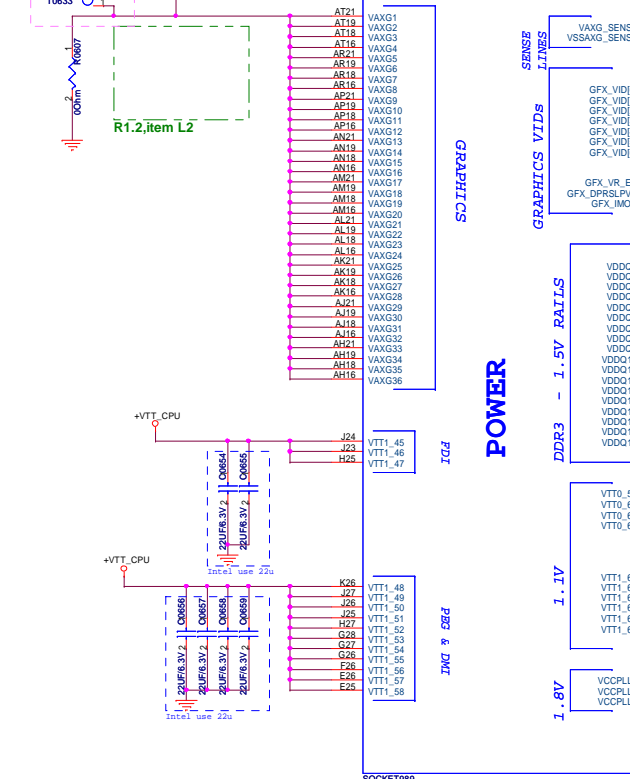
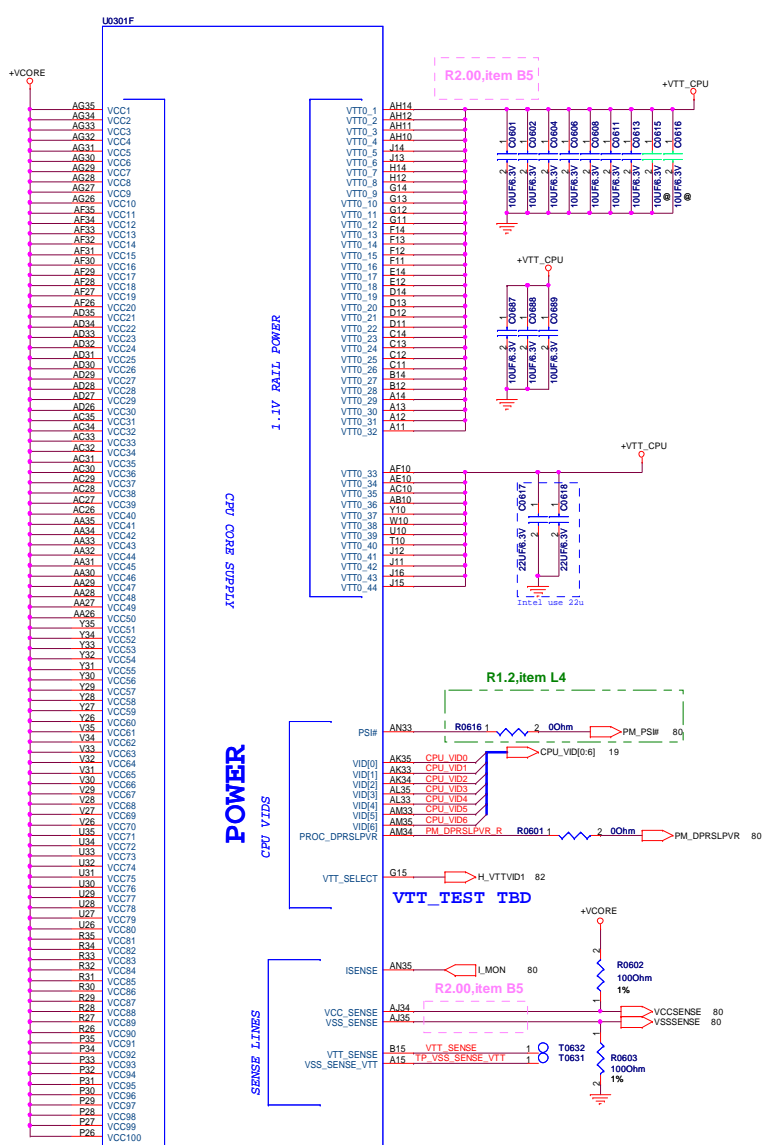
CFG strapping information:

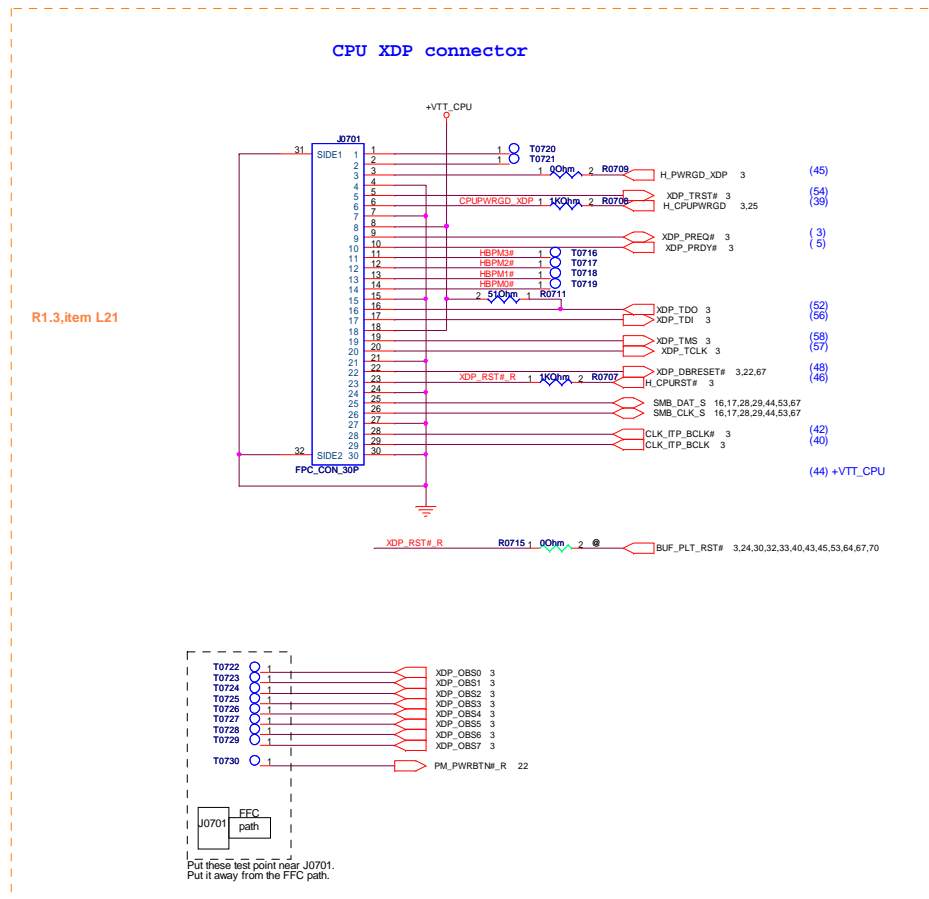
- CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield)**
 - 11 = 1 x 16 PEG (Default)
 - 10 = 2 x 8 PEG
- CFG[3]: PCIe Static Numbering Lane Reversal.(Auburndale Only)**
 - 1:Normal Operation (Default)
 - 0: Lane Numbers Reversed 15 > 0, 14 > 1, ...
- CFG[4]: Embedded DisplayPort Detection.(Auburndale Only)**
 - 1: Disabled - No Physical Display Port attached to Embedded DisplayPort
 - 0: Enabled - An external Display Port device is connected to the Embedded Display Port
- CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)**
 Clarksfield (only for early samples pre-E31) - Connect to GND with 3.01K Ohm/5% resistor for a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.
Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.
 Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



Add Jumper to measure power?





R1.3,item L21

5

4

3

2

1

D

D

C


C

B

B

A

A

		Title : NB ****	
ASUSTek COMPUTER INC. NB1		Engineer: <i>James1_Wu</i>	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date: Thursday, July 02, 2008		Sheet	8 of 99

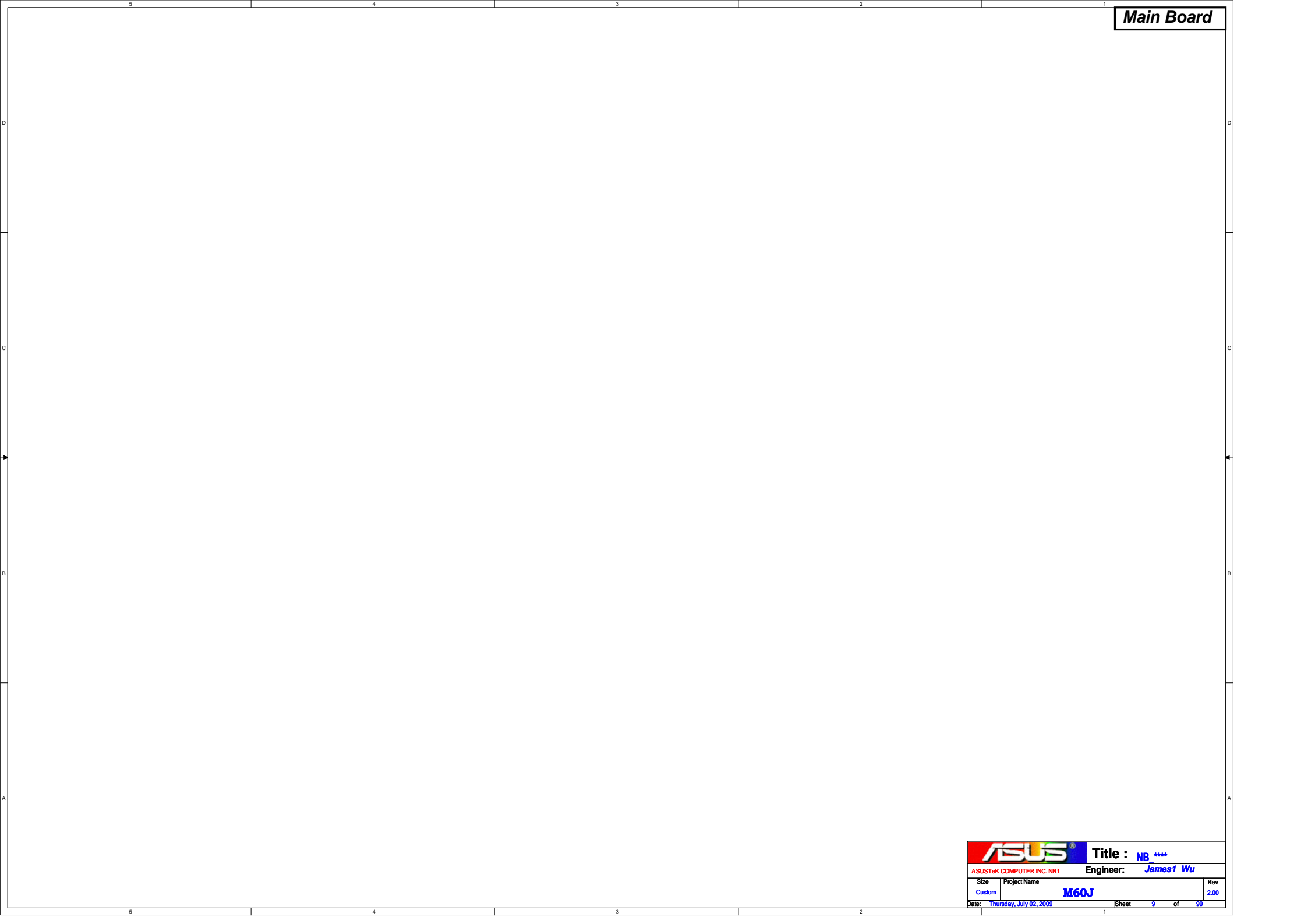
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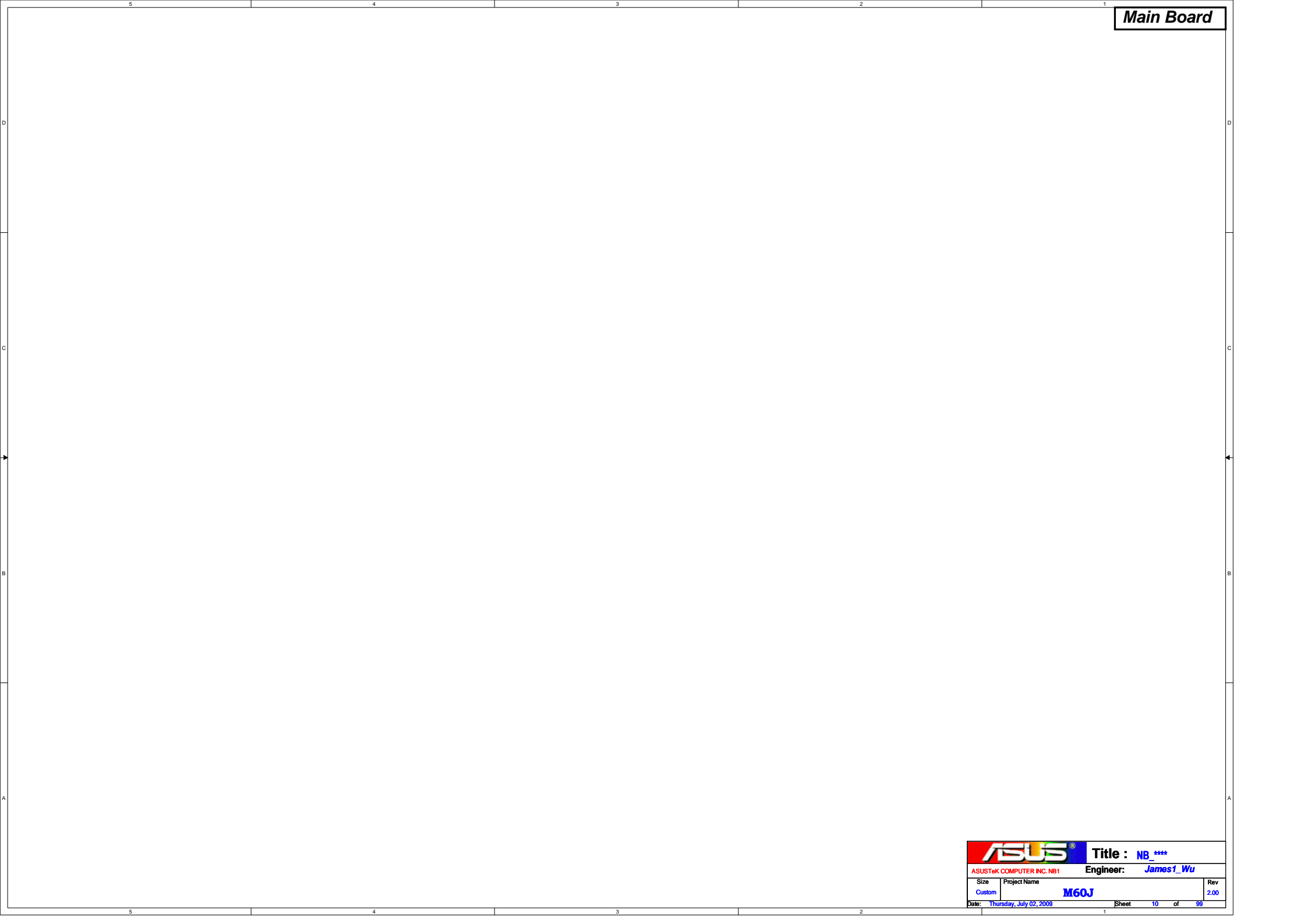
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2

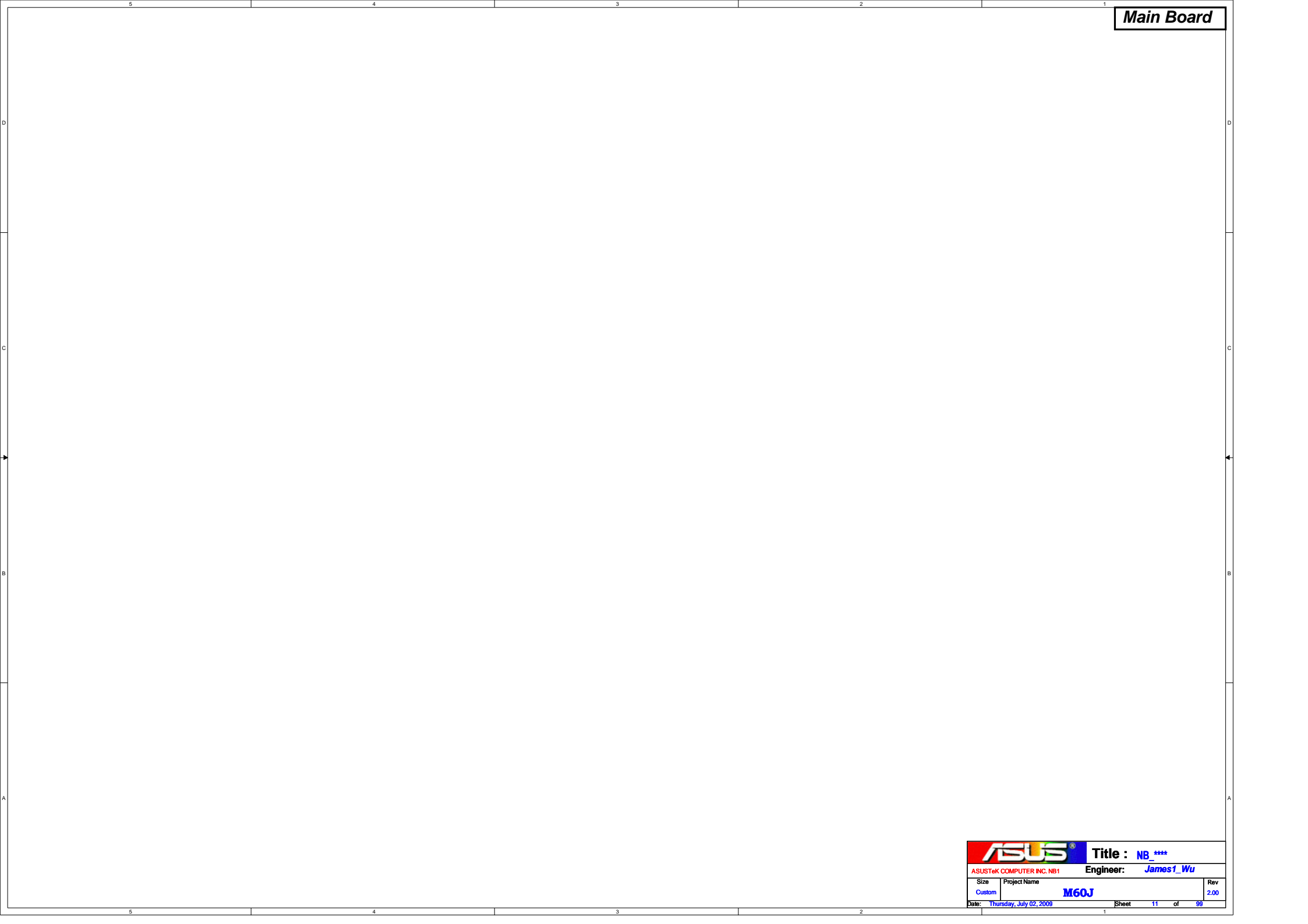
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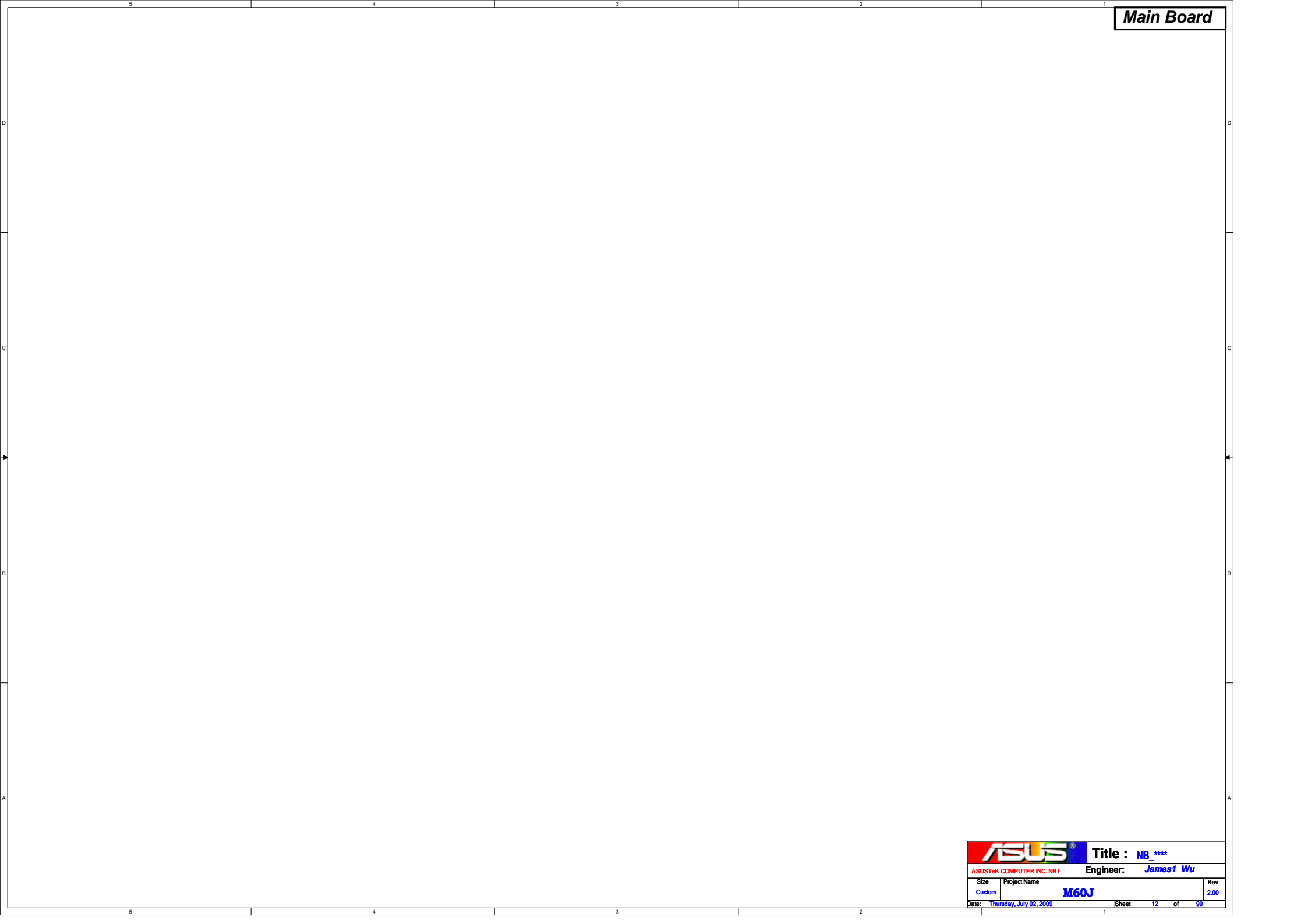
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ASUSTek COMPUTER INC. NB1		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date: Thursday, July 02, 2008		Sheet	9 of 99




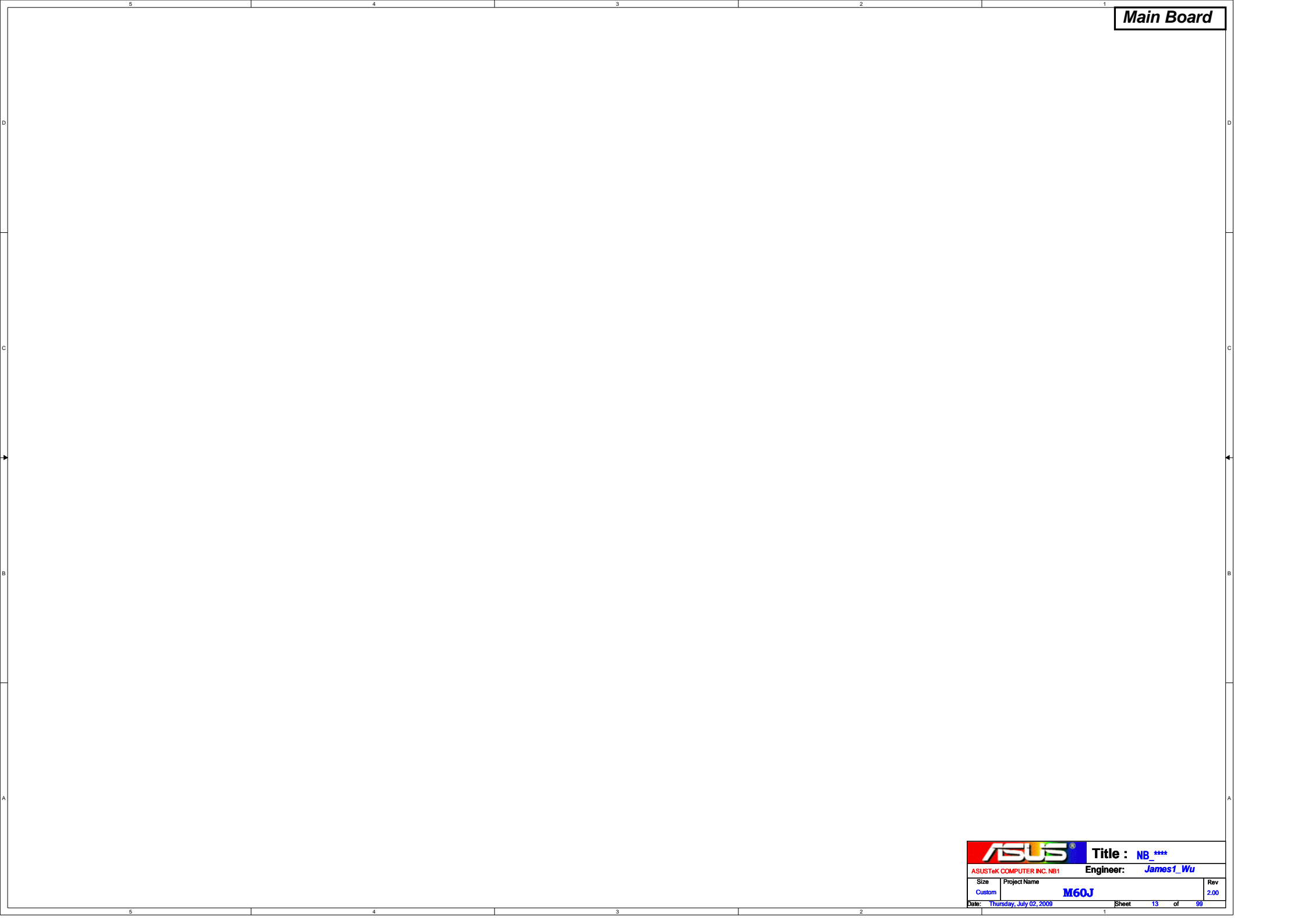
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ASUSTek COMPUTER INC. NB1		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date:	Thursday, July 02, 2008	Sheet	10 of 99




		Title : NB ****	
ASUSTek COMPUTER INC. NB1		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date: Thursday, July 02, 2008	Sheet	11	of 99



		Title : NB ****	
ASUSTek COMPUTER INC. NB1		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date: Thursday, July 02, 2008	Sheet	12	of 99



		Title : NB ****	
ASUSTek COMPUTER INC. NB1		Engineer: James1_Wu	
Size	Project Name		Rev
Custom	M60J		2.00
Date: Thursday, July 02, 2008		Sheet 13 of 99	

5

4

3

2

1

D

D

C

C

B

B

A

A



Title :

ASUSTeK COMPUTER INC. NB6

Engineer: *James1_Wu*

Size	Project Name	Rev
A	M60J	2.00

Date: *Thursday, July 02, 2009*

Sheet *14* of *99*

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

		Title :
ASUSTeK COMPUTER INC. NB6		Engineer: <i>James1_Wu</i>
Size	Project Name	Rev
A	M60J	2.00
Date: <i>Thursday, July 02, 2009</i>		Sheet <i>15</i> of <i>99</i>

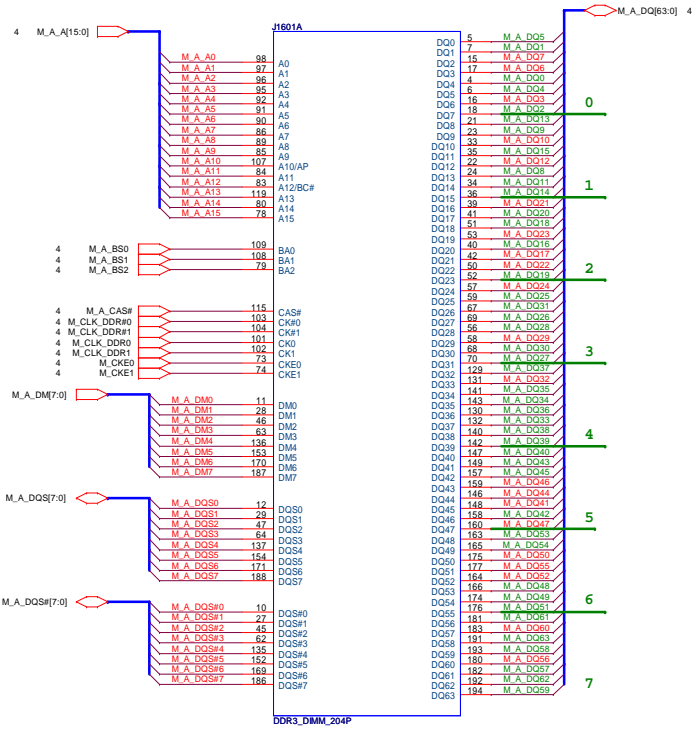
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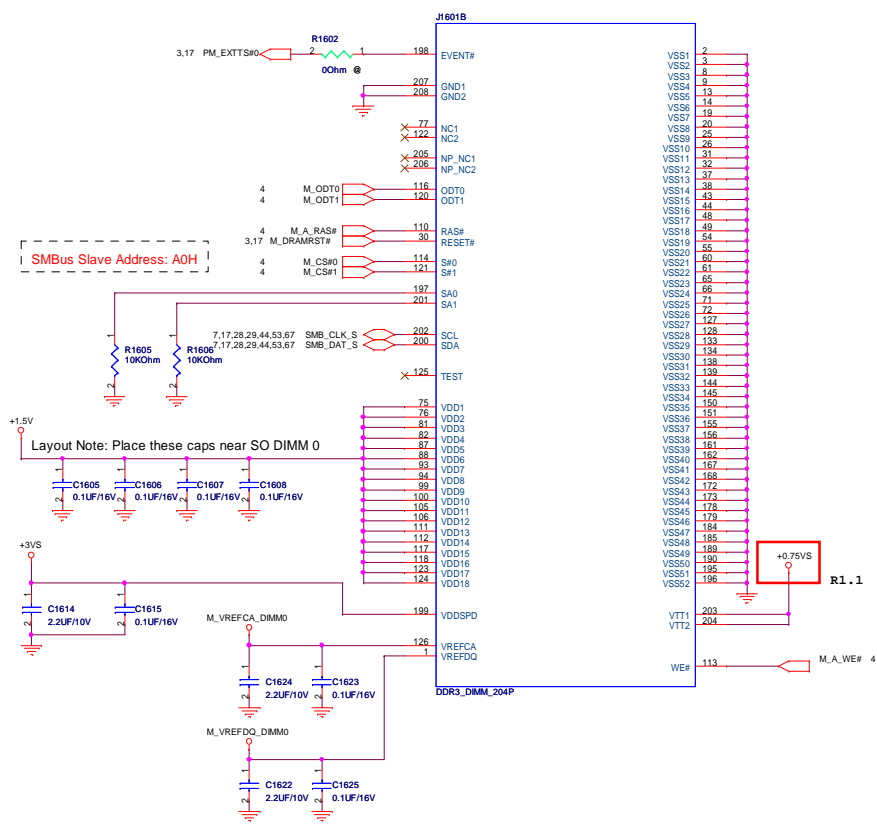
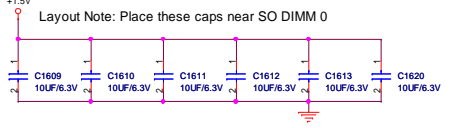
3

2

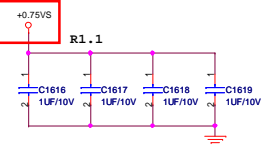
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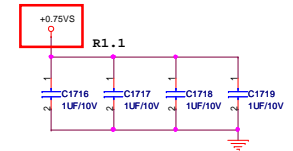
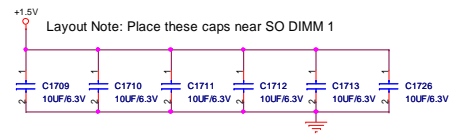
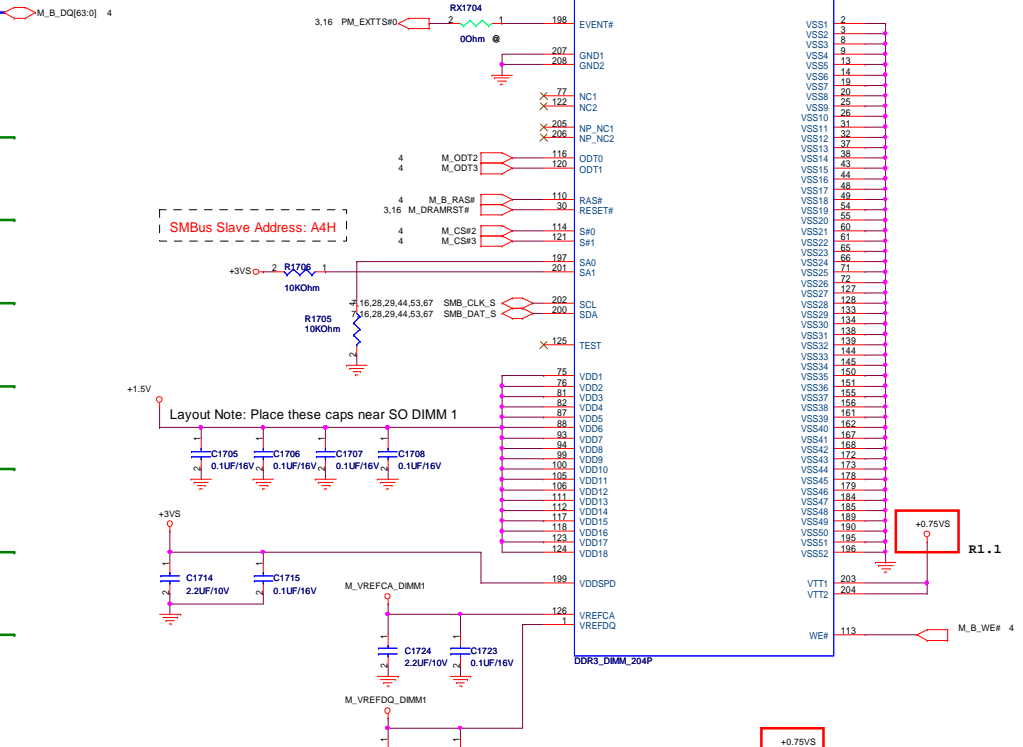
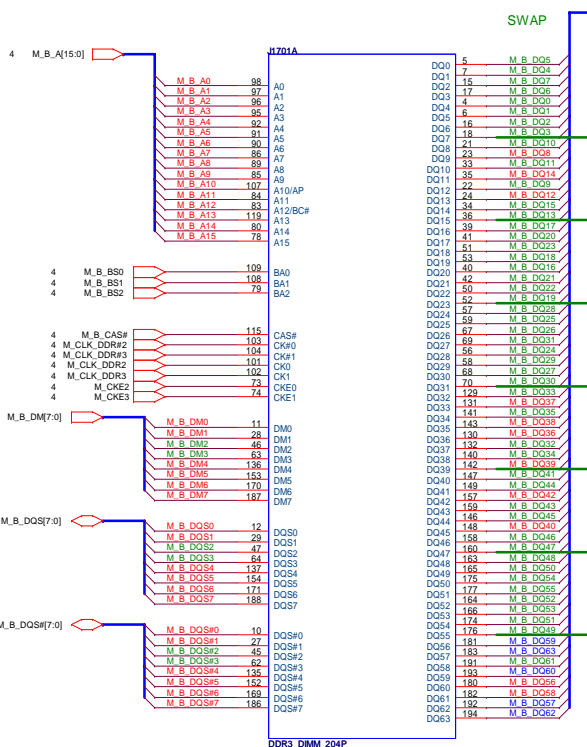


REV 9.2mm



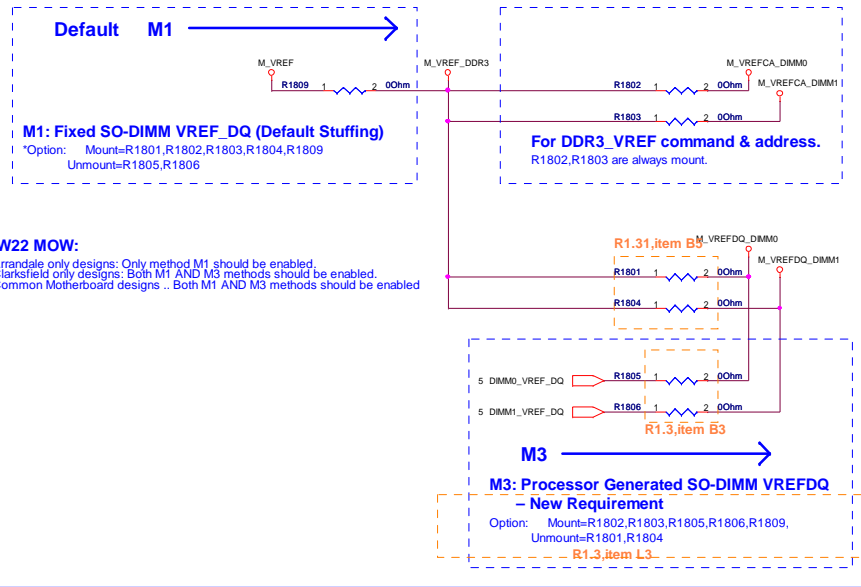
Layout Note: Place these caps near SO DIMM 0



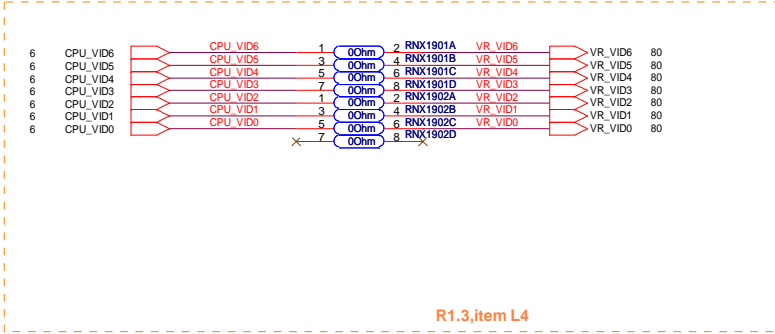


DDR3 Vref

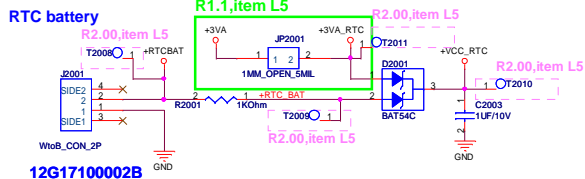
Intel Document Number: 400755
 Calpella Clarksfield DDR3 SO-DIMM VREFDQ
 Platform Design Guide Change Details



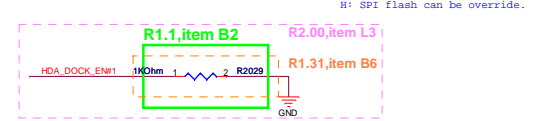
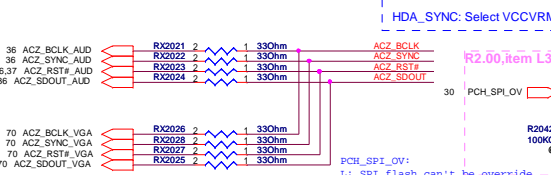
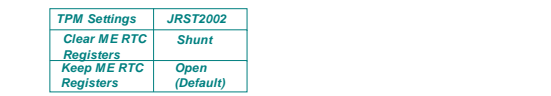
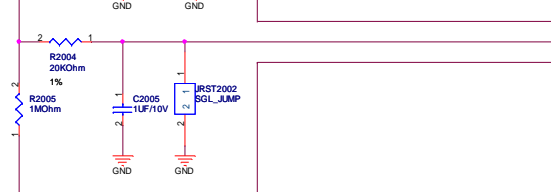
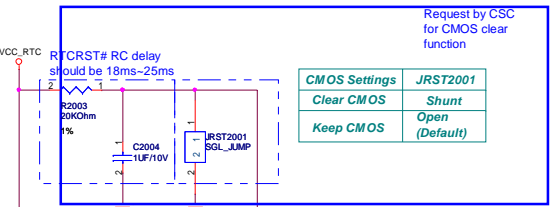
R1.3,item L3



R1.3,item L4



12G17100002B



WW22 MOW: HDA_DOCK_EN# pull-down resistor changed to 1K Ohm.

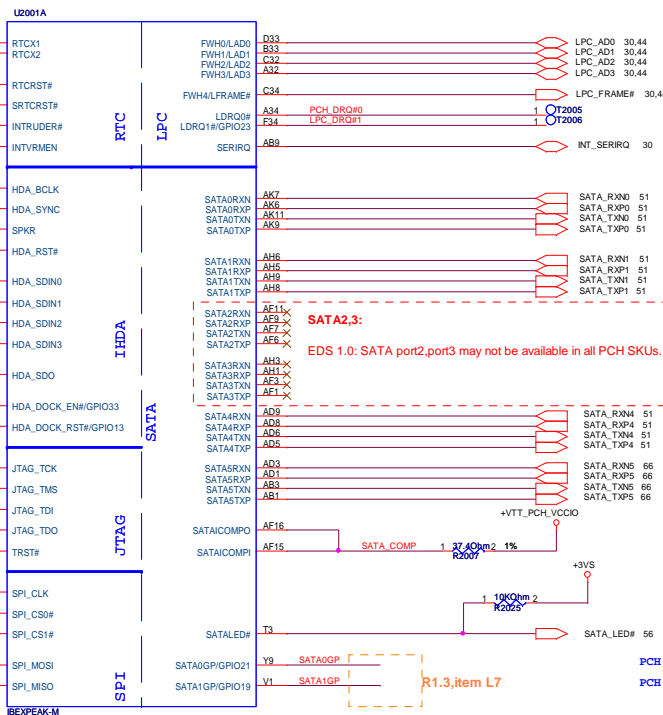
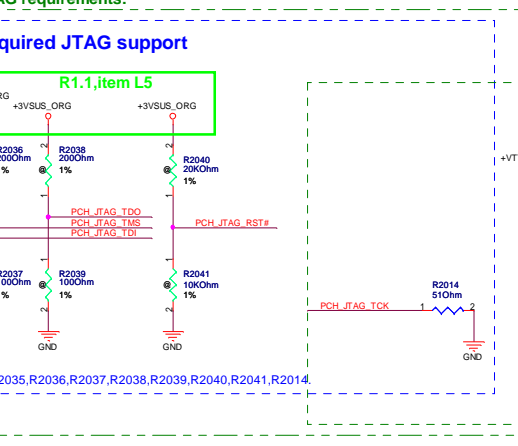
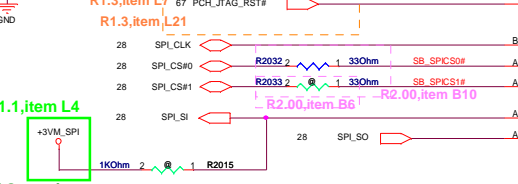
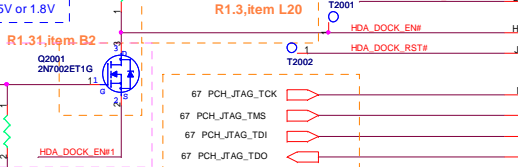
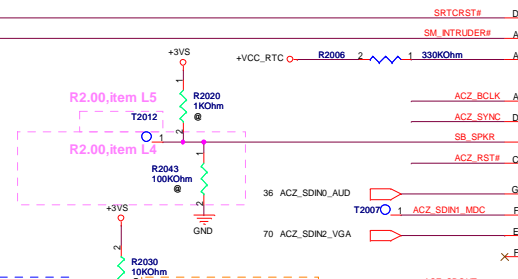
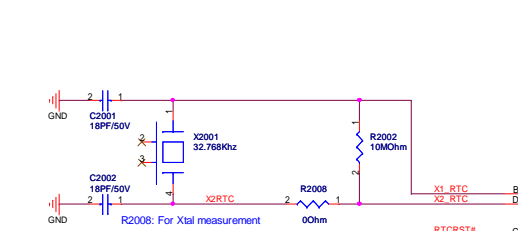
414044 Design Guide R1.11 Update: page9
 GPIO33: This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY. Without connecting GPIO33, customers may not be able to override SPI flash contents.

Strap information:

HDA_SPKR: No reboot strap
 Low: Disable.
 High: Enable

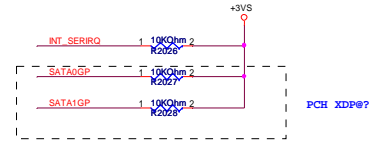
HDA_DOCK_EN#:
 1. Flash descriptor security: Sampled low: override. Sampled high: in effect.
 2. GPIO33 low on the rising edge of PWROK, Will also disable Intel ME.

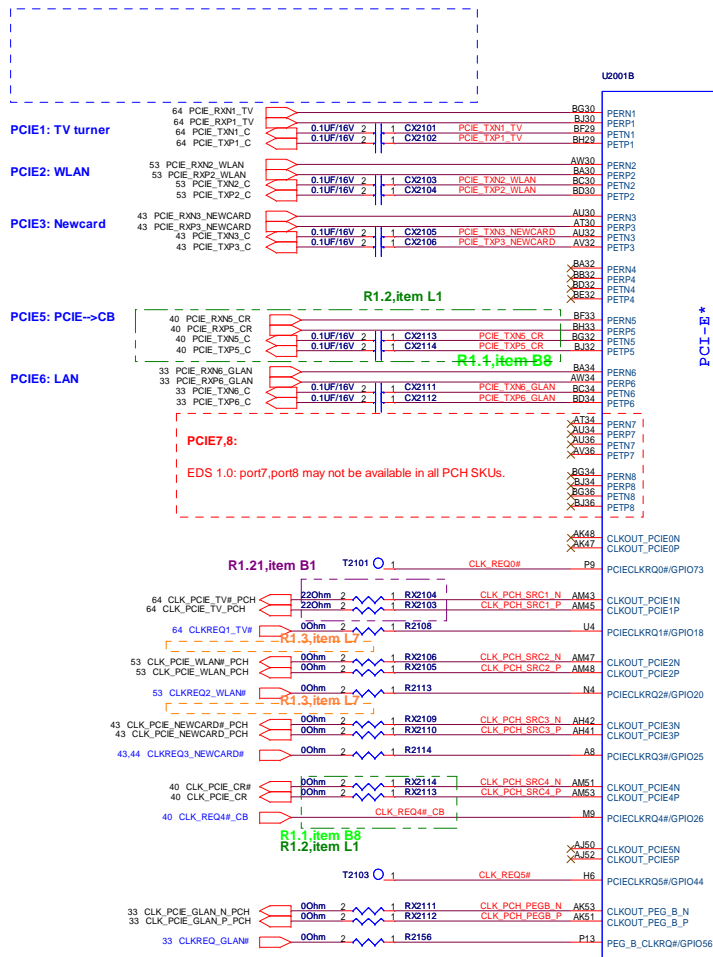
SPI_MOSI: iTPM strap.
 Mount R2015: Enable
 Unmount R2015: Disable(default)



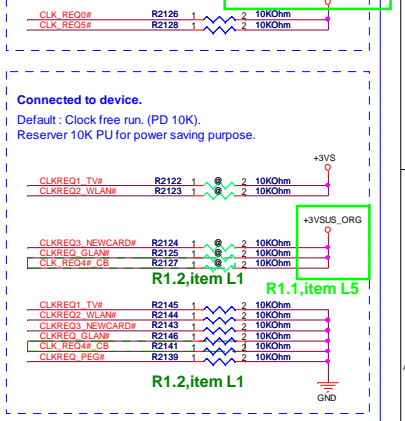
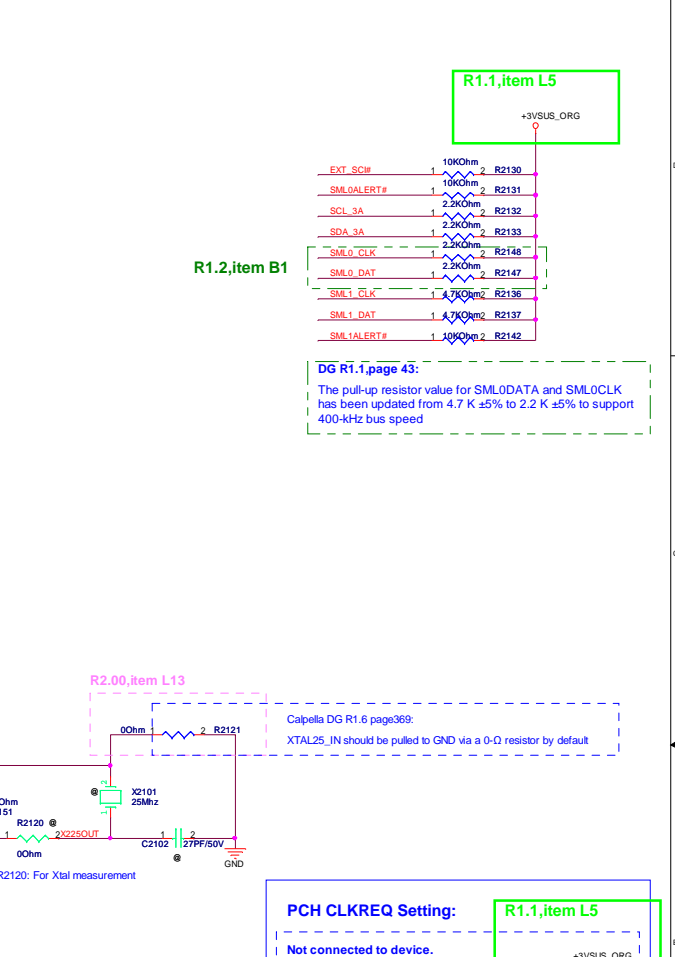
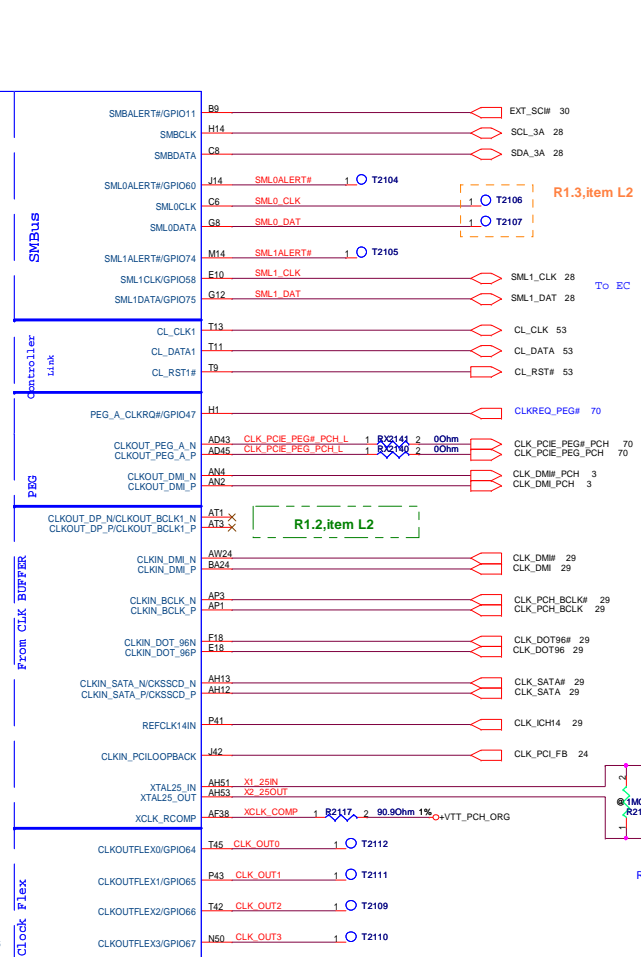
SATA2,3:
 EDS 1.0: SATA port2,port3 may not be available in all PCH SKUs.

MoW36 IbexPeak JTAG requirements:
 ES1 Enable: Mount R2034, R2035, R2036, R2037, R2040, R2041, R2014, DNI R2038, R2039, (TDO)
 ES1 Disable: Mount R2040, R2041, R2014, DNI: others.

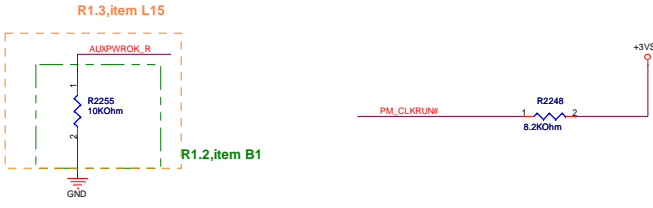




Note: Place these resistors near to PCIe Slots

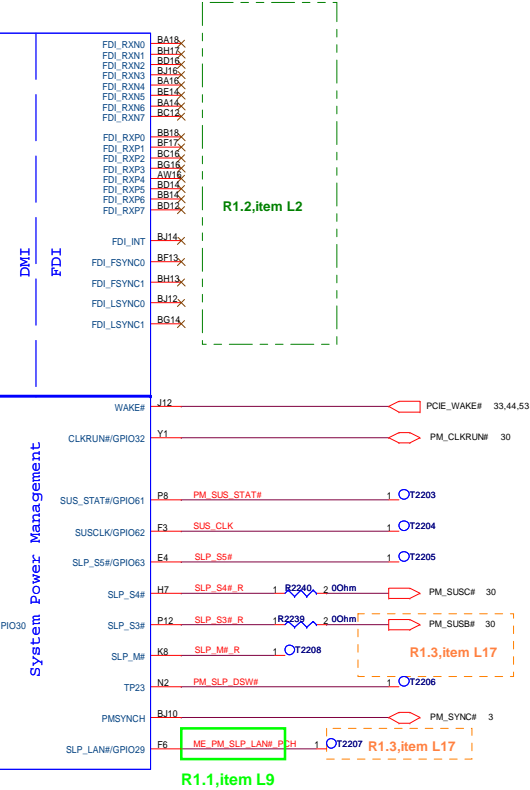


pre-ES1 not support
Reversal Feature

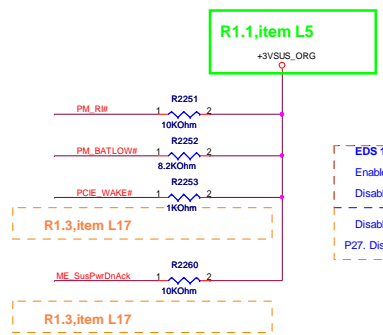


DG R1.1,page 319:
For platforms that do not support Intel LAN, LAN_RST# should be pulled down to ground via a 8.2 kΩ to 10 kΩ pull-down resistor.

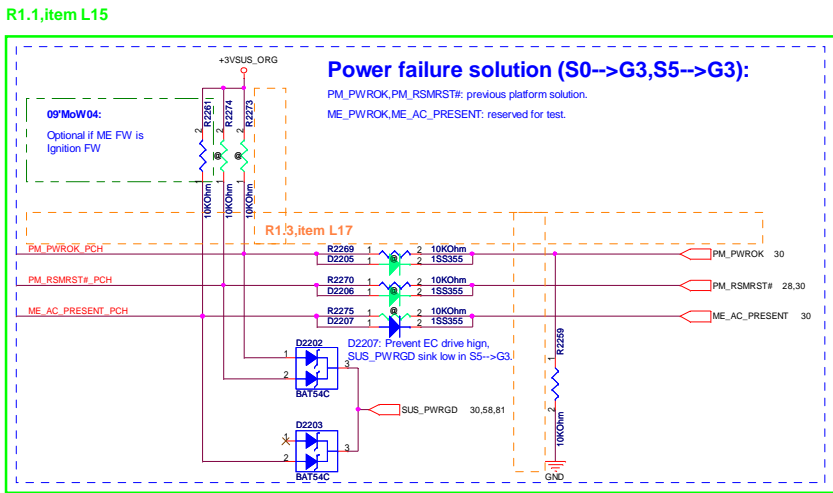
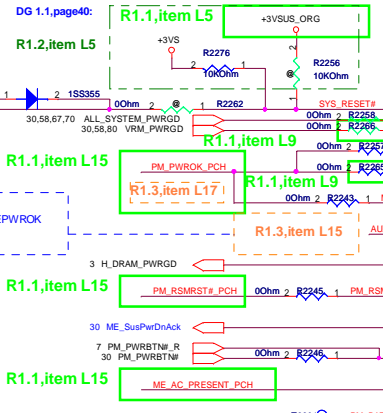
U2001C			
3	DML_RXN0	00hm 2	RX2201 DMI_RXN0_R BC24
3	DML_RXN1	00hm 2	RX2202 DMI_RXN1_R BJ22
3	DML_RXN2	00hm 2	RX2205 DMI_RXN2_R AW20
3	DML_RXN3	00hm 2	RX2204 DMI_RXN3_R BJ20
3	DML_RXP0	00hm 2	RX2207 DMI_RXP0_R BD24
3	DML_RXP1	00hm 2	RX2206 DMI_RXP1_R BG22
3	DML_RXP2	00hm 2	RX2217 DMI_RXP2_R BA20
3	DML_RXP3	00hm 2	RX2208 DMI_RXP3_R BG20
3	DML_TXN0	00hm 2	RX2210 DMI_TXN0_R BE22
3	DML_TXN1	00hm 2	RX2209 DMI_TXN1_R BE21
3	DML_TXN2	00hm 2	RX2212 DMI_TXN2_R BE20
3	DML_TXN3	00hm 2	RX2211 DMI_TXN3_R BE18
3	DML_TXP0	00hm 2	RX2215 DMI_TXP0_R BD22
3	DML_TXP1	00hm 2	RX2213 DMI_TXP1_R BH21
3	DML_TXP2	00hm 2	RX2216 DMI_TXP2_R BC20
3	DML_TXP3	00hm 2	RX2214 DMI_TXP3_R BD18

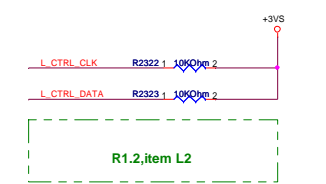


R1.2,item L2



EDS 1.0: Intel LAN
Enabled: LAN_RST# connected to the same source as MEPWROK
Disabled: LAN_RST# must be grounded
Disabled: SLP_LAN#->NC.
P27: Disabled: VCCLAN connected to GND.





LVDS Disable: (For discrete graphic)

1. NC:
 LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
 LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
 LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
 L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
 LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:
 VccLVDS, VccTX_LVDS

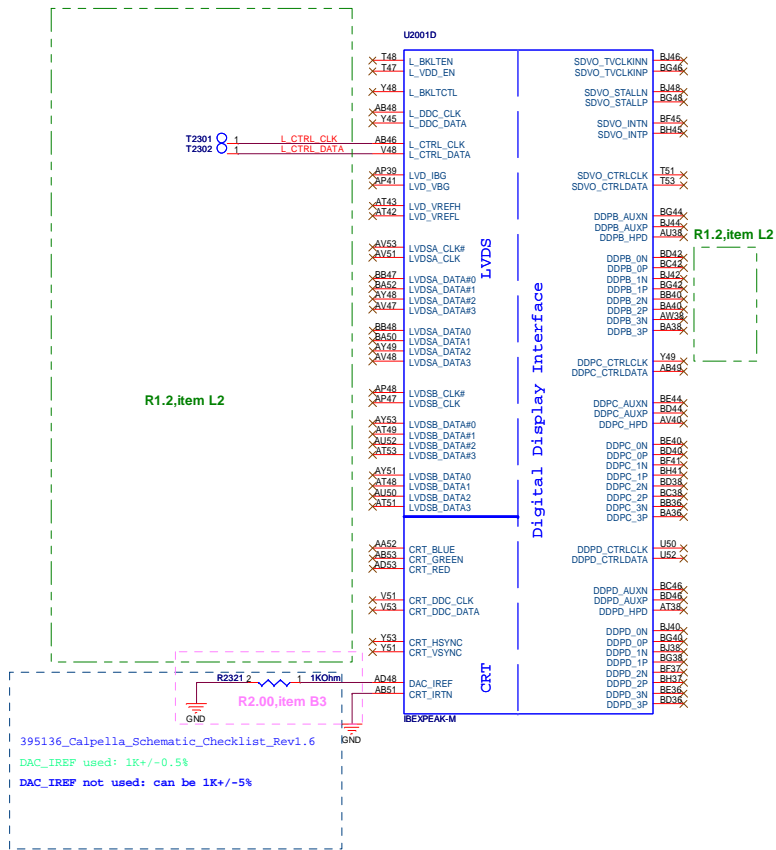
CRT Disable: (For discrete graphic)

1. NC:
 CRT_RED, CRT_GREEN, CRT_BLUE
 CRT_HSYNC, CRT_VSYNC

2. 1-kΩ ±0.5% pull-down to GND:
 DAC_IREF

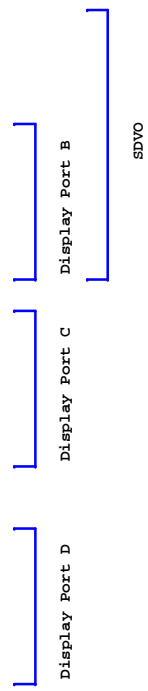
3. Connected to GND:
 CRT_ITRN

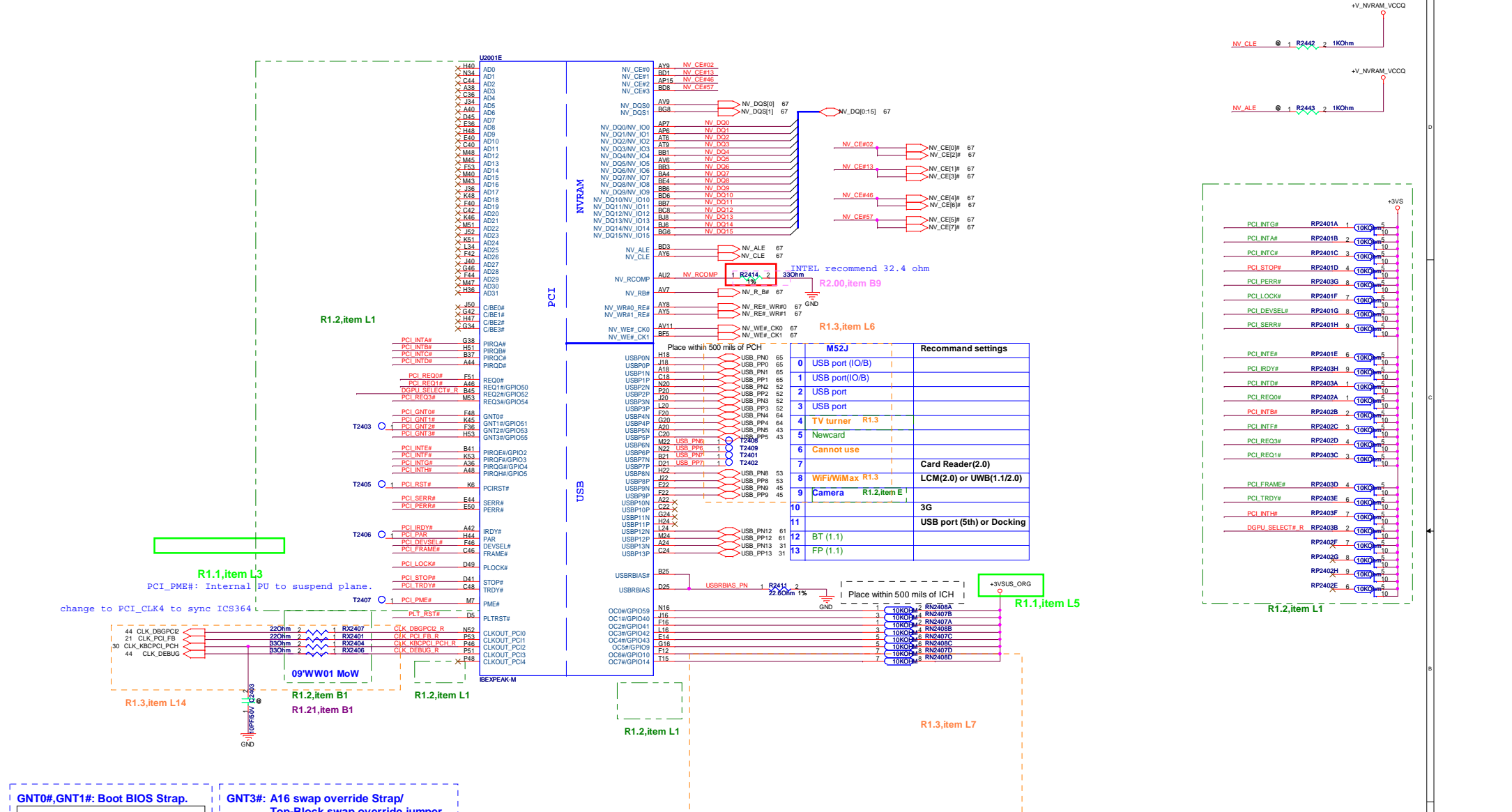
4. Connect to +V3.3:
 VCCADAC



Display Port Disable: (For discrete graphic)

1. NC:
 ALL





GNT0#, GNT1#: Boot BIOS Strap.

Boot BIOS Strap

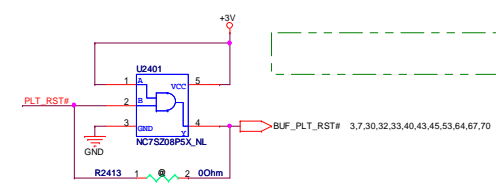
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI (PCH)

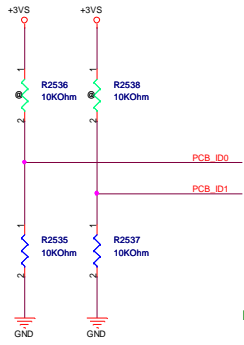
Sampled on rising edge of PWROK.

GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/
Top-Block swap override

High=Default

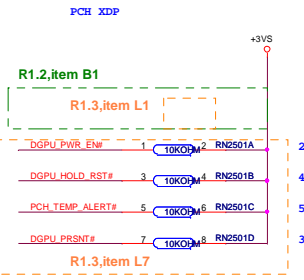
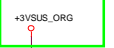




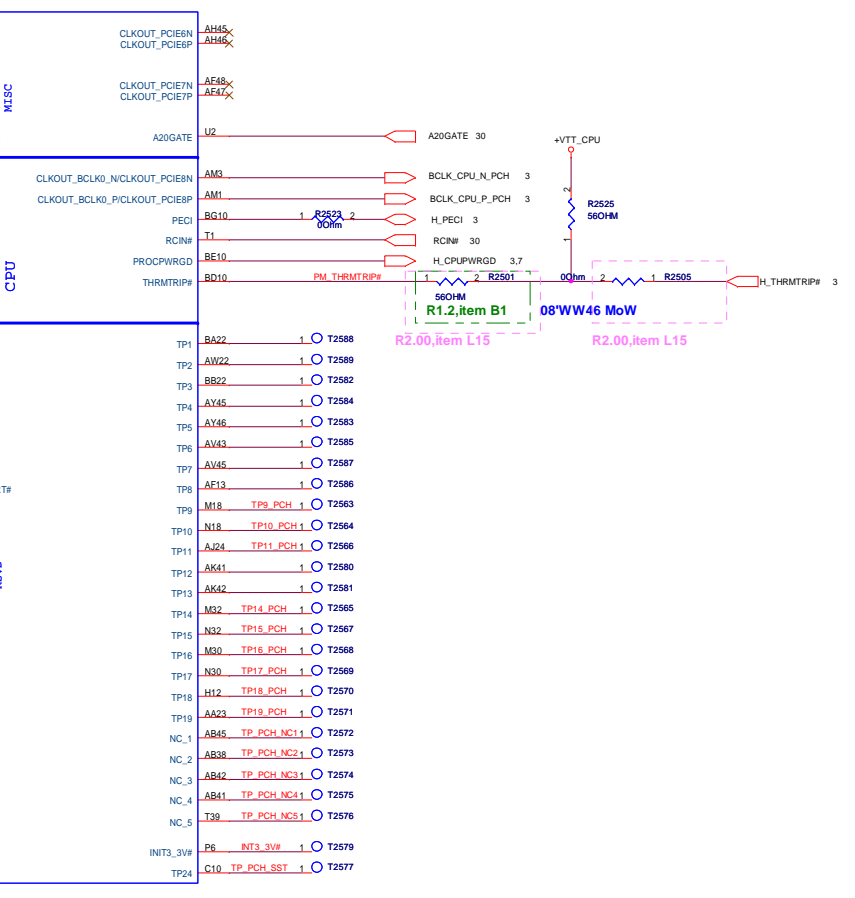
R1.2,item B1

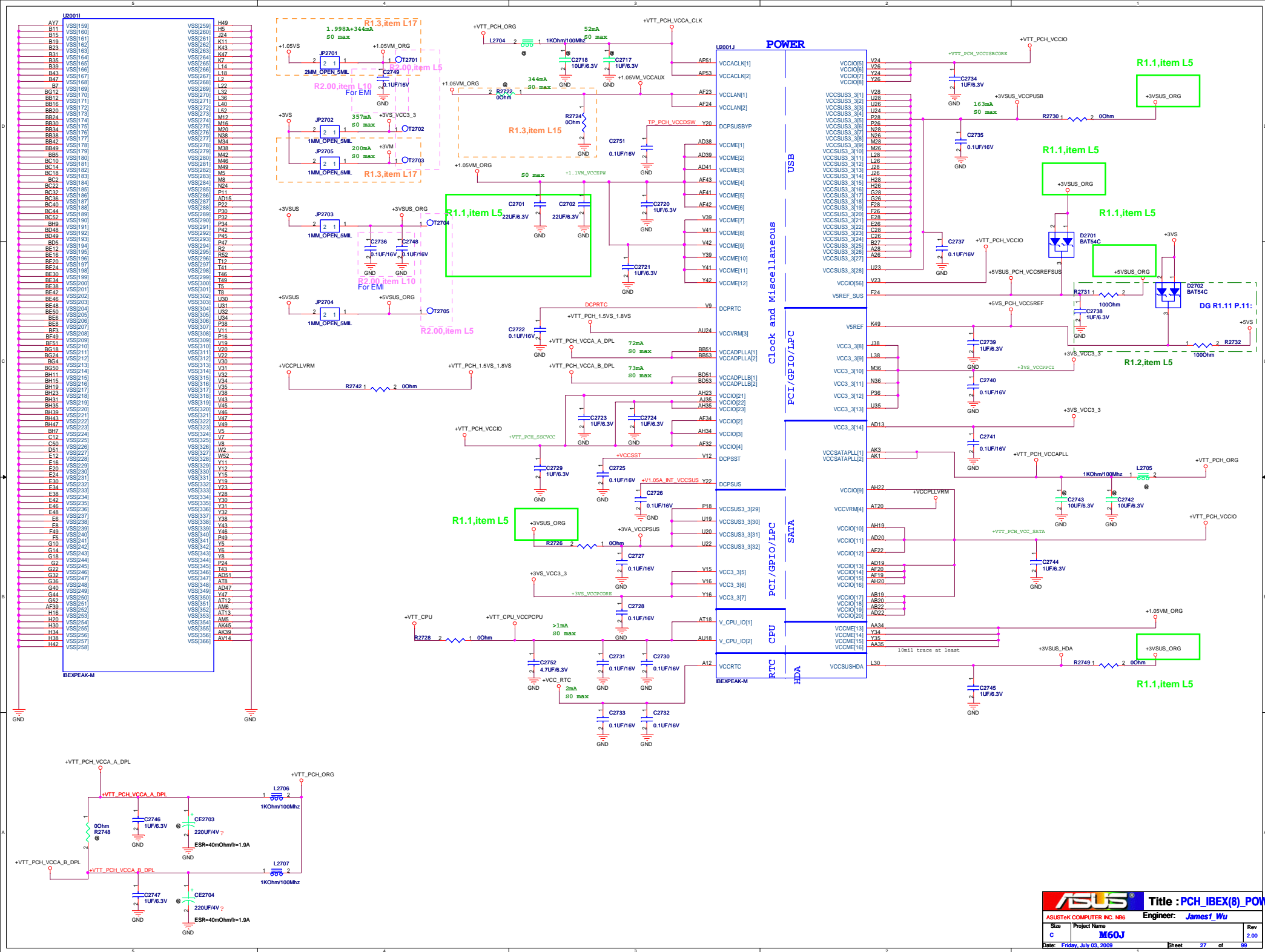


R1.1,item L5



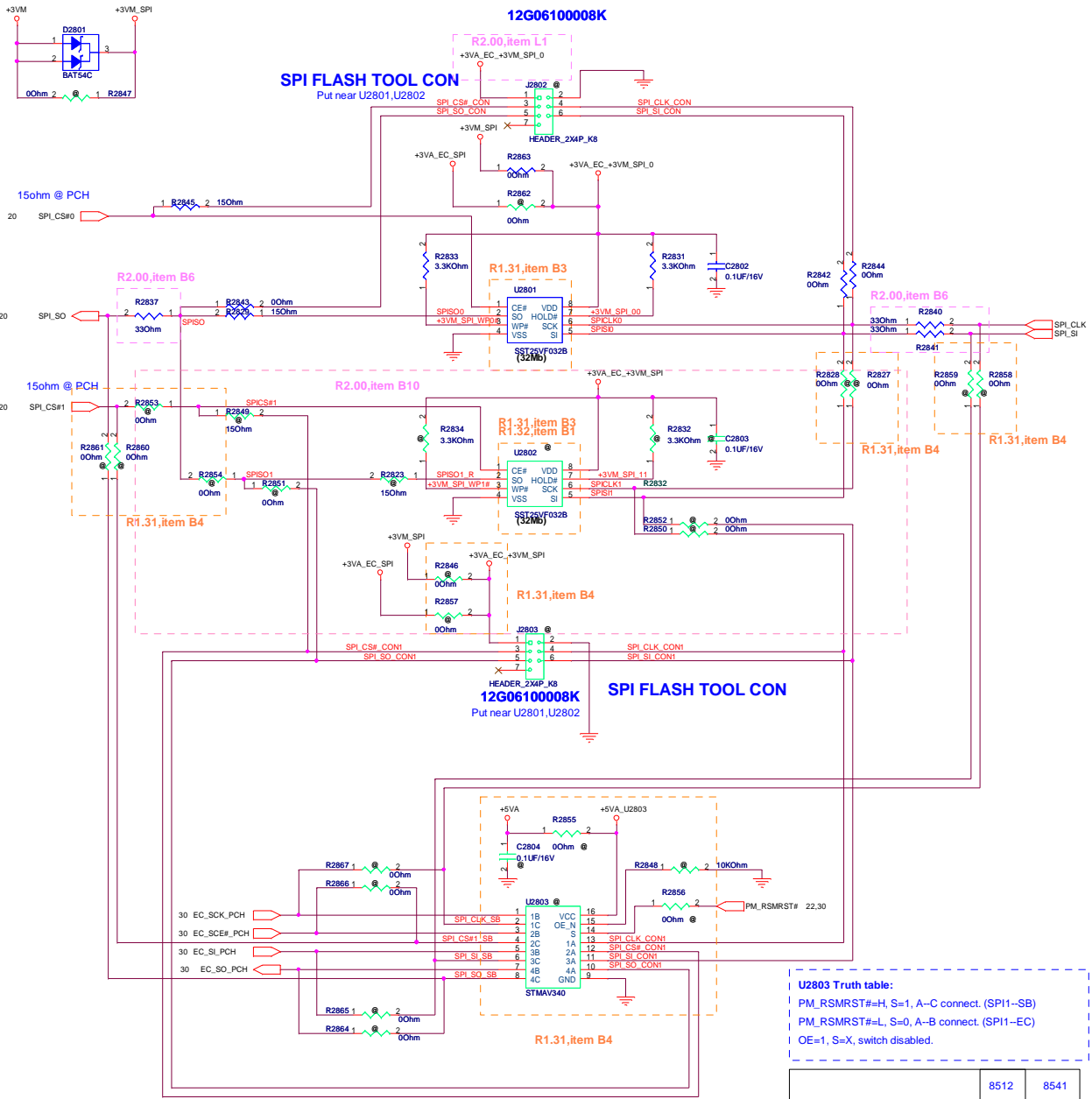
T2596	1	PCH_GPIO0_R	Y3	BMBUS#/GPIO0	
T2590	1	DOCKING_DET#	C38	TACH1/GPIO1	
T2591	1	DOCKING_UNLOCK_BUTTON#	D37	TACH2/GPIO6	
T2592	1	IDE_BAY_IN#	J32	TACH3/GPIO7	
30	EXT_SM#		F10	GPIO8	
R1.3,item L2	T2593	1	PM_LANPHY_EN	K9	LAN_PHY_PWR_CTLR/GPIO12
56	BT_LED	DGPU_HOLD_RST#	A22	GPIO15	
R1.3,item L7	DGPU_PWROK	F38	TACH9/GPIO17	SATA4G/GPIO16	
56	WLAN_LED	OC_LAN_RST#	Y7	TACH0/GPIO17	
T2594	1	OC_LAN_RST#	H10	SCLOCK/GPIO22	
T2595	1	VRM_EN	AB12	GPIO24	
53	WLAN_ON#		V13	GPIO27	
R1.3,item L7	T2548	1	STP_PCW#	M11	GPIO28
R1.3,item L4	STP_PCW#				
T2578	1	SATA_CLK_REQ#	IV6	STP_PCW#/GPIO34	
R1.3,item L7	DGPU_PWROK	AB7	GPIO35	SATA2G/GPIO36	
R1.3,item L7	DGPU_PRSNT#	AB13	SATA3G/GPIO37	SATA3G/GPIO37	
PCB_ID0	V3	SLOAD/GPIO38			
PCB_ID1	P3	SDATAOUT0/GPIO39			
T2597	1	CLK_REQ6#	H3	PCIELCKRQ6#/GPIO45	
T2598	1	CLK_REQ7#	F1	PCIELCKRQ7#/GPIO46	
T2599	1	EMAIL_LED	AB6	SDATAOUT1/GPIO48	
R1.2,item L5	PCH_TEMP_ALERT#	AA4	SATA5G/GPIO49/TEMP_ALERT#		
R1.3,item L7	BT_ON	F8	GPIO57		
T2531	1	TP_VSS_NCTF1	A4	VSS_NCTF_1	
T2532	1	TP_VSS_NCTF2	A49	VSS_NCTF_2	
T2533	1	TP_VSS_NCTF3	A5	VSS_NCTF_3	
T2534	1	TP_VSS_NCTF4	A50	VSS_NCTF_4	
T2535	1	TP_VSS_NCTF5	A52	VSS_NCTF_5	
T2536	1	TP_VSS_NCTF6	A53	VSS_NCTF_6	
T2537	1	TP_VSS_NCTF7	B2	VSS_NCTF_7	
T2538	1	TP_VSS_NCTF8	B4	VSS_NCTF_8	
T2539	1	TP_VSS_NCTF9	B63	VSS_NCTF_9	
T2540	1	TP_VSS_NCTF10	B62	VSS_NCTF_10	
T2541	1	TP_VSS_NCTF11	BE1	VSS_NCTF_11	
T2542	1	TP_VSS_NCTF12	BE3	VSS_NCTF_12	
T2543	1	TP_VSS_NCTF13	BF1	VSS_NCTF_13	
T2544	1	TP_VSS_NCTF14	BF3	VSS_NCTF_14	
T2545	1	TP_VSS_NCTF15	BH1	VSS_NCTF_15	
T2546	1	TP_VSS_NCTF16	BH2	VSS_NCTF_16	
T2547	1	TP_VSS_NCTF17	BH52	VSS_NCTF_17	
T2548	1	TP_VSS_NCTF18	BH53	VSS_NCTF_18	
T2549	1	TP_VSS_NCTF19	BJ1	VSS_NCTF_19	
T2550	1	TP_VSS_NCTF20	BJ2	VSS_NCTF_20	
T2551	1	TP_VSS_NCTF21	BJ4	VSS_NCTF_21	
T2552	1	TP_VSS_NCTF22	BJ9	VSS_NCTF_22	
T2553	1	TP_VSS_NCTF23	BJ5	VSS_NCTF_23	
T2554	1	TP_VSS_NCTF24	BJ60	VSS_NCTF_24	
T2555	1	TP_VSS_NCTF25	BJ62	VSS_NCTF_25	
T2556	1	TP_VSS_NCTF26	BJ63	VSS_NCTF_26	
T2557	1	TP_VSS_NCTF27	BJ1	VSS_NCTF_27	
T2558	1	TP_VSS_NCTF28	D2	VSS_NCTF_28	
T2559	1	TP_VSS_NCTF29	DE3	VSS_NCTF_29	
T2560	1	TP_VSS_NCTF30	ET	VSS_NCTF_30	
T2561	1	TP_VSS_NCTF31	E53	VSS_NCTF_31	





PCH SPI ROM

12G06100008K

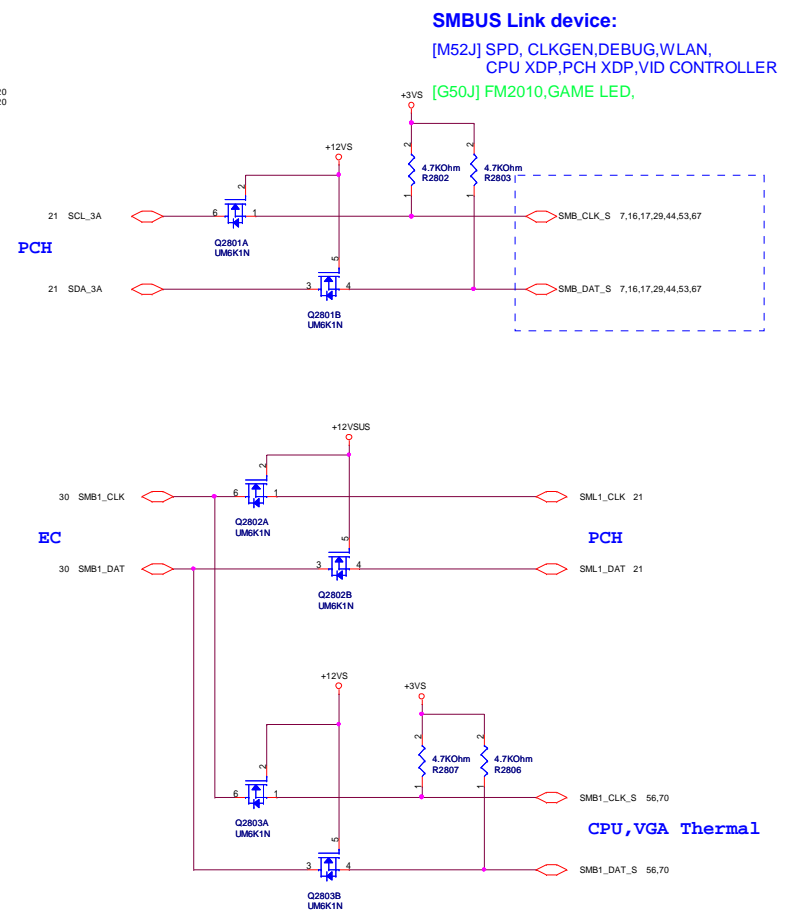


SPI FLASH TOOL CON
Put near U2801,U2802

SPI FLASH TOOL CON
Put near U2801,U2802

U2803 Truth table:
PM_RSMRST#=#, S=1, A-C connect. (SPI1-SB)
PM_RSMRST#=#, S=0, A-B connect. (SPI1-EC)
OE=1, S=X, switch disabled.

	8512	8541
R3002, R2858, R3003, R2859, R3004, R2860, R3005, R2861, R2853, U3003, R2440	R2855, R2849, R2854, R3053, R2441	R2857, R2850, U2803, R2852, R2846
R2827, R3043, R2828, C3019, R2846	R2848, R2851, R2852, C2804	Mount
R3002, R2858, R2849, R3003, R2859, R2850, R3053, R2441, R3004, R2860, R2851, R3043, R3005, R2861, R2852, C3019	R2855, R2857	DNI
		Mount



SMBUS Link device:
[M52J] SPD, CLKGEN, DEBU, WLAN, CPU XDP, PCH XDP, VID CONTROLLER
[G50J] FM2010, GAME LED,

PCH

EC

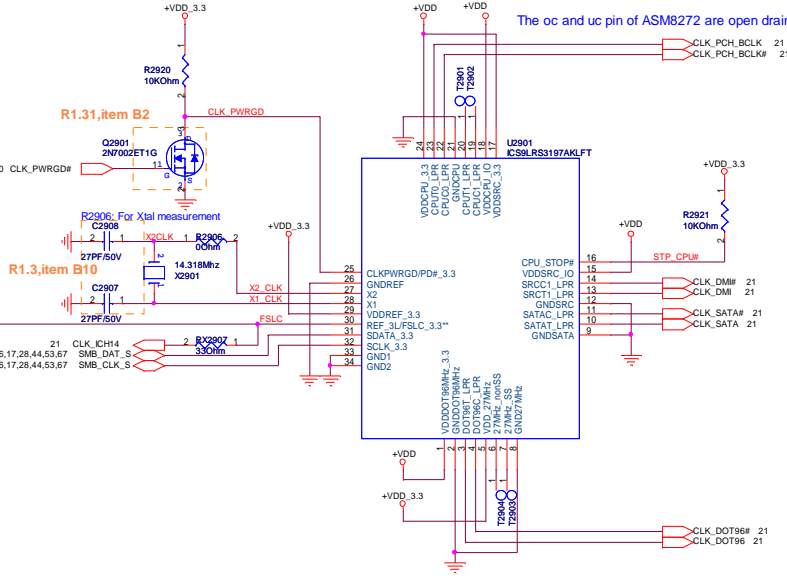
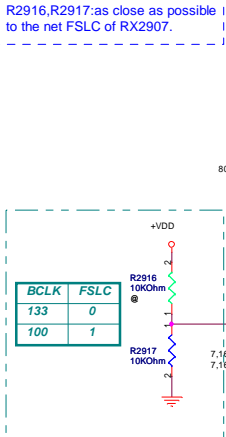
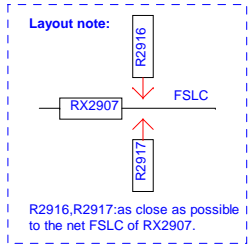
PCH

CPU, VGA Thermal

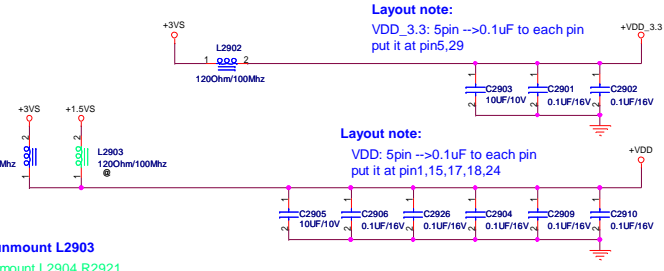
SUBSYSTEM ID : SB_

ASUS Title : PCH_SPI ROM,OTH
ASUSTeK COMPUTER INC. NBS Engineer: James1_Wu
Size: Project Name: M60J Rev: 2.00
Date: Friday, July 10, 2009 Sheet: 28 of 99

R1.3,item L1

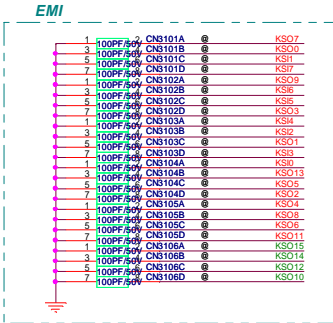
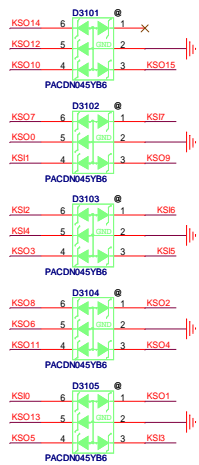


The oc and uc pin of ASM8272 are open drain in next version.

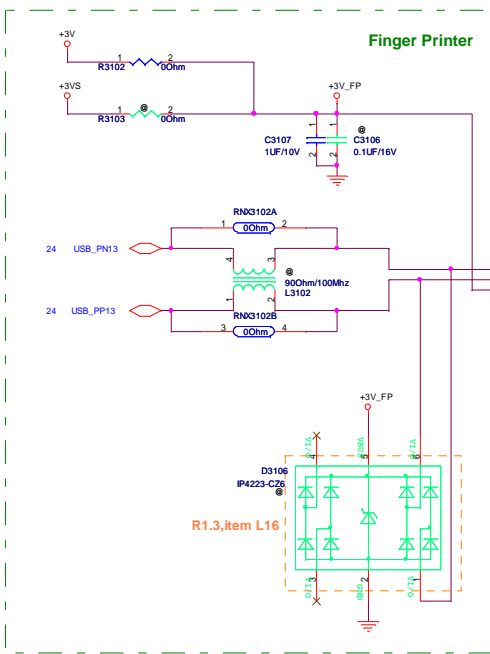
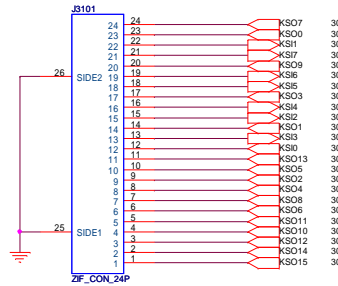


9LRS3197 / 9LVS3162 Colay
 9LRS3197----mount L2904,unmount L2903
 9LVS3162----mount L2903,unmount L2904,R2921

R2.00,item L14

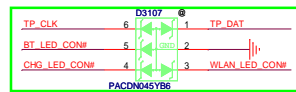


Keyboard

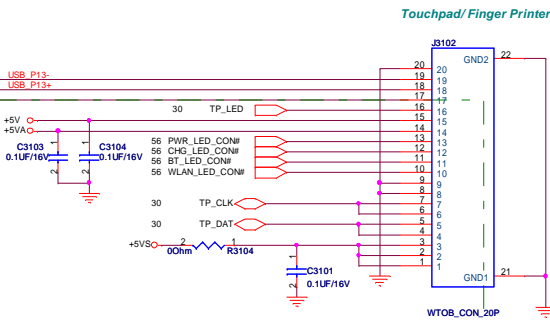


Finger Printer

R1.1,item L14



Touchpad/ Finger Printer / TP_LED

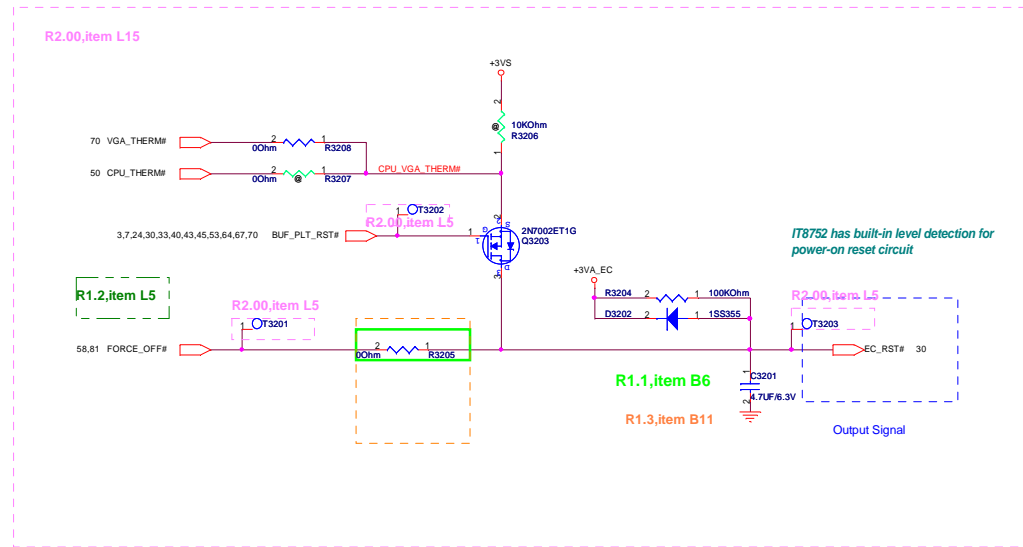


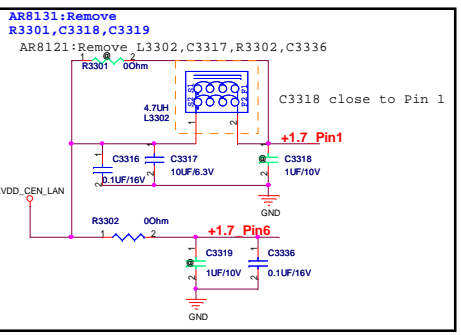
TouchPAD/TP_LED



R1.3,item L17

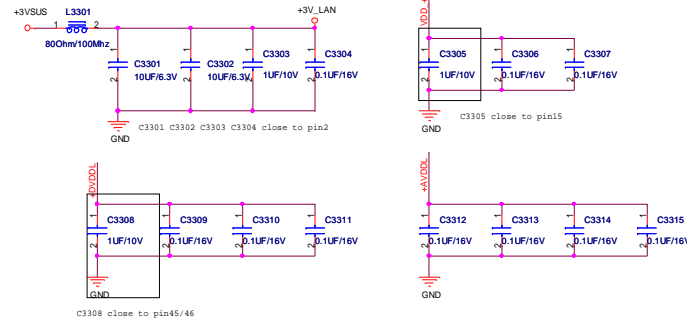
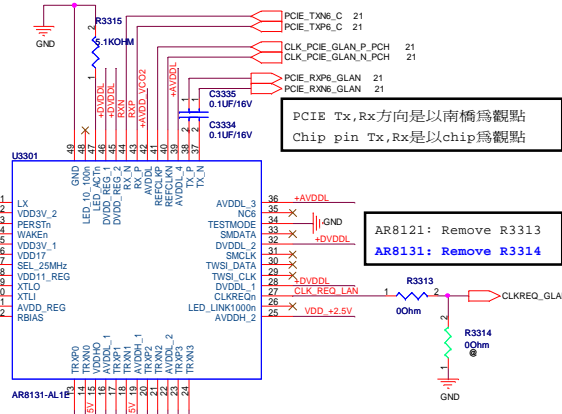
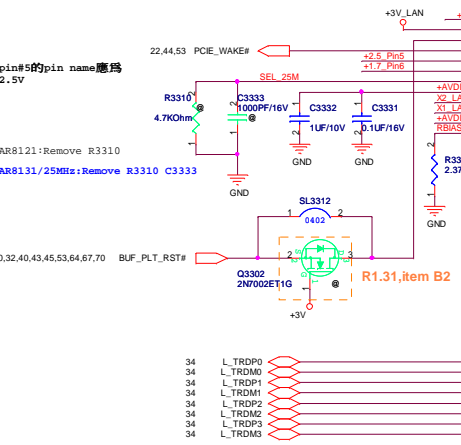
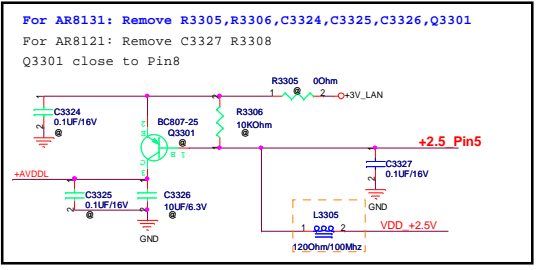
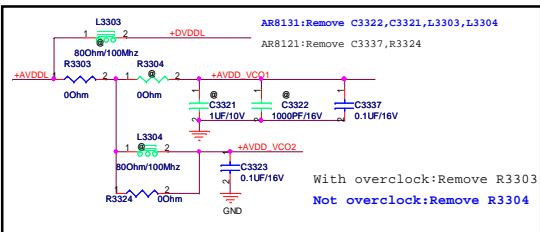
Thermal Policy





AR8131 with overclock: Remove R3315
AR8121: Remove R3315

ground pad要打散熱孔

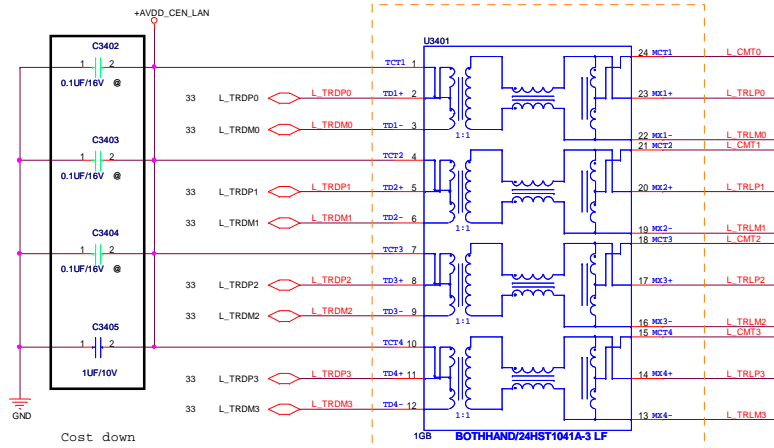


For AR8131: Remove R3309
+1.7 Pin6

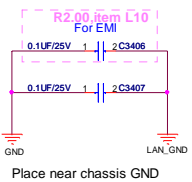
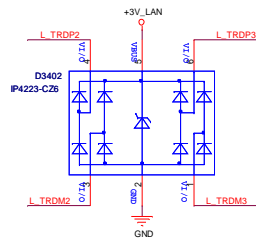
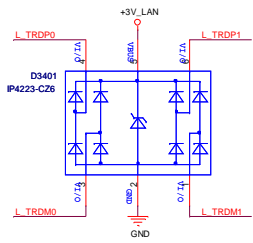
AR8121: Remove C3328
AR8131/25MHz: Remove C3328

R1.3, item L2

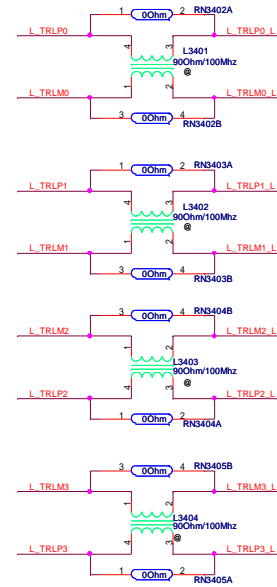
R1.3,item L2



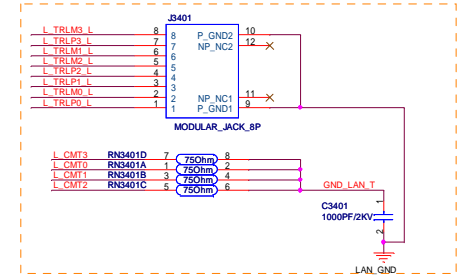
Cost down



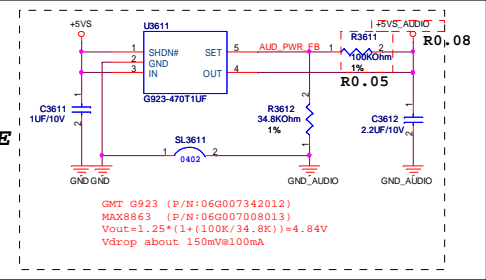
Place near chassis GND



connector without modem

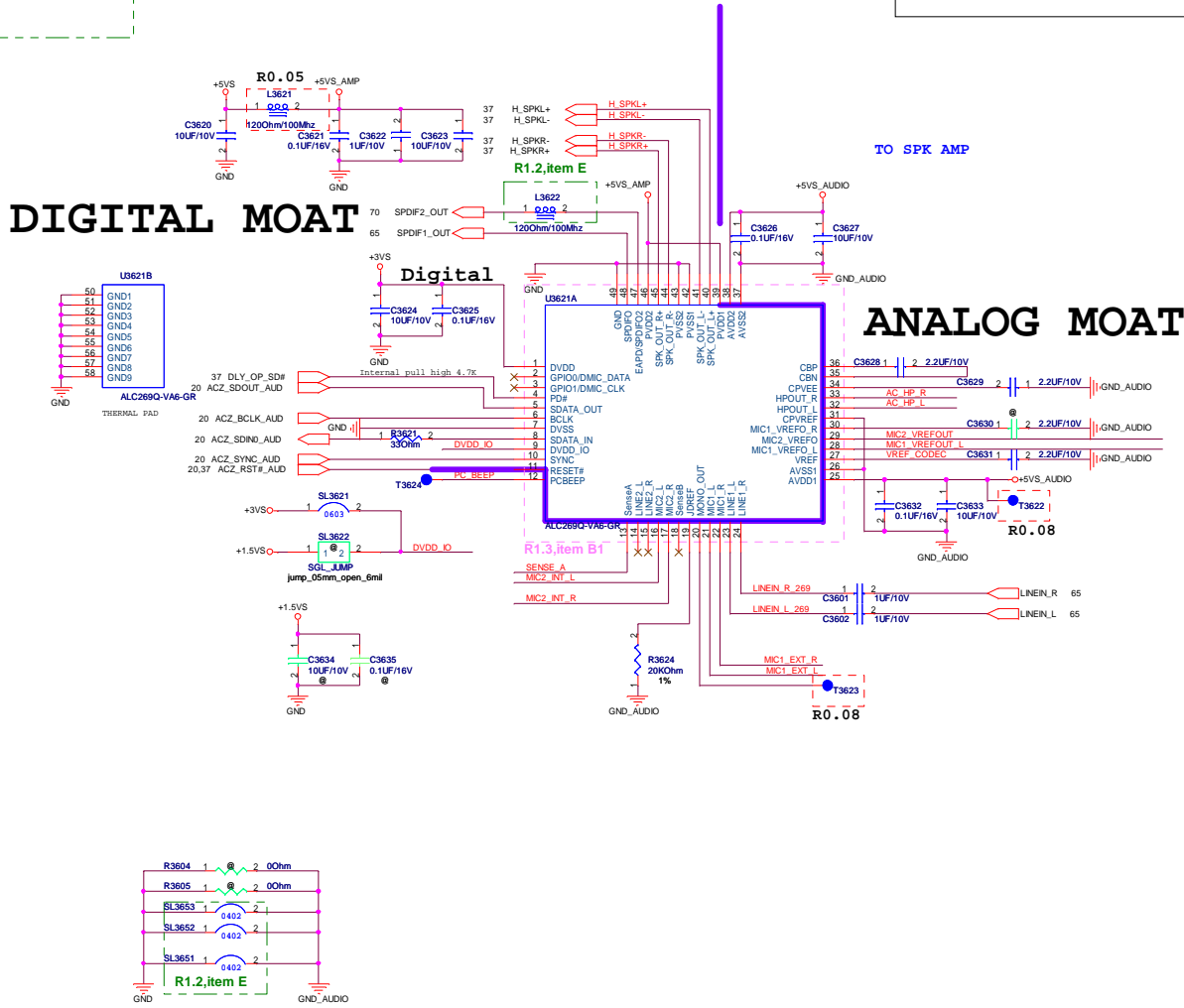


AUDIO POWER

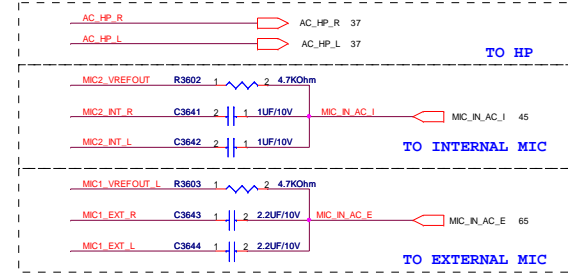


DIGITAL MOAT

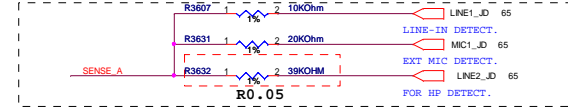
ANALOG MOAT



FOR NORMAL FUNCTION .



DETECTION



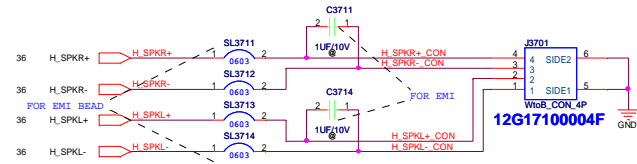
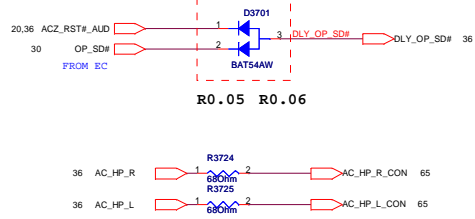
PC BEEP

Remove PC_BEEP Circuit
 Please remove the PC Beep function from VerB table.

For EMI


R1.2,item L3

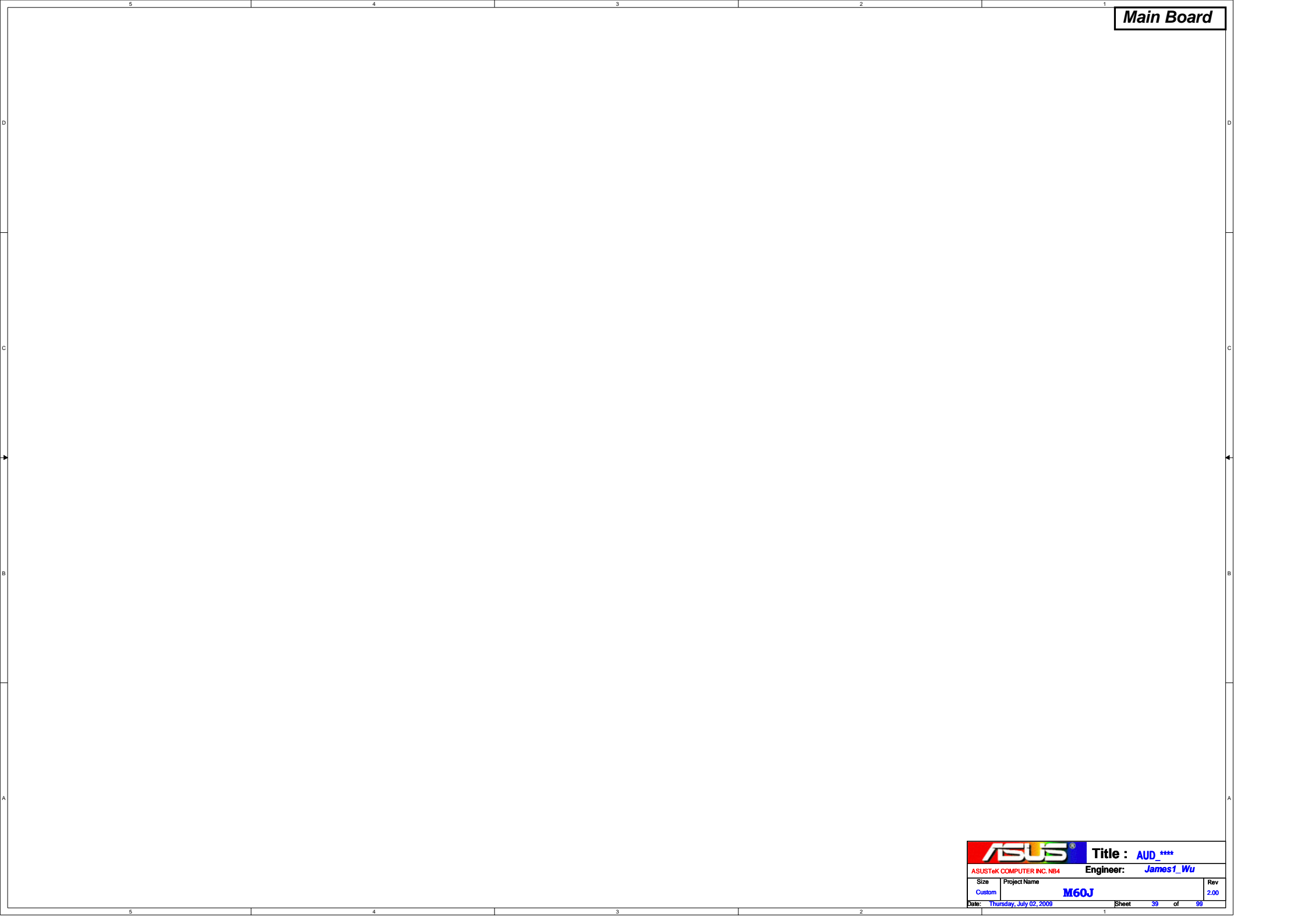
MUTE CONTROL




R1.2,item L3

<Variant Name>

		Title : AUD ****	
ASUSTeK COMPUTER INC. NB2		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
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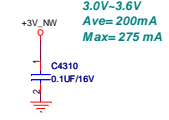
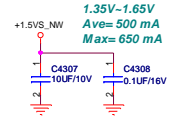
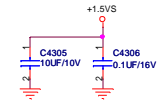
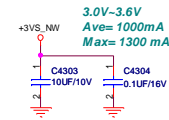
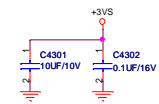
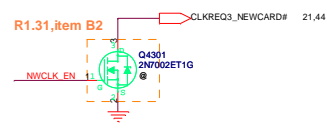
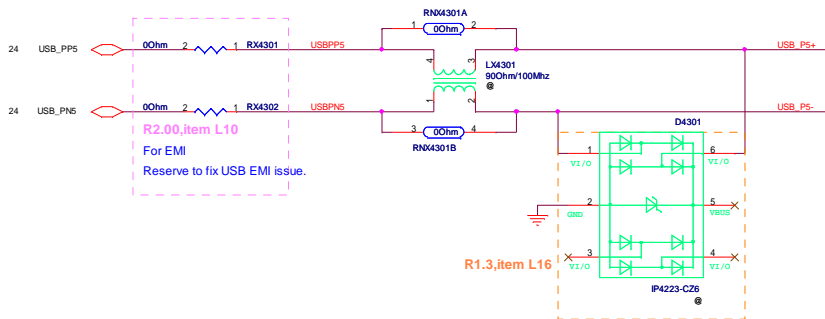
		Title : AUD ****	
ASUSTek COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
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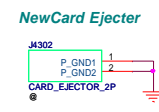
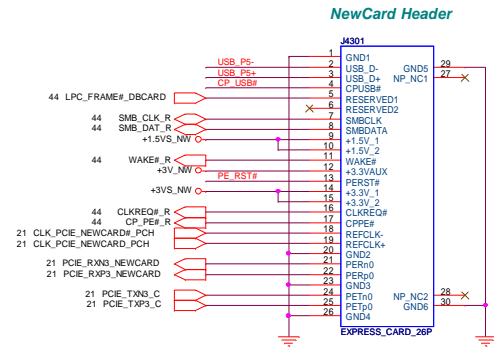
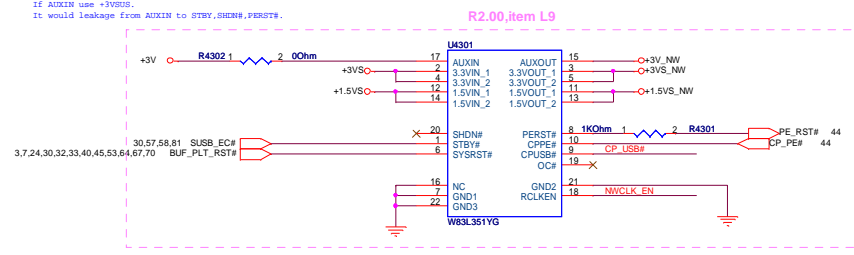
R1.2.item L1



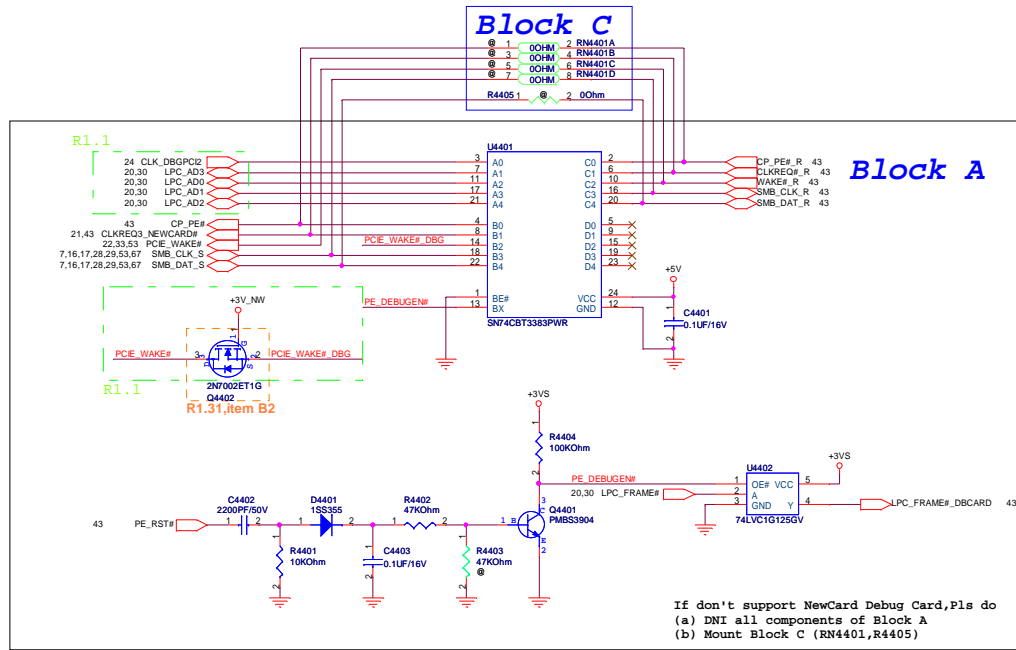
R1.2,item L1



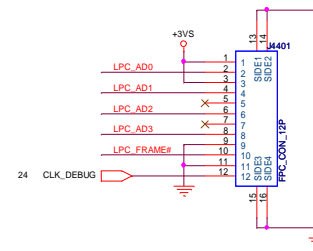
If AUXIN use +3VSUS,
It would leakage from AUXIN to STBY,SHDN#,PERST#.

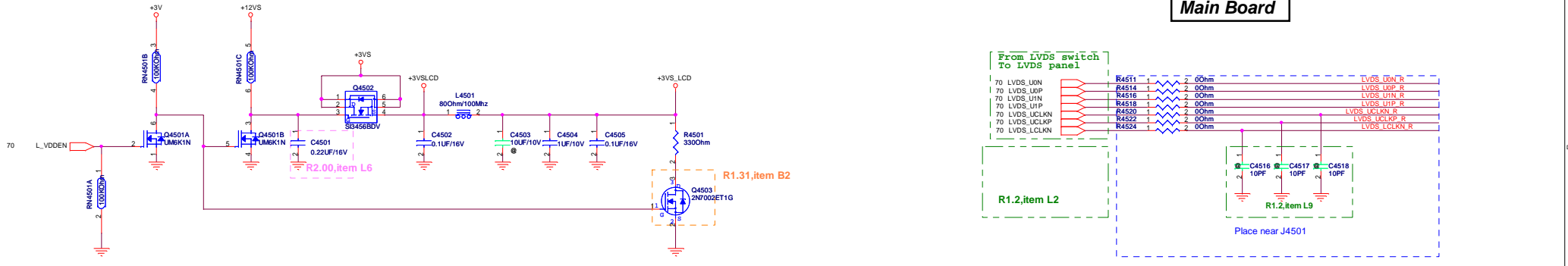


For NewCard Debug Card

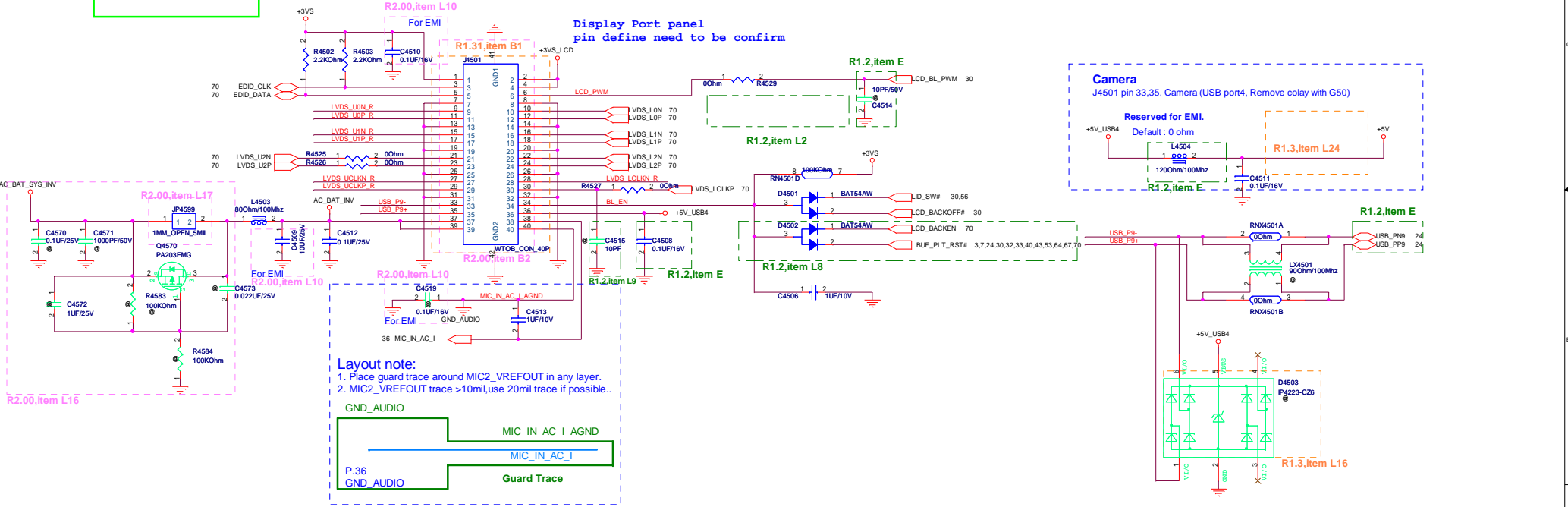


LPC Debug Port



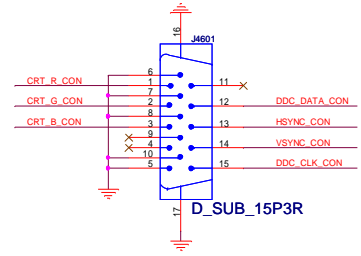
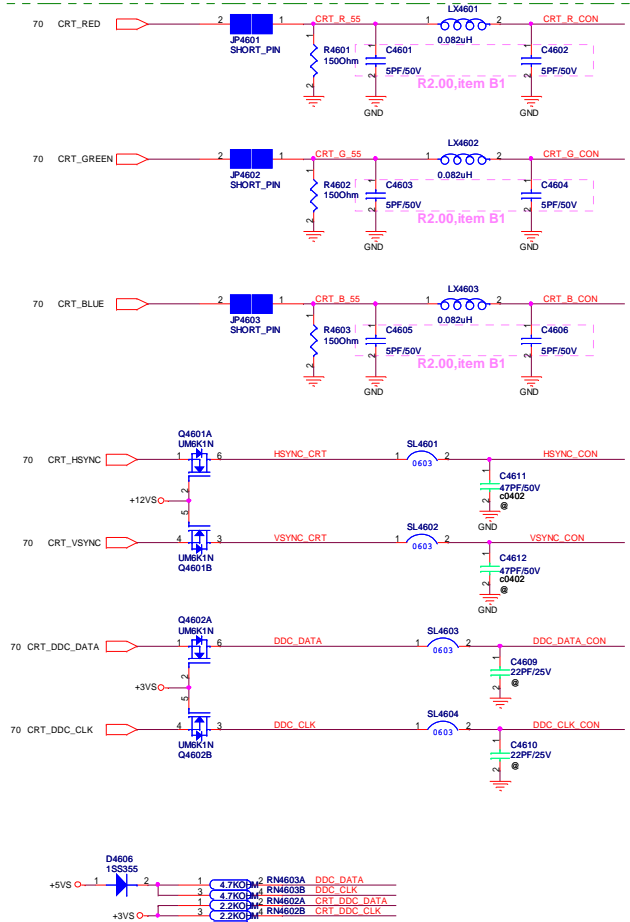


R1.1, item L3
Pin6,30-40 re-define.

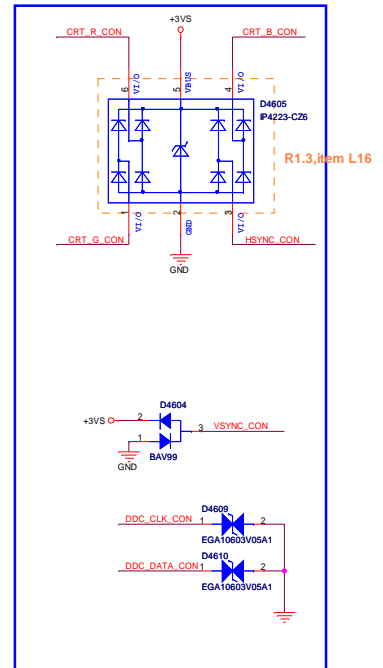


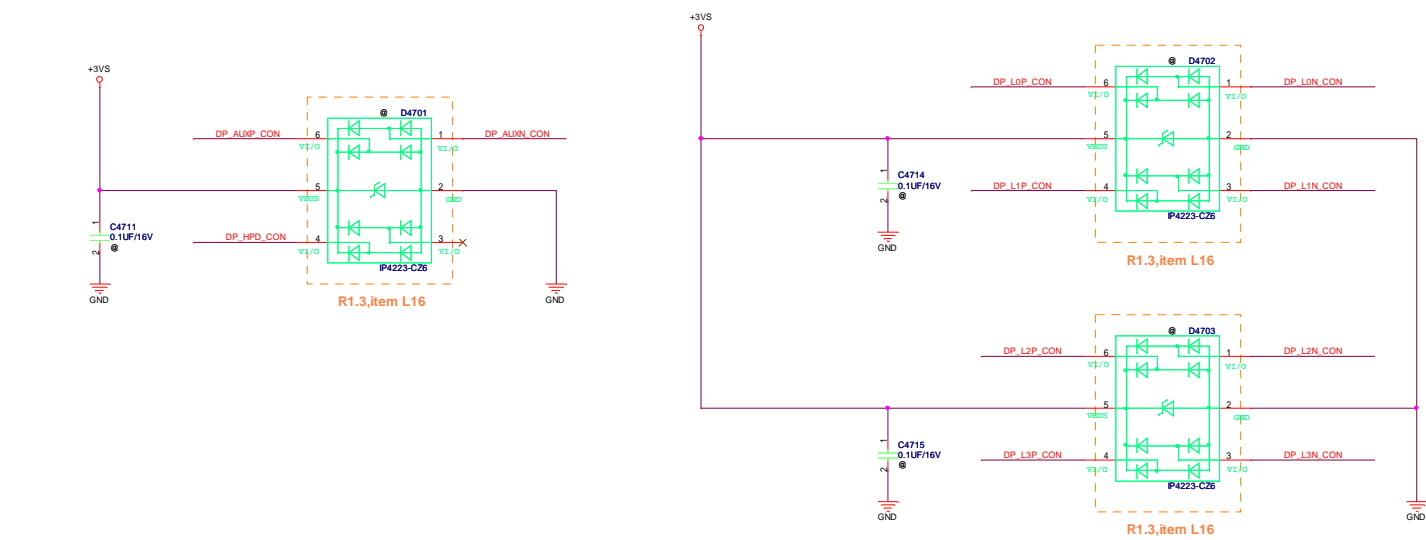
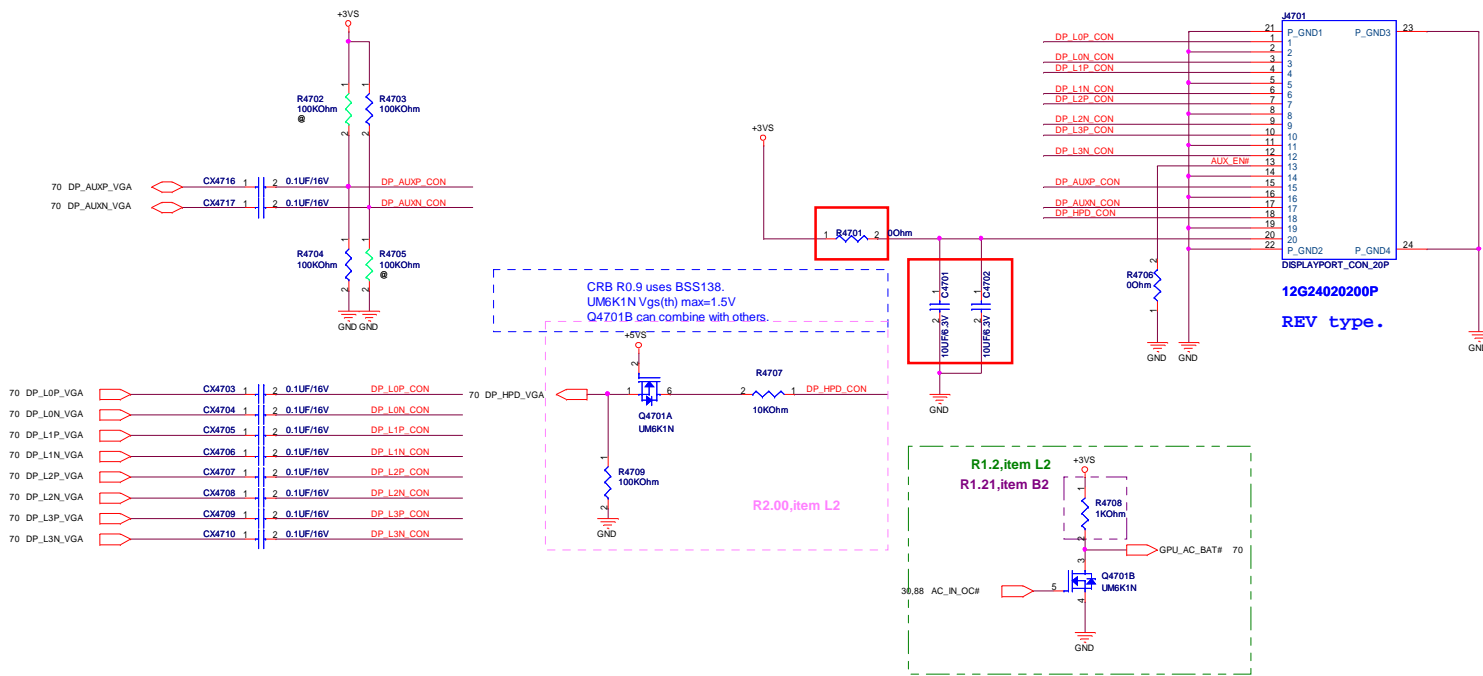
Layout note:
1. Place guard trace around MIC2_VREFOUT in any layer.
2. MIC2_VREFOUT trace >10mil, use 20mil trace if possible..

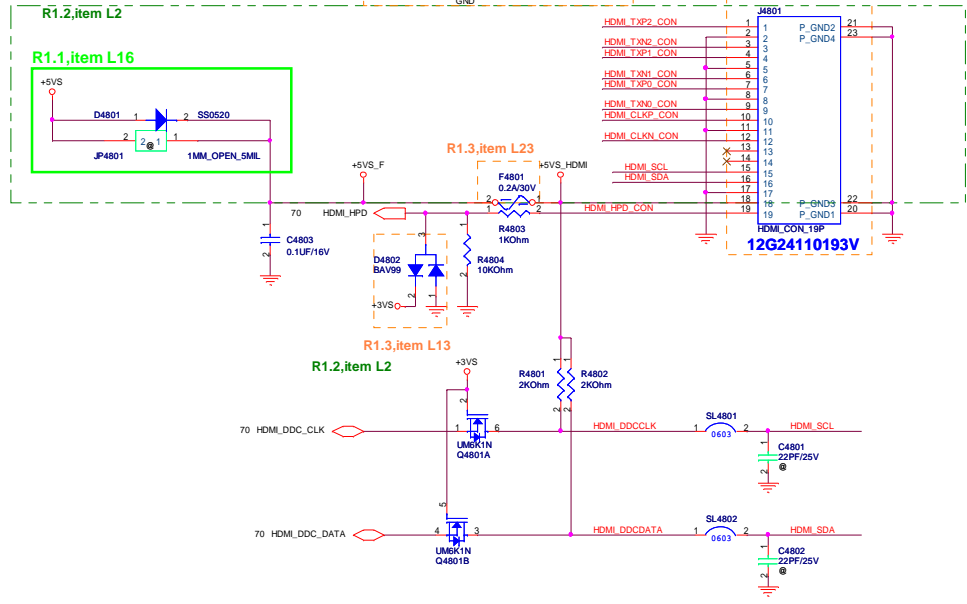
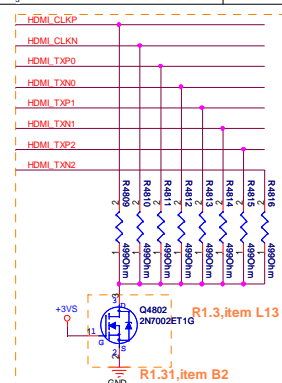
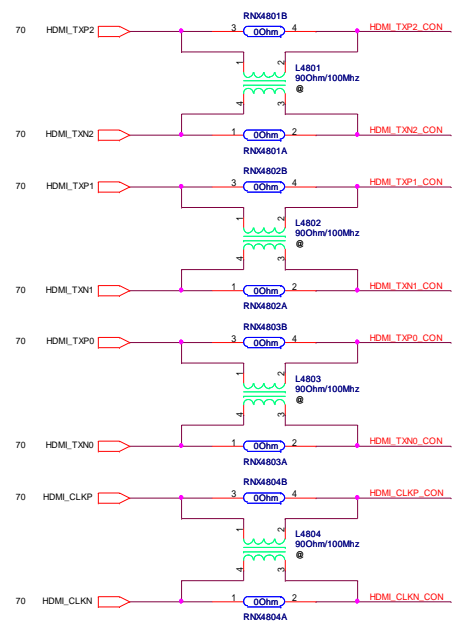
R1.2,item L2




PLACE ESD Diodes near connector



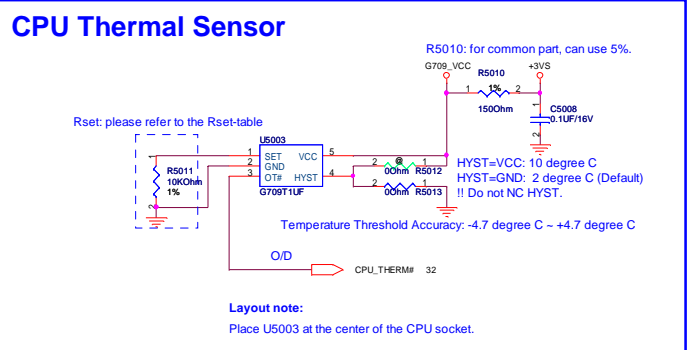




Main Board

		Title : TV ****	
ASUSTeK COMPUTER INC. NB4		Engineer: James1_Wu	
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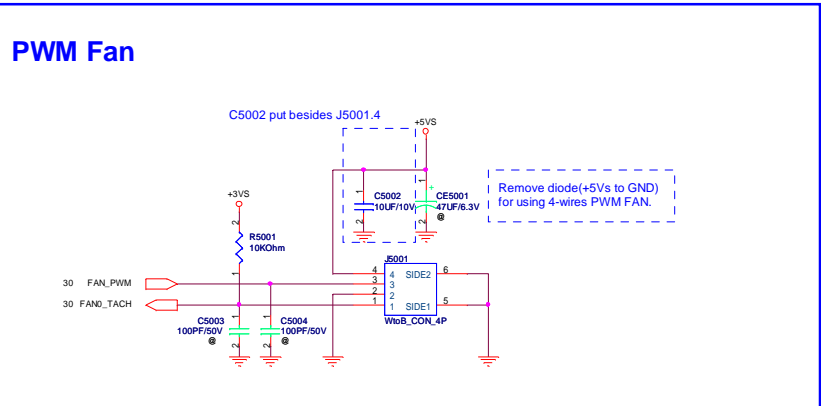
R2.00,item L15



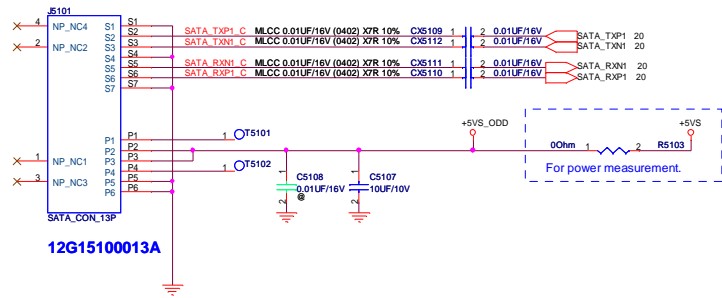
$$Rset(Kohm)=0.0012T^2-0.9308T+96.147$$

Rset table:

T=	degree C , Rset=	Kohm
100		15.07
101		14.38
102		13.69
103		13.01
104		12.32
105		11.64
106		10.97
107		10.29
107.43		10.00 default
109		8.95
110		8.28
111		7.61
112		6.95
113		6.29
114		5.63
115		4.98

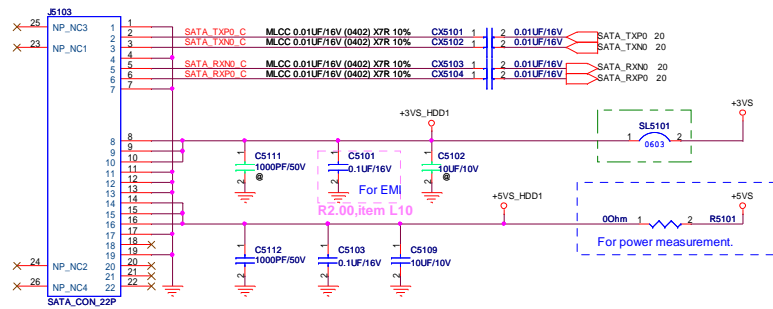


ODD



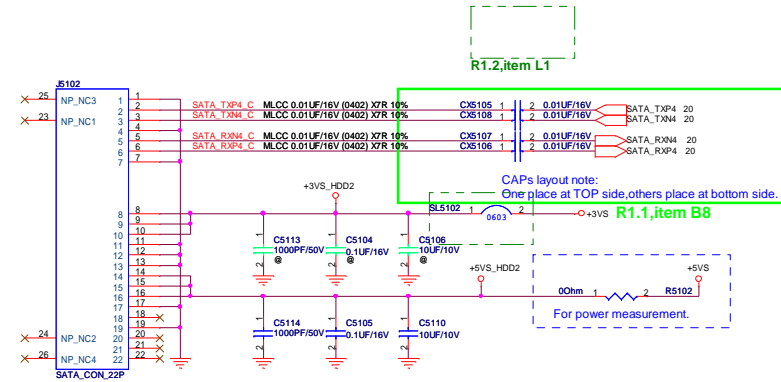
12G15100013A

HDD (1st)



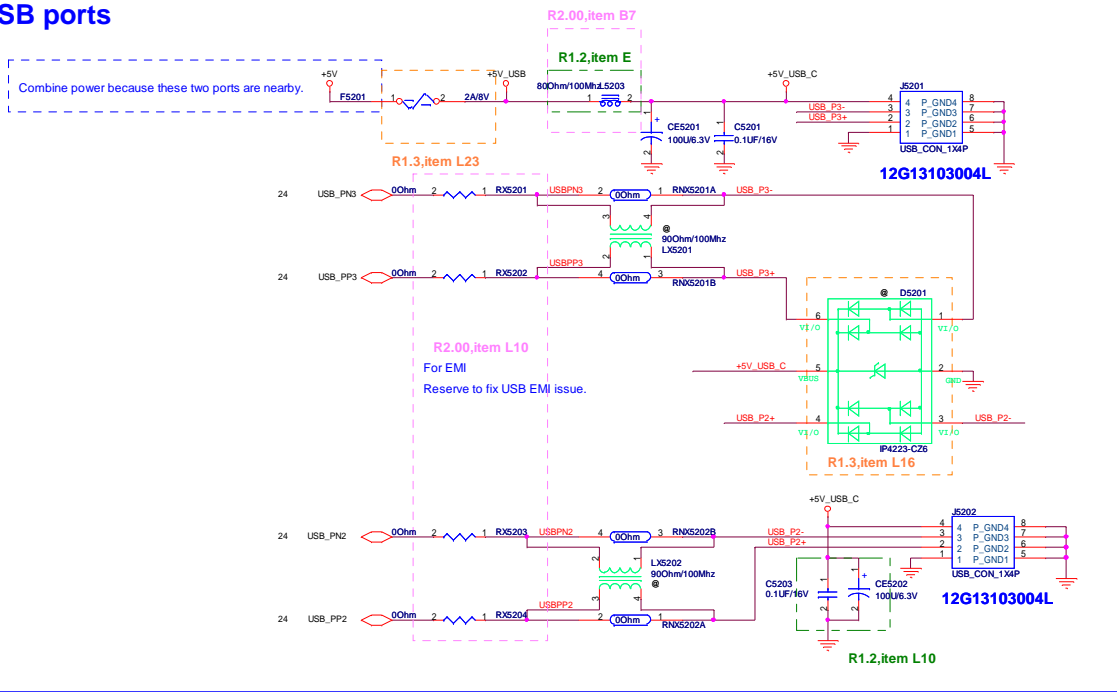
12G15101022M

HDD (2nd)

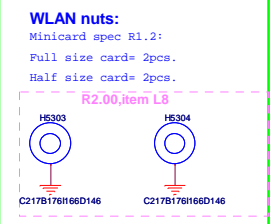
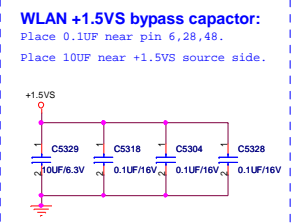
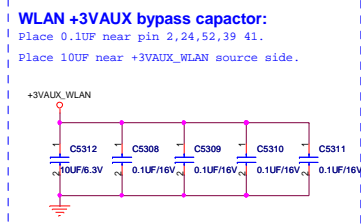
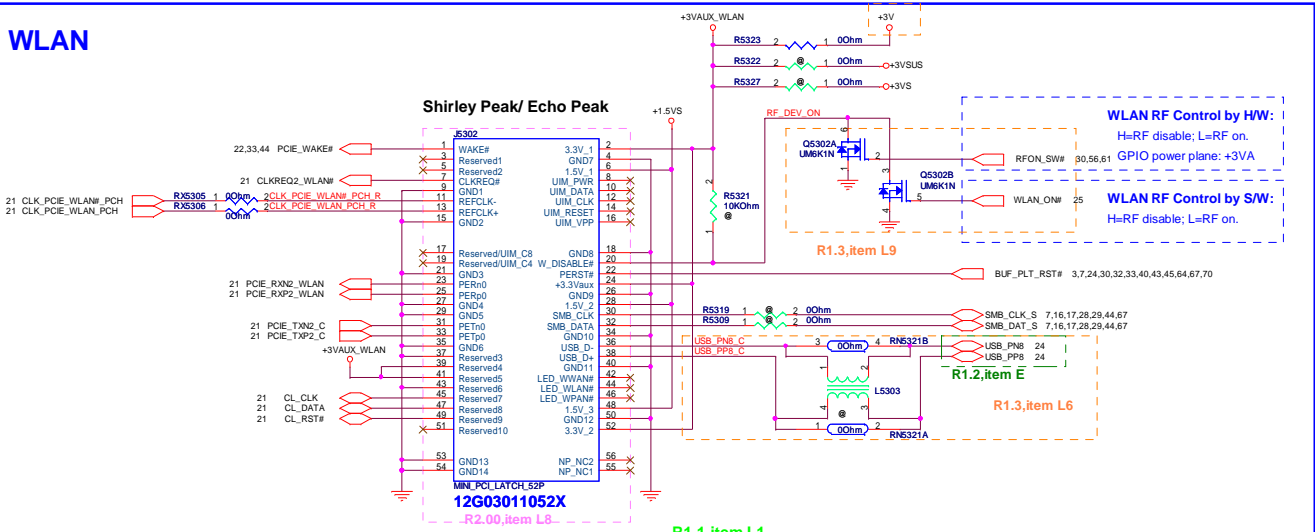


12G15111022J


USB ports



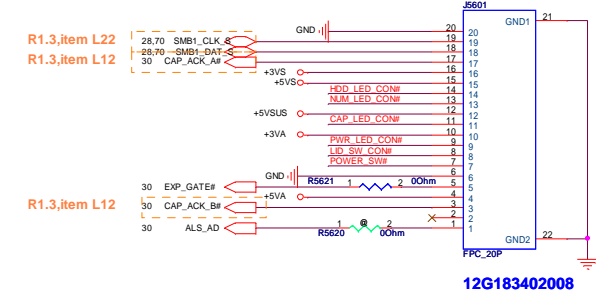
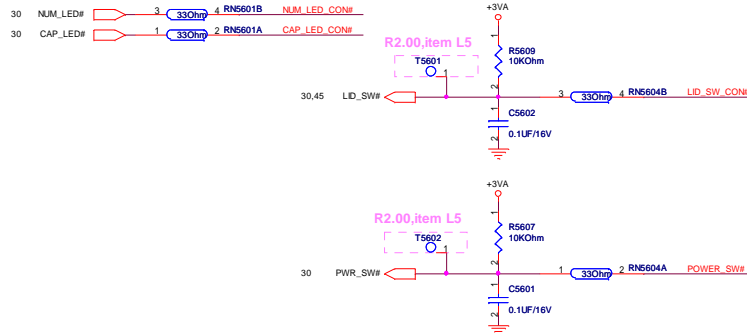
WLAN



Main Board

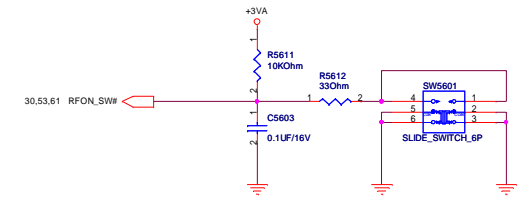
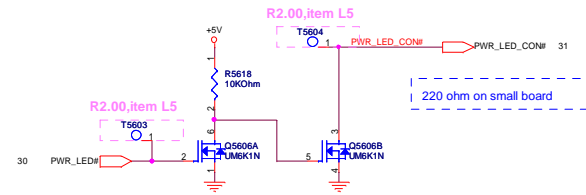
		Title : SIO ****	
ASUSTeK COMPUTER INC. NBD		Engineer: Jamesf_Wu	
Size	Project Name		Rev
C	M60J		2.00
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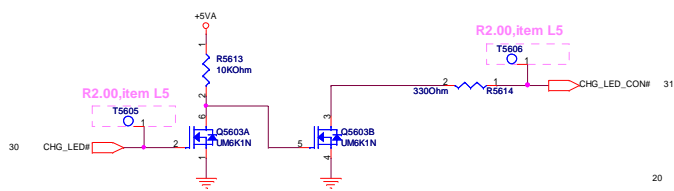


12G183402008

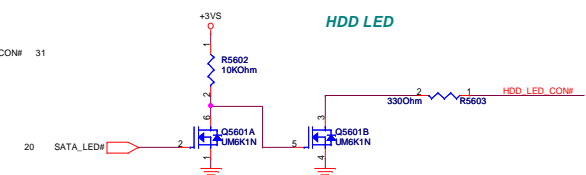
Power LED



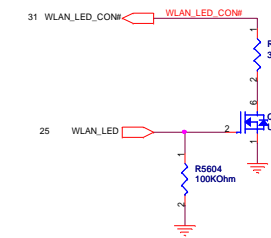
Charger LED



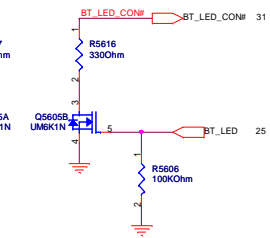
HDD LED

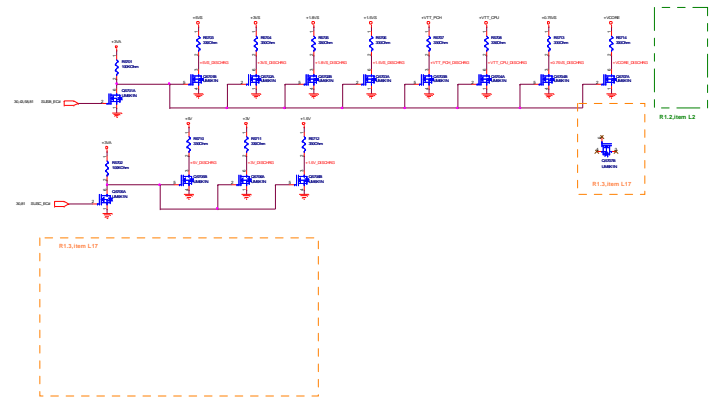


WLAN LED

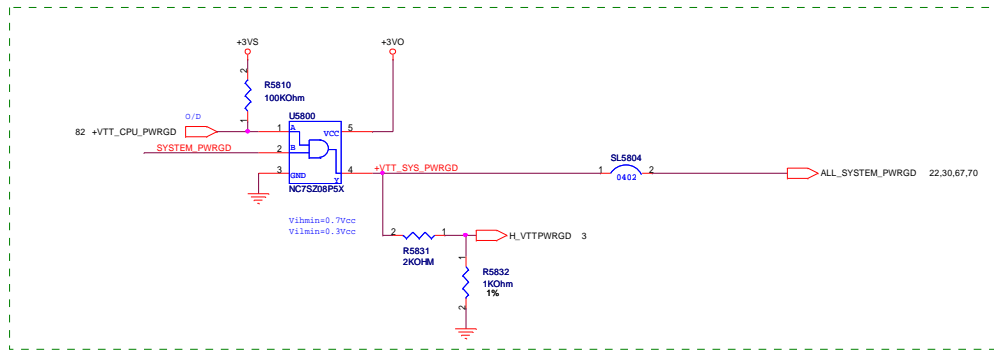
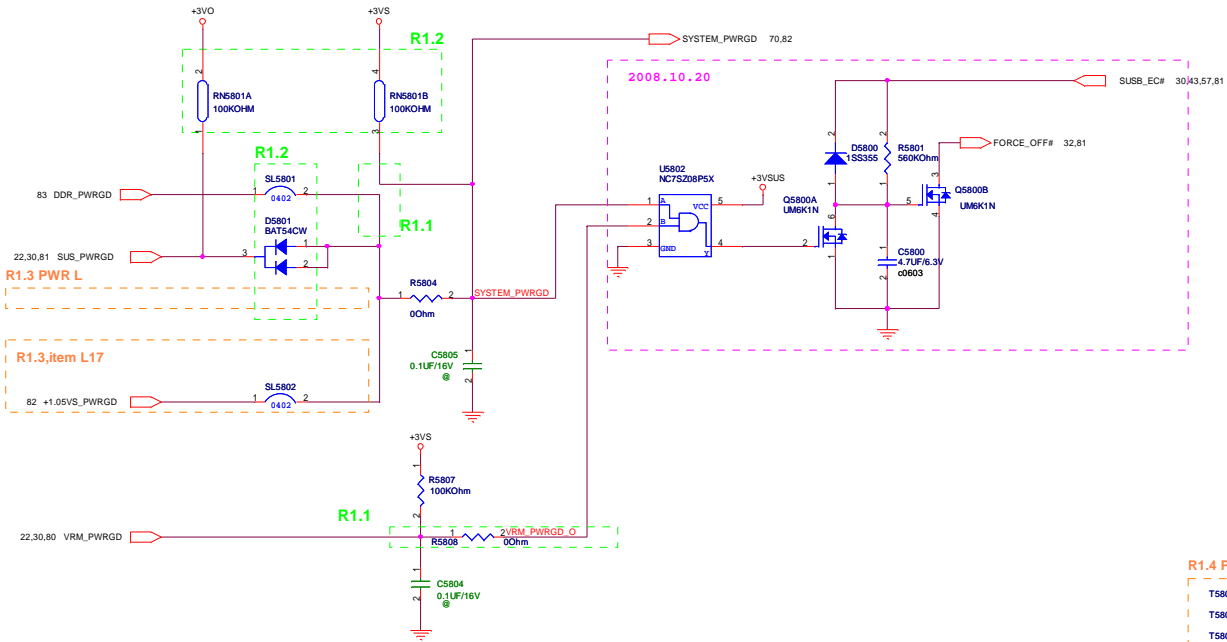


BT LED






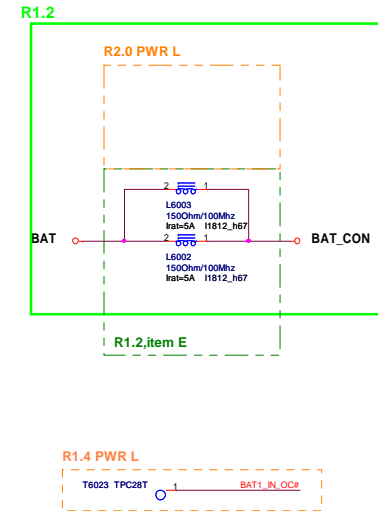
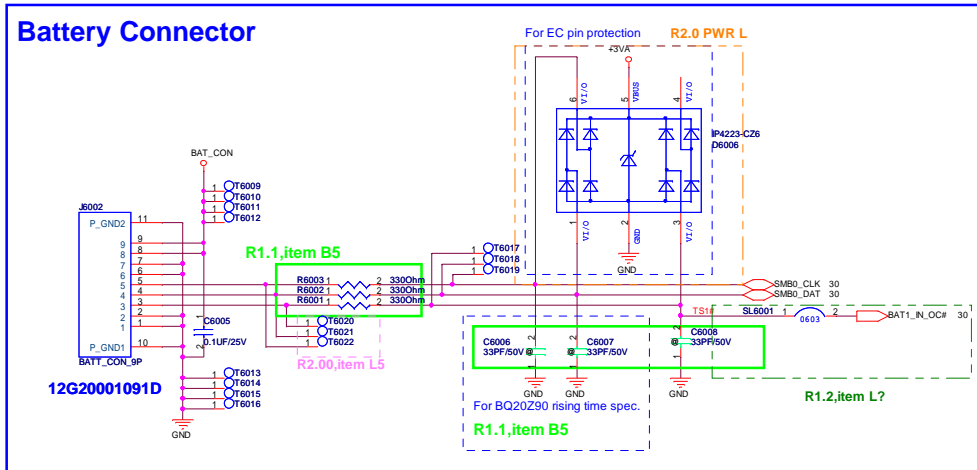
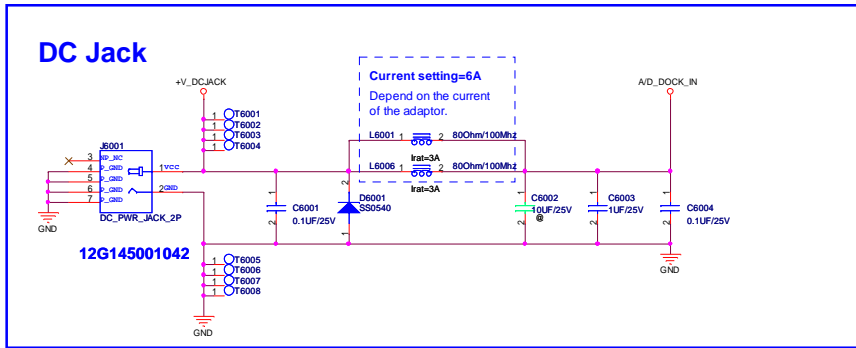
POWER GOOD DETECTOR



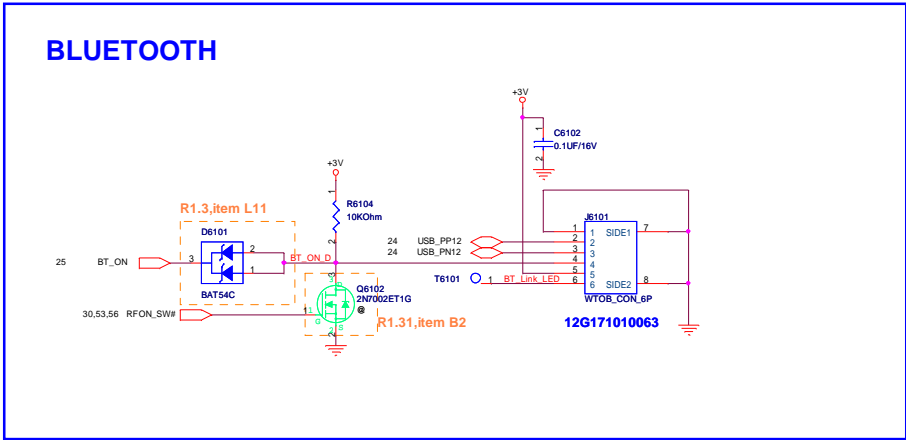
R2.00,item B4

Main Board


		Title : DJ_****	
ASUSTeK COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
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BLUETOOTH

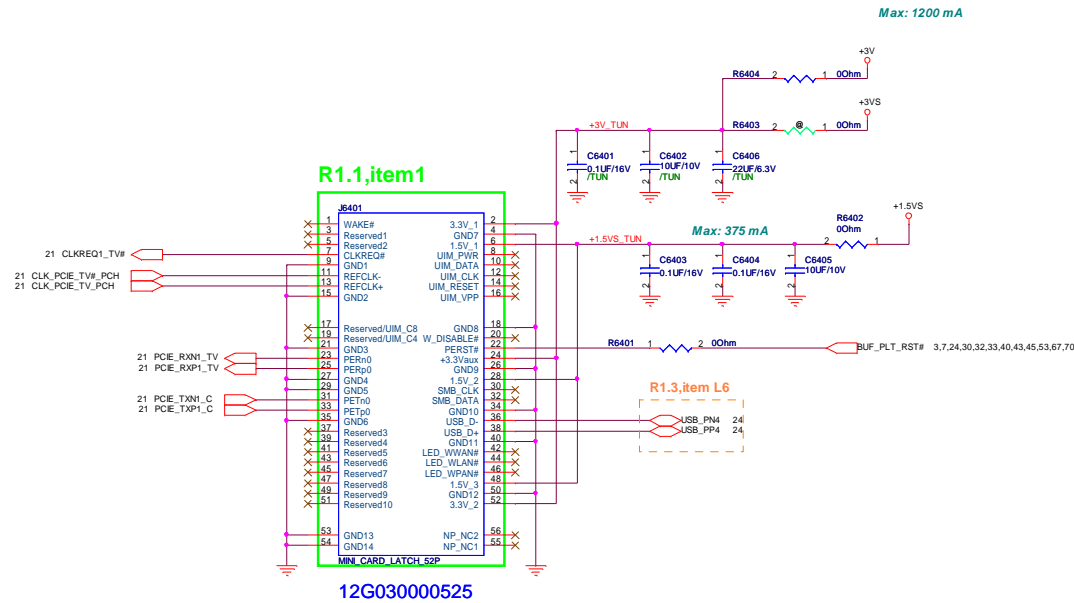


Main Board

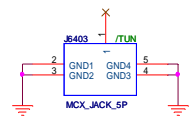
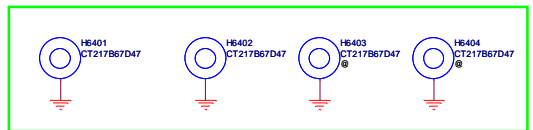
		Title : TPM_****	
ASUSTeK COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
C	M60J	2.00	
Date: Thursday, July 02, 2009		Sheet	62 of 99

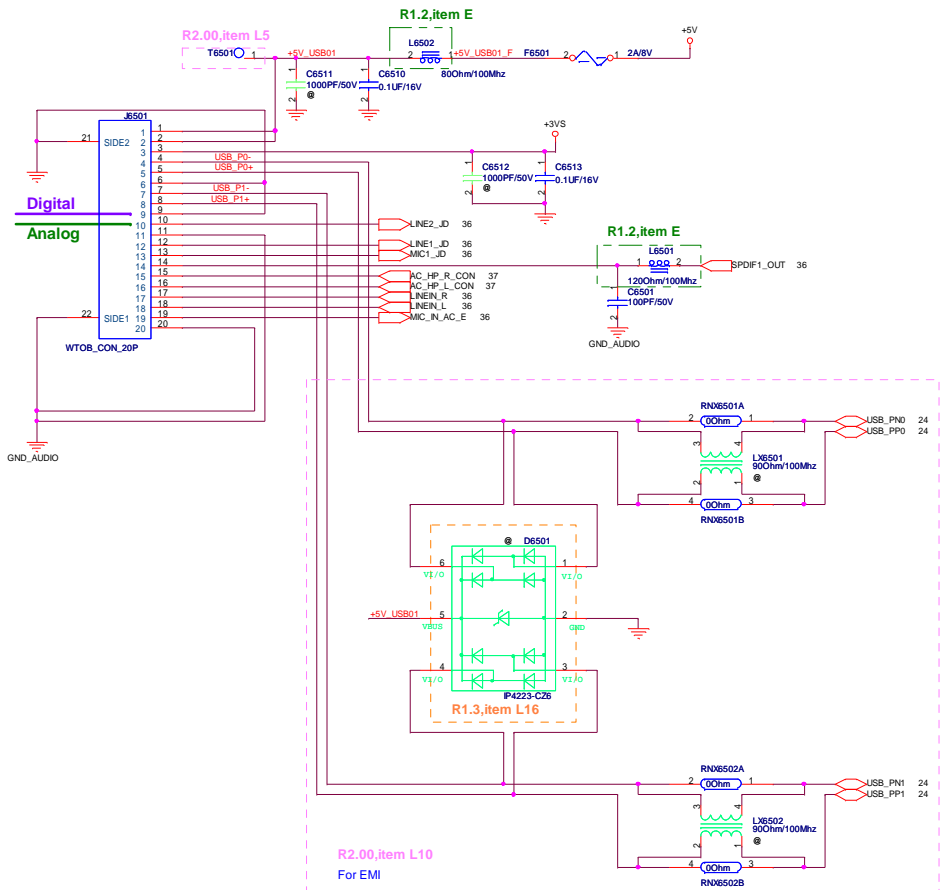
Main Board

		Title : FP_FP Conn	
ASUSTeK COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
C	M60J	2.00	
Date: Thursday, July 02, 2009		Sheet	63 of 99



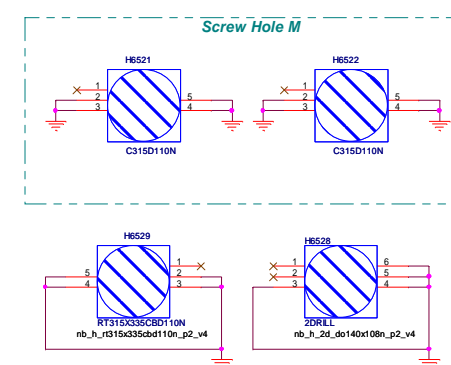
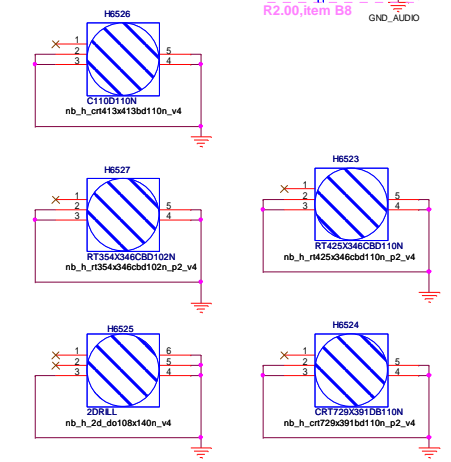
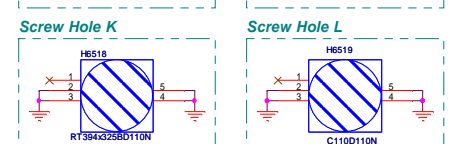
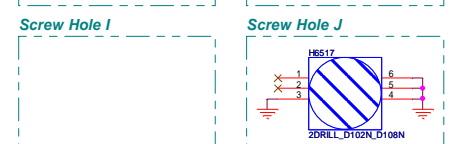
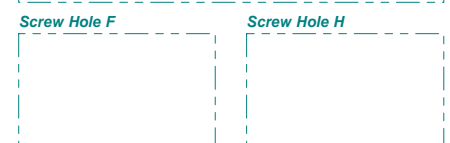
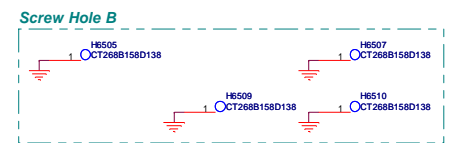
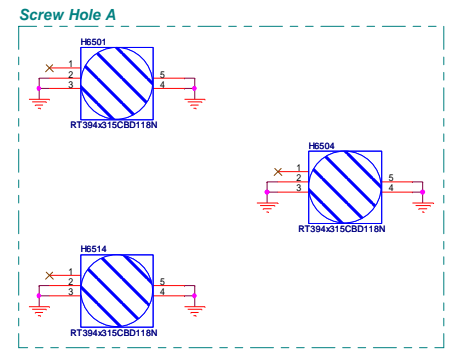
R1.1, item L1

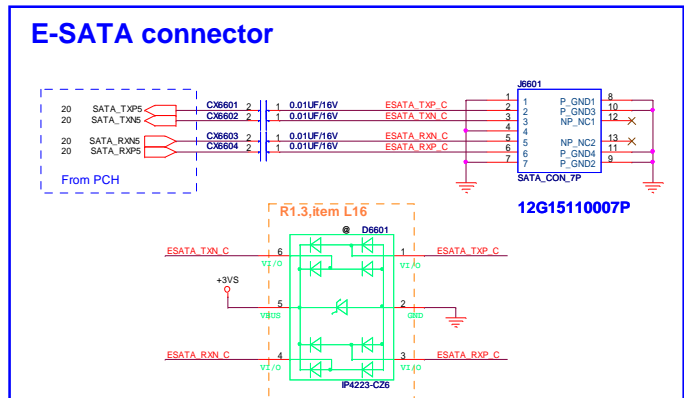
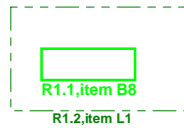




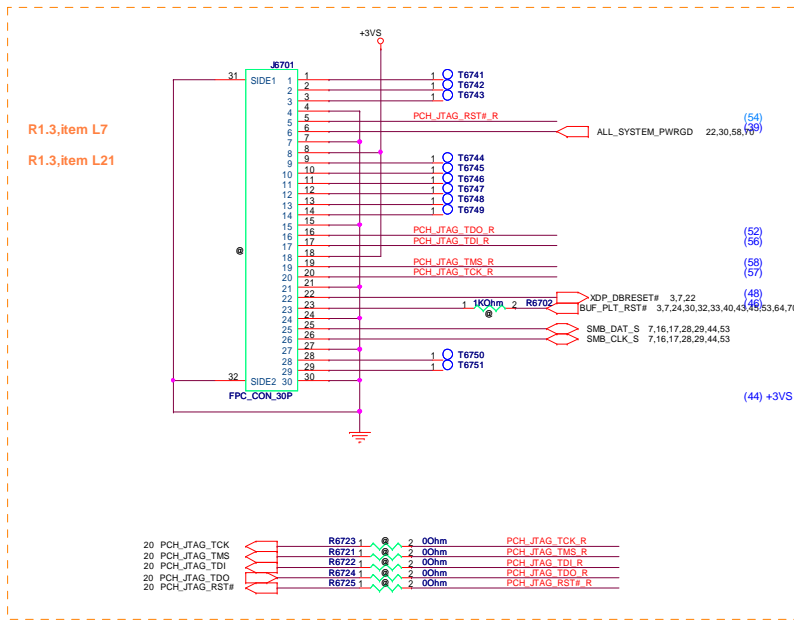
LINE2_ID	C6502	1	2	100PF/50V
LINE1_ID	C6503	1	2	100PF/50V
LINEIN_R	C6504	1	2	100PF/50V
LINEIN_L	C6505	1	2	100PF/50V
MIC_IN_AC_E	C6506	1	2	100PF/50V
MIC1_ID	C6507	1	2	100PF/50V
AC_HP_L_CON	C6508	1	2	100PF/50V
AC_HP_R_CON	C6509	1	2	100PF/50V

Main Board

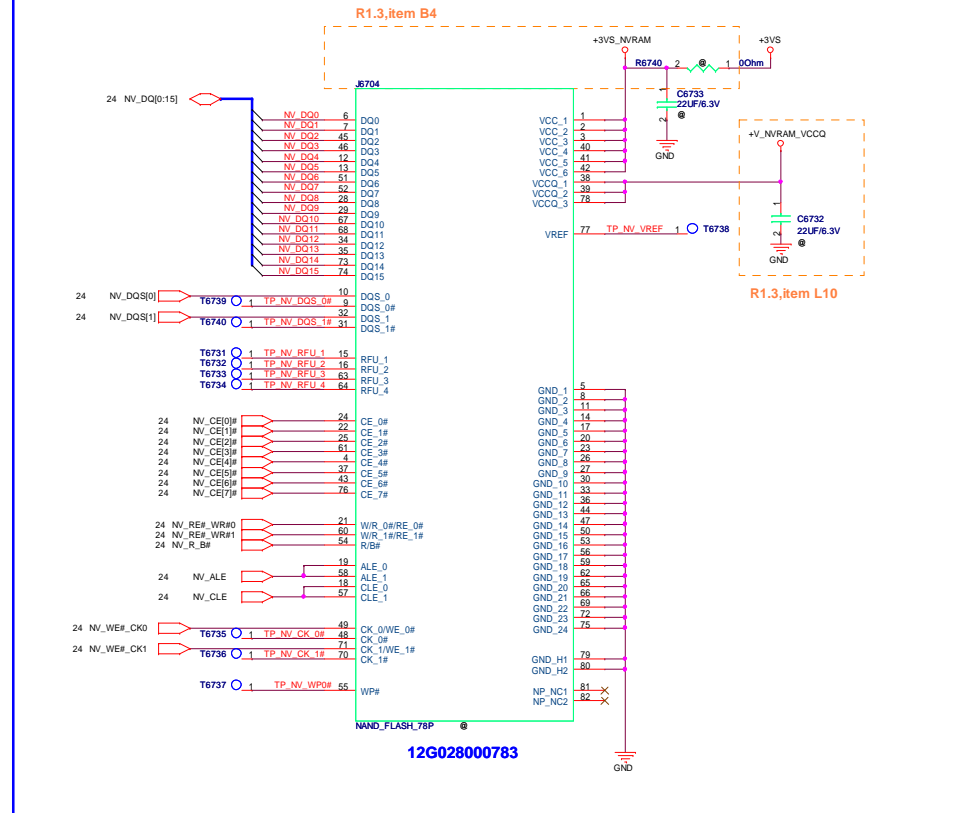




PCH XDP



BRAIDWOOD (ONFI)



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		Title : OTH_LCM	
ASUSTeK COMPUTER INC. NB4		Engineer: JamesT_Wu	
Size	Project Name	Rev	
C	M60J	2.00	
Date: Thursday, July 02, 2009		Sheet	68 of 99

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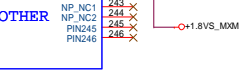
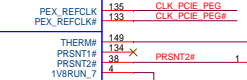
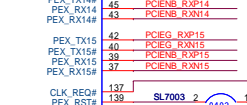
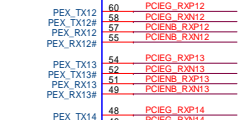
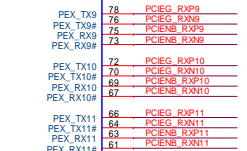
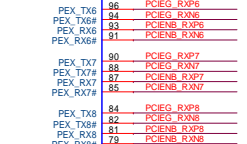
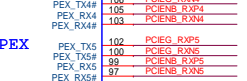
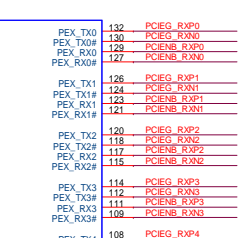
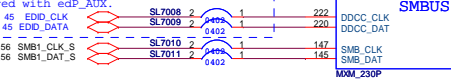
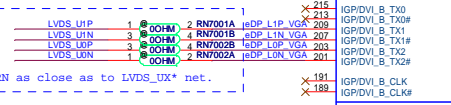
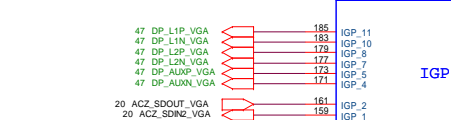
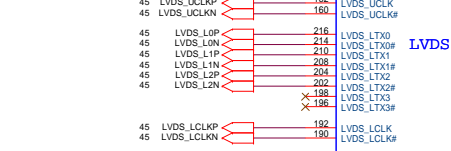
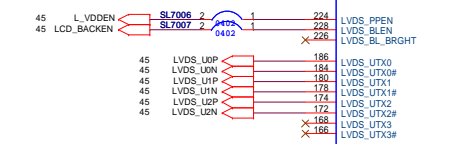
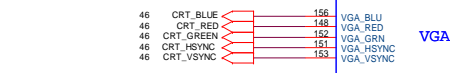
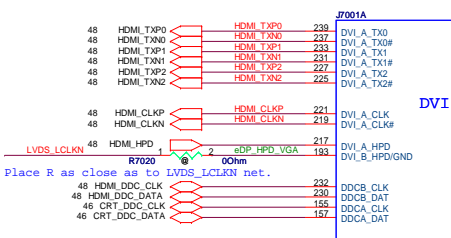
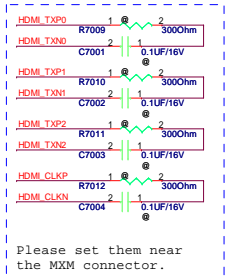
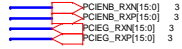
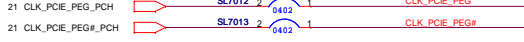
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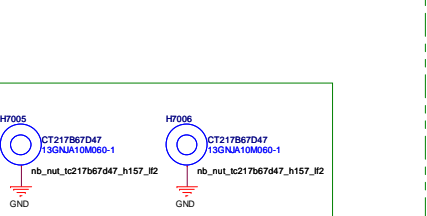
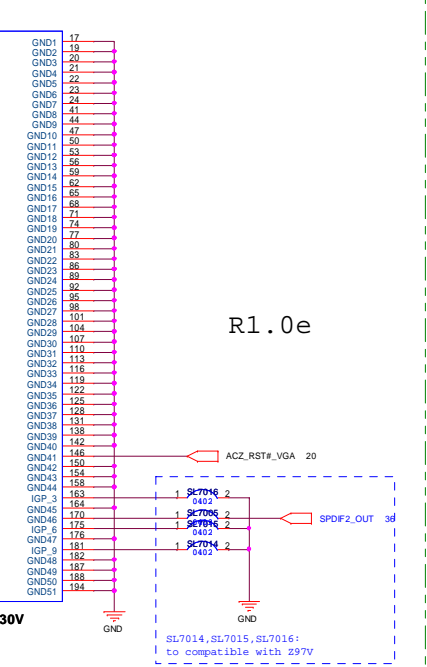
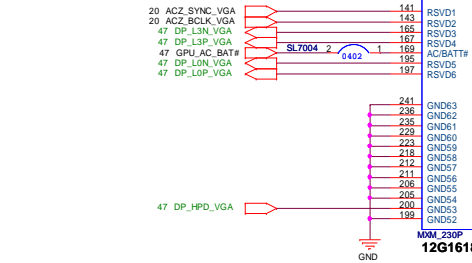
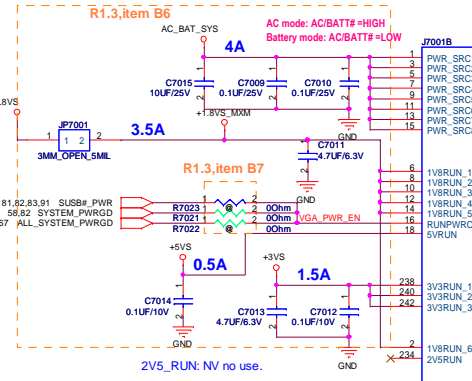
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		Title : OTH_GAME-LED****	
ASUSTeK COMPUTER INC. NB4		Engineer: JamesT_Wu	
Size	Project Name	Rev	
C	M60J	2.00	
Date: Tuesday, July 07, 2009		Sheet	69 of 89

R1.2,item L2

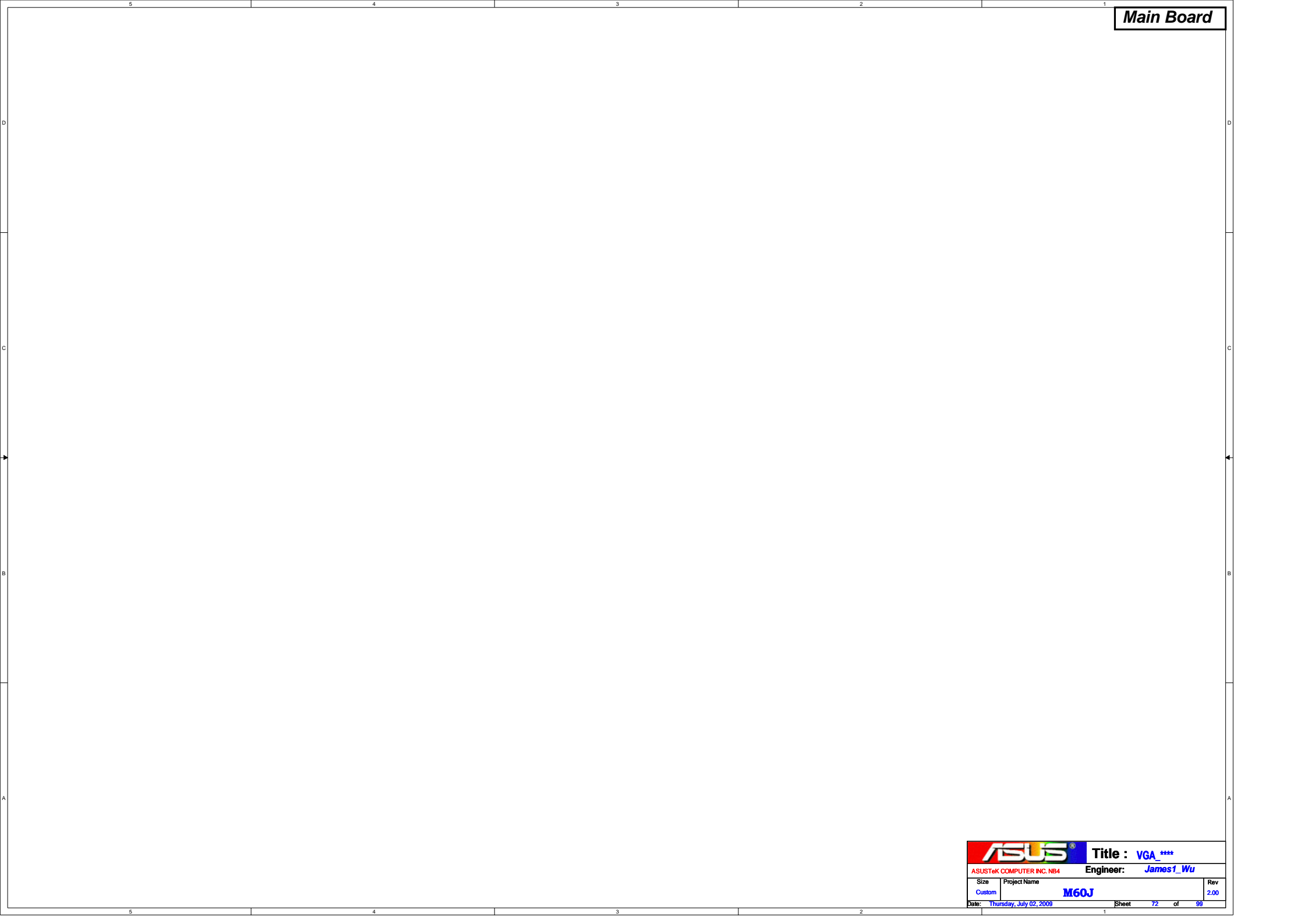



12G16180230V

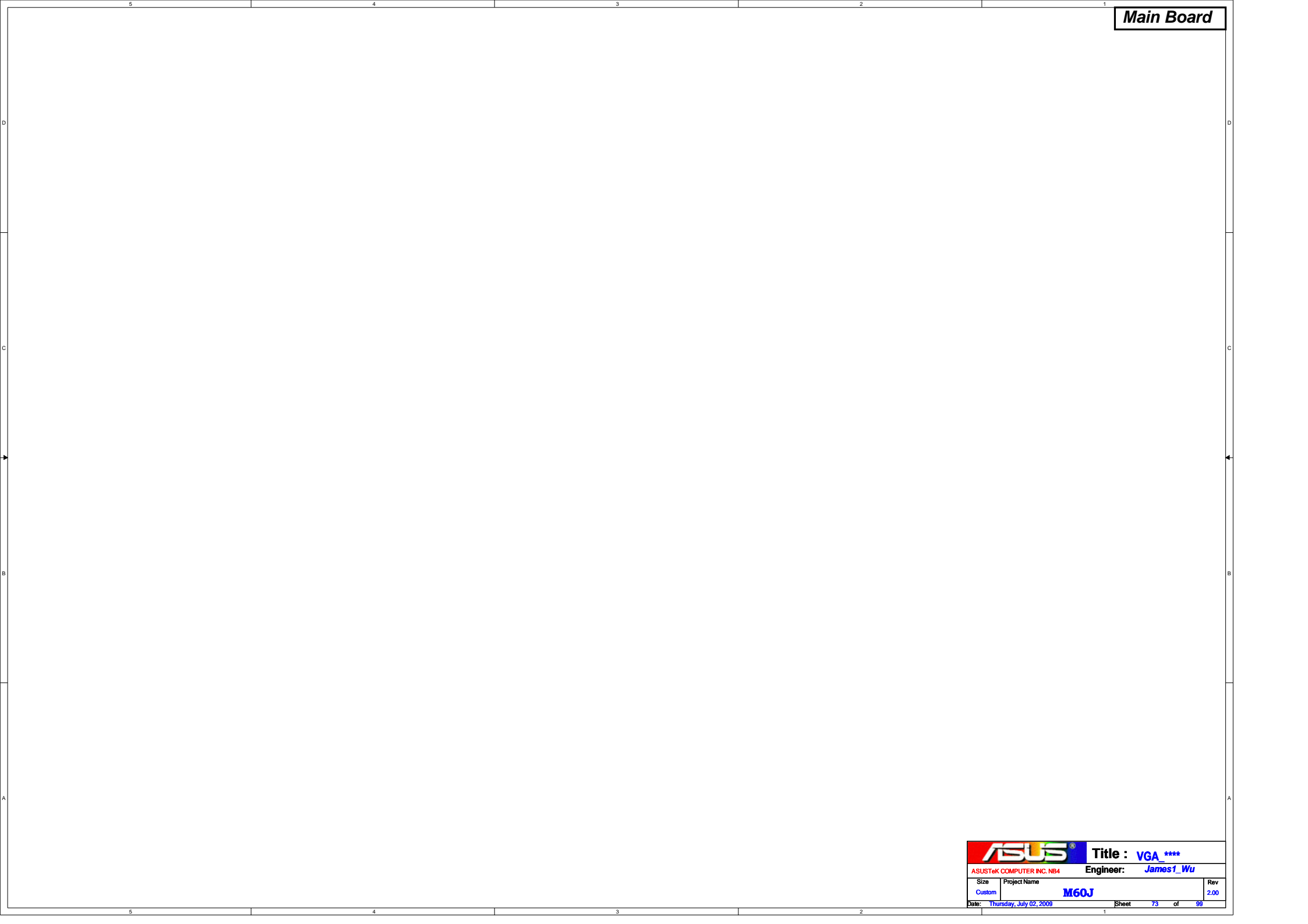



R1.2,item L2

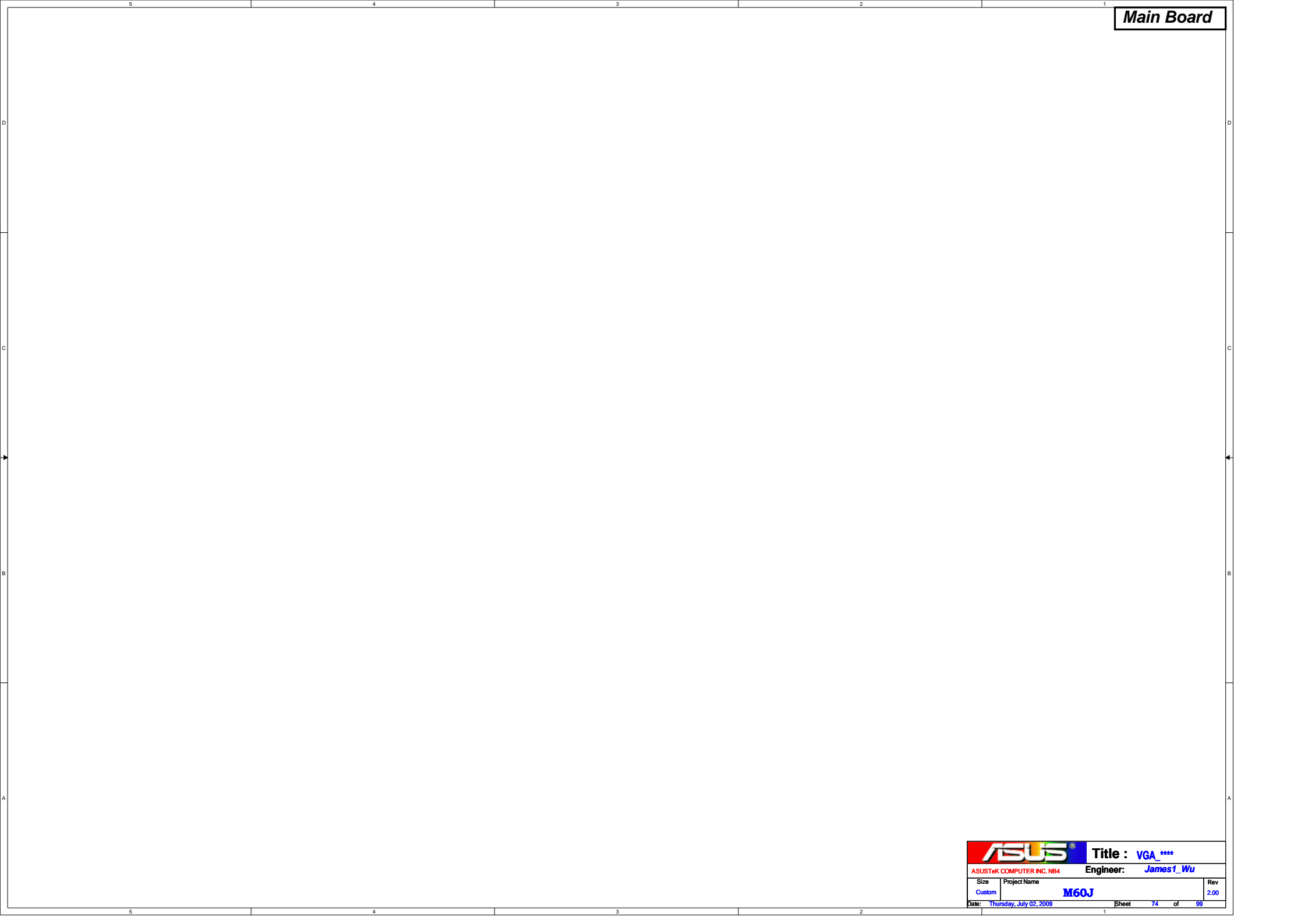





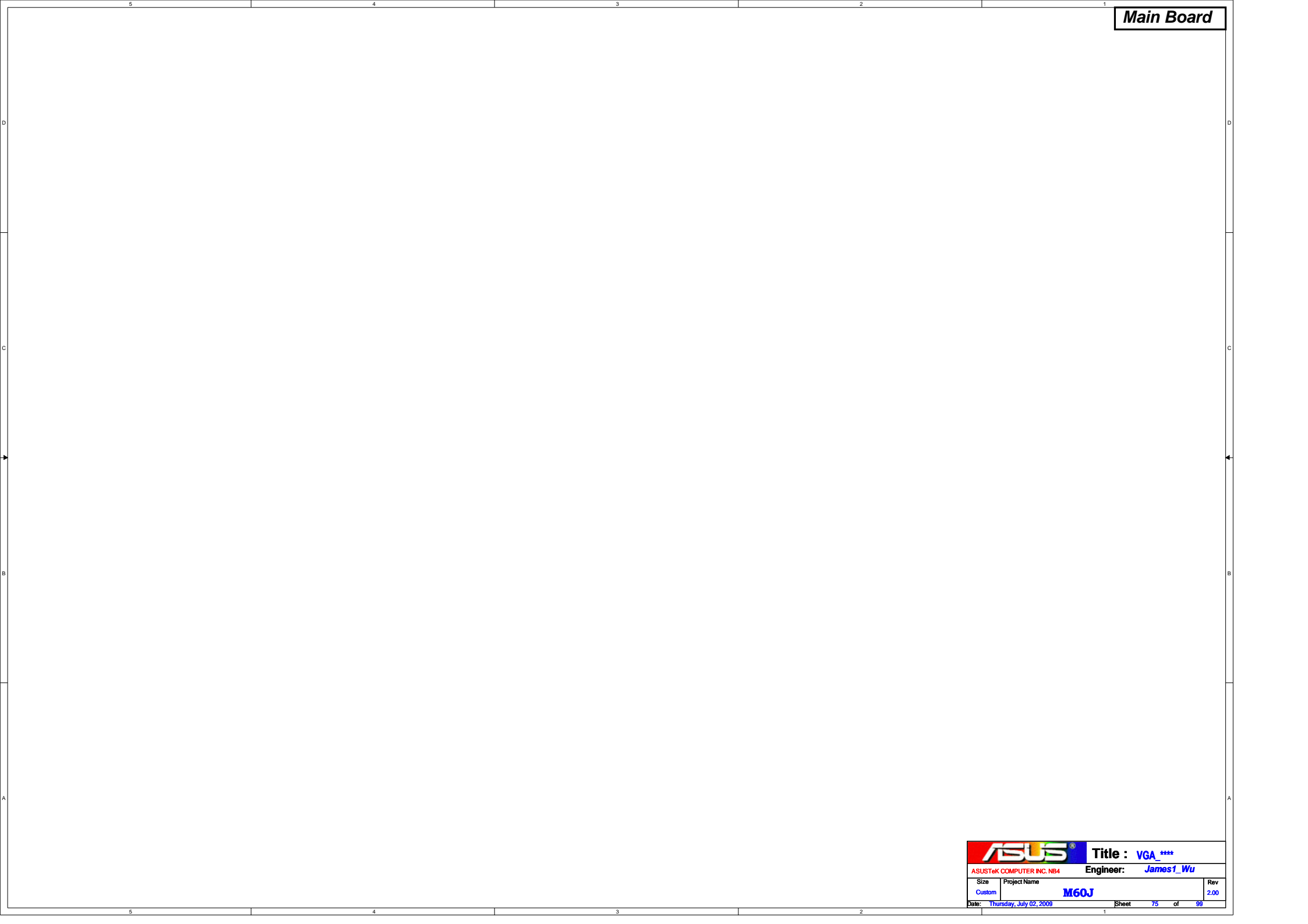
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ASUSTek COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date:	Thursday, July 02, 2008	Sheet	72 of 98




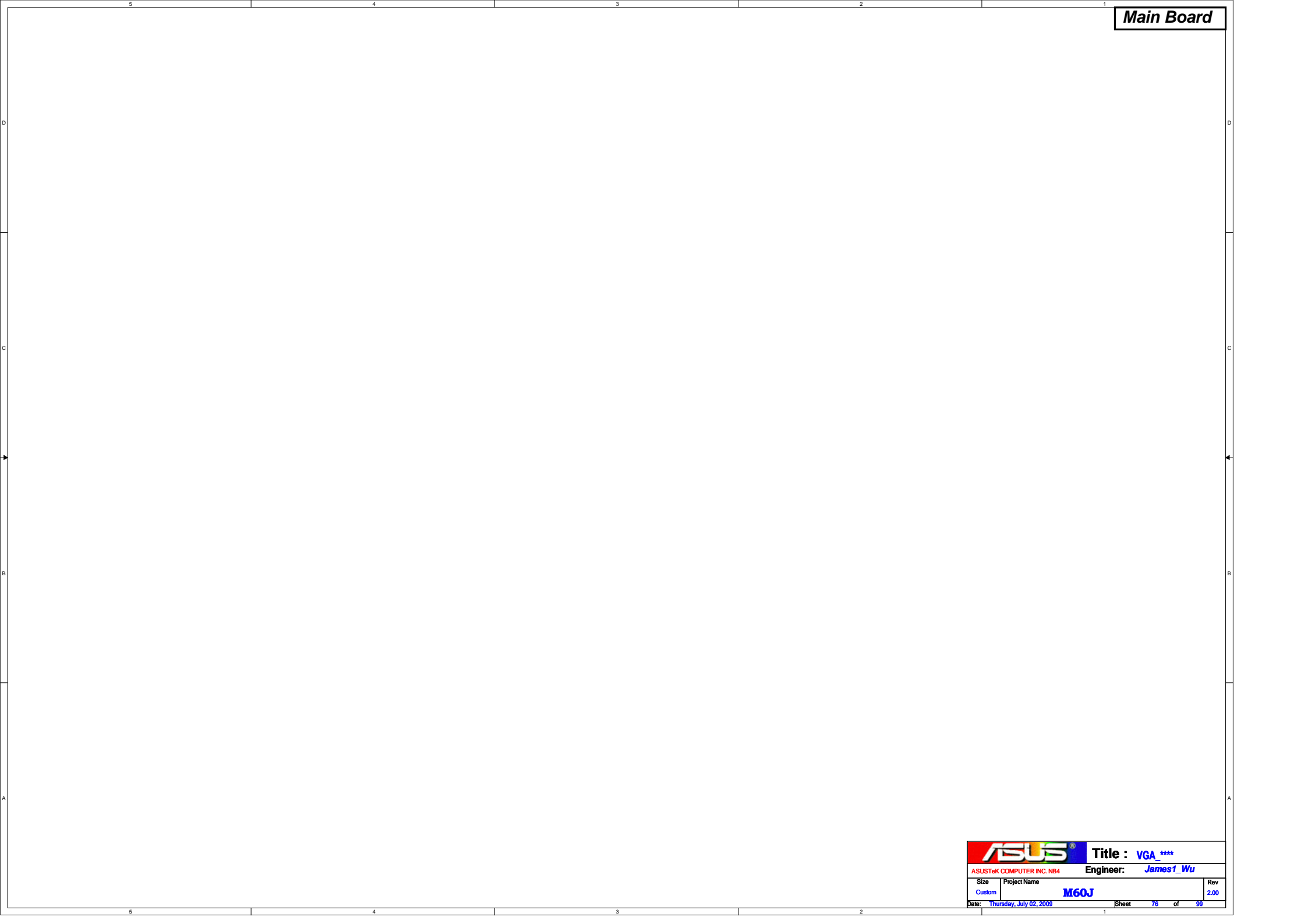
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ASUSTek COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name		Rev
Custom	M60J		2.00
Date: Thursday, July 02, 2008		Sheet	73 of 98




		Title : VGA ****	
ASUSTek COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date: Thursday, July 02, 2008		Sheet	74 of 98



		Title : VGA ****	
ASUSTek COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date: Thursday, July 02, 2008		Sheet	75 of 99



		Title : VGA ****	
ASUSTek COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date: Thursday, July 02, 2008		Sheet	76 of 99

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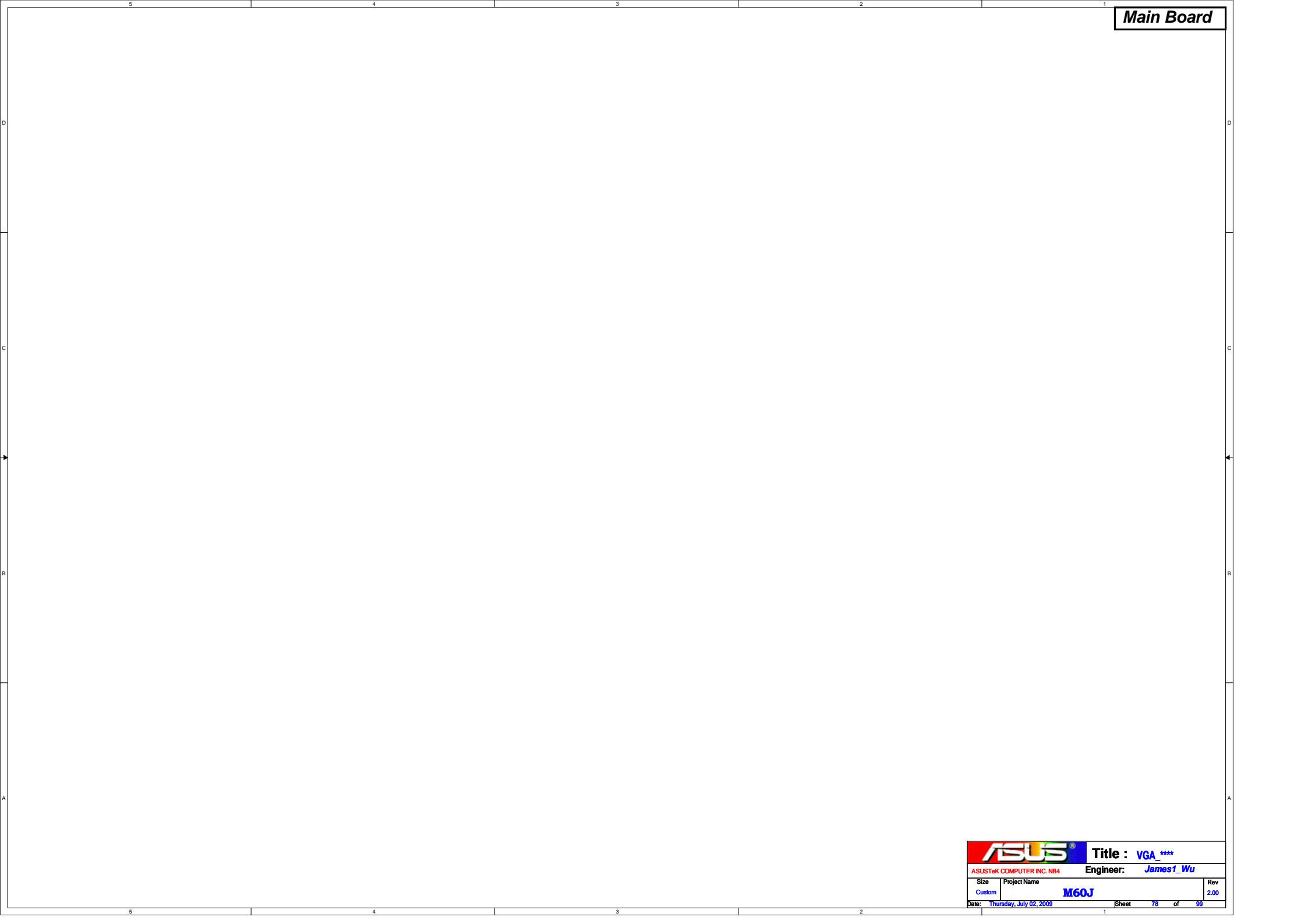
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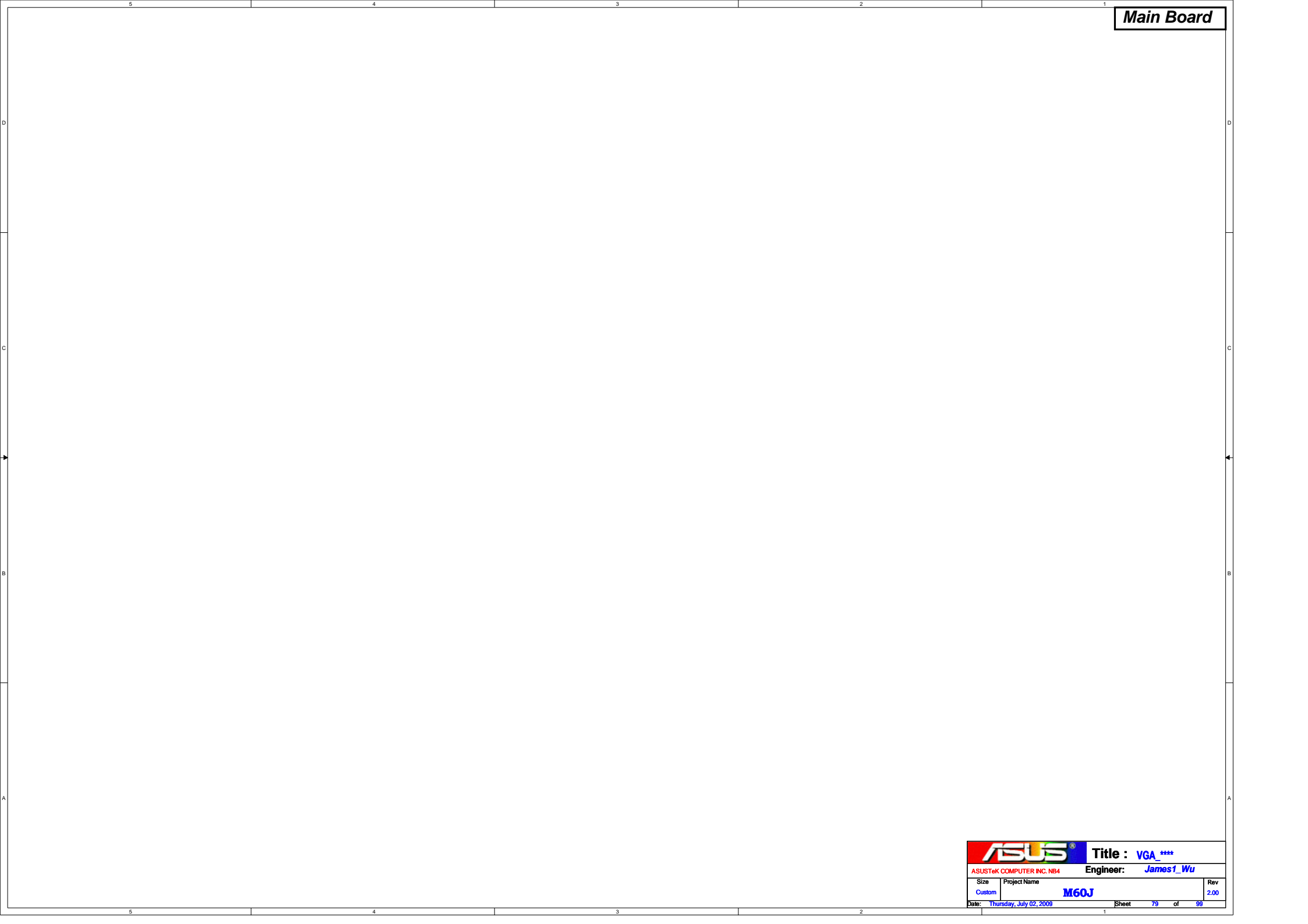
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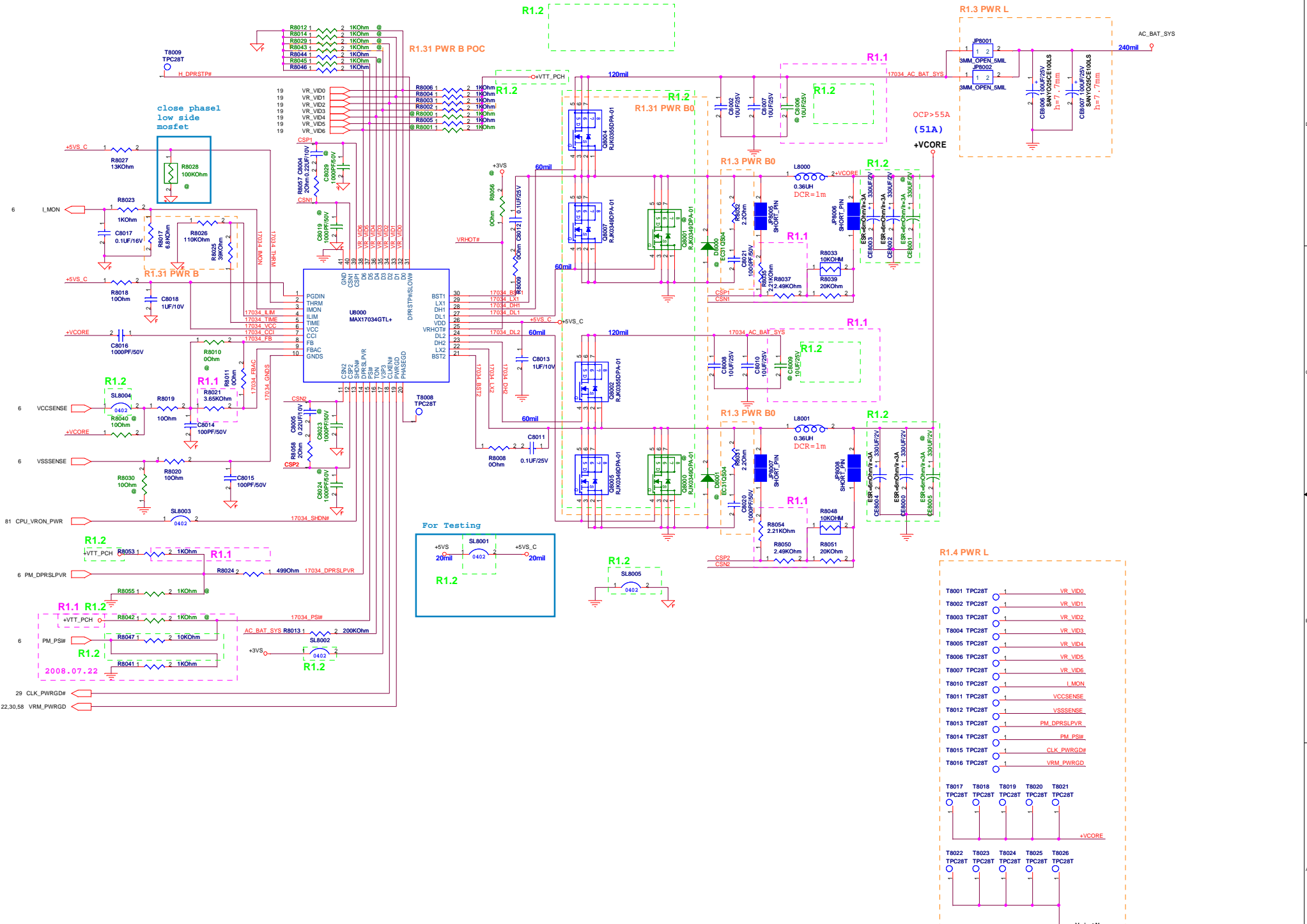
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ASUSTeK COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
C	M60J	2.00	
Date: Thursday, July 02, 2009		Sheet	77 of 99



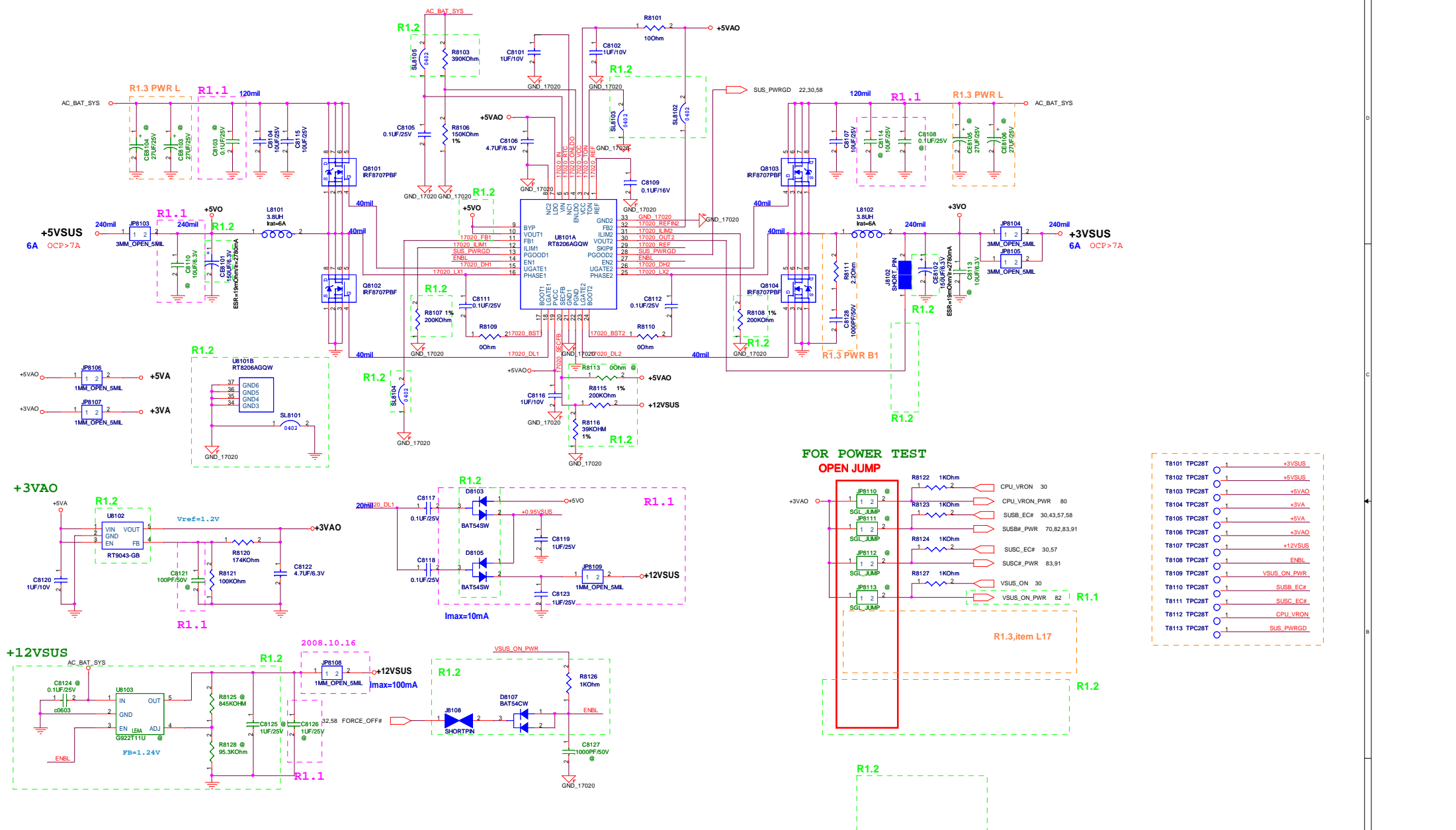
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ASUSTek COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date:	Thursday, July 02, 2008	Sheet	78 of 99



		Title : VGA ****	
ASUSTek COMPUTER INC. NB4		Engineer: James1_Wu	
Size	Project Name	Rev	
Custom	M60J	2.00	
Date: Thursday, July 02, 2008		Sheet	79 of 99

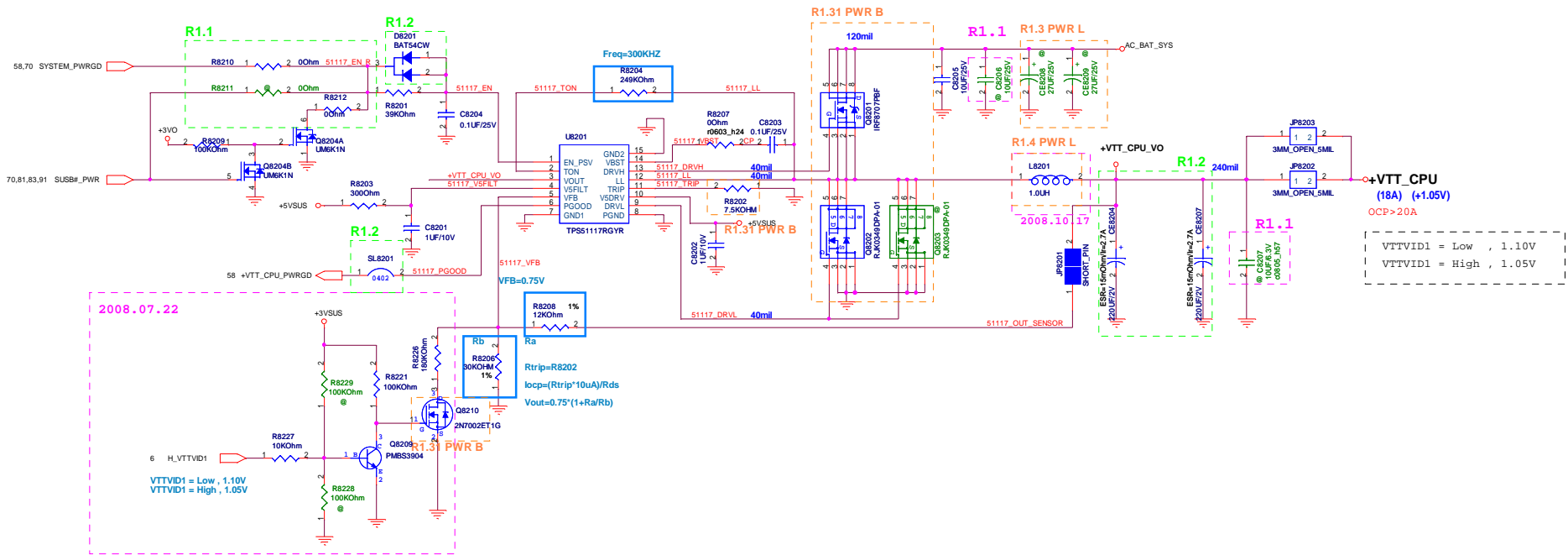


T8001	TPC28T	1	VR_VID0
T8002	TPC28T	1	VR_VID1
T8003	TPC28T	1	VR_VID2
T8004	TPC28T	1	VR_VID3
T8005	TPC28T	1	VR_VID4
T8006	TPC28T	1	VR_VID5
T8007	TPC28T	1	VR_VID6
T8010	TPC28T	1	I_MON
T8011	TPC28T	1	VCCSENSE
T8012	TPC28T	1	VSSSENSE
T8013	TPC28T	1	PM_DPRSLPVR
T8014	TPC28T	1	PM_PSW
T8015	TPC28T	1	CLK_PWRGD
T8016	TPC28T	1	VRM_PWRGD
T8017	TPC28T	1	+VOCORE
T8018	TPC28T	1	
T8019	TPC28T	1	
T8020	TPC28T	1	
T8021	TPC28T	1	
T8022	TPC28T	1	+VOCORE
T8023	TPC28T	1	
T8024	TPC28T	1	
T8025	TPC28T	1	
T8026	TPC28T	1	

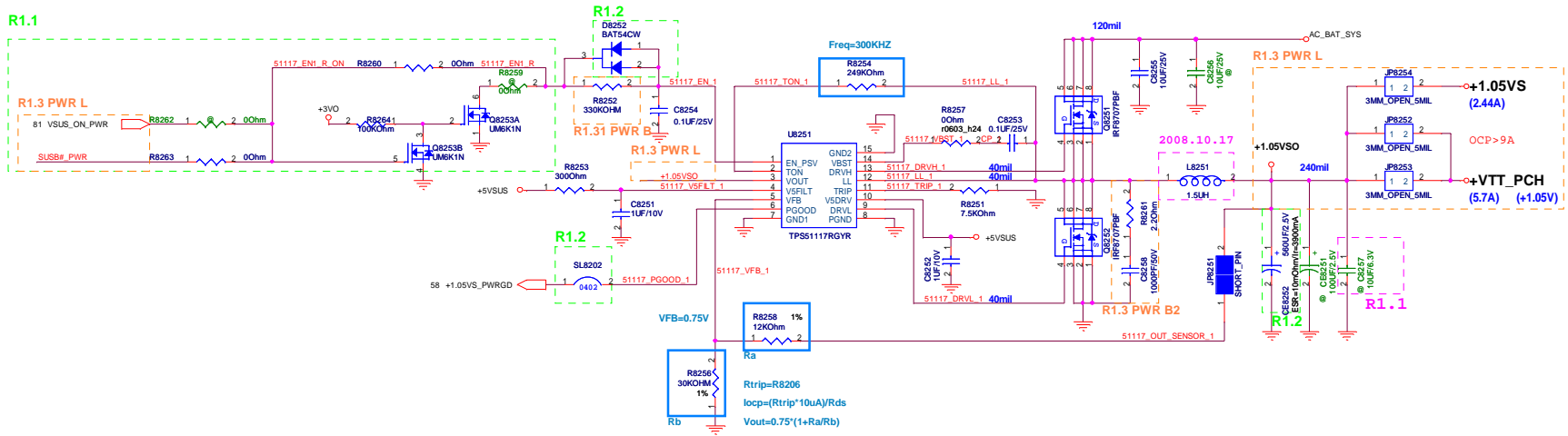


FOR POWER TEST
OPEN JUMP

T8101 TPC28T	+	+3VSUS
T8102 TPC28T	+	+5VSUS
T8103 TPC28T	+	+5VAO
T8104 TPC28T	+	+3VA
T8105 TPC28T	+	+5VA
T8106 TPC28T	+	+3VAO
T8107 TPC28T	+	+12VSUS
T8108 TPC28T	+	ENBL
T8109 TPC28T	+	V\$US_ON_PWR
T8110 TPC28T	+	SUSB_EC#
T8111 TPC28T	+	SUSC_EC#
T8112 TPC28T	+	CPU_VRON
T8113 TPC28T	+	SUS_PWRGD



VTTVID1 = Low , 1.10V
VTTVID1 = High , 1.05V

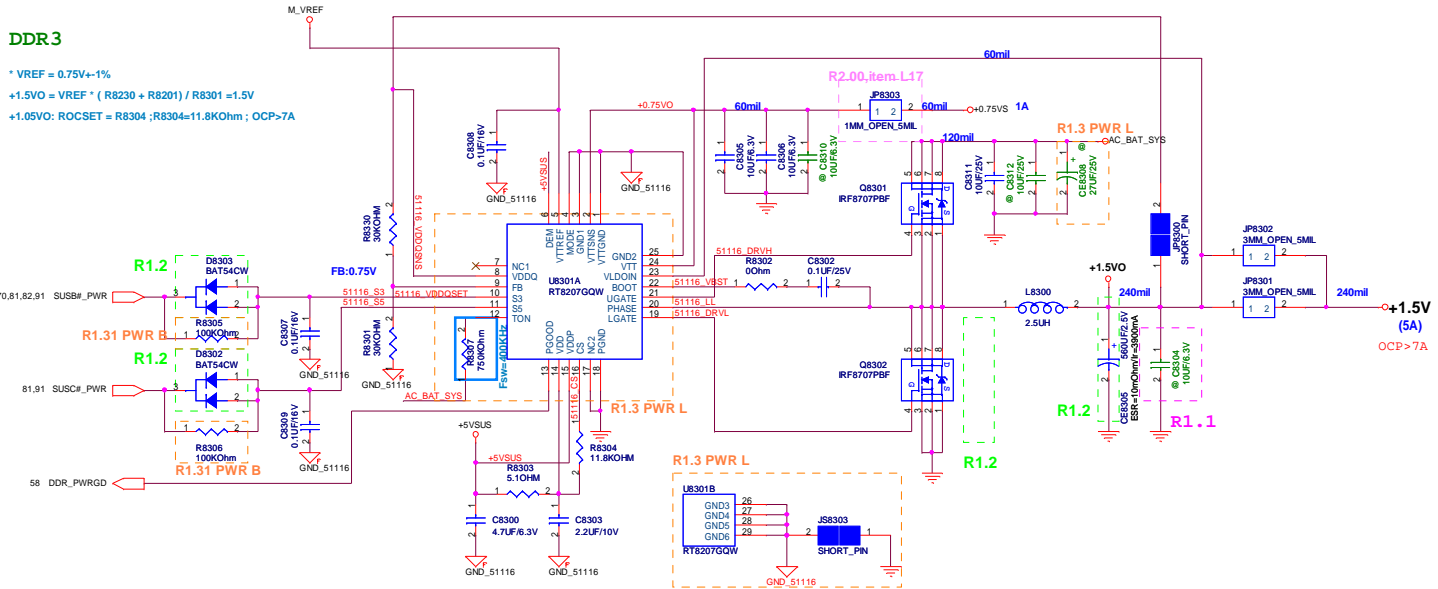


R1.4 PWR L

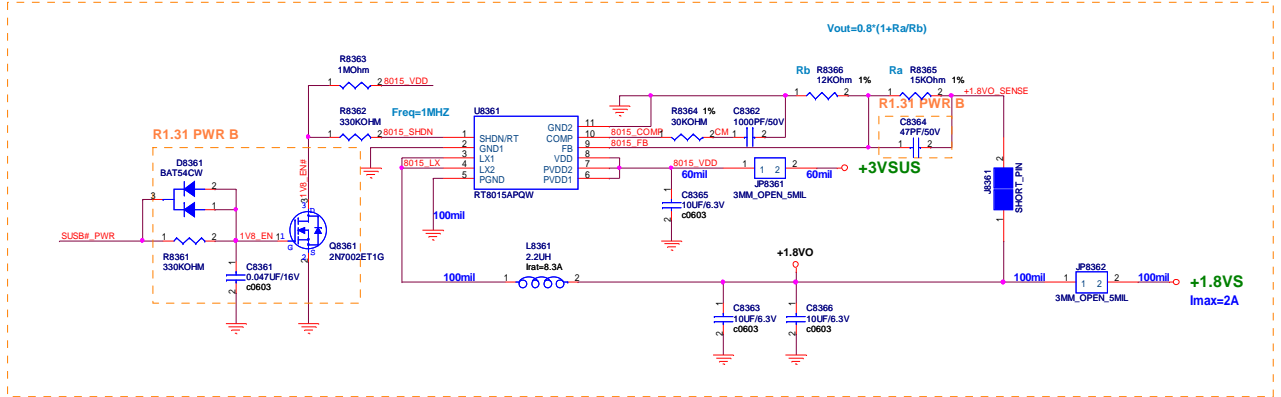
T8201	TPC28T	1	SYSTEM_PWRGD
T8202	TPC28T	1	SUSB#_PWR
T8203	TPC28T	1	+VTT_CPU_PWRGD
T8204	TPC28T	1	H_VTTVID1
T8205	TPC28T	1	+VTT_CPU
T8206	TPC28T	1	+VTT_PCH
T8207	TPC28T	1	+1.05VS
T8208	TPC28T	1	+1.05VS_PWRGD

DDR3

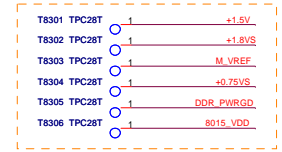
* VREF = 0.75V±1%
 +1.5VO = VREF * (R8230 + R8201) / R8301 = 1.5V
 +1.05VO: ROCSET = R8304 ; R8304=11.8KOhm ; OCP>7A



R1.3 PWR L



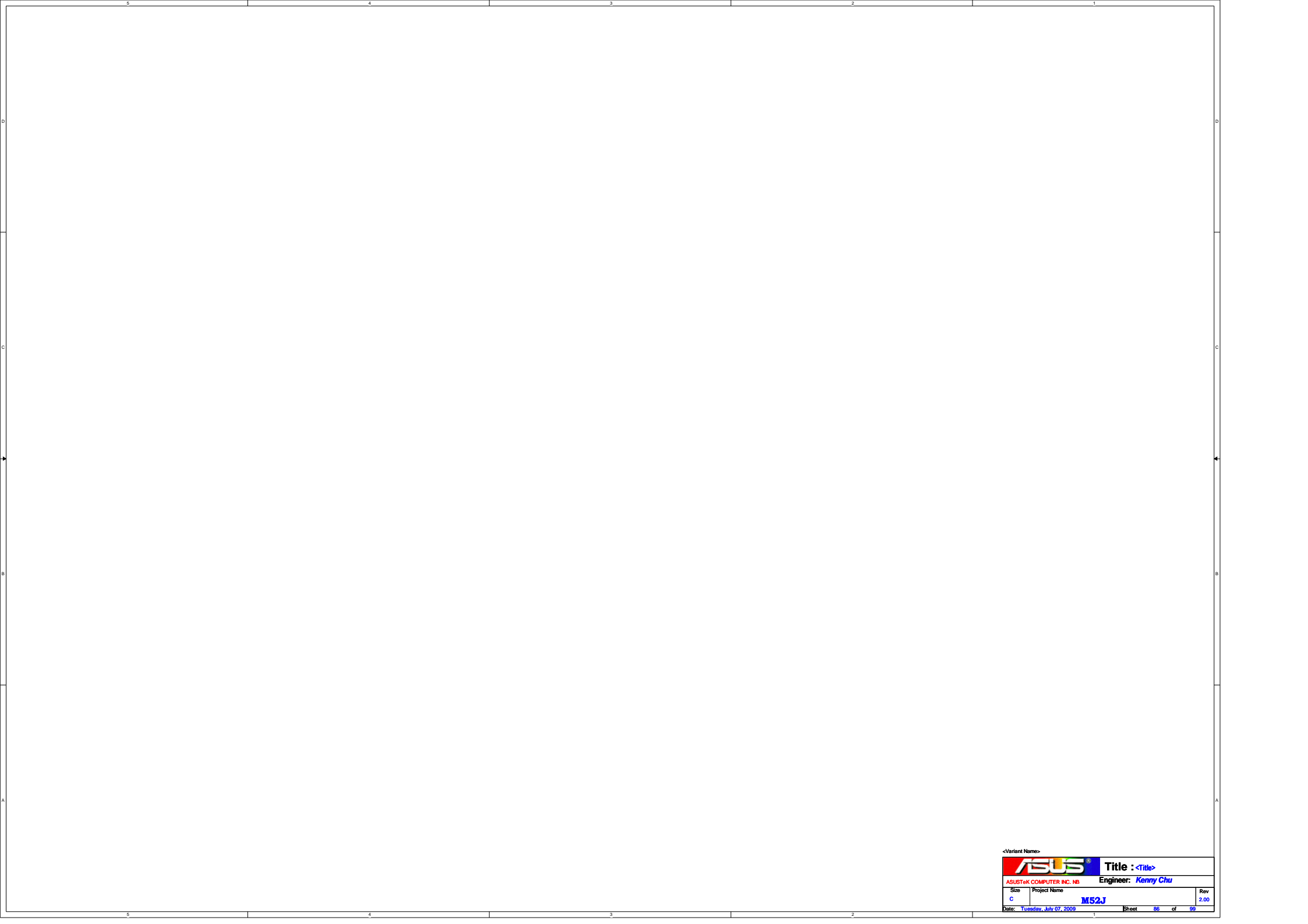
R1.4 PWR L




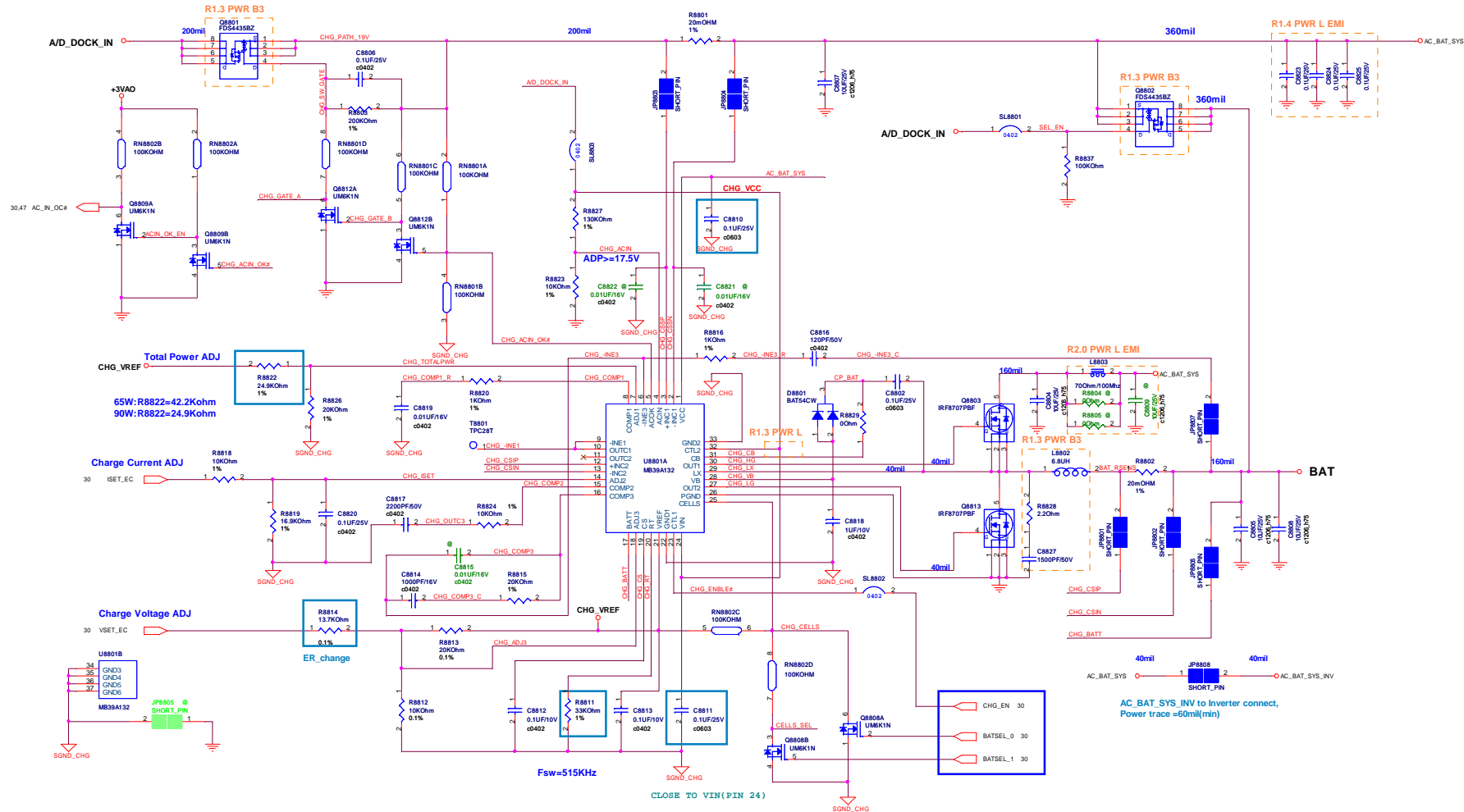
+3VM

R1.3,item L17

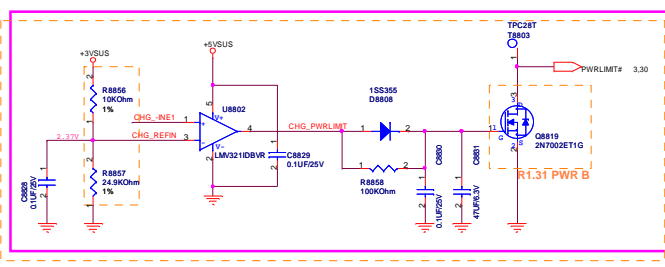
R1.3,item L17



<Variant Name>		
		Title : <Title>
ASUSTeK COMPUTER INC. NB		Engineer: <i>Kenny Chu</i>
Size C	Project Name M52J	Rev 2.00
Date: <u>Tuesday, July 07, 2009</u>		Sheet 86 of 99



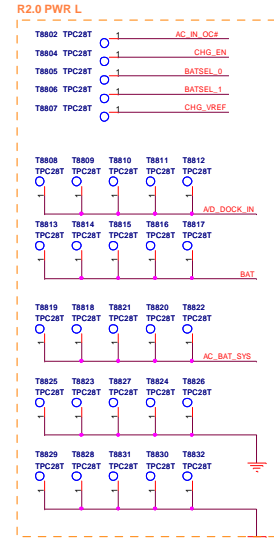
Power Limit



TOTAL COUNT:66 PCS

Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS



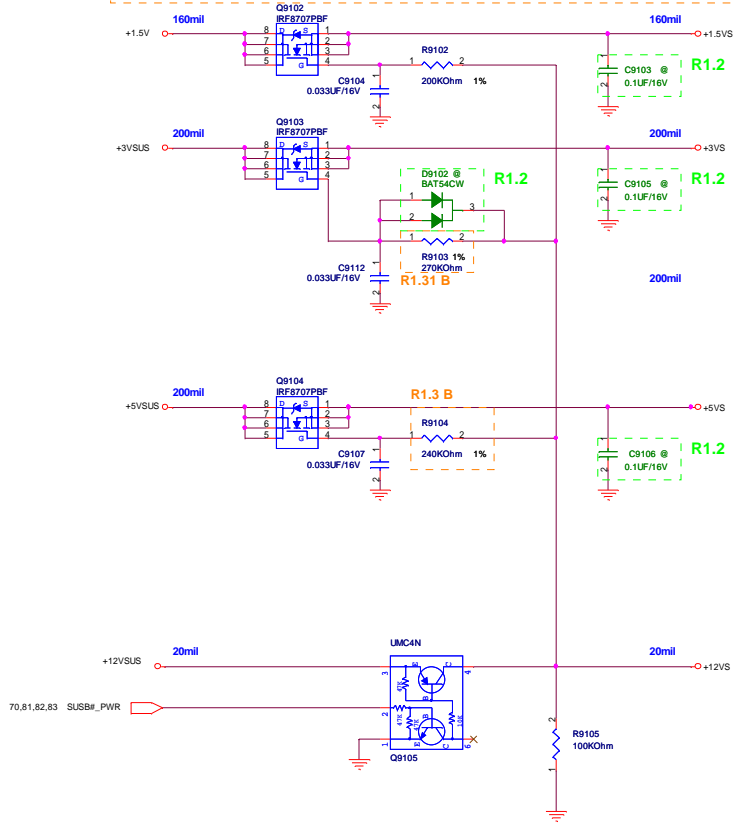
Charger IC and EC Code correlation sheet :
 Charger MAX8725 => EC CODE : 200
 Charger MAX17015 => EC CODE : 201
 Charger MB39A132 => EC CODE : 202

R1.2



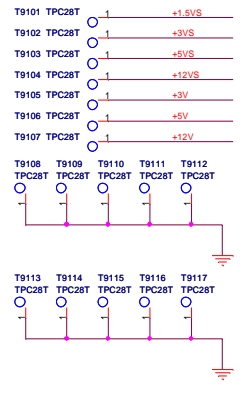
SUSB#_PWR POWER

R1.3 PWR L

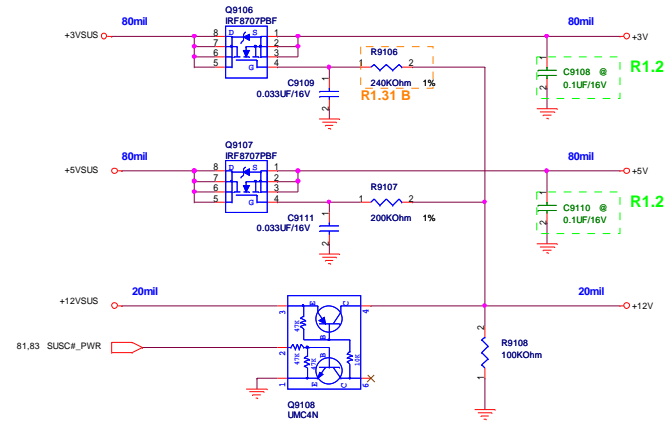


70.81,82,83 SUSB#_PWR

R1.4 PWR L

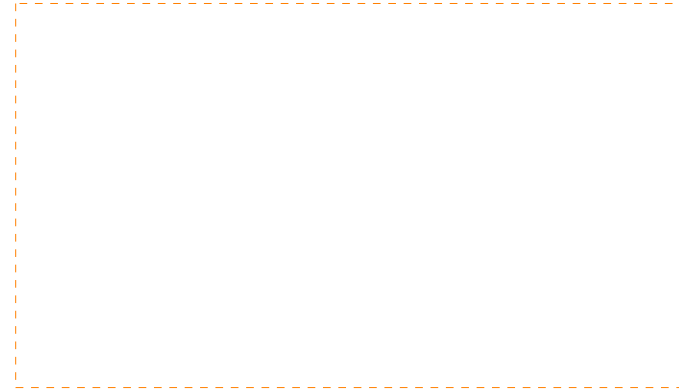


SUSC#_PWR POWER



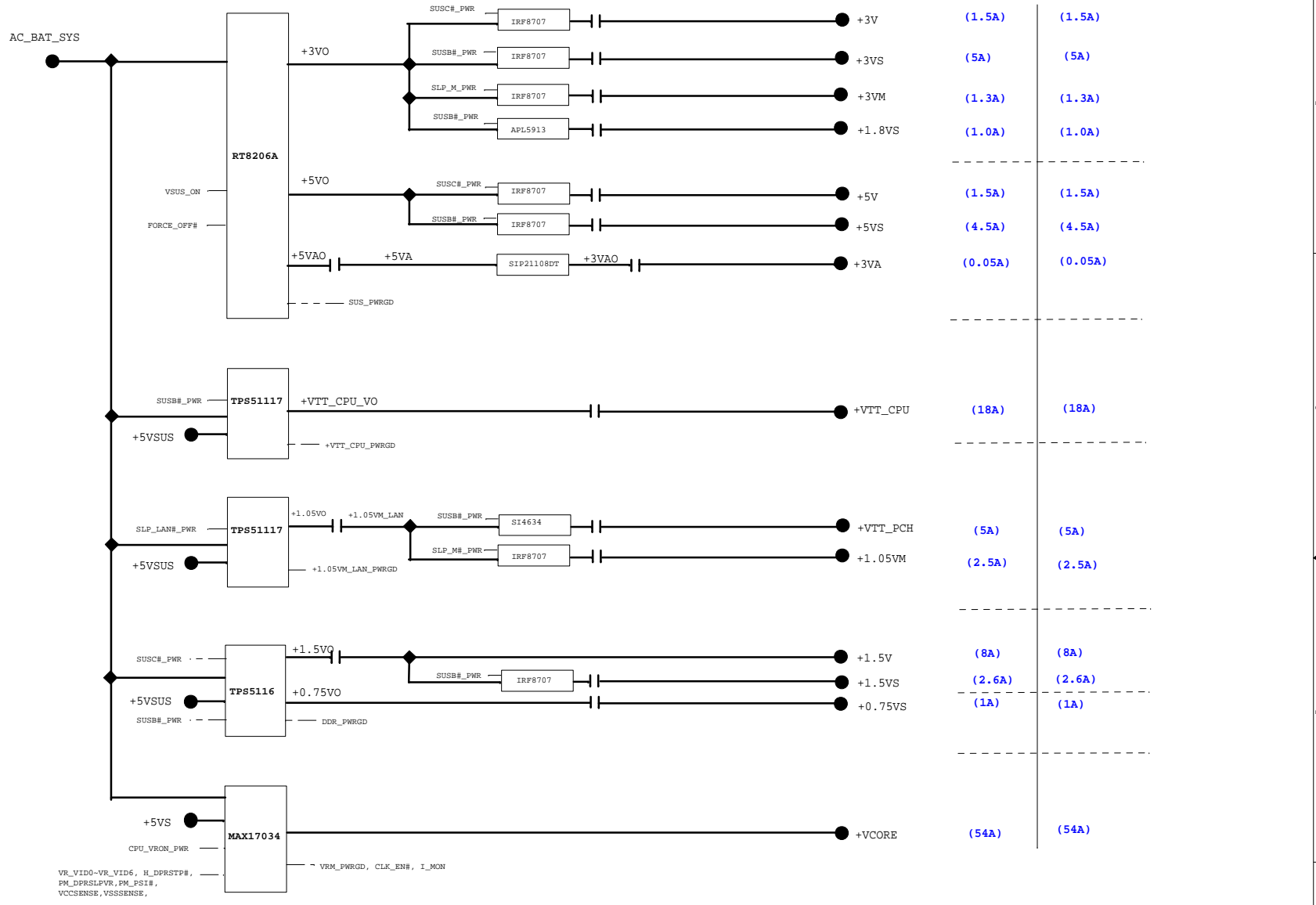
81,83 SUSC#_PWR

R1.3 PWR L



POWER_SIGNAL





[M52J] R1.0

(Release on 2008/09/23)

SR1 Gerber out revision.

[M52J] R1.0 => R1.1

(Release on 2008/10/16)

[Layout Changed - EE]

- L1. For ME request:
 - 1-1. Change H6401 from 12G030000522 to 12G030000525.
 - 1-2. Change J4201 from 12G340003601 to 12G340003605.
 - 1-3. Change H6401, H6402, H6403, H6404 from 13GNHC10M020-1 to 13G021043011.
 - 1-4. Change H5303, H5304, H7003, H7004 from 13GNHC10M020-1 to 13G021036011.
- L2. P18: Change M2 circuit for intel requet.
- L3. Re-define J4501 circuit for cost down.
 - 3-1. P45: Re-define J4501 pin6, pin30-40, delete J4502.
 - 3-2. P36: Delete C3639. (MOMO OUT)
 - 3-3. P38: Modify circuit for Internal MIC.
 - 3-3. P38: Delete all items in this page for spec change.
- L4. For SPT flash circuit:
 - 4-1.P26: Change circuit for PCH SPI flash.
 - P20: Change R2015 pull-up from +3VM to +3VM_SPI
 - 4-2.P30: Change circuit for EC SPI flash.
- L5. To prevent device damage if power not ready:
 - 5-1.P20,P30: Add J2001,J3001 to isolate +3VA.
 - 5-2.P20,P21,P22,P24,P25,P27: Modify +3VSUS to +3VSUS_ORG.
 - P27: Add J2703,J3001 to isolate +3VSUS.
 - 5-3.P27: Modify +3VSUS to +5VSUS_ORG,add J2704 to isolate.
- L6. For decoupling:
 - 6-1: Change C2903 from net +3VS_VDDPCIEX to +VDDIO_42.
 - 6-2: Change C2904 from net +3VS_VDDPCIEX to +VDDIO_28.
 - 6-3: Add C2927 to +VTT_CPU.
- L7. P29: Reserve net +VTT_CPU and add +3VS for frequency 133MHz.
- L8. P03,P29: Delete colay net for PCH buffer mode clock is workable.
Net: CLK_CPU_BCLK_IC5,CLK_CPU_BCLK_IC5#
- L9. For test:
 - 9-1. P22: Add R2265,R2266@,R2267 for test.
 - 9-1. P22: Add R2265,R2266@,R2267 for test.
- L10. P03,P30: Add power limit circuit for power request.
- L11. P91: Add D9101,D9102 for MOS close quickly.
- L12. P03: Add R0366,R0367 to disable FDI for discrete GFX.
- L13. P30,P31: Reserved circuit for testing U3101 removed.
- L14. P31: Exchange D3105 pin 4,5 net for EMI request.
- L15. P22: For S0-to-G3,S5-to-G3 solution.
- L16. P48: Modify circuit for design IP change.
- L17. P30: Delete BAT_LEARN function for power request cost down.

[Layout Changed - PWR]

- L1. For reduce noise add inupt CAP CE8006,CE8007,CE8800.
- L2. P80 change pull high power
Follow intel common schematic from +VTT_CPU_VO to +VTT_PCH
- L3. For +12VSUS test
 - 3-1. P80: bump power from +5VSUS to +5V0
 - 3-2. P80: Add JP8108 JP8109
- L4. To enhance charger bump energy add C8129,D8108,D8109
- L5. Change +1.05VM LAN enable
from SLP_LAN#_PWR to VSUS_ON_PWR for EE request
- L6. For enable frequency test
Add R8210,R8211,R8212,R8259,R8260,R8264,R8266,R8263,Q8253A,Q8253B,R8405
- L7. For test add JP860,JP8606
- L8. P88 Change D8807 PIN2 connect D8805 PIN2 to D8805 PIN1
for solve MAX17015 IC bus
- L9. P88: Add power limit circuit
- L10. P91: Add D9101,D9102,R9117 for EE request
- L11. P92 Change protect circuit to original un-cost down version

[BOM modify - EE]

- B1: P05: DNI R0538 for MoW41 Intel's recommand.
- B2: P20: DNI R2029 to disable Flash descriptor override.
- B3: P31: Change R3101 from 10K ohm to 0 ohm,
DNI C3105 for ECLCK signal quality.
- B4: P42: Change R3101 from 10K ohm to 100L ohm for +12VSUS low rating.
- B5: P60: According to "EOS of Battery SMBus" report:
P60: Change R6001,R6002,R6003 from 0 ohm to 330 ohm.
P60: Change C6006,C6007,C6008 from 47PF to 33PF.
- B6: P32: DNI R3205 for test purpose.
- B7: P32: DNI SW3201,R3202 for not support.
- B8: P66,51,21: DNI JMB360 circuit for ESI sample SATA OK.
- B9: P33: Mount D3301,D3302 for ESD protect as default setting.

[BOM modify - PWR]

- PB1: P80: Adjust loadline change R8021 from 3.92KOhm to 3.65KOhm.
- PB2: P80: Reduce transient undershoot
change R8037,R8060 from 2KOhm to 2.49KOhm.
change R8035,R8054 from 1.5KOhm to 2.21KOhm.
- PB3: P81: +3V0 from FB mode to fix mode
Mount R8133 ,un-mount R8134,change R8111 from 20K Ohm to 0 Ohm
- PB4: P82: Change L8201 from 2.2UF to 1.5UF ,un-mount CE8204 for add FB voltage
Change L8251 from 2.5UF to 1.5UF ,change CE8252 from 100UF to 220UF for reduce transient pulse
for reduce transient pulse
- PB5: P91: Change C9102 from 0.033UF to 0.1UF.
- PB6: P91: Change R9109 from 200K to 100K,adjust +1.05VM rising.
- PB7: P92: Change R9205 from 100K to 10K,adjust SYSTEM_PWRGD rising.
- PB8: P80,P81,P82,P83,P86: Change C8001,C8003,C8006,C8009,C8110,C8113,C from 100K to 10K,adjust SYSTEM_PWRGD rising.

[M52J] R1.1=> R1.2

(Release on 2009/01/12)

[Layout Changed - EE]

- L1. P66,51,21: Del JMB360 circuit for PCH SATA workable.
P21,24,40,41,42: Change CB_ from R5C833 to R5U230.
- L2. For no support AUB,delete or modify related circuit:
P03,P06,P21,P22,P23,P26,P45,P46,P47,P48,,P57,P70,P71,
- L3. Change audio circuit from ALC629 to ALC269.
- L4. For one phase bug fix:R8047: 0-->10K, R8041,2-->R8047.1, R0616: 10K-->0ohm
- L5. Layout modify for DG,Mow,EDS:
P20,P21,P22,P27,P32
- L6. Layout modify for new EC 8541 colay: P28,P30
- L7. Modify EC pin assignment for charger change:P30
- L8. P45: Add BUF_PLT_RST# to BL_EN circuit.
- L9. P45: reserverd for RF request .
- L10. P52: Add CE5202 to avoid voltage droop .
- L11. P32: Delete SW3201,R3202 for no support force-off switch.

[Layout Changed - PWR]

- PL1. P81: SYSTEM PWM change from MAX17020 to pin to pin RT8206A (for IC bug)
- PL2. P88: Charger IC change from MAX17015 to MB39A132 (for IC bug & EMI)
- PL3. P88,P60: Change BAT in jump & bead from P88 to P60
- PL4. P.86: Delete P86 +VGA_CORE
- PL5. P.80: PM_PSI# pull low follow intel schematic
- PL6. P90 Delete battery detect circuit
- PL7. P80 VID0-6, PM_DPRSLLPVR, PM_PSI# pull high power from +VTT_PWR
Change to +VTT_PCH
- PL8. P81 System +3VS,+5V voltage change from resistor adjust to fix mode
- PL9. P90 Delete battery detect circuit

[EMI request]

ITEM E:

- 1.P88. BAT : L8801, L8803 要上 for EMI
-->L6001,L6002
- 2.P29. CLK Gen. : R2935 , R2936 改 Bead 120 ohm for EMI
-->L2901,L2902
- 3.P36. SFDIF1,2_OUT : R6502 , SL3652 改 Bead 120 ohm for EMI
-->L6501,L3622
- 4.USB power : R6501 , R4505 , R5201 改 Bead 120 ohm for EMI
-->L6502,L4504,L5203
- 5.C4508 要上 for EMI
-->Mount C4508
- 6.USB I/O port & CMOS 同時 Run 會有 EMI issue,建議在 USB EHCI define
時能將這兩者分開放
-->已交換, port4=Wi-Fi/WiMax, port9=Camera.
- 7.LAN : R3306 , R3338 , R3332 , R3337 改成 Bead ; +1.05VM_LAN 上 0.1uF 靠近 R3341
-->L3301, L3303, L3302, L3304, C3314.
Note: 1.請協助確認bead是否可以只上一個,上哪一個?
2. C3313, C3314是否可以只上一個,上哪一個?
- 8.LVDS : C4506 要上 0.1uF ; LCD_PWM要上 0.1uF
-->Mount C4506, LCD_PWM預留10PF不上C4514.
- 9. P36. GND 到 GND_Audio of the short line 增加三個 (或是電阻直接改 short line)
-->SL3651, SL3652, SL3653

[BOM modify - EE]

- B1. BOM modify for DG,Mow,EDS:
P03,P21,P24,P25

[BOM modify - PWR]

- B1 P80 Change CE8806,CE8807 from mount to un-mount
- B2 P80 +Vcore output CAP from Panasonic 470UF/2V 4.5m Ohm change to Panasonic 330/2V 6m Ohm
- B3 P80 Change Q8007,Q8001,Q8005,Q8000 from SI4686BDY to SI7170DP
Change Q8002,Q8004 from SI4634BDY to SI7686DP
- B4 P81 Change CE8101,CE8102 from CHEMICON 220UF/6.3V 10m Ohm to CHEMICON 150UF/6.3V 19m Ohm
- B5 P82 Change CE8204,CE8207 from Panasonic 330/2V 6m Ohm to Panasonic 220/2V 15m Ohm
- B6 P82 Change CE8252 from CHEMICON 330UF/4V 10m Ohm to CHEMICON 560UF/2.5V 10m Ohm
- B7 P83 Change CE8305 from CHEMICON 330UF/4V 10m Ohm to CHEMICON 560UF/2.5V 10m Ohm
- B8 P91 Change Q9101 from SI4634DY Rds(on)=6.7mOhm to IRF8707PBF Rds(on)=17.5mOhm
- B9 P91 Change C9101, C9103, C9105, C9106, C9108, C9110, C9122 from mount to un-mount

[M52J] R1.2=> R1.21

(Release on 2009/03/12)

- B1. For team signal quality test:
P21 Change RX2103, RX2104 from 0ohm to 22ohm
P24 Change R2404, R2406 from 22ohm to 33ohm
- B2. P47 R4708:100K-->1K for bug fix(0.3V-->3V).

[M52J] R1.21=> R1.3

(Release on 2009/04/20)

- L1. P29,25: Change clock GEN: ICS9PLR362-->ICS9PLRS3197 for corechip.
- L2. P33,34,21,25: Change LAN:HANKSVILLE-->R81831 for corechip.
- L3. P18: Delete M2 solution and modify description.
- L4. P19: Delete VID controller.
- L5. P30: Fix error: TP_DAT,TP_CLK pull up +3VA_EC-->+5V5.
- L6. P24,53,P64: For PCH SKU compatible:
TV_Turner: port 6-->port4.
WLAN: port 4 -->port8.
- L7. P20,21,24,25,67 delete PCH XDP.
- L8. P25 for PCH GPIO define change:
P25. GPIO15,GPIO28 exchange.
- L9. P53: Fix error for WLAN_ONH.
- L10. R6741,R6742 move to R2621,R2622 for some project without BRAIDWOOD.
- L11. P61: D6101 change from RB751V to BAT54C.
- L12. P30,P56: for touch sensor board ver 1.2.
Move CAP_ACK#(GPB7)-->CAP_ACK_A#(GP16),add CAP_ACK_B#
,delete RS524,delete Q5602B,Q5604B,RS626B,add SL3005,SL3006.
- L13. For N10P-GS VGA card: (Layout impedance change).
P48:Move D4802 from net HDMI_HPD_CON to HDMI_HPD.
P48:Add R4809-R4816,Q4802 for HDMI termination.
- L14. P24,P30: For PCI_CLK layout guide update.
- L15. P21,P27:Disable Intel LAN.
P27. Delete R2723,net +1.05VM_LAN.
- L16. Change ESD diode to IP4223 for cost down.
D3106,D4301,D4503,D4605,D4701,D4702,D4703,D5201,D6501,D6601
- L17. For iAMT disable.
P30,P31,P92. Delete net ME +VM_PWRGD,D9202,R3070#R3105,R3108#
P31.Delete U3101(IT8301E) block
P30.Delete R3065,R3067,R3068,R3072,net EGAD,EQCS,EGCLK,EGCLK_EC.
P57.Delete Q5708,R5709,R5716,R5717,Q5710,R5718,R5719,no connect Q5707B.
P81.Delete net ME_PM_SLP_LAN#,SLP_LAN_PWR,R8131,TP8117
P81.Delete net ME_SLP_M_EC#,SLP_M_PWR,R8129,JP8116
P84.Delete +3VM load switch block,ME +VM_PWRGD block.
P22.Delete ME_PM_SLP_M# to PM_SUSB#,delete R2254,R2238,Add T2208.
P22.Delete net ME_PM_SLP_LAN#,R2254,R2257,add T2207.
Connect ME_PWROK_PCH to PM_PWROK_PCH.
Delete R2272#,R2268,D2204#,R2271.
P27. Delete net +1.05VM_ORG_R11..4),delete R2736,R2727,R2738,R2739.
Connect +1.05VS to +1.05VM_ORG.
Connect +3VS to +3VM via JP2705.
- L18. For EC8541:
P28: Delete R2848,R2856,net PM_RSMRST#
Add Q2804,Q2805,R2830,R2835,R2836,R2838.
P28: Others: please see the description.
- L19. net connection change.(for possible costdown)
PM_PWROK_PCH:D2202.2 -->D2202.1
PM_RSMRST#_PCH:D2203.1 -->D2202.2
R2275:0ohm -->1Kohm
- L20. P20,30.connect HDA_DOCK_EN# to EC for BIOS request
- L21. P7,P37 change XDP from 60pin to 24pin SFF.
- L22. P56: prevent touch sensor board leakage.
Change U5601 net SMB1_CLK-->SMB1_CLK_S,SMB1_DAT-->SMB1_DAT_S
- L23. For component kinds down:P5201--P6501,F4801--F4502
- L24. P45. Delete F4502 for costdown.
- L25. P28. Fix SPI circuit for EC8541.

- B1. P36. Change ALC269 From A5 to VA6(P/N: 026611005006).
- B2. P30. Change U3001 from IT8512E to IT8541E.
- B3. P18. Change Vref solution from M1 to M3.
DNI R1801,R1804,Mount R1805,R1806.
- B4. P67. For no support Braidwood:
DNI R6704,R6740.
- B5. Intel DG update:
P03. change R0320 & R0321.
- B6.P70. correct name to match page rule:
C7709-->C7709, C7010,C7011,C7012,C7013,C7014,C7705.
T7006,T7007,T7008
- B7.P70. DNI R7022, mount R7023 for VGA timing.
- B8.P50. Change U5002 from G781-1 to G781 for SMBUS addr.
- B9.P21. DNI X2101,C2101,C2102,R2151 for PCH only support BTM mode currently.
- B10. Improve clock ppm:
P29: C2907,C2908: 24pF-->27pF.
P40: C4040,C4066: 22pF-->27pF.
- B11. Add R3205 support thermal protection.

[M52J] R1.3=> R1.32

(Release on 2009/06/03)

- B1. Change Connector for ME request.
J4501:12G170010409-->12G170010408
J4801:12G241101928-->12G241101939
- B2. Change MOS 2N7002 P/N to 07G005000313 for RD pool
Q0301,Q2001,Q2901,Q3902B,Q4301B,Q4402,Q4503,Q4802,Q6102#.
- B3. Change U2801,U2802 for vendor EOL.
05G00160F010-->05G00160G010
- B4. Change EC from 8541 to 8512.
DNI C2804,R2848,R2855,R2856,U2803,R2857,R2858,R2859,R2860,R2861,R3002,R3003,R3004,R3005
Mount R2846,R2853,R2854,R2827,R2828,U3003,R3053,R3043,C3019
Change U3003: 05G001405010-->05G00120A010.
Change U3001: 06G042025010-->06G042025012.
- B5. WW22 MOW,Implement M1 & M3 method: mount R1801,R1804.
- B6. WW20 MOW,change R2029 from 100K# to 1K#.

[M52J] R1.31=> R1.32

(Release on 2009/06/05)

- B1. P28. DNI U2802 for costdown.
- B2. P30. Change EC from 8512 to 8502 for costdown.

[M52J] R1.32=> R2.00

(Release on 2009/07/02)

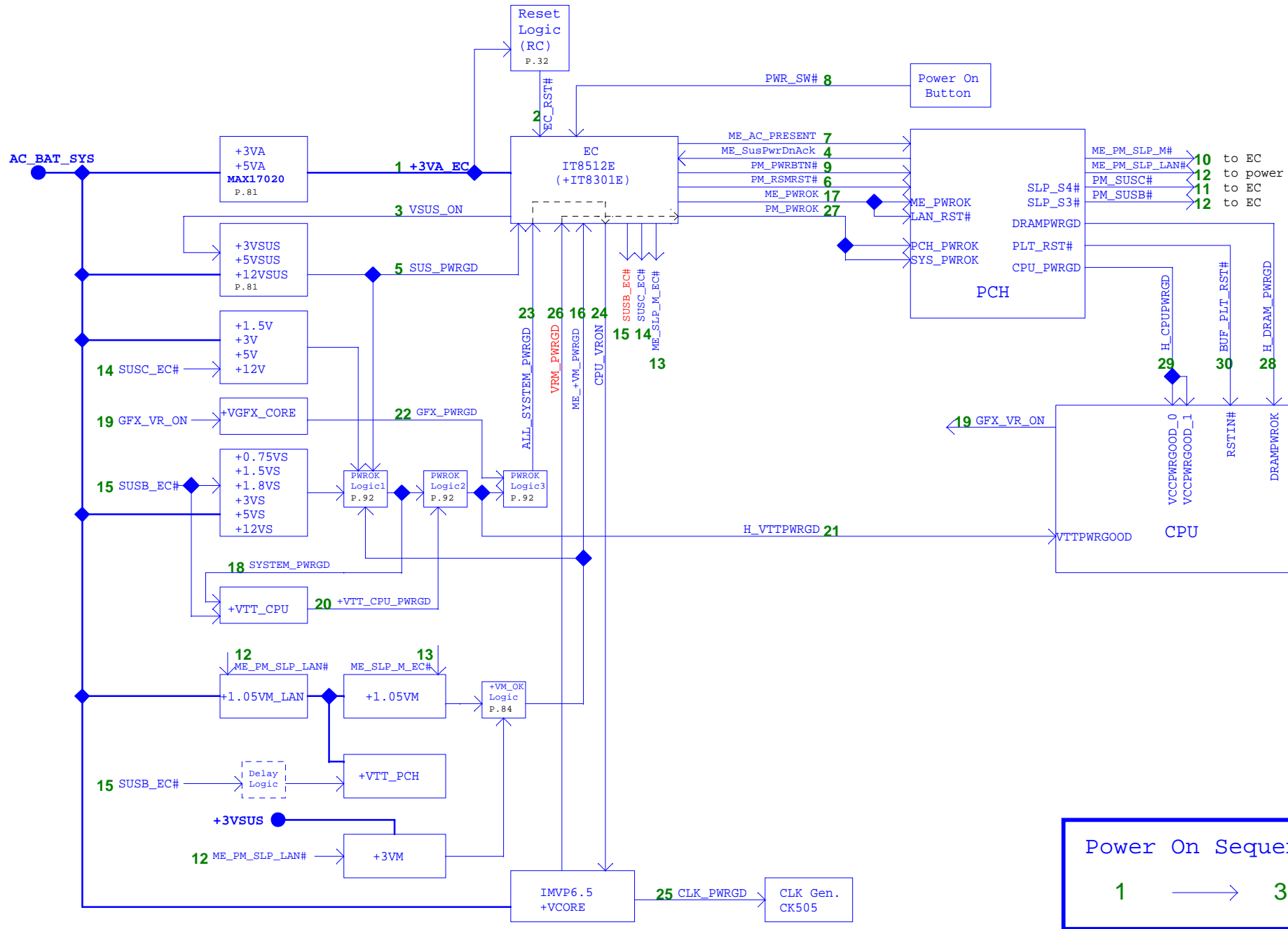
- L1. P28. ChangeJ2801.1 power for dediprog flash.
- L2. P47. ChangeR4701 10K-->100K,add R4709 to fix DP hot--plus issue.
- L3. P20. Fix error that HDA_DOCK_EN# can't pull to GND directly.
- L4. P36.P20. Remove PC beep circuit for design IP change.
- L5. P03,06,20,27,30,32,56,60,65:Add test point for factory request.
- L6. P45: Change C4501 0.1uF(0402)-->0.22uF(0603) for LCD power timing.
- L7. P37: Change J3701 12G171000049-->12G17100004F to fix ME bug.
- L8. P53: Change J5302 12G030000524-->12G03011052X for EOL.
Change H5303 & H5304 13G021036001-->13G023600110 to match 12G03011052X.
- L9. P43: Change U4301 06G0300053010-->06G030091110 for design IP.
- L10. For EMI request:
Add C5617,C2618,C2736,C2748,C2749,C4509,C4510,C4519#,C5101,Mount C3406.
USB_PNO, USB_PMI /UJ6501 預留 choke
USB_PN2,3,5 預留 0 ohm
- L11. For EC request pin assignment:
GPB.2 (ME_AC_PRESENT)/GP.0 (ME_SusPwrDnAck)/GPI.4 (PCH_TEMP_ALERT#)
Change GPF.0 (PCH_SPI_OV) to GPF.7
- L12. For Touch sensor default state:
Del RN3007,change CAP_ACK_A#,CAP_ACK_B# pull up to +3VS(RN3008).
- L13. Change C2101#(27PF) to ohm to meet Calpella DG R1.6,Page 369.
- L14. P29: Colay clock GEN. 9LRS3197/9LVS3162.
- L15. Fix thermal policy!
P25. Move & mount R2501,add R2505
P25. Follow designip.
P50. Use GMT G709 as thermal protection.
- L16. P45. Reserve soft-start circuit to prevent LCD inrush current.
- L17. P65. Add C6514,C6515 for EMI request(prevent TV noise).
- L17. P45,P83: change JP4599 for lead part.

- B1. P46. Change C4601-C4601 10PF-->5PF for CRT signal quality.
- B2. P45. Change J4501:12G170010409-->12G170010408 for footprint not compatible.
- B3. P23. ChangeR2321 from 1Kohm,0.5#-->1Kohm,5# for DAC_IREF not used.
- B4. P58. Move page 92 to page 98, rename components.
- B5. P06. Delete unused nets.
- B6. P20,28: Change R2032,R2033,R2837,R2840,R2841 to 33ohm to fix dediprog checksum error issue.
- B7. P52: Change L5203 05G012080023--> for common part.
- B8. P52: Change C6508,C6509 100pF-->1000pF for EMI request(prevent TV noise).
- B9. P24: DNI R2414 for no braidwood.

[M52J] R2.00=> R2.01

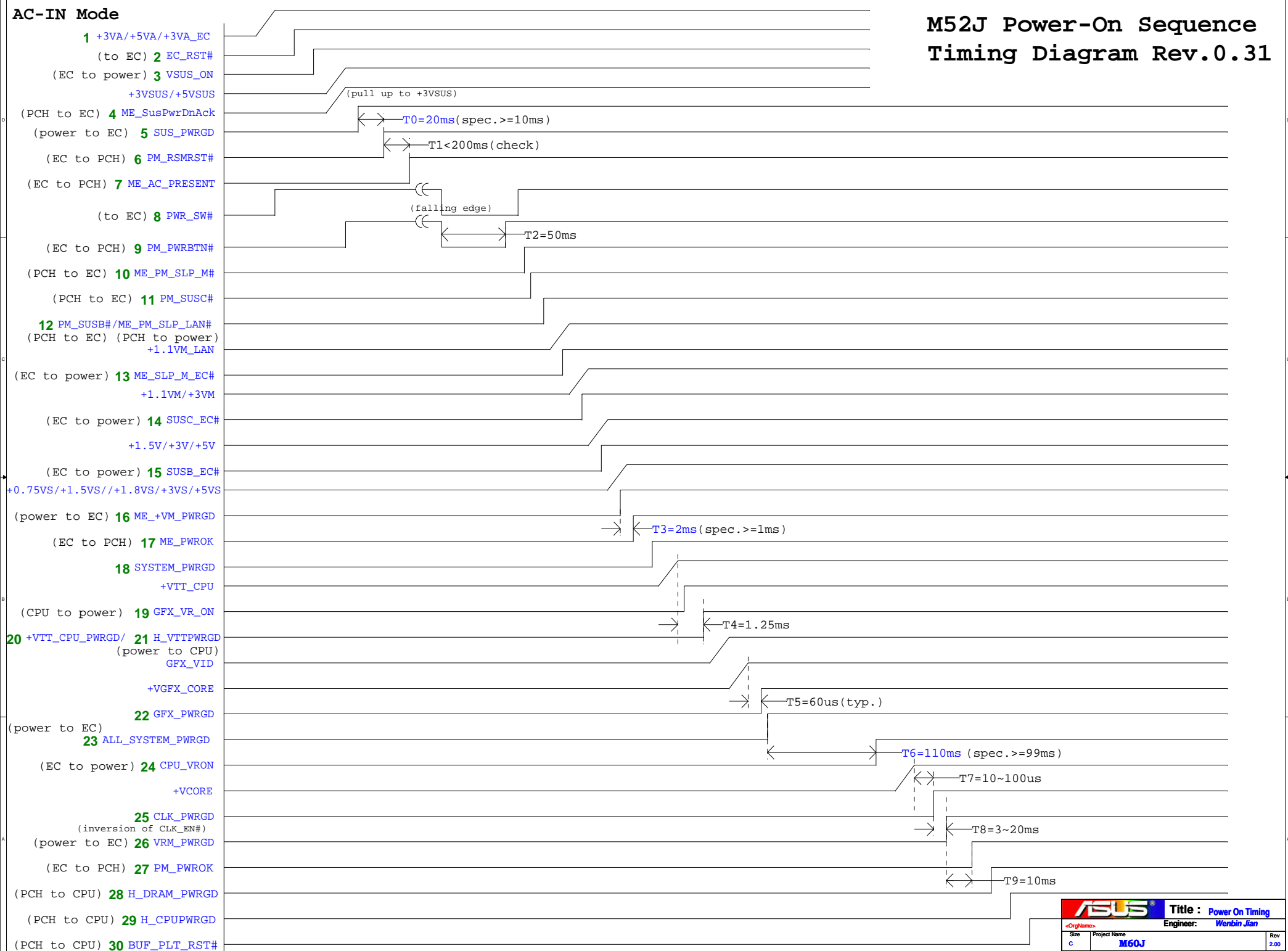
(Release on 2009/07/02)

- B10. P29,P28: For only one SPI ROM:
DNI R2834,R2832,C2803,R2828,R2827,R2852,R2850,R2846,R2851,R2823,R2854,R2849,R2853,R2033
- B11. P20,P67:remove support of PCH JTAG
P00: R2034,R2035,R2036,R2037,R2038,R2039,R2040,R2041
P67: R6702,J6701,R6721,R6722,R6723,R6724



Power On Sequence
1 → 30

M52J Power-On Sequence Timing Diagram Rev.0.31



M52J Power-On Sequence Timing Diagram Rev.0.31

DC-IN Mode

- 1 +3VA/+5VA/+3VA_EC
(to EC) 2 EC_RST#
(to EC) 3 PWR_SW#
- (EC to power) 4 VSUS_ON
+3VSUS/+5VSUS
(PCH to EC) 5 ME_SusPwrDnAck
(power to EC) 6 SUS_PWRGD
(EC to PCH) 7 PM_RSMRST#
(EC to PCH) 8 ME_AC_PRESENT
(EC to PCH) 9 PM_PWRBTN#
(PCH to EC) 10 ME_PM_SLP_M#
(PCH to EC) 11 PM_SUSC#
- 12 PM_SUSB#/ME_PM_SLP_LAN#
(PCH to EC) (PCH to power)
+1.1VM_LAN
(EC to power) 13 ME_SLP_M_EC#
+1.1VM/+3VM
(EC to power) 14 SUSC_EC#
+1.5V/+3V/+5V
(EC to power) 15 SUSB_EC#
+0.75VS/+1.5VS//+1.8VS/+3VS/+5VS
(power to EC) 16 ME_+VM_PWRGD
(EC to PCH) 17 ME_PWROK
- 18 SYSTEM_PWRGD
+VTT_CPU
(CPU to power) 19 GFX_VR_ON
- 20 +VTT_CPU_PWRGD/ 21 H_VTTPWRGD
(power to CPU)
GFX_VID
+VGFX_CORE
- 22 GFX_PWRGD
(power to EC)
- 23 ALL_SYSTEM_PWRGD
(EC to power) 24 CPU_VRON
+VCORE
- 25 CLK_PWRGD
(inversion of CLK_EN#)
(power to EC) 26 VRM_PWRGD
(EC to PCH) 27 PM_PWROK
- (PCH to CPU) 28 H_DRAM_PWRGD
(PCH to CPU) 29 H_CPUPWRGD
(PCH to CPU) 30 BUF_PLT_RST#

