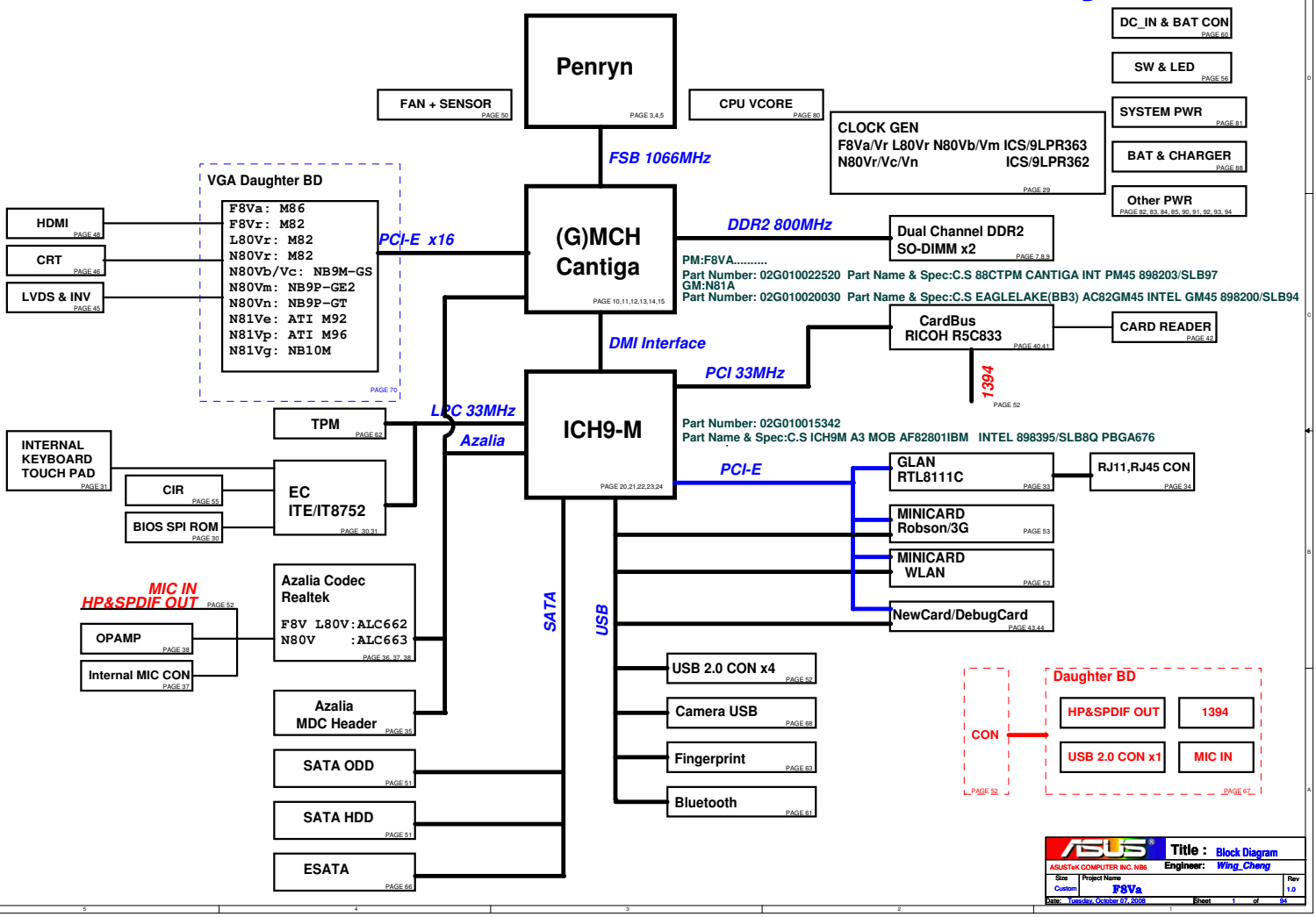
F8V L80V N80V N81 Montevina Block Diagram



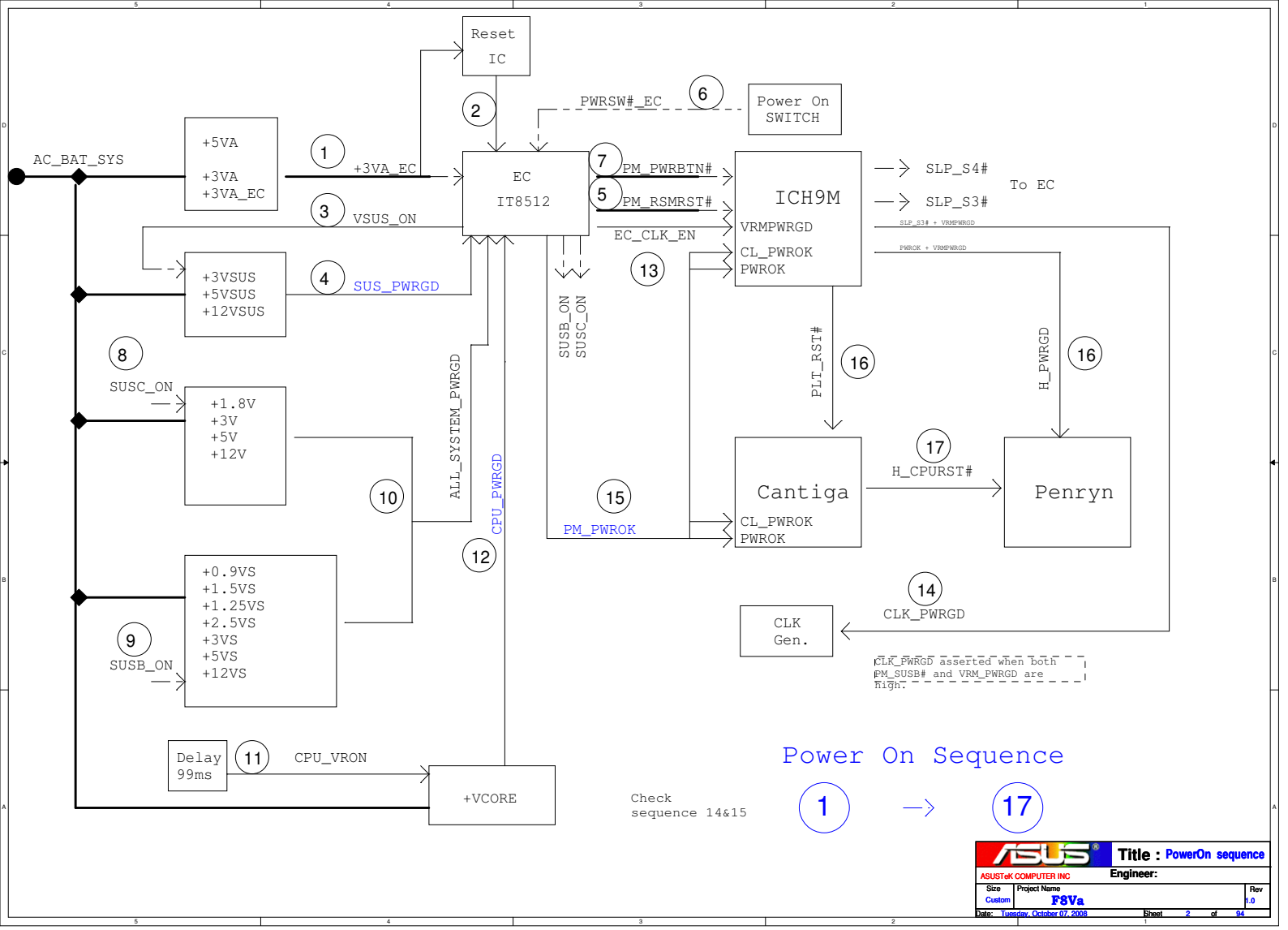
ASUSTeK COMPUTER INC. NB6

Title : Block Diagram

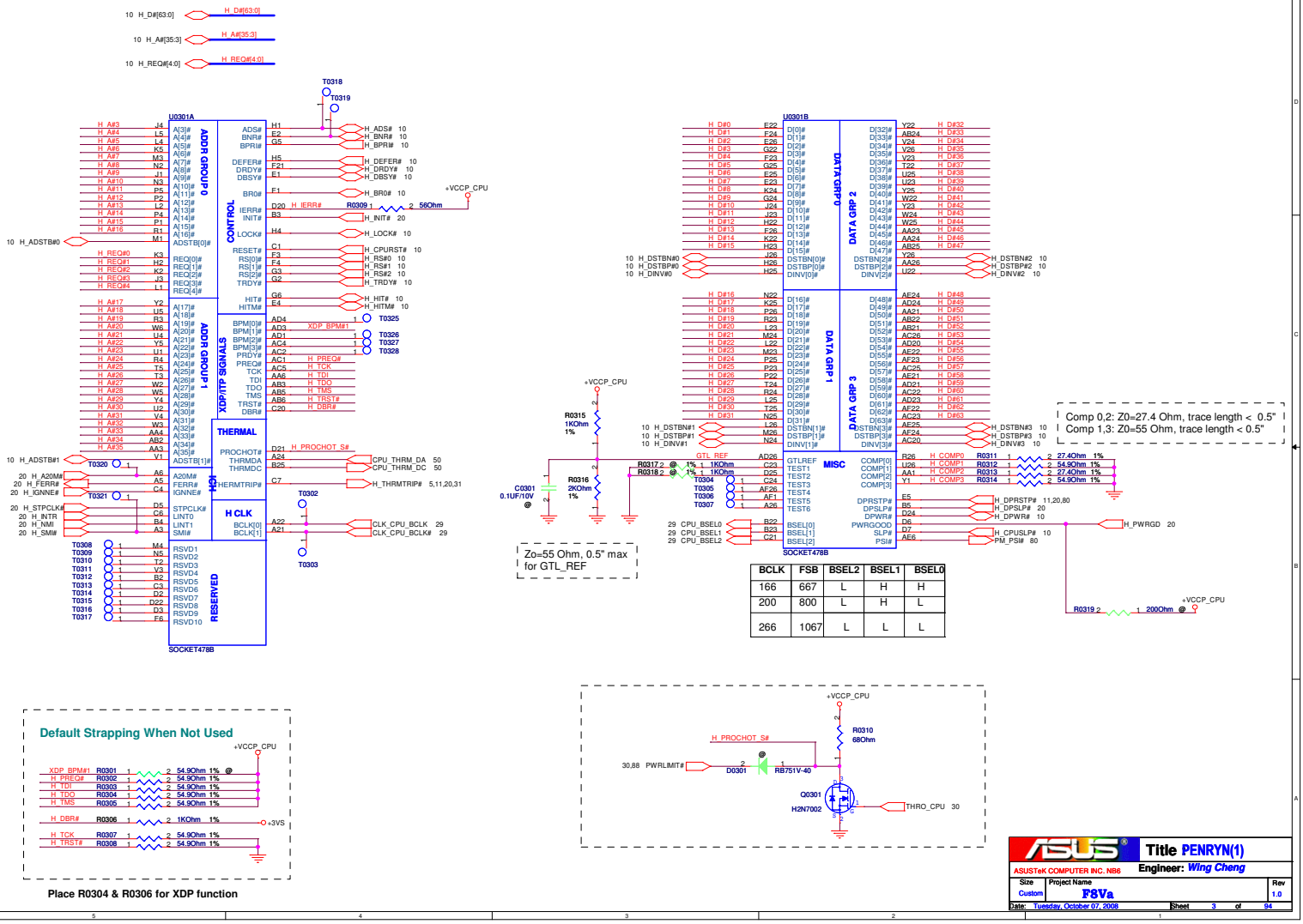
Engineer: Wing_Cheng

Size	Project Name	Rev
Custom	F8Va	1.0

Date: Tuesday, October 07, 2008 Sheet 1 of 94



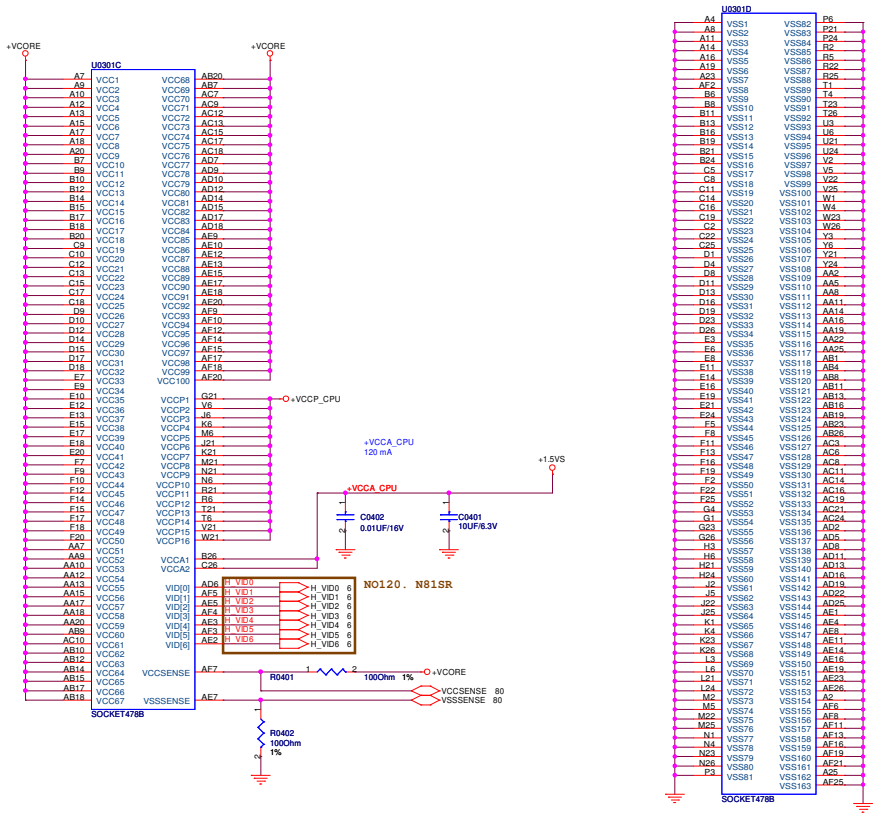
ASUSTeK COMPUTER INC		Title : PowerOn sequence	
		Engineer:	
Size: Custom	Project Name: F8Va		Rev: 1.0
Date: Tuesday, October 07, 2008		Sheet 2 of 94	



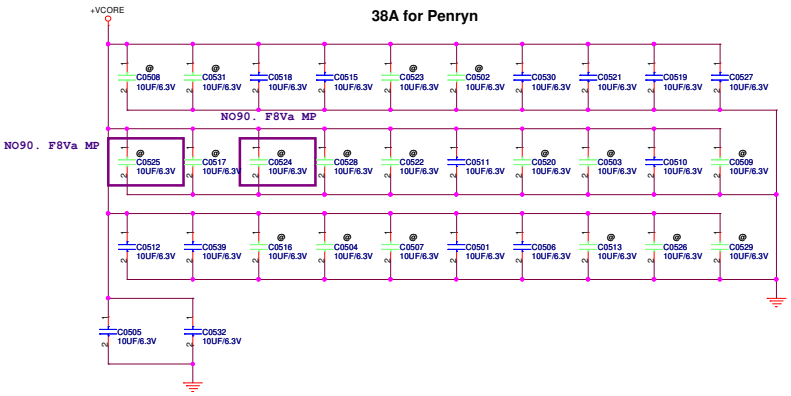
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

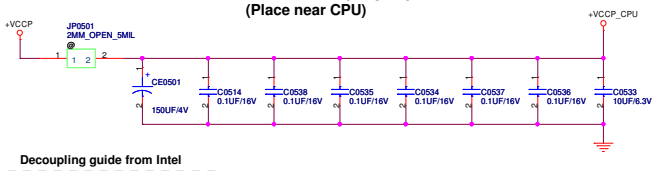
Place R0304 & R0306 for XDP function

Title	PENRYN(1)
ASUSTeK COMPUTER INC. NB6	Engineer: Wing Cheng
Size: Custom	Project Name: F8Va
Rev: 1.0	
Date: Tuesday, October 07, 2008	Sheet 3 of 94



Title :	Penryn CPU (2)
ASUSTeK COMPUTER INC. NB6	Engineer: Wing Cheng
Size: Custom	Project Name: F8Va
Rev:	1.0
Date: Tuesday, October 07, 2008	Sheet 4 of 94





Decoupling guide from Intel

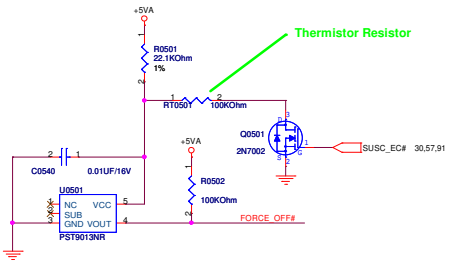
VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

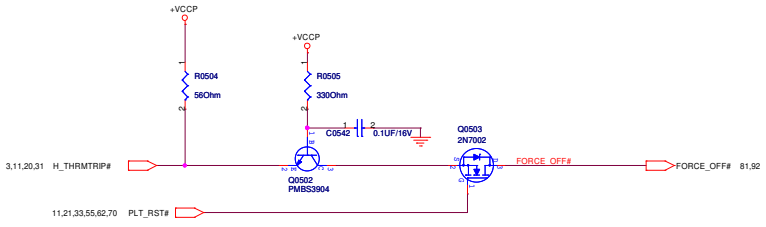
+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F3S: 10UF *16*
*A7S: 10UF *10 ....11/17*
V1V: ?
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *4*
V1V: ?

F8S

VCORE	10uF/10V	* 32pcs
	330uF/2V	* 0pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU
	10uF/10V	* 1pcs
4/20(F8S)		
VCORE	10uF/10V	* 16pcs

? DEGREE C
THERMAL PROTECTION
place in the path of a draft



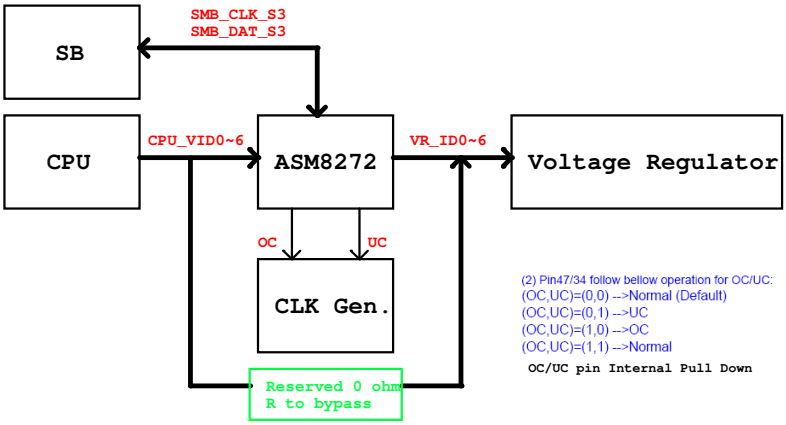


Thermal Trip signal (From CPU to ICH-9M and sequence)

ASUSTeK COMPUTER INC. NB6		Title : CAPS	
		Engineer: Wing Cheng	
Size: Custom	Project Name: F8Va		Rev: 1.0
Date: Tuesday, October 07, 2008		Sheet 5 of 94	

Block Diagram

NO120. N81SR



(2) Pin47/34 follow bellow operation for OC/UC:
(OC,UC)=(0,0) -->Normal (Default)
(OC,UC)=(0,1) -->UC
(OC,UC)=(1,0) -->OC
(OC,UC)=(1,1) -->Normal

OC/UC pin Internal Pull Down

Schematics

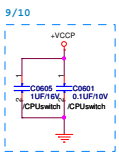
NO143. N81SR

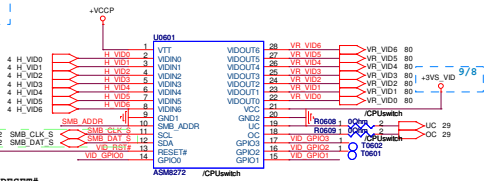
Strapping

SMBus Select

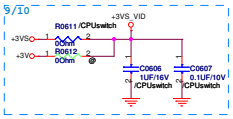
0:37h
1:4Eh

GPIO2	GPIO1	GPIO0	Function
X	0	0	Push-pull IO of VIDIN
X	0	1	Enable VIDIN input termination resistor
X	1	0	Diamondville_DT convert to IMVP6
0	1	1	Test mode
1	1	1	Test mode





ASM8272 used PWR RESET#



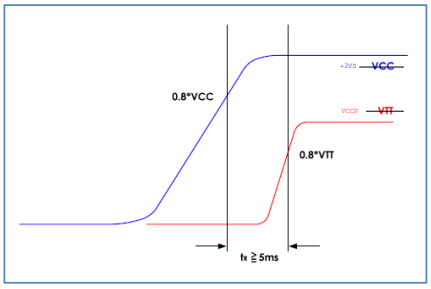
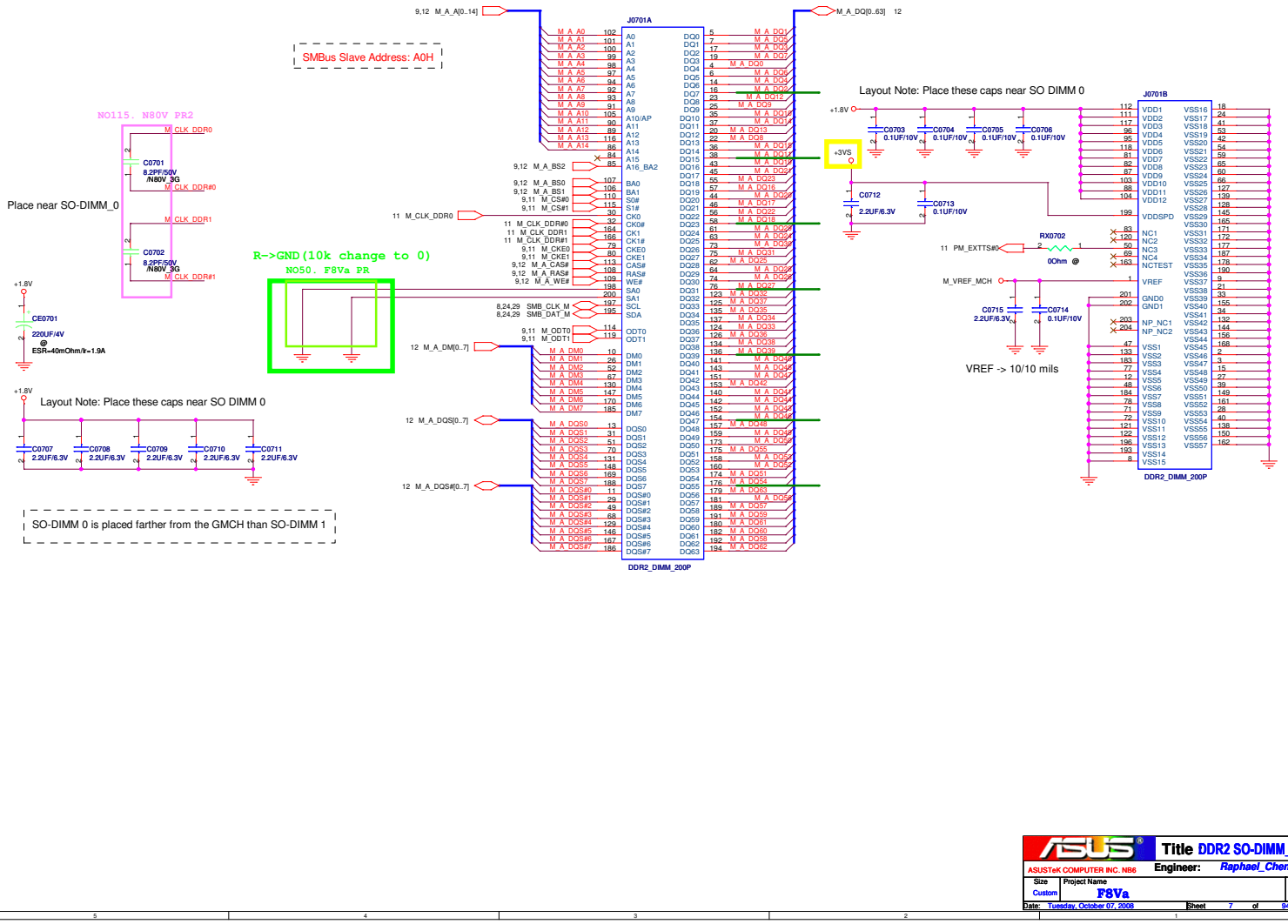
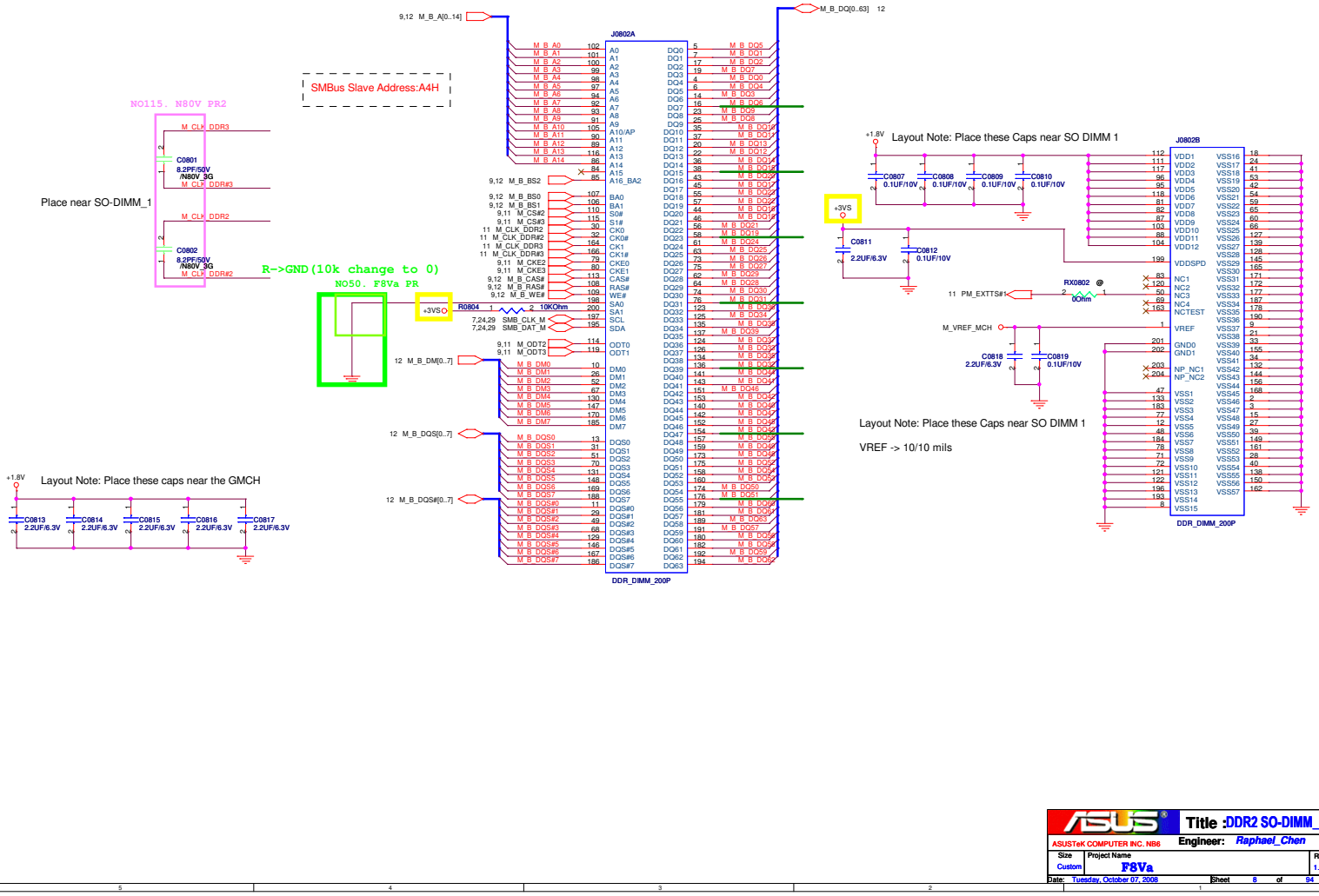


Figure 4: Power Sequence

Title :	NB_965PM(DMI/CFG)
ASUSTeK COMPUTER INC. NB1	Engineer: Kenny Chu
Size: Custom	Project Name: N81
Rev: 0.1a	
Date: Tuesday, October 07, 2008	Sheet 6 of 52



ASUSTeK COMPUTER INC. NB6	Title	DDR2 SO-DIMM_0	
	Engineer:	Raphael_Chen	
Size: Custom	Project Name: F8Va		Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 7 of 94		



ASUSTeK COMPUTER INC. NB6	Engineer: Raphael_Chen	
Size: Custom	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 8 of 94	

Title :DDR2 SO-DIMM_1

+0.9VS

NO50. F8Va PR

M_VREF_MCH

7,8,11,83 0.9V_VTT_REF

C0930 0.1UF/10V

M51VA

+1.8V

+5V

R0903 10KOhm @

C0903 0.1UF/10V @

U0901

LMV321AS5X_NL @

C0902 0.1UF/10V @

R0905 10KOhm @

R0904 0Ohm @

+0.9VS +0.9V change to +0.9VS

C0904 C0905 C0906 C0907 C0908 C0909 C0910 C0911 C0912 C0913 C0914 C0915 C0916 0.1UF/10V @

Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS +0.9V change to +0.9VS

C0929 C0917 C0918 C0919 C0920 C0921 C0922 C0923 C0924 C0925 C0926 C0927 C0928 C0901 0.1UF/10V @

M_A_A[0..13] 7,12

M_A_BS[0..2] 7,12

M_A_CAS# 7,12

M_A_RAS# 7,12

M_A_WE# 7,12

M_B_A[0..13] 8,12

M_B_BS[0..2] 8,12

M_B_CAS# 8,12

M_B_RAS# 8,12

M_B_WE# 8,12

M_CS#[0..3] 7,8,11

M_ODT[0..3] 7,8,11

M_CKE[0..3] 7,8,11

+0.9VS +0.9V change to +0.9VS

RN0901A M_A_A7
RN0901B M_A_A4
RN0901C M_A_A2
RN0901D M_A_BS1
RN0901E M_A_RAS#
RN0901F M_A_A0
RN0901G M_A_A13
RN0901H M_CS#0

RN0902A M_CKE0
RN0902B M_A_BS2
RN0902C M_A_A12
RN0902D M_A_A9
RN0902E M_A_A8
RN0902F M_A_A5
RN0902G M_A_A3
RN0902H M_A_A1

RN0903A M_A_A10
RN0903B M_A_BS0
RN0903C M_A_WE#
RN0903D M_A_CAS#
RN0903E M_CS#1
RN0903F M_ODT1
RN0903G M_ODT0
RN0903H

RN0904A
RN0904B M_CKE3
RN0904C M_B_A0
RN0904D M_B_BS1
RN0904E M_B_RAS#
RN0904F M_CS#2
RN0904G M_ODT2
RN0904H M_B_A13

RN0905A M_B_A11
RN0905B M_B_A9
RN0905C
RN0905D M_B_A2
RN0905E M_B_A4
RN0905F M_B_A7
RN0905G M_B_A6
RN0905H M_B_A3

M_B_A14 8,12

RN0906A M_CKE2
RN0906B M_B_BS2
RN0906C M_B_A12
RN0906D M_B_A8
RN0906E M_B_A5
RN0906F M_B_A1
RN0906G M_B_A10
RN0906H M_B_BS0

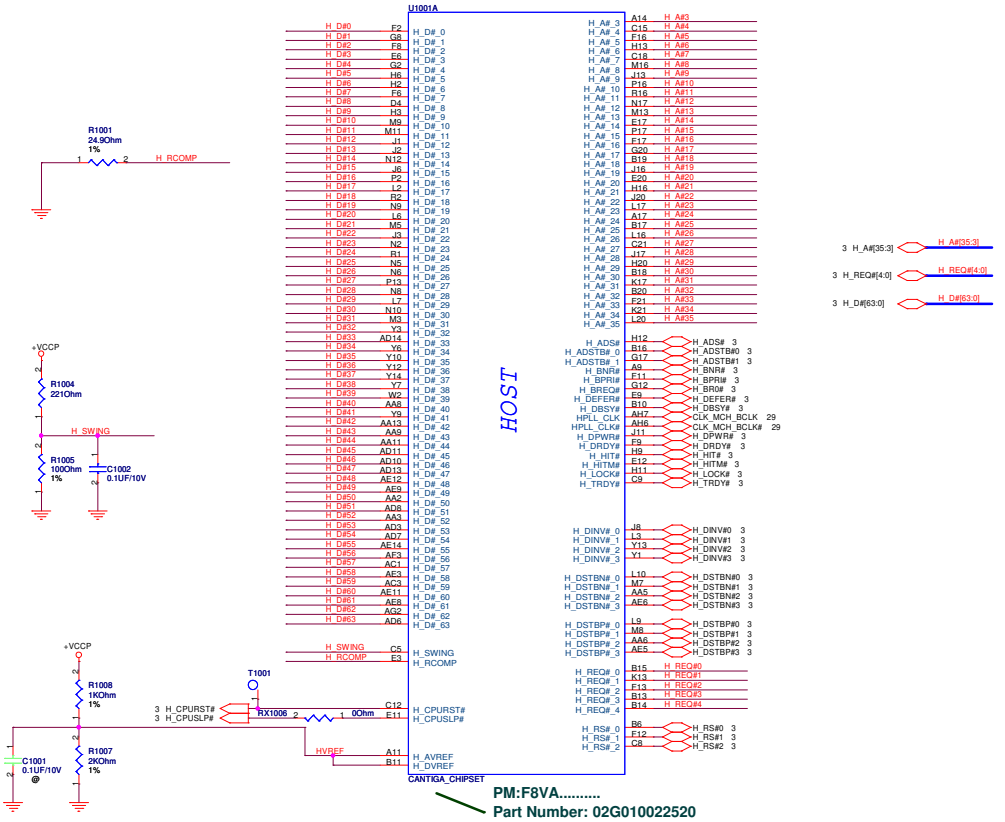
CHECK A14 WHY ?

RN0908A M_B_WE#
RN0908B M_B_CAS#
RN0908C M_CS#3
RN0908D M_ODT3

RN0909A M_A_A6
RN0909B M_CKE1
RN0909C M_A_A11
RN0909D

M_A_A14 7,12

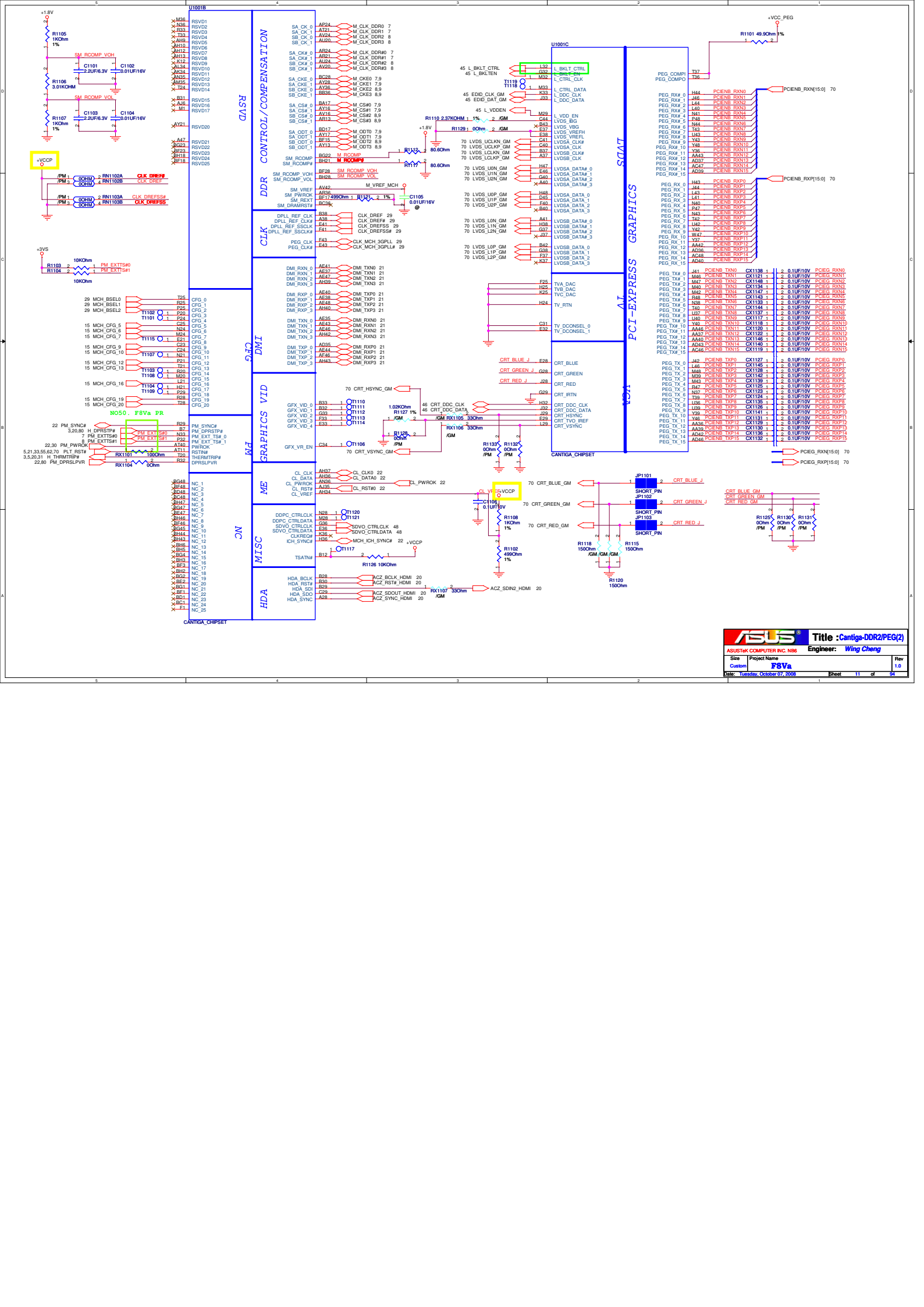
ASUSTeK COMPUTER INC. NB6	Title DDR2 termination	
	Engineer: Wing Cheng	
Size: Custom	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 9 of 94	

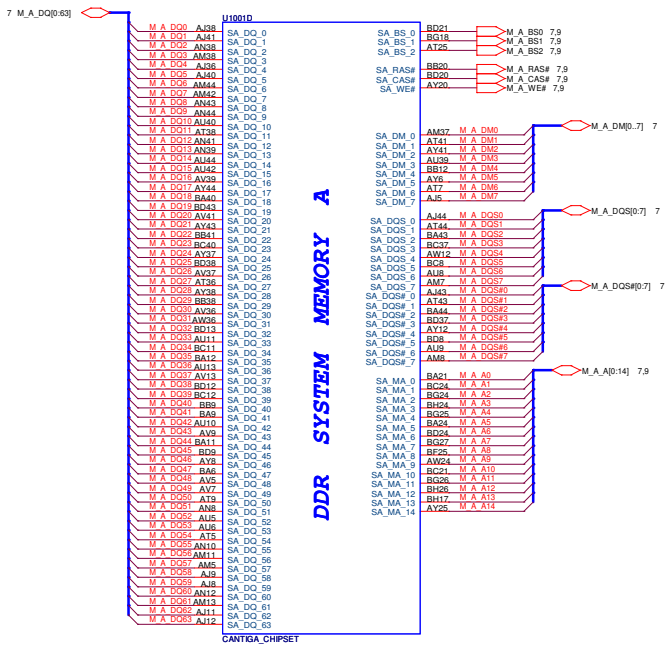


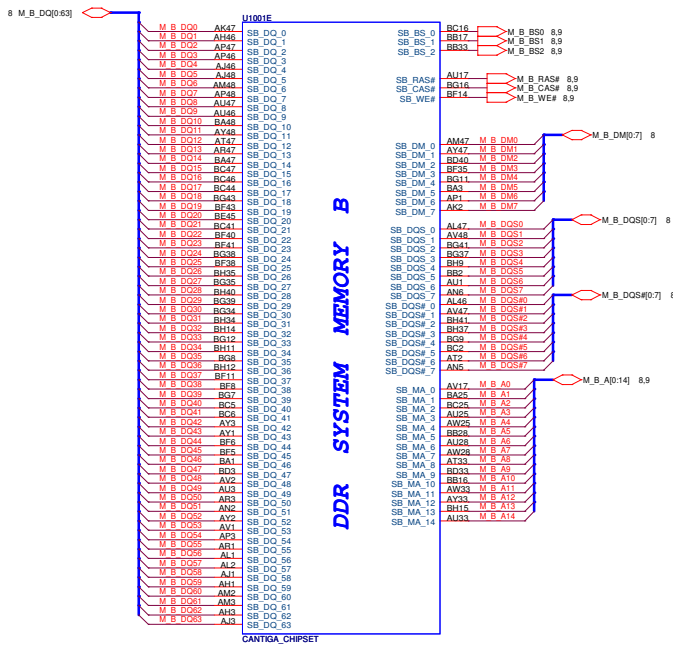
Cap 0.1uF within 100 mils from GMCH

PM:F8VA.....
Part Number: 02G010022520
Part Name & Spec:C.S 88CTPM CANTIGA INT PM45 898203/SLB97
GM:N81A
Part Number: 02G010020030
Part Name & Spec:C.S EAGLELAKE(BB3) AC82GM45 INTEL GM45 898200/SLB94

ASUSTeK COMPUTER INC. NB6	Title : Cantiga – CPU (1)	
	Engineer: Wing Cheng	
Size: Custom	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 10 of 94	


U1001B
U1001C
RSVD
CONTROL/COMPENSATION
DDR
CLK
CFG
DMI
GRAPHICS VID
PM
ME
MISC
HDA
NC
SDVT
PCI-EXPRESS GRAPHICS
DDI
LVDS
CRT
CANTIGA_CHIPSET
+1.8V
+VCCP
+3VS
+VCC_PEG
SM_RCOMP_VOH
SM_RCOMP_VOL
CLK_DREF#
CLK_DREF
CLK_DREFSS#
CLK_DREFSS
PM_EXTTS#0
PM_EXTTS#1
NO50. F8Va PR
PCIENB_RXN[15:0] 70
PCIENB_RXP[15:0] 70
PCIEG_RXN[15:0] 70
PCIEG_RXP[15:0] 70
Title :Cantiga-DDR2/PEG(2)
ASUSTeK COMPUTER INC. NB6
Engineer: Wing Cheng
Project Name
F8Va
Rev
1.0
Date: Tuesday, October 07, 2008
Sheet 11 of 94





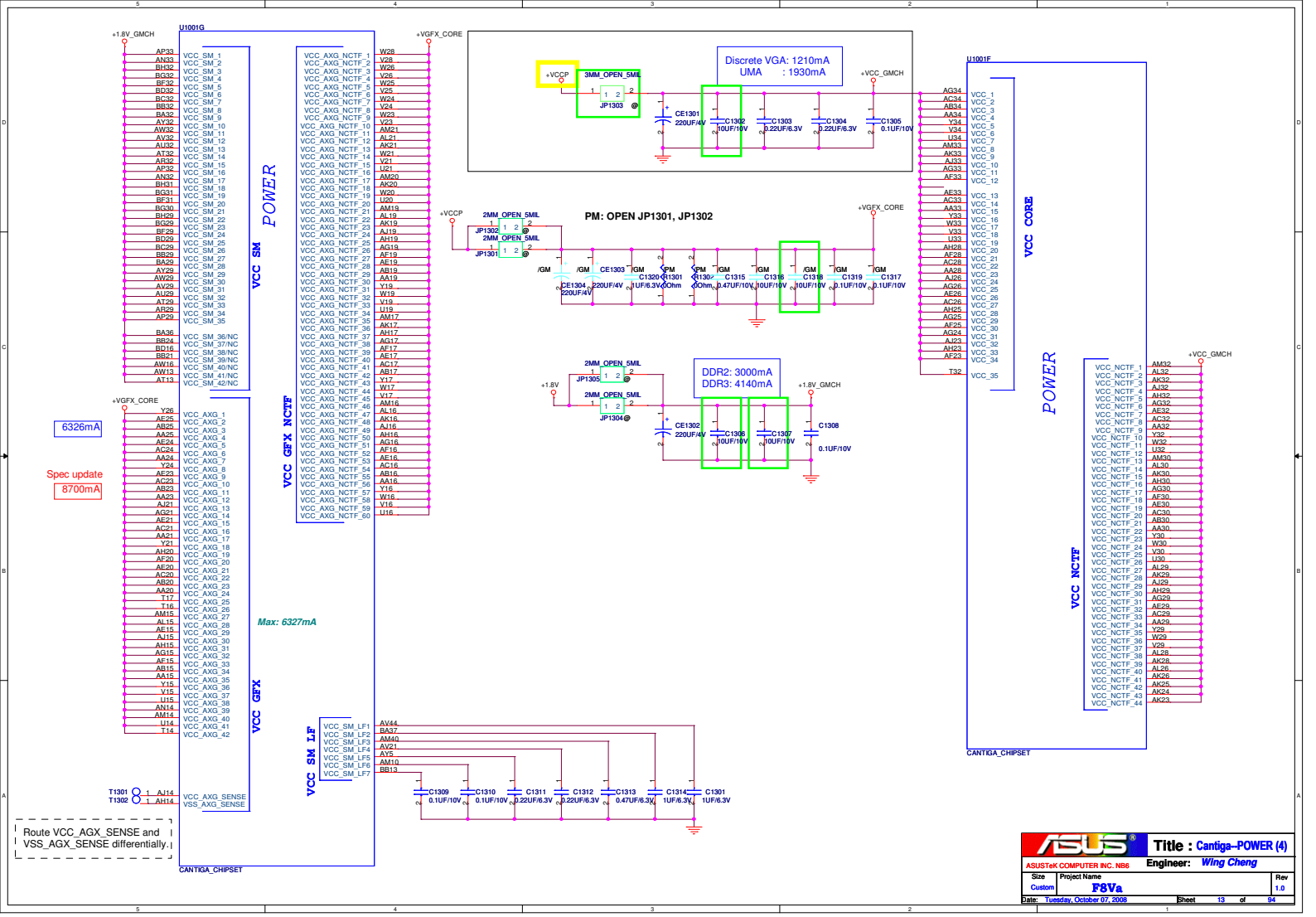
ASUSTeK COMPUTER INC. NB6

Title : Cantiga--DDR2 bus (3)

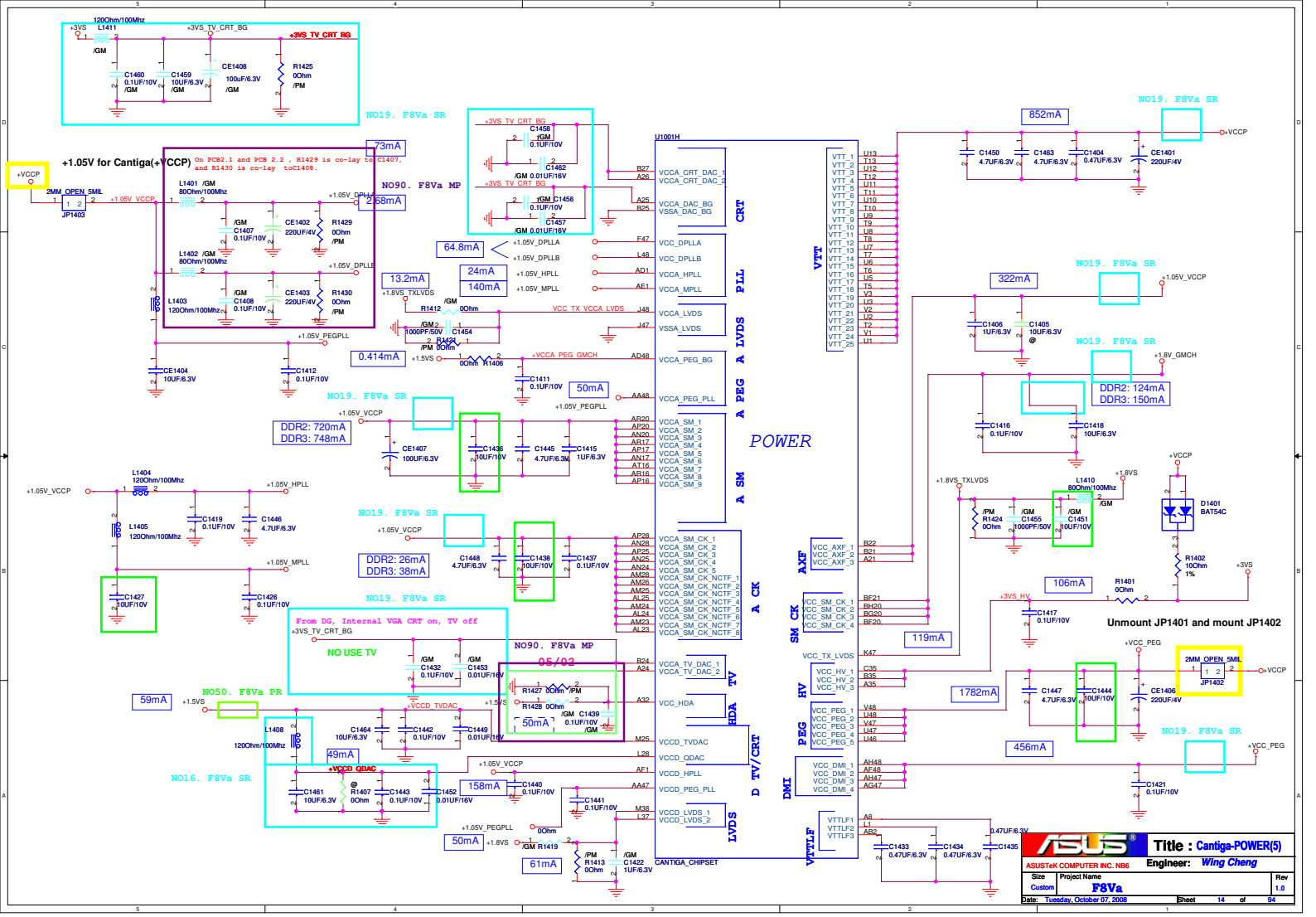
Engineer: Wing Cheng

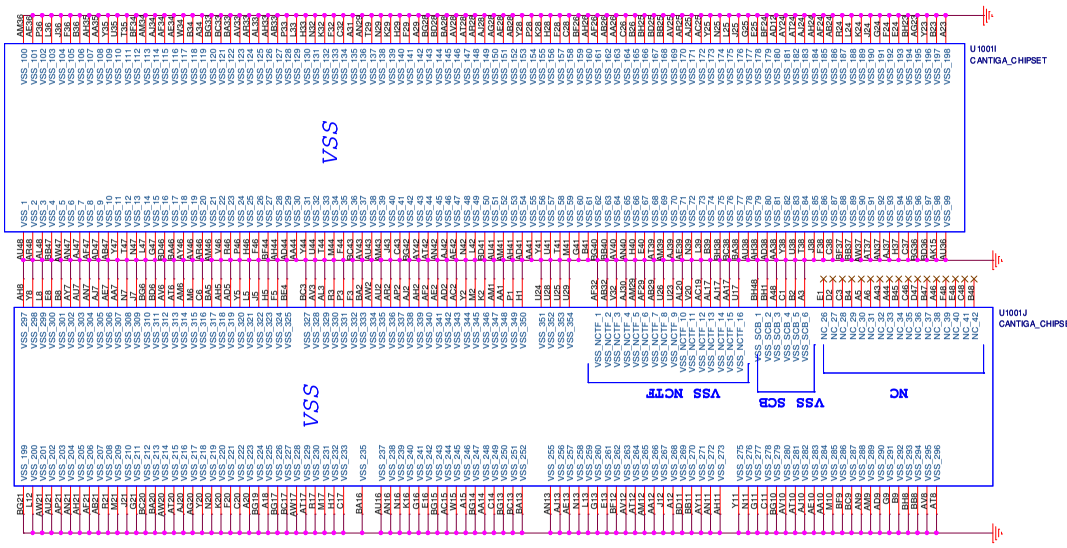
Size	Project Name	Rev
Custom	F8Va	1.0

Date: Tuesday, October 07, 2008 Sheet 12 of 94



ASUSTeK COMPUTER INC. NB6	Title : Cantiga--POWER (4)	
	Engineer: Wing Cheng	
Size: Custom	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 13 of 94	


+1.05V for Cantiga(+VCCP)
On PCB2.1 and PCB 2.2 , R1429 is co-lay to C1407, and R1430 is co-lay toC1408.
NO19. F8Va SR
NO90. F8Va MP
NO16. F8Va SR
NO50. F8Va PR
73mA
2.68mA
64.8mA
24mA
140mA
13.2mA
0.414mA
50mA
DDR2: 720mA
DDR3: 748mA
DDR2: 26mA
DDR3: 38mA
From DG, Internal VGA CRT on, TV off
NO USE TV
59mA
49mA
158mA
50mA
61mA
852mA
322mA
DDR2: 124mA
DDR3: 150mA
106mA
119mA
1782mA
456mA
Unmount JP1401 and mount JP1402
POWER
CRT
PLL
LVDS
PEG
SM CK
AXF
TV
HDA
DMI
VTT
VTTLF
CANTIGA_CHIPSET
Title : Cantiga-POWER(5)
ASUSTeK COMPUTER INC. NB6
Engineer: Wing Cheng
Project Name F8Va
Rev 1.0
Date: Tuesday, October 07, 2008
Sheet 14 of 94



11 MCH_CFG_5 — R1509 2.21KOhm @

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

11 MCH_CFG_6 — R1514 2.21KOhm @ SP1

NO136. N81PR

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

11 MCH_CFG_7 — R1511 2.21KOhm @

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

11 MCH_CFG_9 — R1512 2.21KOhm @

CFG9 : PCIE GRAPHIC LANE
HIGH = Normal Operation (Default)
LOW = Reverse Lanes

11 MCH_CFG_16 — R1507 2.21KOhm @

CFG16 : FSB Dynamic ODT
HIGH = Ensable (Default)
LOW = Disable

11 MCH_CFG_10 — R1508 2.21KOhm @

CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

11 MCH_CFG_12 — R1513 2.21KOhm @

11 MCH_CFG_13 — R1510 2.21KOhm @

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

+3VS — R1503 4.02KOHM @ — 11 MCH_CFG_19

CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

+3VS — R1506 4.02KOHM @ — 11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

NB DS p.70 157

ASUSTeK COMPUTER INC. NB6		Engineer: Wing Cheng	
Size: Custom	Project Name: F8Va		Rev: 1.0
Date: Tuesday, October 07, 2008		Sheet 15 of 94	

Title : Cantiga-GND

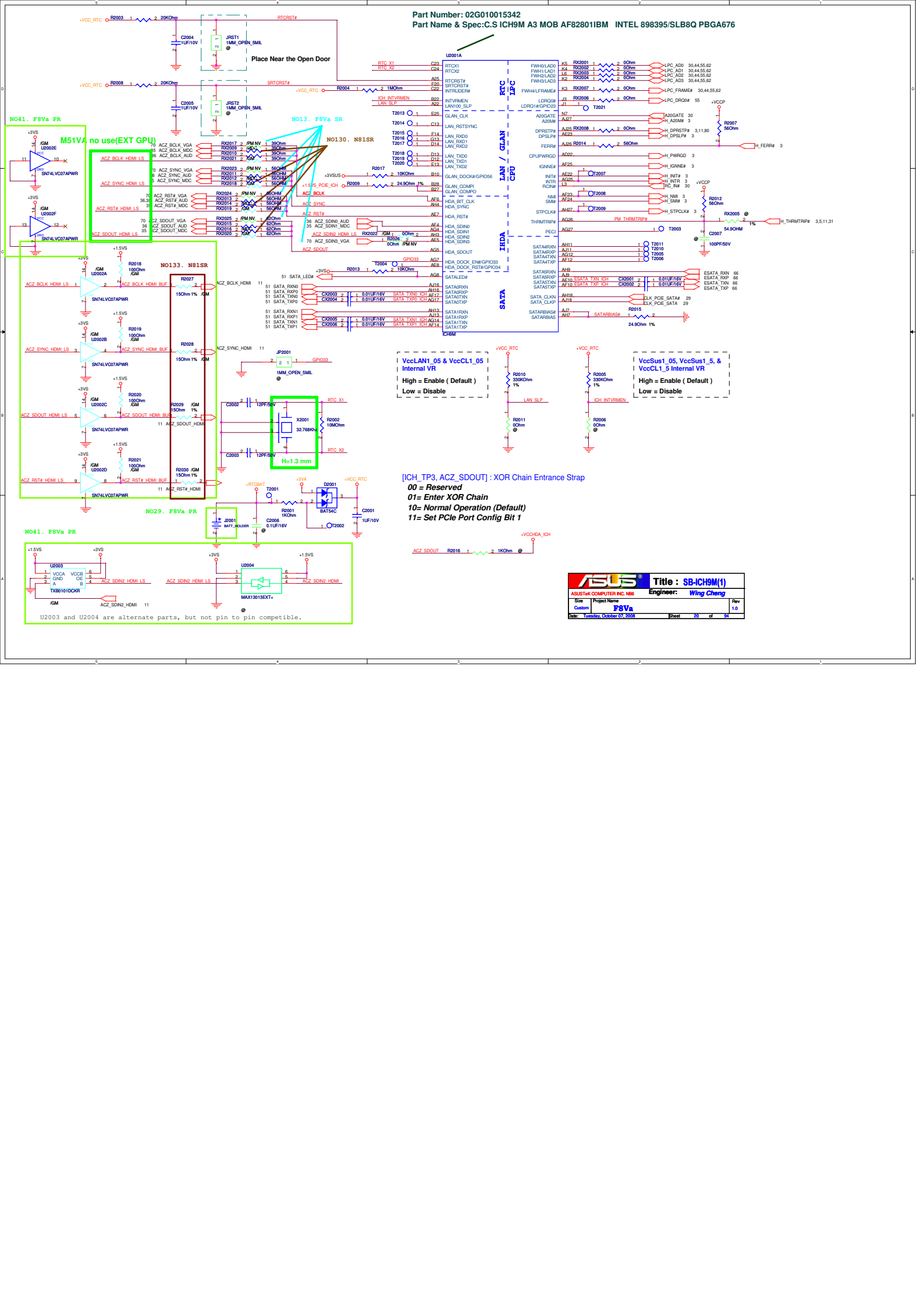
Title :	BLANK
ASUSTeK COMPUTER INC	Engineer:
Size: A	Project Name: F8Va
Rev: 1.0	
Date: Tuesday, October 07, 2008	Sheet 16 of 94

ASUSTeK COMPUTER INC	Title : BLANK		
	Engineer:		
Size: A	Project Name: F8Va		Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 17 of 94		

ASUSTeK COMPUTER INC	Title : BLANK		
	Engineer:		
Size: A	Project Name: F8Va		Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 18 of 94		

ASUSTeK COMPUTER INC	Title : BLANK		
	Engineer:		
Size: A	Project Name: F8Va		Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 19 of 94		

Part Number: 02G010015342
Part Name & Spec:C.S ICH9M A3 MOB AF82801IBM INTEL 898395/SLB8Q PBGA676



PCI BUS cross moat, add Stitching cap

+3VS C2110 0.1UF/10V C2111 0.1UF/10V C2112 0.1UF/10V +1.5VS

40 PCI_AD[31:0]

U2001B

PCI

PCI_AD0 D11 AD0
PCI_AD1 C8 AD1
PCI_AD2 D9 AD2
PCI_AD3 E12 AD3
PCI_AD4 E9 AD4
PCI_AD5 C9 AD5
PCI_AD6 E10 AD6
PCI_AD7 B7 AD7
PCI_AD8 C7 AD8
PCI_AD9 C5 AD9
PCI_AD10 G11 AD10
PCI_AD11 F8 AD11
PCI_AD12 F11 AD12
PCI_AD13 E7 AD13
PCI_AD14 A3 AD14
PCI_AD15 D2 AD15
PCI_AD16 F10 AD16
PCI_AD17 D5 AD17
PCI_AD18 D10 AD18
PCI_AD19 B3 AD19
PCI_AD20 F7 AD20
PCI_AD21 C3 AD21
PCI_AD22 F3 AD22
PCI_AD23 F4 AD23
PCI_AD24 C1 AD24
PCI_AD25 G7 AD25
PCI_AD26 H7 AD26
PCI_AD27 D1 AD27
PCI_AD28 G5 AD28
PCI_AD29 H6 AD29
PCI_AD30 G1 AD30
PCI_AD31 H3 AD31

REQ0# F1 PCI_REQ#0 22,40
GNT0# G4 PCI_GNT#0 40
REQ1#/GPIO50 B6 PCI_REQ1# 22
GNT1#/GPIO51 A7
REQ2#/GPIO52 F13 T2101
GNT2#/GPIO53 F12 T2102 GPIO52 22
REQ3#/GPIO54 E6 GPIO54 GPIO54 22
GNT3#/GPIO55 F6 T2103

C/BE0# D8 PCI_C/BE#0 40
C/BE1# B4 PCI_C/BE#1 40
C/BE2# D6 PCI_C/BE#2 40
C/BE3# A5 PCI_C/BE#3 40

IRDY# D3 PCI_IRDY# 22,40
PAR E3 PCI_PAR 40
PCIRST# R1 PCI_RST# ICH
DEVSEL# C6 PCI_DEVSEL# 22,40
PERR# E4 PCI_PERR# 22,40
PLOCK# C2 PCI_LOCK# 22
SERR# J4 PCI_SERR# 22,40
STOP# A4 PCI_STOP# 22,40
TRDY# F5 PCI_TRDY# 22,40
FRAME# D7 PCI_FRAME# 22,40

PLTRST# C14 PLT_RST# 5,11,33,55,62,70
PCICLK D4 CLK_ICHPCI 29
PME# R2 PCI_PME# 40

Interrupt I/F

22,40 PCI_INTA# J5 PIRQA#
22,40 PCI_INTB# E1 PIRQB#
22 PCI_INTC# J6 PIRQC#
22 PCI_INTD# C4 PIRQD#

PIRQE#/GPIO2 H4 PCI_INTE# 22
PIRQF#/GPIO3 K6 PCI_INTF# 22
PIRQG#/GPIO4 F2 PCI_INTG# 22
PIRQH#/GPIO5 G2 PCI_INTH# 22

ICH9M

53 PCIE_RXN1_ROBSON N29
53 PCIE_RXP1_ROBSON N28
CX2101 1 2 0.1UF/10V PCIE_TXN1_ROBSON
CX2102 1 2 0.1UF/10V PCIE_TXP1_ROBSON
53 PCIE_TXN1_C P27
53 PCIE_TXP1_C P26

53 PCIE_RXN2_MINICARD L29
53 PCIE_RXP2_MINICARD L28
CX2103 1 2 0.1UF/10V PCIE_TXN2_MINICARD
CX2104 1 2 0.1UF/10V PCIE_TXP2_MINICARD
53 PCIE_TXN2_C M27
53 PCIE_TXP2_C M26

43 PCIE_RXN3_NEWCARD J29
43 PCIE_RXP3_NEWCARD J28
CX2105 1 2 0.1UF/10V PCIE_TXN3_NEWCARD
CX2106 1 2 0.1UF/10V PCIE_TXP3_NEWCARD
43 PCIE_TXN3_C K27
43 PCIE_TXP3_C K26

G29
G28
H27
H26

33 PCIE_RXN6_GLAN C29
33 PCIE_RXP6_GLAN C28
CX2111 1 2 0.1UF/10V PCIE_TXN6_GLAN
CX2112 1 2 0.1UF/10V PCIE_TXP6_GLAN
33 PCIE_TXN6_C D27
33 PCIE_TXP6_C D26

NO136. N81SR

+3VS
25 SPI_CLK RX2101 2 SPI 1 15Ohm 1% SB_SPICLK D23
25 SPI_CS#0 RX2102 2 SPI 1 15Ohm 1% SB_SPICS0# D24
SB_SPICS1# F23
R2106 1 2 1KOhm 1% T2106
25 SPI_SI RX2104 2 SPI 1 15Ohm 1% SB_SPISI D25
25 SPI_SO F23

52 USB_OC0#1 USB_OC0#1 N4
52 USB_OC2#3 USB_OC2#3 N6
43 USB_OC4# USB_OC4# M1
52 USB_OC5# USB_OC5# N2
USB_OC6# M4
USB_OC7# M3
80 VCORE_CNT1 VCORE_CNT1 N3
80 VCORE_CNT2 VCORE_CNT2 N1
USB_OC0# P5
USB_OC1# P3

SPI_MOSI
iTPM Enable
High = Enable
Low = Disable(Default)

NO100. N80V PR

NO14. F8Va SR
53 WLAN_ON

NO50. F8Va PR

R2105 2 1 USBRBIAS_PN AG2
22.6Ohm 1% AG1

USBRBIAS
USBRBIAS#

U2001D

PCI-Express
Direct Media Interface
SPI
USB

PERn1 PERp1 PETn1 PETp1
PERn2 PERp2 PETn2 PETp2
PERn3 PERp3 PETn3 PETp3
PERn4 PERp4 PETn4 PETp4
PERn5 PERp5 PETn5 PETp5
PERn6/GLAN_RXN PERp6/GLAN_RXP PETn6/GLAN_TXN PETp6/GLAN_TXP

SPI_CLK SPI_CS0# SPI_CS1#/GPIO58/CLGPIO6 SPI_MOSI SPI_MISO

OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8#/GPIO44 OC9#/GPIO45 OC10#/GPIO46 OC11#/GPIO47

DMI0RXN V27 DMI_RXN0 11
DMI0RXP V26 DMI_RXP0 11
DMI0TXN U29 DMI_TXN0 11
DMI0TXP U28 DMI_TXP0 11

DMI1RXN Y27 DMI_RXN1 11
DMI1RXP Y26 DMI_RXP1 11
DMI1TXN W29 DMI_TXN1 11
DMI1TXP W28 DMI_TXP1 11

DMI2RXN AB27 DMI_RXN2 11
DMI2RXP AB26 DMI_RXP2 11
DMI2TXN AA29 DMI_TXN2 11
DMI2TXP AA28 DMI_TXP2 11

DMI3RXN AD27 DMI_RXN3 11
DMI3RXP AD26 DMI_RXP3 11
DMI3TXN AC29 DMI_TXN3 11
DMI3TXP AC28 DMI_TXP3 11

DMI_CLKN T26 CLK_PCIE_ICH# 29
DMI_CLKP T25 CLK_PCIE_ICH 29

DMI_ZCOMP
DMI_IRCOMP
AF29 DMI_COMP R2103 1 2 24.9Ohm 1% +1.5VS_PCIE_ICH
AF28 L<500mils

USBP0N AC5 USB_PN0 52
USBP0P AC4 USB_PP0 52
USBP1N AD3 USB_PN1 52
USBP1P AD2 USB_PP1 52
USBP2N AC1 USB_PN2 52
USBP2P AC2 USB_PP2 52
USBP3N AA5 USB_PN3 52
USBP3P AA4 USB_PP3 52
USBP4N AB2 USB_PN4 68
USBP4P AB3 USB_PP4 68
USBP5N AA1 USB_PN5 52
USBP5P AA2 USB_PP5 52
USBP6N W5 T2104
USBP6P W4 T2105
USBP7N Y3 USB_PN7 53
USBP7P Y2 USB_PP7 53
USBP8N W1 USB_PN8 43
USBP8P W2 USB_PP8 43
USBP9N V2 USB_PN9 53
USBP9P V3 USB_PP9 53
USBP10N U5 USB_PN10 61
USBP10P U4 USB_PP10 61
USBP11N U1 USB_PN11 63
USBP11P U2 USB_PP11 63

Place within 500 mils of ICH

Place within 500 mils of ICH

+3V

U2101
PLT_RST# 2
1 VCC 5
3 GND 4
BUF_PLT_RST# 30,43,53
NC7SZ08P5X_NL
R2110 1 @ 2 0Ohm

+3V

U2102 @
PCI_RST# ICH 2
1 VCC 5
3 GND 4
PCI_RST# 40
NC7SZ08P5X_NL
R2111 1 2 0Ohm

+3VSUS

NO100. N80V PR
VCORE_CNT1 1 10KOhm 2 RN2101A
22 PM_RI# 3 10KOhm 4 RN2101B
USB_OC6# 5 10KOhm 6 RN2101C
NO100. N80V PR
VCORE_CNT2 7 10KOhm 8 RN2101D
USB_OC01# 1 10KOhm 2 RN2102A
USB_OC11# 3 10KOhm 4 RN2102B
USB_OC4# 5 10KOhm 6 RN2102C
USB_OC5# 7 10KOhm 8 RN2102D
1 10KOhm 2 RN2103A
USB_OC7# 3 10KOhm 4 RN2103B
USB_OC23# 5 10KOhm 6 RN2103C
USB_OC10# 7 10KOhm 8 RN2103D

When supporting CLK GEN Turbo PIN, UNI R2107.

NO100. N80V PR

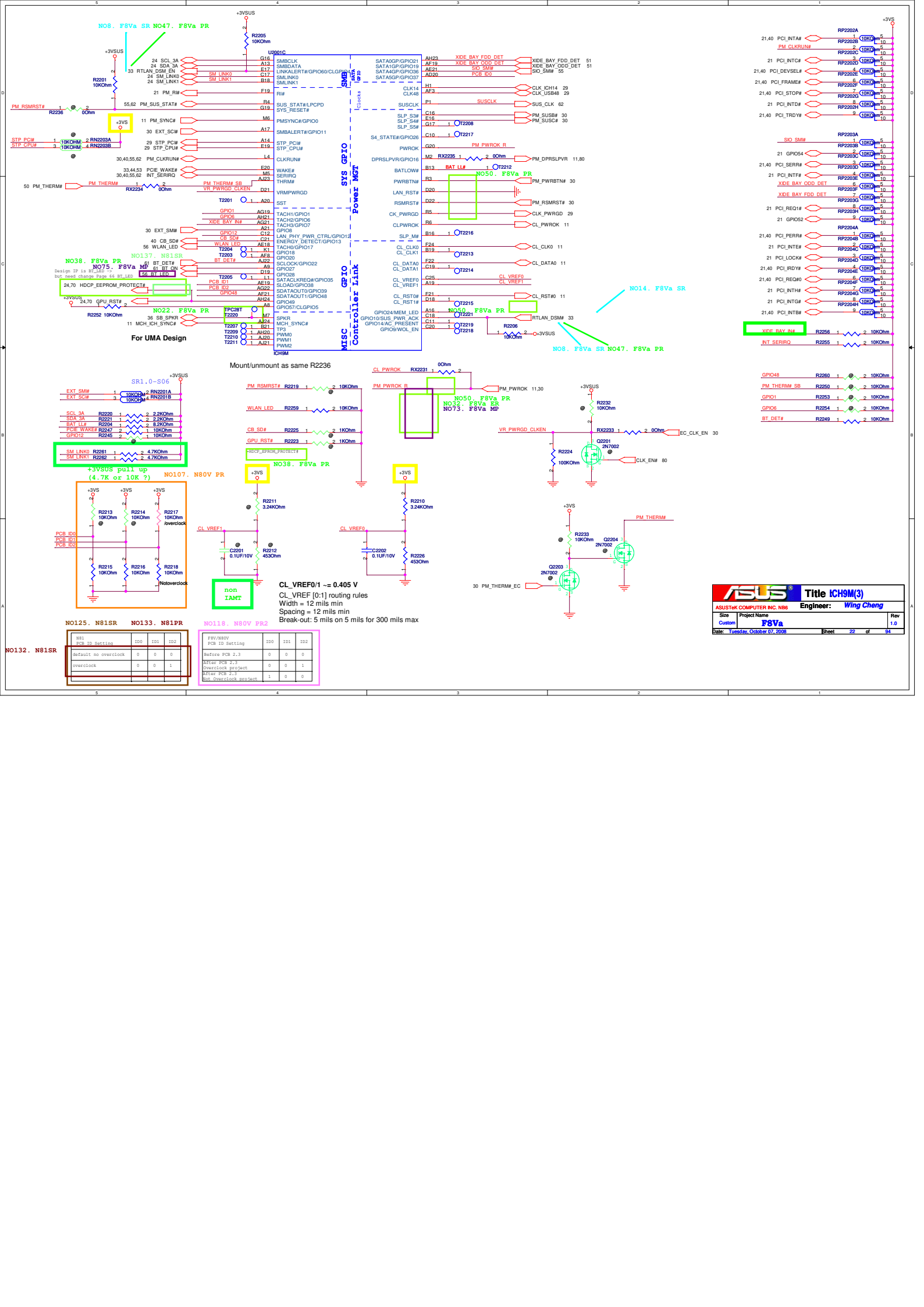
ICH9 Boot BIOS select

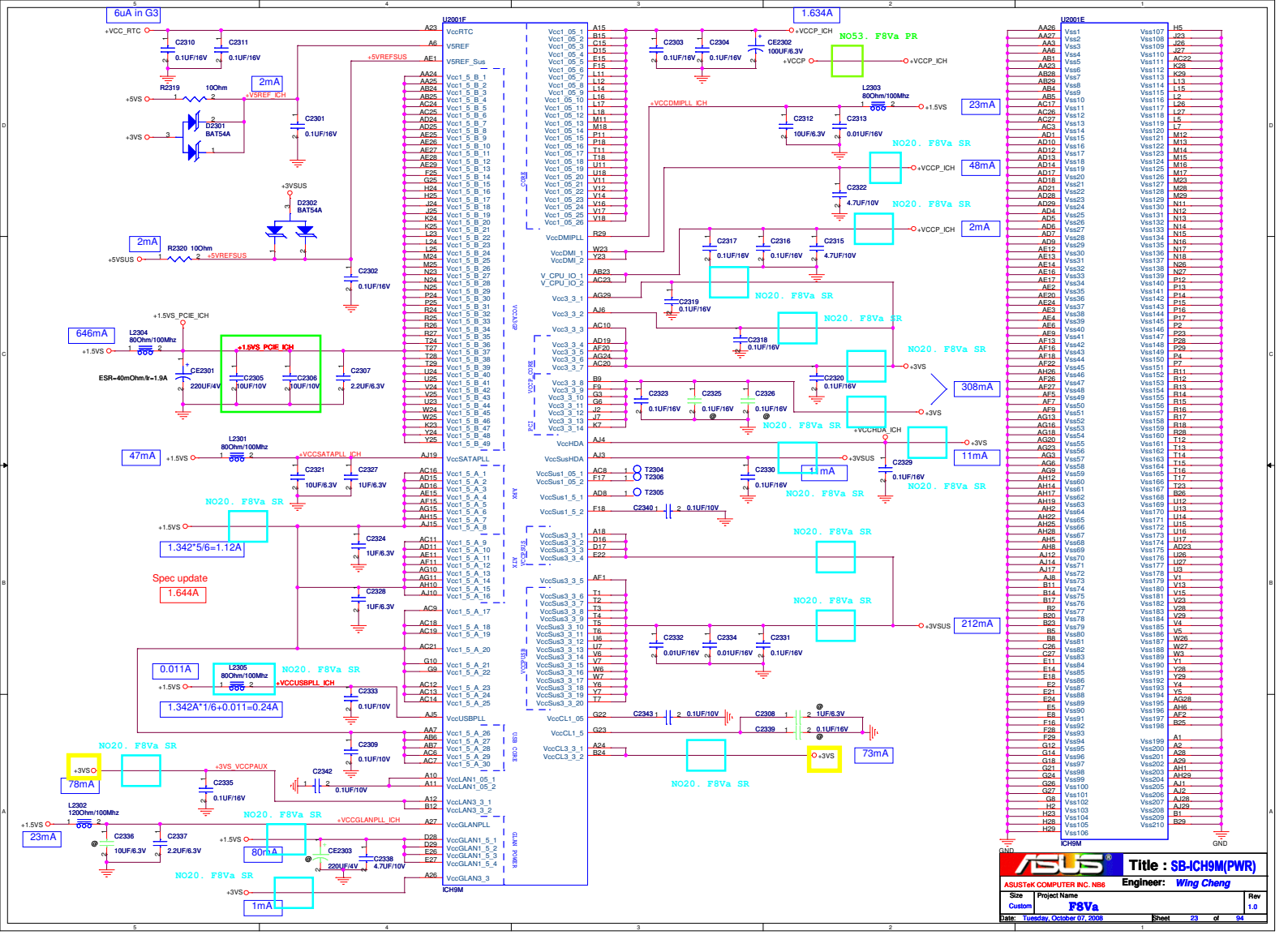
	GNT#0	CS#1	
LPC	11	1	1 (default)
PCI	10	1	0
SPI	01	0	1
reserve	00	0	0

PCI_GNT#0 R2101 1 2 1KOhm @
SB_SPICS1# R2102 1 2 1KOhm @

ASUSTeK COMPUTER INC. NB6

Title : SB-ICH9M(2)
Engineer: Wing Cheng
Size: Custom
Project Name: F8Va
Rev: 1.0
Date: Tuesday, October 07, 2008
Sheet 21 of 94

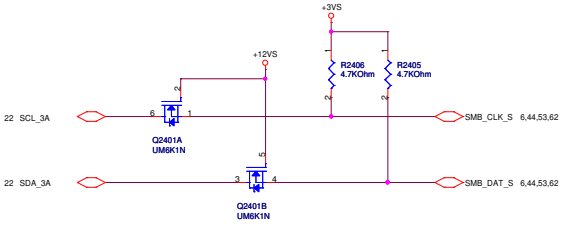

NO8. F8Va SR NO47. F8Va PR
U2001C
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
ICH9M
SMB
GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
XIDE_BAY_FDD_DET
XIDE_BAY_ODD_DET
SIO_SMI#
PCB_ID0
CLK_ICH14
CLK_USB48
SUSCLK
PM_SUSB#
PM_SUSC#
PM_PWROK_R
PM_DPRSLPVR
BAT_LL#
PM_PWRBTN#
PM_RSMRST#
CK_PWRGD
CL_PWROK
CL_CLK0
CL_DATA0
CL_RST#0
RTLAN_DSM#
NO50. F8Va PR
NO14. F8Va SR
NO68. F8Va PR
NO8. F8Va SR NO47. F8Va PR
NO38. F8Va PR
NO75. F8Va MP
NO137. N81SR
NO22. F8Va PR
For UMA Design
Mount/unmount as same R2236
SR1.0~S06
NO32. F8Va ER
NO73. F8Va MP
NO38. F8Va PR
NO107. N80V PR
+3VSUS pull up
(4.7K or 10K ?)
non IAMT
CL_VREF0/1 ~= 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max
NO125. N81SR
NO133. N81PR
NO118. N80V PR2
NO132. N81SR
N81 PCB ID Setting
default no overclock
overclock
F8V/N80V PCB ID Setting
Before PCB 2.3
After PCB 2.3 Overclock project
After PCB 2.3 Not Overclock project
Title ICH9M(3)
ASUSTeK COMPUTER INC. NB6
Engineer: Wing Cheng
Size: Custom
Project Name: F8Va
Rev: 1.0
Date: Tuesday, October 07, 2008
Sheet 22 of 94

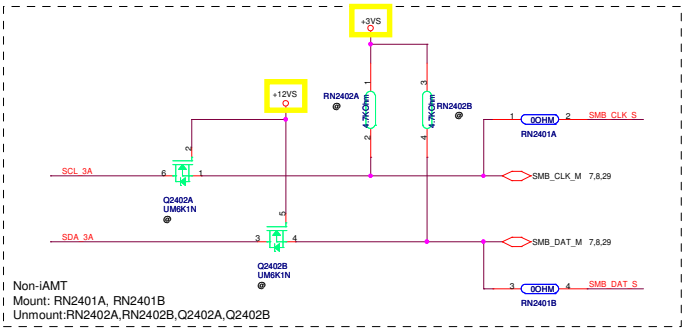


ASUSTeK COMPUTER INC. NB6	Engineer: Wing Cheng		
Size: Custom	Project Name: F8Va		Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 23 of 94		

Title : SB-ICH9M(PWR)

ICH9-M

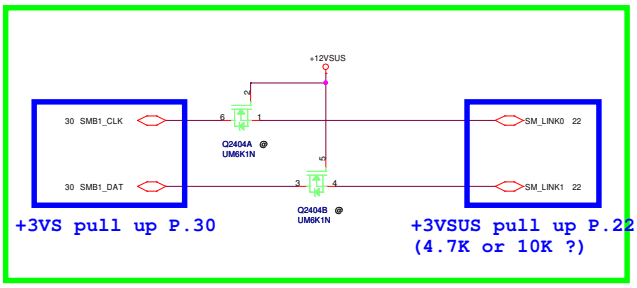


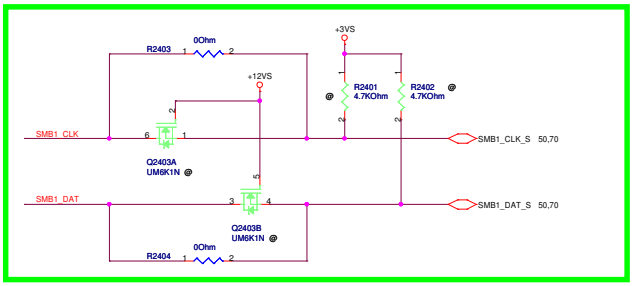


non iAMT

Non-iAMT
Mount: RN2401A, RN2401B
Unmount:RN2402A,RN2402B,Q2402A,Q2402B

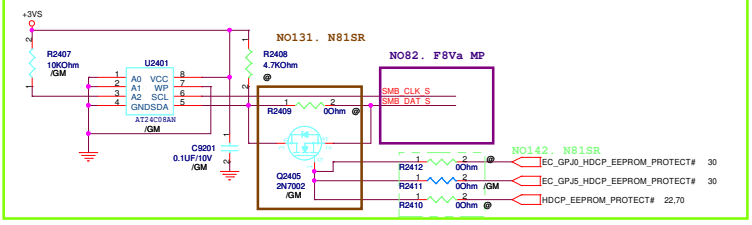
EC-IT8752





NO38. F8Va PR

HDCP ROM



ASUSTeK COMPUTER INC. NB6

Title : ICH9M-Other

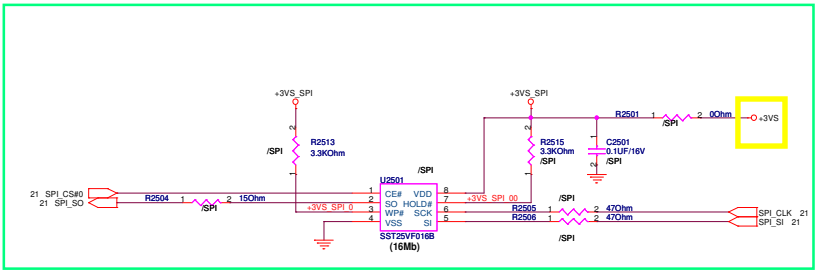
Engineer: Wing Cheng

Size	Project Name	Rev
Custom	F8Va	1.0

Date: Tuesday, October 07, 2008 Sheet 24 of 94

SPI ROM

NO136. N81SR



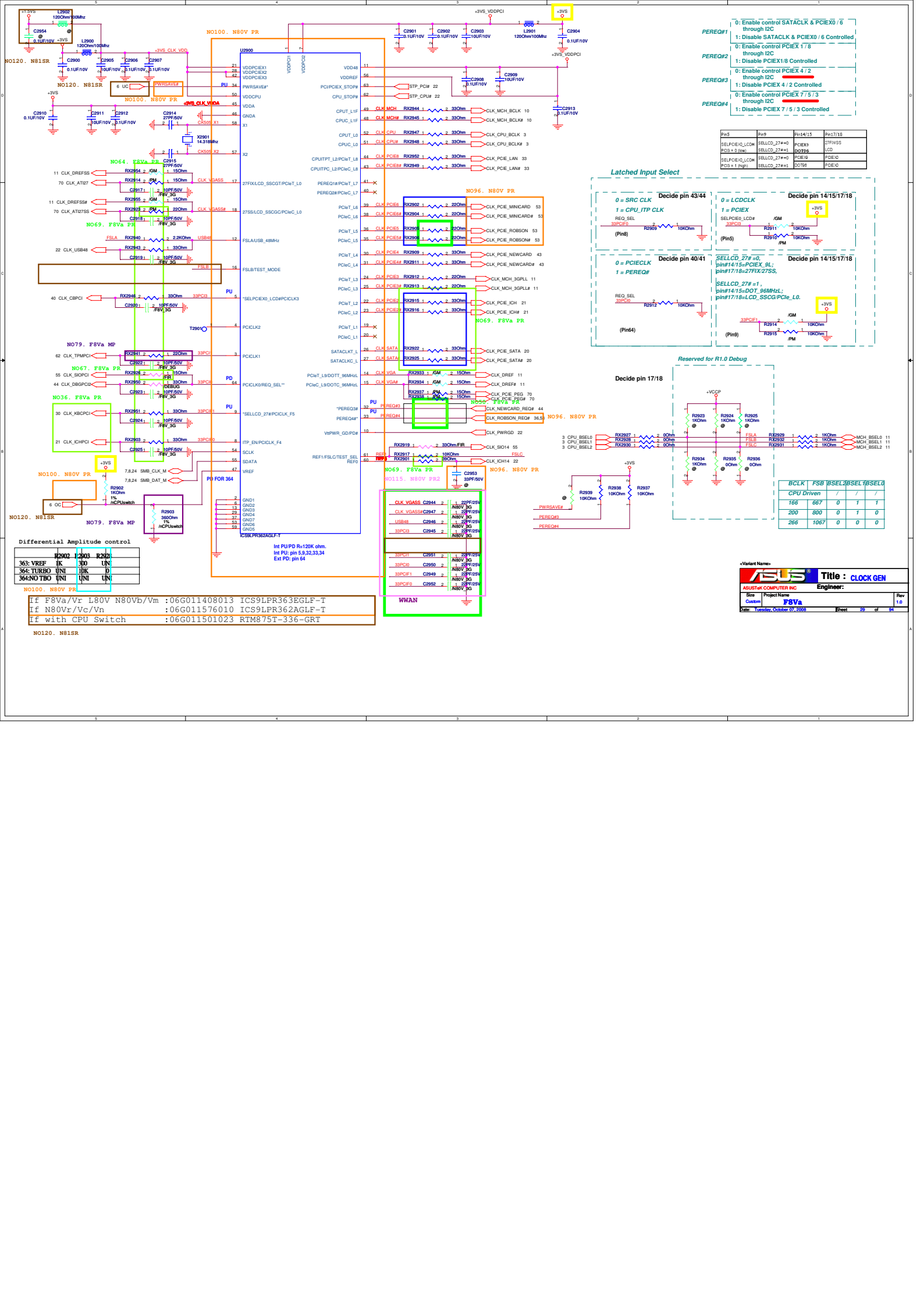
If your Montevina system supports iTPM but does not support iAMT, the ME firmware size for iTPM only should be less than 820KB.
So a 1MByte (8M bits) SPI ROM should be large enough. Please co-work with H/W to use a 8Mbits SPI ROM instead of a 16Mbits one if there is cost gap

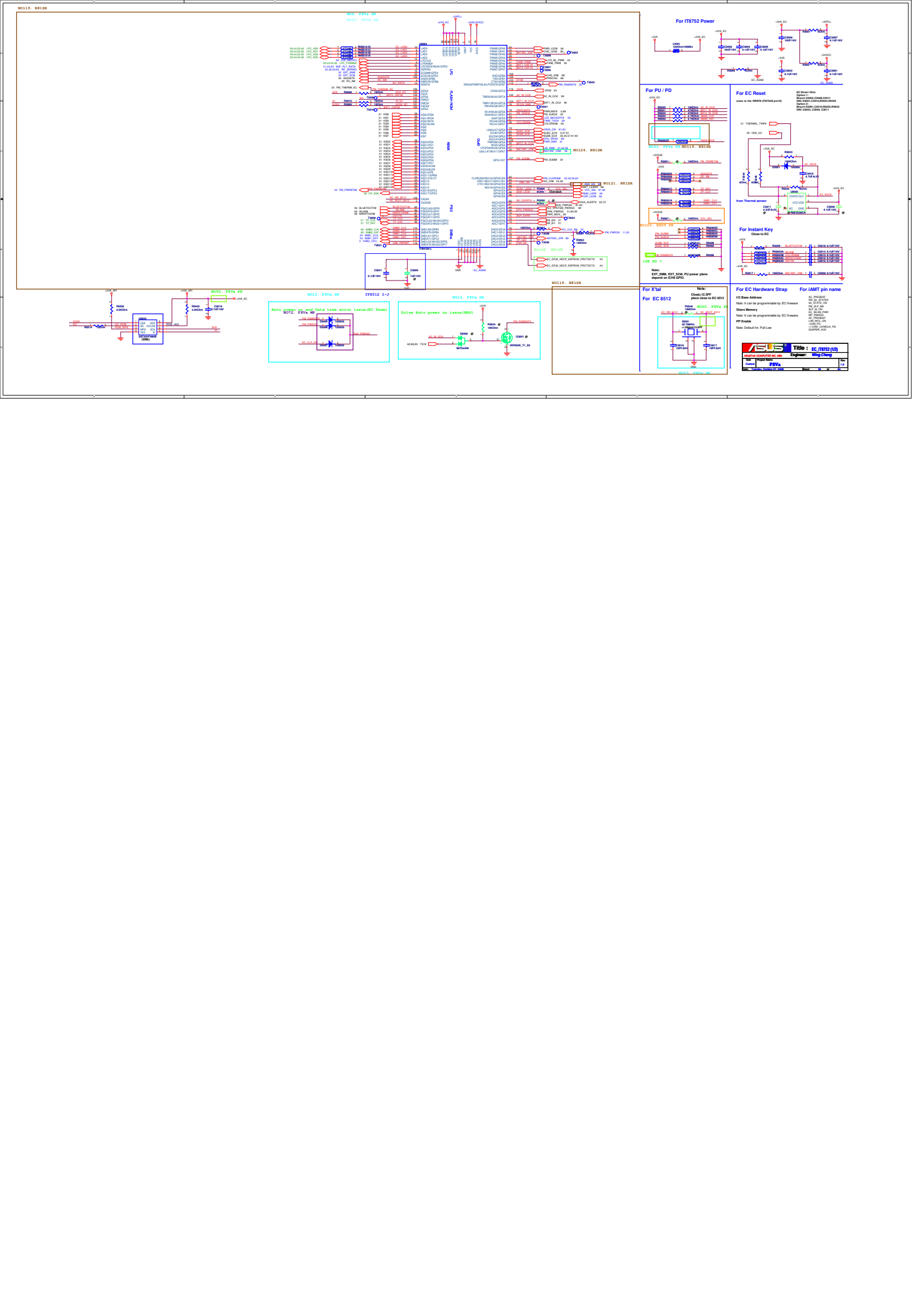
ASUSTeK COMPUTER INC. NB6	Title : SPI ROM	
	Engineer: Wing_Cheng	
Size: Custom	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 25 of 94	

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 26 of 94	

Title : BLANK		
ASUSTeK COMPUTER INC	Engineer:	
Size: A	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 27 of 94	

Title : BLANK				
ASUSTeK COMPUTER INC	Engineer:			
Size: A	Project Name: F8Va			Rev: 1.0
Date: Tuesday, October 07, 2008		Sheet 28 of 94		


PEREQ#1
0: Enable control SATACLK & PCIEX0 / 6 through I2C
1: Disable SATACLK & PCIEX0 / 6 Controlled
PEREQ#2
0: Enable control PCIEX 1 / 8 through I2C
1: Disable PCIEX1/8 Controlled
PEREQ#3
0: Enable control PCIEX 4 / 2 through I2C
1: Disable PCIEX 4 / 2 Controlled
PEREQ#4
0: Enable control PCIEX 7 / 5 / 3 through I2C
1: Disable PCIEX 7 / 5 / 3 Controlled
Latched Input Select
0 = SRC CLK
1 = CPU_ITP CLK
Decide pin 43/44
0 = PCIECLK
1 = PEREQ#
Decide pin 40/41
0 = LCDCLK
1 = PCIEX
Decide pin 14/15/17/18
SELLCD_27# =0, pin#14/15=PCIEX_9L; pin#17/18=27FIX/27SS,
SELLCD_27# =1 , pin#14/15=DOT_96MHzL; pin#17/18=LCD_SSCG/PCIe_L0.
Decide pin 14/15/17/18
Reserved for R1.0 Debug
Decide pin 17/18
Int PU/PD R=120K ohm.
Int PU: pin 5,9,32,33,34
Ext PD: pin 64
Differential Amplitude control
If F8Va/Vr L80V N80Vb/Vm :06G011408013 ICS9LPR363EGLF-T
If N80Vr/Vc/Vn :06G011576010 ICS9LPR362AGLF-T
If with CPU Switch :06G011501023 RTM875T-336-GRT
WWAN
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer:
Project Name F8Va
Rev 1.0
Date: Tuesday, October 07, 2008
Sheet 29 of 94


NO119. N81SR
NO5. F8Va SR
NO23. F8Va SR
For IT8752 Power
For PU / PD
For EC Reset
For Instant Key
Close to EC
For X'tal
For EC 8512
For EC Hardware Strap
For IAMT pin name
NO50. F8Va PR
NO15. F8Va SR
IT8512 1~7
NO72. F8Va MP
Auto power on and Data time error issue(EC Team)
Solve Auto power on issue(NB6)
Title : EC_IT8752 (1/2)
Engineer: Ming Chang
Size: Custom
Project Name: F8Va
Rev: 1.0
Tuesday, October 07, 2008
Sheet 36 of 50

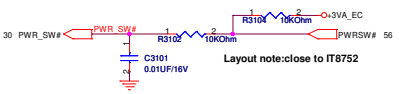
For Battery

Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

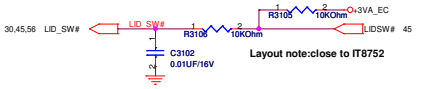
Del

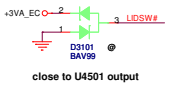
For Switch

PWR SWITCH



LID SWITCH



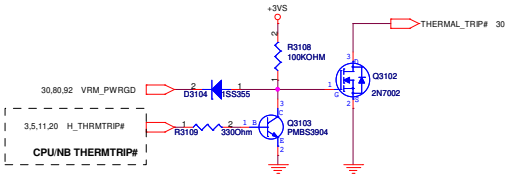


close to connector

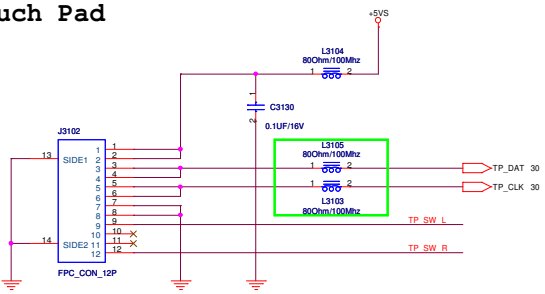
Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

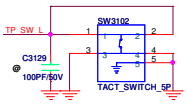
close to U4501 output

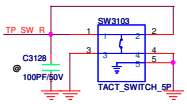
For Thermal Control Method



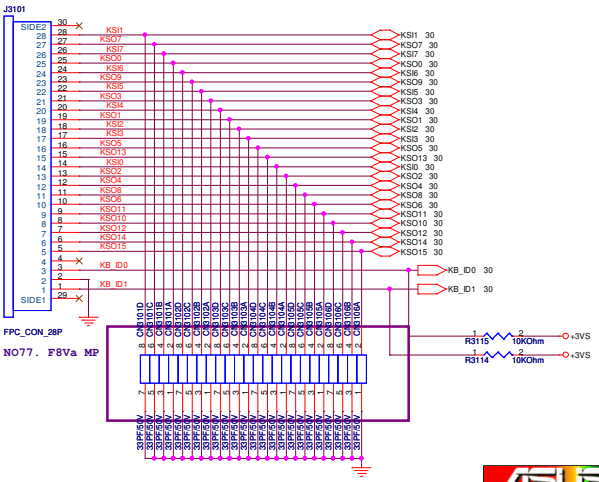
Touch Pad





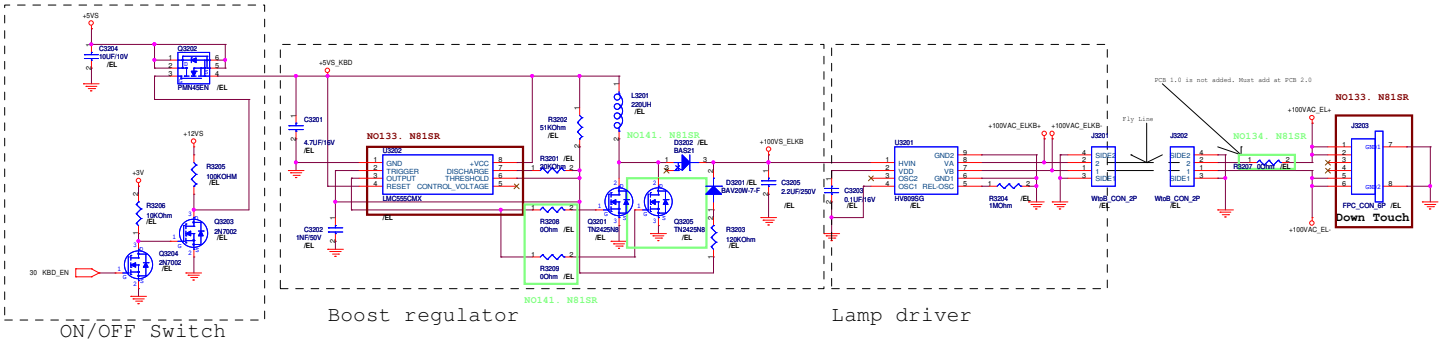


Keyboard Connector



ASUSTeK COMPUTER INC. NB6	Title : EC_IT8511 (2/2)		
	Engineer: Wing Cheng		
Size: Custom	Project Name: F8Va		Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 31 of 94		

NO121. N81SR
NO138. N81SR

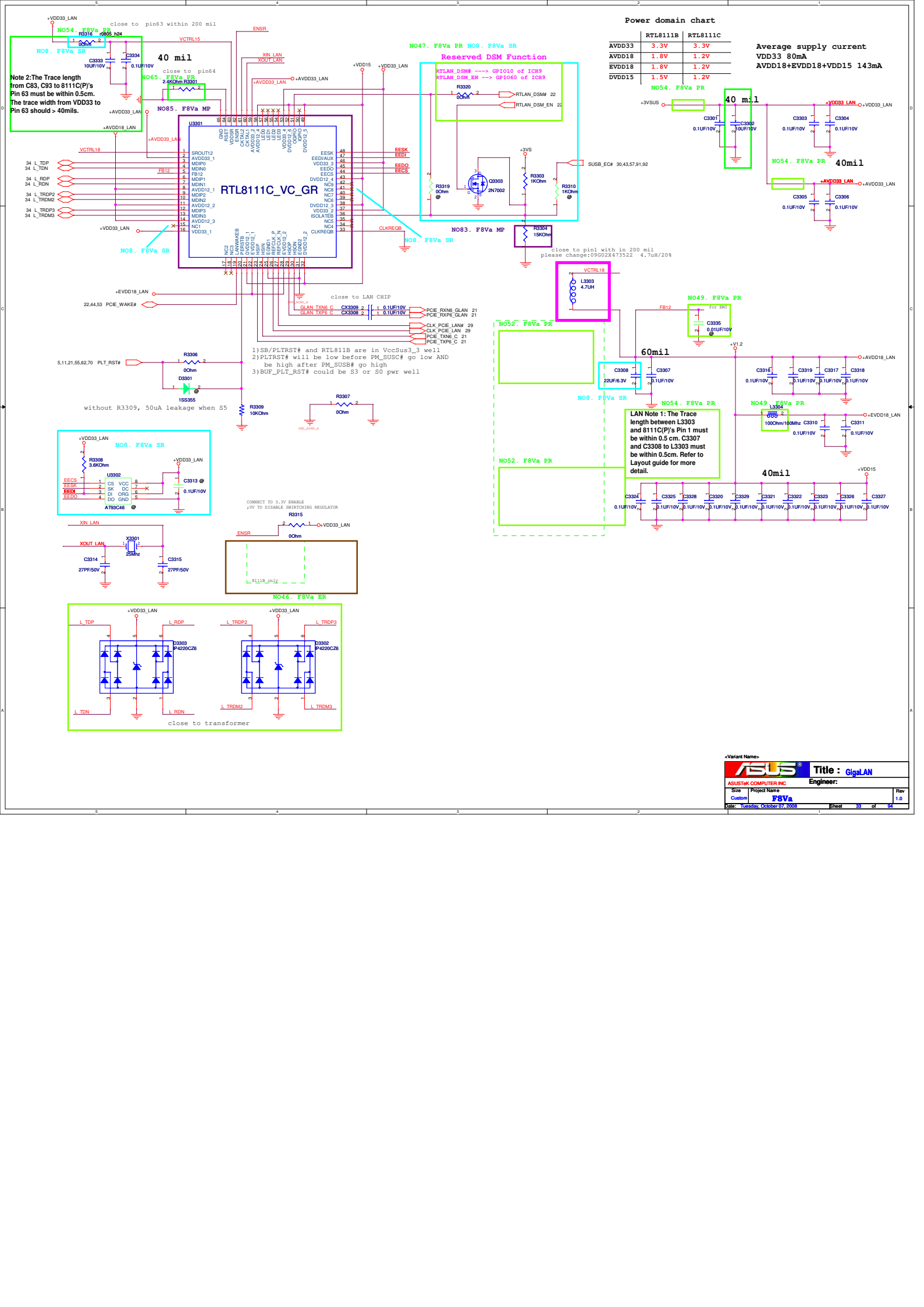


ON/OFF Switch

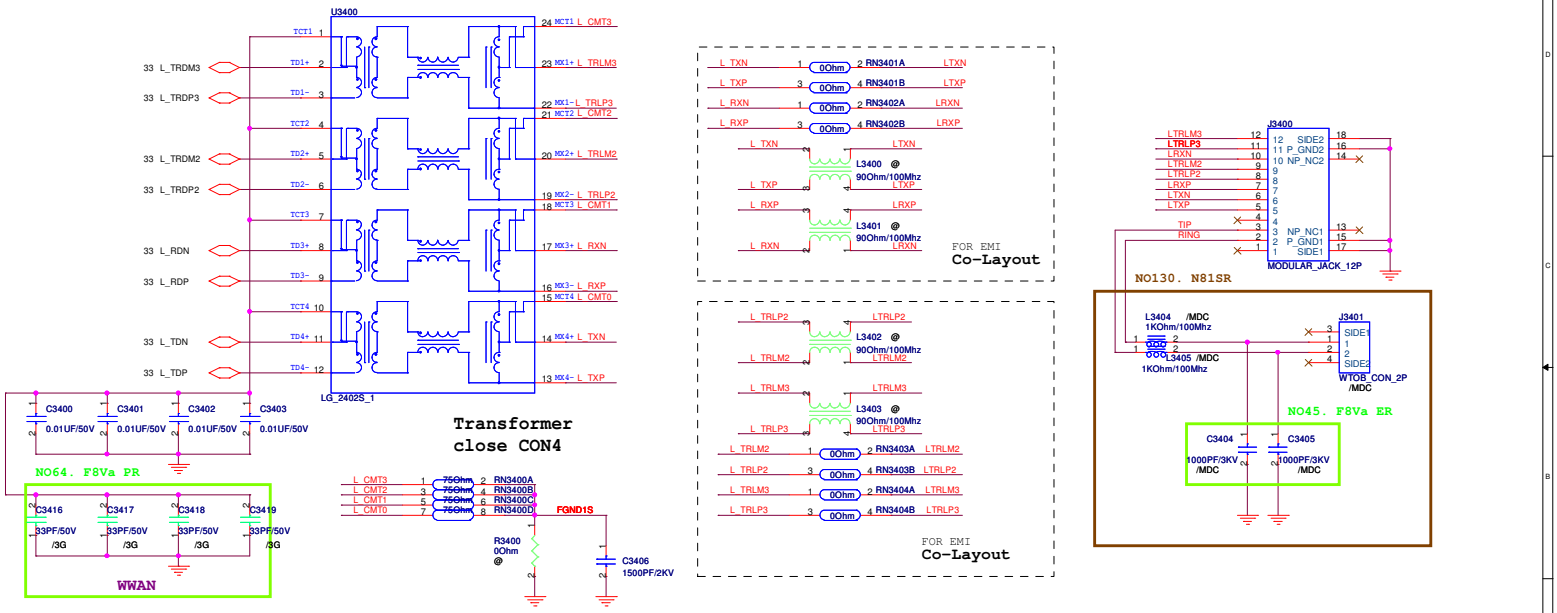
Boost regulator

Lamp driver

ASUSTeK COMPUTER INC	Title : KBD	
	Engineer:	
Size: Custom	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 32 of 94	


Power domain chart
RTL8111B
RTL8111C
AVDD33 3.3V 3.3V
AVDD18 1.8V 1.2V
EVDD18 1.8V 1.2V
DVDD15 1.5V 1.2V
Average supply current
VDD33 80mA
AVDD18+EVDD18+VDD15 143mA
Note 2:The Trace length from C83, C93 to 8111C(P)'s Pin 63 must be within 0.5cm. The trace width from VDD33 to Pin 63 should > 40mils.
RTL8111C_VC_GR
Reserved DSM Function
RTLAN_DSM# ---> GPIO10 of ICH9
RTLAN_DSM_EN --> GPIO60 of ICH9
close to pin63 within 200 mil
close to pin64
close to pin1 with in 200 mil
please change:09G02X473522 4.7uH/20%
close to LAN CHIP
close to transformer
without R3309, 50uA leakage when S5
1)SB/PLTRST# and RTL811B are in VccSus3_3 well
2)PLTRST# will be low before PM_SUSC# go low AND be high after PM_SUSB# go high
3)BUF_PLT_RST# could be S3 or S0 pwr well
LAN Note 1: The Trace length between L3303 and 8111C(P)'s Pin 1 must be within 0.5 cm. C3307 and C3308 to L3303 must be within 0.5cm. Refer to Layout guide for more detail.
40 mil
60mil
40mil
Title : GigaLAN
ASUSTeK COMPUTER INC
Engineer:
Project Name F8Va
Rev 1.0
Date: Tuesday, October 07, 2008
Sheet 33 of 94

2402S have issue after IR reflow,
alternative part:LG-2410S-1



<Variant Name>

ASUSTeK COMPUTER INC

Title : RJ11+45

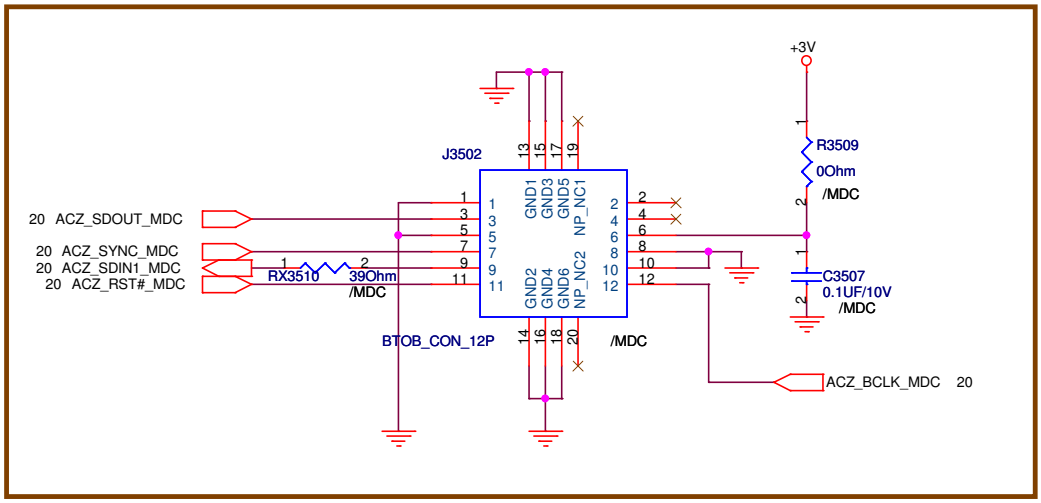
Engineer:

Size	Project Name	Rev
Custom	F8Va	1.0

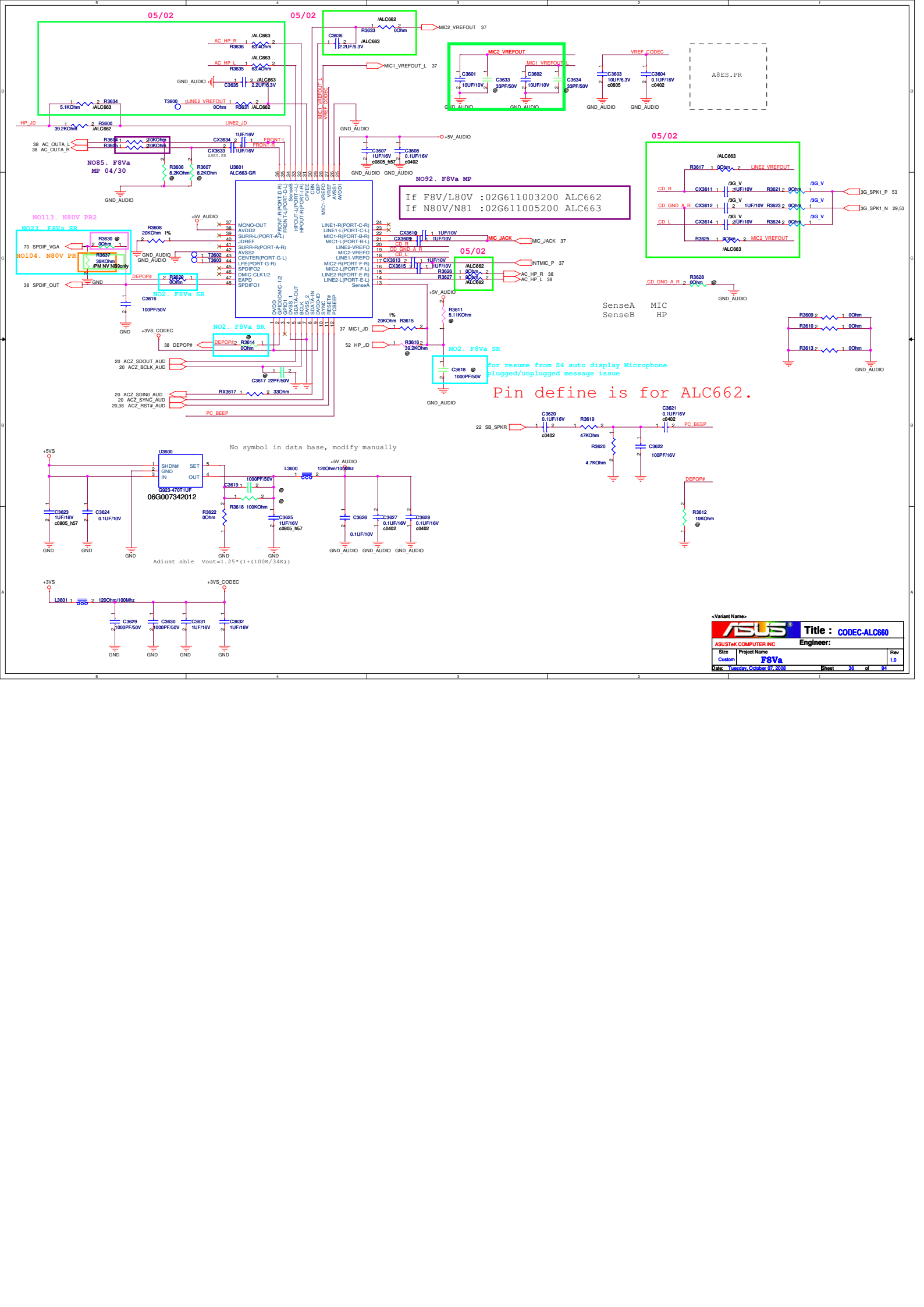
Date: Tuesday, October 07, 2008 Sheet 34 of 94

AZALIA MDC Connector

NO130. N81SR



ASUSTeK COMPUTER INC	Title : MDC	
	Engineer:	
Size: A	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 35 of 94	



<Variant Name>

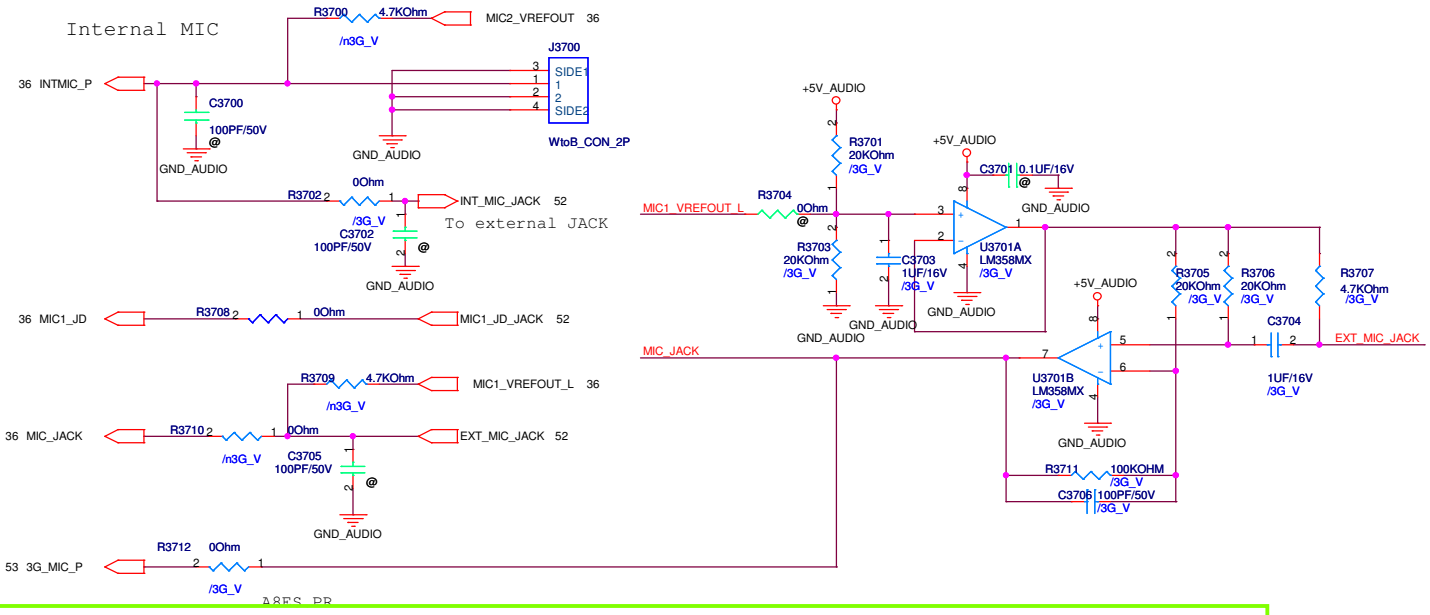
ASUSTeK COMPUTER INC

Title : CODEC-ALC660

Engineer:

Size	Project Name	Rev
Custom	F8Va	1.0

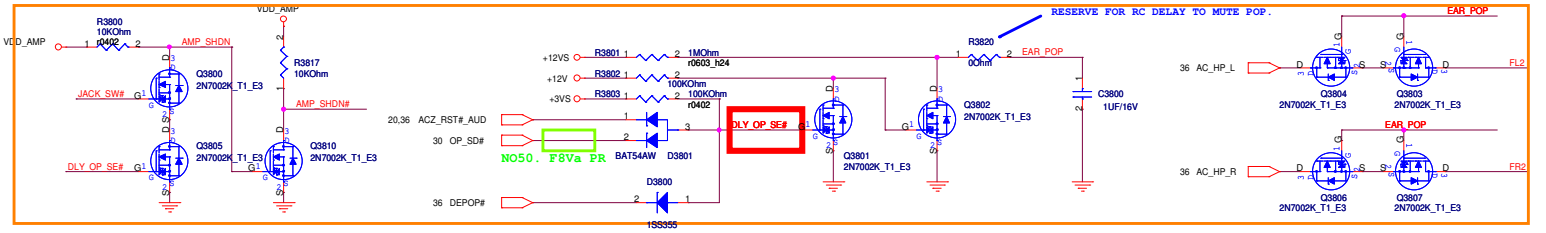
Date: Tuesday, October 07, 2008 Sheet 36 of 94

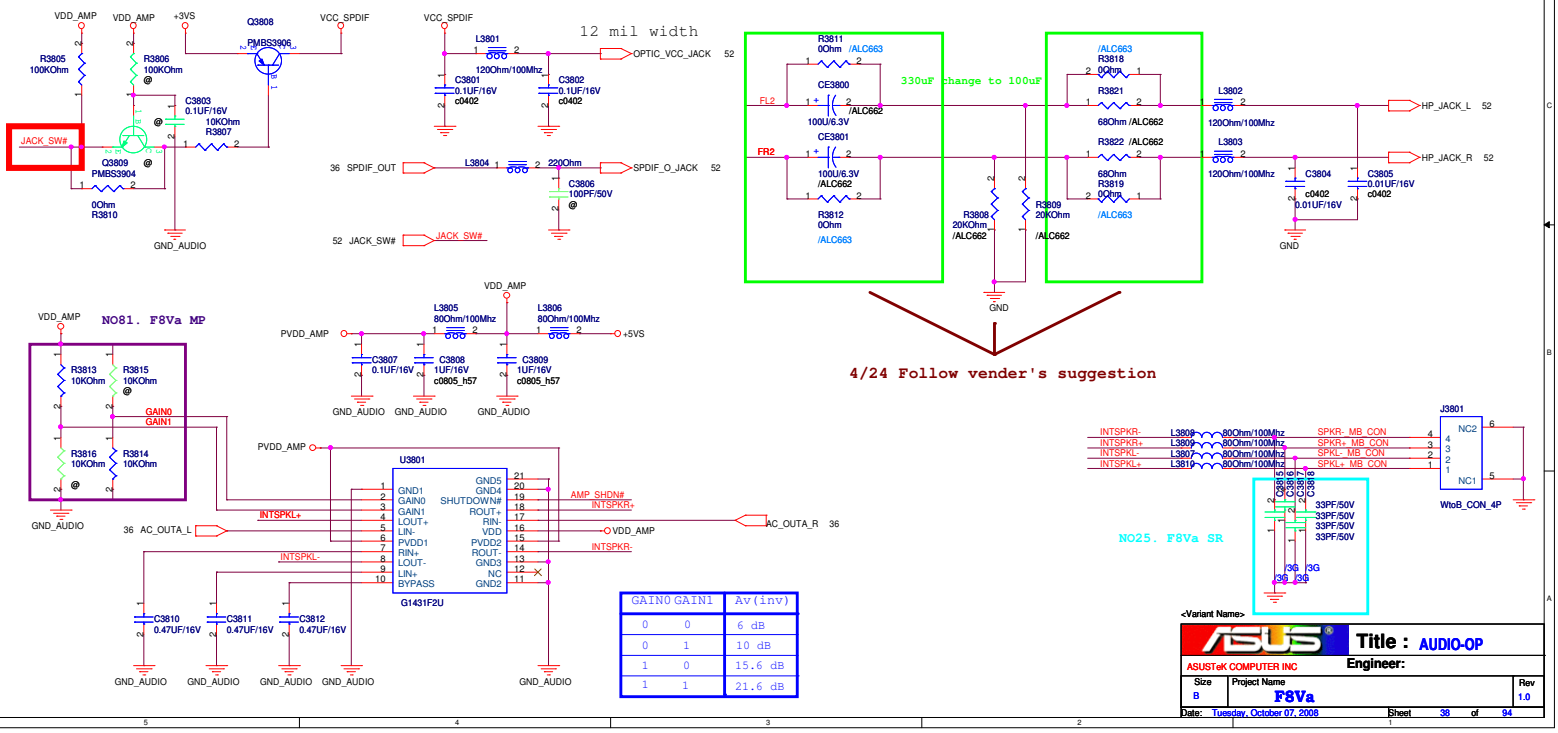


Note：Either 3G or n3G must be chosen, either 3G_V or n3G_V must be chosen

NO33. F8Va ER

ASUSTeK COMPUTER INC	Title : AUDIO-MIC	
	Engineer:	
Size: Custom	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 37 of 94	





GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

<variant_name>

ASUSTeK COMPUTER INC

Title : AUDIO-OP

Engineer:

Size	Project Name	Rev
B	F8Va	1.0

Date: Tuesday, October 07, 2008 Sheet 38 of 94

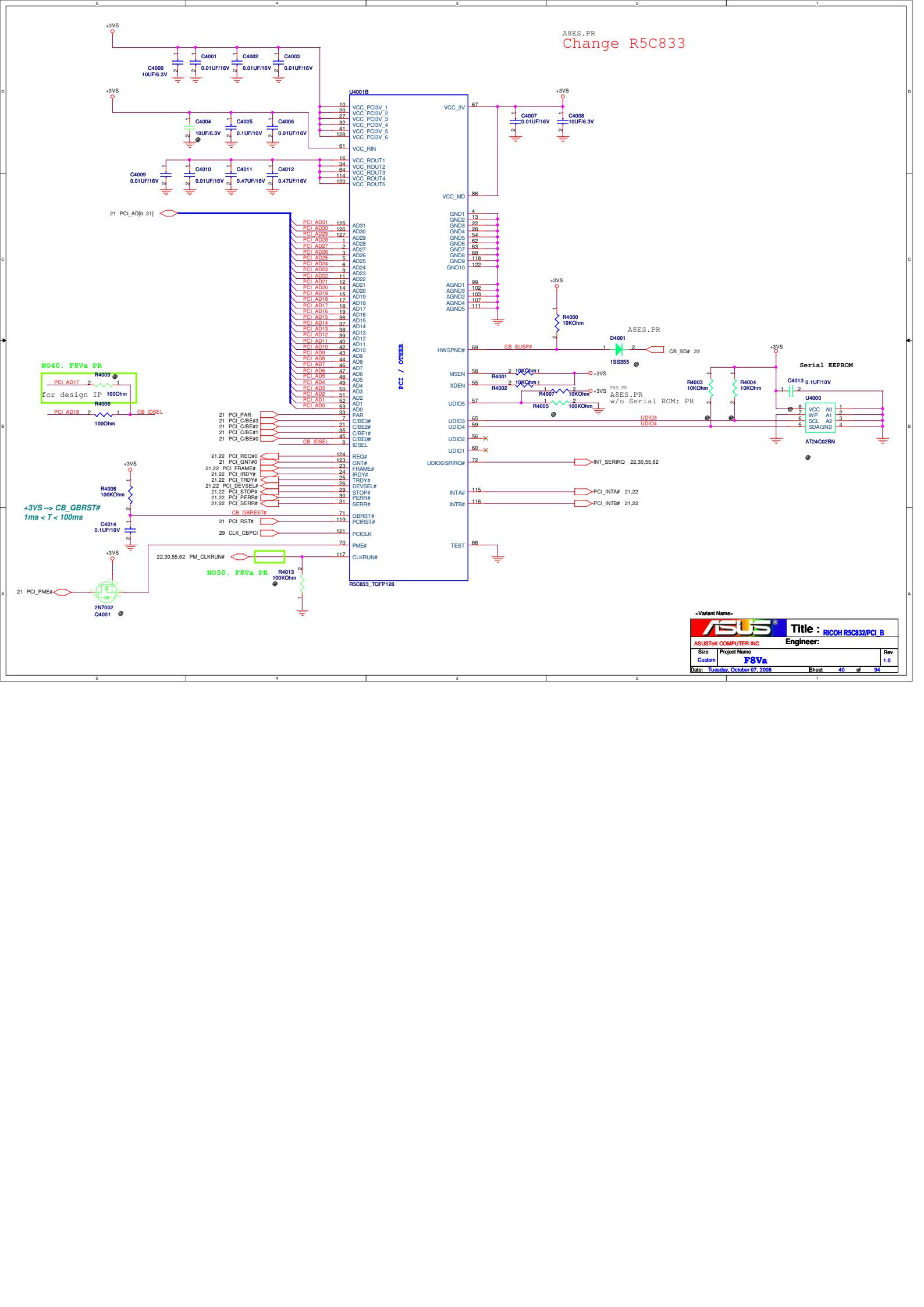
Title : BLANK

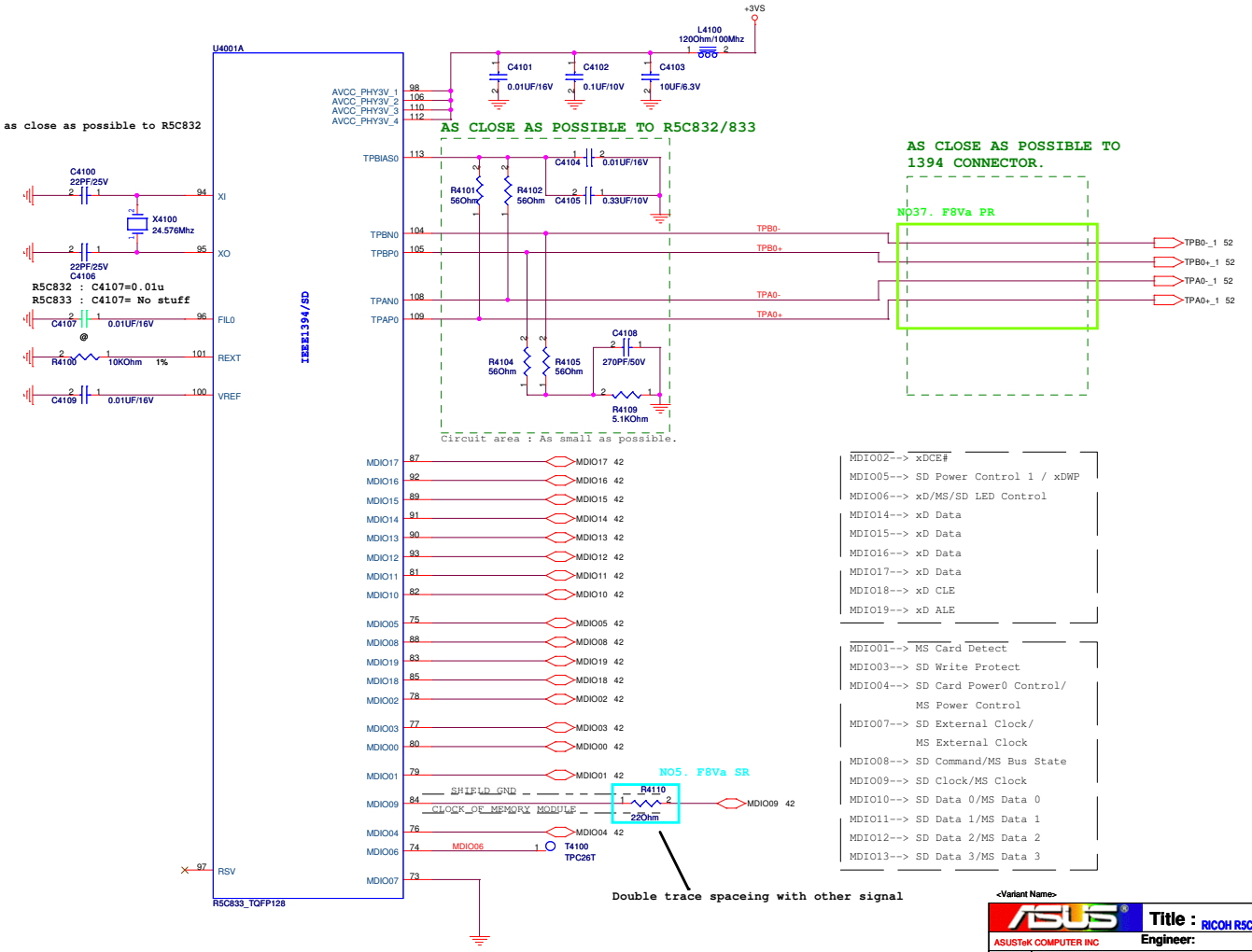
ASUSTeK COMPUTER INC

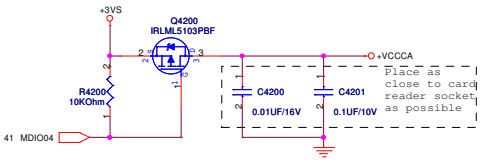
Engineer:

Size	Project Name	Rev
A	F8Va	1.0

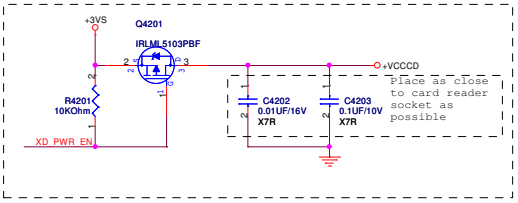
Date: Tuesday, October 07, 2008 Sheet 39 of 94


A8ES.PR
Change R5C833
U4001B
R5C833_TQFP128
PCI / OTHER
NO40. F8Va PR
for design IP
NO50. F8Va PR
+3VS --> CB_GBRST#
1ms < T < 100ms
A8ES.PR
w/o Serial ROM: PH
Serial EEPROM
AT24C02BN
2N7002
Q4001
1SS355
<Variant Name>
Title : RICOH R5C832/PCI_B
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name: F8Va
Rev: 1.0
Date: Tuesday, October 07, 2008
Sheet 40 of 94

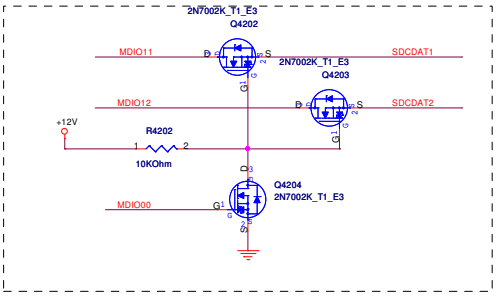

U4001A
IEEE1394/SD
R5C833_TQFP128
as close as possible to R5C832
C4100
22PF/25V
X4100
24.576Mhz
C4106
22PF/25V
R5C832 : C4107=0.01u
R5C833 : C4107= No stuff
C4107
0.01UF/16V
R4100
10KOhm 1%
C4109
0.01UF/16V
XI
XO
FIL0
REXT
VREF
RSV
+3VS
L4100
120Ohm/100Mhz
C4101
0.01UF/16V
C4102
0.1UF/10V
C4103
10UF/6.3V
AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4
AS CLOSE AS POSSIBLE TO R5C832/833
TPBIAS0
C4104
0.01UF/16V
R4101
56Ohm
R4102
56Ohm
C4105
0.33UF/10V
TPBN0
TPBP0
TPAN0
TPAP0
R4104
56Ohm
R4105
56Ohm
C4108
270PF/50V
R4109
5.1KOhm
Circuit area : As small as possible.
AS CLOSE AS POSSIBLE TO
1394 CONNECTOR.
NO37. F8Va PR
TPB0-
TPB0+
TPA0-
TPA0+
TPB0-_1 52
TPB0+_1 52
TPA0-_1 52
TPA0+_1 52
MDIO17
MDIO16
MDIO15
MDIO14
MDIO13
MDIO12
MDIO11
MDIO10
MDIO05
MDIO08
MDIO19
MDIO18
MDIO02
MDIO03
MDIO00
MDIO01
MDIO09
MDIO04
MDIO06
MDIO07
SHIELD GND
CLOCK OF MEMORY MODULE
MDIO06
T4100
TPC26T
NO5. F8Va SR
R4110
22Ohm
Double trace spaceing with other signal
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
<Variant Name>
Title : RICOH R5C832/PCI_A
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F8Va
Rev 1.0
Date: Tuesday, October 07, 2008
Sheet 41 of 94



To correct the problem when MS Duo adaptor is in use.



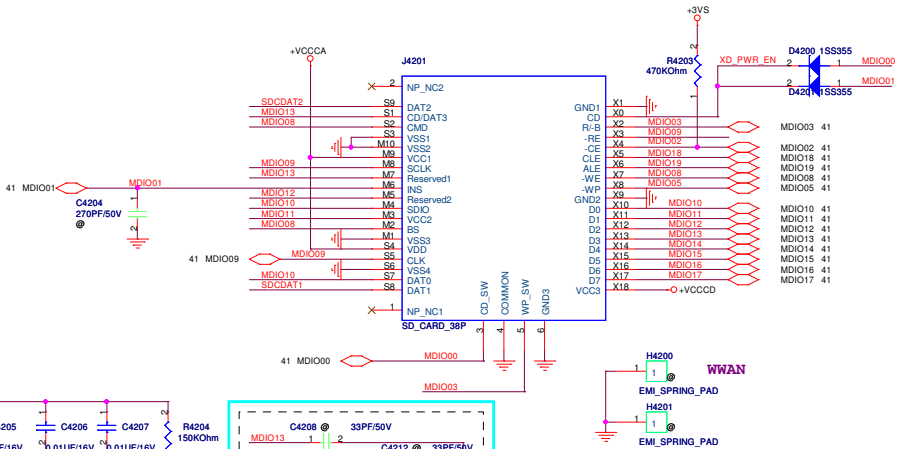
Solve MS Duo Adaptor short issue.

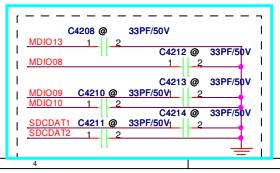


A8ES.PR
Change to 07G005000214, 2KV ESD

MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE





NO17. F8Va SR
Impact MS function

F8S.PR
EMI

<Variant Name>

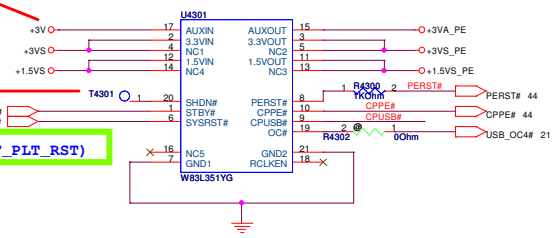
ASUSTeK COMPUTER INC	Title : CardReader	
	Engineer:	
Size: Custom	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 42 of 94	

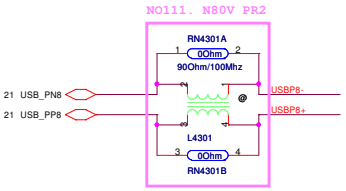
Check
+3VSUS-->+3V

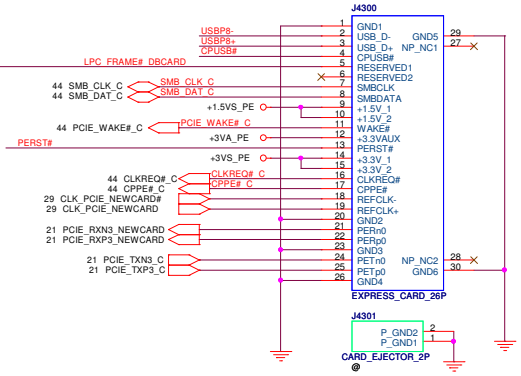
Change RICOH R5538 as 2nd source and Winbond
W83L351YG (06G030091010) put on 1st source.

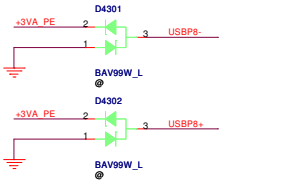
Check
VSUS_ON-->NC or Test point

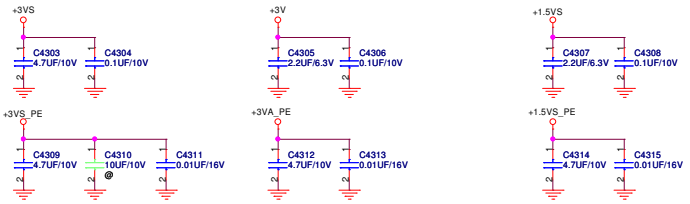
del PCI_RST#(instead of BUF_PLT_RST)











<Variant Name>

ASUSTeK COMPUTER INC

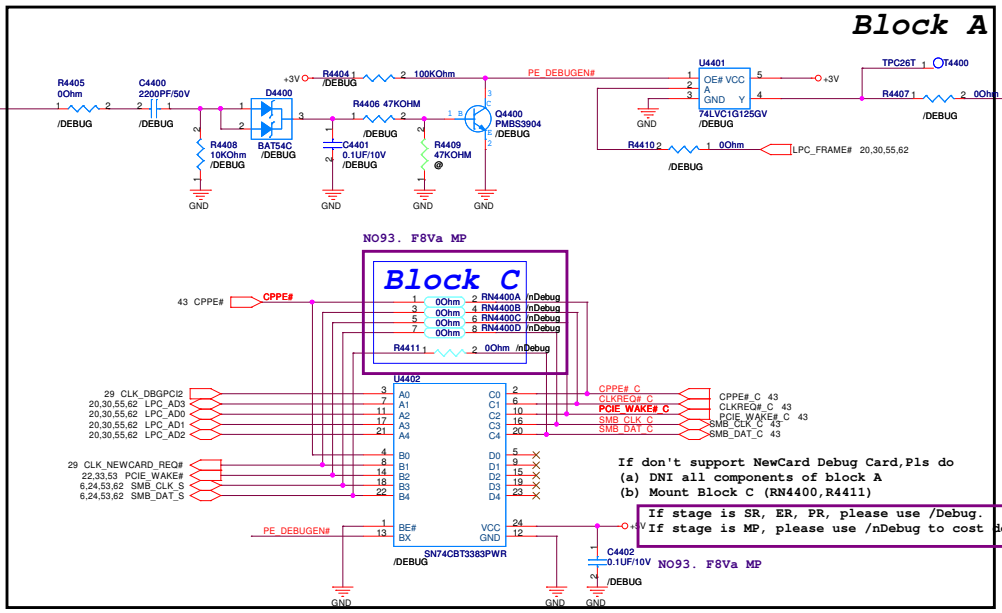
Title : Express Card

Engineer:

Size	Project Name	Rev
Custom	F8Va	1.0

Date: Tuesday, October 07, 2008 Sheet 43 of 94

ABES.PR
Delete NewCars/LPC



<Variant Name>

ASUSTeK COMPUTER INC

Title : Express Card

Engineer:

Size	Project Name	Rev
Custom	F8Va	1.0

Date: Tuesday, October 07, 2008 Sheet 44 of 94

Check stub

+3VS 3,6,7,8,11,14,15,20,21,22,23,24,25,29,30,31,33,36,38,40,41,42,43,46,48,50,51,53,55,57,62,63,70,80,91,92
+3VSUS 20,21,22,23,30,33,81
+12VS 24,32,38,48,57,62,70,91

70 LVDS_U0P — LVDS_YA0P
70 LVDS_U0N — LVDS_YA0N
70 LVDS_U1P — LVDS_YA1P
70 LVDS_U1N — LVDS_YA1N
70 LVDS_U2P — LVDS_YA2P
70 LVDS_U2N — LVDS_YA2N
70 LVDS_UCLKP — LVDS_CLKAP
70 LVDS_UCLKN — LVDS_CLKAN
70 LVDS_L0P — LVDS_YB0P
70 LVDS_L0N — LVDS_YB0N
70 LVDS_L1P — LVDS_YB1P
70 LVDS_L1N — LVDS_YB1N
70 LVDS_L2P — LVDS_YB2P
70 LVDS_L2N — LVDS_YB2N
70 LVDS_LCLKP — LVDS_CLKBP
70 LVDS_LCLKN — LVDS_CLKBN

change to 12G17001030P

J4501 WTOB_CON_30P

+3VS — C4500 0.1UF/16V

+3VS — R4502 10KOhm — R4500 10KOhm

11 EDID_CLK_GM — R4501 0Ohm
11 EDID_DAT_GM — R4503 /GM 0Ohm /GM
70 EDID_CLK_PEG
70 EDID_DATA_PEG

+LCD_VCC — +3VS — EDID_CLK — EDID_DATA

C4501 100PF/50V — C4502 100PF/50V

LVDS_YB0N — LVDS_YA0N
LVDS_YB0P — LVDS_YA0P
LVDS_YB1N — LVDS_YA1N
LVDS_YB1P — LVDS_YA1P
LVDS_YB2N — LVDS_YA2N
LVDS_YB2P — LVDS_YA2P
LVDS_CLKBN — LVDS_CLKAN
LVDS_CLKBP — LVDS_CLKAP

NO140. N81SR

NO64. F8Va PR — NO64. F8Va PR

LVDS_CLKBN — C4511 33PF/50V — C4510 6.2PF/50V — C4517 /3G 33PF/50V
LVDS_CLKBP
LVDS_CLKAN — C4519 33PF/50V — C4518 6.2PF/50V — C4520 /3G 33PF/50V
LVDS_CLKAP

The Caps will impact on LVDS signal!!

NO80. F8Va MP

D4503 1SS355 — R4517 100Ohm

+3V — R4513 100KOHM
+12VS — R4519 100KOHM — R4514 10KOhm
+3VS — Q4503 PMN45EN
Q4500A UM6K1N

+LCD_VCC — L4504 80Ohm/100Mhz

11 L_VDDEN — /GM R4518 0Ohm — LCD_VDD_EN_PEG — Q4500B UM6K1N
70 LCD_VDD_EN_PEG
R4516 10KOhm

C4512 0.1UF/25V — C4513 0.1UF/16V — C4516 0.1UF/16V — C4515 10UF/10V — C4514 10UF/10V

NO128. N81SR

+3VS — U4503 G5243T11U — +LCD_VCC
IN2 — OUT — GND — EN — IN1
LCD_VDD_EN_PEG

power suggest

V1V

AC_BAT_SYS_INV — L4509 80Ohm/100Mhz/VBL — C4503 22UF/25V

11 L_BKLT_CTRL — /GM R4511 0Ohm
30 LCD_BL_PWM — /PM R4514 0Ohm — R4507 100KOHM — L4502 1KOhm/100Mhz — C4505 0.1UF/16V — C4504 100PF/50V

NO25. F8Va SR

+LCD_VCC — L4503 1KOhm/100Mhz

30,31,56 LID_SW# — LID_SW# — D4501 RB717F
30 LCD_BACKOFF# — /GM R4510 0Ohm — D4502 1SS355
11 L_BKLTEN
70 LCD_BACKEN_PEG
R4512 PBS.ER 10KOhm

AC_BAT_SYS_INV — VBL — Q4504 IRLML5103PBF — R4520 100KOHM — Q4505 2N7002K_T1_E3

NO126. N81SR

NO31. F8Va PR — J4502 WTOB_CON_7P
VCC1 VCC2 GND1 GND2 VREF BKEN PWM

INVERTOR CNT

05/02 For N80V

Magnatic Switch For LID_SW# On/OFF Close to SW5605

+3VA — U4502 /N80V — VDD GND OUTPUT — A3212ELHLT
NO89. F8Va MP — LIDSW# — C4523 10PF/50V — C4524 0.1UF/10V /N80V

NO89. F8Va MP

Close to SW5605 For N80 project

05/02 For F8V

Magnatic Switch For LID_SW# On/OFF

+3VA — U4501 /F8V — VDD GND OUTPUT — A3212ELHLT
NO89. F8Va MP — 31 LIDSW# — C4521 10PF/50V — C4522 0.1UF/10V /F8V

<Variant Name>

ASUSTeK COMPUTER INC

Title : LVDS & Inverter
Engineer:

Size	Project Name	Rev
Custom	F8Va	1.0

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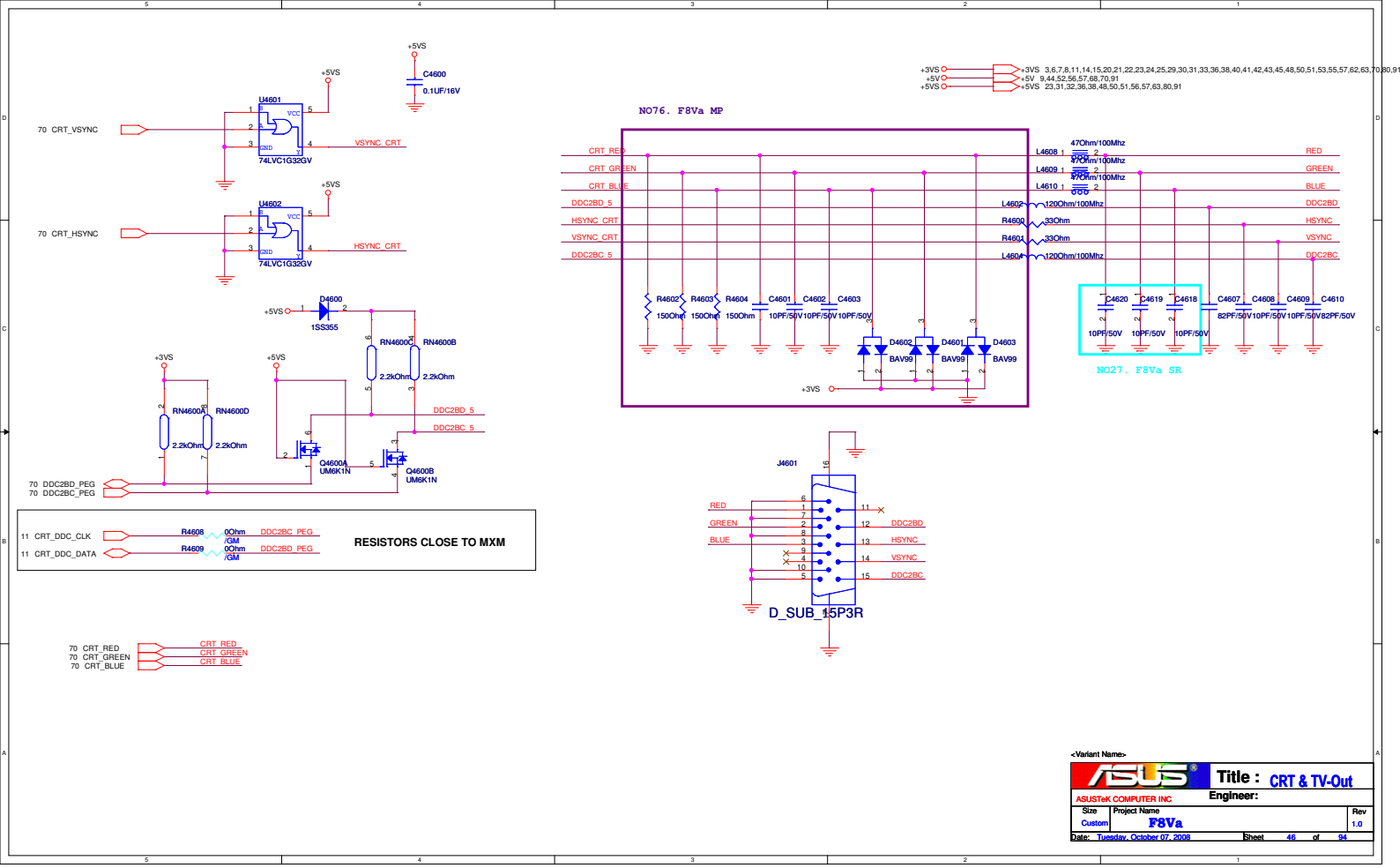

<Variant Name>

ASUSTeK COMPUTER INC

Title : CRT & TV-Out

Engineer:

Size	Project Name	Rev
Custom	F8Va	1.0

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<Variant Name>

Title : DVI-*****

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
B	F8Va	1.0

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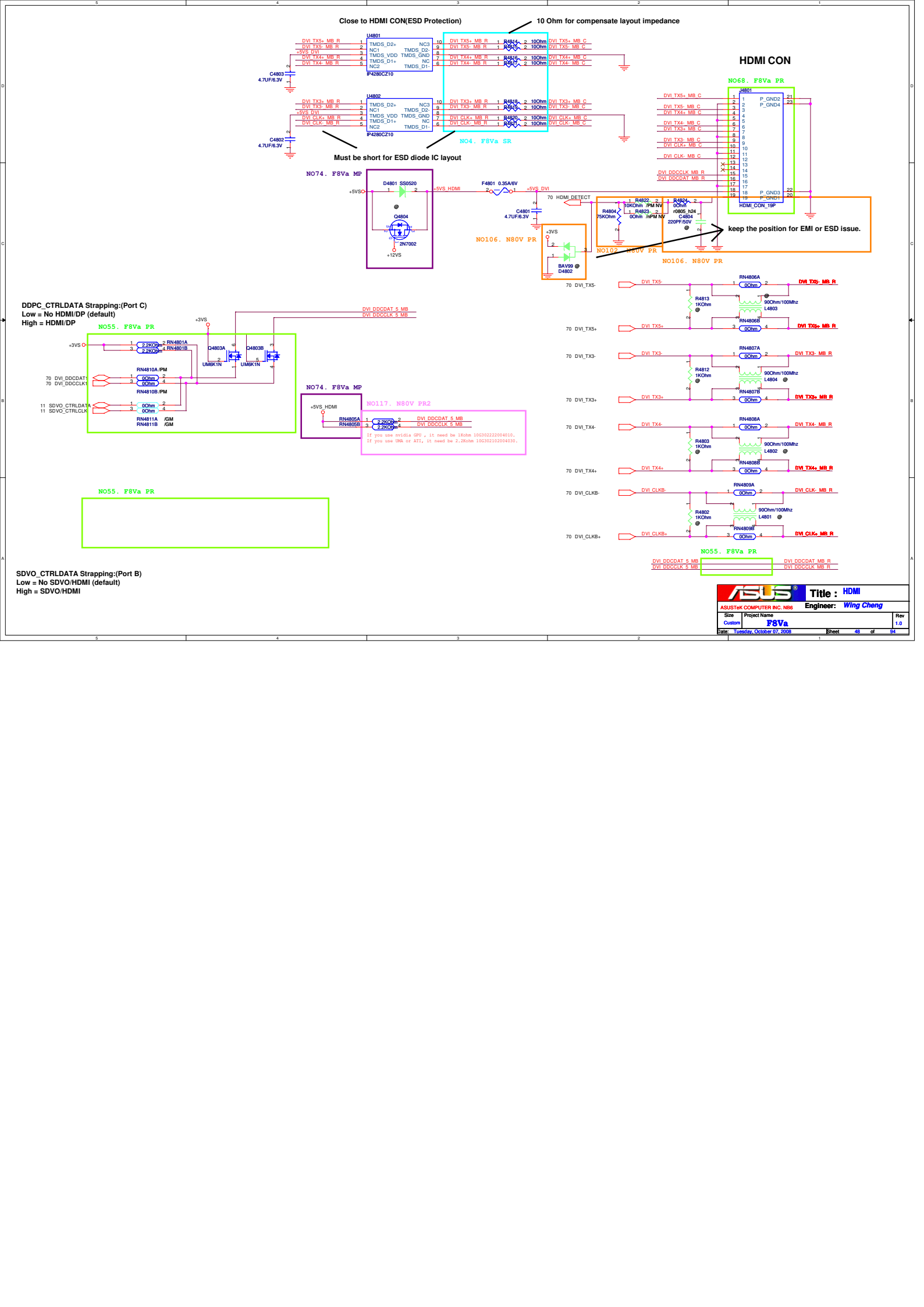
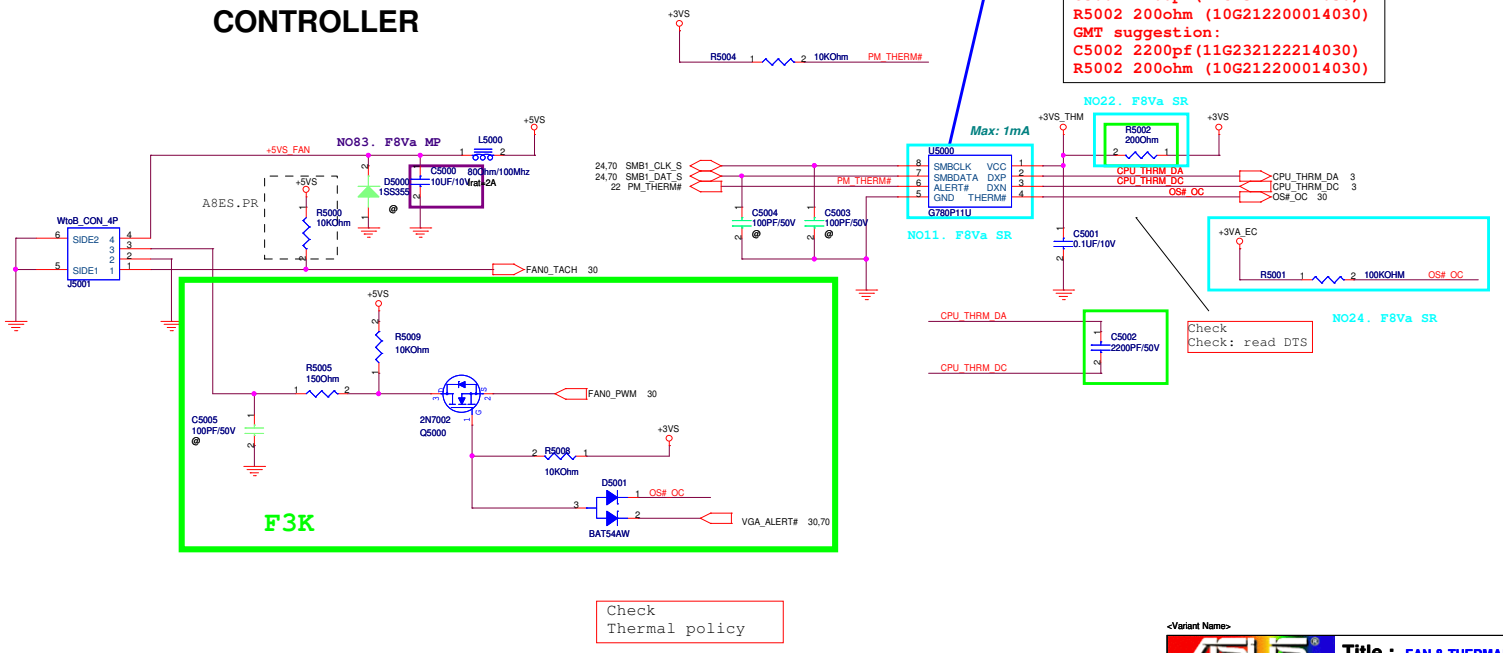

Close to HDMI CON(ESD Protection)
10 Ohm for compensate layout impedance
HDMI CON
U4801
U4802
IP4280CZ10
C4803 4.7UF/6.3V
C4802 4.7UF/6.3V
NO4. F8Va SR
Must be short for ESD diode IC layout
NO74. F8Va MP
D4801 SS0520
Q4804
2N7002
+5VS_HDMI
F4801 0.35A/6V
+5VS_DVI
C4801 4.7UF/6.3V
70 HDMI_DETECT
R4804 75KOhm
R4822 10KOhm /PM NV
R4823 0Ohm /nPM NV
C4804 220PF/50V
R4824 0Ohm r0805_h24
HDMI_CON_19P
keep the position for EMI or ESD issue.
NO106. N80V PR
NO102. N80V PR
BAV99 @ D4802
NO68. F8Va PR
DDPC_CTRLDATA Strapping:(Port C)
Low = No HDMI/DP (default)
High = HDMI/DP
NO55. F8Va PR
RN4801A 2.2KOhm
RN4801B 2.2KOhm
Q4803A UM6K1N
Q4803B UM6K1N
RN4810A /PM 0Ohm
RN4810B /PM 0Ohm
RN4811A /GM 0Ohm
RN4811B /GM 0Ohm
RN4805A 2.2KOhm
RN4805B 2.2KOhm
If you use nvidia GPU , it need be 1Kohm 10G302222004010.
If you use UMA or ATI, it need be 2.2Kohm 10G302102004030.
SDVO_CTRLDATA Strapping:(Port B)
Low = No SDVO/HDMI (default)
High = SDVO/HDMI
RN4806A 0Ohm
RN4806B 0Ohm
RN4807A 0Ohm
RN4807B 0Ohm
RN4808A 0Ohm
RN4808B 0Ohm
RN4809A 0Ohm
RN4809B 0Ohm
R4813 1KOhm
R4812 1KOhm
R4803 1KOhm
R4802 1KOhm
90Ohm/100Mhz L4803
90Ohm/100Mhz L4804
90Ohm/100Mhz L4802
90Ohm/100Mhz L4801
Title : HDMI
ASUSTeK COMPUTER INC. NB6
Engineer: Wing Cheng
Size: Custom
Project Name: F8Va
Rev: 1.0
Date: Tuesday, October 07, 2008
Sheet 48 of 94

ASUSTeK COMPUTER INC. NB6	Title :	
	Engineer: Wing Cheng	
Size: A	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 49 of 94	

FAN & THERMAL CONTROLLER

For Penryn CPU:
1st source: 06G023096010 TEMP.SENSOR G780P11U SOP-8 GMT
2nd source: 06G023026012 TEMP SENSOR MAX6657YMS+ SOP-8 MAXIM

MAXIM suggestion:
C5002 2200pf(11G232122214030)
R5002 200ohm (10G212200014030)
GMT suggestion:
C5002 2200pf(11G232122214030)
R5002 200ohm (10G212200014030)



Check
Thermal policy

<Variant Name>

ASUSTeK COMPUTER INC

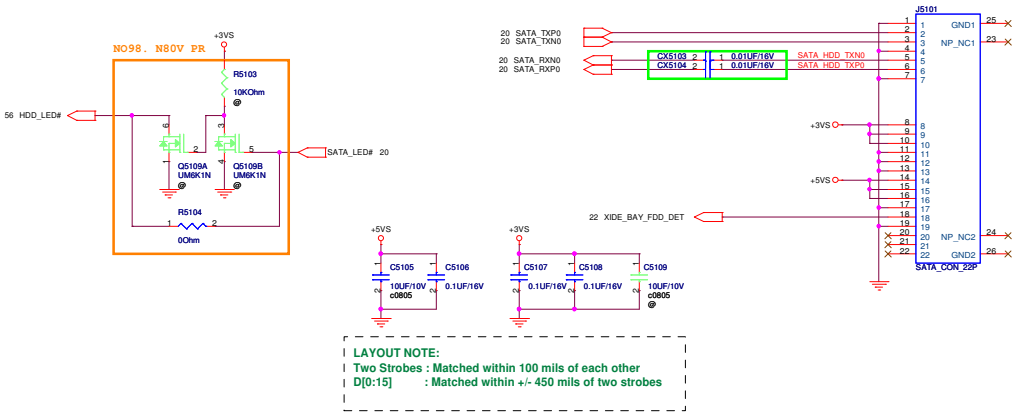
Title : FAN & THERMAL

Engineer:

Size	Project Name	Rev
B	F8Va	1.0

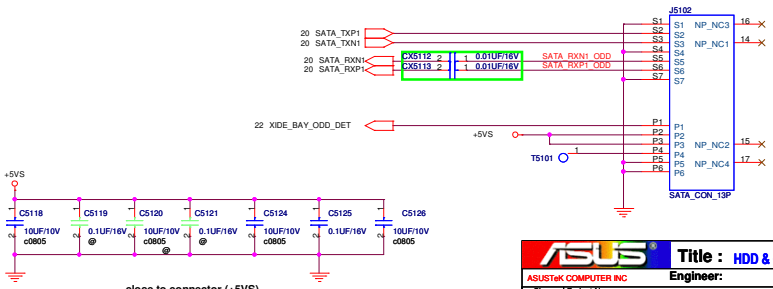
Date: Tuesday, October 07, 2008 Sheet 50 of 94

SATA HDD CON



LAYOUT NOTE:
Two Strobes : Matched within 100 mils of each other
D[0:15] : Matched within +/- 450 mils of two strobes

SATA ODD CON

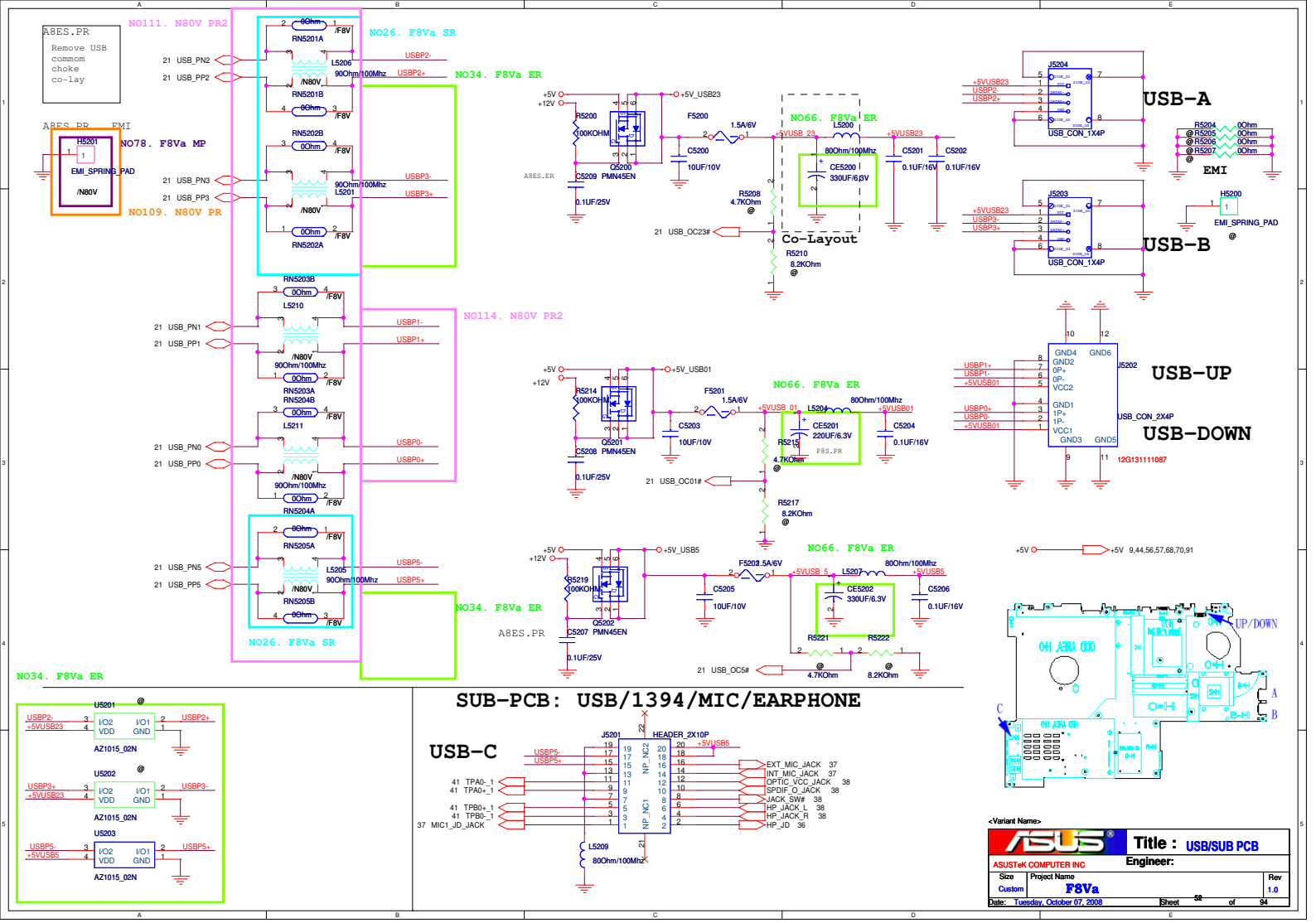


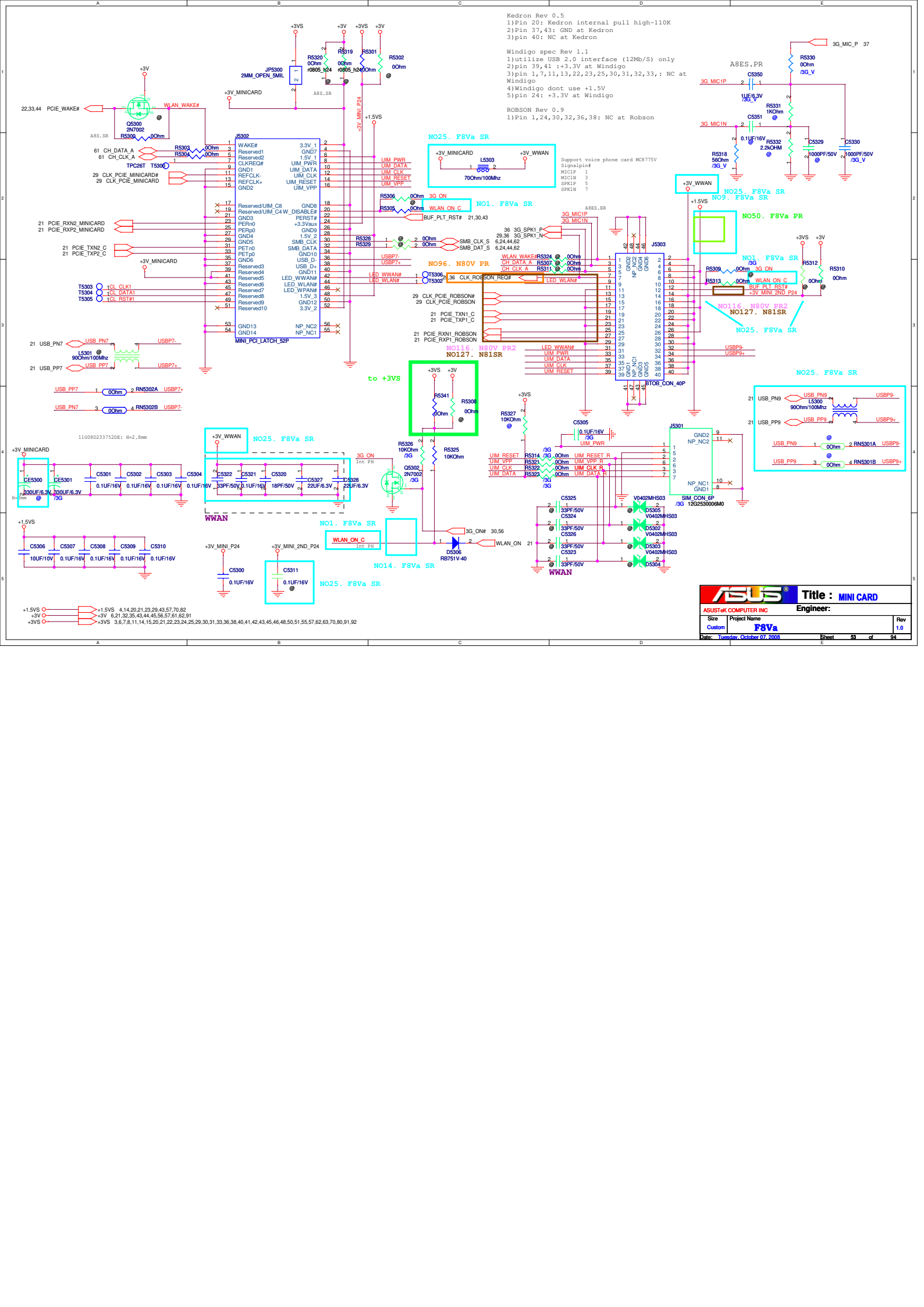
close to connector (+5VS)

Title :	HDD & ODD
ASUSTeK COMPUTER INC	Engineer:
Size: Custom	Project Name: F8Va
Rev: 1.0	
Date: Tuesday, October 07, 2008	Sheet 81 of 94

+3VS
+5VS
+5V

+3VS 3,6,7,8,11,14,15,20,21,22,23,24,25,29,30,31,33,36,38,40,41,42,43,45,46,48,50,53,55,57,62,63,70,80,91,92
+5VS 23,31,32,36,38,46,48,50,56,57,63,80,91
+5V 9,44,52,56,57,68,70,91


A8ES.PR
Remove USB common choke co-lay
NO111. N80V PR2
NO26. F8Va SR
NO78. F8Va MP
NO109. N80V PR
NO114. N80V PR2
NO34. F8Va ER
NO66. F8Va ER
USB-A
USB-B
USB-UP
USB-DOWN
EMI
Co-Layout
USB_CON_1X4P
USB_CON_2X4P
EMI_SPRING_PAD
12G1311111087
SUB-PCB: USB/1394/MIC/EARPHONE
USB-C
HEADER_2X10P
AZ1015_02N
Title : USB/SUB PCB
Engineer:
ASUSTeK COMPUTER INC
Project Name
F8Va
Rev
1.0
Tuesday, October 07, 2008
Sheet 52 of 94


Kedron Rev 0.5
1)Pin 20: Kedron internal pull high~110K
2)Pin 37,43: GND at Kedron
3)pin 40: NC at Kedron
Windigo spec Rev 1.1
1)utilize USB 2.0 interface (12Mb/S) only
2)pin 39,41 :+3.3V at Windigo
3)pin 1,7,11,13,22,23,25,30,31,32,33,: NC at Windigo
4)Windigo dont use +1.5V
5)pin 24: +3.3V at Windigo
ROBSON Rev 0.9
1)Pin 1,24,30,32,36,38: NC at Robson
NO25. F8Va SR
NO1. F8Va SR
NO96. N80V PR
NO116. N80V PR2
NO127. N81SR
NO50. F8Va PR
NO9. F8Va SR
NO14. F8Va SR
to +3VS
WWAN
MINI_PCI_LATCH_52P
BTOB_CON_40P
SIM_CON_6P
Title : MINI CARD
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
F8Va
Rev
1.0
Date: Tuesday, October 07, 2008
Sheet 53 of 94

Title : BLANK

ASUSTeK COMPUTER INC

Engineer:

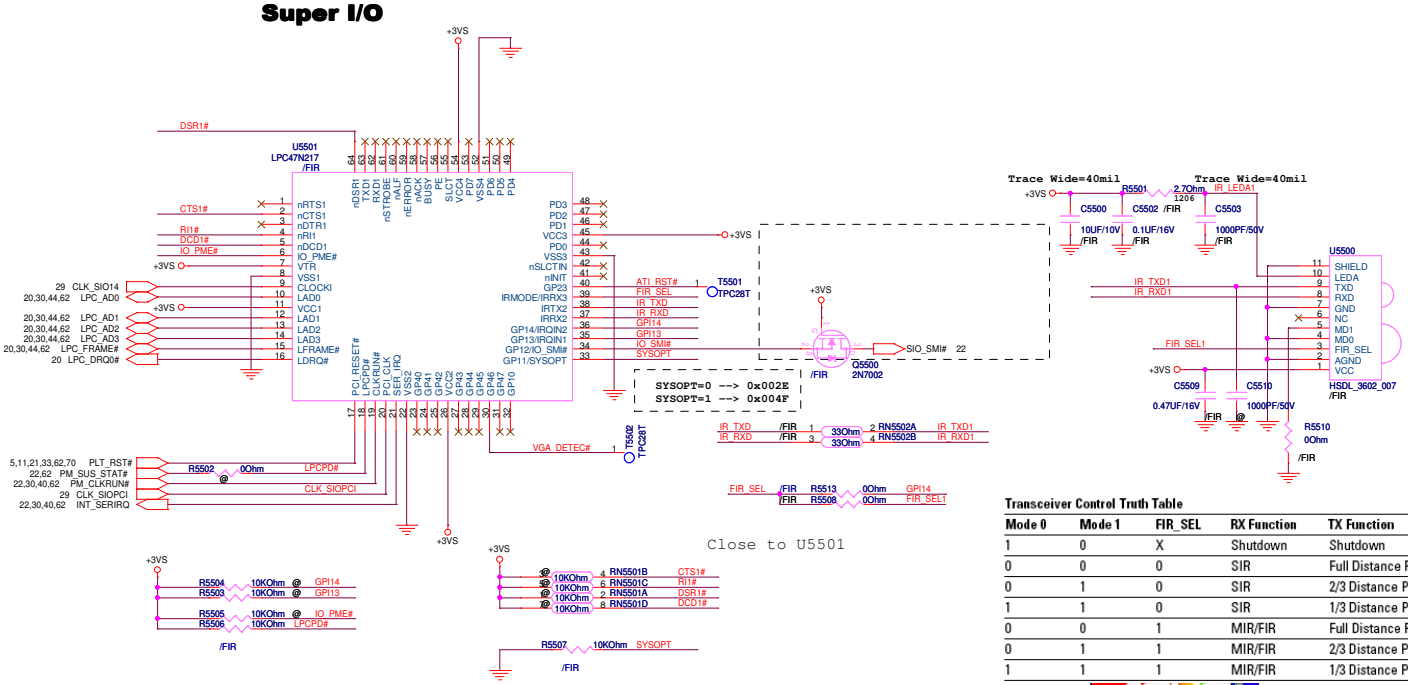
Size	Project Name	Rev
Custom	F8Va	1.0

Date: Tuesday, October 07, 2008 Sheet 54 of 94

CIR
04G231020500
TSOP6238TR

NO58. F8Va PR
NO96. N80V PR
F8S.PR NO58. F8Va PR
+5VA0: is more easy then +5VA for layout

Super I/O



Transceiver Control Truth Table

Mode 0	Mode 1	FIR_SEL	RX Function	TX Function
1	0	X	Shutdown	Shutdown
0	0	0	SIR	Full Distance Power
0	1	0	SIR	2/3 Distance Power
1	1	0	SIR	1/3 Distance Power
0	0	1	MIR/FIR	Full Distance Power
0	1	1	MIR/FIR	2/3 Distance Power
1	1	1	MIR/FIR	1/3 Distance Power

ASUSTeK COMPUTER INC
Title : IrDA
Engineer:
Size: B
Project Name: F8Va
Rev: 1.0
Date: Tuesday, October 07, 2008
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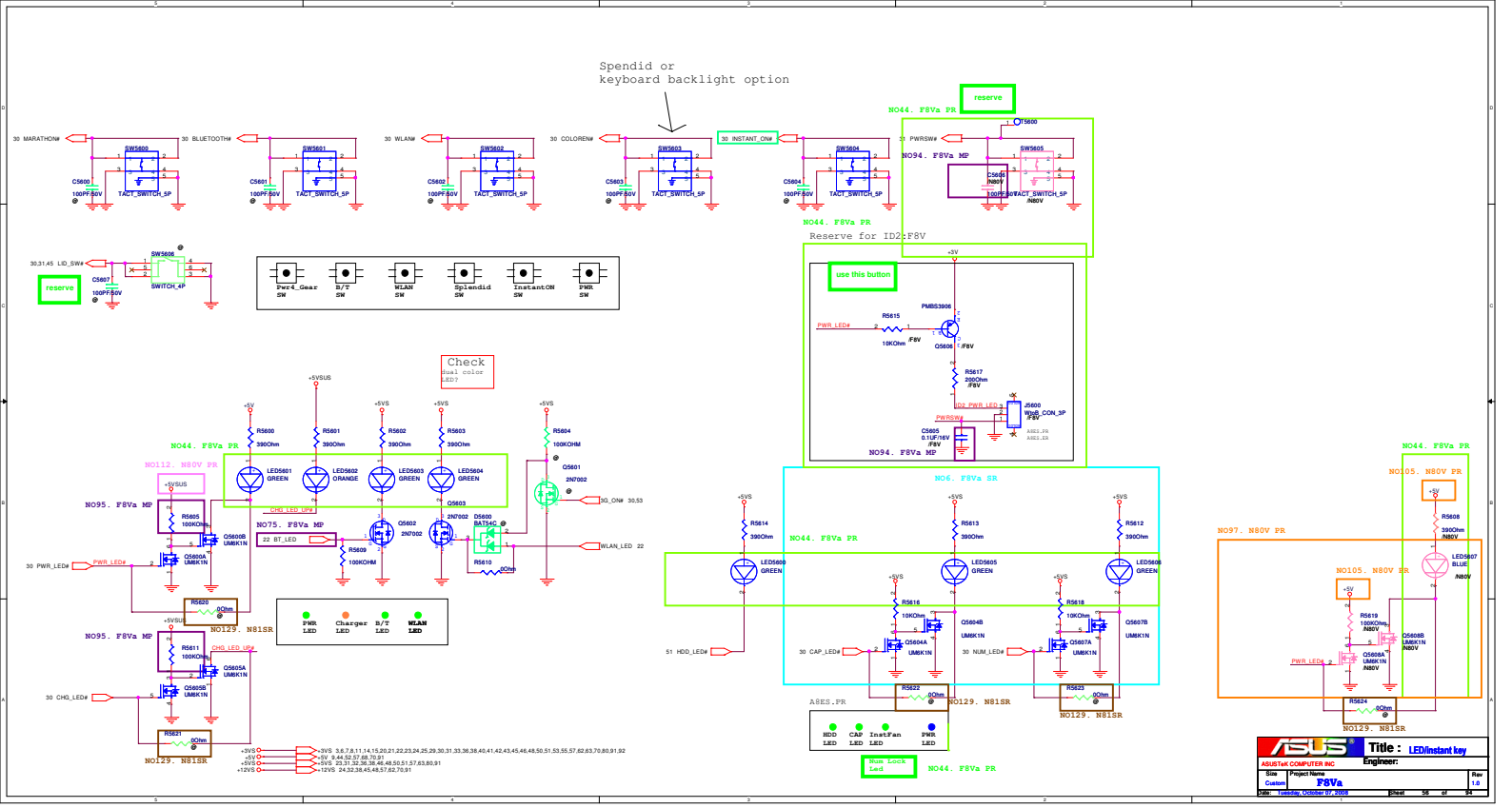
Spendid or
keyboard backlight option
30 MARATHON#
30 BLUETOOTH#
30 WLAN#
30 COLOREN#
30 INSTANT_ON#
31 PWRSW#
SW5600
SW5601
SW5602
SW5603
SW5604
SW5605
C5600
C5601
C5602
C5603
C5604
C5605
100PF/50V
TACT_SWITCH_5P
N80V
NO44. F8Va PR
reserve
NO94. F8Va MP
Reserve for ID2:F8V
30,31,45 LID_SW#
SW5606
C5607
SWITCH_4P
Pwr4_Gear SW
B/T SW
WLAN SW
Splendid SW
InstantON SW
PWR SW
use this button
PMBS3906
R5615
10KOhm
PWR_LED#
Q5606
R5617
200Ohm
ID2_PWR_LED_R
J5600
Wake_CON_SP
PWRSW#
C5605
0.1UF/16V
NO6. F8Va SR
Check
dual color LED?
+5VSUS
+5V
+5VS
R5600
R5601
R5602
R5603
R5604
390Ohm
100KOHM
LED5601
GREEN
LED5602
ORANGE
LED5603
GREEN
LED5604
GREEN
Q5601
2N7002
3G_ON# 30,53
NO112. N80V PR
NO95. F8Va MP
R5605
100KOhm
Q5606B
UM6K1N
Q5606A
UM6K1N
30 PWR_LED#
PWR_LED#
CHG_LED_UP#
NO75. F8Va MP
22 BT_LED
Q5602
2N7002
Q5603
2N7002
D5600
BAT54C
R5609
100KOHM
R5610
0Ohm
WLAN_LED 22
R5620
0Ohm
NO129. N81SR
PWR LED
Charger LED
B/T LED
WLAN LED
R5611
100KOhm
Q5605B
UM6K1N
Q5605A
UM6K1N
30 CHG_LED#
R5621
0Ohm
NO129. N81SR
+3VS 3,6,7,8,11,14,15,20,21,22,23,24,25,29,30,31,33,36,38,40,41,42,43,45,46,48,50,51,53,55,57,62,63,70,80,91,92
+5V 9,44,52,57,68,70,91
+5VS 23,31,32,36,38,46,48,50,51,57,63,80,91
+12VS 24,32,39,45,48,57,62,70,91
R5614
R5613
R5612
LED5609
GREEN
LED5605
GREEN
LED5606
GREEN
51 HDD_LED#
30 CAP_LED#
30 NUM_LED#
R5616
10KOhm
Q5604A
UM6K1N
Q5604B
UM6K1N
Q5607A
UM6K1N
Q5607B
UM6K1N
R5622
0Ohm
R5623
0Ohm
NO129. N81SR
ABES.PR
HDD LED
CAP LED
InstFan LED
PWR LED
Num Lock Led
NO97. N80V PR
NO105. N80V PR
R5608
390Ohm
LED5607
BLUE
R5619
100KOhm
Q5608B
UM6K1N
Q5608A
UM6K1N
R5624
0Ohm
Title : LED/instant key
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
F8Va
Rev
1.0
Date: Tuesday, October 07, 2008
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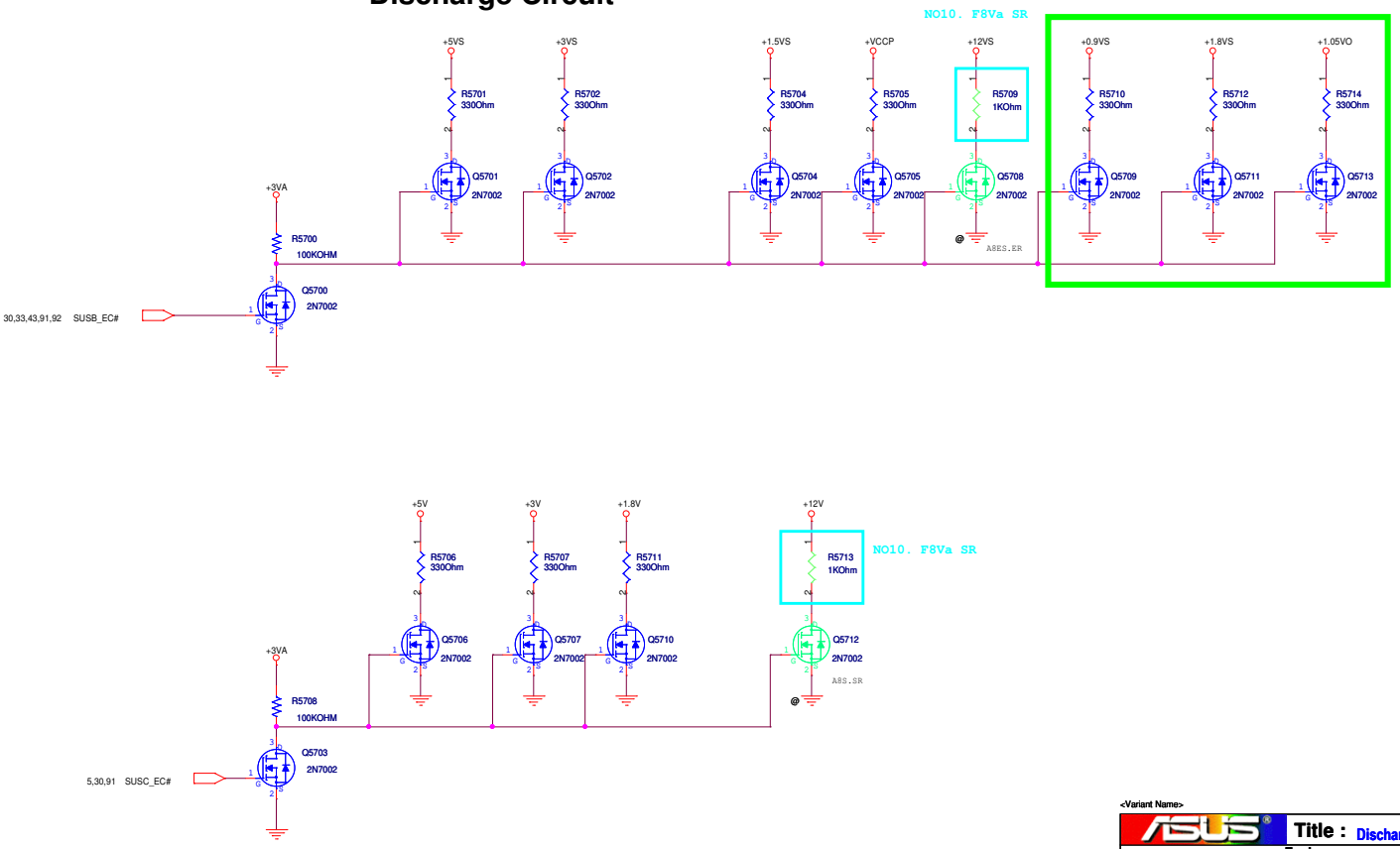
Discharge Circuit



<Variant Name>

ASUSTeK COMPUTER INC

Title : Discharge

Engineer:

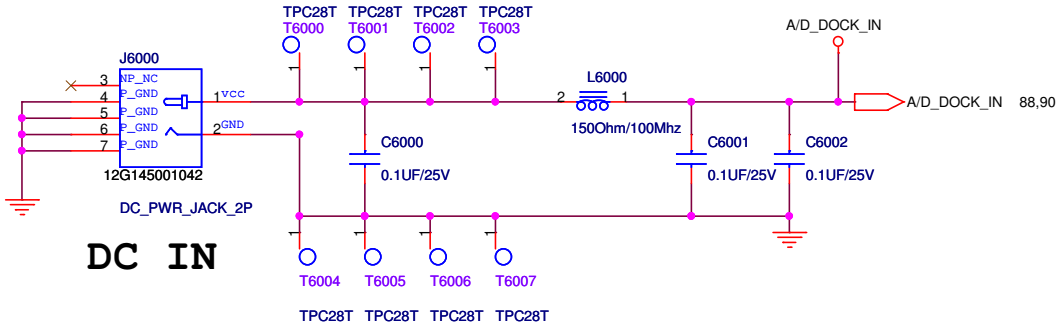
Size	Project Name	Rev
B	F8Va	1.0

Date: Tuesday, October 07, 2008 Sheet 57 of 94

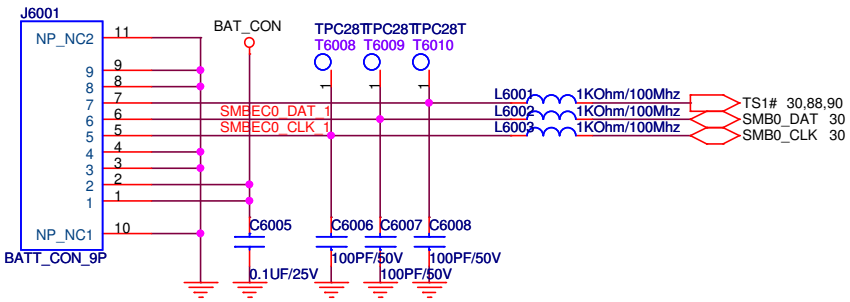
<Variant Name>

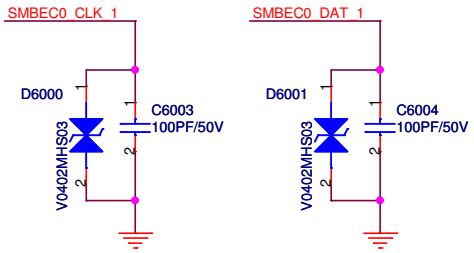
ASUSTeK COMPUTER INC	Title :	
	Engineer:	
Size: A	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet of 94	

Title	<Title>
Size: A	Document Number: F8Va
Rev: 1.0	
Date: Tuesday, October 07, 2008	Sheet 59 of 94



DC IN



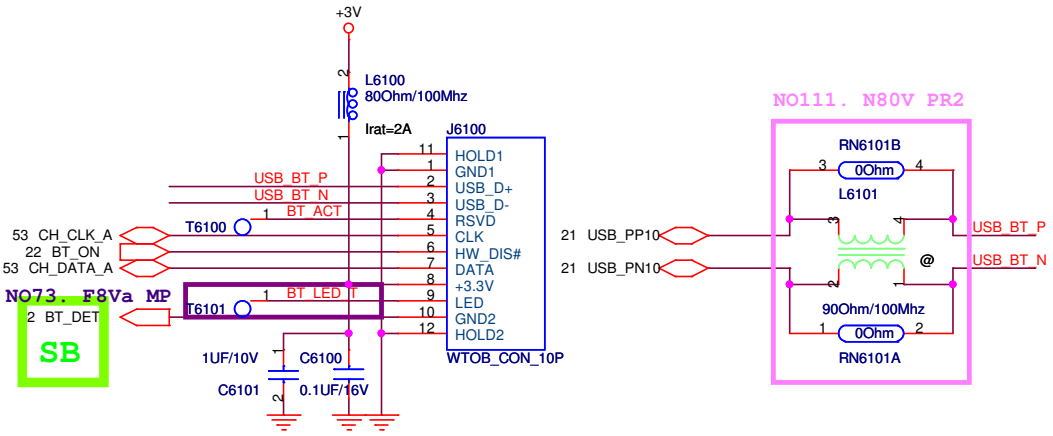


close to connector

Battery Connector

<Variant Name>

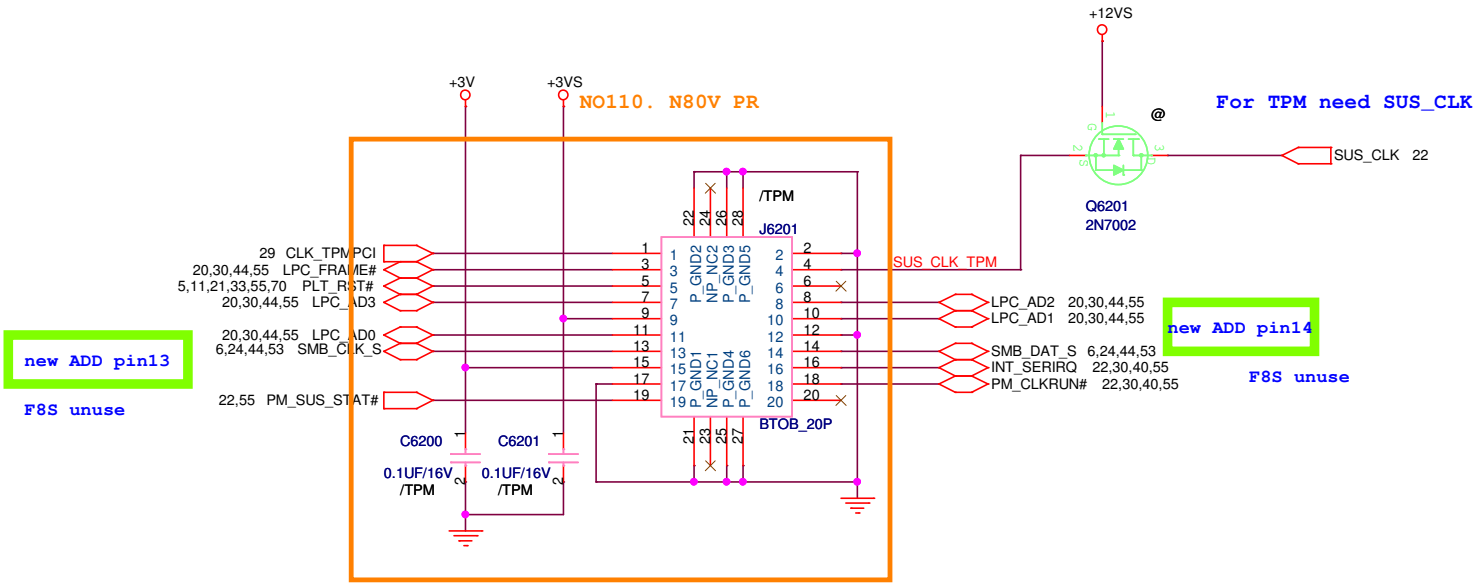
ASUSTeK COMPUTER INC	Title : DC IN / BAT	
	Engineer:	
Size: A	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 60 of 94	



Bluetooth Module CON

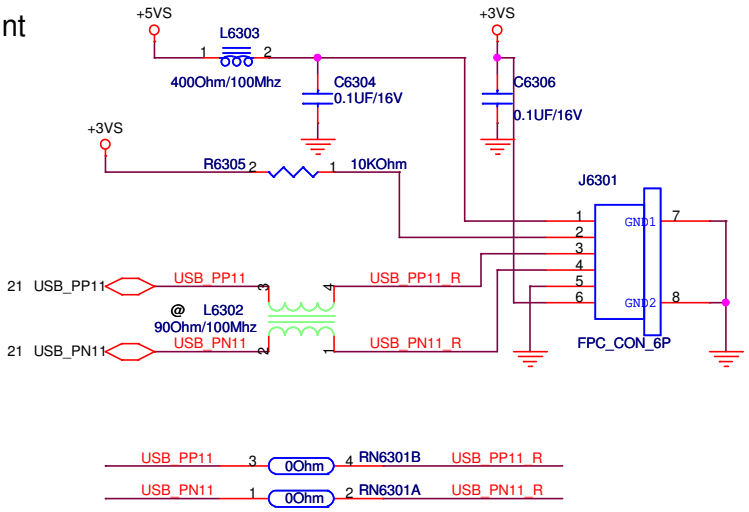
ASUSTeK COMPUTER INC	Title : BT/CAMERA	
	Engineer:	
Size: A	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 61 of 94	

TPM 1.2 Module



ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Wing_Cheng	
Size: A	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 62 of 94	

Finger Print



<Variant Name>

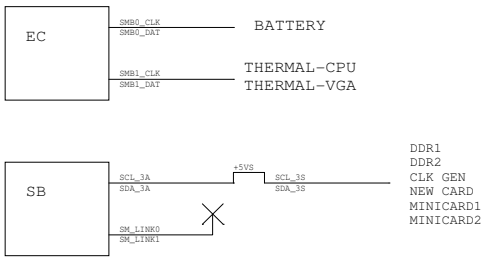
ASUSTeK COMPUTER INC	Title : FingerPrinter	
	Engineer:	
Size: A	Project Name: F8Va	Rev: 1.0
Date: Tuesday, October 07, 2008	Sheet 63 of 94	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARDBUS	AD19	0	F,E

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0 (low)	
SPD/TS	A0/30
SO-DIMM 1(high)	
SPD/TS	A4/34
G781-1	9A
G781(VGA board)	98

Thermal Sensor (CPU)

SM-Bus Mapping 1001100



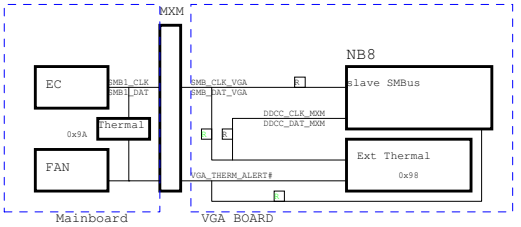
BOM option

```
nGM:yellow
nPM:light red
=========================
@ : no stuff for all
nGM :no stuff for A8E
nPM :no stuff for A8S
nGM1:no stuff for A8E, A8E/SR mount for debuging A8S in advance
3G :for Windigo,SIERRA MC8775V
nA8E  :no stuff Irda for A8E
```

Support ID2:

```
Support ID2:
page 68,Finger print
page 55,IR
Page 56,pwr switch and LED
```

Thermal block diagram



<Variant Name>

ASUSTeK COMPUTER INC

Title :

Engineer:

Size	Project Name	Rev
B	F8Va	1.0

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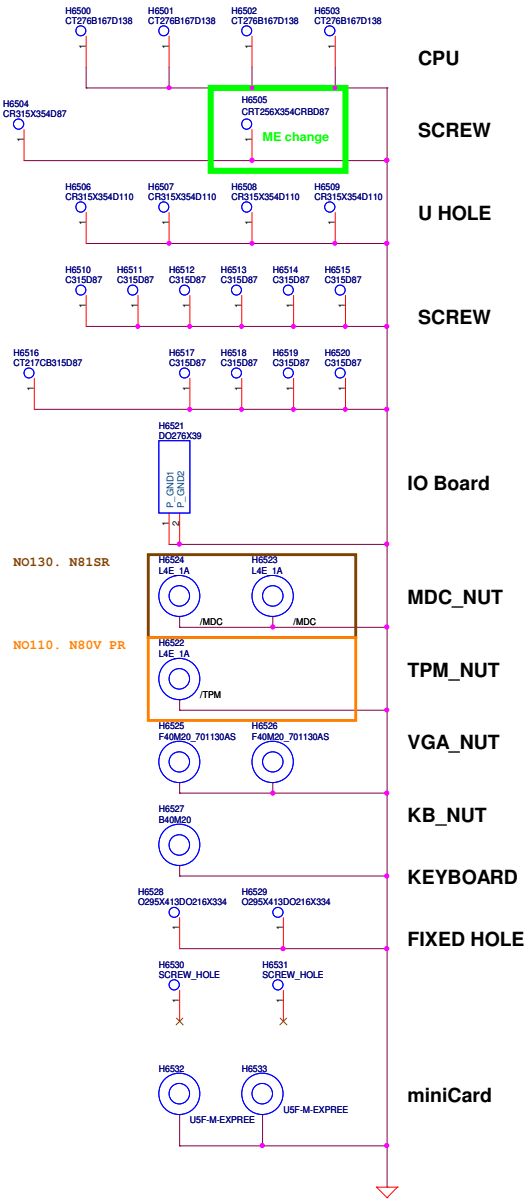
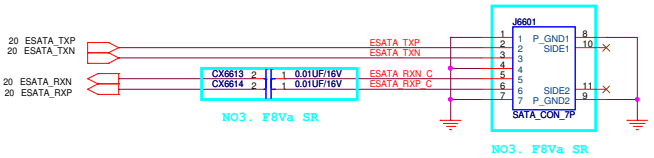


Title	<Title>		
Size	Document Number		Rev
	CustomF8Va		1.0
Date:	Tuesday, October 07, 2008	Sheet 65 of 94	



PIN		FUNCTION
1	Gnd	
2	A+	Differential signal pair from host controller
3	A-	
4	Gnd	
5	B-	Differential signal pair to host controller
6	B+	
7	Gnd	

ASUSTeK COMPUTER INC

Title : E-SATA

Engineer:

Size	Project Name	Rev
B	F8Va	1.0

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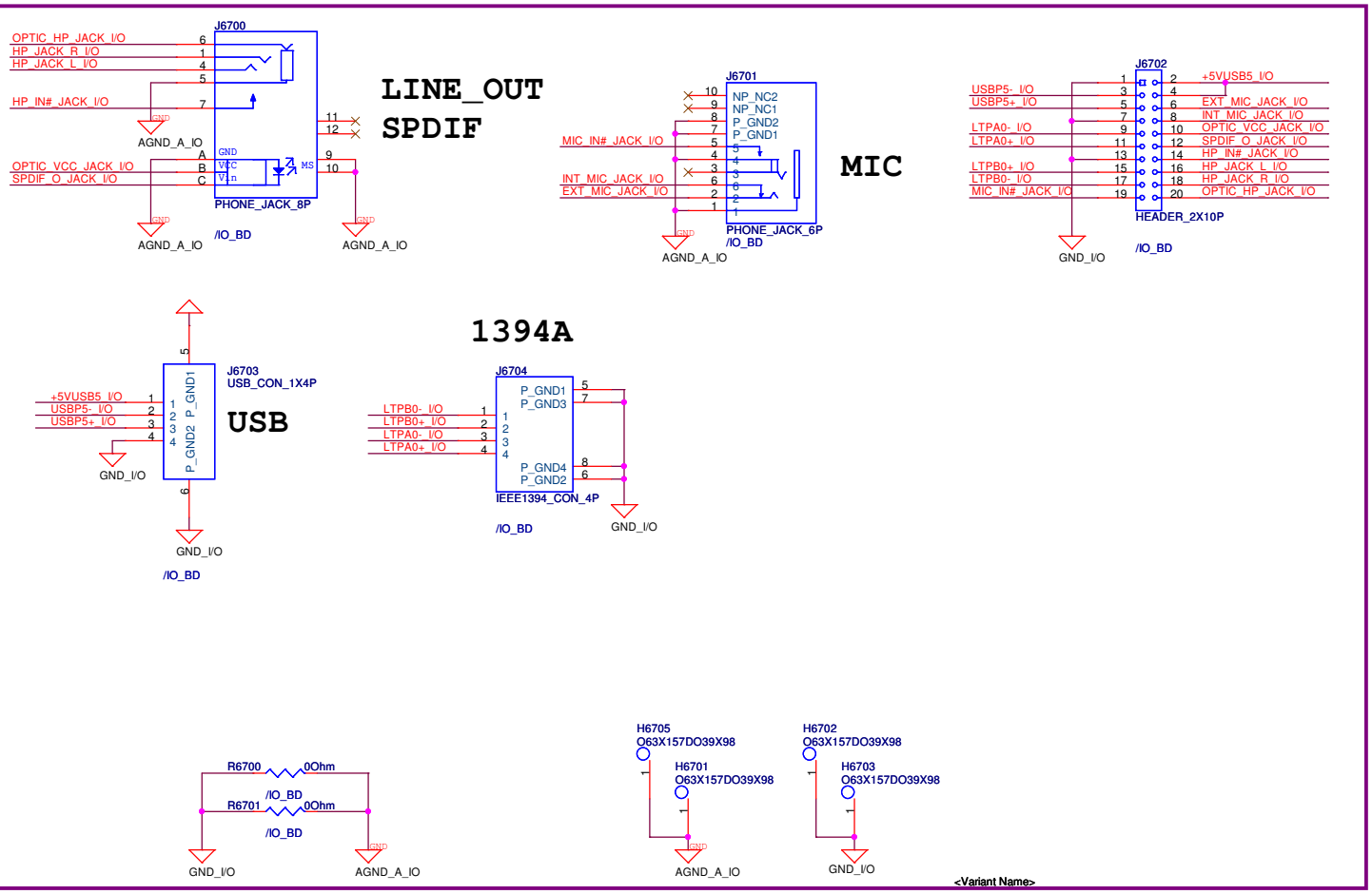

<Variant Name>

ASUSTeK COMPUTER INC

Title : SUB_PCB

Engineer:

Size	Project Name	Rev
A4	F8Va	1.0

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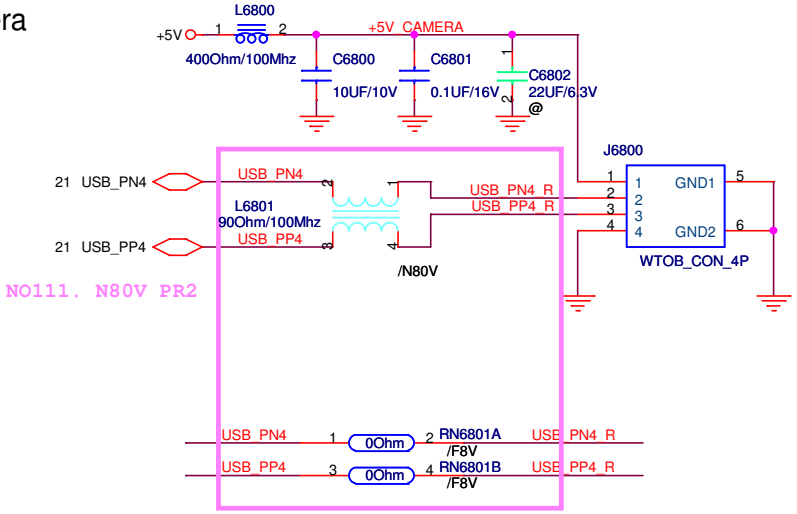
Camera



<Variant Name>

ASUSTeK COMPUTER INC

Title : CAMERA

Engineer:

Size	Project Name	Rev
A	F8Va	1.0

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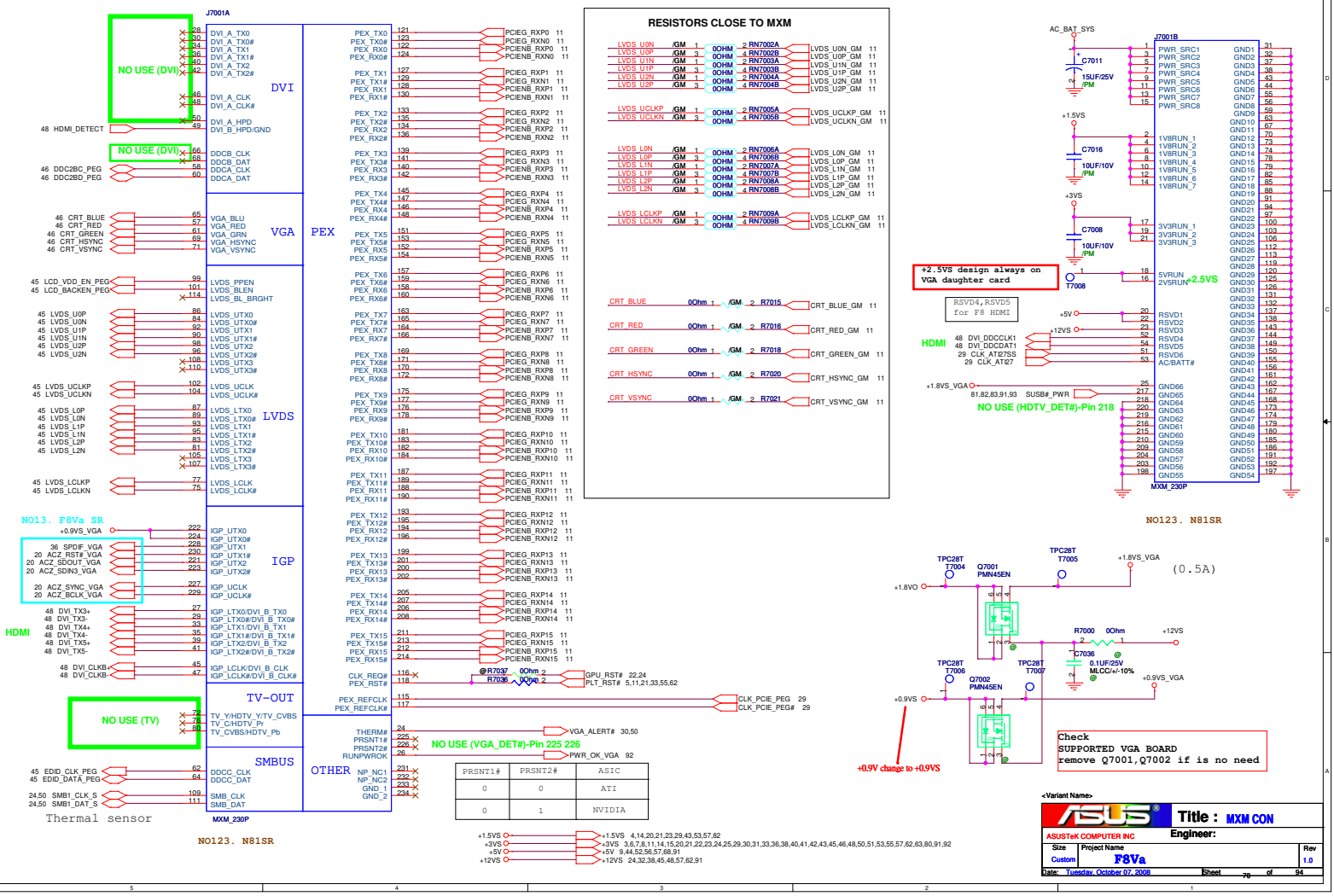
Title :	Other
ASUSTeK COMPUTER INC	Engineer:
Size: A	Project Name: F8Va
Rev: 1.0	
Date: Tuesday, October 07, 2008	Sheet 69 of 94


J7001A
NO USE (DVI)
DVI_A_TX0
DVI_A_TX0#
DVI_A_TX1
DVI_A_TX1#
DVI_A_TX2
DVI_A_TX2#
DVI
DVI_A_CLK
DVI_A_CLK#
DVI_A_HPD
DVI_B_HPD/GND
48 HDMI_DETECT
NO USE (DVI)
DDCB_CLK
DDCB_DAT
46 DDC2BC_PEG
DDCA_CLK
46 DDC2BD_PEG
DDCA_DAT
46 CRT_BLUE
46 CRT_RED
46 CRT_GREEN
46 CRT_HSYNC
46 CRT_VSYNC
VGA_BLU
VGA_RED
VGA_GRN
VGA_HSYNC
VGA_VSYNC
VGA
PEX
45 LCD_VDD_EN_PEG
45 LCD_BACKEN_PEG
LVDS_PPEN
LVDS_BLEN
LVDS_BL_BRGHT
45 LVDS_U0P
45 LVDS_U0N
45 LVDS_U1P
45 LVDS_U1N
45 LVDS_U2P
45 LVDS_U2N
LVDS_UTX0
LVDS_UTX0#
LVDS_UTX1
LVDS_UTX1#
LVDS_UTX2
LVDS_UTX2#
LVDS_UTX3
LVDS_UTX3#
45 LVDS_UCLKP
45 LVDS_UCLKN
LVDS_UCLK
LVDS_UCLK#
45 LVDS_L0P
45 LVDS_L0N
45 LVDS_L1P
45 LVDS_L1N
45 LVDS_L2P
45 LVDS_L2N
LVDS_LTX0
LVDS_LTX0#
LVDS_LTX1
LVDS_LTX1#
LVDS_LTX2
LVDS_LTX2#
LVDS_LTX3
LVDS_LTX3#
LVDS
45 LVDS_LCLKP
45 LVDS_LCLKN
LVDS_LCLK
LVDS_LCLK#
NO13. F8Va SR
+0.9VS_VGA
36 SPDIF_VGA
20 ACZ_RST#_VGA
20 ACZ_SDOUT_VGA
20 ACZ_SDIN3_VGA
20 ACZ_SYNC_VGA
20 ACZ_BCLK_VGA
IGP_UTX0
IGP_UTX0#
IGP_UTX1
IGP_UTX1#
IGP_UTX2
IGP_UTX2#
IGP_UCLK
IGP_UCLK#
IGP
HDMI
48 DVI_TX3+
48 DVI_TX3-
48 DVI_TX4+
48 DVI_TX4-
48 DVI_TX5+
48 DVI_TX5-
IGP_LTX0/DVI_B_TX0
IGP_LTX0#/DVI_B_TX0#
IGP_LTX1/DVI_B_TX1
IGP_LTX1#/DVI_B_TX1#
IGP_LTX2/DVI_B_TX2
IGP_LTX2#/DVI_B_TX2#
48 DVI_CLKB+
48 DVI_CLKB-
IGP_LCLK/DVI_B_CLK
IGP_LCLK#/DVI_B_CLK#
NO USE (TV)
TV_Y/HDTV_Y/TV_CVBS
TV_C/HDTV_Pr
TV_CVBS/HDTV_Pb
TV-OUT
45 EDID_CLK_PEG
45 EDID_DATA_PEG
DDCC_CLK
DDCC_DAT
SMBUS
24,50 SMB1_CLK_S
24,50 SMB1_DAT_S
SMB_CLK
SMB_DAT
Thermal sensor
MXM_230P
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
CLK_REQ#
PEX_RST#
PEX_REFCLK
PEX_REFCLK#
THERM#
PRSNT1#
PRSNT2#
RUNPWROK
OTHER
NP_NC1
NP_NC2
GND_1
GND_2
PCIEG_RXP0 11
PCIEG_RXN0 11
PCIENB_RXP0 11
PCIENB_RXN0 11
PCIEG_RXP1 11
PCIEG_RXN1 11
PCIENB_RXP1 11
PCIENB_RXN1 11
PCIEG_RXP2 11
PCIEG_RXN2 11
PCIENB_RXP2 11
PCIENB_RXN2 11
PCIEG_RXP3 11
PCIEG_RXN3 11
PCIENB_RXP3 11
PCIENB_RXN3 11
PCIEG_RXP4 11
PCIEG_RXN4 11
PCIENB_RXP4 11
PCIENB_RXN4 11
PCIEG_RXP5 11
PCIEG_RXN5 11
PCIENB_RXP5 11
PCIENB_RXN5 11
PCIEG_RXP6 11
PCIEG_RXN6 11
PCIENB_RXP6 11
PCIENB_RXN6 11
PCIEG_RXP7 11
PCIEG_RXN7 11
PCIENB_RXP7 11
PCIENB_RXN7 11
PCIEG_RXP8 11
PCIEG_RXN8 11
PCIENB_RXP8 11
PCIENB_RXN8 11
PCIEG_RXP9 11
PCIEG_RXN9 11
PCIENB_RXP9 11
PCIENB_RXN9 11
PCIEG_RXP10 11
PCIEG_RXN10 11
PCIENB_RXP10 11
PCIENB_RXN10 11
PCIEG_RXP11 11
PCIEG_RXN11 11
PCIENB_RXP11 11
PCIENB_RXN11 11
PCIEG_RXP12 11
PCIEG_RXN12 11
PCIENB_RXP12 11
PCIENB_RXN12 11
PCIEG_RXP13 11
PCIEG_RXN13 11
PCIENB_RXP13 11
PCIENB_RXN13 11
PCIEG_RXP14 11
PCIEG_RXN14 11
PCIENB_RXP14 11
PCIENB_RXN14 11
PCIEG_RXP15 11
PCIEG_RXN15 11
PCIENB_RXP15 11
PCIENB_RXN15 11
@R7037 0Ohm 2
R7038 0Ohm 2
GPU_RST# 22,24
PLT_RST# 5,11,21,33,55,62
CLK_PCIE_PEG 29
CLK_PCIE_PEG# 29
VGA_ALERT# 30,50
NO USE (VGA_DET#)-Pin 225 226
PWR_OK_VGA 92
PRSNT1# PRSNT2# ASIC
0 0 ATI
0 1 NVIDIA
NO123. N81SR
+1.5VS 4,14,20,21,23,29,43,53,57,82
+3VS 3,6,7,8,11,14,15,20,21,22,23,24,25,29,30,31,33,36,38,40,41,42,43,45,46,48,50,51,53,55,57,62,63,80,91,92
+5V 9,44,52,56,57,68,91
+12VS 24,32,38,45,48,57,62,91
RESISTORS CLOSE TO MXM
LVDS_U0N /GM 1 0OHM 2 RN7002A LVDS_U0N_GM 11
LVDS_U0P /GM 3 0OHM 4 RN7002B LVDS_U0P_GM 11
LVDS_U1N /GM 1 0OHM 2 RN7003A LVDS_U1N_GM 11
LVDS_U1P /GM 3 0OHM 4 RN7003B LVDS_U1P_GM 11
LVDS_U2N /GM 1 0OHM 2 RN7004A LVDS_U2N_GM 11
LVDS_U2P /GM 3 0OHM 4 RN7004B LVDS_U2P_GM 11
LVDS_UCLKP /GM 1 0OHM 2 RN7005A LVDS_UCLKP_GM 11
LVDS_UCLKN /GM 3 0OHM 4 RN7005B LVDS_UCLKN_GM 11
LVDS_L0N /GM 1 0OHM 2 RN7006A LVDS_L0N_GM 11
LVDS_L0P /GM 3 0OHM 4 RN7006B LVDS_L0P_GM 11
LVDS_L1N /GM 1 0OHM 2 RN7007A LVDS_L1N_GM 11
LVDS_L1P /GM 3 0OHM 4 RN7007B LVDS_L1P_GM 11
LVDS_L2P /GM 1 0OHM 2 RN7008A LVDS_L2P_GM 11
LVDS_L2N /GM 3 0OHM 4 RN7008B LVDS_L2N_GM 11
LVDS_LCLKP /GM 1 0OHM 2 RN7009A LVDS_LCLKP_GM 11
LVDS_LCLKN /GM 3 0OHM 4 RN7009B LVDS_LCLKN_GM 11
CRT_BLUE 0Ohm 1 /GM 2 R7015 CRT_BLUE_GM 11
CRT_RED 0Ohm 1 /GM 2 R7016 CRT_RED_GM 11
CRT_GREEN 0Ohm 1 /GM 2 R7018 CRT_GREEN_GM 11
CRT_HSYNC 0Ohm 1 /GM 2 R7020 CRT_HSYNC_GM 11
CRT_VSYNC 0Ohm 1 /GM 2 R7021 CRT_VSYNC_GM 11
AC_BAT_SYS
J7001B
C7011
15UF/25V
/PM
+1.5VS
C7016
10UF/10V
/PM
+3VS
C7008
10UF/10V
/PM
T7008
+2.5VS design always on
VGA daughter card
+2.5VS
RSVD4,RSVD5
for F8 HDMI
HDMI
48 DVI_DDCCLK1
48 DVI_DDCDAT1
29 CLK_ATI27S
29 CLK_ATI27
+5V
+12VS
+1.8VS_VGA
81,82,83,91,93 SUSB#_PWR
NO USE (HDTV_DET#)-Pin 218
PWR_SRC1
PWR_SRC2
PWR_SRC3
PWR_SRC4
PWR_SRC5
PWR_SRC6
PWR_SRC7
PWR_SRC8
1V8RUN_1
1V8RUN_2
1V8RUN_3
1V8RUN_4
1V8RUN_5
1V8RUN_6
1V8RUN_7
3V3RUN_1
3V3RUN_2
3V3RUN_3
5VRUN
2V5RUN
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
AC/BATT#
GND66
GND65
GND64
GND63
GND62
GND61
GND60
GND59
GND58
GND57
GND56
GND55
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
GND17
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GND28
GND29
GND30
GND31
GND32
GND33
GND34
GND35
GND36
GND37
GND38
GND39
GND40
GND41
GND42
GND43
GND44
GND45
GND46
GND47
GND48
GND49
GND50
GND51
GND52
GND53
GND54
MXM_230P
NO123. N81SR
TPC28T
T7004
Q7001
PMN45EN
+1.8VO
TPC28T
T7005
+1.8VS_VGA
(0.5A)
R7000 0Ohm
+12VS
C7036
0.1UF/25V
MLCC/+/-10%
TPC28T
T7006
Q7002
PMN45EN
TPC28T
T7007
+0.9VS_VGA
+0.9VS
+0.9V change to +0.9VS
Check
SUPPORTED VGA BOARD
remove Q7001,Q7002 if is no need
<Variant Name>
Title : MXM CON
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F8Va
Rev 1.0
Date: Tuesday, October 07, 2008
Sheet 78 of 94

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Title: TITLE		
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ASUSTeK COMPUTER INC	Title : BLANK	
	Engineer:	
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REVISION LIST

R1.0 2007/10/2
R1.1 2007/10/24
NO1 Page53: Rename WLAN_ON to WLAN_ON_C reset mount?
NO2 Page36: Mount R3629, Unmount R3614,C3618(for resume from S4 auto display Microphone plugged/unplugged message issue)
Page36: Swap R3604,R3605 and CX3633,CX3634
NO3 Page66: Change reference name C6613,C6614 to CX6613,CX6614
NO4 Page66: Swap J6601 ESATA_TXP(J6601/pin2),ESATA_TXN(J6601/pin3), ESATA_RXN(J6601/pin5),ESATA_RXP(J6601/pin6)
Page48: Change net name DVI_TX5+_MB_ESD to DVI_TX5+_MB_R
Change net name DVI_TX5-_MB_ESD to DVI_TX5-_MB_R
Change net name DVI_TX4+_MB_ESD to DVI_TX4+_MB_R
Change net name DVI_TX4-_MB_ESD to DVI_TX4-_MB_R
Change net name DVI_TX3+_MB_ESD to DVI_TX3+_MB_R
Change net name DVI_TX3-_MB_ESD to DVI_TX3-_MB_R
Change net name DVI_CLK+_MB_ESD to DVI_CLK+_MB_R
Change net name DVI_CLK-_MB_ESD to DVI_CLK-_MB_R
for ESD diode IC layout
NO5 Page41: Series R4110 at MDIO09~> SD Clock/MS Clock (double trace spacing with other signal)
NO6 Page30: Change Net name NUM_LED and CAP_LED(high active) to NUM_LED# and CAP_LED#(low active)
for Design IP rule
Page56: Change Net name NUM_LED and CAP_LED(high active) to NUM_LED# and CAP_LED#(low active)
for Design IP rule, Add R5616,R5618,Q5607A,Q5607B
NO7 Page36: Change Option name /3G to /3G_V R3621,R3623,R3624
Page37: Change Option name /3G to /3G_V C3703,C3704,C3706,R3701,C3702, R3703,R3705,R3706,R3707,R3711,R3712,U3701A,U3701B
for 3G Voice Option support
Page53: Change Option name /3G to /3G_V C5350,R5330,C5330,R5318
Page37: Change Option name /n3G to /n3G_V R3700,R3709,R3710
for n3G Voice Option support
NO8 Page33: Reserved DSM(Deep Slumber Mode) function to save power consumption(Add Q3303,R3319,R3320,R2206)
Change R3316 component size from 0402 to 0805
Change CE3301 name to C3308 and part from TAN to MLCC
Remove U3301 Pin.15, 41 power net to NC
Unmount U3302,C3313,R3308 (BIOS include EEPROM Data)
NO9 Page53: Mount R5340 for support digital TV tuner Card (Yuan MC872-1D)
NO10 Page57: Change 330 ohm to 1K ohm (R5709,R5713)
NO11 Page50: Change U5000 to G790 or MAX8565T for support Pennyn CPU
NO12 Page30: Change U3001 P/N 06G042016010 to 06G042016011
NO13 Page20,36,70: Add ACZ_BCLK_VGA(RX2017), ACZ_SYNC_VGA(RX2023), ACZ_RST#_VGA(RX2024), ACZ_SDOUT_VGA(RX2025), ACZ_SDIN3_VGA, SPDIF_VGA(R3630) for Nvidia VGA Card
NO14 Page21,22,53: Change WLAN_ON(GPIO24) to GPIO46. Add R2112,R2227(unmount),delete Q5301
NO15 Page30: Add R3024,D3002,D3001 for Auto power on issue(N86)
Add R3060,R3061,R3063,D3003,D3004 for Auto power on issue(EC Team)
NO16 Page14: Mount L1408,C1461,C1443,C1452 and unmount R1407 for design guideline change
NO17 Page42: Unmount C4208,C4210,C4211,C4212,C4213,C4214 for Memory Stick Card can't access issue
Delete NO18 Page29: Change R2903 330 ohm to 300 ohm
NO19 Page14: Delete component R1417,L1412,R1422,R1423,R1408,R1410,R1403,R1404,L1409,R1405,R1409 and Add R1425,C1432,C1453
NO20 Page23: Delete component R2307,R2312,R2301,R2304,L2305,R2318,R2315,R2316,R2306,R2314, R2308,R2309,R2317,R2310,R2313
Change R2311(0 ohm) to L2305(80Ohm/100Mhz)
NO21 Page69: Delete all component
NO22 Page50: Change component R5002 (33 ohm) to 200 ohm for vendor suggestion
NO23 Page30: Delete ITE512 and X1a(U3004,R3064,X3002,R3054,C3020,C3021)
Change Option name /8752 to N/A (R3056,R3057,R3062,X3001,R3045,C3017,C3016,U3001)
NO24 Page50: Change Pull-High power plane from +3VS to +3VA_EC and change R5001(10K ohm)to 100K ohm for OS# ,OC always keep Low in AC or DC mode will lead to EC_RST# always keep Low(System can't boot)
NO25 Page38: Change option name @ to /3G (C3815,C3816,C3817,C3818)
Page53: Unmount RN5301A,RN5301B and mount L5300
Page53: Add L5303 and JS303(Pin 14) connect to +3V_WWAN(separate power plane) ,unmount R5312,C5311
Page53: Mount C5327,C5328,C5321,C5320,C5322 and change 33PF/50V to 0.1UF/16V(C5321), change 33PF/50V to 18PF/50V(C5320),change option name /3G to @ (CE5300)
for 3G team suggestion
Page45: Change C4503(0603) 0.1uF/25V to (1210) 22uF/25V
NO26 Page52: (0 ohm)RN5201A,RN5201B replace R5201,R5202 and add L5206
(0 ohm)RN5202A,RN5202B replace R5203,R5209 and add L5201
(0 ohm)RN5205A,RN5205B replace R5216,R5220 and add L5205
co-lay for EMI suggestion
NO27 Page46: Change 47PF/50V to 10PF/50V (C4618,C4619,C4620) follow F85p

R1.1 2007/12/14
NO28 Page20: Change 33 Ohm to 39Ohm(RX2009, RX2010)
Change 33 Ohm to 56Ohm(RX2011, RX2012, RX2013, RX2014)
Change 33 Ohm to 62Ohm(RX2015, RX2016)
for F8Va Azalia interface measure
NO29 Page20: Change 12G2011002002 to 12G2001002J (J2001) for quality issue
Not modify ,because part pin define antipodes NO30 Page31: Change 12G182402805 to 12G182102805 (J3101) for quality issue
NO31 Page45: Change 12G1700100073 to 12G170010076 (J4502) for quality issue
NO32 Page33: ADD R3308 to pull high Aux power to fix power down mode fail issue

R1.2 2007/12/24
NO32 Page22: Unmount R2231 for NO15 Auto power on issue, because R3061 and R2231 R3061 deliver the voltage
NO33 Page37: Add Note : Either 3G or n3G must be chosen, either 3G_V or n3G_V must be chosen

R1.2 2008/01/28
NO34 Page52: delete D5200~D5205 because they are no use.
add unmont U5201, unmount U5202, mount U5203 for ESD issue

R1.2 2008/01/28
NO35 Page22: Add test point T2220 for factory isssue

NO36 Page29: Exchange KBC and ICH of PCI CLOCK source.(follow DESIGN IP)

NO37 Page30: EC version is BX or CX to mount R3054 ,un-mount C3020 and C3021.
EC version is DX to mount C3020 and C3021 ,un-mount R3054.

NO38 Page22,24: Implement HDCP ROM to ICH9 SMBUS .(follow DESIGN IP)
NO39 Page38:deleted, no thing
NO40 Page40:add umount R4009, let CB_IDSEL can be chosen to PCI_AD17
NO41 Page20:Add Bi-direction buffer for NB HDMI codec.
NO42: deleted, no thing
R2.0 2008/01/30

NO43 deleted, no thing
NO44 Page56: change LED5600,LED5601,LED5603,LED5604,LED5605,LED5606 to 07G015L00311, and change LED5602 to 07G015700064 for Change LED source to follow IF=5mA,ESD=1KV

Not modify NO45 Page34: Modify C3404 and C3405 value from 1000pF to 100pF to avoid the dial connecting signal quality during modem test in factory.
NO46 Page33: Add D3301 and D3302 to avoid ESD issue.
NO47 Page33 - Page22:
1. Change the RTLAN_VCC33_EN net name to the RTLAN_DSM_EN to meet the pin's behavior.
2. Change the RTLAN_DSM_EN# net name to the RTLAN_DSM# to meet the pin's behavior.
NO48 Page48: Unmount U4801 and U4802 and change 10 ohm to 0 ohm (R4814~R4821) beacuse ESD test is pass
NO49 Page33: add L3304 and unmount C3335 for vendor's hints.

not modify(F85P change for 3G)

NO Page45,53: Change Component 0.1uF to 39pF(C4505,C5303,C5310)
Page45: Change Component 33pF to 39pF(C4500)
Page45: Change Component 100pF to 39pF(C4501)
Page38: Change Component 33pF to 39pF(C3815,C3816,C3817,C3818) and change Option name @ to /3G
Page37: Change Component 100pF to 39pF(C3700) and change Option name @ to /3G
Page33: Change Component 33pF to 39pF(C3320,C5321,C5322) and change Option name @ to /3G
1)C6802, C1327 ,C1328 :EM/PM 未上件-->3G SKU 加上22uF/0805/6.3V

NO Page23: Change Component C2301,C2302(0402) type to 0603 not modify
NO Page53: J5302 pin 37,43,40 ==> Add R53,R53,R53(unmount) not modify

R2.0 2008/01/12

NO50 Delete R0703, R0704, R0803, R0906, R1414, R2112,R2227(unmount), R2230, RX2223, RX2225, R2918, R2919, R3045, R3047, R3305, R3312, R3317, R3318(unmount), R3804, R4012, R5340 ,RX1102, RX1103, RX2230
NO51 Change option of RX2919 to /FIR
NO52 Delete Q3302,R3311,Q3301,C3312,C3330,R3313, because it need not co-lay R8111B.
R2.0 2008/02/13
NO53 Delete JP2301 to improve layout.
NO54 Page33: Delete L3301, L3302,Change C3333,C3334 to close U3301 pin63.Add LAN Note 1,2.
NO55 Page48: Delete R4810,R4811,Q4802,RN4804, Add RN4810, RN4811 , Change optional of RN4801, Q4803 for HDMI DUT
NO56 Page13: Change JP1303 for 2MM_OPEN_5MIL to 3MM_OPEN_5MIL
NO57 Page41: Delete L4101, R4103, R4106, R4107, R4108 for layout issue.
NO58 Page55: Change Power of CIR to +5VSUS
NO59 Page55: Add R1426 at CIR Output.
NO60 Page29: Change U2900 P/N to ICS9LPR363EGLF-T(06G011408013)
Delete NO61 Page22,Page 56: Change net name BT_LED to BTLED_ON
NO64 Page29: Change option name @ to /3G (C2917,C2918,C2919, C2920,C2921,C2922,C2923,C2924,C2925) , and Change to 10PF
Page34: Change option name @ to /3G (4.C3416,C3417,C3418,C3419)
Page29: Change option name @ to /3G (C4510,C4518) , and Change to 8.2PF
NO65 Page 33: R3301 change to 2.4kohm
NO66 Page 52: Change CE5200, CE5202 to 330UF, Chnage CE5201 to 220UF
NO67 Page 29: Change option of RX2926 to /FIR
NO68 Page20: Change 12G24110190X to 12G241101932 (J4801) for factory issue
NO69 Page29: RX2901 change to 10G21239R014020, RX2923 change to 10G21222R014030, RX2915, RX2916, RX2922, RX2925 change to 10G21233R014030
NO71 Page30: Change R3060, R3063 to10K.

MP R2.1 2008/02/26
NO72 Page30: Change D3003 and D3004 to 1SS355 for leakage current issue.
NO73 Page22 30:Delete R2231, Add R3064 10ohm 0402 for Design IP changed.
NO74 Page48: Change the pull-high of RN4805A and RN4805B to +5VS_HDMI, Add Q4804 for EA test. D4801 change to @.
NO75 Page22 56 61: Change BT_LED to BT_LED_T, Change BLED_ON to BT_LED
NO76 Page 46: Change D4601~D4603 to close VGA Connector
NO77 Page 31: Change option of CN3101~CN3106 from /3G to N/A for EMI .
N80 unkown RO78 Page 52: unmount HS201 for factory issue.
NO79 Page 29: Change R2903 to 360 ohm, RX2941 to 22 ohm for SPEC changed and EA test.
NO80 Page 45: Change R4514 to 10 Kohm, R4519 to 100 Kohm for LVDS falling time test.
NO81 Page 38: Change speaker AV to 10dB
NO82 Page 24: Change net of HDCP ROM SMB_CLK_S, SMB_DAT_S from glocal to local.
NO83 Page 33 50: Change R3304 to 10G2121530O4010 for part number issue. Change C5000 to 11G2353106360 70 accord with other 10uF/10V
NO84 Page 1 10 20: Update the MP part number of the NB & SB.
NO85 Page 36: Change R3604,R3605 to 10kohm fro amplifier issue.
Not modify ,because no part: NO86 Page 33: Change U3301 to RTL8111C-VC-GR 02G611003820
NO85.5 Page30: Correct R3061 to 1K, R3063 to10K.

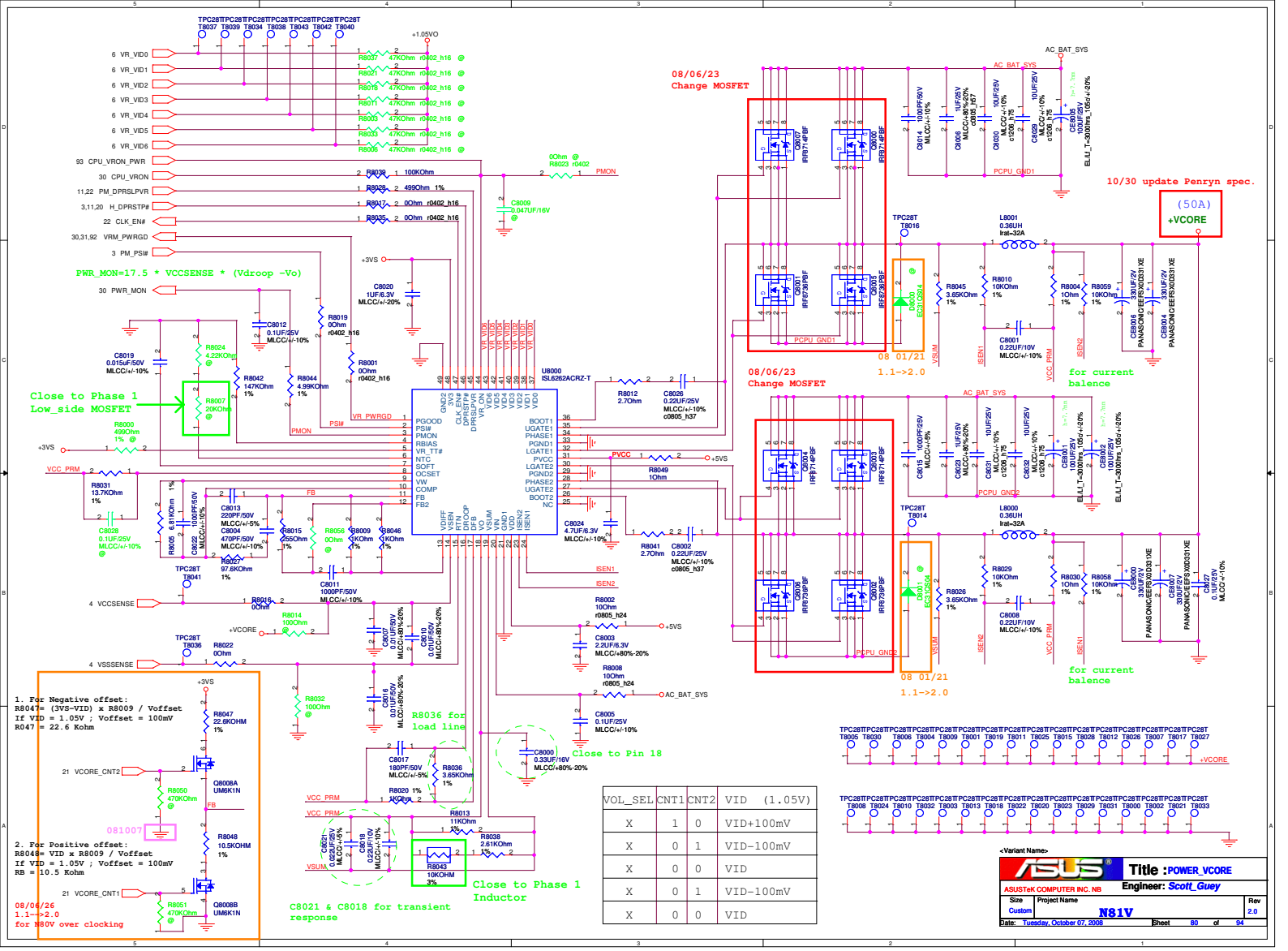
MP R2.2 2008/05/02
NO86 Page 36: Co-Lay ALC663 and ALC662 on Page.36
NO87 Page 45: Added one more LID switch circuit for N80 mechanical modification(U4502)
NO88 Page 14: Follow X80 to add reserve resistor to GND(R1427)
NO89 Page 45: unmount C4521, C4523 because they are not need. U4502 PIN 3 connect to GND.

MP R2.2 2008/06/17
NO90 Page 5 14: unmount C0524, C0525, CE1402, CE1403 for Cost down. Optional of L1401, L1402, C1407, C1408, R1428, C1439 are changed to /GM, and mount R1427 for power saving of PM.
NO91 Page 67: Correct page 67 subsystem ID
NO92 Page 36: add the text, F8V and L80V use ALC662, N80V use ALC663.
NO93 Page 44: Change option of RN4400, R4401 from @ to /nDebug. Change option of C4401 to /DEBUG. Add the txt, If stage is SR, ER, PR, please use /Debug, If stage is MP, please use /nDebug to cost down.
NO94 Page 56: change option of C5605 to /F8V for the parts is only used at ID of F8V. Unmount C5606 because no use.
NO95 Page 56: change R5605, R5611 to 100K for Power Saving.

N80 PR R2.3 2008/06/18
NO96 Page 22 29 53: Modify Net CLK_MINICARD_REQ# to CLK_ROBSON_REQ#.
Change Minicardport to use PCIeT_L5 and Robsonport to use PCIeT_L6.Change PCB ID.
NO97 Page 56: Add R5619, Q5608 to control Power Button LED.
NO98 Page 51: Add R5104 to connect SATA_LED# and HDD_LED#. Unmount R5103 and Q5109 , because no use.
Not modify , no space NO99 Page 52: Co-lay CE5204 to CE5209, and unmount CE5200.
NO100 Page 21 29 30: Add net VCORE_CNT1,VCORE_CNT2, VOL_SEL for overclock setting. Change Clock Gen to ICS9LPR362AGLF-T(no part)
And swap USB_OC01#, USB_OC11#, USB_OC4# for request of layout. Add information to explain what project is used ICS9LPR362.
NO101 Page 29 30: Add C2953 for request of 3G team.
NO102 Page 48: Mount R4804 75 kohm for hot plug issue, and add R4822, R4823. If ATI, mount R4823. If nVidia, mount R4822 for advise of nVidia.
NO103 Page 55: Correct R1426 to R5516 for Define of Page.
NO104 Page 36: Add R3637 to pull-down SPDIF_VGA beacuse the singal is not used.
NO105 Page 56: Change power of POWER LED and Power button LED to +5V to save power.
NO106 Page 48: Keep the D4802, C4804, R4824 for advis e of nVidia for better EMI and ESD.
NO107 Page 22: Set PCB ID: PCB2.2 == 000, PCB2.3 normal => 001, PCB2.3overclock => 100.
NO108 Page 38: Change Q3800, Q3801, Q3802, Q3803, Q3804, Q3805, Q3806, Q3807, Q3810 from 2N7002 to 2N7002K for ESD protection.
NO109 Page 48: At N80V, mount HS201 for EMI.
NO110 Page 62 65: Change the optional of J6201, C6200, C6201, H6522 to /TPM for Russian law.
N80 P02 R2.4 2008/07/09
NO111 Page 43 52 61: Delete R4301, R4303, R5211, R5212, R5213, R5218, Add L4301, L5210, L5211, L6101, RN4301, RN5203, RN5204, RN6101 for EMI isssue.
Add option: If F8V or L80V, mount resistor at 5 USB port and camera. If N80V, mount choke at 5 USB port and camera.
NO112 Page 56: Change Power of Power LED to +5VSUS for LED is too slow.
NO113 Page 36: Unmount R3630 for SPDIF function in DOS mode.
NO114 Page 52: Delete D5206, D5207, D5208, D5209 to add choke L5210, L5211, because of no space.
NO115 Page 7 8 29: Change C2944, C2945, C2946, C2947, C2948, C2949, C2950, C2951, C2952 from 33pF to 22pF.
Change C0701,C0702,C0801,C0802 form 10pF to 8.2pF. And option of all part change to N80V_3G.
Change option of C2917, C2918, C2919, C2920, C2922,C2923,C2924,C2925 from /3G to /F8V_3G.
NO116 Page 53: Cancel n3G optional, all sku will mount.
NO117 Page 48: If you use nvidia GPU , RN4805 need be 1Kohm.
If you use UMA or ATI, RN4805 need be 2.2Kohm.
NO118 Page 22: Add the account of PCB ID.

N81 SR R1.0 2008/08/21
NO119 Page 30: Change EC from 8752 to 8512.
NO120 Page 04 06 29: Add CPU Switch and add Clock GEN OPTIONAL
NO121 Page 30 32: Add Fuction Lamp Driver.
NO122 Page 21 25 29 33 44: Delete /SPI function and J4402, RX2918, C2921, C2948 and C3331,C3332 to increase space for Lamp Driver function.
NO123 Page 70: Change option of J7001 from /PM to N/A because /GM need level shifter.
Not modify NO124 Page 30 56: Change Netname instant_ON# to KBD_ON# for function changing.
NO125 Page 22: Add N81 PCB ID Setting.
NO126 Page 45: Add Q4504, Q4505, R4520 for Panel that does not have Backlight enable PIN.
If mount this option, L4500 should be unmount.
NO127 Page 53: Short the 0 ohm, include R5317, R5333~R5339, beacuse all SKU is mount.
NO128 Page 45: Add unmount High-side power distribution Switch,U4503 and C4525, C4526.
NO129 Page 56: Add 0 ohm at LED pin2 for driving enhance of ITE 8512.
NO130 Page 20 34 35 65: Change MDC function to option /MDC.
NO131 Page 22 24: Change R2409 to unmount, and Change option of Q2405, R7038 to /GM for HDCP_EEPROM_PROTECT.
NO132 Page 22: Change PCB ID 000 to No overclock, Add PCB ID 001 to overclock.
NO133 Page 22: Change U3202 to LMC555CMX because LM555CMX is not productced.Correct the part number of R2027~R2030& J3203.

N81 PR R1.0 2008/08/16
NO134 Page 32:Add R3207 between R3202 and R3203 for tuning the voltage swing for EL noise.
NO135 Page 06: U0601 pin SCL link to SMB_CLK_S from SCL_3A, pin SDA link to SMB_DAT_S from SDA.
NO136 Page 15 21 24: add SPI function again. Change option of R1514, R2106 from @ to /SPI.
NO137 Page 22:Short R7038 because no necessary.
NO138 Page 32: Change option of all EL function from N/A to /EL.
NO139 Page 36: Change option of R3637 from /PM NV to /PM NV NB9only N10P request.
Not modify NO140 Page 11 45 48: Add R1134, R1135,R4521,R4825 for Cantiga EDS V2.1.
NO141 Page 32: Add R3208, R3209, Q3205, beacuse the current limit of TN2425 is not enough(only 1.8A).
NO142 Page 24 30: Add R2410, R2411, R2412 to choose the HDCP_EEPROM_PROTECT control pin.
NO143 Page 06: Change option of all CPU Switch function from N/A to /CPU Switch.



VOL_SEL	CNT1	CNT2	VID (1.05V)
X	1	0	VID+100mV
X	0	1	VID-100mV
X	0	0	VID
X	0	1	VID-100mV
X	0	0	VID

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE

Engineer: Scott_Guey

Size	Project Name	Rev
Custom	N81V	2.0

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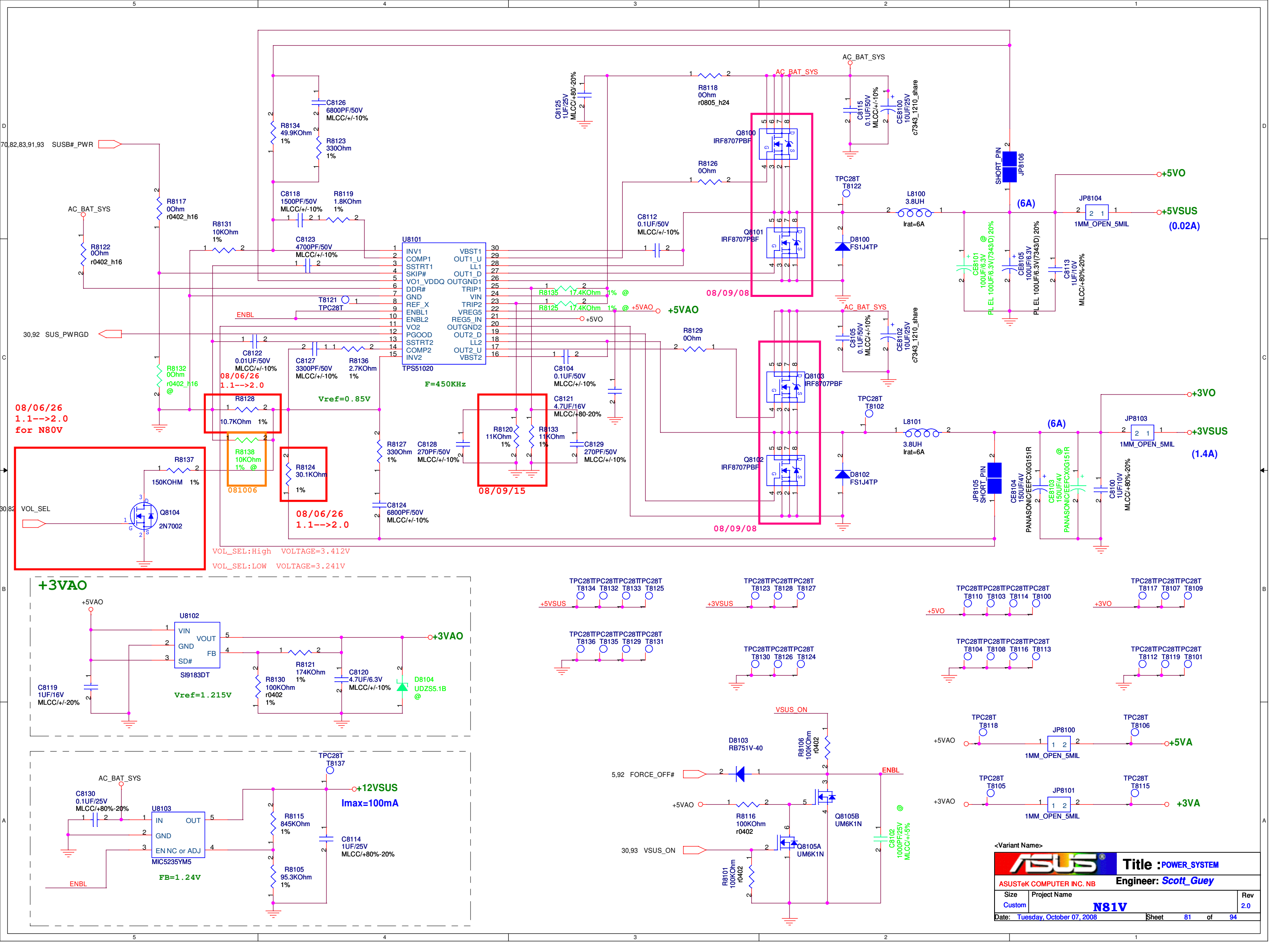

U8101
TPS51020
F=450KHz
INV1
COMP1
SSTRT1
SKIP#
VO1_VDDQ
DDR#
GND
REF_X
ENBL1
ENBL2
VO2
PGOOD
SSTRT2
COMP2
INV2
VBST1
OUT1_U
LL1
OUT1_D
OUTGND1
TRIP1
VIN
TRIP2
VREG5
REG5_IN
OUTGND2
OUT2_D
LL2
OUT2_U
VBST2
AC_BAT_SYS
SUSB#_PWR
SUS_PWRGD
VOL_SEL
ENBL
Q8100
Q8101
Q8102
Q8103
IRF8707PBF
L8100
L8101
3.8UH
Irat=6A
D8100
D8102
FS1J4TP
+5VO
+5VSUS
(6A)
(0.02A)
+3VO
+3VSUS
(1.4A)
JP8103
JP8104
1MM_OPEN_5MIL
SHORT_PIN
+5VAO
+3VAO
Vref=0.85V
08/06/26
1.1-->2.0
for N80V
08/09/08
08/09/15
081006
VOL_SEL:High VOLTAGE=3.412V
VOL_SEL:LOW VOLTAGE=3.241V
Q8104
2N7002
U8102
SI9183DT
VIN
VOUT
GND
FB
SD#
Vref=1.215V
D8104
UDZS5.1B
U8103
MIC5235YM5
IN
OUT
GND
EN NC or ADJ
FB=1.24V
+12VSUS
Imax=100mA
VSUS_ON
FORCE_OFF#
D8103
RB751V-40
Q8105A
Q8105B
UM6K1N
JP8100
JP8101
+5VA
+3VA
<Variant Name>
ASUSTeK COMPUTER INC. NB
Title : POWER_SYSTEM
Engineer: Scott_Guey
Size
Custom
Project Name
N81V
Rev
2.0
Date: Tuesday, October 07, 2008
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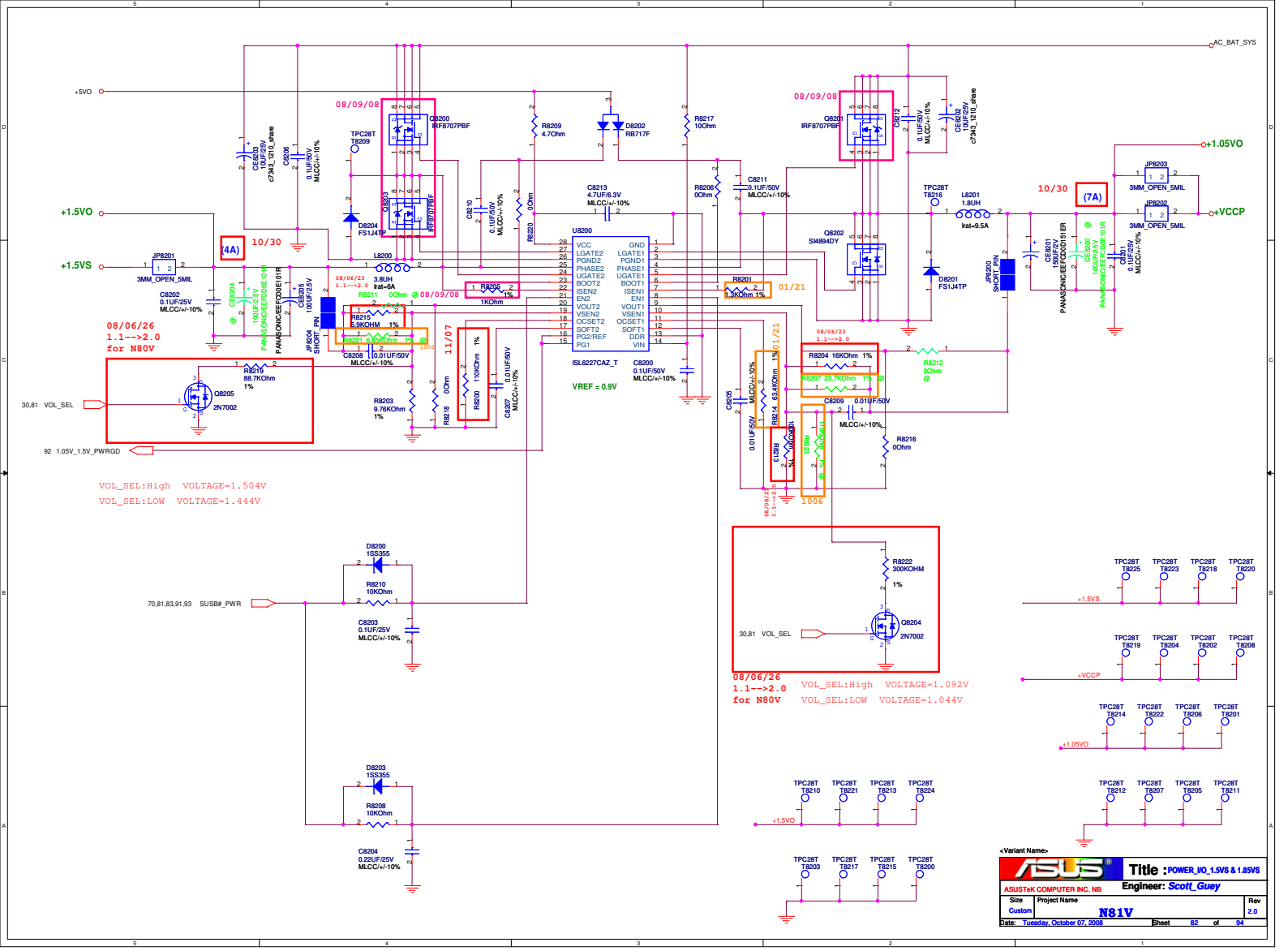
AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
08/09/08
08/09/08
10/30
10/30
(4A)
(7A)
01/21
01/21
11/07
08/06/26
1.1-->2.0
for N80V
08/06/23
1.1-->2.0
08/06/26
1.1-->2.0
for N80V
U8200
ISL6227CAZ_T
VREF = 0.9V
VOL_SEL:High VOLTAGE=1.504V
VOL_SEL:LOW VOLTAGE=1.444V
VOL_SEL:High VOLTAGE=1.092V
VOL_SEL:LOW VOLTAGE=1.044V
30,81 VOL_SEL
92 1.05V_1.5V_PWRGD
70,81,83,91,93 SUSB#_PWR
Q8200 IRF8707PBF
Q8201 IRF8707PBF
Q8202 SI4894DY
Q8205 2N7002
Q8204 2N7002
D8200 1SS355
D8203 1SS355
D8204 FS1J4TP
D8201 FS1J4TP
D8202 RB717F
L8200 3.8UH Irat=6A
L8201 1.8UH Irat=9.5A
JP8201 3MM_OPEN_5MIL
JP8202 3MM_OPEN_5MIL
JP8203 3MM_OPEN_5MIL
JP8204 SHORT PIN
JP8205 SHORT PIN
R8209 4.7Ohm
R8217 10Ohm
R8206 0Ohm
R8220 0Ohm
R8201 1.3KOhm 1%
R8212 0Ohm
R8204 16KOhm 1%
R8207 23.7KOhm 1%
R8214 634KOhm 1%
R8213 549KOhm 1%
R8216 0Ohm
R8222 300KOHM 1%
R8210 10KOhm
R8208 10KOhm
R8211 0Ohm @ 08/09/08
R8215 5.9KOHM 1%
R8221 6.65KOhm 1%
R8219 88.7KOhm 1%
R8203 9.76KOhm 1%
R8218 0Ohm
R8230 110KOhm 1%
C8213 4.7UF/6.3V MLCC/+/-10%
C8211 0.1UF/50V MLCC/+/-10%
C8210 0.1UF/50V MLCC/+/-10%
C8212 0.1UF/50V MLCC/+/-10%
C8202 0.1UF/25V MLCC/+/-10%
C8208 0.01UF/50V MLCC/+/-10%
C8200 0.1UF/50V MLCC/+/-10%
C8207 0.01UF/50V MLCC/+/-10%
C8205 0.01UF/50V MLCC/+/-10%
C8209 0.01UF/50V MLCC/+/-10%
C8203 0.1UF/25V MLCC/+/-10%
C8204 0.22UF/25V MLCC/+/-10%
CE8203 10UF/25V c7343_1210_class
CE8202 150UF/6.3V c7343_1210_class
CE8201 150UF/6.3V PANASONIC/EEFCD0D151ER
CE8200 100UF/2.5V PANASONIC/EEFCD0E101R
CE8204 100UF/2.5V PANASONIC/EEFCD0E101R
CE8205 100UF/2.5V PANASONIC/EEFCD0E101R
C8201 0.1UF/25V MLCC/+/-10%
TPC28T T8209
TPC28T T8216
TPC28T T8225
TPC28T T8223
TPC28T T8218
TPC28T T8220
TPC28T T8219
TPC28T T8204
TPC28T T8202
TPC28T T8208
TPC28T T8214
TPC28T T8222
TPC28T T8206
TPC28T T8201
TPC28T T8212
TPC28T T8207
TPC28T T8205
TPC28T T8211
TPC28T T8210
TPC28T T8221
TPC28T T8213
TPC28T T8224
TPC28T T8203
TPC28T T8217
TPC28T T8215
TPC28T T8200
<Variant Name>
Title : POWER_I/O_1.5VS & 1.05VS
ASUSTeK COMPUTER INC. NB
Engineer: Scott_Guey
Size Custom
Project Name N81V
Rev 2.0
Date: Tuesday, October 07, 2008
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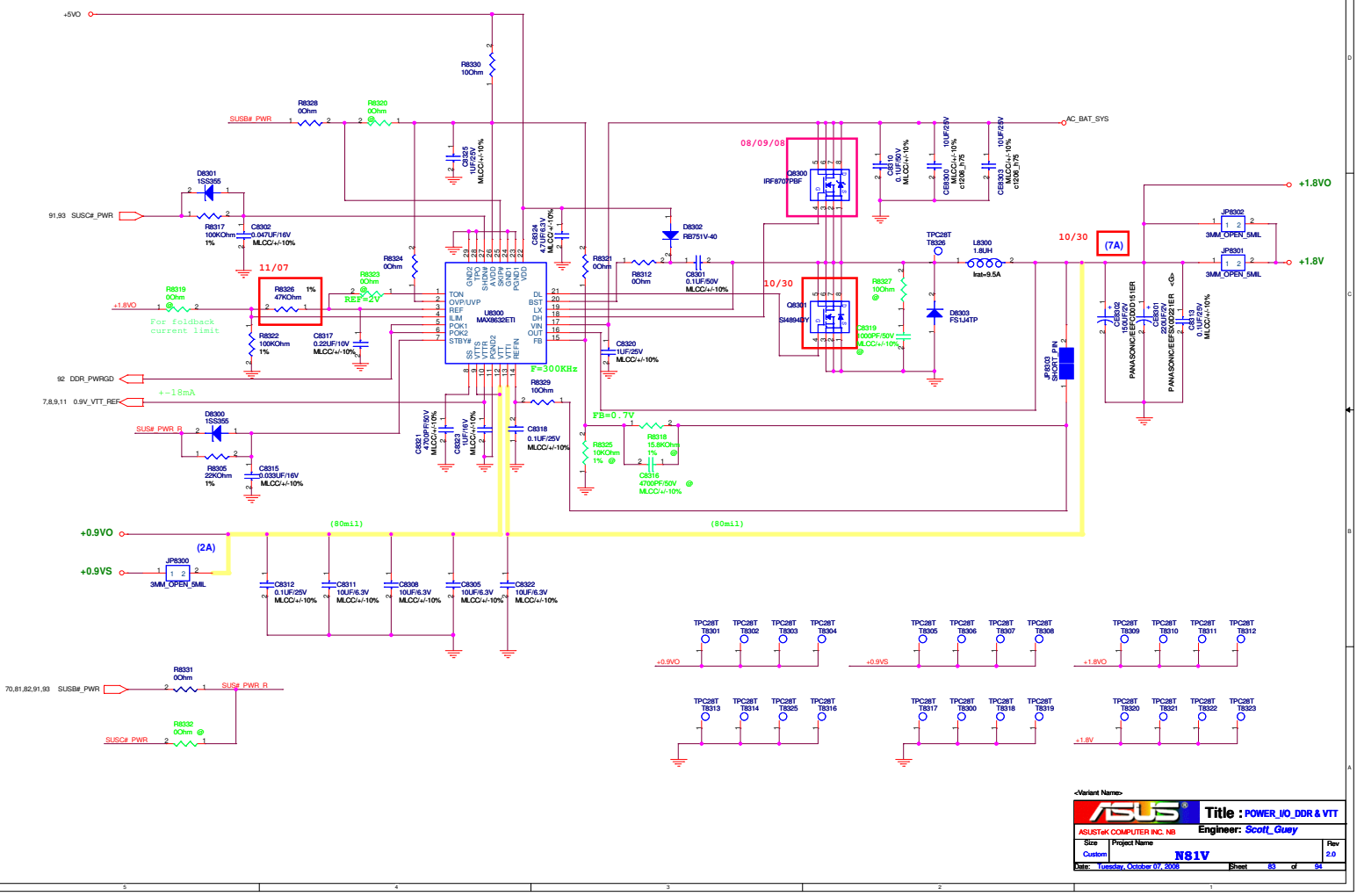

<Variant Name>

Title : POWER_I/O_DDR & VTT

ASUSTeK COMPUTER INC. NB

Engineer: Scott_Guey

Size	Project Name	Rev
Custom	N81V	2.0

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<Variant Name>

Title : N/A

<OrgName> Engineer:

Size	Project Name	Rev
Custom	N81V	2.0

Date: Tuesday, October 07, 2008 Sheet 84 of 94

<Variant Name>

Title : N/A

<OrgName> Engineer:

Size	Project Name	Rev
C	N81V	2.0

Date: Tuesday, October 07, 2008 Sheet 85 of 94

<Variant Name>

Title : N/A

<OrgName>

Engineer:

Size	Project Name	Rev
B	N81V	2.0

Date: Tuesday, October 07, 2008 Sheet 86 of 94

<Variant Name>

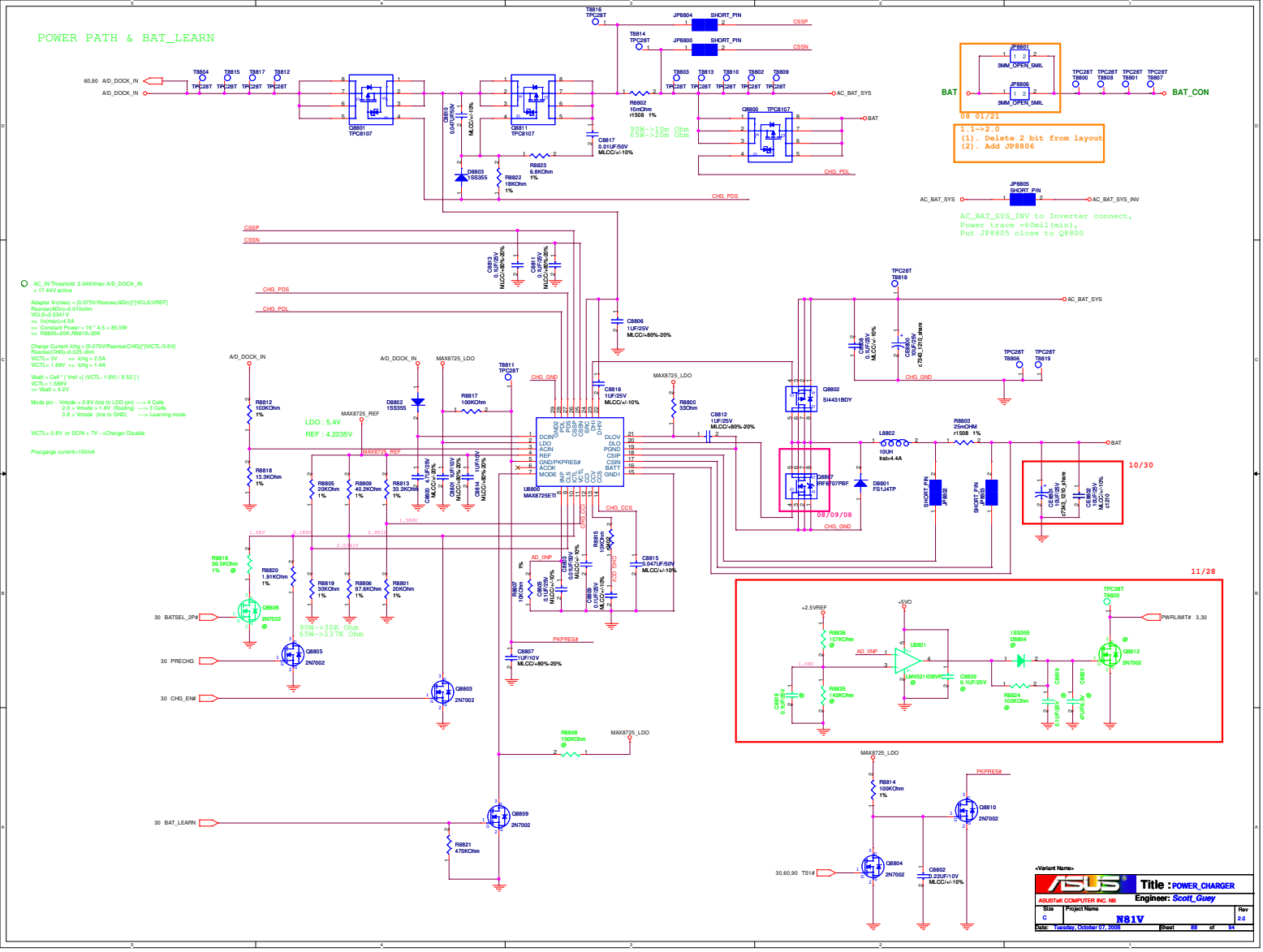
Title : POWER_SHUTDOWN#

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	N81V	2.0

Date: Tuesday, October 07, 2008 Sheet 87 of 94


POWER PATH & BAT_LEARN
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS:VREF]
Rsense(ADin)=0.010ohm
VCLS=2.5341V
=> Iin(max)=4.5A
=> Constant Power = 19 * 4.5 = 85.5W
=> R8805=20K,R8819=30K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]
VCTL= 1.588V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (Ntie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (Ntie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA
LDO : 5.4V
REF : 4.2235V
90W->30K Ohm
65W->137K Ohm
90W->10m Ohm
65W->20m Ohm
08/09/08
08 01/21
1.1->2.0
(1). Delete 2 bit from layout
(2). Add JP8806
AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800
10/30
11/28
BAT
BAT_CON
AC_BAT_SYS
AC_BAT_SYS_INV
CHG_PDS
CHG_PDL
CHG_GND
PKPRES#
MAX8725_LDO
MAX8725_REF
A/D_DOCK_IN
AD_IINP
CHG_CCS
CHG_CCV
PWRLIMIT# 3,30
30 BATSEL_2P#
30 PRECHG
30 CHG_EN#
30 BAT_LEARN
30,60,90 TS1#
MAX8725SETI
SI4431BDY
IRF8707PBF
FDS4435BZ
FS1J4TP
LMV321IDBVR
2N7002
<Variant Name>
Title : POWER_CHARGER
ASUSTeK COMPUTER INC. NB
Engineer: Scott_Guey
Size: C
Project Name: N81V
Rev: 2.0
Date: Tuesday, October 07, 2008
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<Variant Name>

Title : N/A

<OrgName> Engineer:

Size	Project Name	Rev
Custom	N81V	2.0

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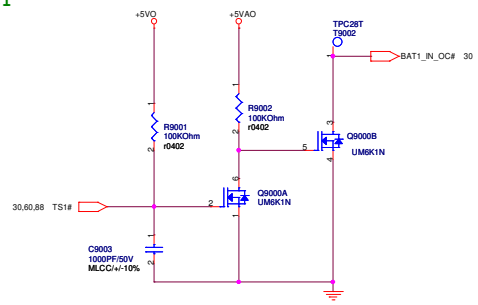
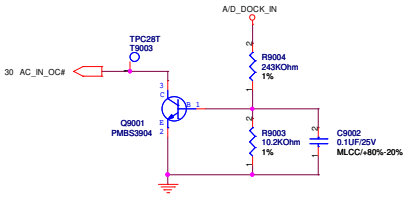
BATTERY IN DETECT

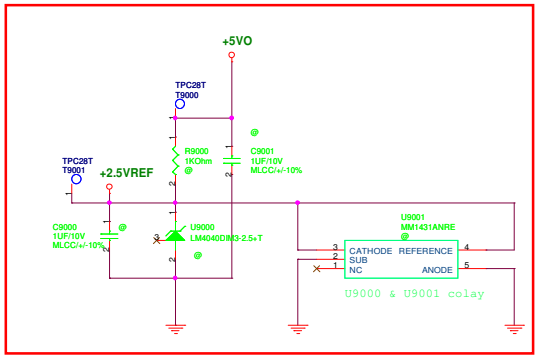


ADAPTER IN DETECT



+2.5VREF

11/28



<Variant Name>

ASUSTeK COMPUTER INC. NB

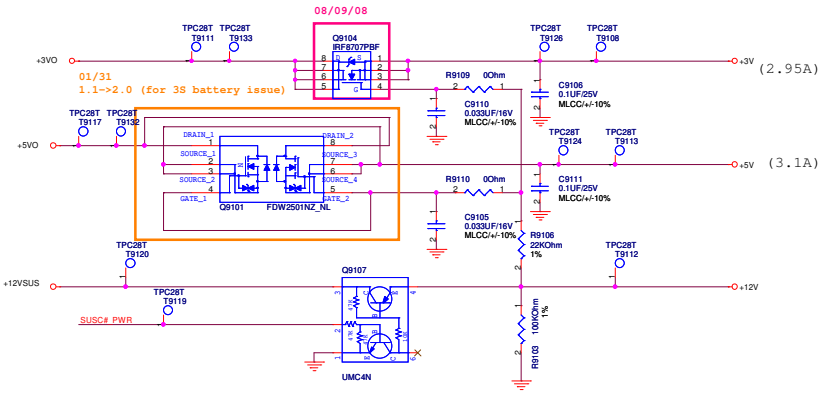
Title : POWER_DETECT

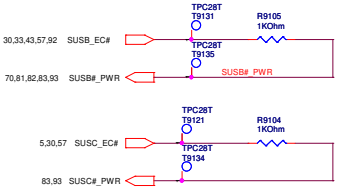
Engineer: Scott_Guey

Size	Project Name	Rev
Custom	N81V	2.0

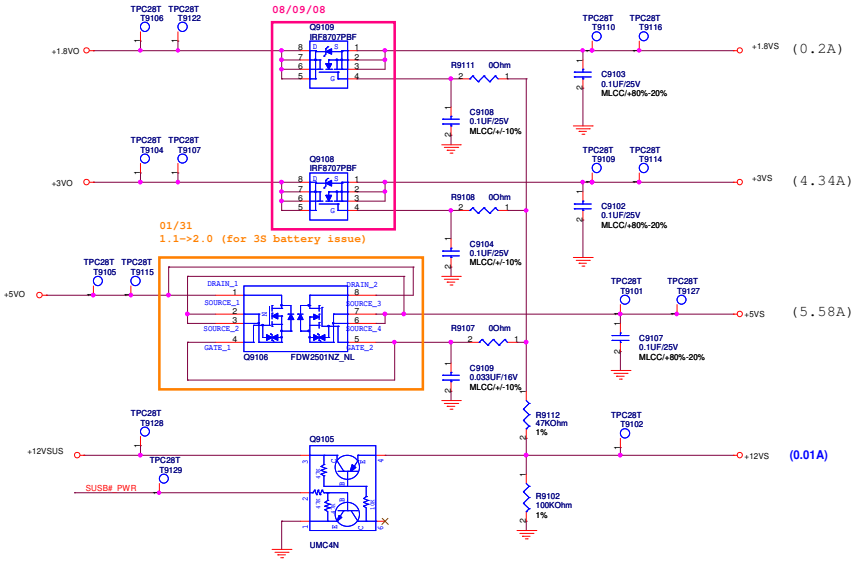
Date: Tuesday, October 07, 2008 Sheet 90 of 94

SUSC#_PWR POWER





SUSB#_PWR POWER

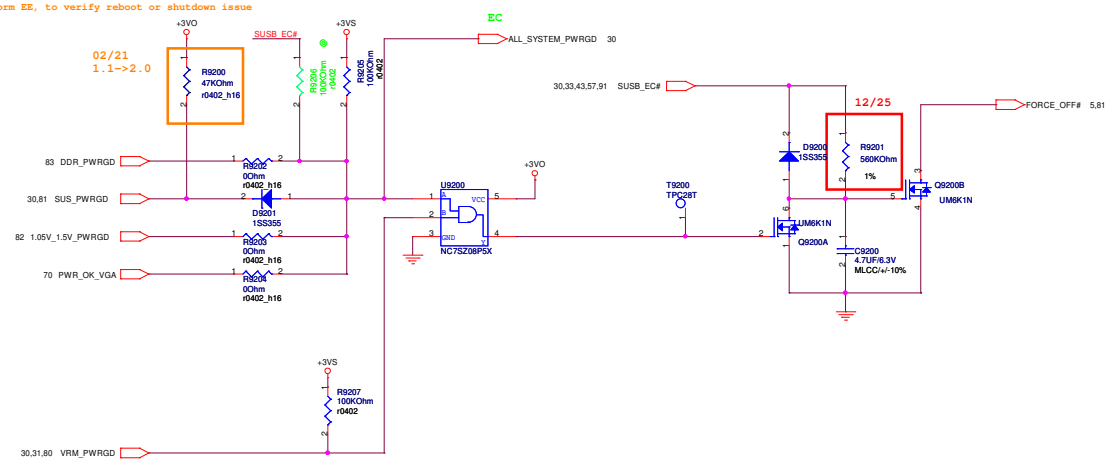


<Variant Name>

<OrgName>	Title : POWER_LOAD SWITCH	
	Engineer: Scott_Guey	
Size: Custom	Project Name: N81V	Rev: 2.0
Date: Tuesday, October 07, 2008	Sheet 91 of 94	

POWER GOOD DETECTER

Request form EE, to verify reboot or shutdown issue



<Variant Name>

<OrgName>	Title : POWER_PROTECT	
	Engineer: Scott_Guey	
Size: Custom	Project Name: N81V	Rev: 2.0
Date: Tuesday, October 07, 2008	Sheet 82 of 94	

AC_BAT_SYS → AC_BAT_SYS 70,80,81,82,83,88

BAT → BAT 88

BAT_CON → BAT_CON 60,88

+3VA → +3VA 20,30,45,57,81

+5VAO → +5VAO 81,90

+5VO → +5VO 81,82,83,88,90,91

+5VSUS → +5VSUS 23,55,56,81

+5V → +5V 9,44,52,56,57,68,70,91

+5VS → +5VS 23,31,32,36,38,46,48,50,51,56,57,63,80,91

+3VO → +3VO 81,91,92

+3VSUS → +3VSUS 20,21,22,23,30,33,81

+3V → +3V 6,21,32,35,43,44,45,53,56,57,61,62,91

+3VS → +3VS 3,6,7,8,11,14,15,20,21,22,23,24,25,29,30,31,33,36,38,40,41,42,43,45,46,48,50,51,53,55,57,62,63,70,80,91,92

+12VSUS → +12VSUS 24,81,91

+12V → +12V 38,42,52,57,91

+12VS → +12VS 24,32,38,45,48,57,62,70,91

+1.8VO → +1.8VO 70,83,91

+1.8V → +1.8V 7,8,9,11,13,57,83

+1.8VS → +1.8VS 14,57,91

+0.9VS → +0.9VS 9,57,70,83

+0.9VO → +0.9VO 83

+1.05VO → +1.05VO 57,80,82

+VCCP → +VCCP 5,6,10,11,13,14,20,23,29,57,82

+1.5VO → +1.5VO 82

+1.5VS → +1.5VS 4,14,20,21,23,29,43,53,57,70,82

FOR POWER TEST

+3VA → JP9300 (SGL_JUMP) pin 1 → pin 2 → CPU_VRON_PWR 80

+3VA → JP9301 (SGL_JUMP) pin 1 → pin 2 → SUSB#_PWR → SUSB#_PWR 70,81,82,83,91

+3VA → JP9302 (SGL_JUMP) pin 1 → pin 2 → SUSC#_PWR → SUSC#_PWR 83,91

+3VA → JP9303 (SGL_JUMP) pin 1 → pin 2 → VSUS_ON → VSUS_ON 30,81

<Variant Name>

Title : POWER_SIGNAL

<OrgName> Engineer: Scott_Guey

Size	Project Name	Rev
Custom	N81V	2.0

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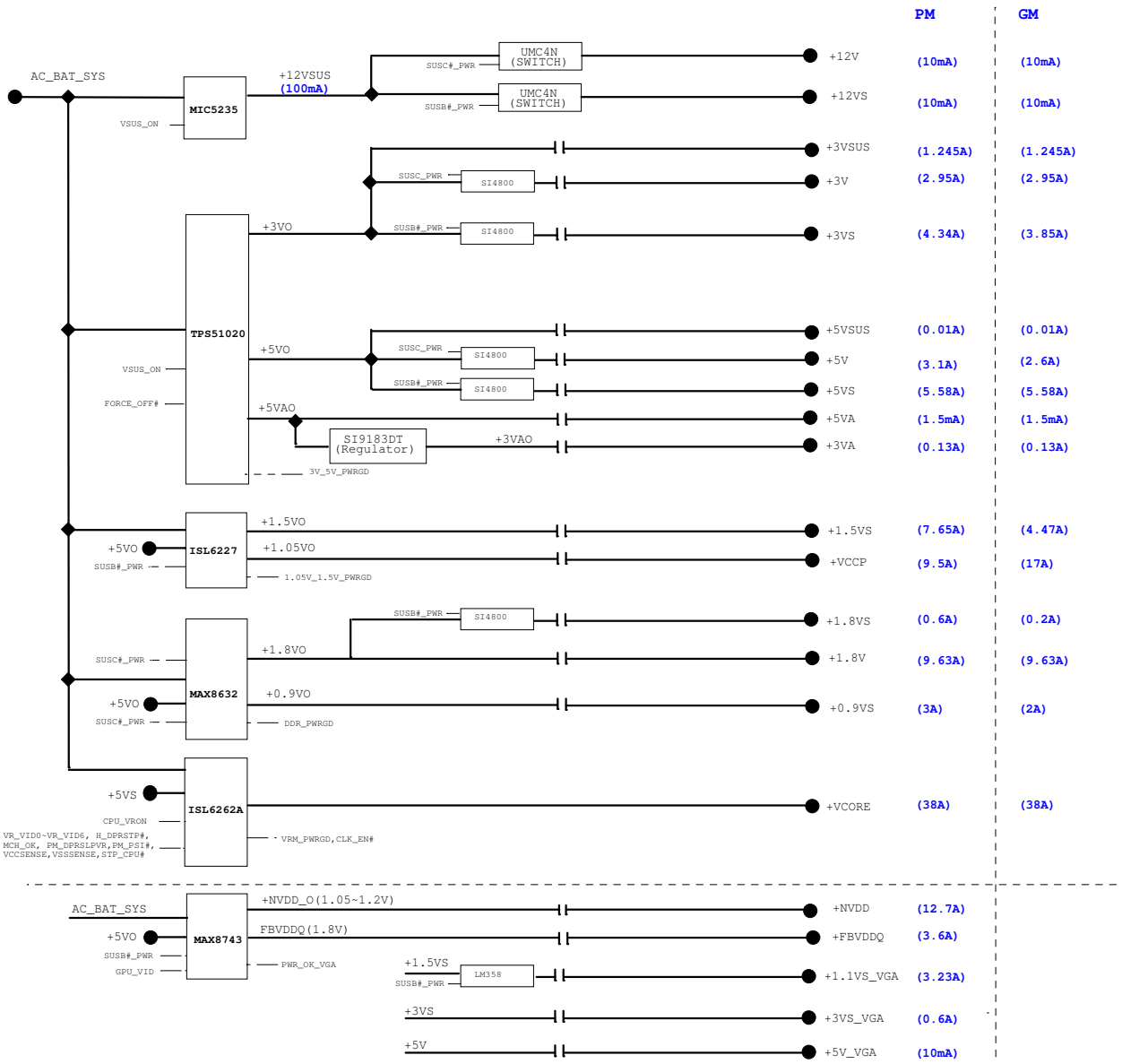

<Variant Name>

Title : POWER_VCORE

<OrgName>

Engineer: Scott_Guey

Size	Project Name	Rev
Custom	N81V	2.0

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