A7V8X

Revision : 1.04

版本：R1.04
RD：舒明達
日期：91.8

CLK GEN.
ICS94228BF
PAGE:6

CPU
AMD K7
SOCKET A 462P
PAGE: 8,9

ATX Power
+5VSB +12V
+3.3V -5V
+5V -12V
PAGE:3

DDR CLK BUF.
ICS93718CF PAGE:7

HOST BUS

AGP SLOT
PAGE:17

CPU DC/DC
ST L6917B
INPUT OUTPUT
+12V +1.85V~1.1V
PAGE:5

DDR SDRAM
DIMM*3
PAGE: 14,15,16

MEM BUS

North Bridge
VT8377
PAGE: 10,11,12,13

AGP BUS

Gigabit LAN
BCM5702
PAGE:27,28

PCI Slot * 6
PAGE:21,22

System
Regulator
INPUT OUTPUT
+5VSB +3VSB
+3V +1.8V
+3V VDDQ
+3V +3V_DUAL
+3VSB
+3V_DUAL +2.5V_DUAL
+2.5V_DUAL VTT_DDR
PAGE:4

V-Link BUS

PCI BUS

Primary IDE
PAGE:23

Secondary IDE
PAGE:23

6 USB1.1/2.0
PAGE:30

South Bridge
VT8235
PAGE: 18,19,20

Serial ATA
PDC20376
PAGE:24

PCI 1394
VT6306
PAGE:29

AC-LINK

AC97 Codec
ALC650
PAGE:25

MIC
Line In
Line Out
PAGE:26

SMBUS

SPEECH
W83791
PAGE:37

LPC

ASUS ASIC
AS2K127
PAGE:33

PS/2
KB,Mouse
PAGE:32

Parallel Port
PAGE:32

Serial Port * 2
PAGE:32

FDD
PAGE:32

Super I/O
ITE 8703F
PAGE:32

PCI Arbiter
AS_007
PAGE:34

JoyStick
PAGE:26

BIOS
29FS020
PAGE:36

Smart Card
Reader
PAGE:31

PCB LAYER
L1 : Component (S1)
L2 :GND
L3 :VCC
L4 : Component (S4)

<Core Design>

Asustek Computer INC.

Title : BLOCK

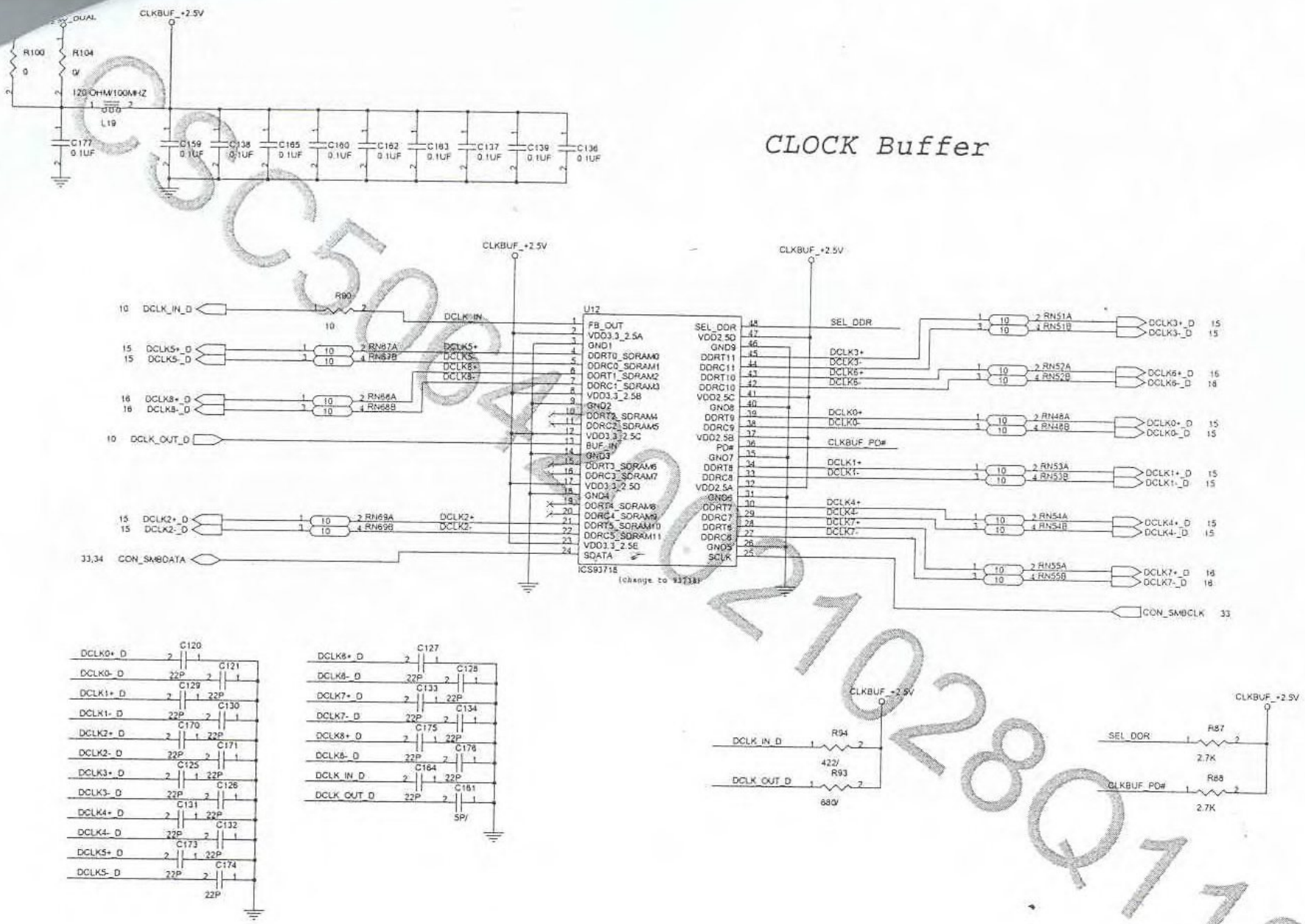
Engineer: Peter Chiou

Size	Project Name	Rev
A4	A7V8X	0.1

Date: 星期六, 八月 17, 2002 Sheet 1 of 38

ESC5064 2002 10 28 0110
華碩電腦股份有限公司 客服中心 OCT 29 2002 發文
研發 AUG 27 2002 編號：1.
hexainf@hotmail.com

CLOCK Buffer

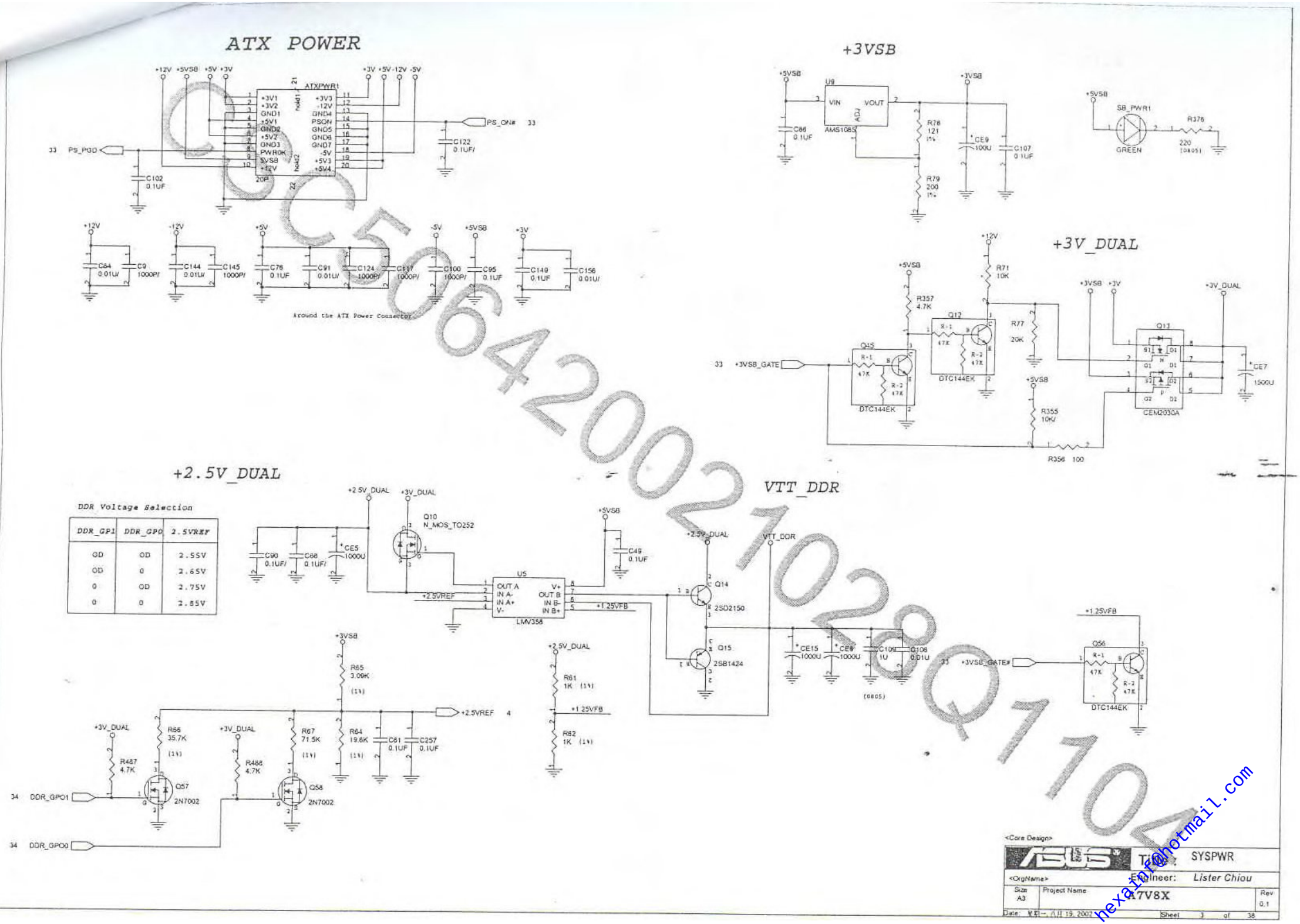


CSC50042002102 8Q1102

<Core Design>

ASUS	Title:	CLOCK BUFFER
<OrgName>	Engineer:	Lister Chiou
Size A3	Project Name A7V8X	Rev 0.1
Date: 星期六, 八月 17, 2002	Sheet 7 of 38	

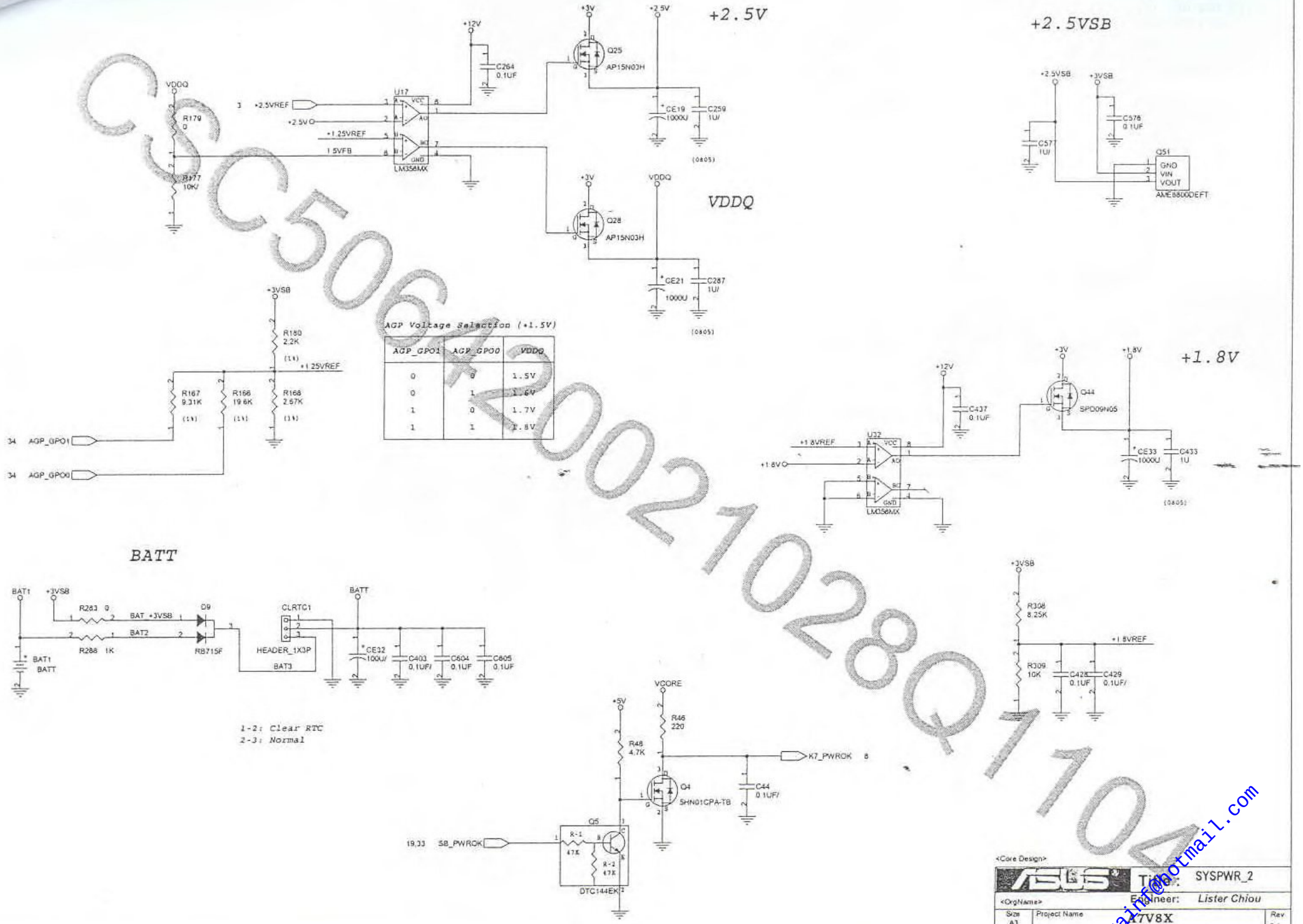
hexainf@hotmail.com



DDR Voltage Selection

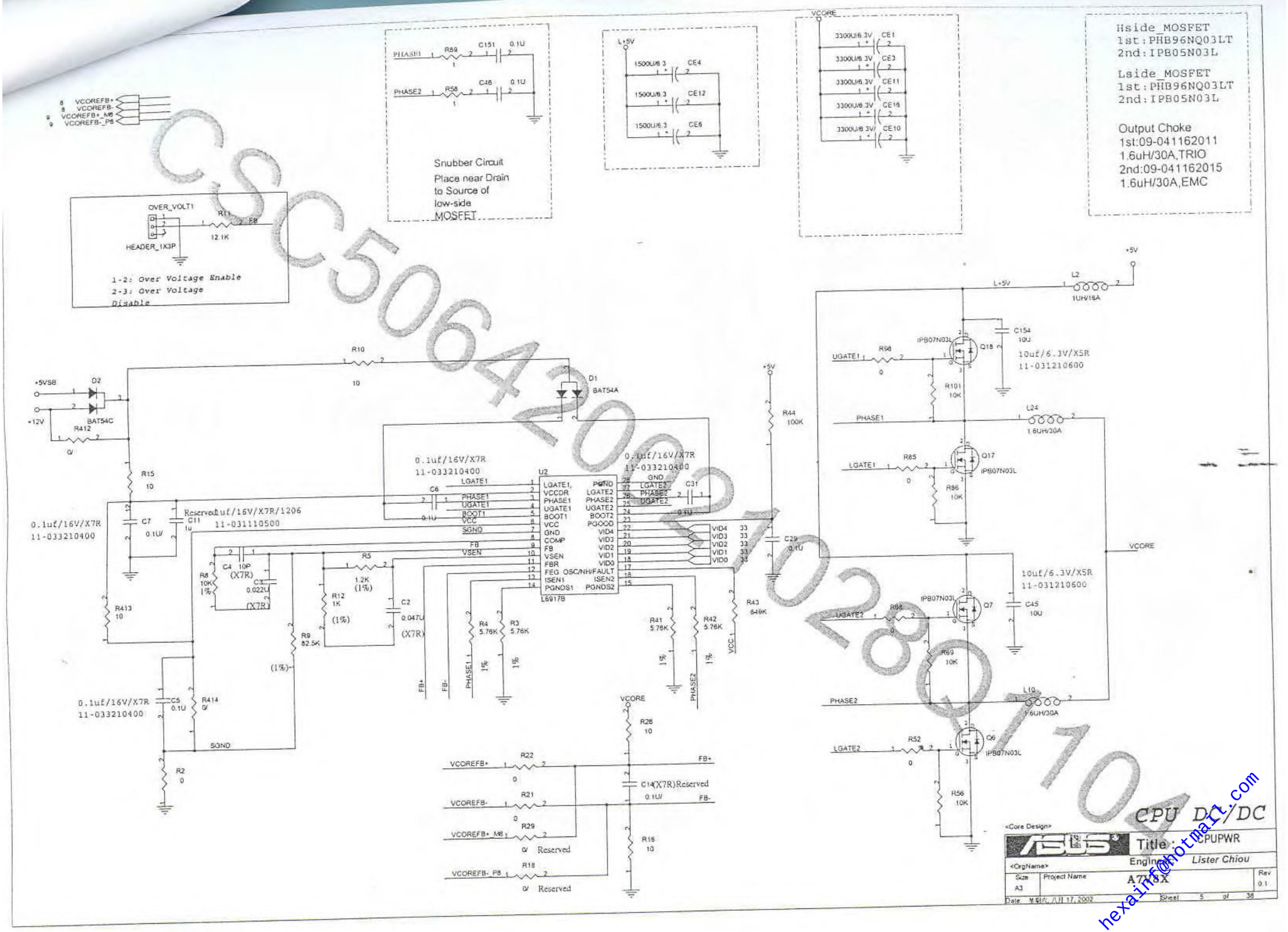
DDR_GP1	DDR_GP0	2.5VREF
OD	OD	2.55V
OD	0	2.65V
0	OD	2.75V
0	0	2.85V

CSC50642002102 8Q1104
hexaint@hotmail.com



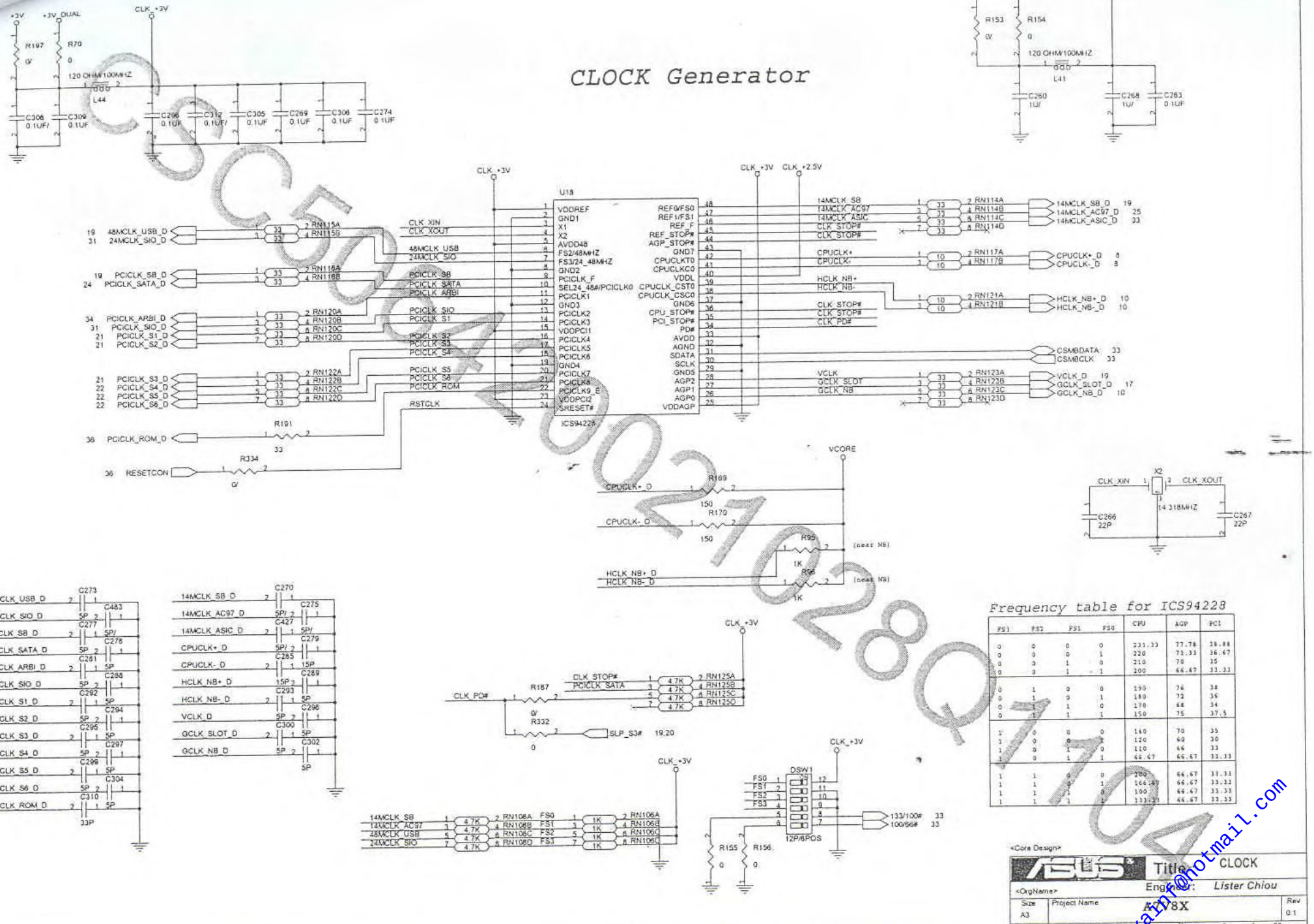
CSC506R0021028Q1104

hexainf@hotmail.com



CSC50642002102801104
hexainf@hotmail.com

CLOCK Generator



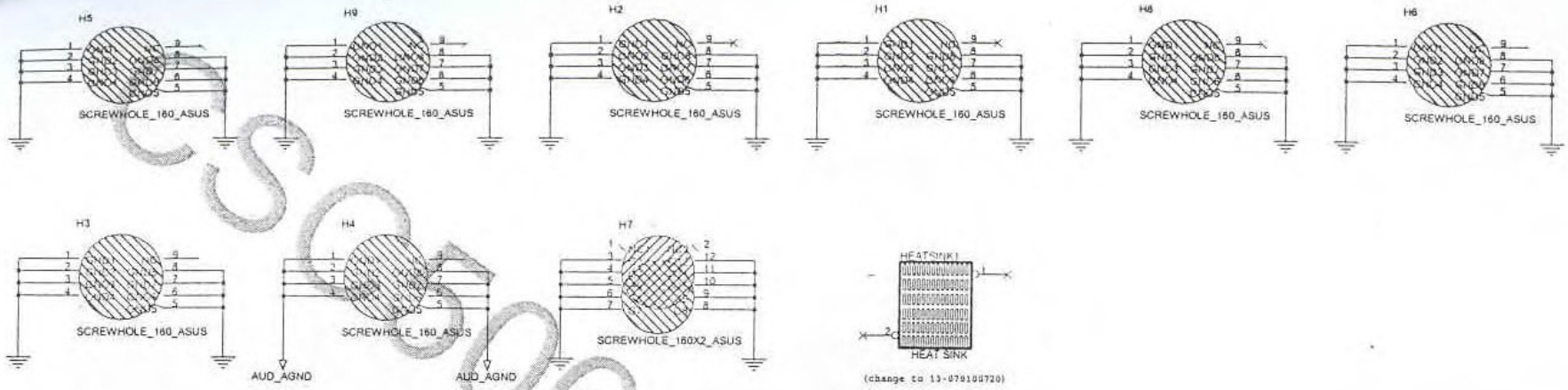
Frequency table for ICS94228

FS3	FS2	FS1	FS0	CPU	AGP	PCI
0	0	0	0	233.33	77.78	38.88
0	0	0	1	220	73.33	36.67
0	0	1	0	210	70	35
0	0	1	1	200	66.67	33.33
0	1	0	0	150	75	38
0	1	0	1	180	72	36
0	1	1	0	170	68	34
0	1	1	1	150	75	37.5
1	0	0	0	140	70	35
1	0	0	1	120	60	30
1	0	1	0	110	66	33
1	0	1	1	66.67	66.67	33.33
1	1	0	0	200	66.67	33.33
1	1	0	1	166.67	66.67	33.33
1	1	1	0	100	66.67	33.33
1	1	1	1	133.33	66.67	33.33

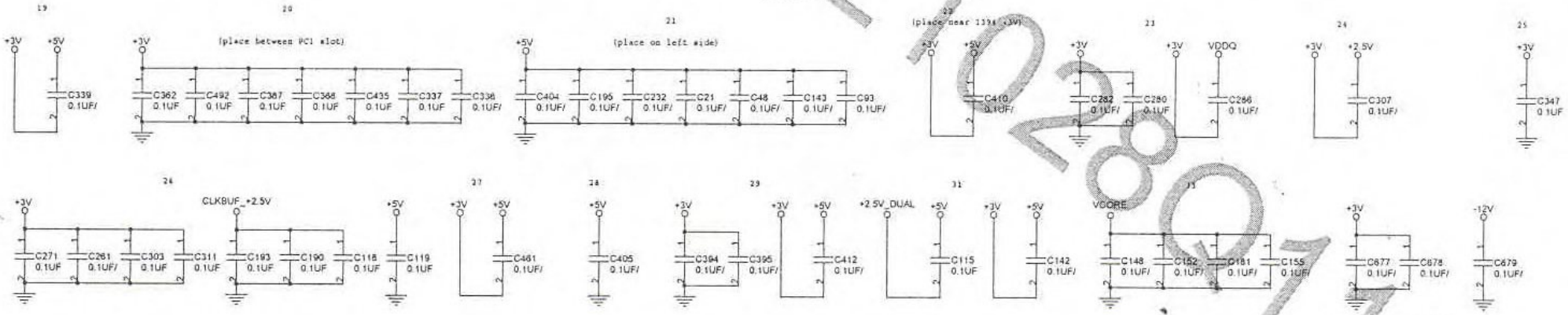
<Core Design>

Title: CLOCK		
<OrgName>	Engineer: Lister Chiou	
Size: A3	Project Name: A7V8X	Rev: 0.1
Date: Wed, Jul 17, 2002	Sheet 6 of 38	

hexainf@hotmail.com



EMI



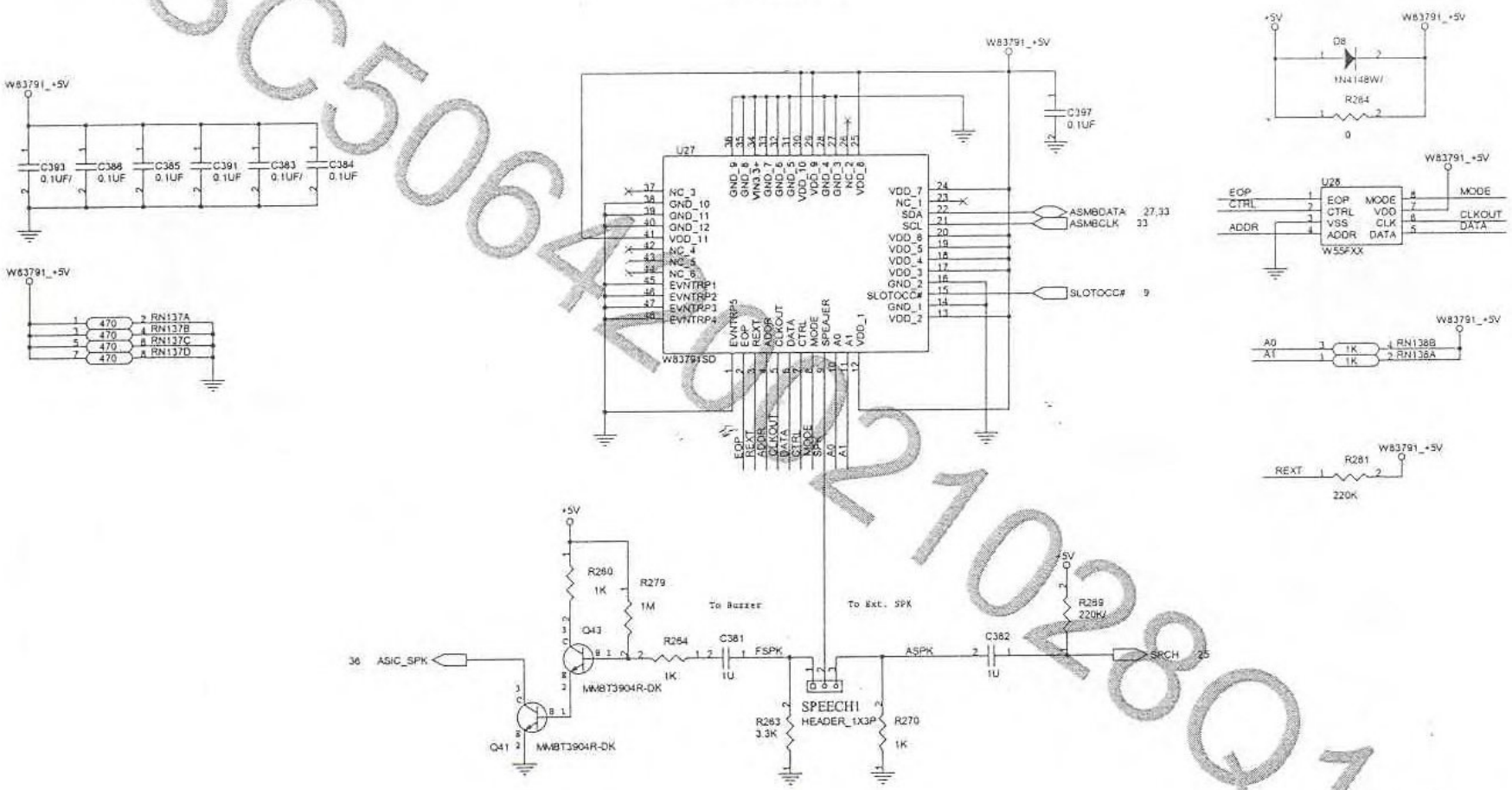
CSC50642002102801104

<Core Design>

ASUS	Title :	RESERVED
<OrgName>	Engineer:	Lister Chiou
Size A3	Project Name A7V8X	Rev 0.1
Date: 星期六, 八月 17, 2002	Sheet 38 of 38	

hexainf@hotmail.com

SPEECH

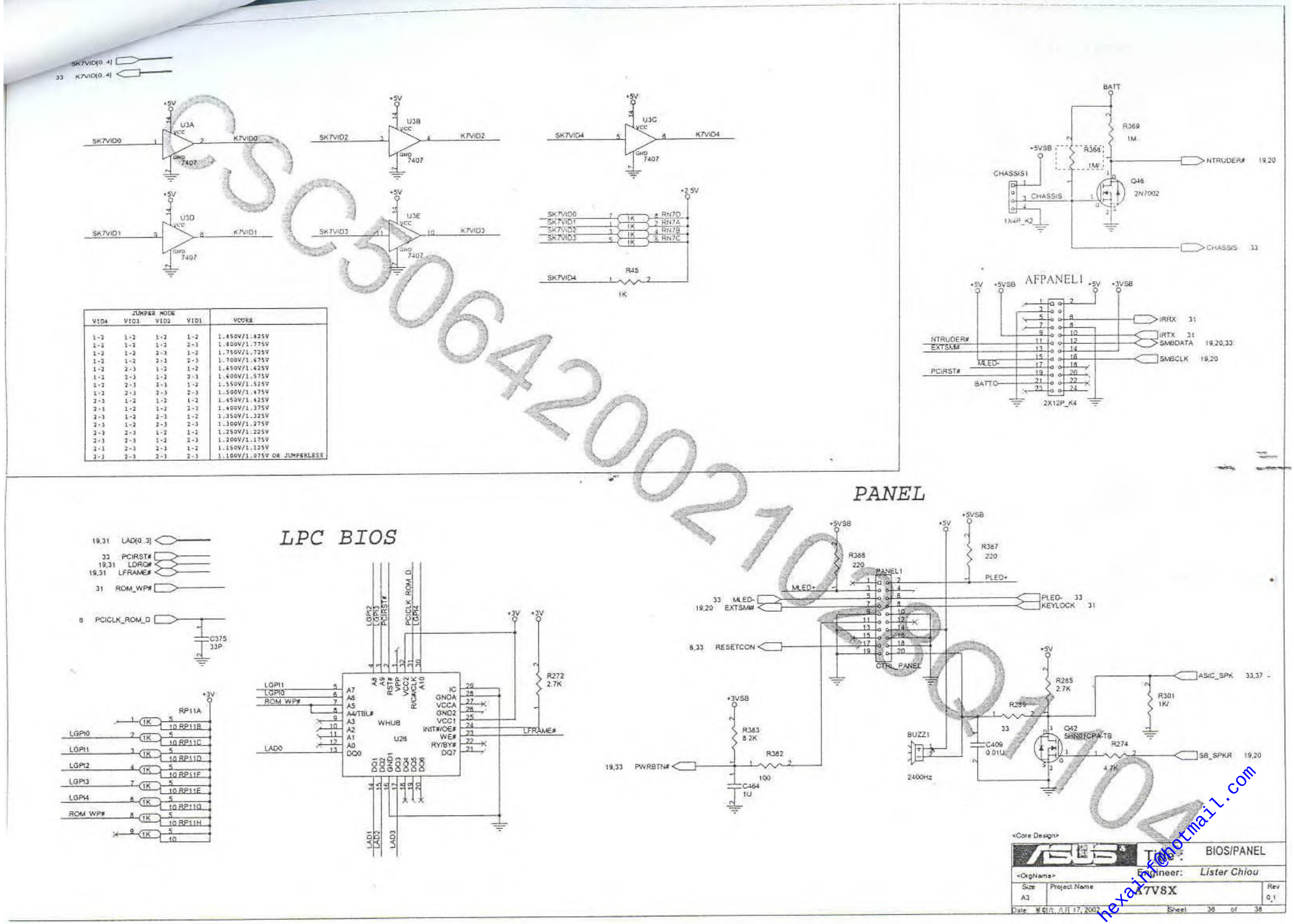


CSC50642002102 8Q1104

<Core Design>

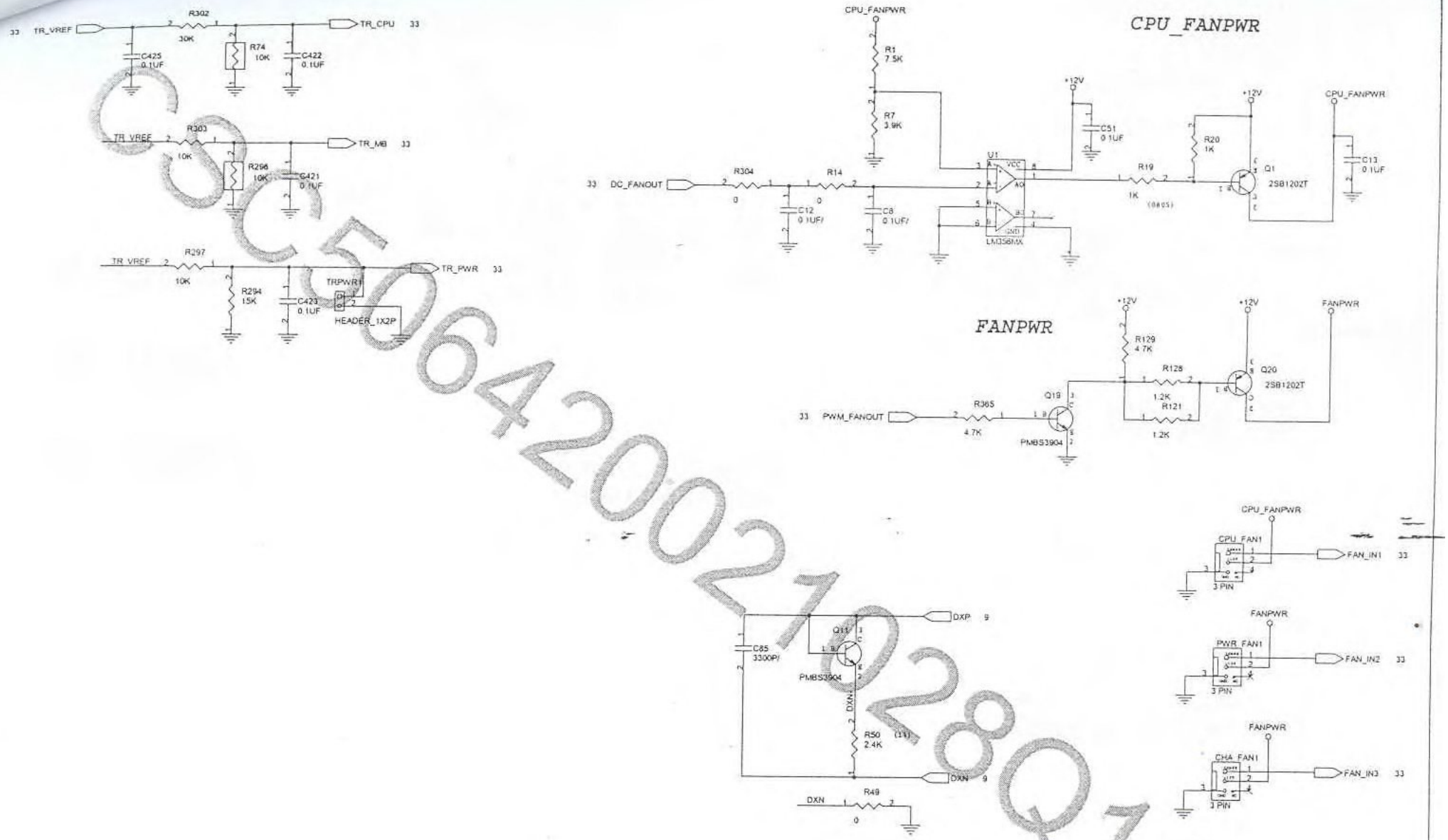
ASUS	Title : SPEECH		
<OrgName>	Engineer: Lister Chiou		
Size A3	Project Name A7V8X		Rev 0.1
Date: 星期六, 八月 17, 2002	Sheet 37 of 38		

hexainf@hotmail.com

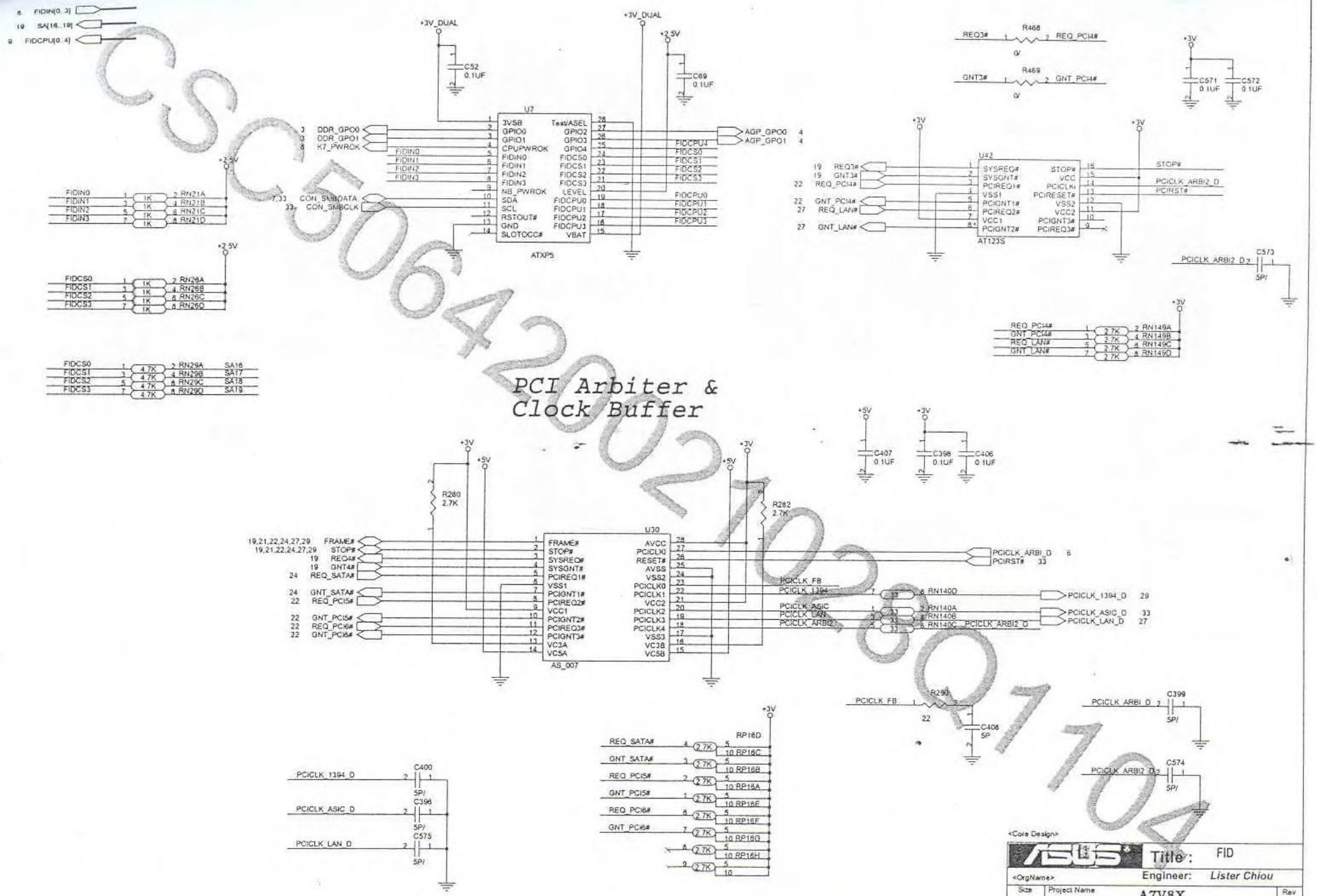


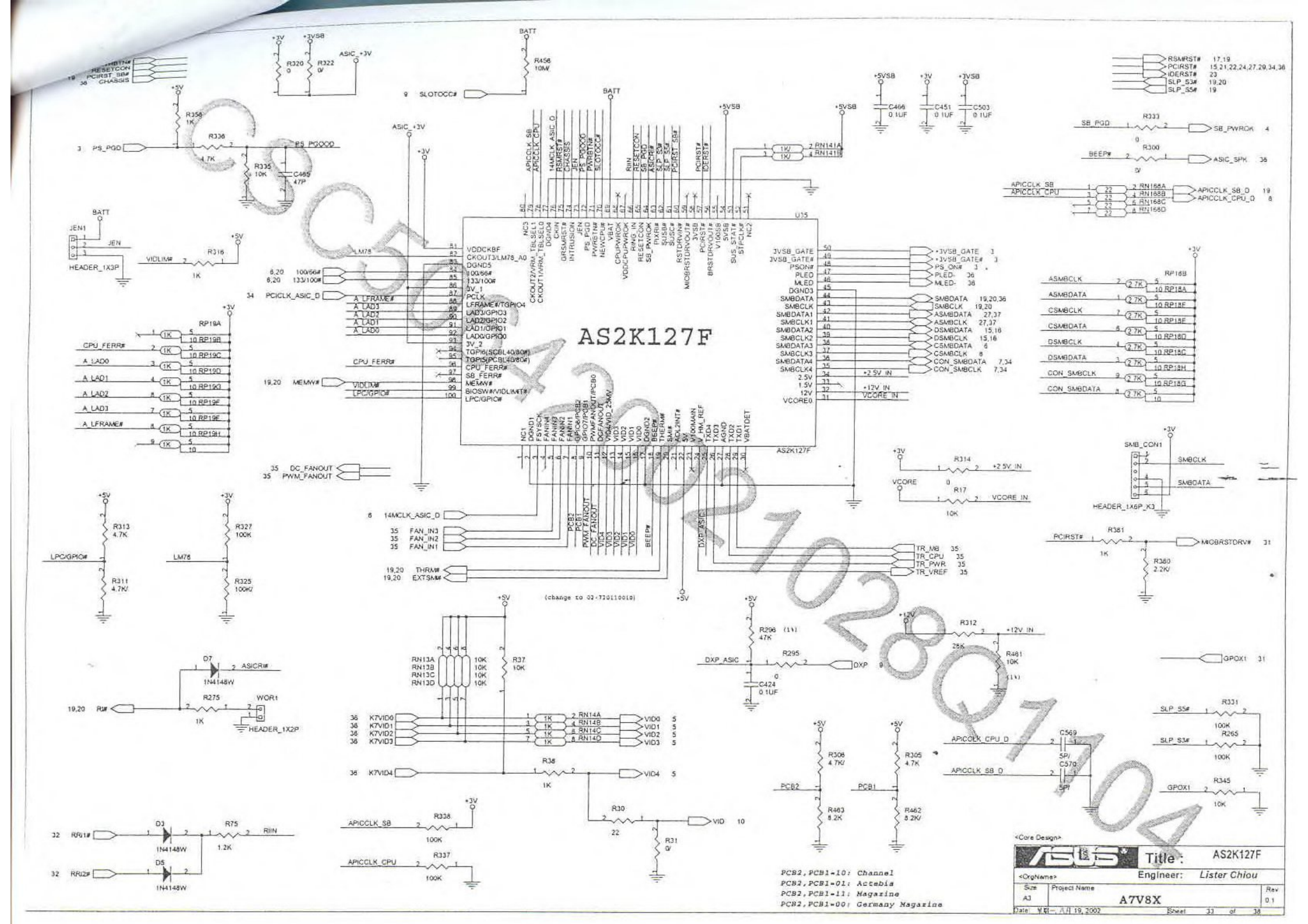
JUMPER MODE				
VID4	VID3	VID2	VID1	VCORE
1-2	1-2	1-2	1-2	1.850V/1.825V
1-2	1-2	1-2	2-3	1.800V/1.775V
1-2	1-2	2-3	1-2	1.750V/1.725V
1-2	1-2	2-3	2-3	1.700V/1.675V
1-2	2-3	1-2	1-2	1.650V/1.625V
1-2	2-3	1-2	2-3	1.600V/1.575V
1-2	2-3	2-3	1-2	1.550V/1.525V
1-2	2-3	2-3	2-3	1.500V/1.475V
2-3	1-2	1-2	1-2	1.450V/1.425V
2-3	1-2	1-2	2-3	1.400V/1.375V
2-3	1-2	2-3	1-2	1.350V/1.325V
2-3	1-2	2-3	2-3	1.300V/1.275V
2-3	2-3	1-2	1-2	1.250V/1.225V
2-3	2-3	1-2	2-3	1.200V/1.175V
2-3	2-3	2-3	1-2	1.150V/1.125V
2-3	2-3	2-3	2-3	1.100V/1.075V OR JUMPERLESS

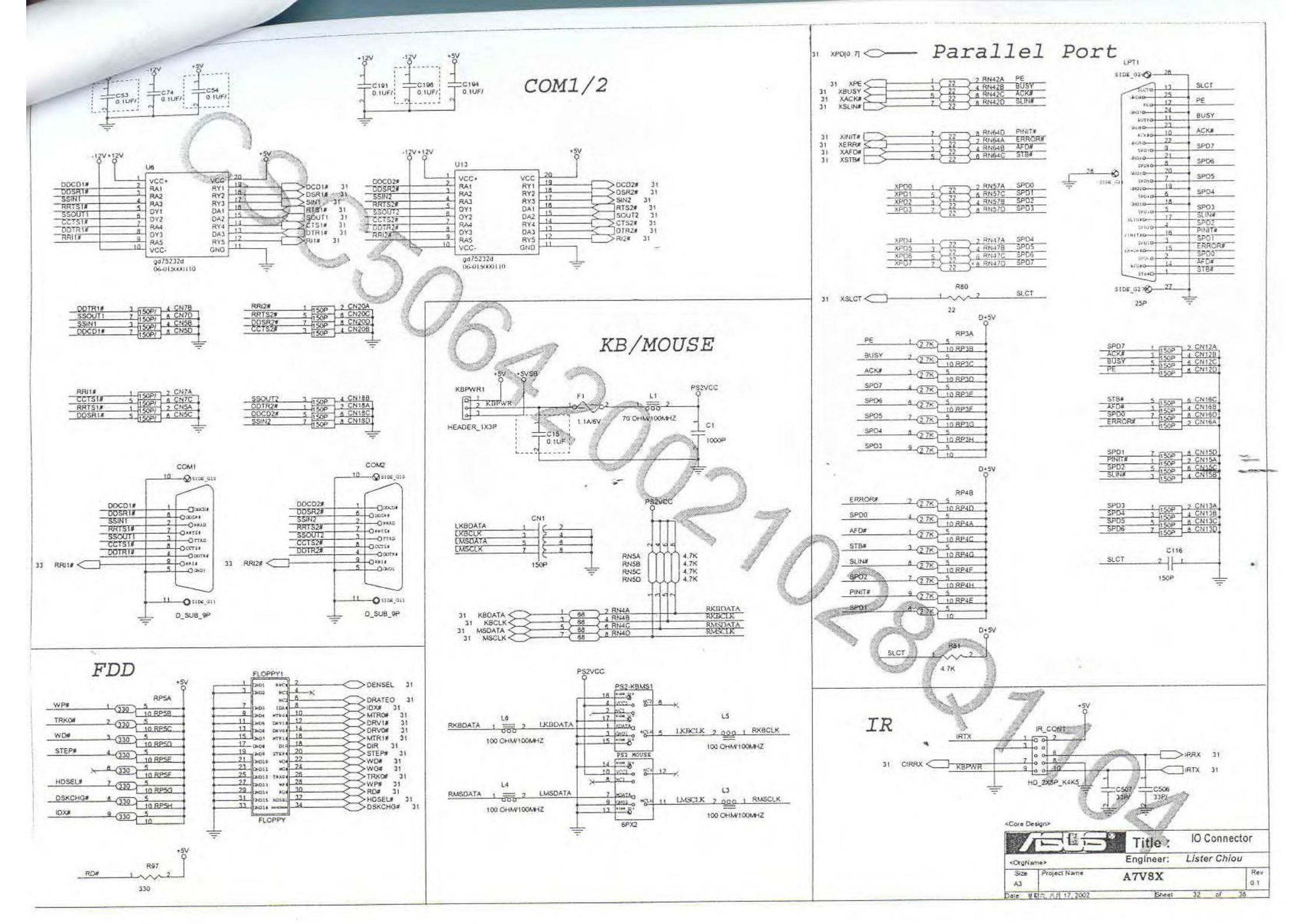
CSC50642002102301104
hexainf@hotmail.com

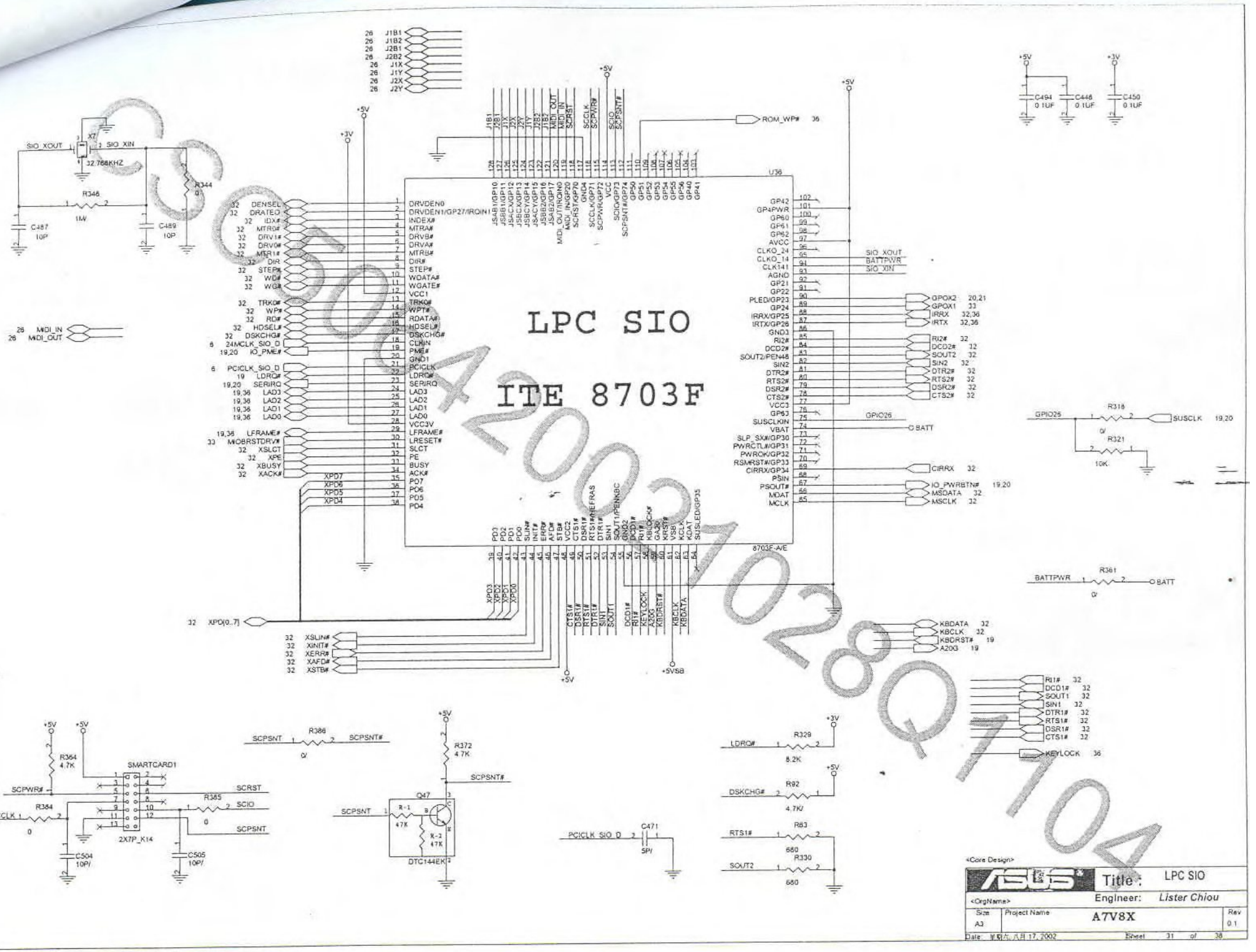


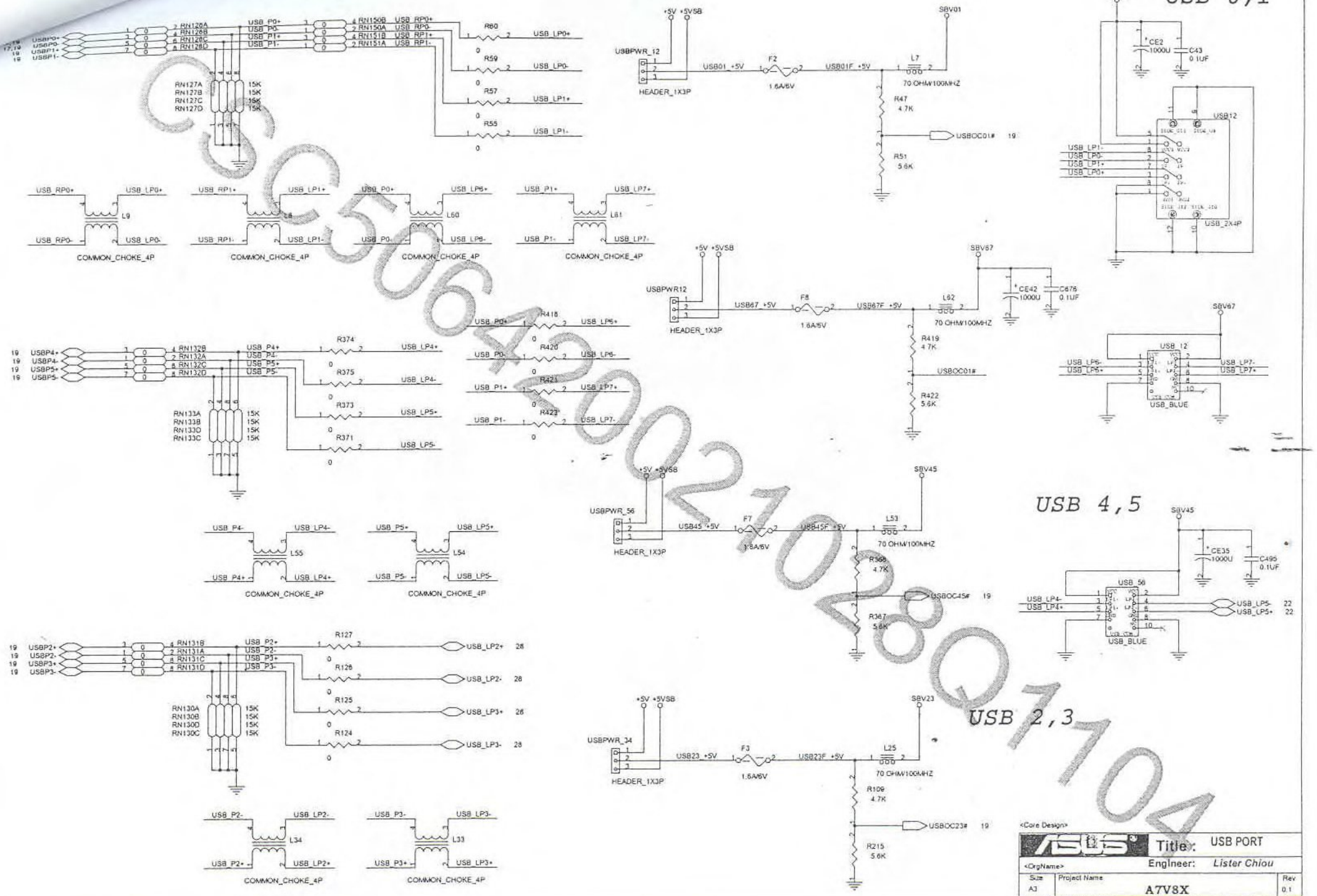
SSC5064200210280Q1104
hexanf@hotmail.com

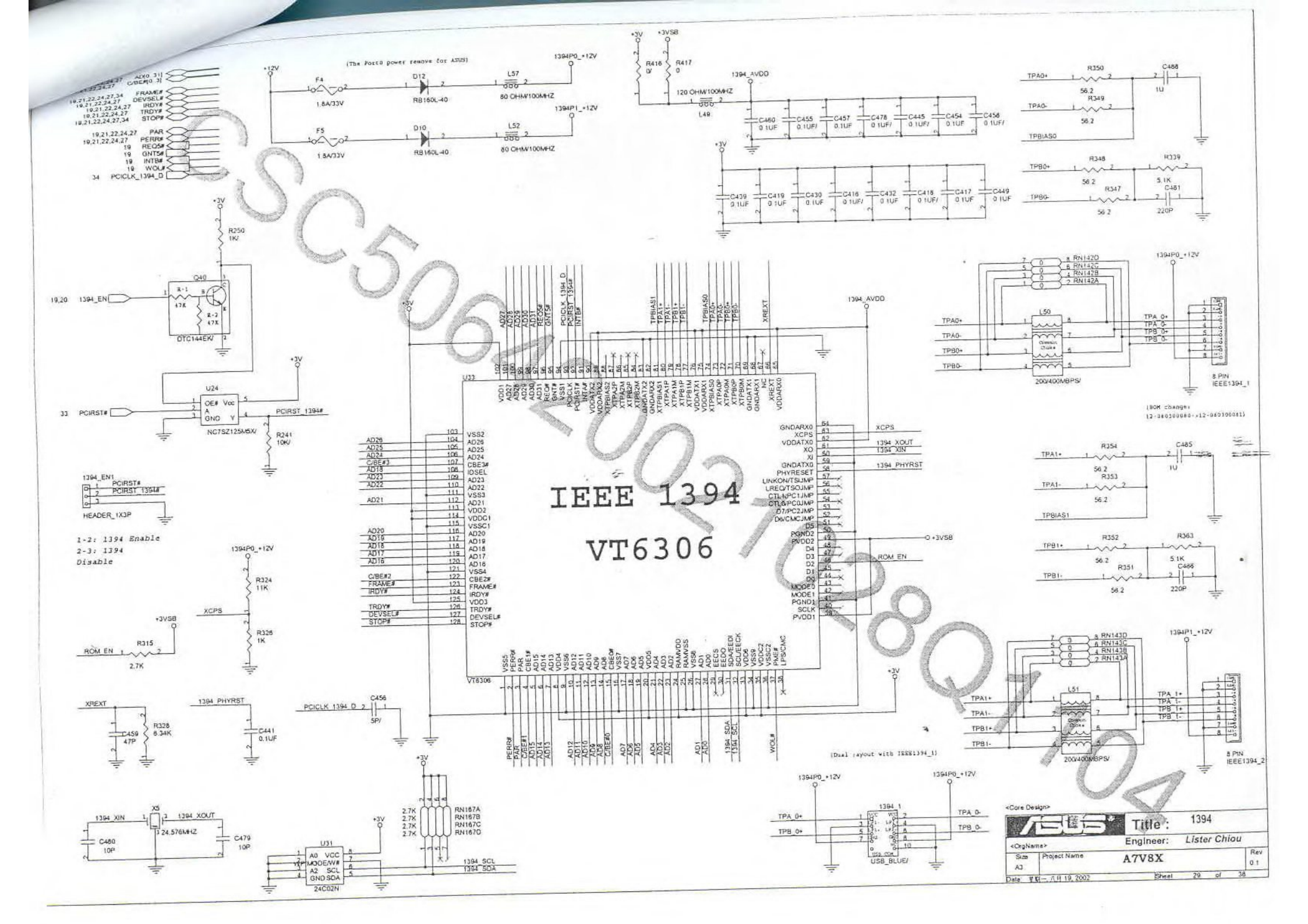

PCI Arbiter &
Clock Buffer
U7
ATXP5
U42
AT123S
U30
AS_007
Title: FID
Engineer: Lister Chiou
A7V8X
Rev 0.1
Sheet 34 of 38

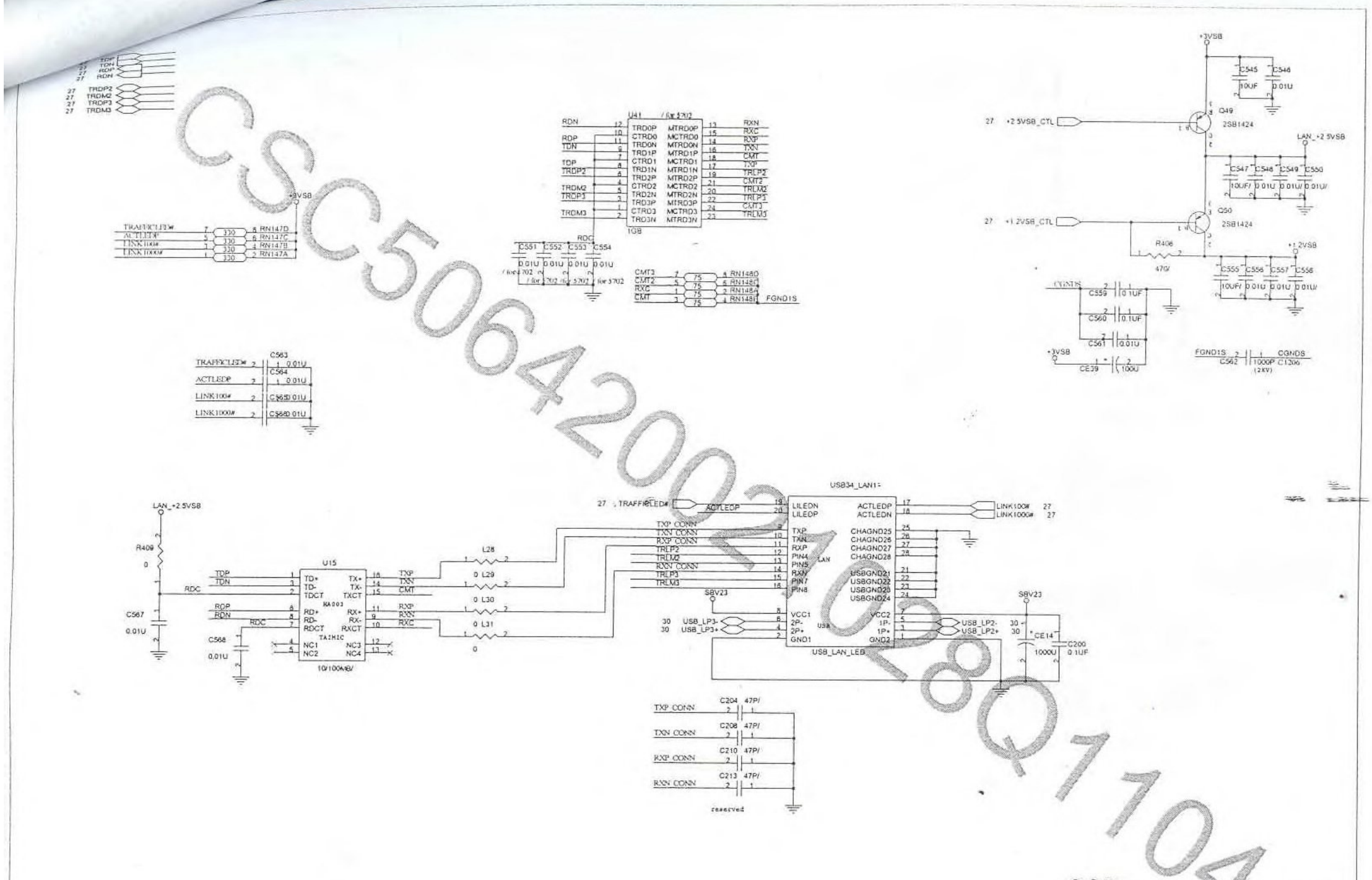

AS2K127F
PCB2,PCB1=10: Channel
PCB2,PCB1=01: Actabis
PCB2,PCB1=11: Magazine
PCB2,PCB1=00: Germany Magazine
Title : AS2K127F
Engineer: Lister Chiou
A7V8X
Date 十月 一, 八月 19, 2002
Sheet 33 of 38


COM1/2
Parallel Port
KB/MOUSE
FDD
IR
U6
U13
gd75232d
06-015000110
COM1
COM2
D_SUB_9P
FLOPPY1
FLOPPY
PS2-KBMS1
PS2_MOUSE
6PX2
LPT1
25P
IR_CON1
HD_2X5P_K4K5
<Core Design>
Title : IO Connector
Engineer: Lister Chiou
<OrgName>
Size A3
Project Name A7V8X
Rev 0.1
Date: 星期六, 八月 17, 2002
Sheet 32 of 36


LPC SIO
ITE 8703F
U36
8703F-A/E
SMARTCARD1
2X7P_K14
Q47
DTC144EK
ROM_WP# 36
SIO_XOUT
SIO_XIN
32.768KHZ
MIDI_IN
MIDI_OUT
GPIO26
BATT
BATTPWR
SUSCLK 19,20
KEYLOCK 36
PCICLK_SIO_D
SCPSNT
SCPSNT#
SCRST
SCIO
SCPWR#
SCCLK
LDRQ#
DSKCHG#
RTS1#
SOUT2
+5V
+3V
+5VSB
<Core Design>
Title : LPC SIO
<OrgName>
Engineer: Lister Chiou
Size A3
Project Name A7V8X
Rev 0.1
Date: 17, 2002
Sheet 31 of 38


USB 0,1
USB 4,5
USB 2,3
USB_2X4P
USB_BLUE
COMMON_CHOKE_4P
HEADER_1X3P
70 OHM/100MHZ
1.6A/6V
<Core Design>
Title: USB PORT
Engineer: Lister Chiou
A7V8X
Sheet 30 of 38

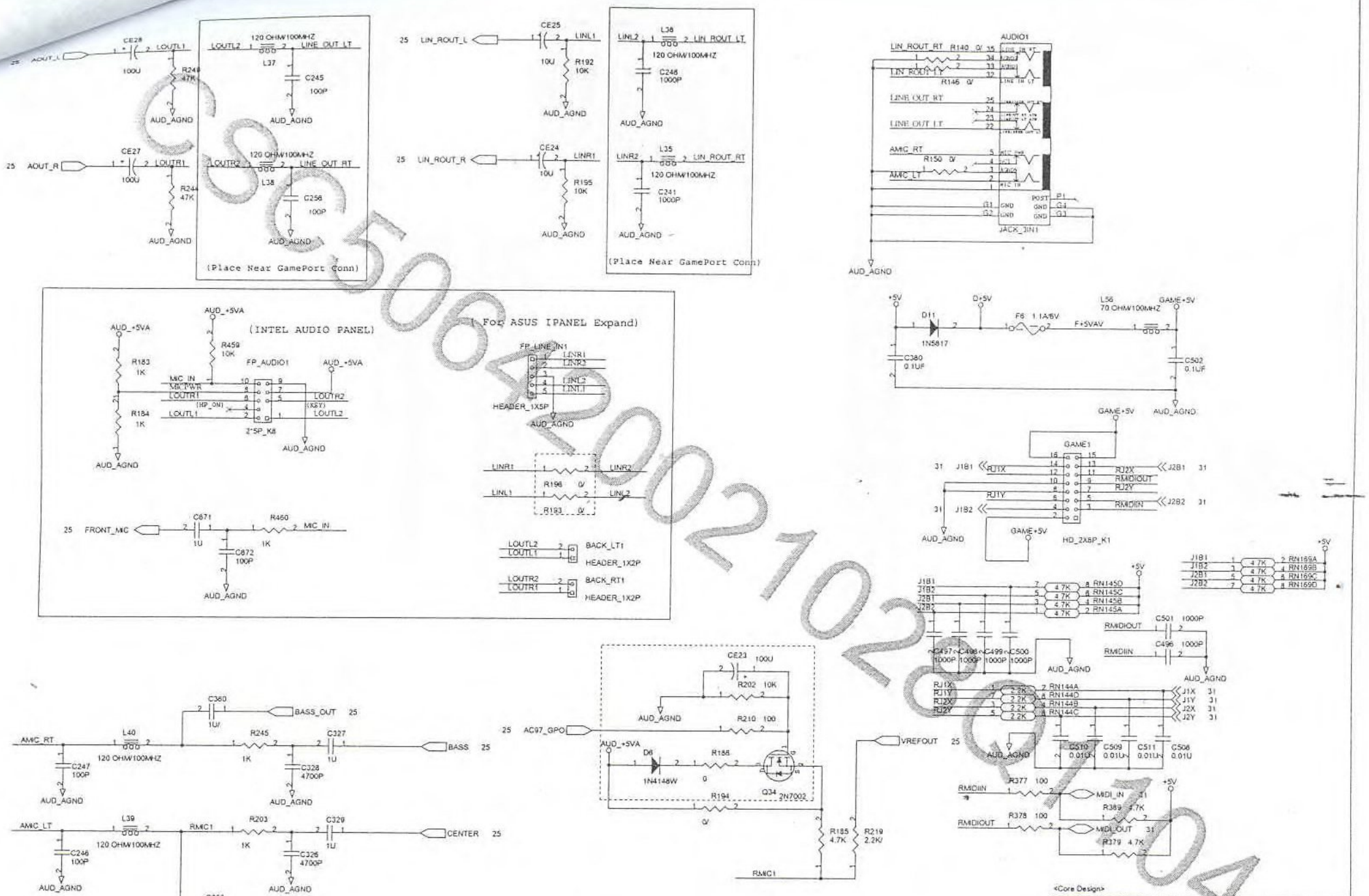

IEEE 1394
VT6306
1394_EN
PCIRST#
PCIRST_1394#
HEADER_1X3P
1-2: 1394 Enable
2-3: 1394 Disable
1394P0_+12V
1394P1_+12V
1394_AVDD
+3VSB
+3V
XCPS
ROM_EN
XREXT
1394_PHYRST
1394_XIN
1394_XOUT
1394_SCL
1394_SDA
PCICLK_1394_D
TPA0+
TPA0-
TPB0+
TPB0-
TPA1+
TPA1-
TPB1+
TPB1-
TPBIAS0
TPBIAS1
200/400MBPS/
8 PIN IEEE1394_1
8 PIN IEEE1394_2
USB_BLUE/
24C02N
NC7SZ125M5X/
DTC144EK/
(Dual layout with IEEE1394_1)
(BOM change: 12-000000080->12-000100081)
(The Port0 power remove for ASUS)
<Core Design>
Title: 1394
Engineer: Lister Chiou
A7V8X
Rev 0.1
Sheet 29 of 38



CSC50642002402 8Q1104

<Core Design>

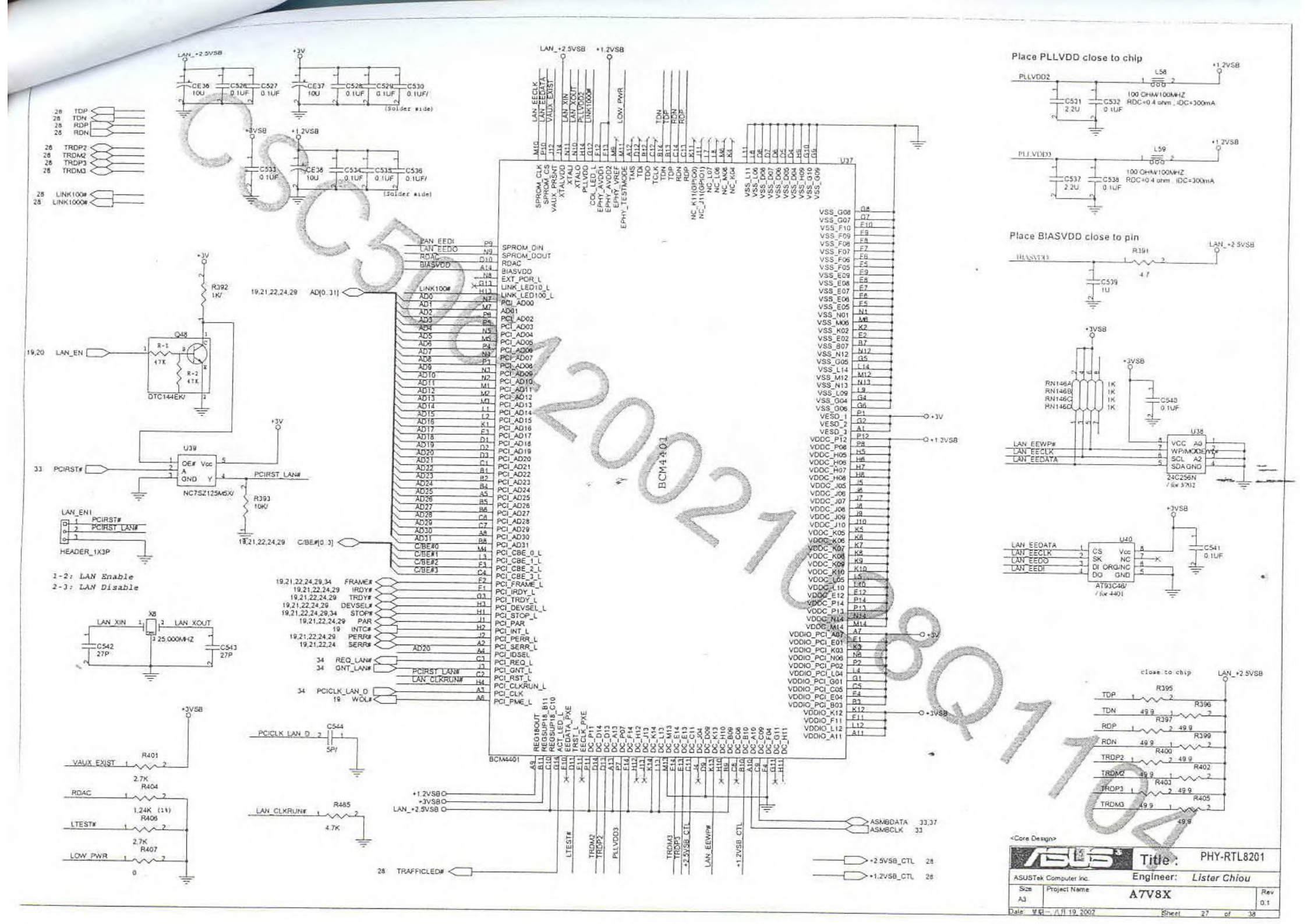
ASUSTek Computer Inc.	Title :	PHY-RTL8201	
	Engineer:	Lister Chiou	
Size A3	Project Name	A7V8X	Rev 0.1



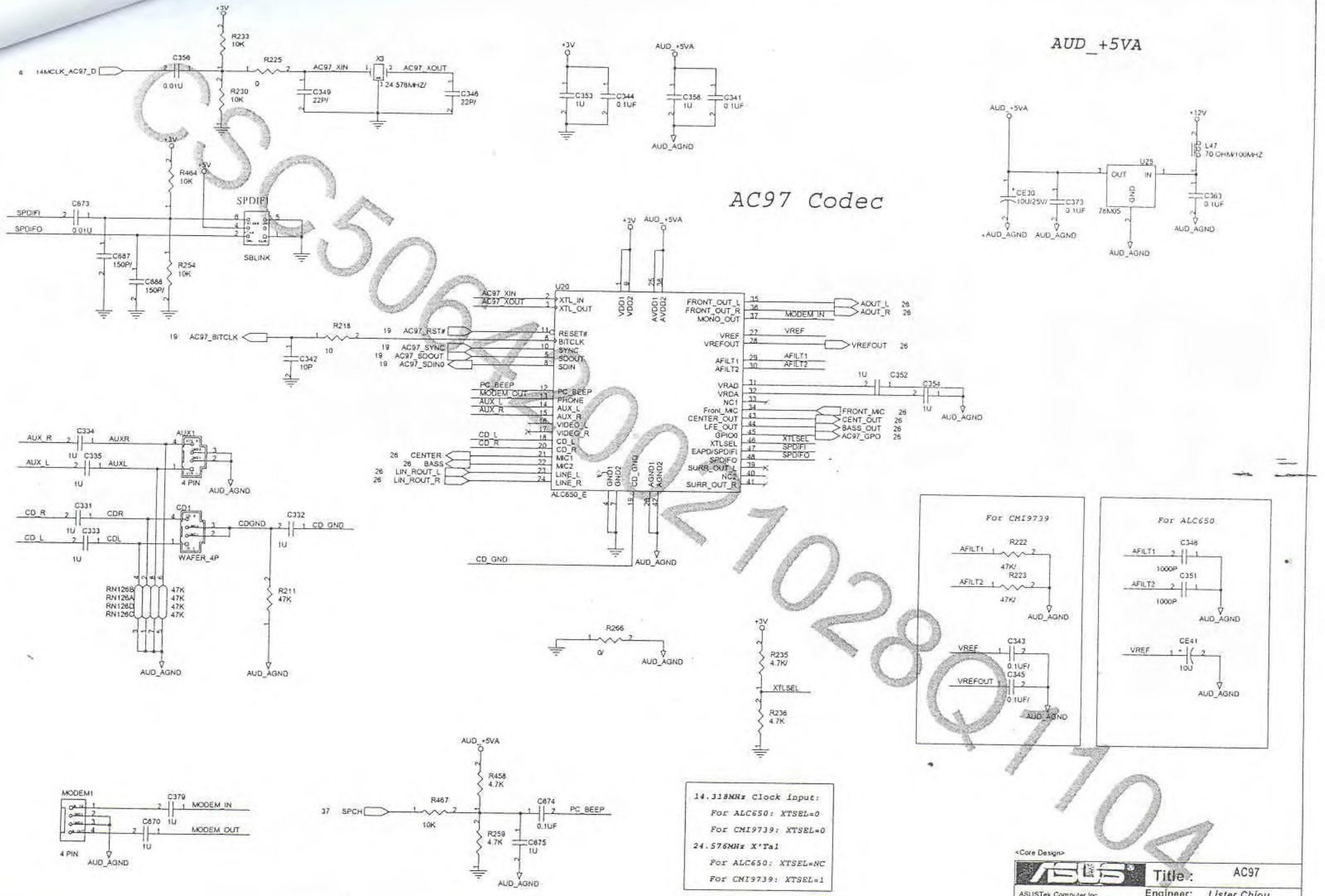
CSC50642002102001404

<Core Design>

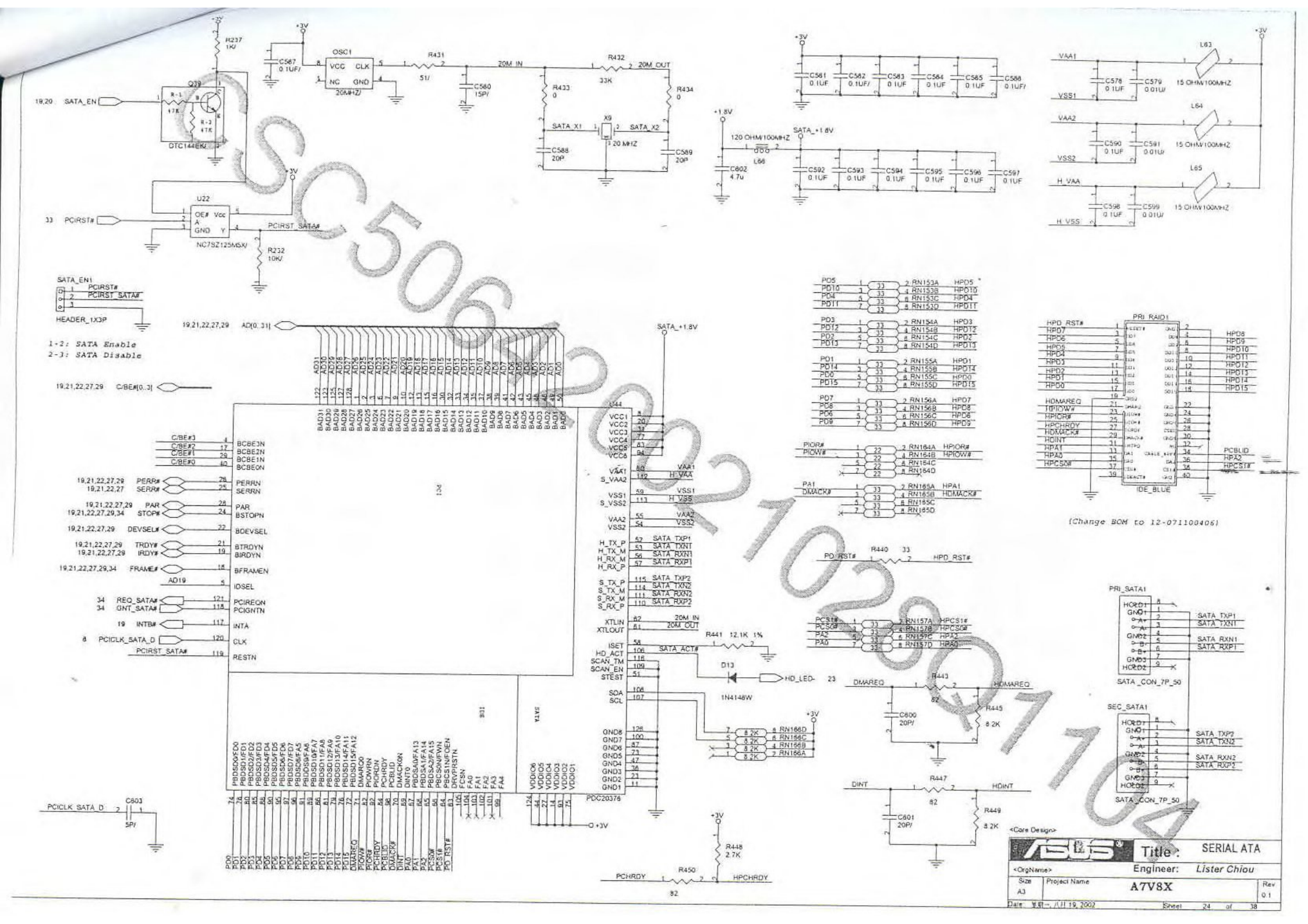
ASUS	Title:	Audio Connector	
ASUSTek Computer Inc.	Engineer:	Lister Chiou	
Size A3	Project Name	A7V8X	Rev 0.1
Date 星期六 八月 17, 2002	Sheet 26 of 38		



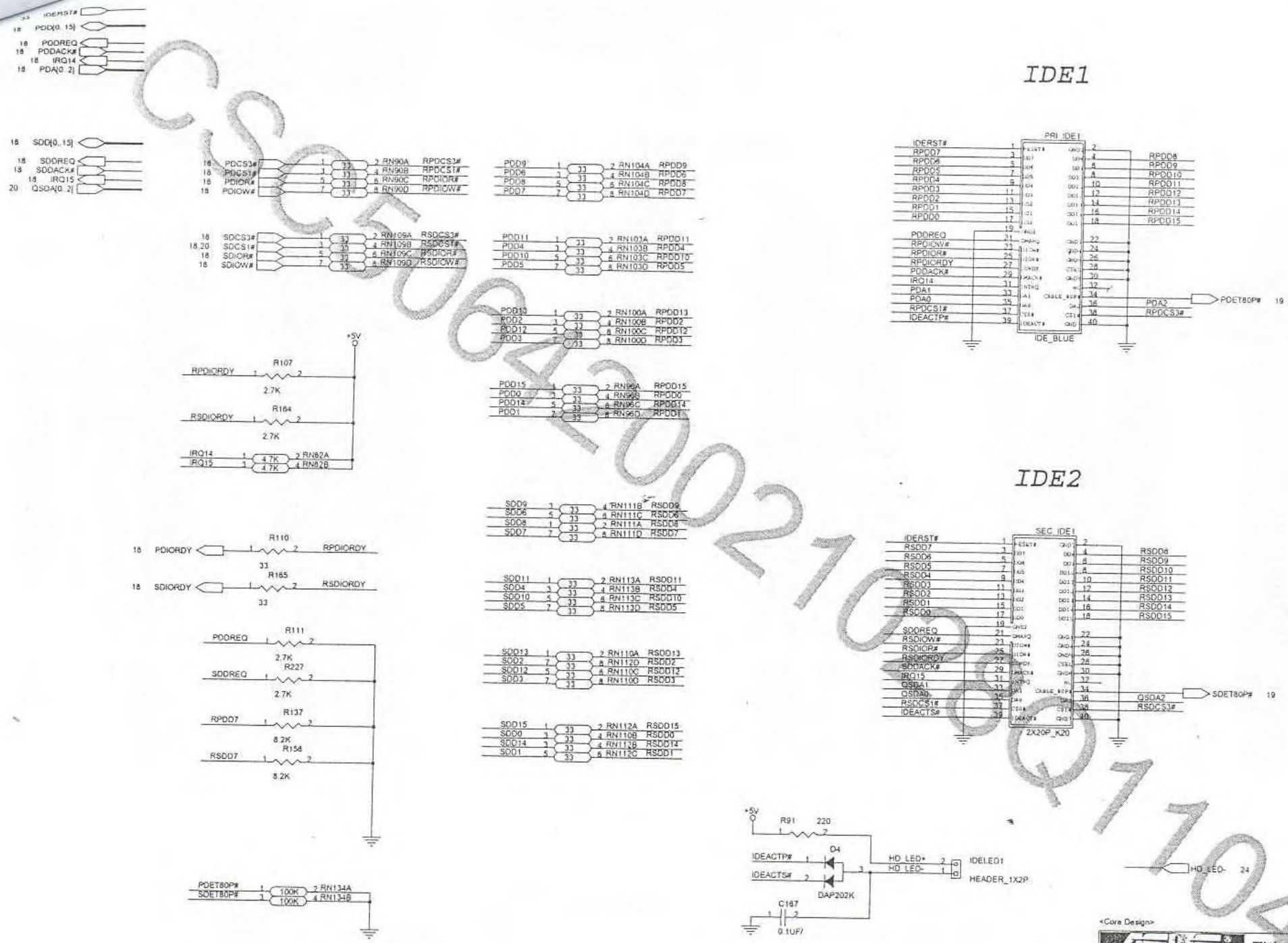
Place PLLVDD close to chip
Place BIASVDD close to pin
BCM4401
U37
U38
U39
U40
Q48
DTC144EK/
NC7SZ125M5X/
24C256N
AT93C46/
X8
25.000MHZ
HEADER_1X3P
1-2: LAN Enable
2-3: LAN Disable
close to chip
LAN_+2.5VSB
+1.2VSB
+3VSB
+3V
LAN_EN
PCIRST#
PCIRST_LAN#
LAN_EN1
LAN_XIN
LAN_XOUT
VAUX_EXIST
RDAC
LTEST#
LOW_PWR
LAN_CLKRUN#
PCICLK_LAN_D
TRAFFICLED#
ASMBDATA
ASMBCLK
+2.5VSB_CTL
+1.2VSB_CTL
<Core Design>
Title : PHY-RTL8201
ASUSTek Computer Inc.
Engineer: Lister Chiou
Size A3
Project Name A7V8X
Rev 0.1
Sheet 27 of 38

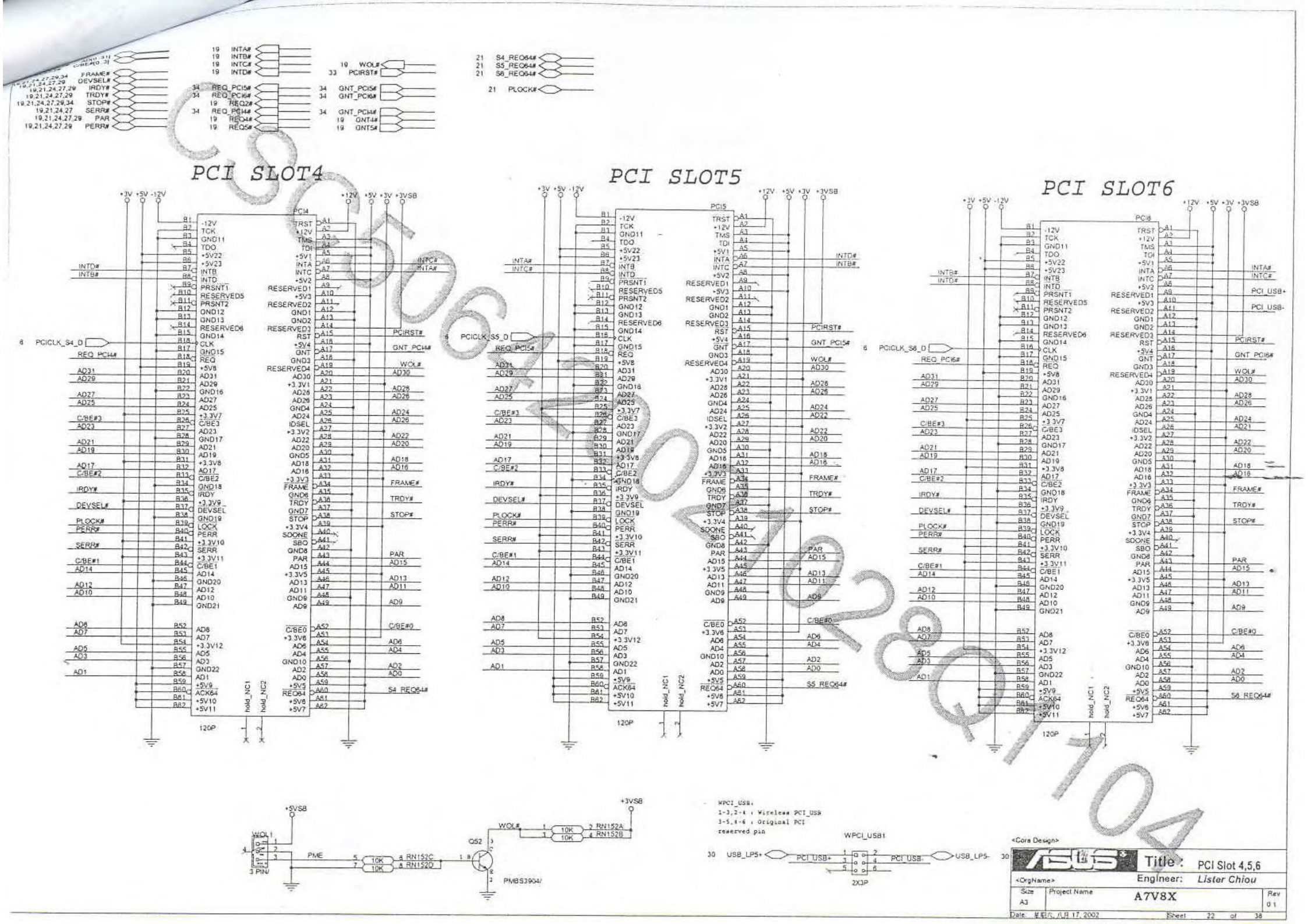


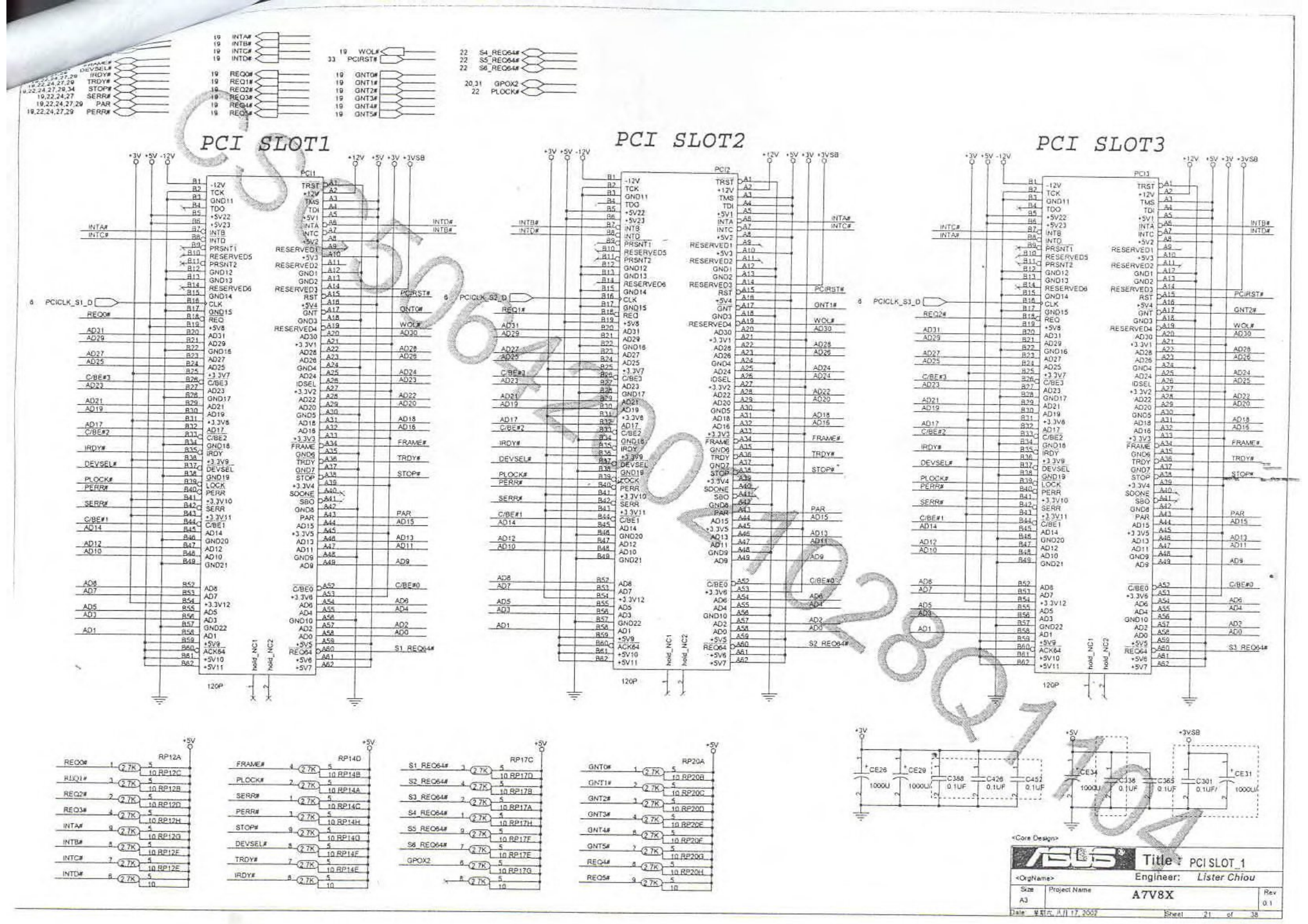
CSC50642002102801104

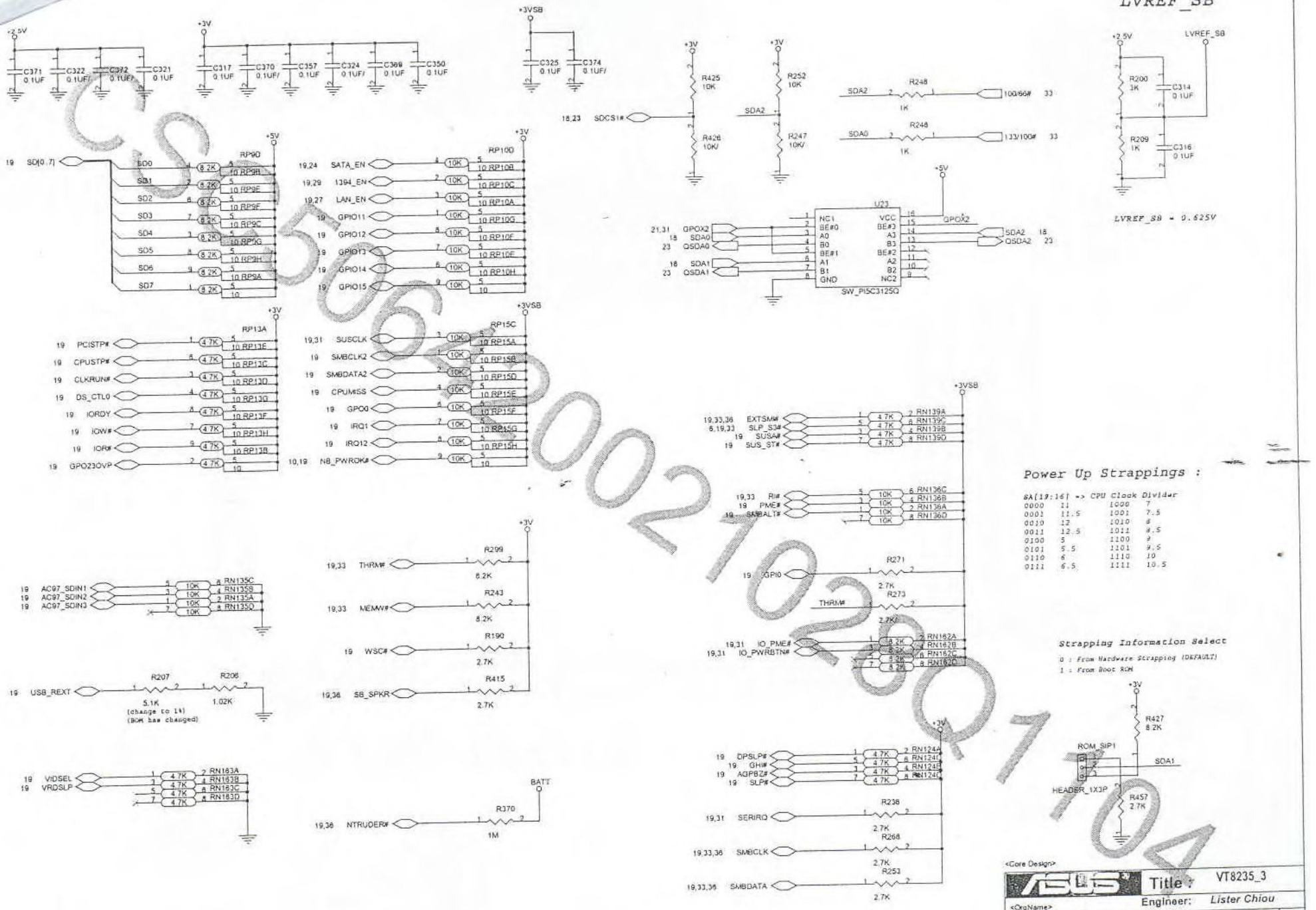


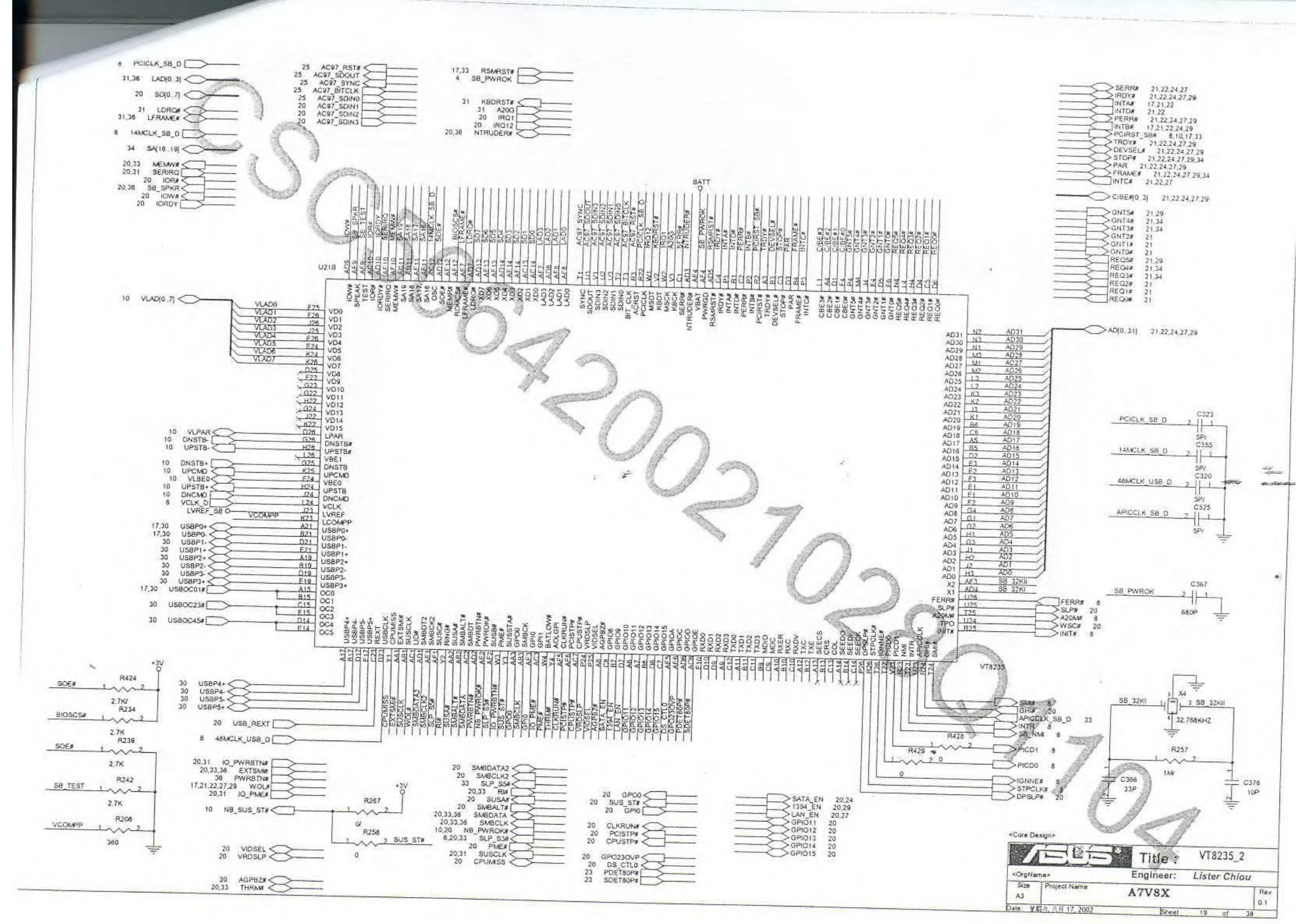
CSC50642002102821104


IDERST#
PDD[0..15]
PDDREQ
PDDACK#
IRQ14
PDA[0..2]
SDD[0..15]
SDDREQ
SDDACK#
IRQ15
QSDA[0..2]
PDCS3#
PDCS1#
PDIOR#
PDIOW#
RPDCS3#
RPDCS1#
RPDIOR#
RPDIOW#
SDCS3#
SDCS1#
SDIOR#
SDIOW#
RSDCS3#
RSDCS1#
RSDIOR#
RSDIOW#
RN90A
RN90B
RN90C
RN90D
RN109A
RN109B
RN109C
RN109D
RN104A
RN104B
RN104C
RN104D
RN103A
RN103B
RN103C
RN103D
RN100A
RN100B
RN100C
RN100D
RN96A
RN96B
RN96C
RN96D
RN111A
RN111B
RN111C
RN111D
RN113A
RN113B
RN113C
RN113D
RN110A
RN110B
RN110C
RN110D
RN112A
RN112B
RN112C
RN112D
RN134A
RN134B
PDD0
PDD1
PDD2
PDD3
PDD4
PDD5
PDD6
PDD7
PDD8
PDD9
PDD10
PDD11
PDD12
PDD13
PDD14
PDD15
SDD0
SDD1
SDD2
SDD3
SDD4
SDD5
SDD6
SDD7
SDD8
SDD9
SDD10
SDD11
SDD12
SDD13
SDD14
SDD15
+5V
R107
2.7K
RPDIORDY
R164
2.7K
RSDIORDY
IRQ14
IRQ15
4.7K
RN82A
RN82B
R110
PDIORDY
RPDIORDY
33
R165
SDIORDY
RSDIORDY
33
R111
2.7K
PDDREQ
R227
2.7K
SDDREQ
R137
8.2K
RPDD7
R158
8.2K
RSDD7
PDET80P#
SDET80P#
100K
IDE1
PRI_IDE1
RPDD0
RPDD1
RPDD2
RPDD3
RPDD4
RPDD5
RPDD6
RPDD7
RPDD8
RPDD9
RPDD10
RPDD11
RPDD12
RPDD13
RPDD14
RPDD15
PDDREQ
RPDIOW#
RPDIOR#
RPDIORDY
PDDACK#
IRQ14
PDA1
PDA0
RPDCS1#
IDEACTP#
PDA2
RPDCS3#
PDET80P#
19
IDE_BLUE
IDE2
SEC_IDE1
RSDD0
RSDD1
RSDD2
RSDD3
RSDD4
RSDD5
RSDD6
RSDD7
RSDD8
RSDD9
RSDD10
RSDD11
RSDD12
RSDD13
RSDD14
RSDD15
SDDREQ
RSDIOW#
RSDIOR#
RSDIORDY
SDDACK#
IRQ15
QSDA1
QSDA0
RSDCS1#
IDEACTS#
QSDA2
RSDCS3#
SDET80P#
19
ZX20P_K20
R91
220
IDEACTP#
IDEACTS#
D4
DAP202K
HD_LED+
HD_LED-
IDELED1
HEADER_1X2P
C167
0.1UF/
HD_LED-
24
<Core Design>
Title : IDE
<OrgName>
Engineer: Lister Chiou
Size A3
Project Name A7V8X
Rev 0.1

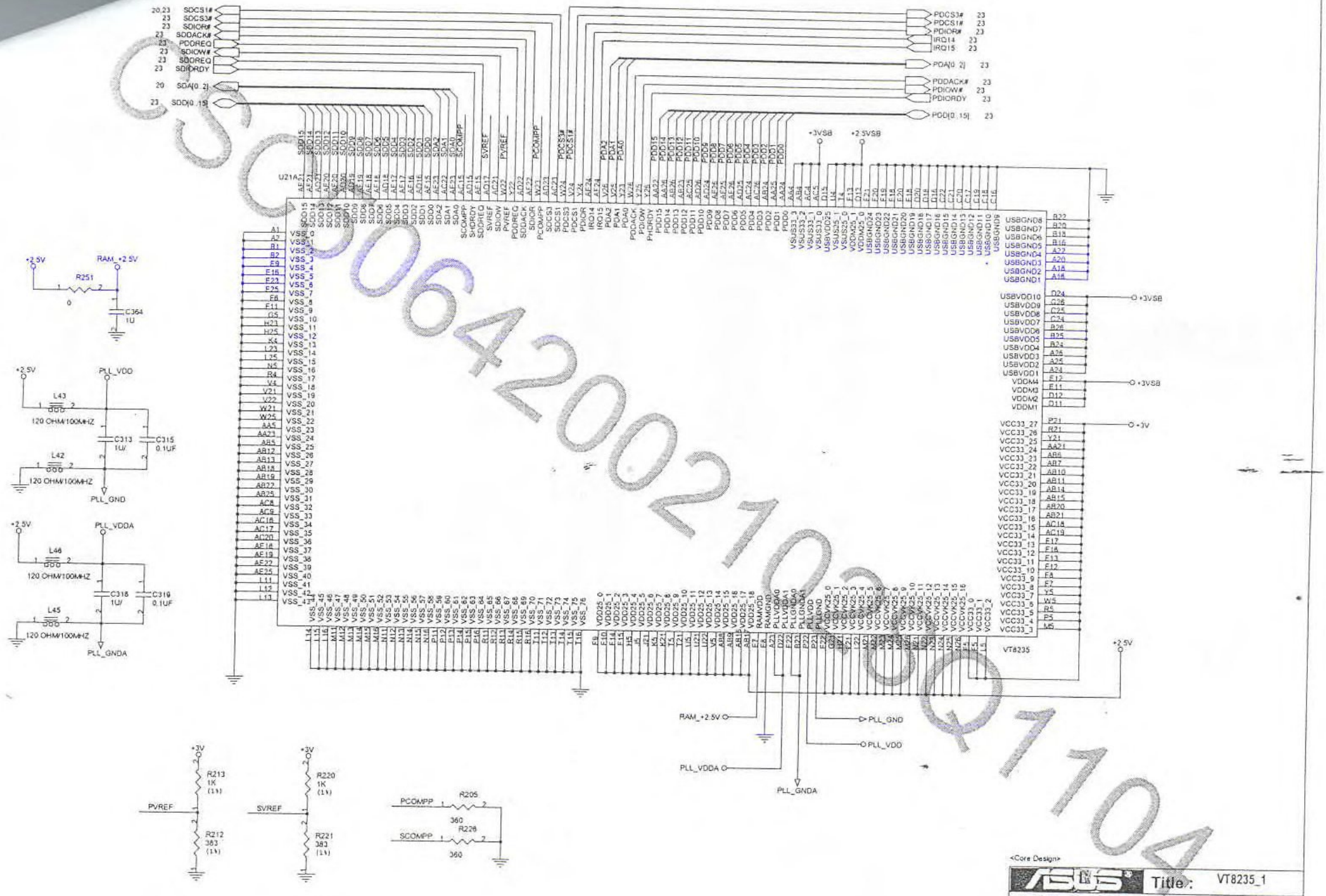

PCI SLOT4
PCI SLOT5
PCI SLOT6
PCI4
PCI5
PCI6
120P
WPCI_USB1
2X3P
PMBS3904/
WOL1
Q52
WPCI_USB:
1-3,2-4 : Wireless PCI_USB
3-5,4-6 : Original PCI
reserved pin
<Core Design>
Title : PCI Slot 4,5,6
Engineer: Lister Chiou
<OrgName>
Size A3
Project Name A7V8X
Rev 0.1
Date: 星期六, 八月 17, 2002
Sheet 22 of 38

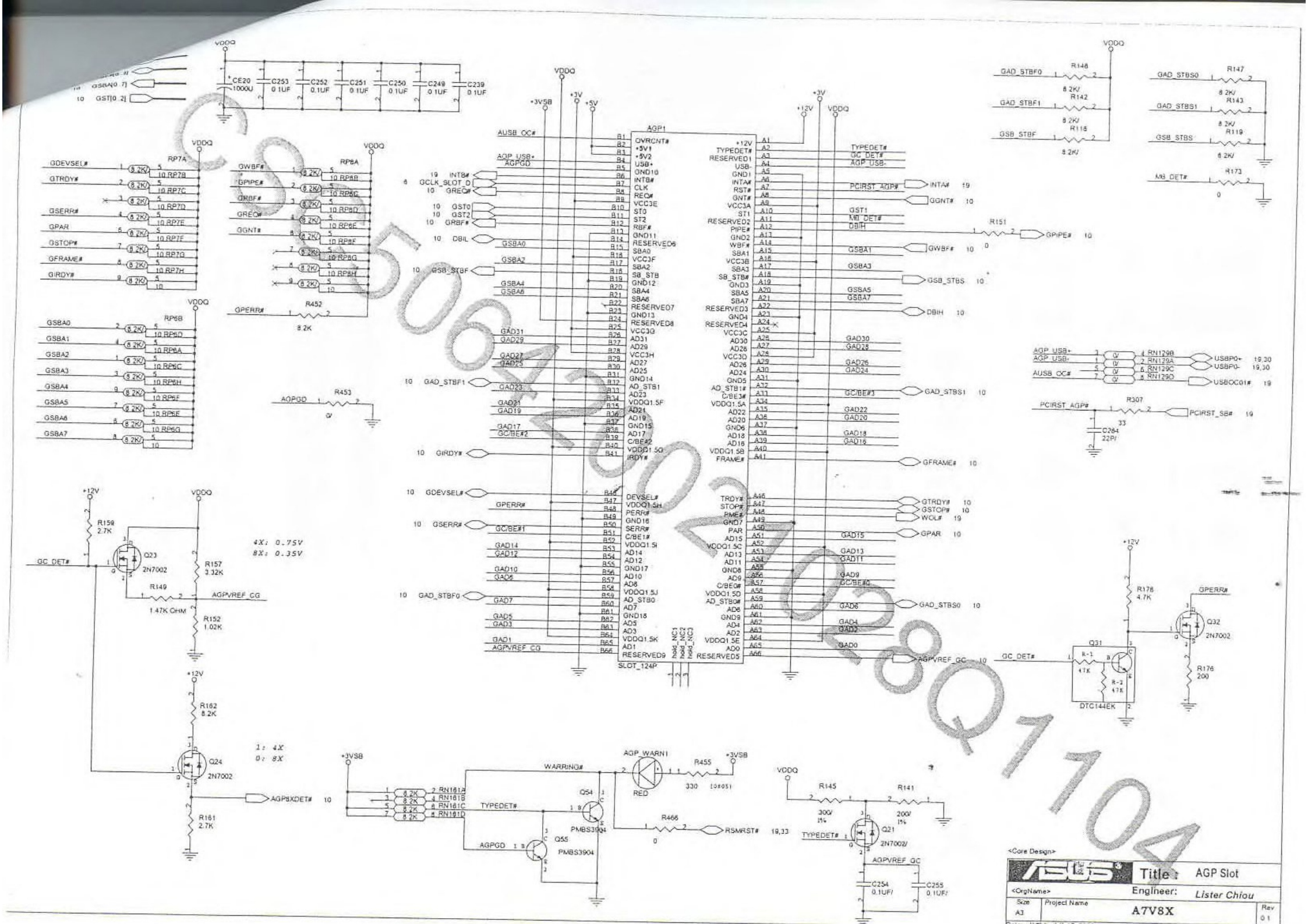

PCI SLOT1
PCI SLOT2
PCI SLOT3
INTA#
INTB#
INTC#
INTD#
PCICLK_S1_D
PCICLK_S2_D
PCICLK_S3_D
PCIRST#
FRAME#
IRDY#
TRDY#
STOP#
DEVSEL#
PLOCK#
PERR#
SERR#
PAR
C/BE#0
C/BE#1
C/BE#2
C/BE#3
S1_REQ64#
S2_REQ64#
S3_REQ64#
RP12A
RP14D
RP17C
RP20A
Title : PCI SLOT_1
Engineer: Lister Chiou
A7V8X
Sheet 21 of 38


LVREF_SB
LVREF_SB = 0.625V
Power Up Strappings :
SA[19:16] -> CPU Clock Divider
0000 11 1000 7
0001 11.5 1001 7.5
0010 12 1010 8
0011 12.5 1011 8.5
0100 5 1100 9
0101 5.5 1101 9.5
0110 6 1110 10
0111 6.5 1111 10.5
Strapping Information Select
0 : From Hardware Strapping (DEFAULT)
1 : From Boot ROM
<Core Design>
Title : VT8235_3
<OrgName>
Engineer: Lister Chiou
Size A3
Project Name A7V8X
Rev 0.1
Date: 四月 17, 2002
Sheet 20 of 38



U21B
VT8235
BATT
PCICLK_SB_D
LAD[0..3]
SD[0..7]
LDRQ#
LFRAME#
14MCLK_SB_D
SA[16..19]
MEMW#
SERIRQ
IOR#
SB_SPKR
IOW#
IORDY
AC97_RST#
AC97_SDOUT
AC97_SYNC
AC97_BITCLK
AC97_SDIN0
AC97_SDIN1
AC97_SDIN2
AC97_SDIN3
RSMRST#
SB_PWROK
KBDRST#
A20G
IRQ1
IRQ12
NTRUDER#
SERR#
IRDY#
INTA#
INTD#
PERR#
INTB#
PCIRST_SB#
TRDY#
DEVSEL#
STOP#
PAR
FRAME#
INTC#
C/BE#[0..3]
GNT5#
GNT4#
GNT3#
GNT2#
GNT1#
GNT0#
REQ5#
REQ4#
REQ3#
REQ2#
REQ1#
REQ0#
VLAD[0..7]
VLPAR
DNSTB-
UPSTB-
DNSTB+
UPCMD
VLBE0
UPSTB+
DNCMD
VCLK_D
LVREF_SB
VCOMPP
USBP0+
USBP0-
USBP1-
USBP1+
USBP2+
USBP2-
USBP3-
USBP3+
USBOC01#
USBOC23#
USBOC45#
AD[0..31]
PCICLK_SB_D
14MCLK_SB_D
48MCLK_USB_D
APICCLK_SB_D
SB_PWROK
C323
C355
C320
C525
C367
680P
FERR#
SLP#
A20M#
WSC#
INIT#
SB_32KI
SB_32KII
X4
32.768KHZ
R257
1M
C366
33P
C376
10P
SM#
GHI#
APICCLK_SB_D
INTR
SB_NMI
PICD1
PICD0
IGNNE#
STPCLK#
DPSLP#
R428
R429
SOE#
BIOSCS#
SB_TEST
VCOMPP
R424
R234
R239
R242
R206
2.7K
360
+3V
USBP4+
USBP4-
USBP5-
USBP5+
USB_REXT
48MCLK_USB_D
IO_PWRBTN#
EXTSMI#
PWRBTN#
WOL#
IO_PME#
NB_SUS_ST#
R267
R258
SUS_ST#
VIDSEL
VRDSLP
AGPBZ#
THRM#
SMBDATA2
SMBCLK2
SLP_S5#
RI#
SUSA#
SMBALT#
SMBDATA
SMBCLK
NB_PWROK#
SLP_S3#
PME#
SUSCLK
CPUMISS
GPO0
SUS_ST#
GPI0
CLKRUN#
PCISTP#
CPUSTP#
GPO23OVP
DS_CTL0
PDET80P#
SDET80P#
SATA_EN
1394_EN
LAN_EN
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
<Core Design>
Title : VT8235_2
<OrgName>
Engineer: Lister Chiou
Size A3
Project Name A7V8X
Rev 0.1
Date: 星期六, 八月 17, 2002
Sheet 19 of 38

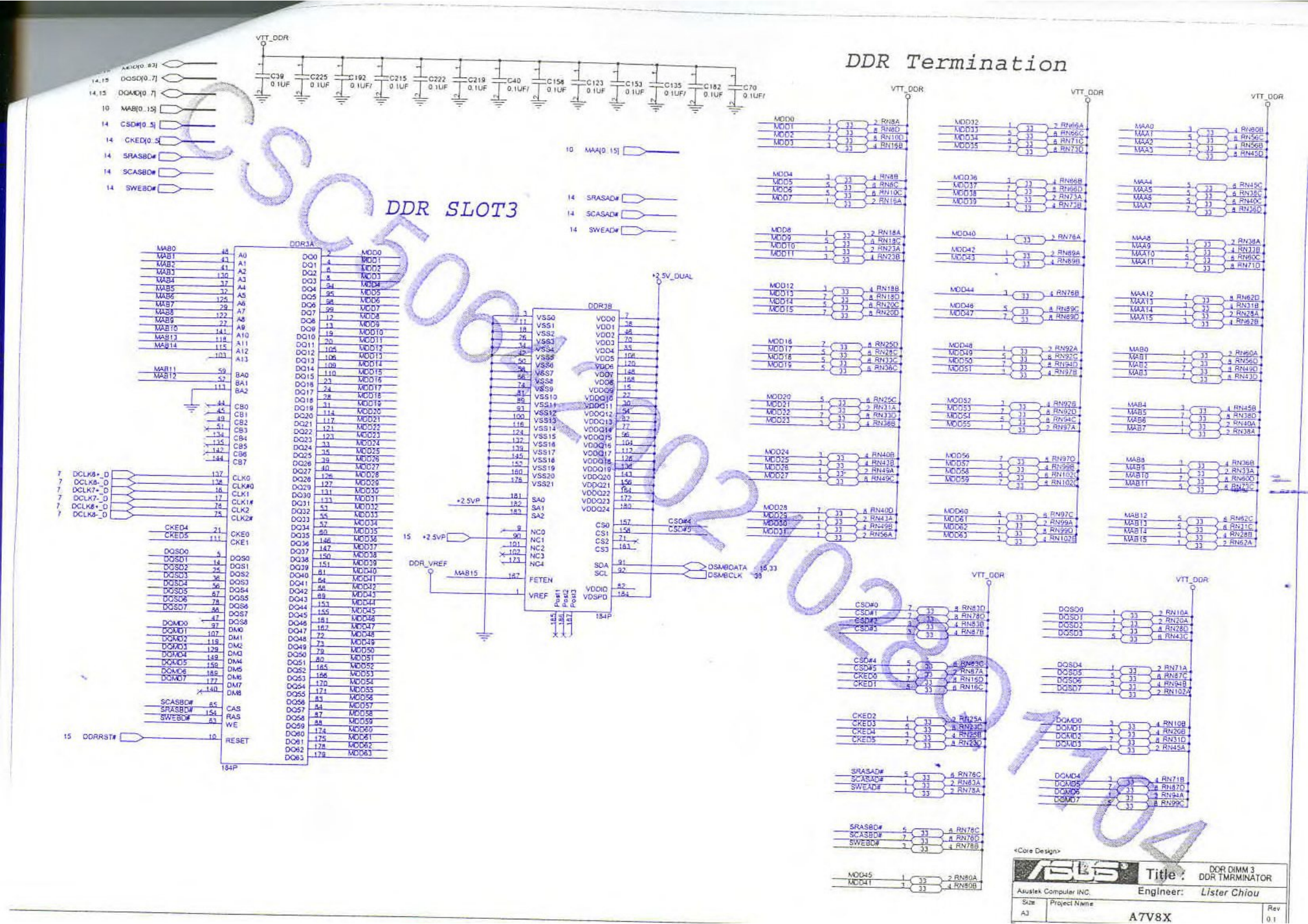

SDCS1#
SDCS3#
SDIOR#
SDDACK#
PDDREQ
SDIOW#
SDDREQ
SDIORDY
SDA[0..2]
SDD[0..15]
PDCS3#
PDCS1#
PDIOR#
IRQ14
IRQ15
PDA[0..2]
PDDACK#
PDIOW#
PDIORDY
PDD[0..15]
U21A
+3VSB
+2.5VSB
VT8235
+3V
+2.5V
RAM_+2.5V
PLL_GND
PLL_VDO
PLL_VDDA
PLL_GNDA
R251
C364
1U
L43
120 OHM/100MHZ
C313
1UF
C315
0.1UF
L42
L46
C318
C319
L45
R213
1K
PVREF
R212
383
R220
SVREF
R221
R205
PCOMPP
360
R226
SCOMPP
<Core Design>
Title: VT8235_1
Engineer: Lister Chiou
A7V8X
Rev 0.1
Sheet 18 of 35

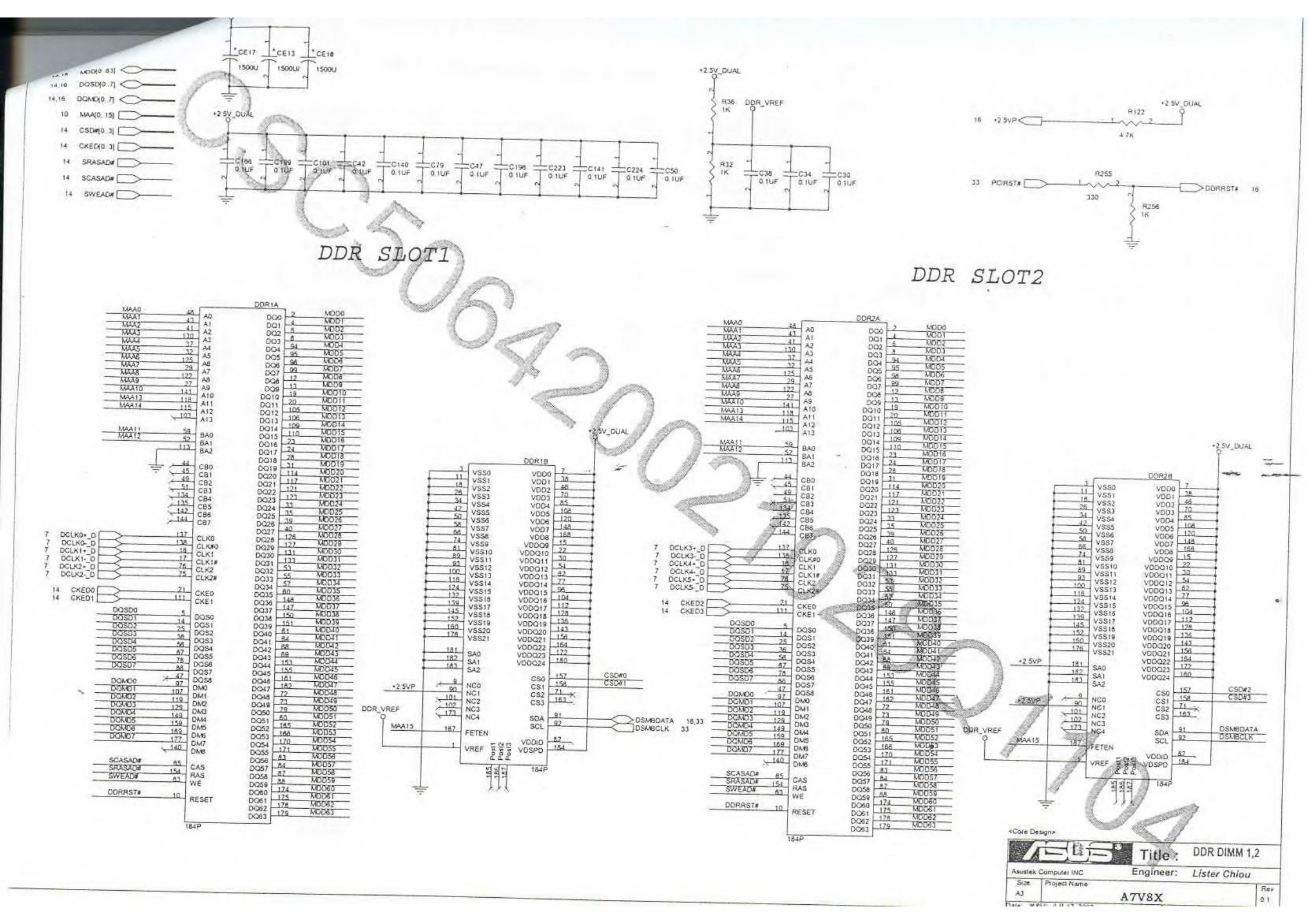


ES506XS02Q1104

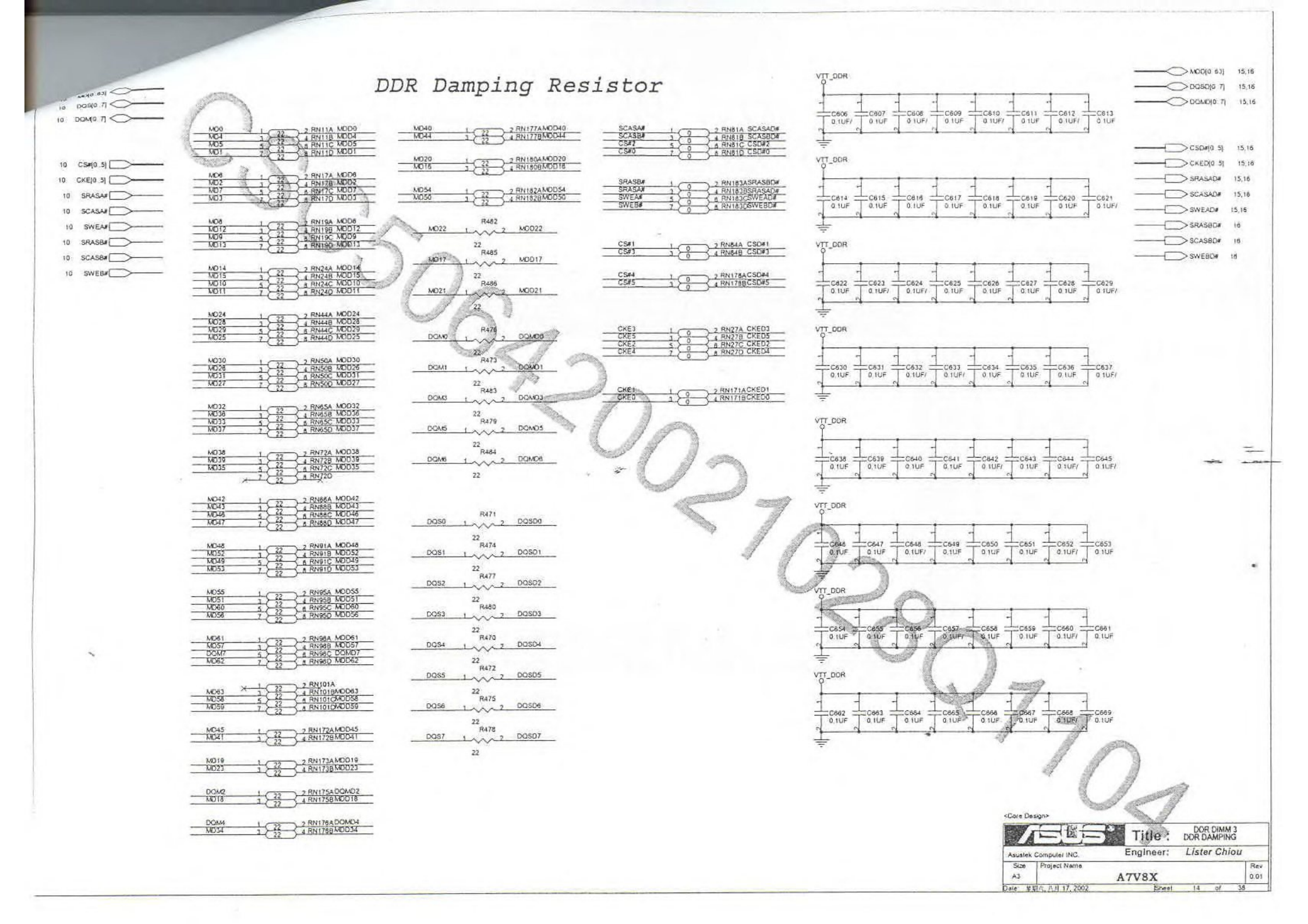
<Core Design>

<OrgName>	Title : AGP Slot	
	Engineer: Lister Chiou	
Size A3	Project Name A7V8X	Rev 0.1


DDR Termination
DDR SLOT3
VTT_DDR
DDR3A
DDR3B
+2.5V_DUAL
+2.5VP
DDR_VREF
184P
<Core Design>
Title : DDR DIMM 3 DDR TMRMINATOR
Asustek Computer INC.
Engineer: Lister Chiou
Size A3
Project Name A7V8X
Rev 0.1


DDR SLOT1
DDR SLOT2
DDR1A
DDR1B
DDR2A
DDR2B
184P
+2.5V_DUAL
+2.5VP
DDR_VREF
MAA15
DSMBDATA
DSMBCLK
CSD#0
CSD#1
CSD#2
CSD#3
PCIRST#
DDRRST#
R122
4.7K
R255
330
R256
1K
R36
1K
R32
1K
C38
0.1UF
C34
0.1UF
C30
0.1UF
C50
0.1UF
C224
0.1UF
C141
0.1UF
C223
0.1UF
C198
0.1UF
C47
0.1UF
C140
0.1UF
C42
0.1UF
C101
0.1UF
C199
0.1UF
C166
0.1UF
CE17
1500U
CE13
1500U
CE18
1500U
MDD[0..63]
DQSD[0..7]
DQMD[0..7]
MAA[0..15]
CSD#[0..3]
CKED[0..3]
SRASAD#
SCASAD#
SWEAD#
DCLK0+_D
DCLK0-_D
DCLK1+_D
DCLK1-_D
DCLK2+_D
DCLK2-_D
DCLK3+_D
DCLK3-_D
DCLK4+_D
DCLK4-_D
DCLK5+_D
DCLK5-_D
CKED0
CKED1
CKED2
CKED3
DQSD0
DQMD0
SCASAD#
SRASAD#
SWEAD#
DDRRST#
<Core Design>
Title: DDR DIMM 1,2
Asustek Computer INC
Engineer: Lister Chiou
Size A3
Project Name A7V8X
Rev 0.1

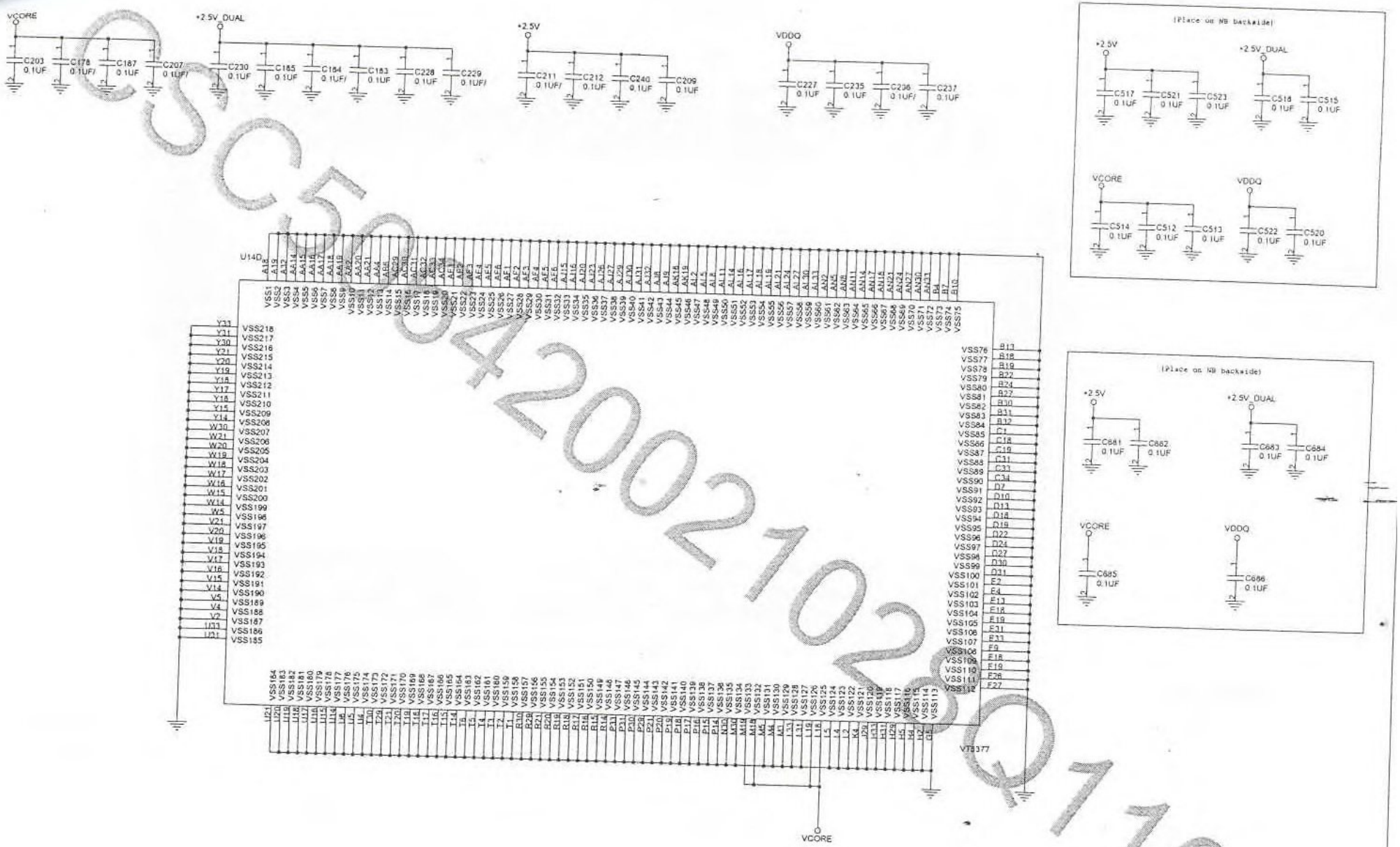
DDR Damping Resistor



CS3506A2002102800104

<Core Design>

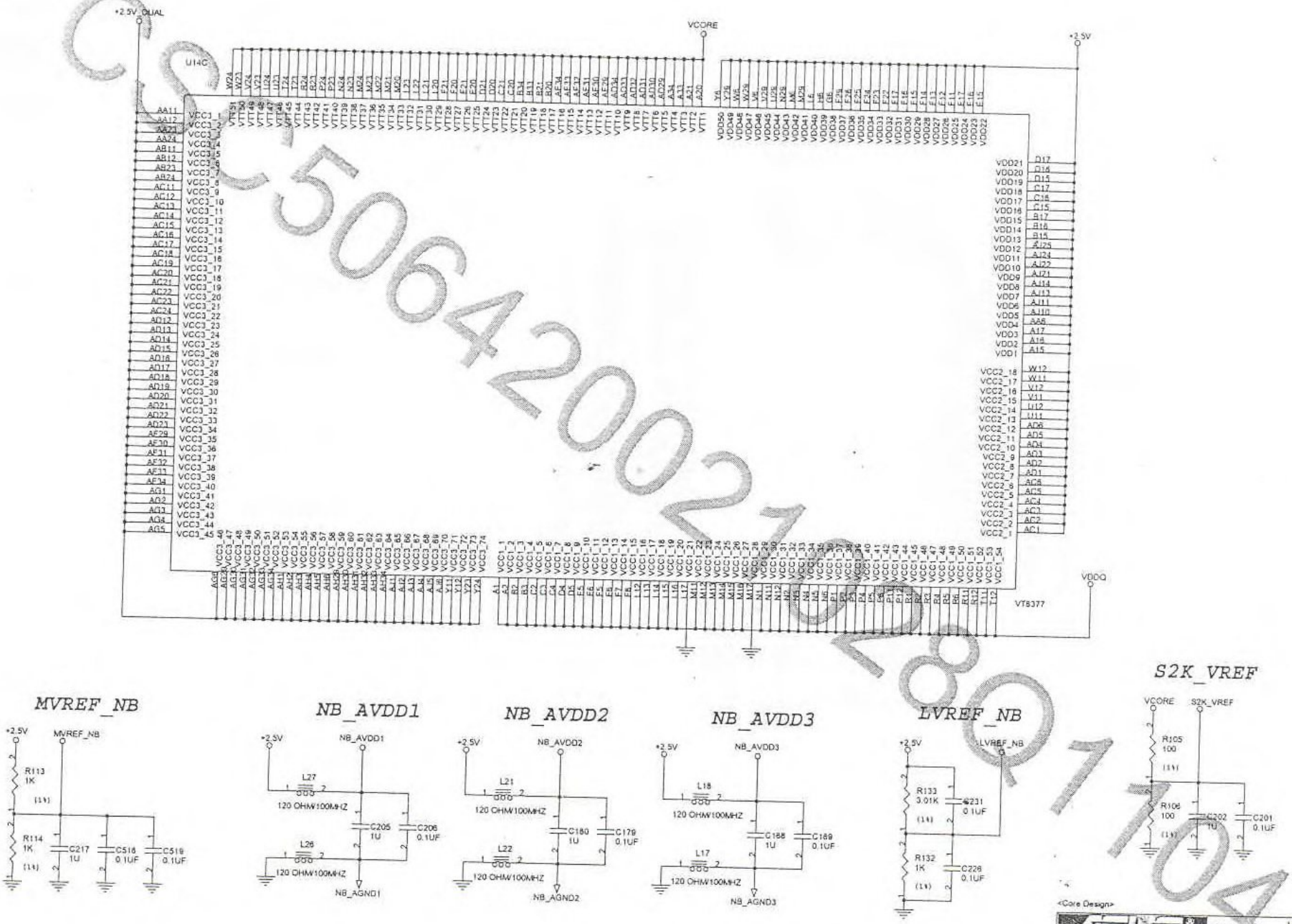
ASUS	Title :	DDR DIMM 3 DDR DAMPING
Asustek Computer INC.	Engineer:	Lister Chiou
Size: A3	Project Name: A7V8X	Rev: 0.01
Date: 十月 17, 2002	Sheet 14 of 38	



SC5042002102300Q1104

<Core Design>

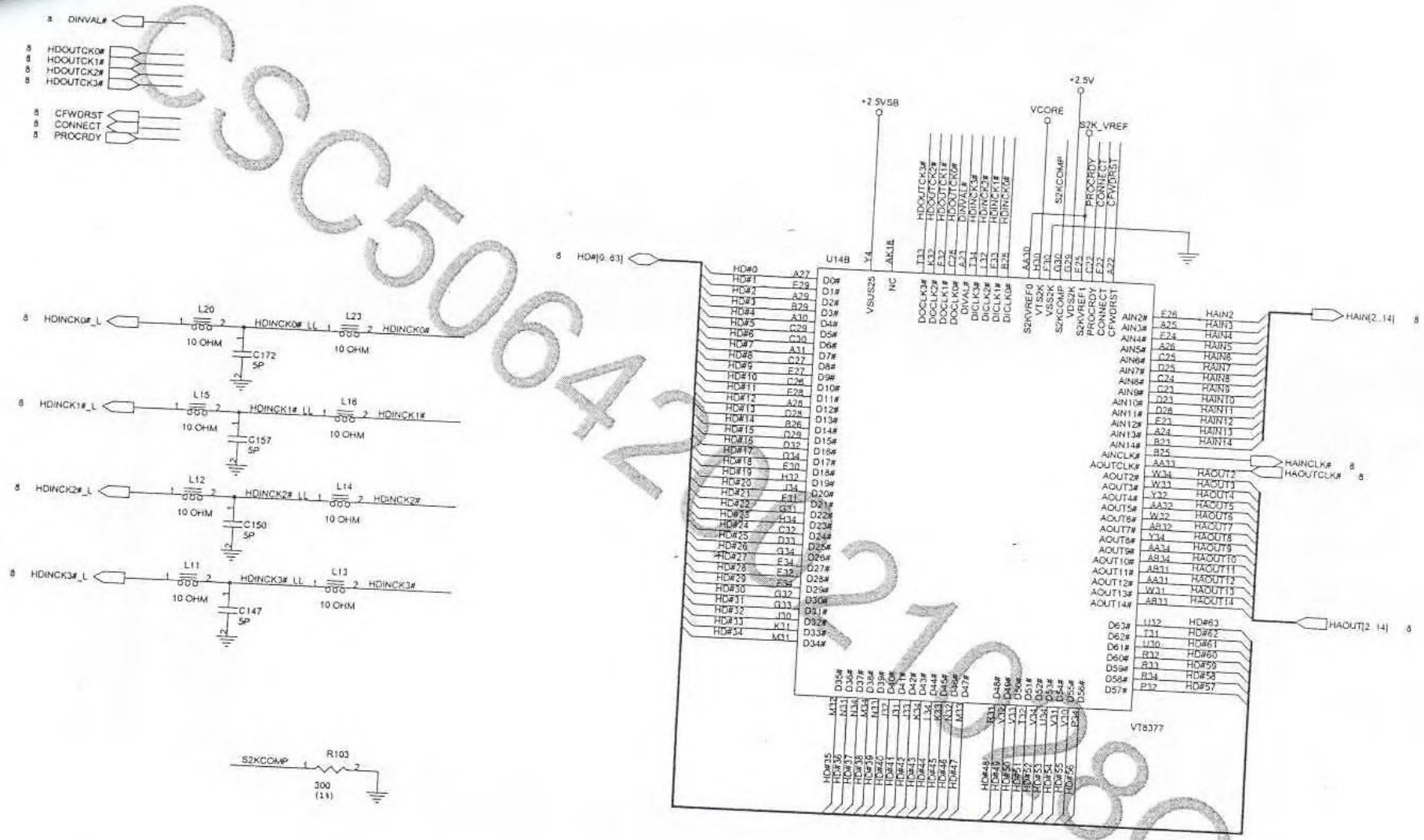
<OrgName>	Title: VT8377_4	
	Engineer: Lister Chiou	
Size: A3	Project Name: A7V8X	Rev: 0.1
Date: 星期六, 八月 17, 2002	Sheet 13 of 38	



CSC50642002102801104

<Core Design>

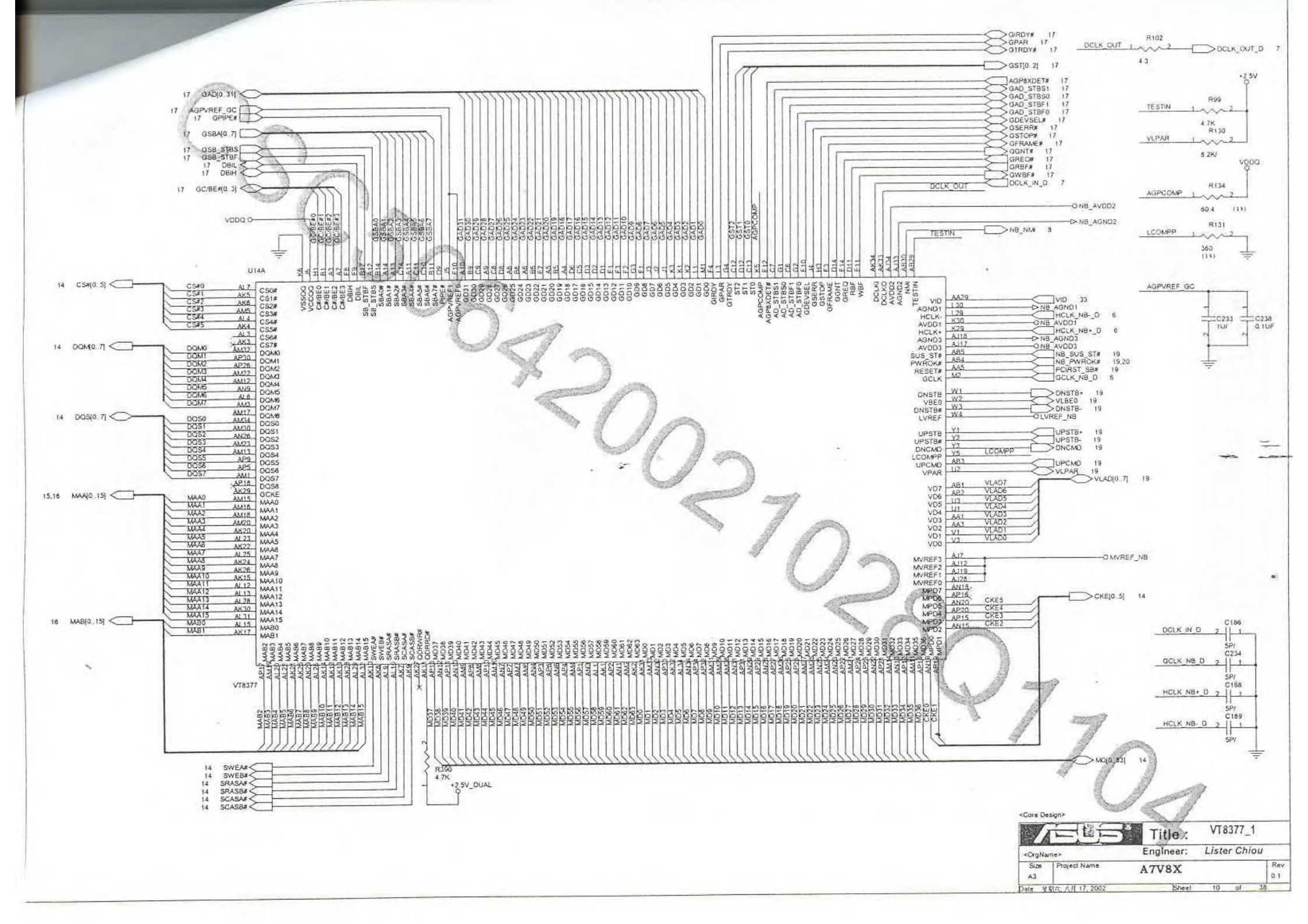
ASUS	Title :	VT8377_3	
<OrgName>	Engineer:	Lister Chiou	
Size A3	Project Name	A7V8X	Rev 0.1
Date: 星期六, 八月 17, 2002	Sheet 12 of 38		

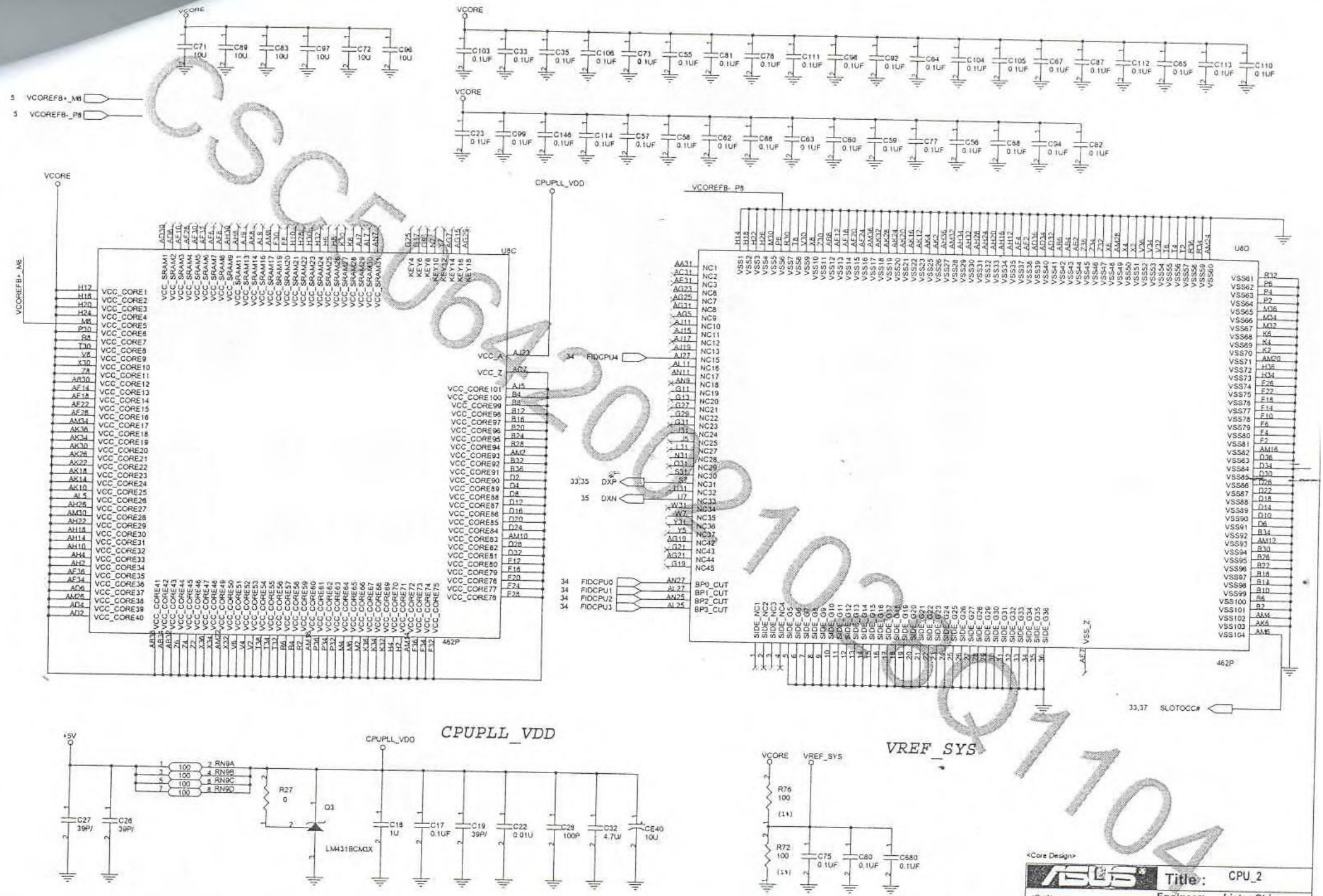


CSC50642002108Q1104

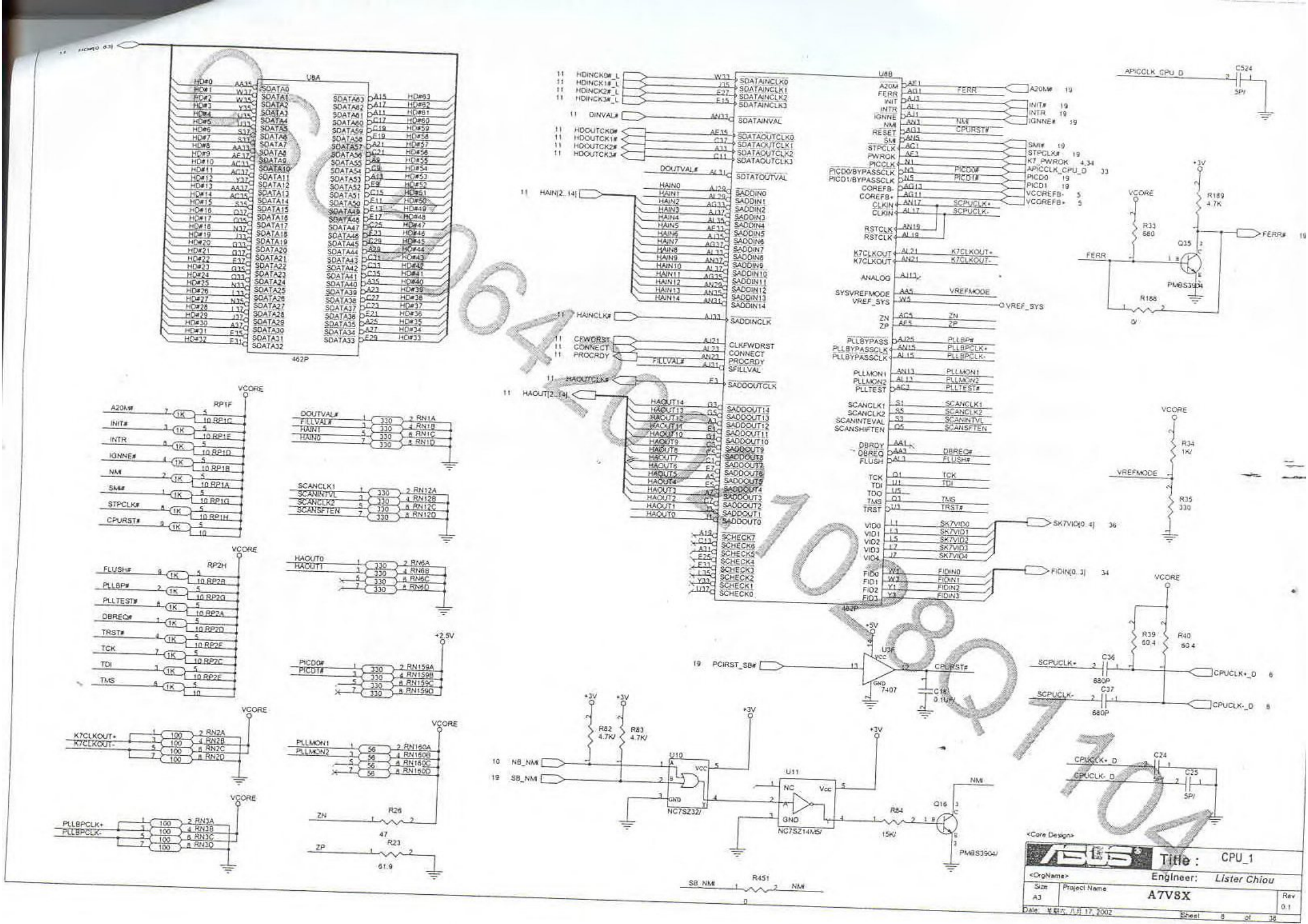
<Core Design>

ASUS	Title:	VT8377_2
<OrgName>	Engineer:	Lister Chiou
Size A3	Project Name A7V8X	Rev 0.1
Date: 星期六, 八月 17, 2002	Sheet 11 of 38	


U14A
VT8377
R390
4.7K
+2.5V_DUAL
R102
DCLK_OUT
DCLK_OUT_D
R99
4.7K
R130
8.2K/
R134
60.4
R131
360
C233
10/
C238
0.1UF
C186
C234
C188
C189
5P/
Title: VT8377_1
Engineer: Lister Chiou
<OrgName>
Project Name
A7V8X
Size
A3
Rev
0.1
Date: 八月 17, 2002
Sheet 10 of 38
<Core Design>



CSCE64200102Q1104



U8A
462P
U8B
462P
RP1F
RP2H
U3F
7407
U10
NC7SZ32/
U11
NC7SZ14M5/
Q16
PMBS3904/
Q35
PMBS3904
APICCLK_CPU_D
VCORE
+2.5V
+3V
+5V
VREF_SYS
VREFMODE
SK7VID[0..4]
FIDIN[0..3]
PCIRST_SB#
CPURST#
SCPUCLK+
SCPUCLK-
CPUCLK+_D
CPUCLK-_D
NB_NMI
SB_NMI
NMI
<Core Design>
Title : CPU_1
<OrgName>
Engineer: Lister Chiou
Size A3
Project Name A7V8X
Rev 0.1
Date: 星期六, 八月 17, 2002
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