JE40 HR
DIS/UMA/Muxless Schematics Document
Sandy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

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JE40 HR Block Diagram (Discrete/UMA/co-lay)

Project code : 91.4IQ01.001
PCB P/N : 48.4IQ01.0SA
Revision : 10267-1

##OnMainBoard

VRAM
2GB/1GB/512MB
88,89,90,91

DDR3
800MHz

Nvidia N12P
83.84,85,86,87

PCIe x 16
(Discrete only)

Intel CPU
Sandy Bridge
FSB: 1066 MHz
4,5,6,7,8,9,10,11,12,13

DDRIII 1066/1333 Channel A
DDRIII 1066/1333 Channel B

DDRIII Slot 0 1066/1333 14
DDRIII Slot 1 1066/1333 15

Discreet/UMA/PX Co-lay

FDIx4x2
(UMA only)

DMIx4

HDMI 51
LCD 49
CRT 50

HDMI
LVDS(Dual Channel)
RGB CRT

Level shifter 57

Intel
PCH
Cougar Point

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1

17,18,19,20,21,22,23,24,25,26

PCIE x 1
USB x 2
USB3.0
uPD720200
75

PCIE x 1
USB x 1
Mini-Card
802.11a/b/g
65

PCIE x 1
1000 NIC
BCM57780A1
31

RJ45 CONN 59

SD/MMC+/MS/
MS Pro/xD

PCIE x 1,USB x 1
Mini-Card
WWAN 66

SIM 66

USB 2.0 x 1
Right Side:
USB x 1

Left Side:
USB x 1

Bluetooth 63

CAMERA 49

64

USB2.0 x 4

AZALIA

Azalia
CODEC
ALC271X
29

Internal Analog MIC
HP1
MIC IN
2CH SPEAKER

SPI

Flash ROM
4MB 60

LPC Bus

LPC debug port 71

SATA x 2

HDD 56

ODD 56

KBC
NUVOTON
NPCE795P
27

SMBus

Touch PAD 69

Int. KB 69

Thermal
ENE P2800
ENE P2793
68

Fan 28

SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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SSID = CPU

CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

JE40 delete eDP function

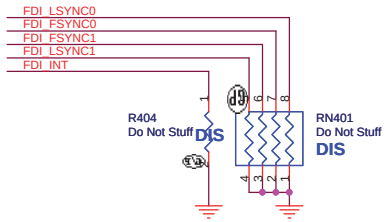
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Stuff to disable internal graphics function for power saving.



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Title: CPU (PCIE/DMI/FDI)

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SSID = CPU

CPU1B
SANDY

2 0F 9

SANDY

MISC
- SNB_IVB#
- SKTOCC#

THERMAL
- CATERR#
- PECI
- PROCHOT#
- THERMTRIP#

PWR MANAGEMENT
- PM_SYNC
- UNCOREPWRGOOD
- SM_DRAMPWROK
- RESET#

CLOCKS
- BCLK / BCLK#
- DPLL_REF_SSCLK / DPLL_REF_SSCLK#

DDR3 MISC
- SM_DRAMRST#
- SM_RCOMP0 / SM_RCOMP1 / SM_RCOMP2

JTAG & BPM
- PRDY# / PREQ#
- TCK / TMS / TRST#
- TDI / TDO
- DBR#
- BPM#0 / BPM#1 / BPM#2 / BPM#3 / BPM#4 / BPM#5 / BPM#6 / BPM#7

1D05V_VTT
R501 62R2J-GP
C502 SC47P50V2JN-3GP
H_PROCHOT#

CRB : 47pf
CEKLT:43pf

Connect EC to PROCHOT# through inverting OD buffer.

18 H_SNB_IVB# — C26 — SNB_IVB#
JE40 modify — AN34 — SKTOCC#
JE40 modify — AL33 — CATERR#
22,27 H_PECI — AN33 — PECI
27,42 H_PROCHOT# — R513 56R2J-4-GP — H_PROCHOT# R — AL32 — PROCHOT#
22,36 H_THERMTRIP# — AN32 — THERMTRIP#

19 H_PM_SYNC — AM34 — PM_SYNC
R503 10KR2J-3-GP
22,36,97 H_CPUPWRGD — AP33 — UNCOREPWRGOOD
19,37 PM_DRAM_PWRGD — R505 DX Do Not Stuff — V8 — SM_DRAMPWROK
37 VDDPWRGOOD
BUF_CPU_RST# — AR33 — RESET#

BCLK / BCLK# — A28 / A27 — CLK_EXP_P 20 / CLK_EXP_N 20
DPLL_REF_SSCLK / DPLL_REF_SSCLK# — A16 / A15 — CLK_DP_P_R / CLK_DP_N_R
RN502 Do Not Stuff
JE40 modify
1D05V_VTT

SM_DRAMRST# — R8 — R502 4K99R2F-L-GP — SM_DRAMRST# 37

SM_RCOMP0 — AK1 — SM_RCOMP_0 R506 140R2F-GP
SM_RCOMP1 — A5 — SM_RCOMP_1 R507 25D5R2F-GP
SM_RCOMP2 — A4 — SM_RCOMP_2 R508 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

PRDY# — AP29
PREQ# — AP27
JE40 modify
TCK — AR26
TMS — AR27
TRST# — AP30 — XDP_TRST#
TDI — AR28
TDO — AP26 — XDP_TDO
DBR# — AL35 — XDP_DBRESET#
BPM#0 — AT28
BPM#1 — AR29
BPM#2 — AR30
BPM#3 — AT30
BPM#4 — AP32
BPM#5 — AR31
BPM#6 — AT31
BPM#7 — AR32
JE40 modify

1D05V_VTT
RN501 SRN51J-GP
XDP_TDO
XDP_TRST#

3D3V_S0
RN503 SRN1K5J-1-GP
XDP_DBRESET#
18,27,31,36,65,66,71,82,97 PLT_RST# — BUF_CPU_RST#

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

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Title: CPU (THERMAL/CLOCK/PM)
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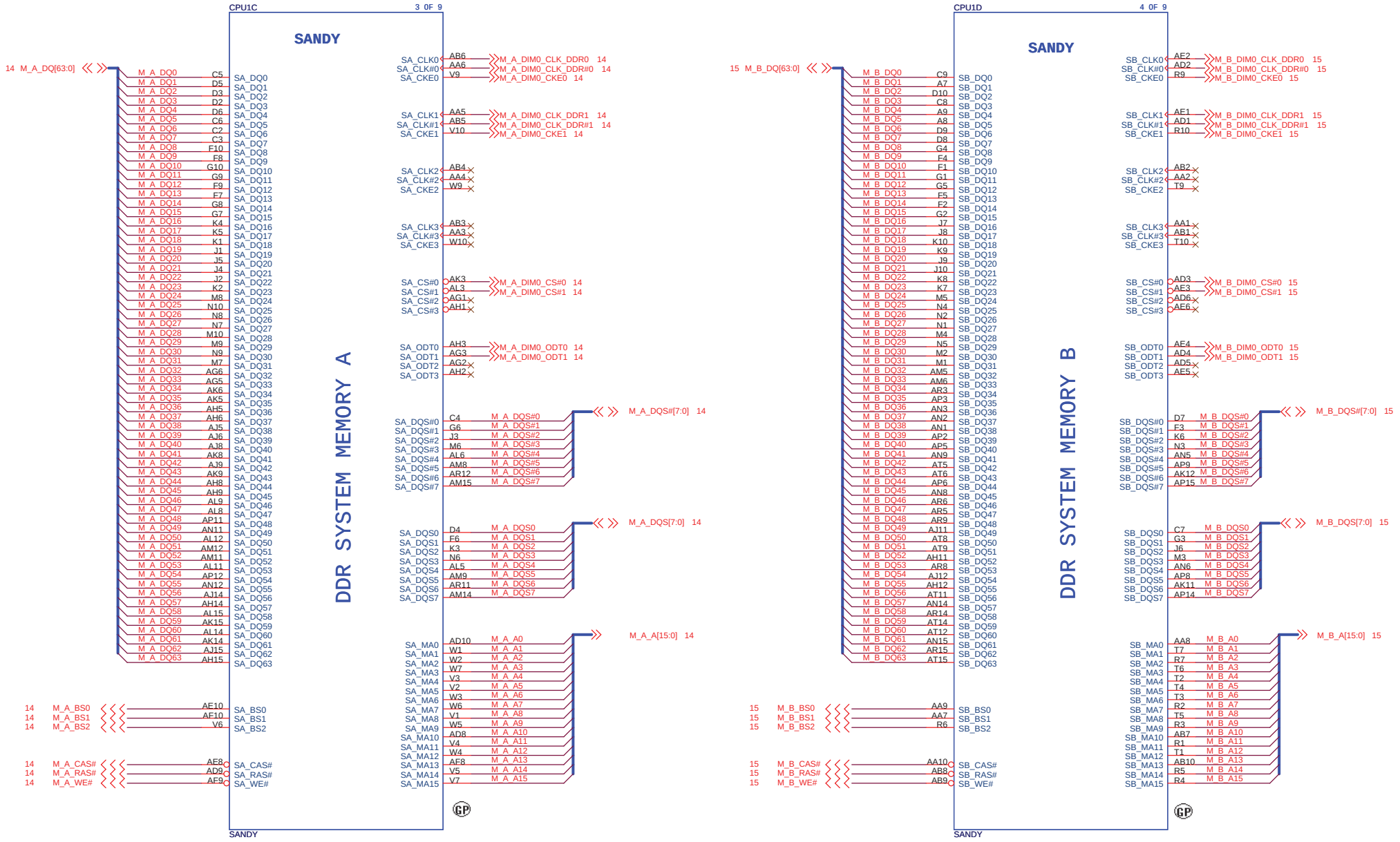
SSID = CPU



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Title: ***CPU (DDR)***

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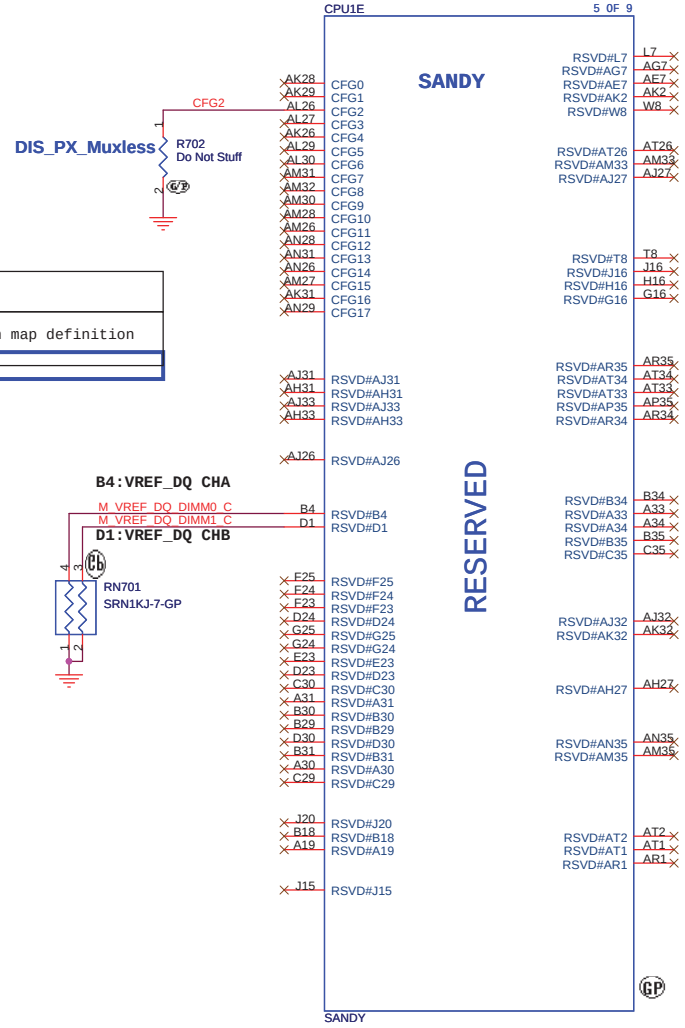
SSID = CPU



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Title	***CPU (RESERVED)***
Size A3	Document Number **JE40-HR** Rev **-1**
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SSID = CPU

PROCESSOR CORE POWER

53A

VCC_CORE

C801 Do Not Stuff, C802 Do Not Stuff, C803 Do Not Stuff, C804 Do Not Stuff, C811 Do Not Stuff

C820 Do Not Stuff, C819 Do Not Stuff, C818 Do Not Stuff, C817 Do Not Stuff, C815 Do Not Stuff

C816 SC10U6D3V5KX-1GP, C821 Do Not Stuff, C822 SC10U6D3V5KX-1GP, C823 SC10U6D3V5KX-1GP, C824 SC10U6D3V5KX-1GP, C825 SC10U6D3V5KX-1GP, C826 SC10U6D3V5KX-1GP, C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP, C836 SC10U6D3V5KX-1GP, C835 SC10U6D3V5KX-1GP, C834 SC10U6D3V5KX-1GP, C833 SC10U6D3V5KX-1GP, C832 Do Not Stuff, C831 Do Not Stuff, C828 SC10U6D3V5KX-1GP

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

POWER

CPU1F — SANDY — 6 OF 9

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

SANDY

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 F14 F12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

C805 SC10U6D3V5KX-1GP, C806 SC10U6D3V5KX-1GP, C807 SC10U6D3V5KX-1GP, C809 SC10U6D3V5KX-1GP, C810 SC10U6D3V5KX-1GP, C838 SC10U6D3V5KX-1GP, C839 SC10U6D3V5KX-1GP, C840 SC10U6D3V5KX-1GP, C841 SC10U6D3V5KX-1GP

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

C812 SC10U6D3V5KX-1GP, C813 SC10U6D3V5KX-1GP, C814 SC10U6D3V5KX-1GP, C829 SC10U6D3V5KX-1GP, C830 SC10U6D3V5KX-1GP, C842 Do Not Stuff, C843 Do Not Stuff, C844 SC10U6D3V5KX-1GP, C845 SC10U6D3V5KX-1GP

VIDALERT# AJ29 — H_CPU_SVIDALRT# — R803 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK AJ30 — H_CPU_SVIDCLK 42
VIDSOUT AJ28 — H_CPU_SVIDDAT 42

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT

H_CPU_SVIDDAT — R804 130R2F-1-GP

VCC_CORE

R801,R802 close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 — VCCSENSE 42
VSS_SENSE AJ34 — VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 — VCCIO_SENSE 45
VSSIO_SENSE A10 — VSSIO_SENSE 45

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Title: **CPU (VCC_CORE)**

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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

CPU1G — SANDY — 7 OF 9

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 Do Not Stuff (DY) UMA_PX_Muxless
C902 SC10U6D3V5KX-1GP
C903 SC10U6D3V5KX-1GP
C904 SC10U6D3V5KX-1GP
C905 SC10U6D3V5KX-1GP
C906 Do Not Stuff (DY) UMA_PX_Muxless
C907 Do Not Stuff (DY) UMA_PX_Muxless
C908 SC10U6D3V5KX-1GP
C918 Do Not Stuff (DY) UMA_PX_Muxless
C919 SC10U6D3V5KX-1GP
C920 SC10U6D3V5KX-1GP
C921 SC10U6D3V5KX-1GP

VAXG: AT24 AT23 AT21 AT20 AT18 AT17 AP24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

VCC_GFXCORE

R903 Do Not Stuff (DIS)
R904 Do Not Stuff (DIS)
R905 Do Not Stuff (DIS)
R901 Do Not Stuff (DIS)

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

SENSE LINES

VAXG_SENSE AK35 → VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 → VSS_AXG_SENSE 42

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF AL1 → +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_S0

PROCESSOR VDDQ: 10A

VDDQ: AE7 AE4 AE1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 Do Not Stuff (DY)
C910 SC10U6D3V5KX-1GP
C911 SC10U6D3V5KX-1GP
C912 SC10U6D3V5KX-1GP
C913 SC10U6D3V5KX-1GP
C914 Do Not Stuff (DY)

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

VCCSA: M27 M26 L26 J26 J25 J24 H26 H25

C916 Do Not Stuff (DY)
C915 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

VCCPLL: B6 A6 A2

C922 SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

MISC

VCCSA_SENSE H23 → VCCUSA_SENSE
R902 10R2J-2-GP
R902 need be close to pin H23.
TP901 Do Not Stuff

FC_C22 C22
VCCSA_VID1 C24
H_FC_C22
VCCSA_SEL 48

RN901 SRN1KJ-7-GP

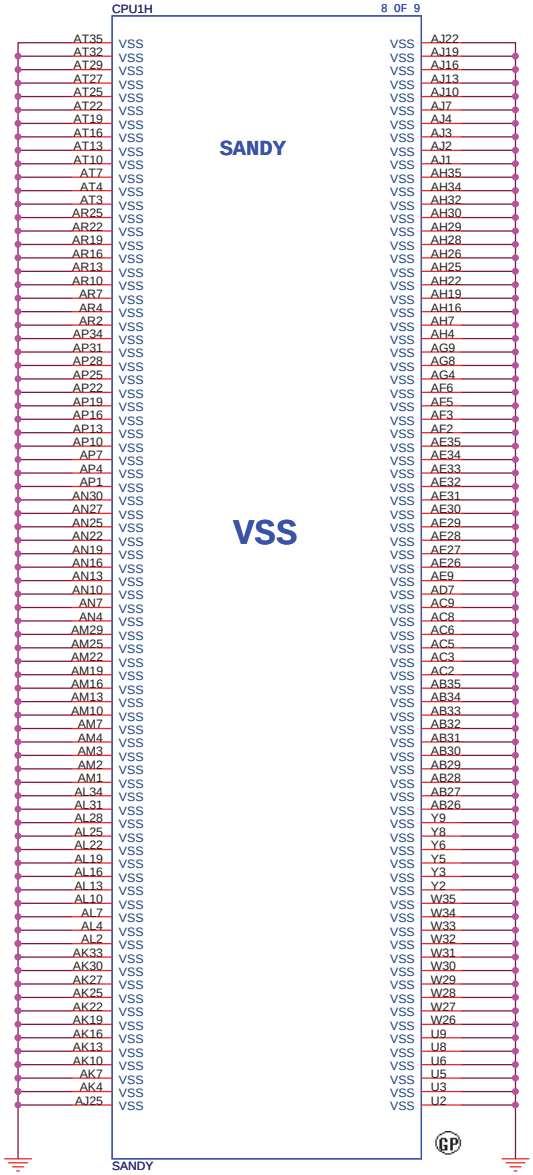
SANDY

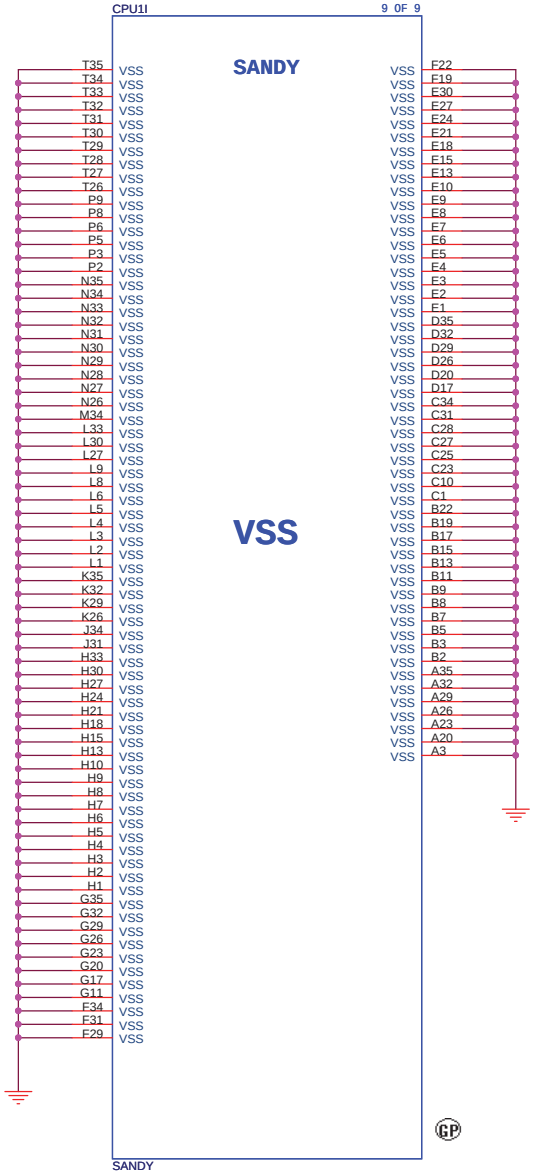
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 9 of 102

SSID = CPU





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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 10 of 102

JE40 delete XDP function

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Title: ***XDP***

Size: A3 | Document Number: **JE40-HR** | Rev: **-1**

Date: Thursday, December 02, 2010 | Sheet 11 of 102

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Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 12 of 102

(Blanking)

HR UMA

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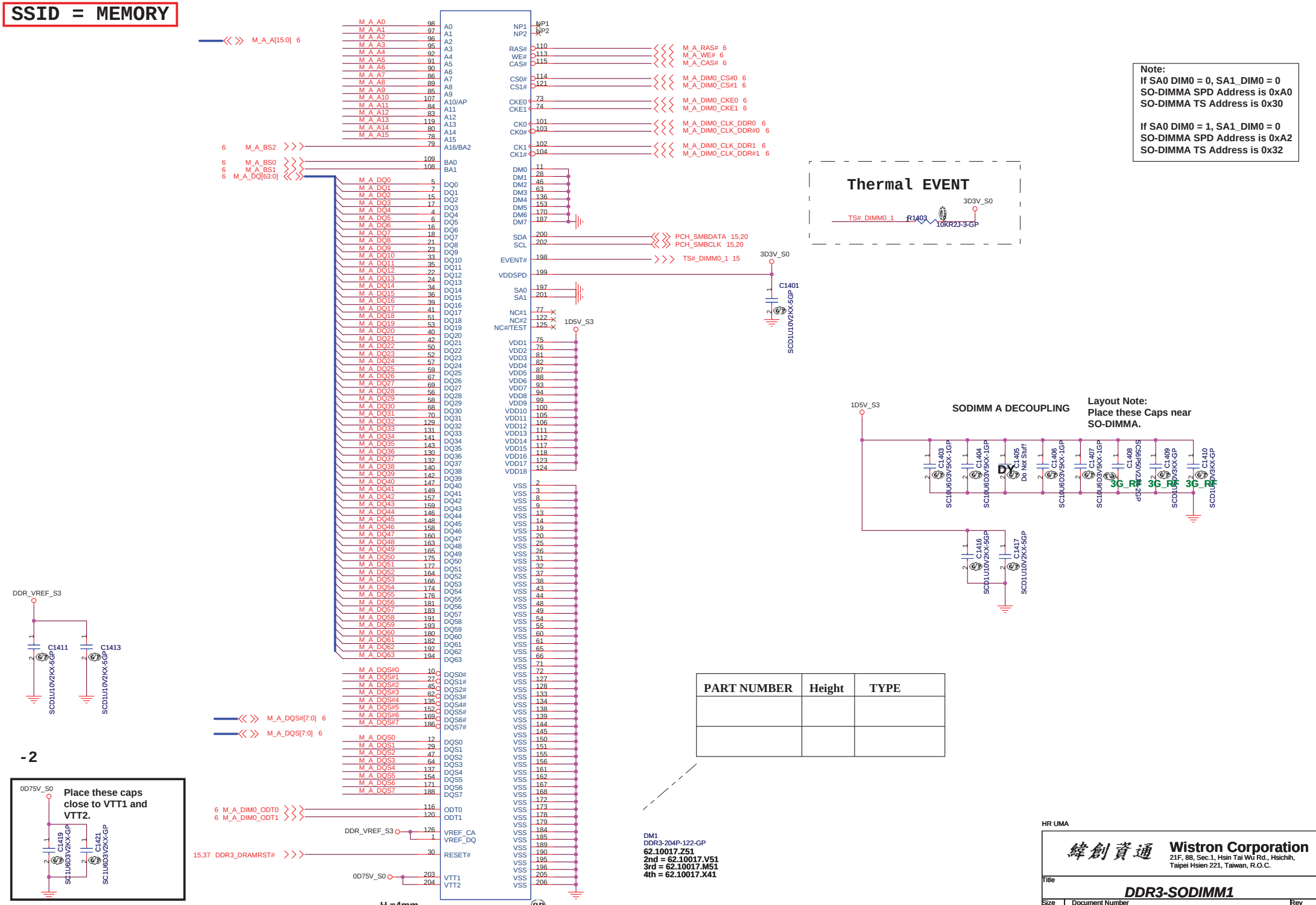
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 13 of 102

SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

SODIMM A DECOUPLING

Layout Note:
Place these Caps near
SO-DIMMA.

DDR_VREF_S3

-2

0D75V_S0

Place these caps close to VTT1 and VTT2.

PART NUMBER	Height	TYPE

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
Custom	JE40-HR	-1

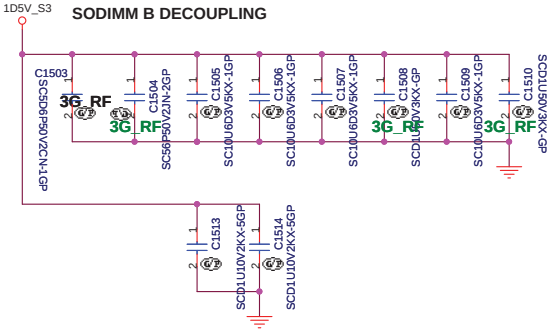
Date: Thursday, December 02, 2010 Sheet 14 of 102

SSID = MEMORY

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

SODIMM B DECOUPLING



Layout Note:
Place these Caps near SO-DIMMB.

DDR_VREF_S3
C1515 SCD1U10V2KX-5GP
C1517 SCD1U10V2KX-5GP

-2

Place these caps close to VTT1 and VTT2.

0D75V_S0
C1519 SC1U6D3V2KX-GP
C1521 SC1U6D3V2KX-GP

DM2
DDR3-204P-126-GP
62.10024.D41

2nd = 62.10017.R91
3rd = 62.10017.V61
4th = 62.10017.X51

H = 8mm

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
Custom	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 15 of 102

(Blanking)

HR UMA

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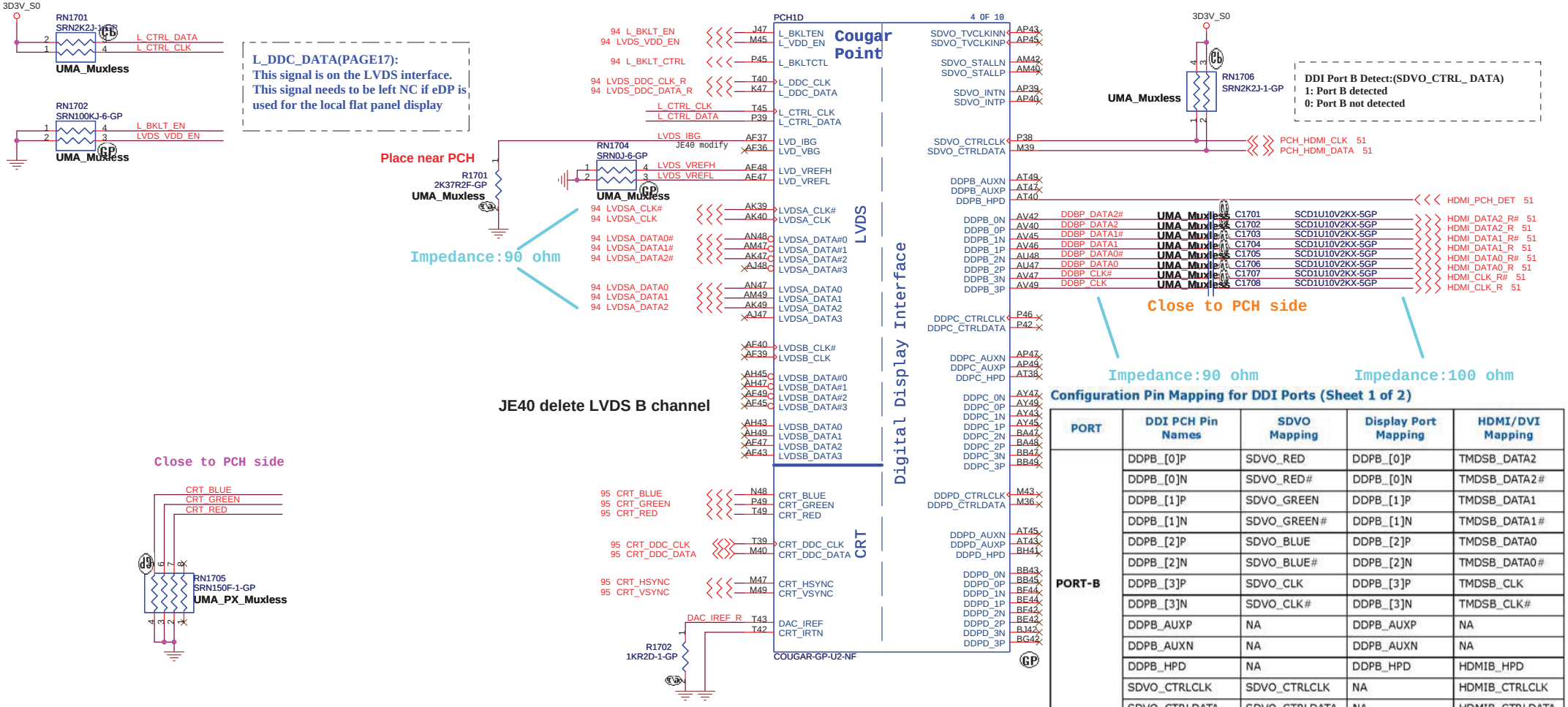
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 16 of 102



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 17 of 102

SSID = PCH

RN1801
SRN8K2J-2-GP-U

INT_PIRQH#	1	10	3D3V_S0
INT_PIRQB#	2	9	INT_PIRQD#
INT_PIRQF#	3	8	INT_PIRQE#
INT_PIRQA#	4	7	INT_PIRQC#
3D3V_S0	5	6	USB30_SMI#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

PCH1E — 5 OF 10

Cougar Point

RSVD | NVRAM | PCI | USB

TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20
TP21 TP22 TP23 TP24
TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38 TP39 TP40

RSVD: AY7 AV7 AU3 BG4 AT10 BC8 AU2 AT4 AT3 AT1 AY3 AT5 AV3 AV1 BB1 BA3 BB5 BB3 BB7 BE8 BD4 BF6 AV5 AY1 AV10 AT8 AY5 BA2 AT12 BF3

DF_TVS — NV_CLE

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USBP0N/P C24/A24 — USB_PN0 66 / USB_PP0 66
USBP1N/P C25/B25 — USB_PN1 61 / USB_PP1 61
USBP2N/P C26/A26 — JE40 delete FP function
USBP3N/P K28/H28 — USB_PN3 63 / USB_PP3 63
USBP4N/P E28/D28 — USB_PN4 66 / USB_PP4 66
USBP5N/P C28/A28 — USB_PN5 32 / USB_PP5 32

SB add USB port 5

USBP6N/P C29/B29
USBP7N/P N28/M28
USBP8N/P L30/K30 — USB_PN8 82 / USB_PP8 82
USBP9N/P G30/E30 — USB_PN9 61 / USB_PP9 61

JE40 co-lay USB2.0

USBP10N/P C30/A30 — JE40 delete eDP function
USBP11N/P L32/K32 — USB_PN11 65 / USB_PP11 65
USBP12N/P G32/E32 — USB_PN12 49 / USB_PP12 49
USBP13N/P C32/A32 — JE40 delete New Card function

USBRBIAS# C33 — USB_RBIAS — R1811 22D6R2F-L1-GP
USBRBIAS B33

OC0#/GPIO59 A14
OC1#/GPIO40 K20
OC2#/GPIO41 B17
OC3#/GPIO42 C16
OC4#/GPIO43 L16
OC5#/GPIO9 A16
OC6#/GPIO10 D14
OC7#/GPIO14 C14

3D3V_S5 — R1820 10KR2J-3-GP

INT_PIRQA# K40 — PIRQA#
INT_PIRQB# K38 — PIRQB#
INT_PIRQC# H38 — PIRQC#
INT_PIRQD# G38 — PIRQD#

83 DGPU_HOLD_RST# — DGPU_SELECT# C46 — REQ1#/GPIO50
93 DGPU_PWR_EN# — C44 — REQ2#/GPIO52
E40 — REQ3#/GPIO54

Do Not Stuff TP1806 — DGPU_PWM_SELECT# D47 — GNT1#/GPIO51
Do Not Stuff TP1804 — E42 — GNT2#/GPIO53
F46 — GNT3#/GPIO55

R1813 Do Not Stuff
56 SATA_ODD_DA# — INT_PIRQE# G42 — PIRQE#/GPIO2
82 USB30_SMI# — INT_PIRQF# G40 — PIRQF#/GPIO3
C42 — PIRQG#/GPIO4
INT_PIRQH# D44 — PIRQH#/GPIO5

JE40 modify 07/16

PME# K10
5,27,31,36,65,66,71,82,97 PLT_RST# — C6 — PLTRST#

71 CLK_PCI_LPC — R1804 22R2J-2-GP — CLK_PCI_LPC_R H49 — CLKOUT_PCI0
20 CLK_PCI_FB — R1805 22R2J-2-GP — CLK_PCI_FB_R H43 — CLKOUT_PCI1
27 CLK_PCI_KBC — R1806 22R2J-2-GP — CLK_PCI_KBC_R J48 — CLKOUT_PCI2
K42 — CLKOUT_PCI3
H40 — CLKOUT_PCI4

EC1803 EC1802 EC1801 — DY Do Not Stuff

KBC CLK EMI

COUGAR-GP-U2-NF

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

RN1803
SRN10KJ-5-GP

DGPU_HOLD_RST# — DGPU_PWR_EN#

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

check R1808 R1809 阻值

CRB : 2.2K
CEKLT: 1K

1D8V_S0 — R1808 2K2R2J-2-GP — NV_CLE — R1809 1KR2J-1-GP — H_SNB_IVB# 5

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

HR UMA

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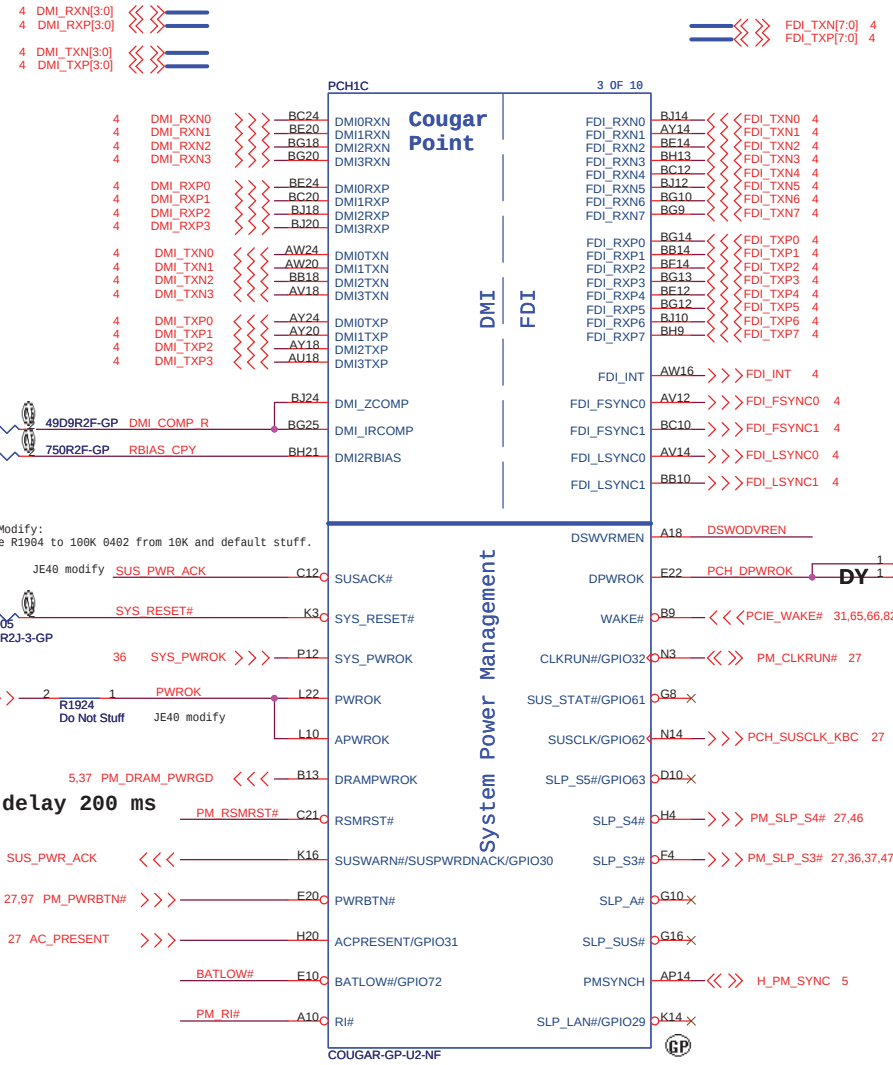
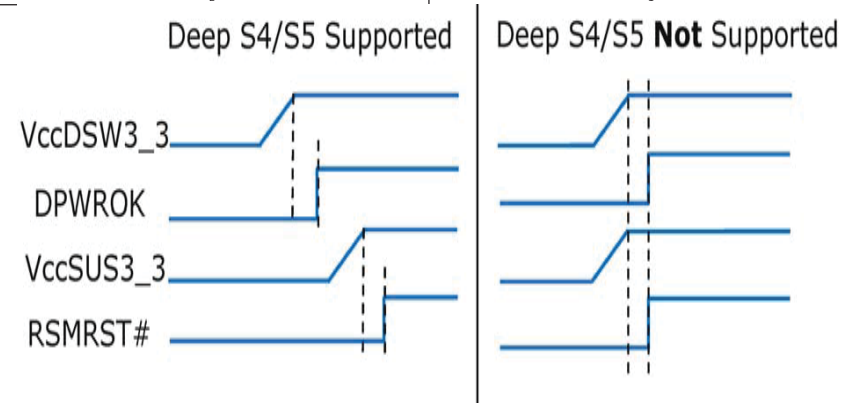
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 18 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.





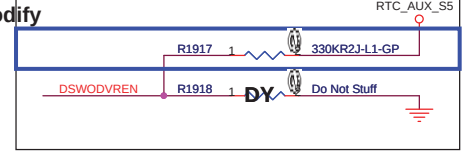
For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

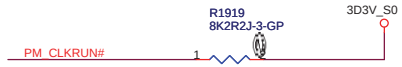
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

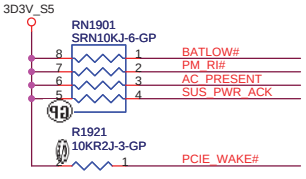
JE40 modify 07/16

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify

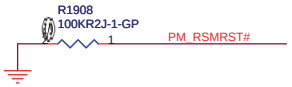




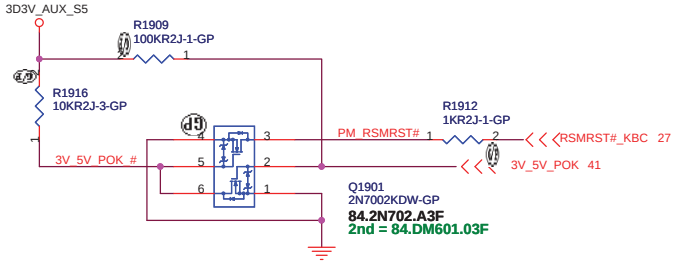


PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor



PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 19 of 102

SSID = PCH

PCH1B — Cougar Point — 2 OF 10

PCI-E*: W-WAN, WLAN, Card Reader, LAN, USB3.0, Intel GBE LAN, Dock, NEW CARD

SMBUS: SMBALERT#/GPIO11, SMBCLK, SMBDATA, SML0ALERT#/GPIO60, SML0CLK, SML0DATA, SML1ALERT#/PCHHOT#/GPIO74, SML1CLK/GPIO58, SML1DATA/GPIO75

Controller Link: CL_CLK1, CL_DATA1, CL_RST1#

CLOCKS: CLKOUT_PCIE0N/P, PCIECLKRQ0#/GPIO73, CLKOUT_PCIE1N/P, PCIECLKRQ1#/GPIO18, CLKOUT_PCIE2N/P, PCIECLKRQ2#/GPIO20, CLKOUT_PCIE3N/P, PCIECLKRQ3#/GPIO25, CLKOUT_PCIE4N/P, PCIECLKRQ4#/GPIO26, CLKOUT_PCIE5N/P, PCIECLKRQ5#/GPIO44, CLKOUT_PEG_B_N/P, PEG_B_CLKRQ#/GPIO56, CLKOUT_PCIE6N/P, PCIECLKRQ6#/GPIO45, CLKOUT_PCIE7N/P, PCIECLKRQ7#/GPIO46, CLKOUT_ITPXDP_N/P

FLEX CLOCKS: CLKOUTFLEX0/GPIO64, CLKOUTFLEX1/GPIO65, CLKOUTFLEX2/GPIO66, CLKOUTFLEX3/GPIO67

COUGAR-GP-U2-NF

JE40 delete New Card function

JE40 delete XDP function

JE40 modify

For DIS_PX mode or MXM mode.

SB

CRB : 1K
CEKLT: 10K

R2008 and C2008 CO-LAY

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

WWAN CLK

WLAN CLK

LAN CLK

USB3.0 CLK

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

need very close to PCH

RTS

– Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
– Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2
if more than 2 PCI clocks are required.

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 20 of 102

SSID = PCH

RTC_X1
RTC_X2
R2101 10MR2J-L-GP
X2101
X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
C2101
C2102 SC5P50V2CN-2GP

SB SEIKO suggest modify to 5P
EPSON suggest modifyg to 6P

RTC_AUX_S5
RN2104 SRN20KJ-GP-U
C2103 SC1U6D3V2KX-GP
C2104 SC1U6D3V2KX-GP
G2101 Do Not Stuff

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

R2104 1M1R2J-GP
R2105 330KR2F-L-GP

RTC Reset

-1M
R2122 33R2J-2-GP DY
R2123 33R2J-2-GP
29 HDA_CODEC_SYNC
29 HDA_CODEC_SDOUT
HDA_SYNC
HDA_SDOUT
29 HDA_CODEC_RST#
29 HDA_CODEC_BITCLK
HDA_RST#
HDA_BITCLK
RN2102 SRN33J-5-GP-U

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO
R2102 DY Do Not Stuff
HDA_SDOUT

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

+3VS_+1.5VS_HDA_IO
R2103 1KR2J-1-GP
HDA_SYNC

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

5V_S0
-1M
Q2101 Do Not Stuff
Do Not Stuff
2ND = 84.2N702.031
HDA_CODEC_SYNC
HDA_SYNC_R
-1M
R2124 Do Not Stuff
HDA_SYNC

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

PCH1A 1 OF 10
Cougar Point
COUGAR-GP-U2-NF

RTC: RTCX1 A20, RTCX2 C20, RTCRST# D20, SRTCRST# G22, INTRUDER# K22, INTVRMEN C17
IHDA: HDA_BCLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN#/GPIO33 C36, HDA_DOCK_RST#/GPIO13 N32
JTAG: JTAG_TCK J3, JTAG_TMS H7, JTAG_TDI K5, JTAG_TDO H1
SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3
LPC: FWH0/LAD0 C38, FWH1/LAD1 A38, FWH2/LAD2 B37, FWH3/LAD3 C37, FWH4/LFRAME# D36, LDRQ0# E36, LDRQ1#/GPIO23 K36, SERIRQ V5
SATA: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5, SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10, SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4, SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1, SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1, SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO Y11, SATAICOMPI Y10, SATA3RCOMPO AB12, SATA3COMPI AB13, SATA3RBIAS AH1, SATALED# P3, SATA0GP/GPIO21 V14, SATA1GP/GPIO19 P1

HDD1
HDD2
ODD
ESATA

27 ME_UNLOCK
R2107 1KR2J-1-GP
?????

R2121 4K7R2J-2-GP
JE40 modify
R2108 33R2J-2-GP
R2109 33R2J-2-GP
R2110 33R2J-2-GP
27,60 SPI_CLK_R
27,60 SPI_CS0#_R
27,60 SPI_SI_R
27,60 SPI_SO_R
PCH_SPI_CLK
PCH_SPI_CS0#
PCH_SPI_SI

HDA_CODEC_BITCLK
HDA_CODEC_SDOUT
SPI_CS0#_R
EC2102 DY Do Not Stuff
EC2103 DY Do Not Stuff
EC2101 DY Do Not Stuff

LPC_AD[0..3] 27,71
LPC_FRAME# 27,71
INT_SERIRQ 27
SATA_RXN0 56
SATA_RXP0 56
SATA_TXN0 56
SATA_TXP0 56
SATA_RXN4 56
SATA_RXP4 56
SATA_TXN4 56
SATA_TXP4 56
SATA_COMP R2112 37D4R2F-GP 1D05V_VTT
SATA3_COMP R2113 49D9R2F-GP 1D05V_VTT
RBIAS_SATA3 R2114 750R2F-GP
SATA_LED# 68
SATA_DET#0

22 PSW_CLR#
RN2103 SRN10KJ-6-GP 3D3V_S0
SATA_LED#
INT_SERIRQ
SATA_DET#0

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 21 of 102

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_RCIN# — H_A20GATE

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

3D3V_S0 — R2220 10KR2J-3-GP — FFS_INT2_R

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

Pass Word Clear

GFX_CRB_DET — R2206 100KR2J-1-GP

3D3V_S0 — RN2201 SRN10KJ-6-GP — EC_SMI# / DGPU_HPD_INTR# / EC_SCI#

RN2202 SRN10KJ-6-GP — MFG_MODE / FP_DET# / S_GPIO / PCH_TEMP_ALERT#

3D3V_S5 — RN2204 SRN10KJ-6-GP — USB3_PWR_ON / PCH_GPIO12 / PCH_GPIO24

PCH_GPIO15 — R2201 1KR2J-1-GP

JE40 delete G Sensor

SB VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

3D3V_S0 — R2218 10KR2J-3-GP — UMA_VRAM800MHZ — PCH_GPIO22 — R2219 10KR2J-3-GP — VRAM900MHZ

VRAM Size

3D3V_S0 — R2214 2G (Do Not Stuff) / R2216 1G (Do Not Stuff) — VRAM_SIZE1 / VRAM_SIZE2 — R2215 1G_512M (Do Not Stuff) / R2217 512M_2G (Do Not Stuff)

PCH1F — 6 OF 10 — Cougar Point — COUGAR-GP-U2-NF

GPIO: S_GPIO, EC_SMI#, DGPU_HPD_INTR#, EC_SCI#, ICC_EN#, PCH_GPIO12, PCH_GPIO15, SATA_ODD_PRSNT#, DGPU_PWROK, PCH_GPIO22, PCH_GPIO24, PCH_GPIO27, PLL_ODVR_EN, PSW_CLR#, FP_DET#, DMI_OVRVLTG, FDI_OVRVLTG, MFG_MODE, GFX_CRB_DET, FFS_INT2_R, PCH_TEMP_ALERT#, USB3_PWR_ON, PCH_NCTF_1, PCH_NCTF_3, PCH_NCTF_2, PCH_NCTF_4

CPU/MISC: TACH4/GPIO68, TACH5/GPIO69, TACH6/GPIO70, TACH7/GPIO71, A20GATE, PECI, RCIN#, PROCPWRGD, THRMTRIP#, INIT3_3V#, TS_VSS1–4, NC_1

NCTF: NCTF_VSS#A4 … NCTF_VSS#F49

NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49

NCTF TEST PIN: BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49

SB add Zero ODD function

SATA_ODD_PWRGT 56 — UMA_DIS# 20 — VRAM_SIZE1 — VRAM_SIZE2

H_A20GATE 27 — R2203 Do Not Stuff DY — H_PECI 5,27 — H_RCIN# 27 — H_CPUPWRGD 5,36,97 — PCH_THERMTRIP_R — R2204 54D9R2F-L1-GP — H_THERMTRIP# 5,36

RN2205 Do Not Stuff DY — SB — 1D05V_VTT

SB 公板 check different , check need modify or not check intel , R2204

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI_OVRVLTG — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI_OVRVLTG — R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

ICC_EN# — R2211 1KR2J-1-GP

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN — R2212 DY Do Not Stuff

HR UMA

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Title: **PCH (GPIO/CPU)**

Size: A3 | Document Number: **JE40-HR** | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 22 of 102

SSID = PCH 6A

PCH1G **POWER** 7 OF 10

Cougar Point

VCC CORE: CRT, LVDS, HVCMOS, DMI, NAND / SPI, FDI

VCCIO

1D05V_VTT 1.3A

(1uFx3) (10uFx1_0603)

C2301 SC10U6D3V5KX-1GP, C2302 SC1U6D3V2KX-GP, C2303 SC1U6D3V2KX-GP, C2304 SC1U6D3V2KX-GP

AA23 AC23 AD21 AD23 AE21 AE23 AG21 AG23 AG24 AG26 AG27 AG29 AJ23 AJ26 AJ27 AJ29 AJ31 VCCCORE

1D05V_VTT AN19 VCCIO

JE40 modify 07/16

JE40 modify BJ22 VCCAPLLEXP

1D05V_VTT 2.925A(Total current of VCCIO)

(1uF x4)

C2306 DY Do Not Stuff, C2307 SC1U6D3V2KX-GP, C2308 SC1U6D3V2KX-GP, C2309 SC1U6D3V2KX-GP

AN16 AN17 AN21 AN26 AN27 AP21 AP23 AP24 AP26 AT24 AN33 AN34 VCCIO

0.266A (Totally VCC3_3 current)

3D3V_S0 (0.1uF x1) C2310 SCD1U10V2KX-5GP

BH29 VCC3_3

0.159A(Totally current of VCCVRM) -2 modify power net name

VCCVRM_S0 AP16 VCCVRM

0806 check VCCAFDIPLL BG6 VCCAFDIPLL

1D05V_VTT AP17 VCCIO

0.042A (Totally current of VCCDMI) 1D05V_VTT AU20 VCCDMI JE40 modify

COUGAR-GP-U2-NF

VCCADAC U48 +VCCA_DAC_1_2 (0.1uF/0.01uF x1) (10uF x1_0603) C2313 SCD01U16V2KX-3GP, C2314 SCD01U16V2KX-5GP, C2315 DY Do Not Stuff

R2301 Do Not Stuff DIS 3D3V_S0

R2315 Do Not Stuff 3D3V_DAC_S0

UMA_PX_Muxless UMA_PX_Muxless

VSSADAC U47

VCCALVDS AK36 +3VS_VCCA_LVDS 0.001A R2304 0R3J-0-U-GP 3D3V_S0

UMA_PX_Muxless

VSSALVDS AK37 DIS R2303 Do Not Stuff

VCCTX_LVDS AM37 AM38 AP36 AP37

0.06A +1.8VS_VCCTX_LVDS R2305 0R5J-5-U-GP 1D8V_S0

UMA_PX_Muxless

R2309 Do Not Stuff DIS C2316 SCD01U16V2KX-3GP, C2317 SCD01U16V2KX-3GP, C2318 DY Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless

(0.01uF x2) (22uF x1)

VCC3_3 V33 V34

3D3V_S0 C2319 SCD1U10V2KX-5GP

-2 modify power net name

VCCVRM AT16 VCCVRM_S0

VCCDMI AT20 JE40 modify 1D05V_VTT (1uF x1) C2320 SC1U6D3V2KX-GP

VCCCLKDMI AB36

0.02A +1.05VS_VCC_DMI_CCI L2303 IND-10UH-218-GP 1D05V_VTT

68.10050.10Y 2nd = 68.10090.10B

C2321 SC1U6D3V2KX-GP, C2325 DY Do Not Stuff

(1uFx1) (10uFx1)

VccDFTERM AG16 AG17 AJ16 AJ17

1D8V_S0 0.19A JE40 modify

C2326 SCD1U10V2KX-5GP, C2322 SCD1U10V2KX-5GP

VCCSPI V1

0.02A 3D3V_S5 (1uFx1)

C2323 SC1U6D3V2KX-GP

SB 公板suggest delete 3D3V_S0, R2313

SPI only support 3D3V_S5

The same BIOS SPI ROM power

U2301 for ANNIE flicker issue

R2312 for don't flicker solution

3.3V CRT LDO

U2301 G9091-330T11U-GP 74.09091.J3F 2nd = 74.09198.G7F

5V_S0 C2311 SC1U6V2KX-1GP

VIN GND EN VOUT NC#4

3D3V_DAC_S0 C2312 SC1U6D3V2KX-GP C2327 SC1U6D3V3MX-GP

UMA_PX_Muxless UMA_PX_Muxless UMA_PX_Muxless UMA_PX_Muxless

SB add C2327

-1M add LDO for VCCVRM_S0

3D3V_S0 1D5V_S0 VCCVRM_S0

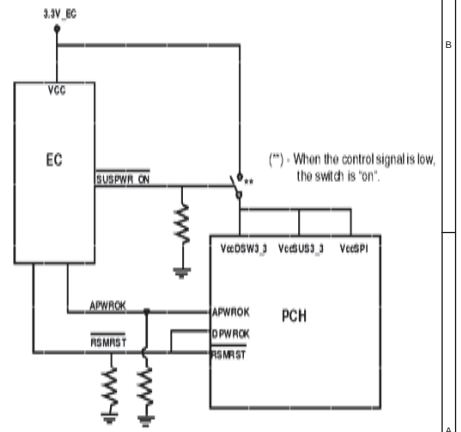
U2302 G913CF-GP 74.00913.A3F

SHDN# GND IN SET OUT

DY C2328 SC1U10V3KX-3GP, C2329 DY SC4D7U6D3V3KX-GP, C2330 DY SC22P50V2JN-4GP, R2316 DY 2K8R2F-GP, C2331 DY SCD1U10V2KX-5GP, R2317 DY 10KR2J-3-GP

Vout=1.25*(1+R1/R2)

Refer to NPCE795 shared SPI flash architecture



HR UMA

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Title: **PCH (POWER1)**

Size: A3 | Document Number: **JE40-HR** | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 23 of 102

JE40 modify 07/16

SSID = PCH

PCH1J

POWER

10 OF 10

Cougar Point

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

COUGAR-GP-U2-NF

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.16A (Totally current of VCCVRM

0.08A

0.055A

0.095A

0.001A

6uA

0.01A

-1M

-1M modify power net name

JE40 modify 07/16

http://hobi-elektronika.blogspot.com/

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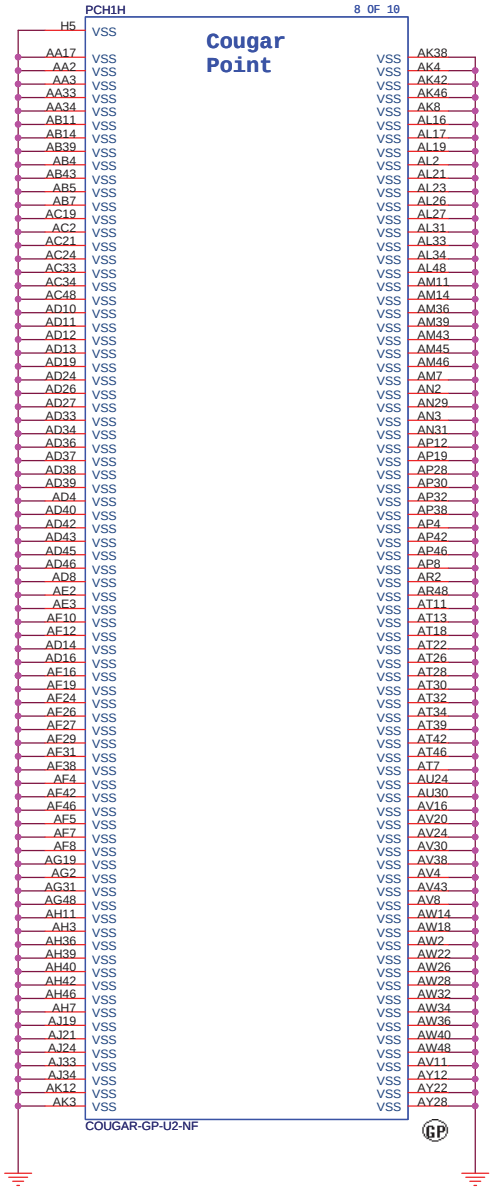
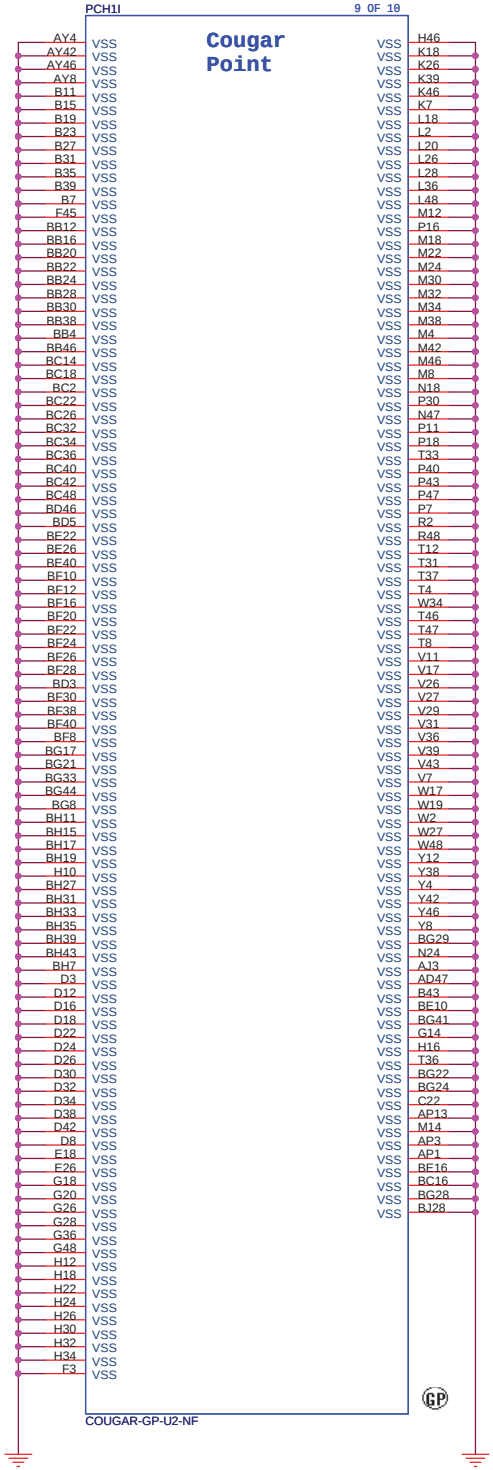
Title: PCH (POWER2)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 24 of 102

SSID = PCH





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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 25 of 102

HR UMA

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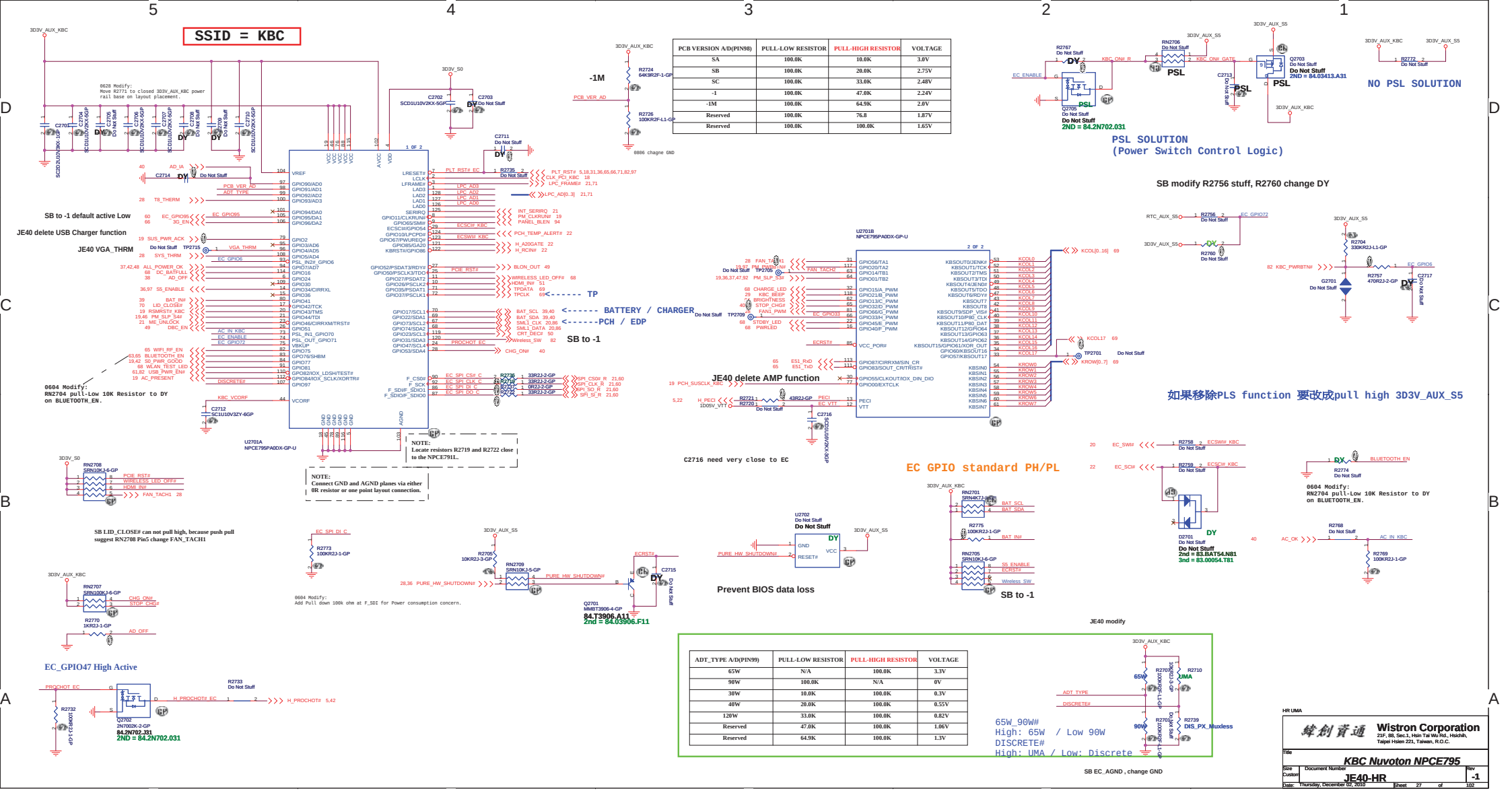
Title: ***Clock(colay)***

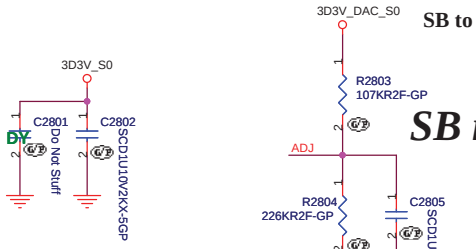
Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Thursday, December 02, 2010 Sheet 26 of 102

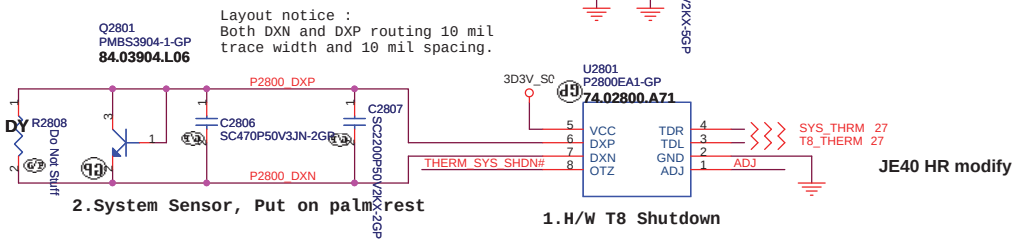


SSID = Thermal

Thermal sensor P2800



SB modify R2803,R2804 setting



JE40 HR modify

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

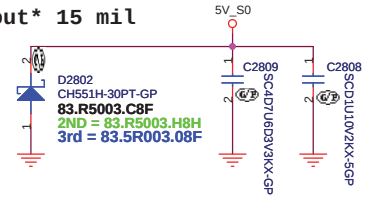
RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

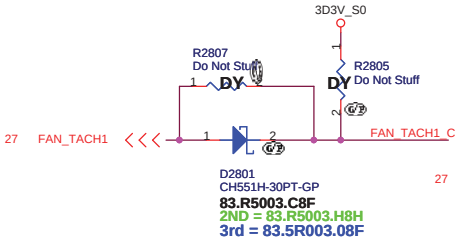
VGA Thermal sensor P2800

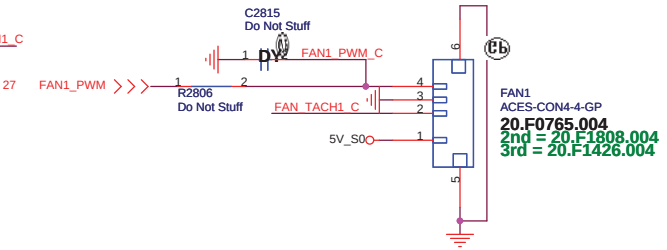
SMBUS modify to Page 84

Fan controller P2793

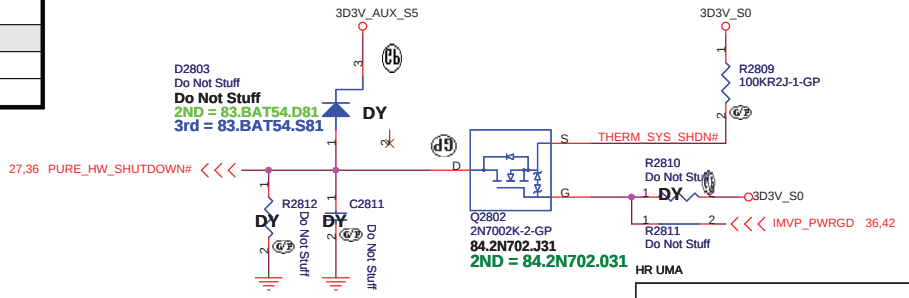
Layout 15 mil







For PWM FAN



HR UMA

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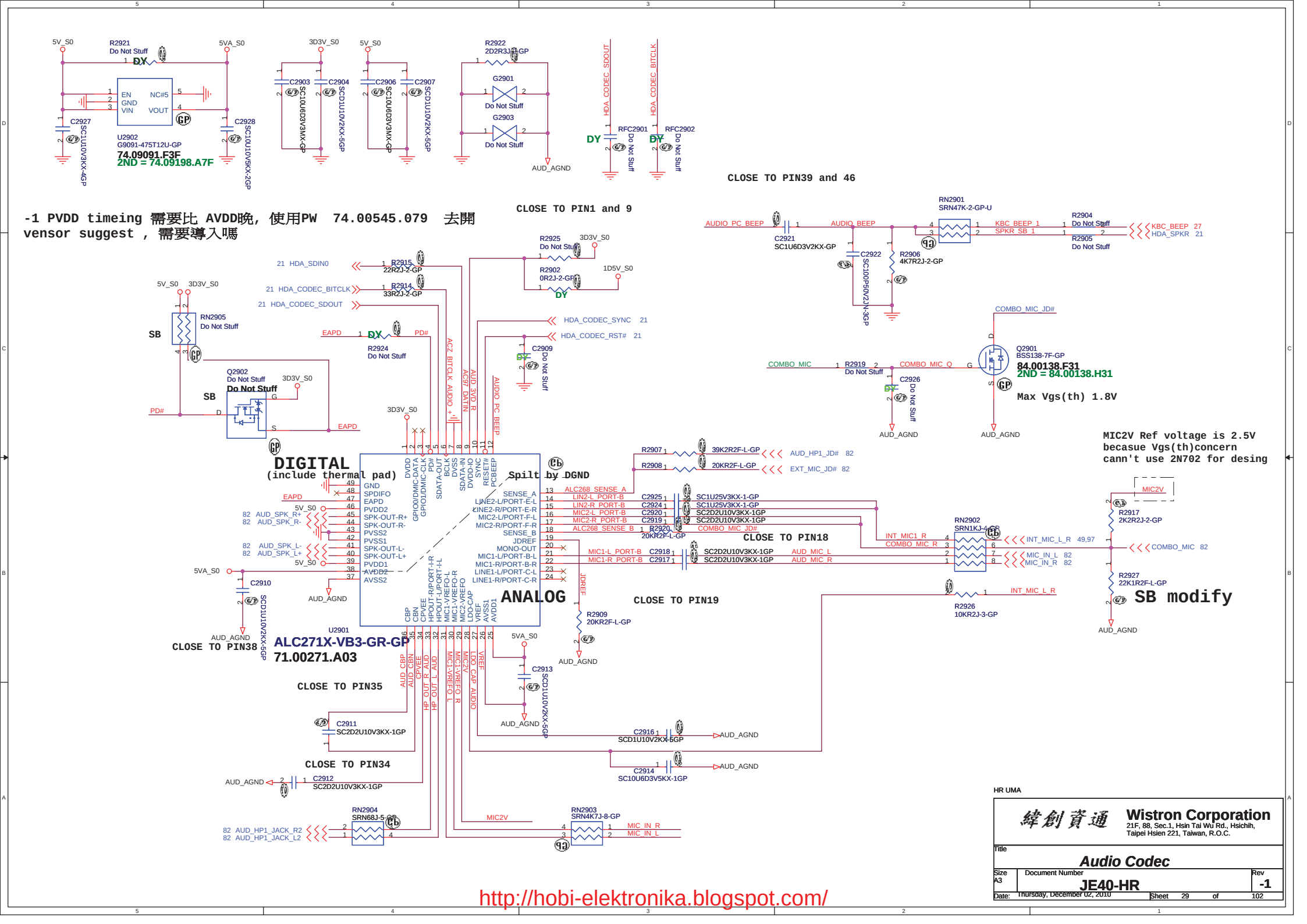
Title: Thermal P2800/Fan Controllor P2793		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 28 of 102	


-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎
CLOSE TO PIN1 and 9
CLOSE TO PIN39 and 46
CLOSE TO PIN18
CLOSE TO PIN19
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB3-GR-GP
71.00271.A03
U2901
U2902
G9091-475T12U-GP
74.09091.F3F
2ND = 74.09198.A7F
Q2901
BSS138-7F-GP
84.00138.F31
2ND = 84.00138.H31
Max Vgs(th) 1.8V
MIC2V Ref voltage is 2.5V
becasue Vgs(th)concern
cann't use 2N702 for desing
SB modify
SB
Do Not Stuff
DY
GP
HR UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec
JE40-HR
-1
Thursday, December 02, 2010
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http://hobi-elektronika.blogspot.com/

AUDIO OP AMPLIFIER

JE40 delete AMP function

HR UMA

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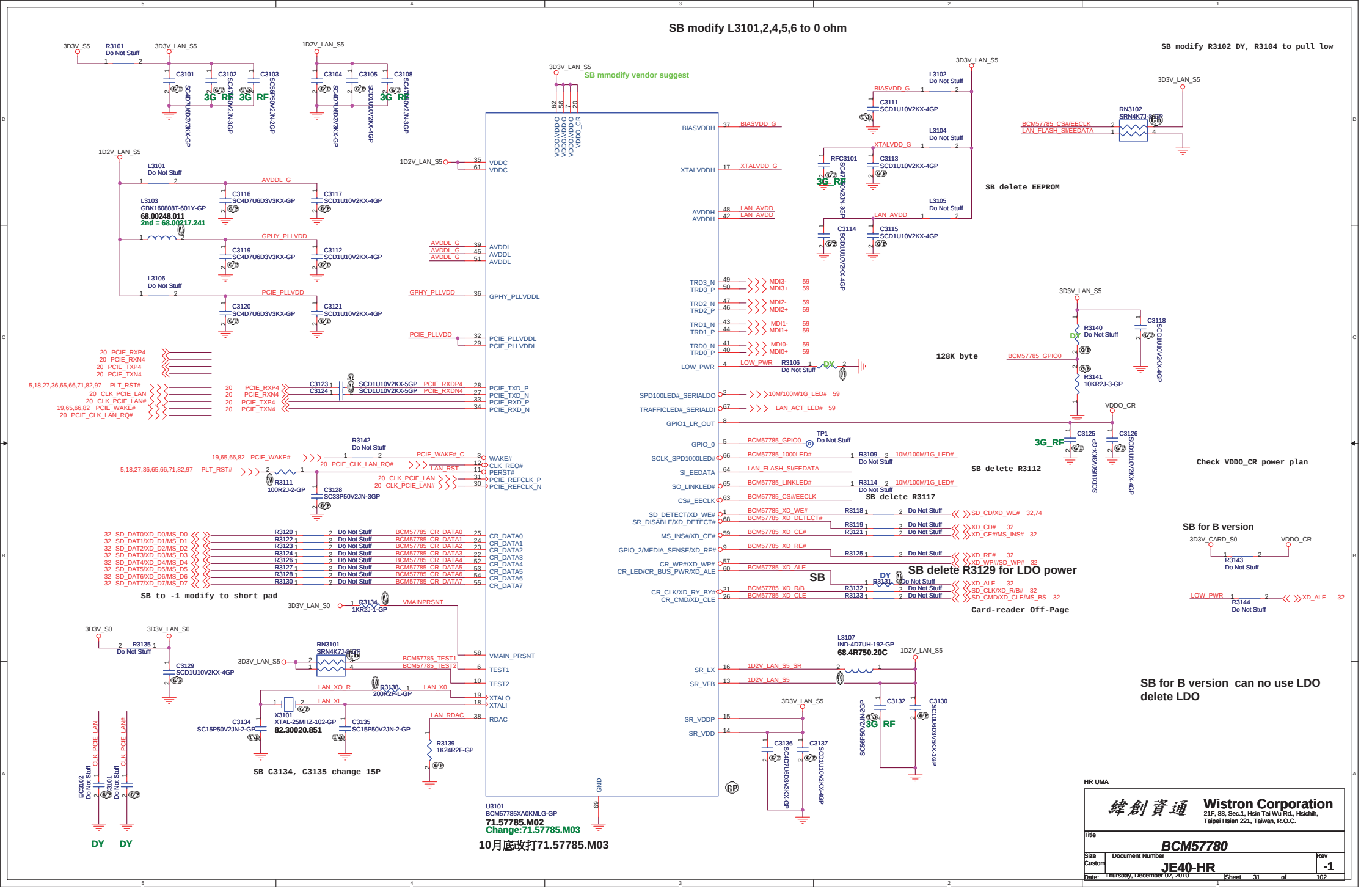
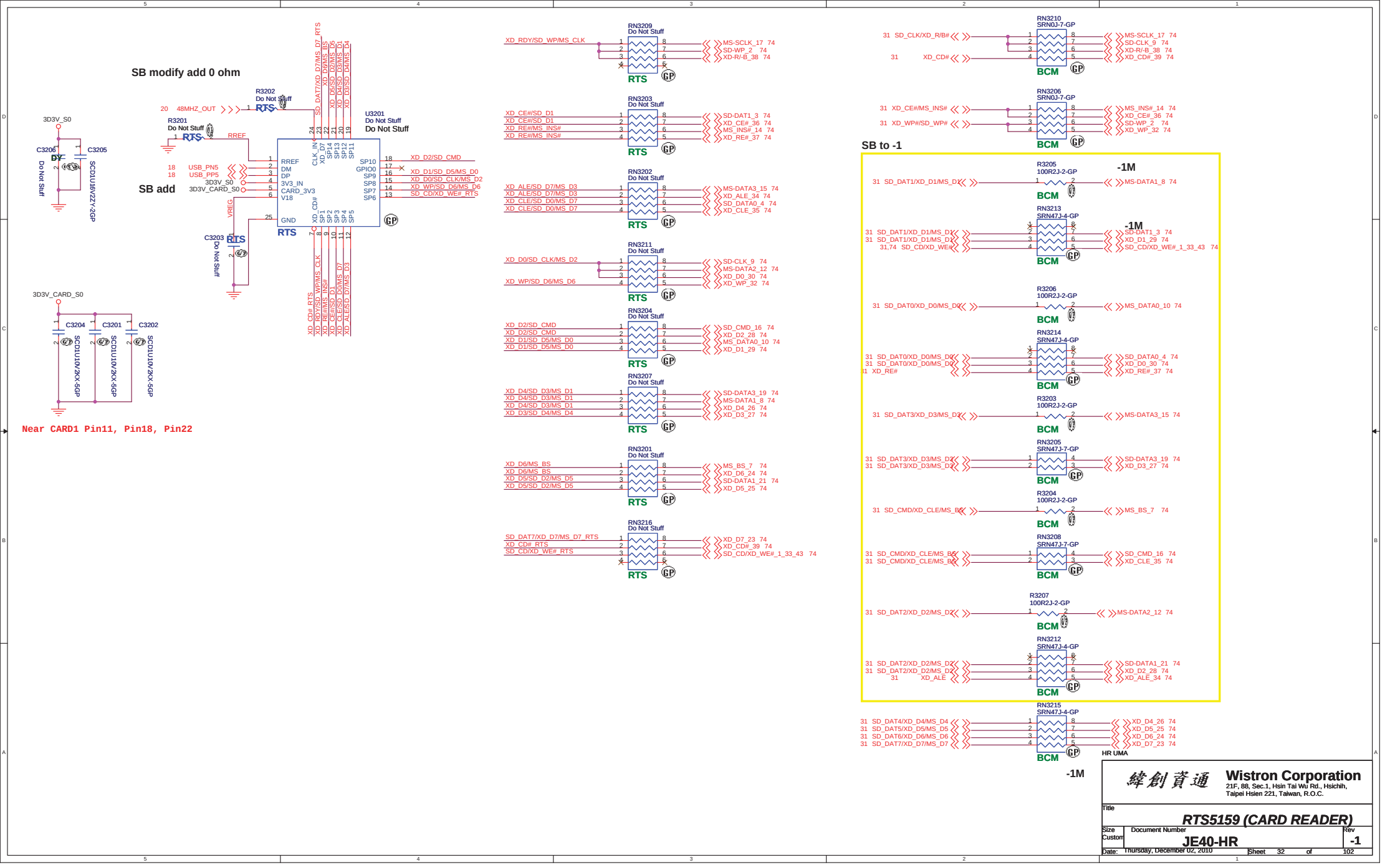
Title: ***Audio AMP***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 30 of 102	





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HR UMA

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Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 33 of 102

(Blanking)

HR UMA

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Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 34 of 102

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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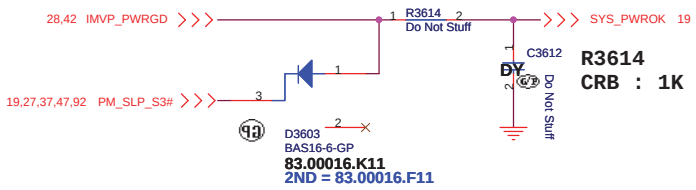
Title: ***USB 3.0 Controller***

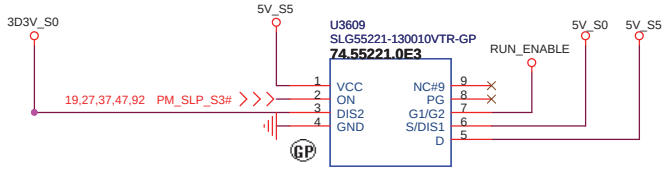
Size	Document Number	Rev
A3	**JE40-HR**	**-1**

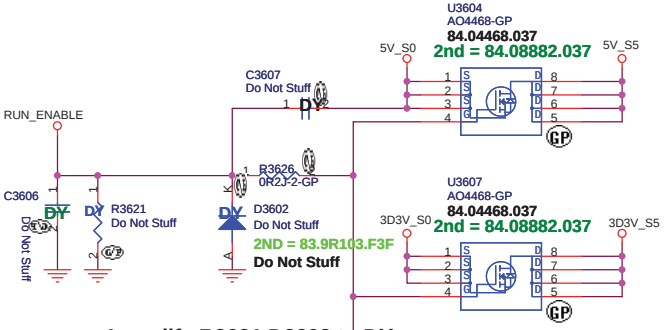
Date: Thursday, December 02, 2010 Sheet 35 of 102

Power Sequence

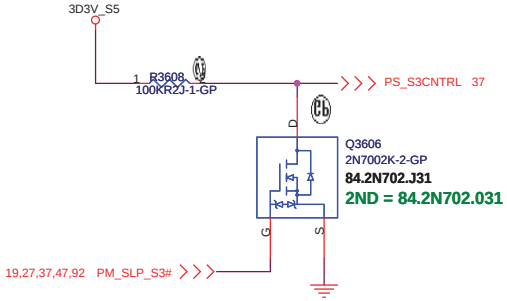


ANNIE Run Power



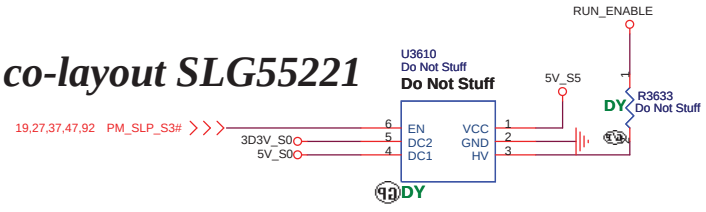


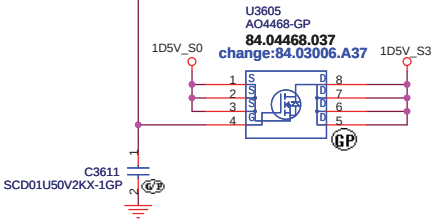
-1 modify R3621,D3602 to DY



SB modify part number

-1 co-layout SLG55221

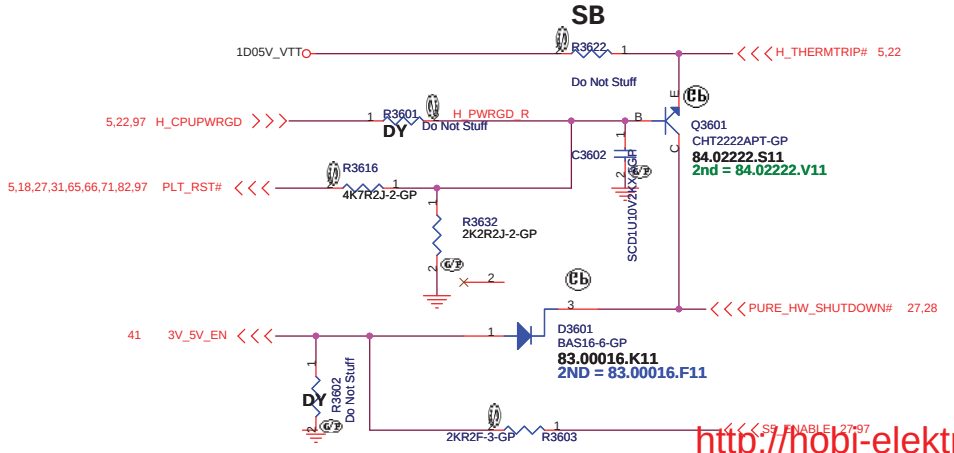




1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

SB



HR UMA

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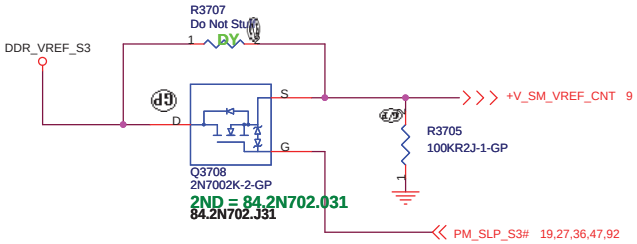
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

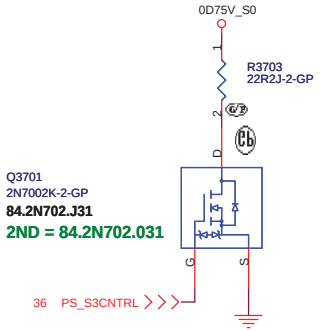
Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 36 of 102

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

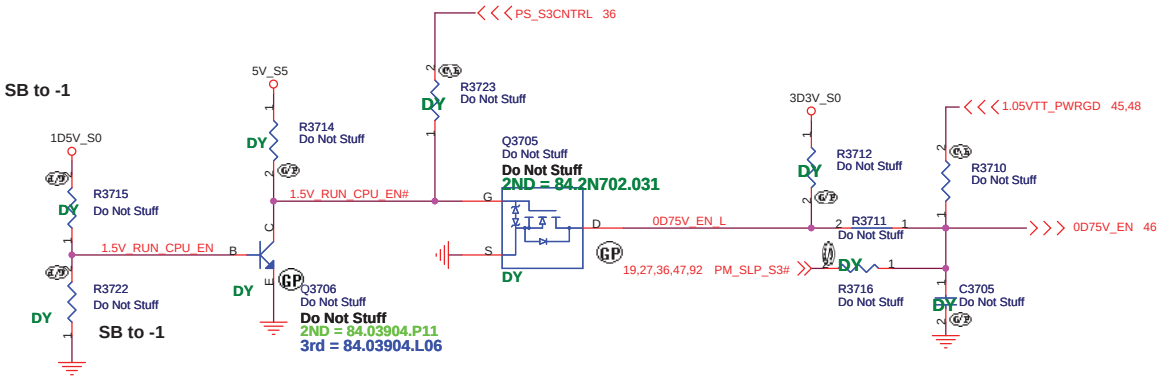


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

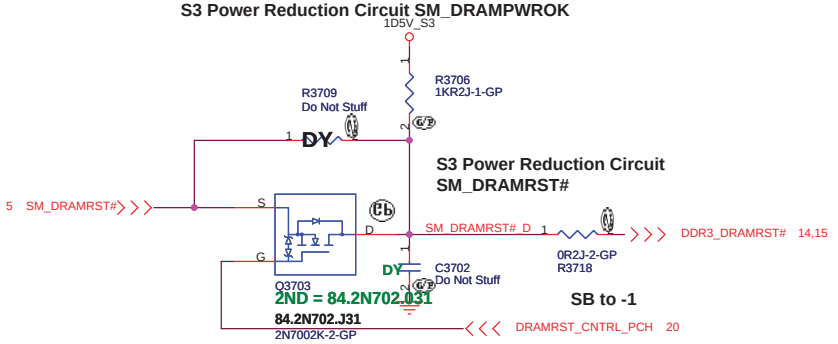


5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

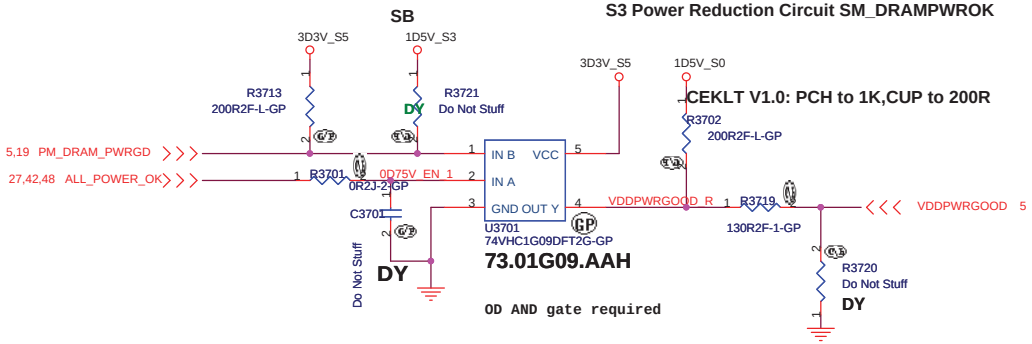
SB to -1 reserve R3723



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ ± 0.55± 200mV and the edge must be monotonic

HR UMA

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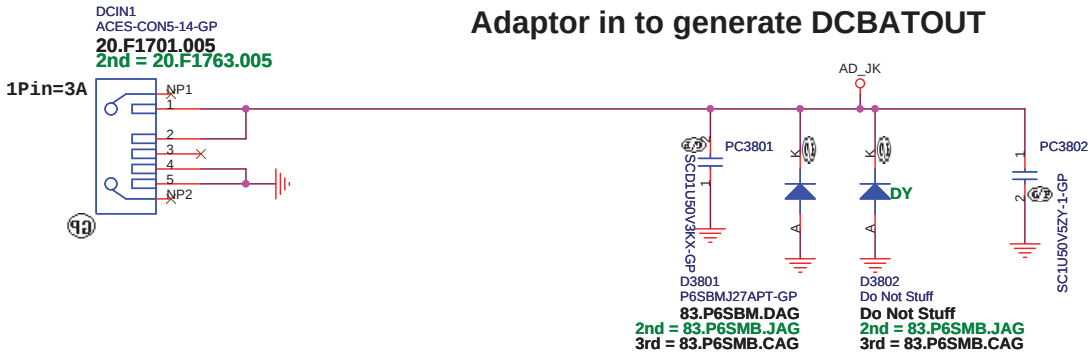
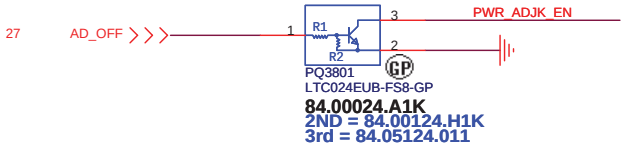
Title: ADAPTER
Size: A3
Document Number: JE40-HR
Rev: -1
Date: Thursday, December 02, 2010
Sheet 37 of 102

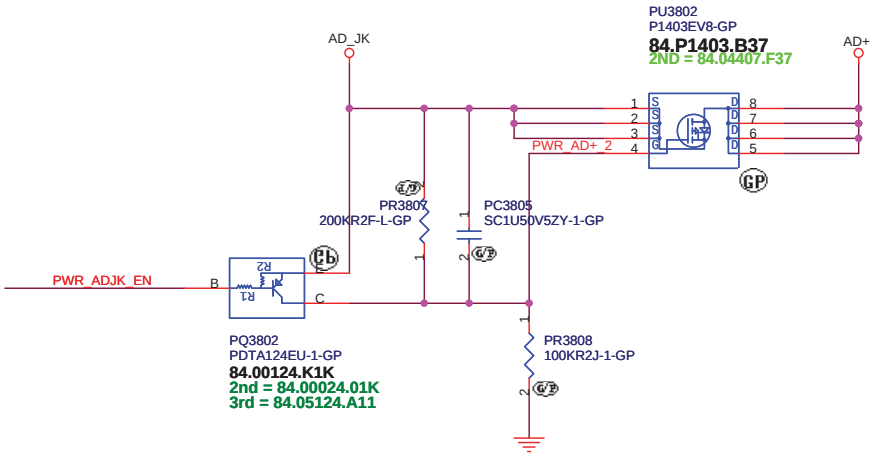
ANNIE solution

Adaptor in to generate DCBATOUT



JE40 change DCIN1 part number

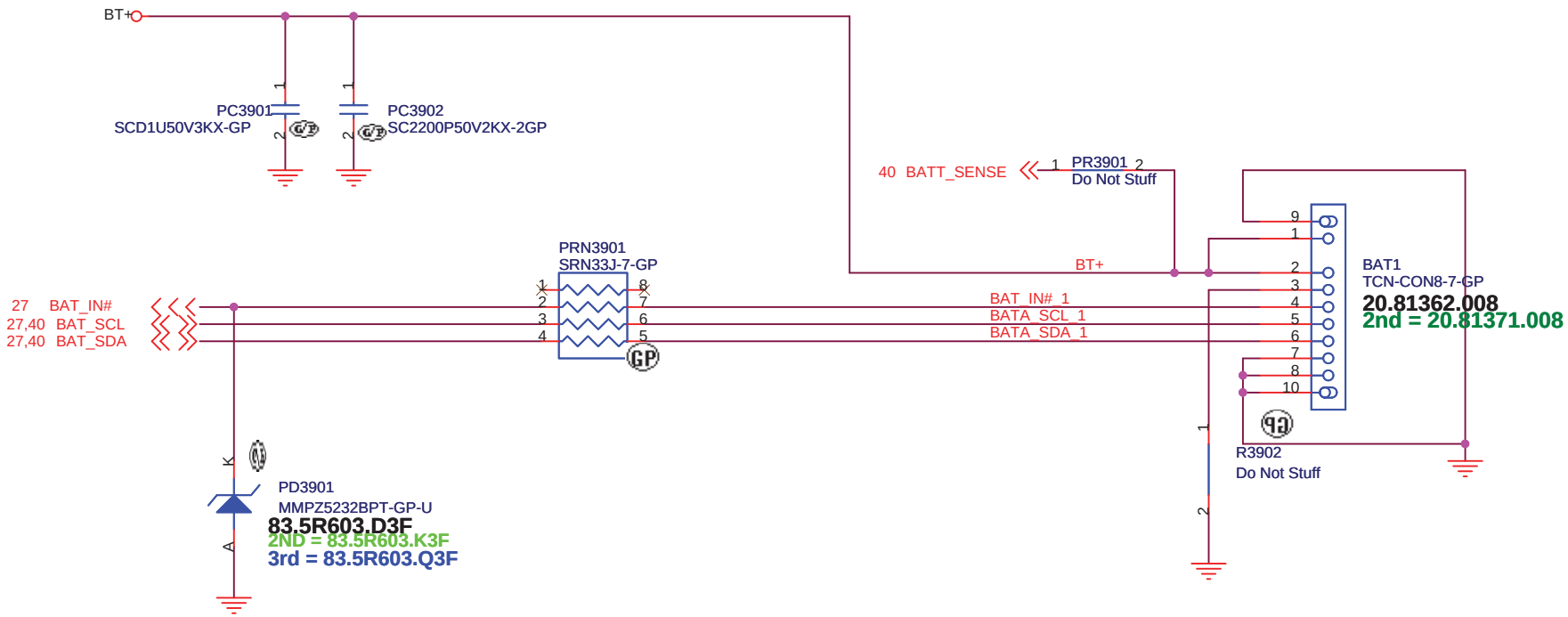




HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN JACK*		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 38 of 102	

BATTERY CONNECTOR



EC Protect

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *BATT CONN*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 39 of 102	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

NEAR

ADD A 24V ZENAR

20100706 Wayne

20100721

20101018

JE40 HR RF

DY

-1M

-1M

AC_OK to KBC

HR UMA

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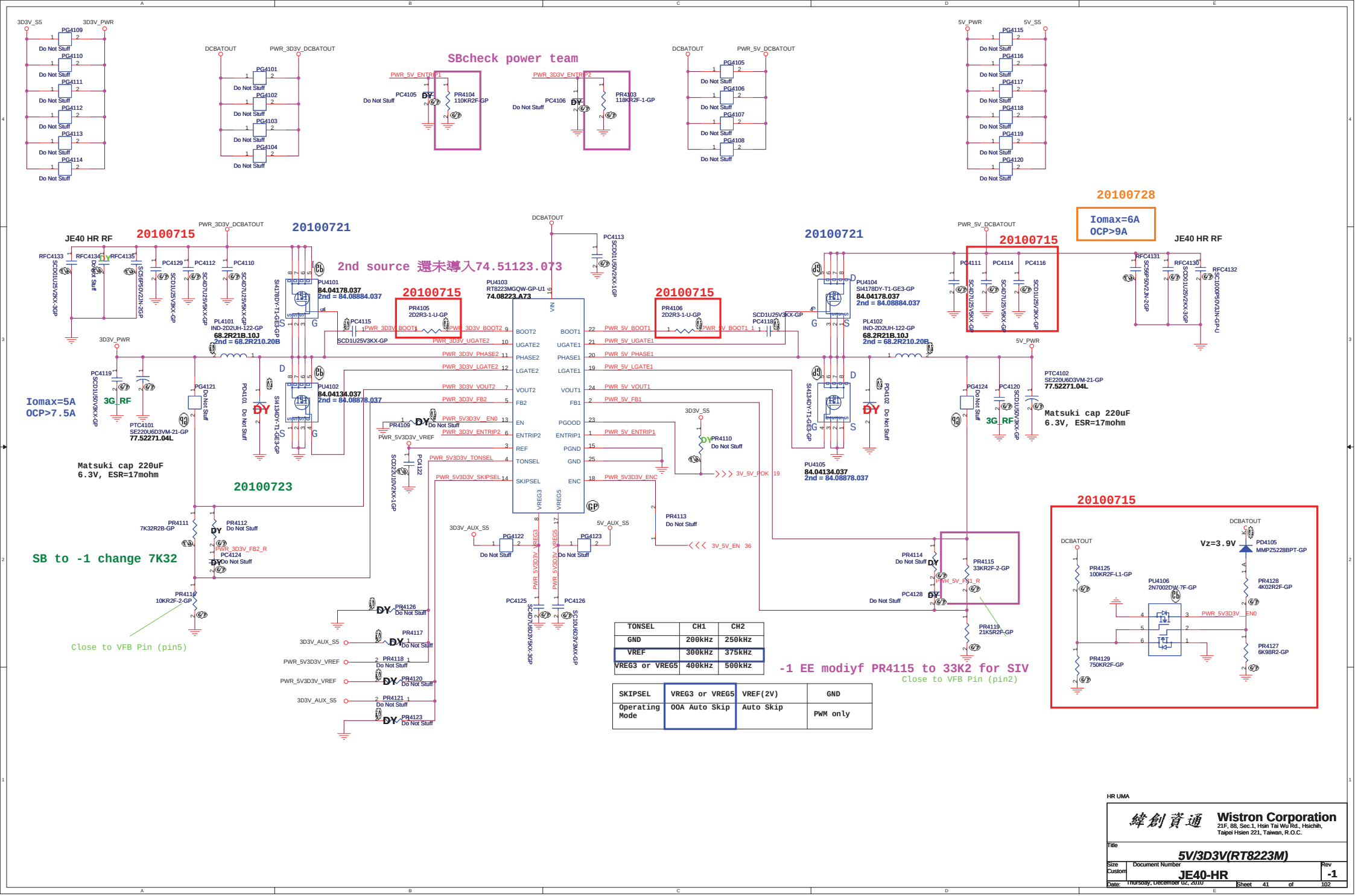
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

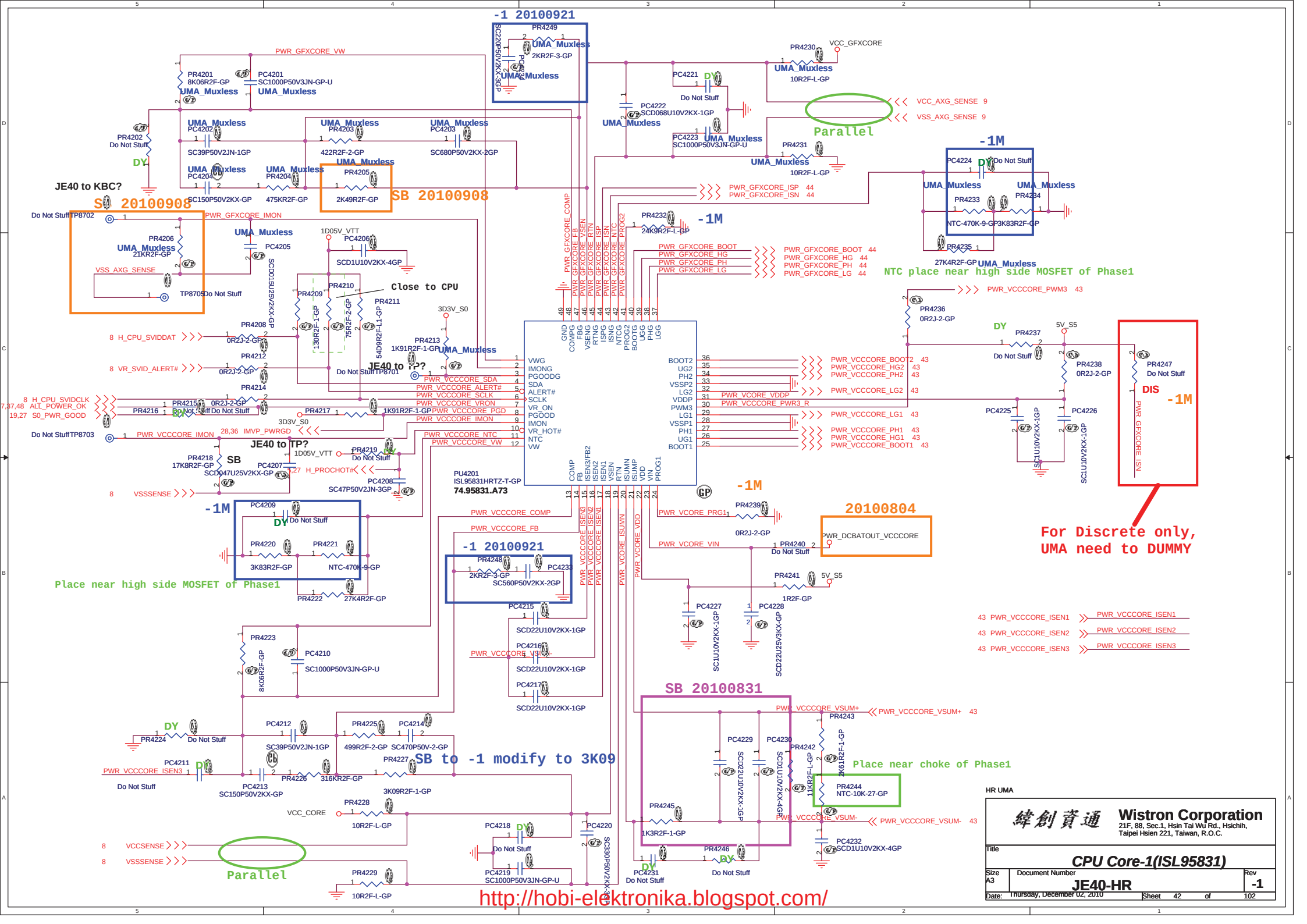
Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 40 of 102



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only



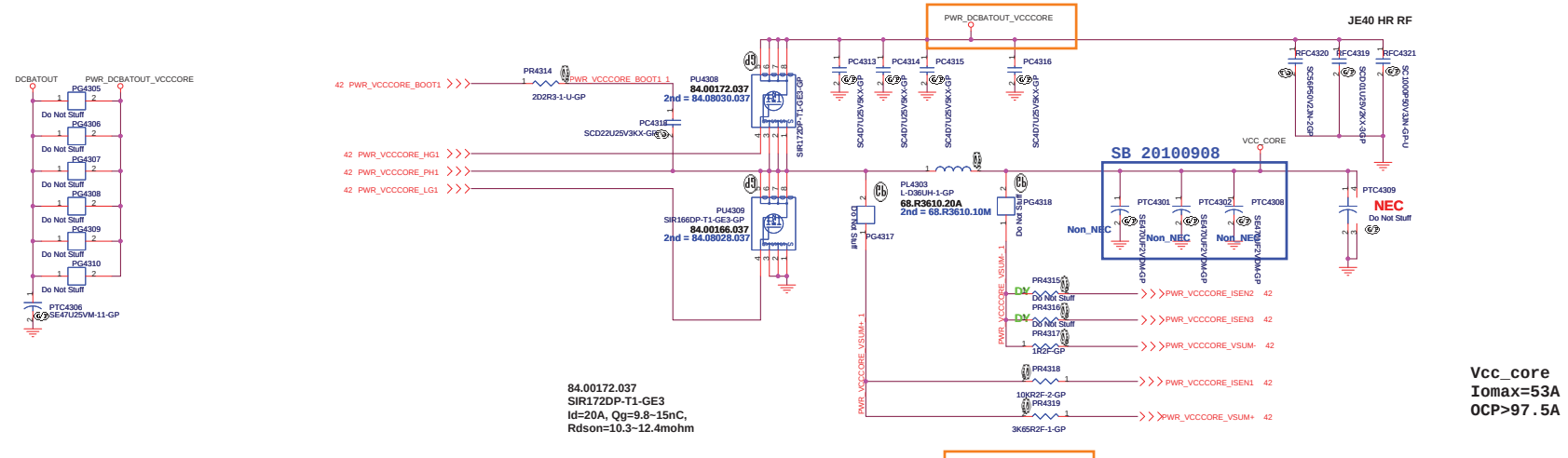
HR UMA

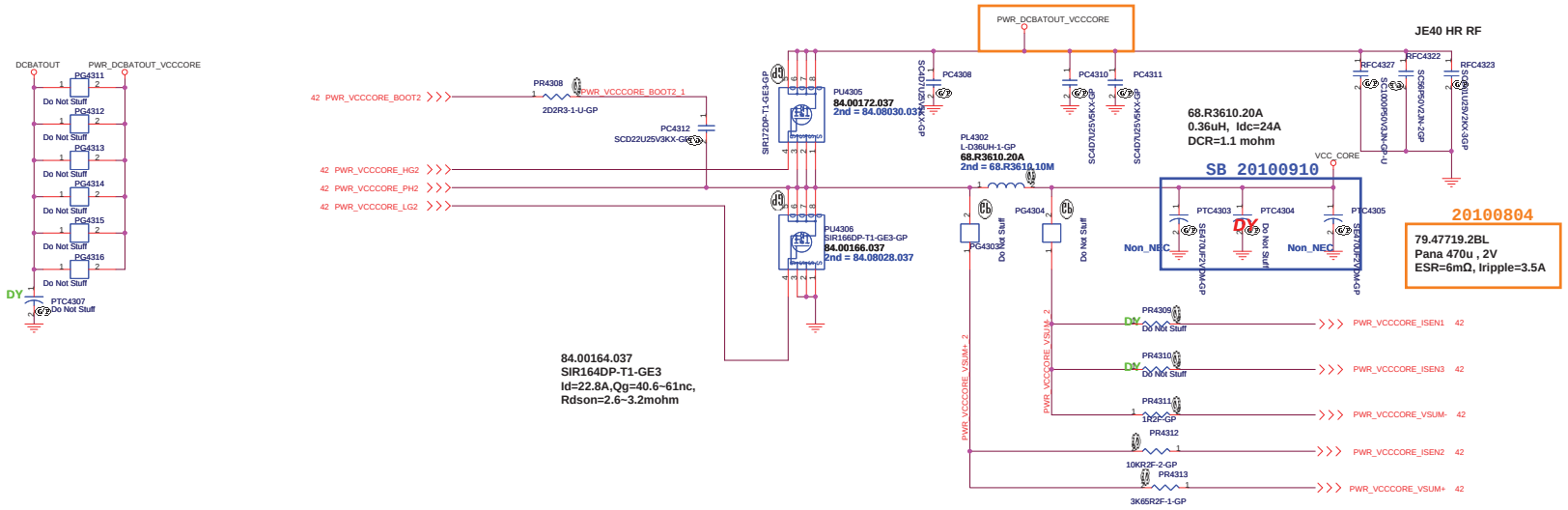
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

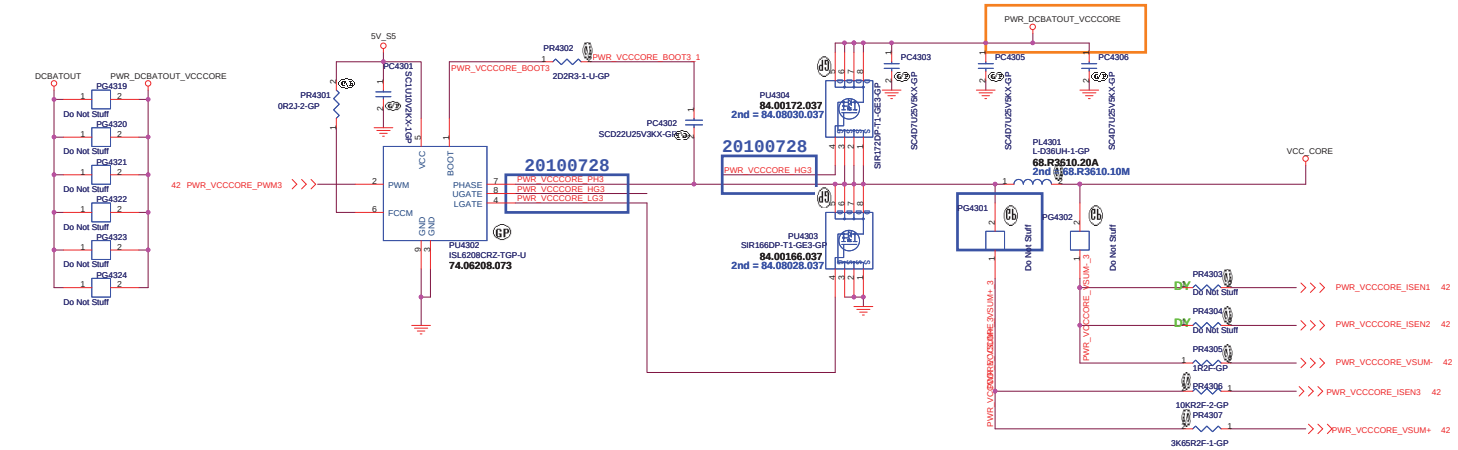
Title: CPU Core-1(ISL95831)

Size: A3 | Document Number: JE40-HR | Rev: -1

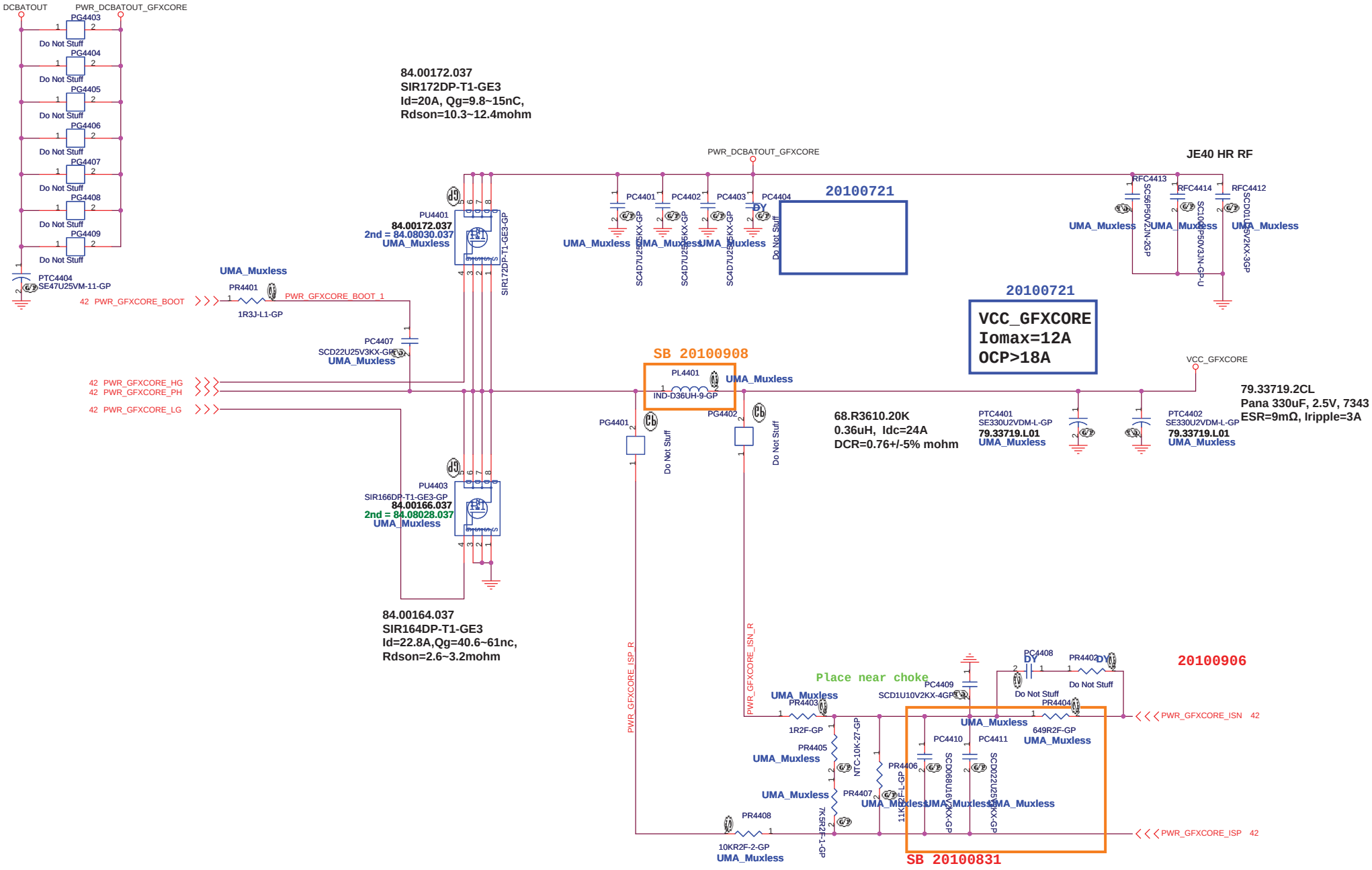
Date: Thursday, December 02, 2010 | Sheet 42 of 102







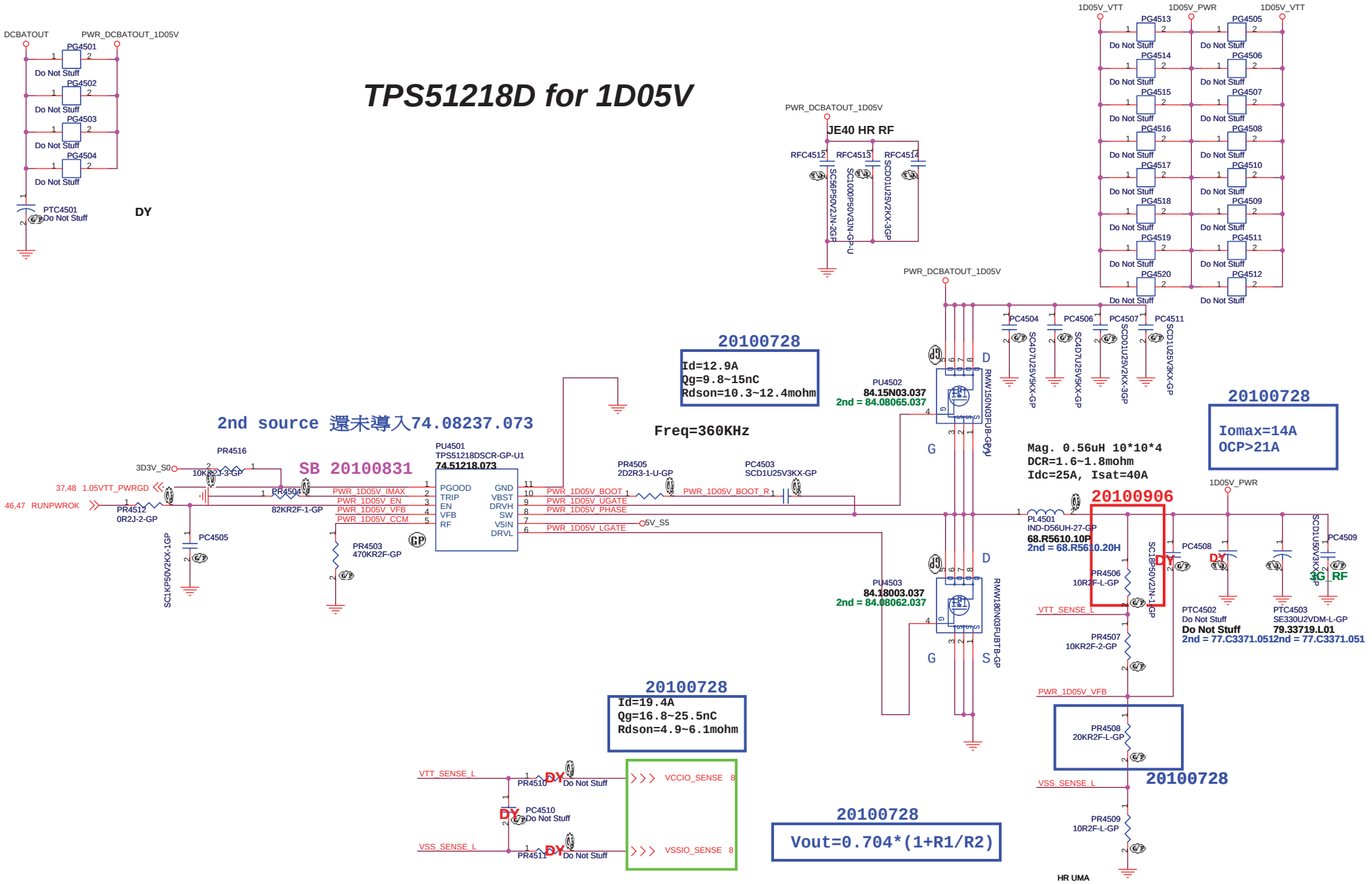
絳創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: CPU Core-2(ISL95831)			
Size: A2	Document Number: JE40-HR	Rev: -1	
Date: Thursday, December 02, 2010	Sheet 43 of 102		



HR UMA

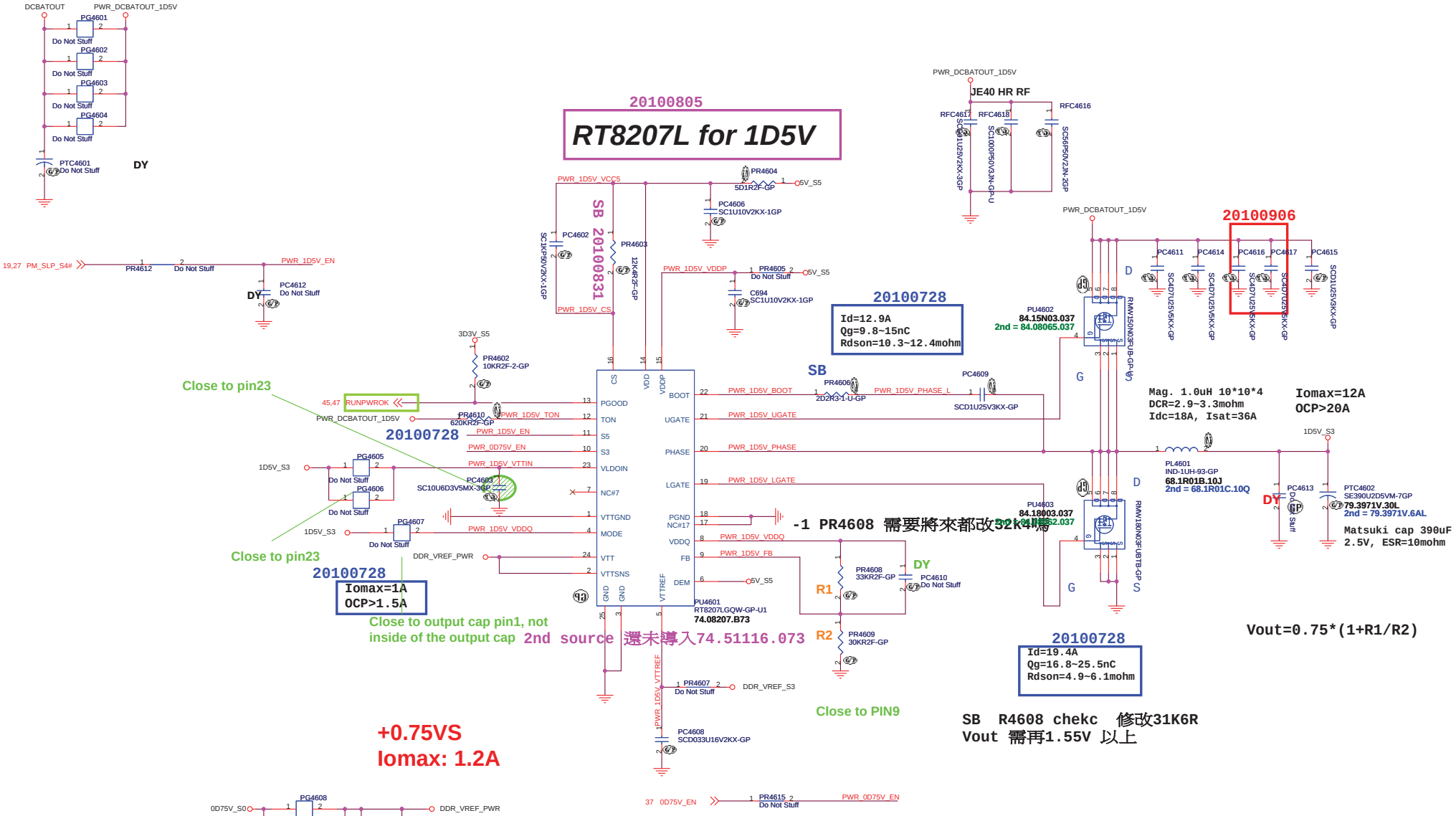
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU Core-3(ISL95831)***	
Size A3	Document Number **JE40-HR**	Rev **-1**
Date: Thursday, December 02, 2010	Sheet 44 of 102	

TPS51218D for 1D05V



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DC to DC 1D05V(TPS51218D)	
Size A3	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 45 of 102	

SSID = PWR.Plane.Regulator_1p5v0p75v



HR UMA

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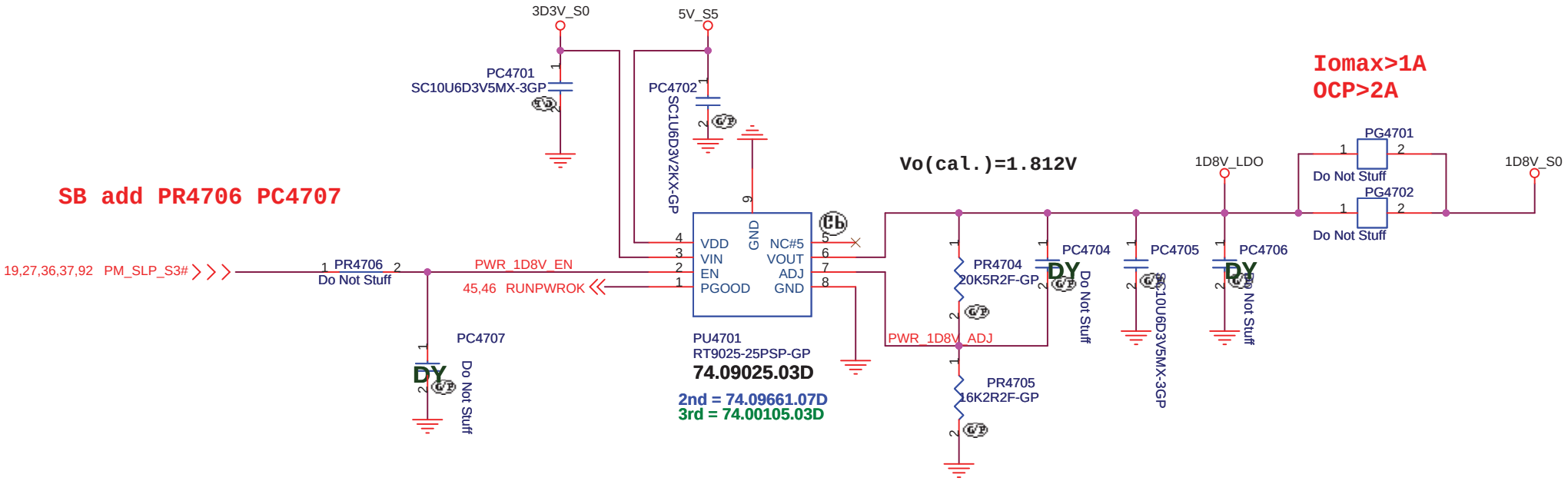
Title: TPS5111		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 46 of 102	

SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0

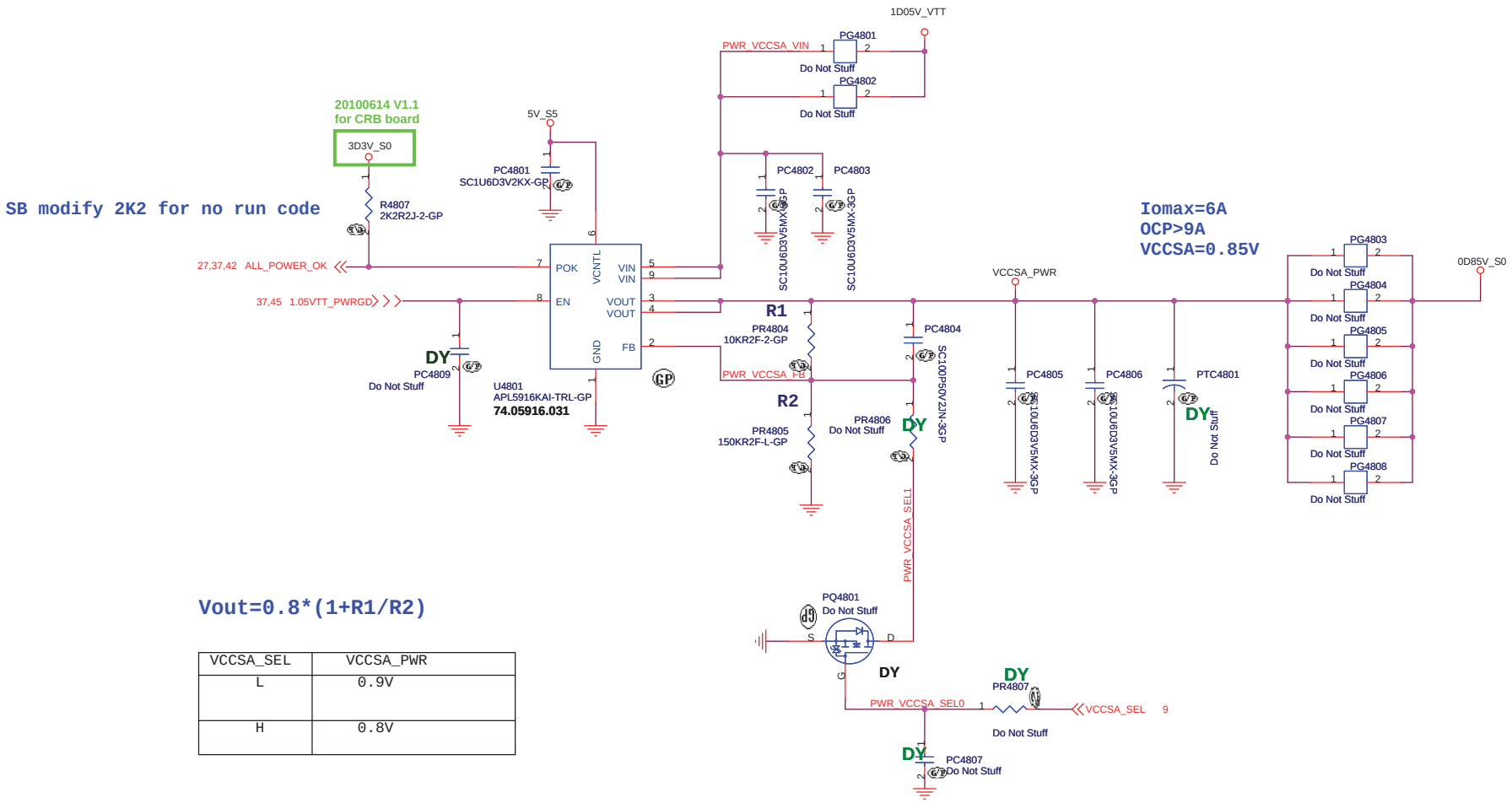


http://hobi-elektronika.blogspot.com/

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LDO_1D8V(RT9025)*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 47 of 102	

APL5916 for VCCSA



Vout=0.8*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

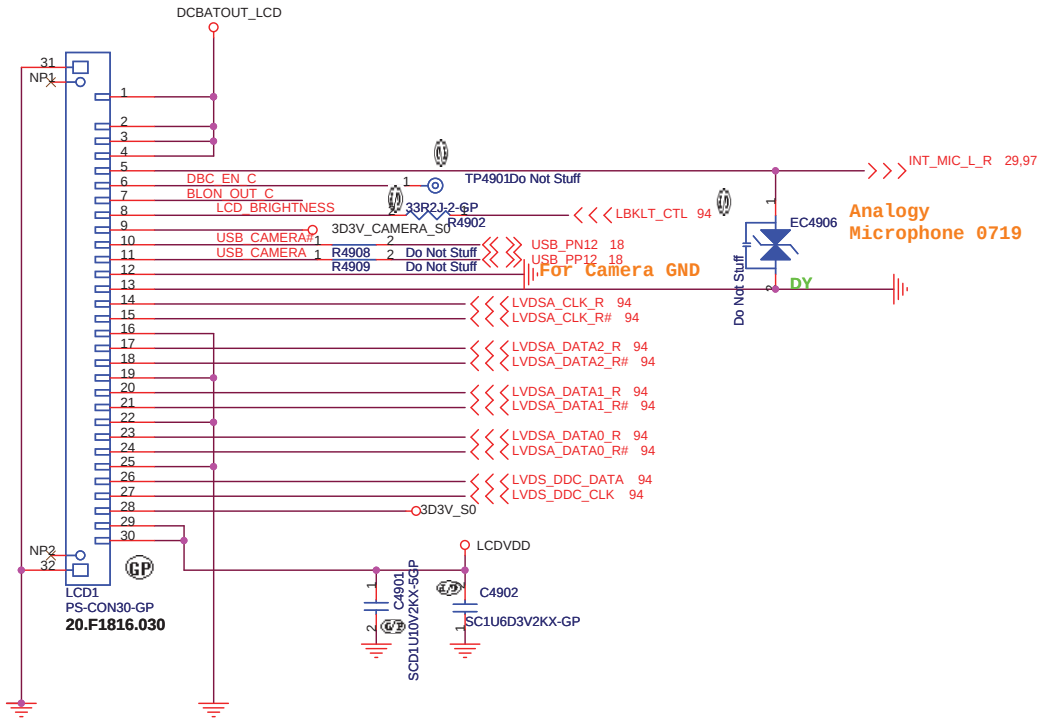
Title: LDO VCCSA(APL5916)

Size: A3 | Document Number: JE40-HR | Rev: -1

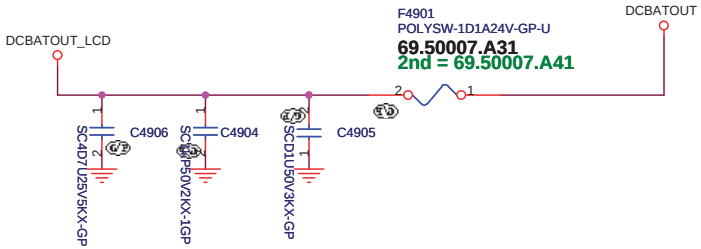
Date: Thursday, December 02, 2010 | Sheet 48 of 102

SSID = VIDEO

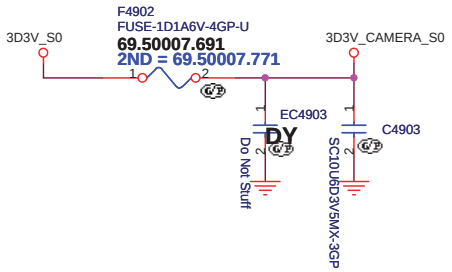
LVDS CONNECTOR



INVERTER POWER

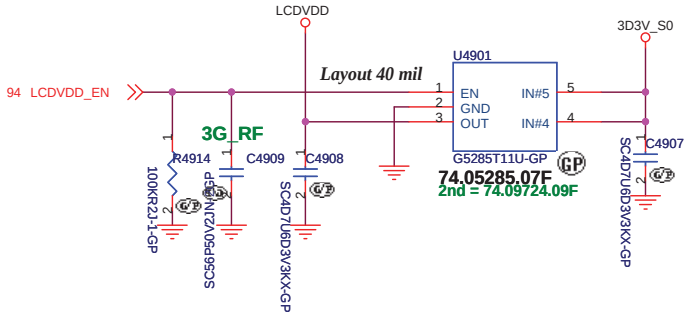


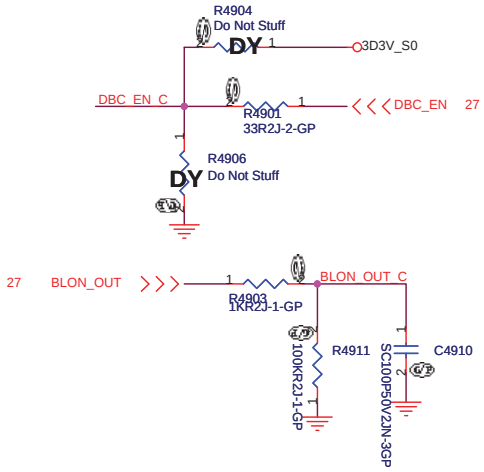
Camera Power



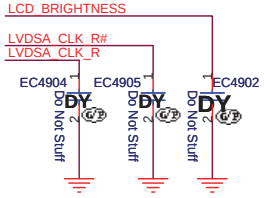
SSID = VIDEO

LCD POWER for ANNIE





For EMI request
Close to LVDS connector



HR UMA

緯創資通 **Wistron Corporation**
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Title	*LCD Connector*	
Size: Custom	Document Number: JE40-HR	Rev: -1
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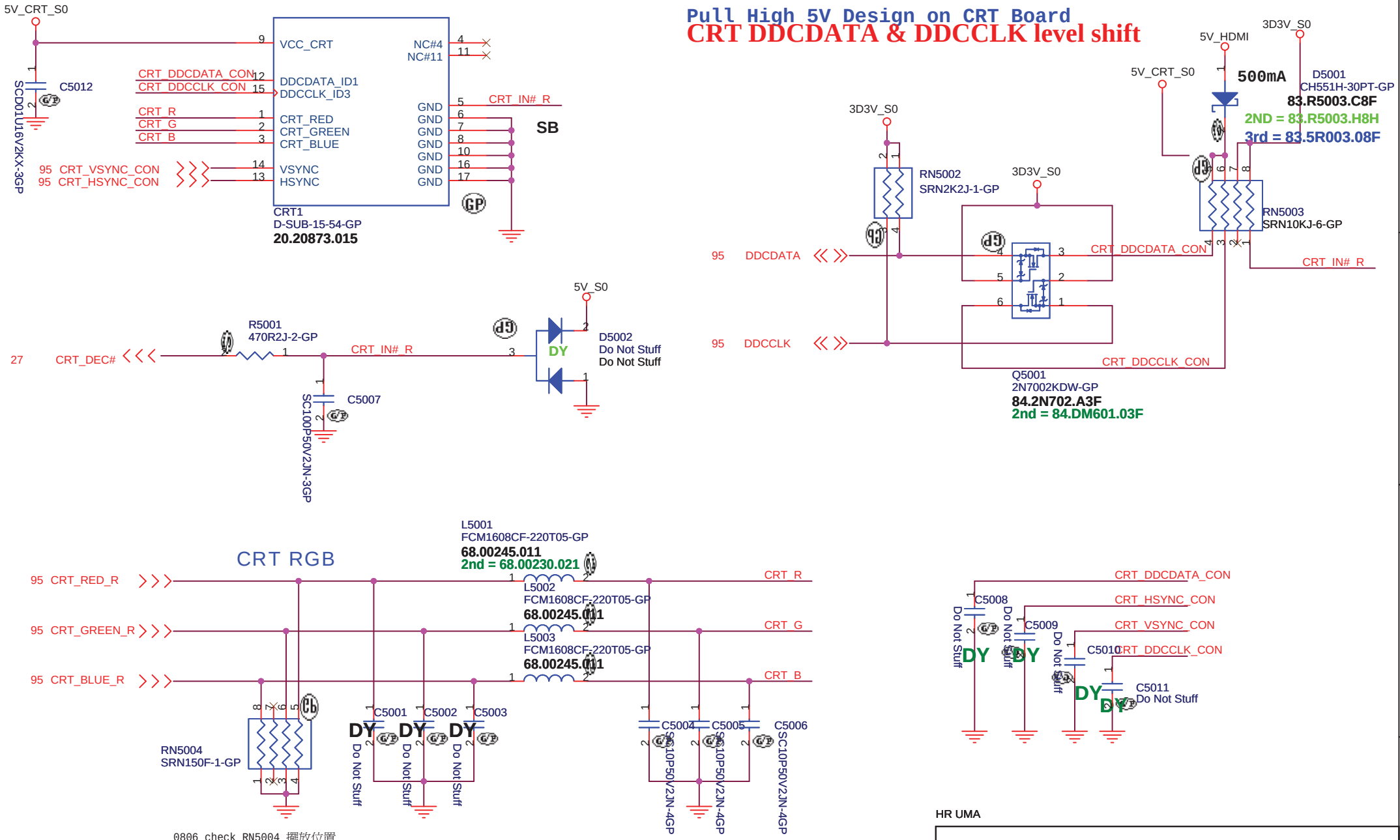
Pull High 5V Design on CRT Board

CRT DDCDATA & DDCCLK level shift



0806 check RN5004 擺放位置

HR UMA

緯創資通

Wistron Corporation

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Title: **CRT Connector**

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A4	JE40-HR	-1

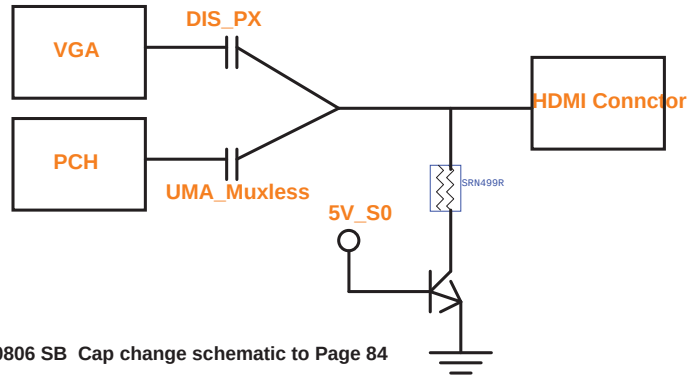
Date: Thursday, December 02, 2010 Sheet 50 of 102

SSID = VIDEO

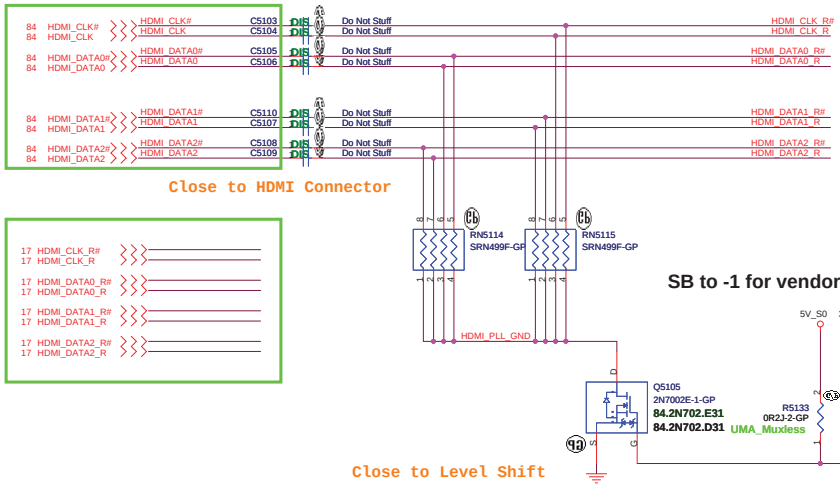
HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

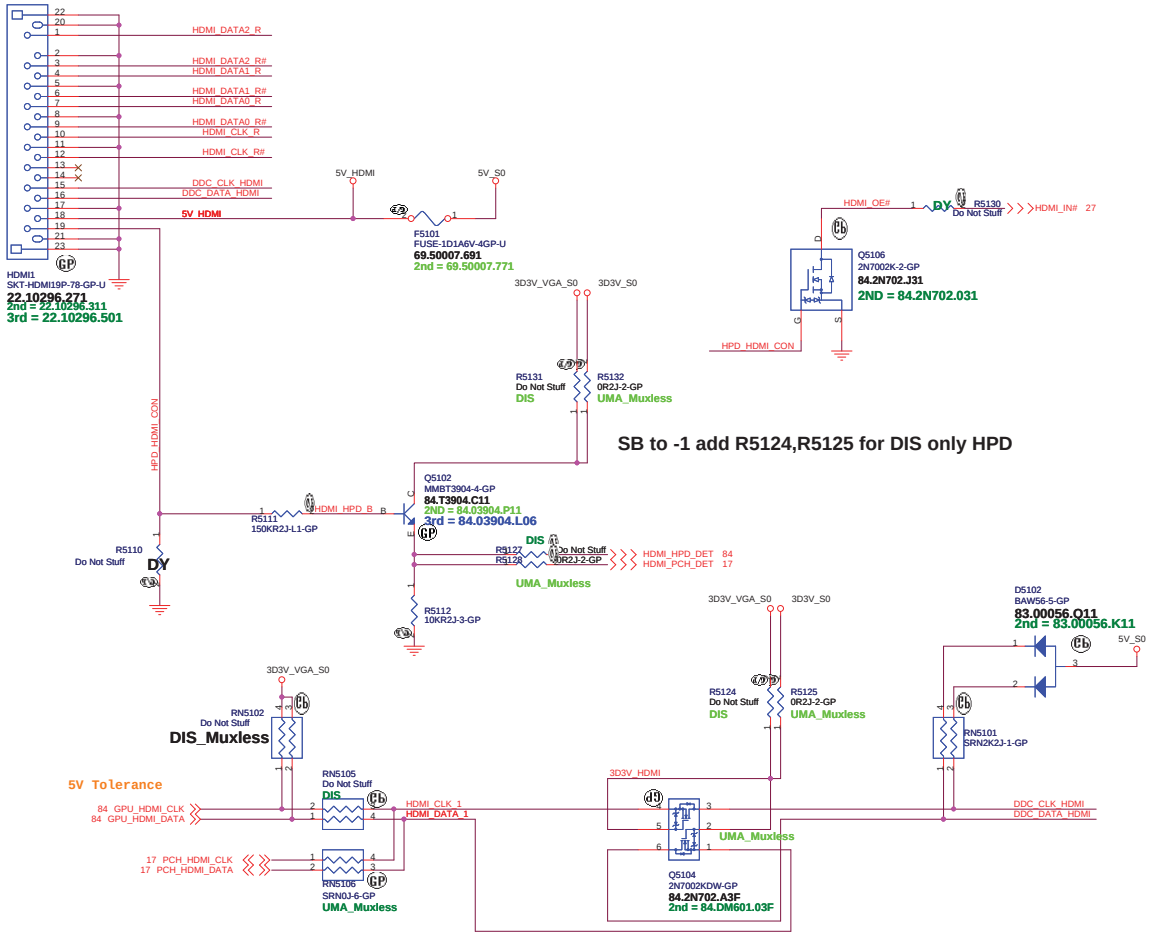
HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84



HDMI CONN



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
Custom	JE40-HR	-1

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LED BACKLIGHT CONVERTER POWER

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***eDP***

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 52 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 53 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

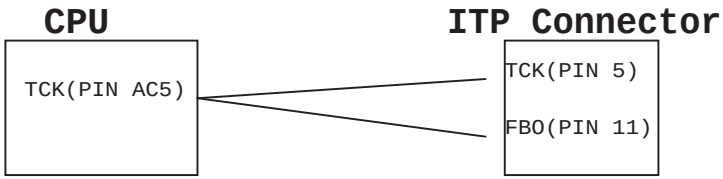
Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



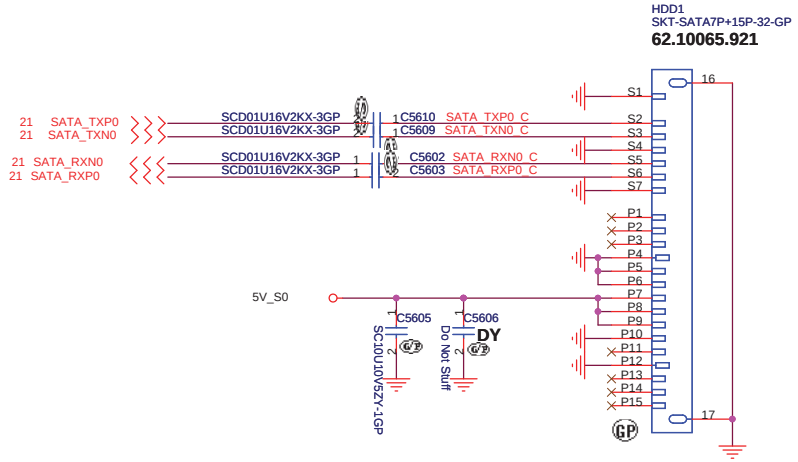
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

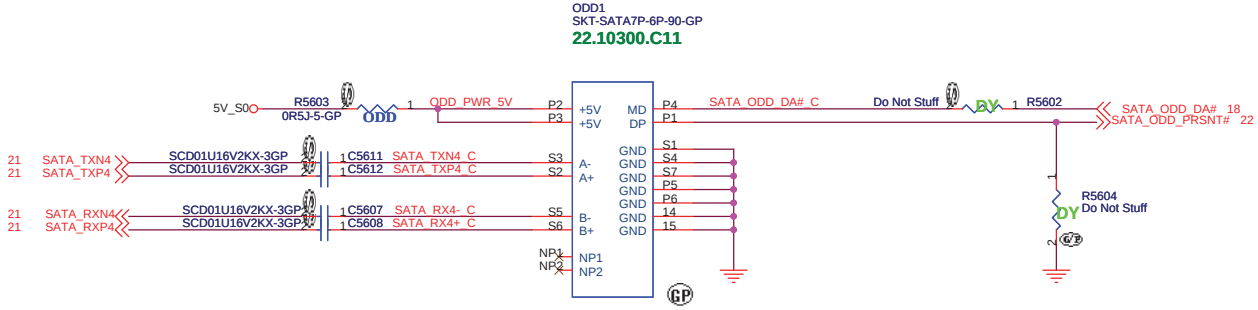
Title: ITP		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 55 of 102	

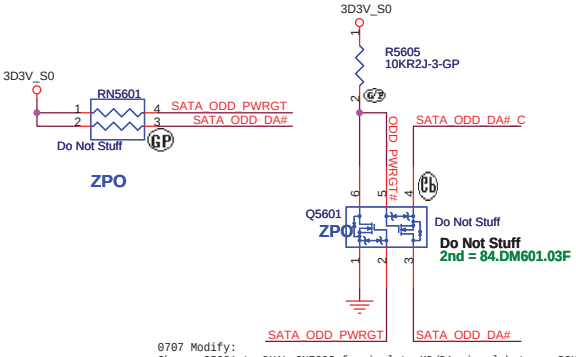
SSID = SATA

SATA HDD Connector



ODD Connector



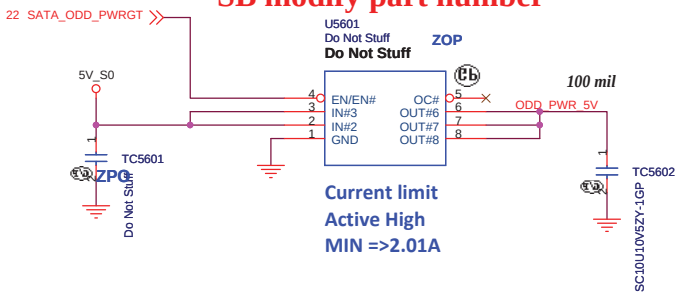


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 56 of 102

ESATA Power

USB CHARGER

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***E-SATA/USB CHARGER***

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 57 of 102

SSID = AUDIO

Speaker Connector

LINE1 OUT
SPDIF

JE40 Modify LINE OUT

Audio at small board

MIC IN

Internal
Microphone

JE40 delete Line in function

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 58 of 102	

GIGA Lan Transformer

SSID = LOM

LAN MDI Off-Page

XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

XF5902
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

SB modiyf Pin9 Pin10 SWAP

LED COLOR
10(+) 9(-)::GREEN
12(+) 13(-):ORANGE

RJ45
RJ45-12P-16-GP
22.10321.Y21
2nd = 22.10321.Y91

RN5901
SRN470J-4-GP-U

EC5901 EC5902
Do Not Stuff
DY DY

SB modify For EMI

U5901 U5902 U5903 U5904
TVLST2304AD0-GP
SURGE

GDT1 GDT2 GDT3 GDT4
B88069X9231T103-GP
SURGE

R5903 R5901 R5902 R5904
75R3J-L-GP

C5905
SC1KP2KV6KX-GP

C5916 C5917 C5918 C5919
Do Not Stuff

EC5910 EC5909 EC5903 EC5904 EC5905 EC5906 EC5908 EC5907
SCB2BF50V2CN2GP

C5907 C5906
Do Not Stuff

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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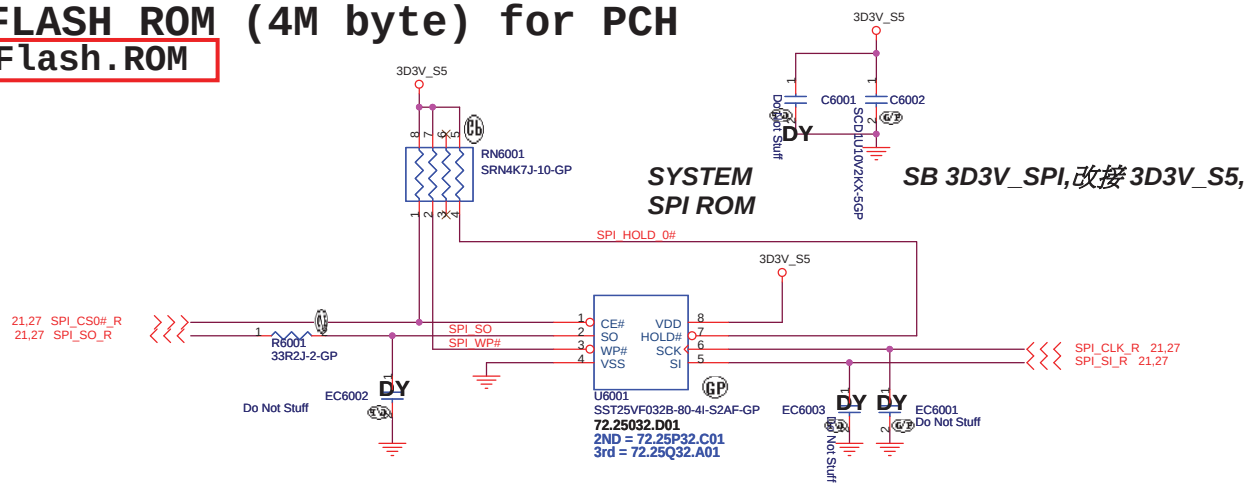
Title: LAN CONNECTOR
Size: Custom | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 59 of 102

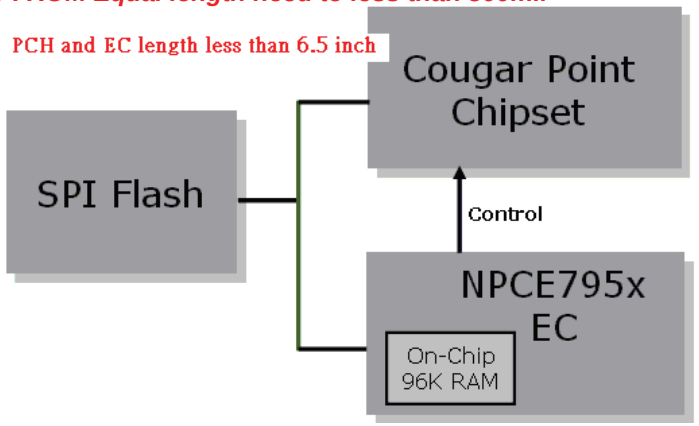
SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

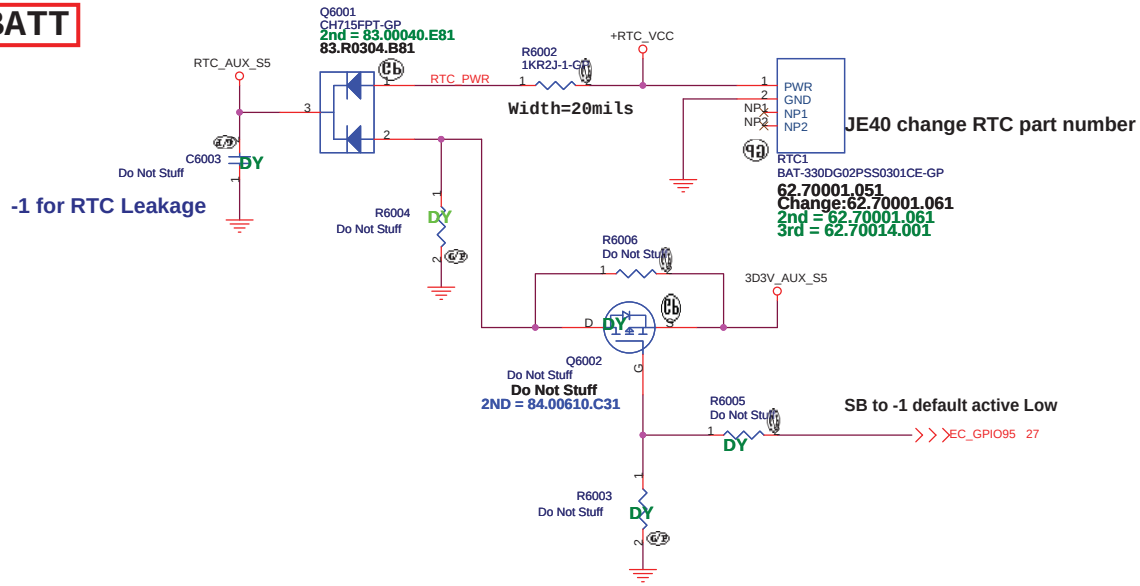


SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



SSID = RBATT

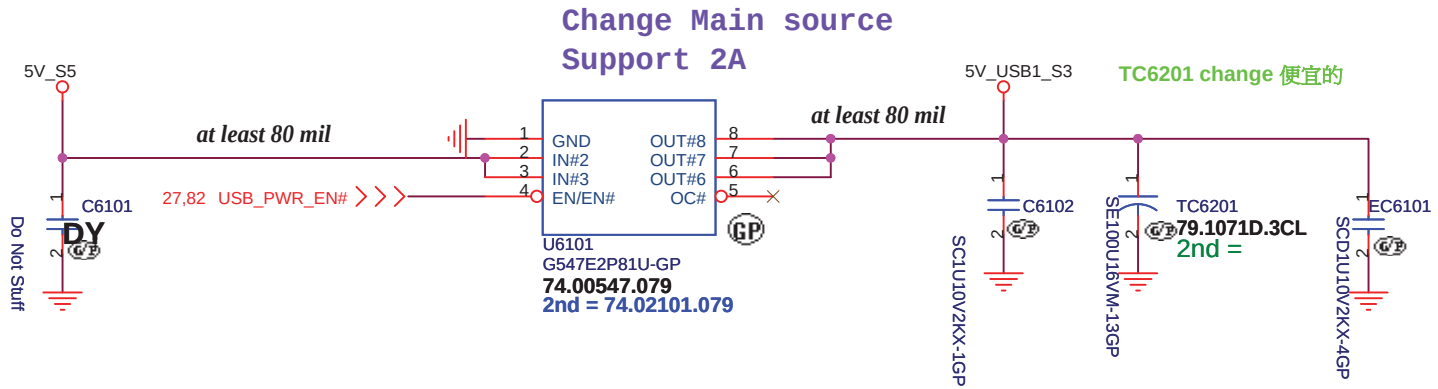


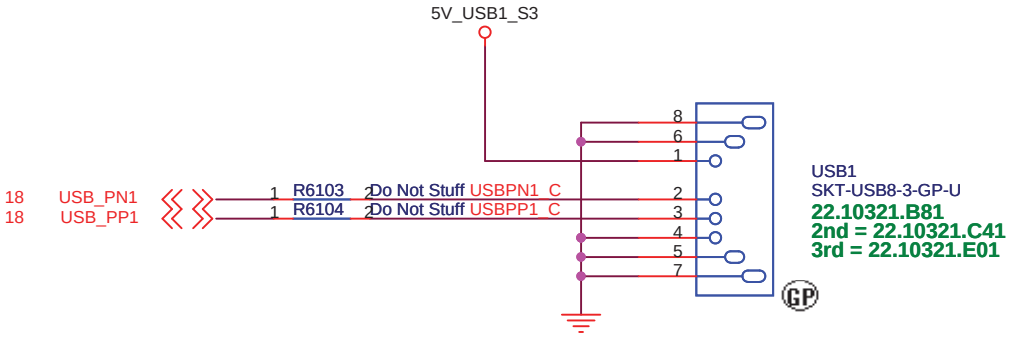
HR UMA

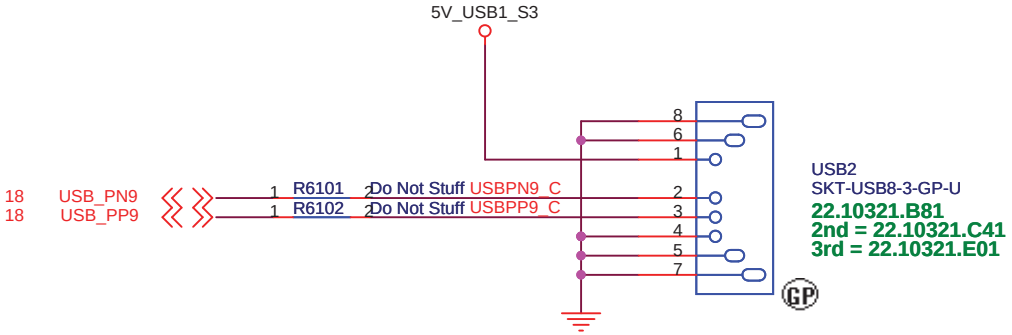
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Flash/RTC*		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 60 of 102	

SSID = USB

IO Board USB Power







HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A4	JE40-HR	-1

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Port***

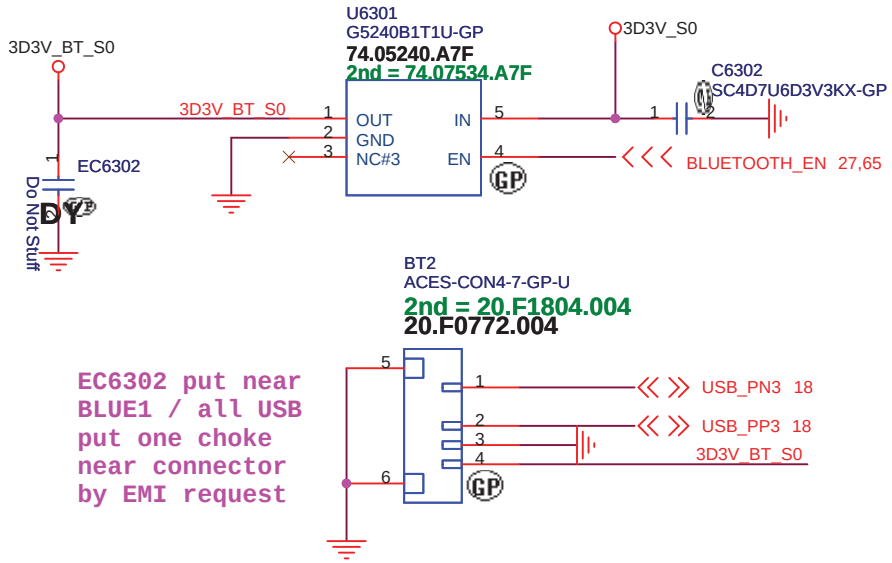
Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 62 of 102

SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module



http://hobi-elektronika.blogspot.com/

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 63 of 102	

Finger printer

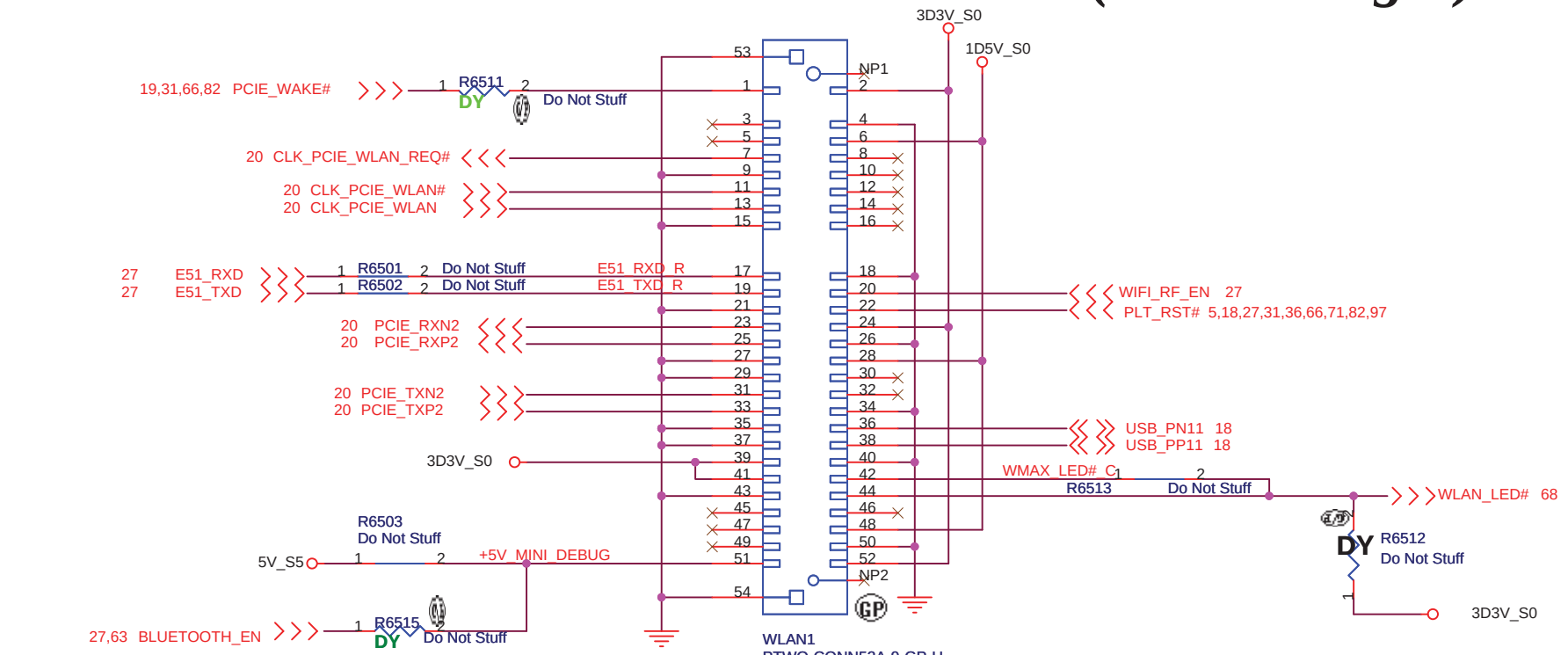
JE40 delete FP function

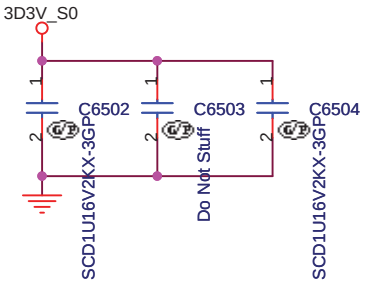
HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***RESERVED***	
Size: A4	Document Number: **JE40-HR** Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 64 of 102

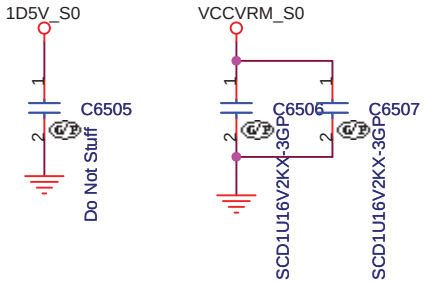
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

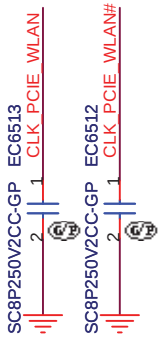




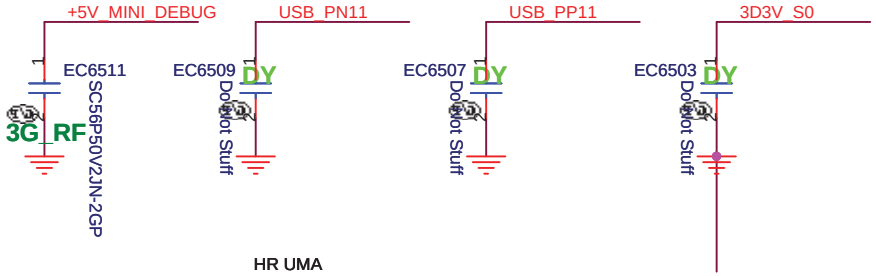
-2



SB modify for SIV



RF suggestion



HR UMA

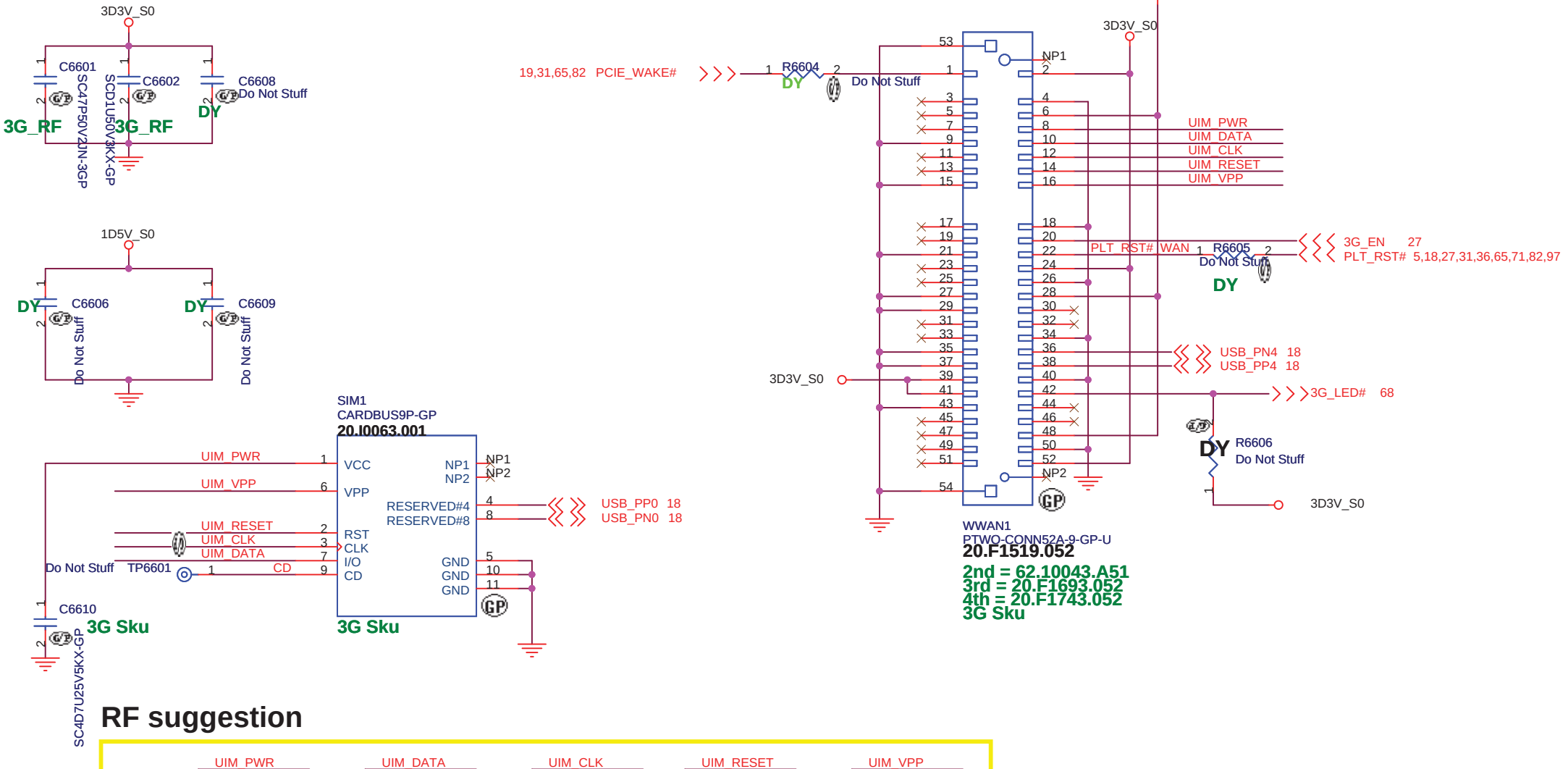
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINICARD(WLAN)/ITP CONN***	
Size A4	Document Number **JE40-HR**	Rev **-1**
Date: Thursday, December 02, 2010	Sheet 65 of 102	

SSID = Wireless

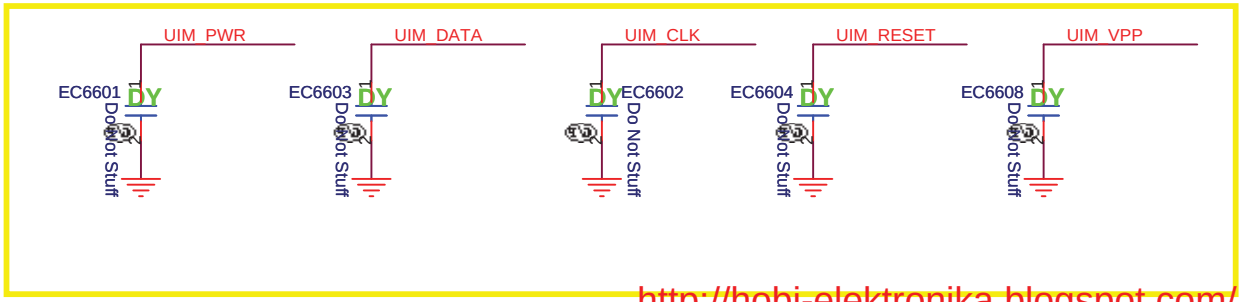
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



RF suggestion



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 66 of 102

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

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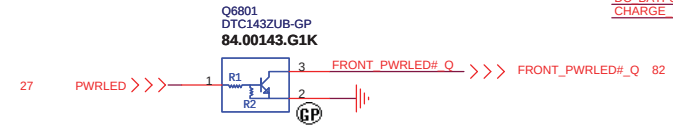
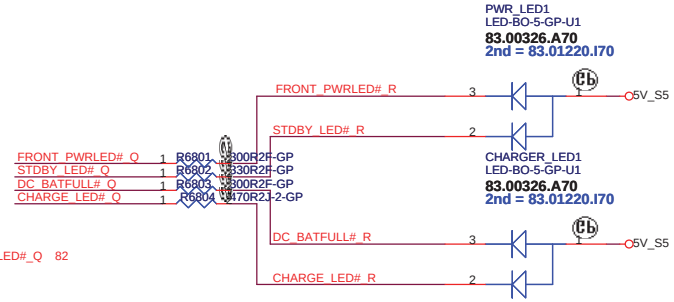
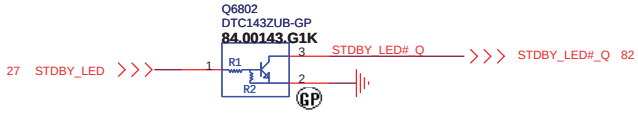
SSID = User.Interface

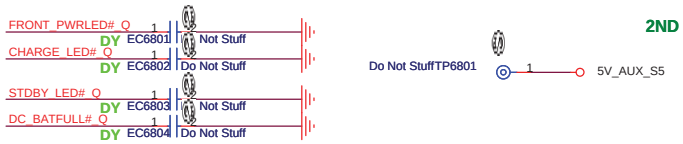
Power button LED





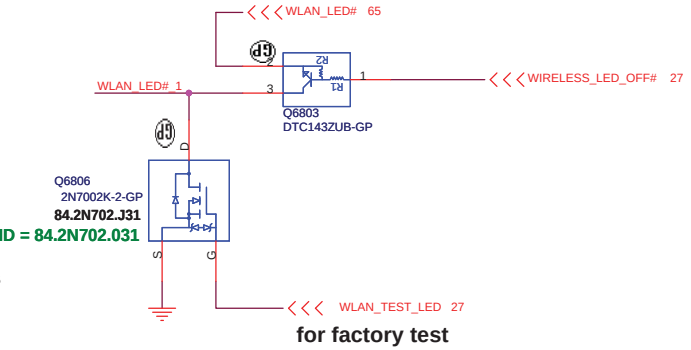
Power STDBY_LED





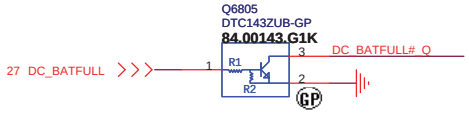
WLAN_LED

From module

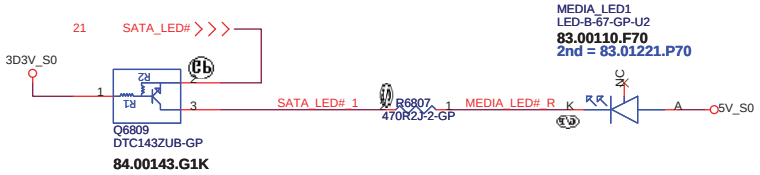


for factory test

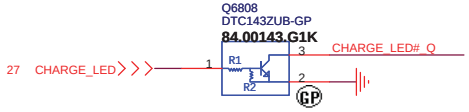
Battery LED2(DC_BATFULL)

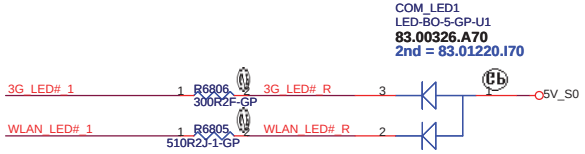


SATA HDD LED



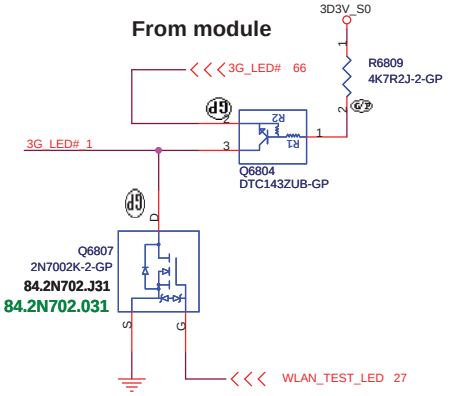
Battery LED1(CHARGE)





3G LED

From module



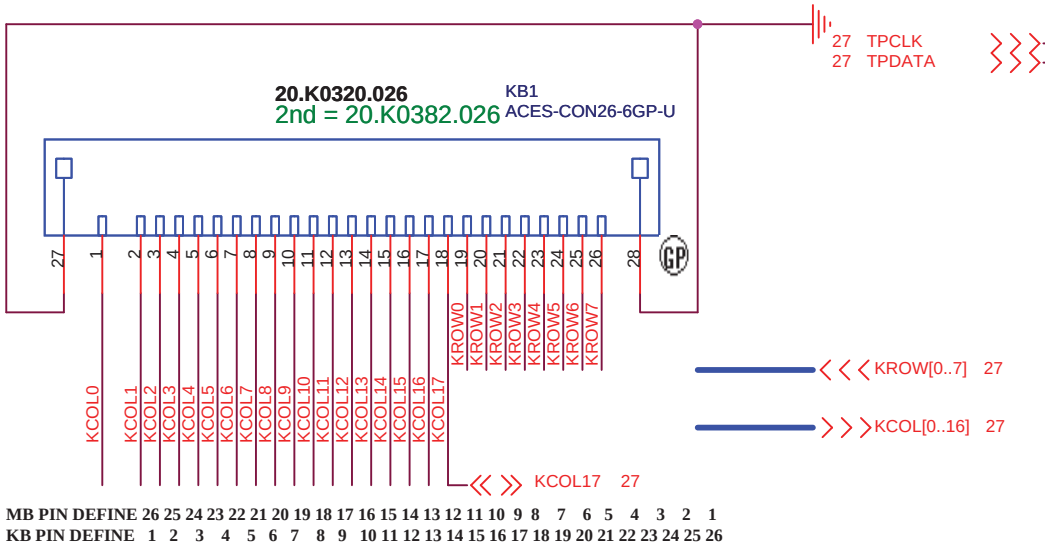
for factory test

HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED Bard/Power Button	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 68 of 102	

SSID = KBC

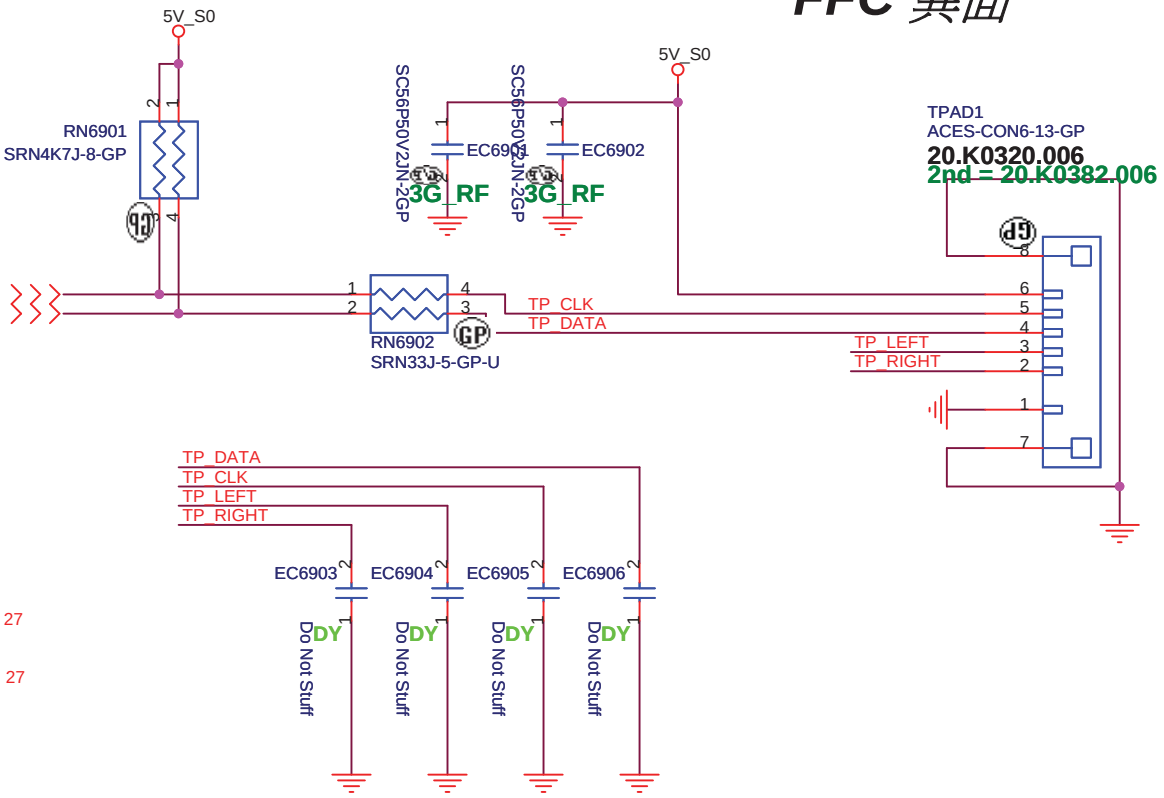
Internal KeyBoard Connector



MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1 **SB to -1 modify Part number**

TOUCH PAD



FFC 異面

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size	Document Number	Rev
A4	JE40-HR	-1

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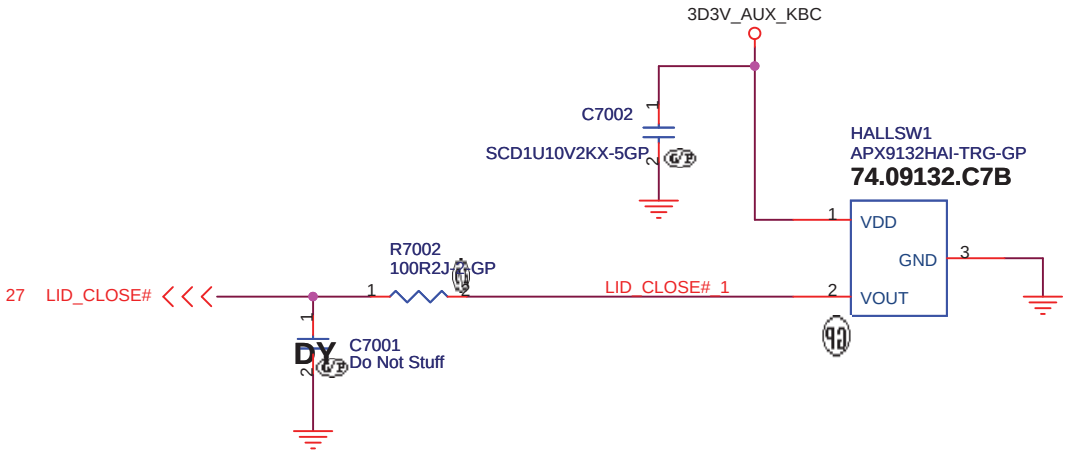

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

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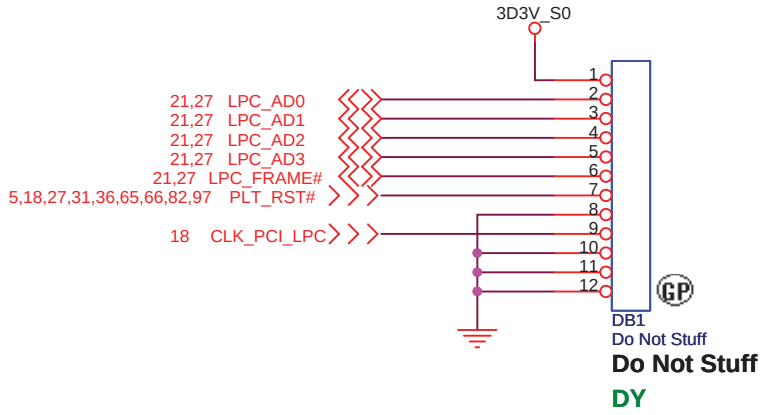

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

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HR UMA

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Reserved*
Size A3 / Document Number	JE40-HR / Rev -1
Date: Thursday, December 02, 2010	Sheet 72 of 102

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HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

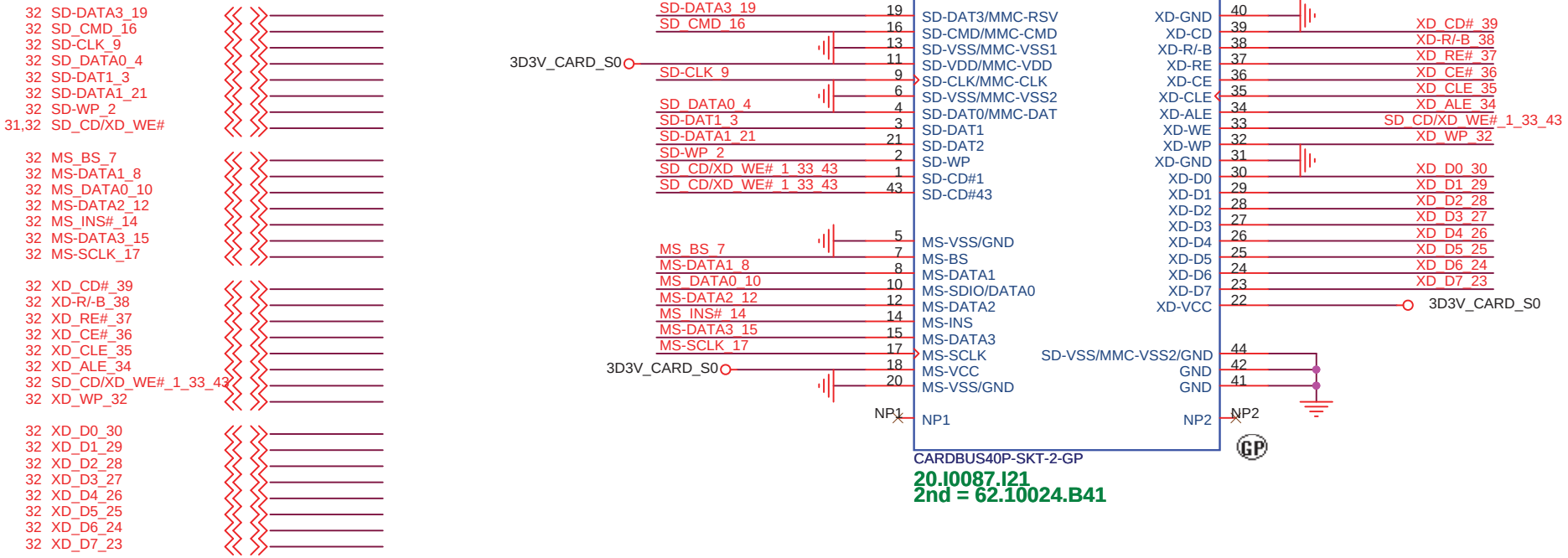
Title: *Reserved*

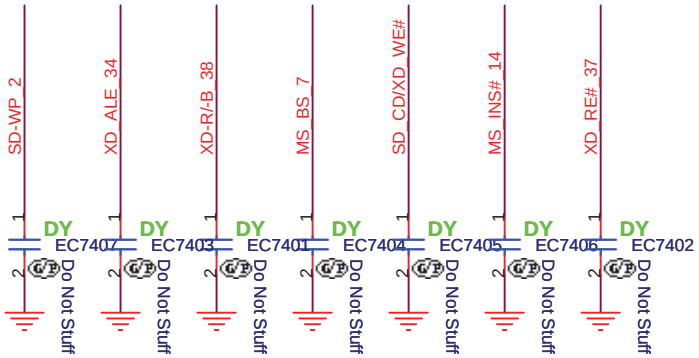
Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 73 of 102

SD/XD/MS Card Reader

SSID = SDIO





HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 74 of 102

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 75 of 102

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 76 of 102

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 78 of 102

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 79 of 102	

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

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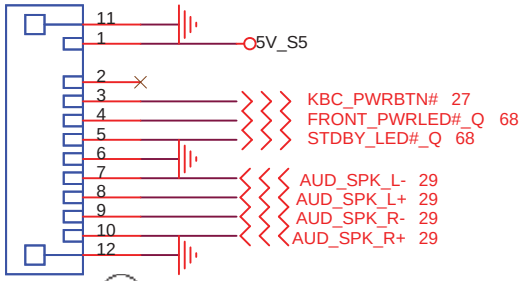
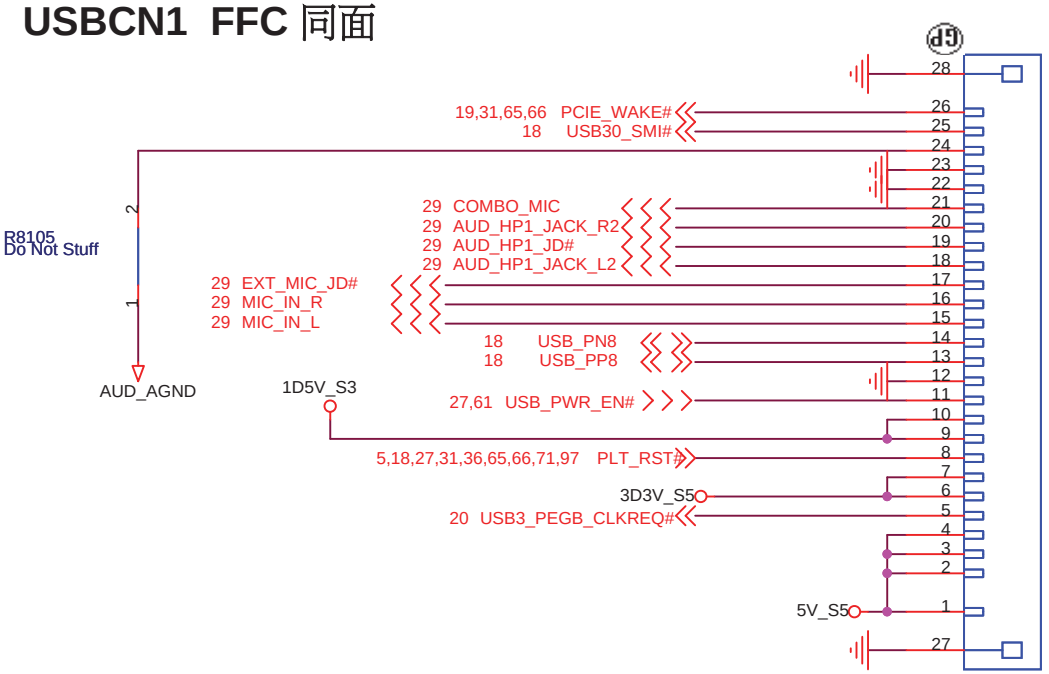
PWRCN1 FFC 異面



PWRCN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010

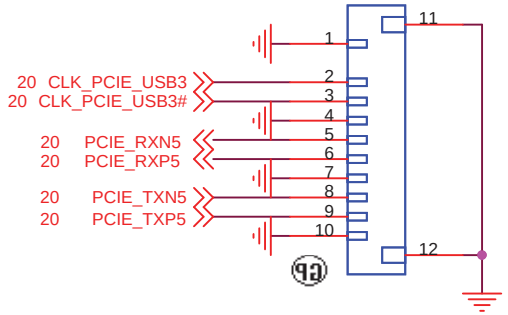
USBCN1 FFC 同面



USBCN1
ACES-CON26-11-GP
20.K0315.026
2nd = 20.K0370.026

0806 change 10Pin

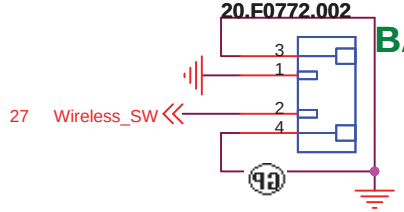
USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010



USBCN2 FFC 同面

-1 add RF connector
BAE40 Only

RF_CN1
ACES-CON2-11-GP
20.F0772.002
BAE40



Cabele Wire to BD

HR UMA

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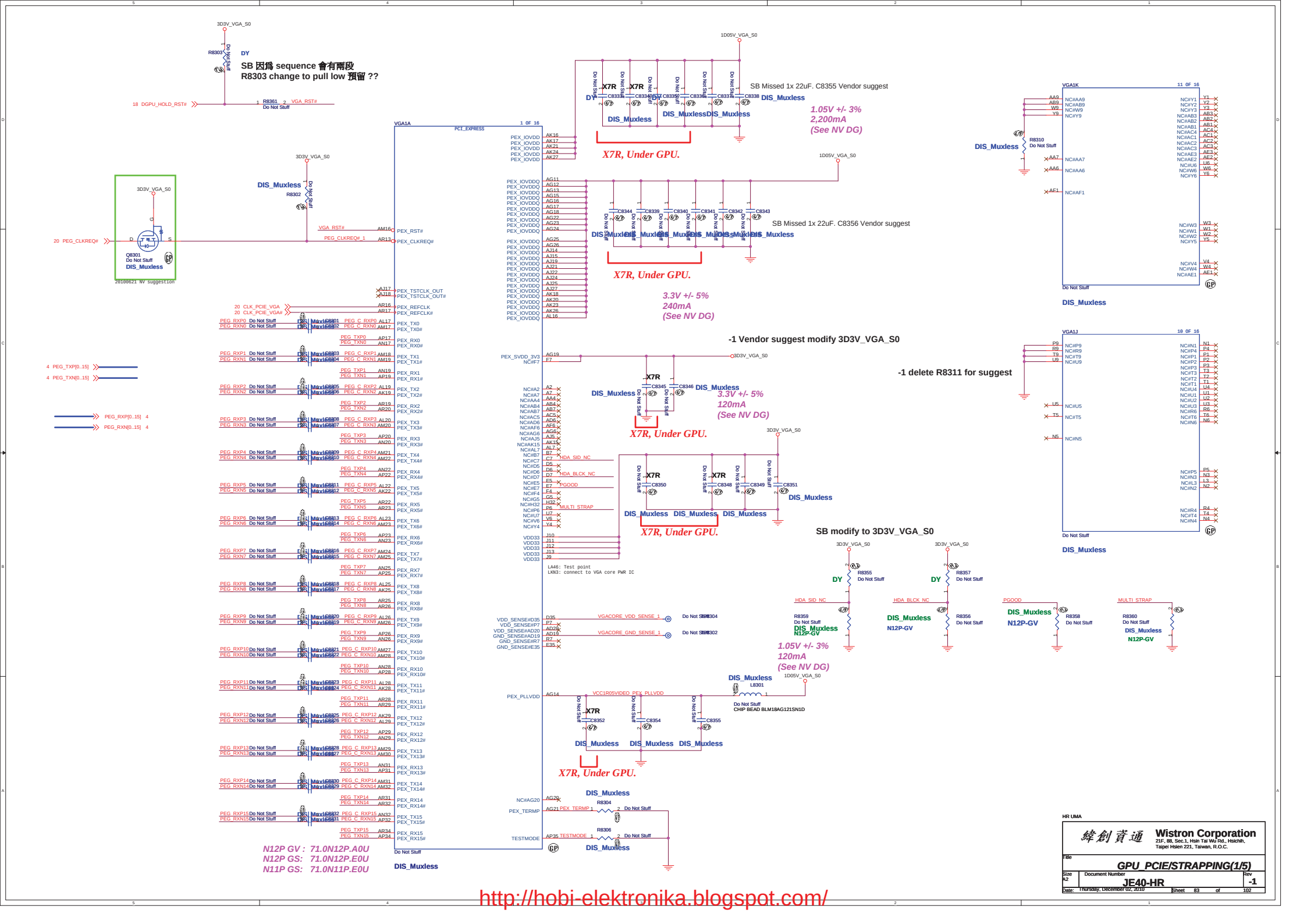
Taipei Hsien 221, Taiwan, R.O.C.

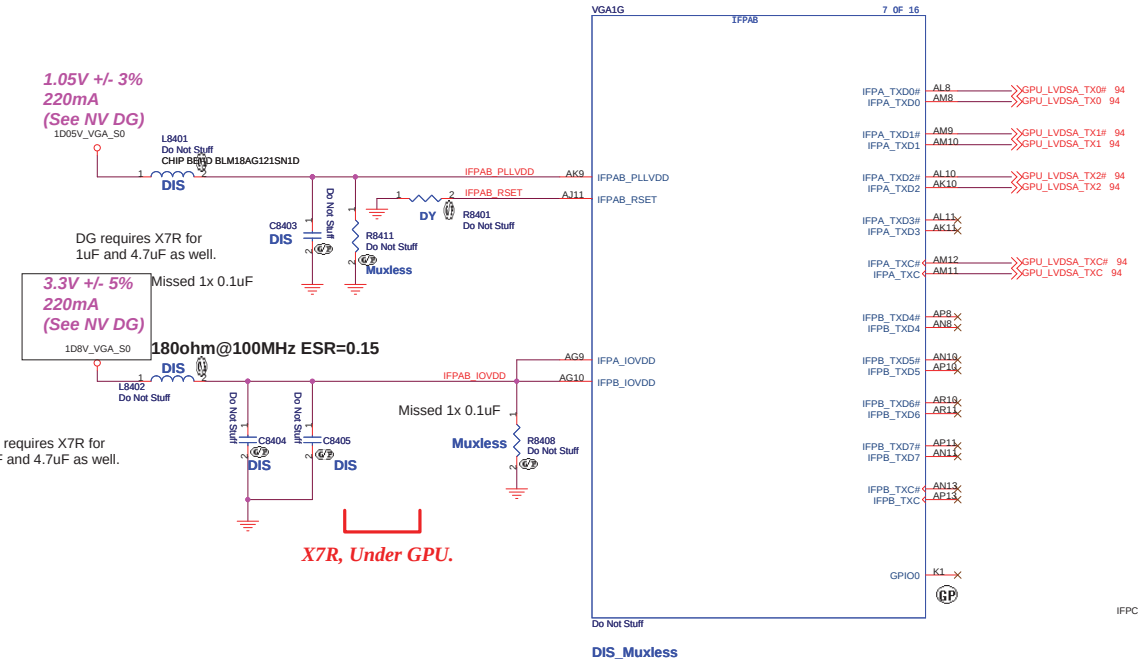
Title: ***IO Board Connector***

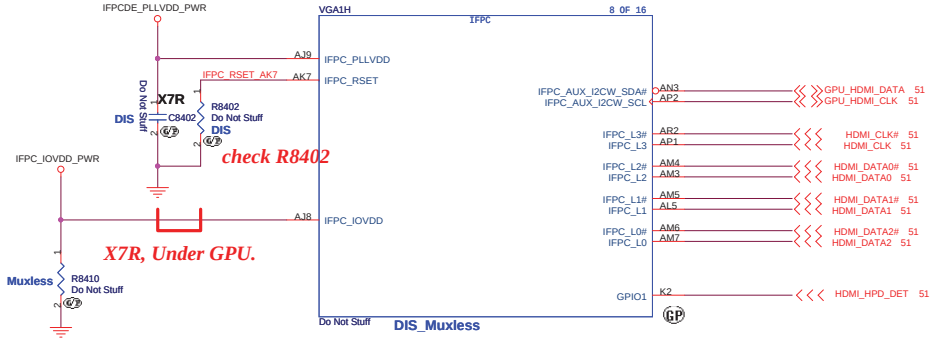
Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 82 of 102

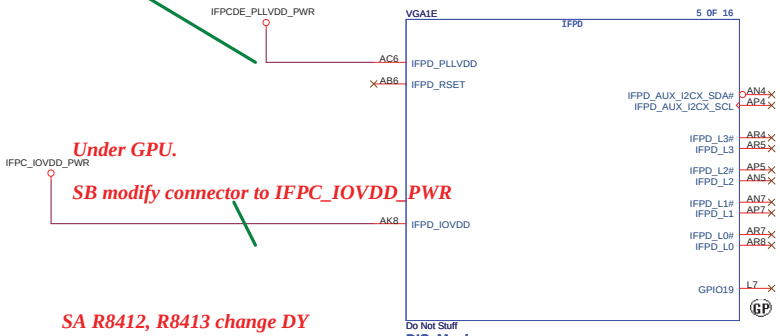

SB 因爲 sequence 會有兩段
R8303 change to pull low 預留 ??
SB Missed 1x 22uF. C8355 Vendor suggest
1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
SB Missed 1x 22uF. C8356 Vendor suggest
3.3V +/- 5%
240mA
(See NV DG)
-1 Vendor suggest modify 3D3V_VGA_S0
3.3V +/- 5%
120mA
(See NV DG)
-1 delete R8311 for suggest
SB modify to 3D3V_VGA_S0
1.05V +/- 3%
120mA
(See NV DG)
N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
N11P GS: 71.0N11P.E0U
Wistron Corporation
GPU_PCIE/STRAPPING(1/5)
JE40-HR
-1
http://hobi-elektronika.blogspot.com/

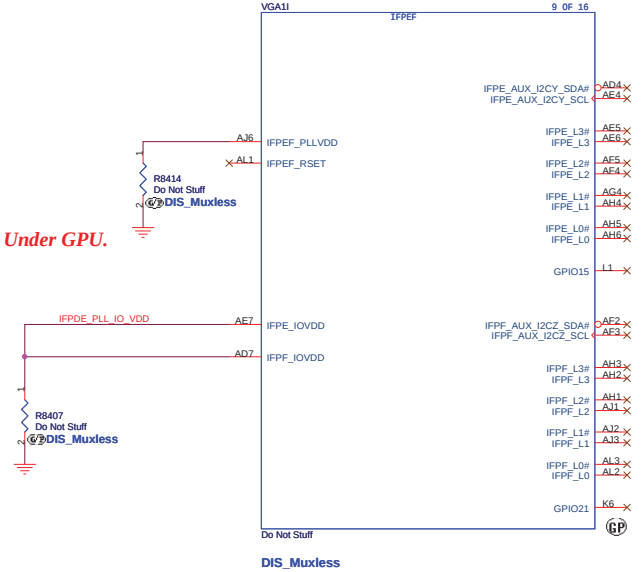
LVDS Interface



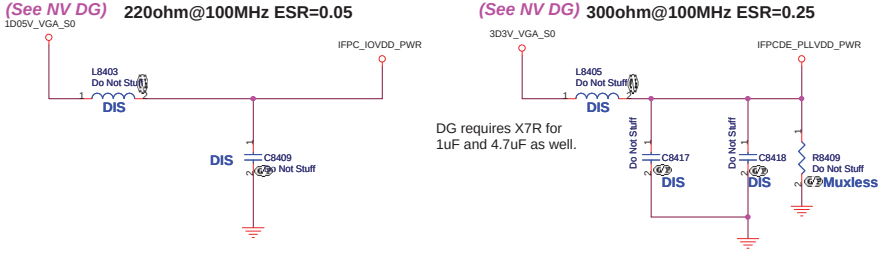


SB modify connector to IFPCDE_PLLVDD_PWR





HDMI Interface



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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size	Document Number	Rev
Custom	JE40-HR	-1

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EDP 10A

DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz

X7R, Under GPU.

X7R, Near GPU.

1.05V +/- 3%
200mA
(See NV DG)

X7R, Under GPU.

FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

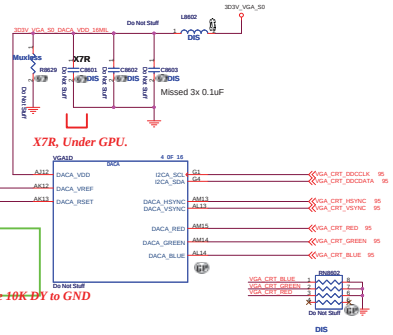
Group A

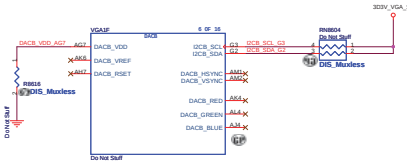
Group B

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU_DP/LVDS/CRT/GPIO(3/5)
Size / Document Number / Rev	Custom / JE40-HR / -1
Date: Thursday, December 02, 2010	Sheet 85 of 102

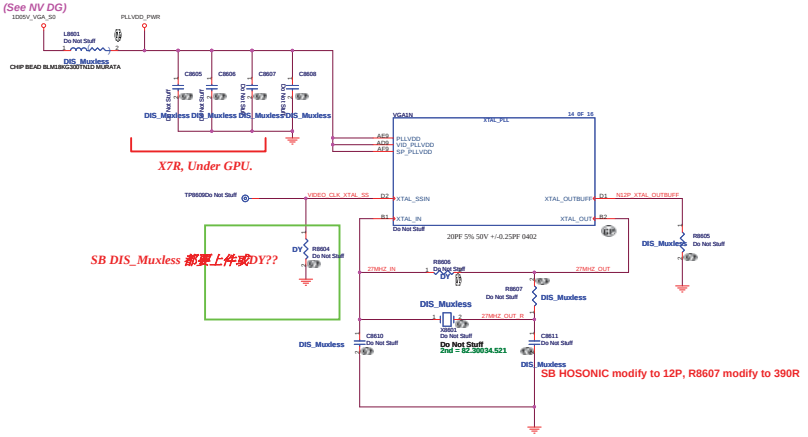
300ohm@100MHz ESR=0.25ohm

3.3V +/- 5%
120mA
(See NV DG)

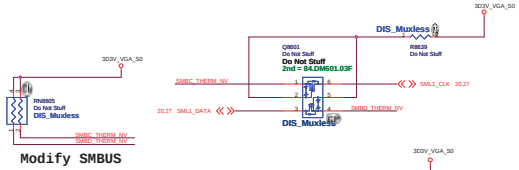


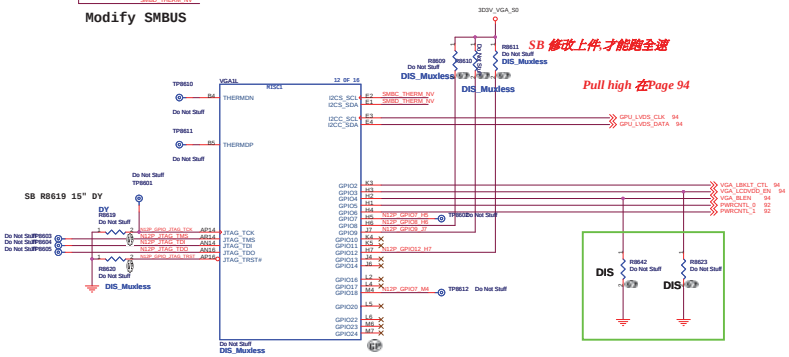


1.05V +/- 3%
150mA
(See NV DG)



VGA Thermal sensor P2800

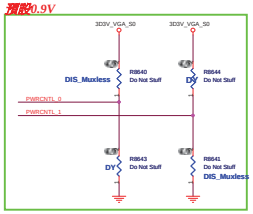




SJM50-CP SUPPORT

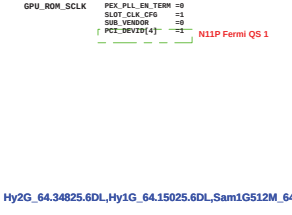
P-STATE	NVVDD_ALTV1	NVVDD_ALTV0	N11M-GE1	N11M-GE2	N11M-OP1	N11P-GE1	N11P-GE Fermi
P12	0	0	0.85V	0.85V	0.85V	0.80V	0.85V
P8	0	1	0.85V	0.85V	0.85V	0.85V	0.9V
P0	1	0	1.02V	1.02V	1.02V	0.95V	0.95V

預設0.9V



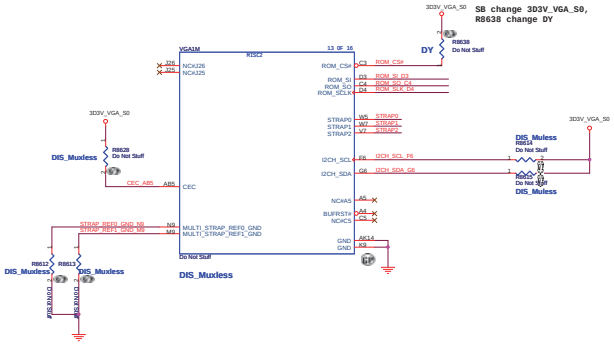
NVIDIA TABLE

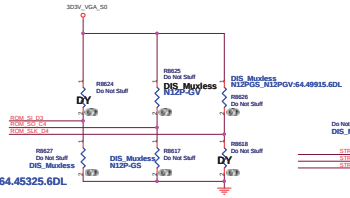
	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL



Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111





Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL,Sam2G_64.45325.6DL

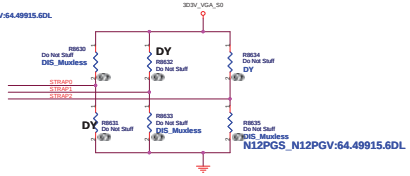


TABLE NVIDIA 71.0N12P.E0U

-1 modify N12P GV setting 71.0N12P.A0U

	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

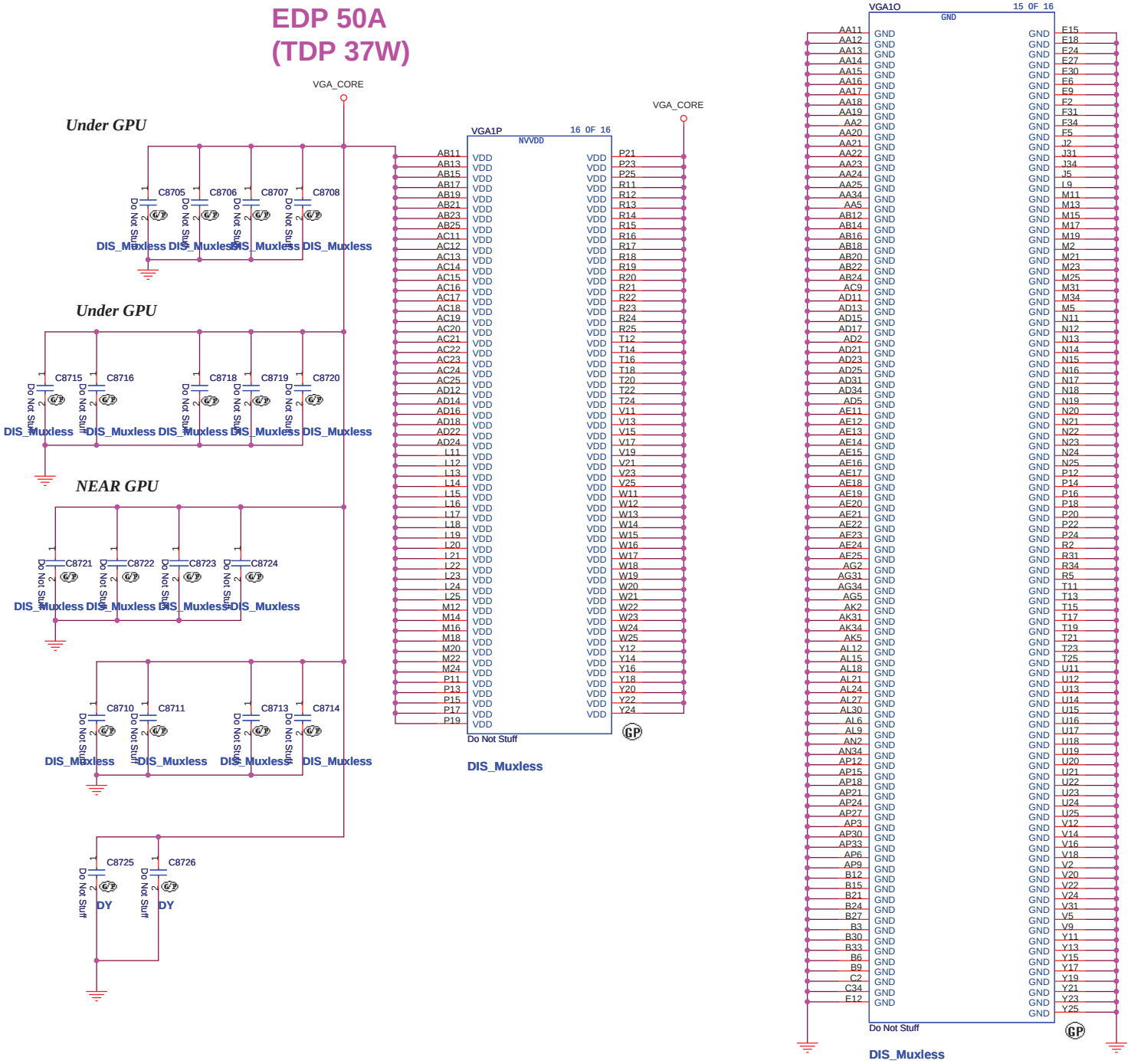
STRAP0 USER[0]=1 USER[1]=1 USER[2]=1 USER[3]=1 — N12P-GS USE 1111 (45K) — N12P-GV — N11P-GE Pull Low — N11P-GS Pull Low — N12P-GE

STRAP1 3GIO_PADCFG[0]=0 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1 — USE 0110 (35K)

STRAP2 PCI_DEVID[0]=1 PCI_DEVID[1]=0 PCI_DEVID[2]=0 PCI_DEVID[3]=0
N12P-GS GF108-730-A1 0x0DF4 (0X4) (0100)
N12P-GV1 GF108-705-A1 0x0DF7 (0X7) (0111)
N11P-GS Fermi 0x0DF0 (0000)
N11P-GE Fermi 0x0DF1 (0001)

Wistron Corporation
GPU_POWER(4/5)
JE40-HR
-1
Thursday, December 09, 2010

EDP 50A
(TDP 37W)



HR UMA

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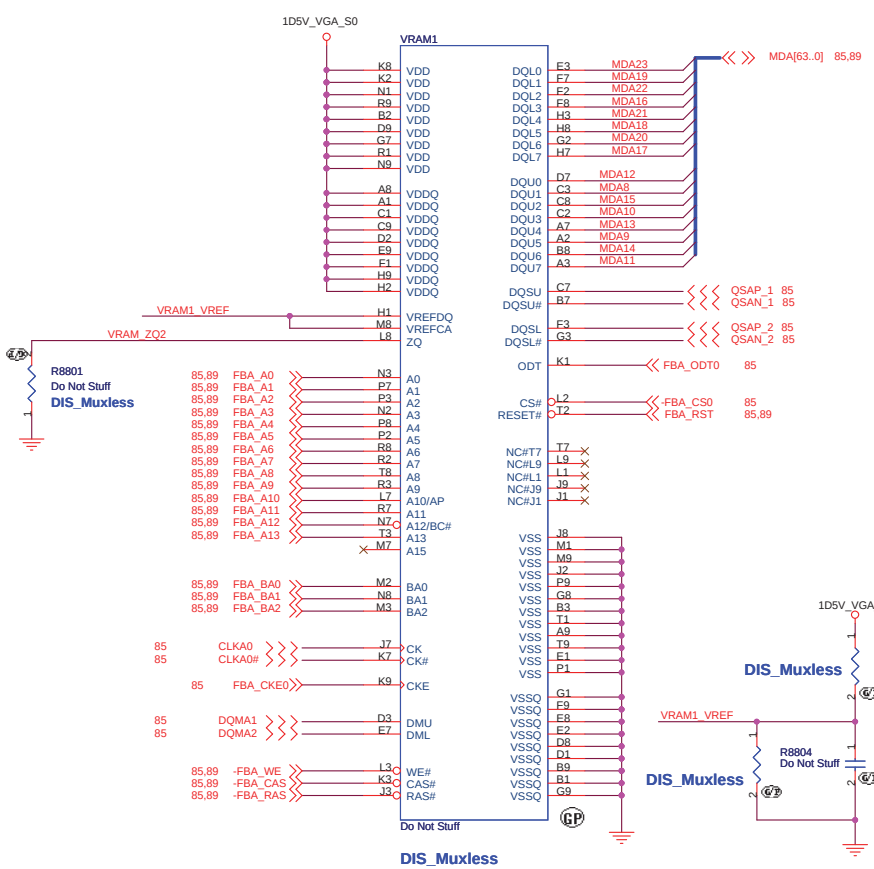
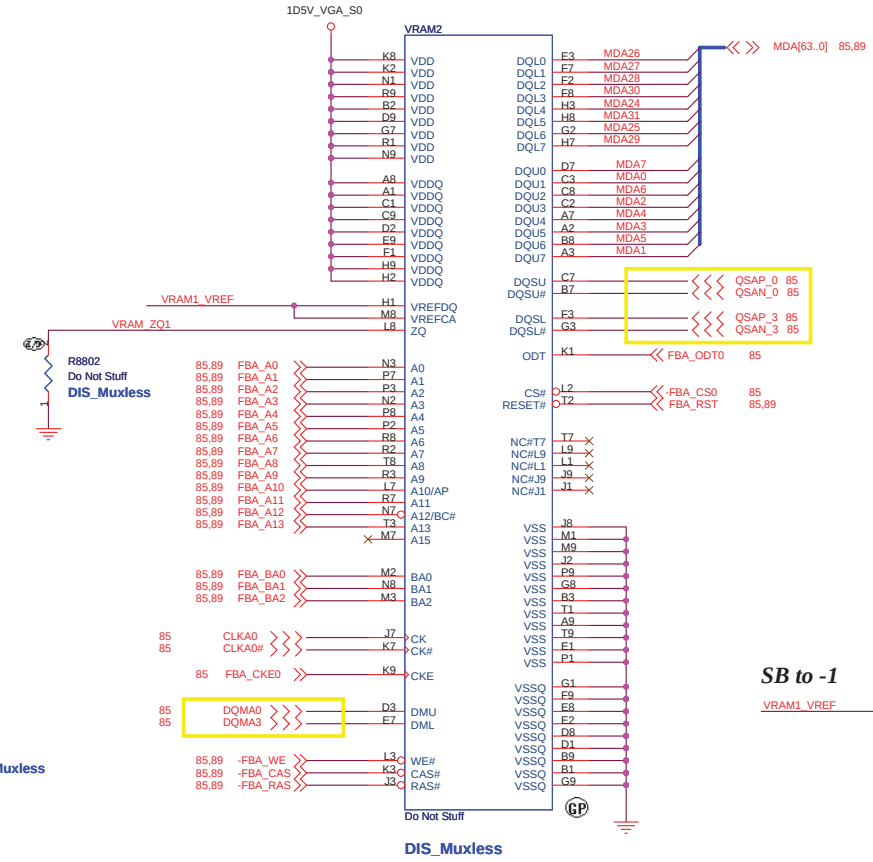
Title: GPU_DPPWR/GND(5/5)	
Size: A3	Document Number: JE40-HR
Rev: -1	
Date: Thursday, December 02, 2010	Sheet 87 of 102



DIS_Muxless

VRAM = N12PGS_N12PGV

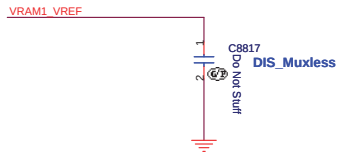


DIS_Muxless

VRAM = N12PGS_N12PGV

FB CMD mapping Mode D-N12x

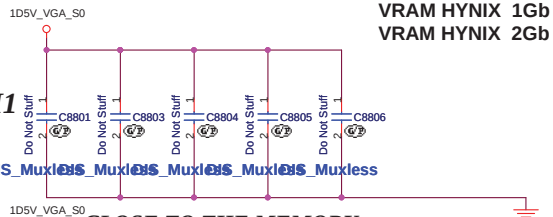
SB to -1



VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

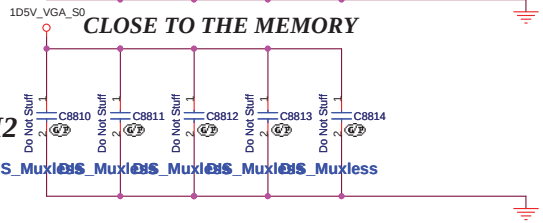
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

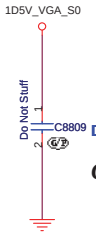
FOR VRAM1



CLOSE TO THE MEMORY

FOR VRAM2





CLOSE TO THE MEMORY

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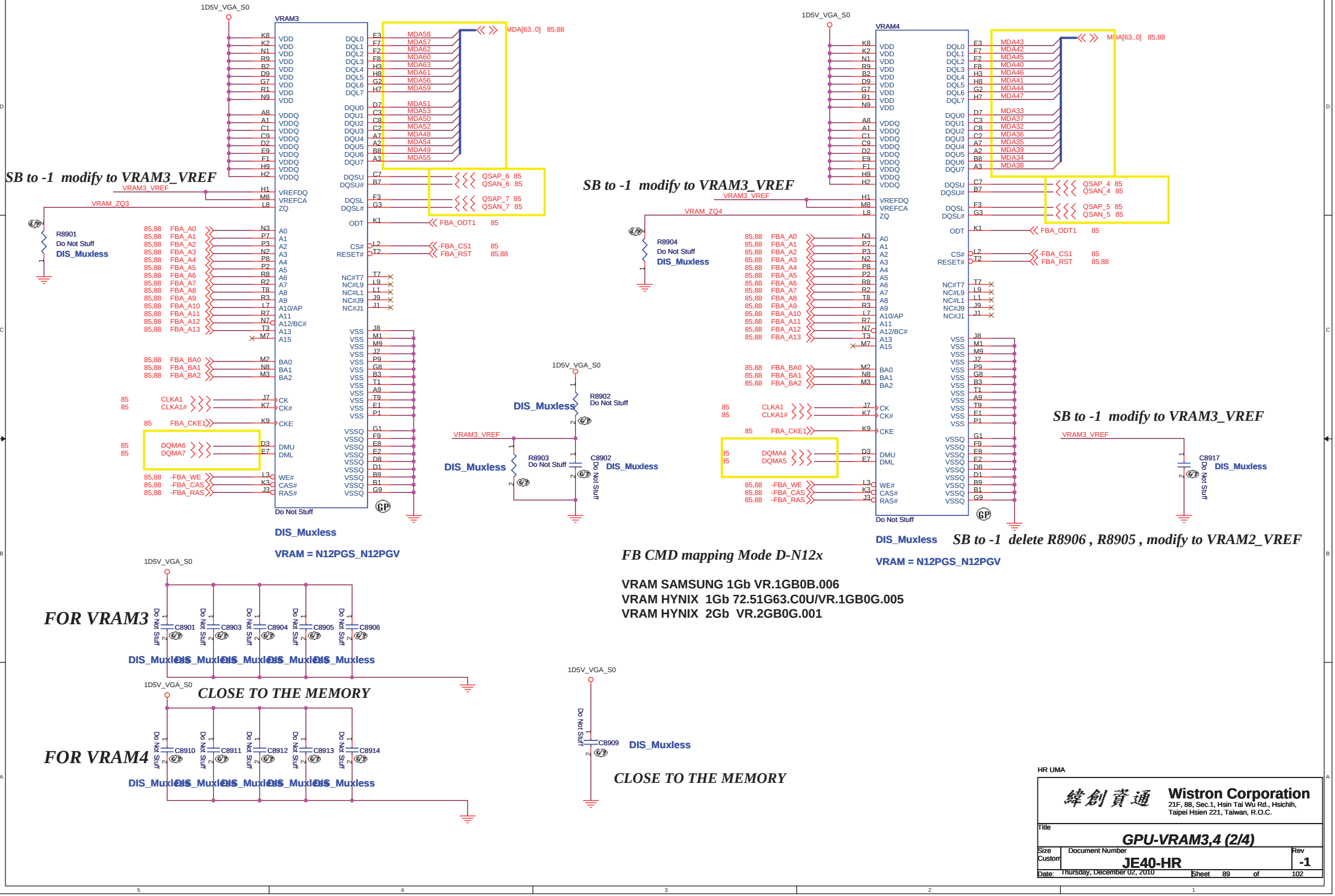
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM1,2 (1/4)***

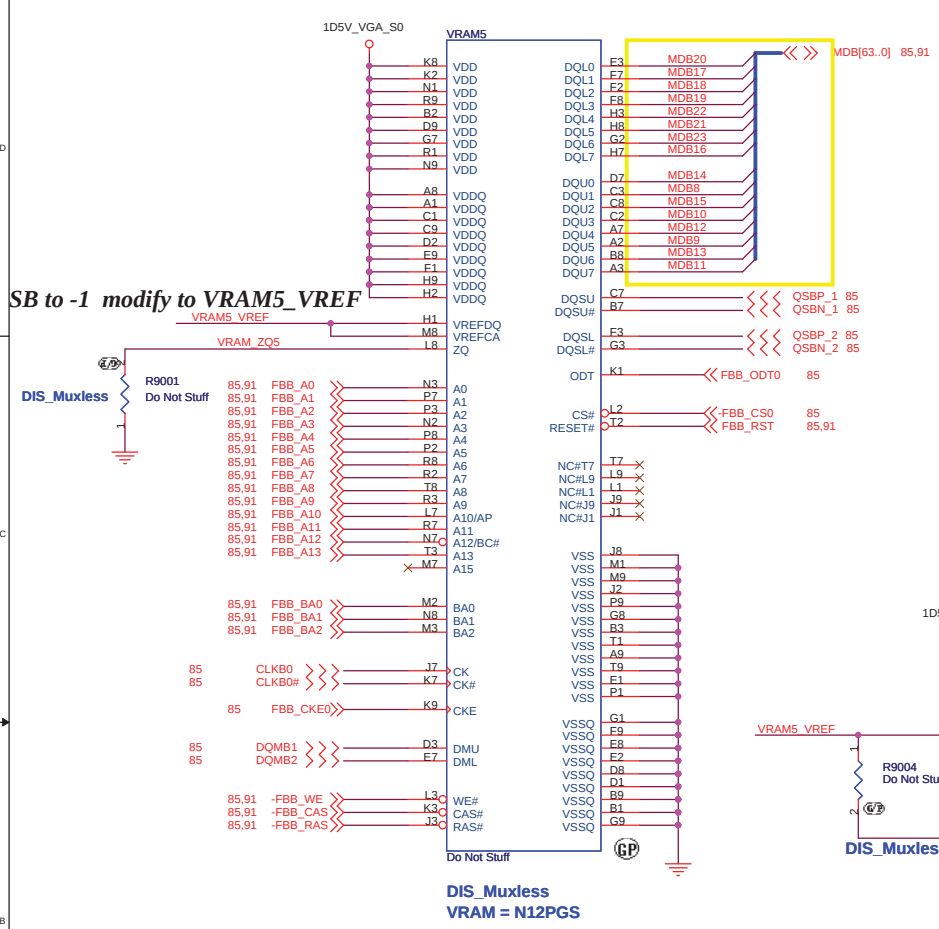
Size: Custom | Document Number: **JE40-HR** | Rev: **-1**

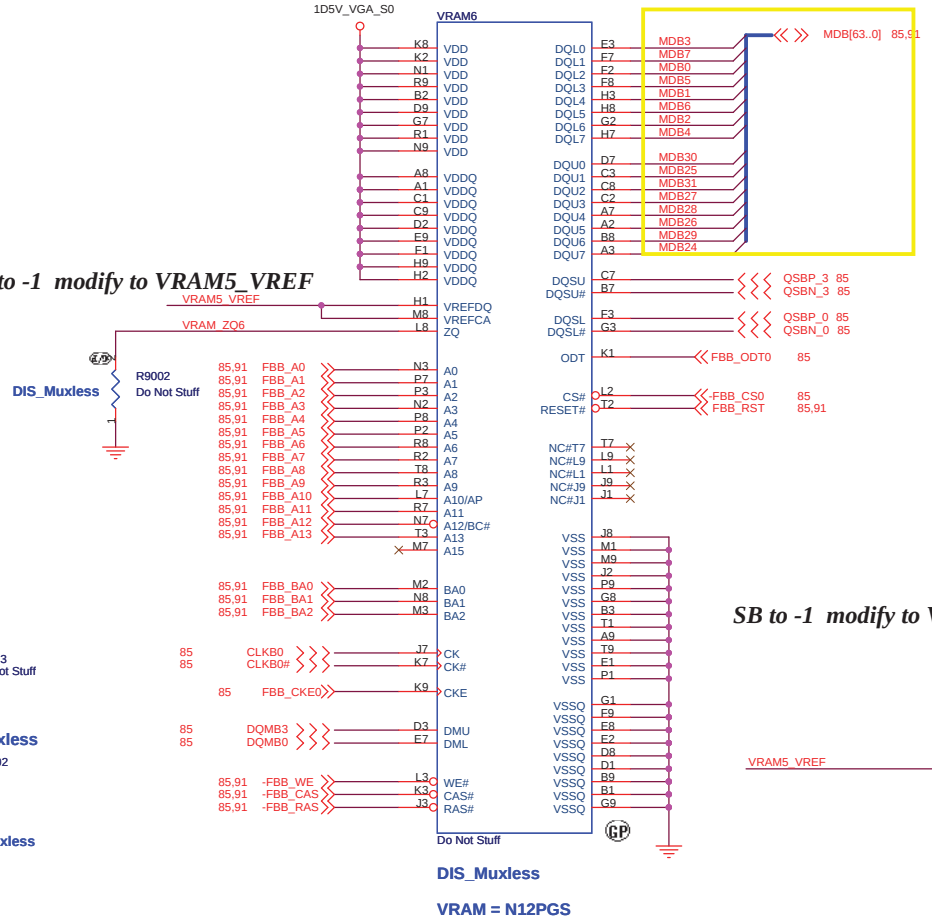
Date: Thursday, December 02, 2010 | Sheet 88 of 102



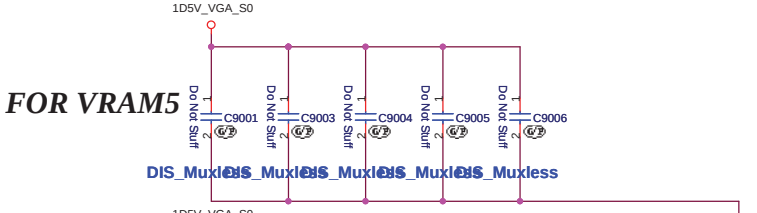
HR UMA

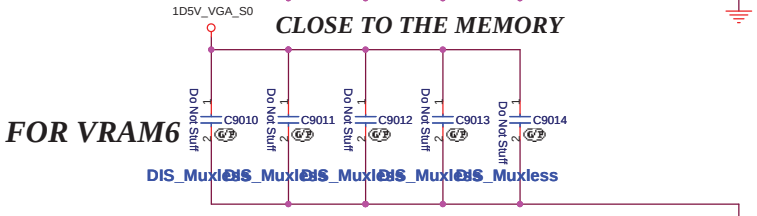
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**GPU-VRAM3,4 (2/4)**	
Size: Custom	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 89 of 102	



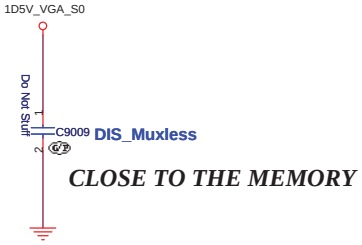


VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001





DG requires 4x0.1uF and 8x1.0uF per VRAM chip



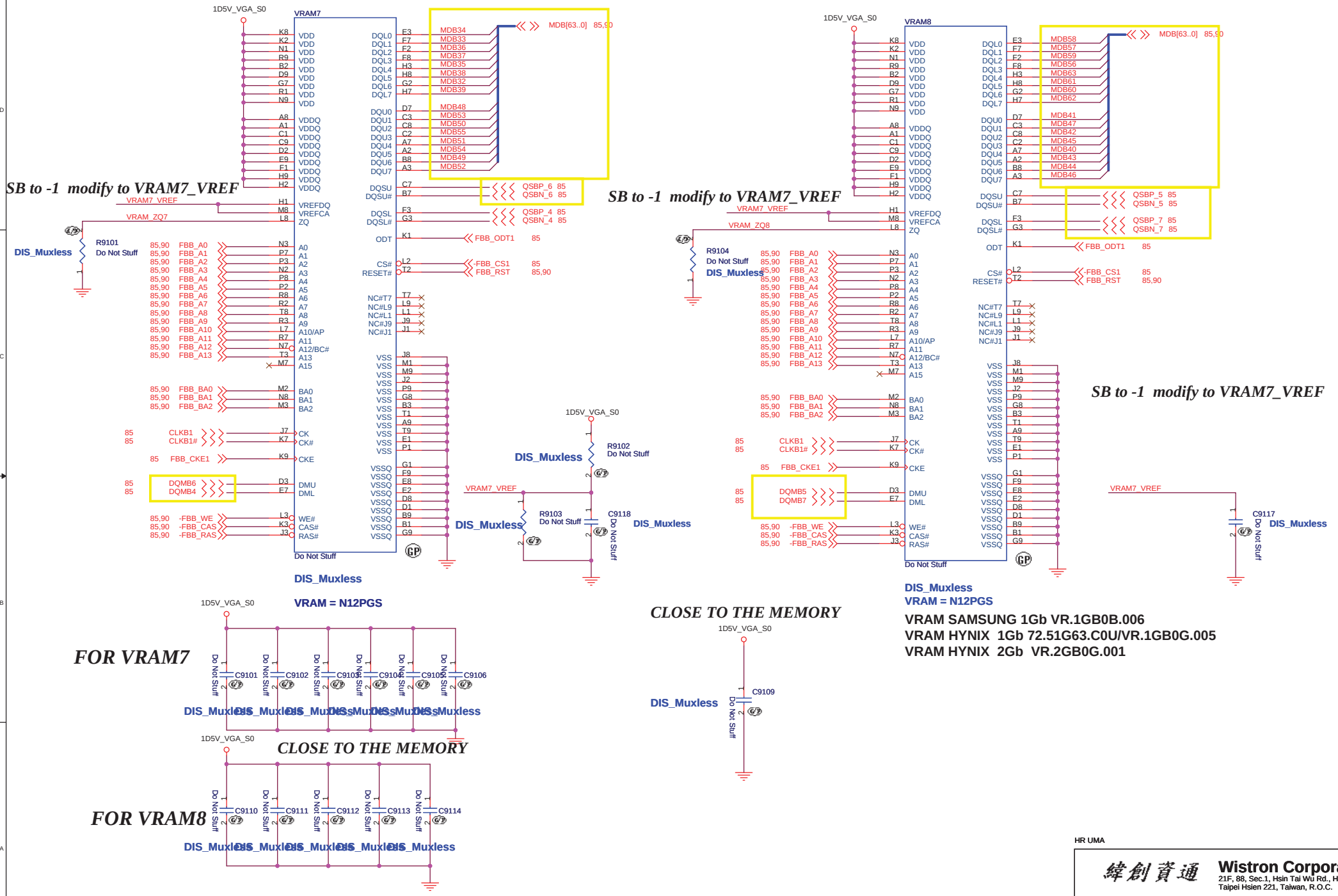
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 90 of 102



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU-VRAM7,8 (4/4)	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 91 of 102	

SSID = PWR.Plane.Regulator_GFX

20100715

20100719

SB 20100831

SB 20100831

RT8208A

N12P GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.00V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

Vout=0.75V*(R1+R2)/R2

SB to -1 modify PR9213 VGA_Core to 1.05V

N12P GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

HR UMA

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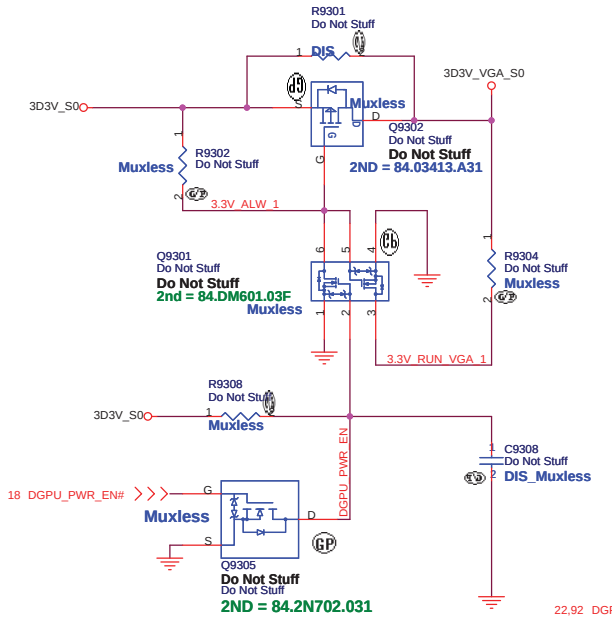
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VGA_CORE

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 92 of 102

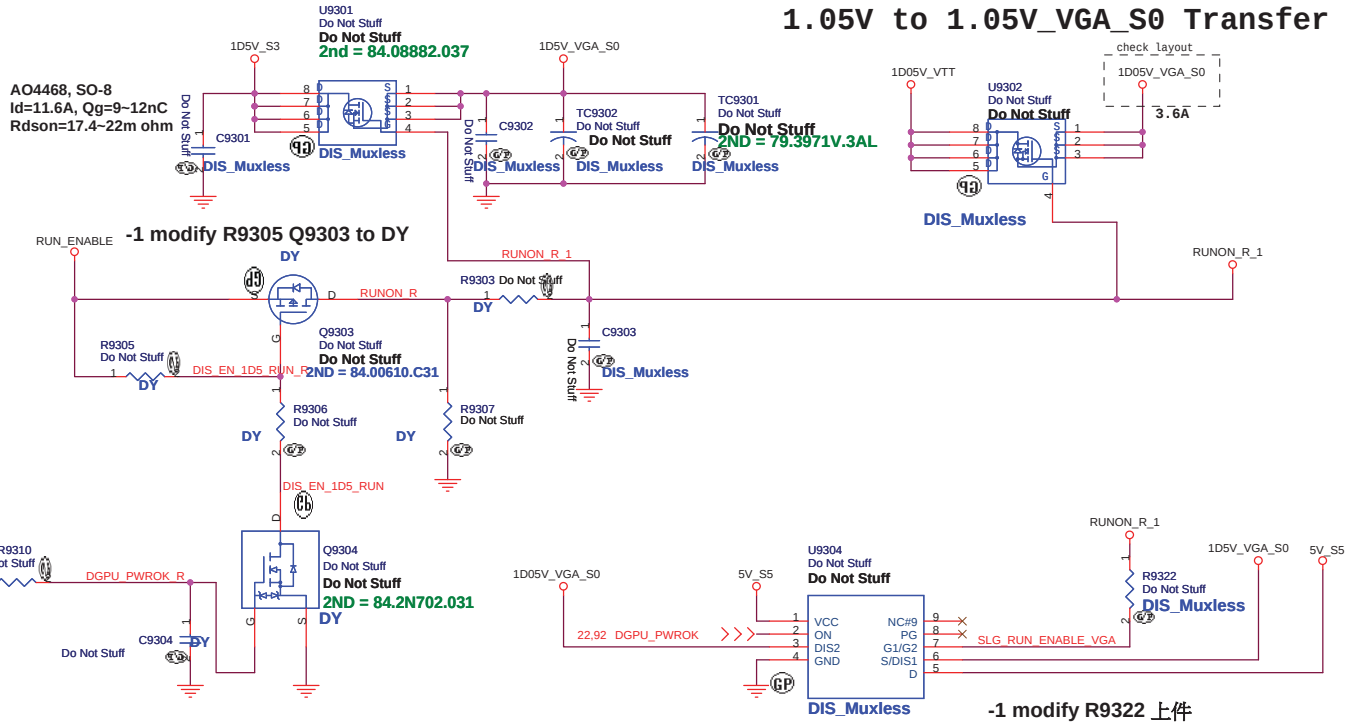
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

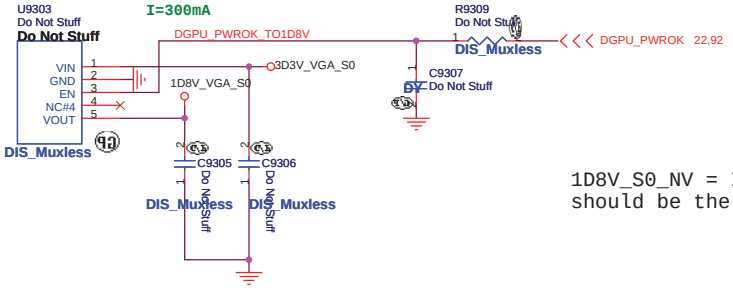
SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer



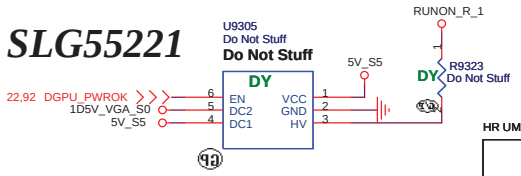
RT9025 for 1D8V_VGA

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

-1 co-layout SLG55221



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DISCRETE VGA POWER		
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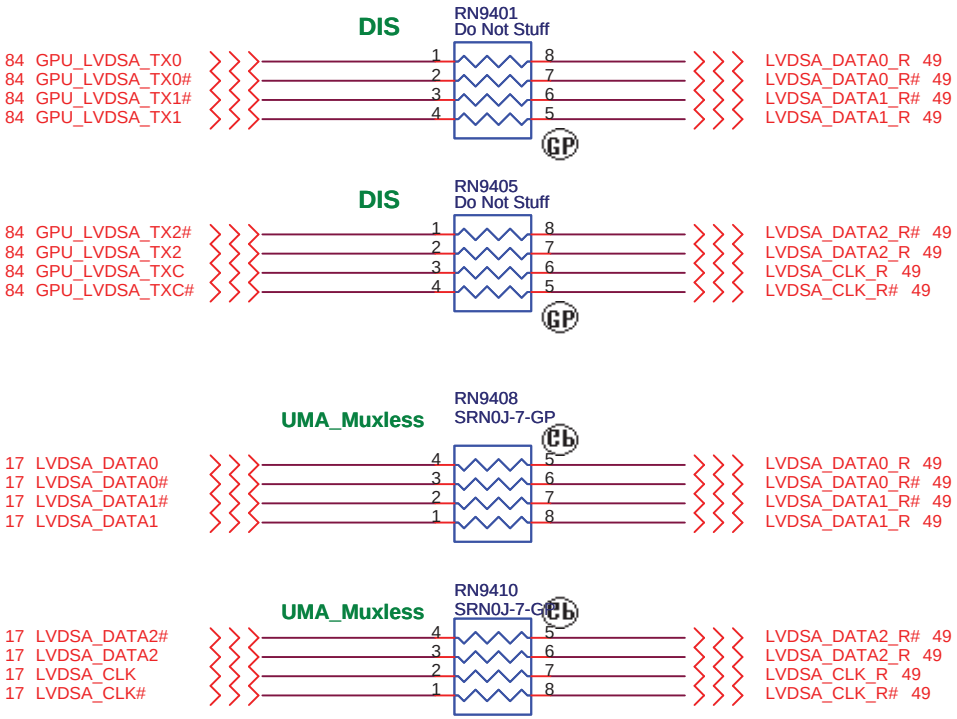
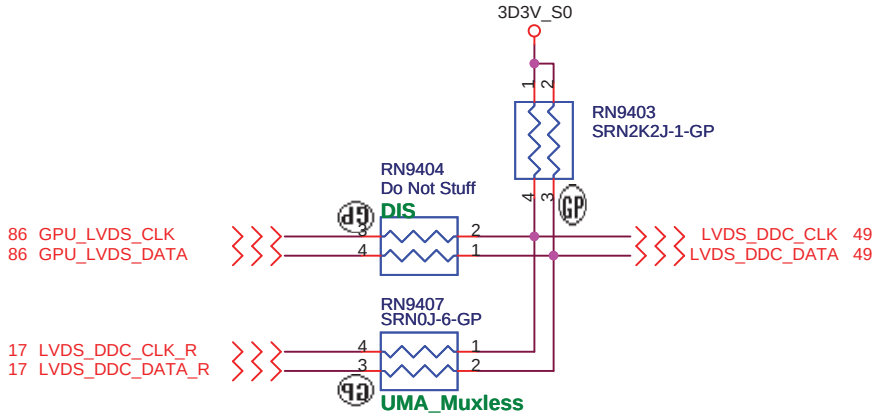
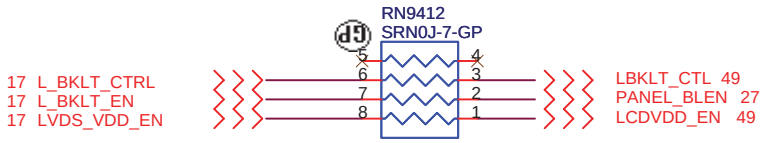
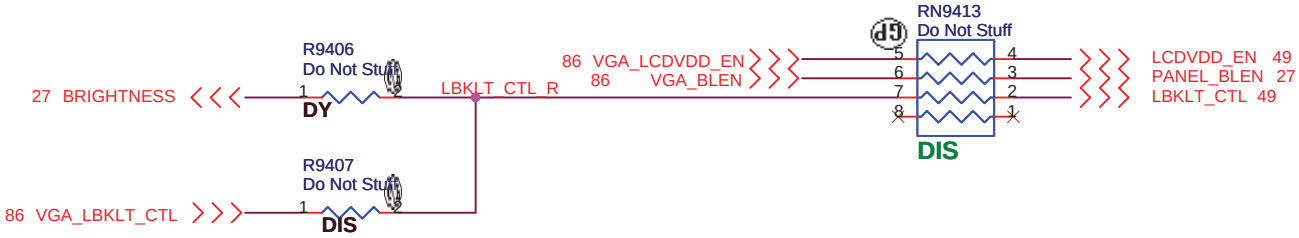
LVDS Channel A





Panel BL brightness/Power En/BL En





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Title: *LVDS_Switch*

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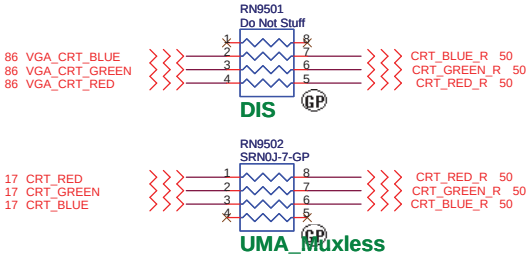
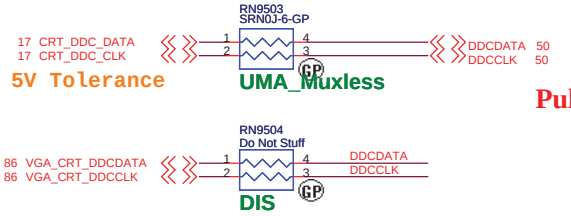
Close to CRT Board CONN

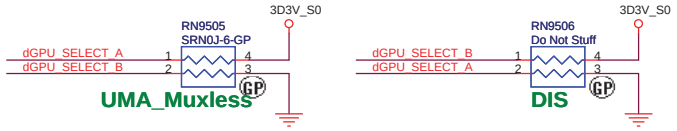


CRT DDCDATA & DDCCLK



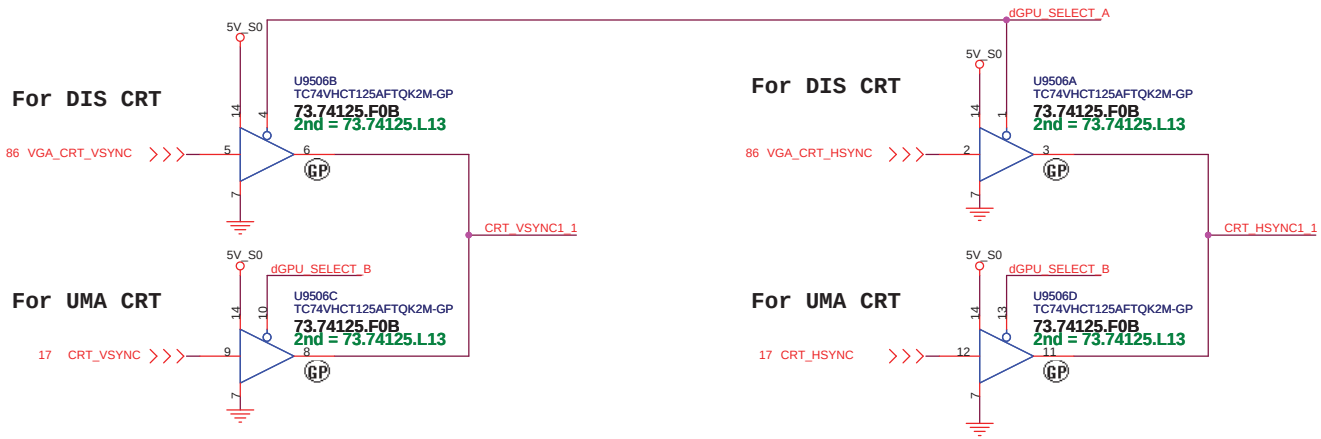
Pull high 在CRT

SB to -1 modify 4 port Logic



CRT Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA



SB to -1 modify R9503,R9504 to 10 ohm

HR UMA

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Title: CRT Switch

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SSID = SDIO

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Title: ***TOUCH PANEL***

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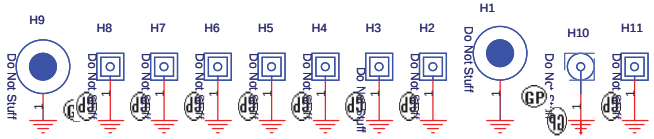
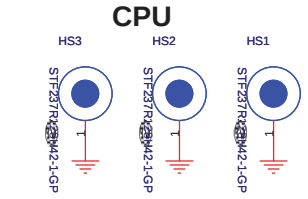
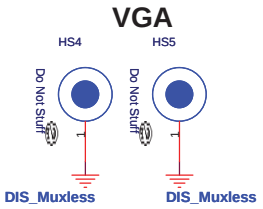
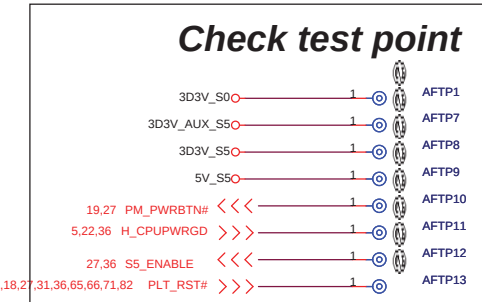


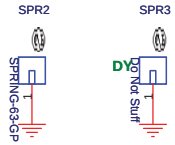




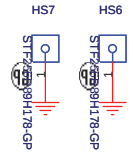


SB to -1 BOM add SPR2

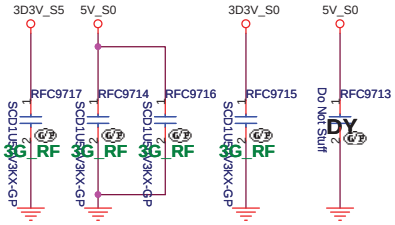
-2 delete SPR5

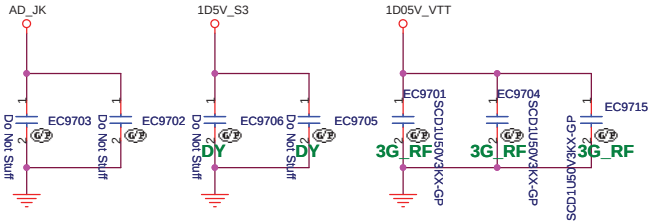


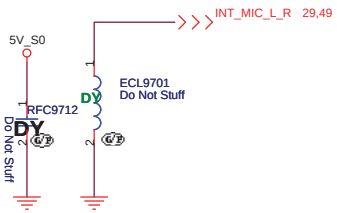
Change:34.40V16.001

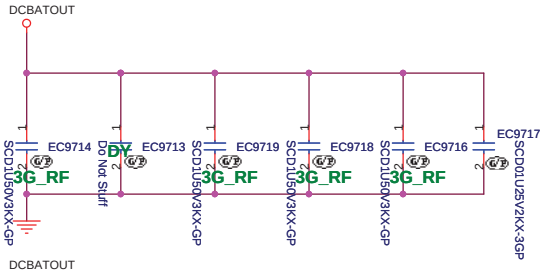


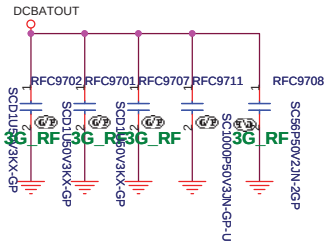
3G Sku

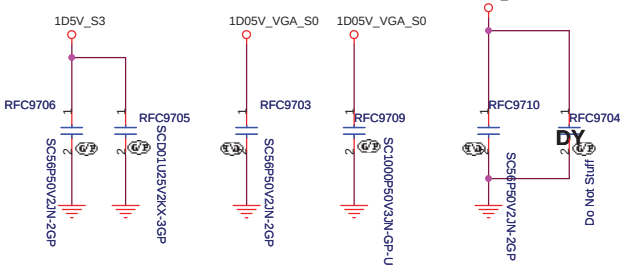


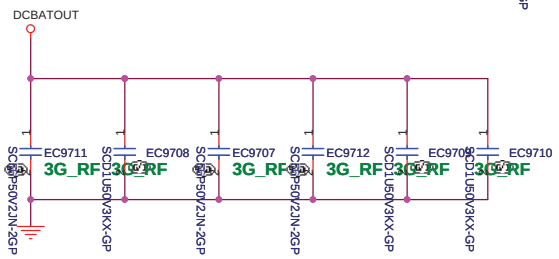












HR UMA

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Title: ***UNUSED PARTS/EMI Capacitors***

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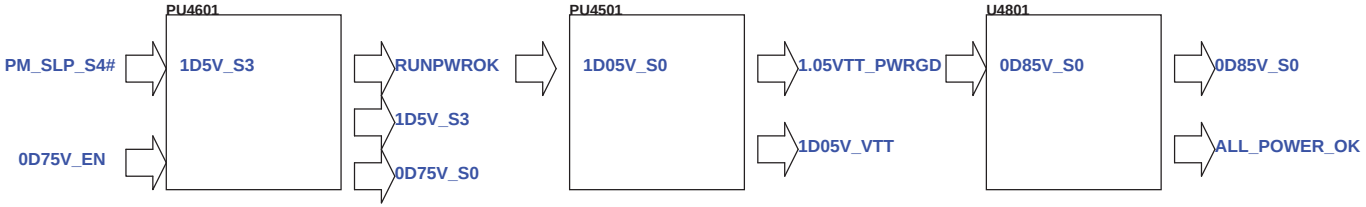
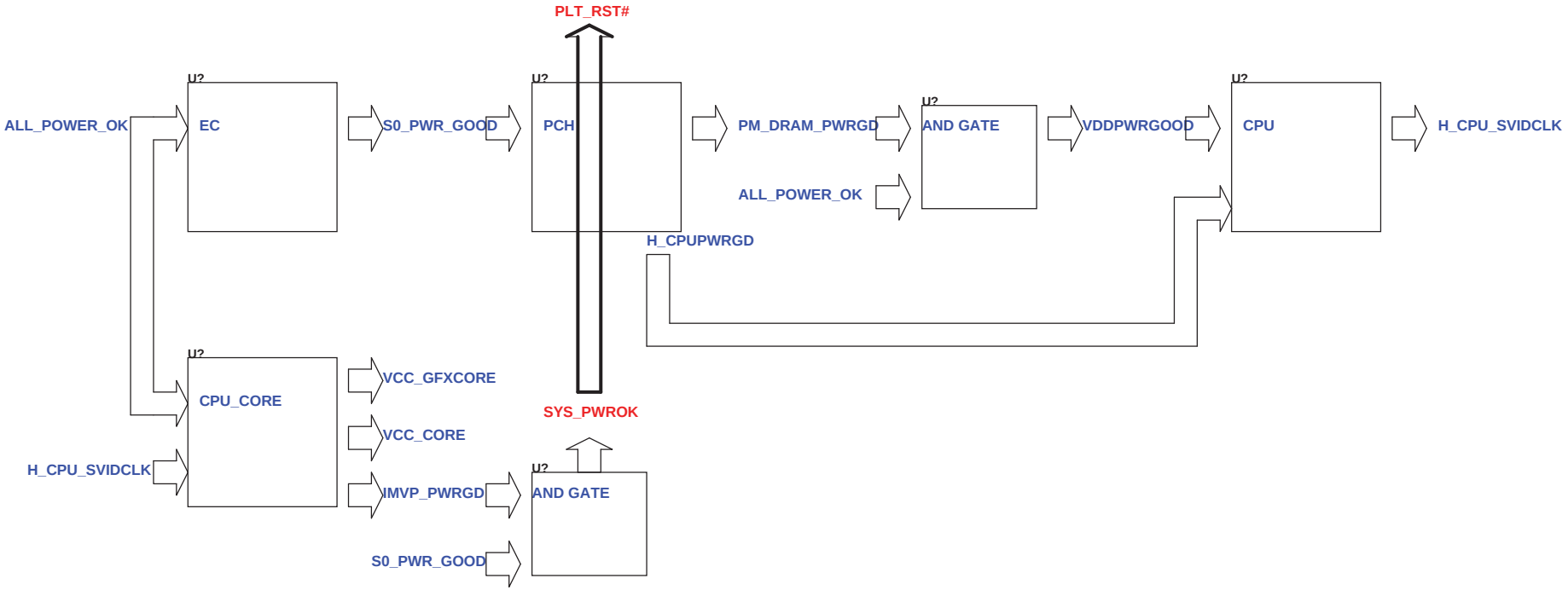
Power Sequence





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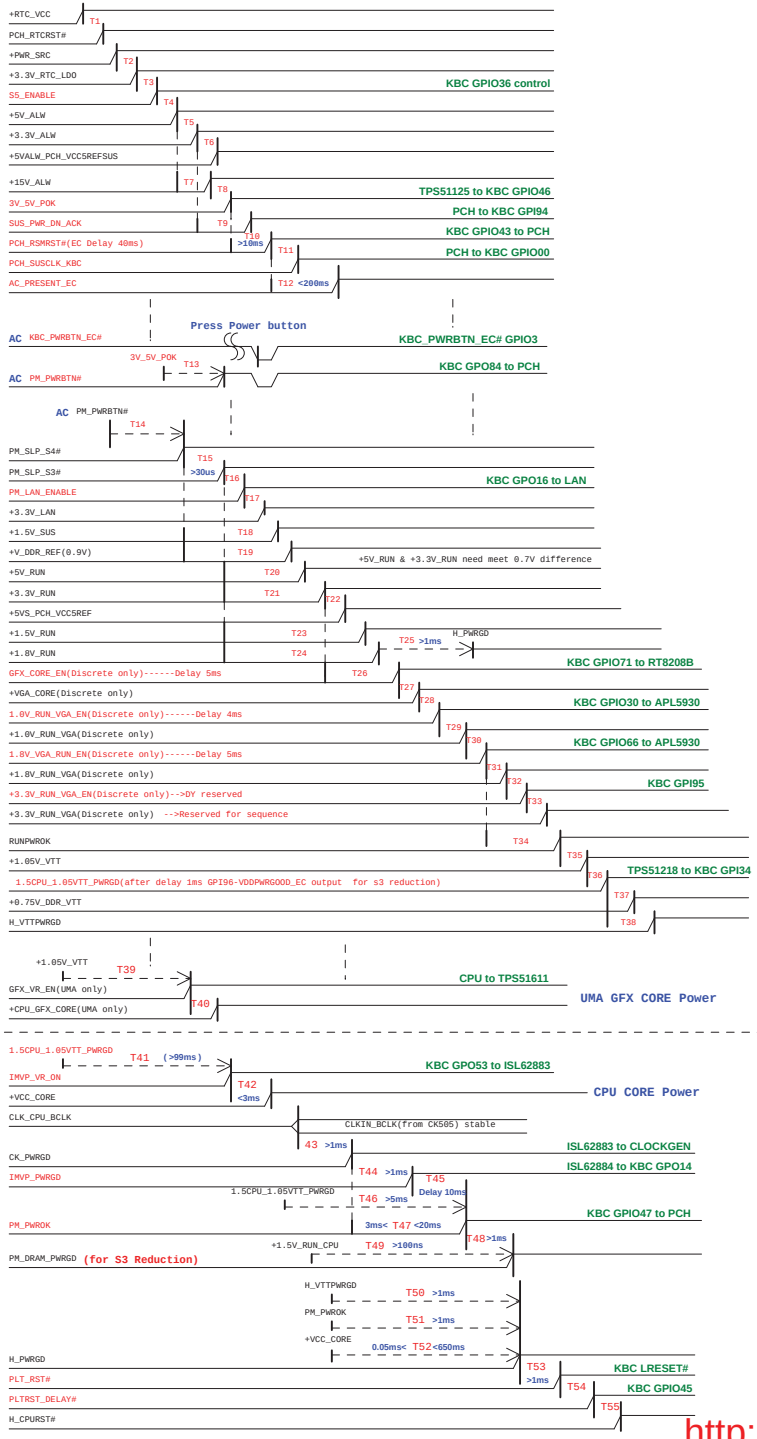
Intel-Power Up Sequence

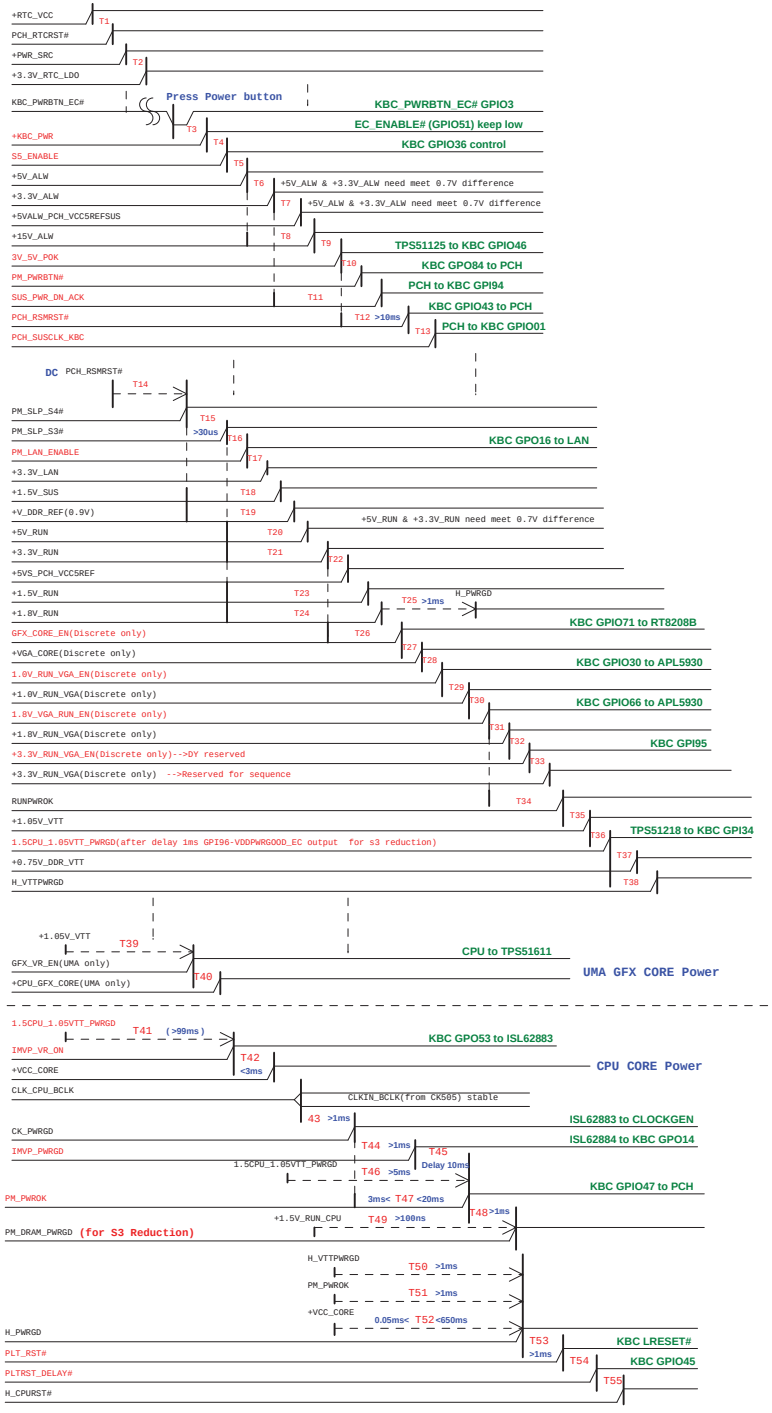
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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Title: Power Sequence

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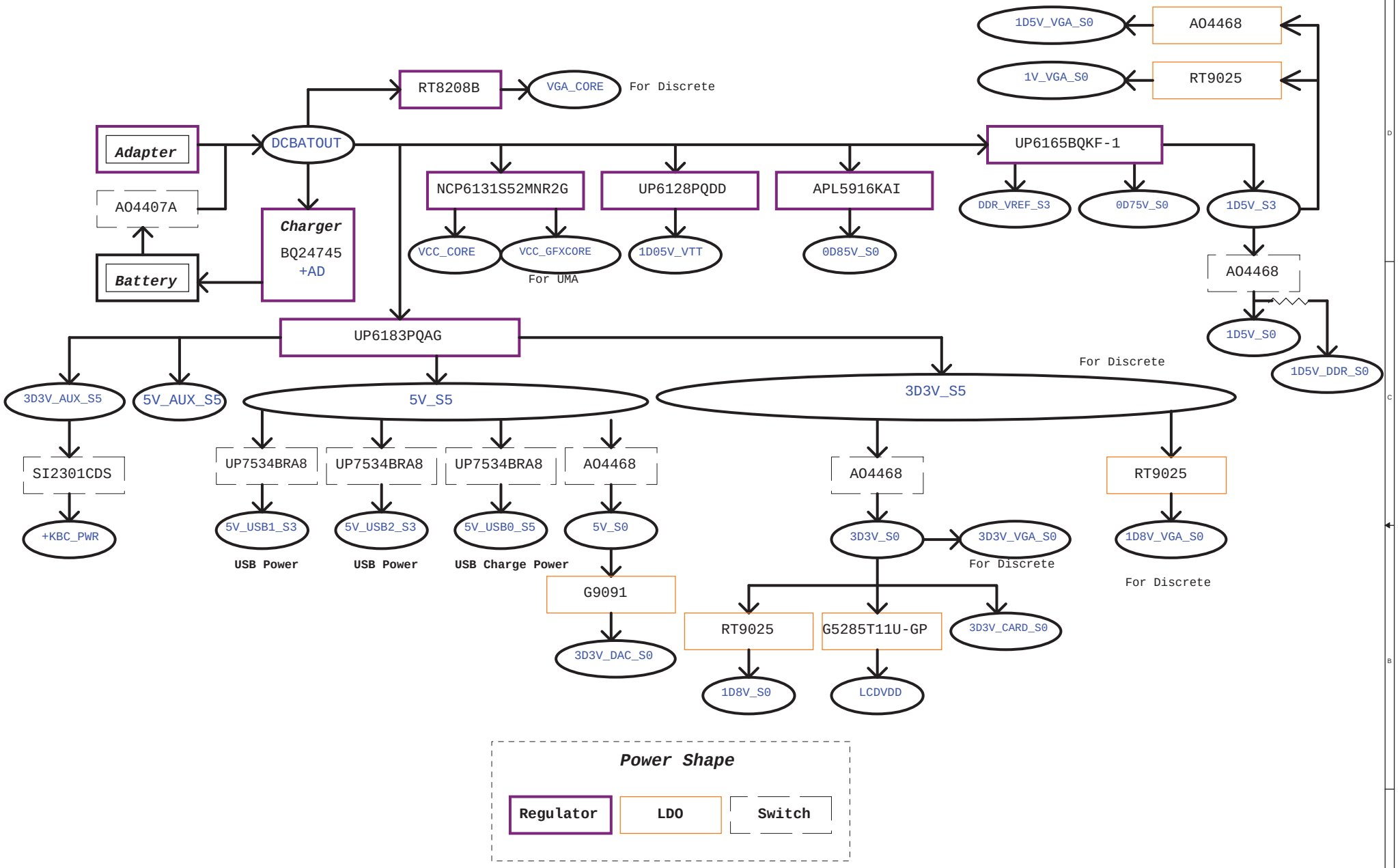

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Title: Power Block Diagram		
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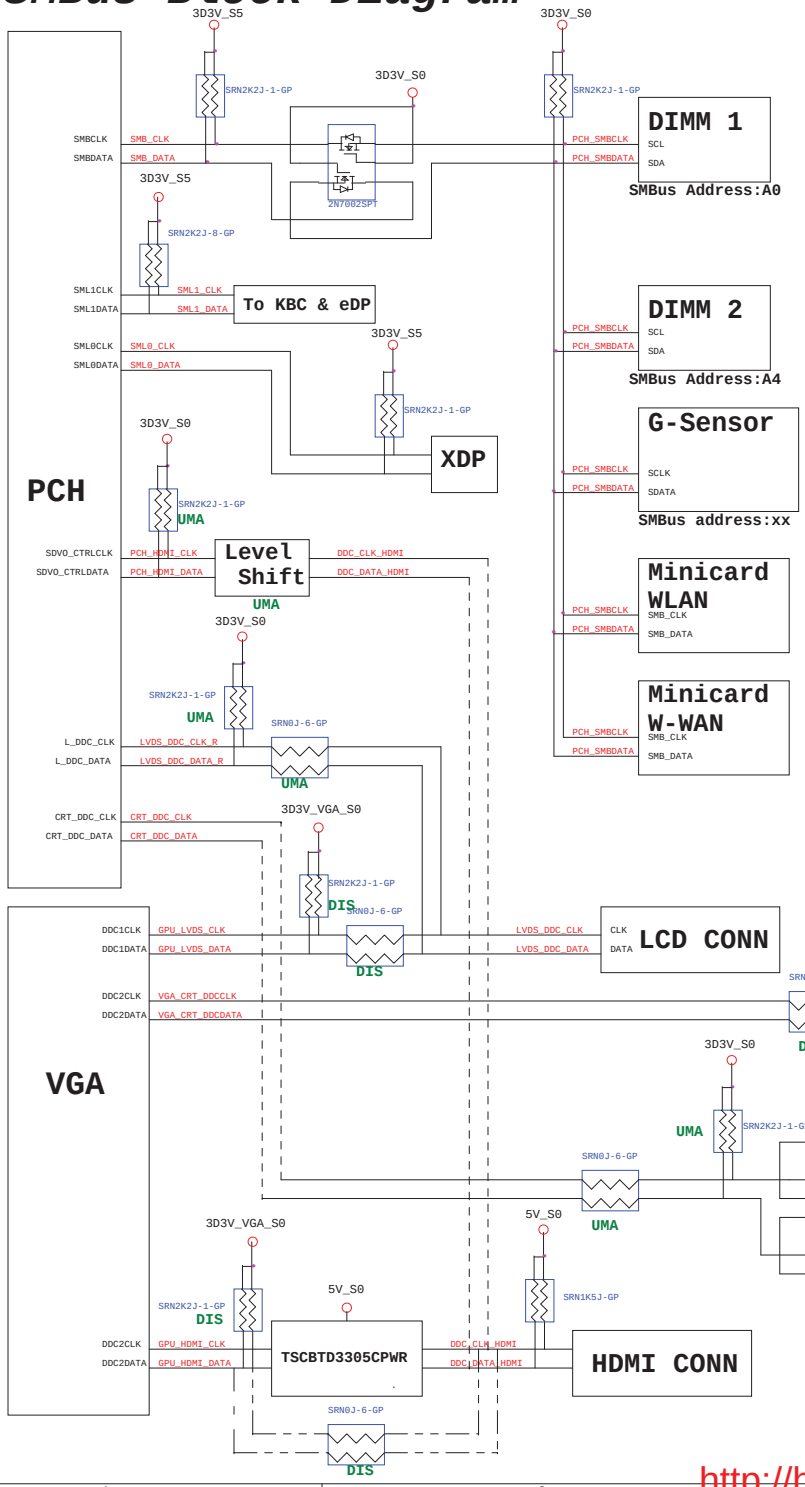
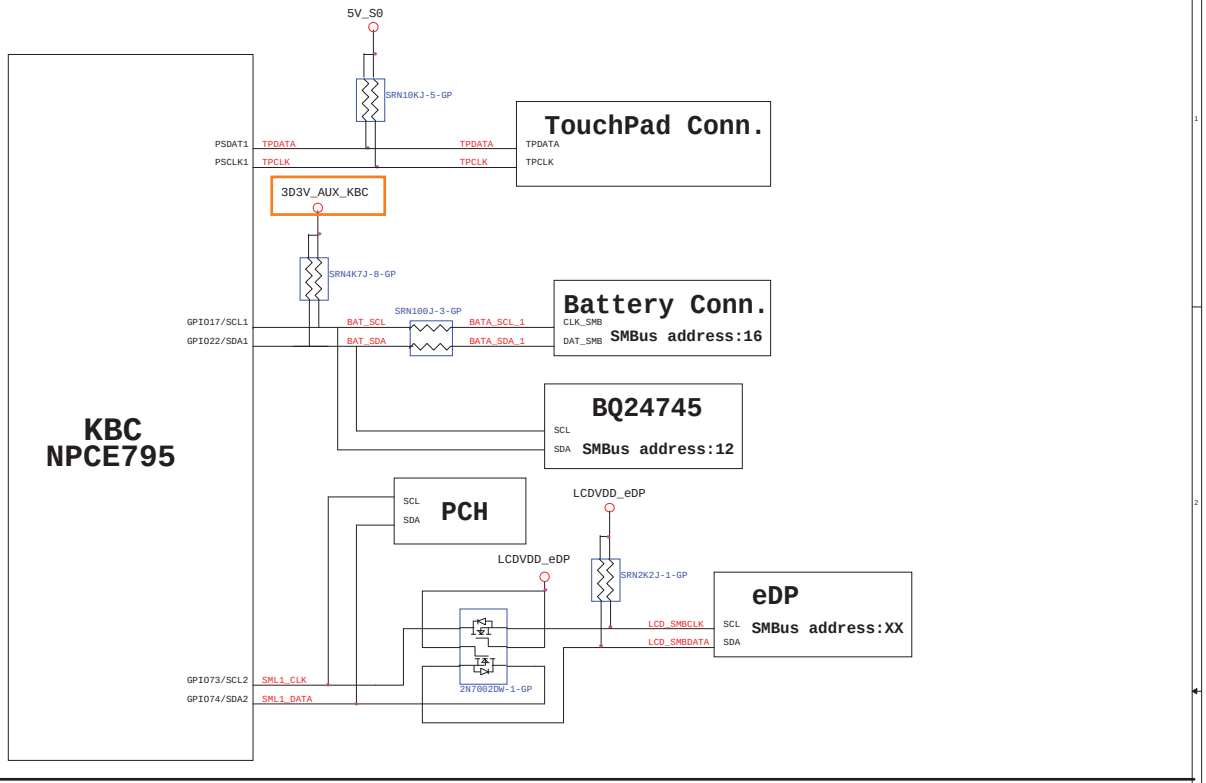
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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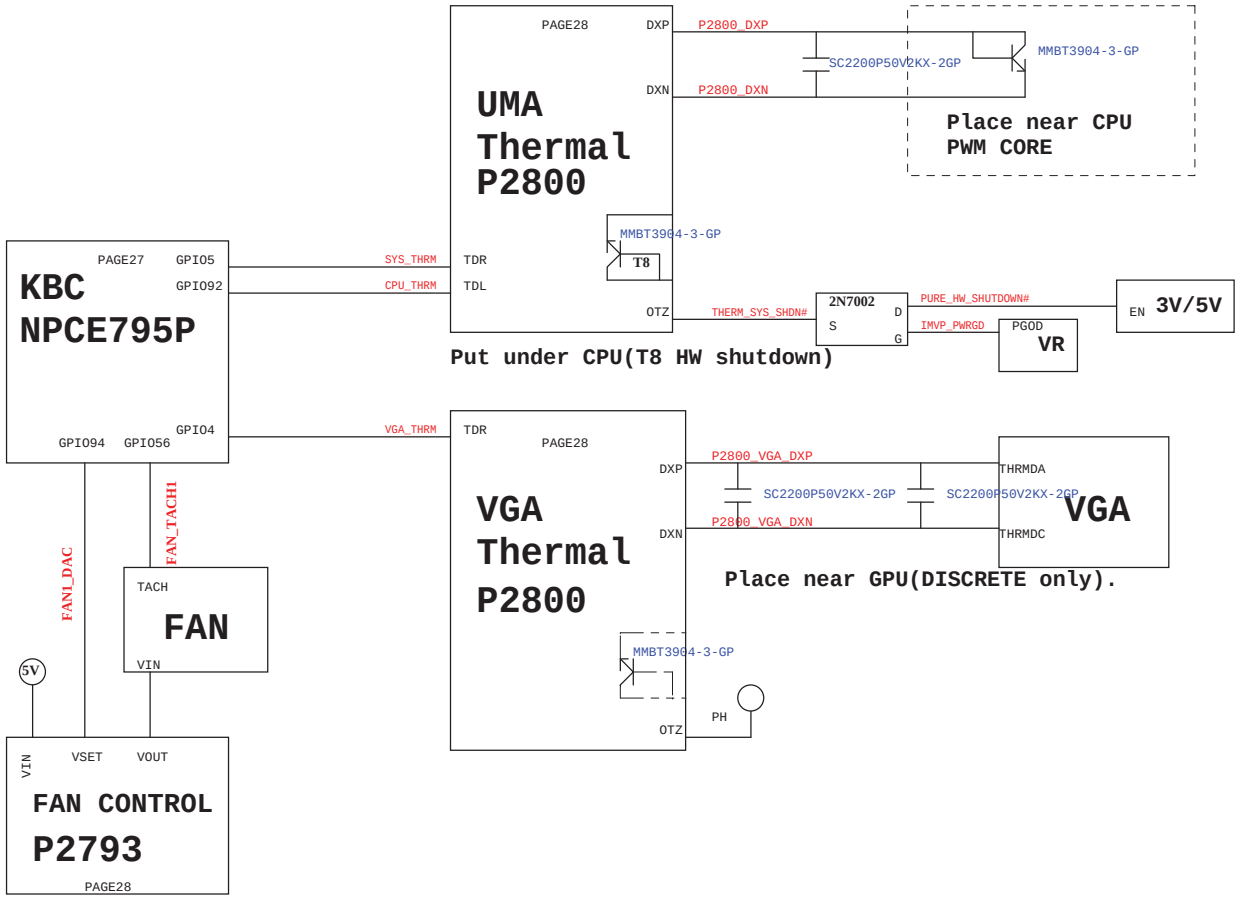
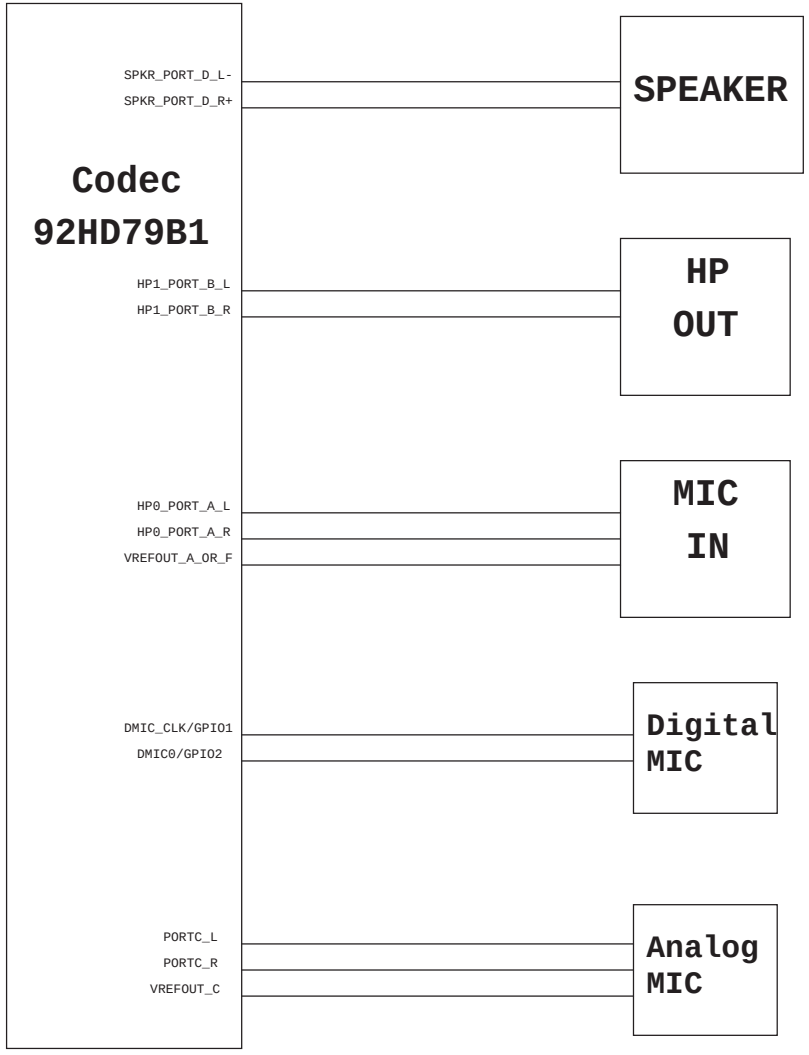
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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