

www.rosefix.com

LCFC Confidential


AMD 2 Chip M/B Schematics Document

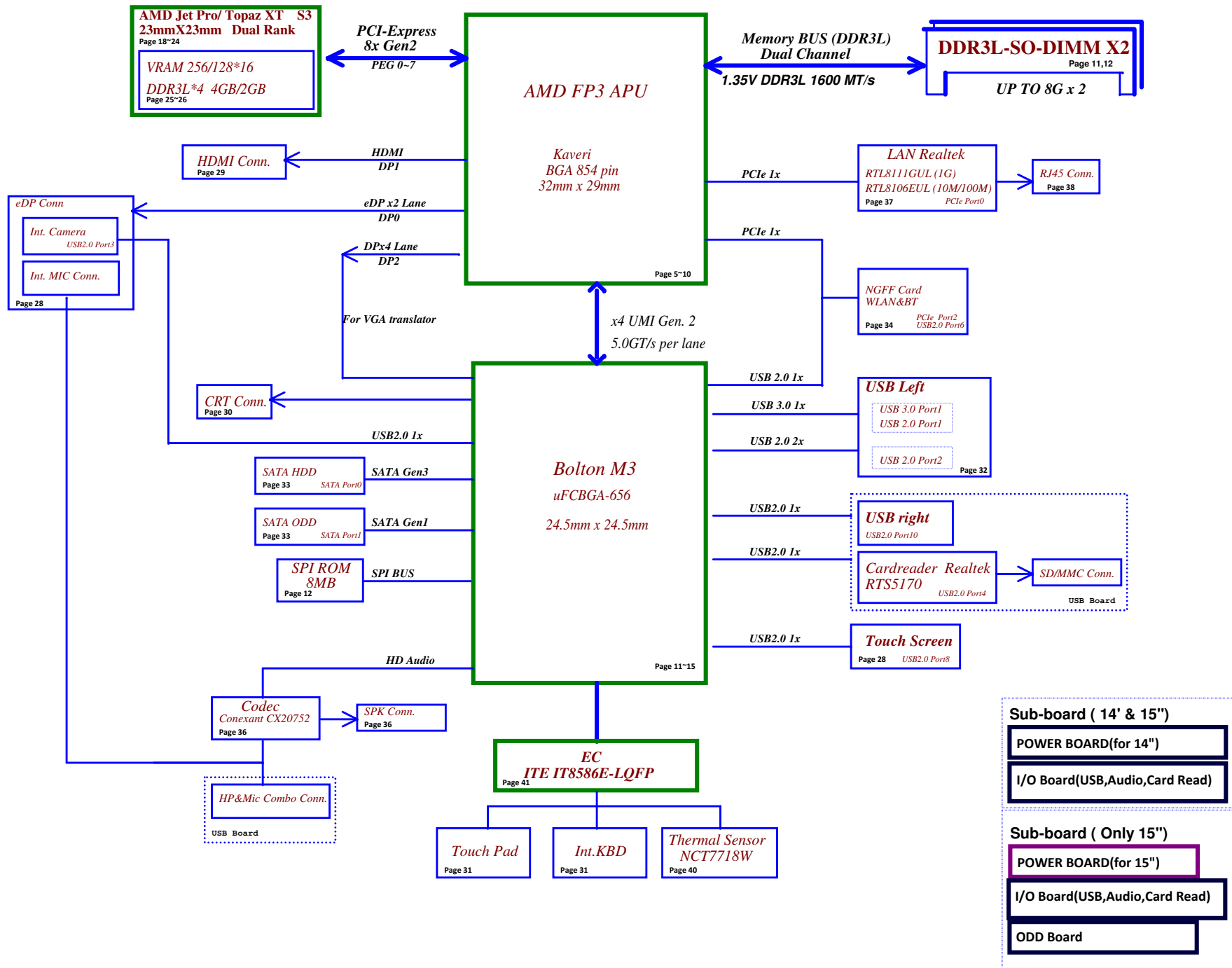
AMD Kaveri Processor with DDRIII + Bolton FCH

AMD GPU JET PRO/TOPAZ XT S3

2013-09-25

REV: 0.1

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/05/17	Deciphered Date	2012/12/21	Cover Page	
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</small>				Size	Rev
				Custom	Document Number
				Date:	Monday, December 16, 2013
				Sheet	1 of 52



- Sub-board (14' & 15")**
 - POWER BOARD(for 14")
 - I/O Board(USB,Audio,Card Read)
- Sub-board (Only 15")**
 - POWER BOARD(for 15")
 - I/O Board(USB,Audio,Card Read)
 - ODD Board

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW	+5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O	
S3	O	O	O	X	
S5 S4/AC Only	O	O	X	X	
S5 S4 Battery only	O	X	X	X	
S5 S4 AC & Battery don't exist	X	X	X	X	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port	
			Camera	
	XHCCI	1	0	
EHCCI1		2	1	USB Port (Right Side)
		3	2	USB Port (Left Side)
		4	3	
	4	4		
		5	USB Port (Right Side)	
		6		
		7		
EHCCI2		8		
		9		
		10	Mini Card(WLAN)	
		11		
		12		
		13	Blue Tooth	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
100M@	100M LAN Part
14@	For 14" part
15@	For 15" part
AOAC@	AOAC support part
GIGA@	GIGA LAN Part
JET@	For AMD Jet GPU part
ME@	ME part(connector, hole)
DIS@	Discrete GPU SKU part
UMA@	UMA SKU part
TS@	For support touch panel sku part
TOPAZ@	For AMD Topaz GPU part
A10@	For APU Kaveri A10(19W)S IC KAVERI
A4@	For APU Kaveri A4(17W)S IC KAVERI
EMC@	EMC components

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	CP Module
EC_SMB_CK1	IT8580E									
EC_SMB_DA1	+3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2	IT8580E									
EC_SMB_DA2	+3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
PM_SMBCLK	PCH									
PM_SMBDATA	+3V_PCH	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIe PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	
5	
6	
7	
8	

EC SM Bus1 address


EC SM Bus2 address

PCH SM Bus address

Device	Address
Smart Battery	0001 011X b

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

Security Classification	LC Future Center Secret Data		Title Notes List	
Issued Date	2012/12/05	Deciphered Date		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				
Size	Document Number	Date		Rev
Custm	ACLU7	Monday, December 16, 2013		04
Sheet 3 of 52				

Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.

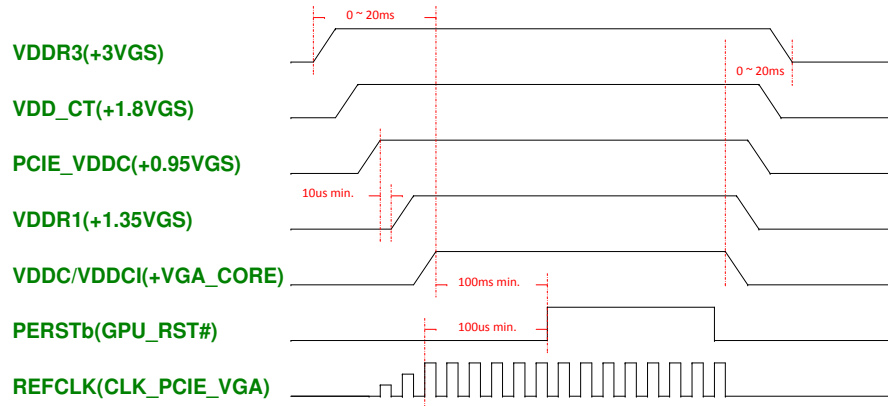
It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μs before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU.

The gate circuits must meet the slew rate requirement (such as 50 mV/μs).

For power down, reversing the ramp-up sequence is recommended.



CONFIGURATION STRAPS



ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

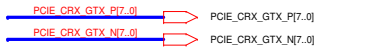
RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 10K RESISTOR
 X= DESIGN DEPENDANT
 NA= NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory aperture size when STRAP_BIOS_ROM_EN = 0. 100 = 256MB	X
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 0= Not support	X
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKRECB power management capability is disabled 1 = The CLKRECB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	X
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved.	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 000 = Hynix 256M*16 001 = Hynix 128M*16 100 = Samsung 256M*16 011 = Samsung 128M*16 010 = Micron 256M*16 111 = Micron 128M*16	X
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. (Combine with PS_0[5]) 110 = No usable endpoints. 111 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable. 111= No usable endpoints.	11

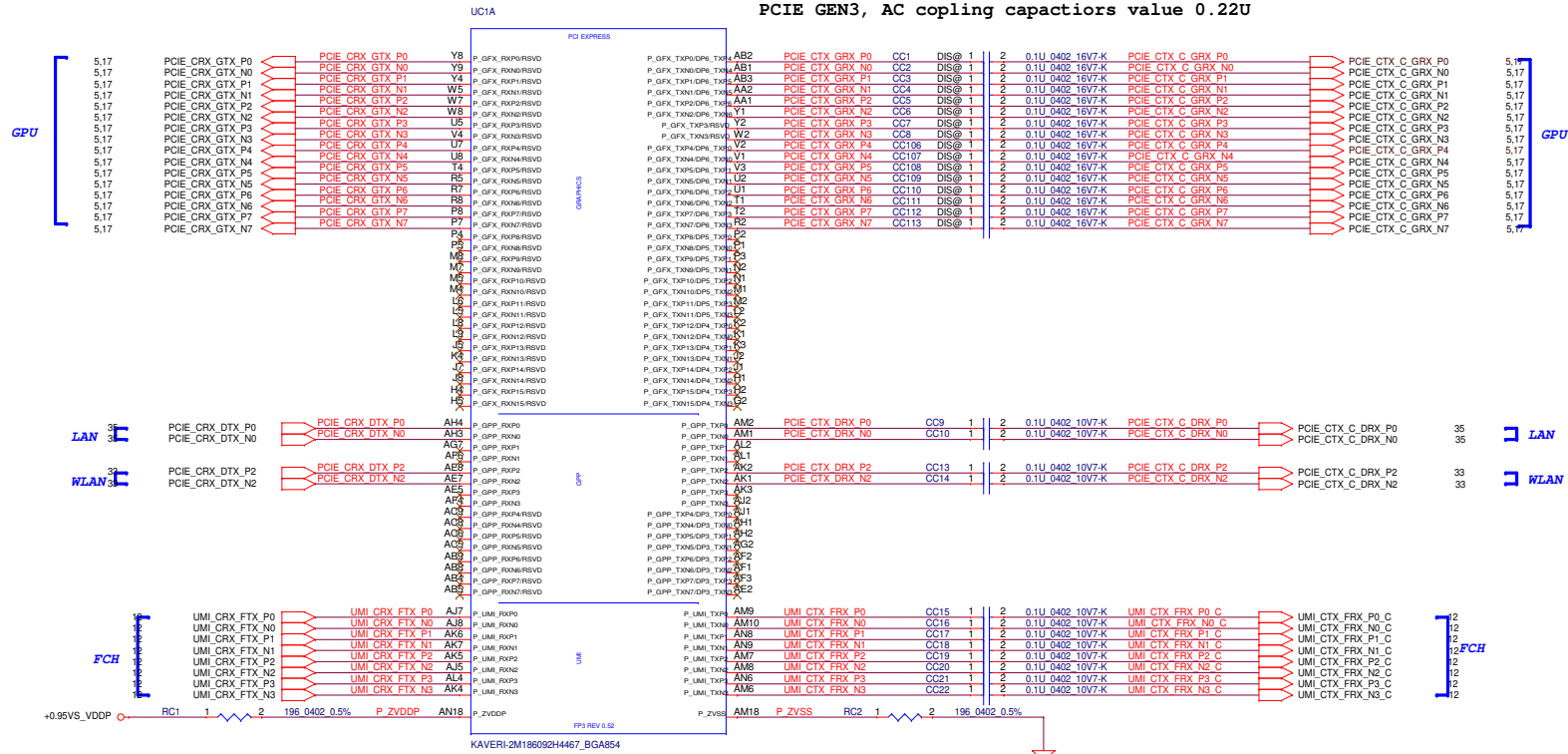
VRAM ID config

Memory Type	VRAM ID PS_3[3:1]	PU resistor	PD resistor	
		RV33	RV36	
128Mx16	Hynix H5TC2G63FFR-11C	100	4.53K	4.99K
	Micron MT41J128M16JT-093G	111	4.75K	NC
	Samsung K4W2G1646Q-BC1A	110	3.4K	10K
256Mx16	Hynix H5TC4G63AFR-11C	000	NC	4.75K
	Micron MT41J256M16HA-093G	010	4.53K	2K
	Samsung K4W4G1646D-BC1A	001	8.45K	2K

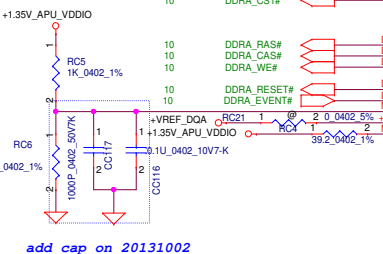
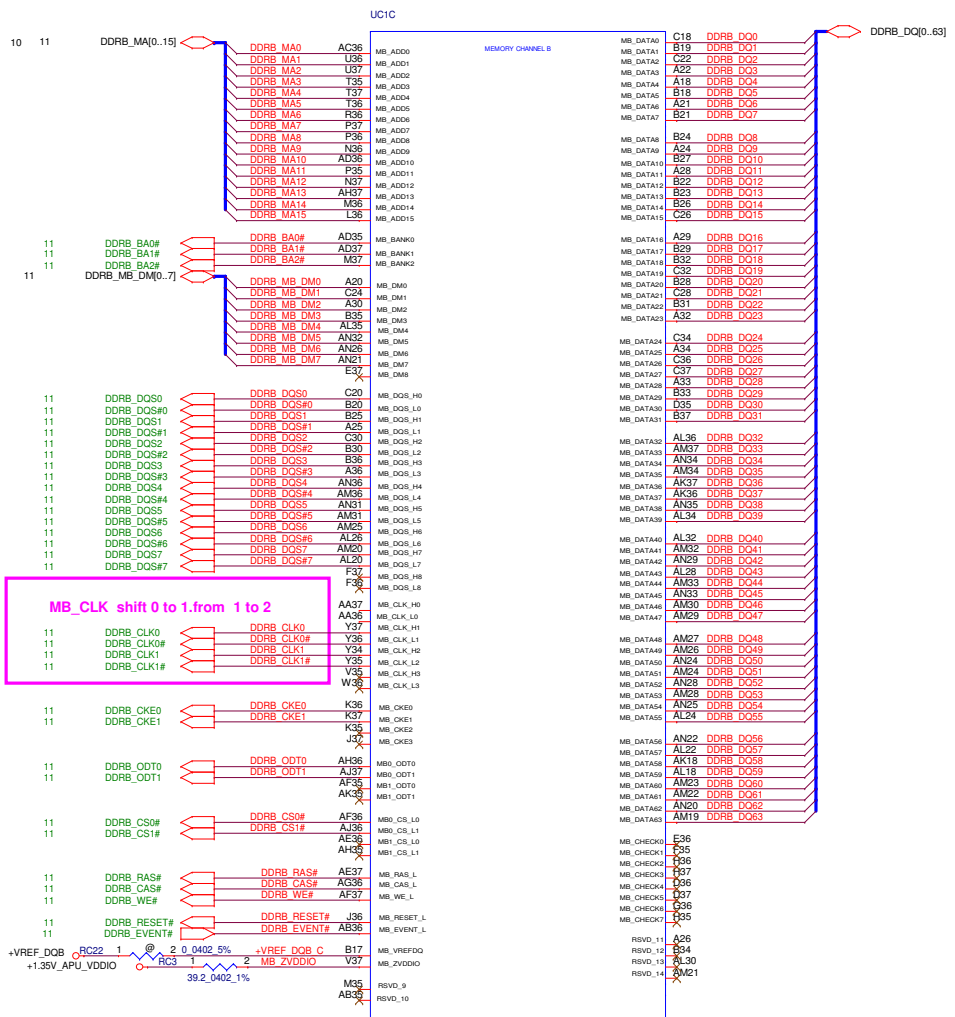
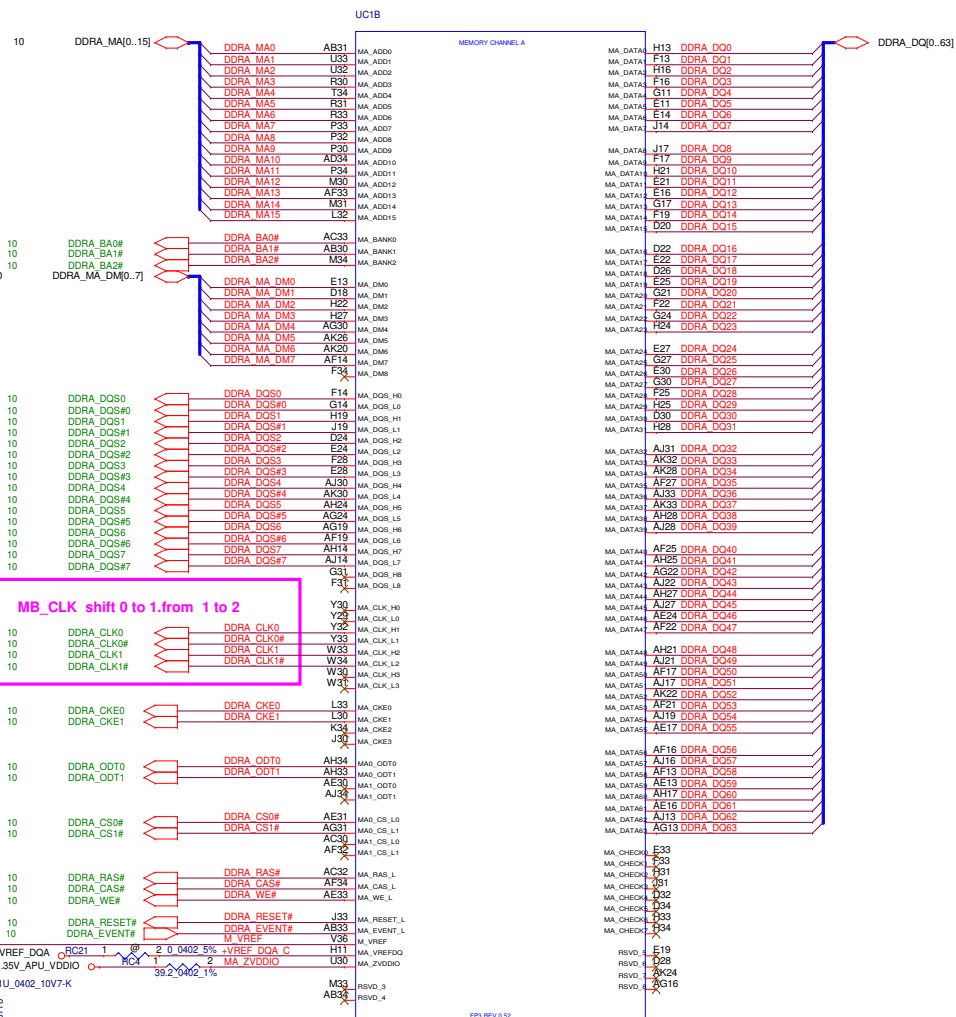
Security Classification	LC Future Center Secret Data		Title	 VGA Notes List
Issued Date	2013/08/08	Deciphered Date	2013/08/05	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Document Number Custom 
Date: Monday, December 16, 2013				Sheet 4 of 52



FP3 Kaveri APU supports
 PCIE Gen2, AC coupling capacitors value 0.1U.
 PCIE GEN3, AC coupling capacitors value 0.22U



Security Classification		LC Future Center Secret Data	
Issued Date	2012/12/05	Deciphered Date	2014/12/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			
Title	APU PEG/PCIE/UMI		
Size	Document Number	Customer	
Date	Monday, December 16, 2013	Sheet	5 of 52

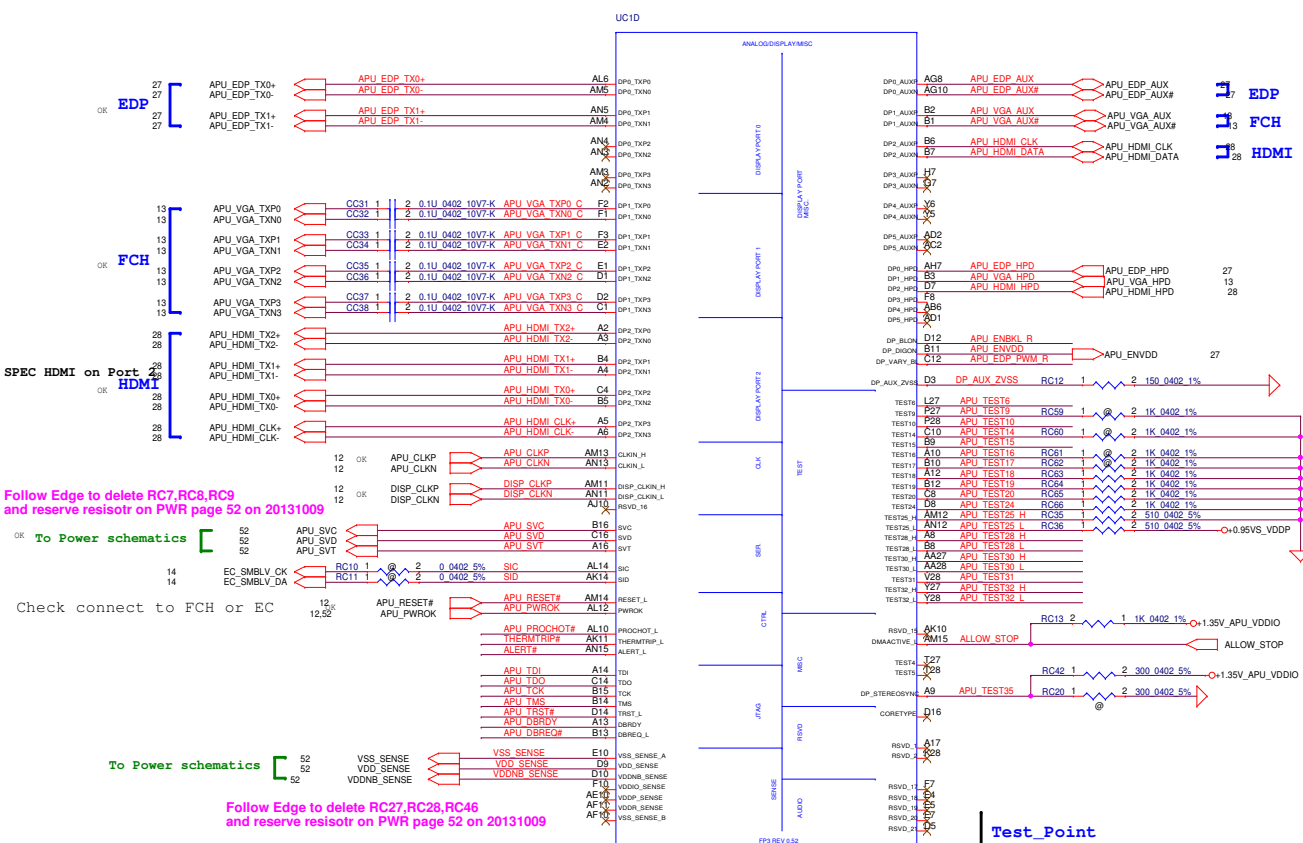


add cap on 20131002

KAVERI-2M186092H4467_BGA854

KAVERI-2M186092H4467_BGA854

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	APU DDRA/B	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Document Number		Rev. 1.A		
Date:	Monday, December 16, 2013	Sheet	6	of	52



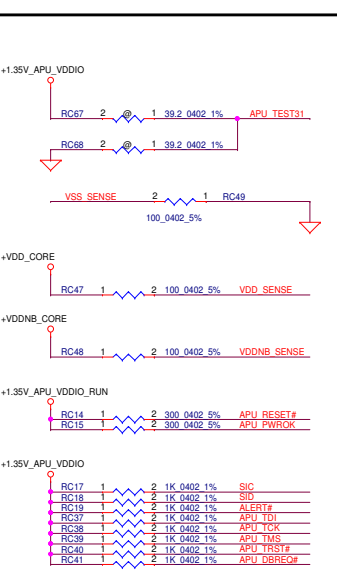
Follow Edge to delete RC7,RC8,RC9 and reserve resistor on PWR page 52 on 20131009

To Power schematics

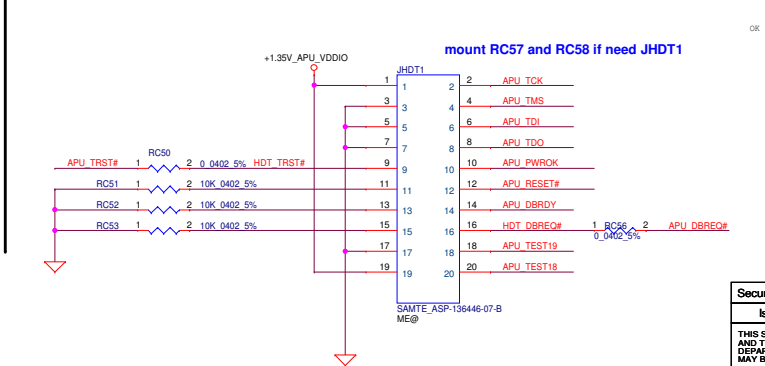
Check connect to FCH or EC

To Power schematics

Follow Edge to delete RC27,RC28,RC46 and reserve resistor on PWR page 52 on 20131009

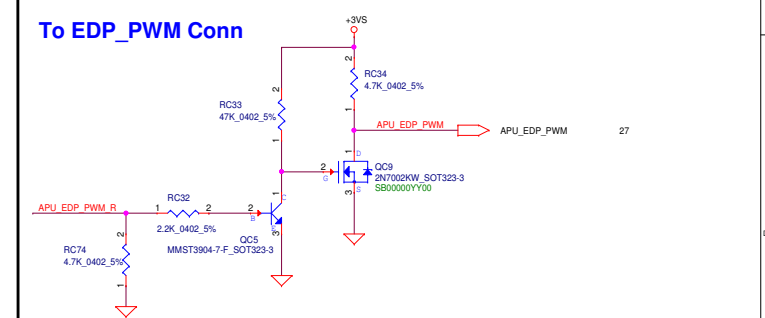
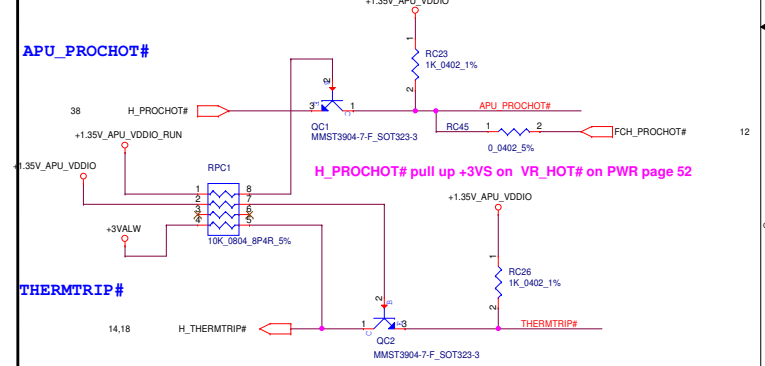
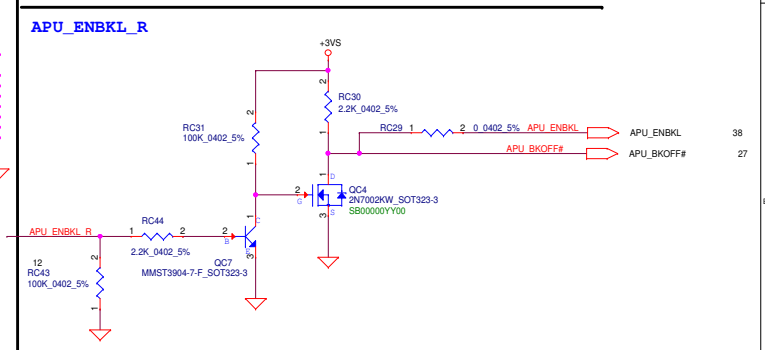
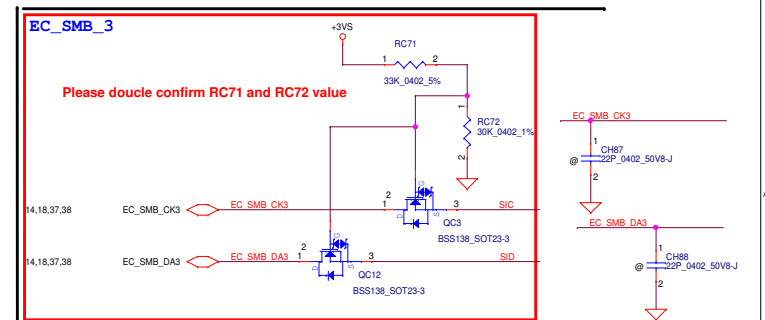


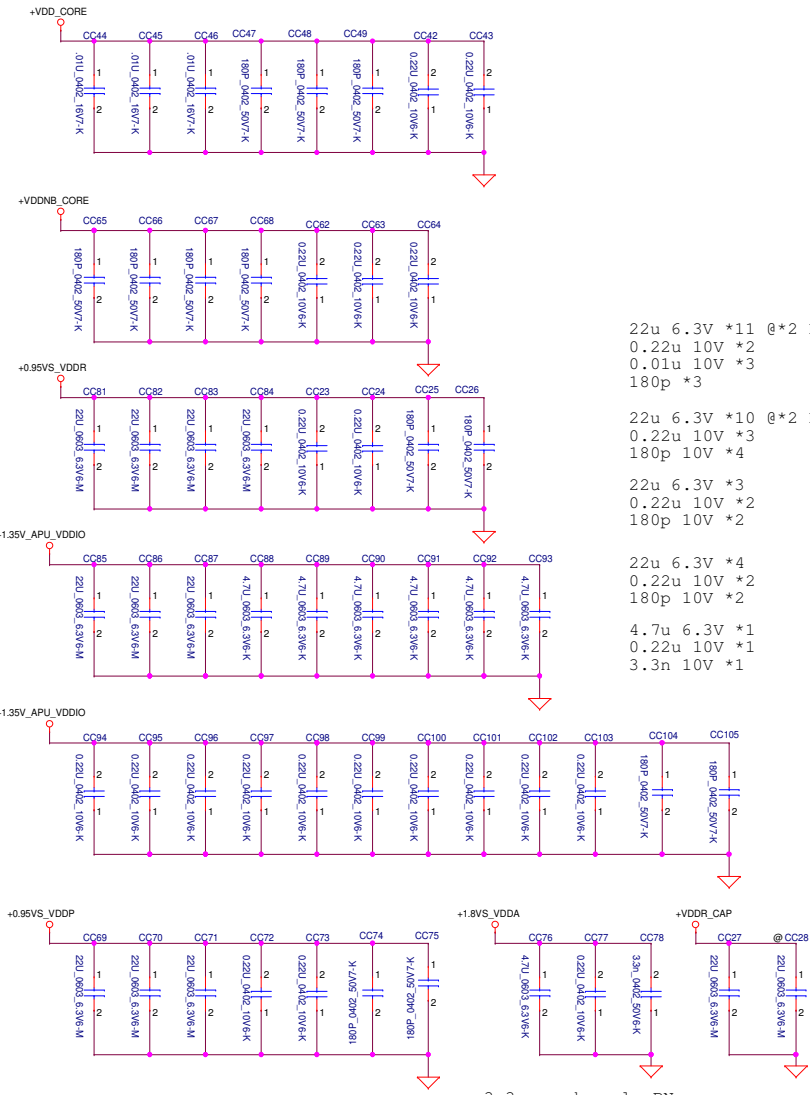
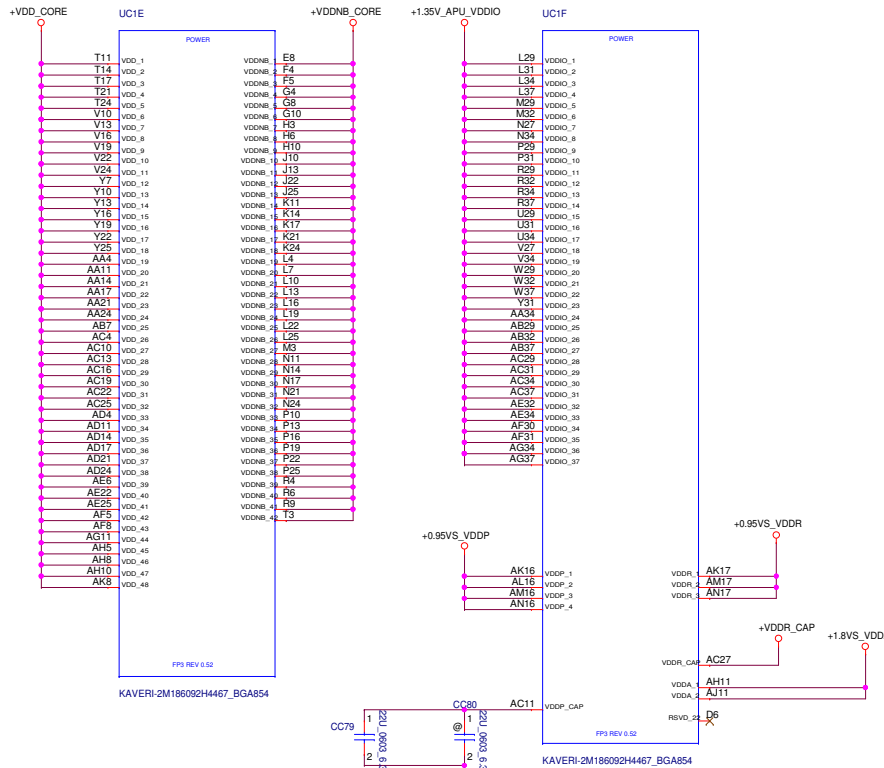
HDT Debug conn



Test Point

VSS_SENSE	TPC1	1	Test_Point_40MIL
VDD_SENSE	TPC2	1	Test_Point_40MIL
VDDNB_SENSE	TPC3	1	Test_Point_40MIL
APU_TEST10	TPC4	1	Test_Point_40MIL
APU_TEST11	TPC5	1	Test_Point_40MIL
APU_TEST15	TPC6	1	Test_Point_40MIL
APU_TEST16	TPC7	1	Test_Point_40MIL
APU_TEST17	TPC8	1	Test_Point_40MIL
APU_TEST18	TPC9	1	Test_Point_40MIL
APU_TEST19	TPC10	1	Test_Point_40MIL
APU_TEST20	TPC11	1	Test_Point_40MIL
APU_TEST32	TPC12	1	Test_Point_40MIL





22u 6.3V *11 @*2 Design Guide
 0.22u 10V *2
 0.01u 10V *3
 180p *3

22u 6.3V *10 @*2 Design Guide
 0.22u 10V *3
 180p 10V *4

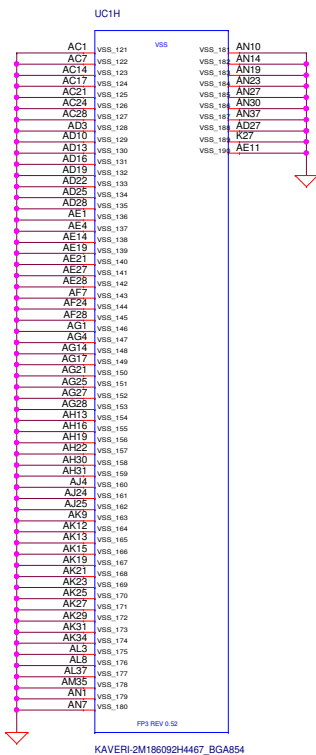
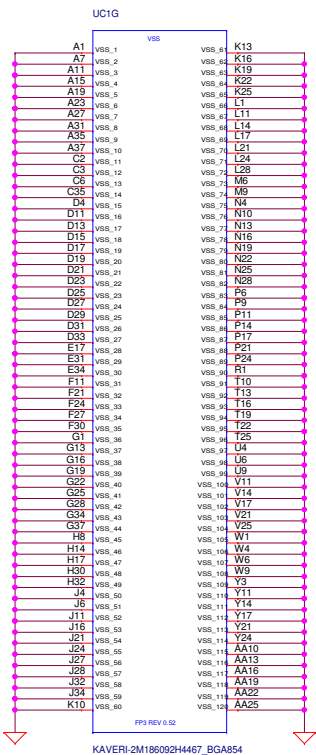
22u 6.3V *3
 0.22u 10V *2
 180p 10V *2

22u 6.3V *4
 0.22u 10V *2
 180p 10V *2

4.7u 6.3V *1
 0.22u 10V *1
 3.3n 10V *1

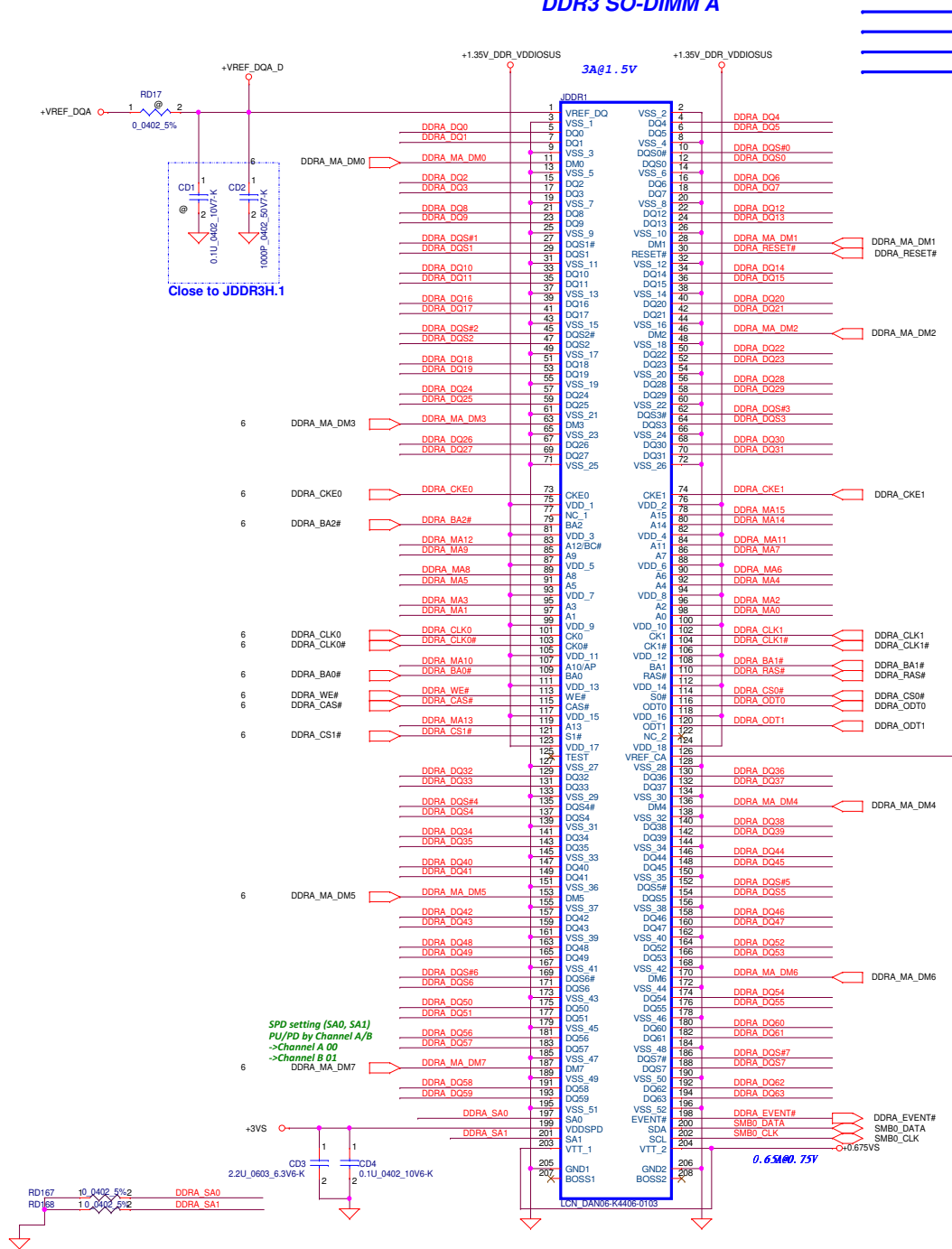
3.3n need apply PN

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	APU Power	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Document Number	Date		Rev	
Custom		Monday, December 16, 2013		1.A	
				ACLU7	
				Sheet 8 of 52	

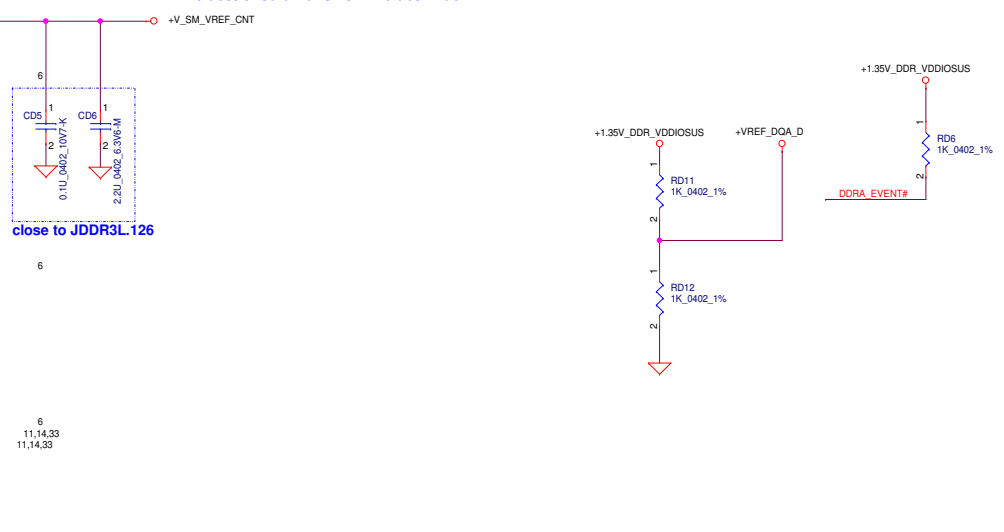
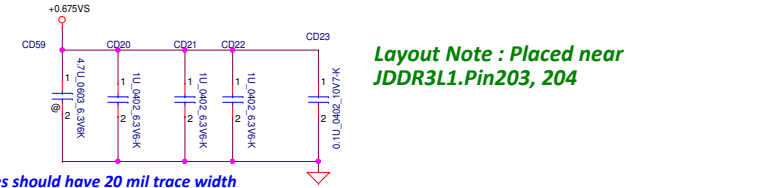
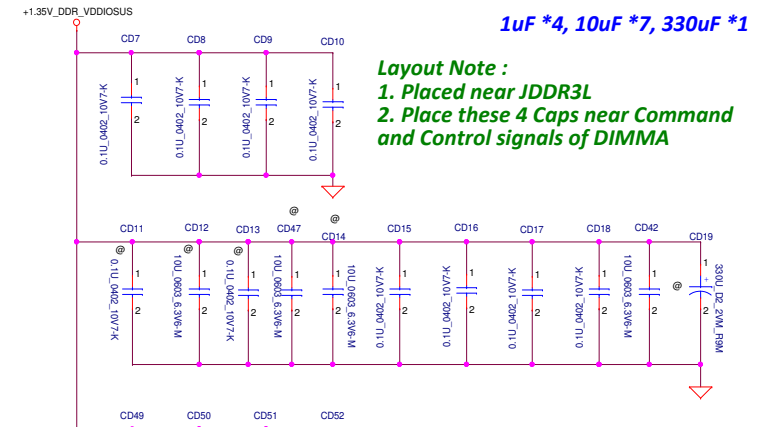


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	APU GND	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Document Number	Date		Rev	
Custom	ACLUT	Monday, December 16, 2013		1.A	
Date				Sheet	
Monday, December 16, 2013				9 of 52	

DDR3 SO-DIMM A

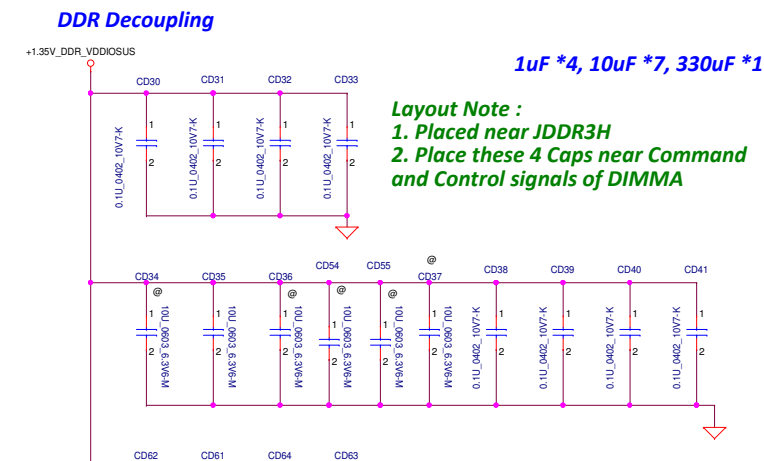
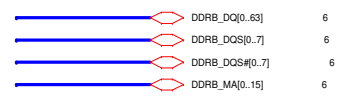
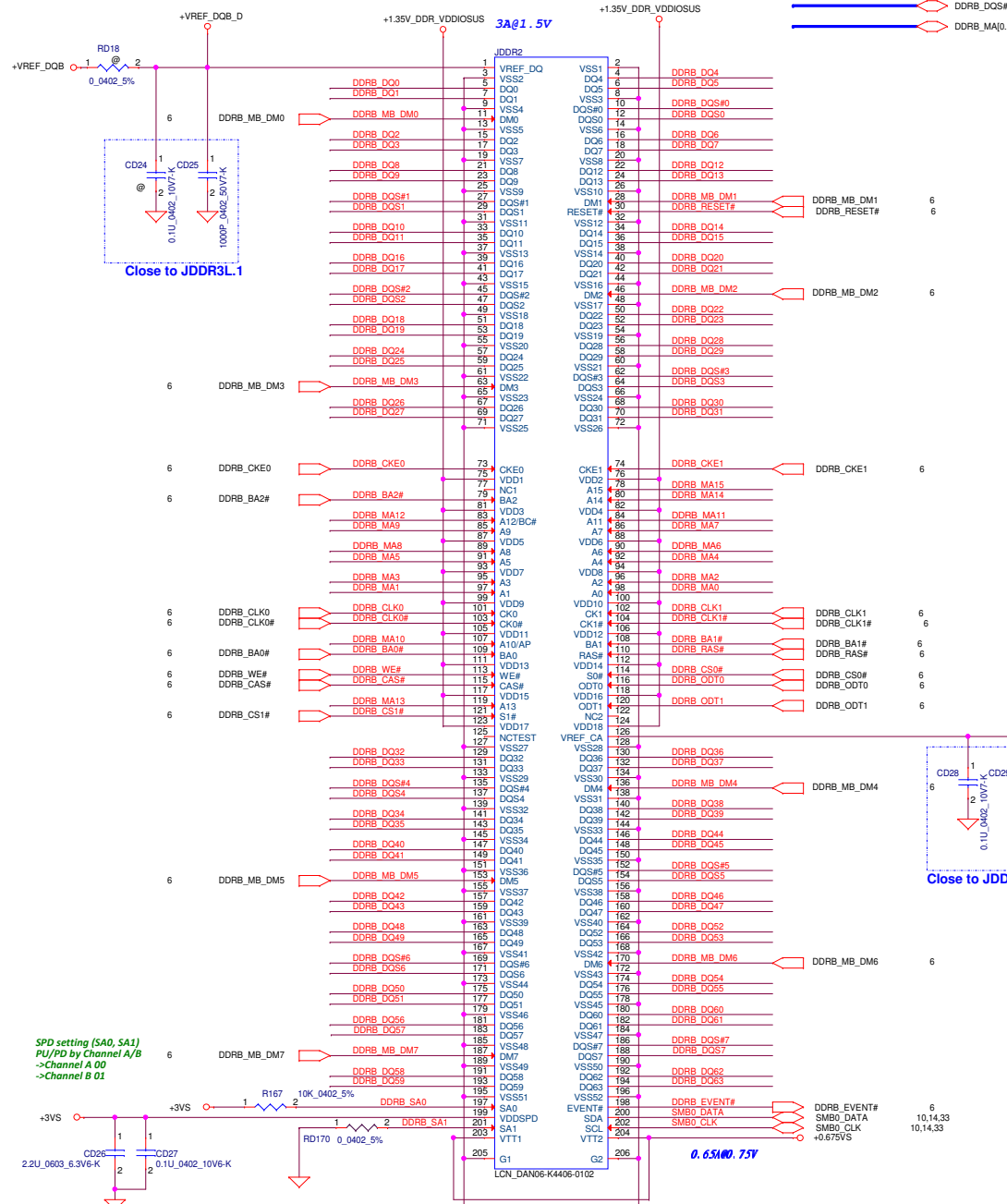


DDR Decoupling

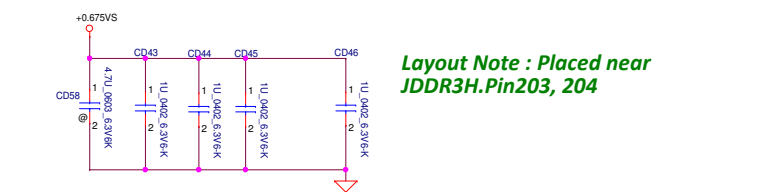


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	DDR3 SO-DIMMA/1	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Document Number	Customer		Rev	
Date:	Monday, December 16, 2013	Sheet	10	of 52	

DDR3 SO-DIMM B



Layout Note :
 1. Placed near JDDR3H
 2. Place these 4 Caps near Command and Control signals of DIMMA

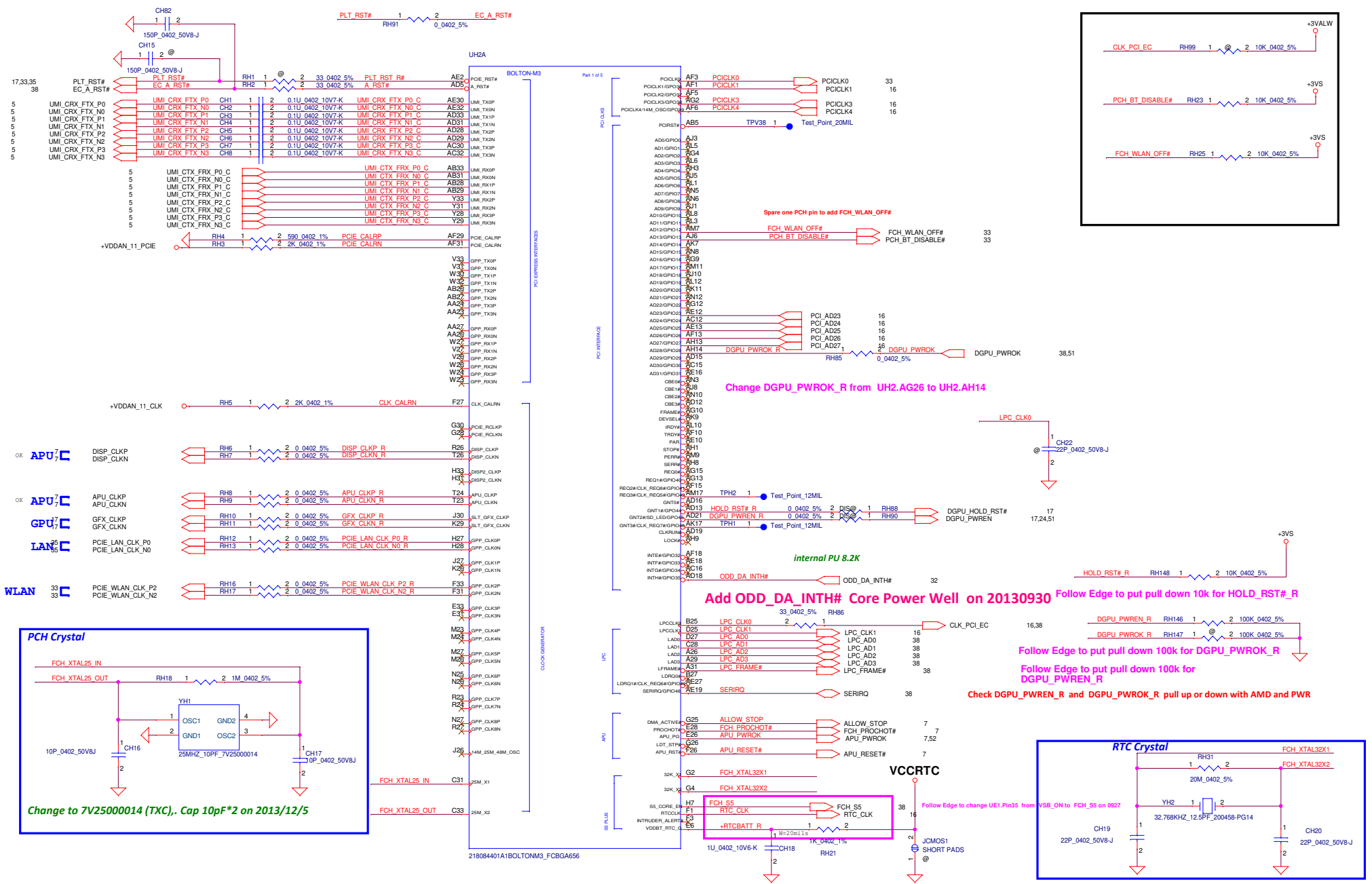


Layout Note : Placed near JDDR3H.Pin203, 204

SPD setting [SA0, SA1]
 PU/PD by Channel A/B
 ->Channel A 00
 ->Channel B 01

CRB: DDRB_SA1 pull low / DDRB_SA0 pull high
 Edge: DDRB_SA1 pull high / DDRB_SA0 pull low

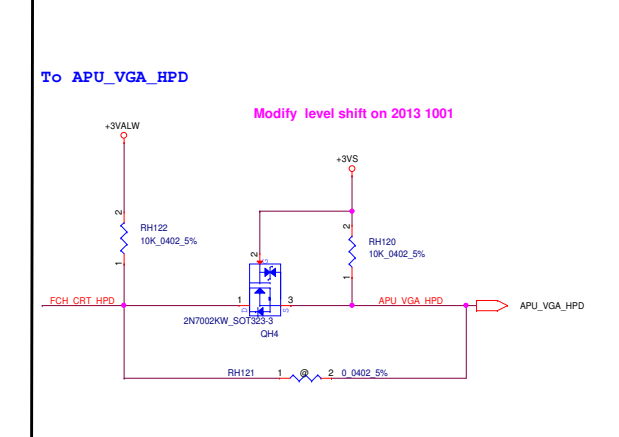
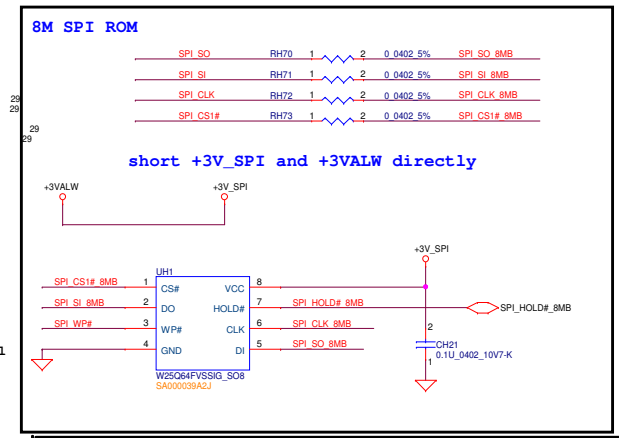
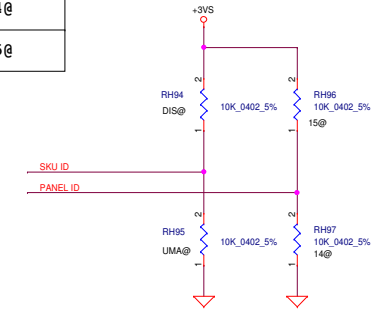
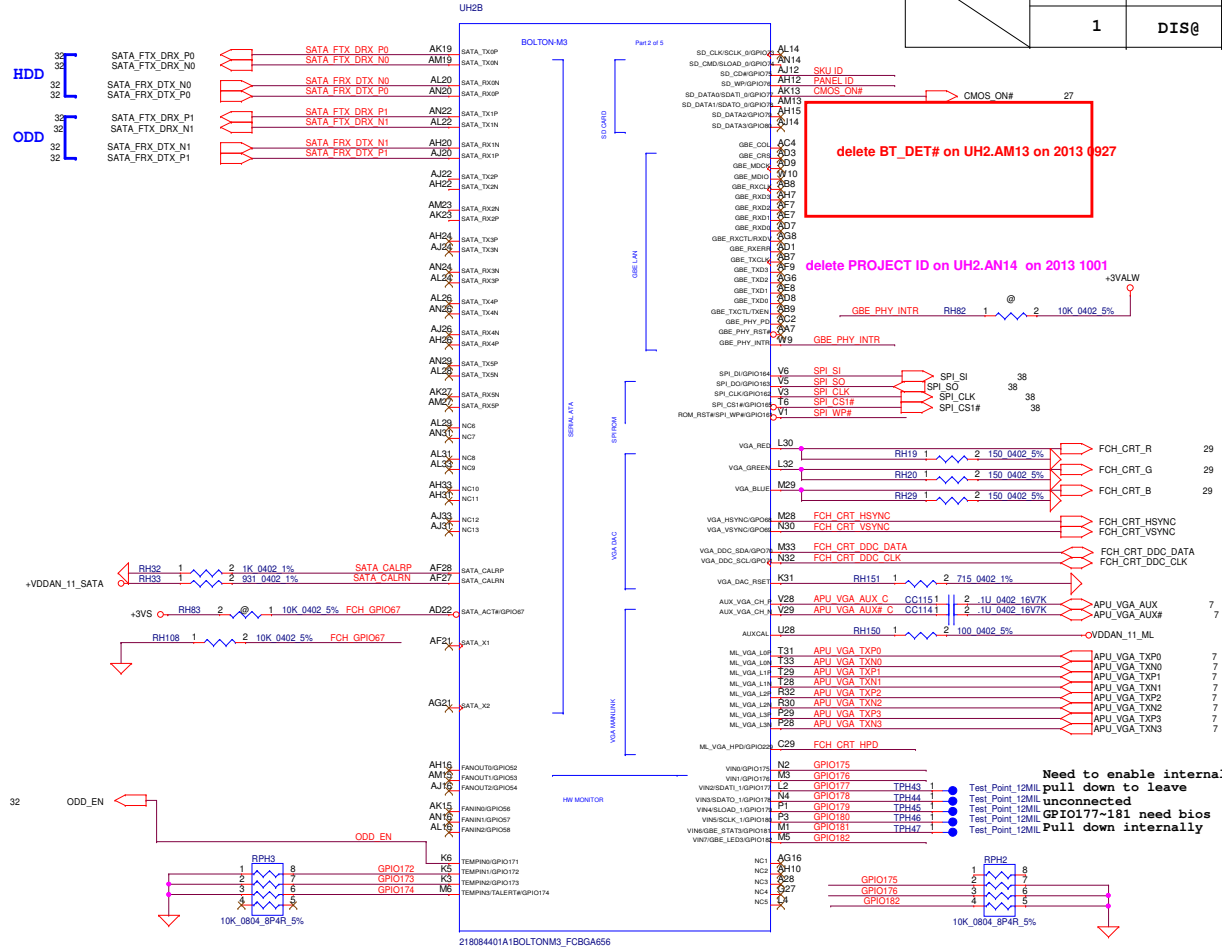
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	DDR3 SO-DIMMB/2	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Document Number	Date		Monday, December 16, 2013	Sheet 11 of 52
Customer	ACLU7	Rev		0.4	

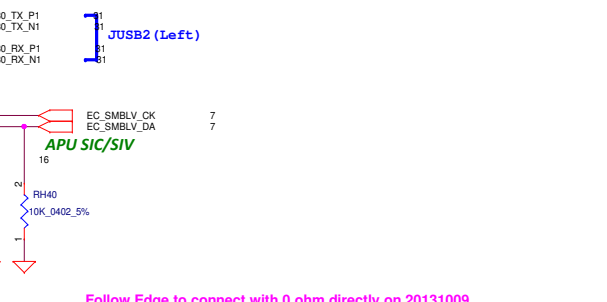
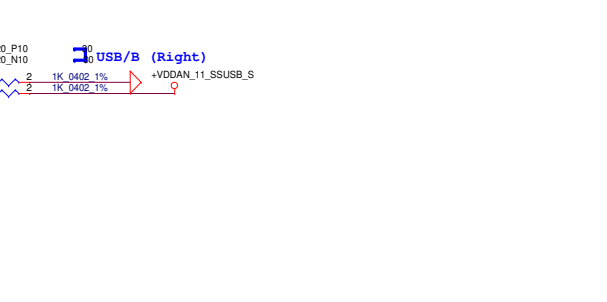
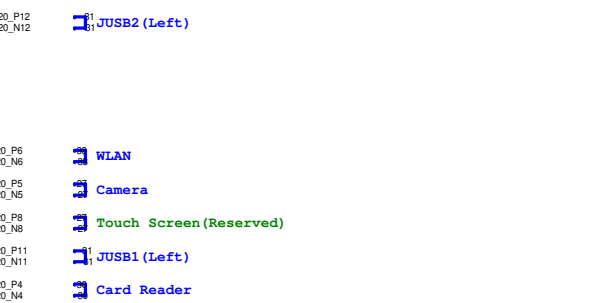
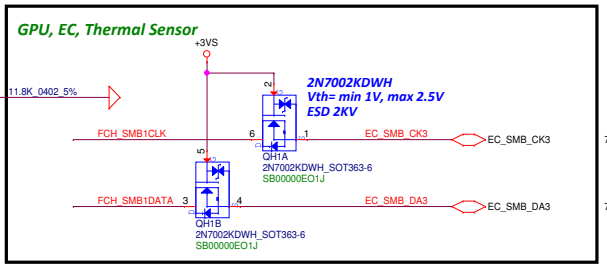
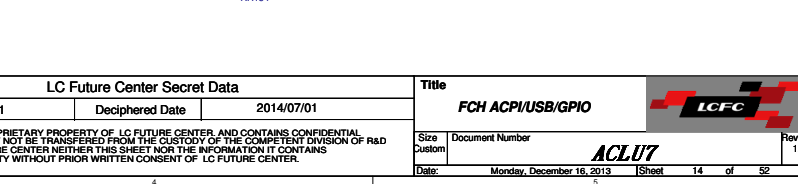
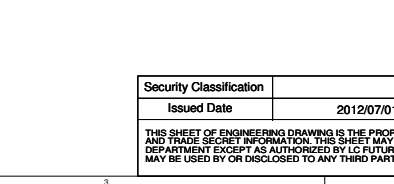
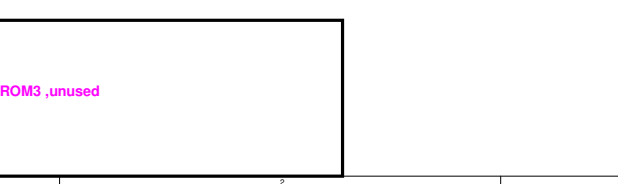
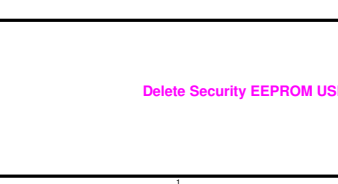
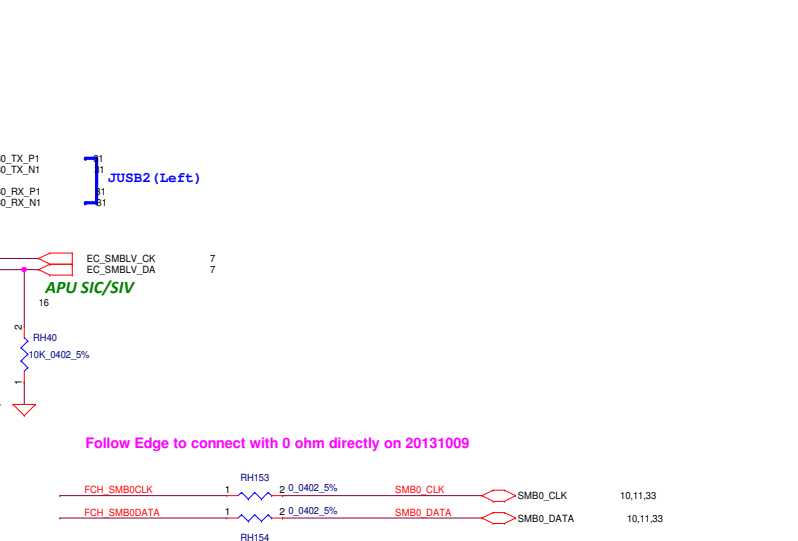
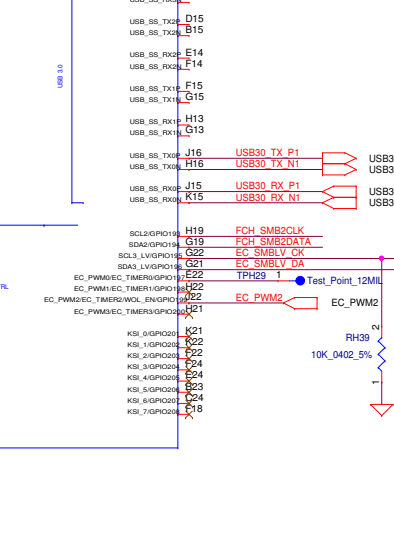
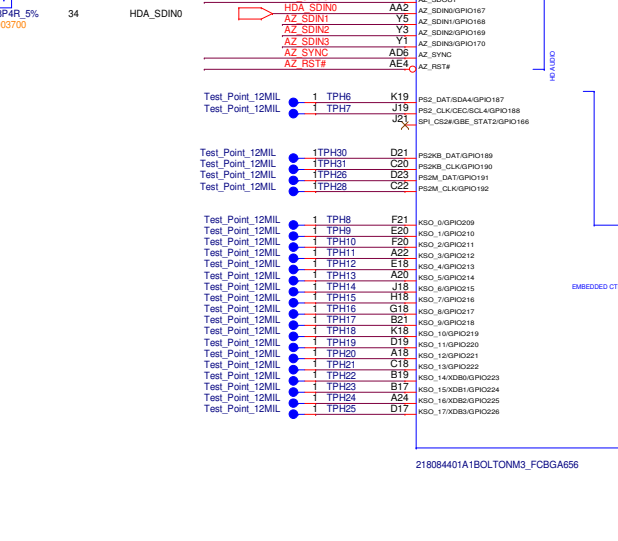
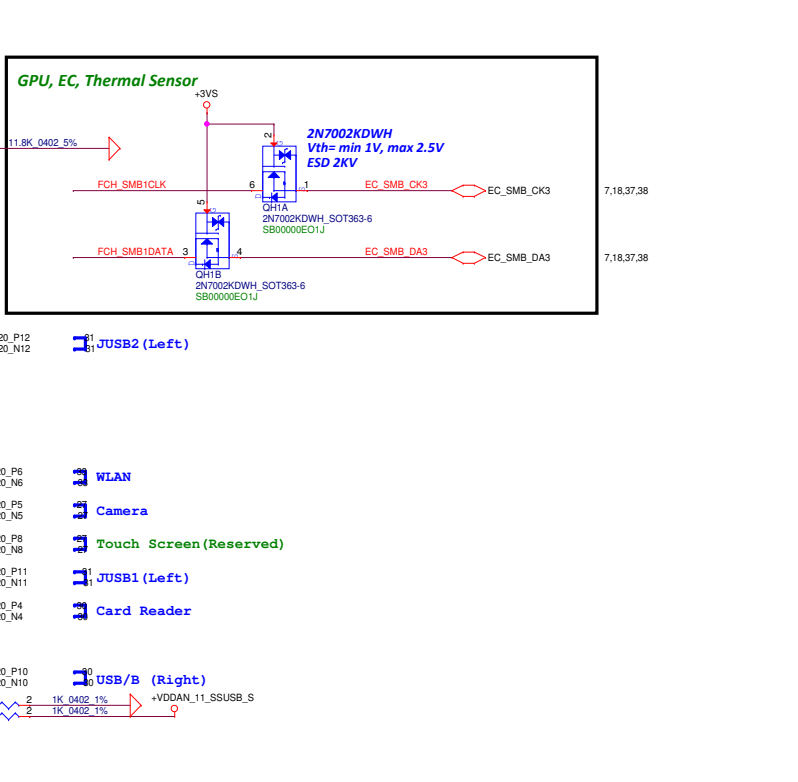
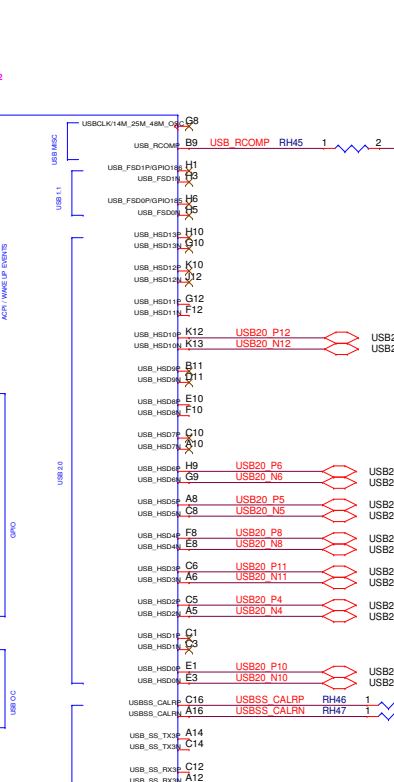
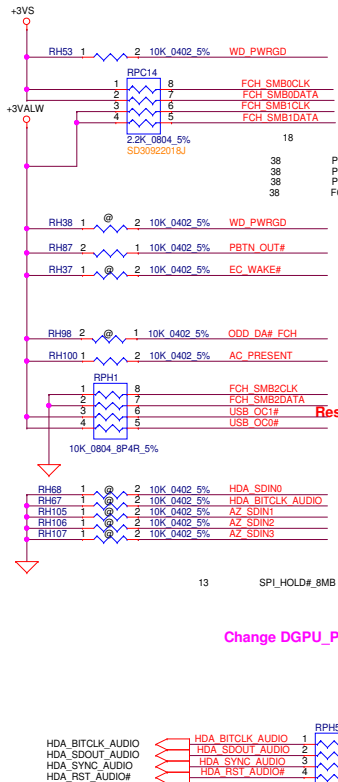


Security Classification				LC Future Center Secret Data				Title	
Issued Date		Deciphered Date		Document Number		Date		Rev	
2012/07/01		2014/07/01		FCH PCIe/PCI/LPC/APU/S5+		Monday, December 16, 2013		1.A	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>									

Add table on 2013 1001

BOARD ID Config.	SKU ID	Function	PANEL ID	Function
	0	UMA@	0	14@
	1	DIS@	1	15@

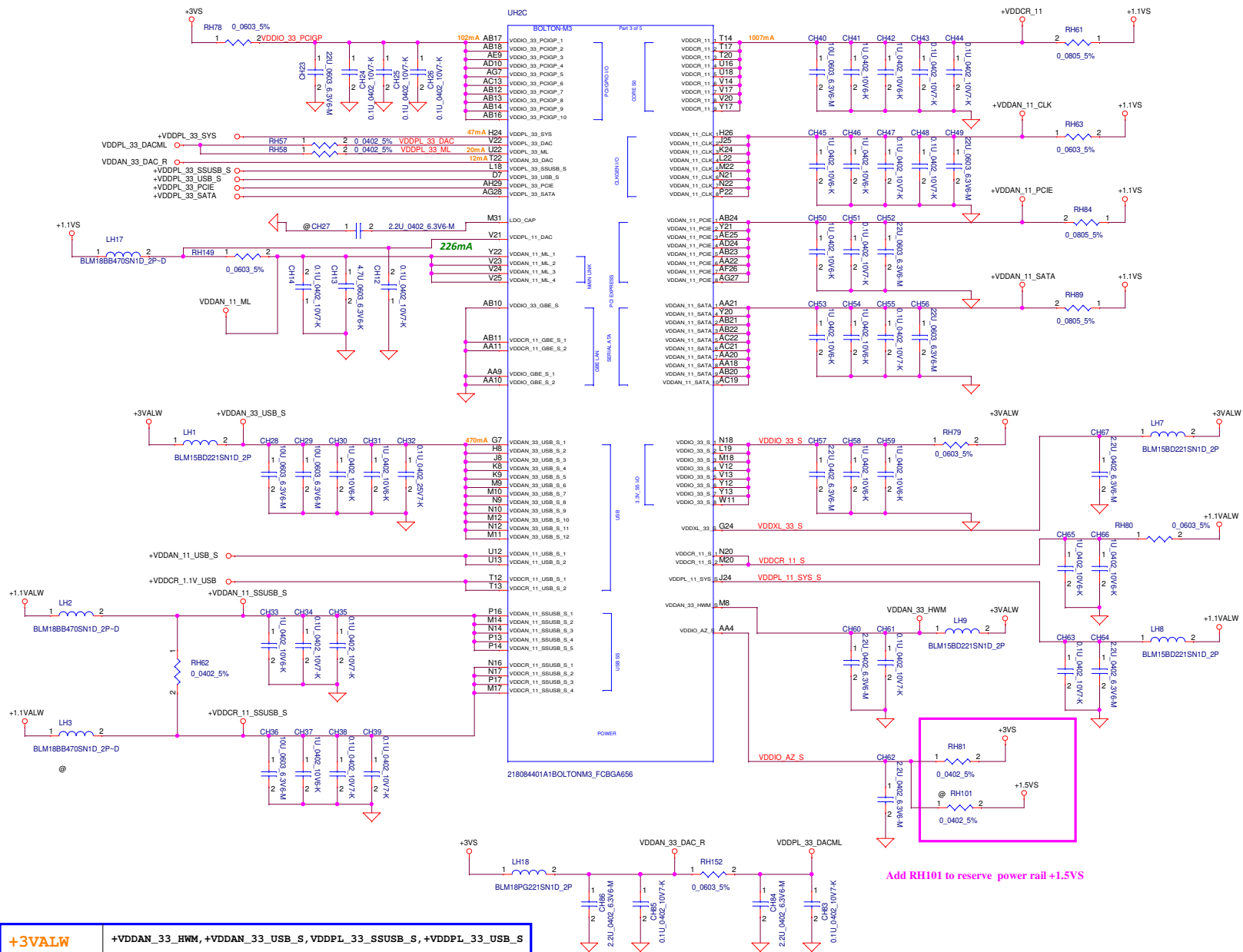




Delete Security EEPROM USROM3_unused

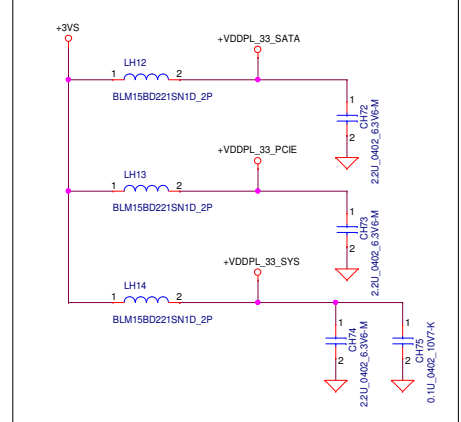
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	FCH ACPI/USB/GPIO	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Document Number		ACLU7		Rev
Date:	Monday, December 16, 2013		Sheet	14	of 52

22u *1, 1u*1 for circuit check list

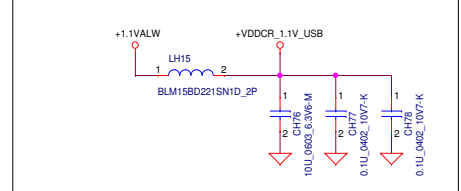


+3VALW	+VDDAN_33_HWM,+VDDAN_33_USB_S,+VDDPL_33_SSUSB_S,+VDDPL_33_USB_S
+3VS	+VDDPL_33_SATA,+VDDPL_33_PCIE,+VDDPL_33_SYS
+1.1VALW	+VDDCR_11_SSUSB_S,+VDDAN_11_SSUSB_S,+VDDAN_11_USB_S,+VDDAN_11_USB_S,+VDDCR_1.1V_USB
+1.1VS	+VDDCR_11,+VDDAN_11_CLK,+VDDAN_11_PCIE,+VDDAN_11_SATA,

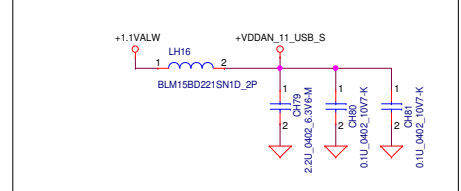
VDDPL_33_SATA & PCIE & SYS



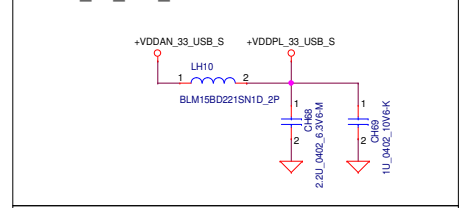
VDDCR_1.1V_USB



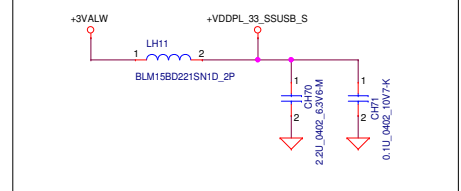
VDDAN_11_USB_S



VDDPL_33_USB_S



VDDPL_33_SSUSB_S



Add RHI01 to reserve power rail +1.5VS

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	FCH POWER/GND	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Document Number	Date		Rev	
		Monday, December 16, 2013		15 of 52	

STRAP PINS

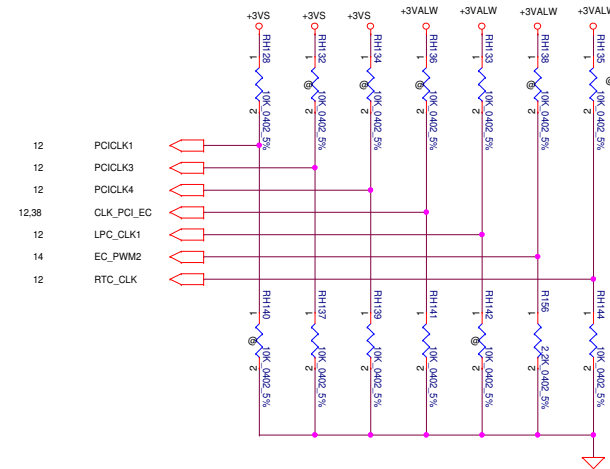
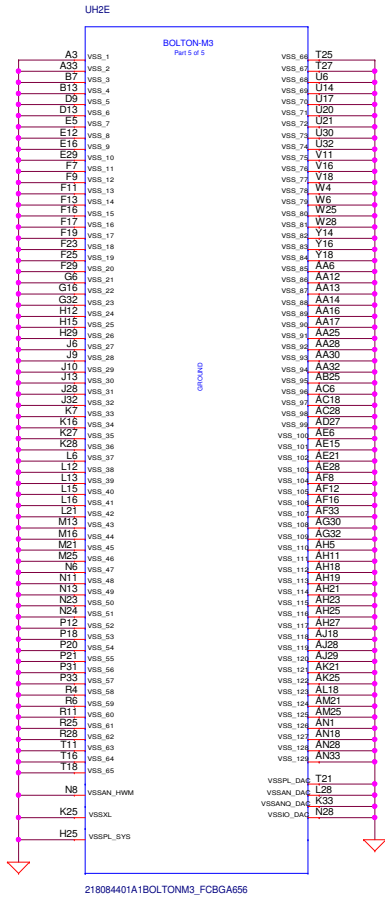
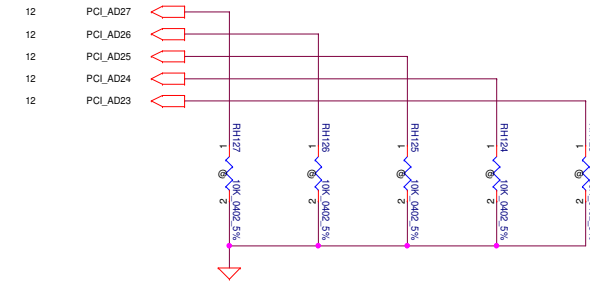
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED DEFAULT

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

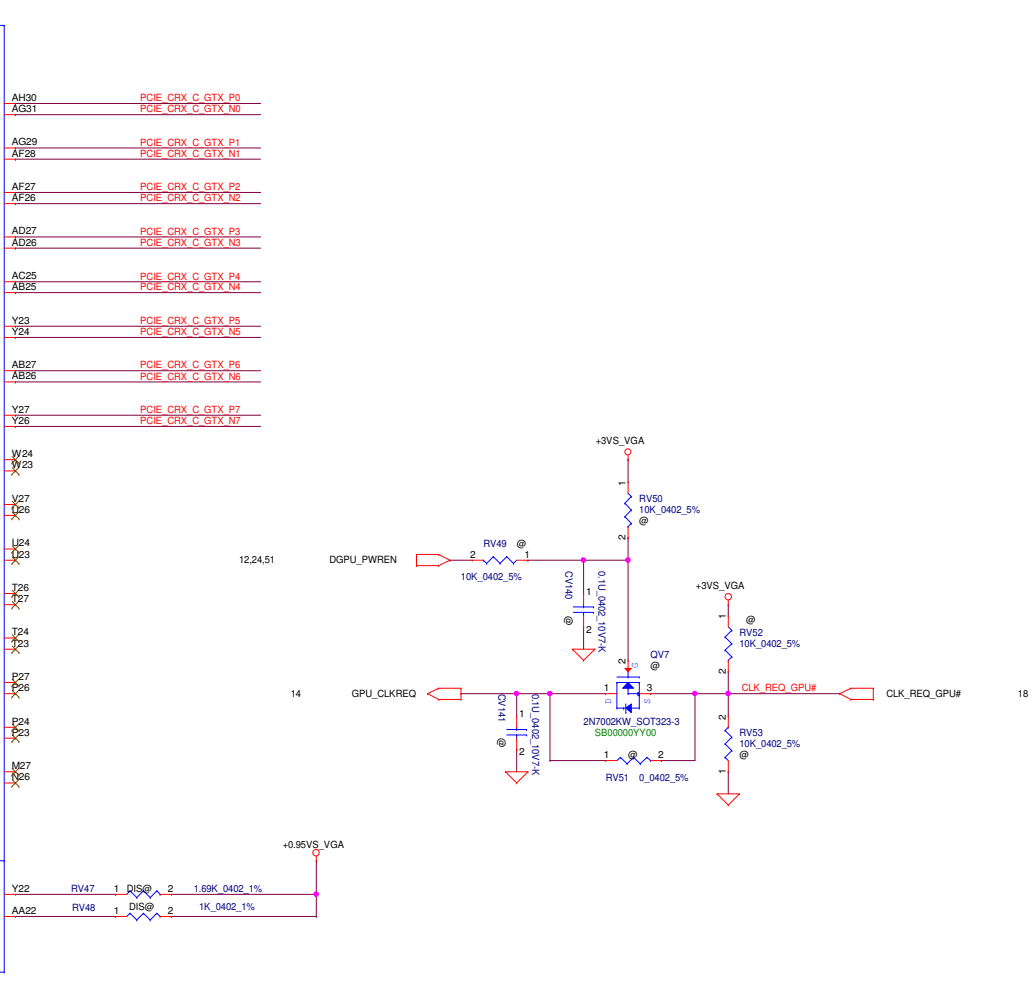
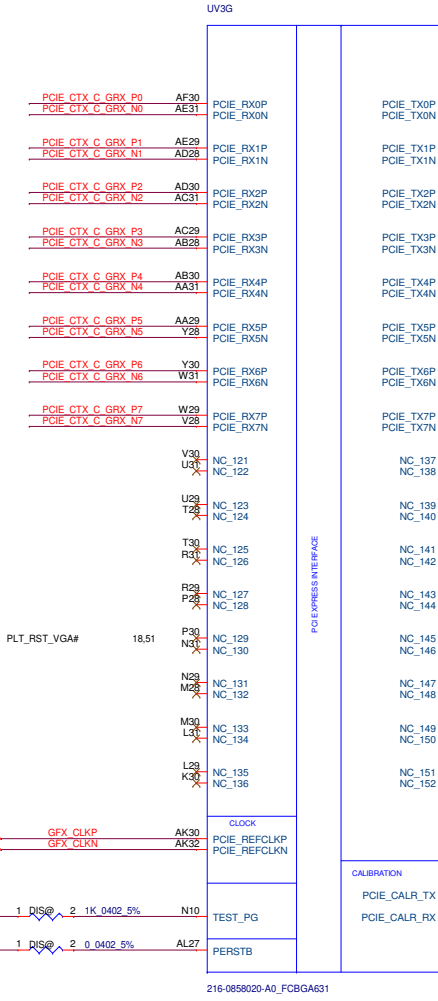
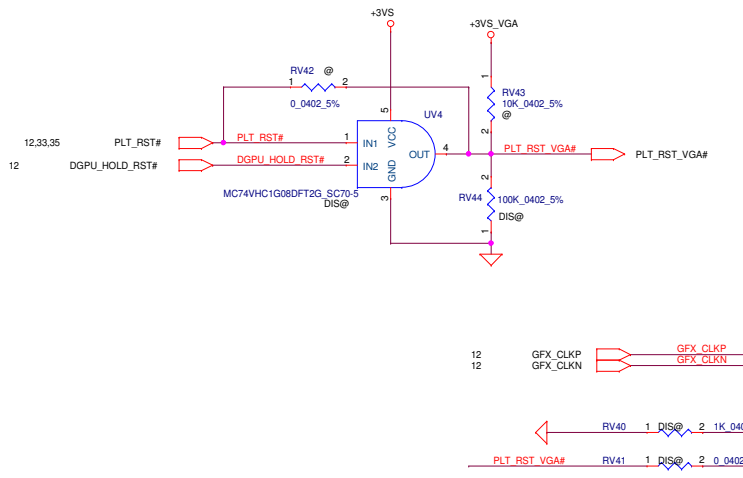
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

need confirm AD26

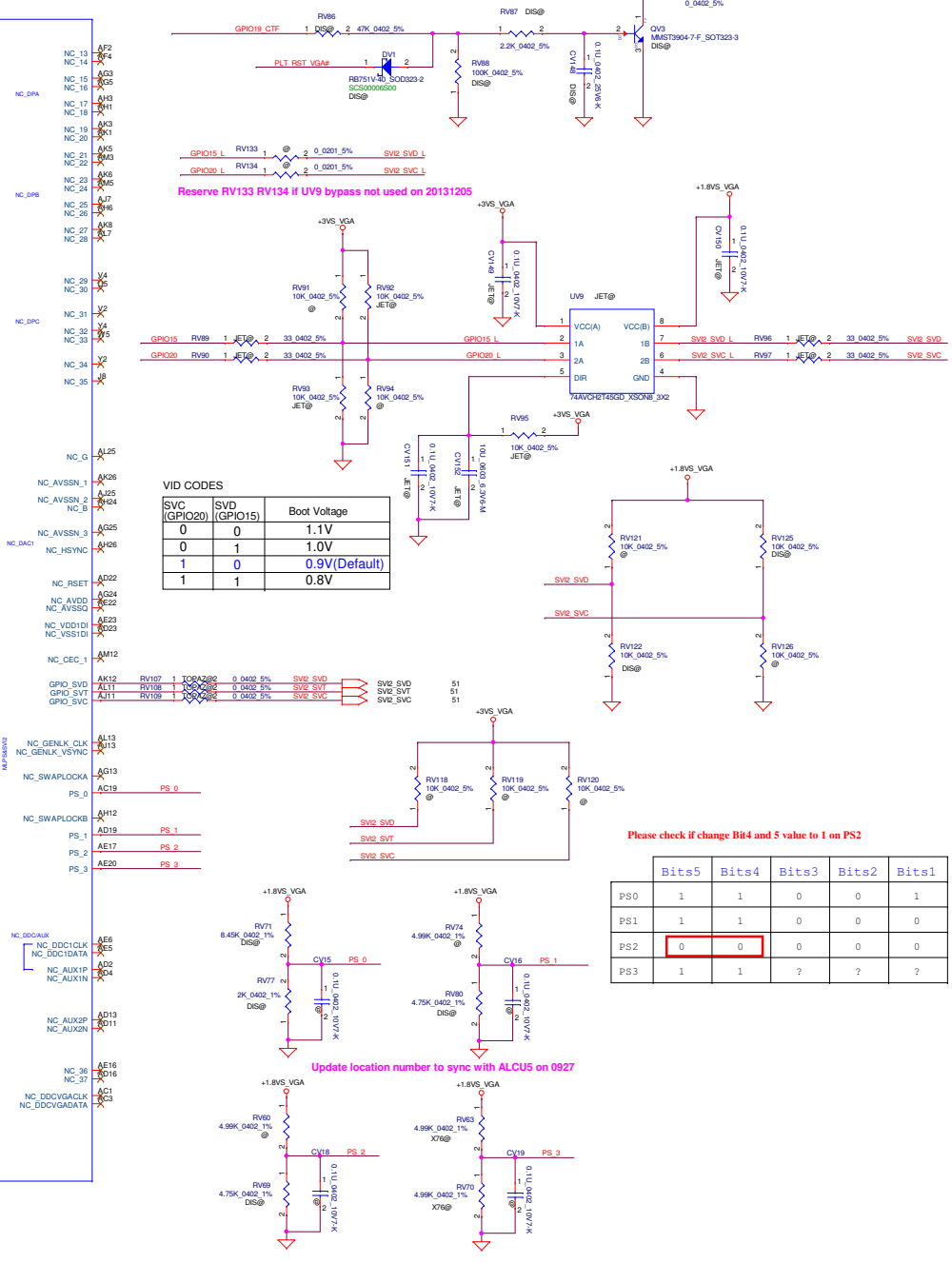
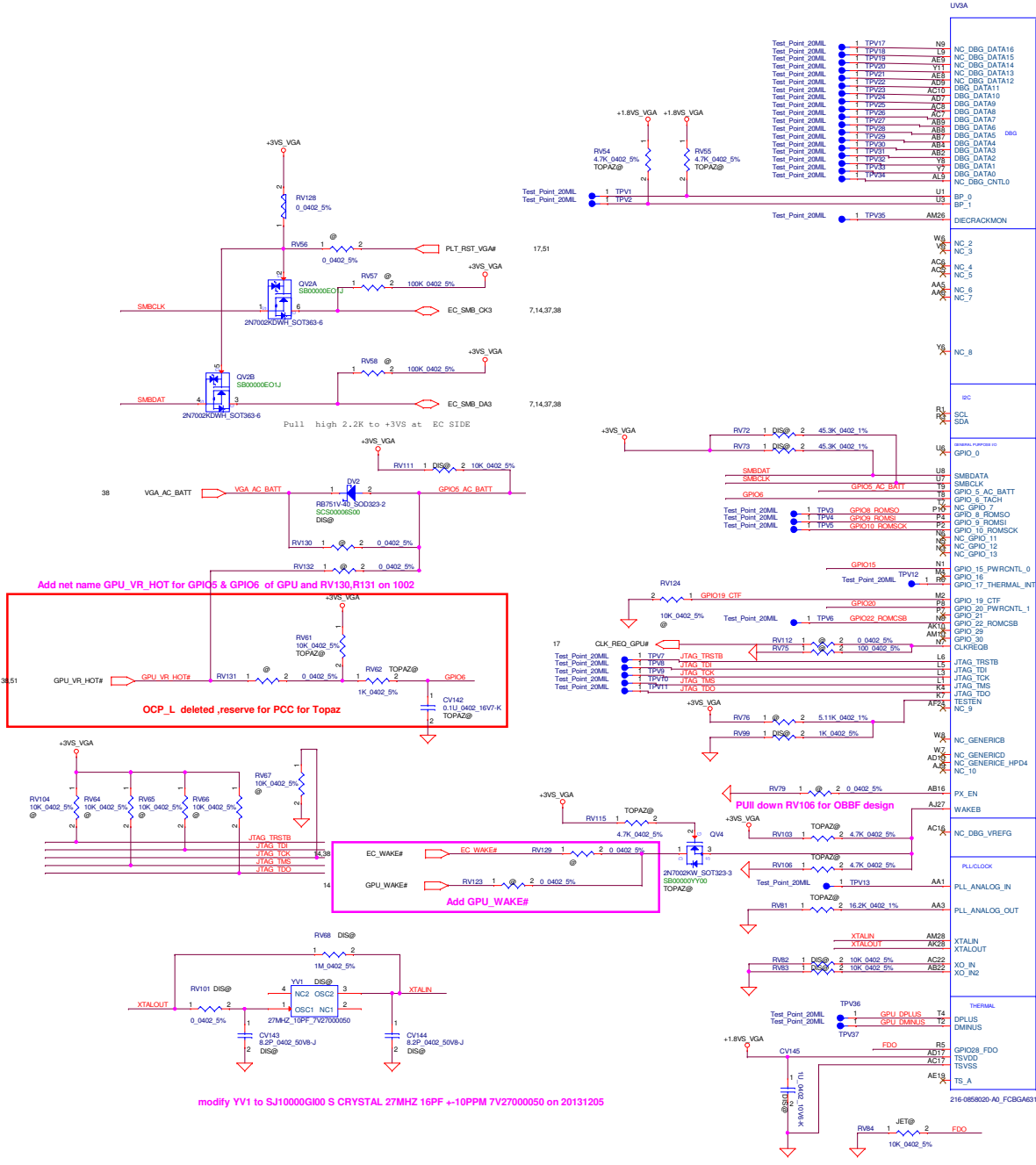


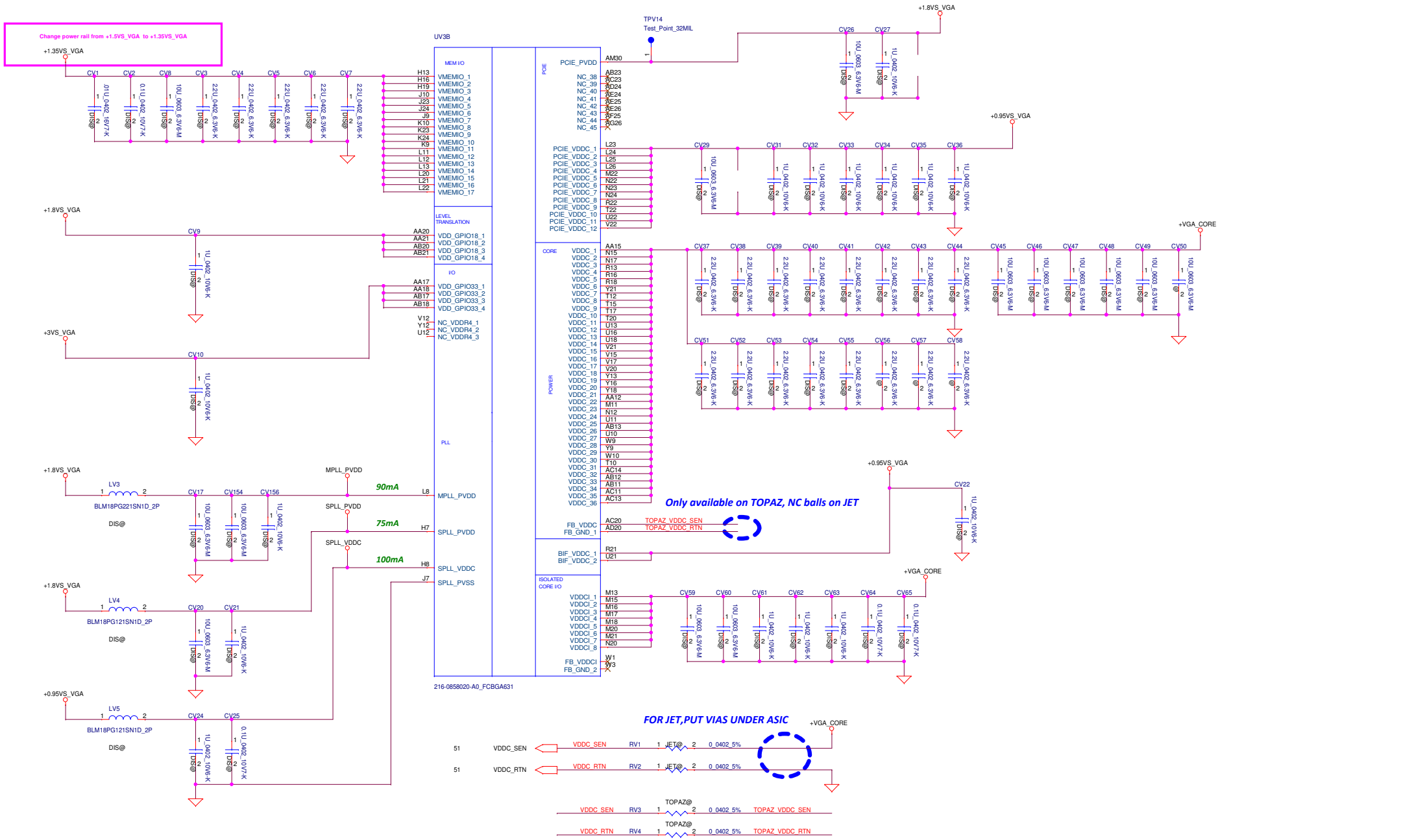
5	PCIE_CTX_C_GRP_N[0..7]	PCIE_CTX_C_GRP_N0..7
5	PCIE_CTX_C_GRP_P[0..7]	PCIE_CTX_C_GRP_P0..7
5	PCIE_CRX_GTX_N[0..7]	PCIE_CRX_GTX_N0..7
5	PCIE_CRX_GTX_P[0..7]	PCIE_CRX_GTX_P0..7

DIS@			
PCIE_CRX_GTX_P0	CV132	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_N0	CV133	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_P1	CV134	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_N1	CV135	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_P2	CV136	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_N2	CV137	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_P3	CV138	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_N3	CV139	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_P4	CV157	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_N4	CV158	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_P5	CV159	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_N5	CV175	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_P6	CV176	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_N6	CV177	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_P7	CV178	DIS@ 1	2 0.1U 0402 16V7-K
PCIE_CRX_GTX_N7	CV179	DIS@ 1	2 0.1U 0402 16V7-K



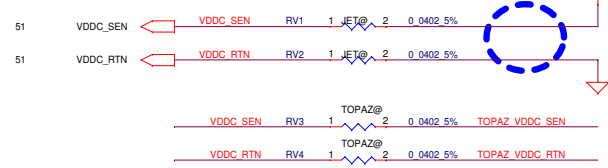
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Topaz & Jet PCIE	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Custom	Document Number	ACLU7		Rev
Date	Monday, December 16, 2013	Sheet	17	of	85



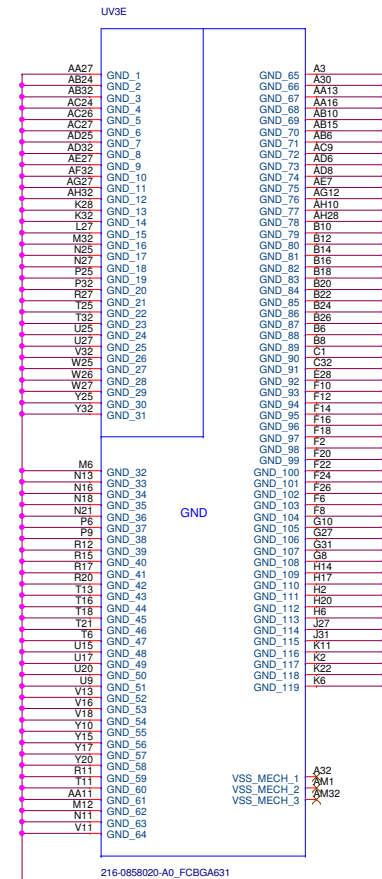
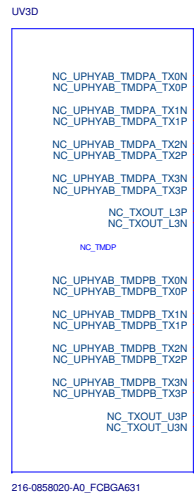
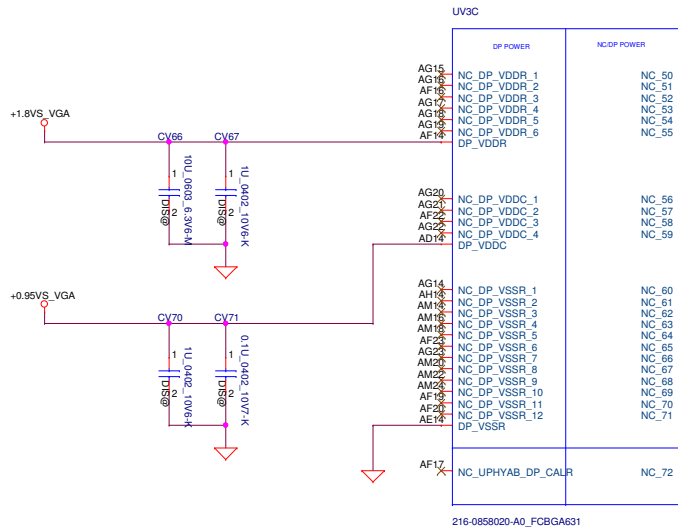


216-0858020-A0_FCBGA631

FOR JET, PUT VIAS UNDER ASIC



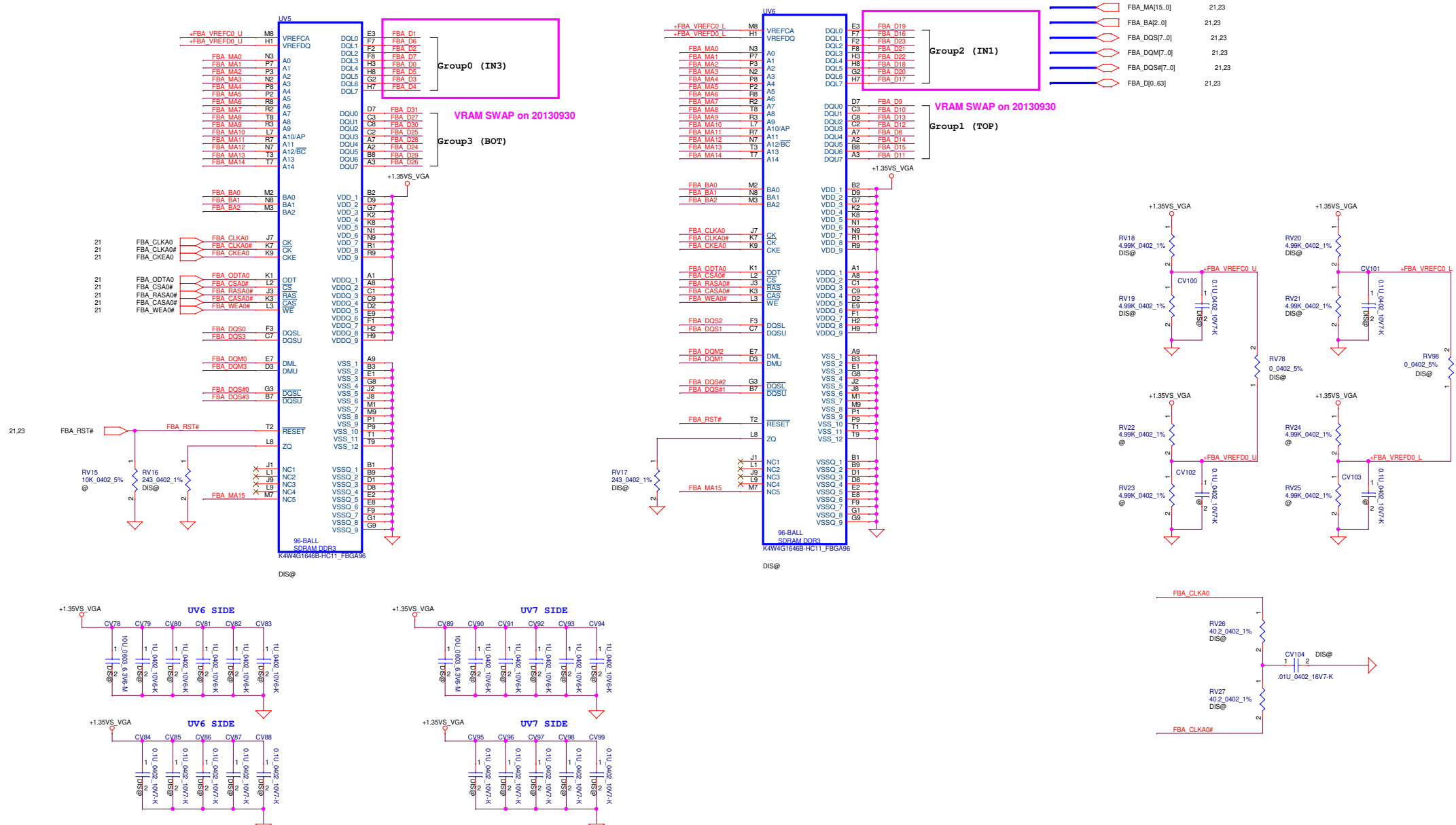
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Topaz & Jet Core Power	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Document Number	Date		Monday, December 16, 2013	Sheet 19 of 85
				Rev I.A	



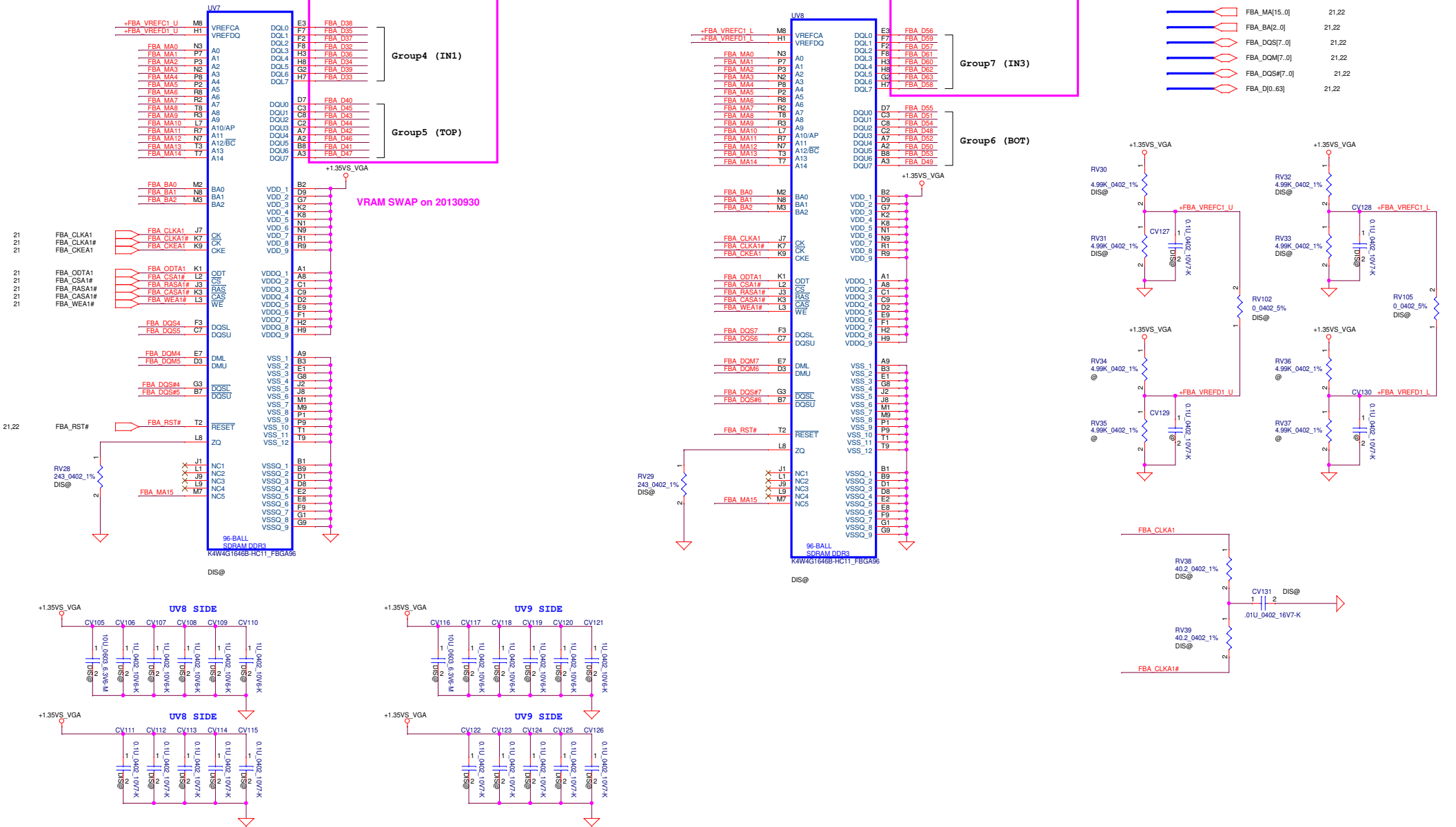
ASIC Ball	Topaz	Jet
U10, T10 AB13, W9 AB11, AB12 AC11, AC13 AC14, Y9, W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA3	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTRL0
H13, H16, H19, J10 J23, J24, J9, K10 K23, K24, K9, L11 L12, L13, L20, L21 L22	VMEMIO	VDDR1
AA17, AA18 AB17, AB18	VDD_GPIO33	VDDR3
AA20, AA21 AB20, AB21	VDD_GPIO18	VDD_CT

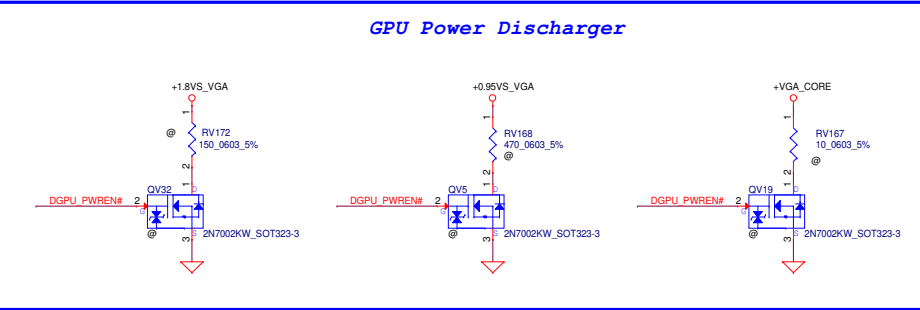
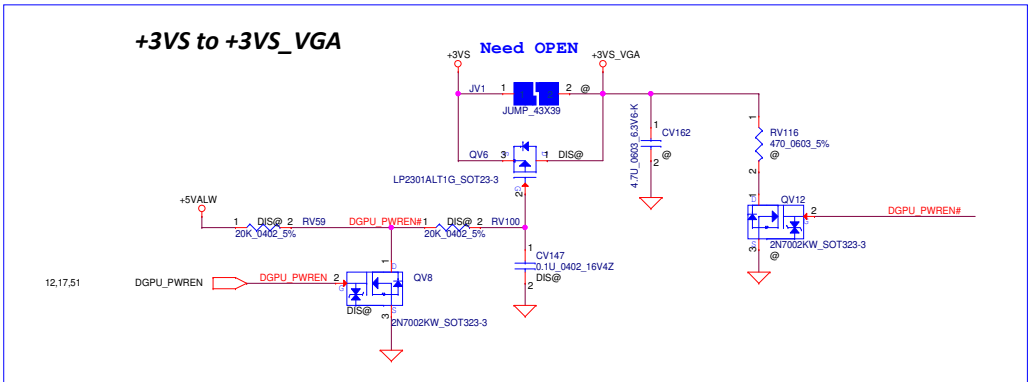
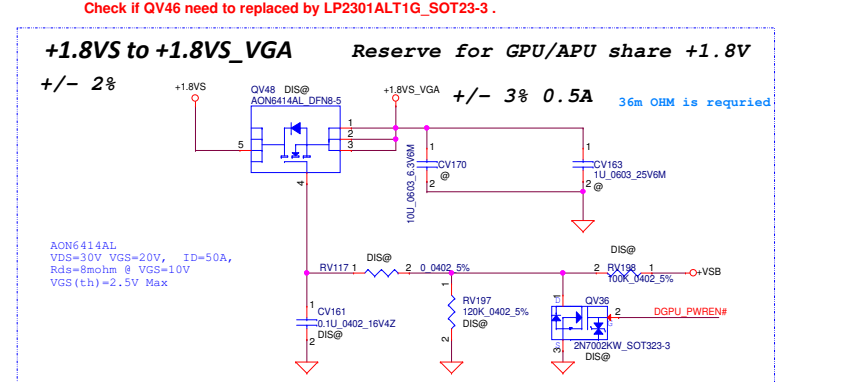
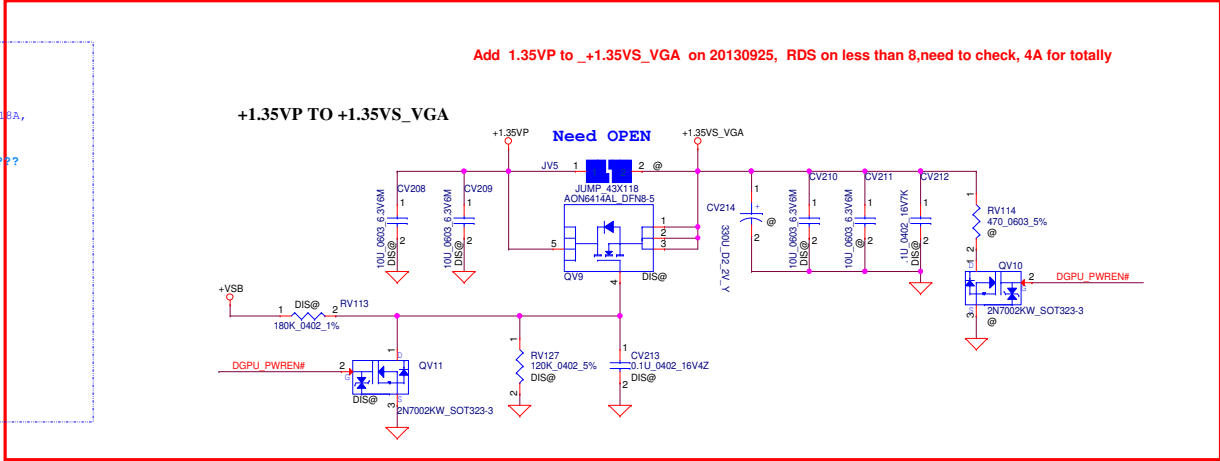
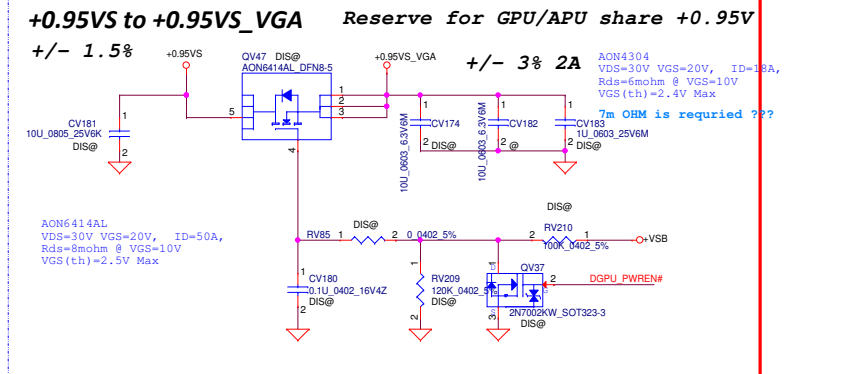
Memory Partition A - Lower 32 bits



Memory Partition A - Upper 32 bits



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Topaz & Jet DDR3 VRAM	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Document Number	Date		Rev	
		Monday, December 16, 2013		1.A	



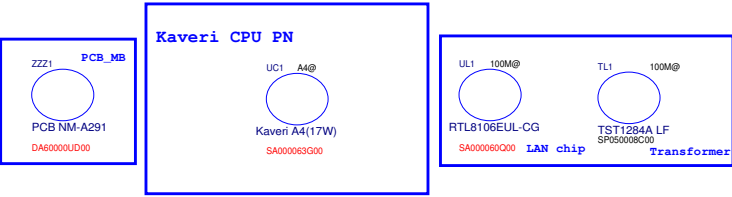
reserve RV167 change to 10 ohm to meet power off sequence on 1202

Security Classification	LC Future Center Secret Data			Title	Topaz & Jet SWITCH POWER
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Size	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Date:	Monday, December 16, 2013	Sheet	24	of	65

BLANK



Security Classification	LC Future Center Secret Data			Title	Topaz & Jet BLANK	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	Size	Document Number	Rev
				Custom	ACLU7	0.4
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</small>				Date:	Monday, December 16, 2013	Sheet 25 of 65

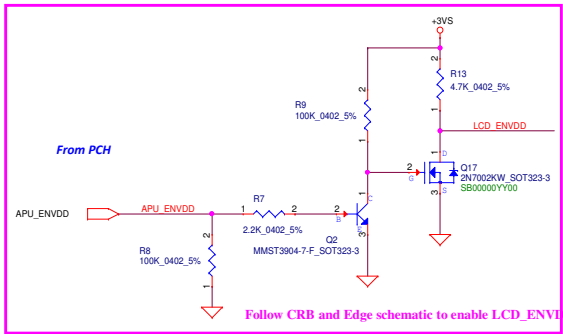




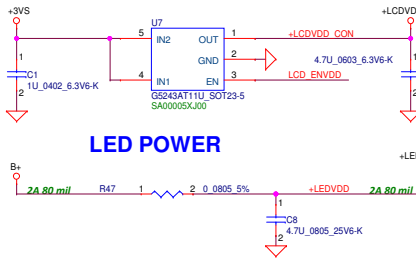
Board ID

BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Stuff Resistor
0	0	0	0	BDW + Jet-LE sku	RC107,RC108,RC109,RC123
0	0	1	0	BDW + Topaz-XT sku	RC107,RC108,RC102,RC123
0	1	0	0	BDW + N15V-GM sku	RC107,RC101,RC109,RC123
0	1	1	0	BDW + N158-GT sku	RC107,RC101,RC102,RC123
1	0	0	0	HSW + Jet-LE sku	RC100,RC108,RC109,RC123
1	0	1	0	HSW + Topaz-XT sku	RC100,RC108,RC102,RC123
1	1	0	0	HSW + N15V-GM sku	RC100,RC101,RC109,RC123
1	1	1	0	HSW + N158-GT sku	RC100,RC101,RC102,RC123
0	0	0	1	BDW + UMA sku	RC107,RC108,RC109,RC123
1	0	0	1	HSW + UMA sku	RC100,RC108,RC109,RC123

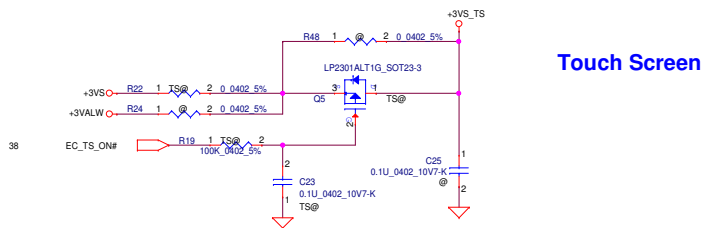
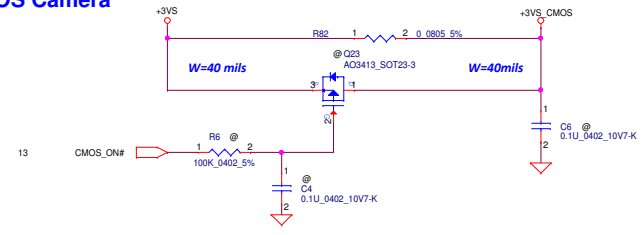
Security Classification	LC Future Center Secret Data		Title	 
Issued Date	2013/08/05	Deciphered Date	2013/08/05	
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</small>				Size C Document Number ACL07 Date: Monday, December 16, 2013 Sheet 26 of 52
				Rev 0.1



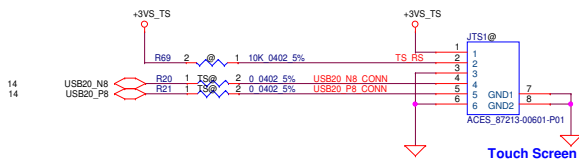
LCD POWER CIRCUIT



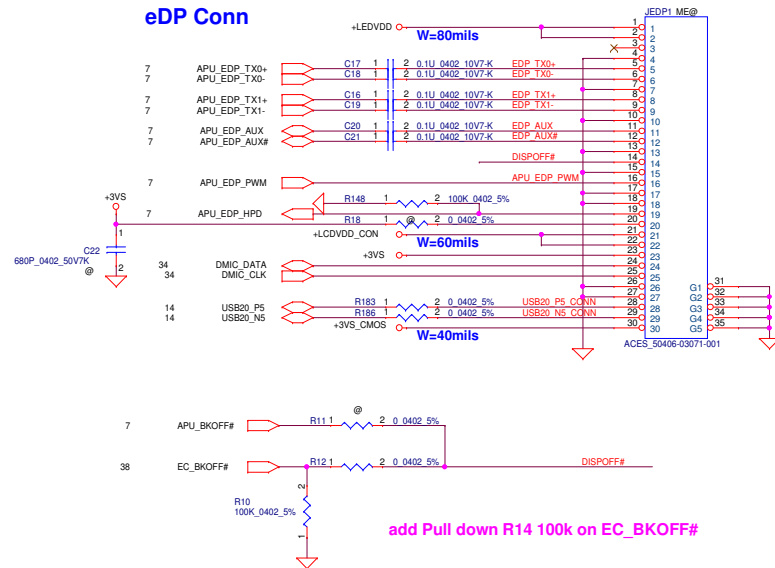
CMOS Camera



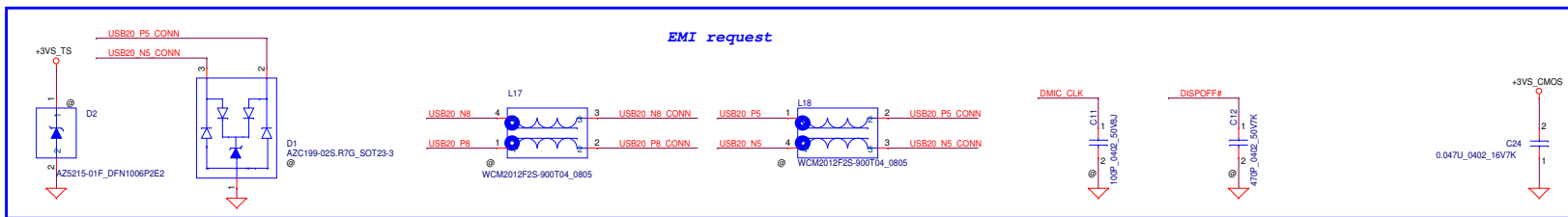
Touch Screen reserved

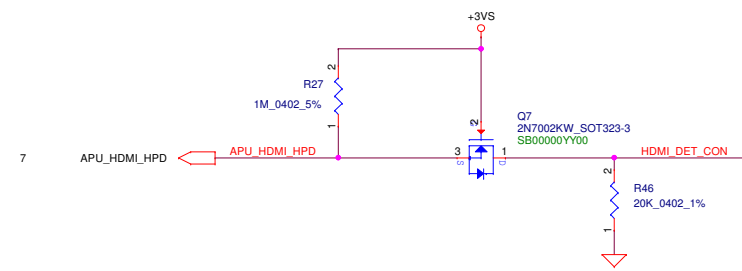
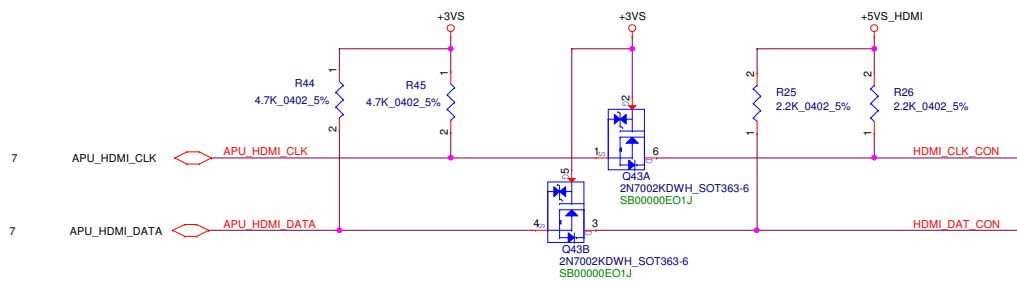


eDP Conn

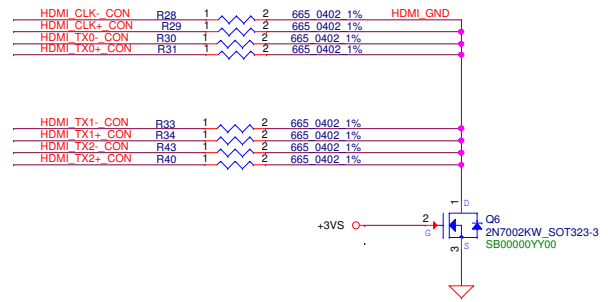
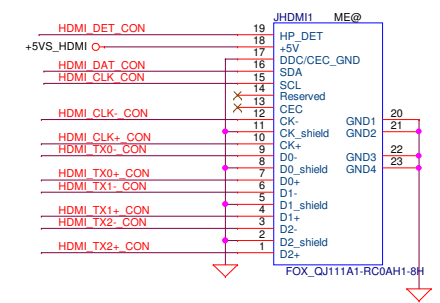
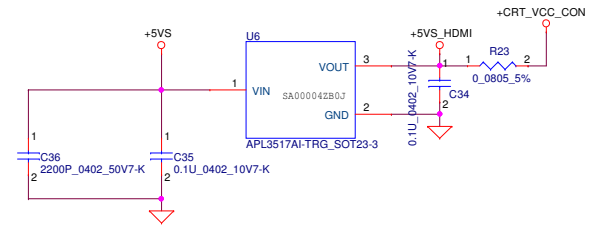
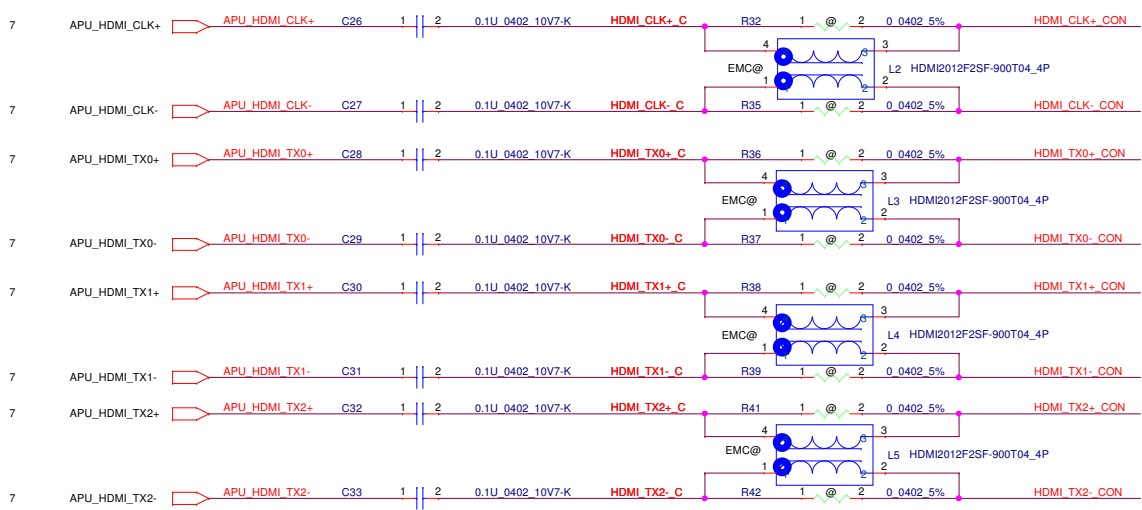


EMI request

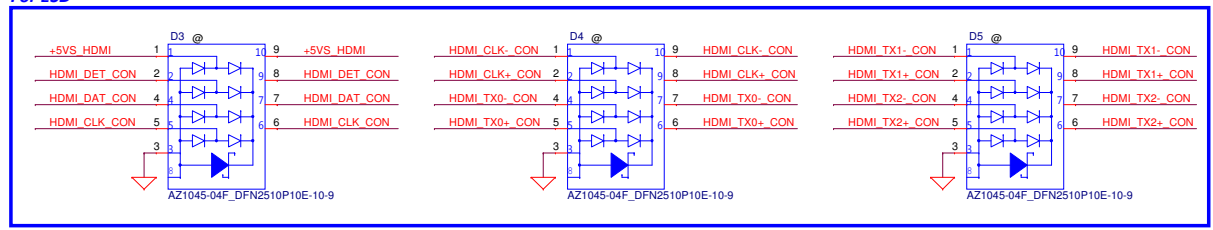




+CRT_VCC_CON and +5VS_HDMI trace width 100 mils

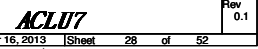


For ESD

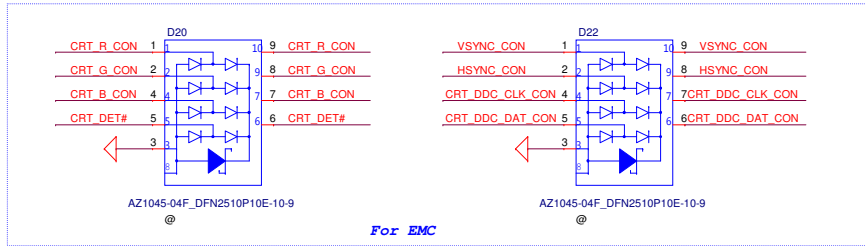
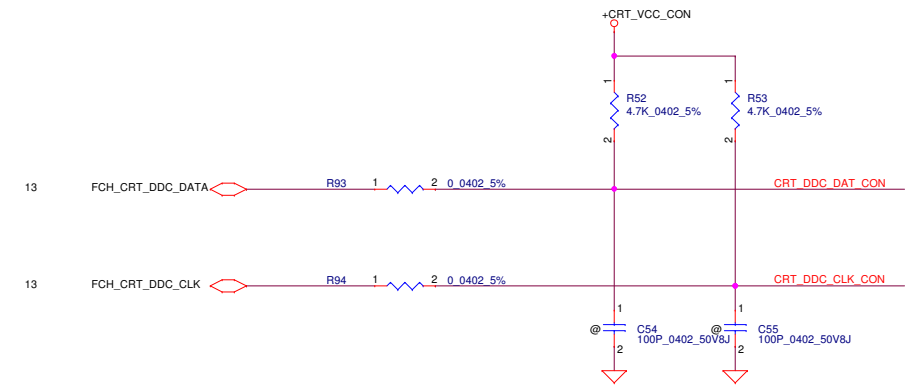
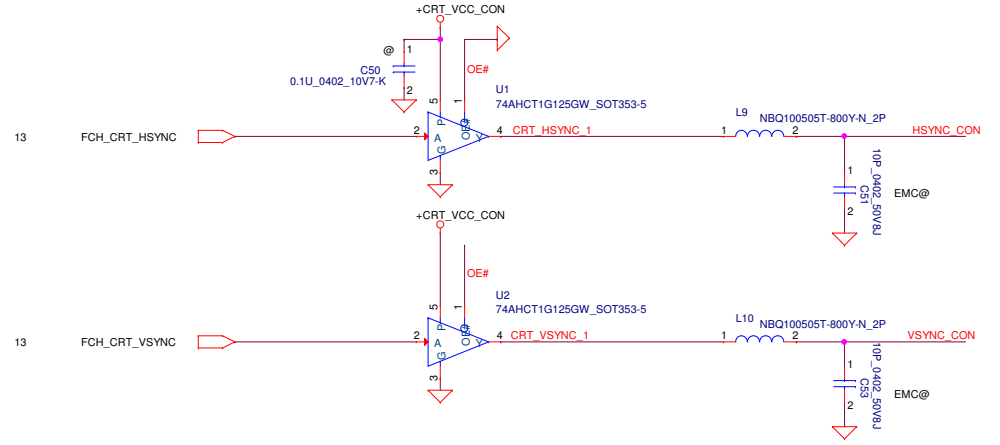
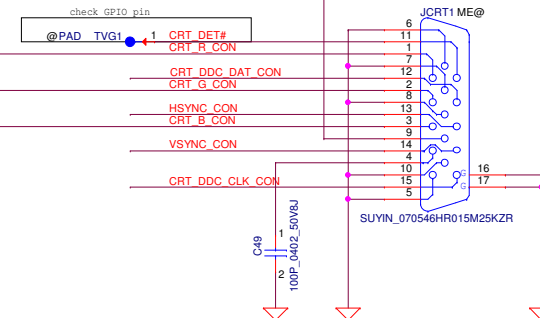
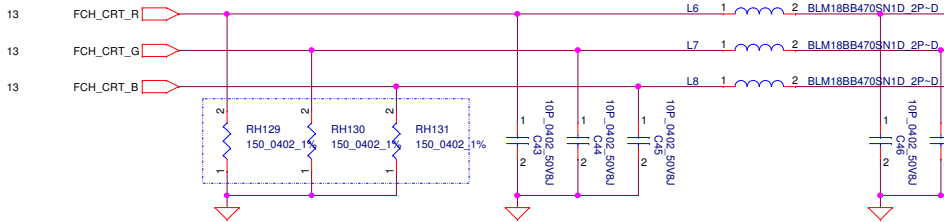
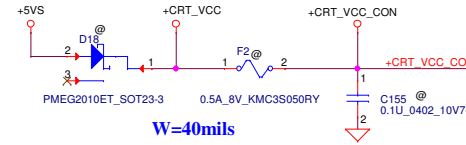


Security Classification	LC Future Center Secret Data		Title
Issued Date	2013/08/08	Deciphered Date	2013/08/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

Title		Rev
HDMI_CONN		0.1
Date:	Monday, December 16, 2013	Sheet 28 of 52



CRT Connector



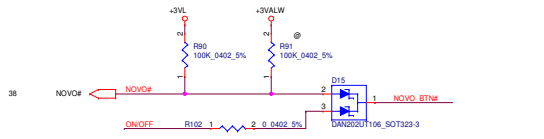
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

Title	CRT_CONN		
Document Number	Custom	Rev	0.1
Date:	Monday, December 16, 2013	Sheet	29 of 52



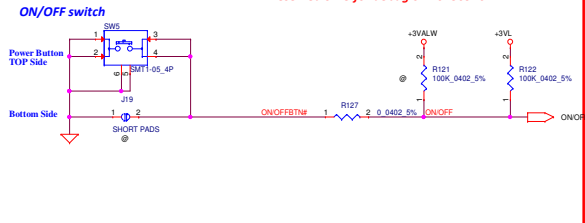
ACLU7

ON/OFF switch

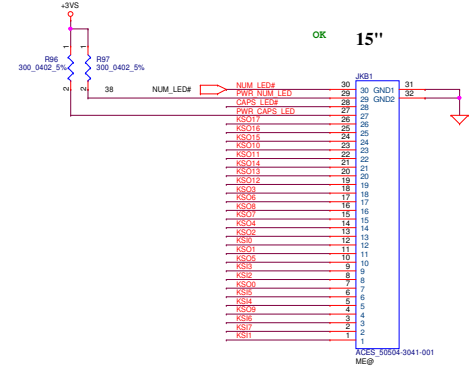
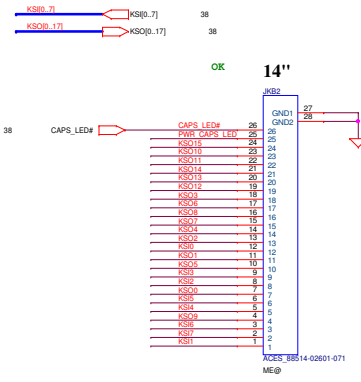


Power Button

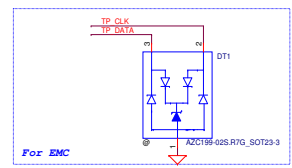
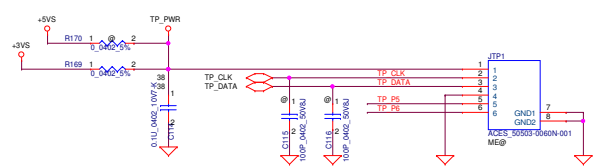
Reserved SW5 for debug on 20130926



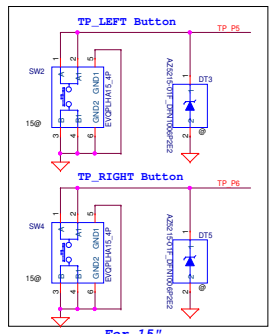
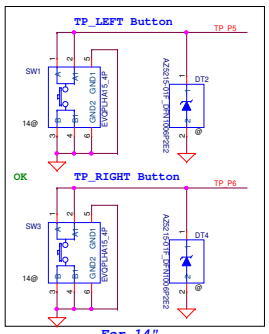
K/B Connector



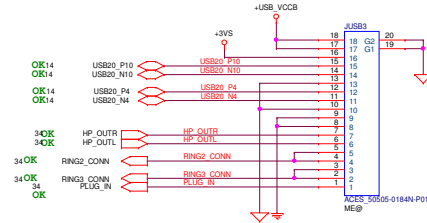
TP/B Connector



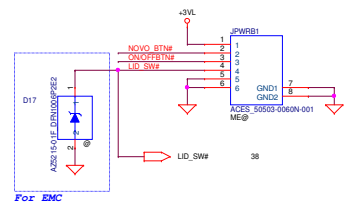
For 14"		For 15"	
1	VDD	1	VDD
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	GND
5	TP-L	5	TP-L
6	TP-R	6	TP-R



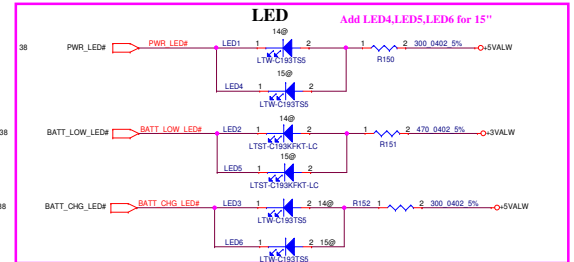
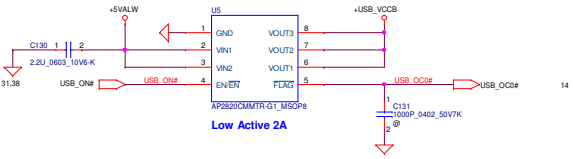
USB I/O Connector



PWR/B Connector

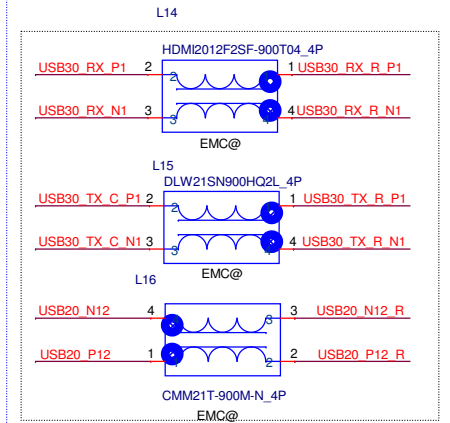
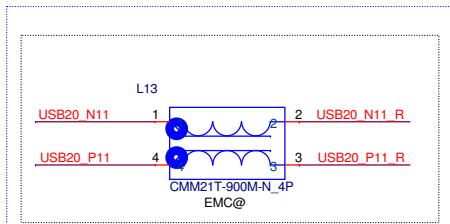
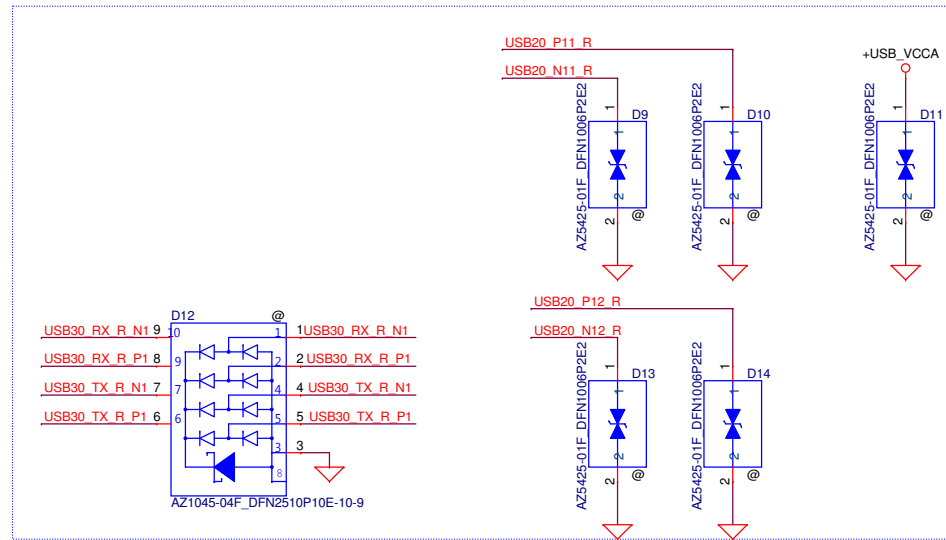
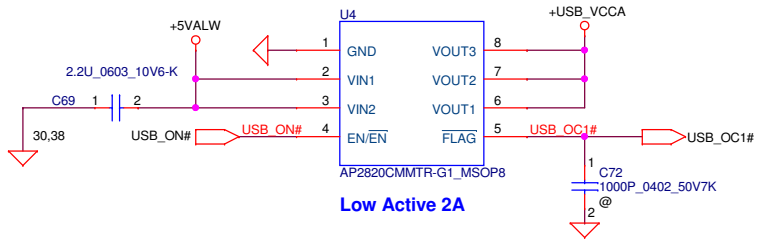


Right Side USB2.0 Port X 1 (USB/B)

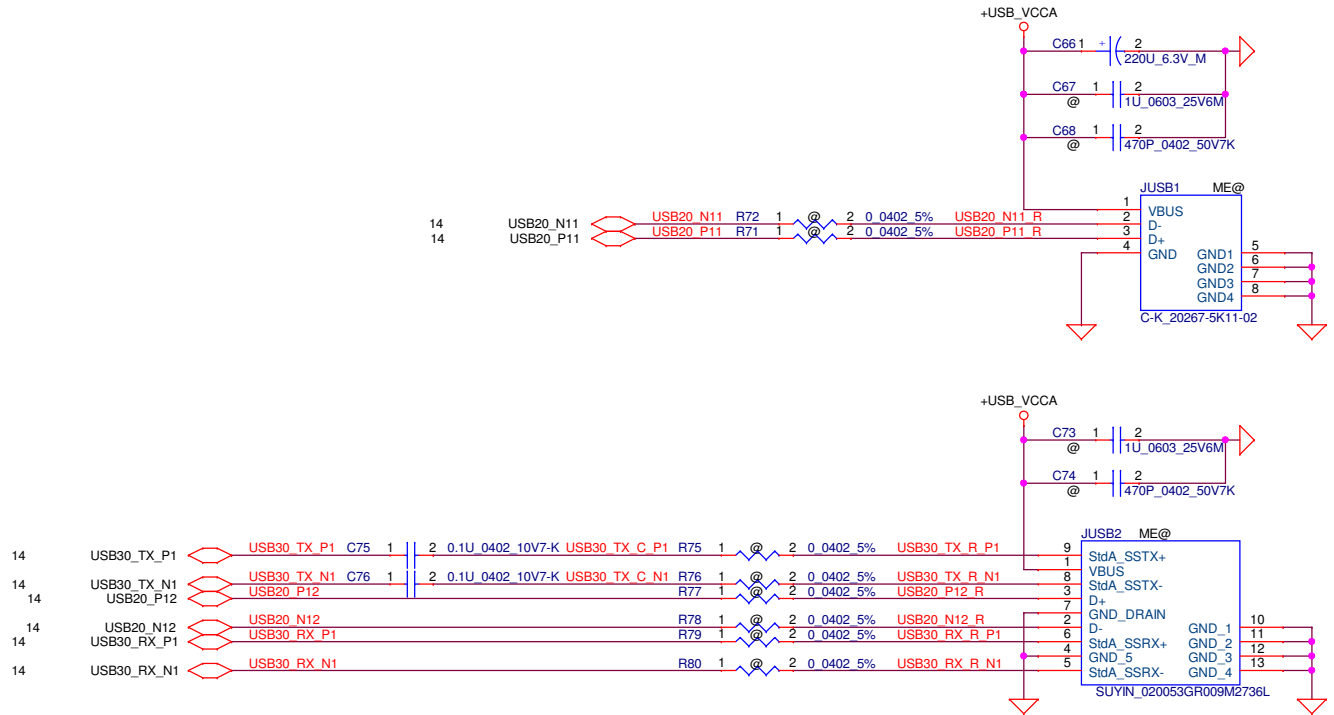


Delete JLED1 on due to both G14 and G15 move LED to MB

LEFT SIDE USB3.0 PORT X2



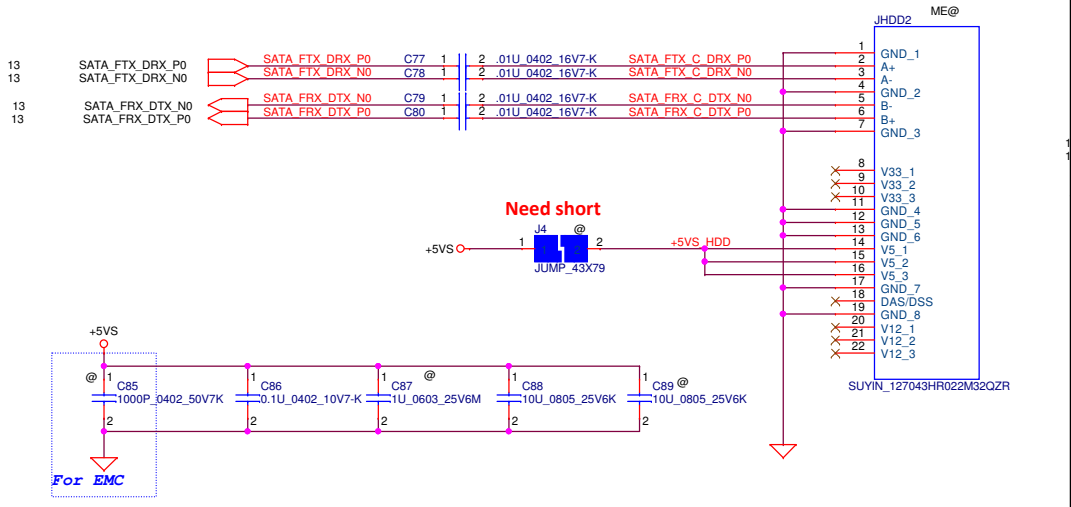
For EMC



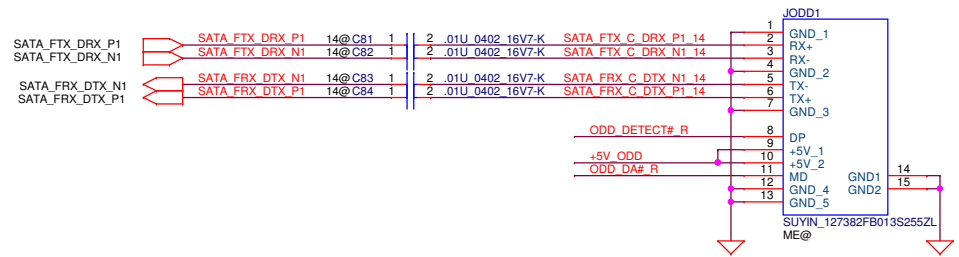
Security Classification		LC Future Center Secret Data	
Issued Date	2013/08/08	Deciphered Date	2013/08/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

Title		
USB 3.0 PORT (LEFT)		
Size	Document Number	
Custom		
Date:	Monday, December 16, 2013	Sheet 31 of 52

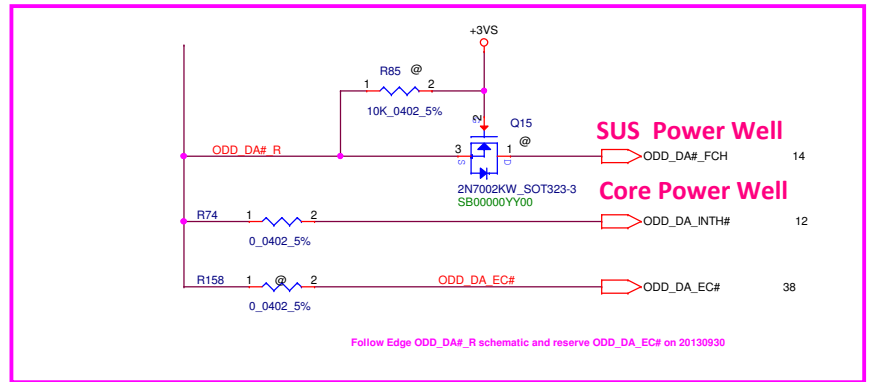
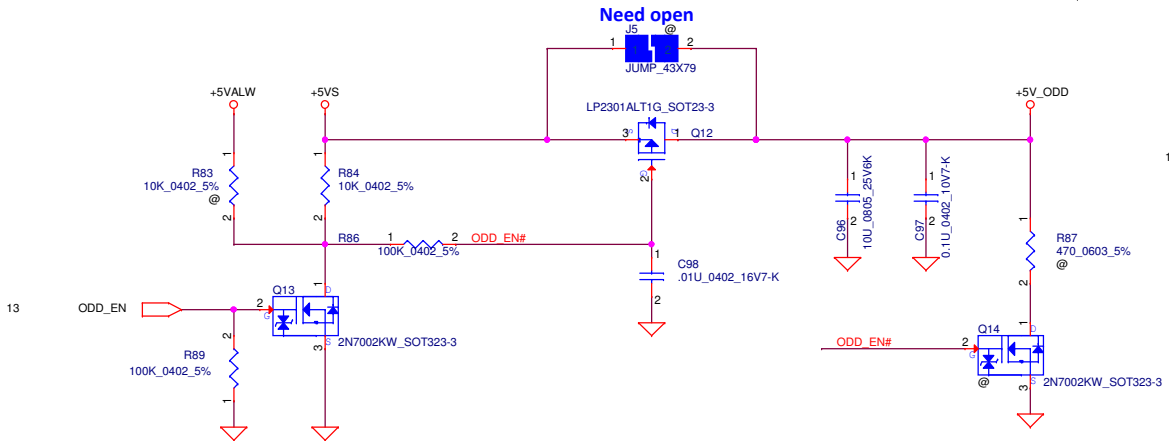
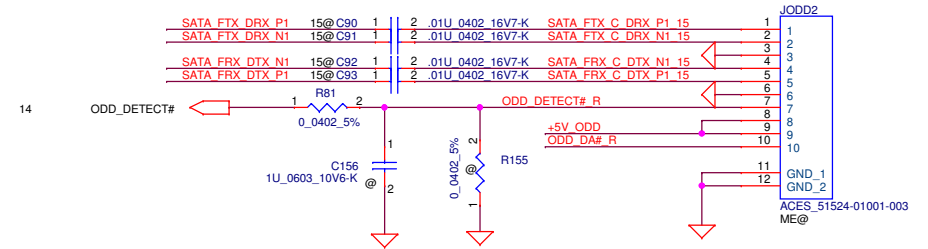
SATA HDD Conn.



FOR 14" SATA ODD Conn.

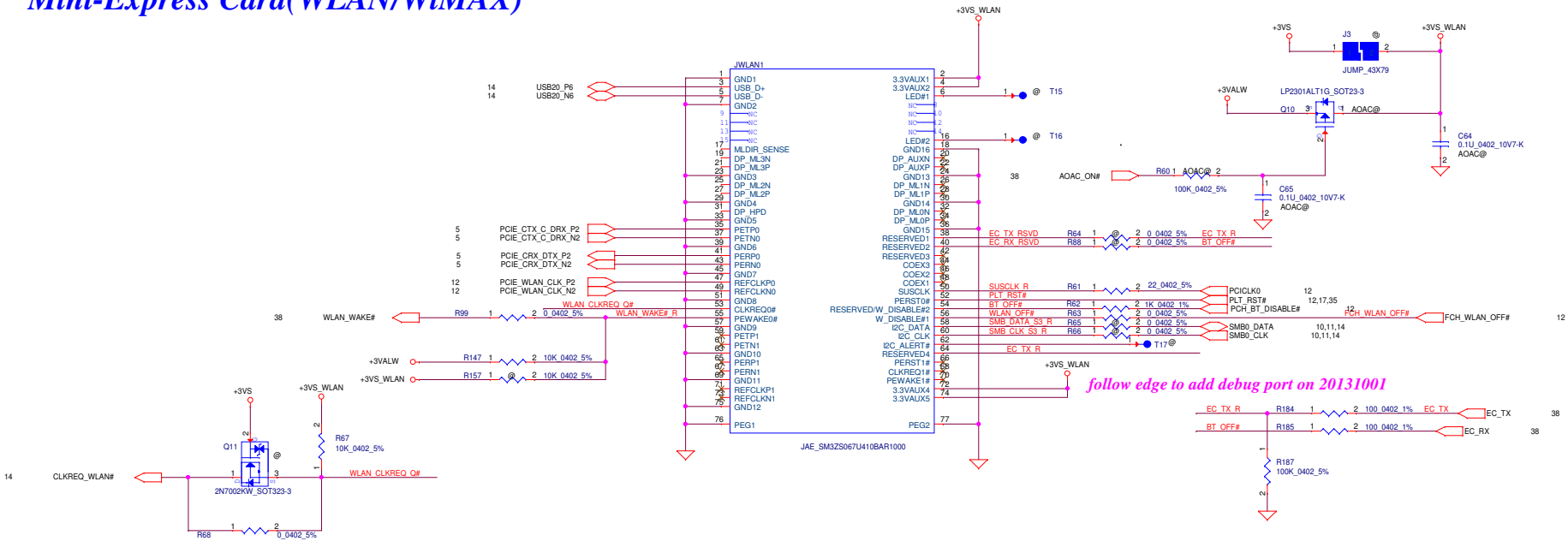


FOR 15" SATA ODD FFC Conn



Security Classification				LC Future Center Secret Data				Title	
Issued Date		2013/08/08		Deciphered Date		2013/08/05		HDD/ODD CONN	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.									
Size	Document Number	ACLU7		Rev	0.1				
Date:	Monday, December 16, 2013	Sheet	32	of	52				

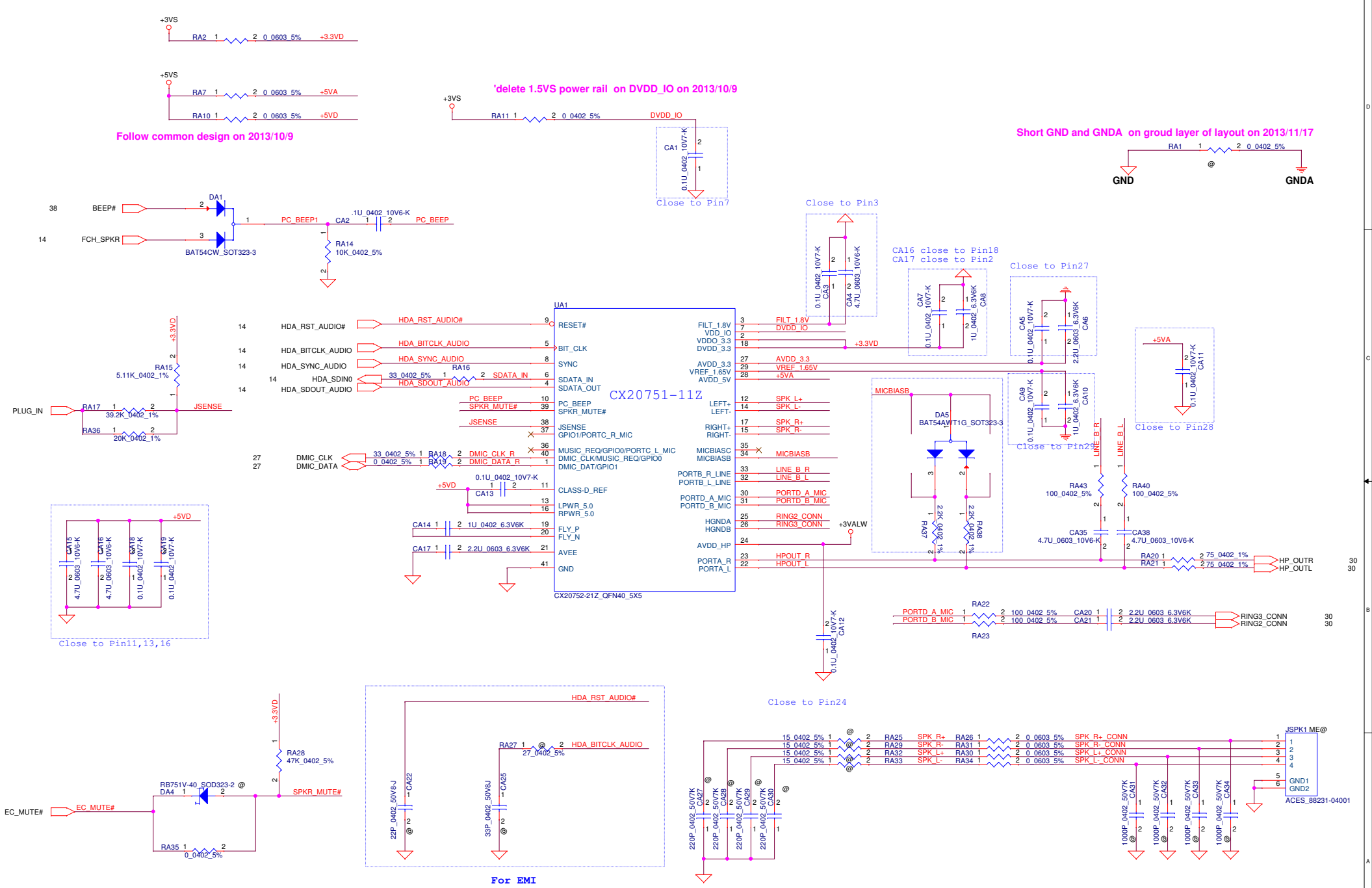
Mini-Express Card(WLAN/WiMAX)




Connect CLKREQ_WLAN# and WLAN_CLKREQ_Q# directly and reserve Q11 on 20131004

Change R67 power rail from 3VS to +3VS_WLAN on 20131011

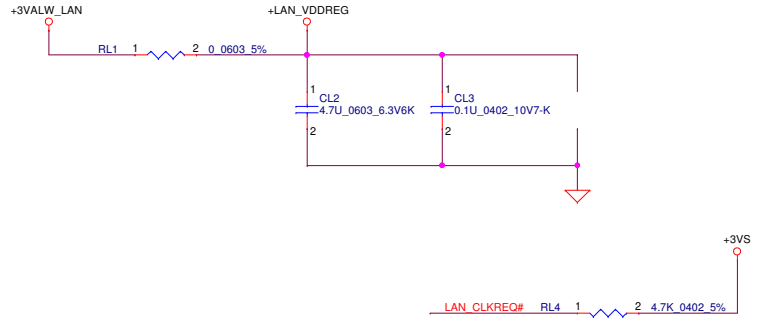
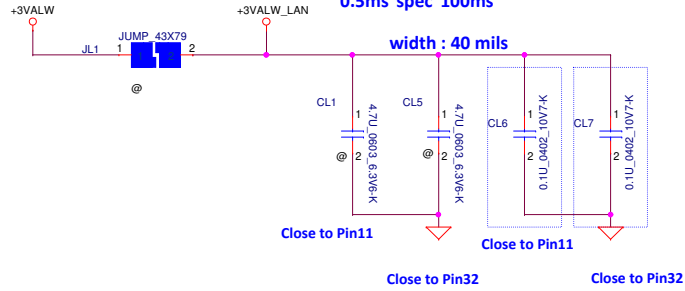
Security Classification	LC Future Center Secret Data		Title
Issued Date	2013/08/08	Deciphered Date	2013/08/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			
Size	Document Number	Rev	0.1
Date:	Monday, December 16, 2013	Sheet	33 of 52



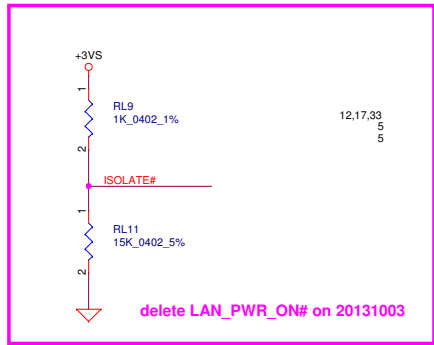
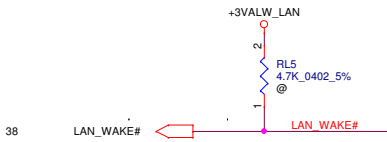
Security Classification				LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Size	Document Number		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.							
Date:	Monday, December 16, 2013	Sheet	34	of	52	Rev	0.1

+3VALW TO +3VALW_LAN

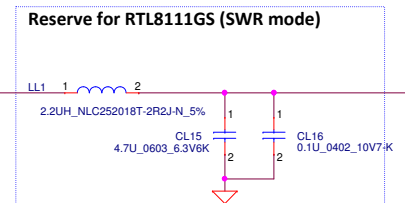
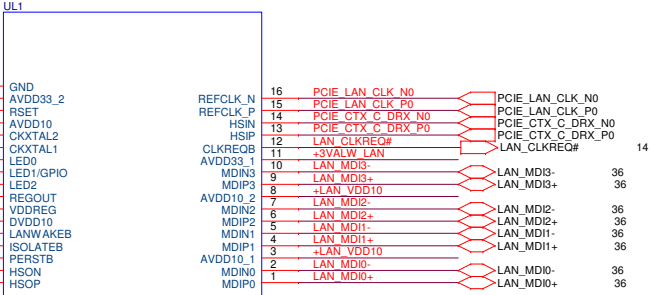
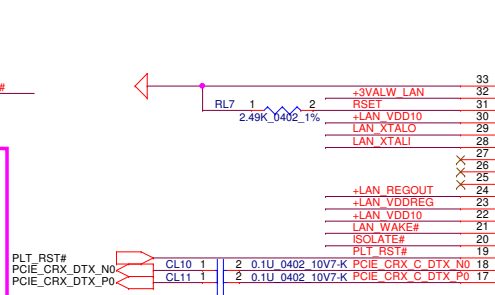
+3VALW_LAN rising time (10%~90%):
0.5ms spec 100ms



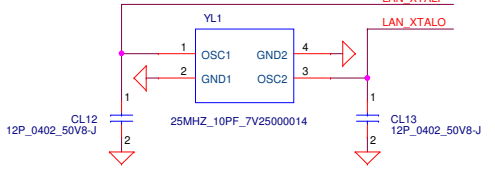
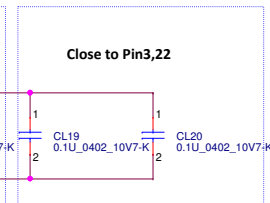
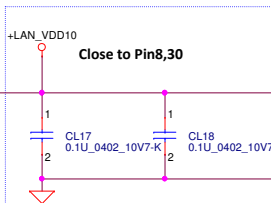
Vendor recommend reserve the PU resistor close LAN chip



delete LAN_PWR_ON# on 20131003

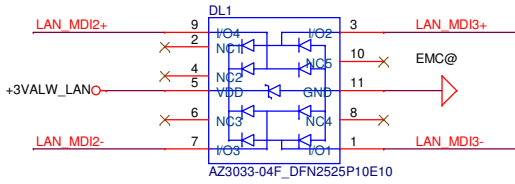


Layout Note: LL1 must be within 200mil to Pin36, CL15, CL16 must be within 200mil to LL1 +LAN_REGOUT: Width = 60mil

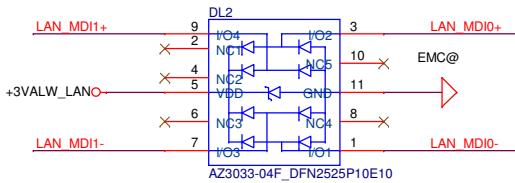


Security Classification	LC Future Center Secret Data		Title
Issued Date	2013/08/08	Deciphered Date	2013/08/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			Size Custom
			Document Number
			ACL07
			Rev 0.1
			Date: Monday, December 16, 2013 Sheet 35 of 52

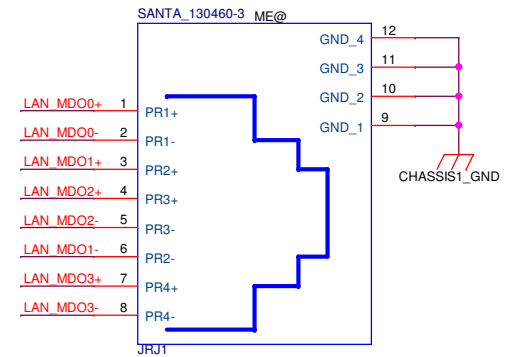
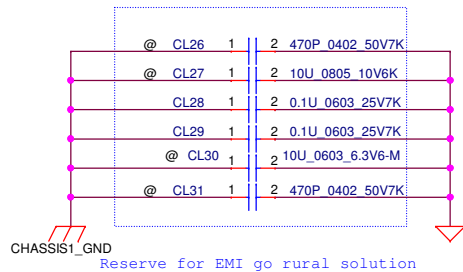
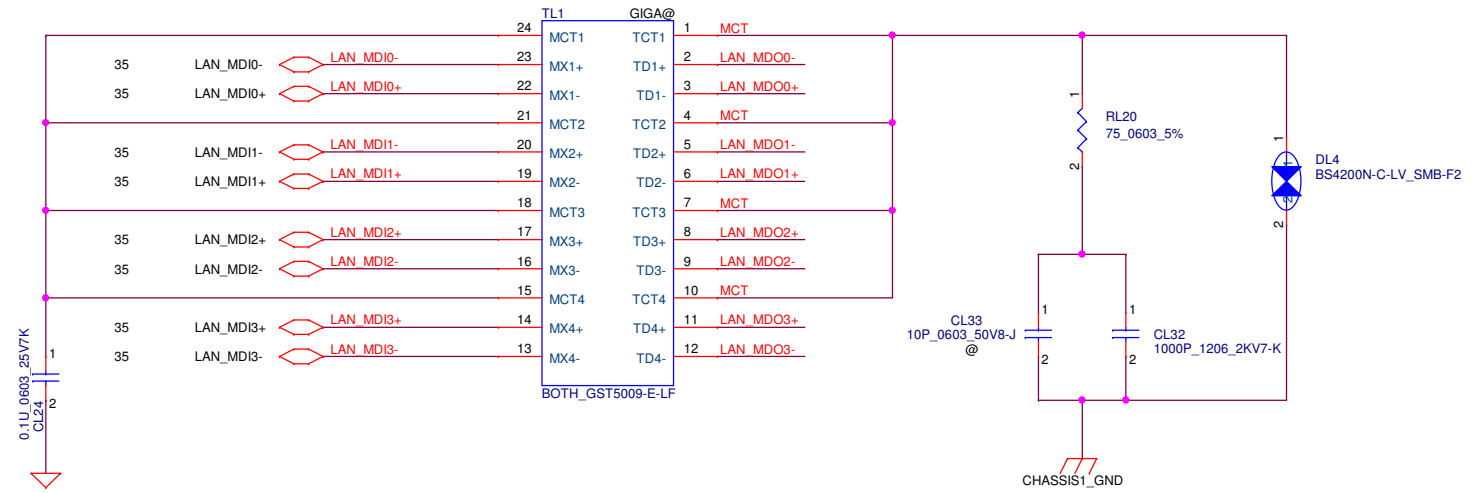
DL1/DL2
1'S PN:SC300003M00



Place Close to TL1

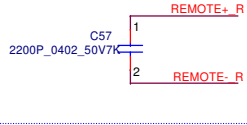


Place Close to TL2

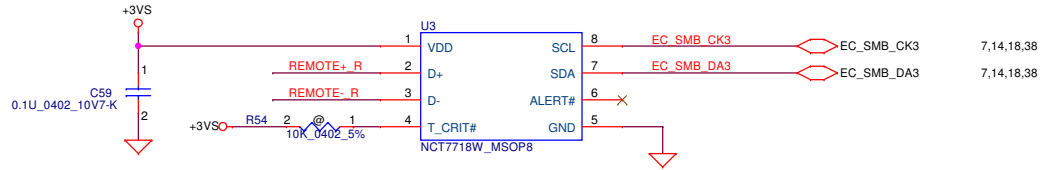


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	LAN_Transformer	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number
				B	ACLU7
				Date:	Monday, December 16, 2013
				Sheet	36 of 52
				Rev	0.1

Close U3



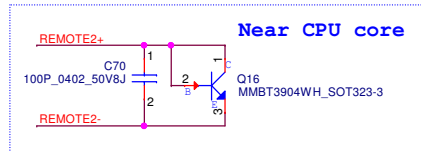
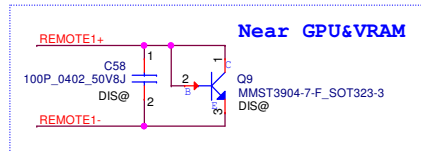
SMSC thermal sensor placed near DIMM



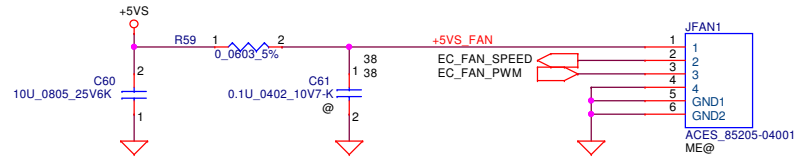
Address 1001_101xb



REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space: 10/10 mil
Trace length: <8"

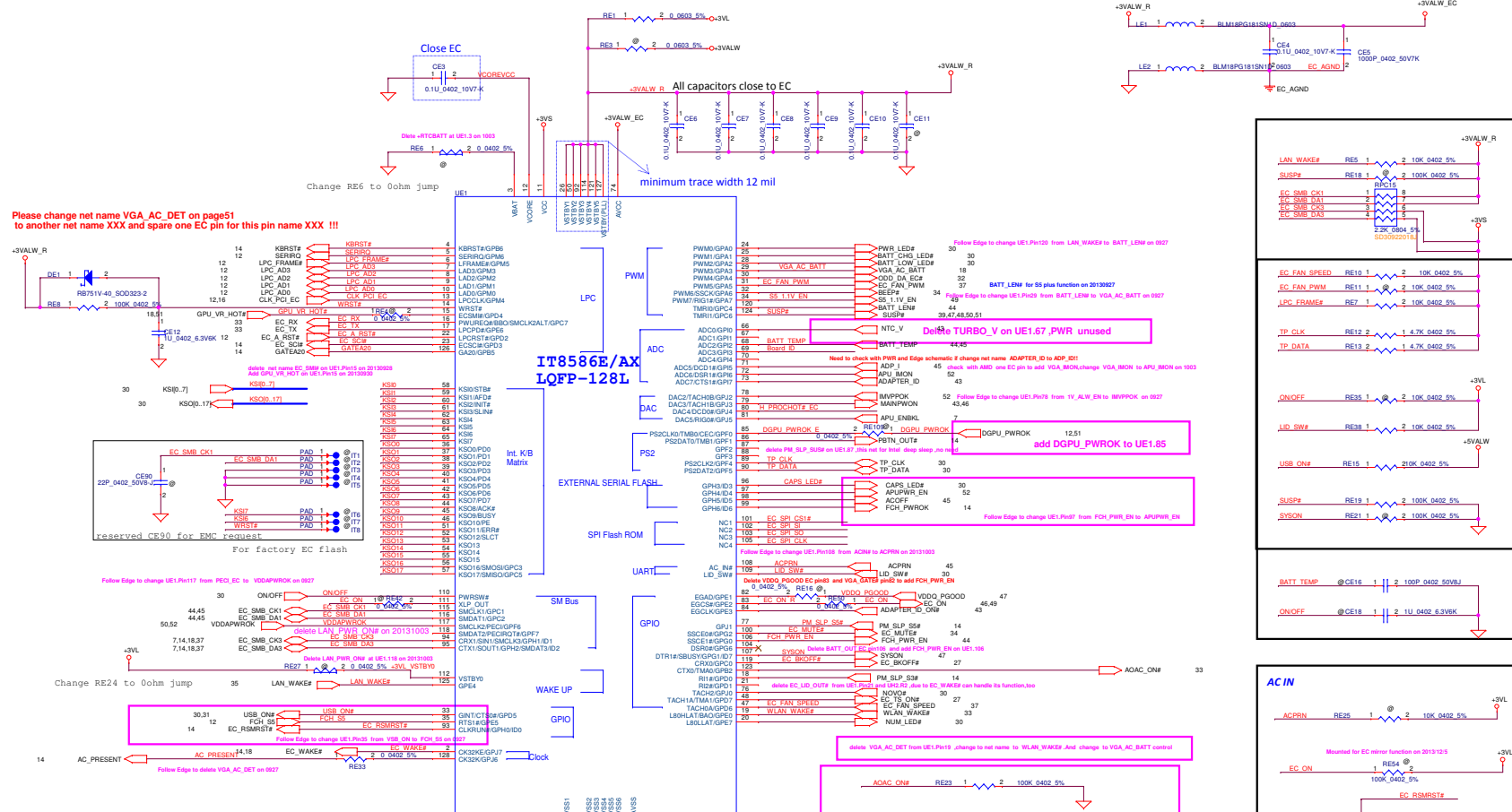


FAN Conn



Security Classification	LC Future Center Secret Data	
Issued Date	2013/08/08	Deciphered Date 2013/08/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.		

Title		
Thermal sensor/FAN CONN		
Size Custom	Document Number	Rev 0.1
Date: Monday, December 16, 2013	Sheet 37 of 52	



Please change net name VGA_AC_DET on page51 to another net name XXX and spare one EC pin for this pin name XXX !!!

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

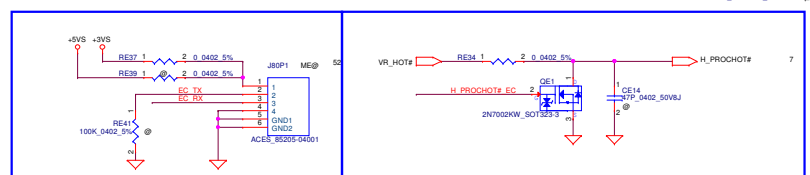
When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003

When LAN_PWR_ON at UE1.118 on 20131003
Delete LAN_PWR_ON at UE1.118 on 20131003



when mirror, RE45 RE47 RE48 RE49 mounted
when no mirror, RE45 RE47 RE48 RE49 reserved

EC SPI_CS1# RE45 2 1 0.0402 5% SPI_CS1#
EC SPI_SI RE47 2 1 0.0402 5% SPI_SI
EC SPI_SO RE48 2 1 0.0402 5% SPI_SO
EC SPI_CLK RE49 2 1 0.0402 5% SPI_CLK

Mounted RE43 for EC mirror function on 20131215

when mirror, GP22 pull high
when no mirror, GP22 pull low

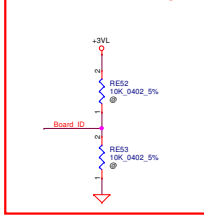
Mounted RE43 for EC mirror function on 20131215

EC MUTE# RE43 2 1 10K 0.402 5%
RE46 2 1 10K 0.402 5%
RE44 2 1 100K 0.402 5%

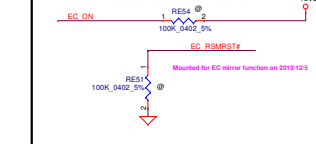
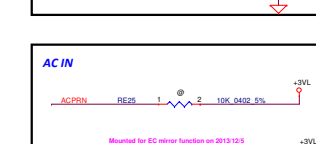
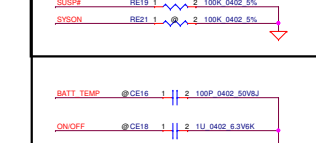
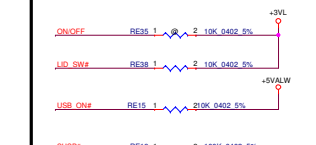
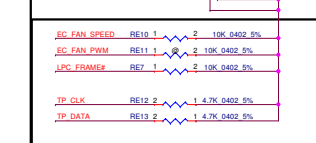
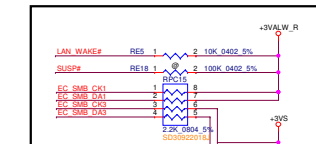
EMI/ESD

EC_A_RST# CE1 2 20P 0.402 50V7K
CLK_PCl_EC RE2 1 2 10 0.402 5%
SYN0N CE2 1 10P 0.402 50V7K
CE11 1 10P 0.402 50V7K
CE12 1 10P 0.402 50V7K
CE19 1 10P 0.402 50V7K

Add Board ID, please check with Edge

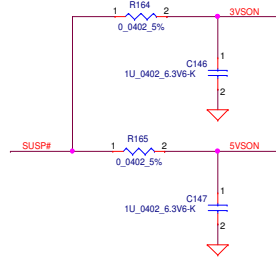
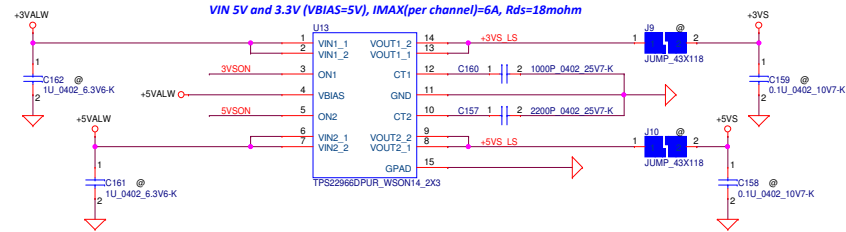


Vcc	3.3V +/- 5%				
RE33	100K +/- 1%				
Board ID	RE34	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



Load Switch
+5VALW To +5VS
+3VALW To +3VS

+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms



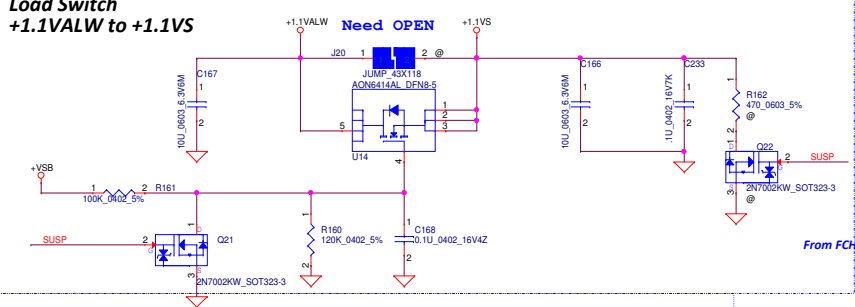
R164 and R165 to adjust 3VALW and 5VALW timing

Delete +3VALW To +3VALW_FCH on 20131001

Load Switch
+1.1VALW to +1.1VS

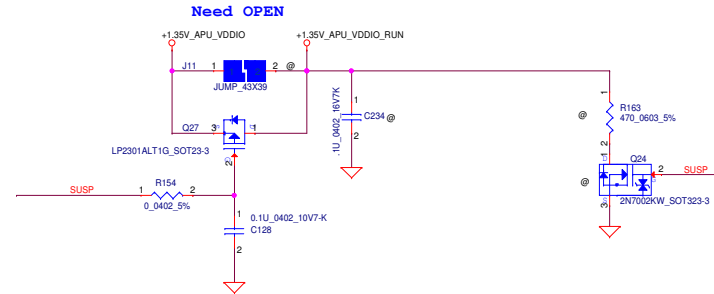
1.1VS :4A

Update Load Switch +1.1VALW to +1.1VS to AON6414AL on 20130926

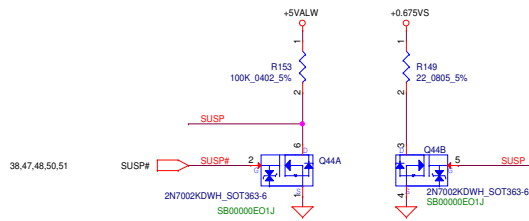


From FCH

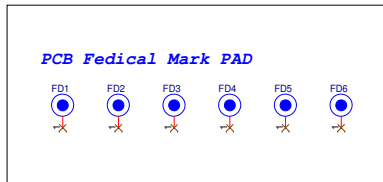
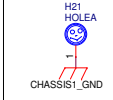
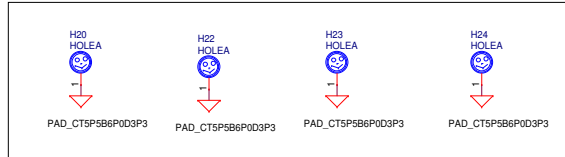
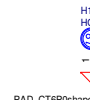
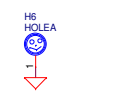
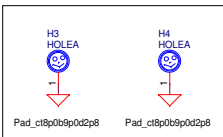
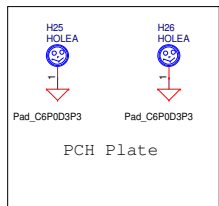
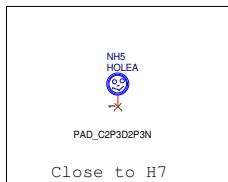
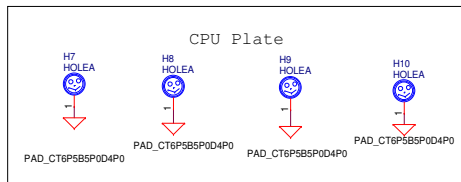
+VDDIO to +VDDIO_RUN



For DisCharge



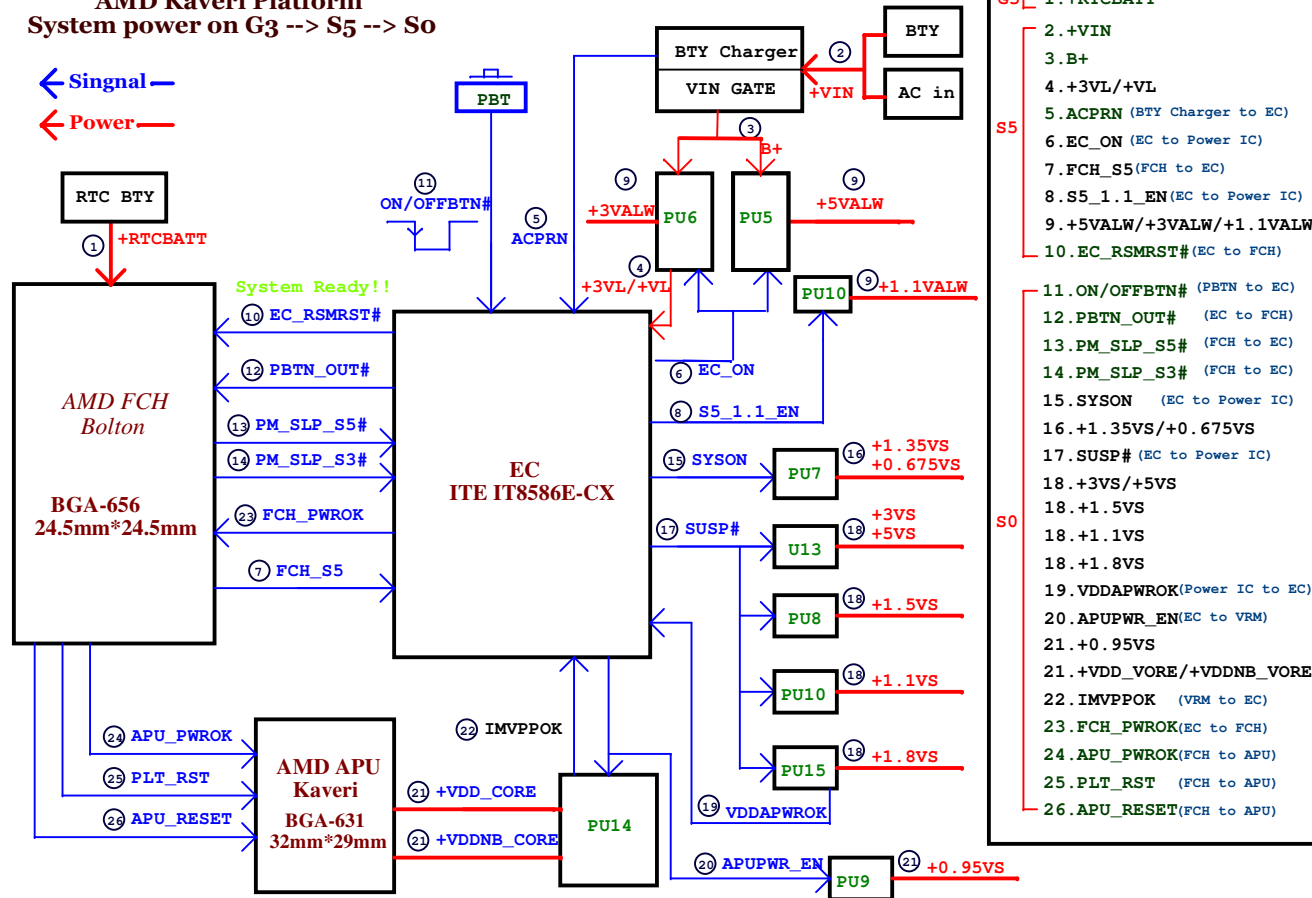
Short +1.35V_DDR_VDDIOSUS & +1.35V_APU_VDDIO directly on 20130930



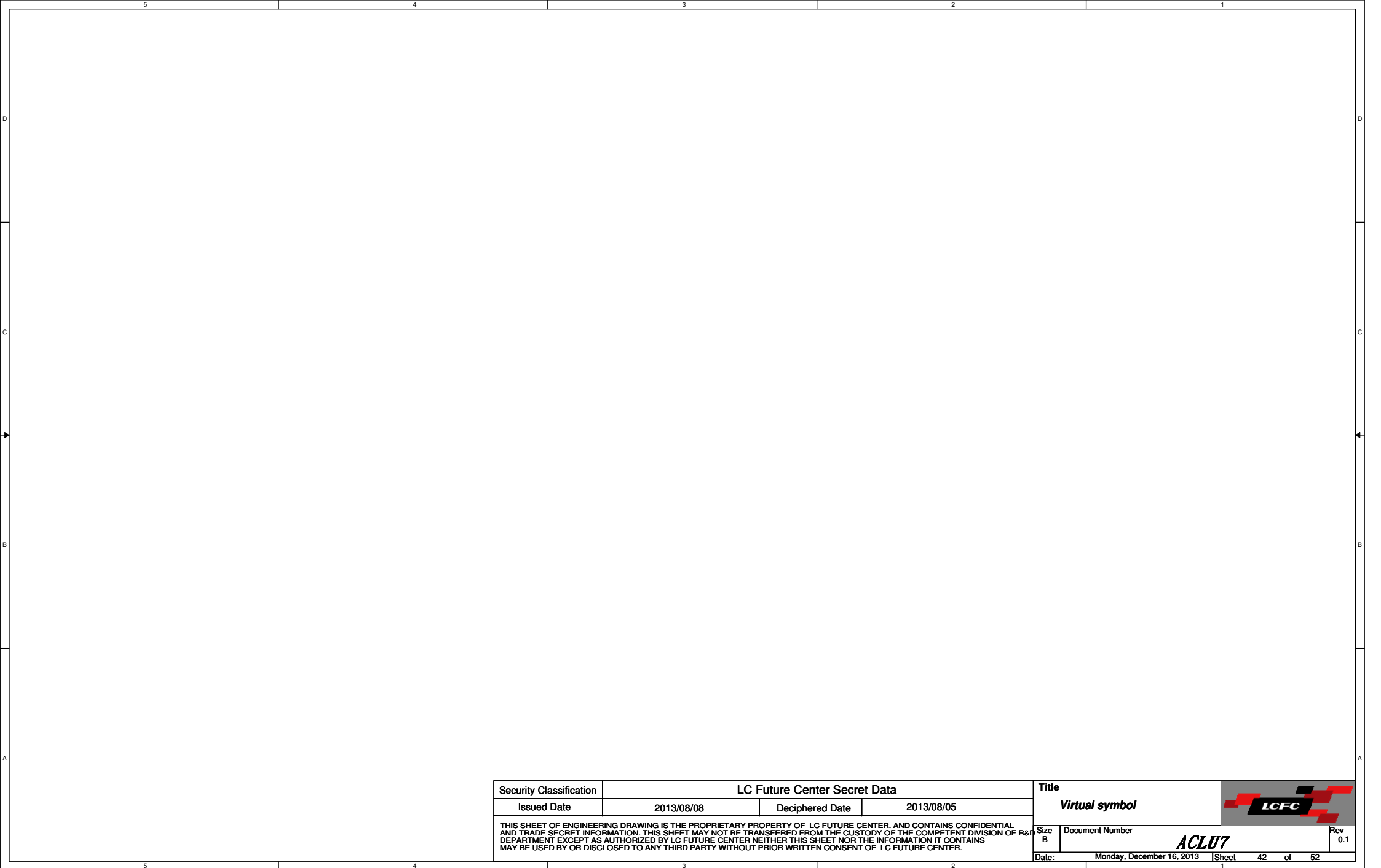
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	SCREW	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size	Custom	Document Number	ACLU7		Rev
Date:	Monday, December 16, 2013	Sheet	40	of	52


AMD Kaveri Platform System power on G3 --> S5 --> S0

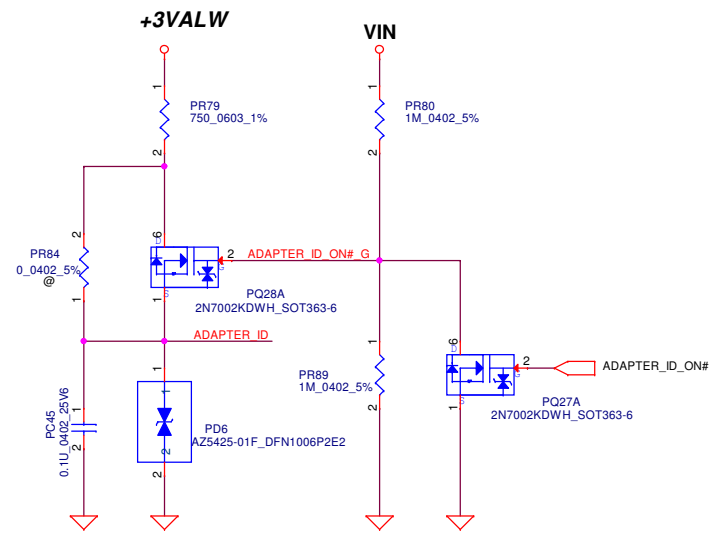
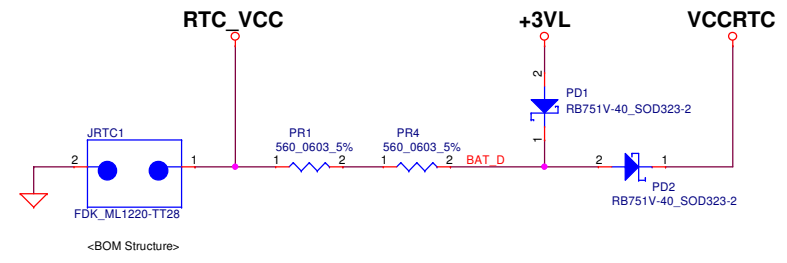
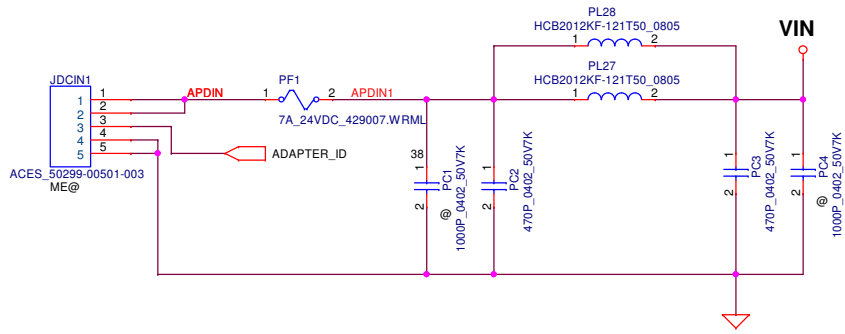
← Signal —
← Power —



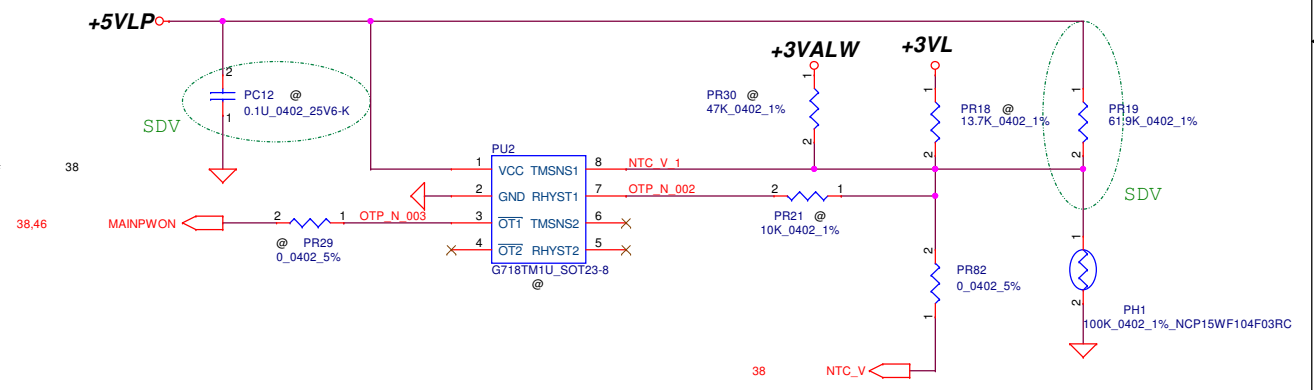
- G3**
1. +RTCBATT
 2. +VIN
 3. B+
 4. +3VL/+VL
- S5**
5. ACPRN (BTY Charger to EC)
 6. EC_ON (EC to Power IC)
 7. FCH_S5 (FCH to EC)
 8. S5_1.1_EN (EC to Power IC)
 9. +5VALW/+3VALW/+1.1VALW
 10. EC_RSMRST# (EC to FCH)
- S0**
11. ON/OFFBTN# (PBTN to EC)
 12. PBTN_OUT# (EC to FCH)
 13. PM_SLP_S5# (FCH to EC)
 14. PM_SLP_S3# (FCH to EC)
 15. SYSON (EC to Power IC)
 16. +1.35VS/+0.675VS
 17. SUSP# (EC to Power IC)
 18. +3VS/+5VS
 18. +1.5VS
 18. +1.1VS
 18. +1.8VS
 19. VDDAPWROK (Power IC to EC)
 20. APUPWR_EN (EC to VRM)
 21. +0.95VS
 21. +VDD_VORE/+VDDNB_VORE
 22. IMVPPOK (VRM to EC)
 23. FCH_PWROK (EC to FCH)
 24. APU_PWROK (FCH to APU)
 25. PLT_RST (FCH to APU)
 26. APU_RESET (FCH to APU)





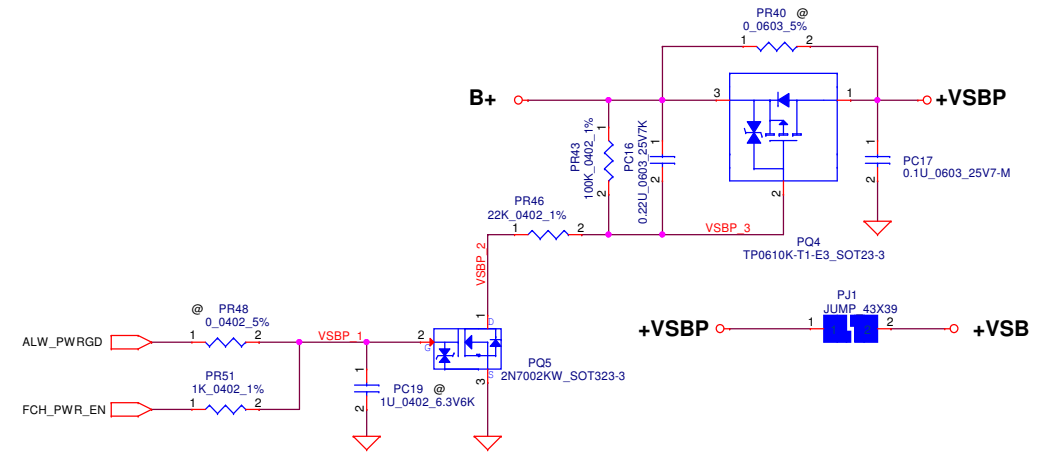
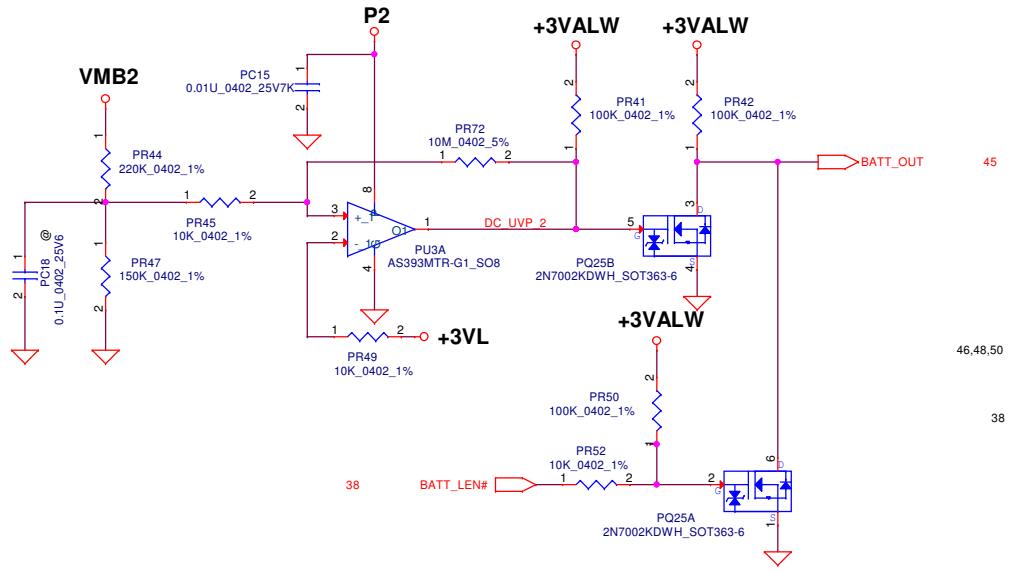
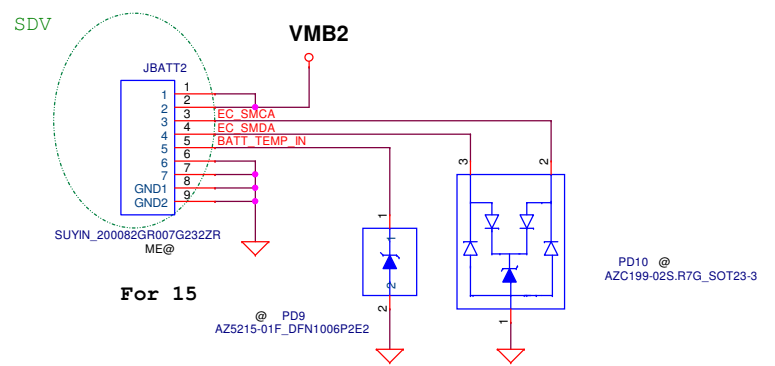
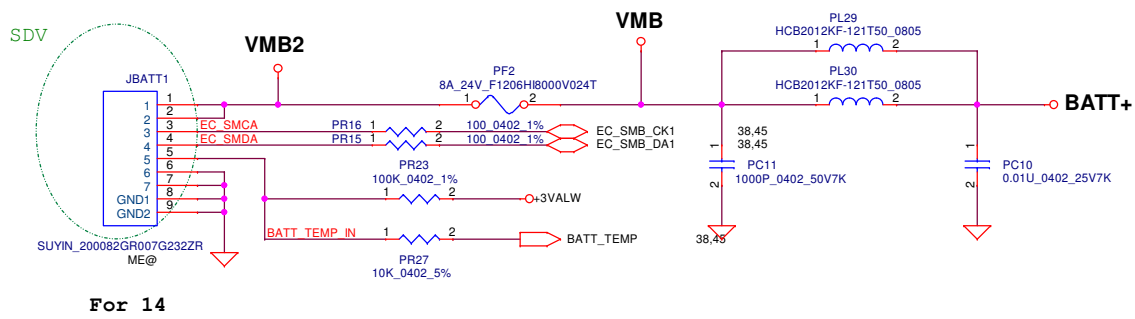
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Virtual symbol		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Document Number	Rev
				B	ACLU7	0.1
				Date:	Monday, December 16, 2013	Sheet 42 of 52



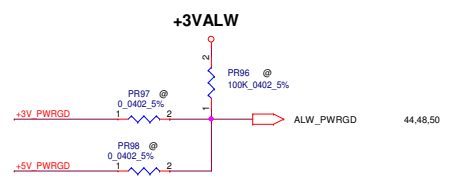
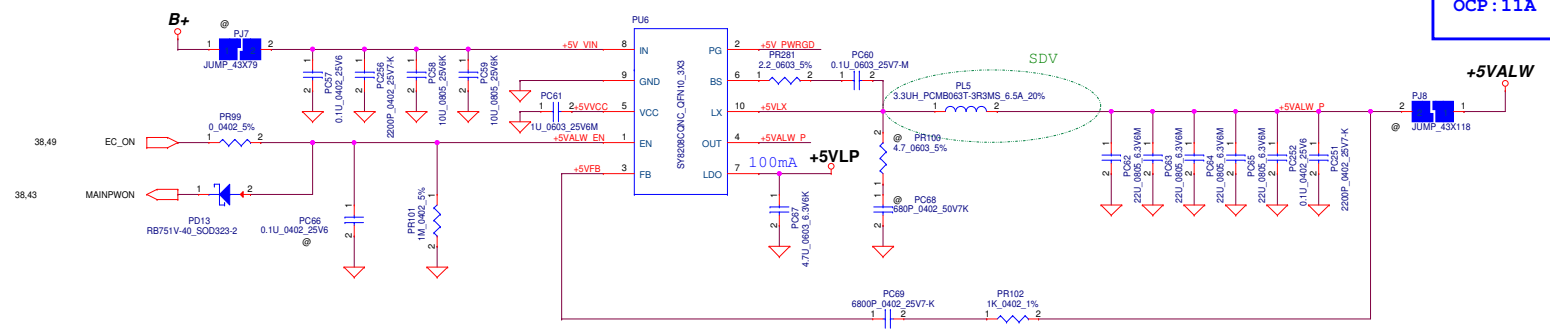
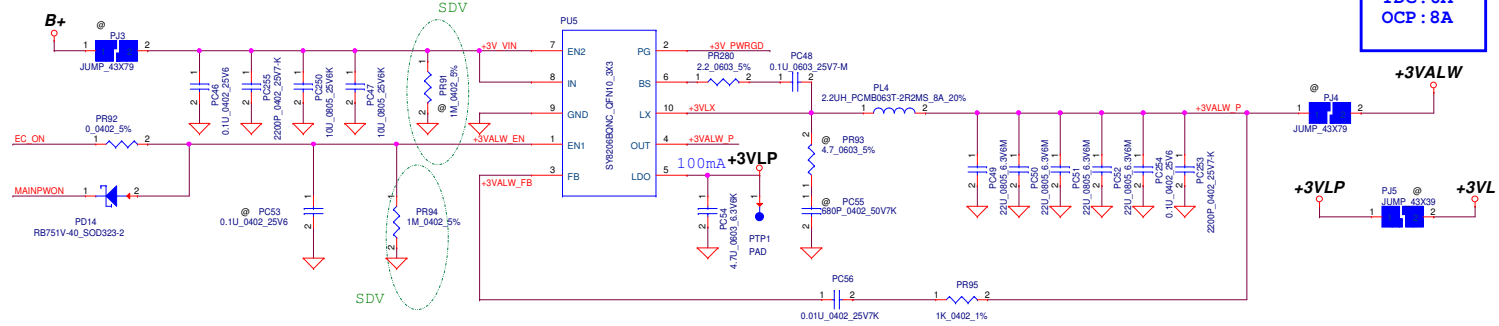
PH1 under CPU bottom side :
CPU thermal protection at 92+-3 degree C
Recovery at 56 +-3 degree C



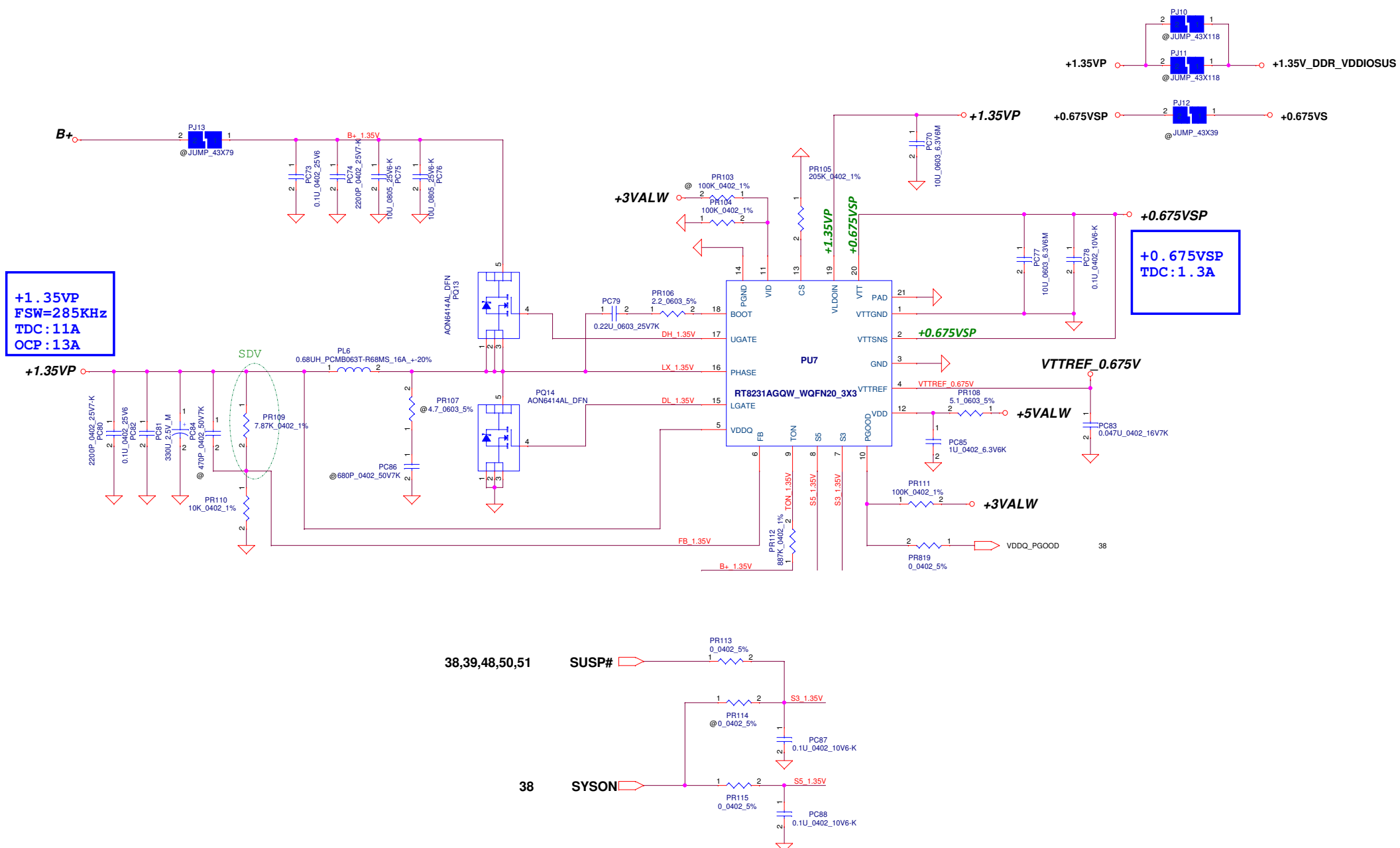
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2013/08/15	Deciphered Date	2013/08/15	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				
Size	Custom	Document Number		
Date:	Monday, December 16, 2013	Sheet	43	of 43



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/15	Deciphered Date	2013/08/15	BATTERY CONN/OTP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
Size Custom	Document Number	G(AND Beema)		Rev	0.1
Date:	Monday, December 16, 2013	Sheet	44	of	44



Security Classification	LC Future Center Secret Data		Title	
Issued Date	2013/08/15	Deciphered Date	2013/08/15	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size
				Document Number
				G(AND Beema)
				Rev
				0.1
				Date: Monday, December 16, 2013 Sheet 46 of 46

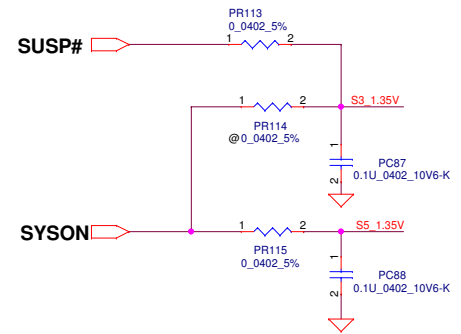


+1.35VP
FSW=285KHz
TDC:11A
OCP:13A

+0.675VSP
TDC:1.3A

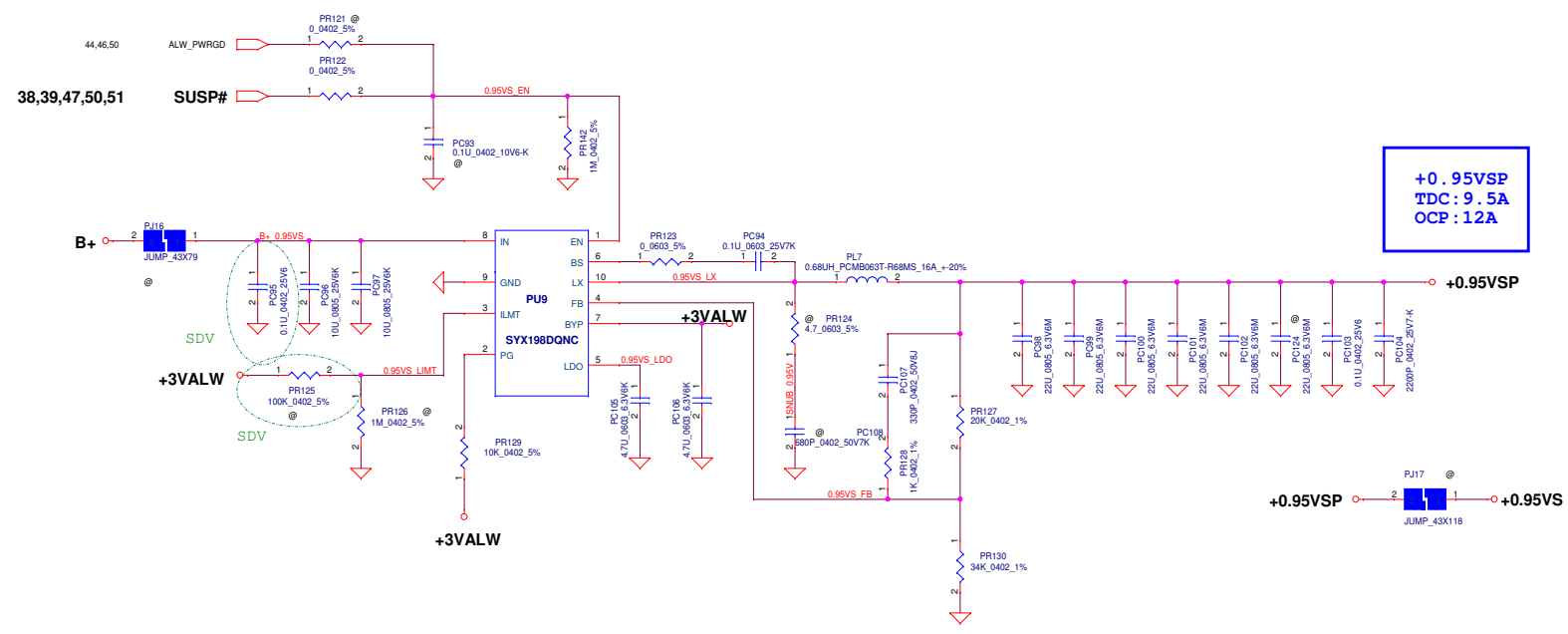
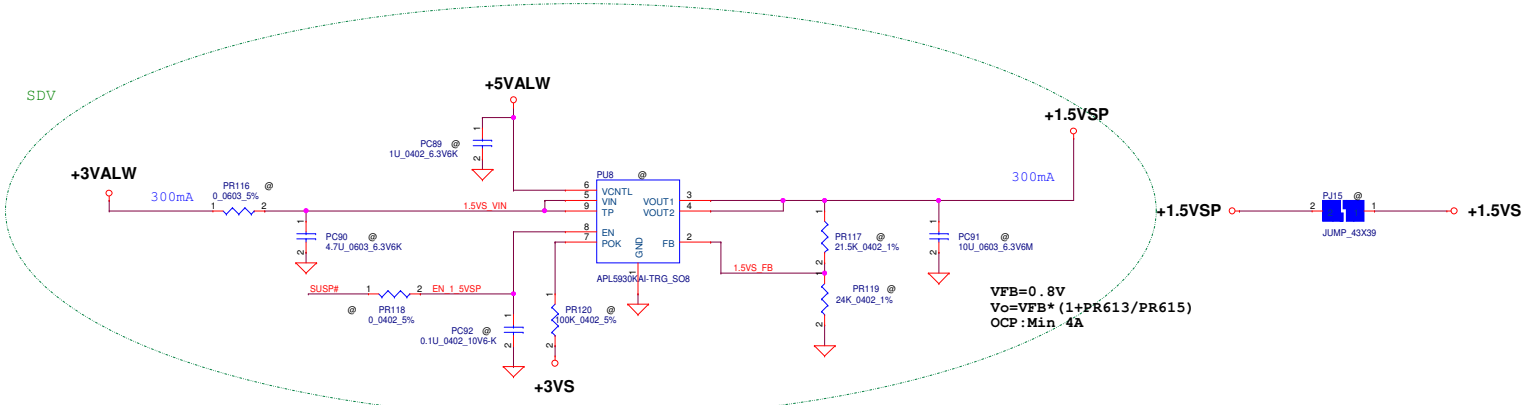
38,39,48,50,51

38



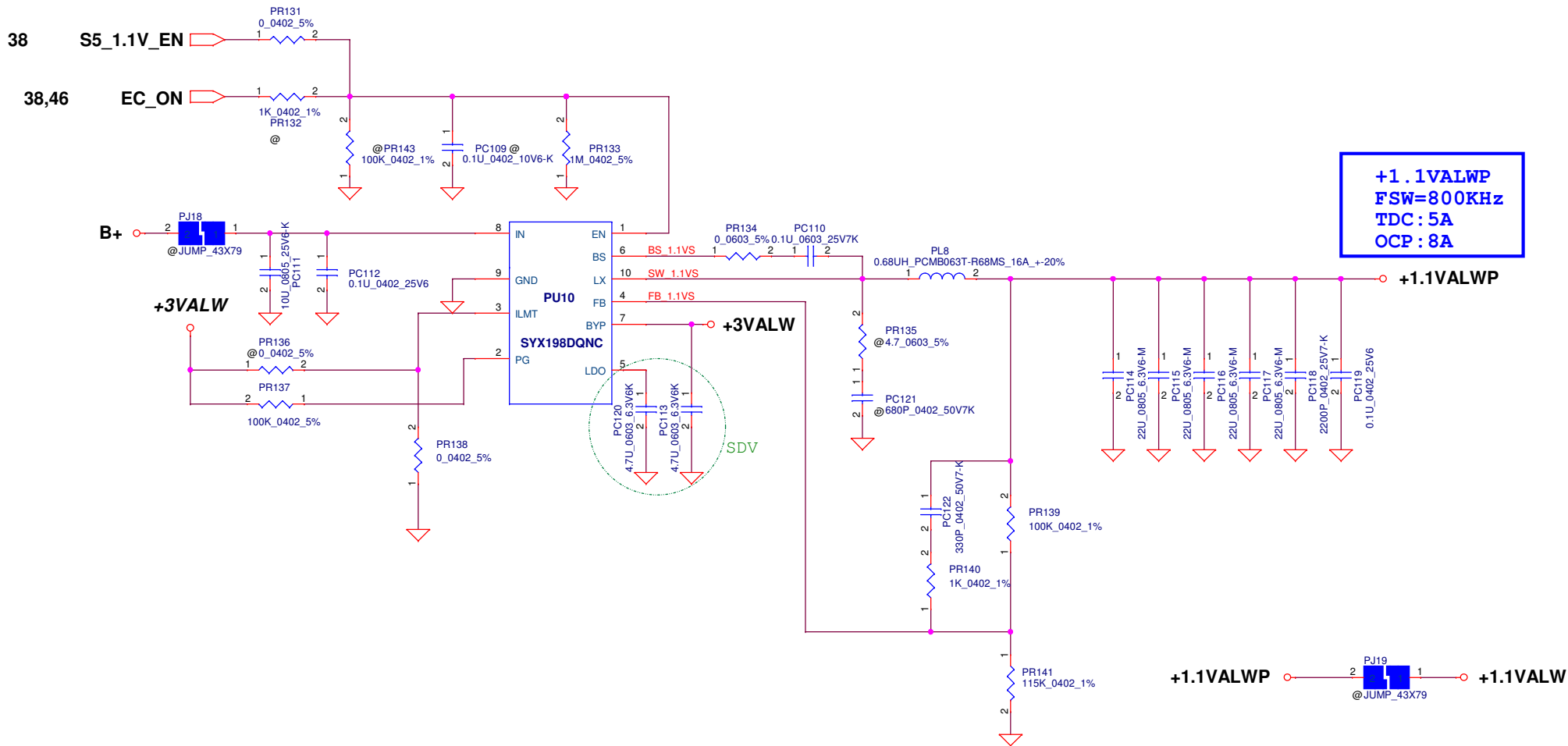
Security Classification		LC Future Center Secret Data	
Issued Date	2013/08/01	Deciphered Date	2014/08/01
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

Title		LCFC	
+1.35VP/+0.675VSP		Size Custom	Rev 0.1
Date:	Monday, December 16, 2013	Sheet	47 of 47




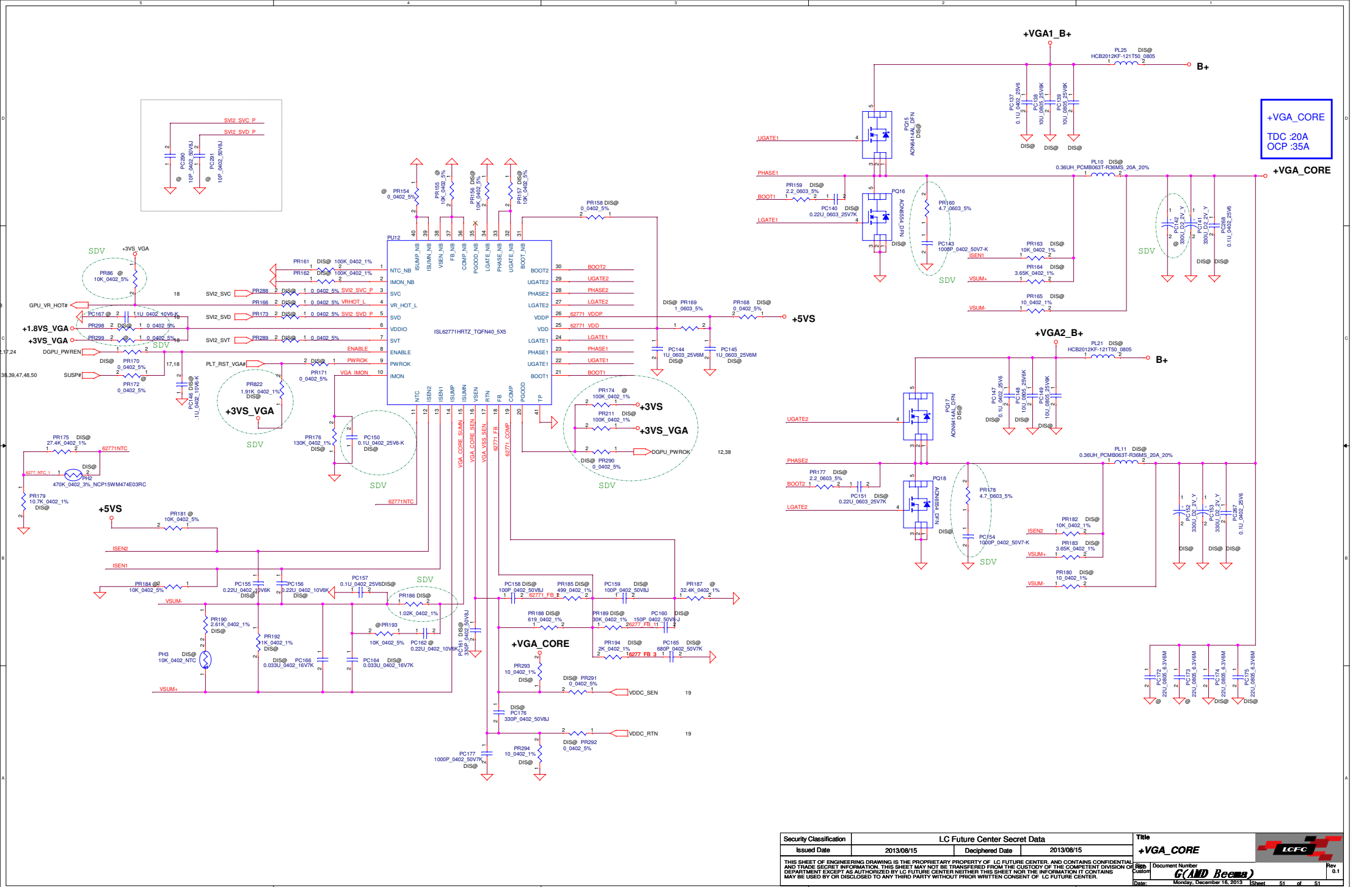
Current limit setting pin. The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

Security Classification	LC Future Center Secret Data		Title	
Issued Date	2013/08/15	Deciphered Date	2013/08/15	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				
Size	Document Number	Date		Rev
	G(AMD Beema)	Monday, December 16, 2013		0.1
		Sheet	48	of
			48	



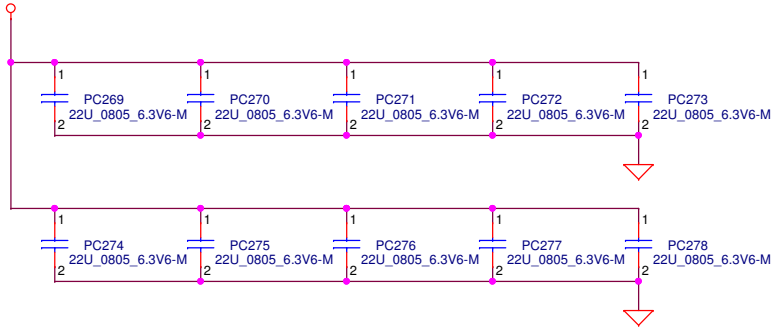
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/08/01
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			

Title		
+1.1VALWP		
Size	Document Number	Rev
B	AAVE1	0.1
Date:	Monday, December 16, 2013	Sheet 49 of 49

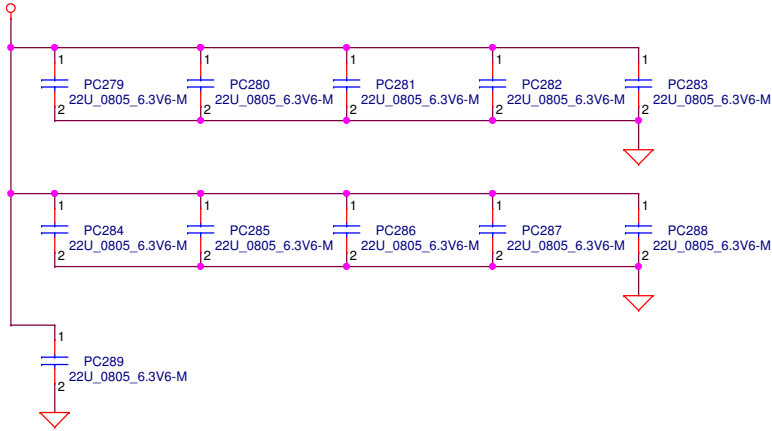


Security Classification	LC Future Center Secret Data		Title	+VGA_CORE	
Issued Date	2013/08/15	Deciphered Date	2013/09/15		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					Rev 0.1
Page	Monday, December 16, 2013 11:58 AM			Sheet	51 of 51

+VDDNB_CORE



+VDD_CORE



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/01	Deciphered Date	2014/08/01	VCCPUCORE DECOUPLING	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size	Rev
				Document Number	0.1
				Date:	Monday, December 16, 2013
				Sheet	53 of 53



AAVE1

