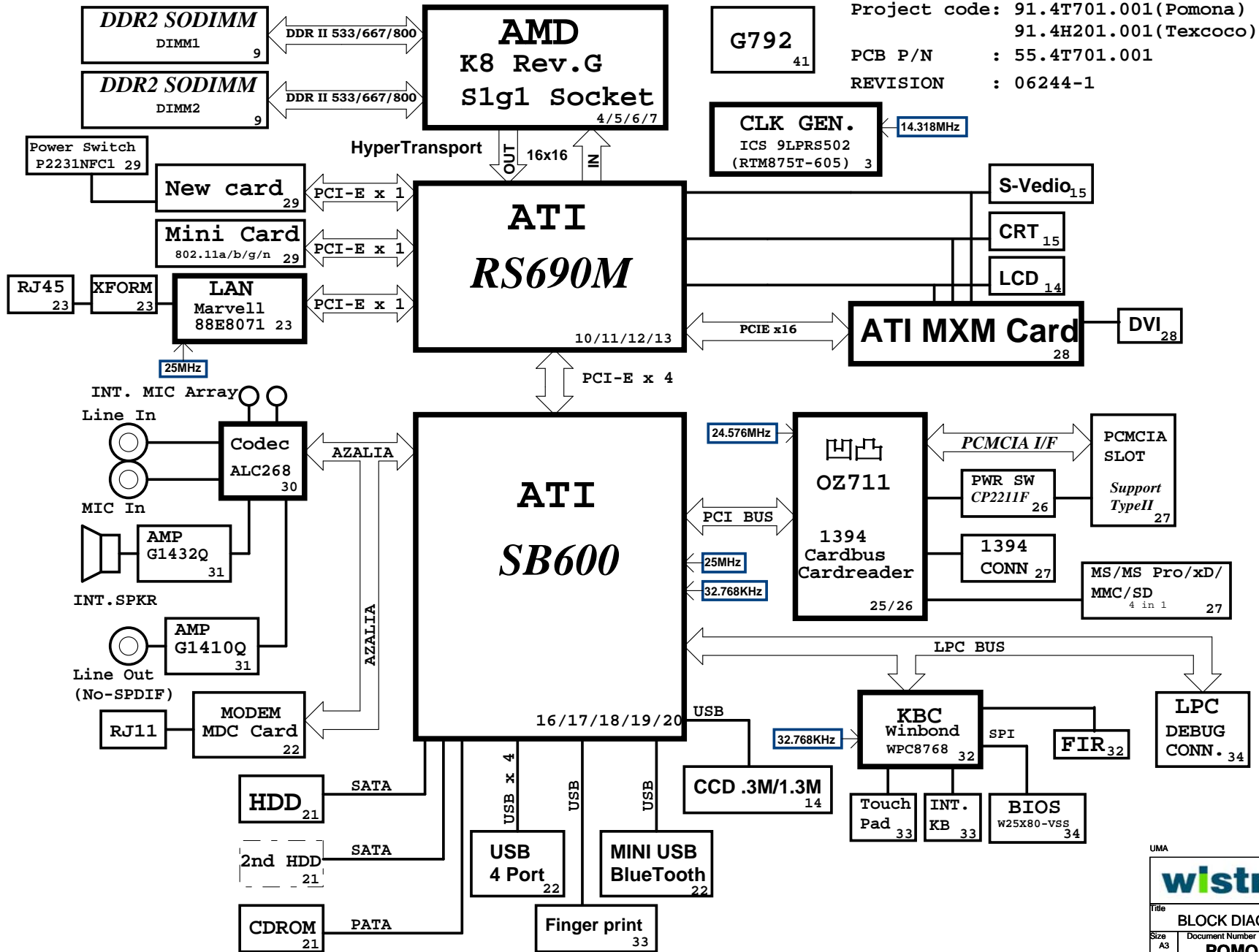


Pomona/Texcoco Block Diagram

Ver. -1



Project code: 91.4T701.001 (Pomona)
 91.4H201.001 (Texcoco)
 PCB P/N : 55.4T701.001
 REVISION : 06244-1

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

ISL6264 38/39	
INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

TPS51124 47	
INPUT	OUTPUT
DCBATOUT	ID2V_S0 ID8V_S3

SYSTEM DC/DC

ISL6236 46	
INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

TPS51100 48	
INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

APL5915 48	
INPUT	OUTPUT
3D3V_S5	1D2V_S5
3D3V_S0	2D5V_S0
3D3V_S0	1D5V_S0

SYSTEM LDO

ISL6236 46	
INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

ISL6255 42	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

wistron Wistron Incorporated
 21F, 88, Hsin Tai Wu Rd
 Hsichih, Taipei

Title: **BLOCK DIAGRAM**

Size: A3 Document Number: **POMONA/TEXCOCO** Rev: 1

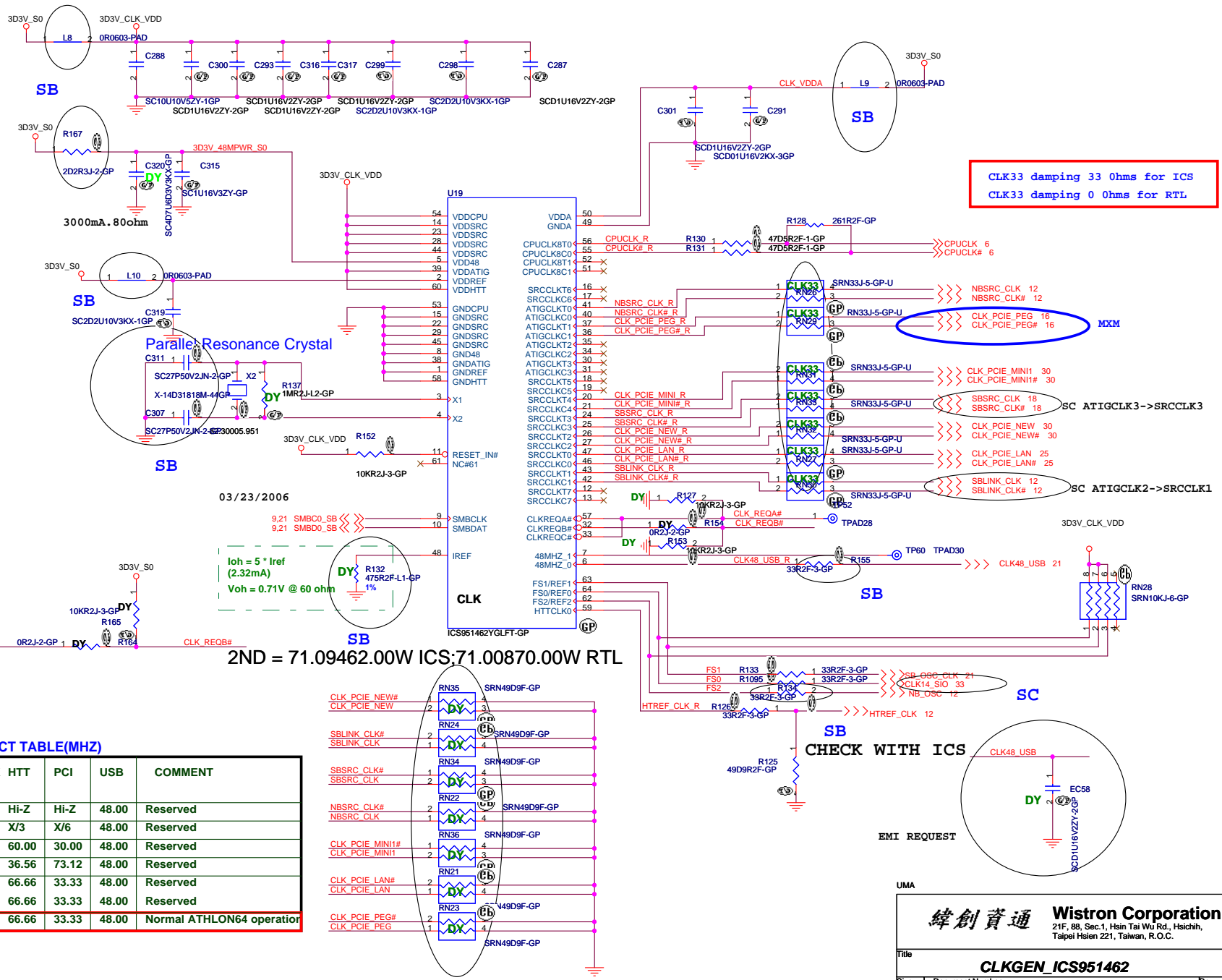
Date: Thursday, March 29, 2007 Sheet 1 of 49

SA: 07/31/06 Start

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CHANGE HISTORY		
Size A3	Document Number Pomona/Texcoco	Rev 1
Date: Thursday, March 29, 2007 Sheet 2 of 49		

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2ND = 71.09462.00W ICS:71.00870.00W RTL

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CLKGEN_ICS951462**

Size A3 Document Number **Pomona/Textcoco** Rev 1

Date: Thursday, March 29, 2007 Sheet 3 of 49

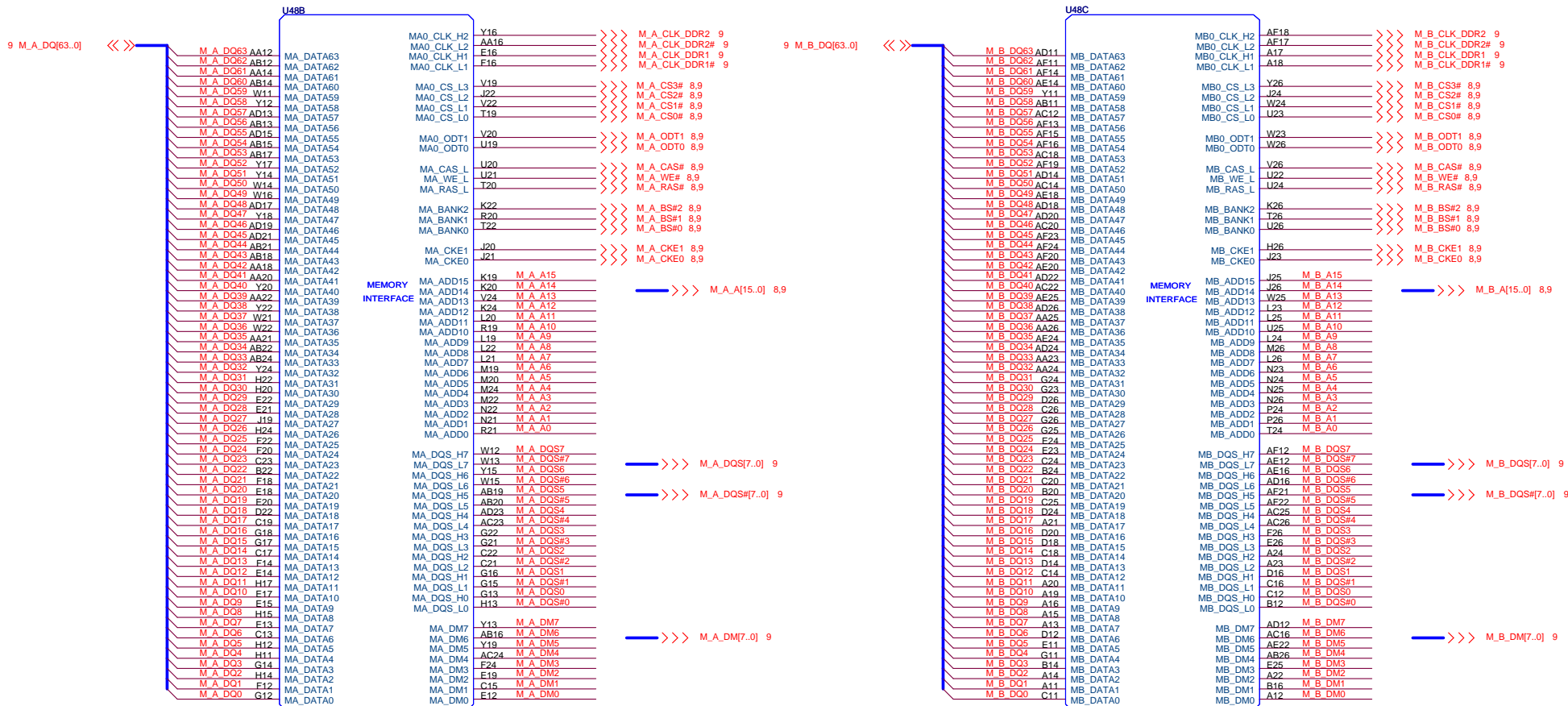


62-10055.111

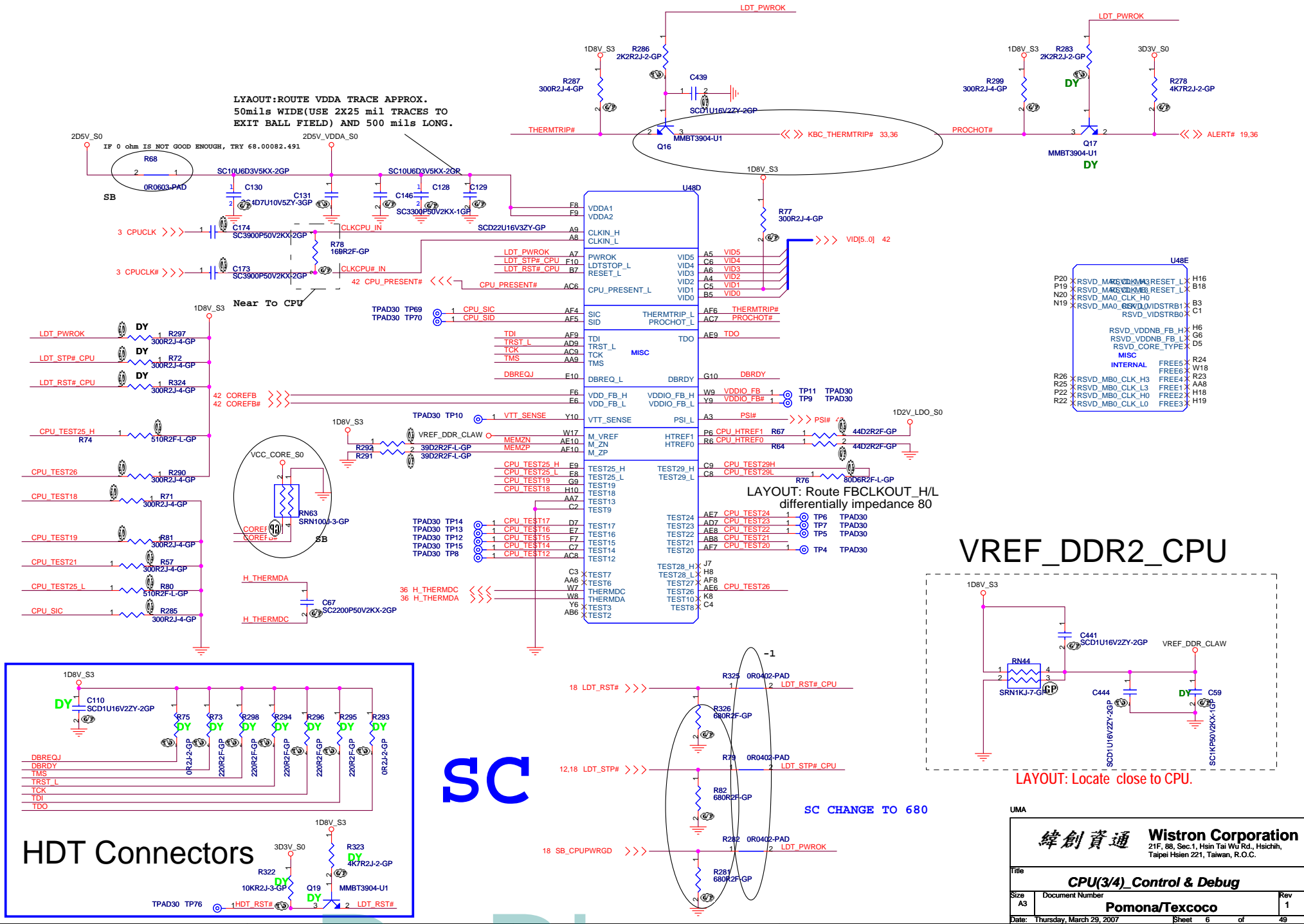
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU(1/4)_HyperTransport I/F		
Size	Document Number	Rev			1
A3	Pomona/Textcoco				
Date:	Thursday, March 29, 2007	Sheet	4	of	49

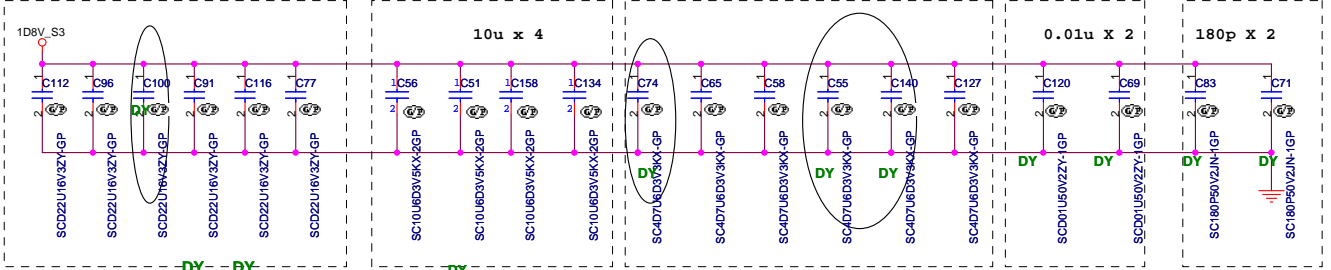
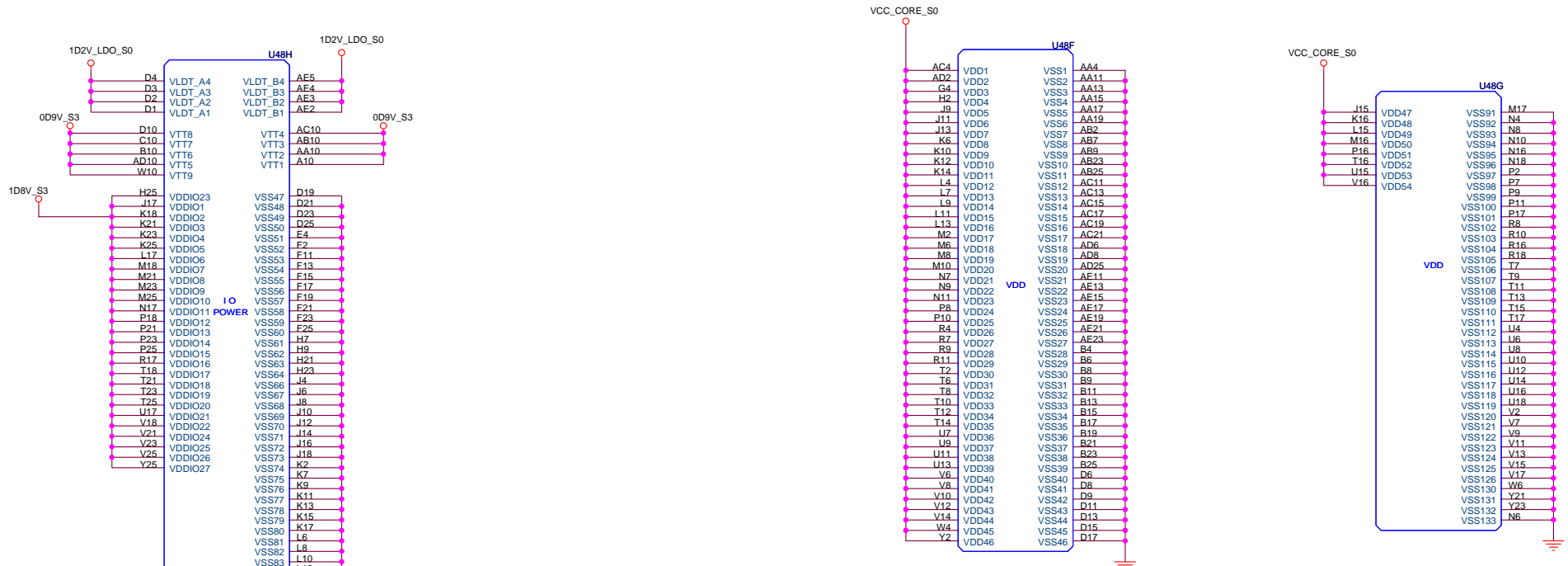


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File			
CPU(2/4)_DDR2			
Size	Document Number		Rev
A3	Pomona/Textcoco		1
Date:	Thursday, March 29, 2007	Sheet	5 of 49

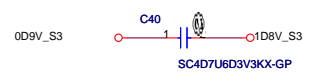
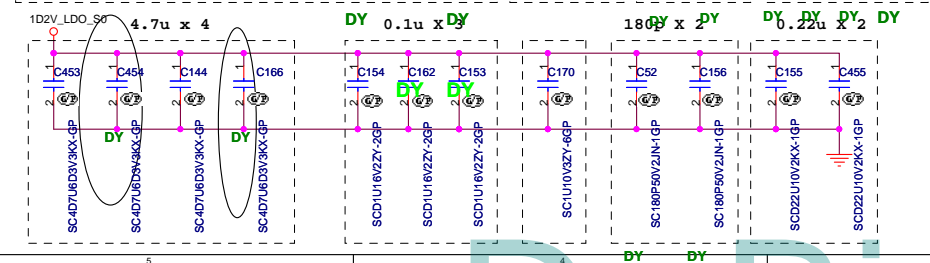
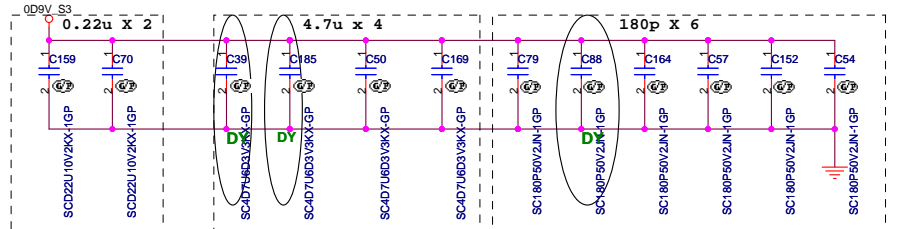
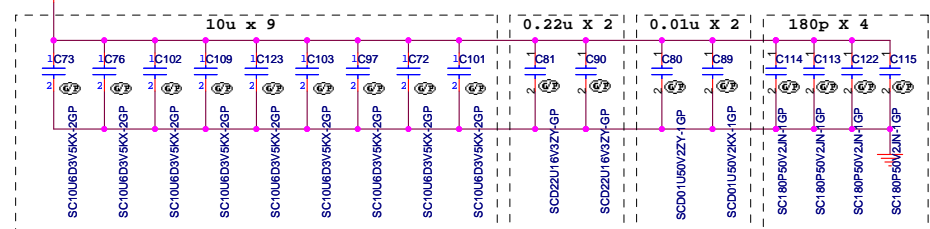


SC

UMA		
緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU(3/4)_Control & Debug		
Size A3	Document Number Pomona/Textcoco	Rev 1
Date: Thursday, March 29, 2007	Sheet 6 of 49	



VCC_CORE_S0 LAYOUT: Place on backside of processor.



UMA

緯創資通 Wistron Corporation
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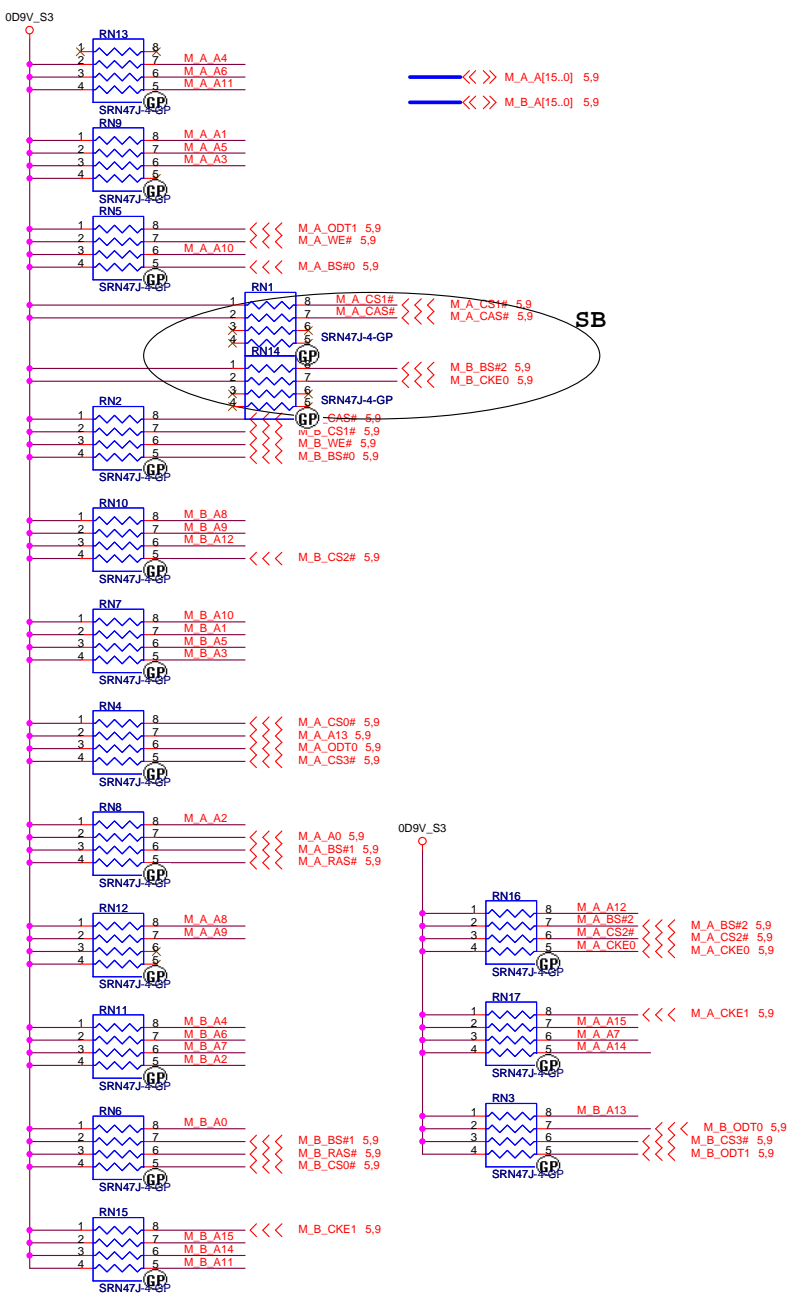
Title: **CPU(4/4)_Power**

Size: A3 Document Number: **Pomona/Textcoco** Rev: 1

Date: Thursday, March 29, 2007 Sheet: 7 of 49

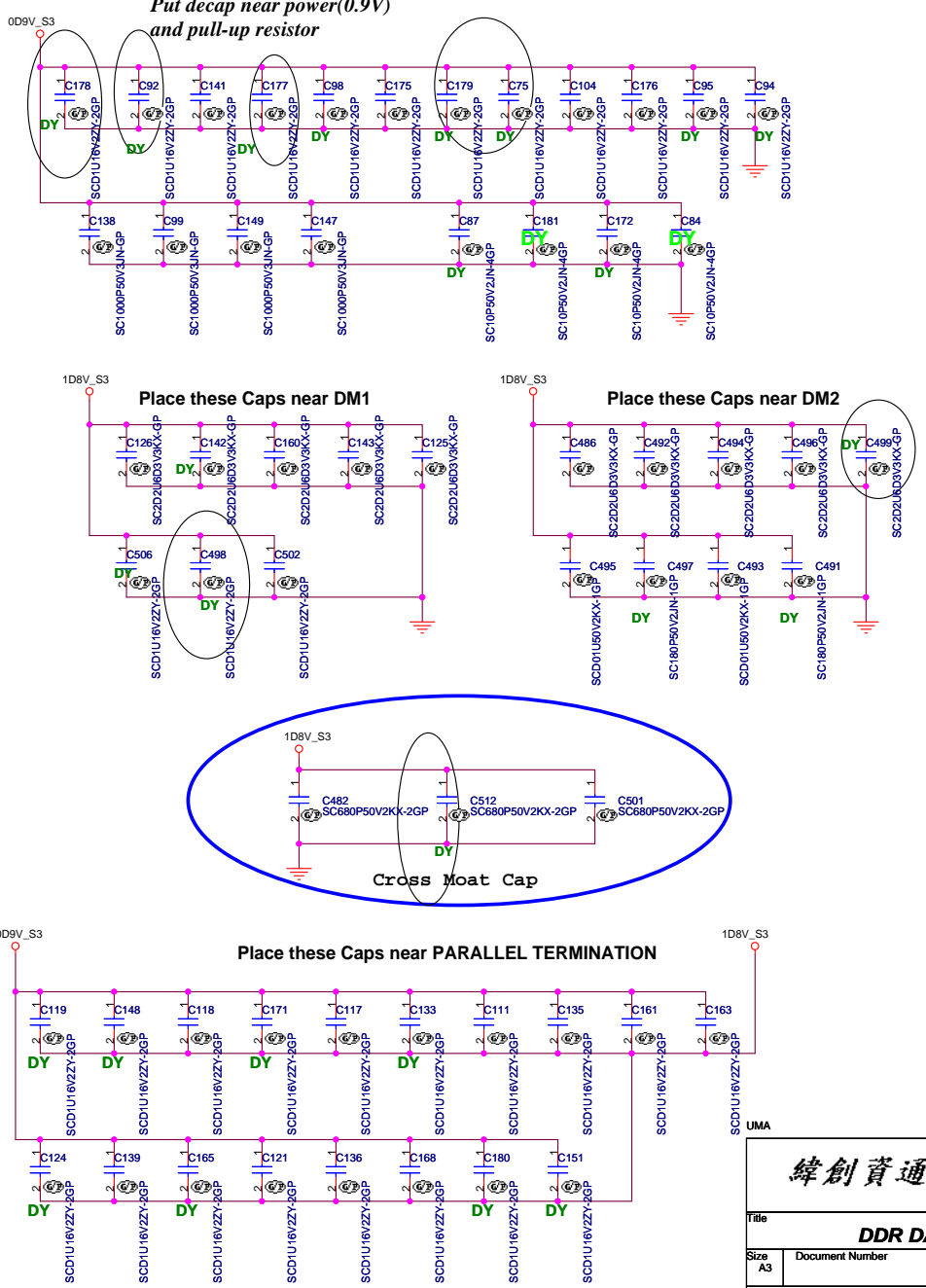
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

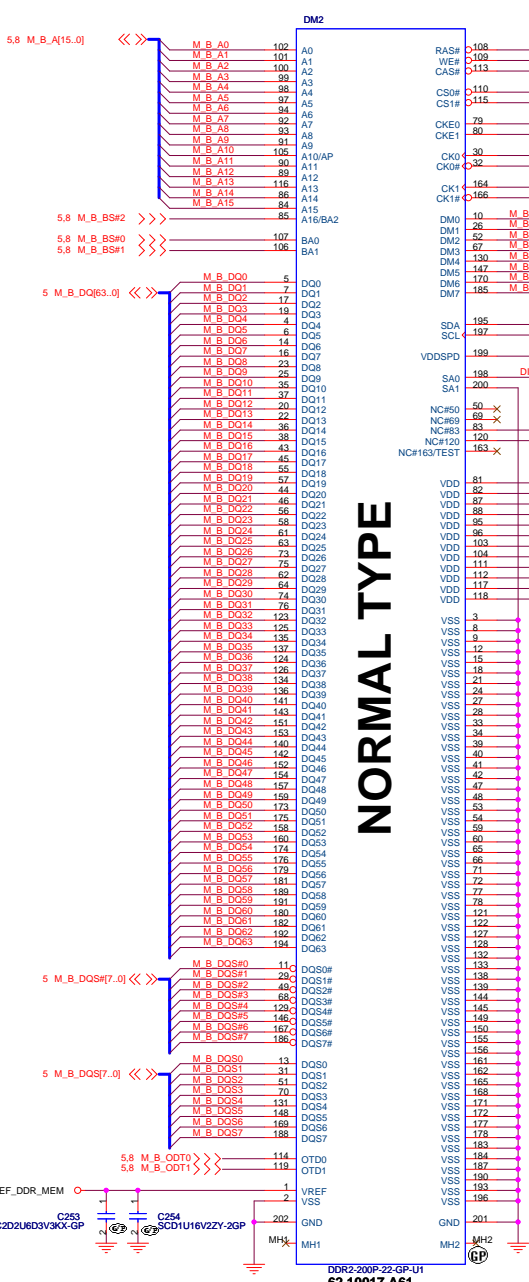


緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR DAMPING & TERMINATION**

Size A3 Document Number **Pomona/Texcoco** Rev 1

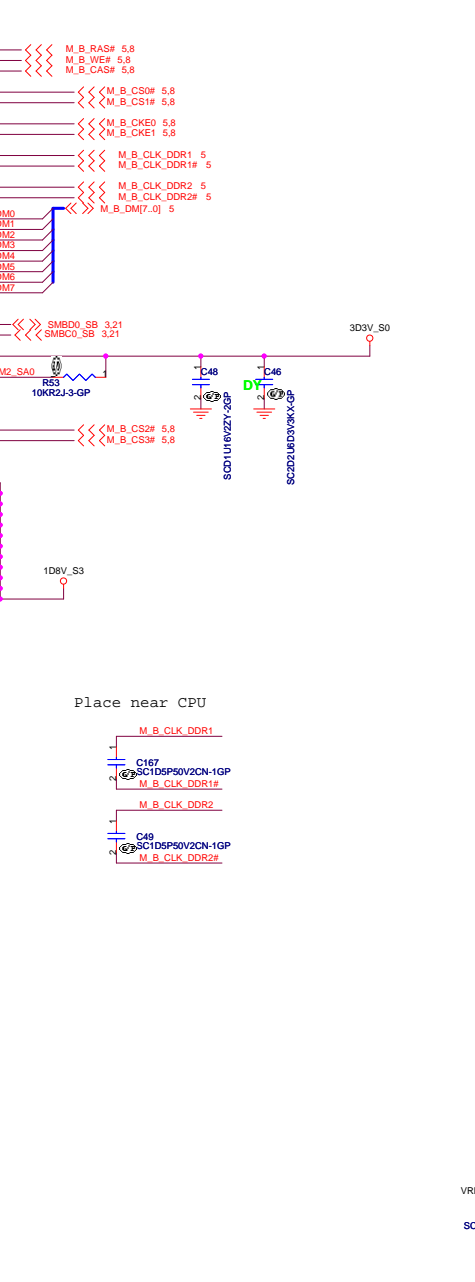
Date: Thursday, March 29, 2007 Sheet 8 of 49



NORMAL TYPE

High 9.2mm

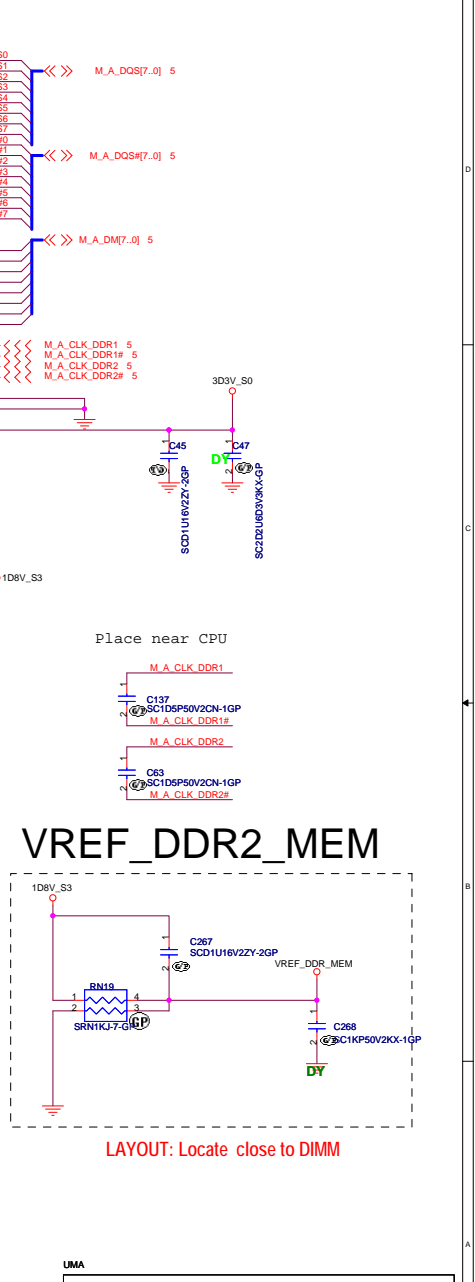
2ND = 62.10017.761



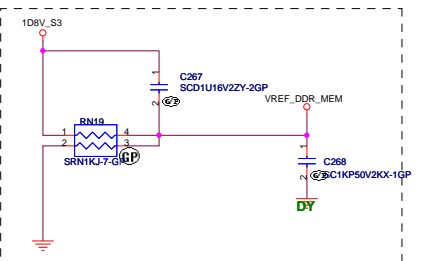
NORMAL TYPE

High 5.2mm

2ND = 62.10017.D91



VREF_DDR2_MEM



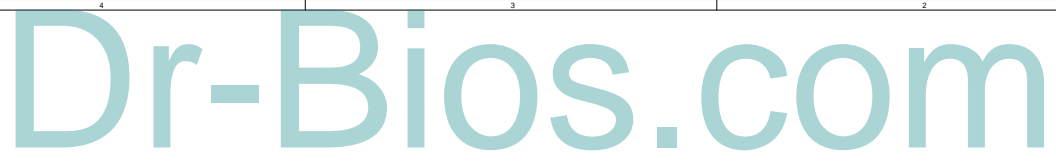
LAYOUT: Locate close to DIMM

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

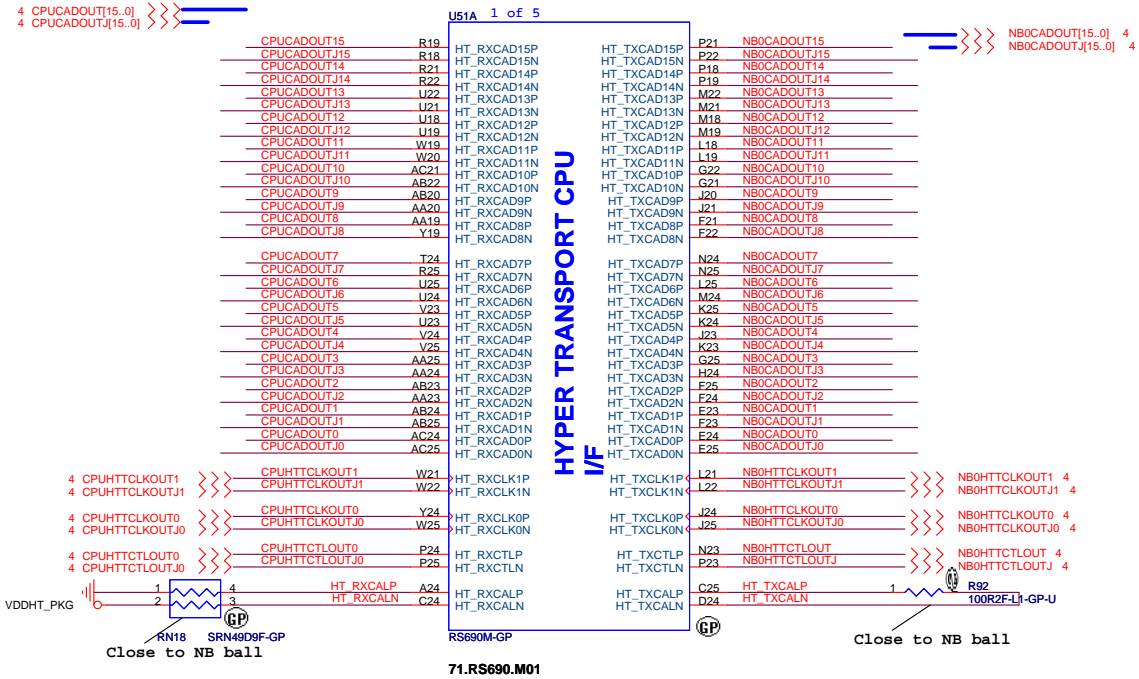
DDR SO-DIMM SKT

Doc No	Document Number	Rev
Custom	Pomona/Texcoco	1
Date	Thursday, March 29, 2007	Sheet 9 of 48



CPU TO NB

NB TO CPU

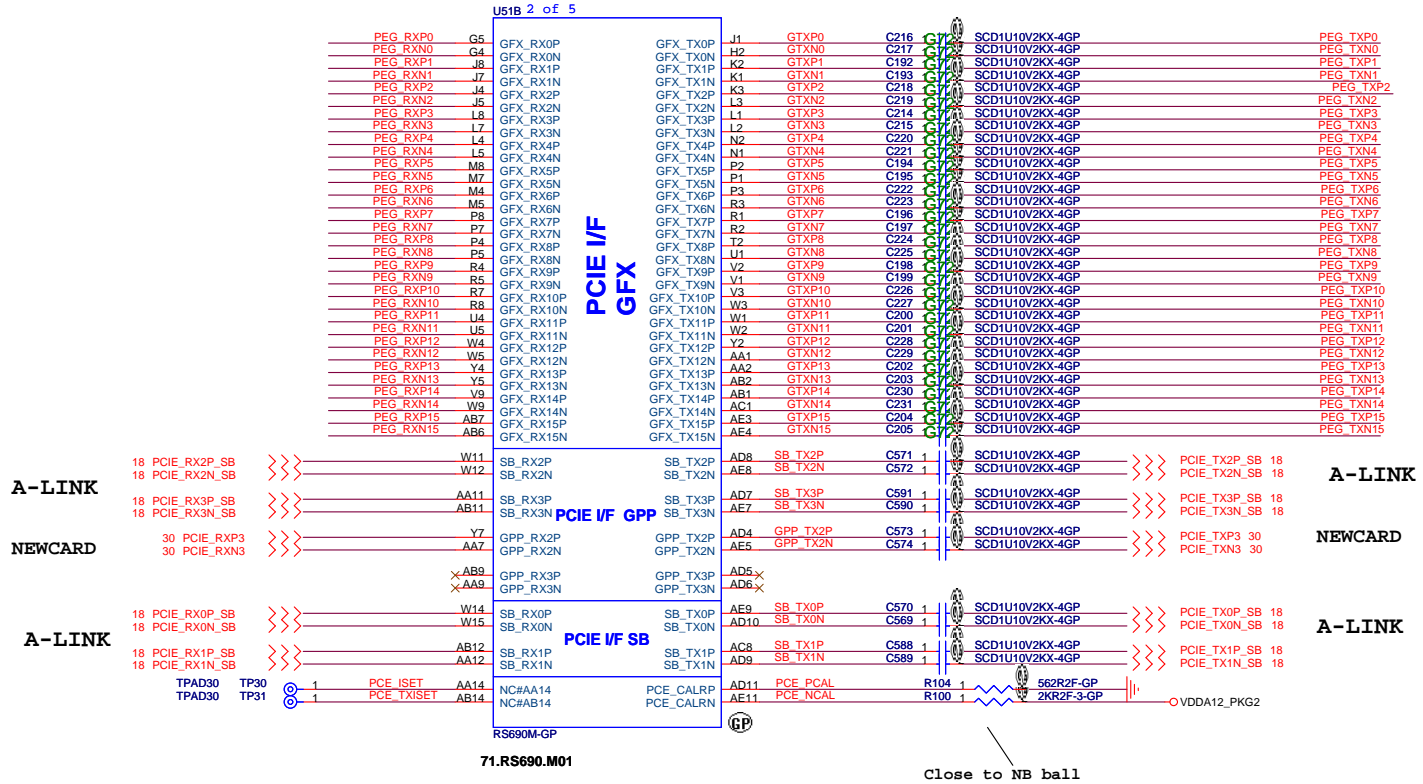


UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title NB-RS690M HT	
Size A3	Document Number Pomona/Textcoco
Date: Thursday, March 29, 2007	Rev 1
Sheet 10 of 49	49

16 PEG_RXN[15..0] >>>
 16 PEG_RXP[15..0] >>>

>>> PEG_TXN[15..0] 16
 >>> PEG_TXP[15..0] 16



UMA

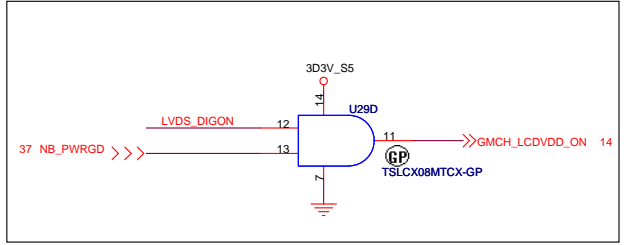
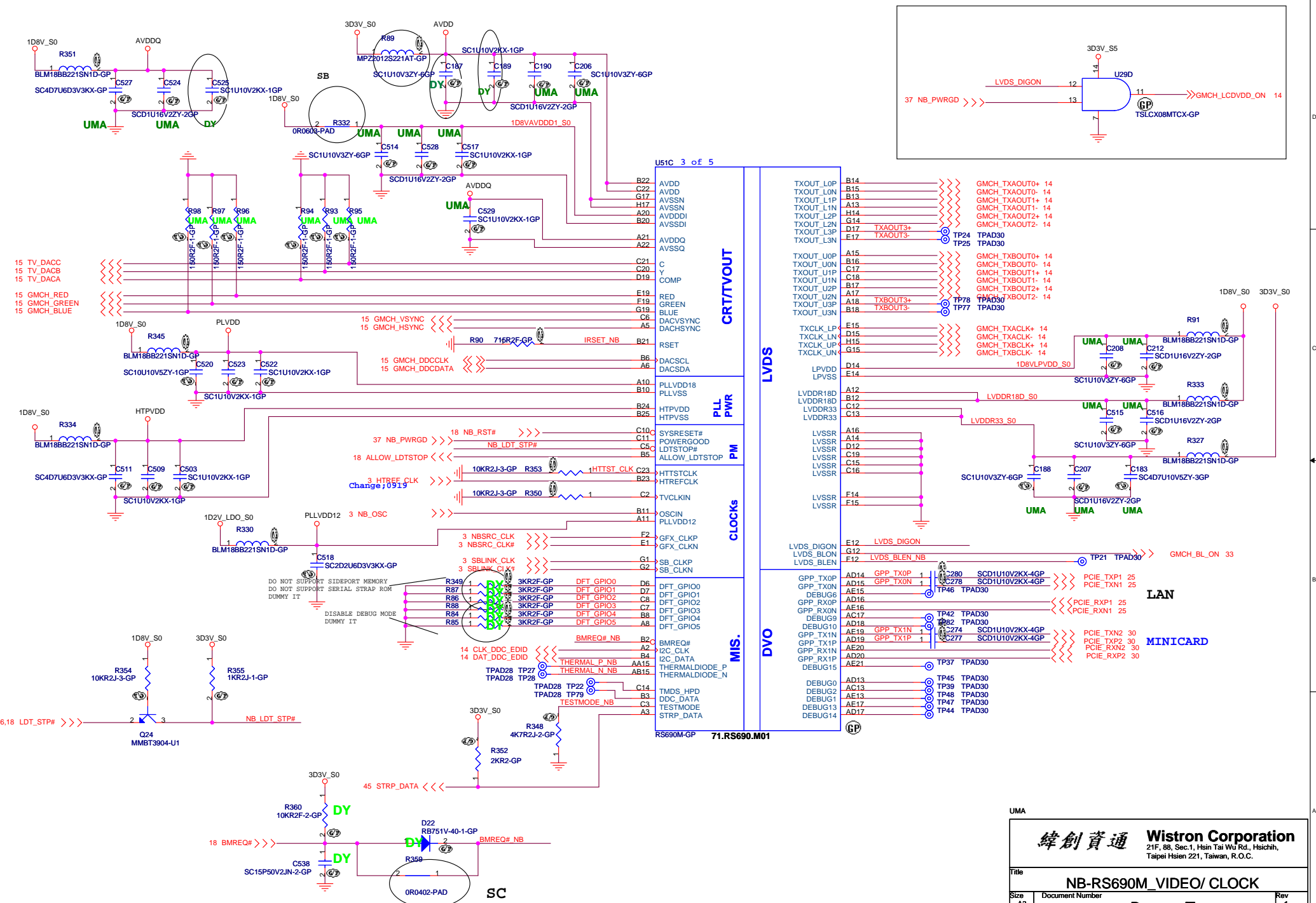
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_MEM/PCIE_LINK I/F

Size: A3 Document Number: Pomona/Textcoco Rev: 1

Date: Thursday, March 29, 2007 Sheet: 11 of 49

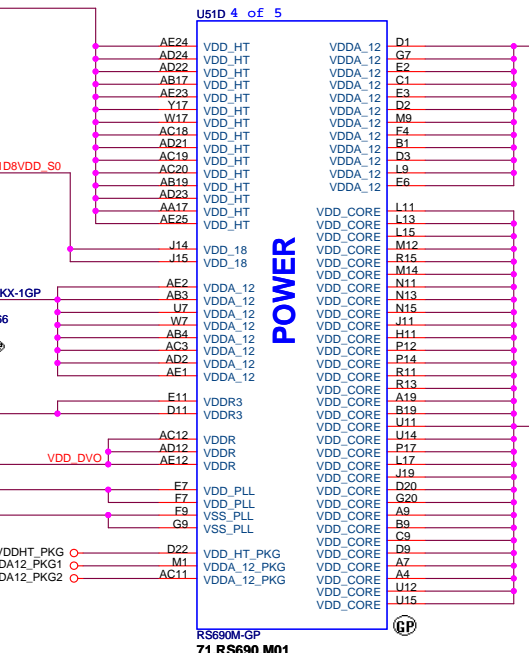
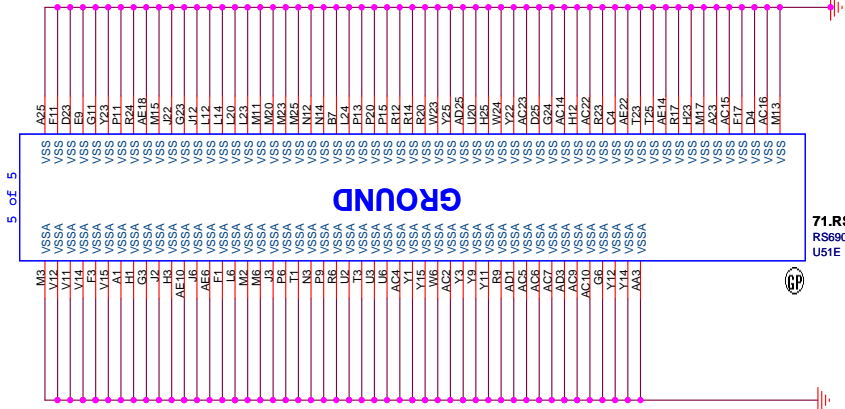
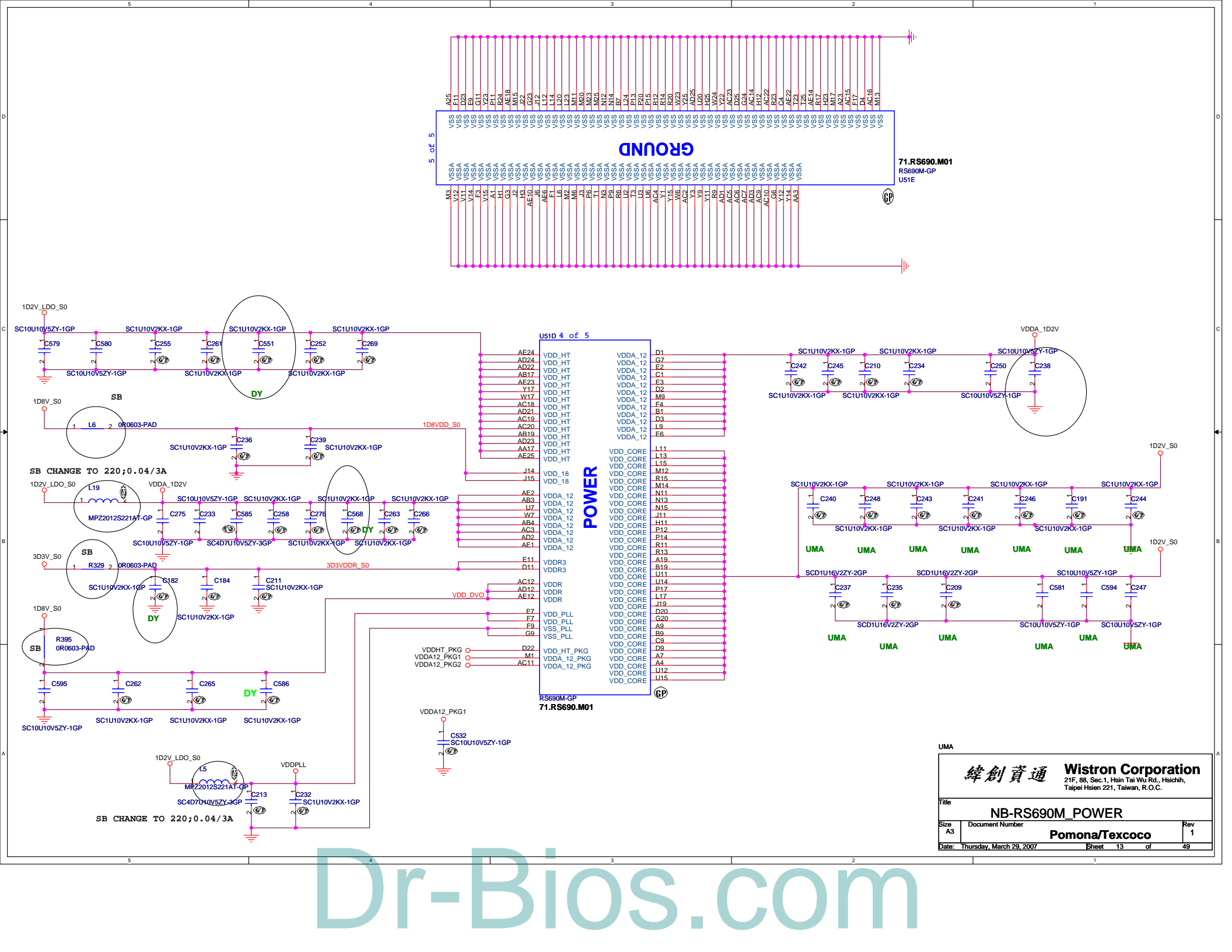
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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_VIDEO/ CLOCK
 Size: A3 Document Number: Pomona/Textcoco Rev: 1
 Date: Thursday, March 29, 2007 Sheet: 12 of 49

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UMA

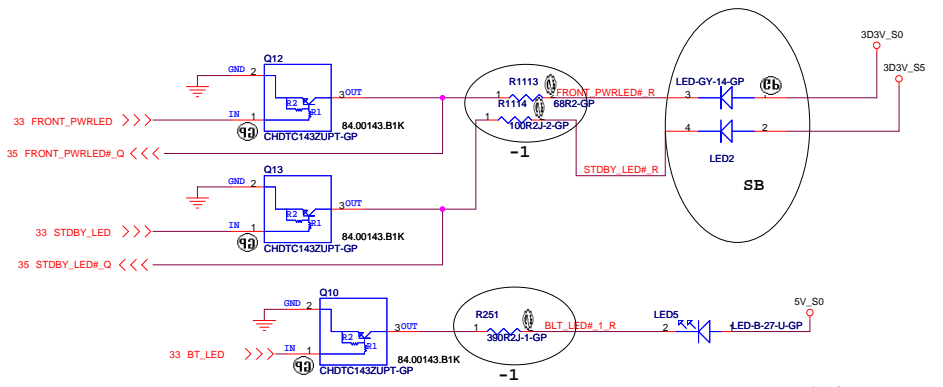
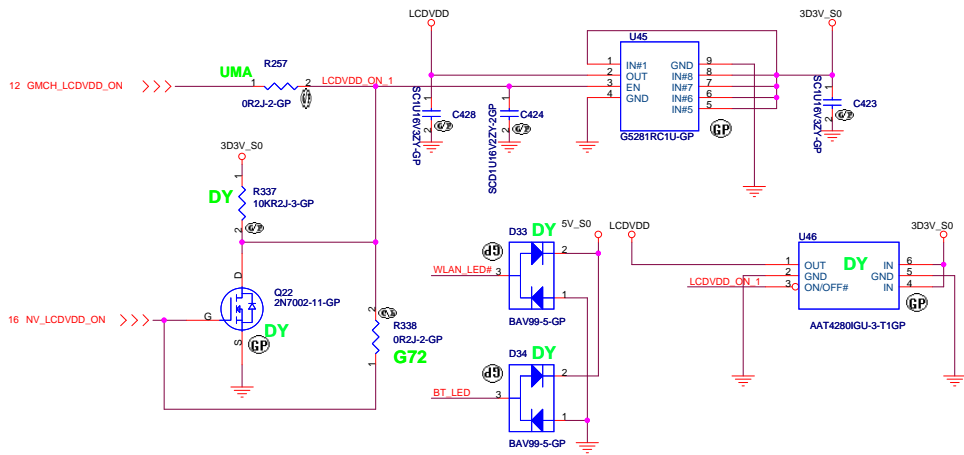
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **NB-RS690M_POWER**

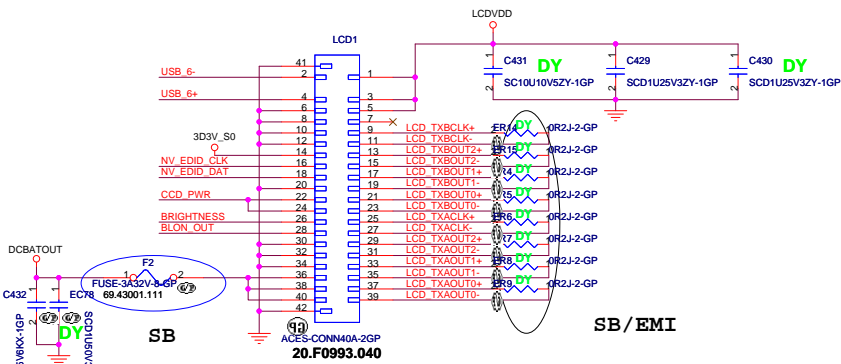
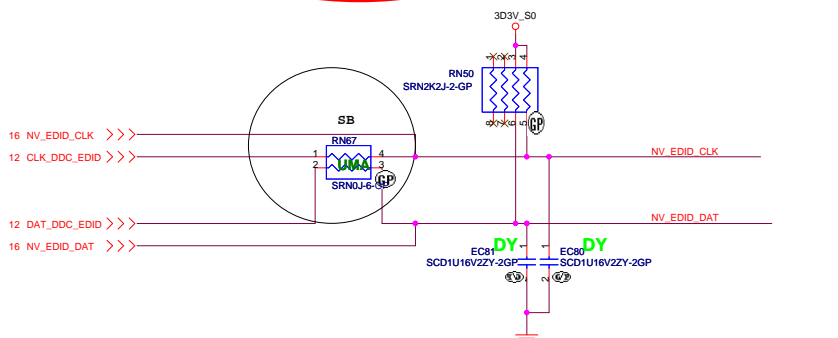
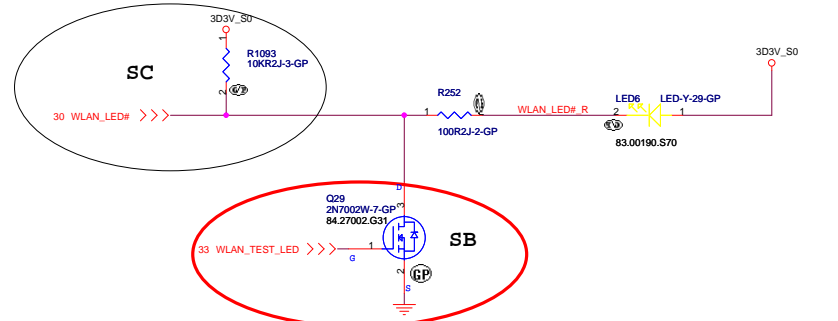
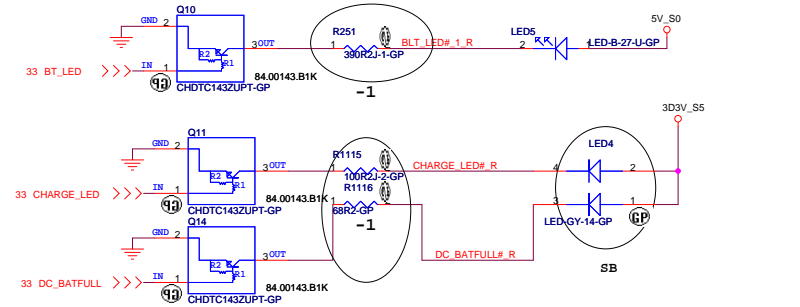
Size: A3 Document Number: **Pomona/Textcoco** Rev: 1

Date: Thursday, March 29, 2007 Sheet 13 of 49

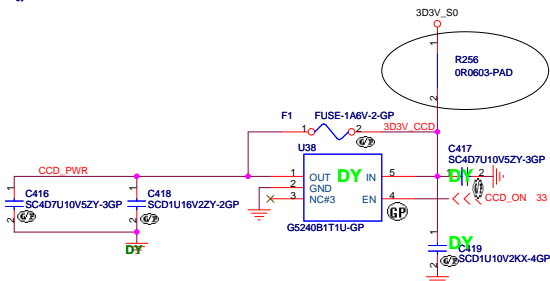
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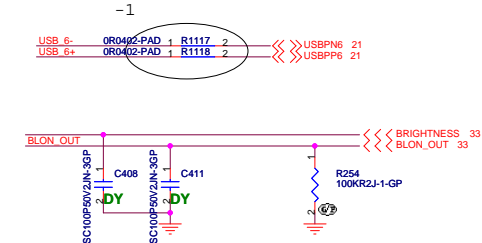
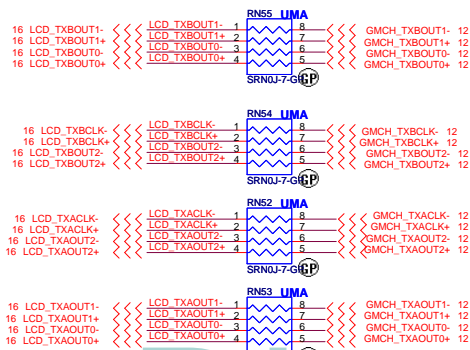
LCD/INVERTER CONN



SB/EMI



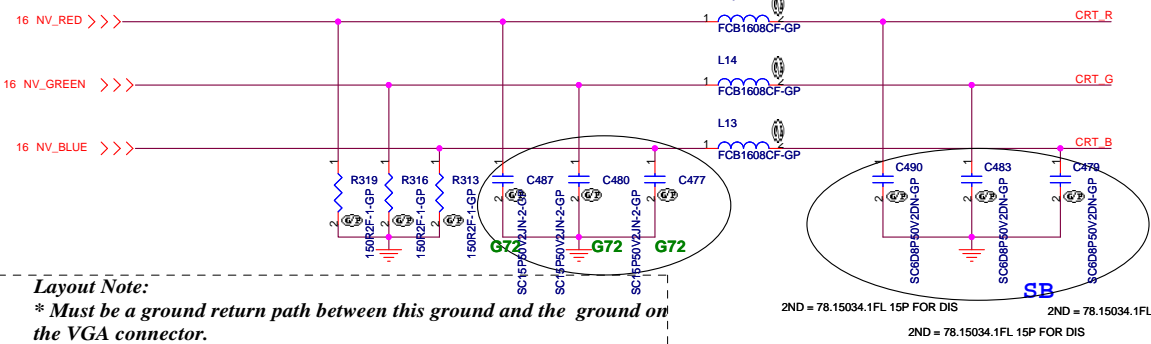
SB



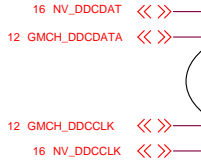
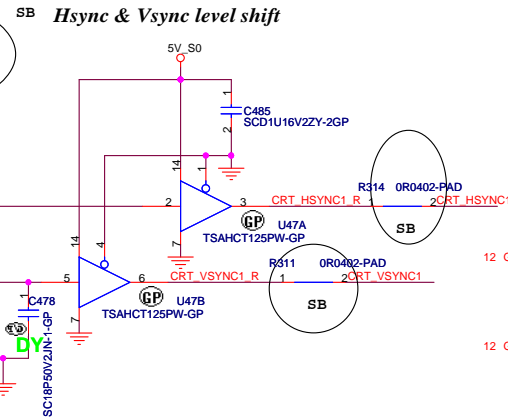
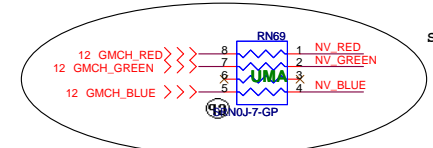
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

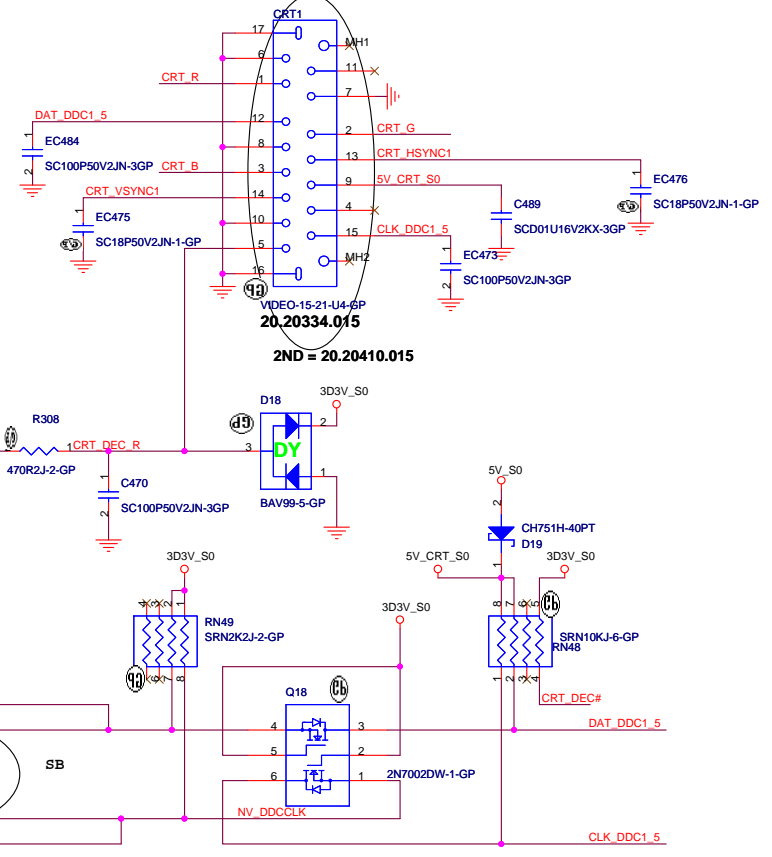
Ferrite bead impedance: 10 ohm@100MHz:



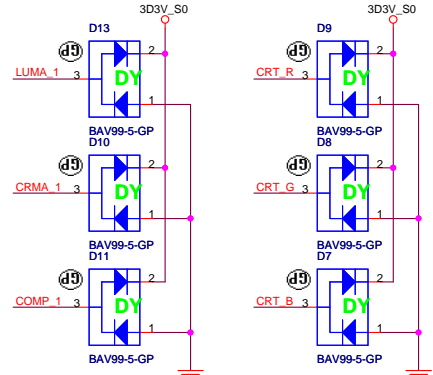
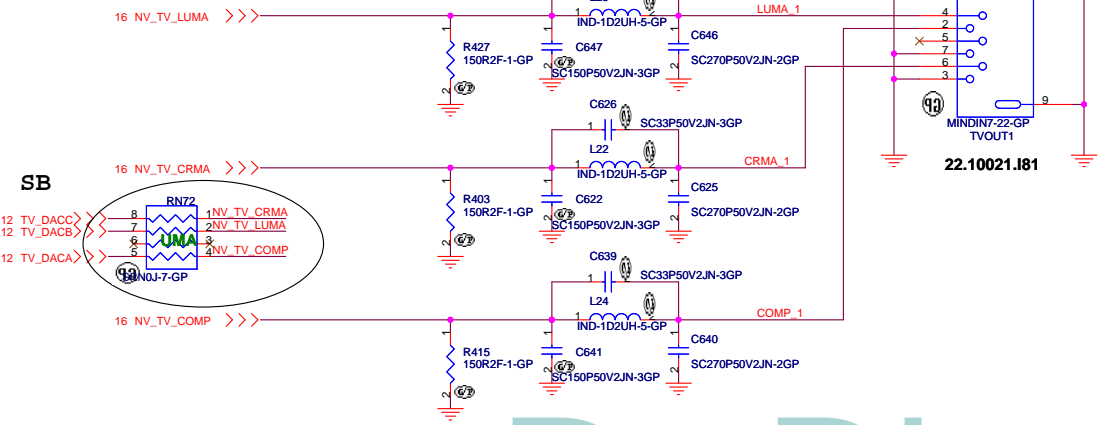
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



DDC_CLK & DATA level shift



TV CONN



緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		CRT/TV Connector	
Size	Document Number	Pomona/Textcoco	
Date: Thursday, March 29, 2007	Sheet 15	of	49

NV SMBus
 A(pin143&145) : VGA(CRT) / DOCK
 B(pin218&220) : DVI
 C(pin208&210) : HDMI / TPI / LVDS

ENG MUST STUFF FOR ATI

Put near graphic connector

11 PEG_TXP[15..0] <<<
 11 PEG_TXN[15..0] <<<
 11 PEG_RXP[15..0] <<<
 11 PEG_RXN[15..0] <<<

14 LCD_TXBOUT0+ <<<
 14 LCD_TXBOUT0- <<<
 14 LCD_TXBOUT1+ <<<
 14 LCD_TXBOUT1- <<<
 14 LCD_TXBOUT2+ <<<
 14 LCD_TXBOUT2- <<<

14 LCD_TXBCLK+ <<<
 14 LCD_TXBCLK- <<<

15 NV_BLUE <<<
 15 NV_GREEN <<<
 15 NV_RED <<<

15 NV_TV_COMP <<<
 15 NV_TV_LUMA <<<
 15 NV_TV_CRMA <<<

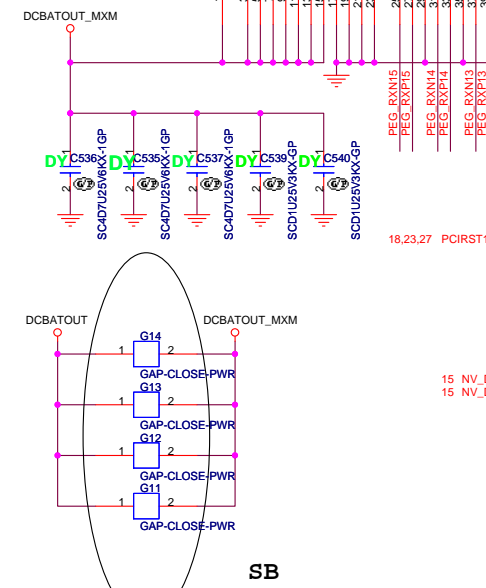
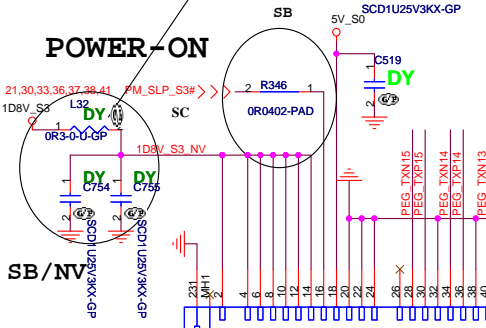
19 UMA_DIS <<<

LCD_TXACLK- 14 <<<
 LCD_TXACLK+ 14 <<<
 LCD_TXAOUT2- 14 <<<
 LCD_TXAOUT2+ 14 <<<
 LCD_TXAOUT1- 14 <<<
 LCD_TXAOUT1+ 14 <<<
 LCD_TXAOUT0- 14 <<<
 LCD_TXAOUT0+ 14 <<<

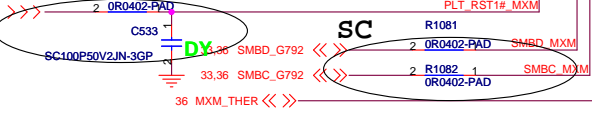
>>> NV_EDID_DAT 14
 >>> NV_EDID_CLK 14

>>> NV_LCDVDD_ON 14
 >>> NV_BLON 33

>>> NV_DVI_DAT 17
 >>> NV_DVI_CLK 17



RESET



15 NV_DDCCLK <<<
 15 NV_DDCDAT <<<

15 NV_HSYNC <<<
 15 NV_VSYNC <<<

EMI REQUEST

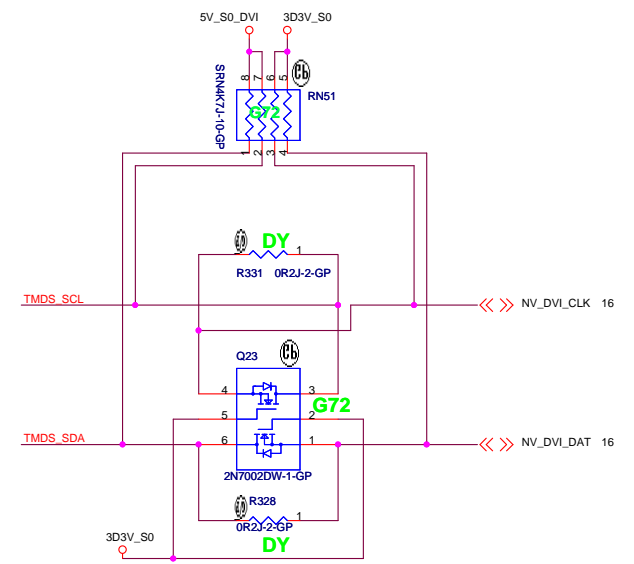
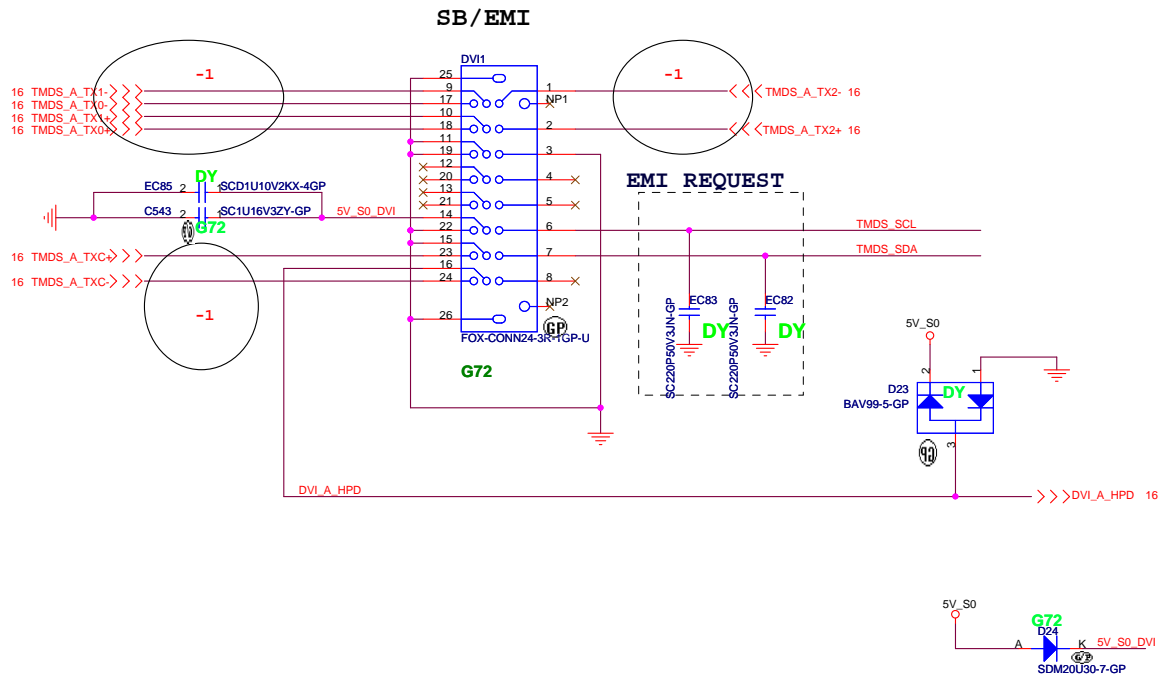
<<< MDS_A_TX0+ 17
 <<< MDS_A_TX0- 17
 <<< MDS_A_TX1+ 17
 <<< MDS_A_TX1- 17
 <<< MDS_A_TX2+ 17
 <<< MDS_A_TX2- 17
 <<< MDS_A_TXC+ 17
 <<< MDS_A_TXC- 17

<<< DVI_A_HPD 17

UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Graphic MXM CONN			
Title		Document Number	
		Pomona/Texcoco	
Size A3			Rev 1
Date: Thursday, March 29, 2007		Sheet 16	of 49

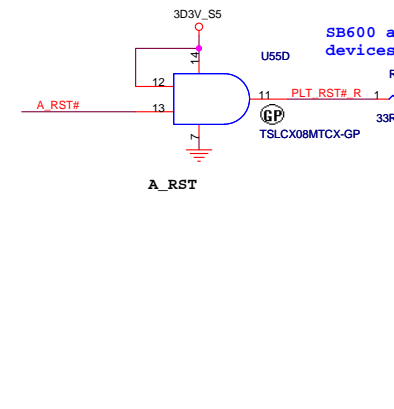
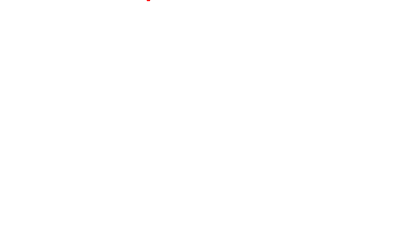
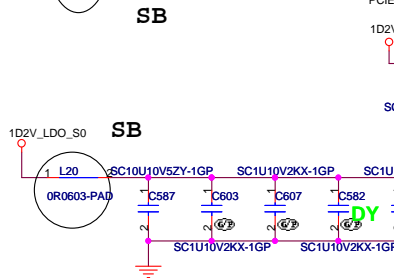
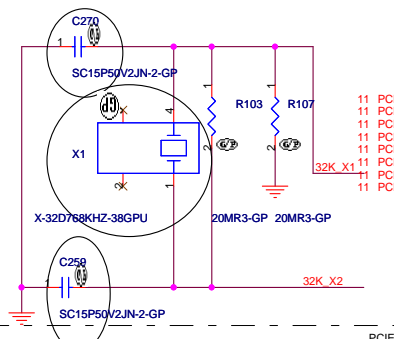
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UMA		
緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DVI CONNECTOR		
Size: A3	Document Number: Pomona/Textcoco	Rev: 1
Date: Thursday, March 29, 2007	Sheet: 17	of 49

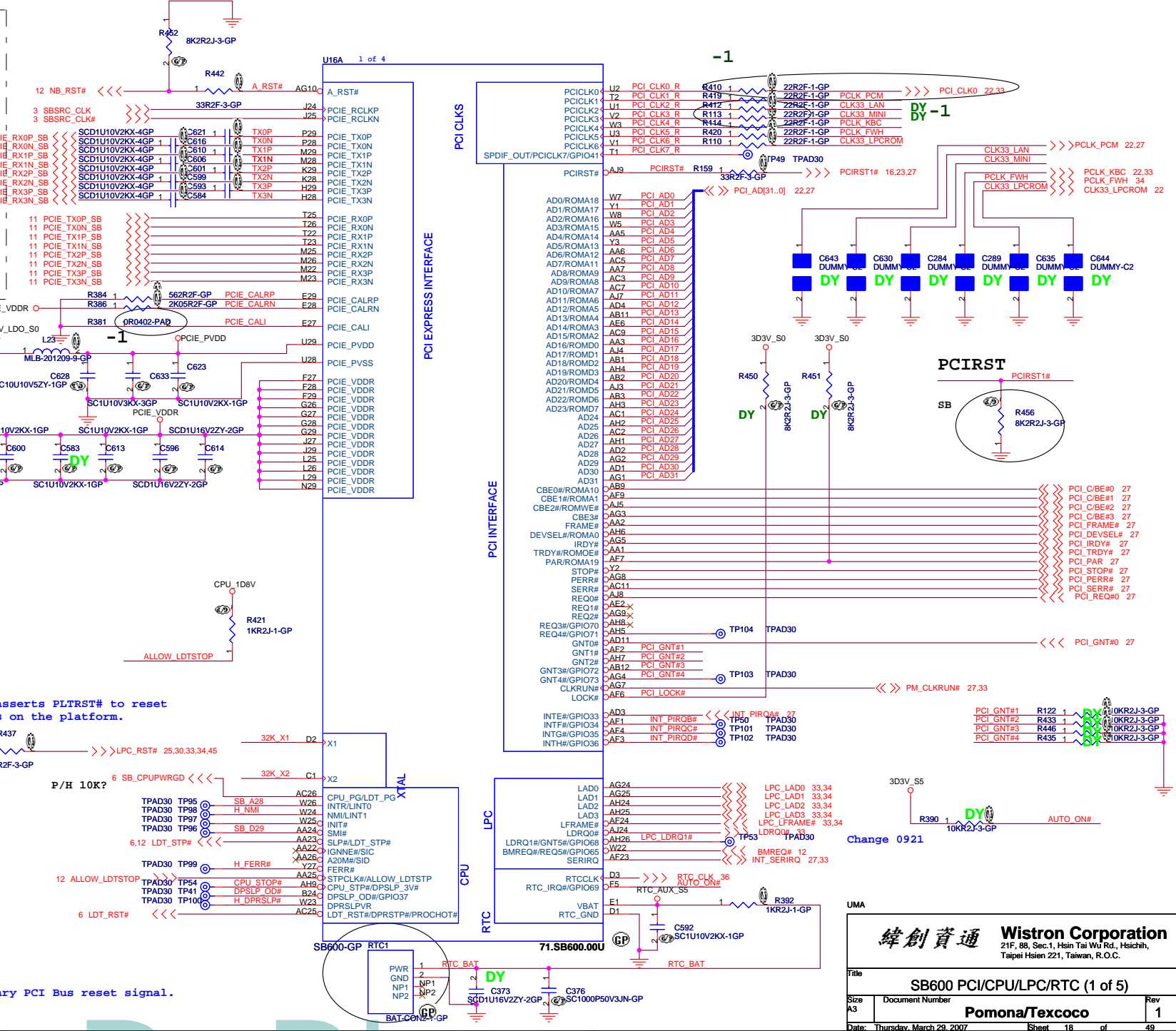
Dr-Bios.com

Place these components close to U13 and use ground guard for 32K_X1 and 32K_X2.



SB600 asserts PLTRST# to reset devices on the platform.

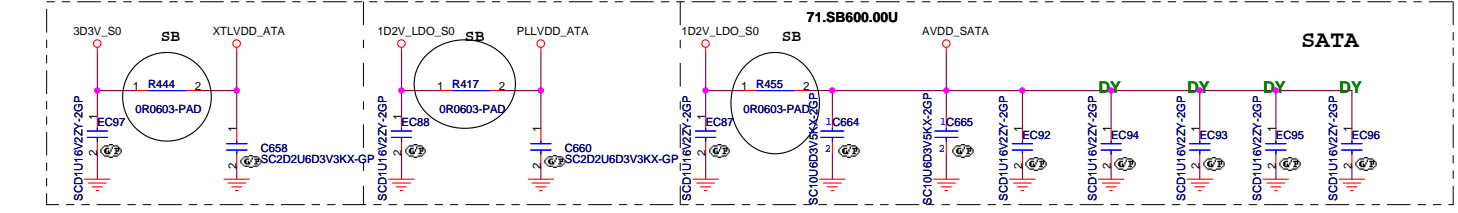
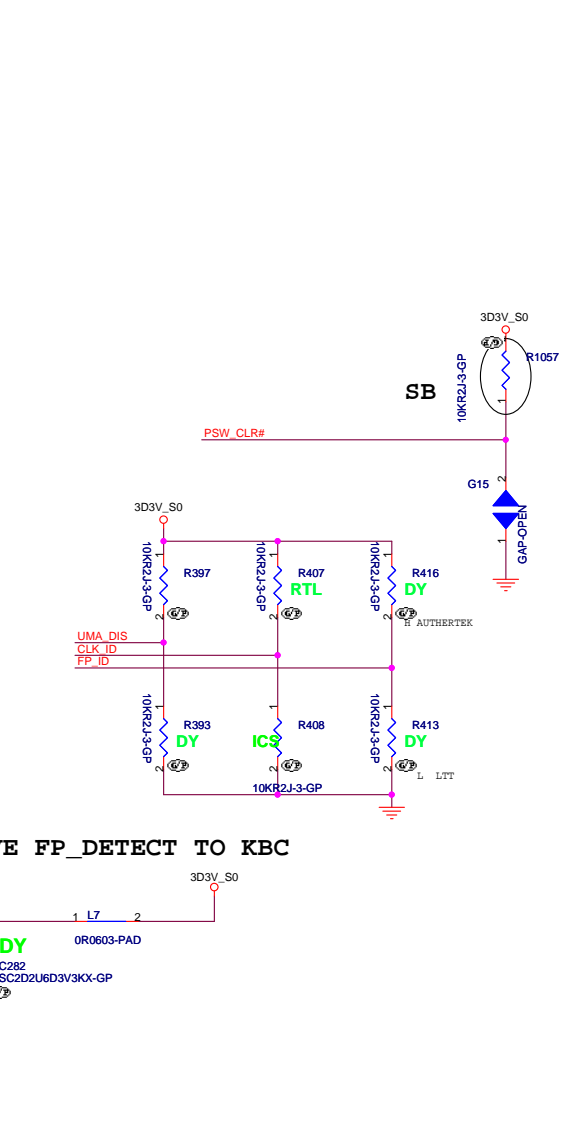
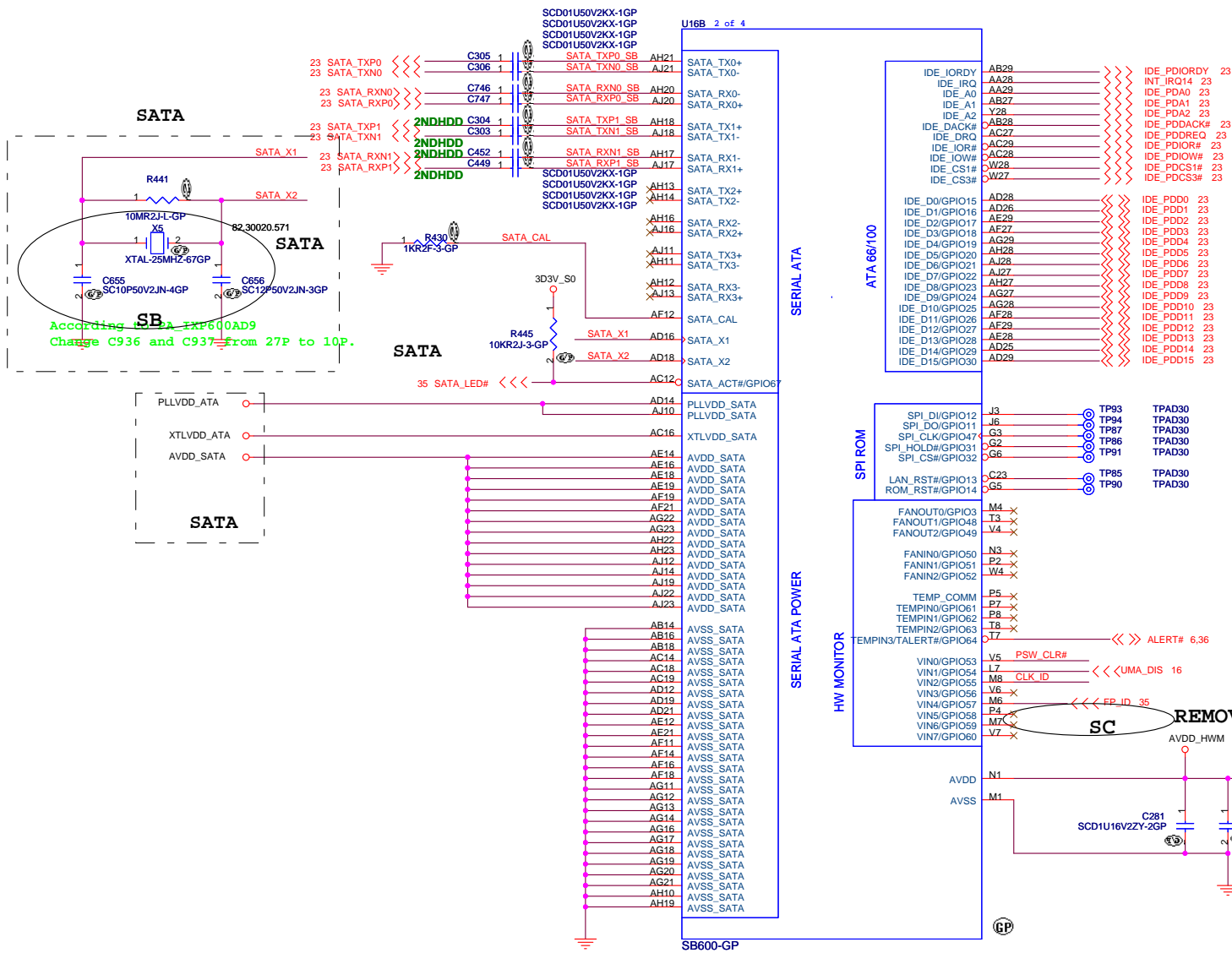
Secondary PCI Bus reset signal.



		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: SB600 PCI/CPU/LPC/RTC (1 of 5)			
Size A3	Document Number	Pomona/Texcoco	
Date: Thursday, March 29, 2007	Sheet	18	of 49

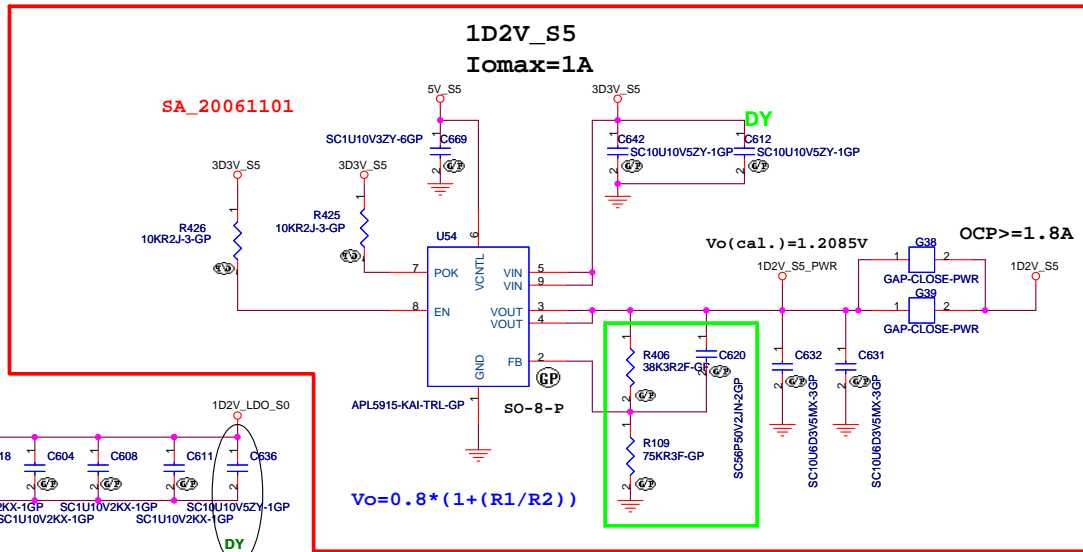
Dr-Bios.com

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB460

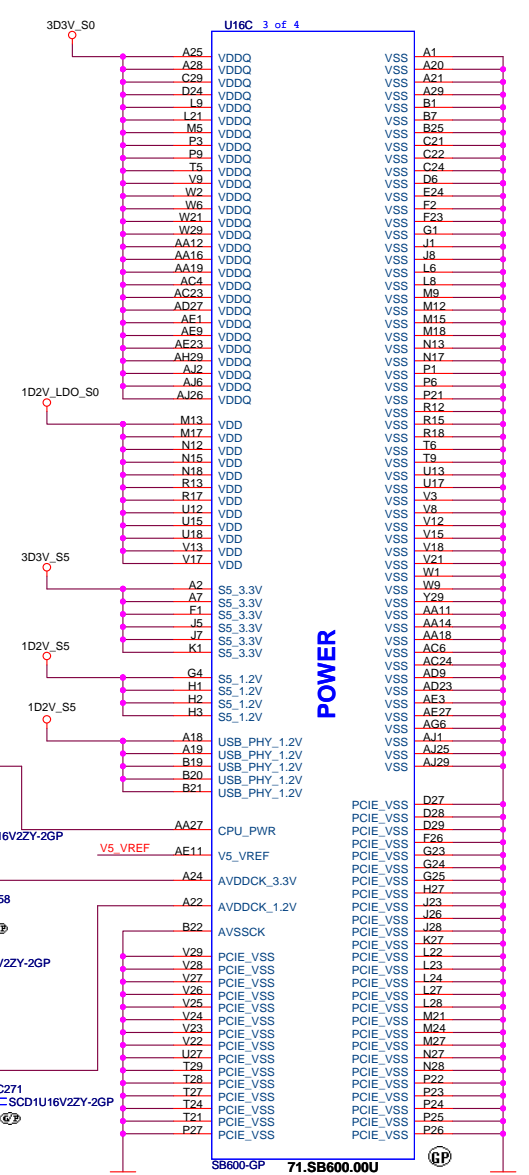
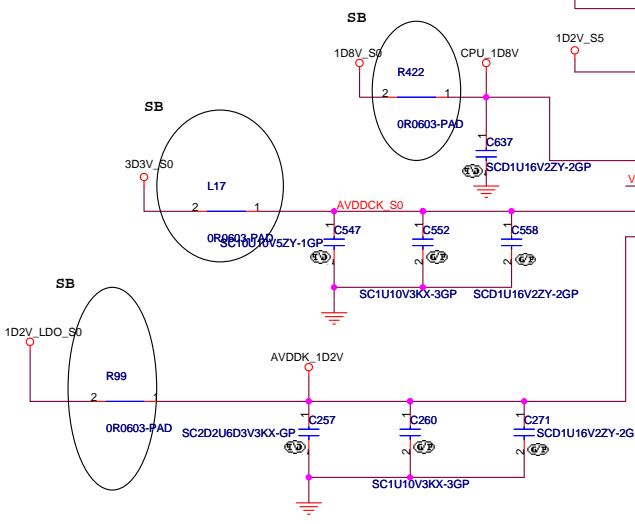
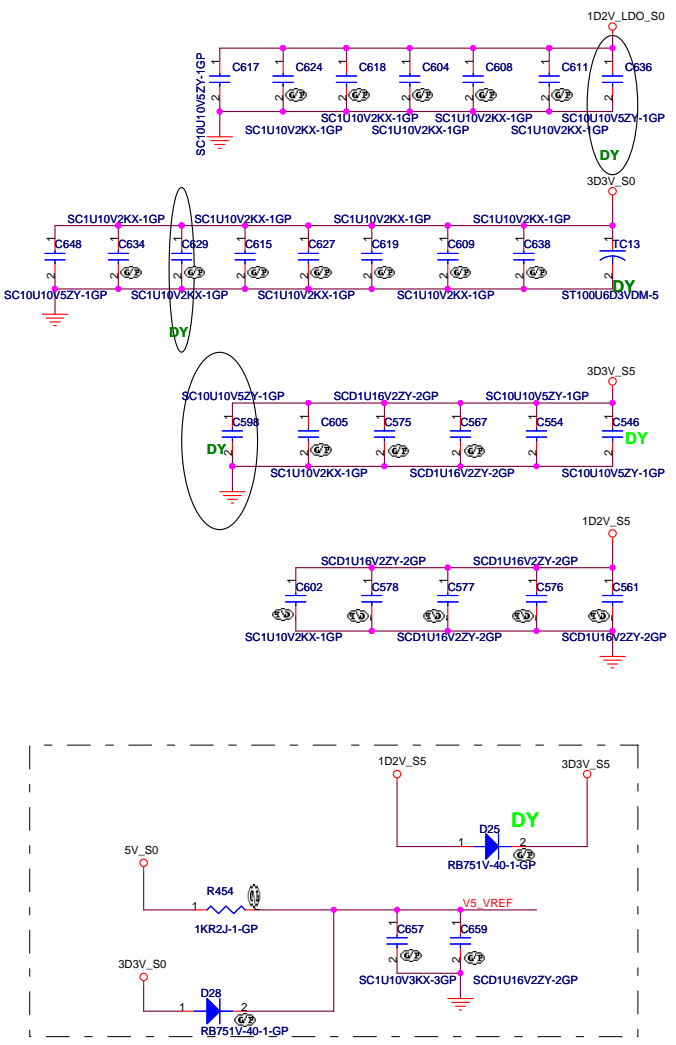


UMA		緯創資通 Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: SB600 ACPI/GPIO/SATA/IDE (2 of 5)			
Size A3	Document Number	Rev 1	
		Pomona/Textcoco	
Date: Thursday, March 29, 2007	Sheet 19	of 49	

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Place near to SB600



UMA

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Title: **SB600 POWER/DECOUPLING**

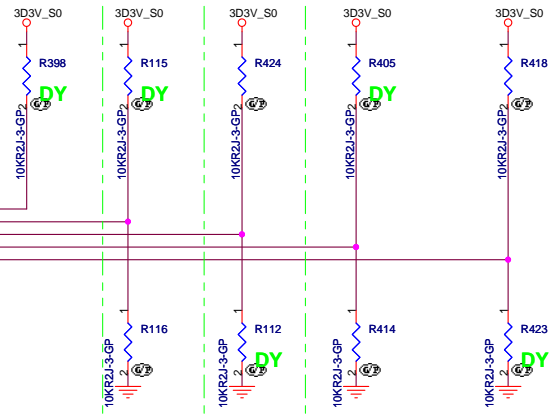
Size A3 Document Number **Pomona/Textcoco** Rev 1

Date: Thursday, March 29, 2007 Sheet 20 of 49

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PCI_CLK4
PCI_CLK6
PCI_CLK0
PCI_CLK1

21 AC_SDOUT
18,33 PCLK_KBC
18 CLK33 LPCROM
18,33 PCI_CLK0
18,27 PCLK_PCM

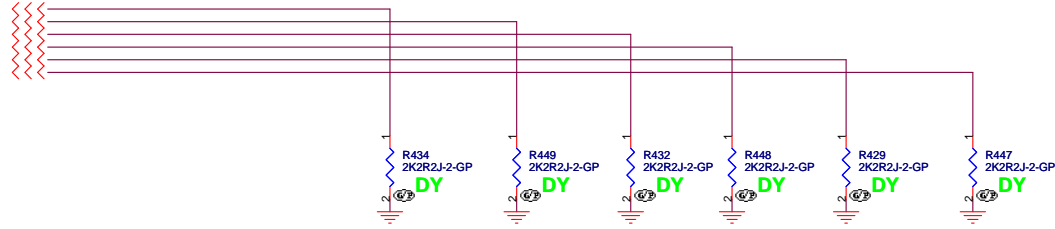


REQUIRED SYSTEM STRAPS

		SB600				
		AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM		
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

18,27 PCI_AD28
18,27 PCI_AD27
18,27 PCI_AD26
18,27 PCI_AD25
18,27 PCI_AD24
18,27 PCI_AD23



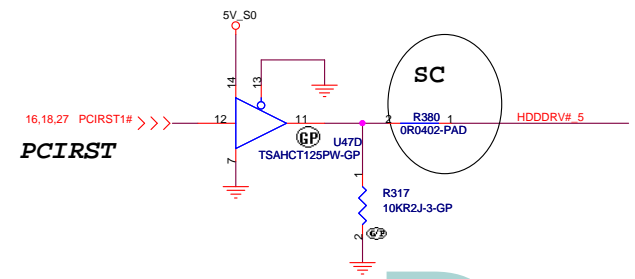
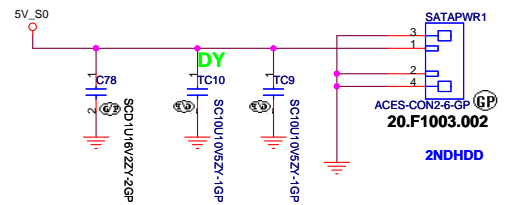
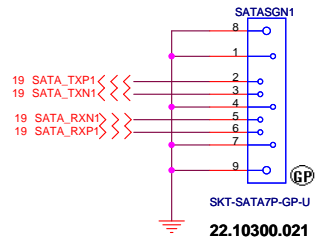
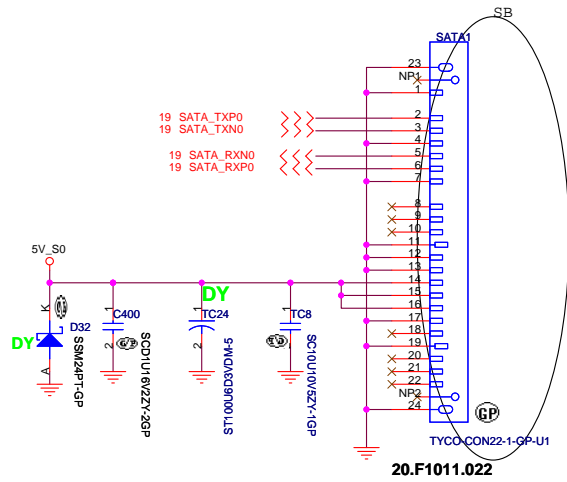
DEBUG STRAPS

STRAP	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

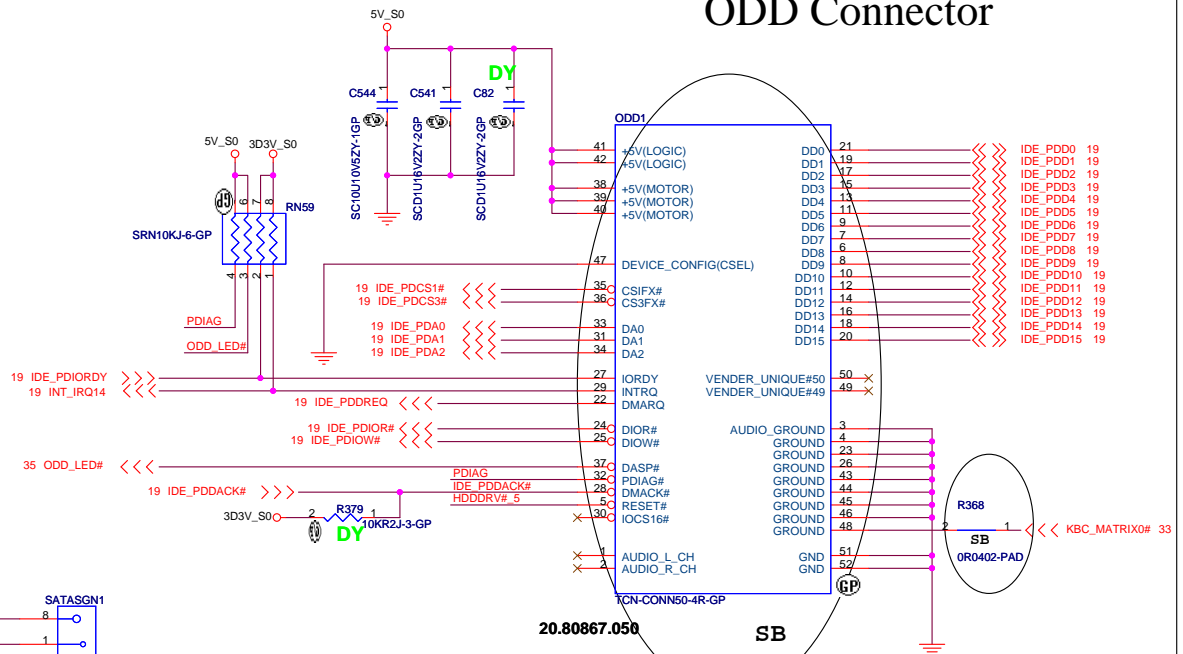
UMA

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
SB600 STRAPPING PIN	
Title	Rev 1
Size A3	Document Number Pomona/Texcoco
Date: Thursday, March 29, 2007 Sheet 22 of 49	

SATA HD Connector



ODD Connector



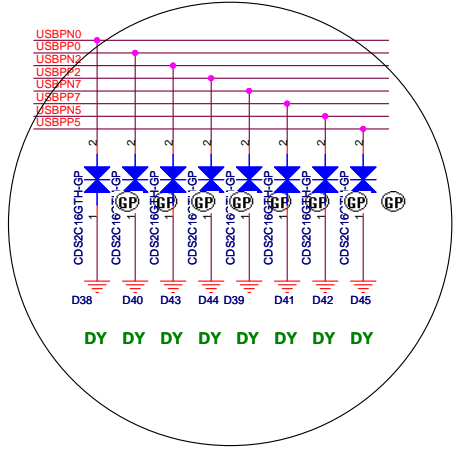
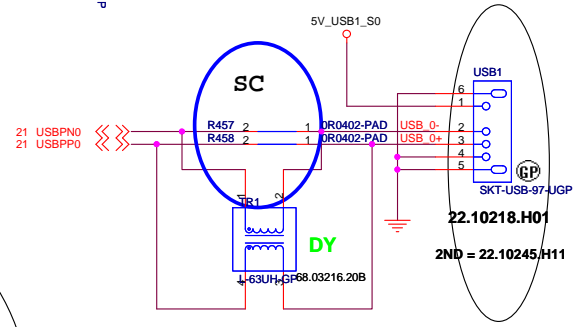
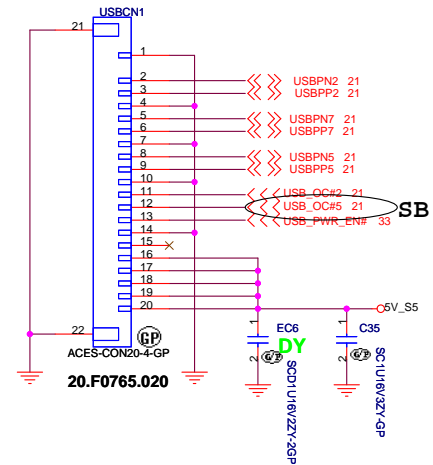
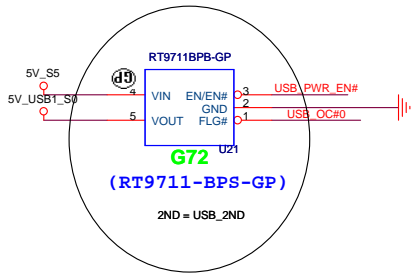
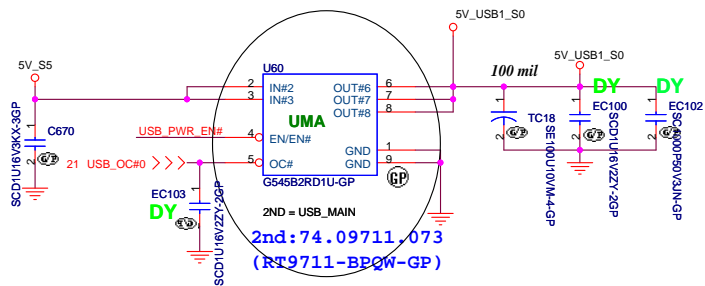
UMA

緯創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

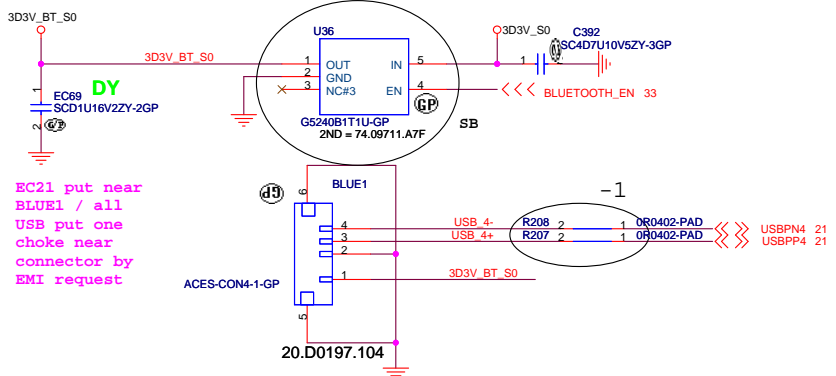
Title
HDD and CDROM

Size Document Number
Pomona/Textcoco

Date: Thursday, March 29, 2007 Sheet 23 of 49

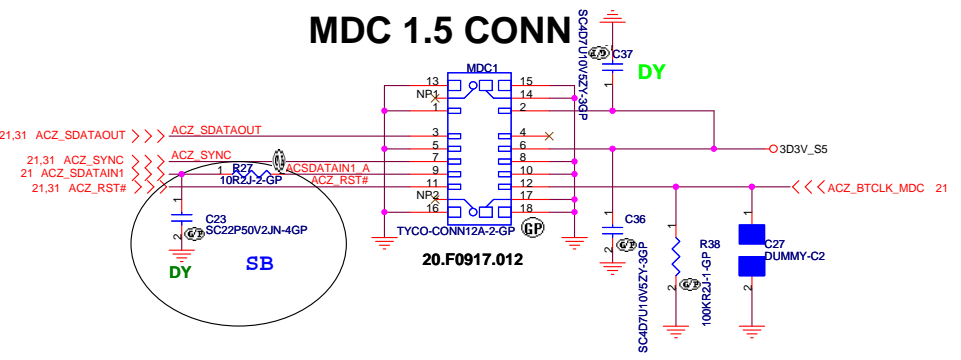


BLUETOOTH MODULE

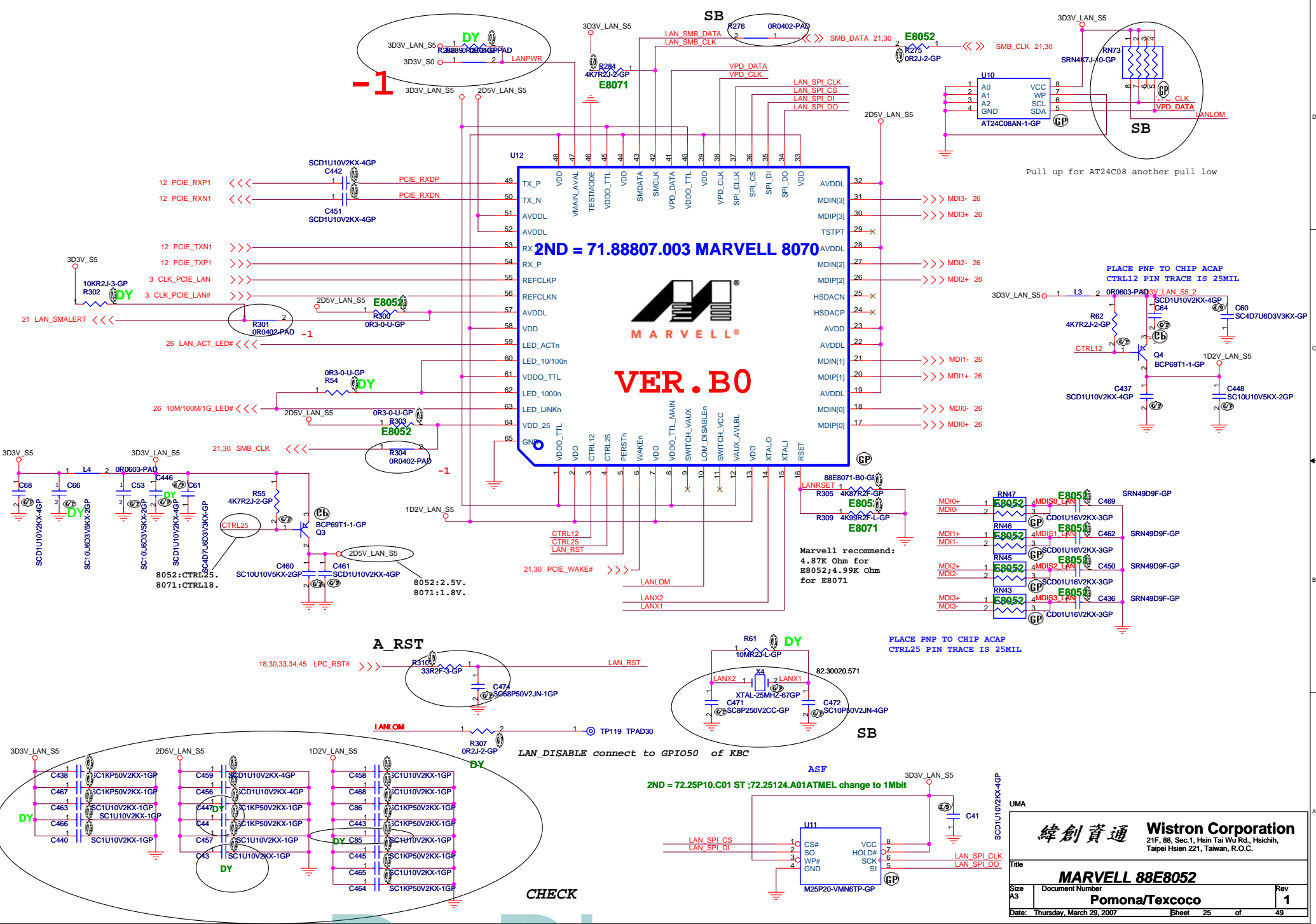


EC21 put near BLUE1 / all USB put one choke near connector by EMI request

MDC 1.5 CONN



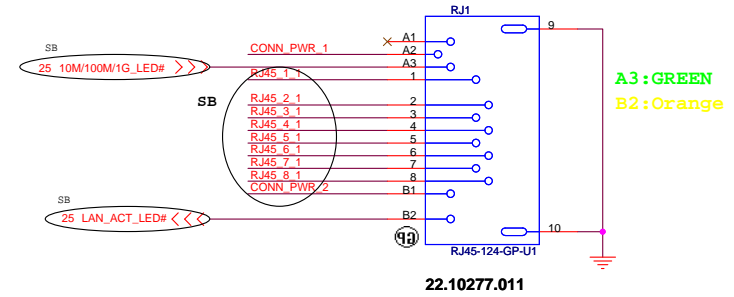
UMA		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB / MDC / BLUETOOTH			
Size	Document Number	Pomona/Textcoco	Rev 1
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<p>緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>TITLE MARVELL 88E8052</p>	
<p>Size A3</p>	<p>Document Number Pomona/Textcoco</p>
<p>Date Thursday, March 29, 2007</p>	<p>Rev 1</p>
<p>Sheet 25 of 49</p>	

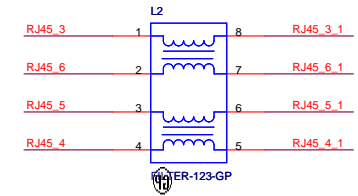
LAN Connector



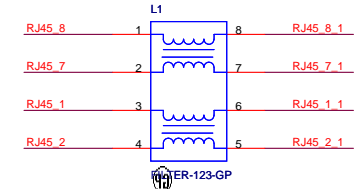
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

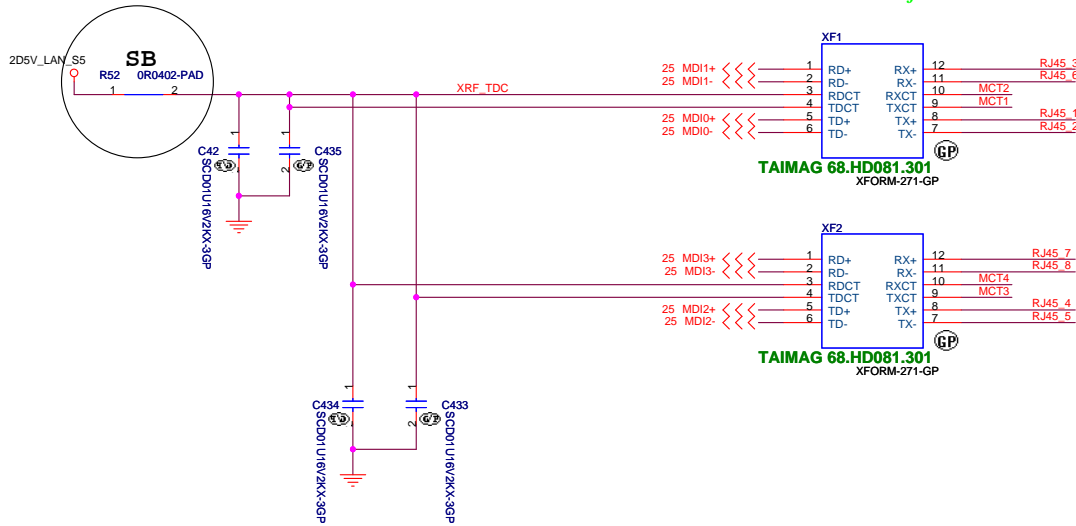
For EMI



-1



SC CHANGE 69.10106.021 TO 69.10106.011



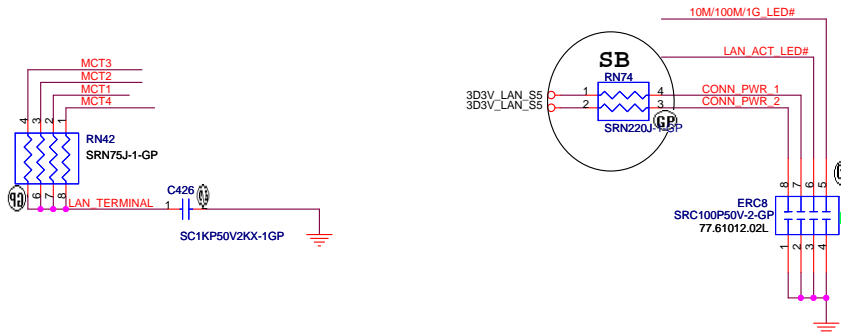
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP, DOC_RING, TIP, RING:

W/S: 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



UMA

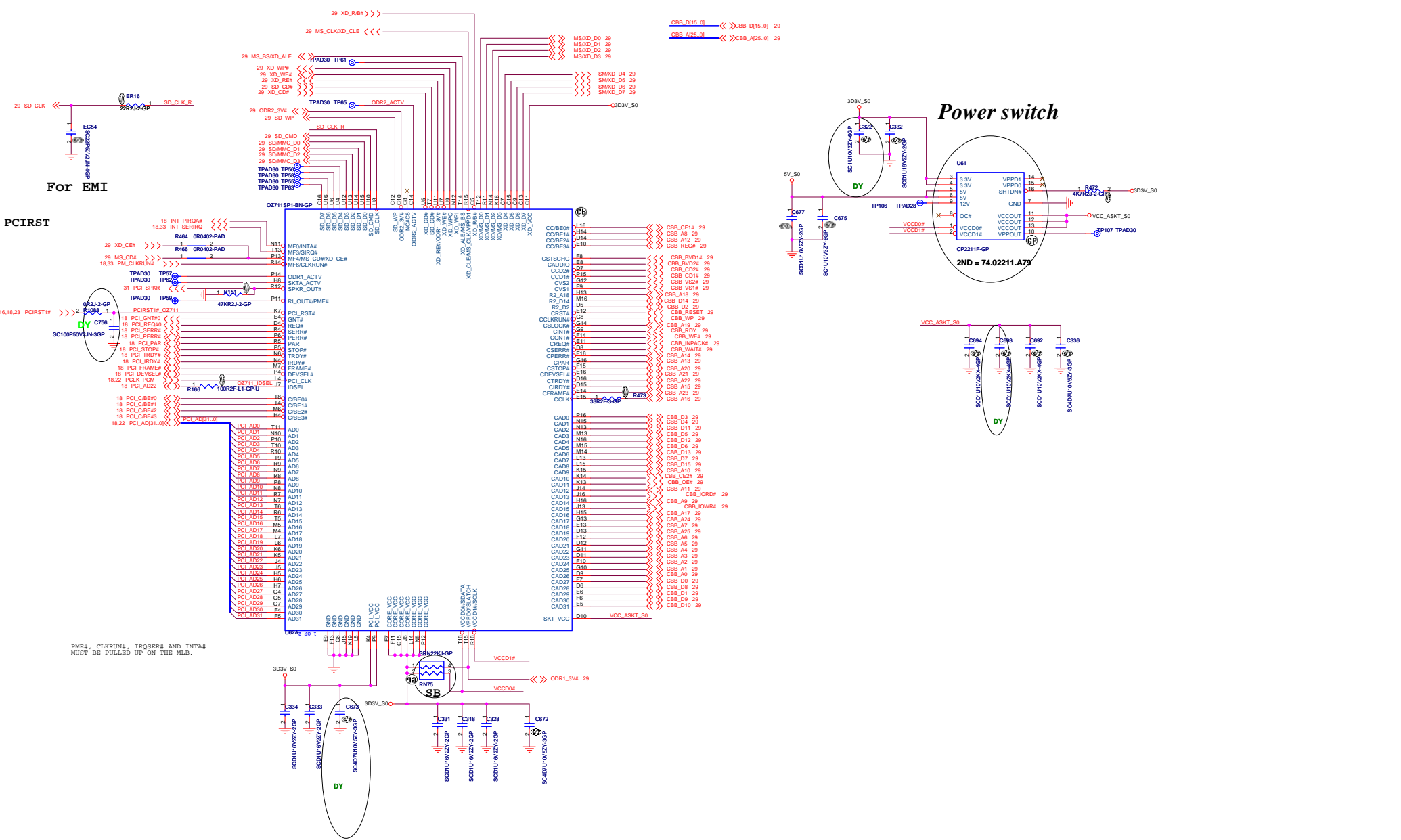
緯創資通 Wistron Corporation
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Title

LAN Connector

Size A3 Document Number Pomona/Textcoco Rev 1

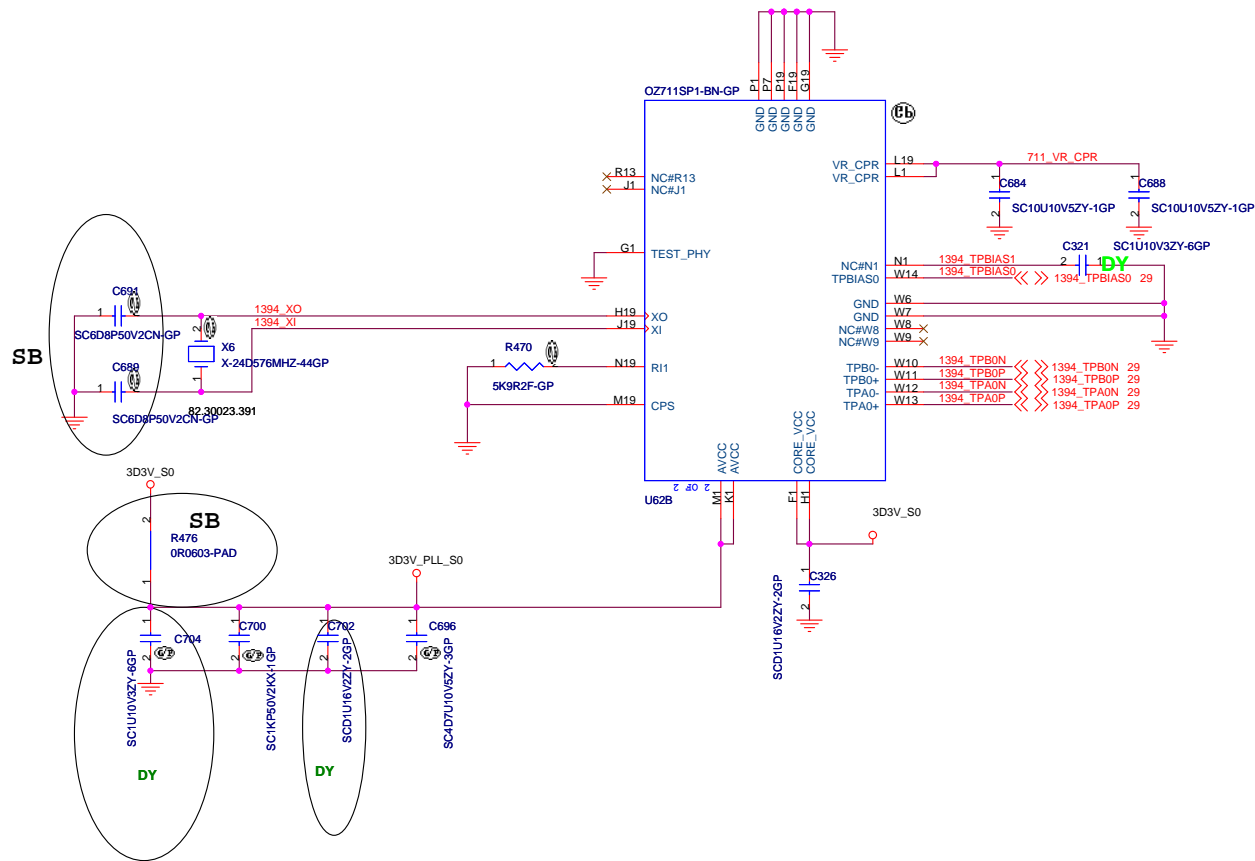
Date: Thursday, March 29, 2007 Sheet 26 of 49



For EMI

PCIRST

Power switch

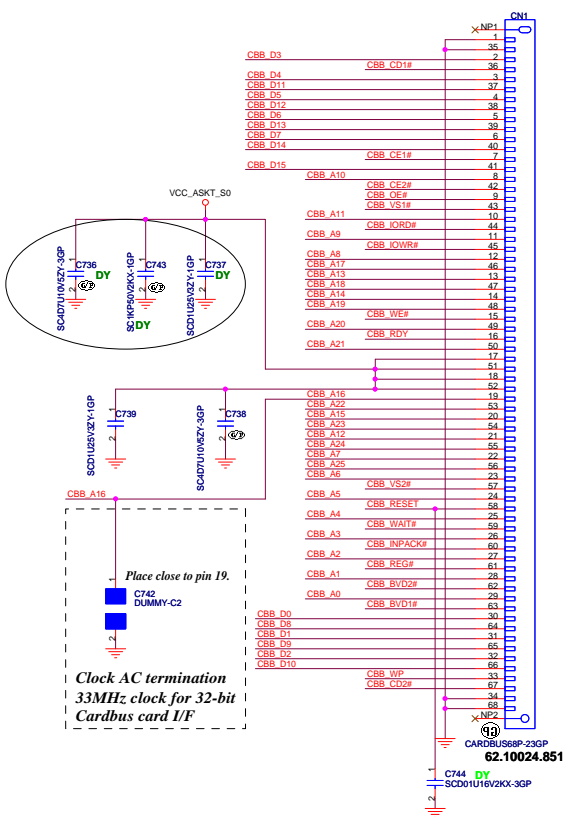


UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
OZ711SP1 (2 of 2)			
Size	Document Number	Pomona/Textcoco	
			Rev 1
Date: Thursday, March 29, 2007		Sheet 28 of 49	

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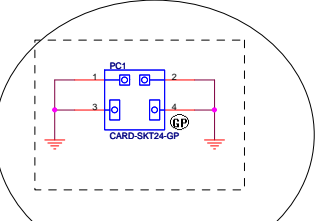
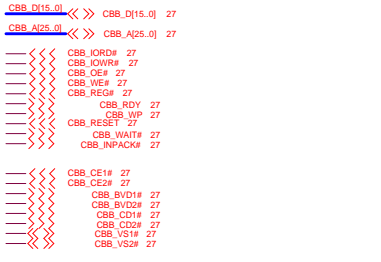
PCMCIA Socket



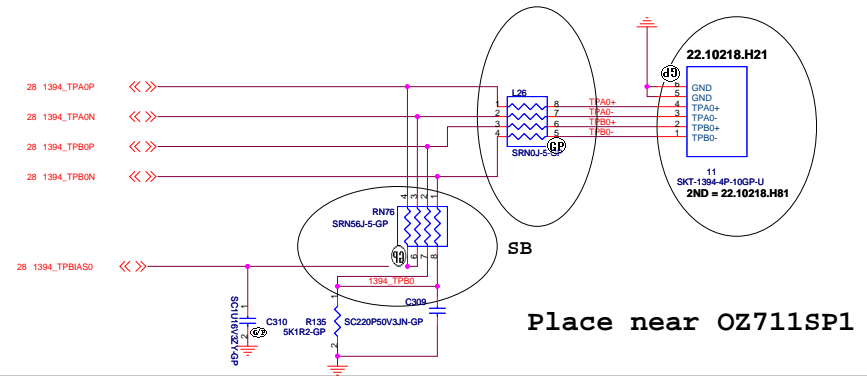
Place close to pin 19.
C742
DUMMY-C2

Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F

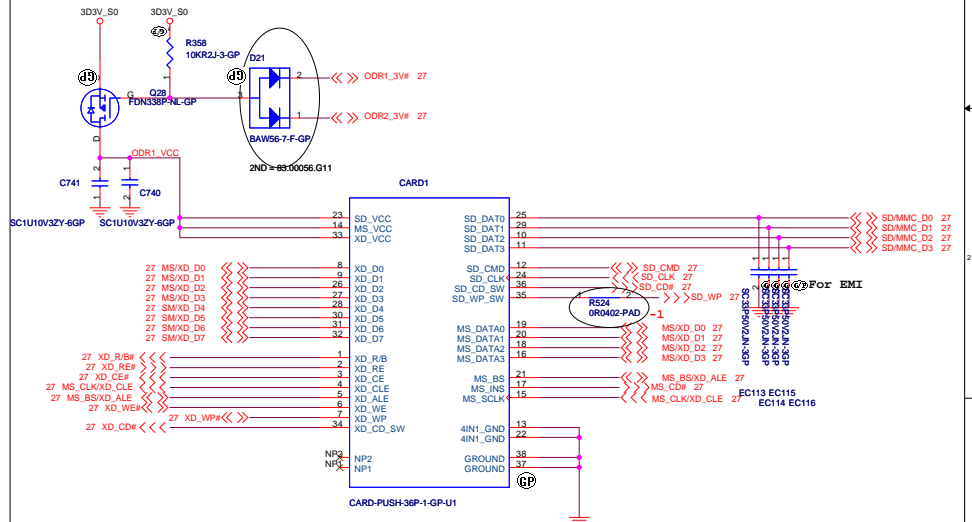
Cardbus I/F



1394 Connector



Place near OZ711SP1



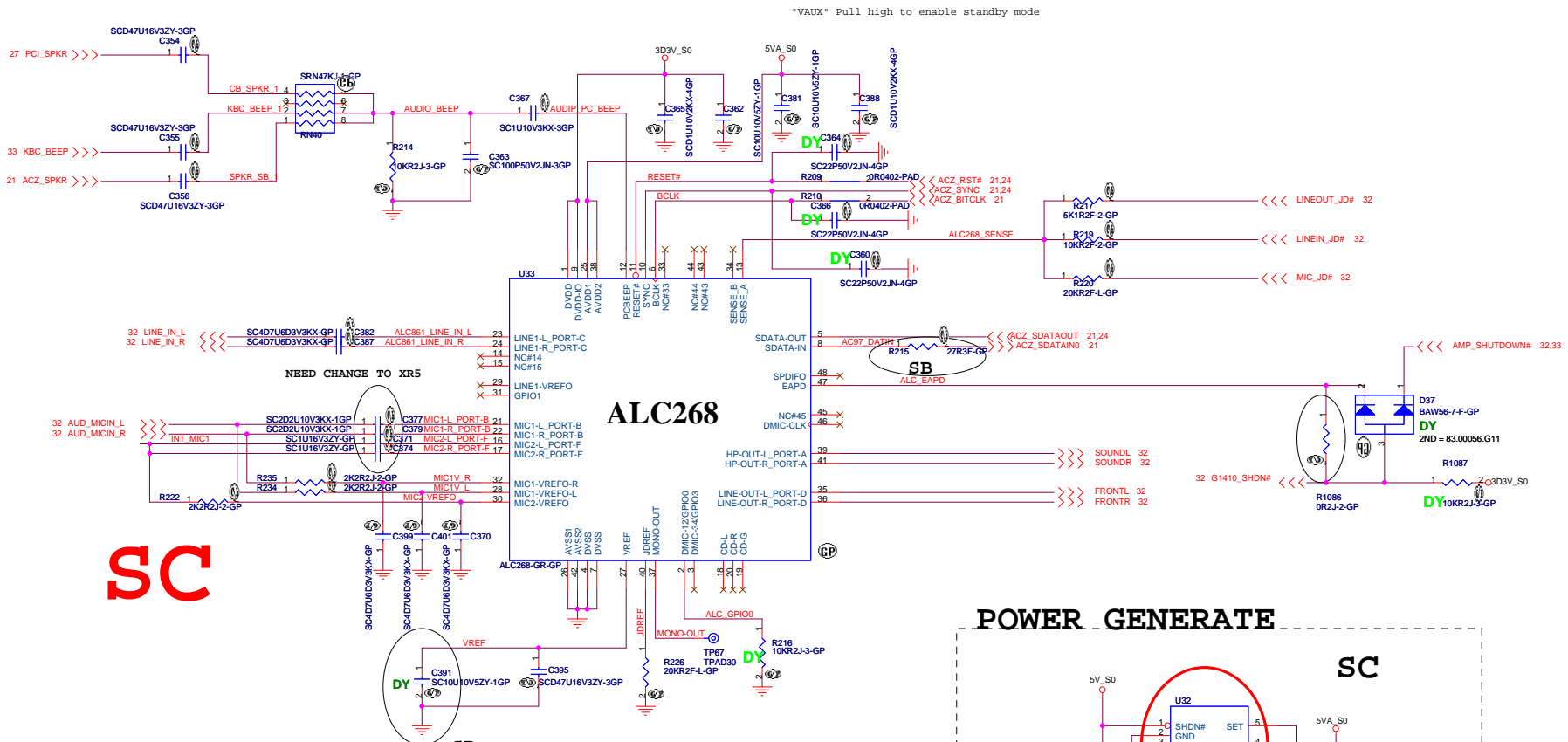
XD
MS / MS PRO
SD / SD IO / MMC

UMA
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichu, Taipei Hsin 221, Taiwan, R.O.C.

Title **PCMCIA / 1394 / CARD READER**

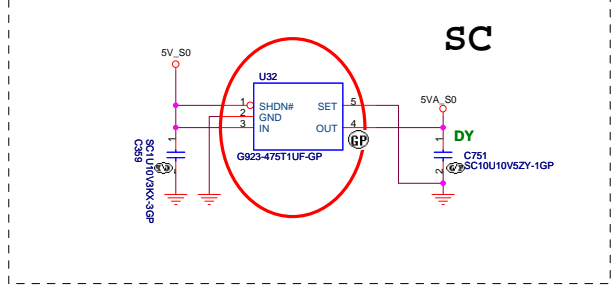
Size Document Number **Pomona/Textcoco** Rev 1

Date: Thursday, March 29, 2007 Sheet 29 of 49

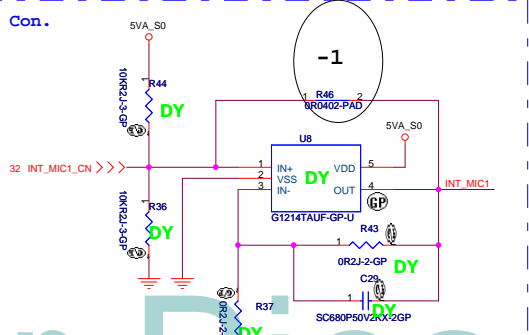


SC

POWER GENERATE



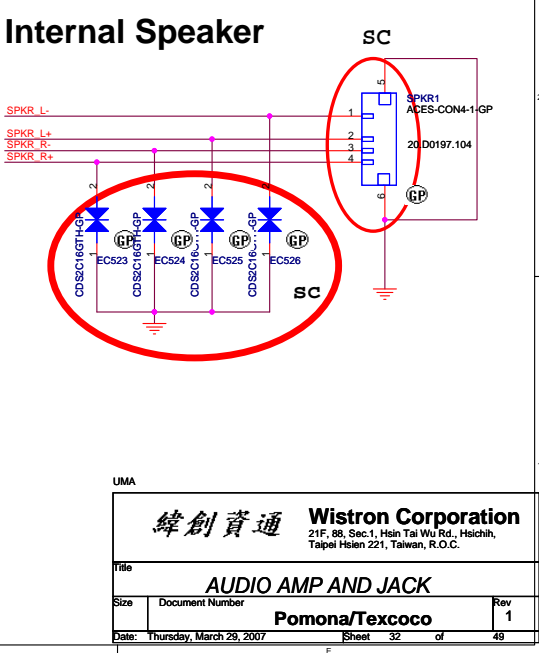
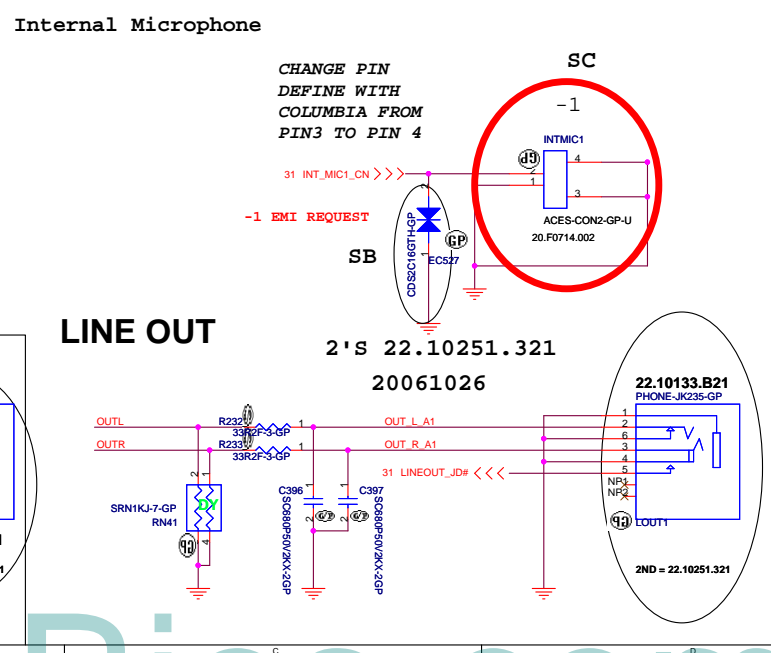
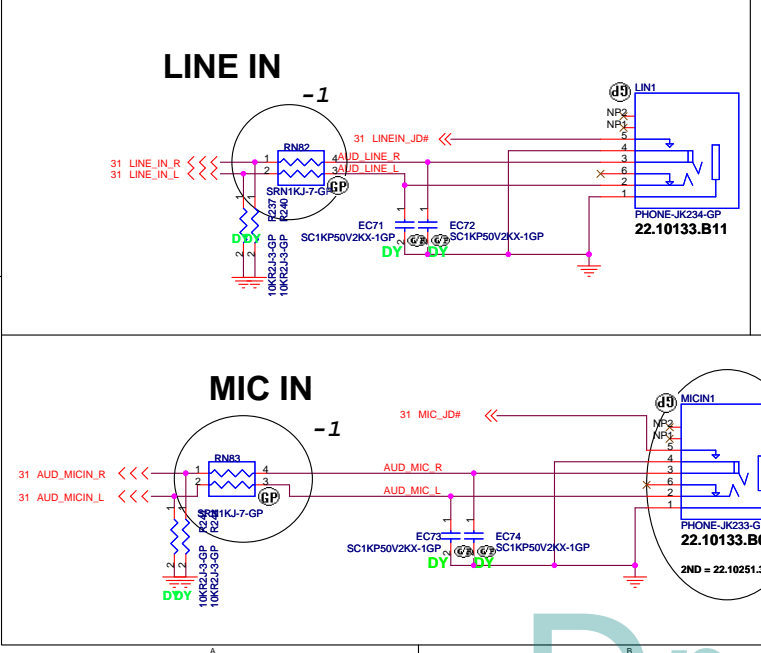
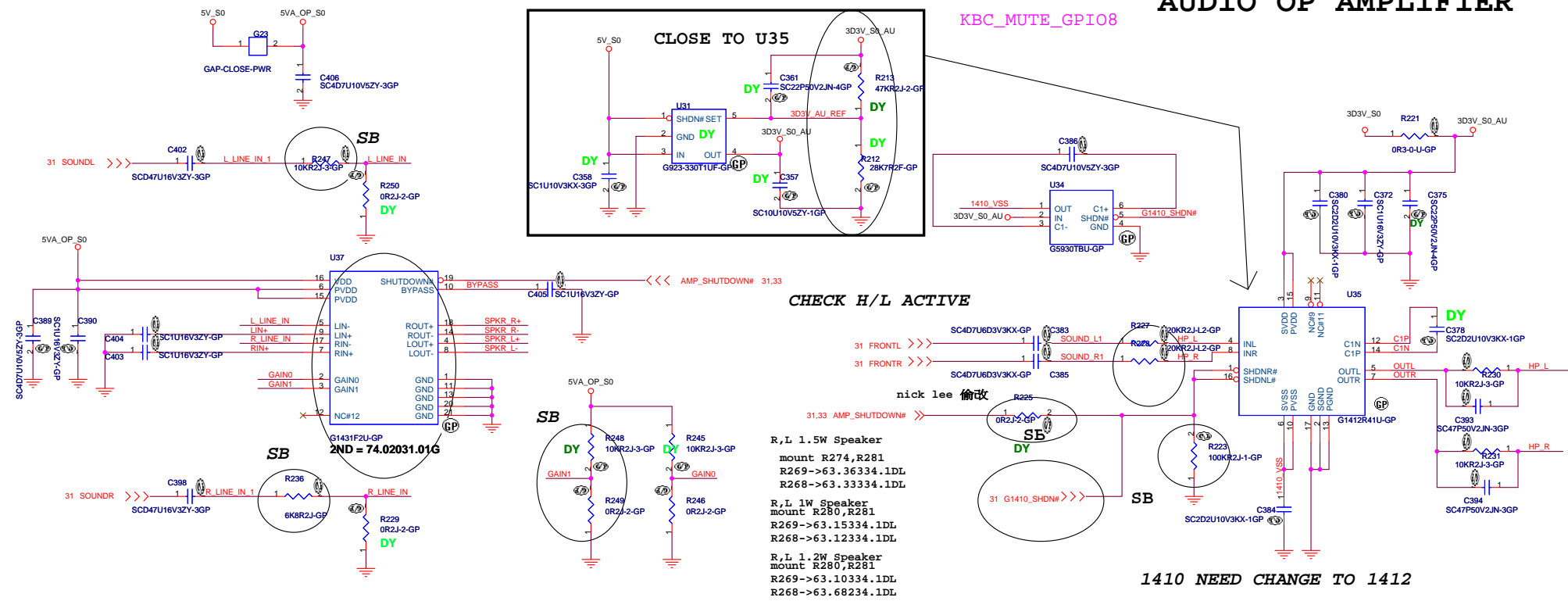
Near INTMIC Con.



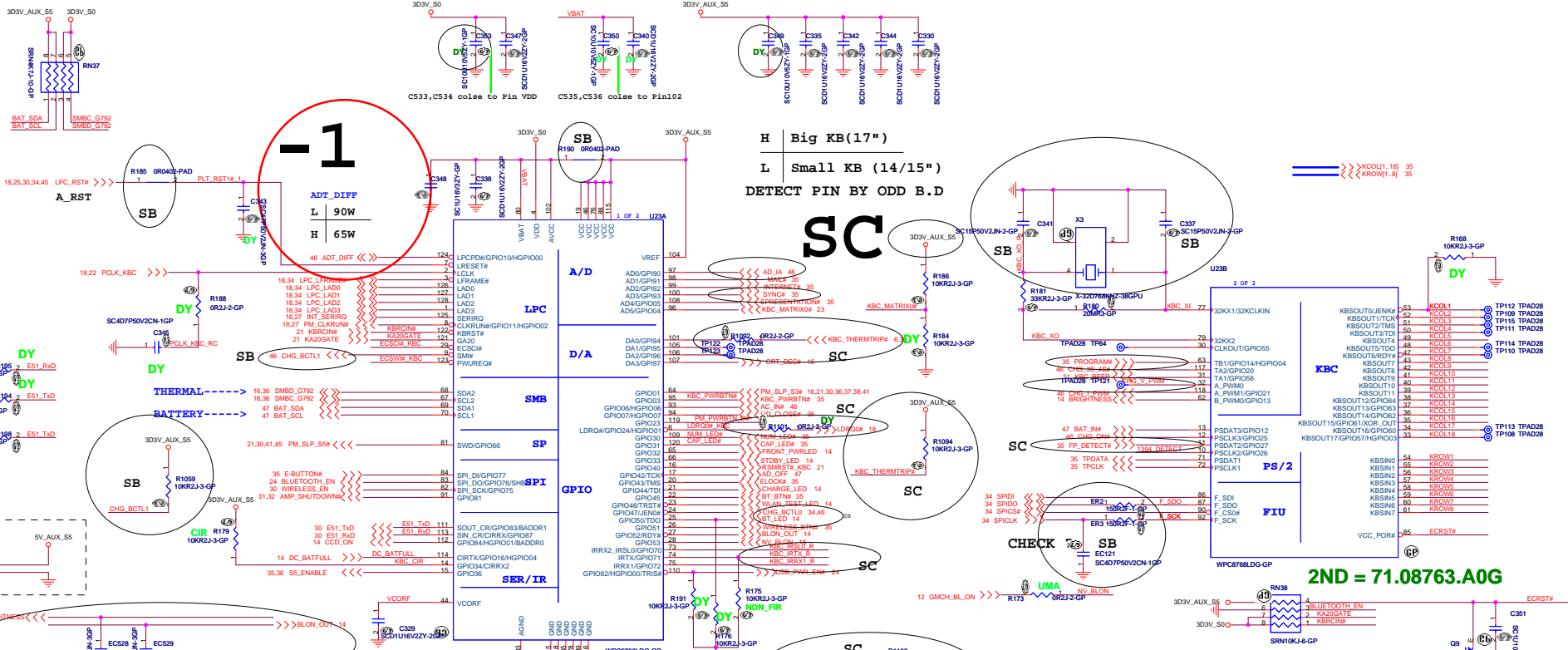
SC

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AUDIO OP AMPLIFIER



UMA		Wistron Corporation	
緯創資通		21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: AUDIO AMP AND JACK			
Size	Document Number	Pomona/Textcoco	
Date: Thursday, March 29, 2007	Sheet 32	of	49



H Big KB (17")
 L Small KB (14/15")
 DETECT PIN BY ODD B.D

SC

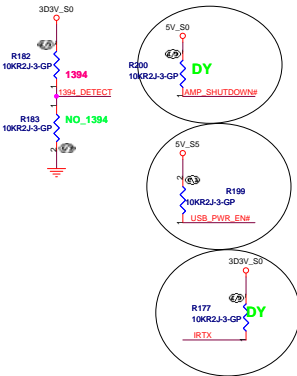
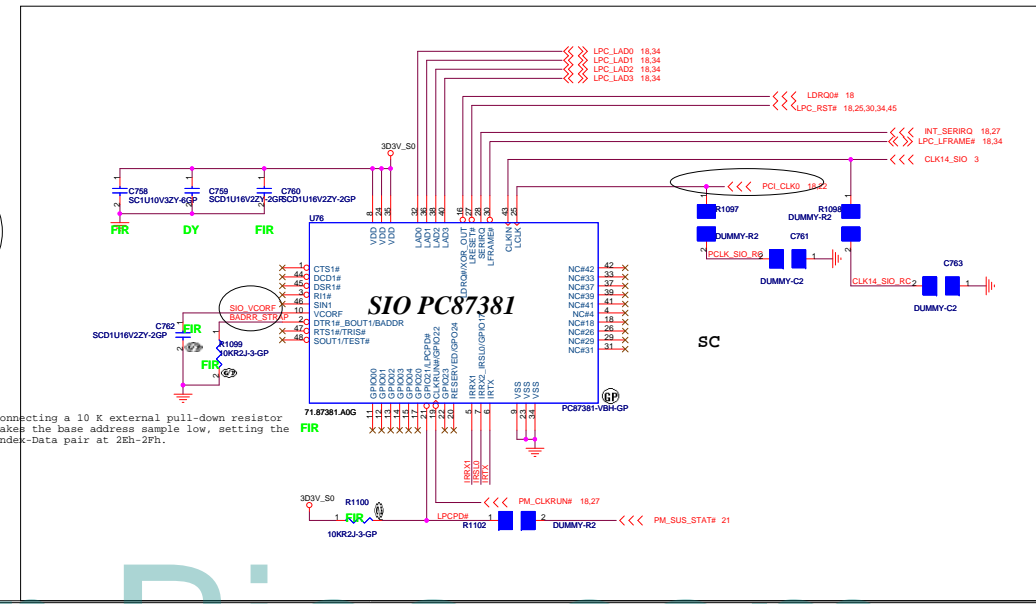
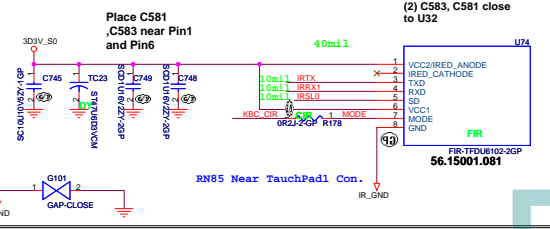
2ND = 71.08763.A0G

2ND = 71.08763.A0G

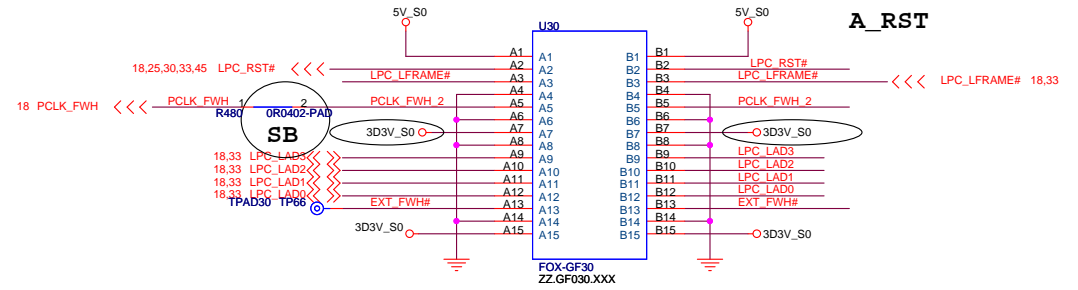
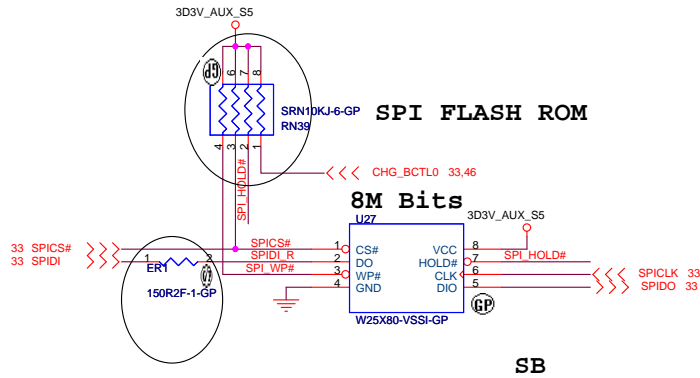
FOR KBC DEBUG

SC

VISHAY FIR Module



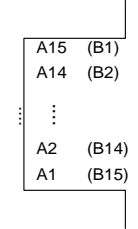
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GOLDEN FINGER FOR DEBUG BOARD
Check;MYALL M

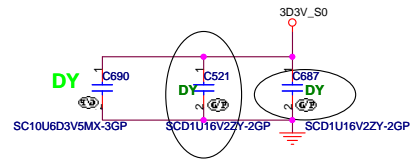
1. Add serial resistor 150 Ohm and Bypass Cap 4.7P on SPI_CLK(Close to KBC)
2. Add serial resistor 150 Ohm on SPI_DO(Close to KBC)
3. Add serial resistor 150 Ohm on SPI_DI(Close to SPI Flash)

TOP VIEW

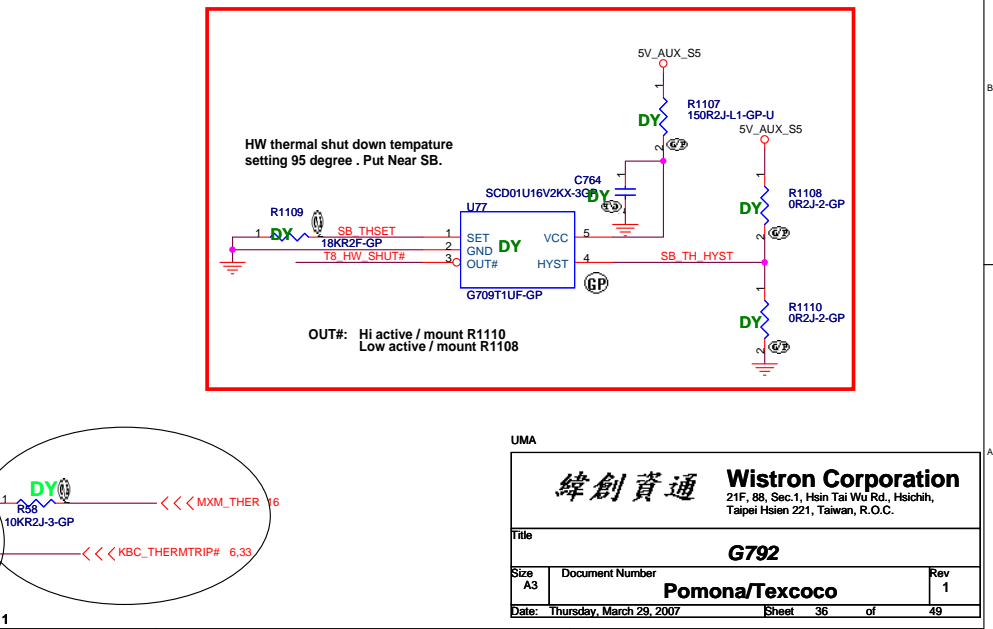
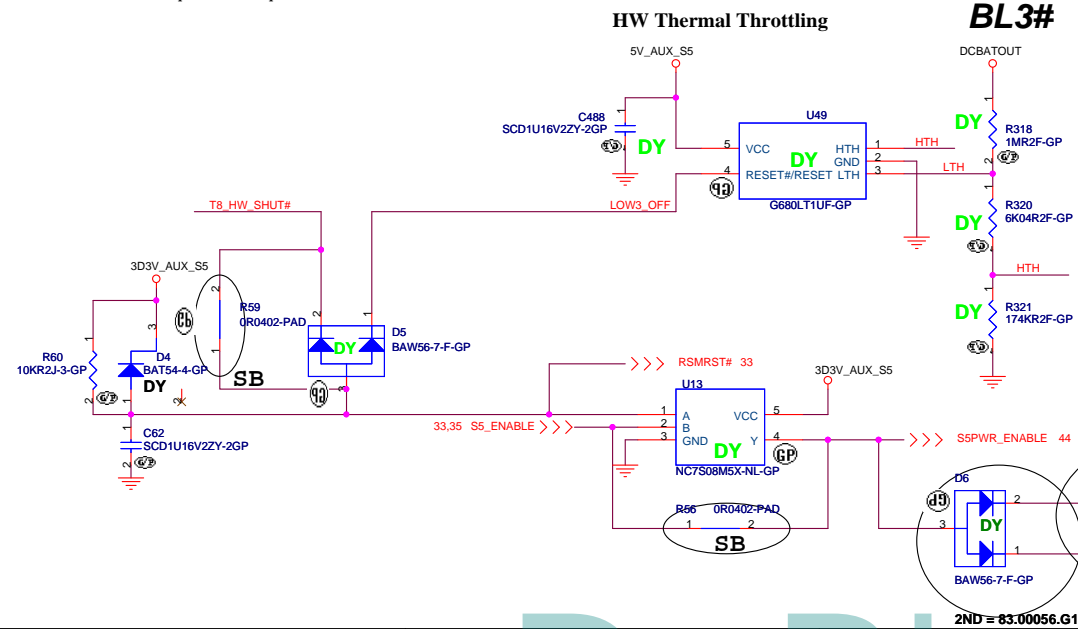
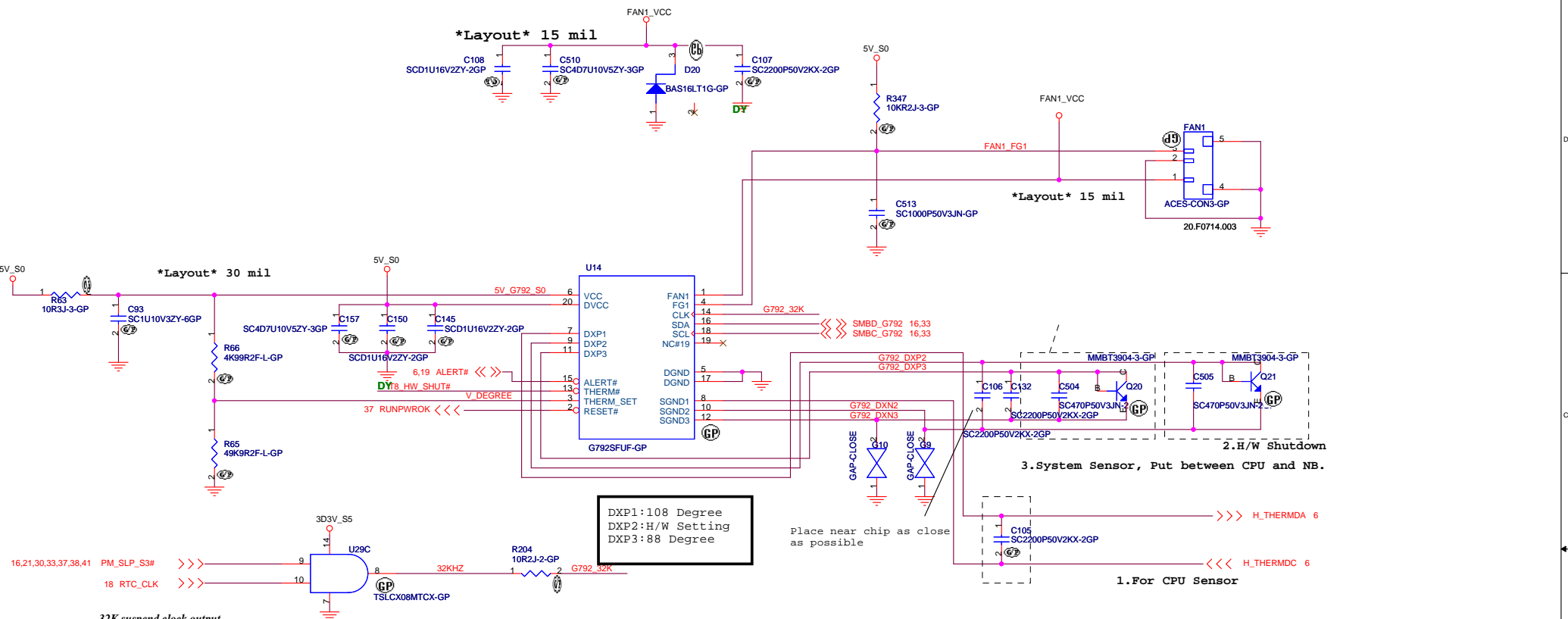


(BOTTOM VIEW)

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

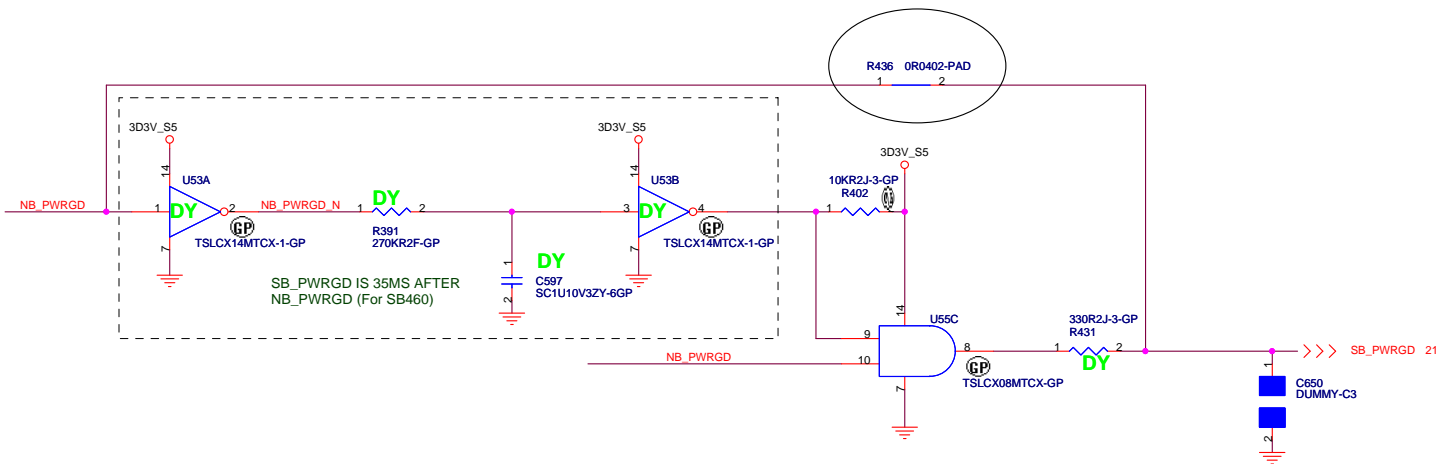
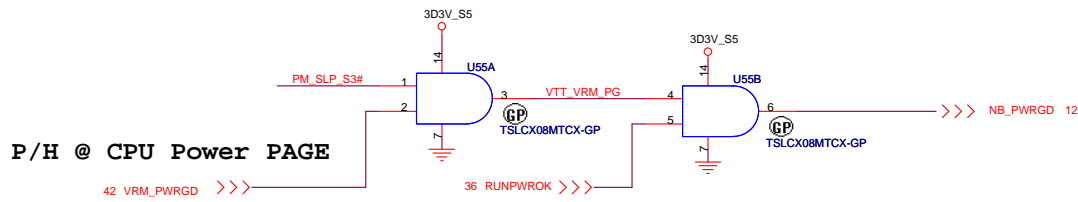
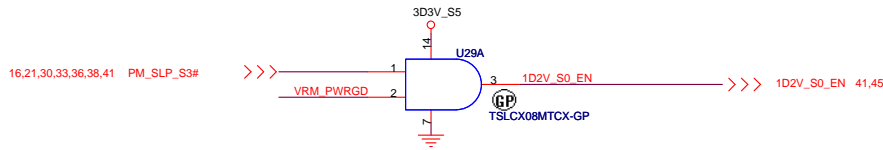
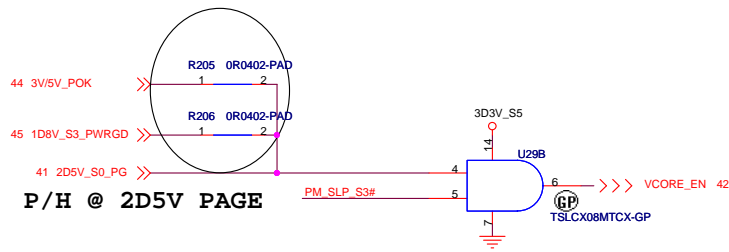


UMA			
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BIOS			
Size	Document Number	Rev	
A3	Pomona/Texcoco	1	
Date: Thursday, March 29, 2007		Sheet	49



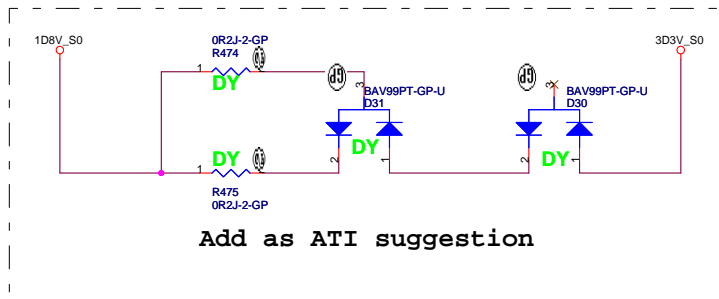
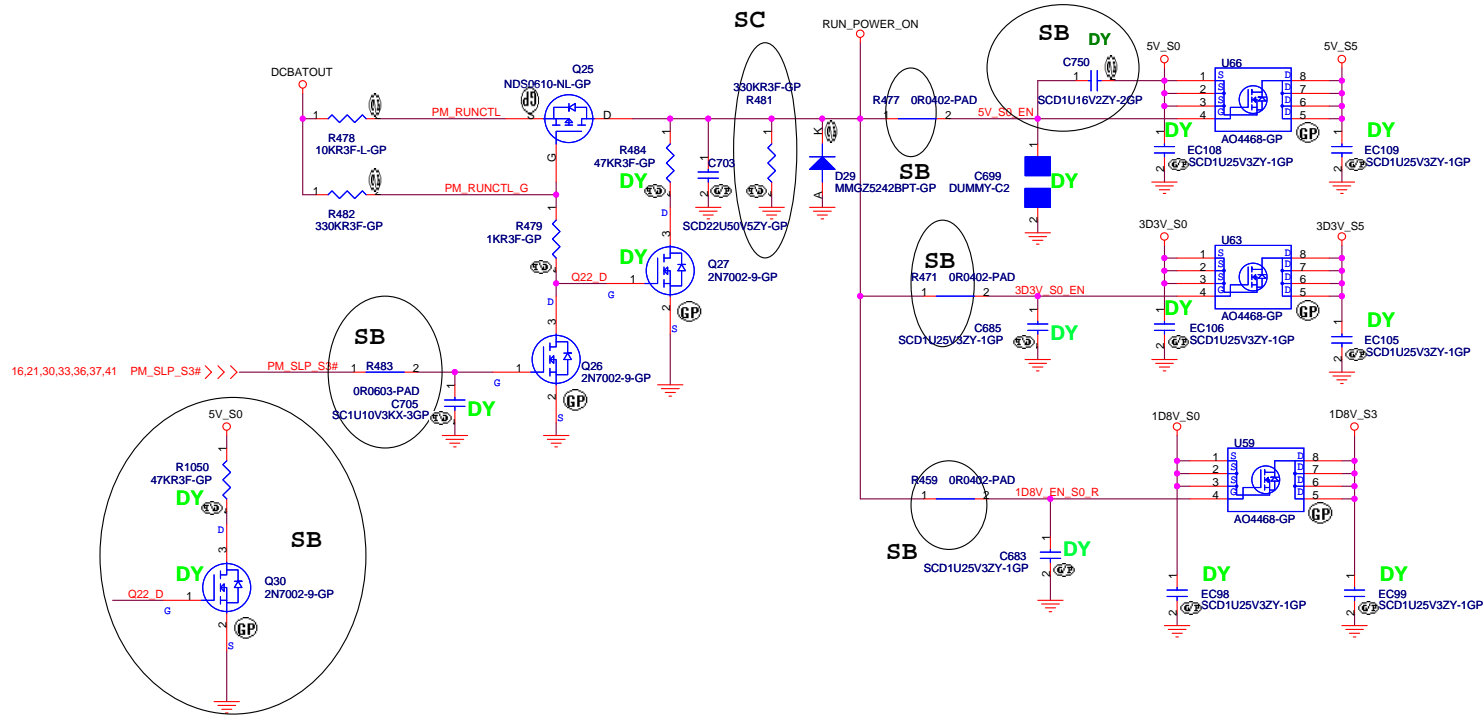
UMA		緯創資通 Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		G792	
Size A3	Document Number	Pomona/Textcoco	
Date: Thursday, March 29, 2007	Sheet 36	of 49	

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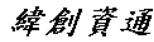
UMA		
緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	POWERGOOD&ENABLES(1/2)	
Size	Document Number	Rev
A3	Pomona/Textcoco	1
Date:	Thursday, March 29, 2007	Sheet 37 of 49

Run Power Switch



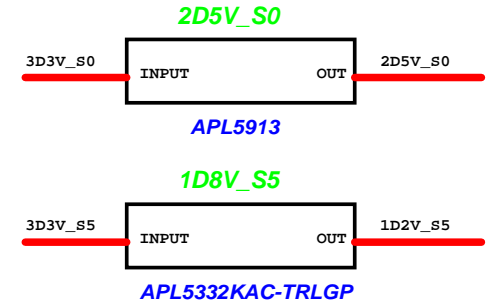
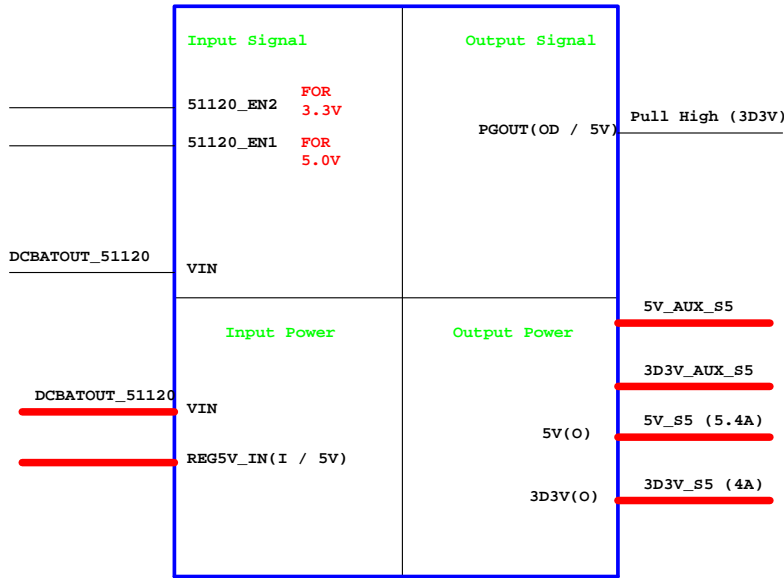
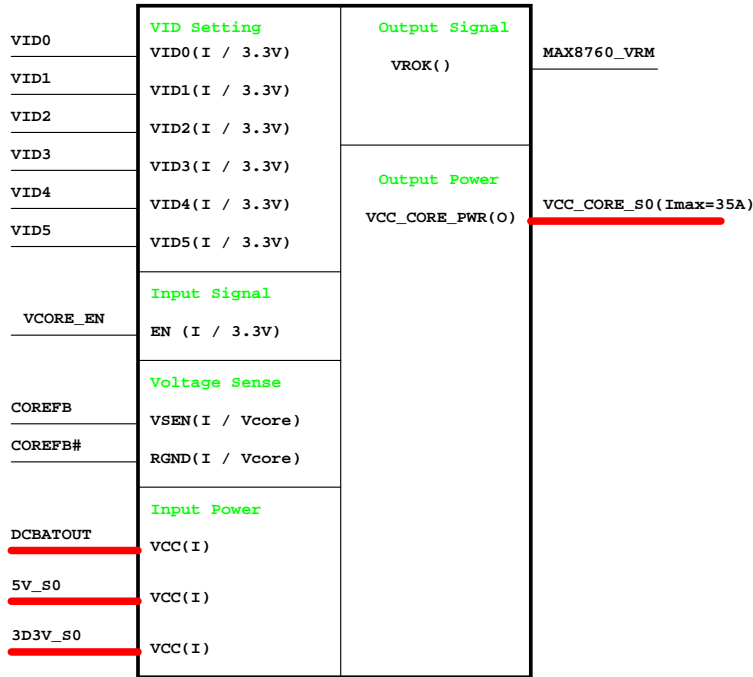
Add as ATI suggestion

UMA

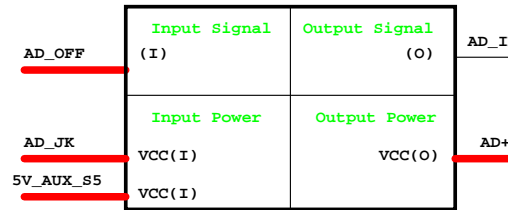
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title PWR CTL LOGIC / PWR PLANE		
Size A3	Document Number Pomona/Textcoco	Rev 1
Date: Thursday, March 29, 2007		Sheet 38 of 49

TI TPS51120
3D3V/5V

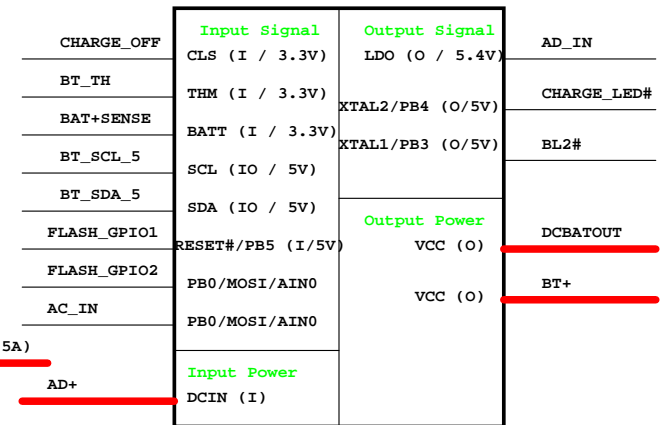
CPU_CORE
ISL6264CRZ



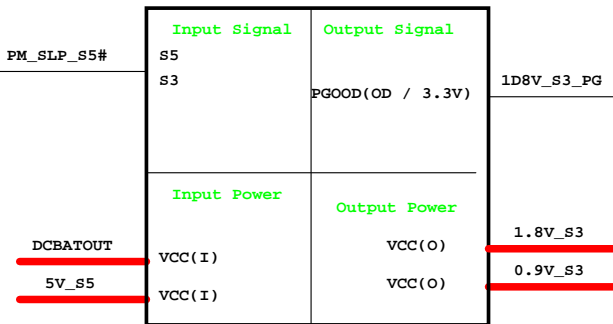
Adapter



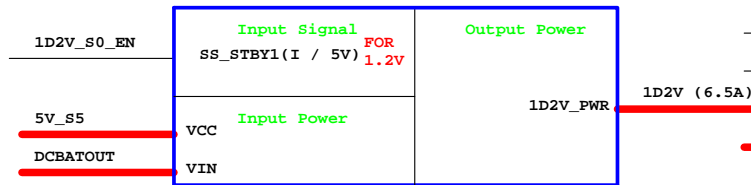
Charger_ISL6255



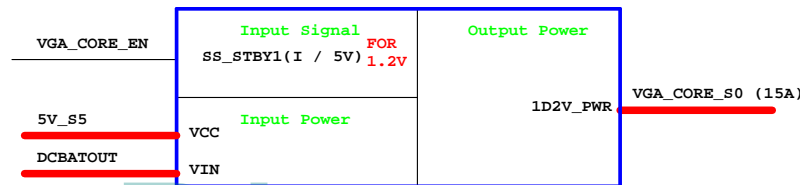
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



ISL6268_VGA_CORE

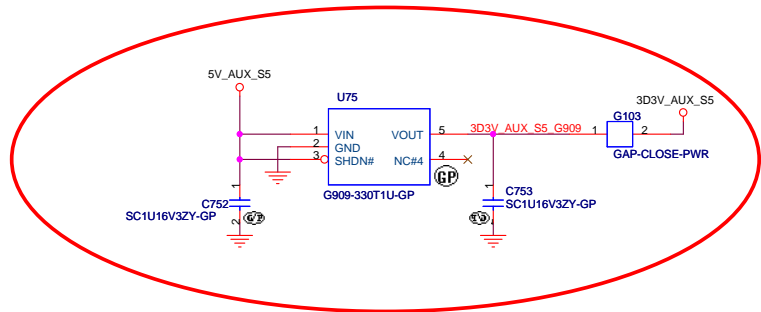


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Power Block Diagram	
Title	Rev
Size A3	Document Number
Pomona/Texcoco	
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Aux Power 3D3V_AUX_S5

Aux Power 3D3V_AUX_S5

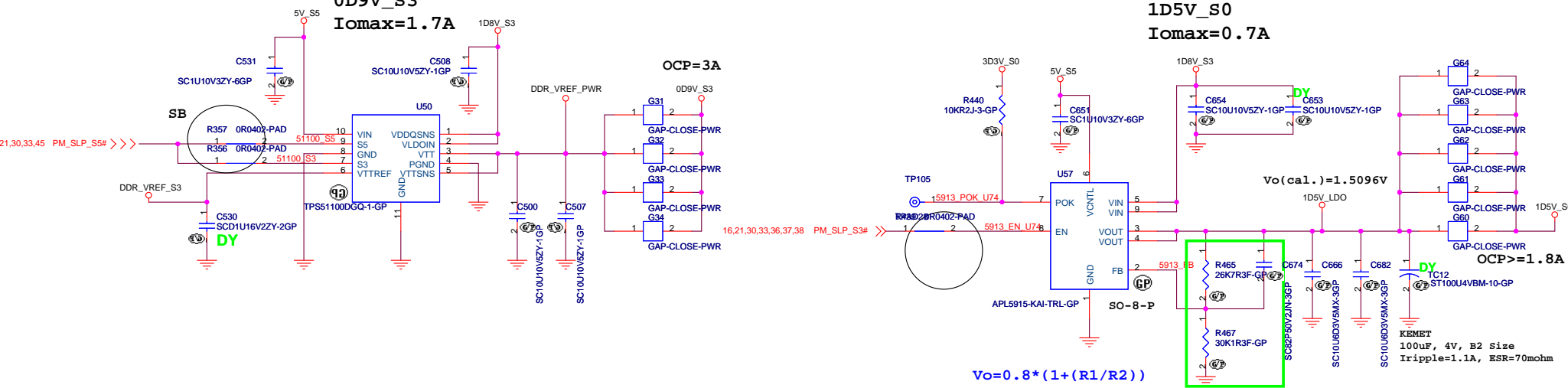


SB modify

UMA			
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Title			
3D3V_AUX			
Size	Document Number		Rev
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0D9V_S3
Iomax=1.7A

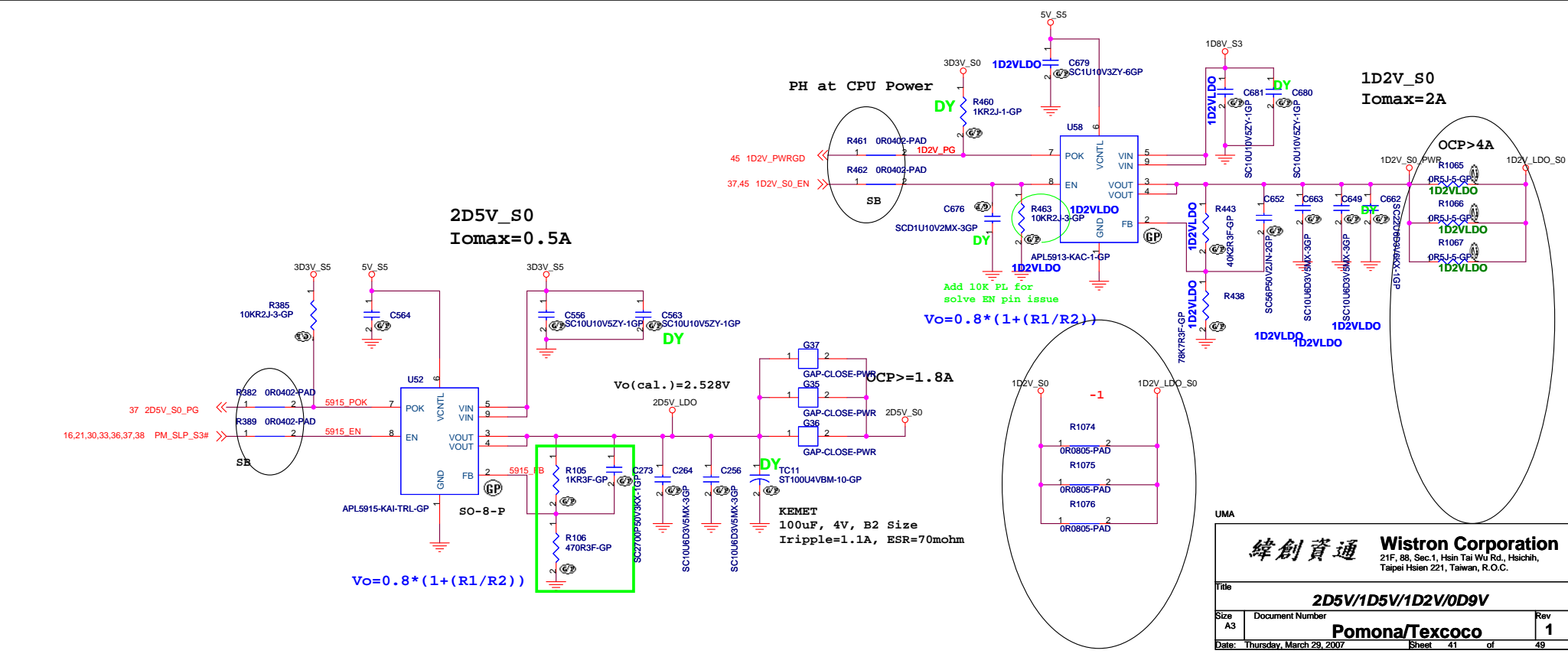
1D5V_S0
Iomax=0.7A



2D5V_S0
Iomax=0.5A

PH at CPU Power

1D2V_S0
Iomax=2A



UMA

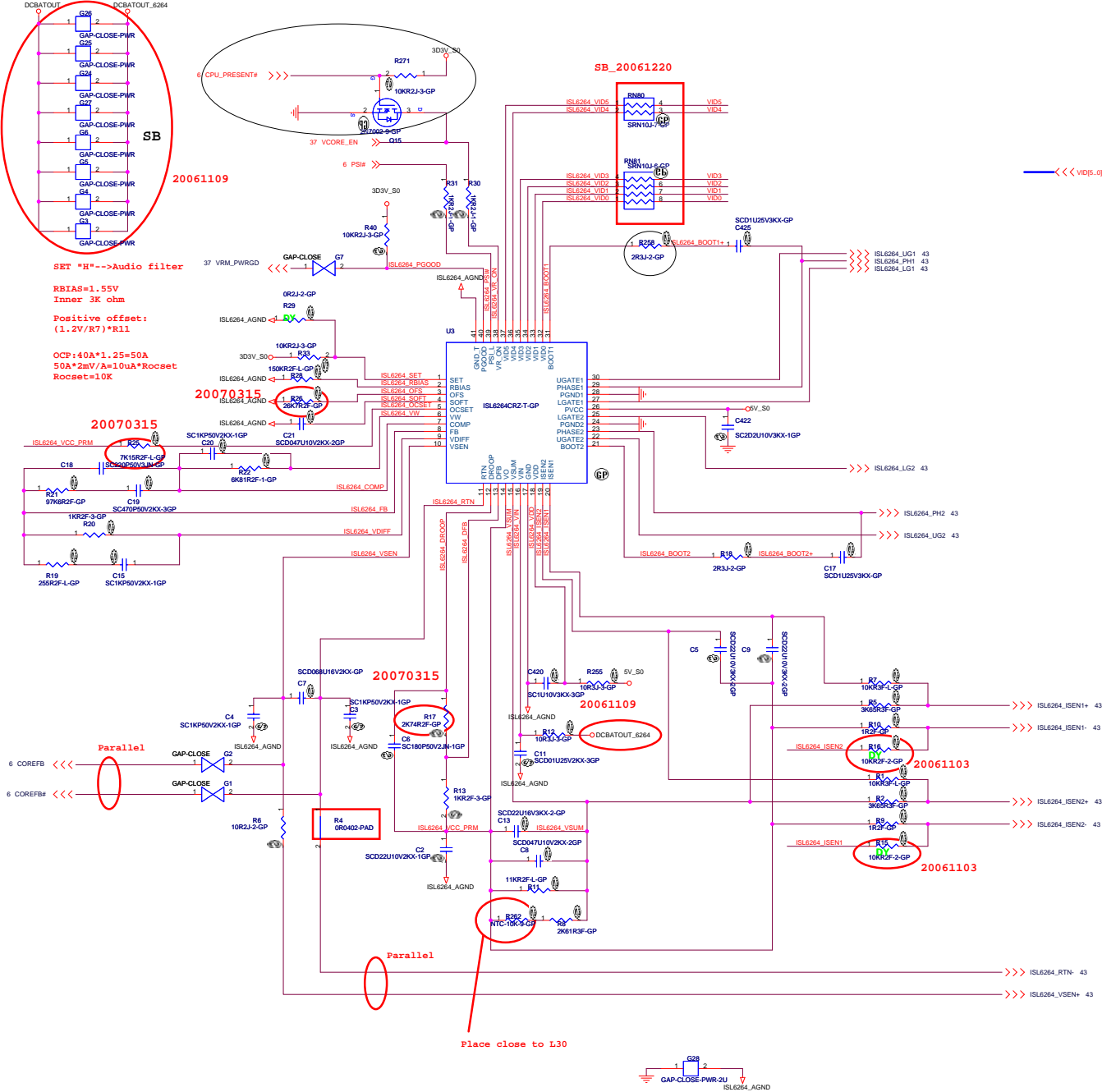
緯創資通 Wistron Corporation
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Title			
2D5V/1D5V/1D2V/0D9V			
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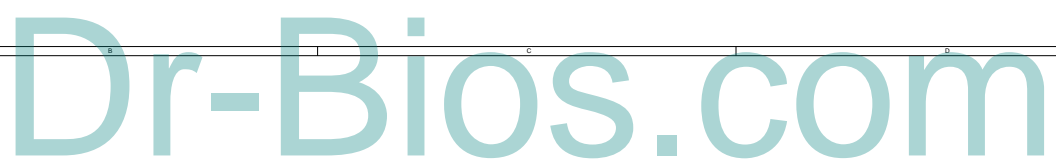
CPU_VCORE
 VID=1.20V(25W)/1.15V(35W)
 I_omax=21A(25W)/35A(35W)
 OCP=40A~45A

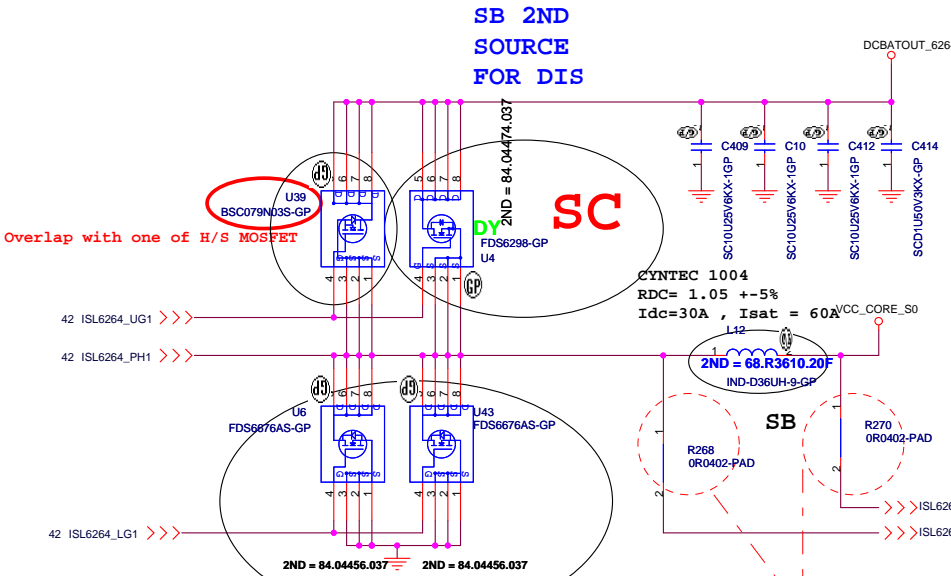
TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.500
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	1	0	0	0	1.000
0	1	1	0	0	1	0.975
0	1	1	0	1	0	0.950
0	1	1	0	1	1	0.925
0	1	1	1	0	0	0.900
0	1	1	1	0	1	0.875
0	1	1	1	1	0	0.850
0	1	1	1	1	1	0.825
1	0	0	0	0	0	0.800
1	0	0	0	0	1	0.775
1	0	0	0	1	0	0.750
1	0	0	1	0	0	0.725
1	0	0	1	0	1	0.700
1	0	1	0	0	0	0.675
1	0	1	0	0	1	0.650
1	0	1	1	0	0	0.625
1	0	1	1	0	1	0.600
1	0	1	1	1	0	0.575
1	0	1	1	1	1	0.550
1	1	0	0	0	0	0.525
1	1	0	0	0	1	0.500
1	1	0	0	1	0	0.475
1	1	0	0	1	1	0.450
1	1	0	1	0	0	0.425
1	1	0	1	0	1	0.400
1	1	0	1	1	0	0.375
1	1	0	1	1	1	0.350
1	1	1	0	0	0	0.325
1	1	1	0	0	1	0.300
1	1	1	0	1	0	0.275
1	1	1	0	1	1	0.250
1	1	1	1	0	0	0.225
1	1	1	1	0	1	0.200
1	1	1	1	1	0	0.175
1	1	1	1	1	1	0.150

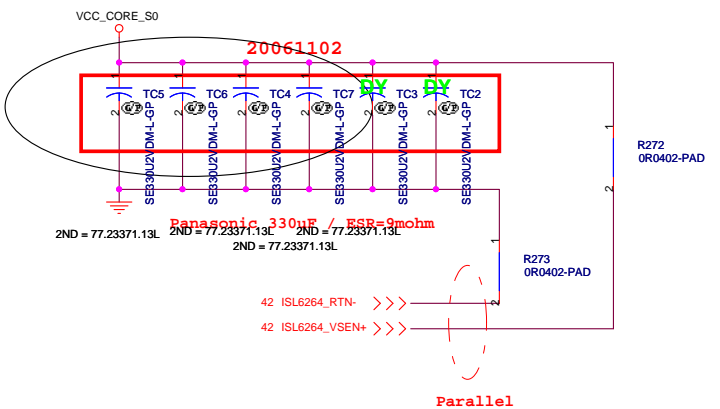
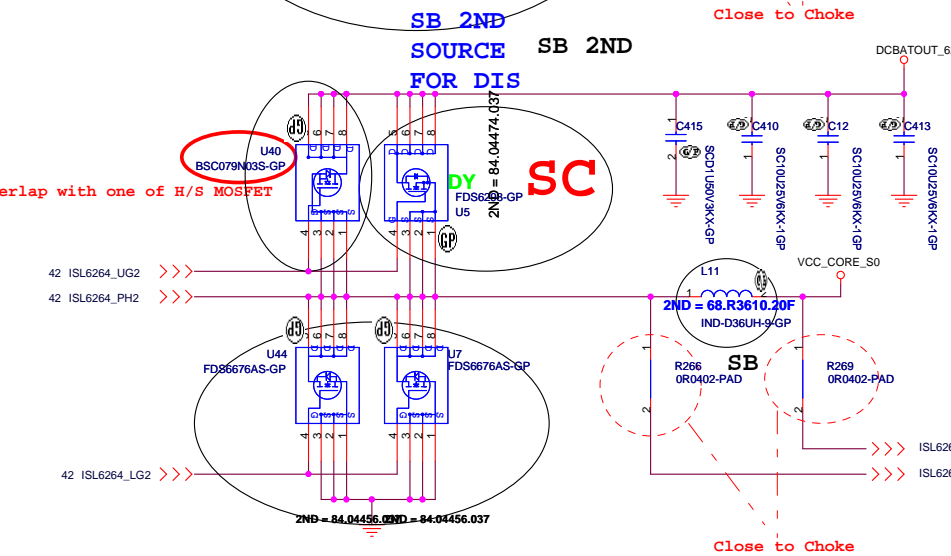


SET "H"-->Audio filter
 RBIAS=1.55V
 Inner 3K ohm
 Positive offset:
 (1.2V/R7)*R11
 OCP=40A~1.25~50A
 50A*2mV/A=10uA*Rocset
 Rocset=10K



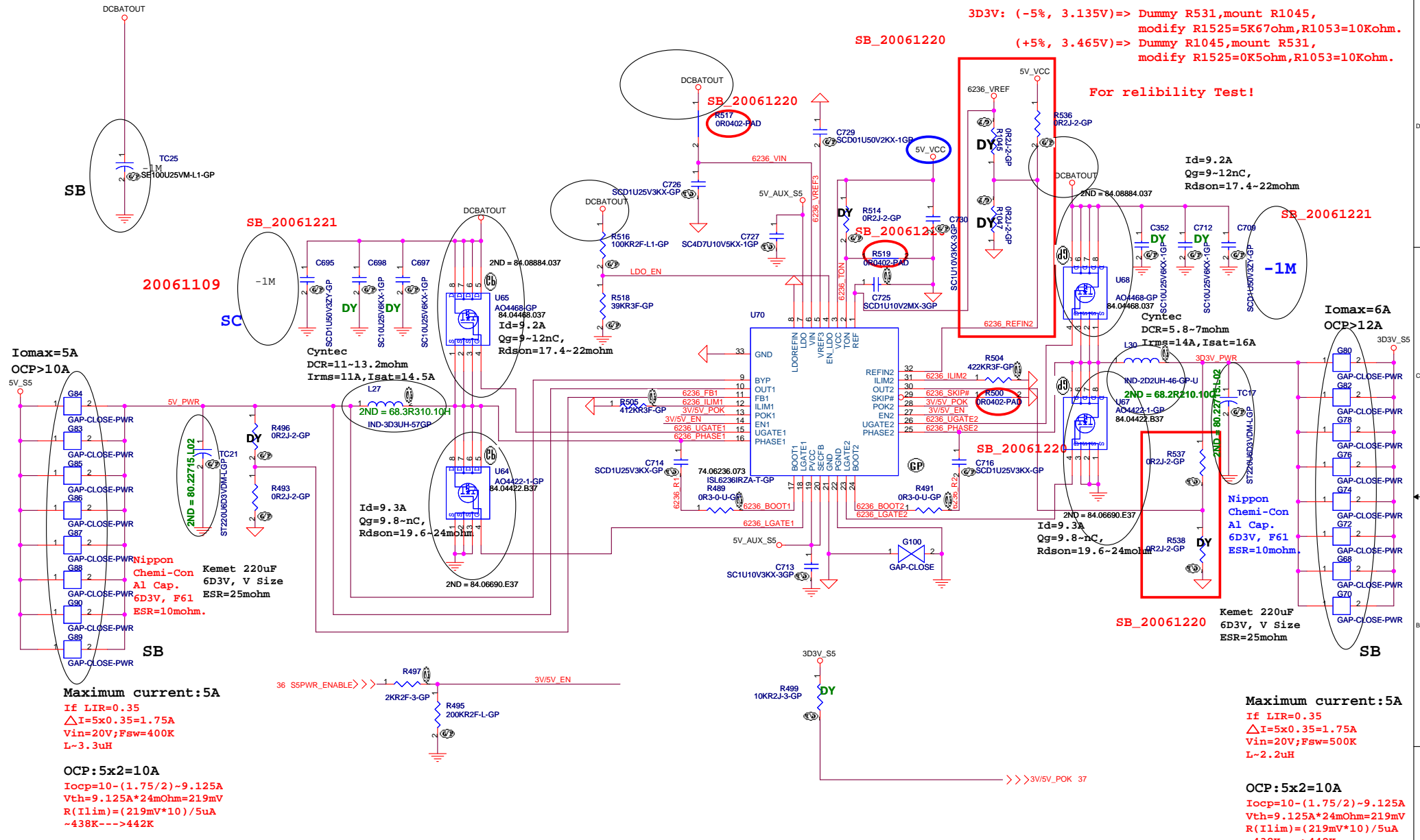


VCC_CORE_S0



UMA		緯創資通 Wistron Corporation	
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Title		CPU Vcore Power_2	
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Iomax=5A
OCP>10A

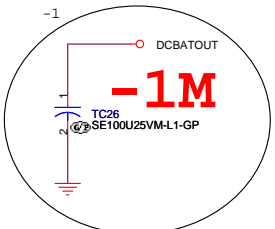
Maximum current:5A
 If LIR=0.35
 $\Delta I = 5 \times 0.35 = 1.75A$
 $V_{in} = 20V; F_{sw} = 400K$
 $L \sim 3.3\mu H$

OCP: 5x2=10A
 $I_{ocp} = 10 - (1.75/2) \sim 9.125A$
 $V_{th} = 9.125A \times 24m\Omega = 219mV$
 $R(I_{lim}) = (219mV \times 10) / 5uA$
 $\sim 438K \rightarrow 442K$

Maximum current:5A
 If LIR=0.35
 $\Delta I = 5 \times 0.35 = 1.75A$
 $V_{in} = 20V; F_{sw} = 500K$
 $L \sim 2.2\mu H$

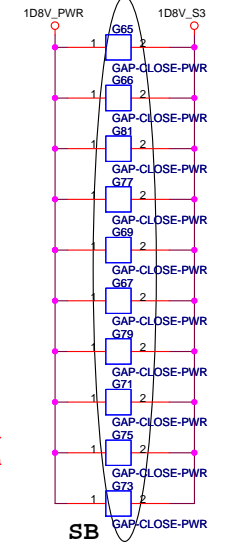
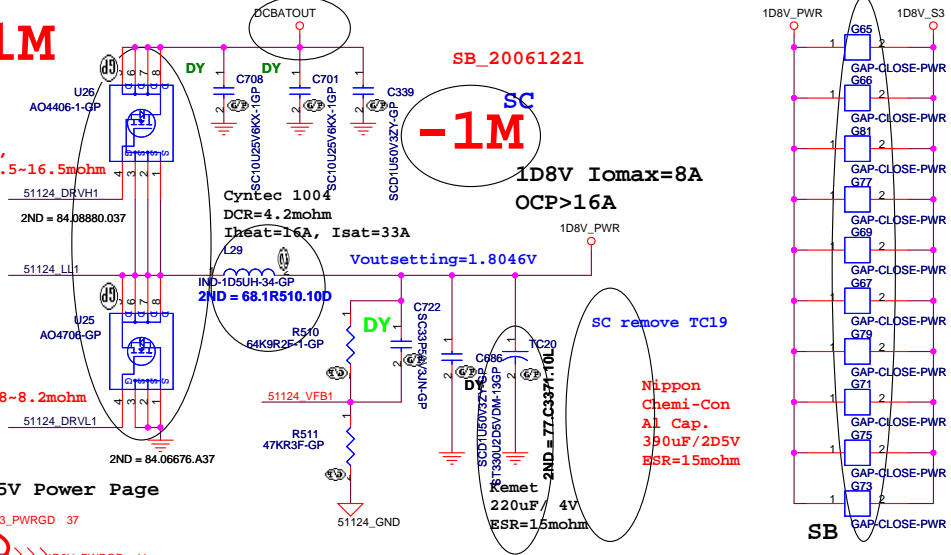
OCP: 5x2=10A
 $I_{ocp} = 10 - (1.75/2) \sim 9.125A$
 $V_{th} = 9.125A \times 24m\Omega = 219mV$
 $R(I_{lim}) = (219mV \times 10) / 5uA$
 $\sim 438K \rightarrow 442K$

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Title			
ISL6236 5V 3D3V			
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-1M

$I_d = 9.6A$
 $Q_g = 18-nC$
 $R_{dson} = 13.5-16.5m\Omega$



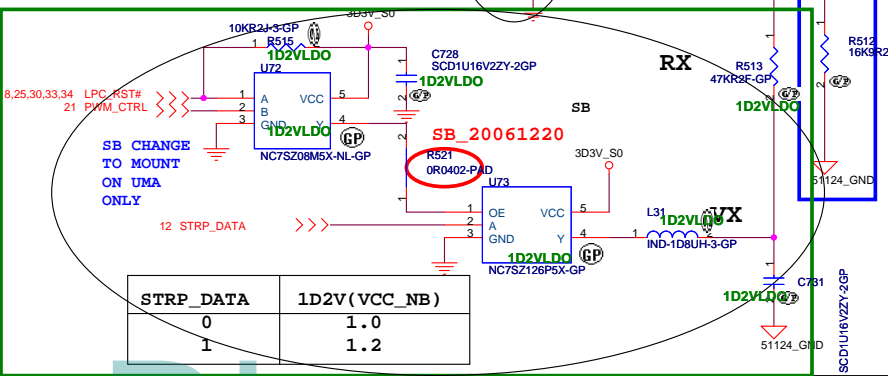
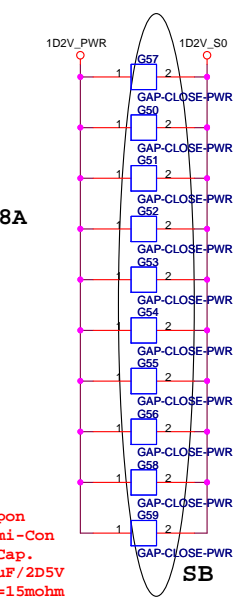
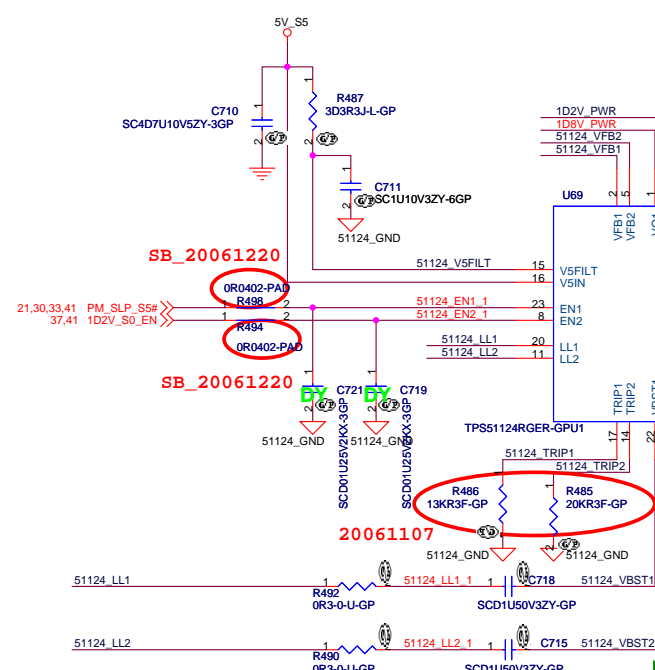
PH at 2D5V Power Page
 >>> 1D8V_S3_PWRGD 37

PH at CPU Power Page
 >>> 1D2V_PWRGD 41

SB_20061220

SC

-1M



STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

UMA

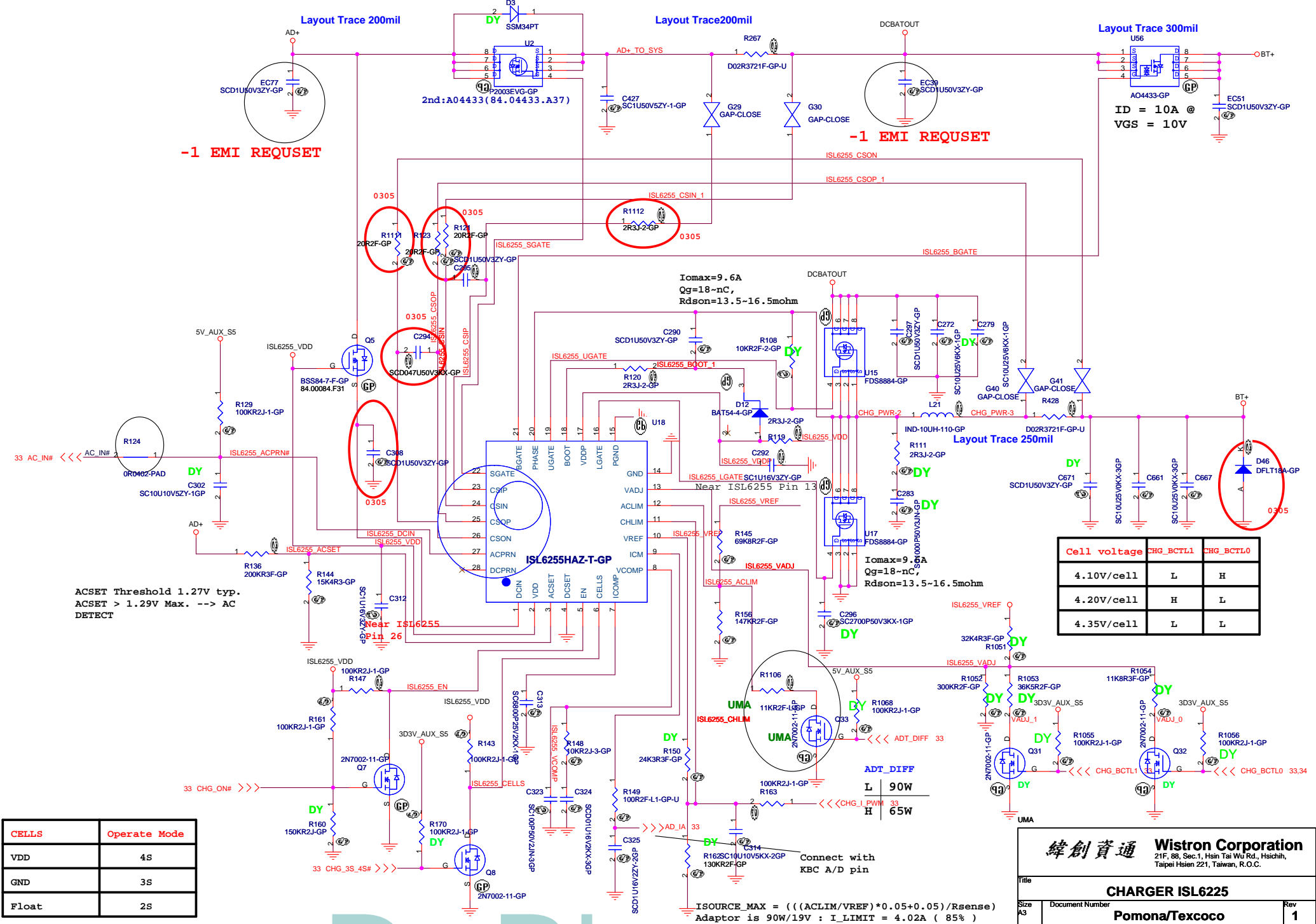
緯創資通 Wistron Corporation
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Title: **TPS51124 1D8V 1D2V**

Size A3 Document Number: **Pomona/Texcoco** Rev: **1**

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-1 EMI REQUSET

-1 EMI REQUSET

ID = 10A @
VGS = 10V

Iomax=9.6A
Qg=18-nC,
Rdson=13.5~16.5mohm

Iomax=9.6A
Qg=18-nC,
Rdson=13.5~16.5mohm

ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. --> AC
DETECT

Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

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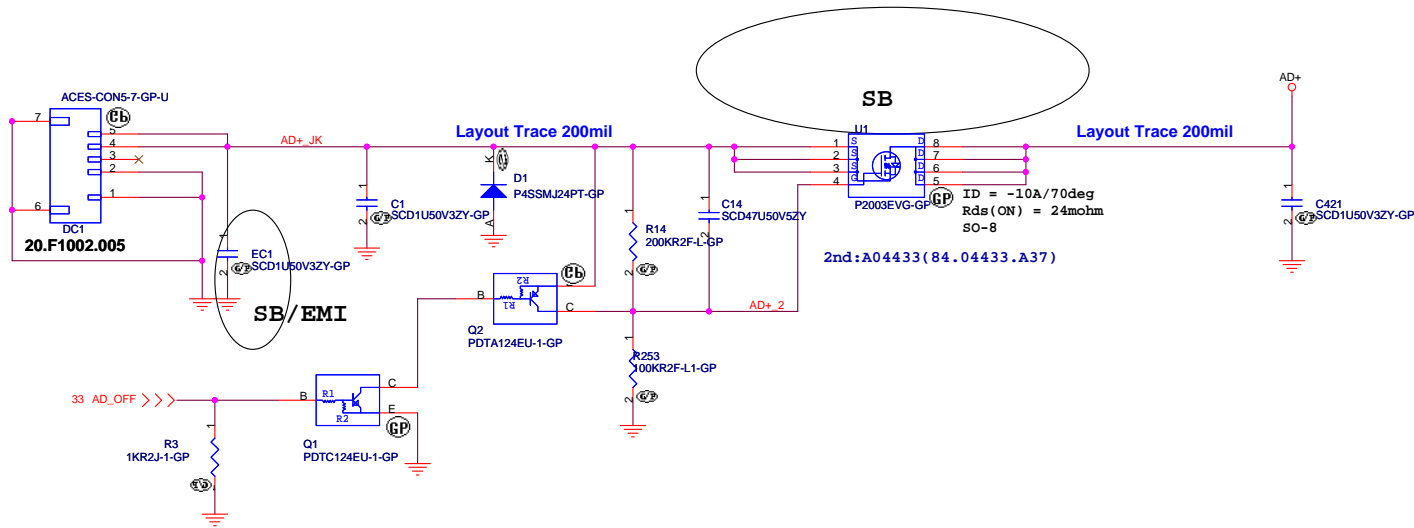
CHARGER ISL6225

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Size: A3 Document Number: _____ Rev: **1**
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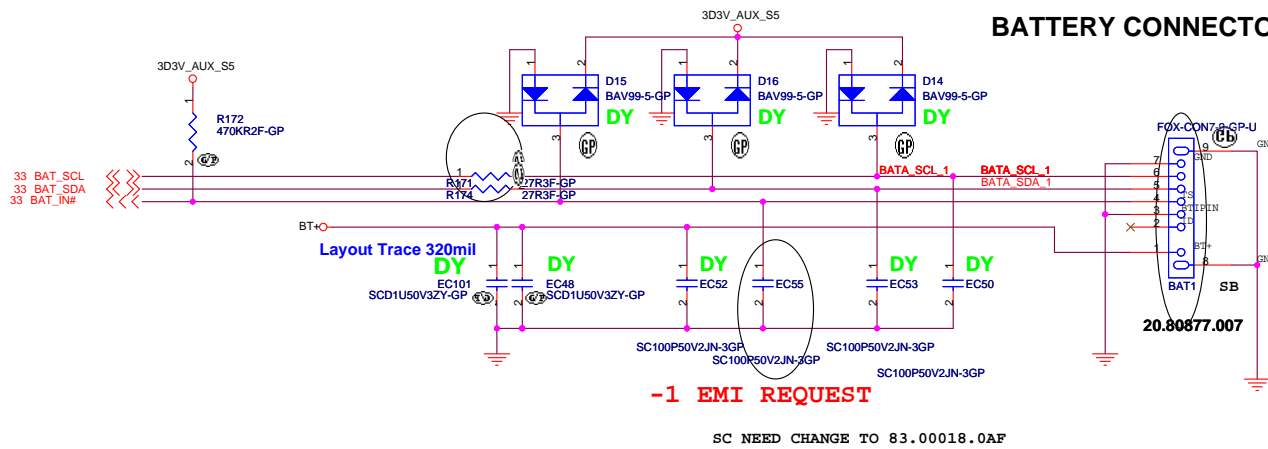
ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)

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Adaptor in to generate DCBATOUT



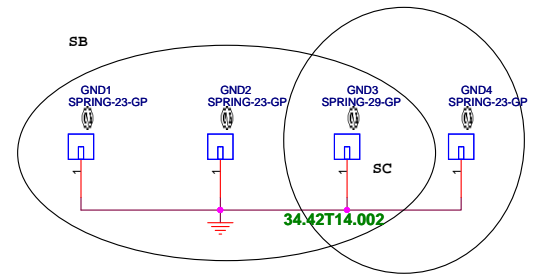
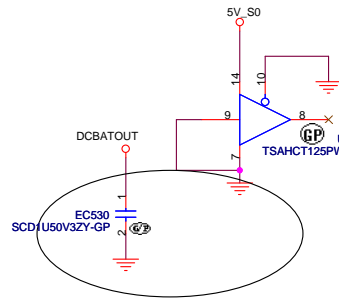
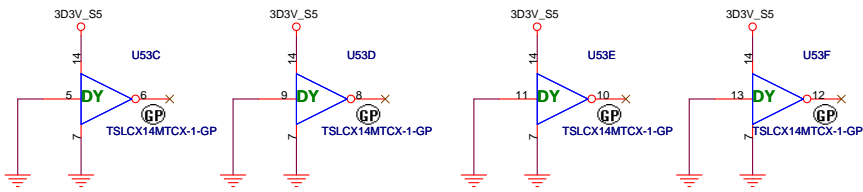
BATTERY CONNECTOR



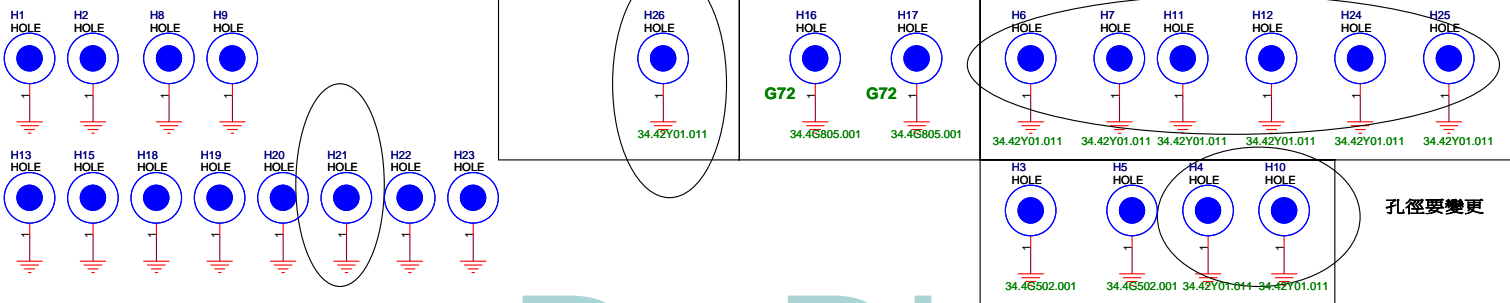
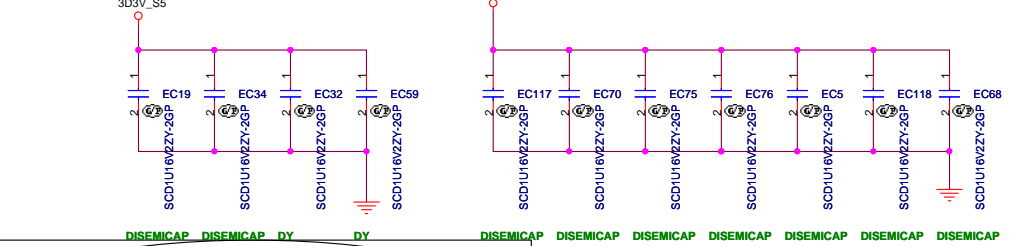
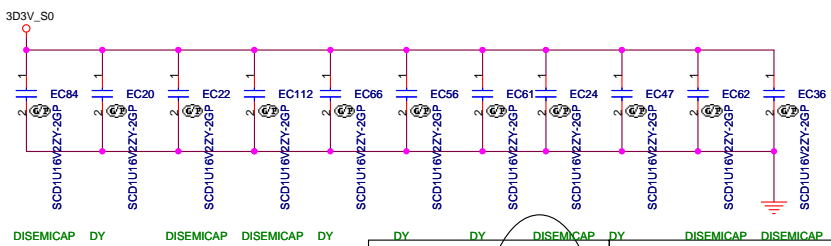
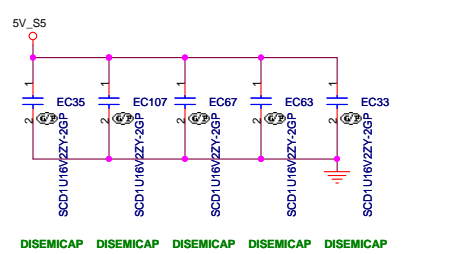
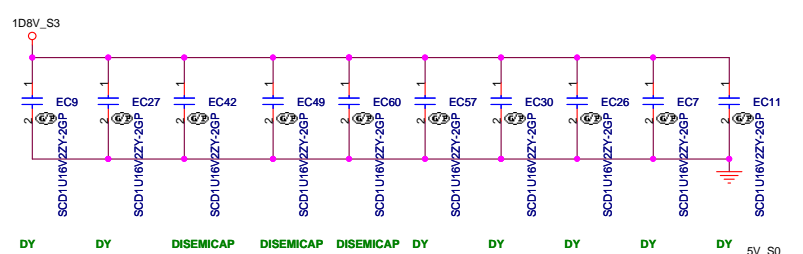
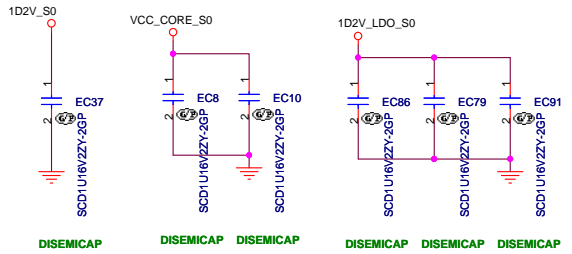
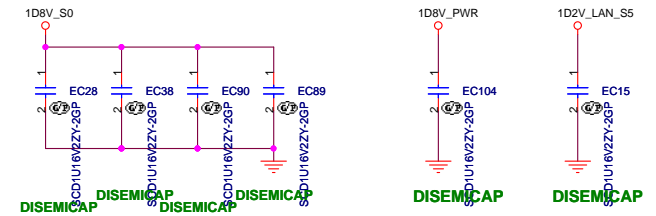
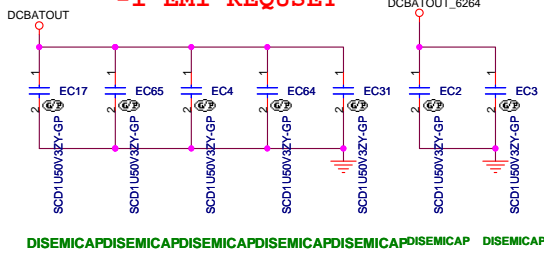
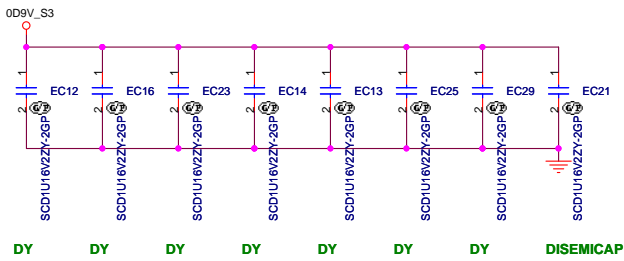
SC

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Title	
AD/BATT CONN	
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-1 EMI REQUSET



UMA

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Title: **EMI/Spring/Boss**

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PAGE3 BY RN21-24,RN34-RN36,R132,9LPR462AGLF INTERNAL P/D.
PAGE3 CHANGE X2,C307,C311 BY KDS SUGGESTION
PAGE14 ADD F2 BETWEEN DCBATOUT AND LCD CONN.
PAGE14 CHANGE LED2 TO DUAL COLOR LED FOR POWER LED AND STANDBY LED
PAGE14 CHANGE LED4 TO DUAL COLOR LED FOR CHARGER LED AND DC_BATFULL_LED
PAGE15 CHANGE C477,480,487 TO 15P FROM DY FOR SOLVE SIV ISSUE,DIS ONLY
PAGE15 CHANGE C477,480,487 TO 15P FROM DY FOR SOLVE SIV ISSUE,DIS ONLY
PAGE15 CHANGE C479,483,490 TO 15P FROM 6.8P FOR SOLVE SIV ISSUE.DIS ONLY;UMA WILL KEEP 6.8P
PAGE18 CHANGE X1,C259,C270 BY KDS SUGGESTION
PAGE19 CHANGE X5,C655,C656 BY KDS SUGGESTION
PAGE19 P/W CLR# P/U LK TO 3D3V_S5
PAGE21 CHANGE R101 TO DY FOR EC5WI#_KBC AND CHANGE TO R531 THAT CONNECT TO USB_OC6#(GEVENT6#)
PAGE23 CHANGE SATA1 CONN.
PAGE23 CHANGE ODD1 CONN.
PAGE24 CHANGE R27 TO 10R FOR SOLVE ACZ_SDATAIN1 OF SIV FAIL ITEM
PAGE25 CHANGE X4,C471,C472 BY KDS SUGGESTION
PAGE26 CHANGE RJ1 CONN.AND LAN_ACT_LED# TO B2 FROM A1,10M/100M/1G_LED# FROM B2 TO A3
PAGE26 CHANGE LAN_ACT_LED# TO B2 FROM A1
PAGE26 CHANGE 10M/100M/1G_LED# FROM B2 TO A3
PAGE28 CHANGE C691,C689 TO 6.8P BY KDS SUGGESTION
PAGE30 CHANGE NEW1 CONN.
PAGE30 CHANGE MINIC1 CONN.
PAGE30 ADD R537 AND SET TO DY
PAGE31 CHANGE R215 TO 27R FOR SOLVE ACZ_SDATAIN0 OF SIV FAIL ITEM
PAGE31 ADD R538 OR AND SET INTERNAL MIC TO LEFT CHANNEL,DY R224,D17 AND ADD D36
PAGE31 SET C391 TO DY FOR POP SOUND
PAGE31 CHANGE R247 TO 10K;R236 TO 6.8K;R248 TO DY;249 TO STUFF FOR SET GAIN TO 1.2W
PAGE31 CHANGE R238,239,242,243 TO 0R
PAGE31 CHANGE R223 TO STUFF
PAGE31 CHANGE INTMIC1 CONN.
PAGE31 CHANGE SPKR1 CONN.
PAGE33 ADD D35 BETWEEN KBC AND PM_PWRBTN#
PAGE33 DY R197 AND STUFF R193 FOR SET PCB VER. TO 001
PAGE33 CHANGE X3,C337,C341 BY KDS SUGGESTION
PAGE34 Add serial resistor 150 Ohm and Bypass Cap 4.7P on SPI_CLK(Close to KBC)
Add serial resistor 150 Ohm on SPI_DO(Close to KBC)
Add serial resistor 150 Ohm on SPI_DI(Close to SPI Flash)
PAGE33 CHANGE WLAN1,BLUE2 CONN.
PAGE37 SET R453 TO DY
PAGE38 ADD C750

-1

- 1.Change U19 ATIGLCK3 to SRCCLK3.PAGE3
- 2.Change U19 ATIGLCK2 to SRCCLK1.PAGE3
- 3.Add CLK14_SIO of U19;PIN62 FOR Super I/O.PAGE3
- 4.Change THERMTRIP# TO KBC GPI94.PAGE6
- 5.Change LDT_RST#;LDT_STP#;SB_CUPWRGD P/L resistor to 680 ohms by AMD reccommand.PAGE6
- 6.Adjust current limit resistor for FRONT_PWRLED.R1113 change to 68 ohms.PAGE14
- 7.Adjust current limit resistor for BT_LED.R251 change to 390 ohms.PAGE14
- 8.Adjust current limit resistor for DC_BATFULL_LED.R1116 change to 68 ohms.PAGE14
- 9.Add R1093 P/H 10K ohms TO 3D3V_S0 for solve WLAN_LED light leak in dos mode.PAGE14
- 10.Remove damping resistor of TMDS signal.PAGE16
- 11.Remove bridge resistor of TMDS signal.PAGE17
- 12.Change FP_DETECT TO KBC GPIO27.PAGE19
- 13.Change USB7 from PORT7 to PORT1 of U19.PAGE21
- 14.Change PCB_VER0/1 form KBC to GPIO4/5 of U19.PAGE21
- 15.Add ESD diode D38-D45 for USB signal.PAGE23
- 16.Add damping resistor 22 ohms and P/L CAP 22P for SD_CLK for EMI.PAGE27
- 17.Add P/L CAP 33P for SD/MMC_D0-D3 for EMI.PAGE29
- 18.Dummy R1062,R1058 and mount R1061 for MINICARD.PAGE30
- 19.Remove MIC array design.PAGE31
- 20.Add ESD diode EC523-526 for internal speaker.PAGE32
- 21.Add AD_DIFF on GPIO10 for separate 65W/90W adapter.PAGE33
- 22.Change KBC_MATRIX0# P/H to 3D3V_AUX_S5.PAGE33
- 23.Add SUPER IO circuit U76 for FIR function.PAGE33
- 24.BLON_OUT and BRIGHTNESS P/L cap close to KBC.PAGE33
- 25.Add R1089 to set BLON timing.PAGE33
- 26.Add U77 T8 shutdown circuit FOR U19(SB600).PAGE36
- 28.Change KBC_THERMTRIP# to KBC GPI94.PAGE36
- 29.Change value of R25.R26 and mount R17 to modify SUSTAND LOAD LINE to meet AMD spec.PAGE42
- 30.Add AD_DIFF for separate 65W/90W adapter.PAGE46
- 31.Add D46 and modify resistor value of R1111,R1112,R121,C294,C308 by vendor reccommand.PAGE46

UMA

Title		
<Title>		
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