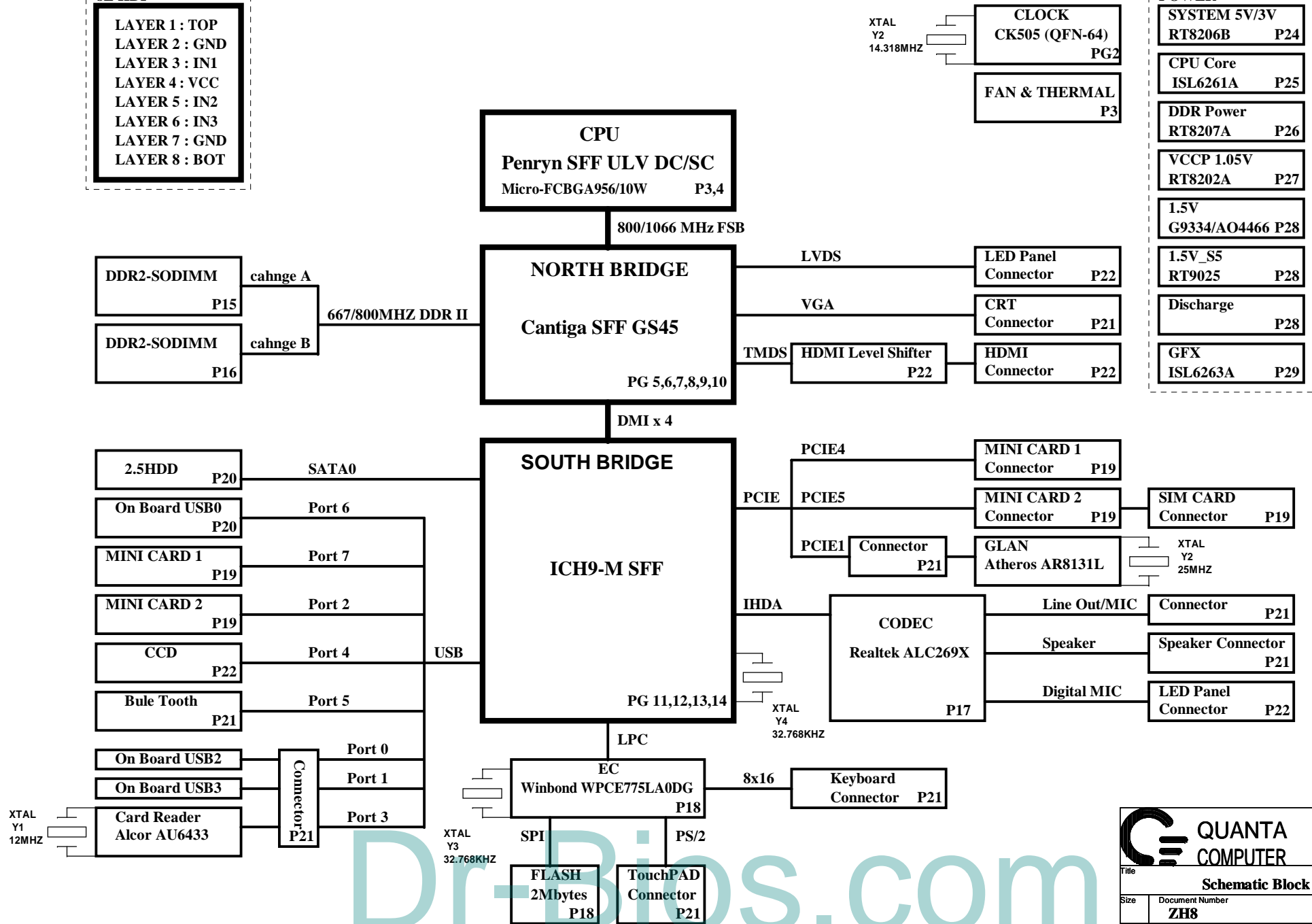


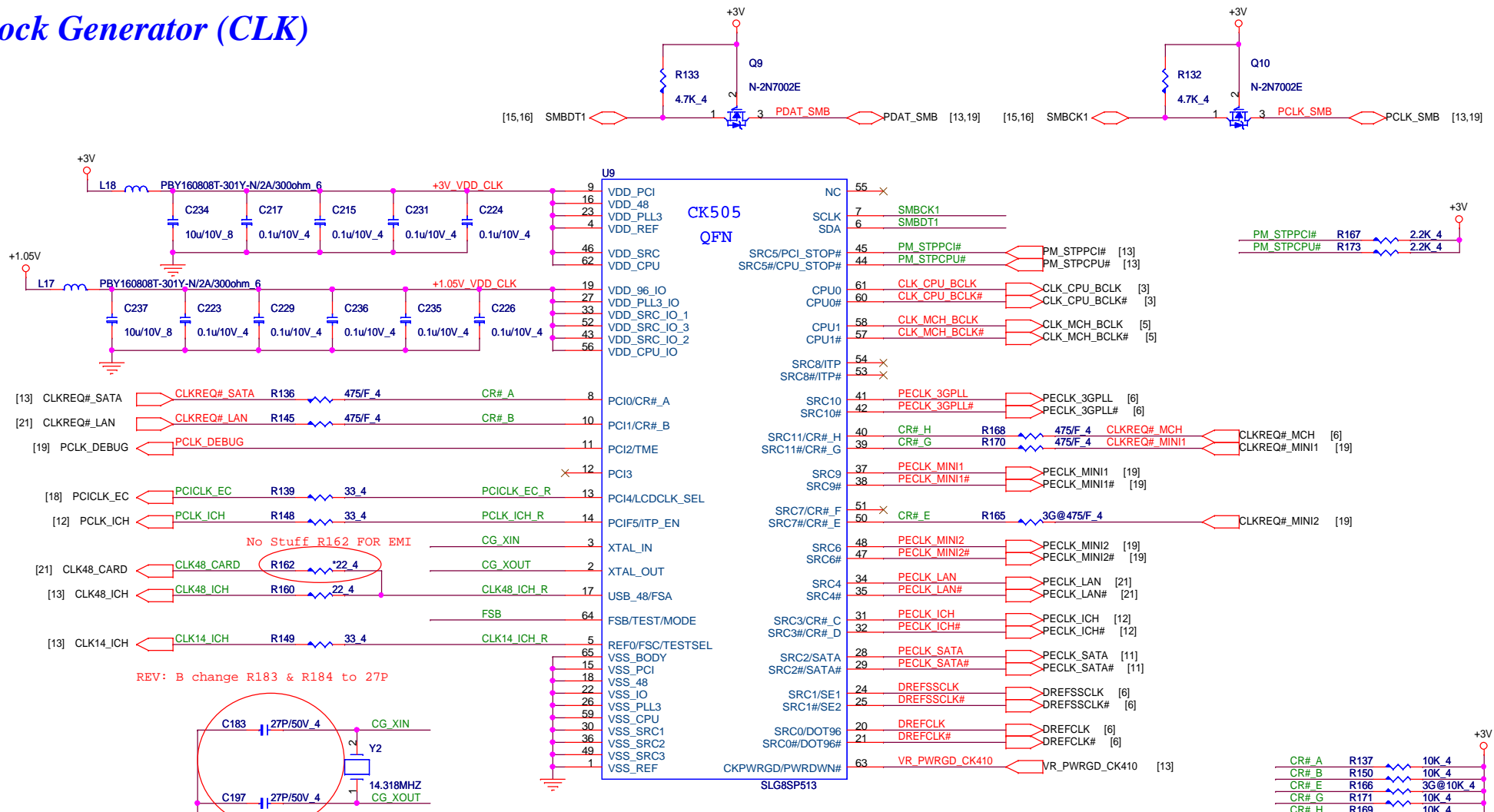
SJM11_MS (ZH8) BLOCK DIAGRAM

PCB STACK UP 8L HDI

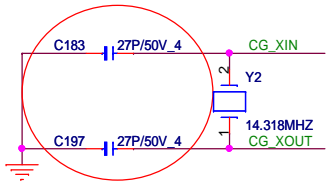
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT



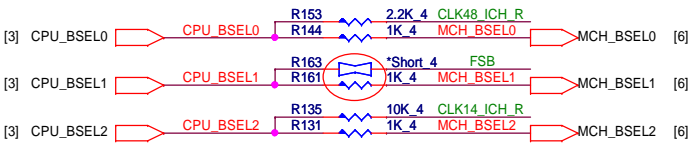
Clock Generator (CLK)



REV: B change R183 & R184 to 27P



REV: B Change R161 to short pad

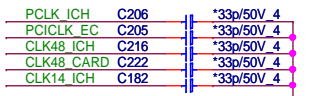


FSC	FSB	FSA	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1						


Reserved

ITP EN	Pin 53/54
0	SRC 8/SRC 8#
1	ITP/ITP#

LCDCLK SEL	Pin 20/21	Pin 24/25
0	DOT 96/DOT96#	LCDCLK/LCDCLK#
1	SRC 0/SRC 0#	27M/27M SS



CLKREQ#	MAPPING		Control
	0	1	
CR# A	SRC0	SRC2	SATA
CR# B	LCDCLK	SRC4	LAN
CR# C	SRC0	SRC2	N/A
CR# D	LCDCLK	SRC4	N/A
CR# E	SRC6		MINI2
CR# F	SRC8		N/A
CR# G	SRC9		MINI1
CR# H	SRC10		MCH



QUANTA COMPUTER

Title: **CLOCK GENERATOR CK505**

Size: Document Number **ZH8** Rev **0C**

Date: Saturday, June 27, 2009 Sheet 2 of 31

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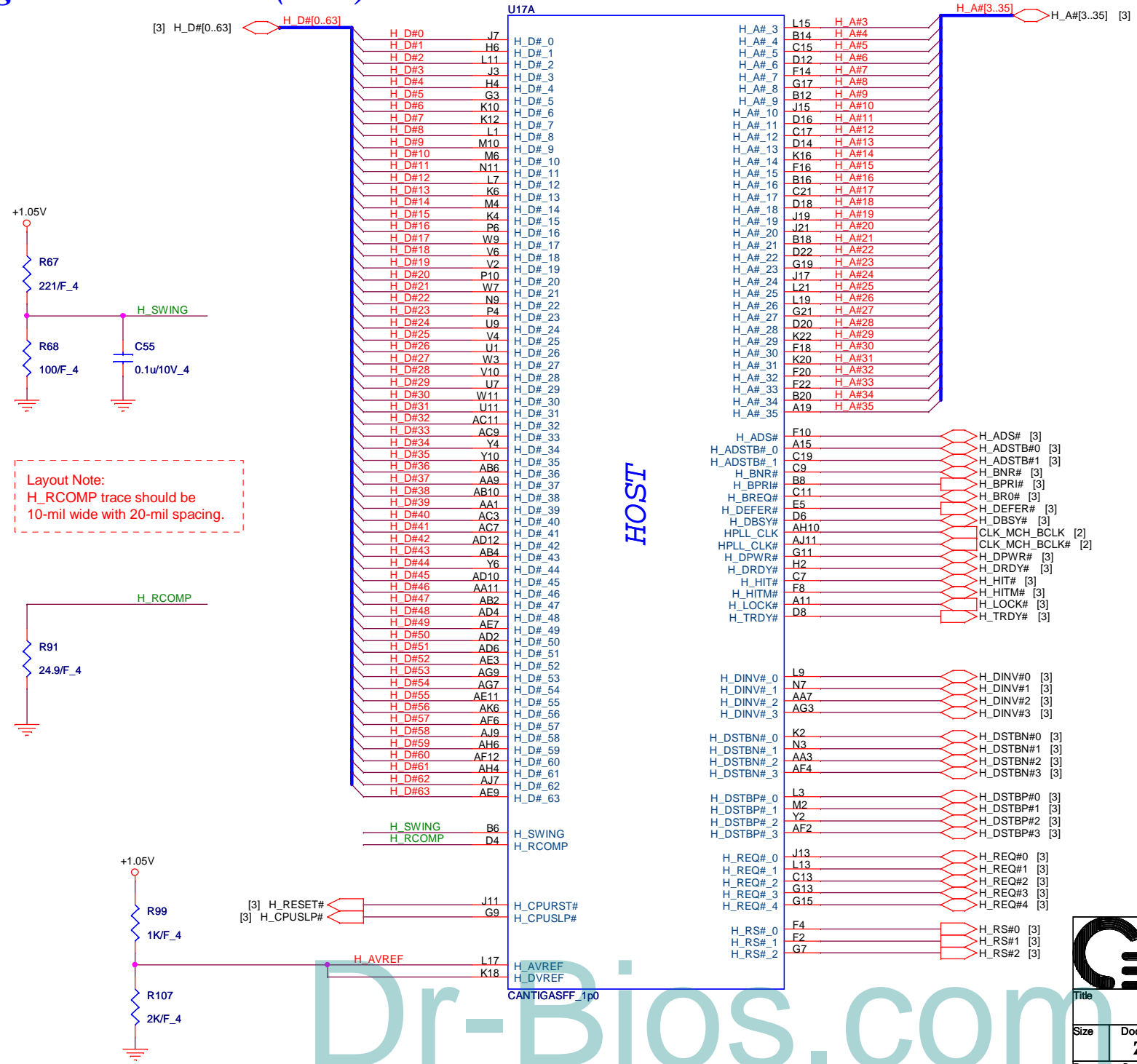
Penryn SFF - Power (CPU)



DrBios.com



Cantiga SFF - Host Bus (CLG)



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QUANTA COMPUTER

Title: **Cantiga SFF (Host Bus)**

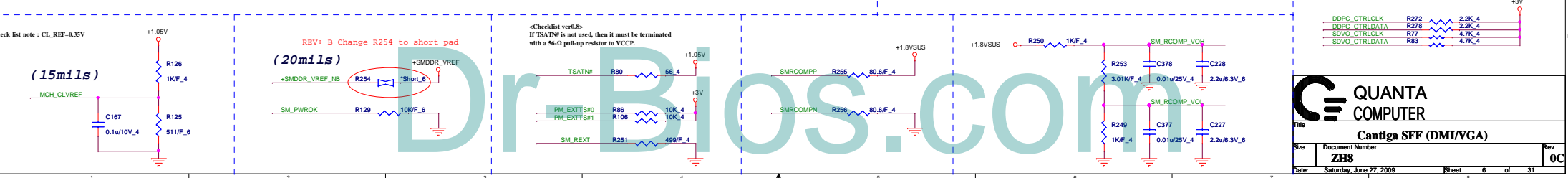
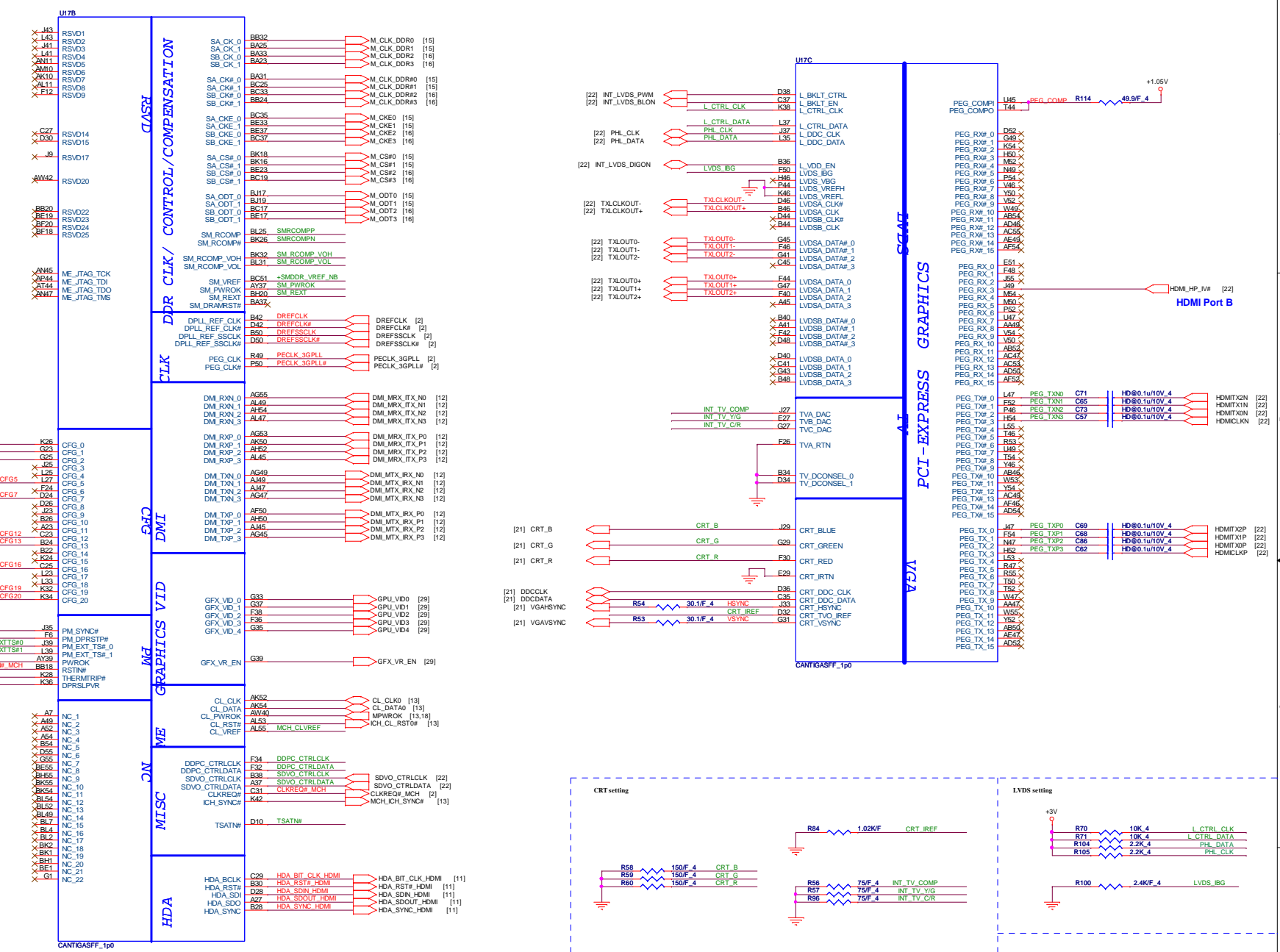
Size: **ZH8** Document Number: **0C**

Date: **Saturday, June 27, 2009** Sheet: **5** of **31**

Cantiga SFF - DMI/VGA (CLG)

Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Other = Reserved
CFG4:3	Reserved	
CFG5	DMI x2 Select	0 = DMI x4 1 = DMI x2
CFG6	ITPM Host Interface	0 = ITPM disabled
CFG7	Intel Management Engine Crypto Strap	0 = Intel Management Engine Crypto Strap cipher suite with confidentiality 1 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
CFG8	Reserved	
CFG9	PCIe Graphics Lane	0 = Normal operation : Lane Numbered in Order
CFG10	PCIe Loopback enable	0 = Disabled 1 = Enabled
CFG11	Reserved	
CFG12	ALLZ	0 = Disabled 1 = ALLZ mode enabled
CFG13	XOR	0 = Disabled 1 = XOR mask enabled
CFG14	Reserved	
CFG15	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT enabled 1 = Dynamic ODT disabled
CFG17	Reserved	
CFG18	Reserved	
CFG19	DMI Lane Reversal	0 = Reverse Lanes 1 = Normal operation : Lane Numbered in Order
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIe	0 = Digital DisplayPort (SDVO/DP/HDMI) and PCIe are operating simultaneously via the PEG port. 1 = Digital DisplayPort (SDVO/DP/HDMI) or PCIe are operational. 2 = No SDVO/DP/HDMI/DP interface enabled.
SDVO_CTRLDATA	SDVO Present	0 = SDVO/DP/HDMI/DP interface enabled 1 = No SDVO/DP/HDMI/DP interface enabled
L_DDC_DATA	Local Flat Panel LFP Present	0 = LFP Card Present: PCIe disabled 1 = LFP Card Present: PCIe enabled
DDPC_CTRLDATA	Digital Display Present	0 = Digital display (HDMI/DP) is/are present 1 = Digital display (HDMI/DP) interface absent

* The recommended pull-up resistor value is 4.02 kΩ ±1%.
* The recommended pull-down resistor value is 2.21 kΩ ±1%.



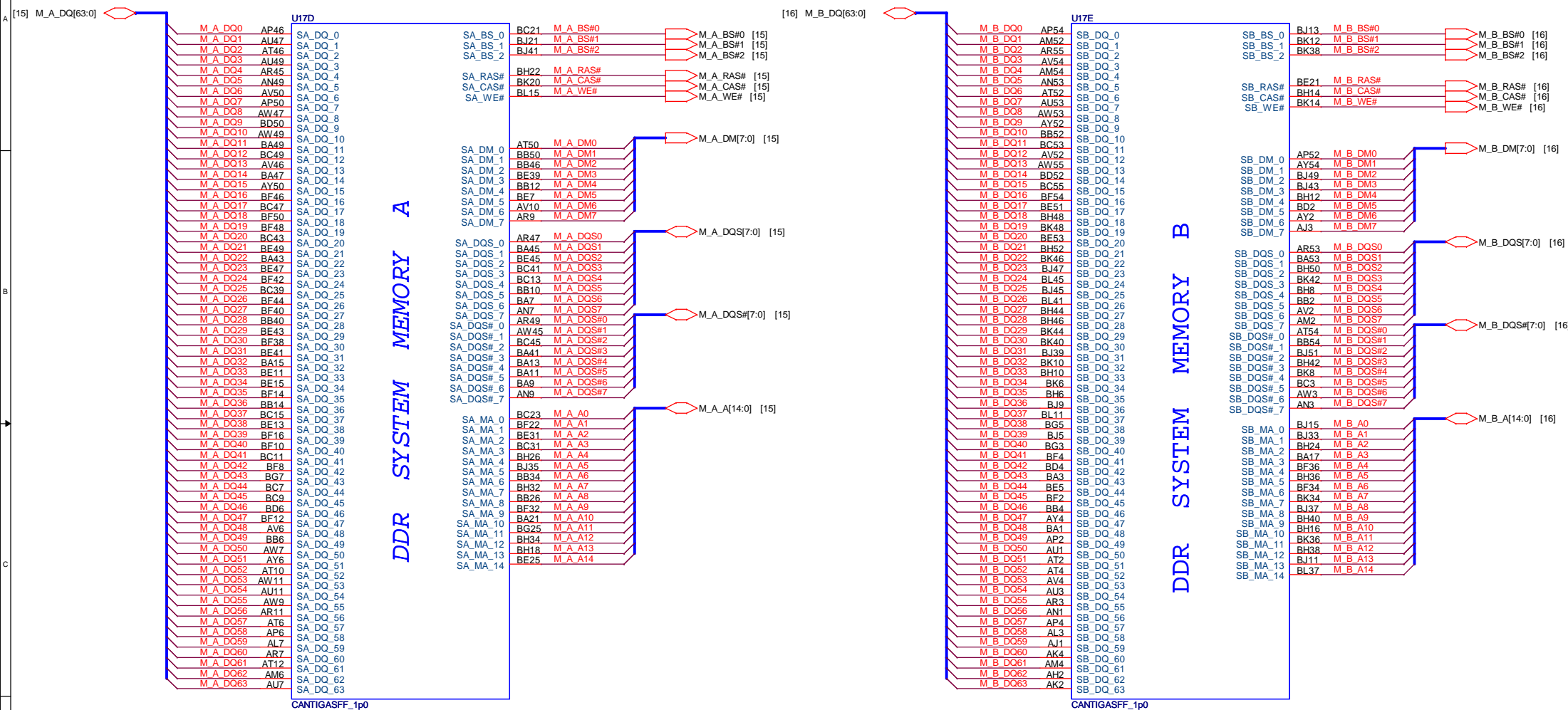
QUANTA COMPUTER

Document Number: **Cantiga SFF (DMI/VGA)**

Rev: **0C**

Date: Saturday, June 27, 2009 Sheet: 6 of 31

Cantiga SFF - DDRII (CLG)



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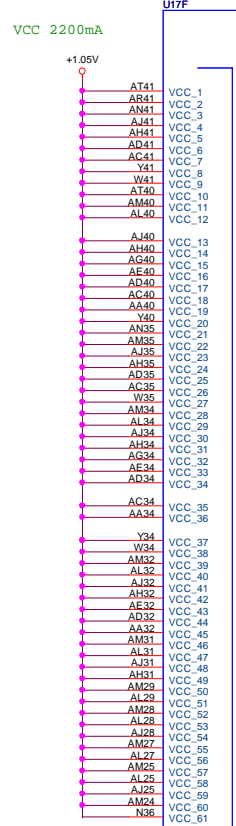
Title: Cantiga SFF (DDRII)

Size: ZH8 Document Number: Rev: 0C

Date: Saturday, June 27, 2009 Sheet: 7 of 31

Cantiga SFF - VCC/NCTF (CLG)

Vcc internal VGA 2.4A
(Shape or 140mils)

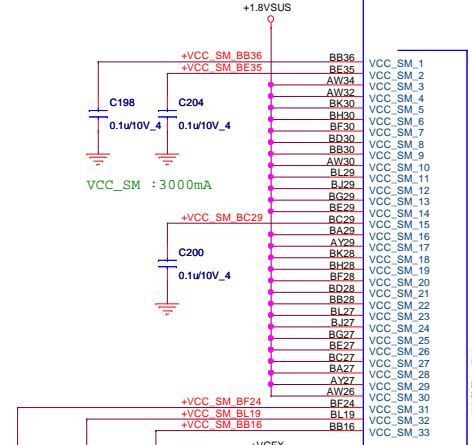


VCC CORE

POWER

VCC NCTF

DDR2-667 2.6A
DDR2-800 3A
(Shape or 140mils)



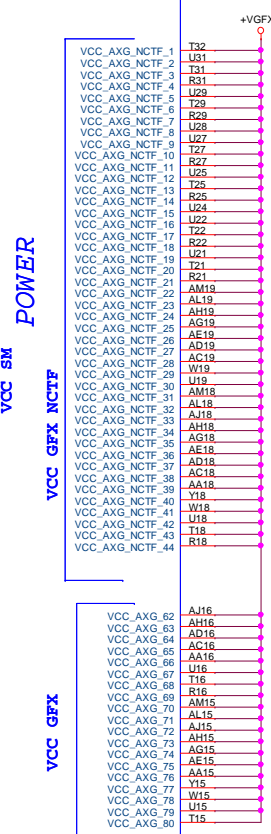
+VCC SM BB36
+VCC SM BE36

+VCC SM BC29

+VCC SM BF24
+VCC SM BL19
+VCC SM BB16

VCC_AXG 7700mA

UMA 9.6A(GM45)
(Plane or shape)

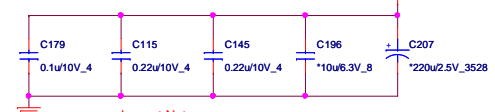


VCC SM

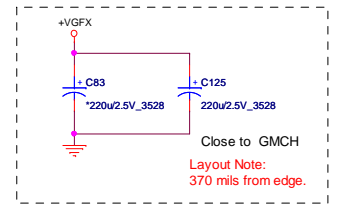
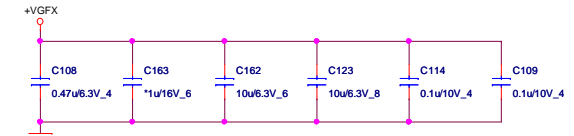
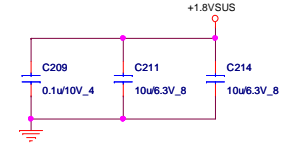
VCC GFX NCTF

VCC GFX

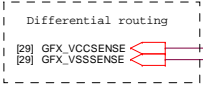
VCC SM I/F



Layout Note:
Inside GMCH cavity.



Close to GMCH
Layout Note:
370 mils from edge.



1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

QUANTA COMPUTER

Title: **Cantiga SFF (VCC/NCTF)**

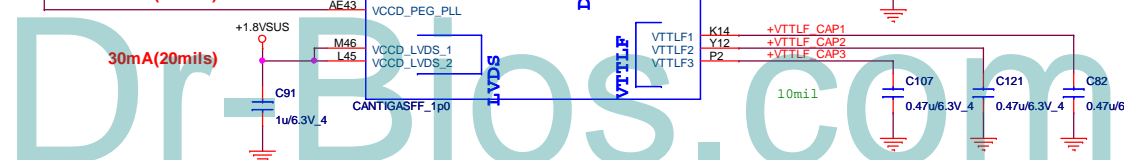
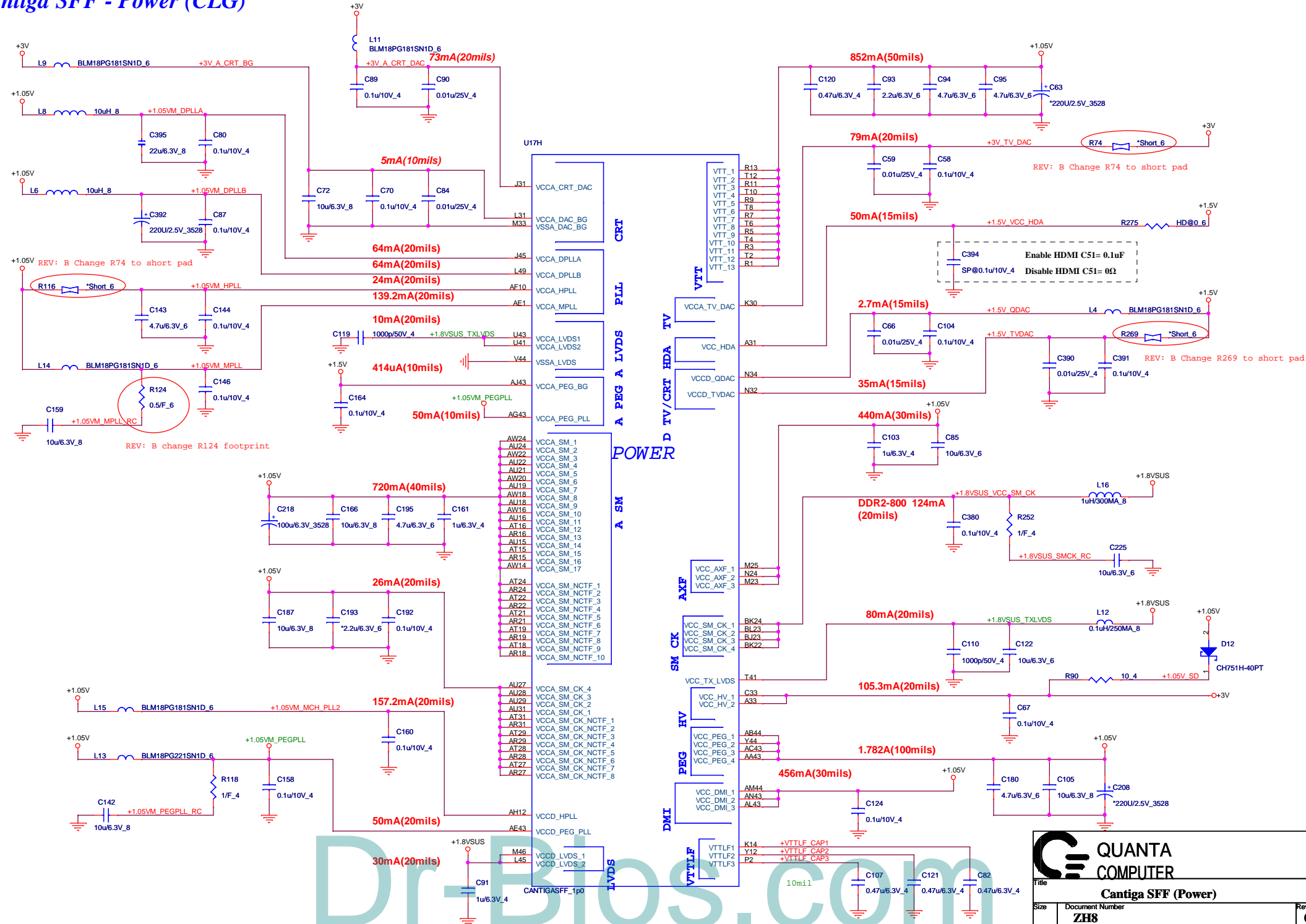
Size: **ZH8**

Date: Saturday, June 27, 2008

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Rev: **0C**

Cantiga SFF - Power (CLG)



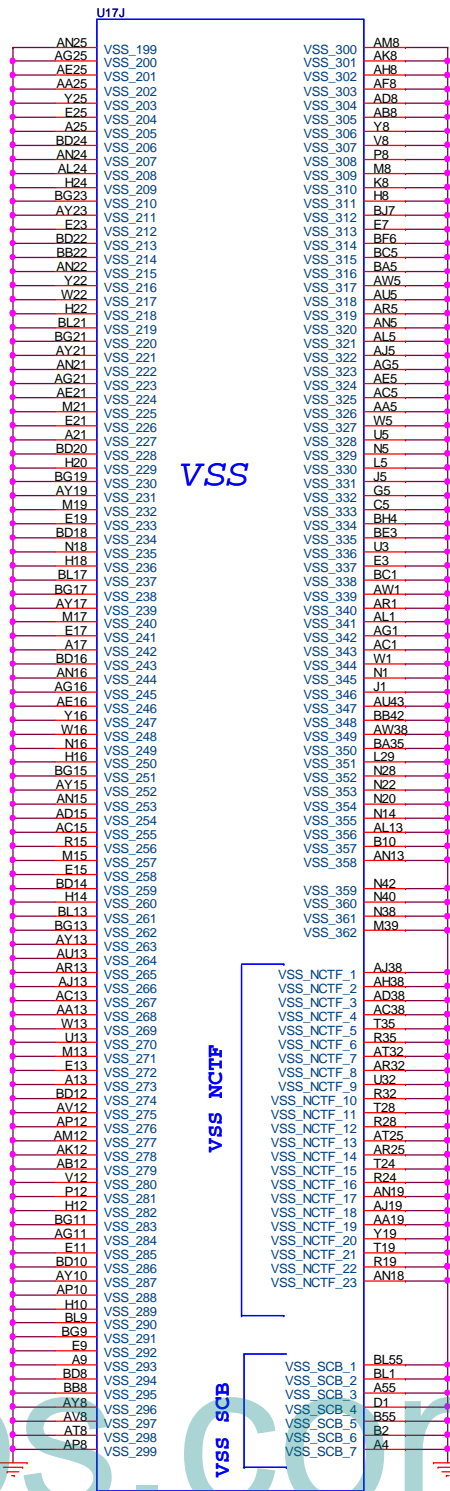
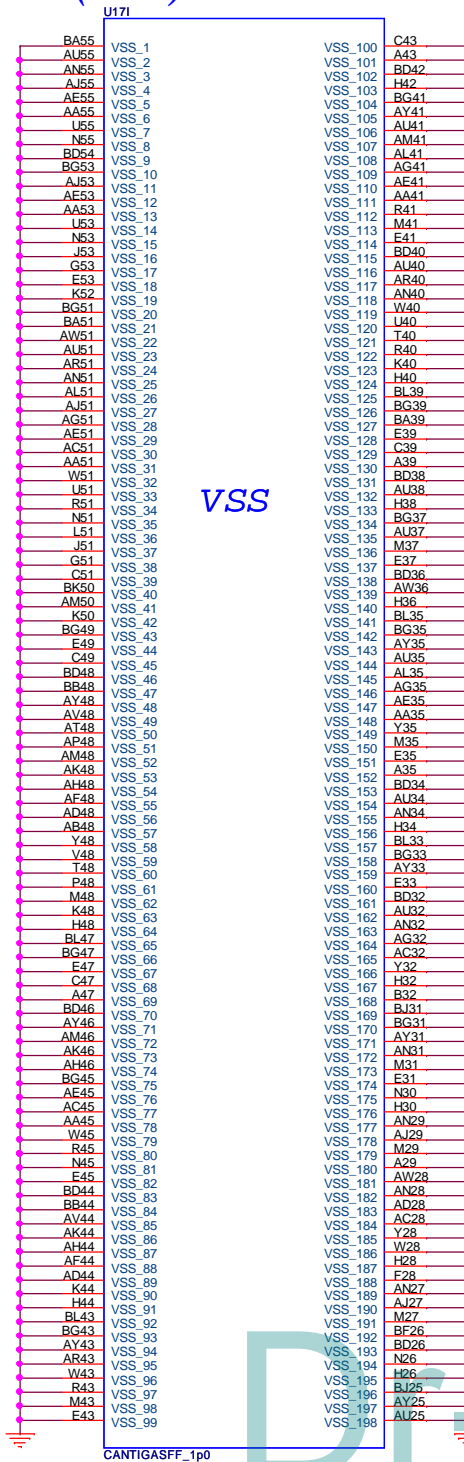
QUANTA COMPUTER


File: **Cantiga SFF (Power)**

Size	Document Number	Rev
	ZH8	0C

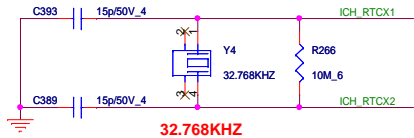
Date: Saturday, June 27, 2009 Sheet 9 of 31

Cantiga SFF - GND (CLG)



 QUANTA COMPUTER	
Title: Cantiga SFF (GND)	
Size:	Document Number: ZH8
Date: Saturday, June 27, 2009	Sheet: 10 of 31
Rev: 0C	

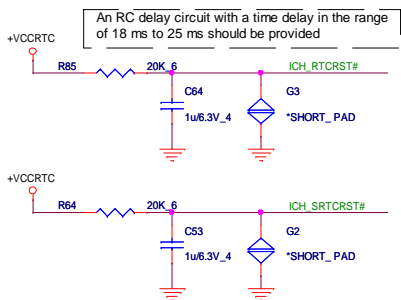
RTC CRYSTAL



(Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
--------------	---

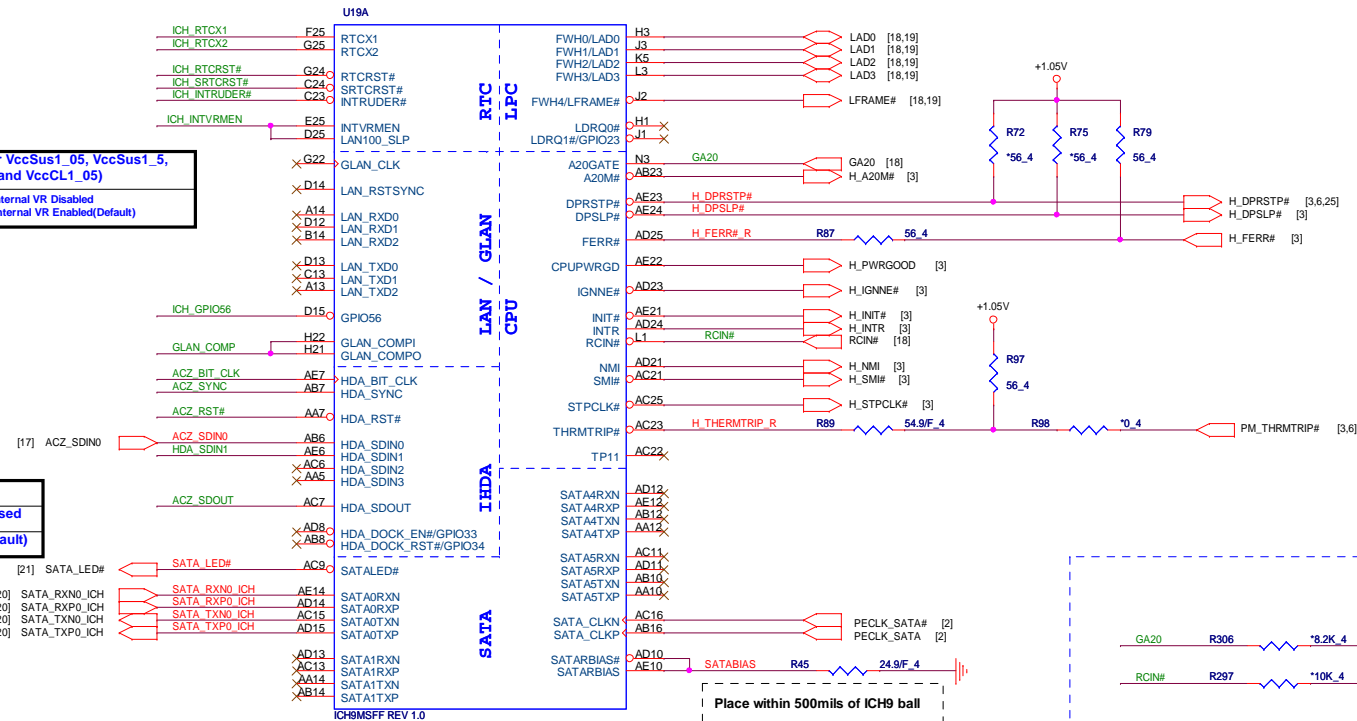
RESET JUMP



ICH_SATA_LED#

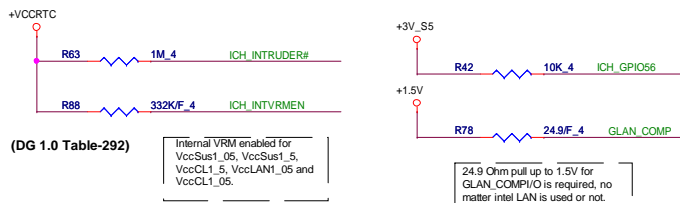
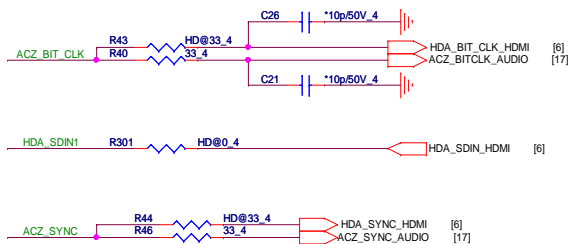
0	PCIe Lane Reversed
1	PCIe Straight(default)

ICH9M SFF - Host,SATA,HDA (CLG)

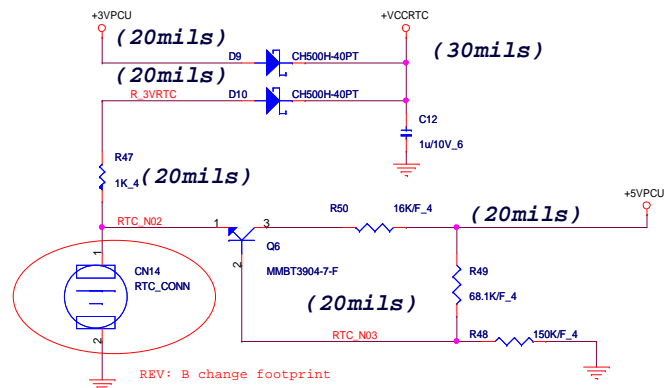


Place within 500mils of ICH9 ball

HD Audio Interface



RTC BATTERY (RTC)



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD	
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.	
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU		
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	ICH_TP3	HDA_SDOUT	Description
			0	0	RSVD
			0	1	Enter XOR Chain
			1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1			

QUANTA
COMPUTER

Item: ICH9M SFF (Host/SATA/HDA)

Size: Document Number: ZH8

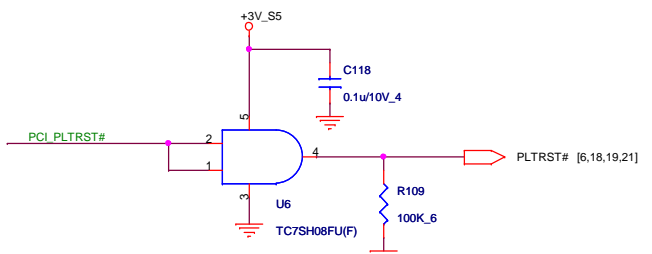
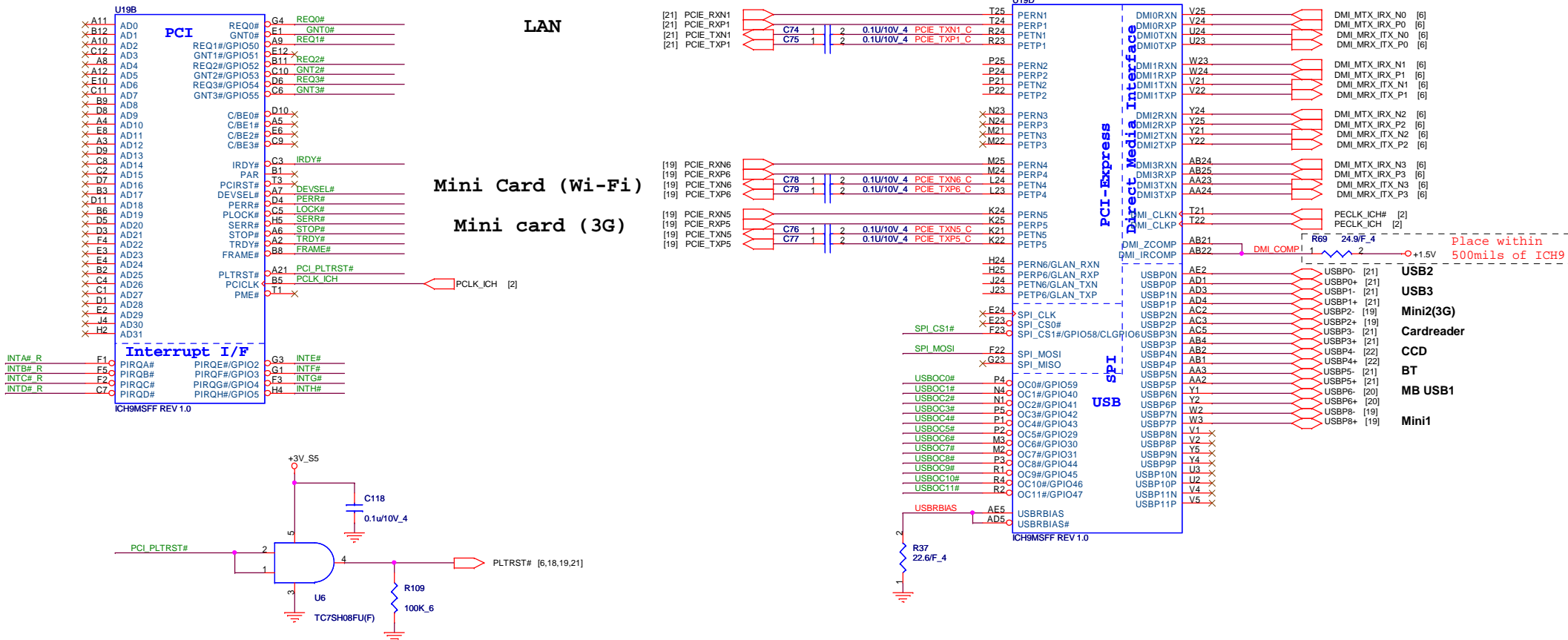
Date: Saturday, June 27, 2009

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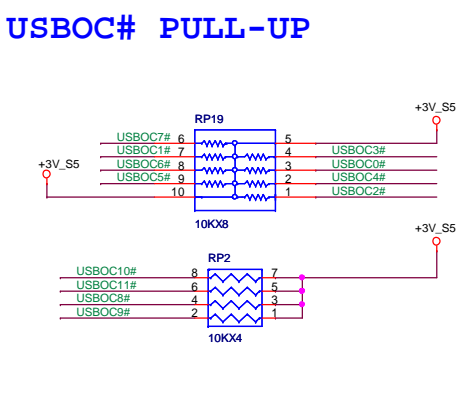
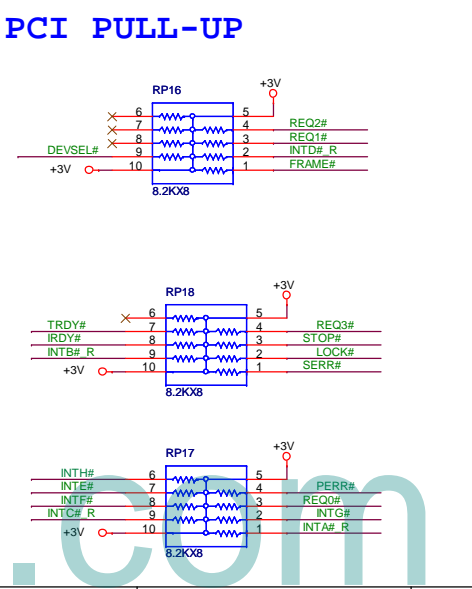
Rev: 0C

ICH9M SFF - USB/PCIE/DMI (CLG)

Place TX DC blocking caps close ICH9.



Pin Name	Strap description	Sampled	Configuration	PU/PD									
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0										
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	GNT2# T6									
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# T4									
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI T11									
GNT0#	Boot BIOS Selection 0	PWROK	<table border="1"> <thead> <tr> <th>PCI_GNT#0</th> <th>SPI_CS#1</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>SPI(Default)</td> </tr> <tr> <td>1</td> <td>0</td> <td>PCI</td> </tr> </tbody> </table>	PCI_GNT#0	SPI_CS#1	Boot Location	0	1	SPI(Default)	1	0	PCI	GNT0# T2
PCI_GNT#0	SPI_CS#1	Boot Location											
0	1	SPI(Default)											
1	0	PCI											
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# T10									



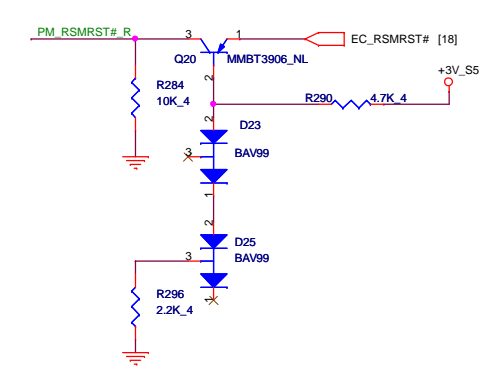
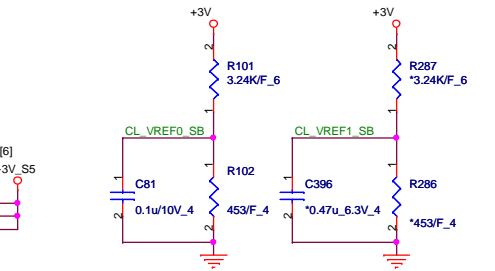
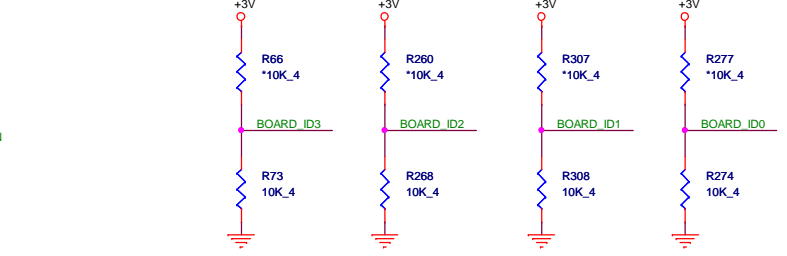
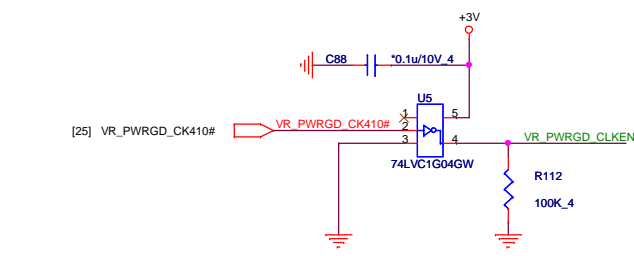
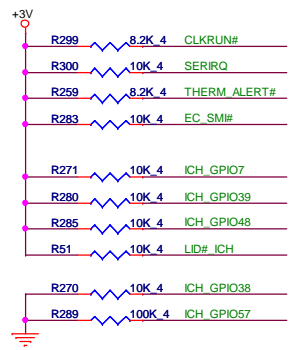
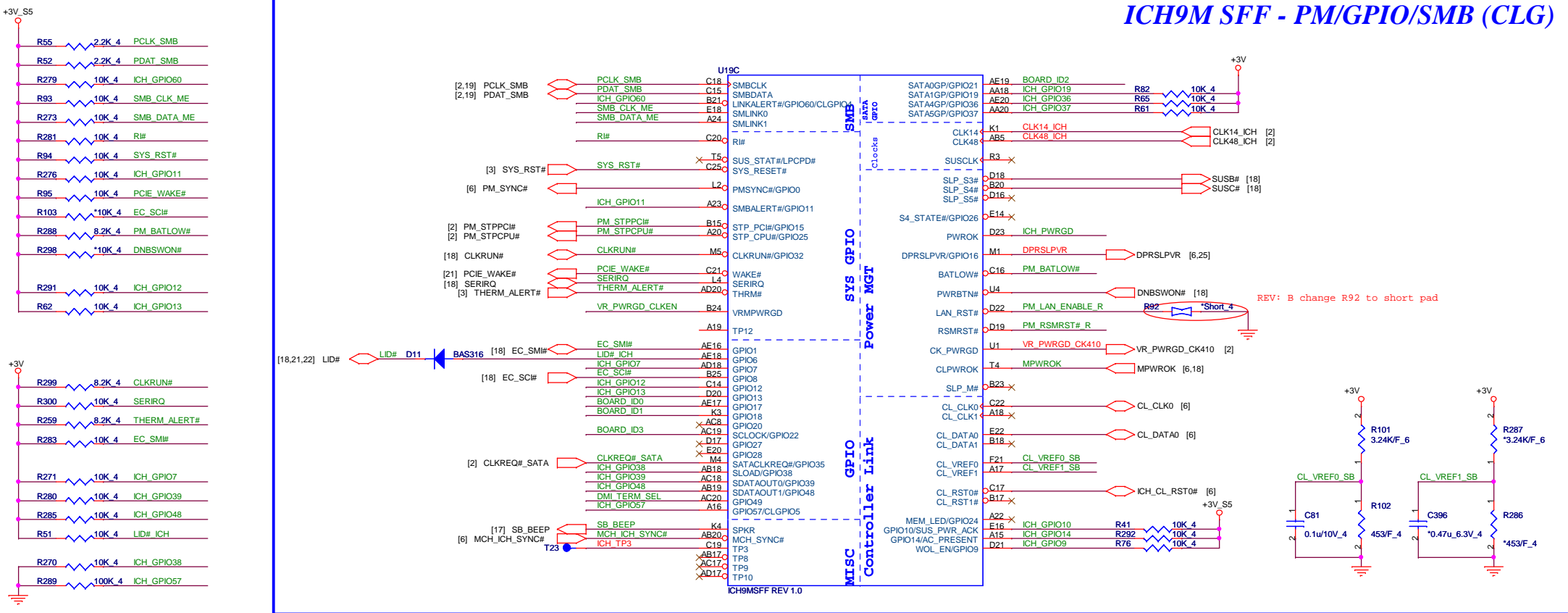
QUANTA COMPUTER

File: **ICH9M SFF (USB/PCIE/DMI)**

Size: Document Number **ZH8** Rev **0C**

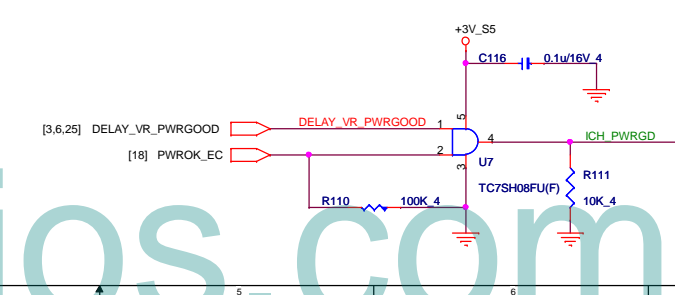
Date: Saturday, June 27, 2009 Sheet 12 of 31

ICH9M SFF - PM/GPIO/SMB (CLG)



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL T12



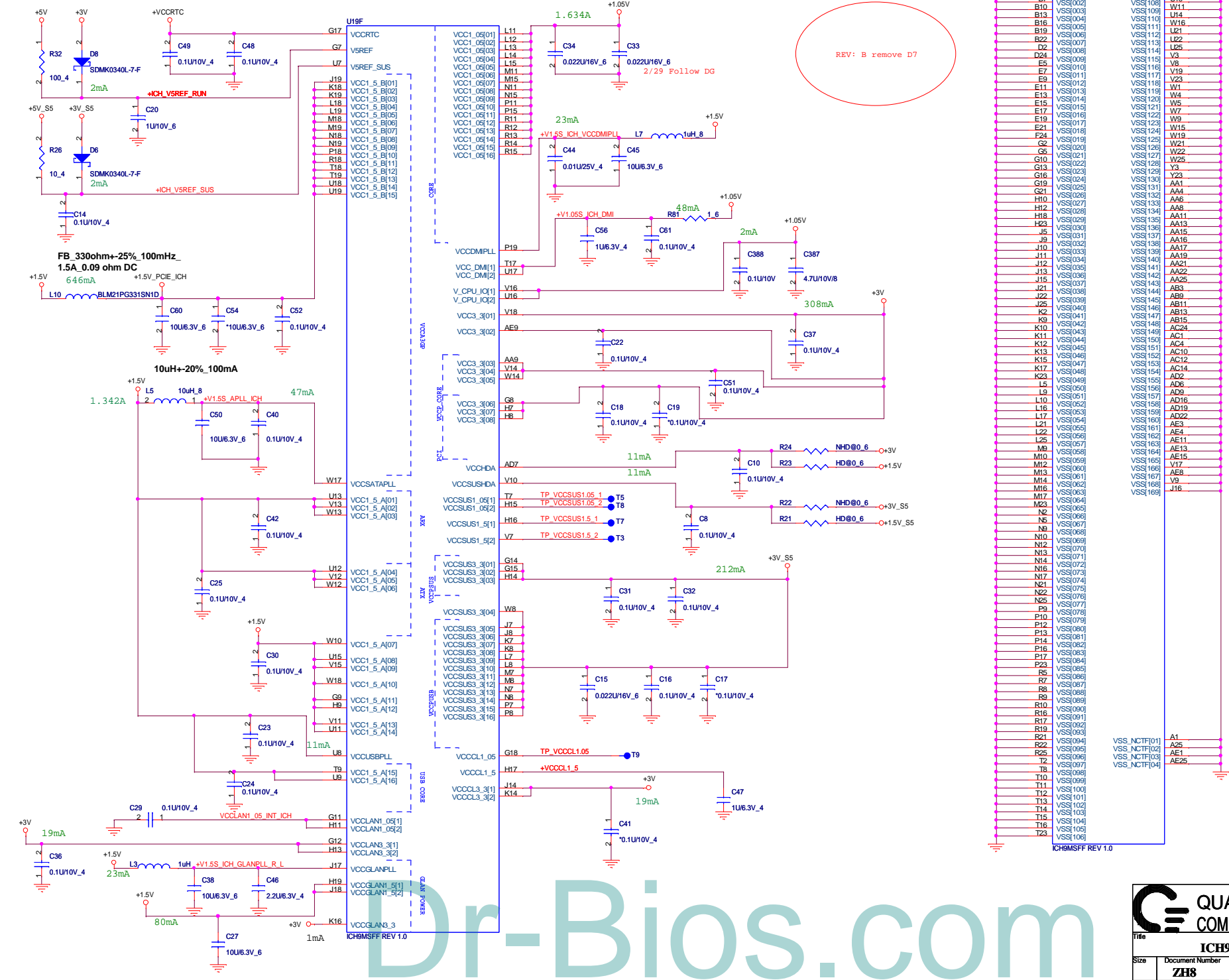
QUANTA COMPUTER

Title: **ICH9M SFF (PM/GPIO/SMB)**

Size: Document Number **ZH8** Rev **0C**

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ICH9M SFF - Power/GND (CLG)



U19E	U19E	U5
B4	VSS[001]	VSS[107]
B7	VSS[002]	VSS[108]
B10	VSS[003]	W11
B13	VSS[004]	W14
B16	VSS[005]	W16
B19	VSS[006]	W17
B22	VSS[007]	W18
D24	VSS[008]	W19
D2	VSS[009]	W2
E5	VSS[010]	W8
E7	VSS[011]	W9
E9	VSS[012]	W23
E11	VSS[013]	W1
E13	VSS[014]	W4
E15	VSS[015]	W5
E17	VSS[016]	W7
E19	VSS[017]	W9
E21	VSS[018]	W15
F24	VSS[019]	W19
G2	VSS[020]	W22
G5	VSS[021]	VSS[127]
G10	VSS[022]	VSS[128]
G13	VSS[023]	Y3
G16	VSS[024]	Y23
G19	VSS[025]	AA1
G21	VSS[026]	AA4
H10	VSS[027]	AA6
H12	VSS[028]	AA8
H18	VSS[029]	AA9
H23	VSS[030]	AA11
J5	VSS[031]	AA15
J8	VSS[032]	AA16
J11	VSS[033]	AA19
J12	VSS[034]	AA21
J13	VSS[035]	AA22
J15	VSS[036]	AA25
J21	VSS[037]	AB3
J22	VSS[038]	AB9
J25	VSS[039]	AB11
K2	VSS[040]	AB15
K9	VSS[041]	AB15
K10	VSS[042]	AC24
K12	VSS[043]	AC1
K13	VSS[044]	AC10
K15	VSS[045]	AC12
K17	VSS[046]	AC14
K23	VSS[047]	AD2
L5	VSS[048]	AD6
L9	VSS[049]	AD9
L10	VSS[050]	AD16
L16	VSS[051]	AD19
L17	VSS[052]	AD22
L21	VSS[053]	AE3
L22	VSS[054]	AE4
L25	VSS[055]	AE11
M1	VSS[056]	AE13
M10	VSS[057]	AE15
M12	VSS[058]	V17
M13	VSS[059]	VSS[165]
M14	VSS[060]	VSS[166]
M16	VSS[061]	AE8
M17	VSS[062]	VSS[168]
M23	VSS[063]	VSS[169]
N2	VSS[064]	
N6	VSS[065]	
N9	VSS[066]	
N10	VSS[067]	
N12	VSS[068]	
N14	VSS[069]	
N16	VSS[070]	
N17	VSS[071]	
N21	VSS[072]	
N22	VSS[073]	
N25	VSS[074]	
P9	VSS[075]	
P10	VSS[076]	
P12	VSS[077]	
P13	VSS[078]	
P14	VSS[079]	
P16	VSS[080]	
P17	VSS[081]	
P23	VSS[082]	
R5	VSS[083]	
R7	VSS[084]	
R8	VSS[085]	
R9	VSS[086]	
R10	VSS[087]	
R16	VSS[088]	
R17	VSS[089]	
R19	VSS[090]	
R21	VSS[091]	
R22	VSS[092]	
R25	VSS[093]	
T2	VSS[094]	
T8	VSS[095]	
T10	VSS[096]	
T11	VSS[097]	
T12	VSS[098]	
T13	VSS[099]	
T14	VSS[100]	
T15	VSS[101]	
T16	VSS[102]	
T23	VSS[103]	
	VSS[104]	
	VSS[105]	
	VSS[106]	



QUANTA COMPUTER

File: ICH9M SFF (Power/GND)

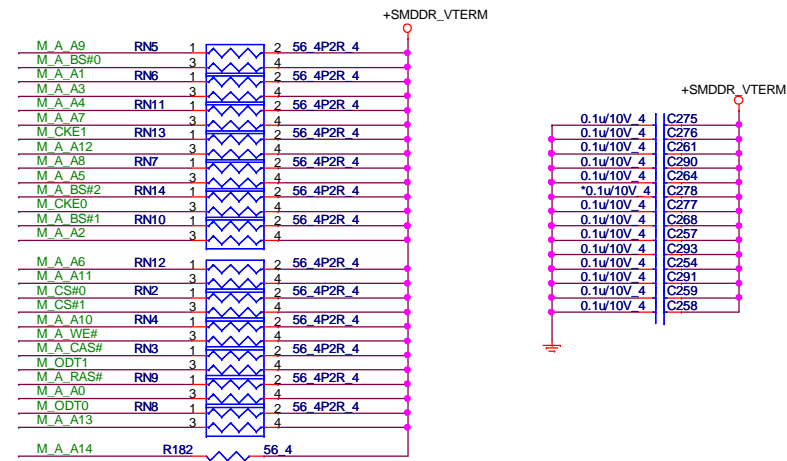
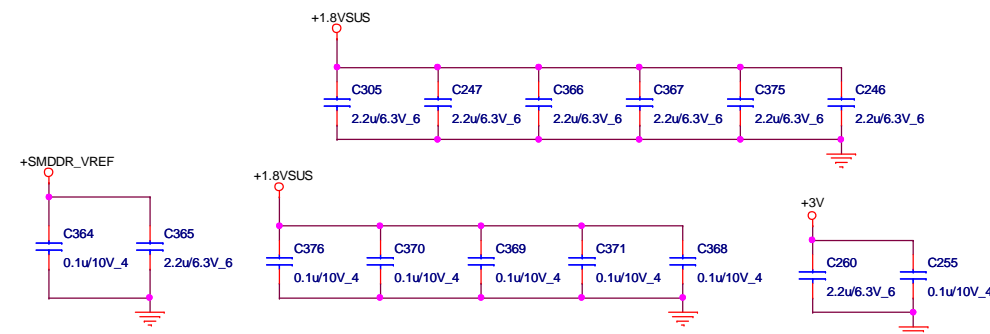
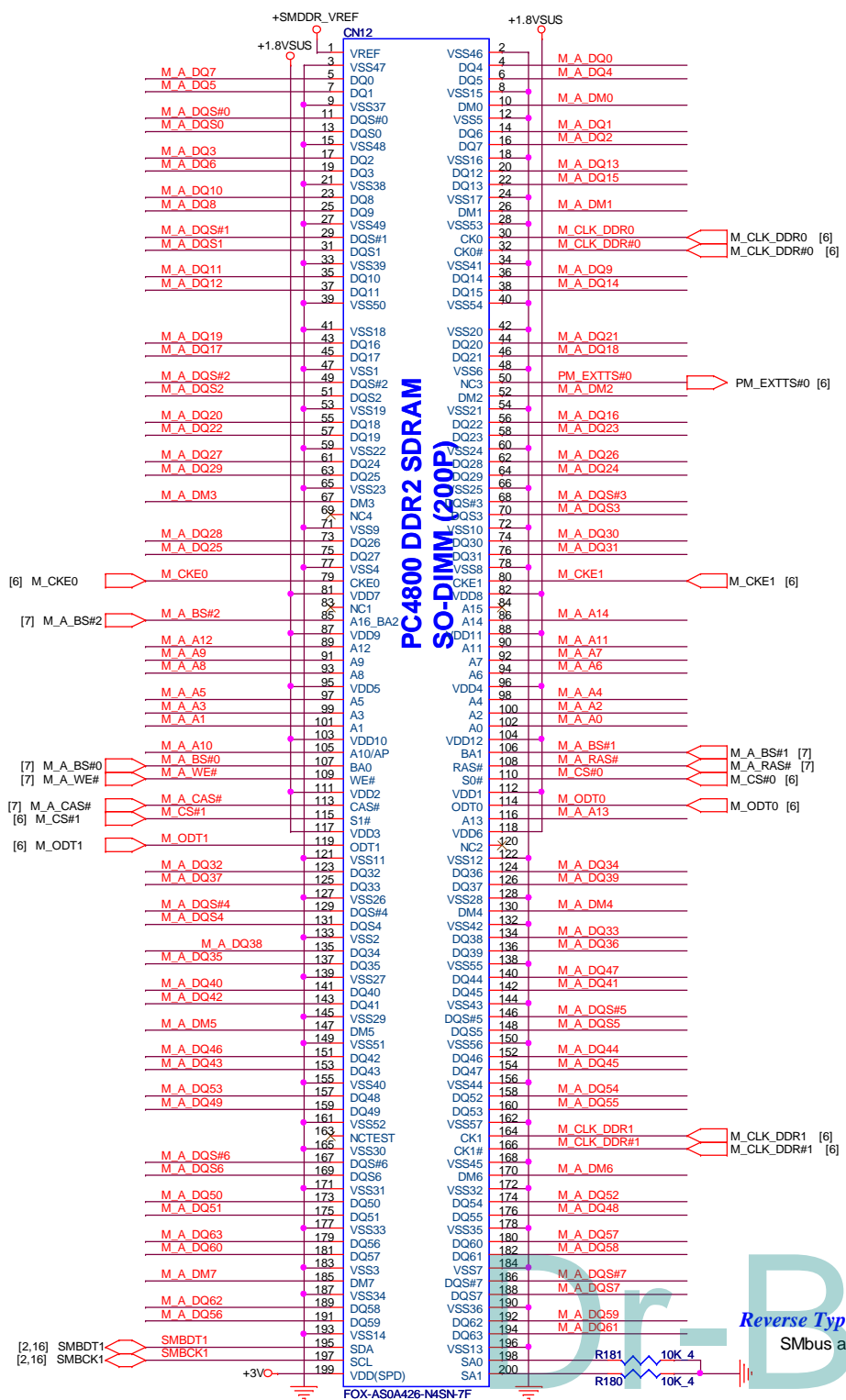
Size: ZHS

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DDRII SO-DIMM (DDR)



- [7] M_A_DQ[63:0]
- [7] M_A_DM[7:0]
- [7] M_A_DQS[7:0]
- [7] M_A_DQS#7:0]
- [7] M_A_A[14:0]

Reverse Type H: 5.2mm

SMBus address A0

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COMPUTER

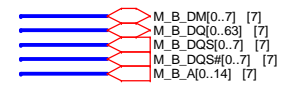
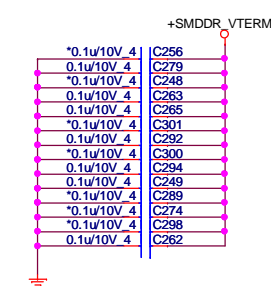
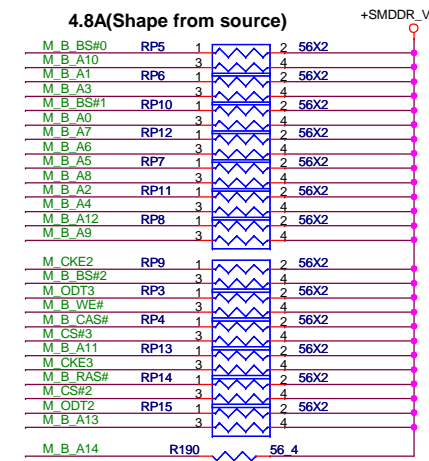
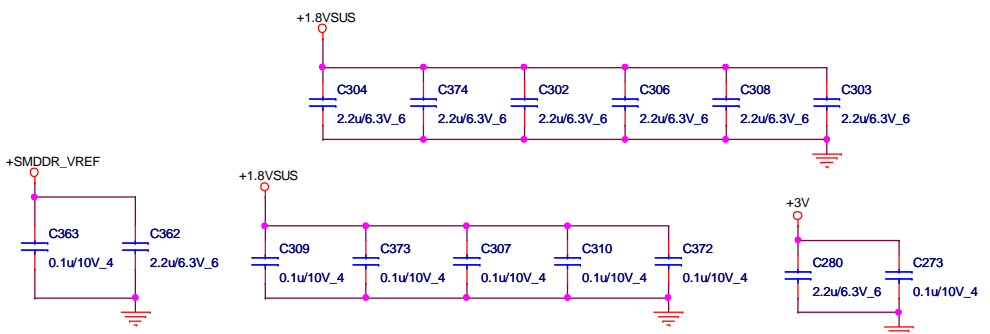
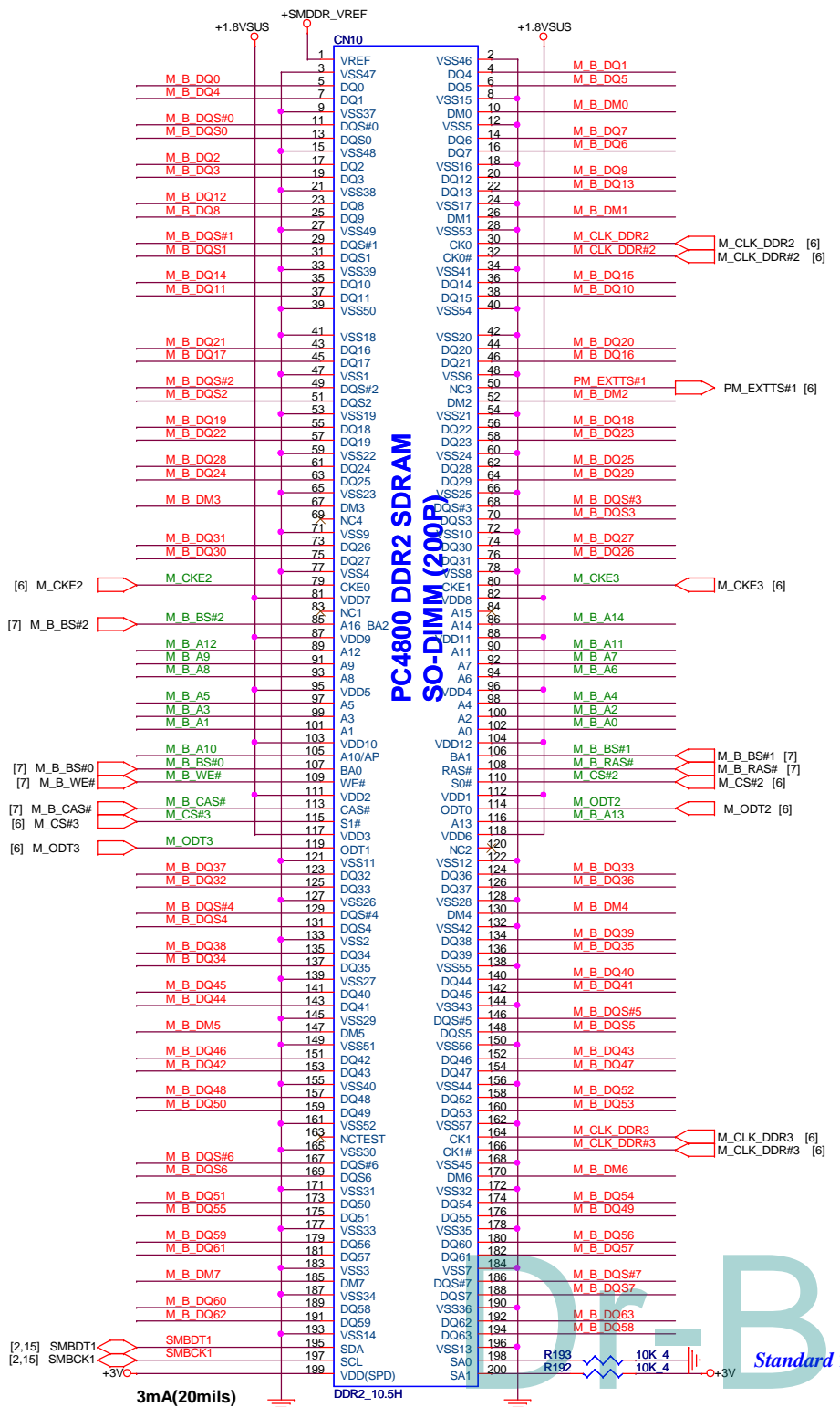
Title: **DDRII SO-DIMM**

Size: **ZH8** Document Number: **ZH8**

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DDRII SO-DIMM (DDR)

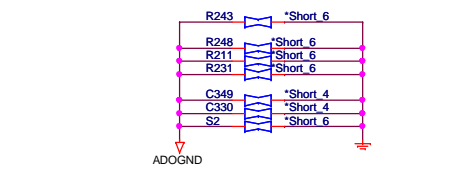
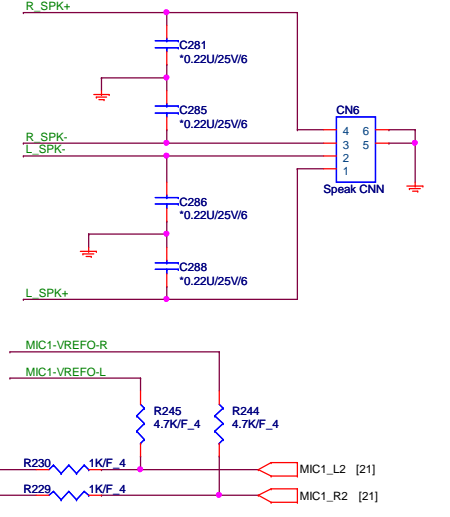
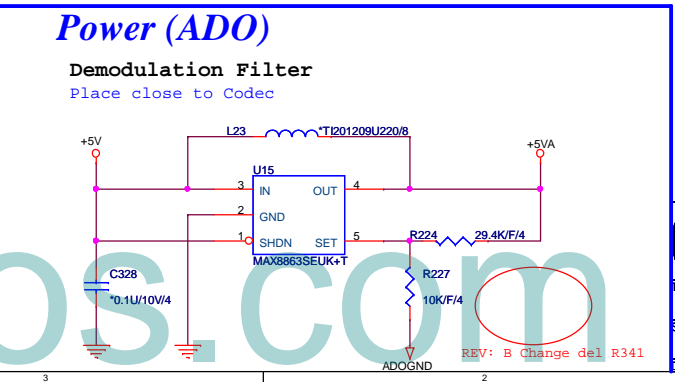
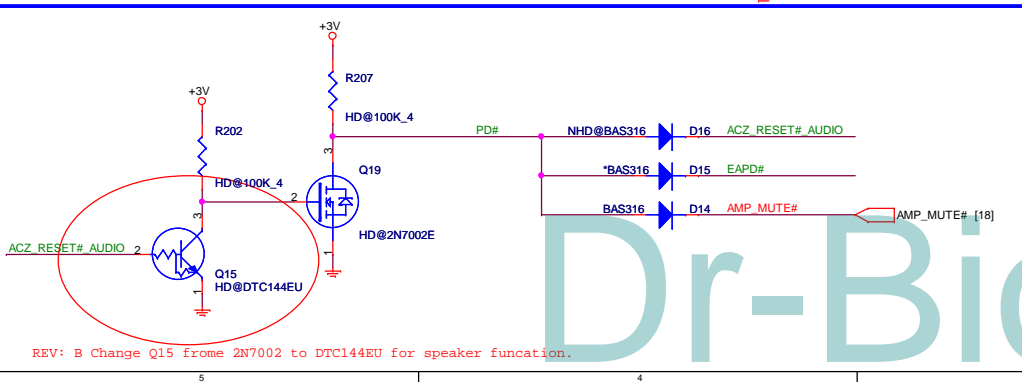
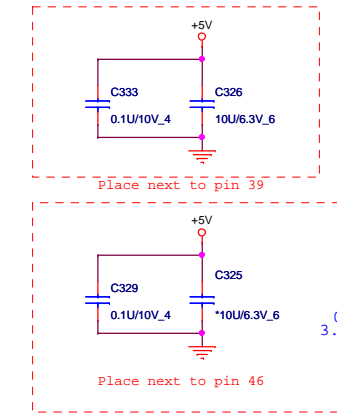
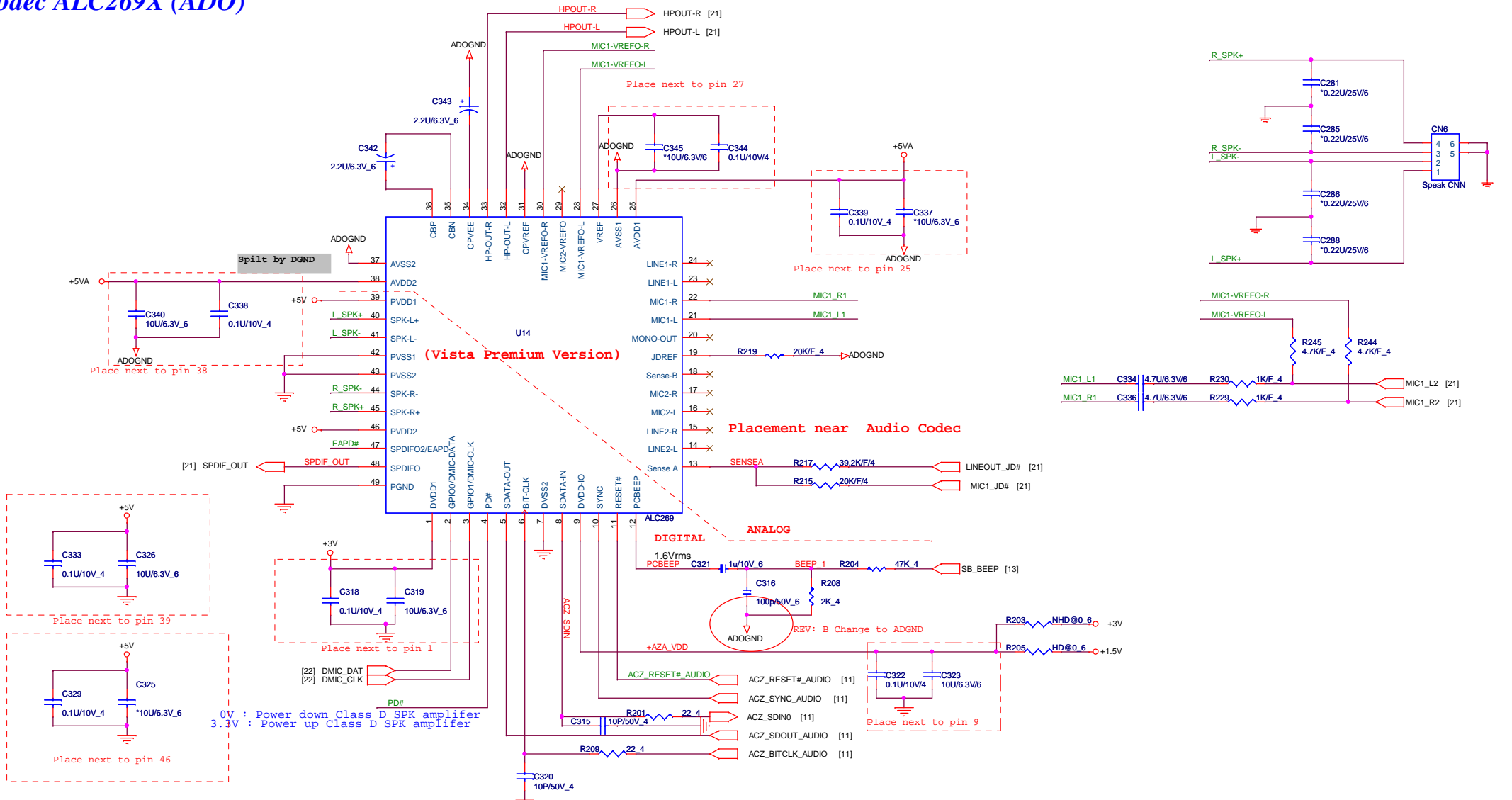
PC480 DDR2 SDRAM SO-DIMM (200R)



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Standard Type H: 5.2mm

QUANTA COMPUTER
Title: **DDRII SO-DIMM**
Size: Document Number **ZH8** Rev **0C**
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Codec ALC269X (ADO)



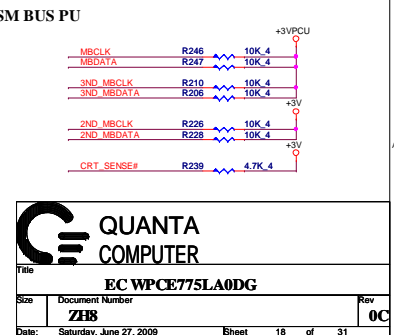
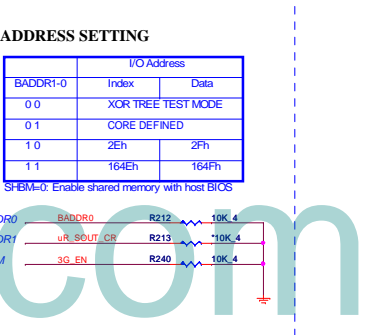
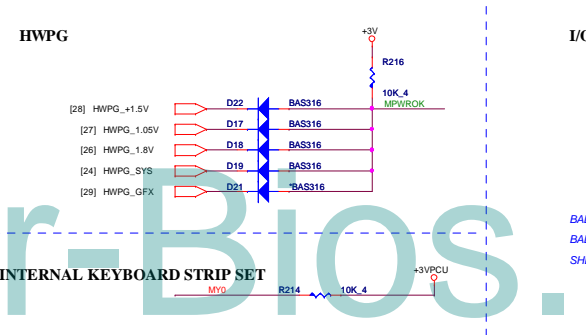
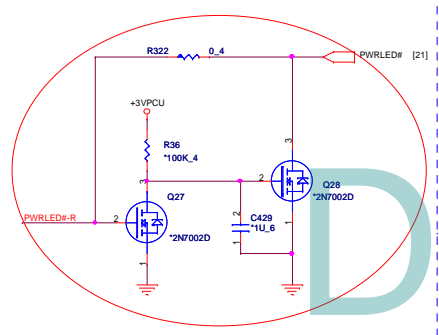
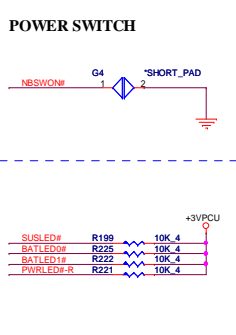
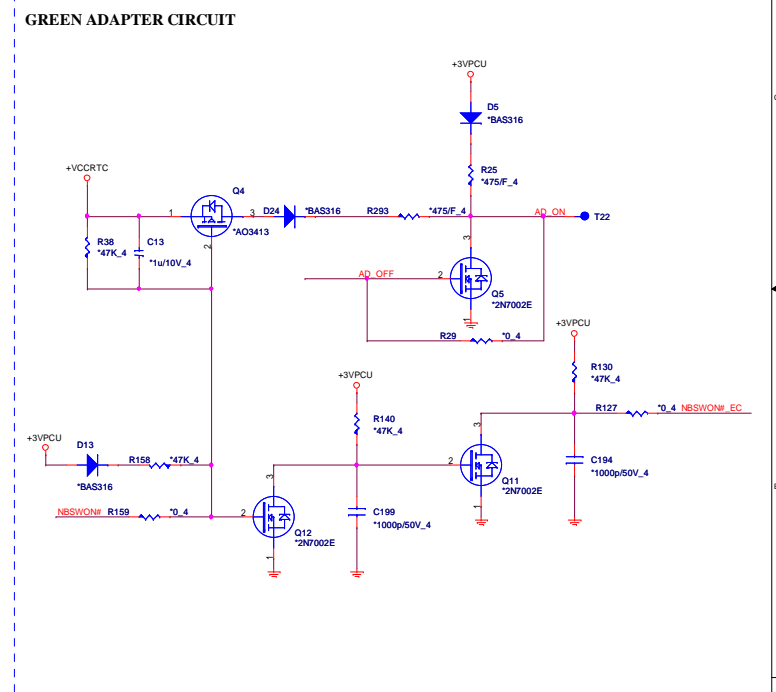
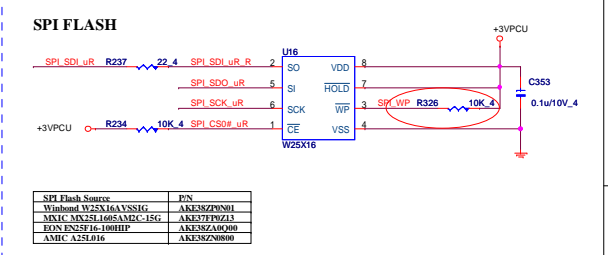
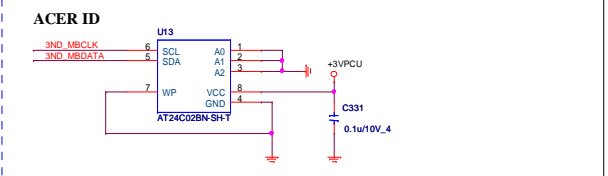
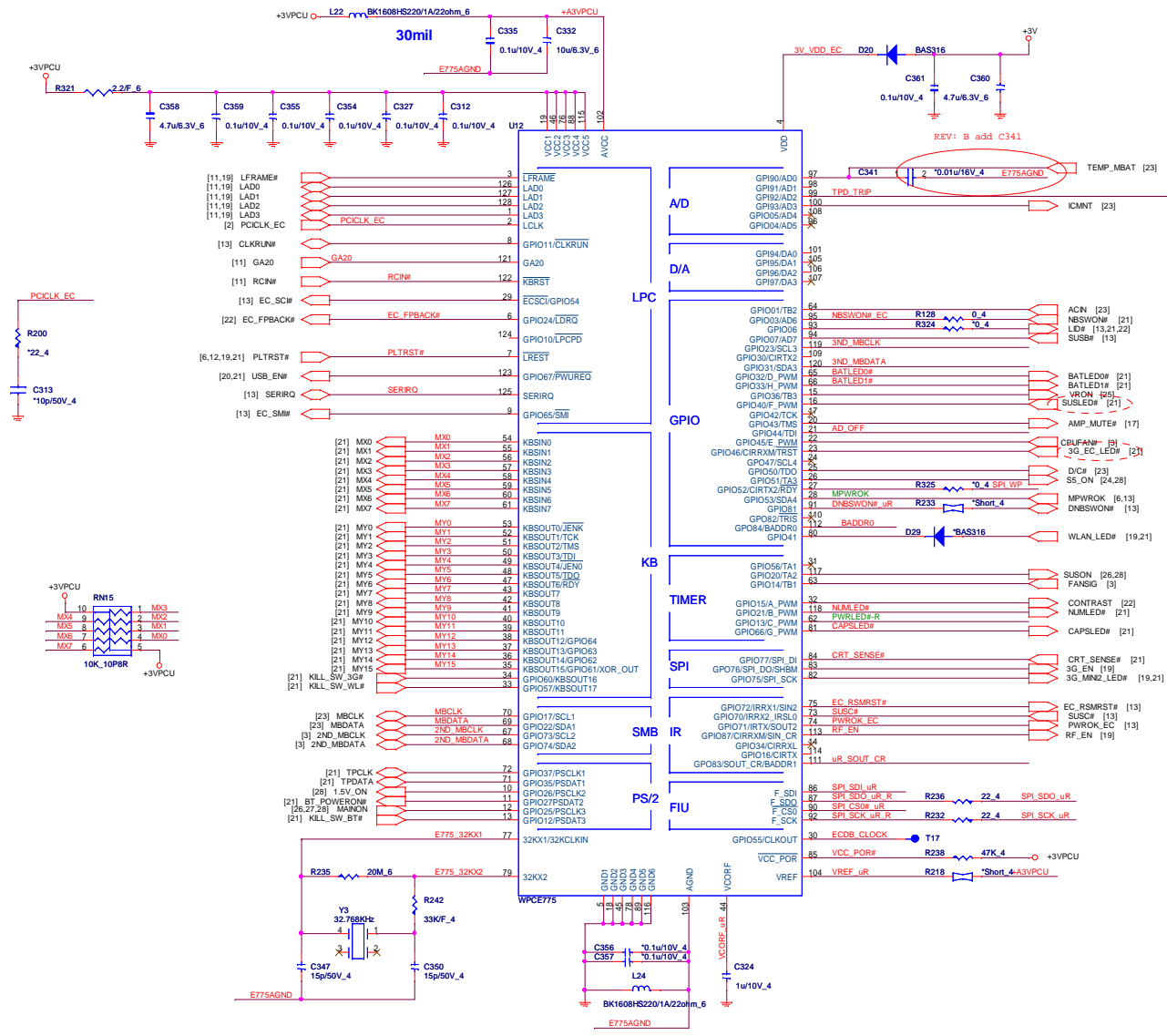
QUANTA COMPUTER

File: **Codec ALC269X**

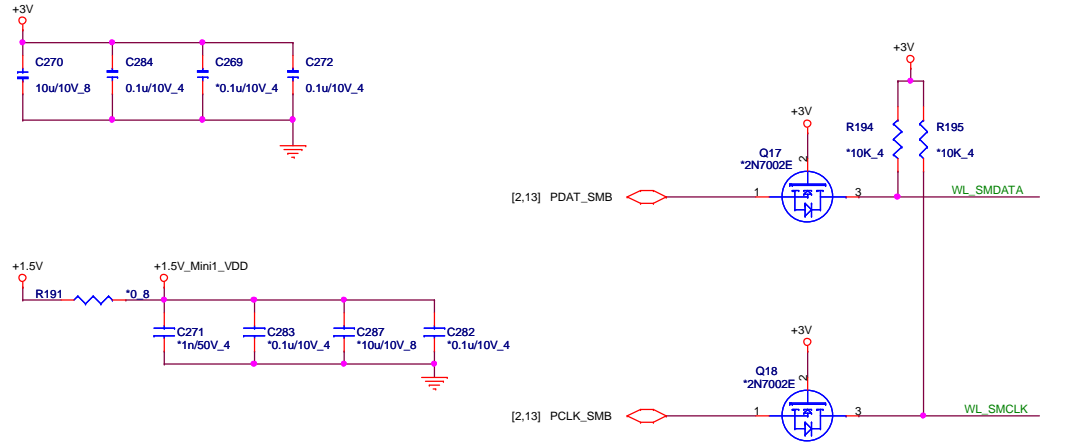
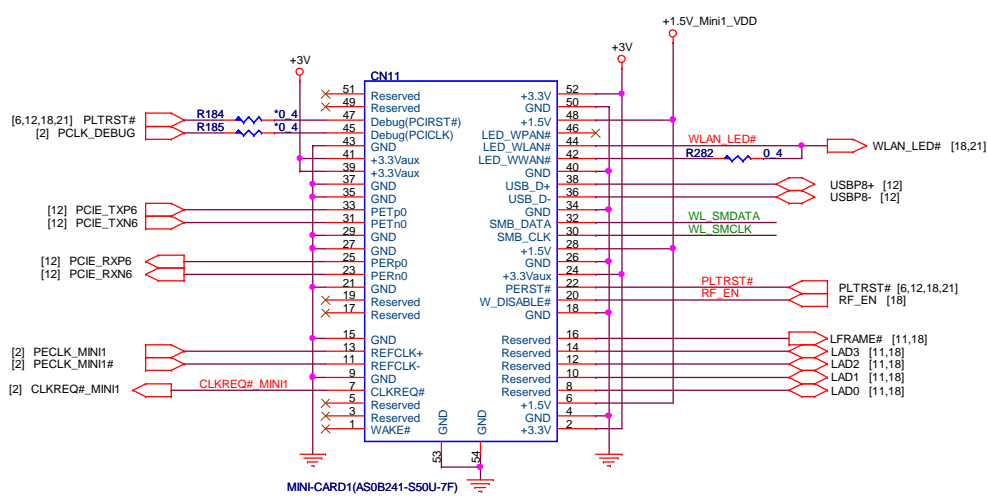
Size	Document Number	Rev
	ZH8	0C

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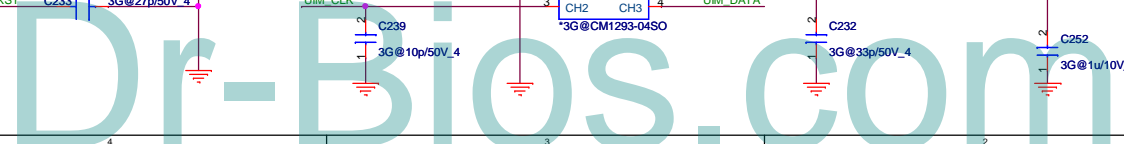
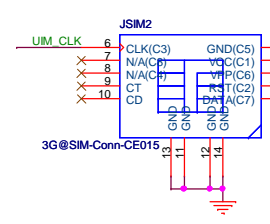
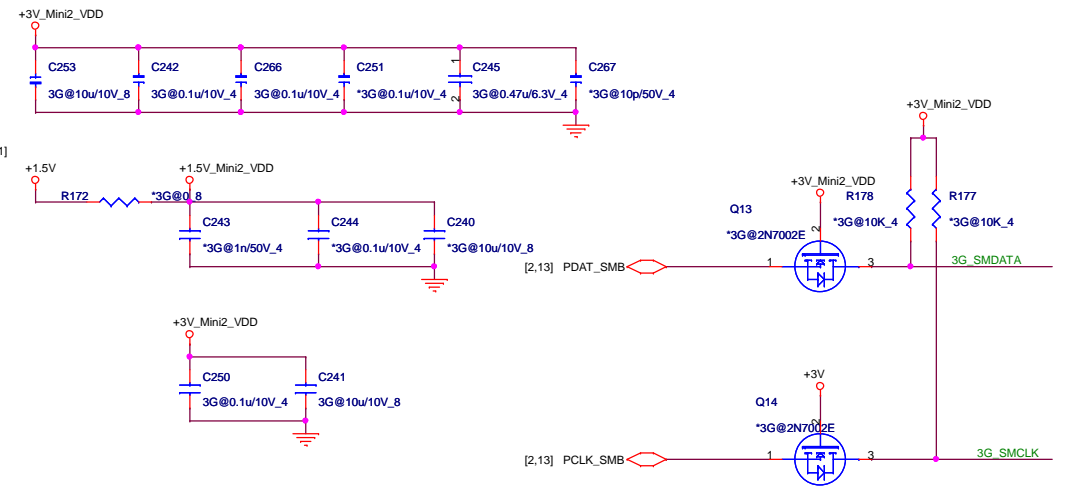
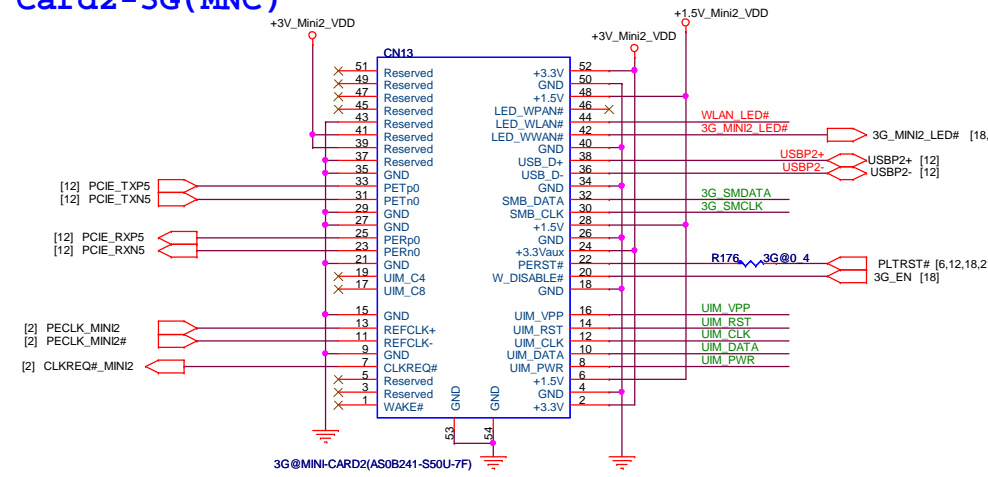
EC WPCE775LA0DG (KBC)



Mini Card1-WLAN/WMAX(MPC)

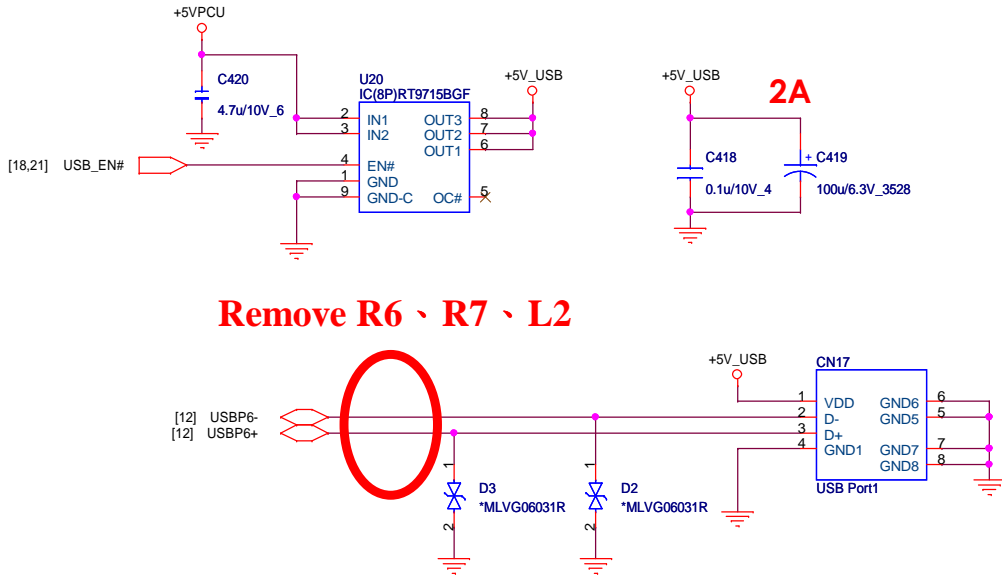


Mini Card2-3G(MNC)



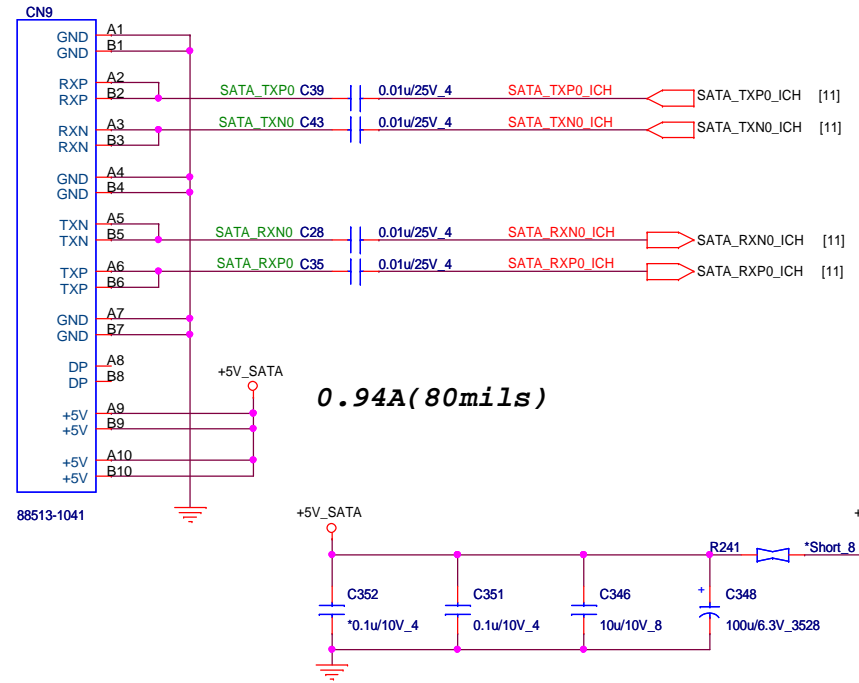
Title: MINI PCIE (WLAN/WMAX/3G)			
Size:	Document Number:	Rev: 0C	
	ZH8		
Date:	Saturday, June 27, 2009	Sheet:	19 of 31

MB USB (USB)

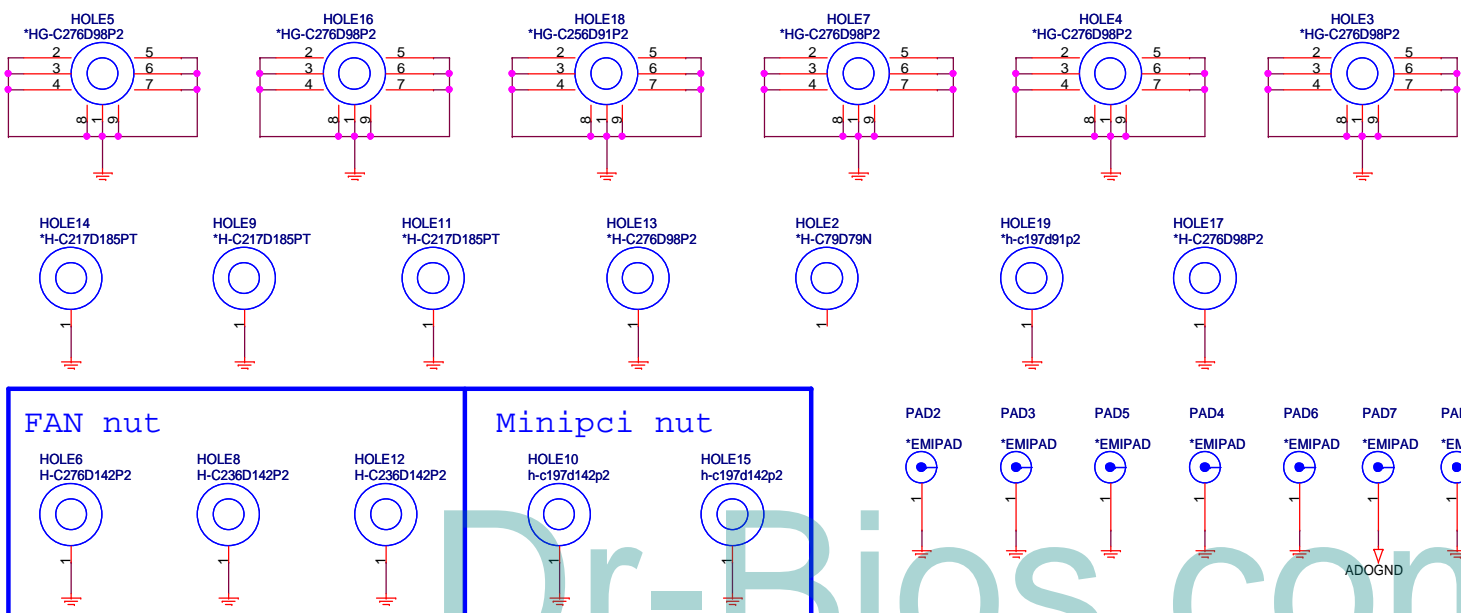


Remove R6、R7、L2

2.5" SATA HDD(HDD)



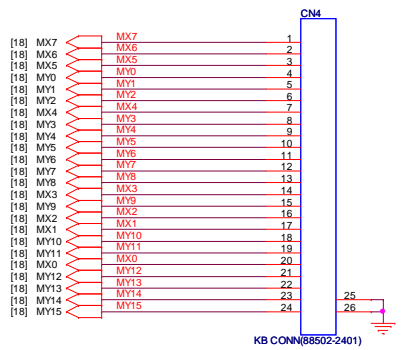
HOLE (EXC)



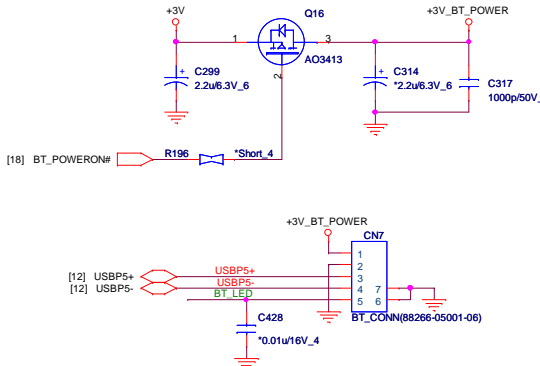
QUANTA COMPUTER
 Title: **USB/HDD/HOLE**
 Size: Document Number **ZH8** Rev **0C**
 Date: Saturday, June 27, 2009 Sheet 20 of 31

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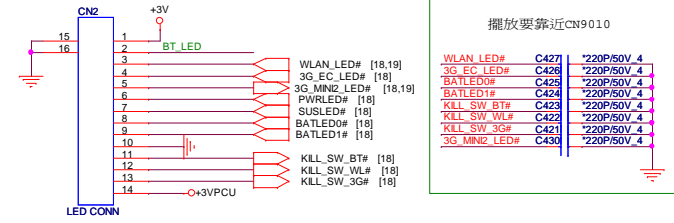
Keyboard(KBC)



BuleTooth (BTM)



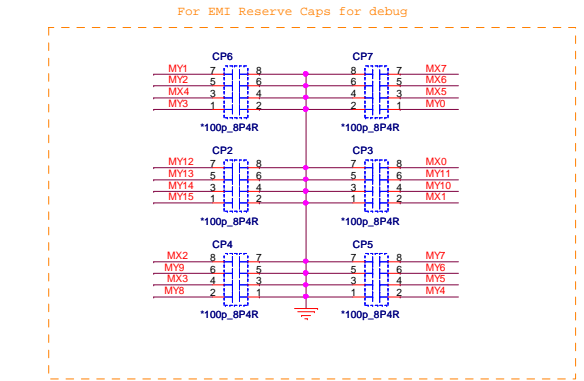
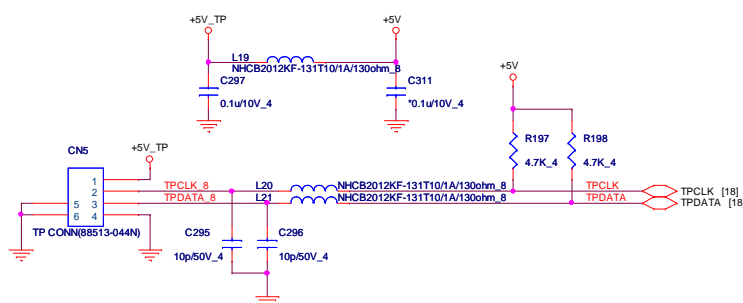
LED D/B (UIF)



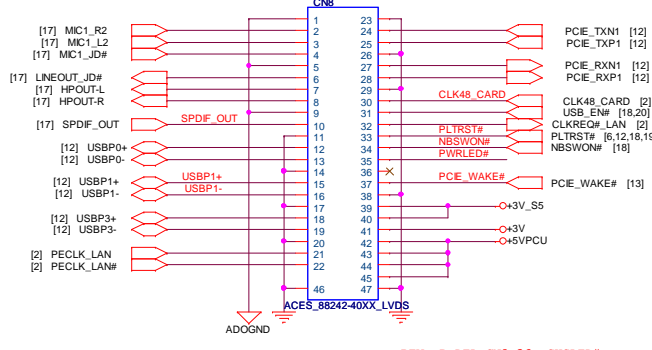
Check P/N footprint

擺放要靠近CN9010

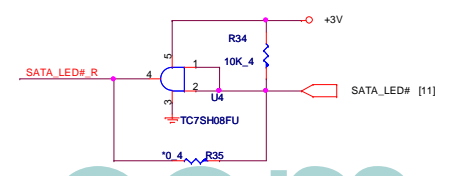
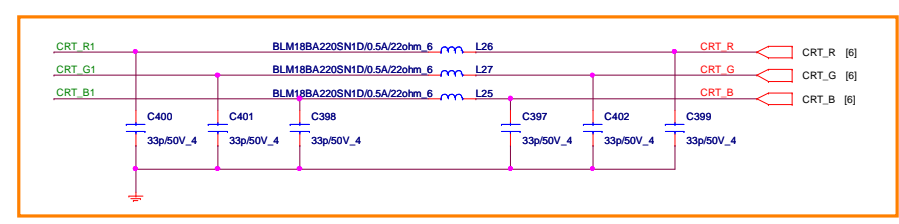
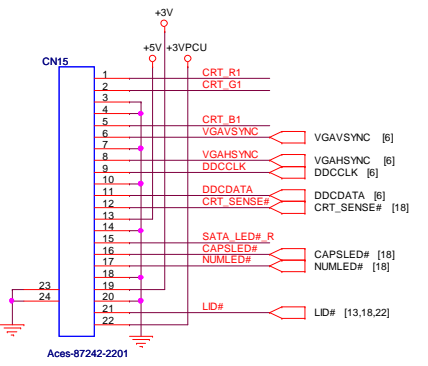
Touch Pad D/B (TPD)



Card Reader/USB DB CONNECTER(MMC)/Power Connector



CRT D/B (UIF)



QUANTA COMPUTER

Document Number: **ZHS**

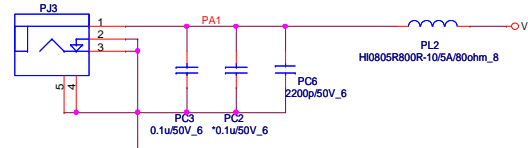
Date: Saturday, June 27, 2009

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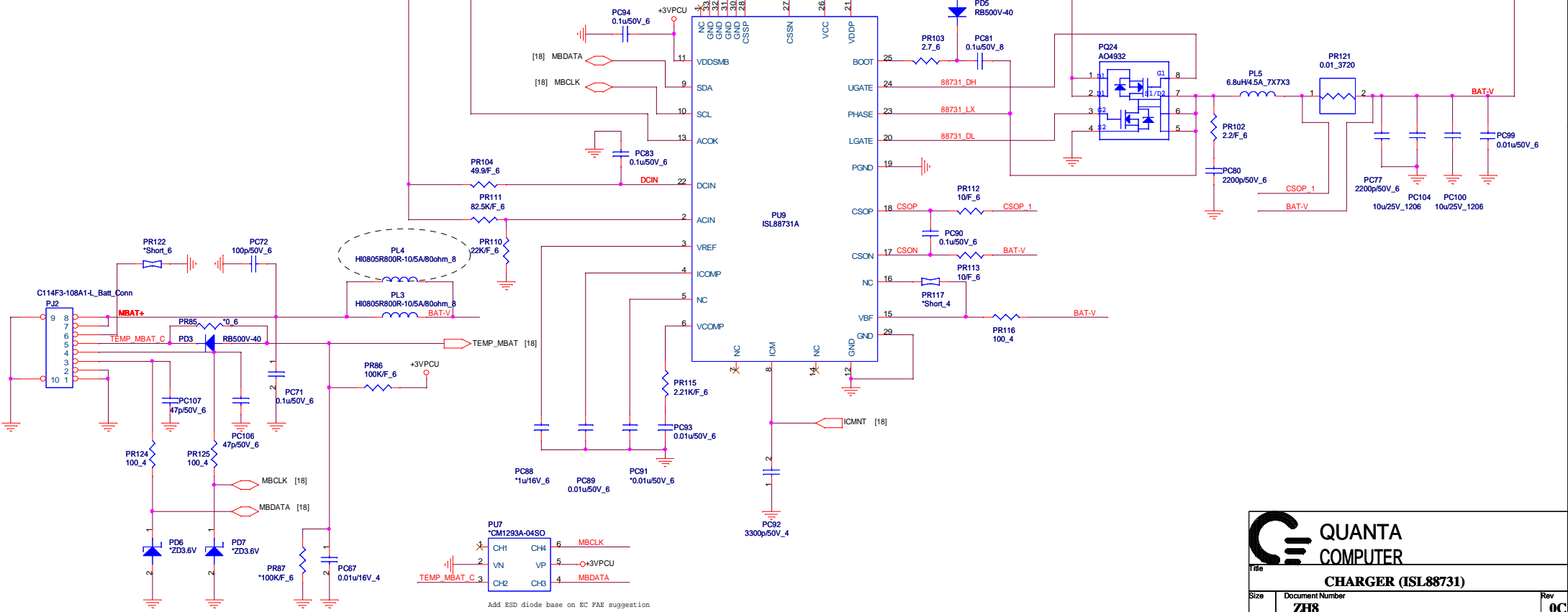
Charger(DCD)

DC-IN JACK



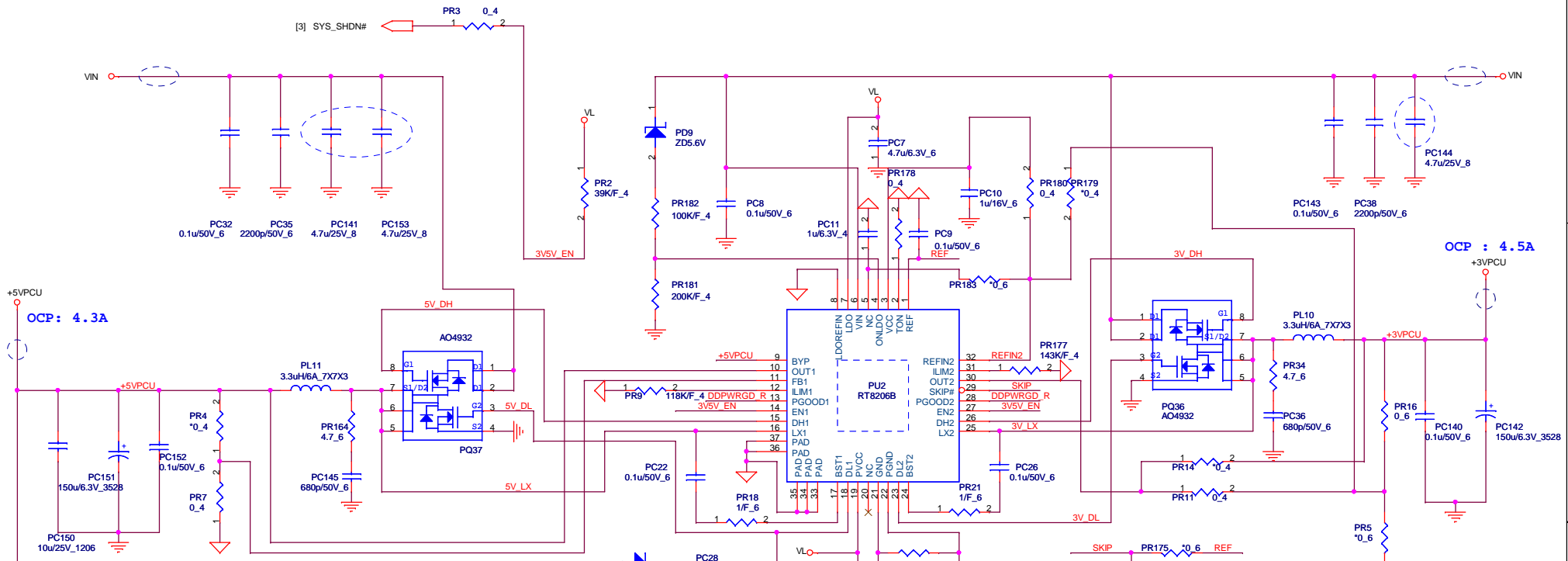
POWER JACK

dclj-2dc3003-001211-5p



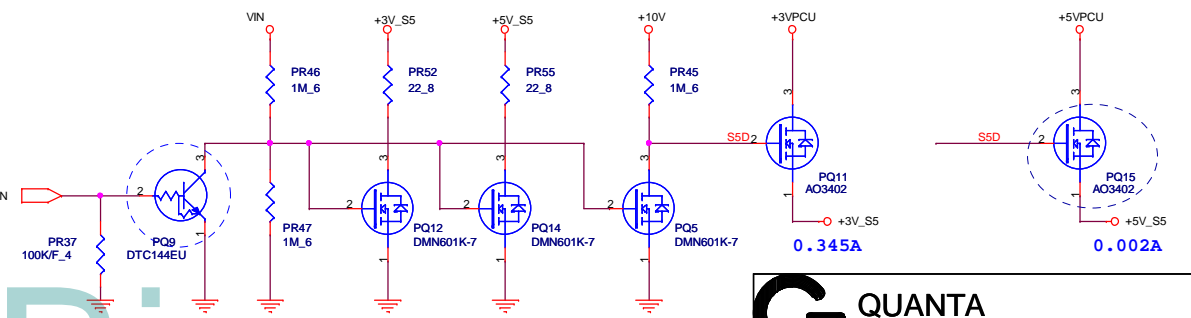
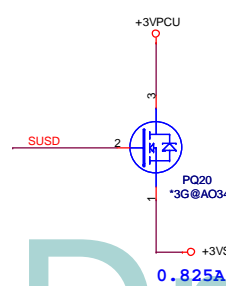
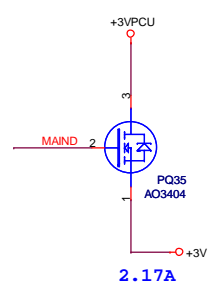
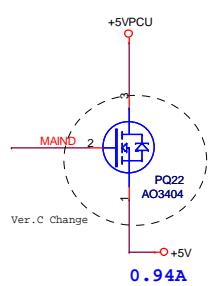
Title: CHARGER (ISL88731)	
Size: ZH8	Document Number: ZH8
Date: Saturday, June 27, 2009	Sheet: 23 of 30
Rev: 0C	

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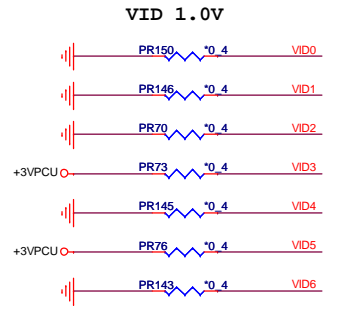
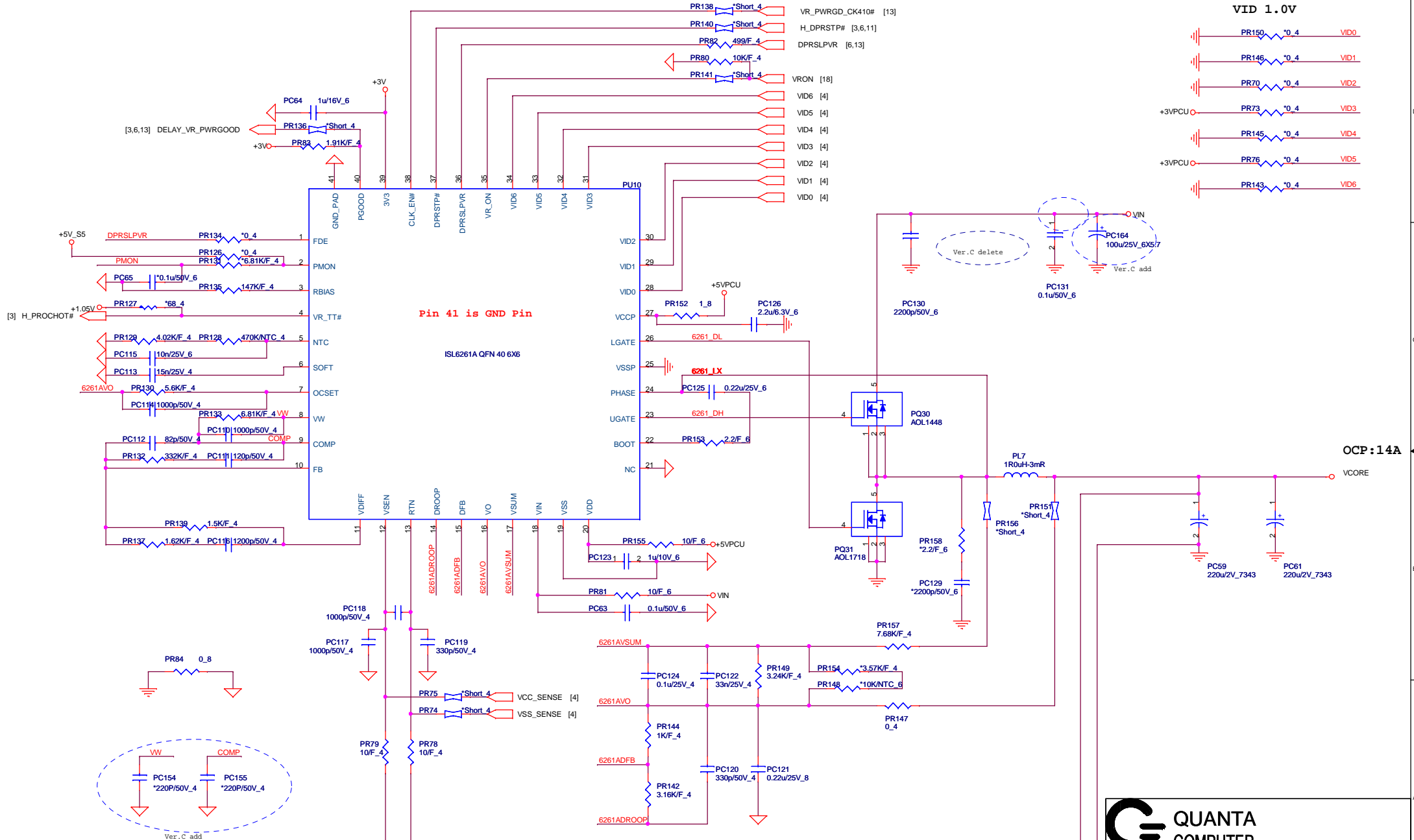
AO4932 Rds=15.8~19.6mOhm
 +5VPCU OCP:4.3A 400K
 $L(\text{ripple current}) = (19-5) * 5 / (3.3u * 400k * 19) \sim 2.791A$
 $I_{ocp} = 4.3 - (2.791 / 2) \sim 2.9045A$
 $V_{th} = 2.9045A * 19.6mOhm = 56.9282mV$
 $R(I_{lim}) = (56.9282mV * 10) / 5uA \sim 113.8K = 118K$

AO4932 Rds=15.8~19.6mOhm
 +3VPCU OCP:4.5A 500K
 $L(\text{ripple current}) = (19-3.3) * 3.3 / (3.3u * 500k * 19) \sim 1.653A$
 $I_{ocp} = 4.5 - (1.653 / 2) \sim 3.6735A$
 $V_{th} = 3.6735A * 19.6mOhm = 72mV$
 $R(I_{lim}) = (72mV * 10) / 5uA \sim 144K = 143K$



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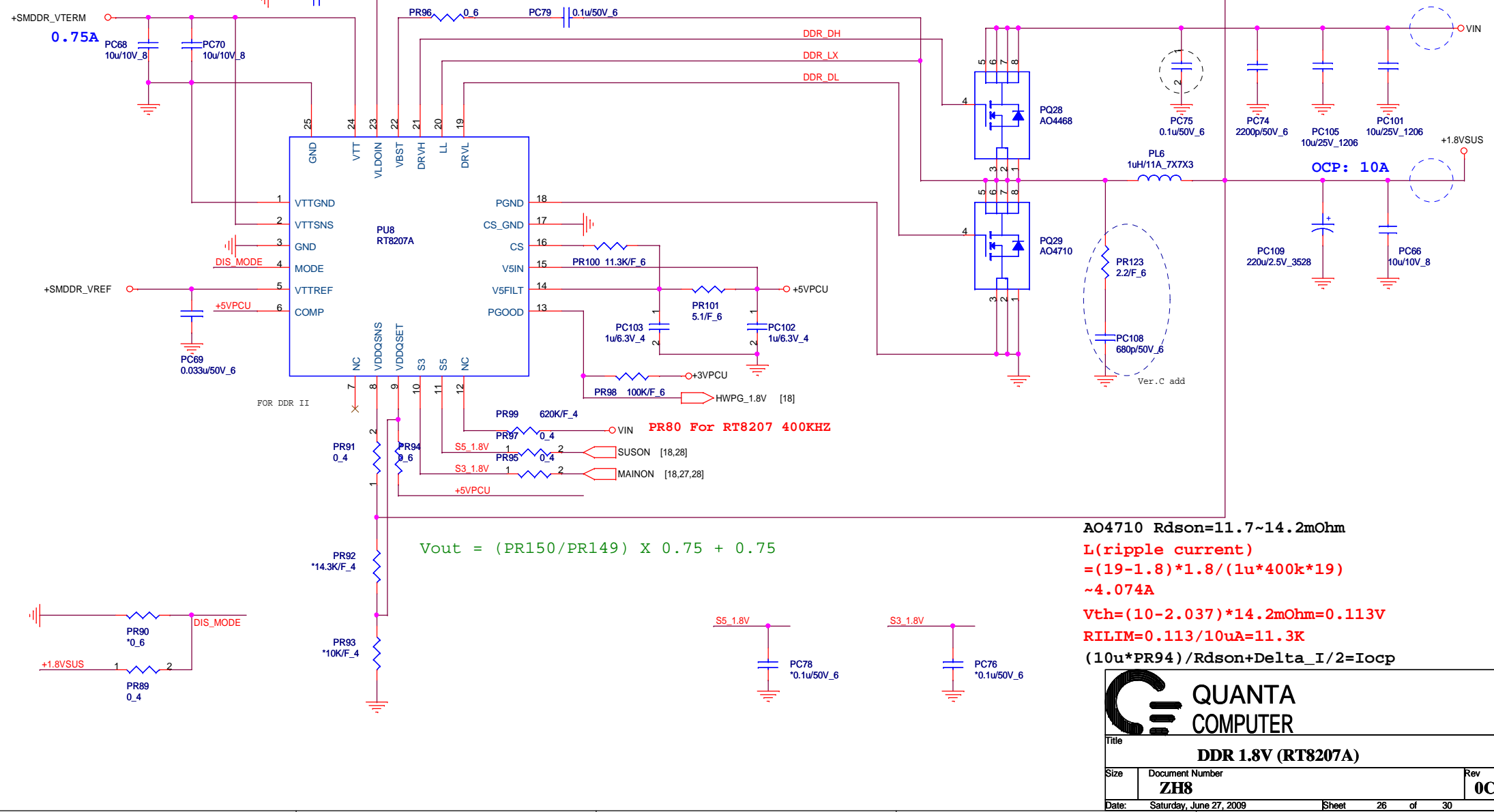
QUANTA COMPUTER
 Title: **SYSTEM 5V/3V (RT8206B)**
 Size: Document Number: **ZHS** Rev: **0C**
 Date: Saturday, June 27, 2009 Sheet: 24 of 30



QUANTA COMPUTER		
Title: VCore (ISL6261A)		
Size:	Document Number: ZH8	Rev: 0C
Date: Saturday, June 27, 2009	Sheet: 25	of 30

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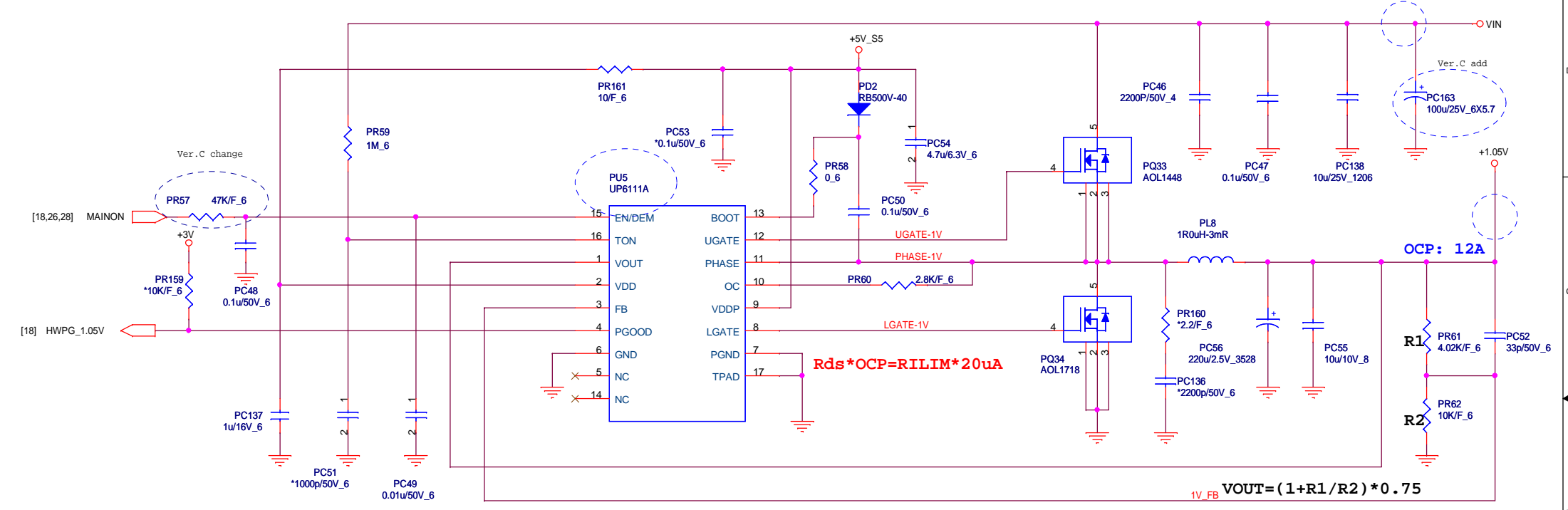
DDR 1.8V(DCD)



$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

AO4710 $R_{ds(on)} = 11.7 \sim 14.2 \text{ m}\Omega$
 I_L (ripple current)
 $= (19 - 1.8) \times 1.8 / (1 \mu \times 400 \text{ k} \times 19)$
 $\sim 4.074 \text{ A}$
 $V_{th} = (10 - 2.037) \times 14.2 \text{ m}\Omega = 0.113 \text{ V}$
 $R_{ILIM} = 0.113 / 10 \mu \text{ A} = 11.3 \text{ K}$
 $(10 \mu \times PR94) / R_{ds(on)} + \Delta I / 2 = I_{ocp}$


Title		
DDR 1.8V (RT8207A)		
Size	Document Number	Rev
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Date:	Saturday, June 27, 2009	Sheet 26 of 30



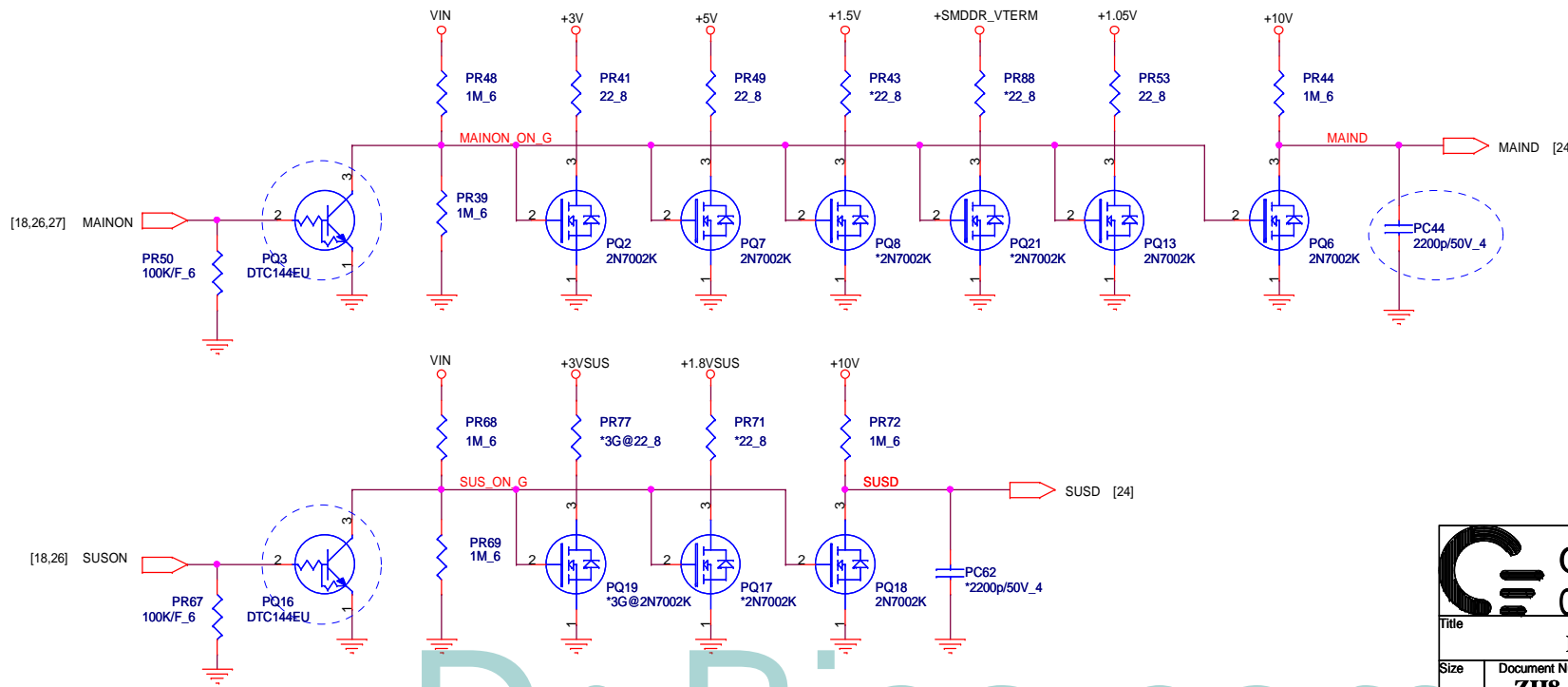
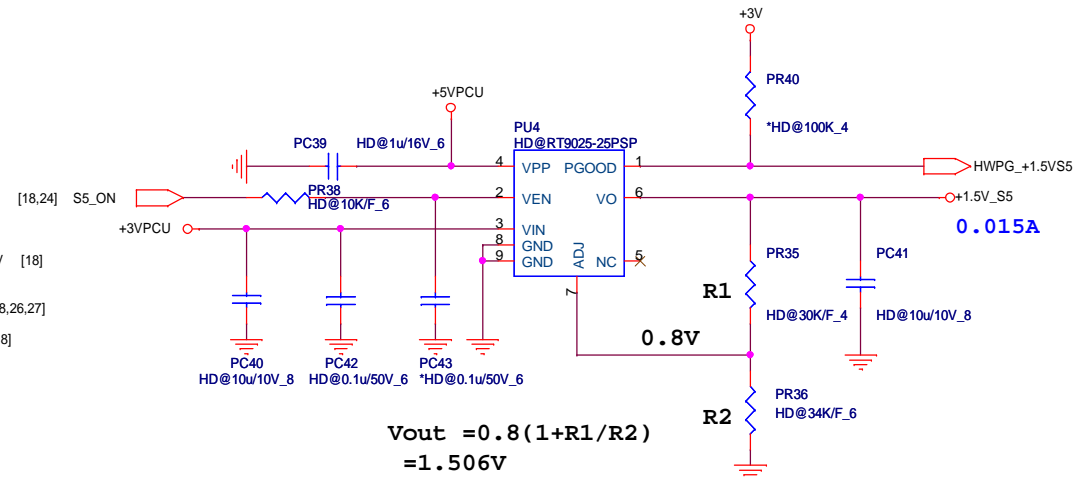
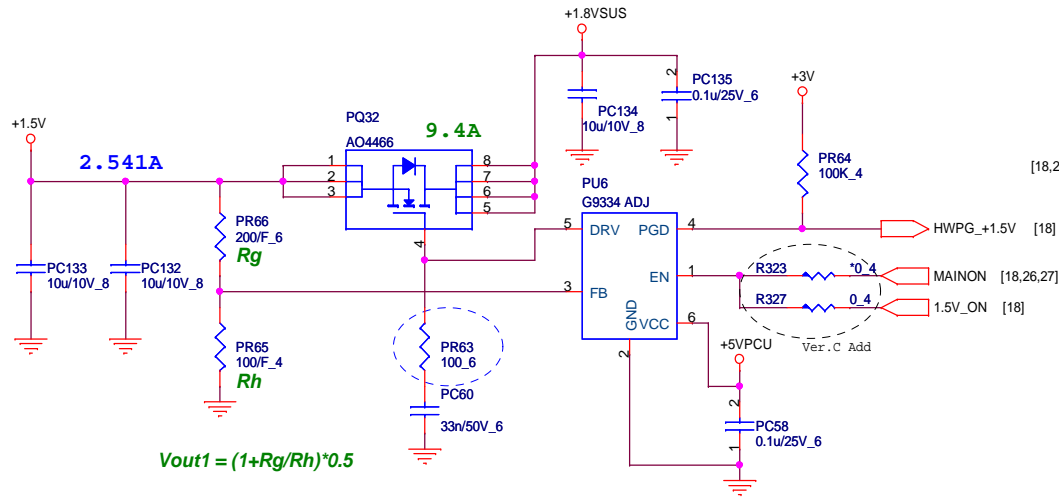
$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

AOL1412 $R_{dson} = 4.6m\Omega$
OCP = 16 - 0.8A
L(ripple current)
 $= (19 - 1.05) * 1.05 / (1u * 272k * 19)$
 $\sim 3.646A$
 $4.6m * 12 = RILIM * 20uA$
 $RILIM = 2.76K \text{ --- } 2.8K$

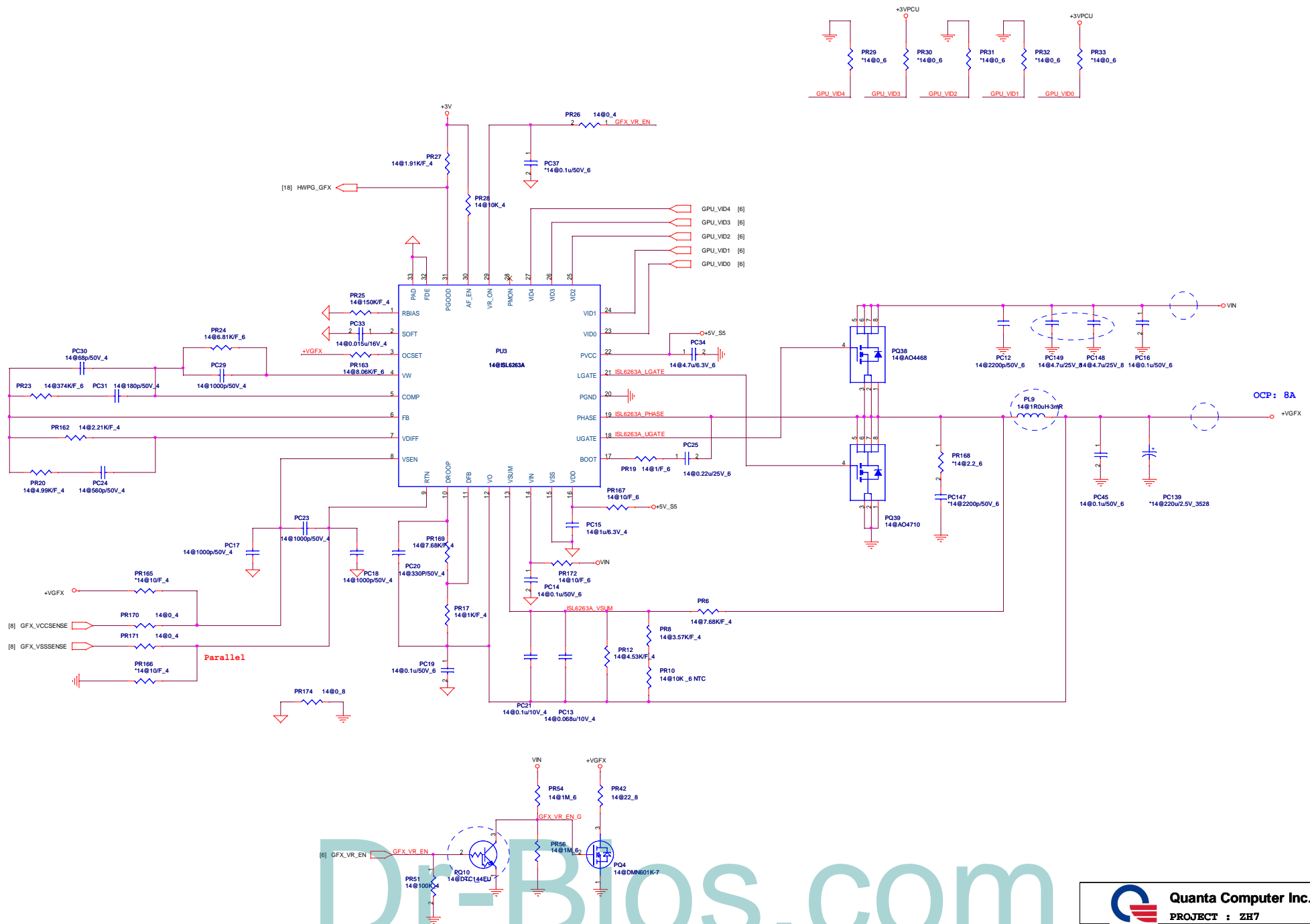
$V_{OUT} = (1 + R1/R2) * 0.75$


**QUANTA
COMPUTER**
 Title: **VCCP 1.05V (RT8202A)**
 Size: Document Number **ZH8** Rev **0C**
 Date: Saturday, June 27, 2009 Sheet 27 of 30

Discharger/1.5V(DCD)

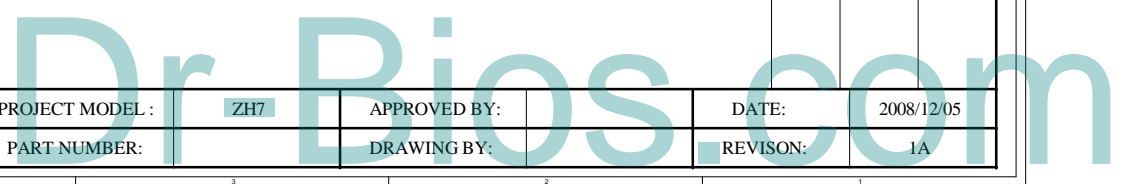


		QUANTA COMPUTER
Title Discharge/1.5V		
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Model	CHANGE LIST		MODEL	ZH7	
	REV			FROM	To
ZH7 MB	1A	FIRST RELEASED: (PCB:A)	X	1A	
	2B	<p>Page 2 : No Stuff R162 FOR EMI</p> <p>Page11 : Remove R282 ,R36 & R39</p> <p>Page11 : Change CN14 footprint.</p> <p>Page14 : Remove D7</p> <p>Page17 : Change Q15 frome 2N7002 to DTC144EU for speaker funcation.</p> <p>Page17 :Stuff U15, R244 & R227 , No stuff L23 for audio noisy.</p> <p>Page18 : Add R324</p> <p>Page18 : Add R323</p> <p>Page19 : Add R325 and short to CN11.44 for 3G LED function</p> <p>Page19 : Remove 3G wake up funcation ,Remove R179 , R183 & U11</p> <p>Page20 : CN9 Change pin define.(CONN. reverse)</p> <p>Page 9 ,13 ,17 ,22 ,23 &25 : R116 ,R269 ,R74 ,R92 ,C330 ,C349 ,R211 ,R220 ,R231 ,R243 ,R248 &R317 Change to short pad</p> <p>Page 18 : D5 ,D20 & D13 Change footprint.</p> <p>Page 29 : PL9 Change footprint.</p> <p>Page 3 : R142 Change footprint.</p> <p>Page 25 : FU10 Change footprint.</p> <p>Page 11 : CN14 Change footprint.</p> <p>Page 21 : CN4 Change footprint.</p>	1A	2A	
			1A	2A	
3C			<p>Page 17 ,20 ,21 & 22 : R186 ,R187 ,R188 ,R189 ,R241 ,R196 ,R315 ,R20 & R316 Change to short pad</p> <p>Page 18 : Add R321 for ESD(Vedor suggest)</p> <p>Page 18 : D21 connect to HWPG_GFX</p> <p>Page 18 : D29 replace by R323.</p> <p>Page 20 : DEL R6 ,R7 & L2</p> <p>Page 21 : CN2 cconnect to 3G_MINI2_LED meet customer request. and add C430 for EMI</p> <p>Page 22 : CN3.21 Change to floating</p> <p>Page 25 : page25 Delete PC127;PC128 10uf/25V_1206 and add PC164 100uF/25V 6x5.7</p> <p>Page 27 : Add PC163 100uF/25V 6x5.7</p> <p>Page 28 : Add R323 and R327</p>	1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				1A	2A
				2A	2B
				2A	2B
				2A	2B
				2A	2B
				2A	2B
2A			2B		
2B			3A		
2B			3A		
2B	3A				
2B	3A				
2B	3A				
2B	3A				
2B	3A				
1D					



EC GPIO Setting

Table with columns: Pin Name, Net Name, Setting, Description. Lists various GPIO pins and their configurations.

ICH9M GPIO Setting

Table with columns: Pin Name, Power, ICH9M Default, Net Name, Description, Setting, Internal PU/PD, External PU/PD. Lists ICH9M GPIO pins and their configurations.

CK505 Clock Setting Table

Table with columns: Pin Name, Pin, Net Name, Description. Lists Differential CPU Clock settings.

PCI Express Clock

Table with columns: Pin Name, Pin, Net Name, Description. Lists PCI Express Clock settings.

PCI Clock

Table with columns: Pin Name, Pin, Net Name, Description. Lists PCI Clock settings.

Other Clock

Table with columns: Pin Name, Pin, Net Name, Description. Lists other clock settings.

Clock Request Table

Table with columns: CLKREQ#, MAPPING, Control. Lists clock request settings.

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QUANTA COMPUTER Schematic Setting. Includes title, document number (ZH8), date (Saturday, June 27, 2009), and sheet number (31 of 31).