

A6G BLOCK DIAGRAM

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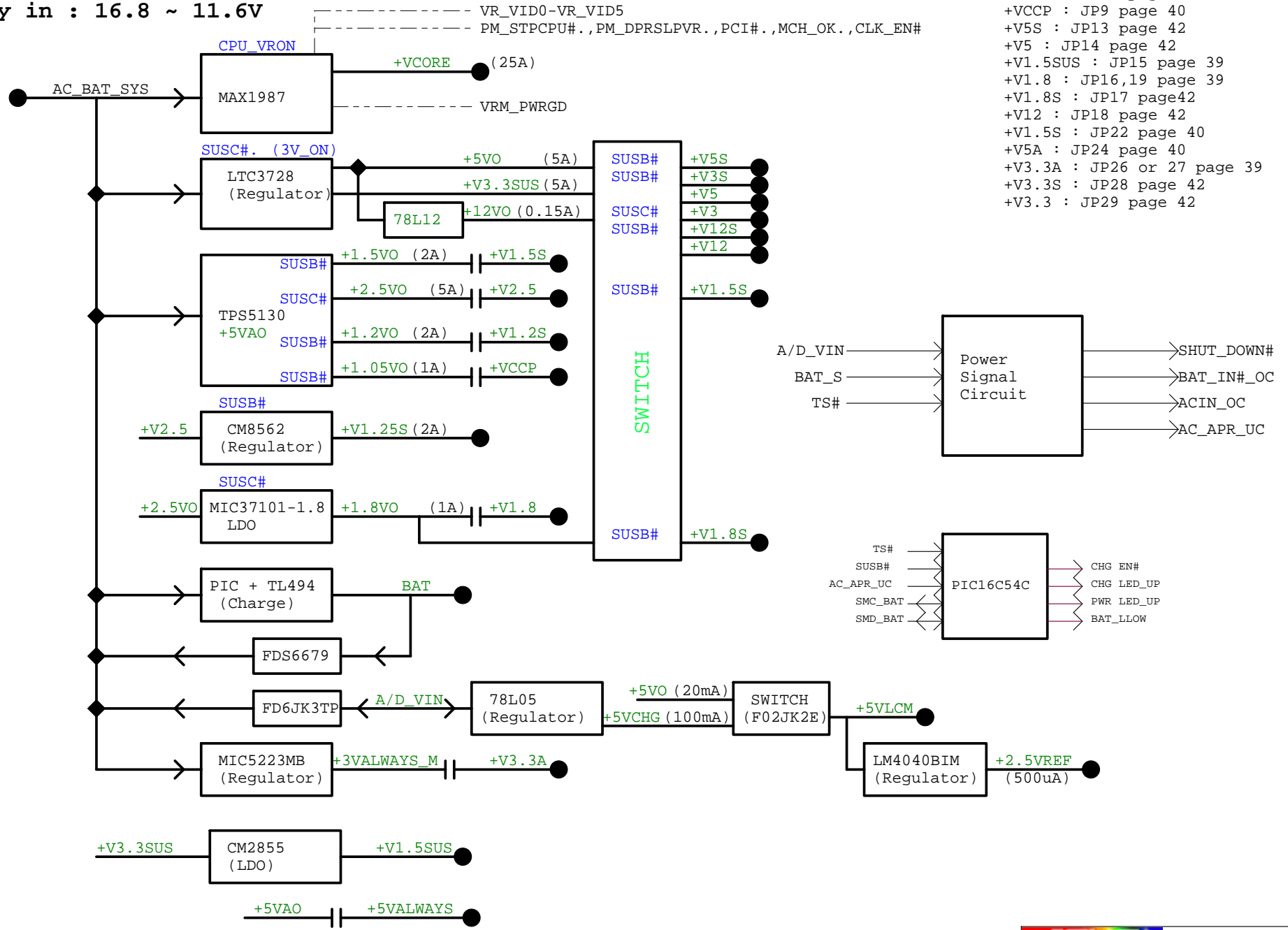
Function Key
Page 41

FILE LIST

- 01_BLOCK DIAGRAM
- 02_POWER DIAGRAM
- 03_CPU-BANIAS(HOST)
- 04_CPU-BANIAS(PWR)
- 05_THERMAL SENSOR
- 06_NB-MCHM(DDR)
- 07_NB-MCHM(HOST)
- 08_NB-MCHM(VGA)
- 09_NB-MCHM(PWR)
- 10_DUAL DDR SODIMM
- 11_DDR TREMINATION
- 12_ATI M11-P(AGP,LVDS)
- 13_ATI M11-P(MEMORY IF)
- 14_ATI M11-P(PWR)
- 15_VRAM(A CHANNEL)
- 16_VRAM(B CHANNEL)
- 17_LVDS & BACKLIGHT
- 18_CRT & TV-OUT
- 19_ICH4-M(HUB_PCI)
- 20_ICH4-M(H_U_IDE_PM)
- 21_ICH4-M(PWR)
- 22_ICH4-M(PULLUP)
- 23_CLOCK-ICS950815
- 24_LAN-RTL8100CL
- 25_MINIPCI
- 26_CB1394-R5C593 (1)
- 27_CB1394-R5C593 (2)
- 28_PCMCIA SOCKET
- 29_IDE-HDD
- 30_IDE-ODD
- 31_KBC-M38857
- 32_SIO-ITE8705 & FW
- 33_LPT PORT & IR
- 34_DISCHARGE CIRCUIT
- 35_CODEC-ALC650
- 36_AUDIO AMP
- 37_MIC
- 38_MDC & RJ45 & RJ11
- 39_USB
- 40_FAN & AUDIO DJ
- 41_FUNCTION KEY
- 42_PWR & RESET SEQ
- 43_VCORE
- 44_1.25V&1.8V
- 45_2.5V&1.5V&1.2V&1.05V
- 46_SYSTEM
- 47_LOAD SWITCH
- 48_CHARGER
- 49_PIC16C54
- 50_BATLOW/SD#
- 51_VGACORE
- 52_SCREW HOLE & EMI CAP
- 53_M/B SETTING
- 54_REVISION HISTORY

System work voltage
 Adapter in : 19.5 ~18.5 V
 Battery in : 16.8 ~ 11.6V

+V1.25S : JP4,5 page 39
 +V2.5 : JP6 page 40
 +V1.2S : JP7 page 40
 +VCCP : JP9 page 40
 +V5S : JP13 page 42
 +V5 : JP14 page 42
 +V1.5SUS : JP15 page 39
 +V1.8 : JP16,19 page 39
 +V1.8S : JP17 page42
 +V12 : JP18 page 42
 +V1.5S : JP22 page 40
 +V5A : JP24 page 40
 +V3.3A : JP26 or 27 page 39
 +V3.3S : JP28 page 42
 +V3.3 : JP29 page 42

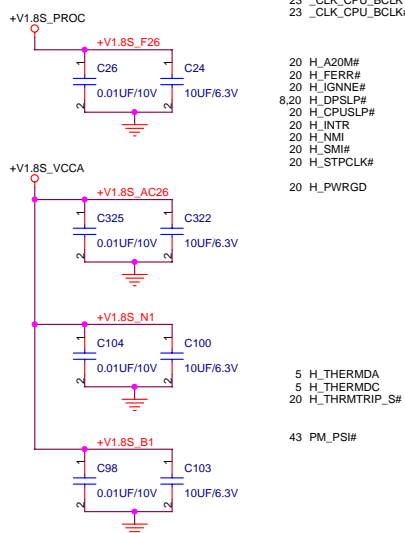


ADDR GROUP 0 -> L1
 ADDR GROUP 1 -> L4
 SPACE >= 1:2
 STROBE SPACE >= 1:2
 GROUP SPACE >= 20 mils
 LENGTH: 0.5" - 6.5"

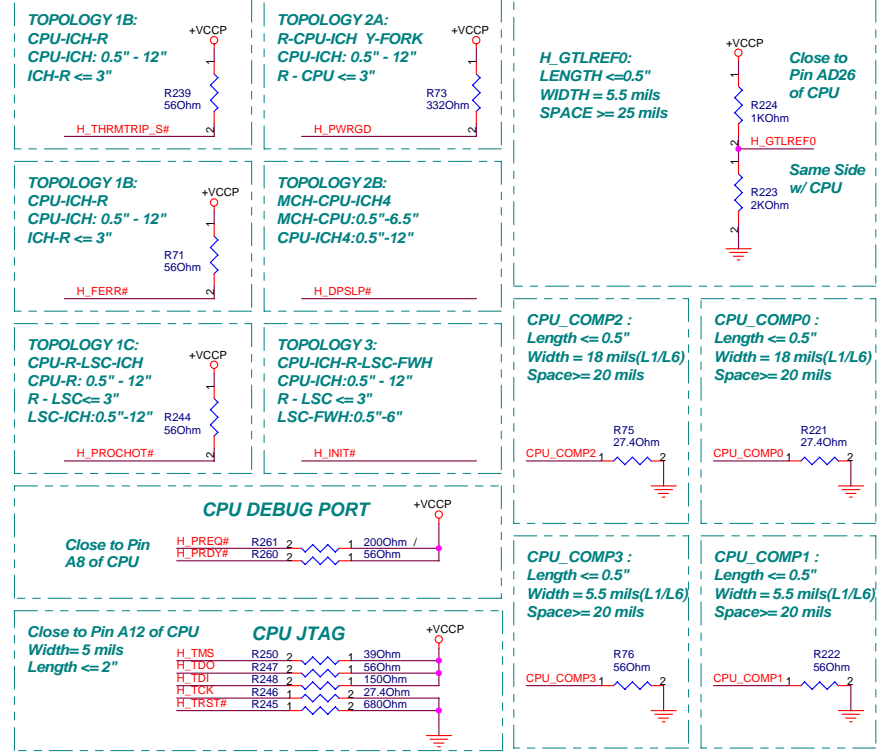
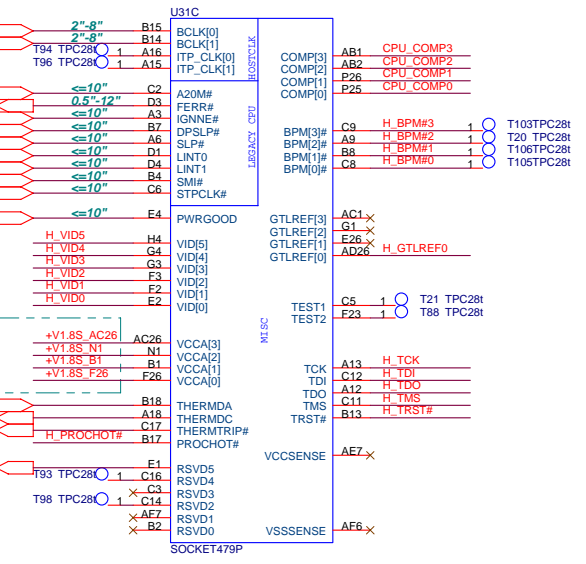
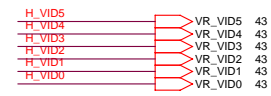
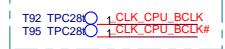
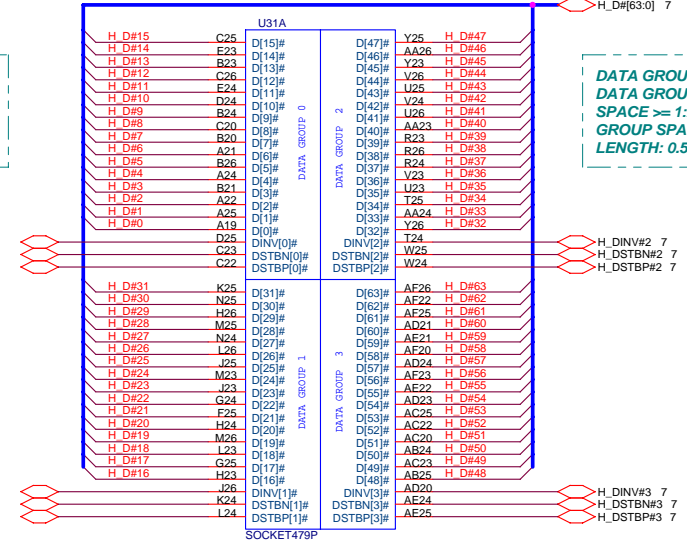
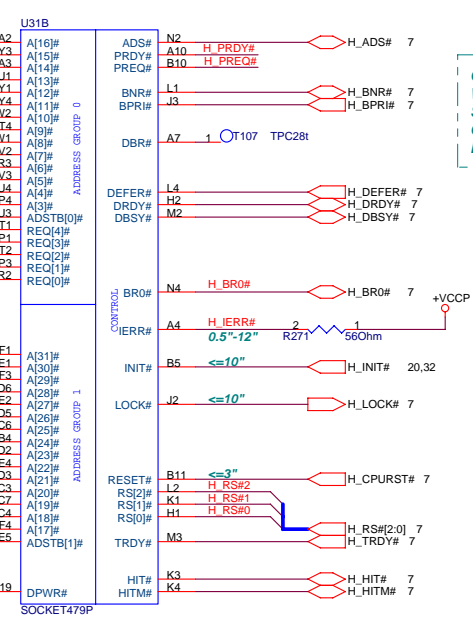
COMMON CLOCK -> L4
 WIDTH: 4.5 mils
 SPACE >= 1:2
 GROUP SPACE >= 20 mils
 LENGTH: 2.2" - 6.5"

DATA GROUP 0,2 -> L1
 DATA GROUP 1,3 -> L4
 SPACE >= 1:2
 GROUP SPACE >= 20 mils
 LENGTH: 0.5" - 5.5"

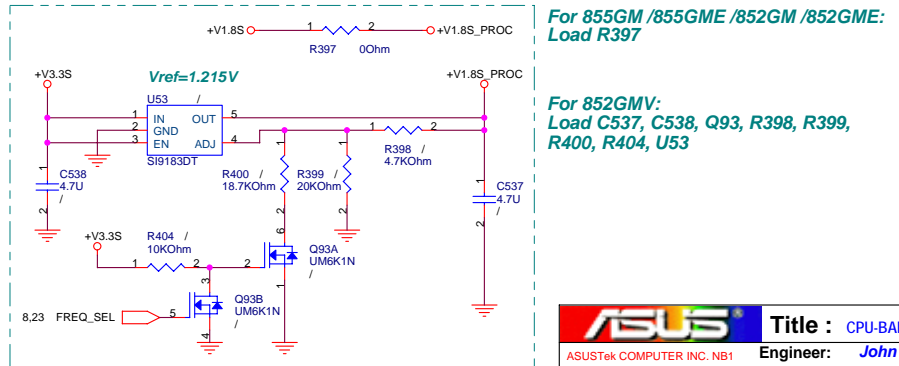
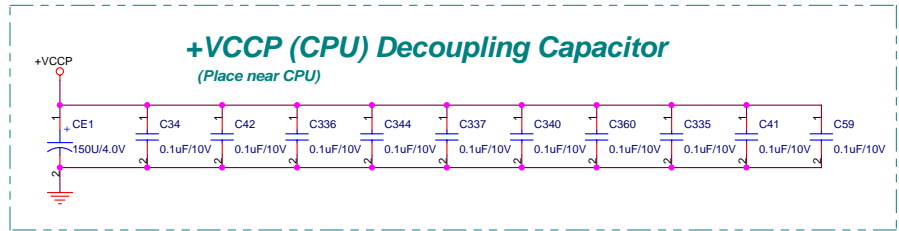
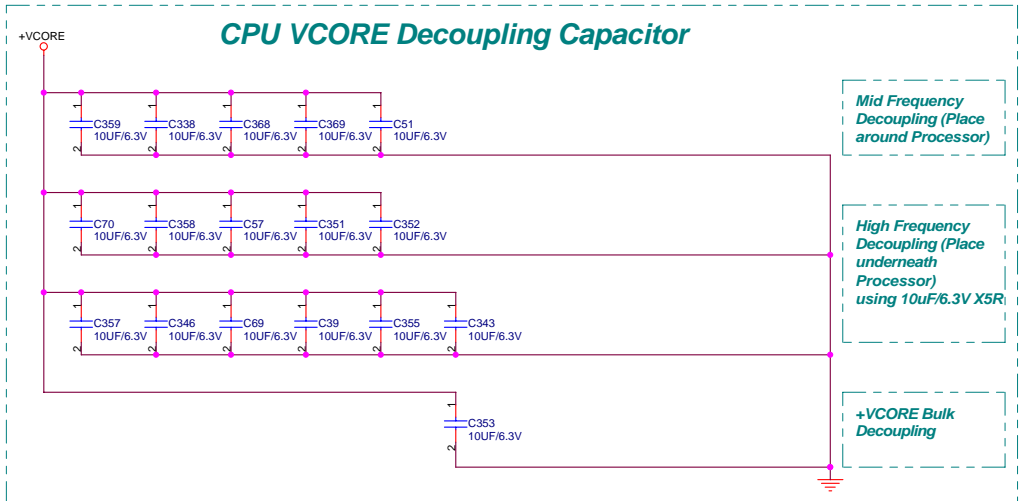
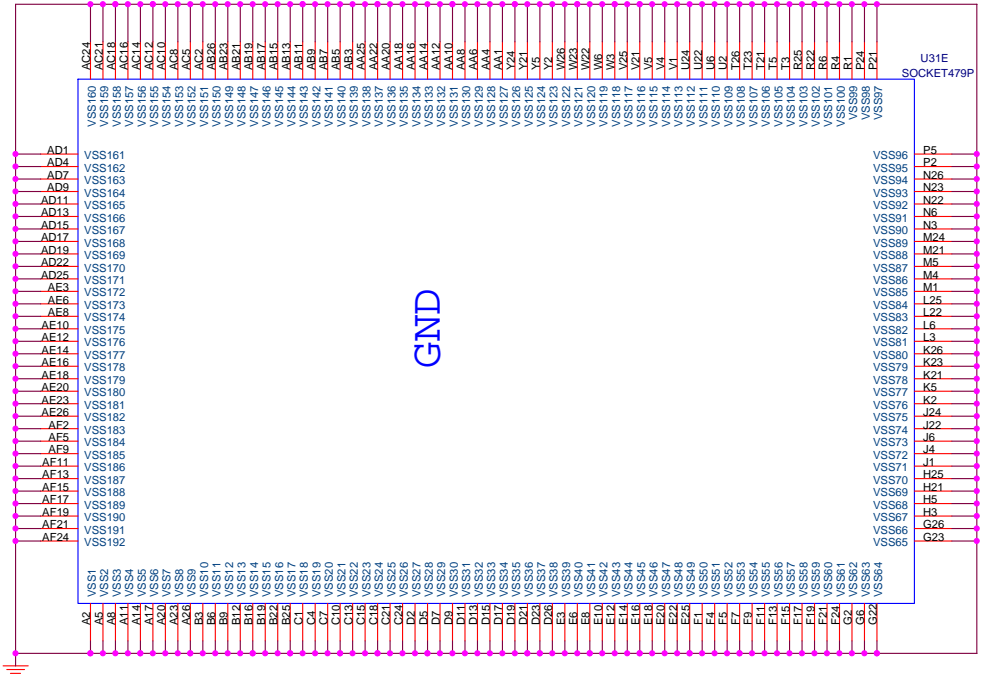
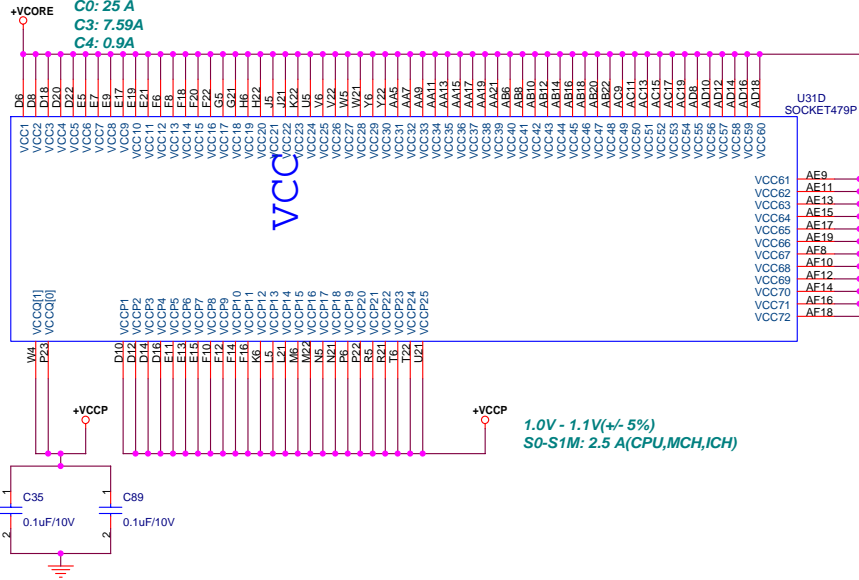
CPU PLL CIRCUITS
 1.71V - 1.89V(+/- 5%)
 SO-S1M: 0.3A



	Celeron	Banias	Dothan (400)	Dothan (533)
Frequency	100	100	100	133
VCCA[1:3]	1.8V	1.8V	1.8V	NC
VCCA[0]	1.8V	1.8V	1.8V	1.5V
U54 switch to	Pin 3,4			Pin 1,2



HFM(1.3GHz-1.7GHz): 1.468V
 LFM(600MHz): 0.956V
 0.745V - 1.356V(+/- 1.5%)
 C0: 25 A
 C3: 7.59A
 C4: 0.9A



M3N : Four 200 uF are located in IMPV4
 A3N : Delete 10uF/6.3V from 35pcs to 17pcs

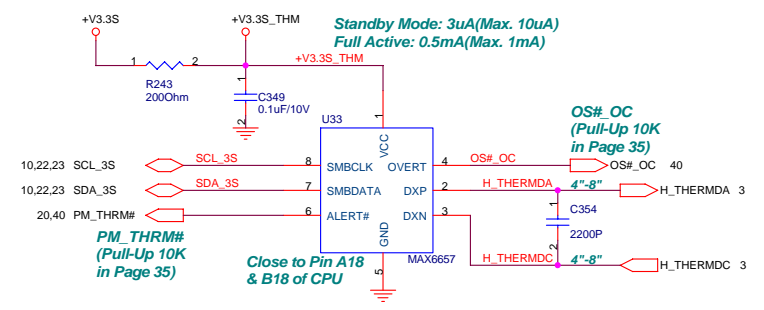
For 855GM /855GME /852GM /852GME:
 Load R397

For 852GMV:
 Load C537, C538, Q93, R398, R399,
 R400, R404, U53

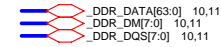
Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
 12 mils
 =====GND
 10 mils
 =====H_THERMDA(10 mils)
 10 mils
 =====H_THERMDC(10 mils)
 10 mils
 =====GND
 12 mils
 -----OTHER SIGNALS

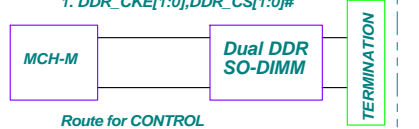
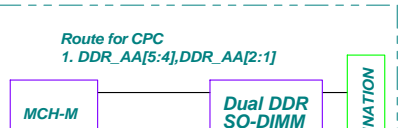
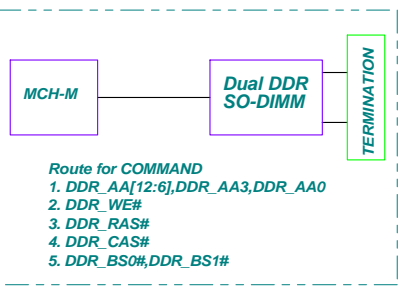
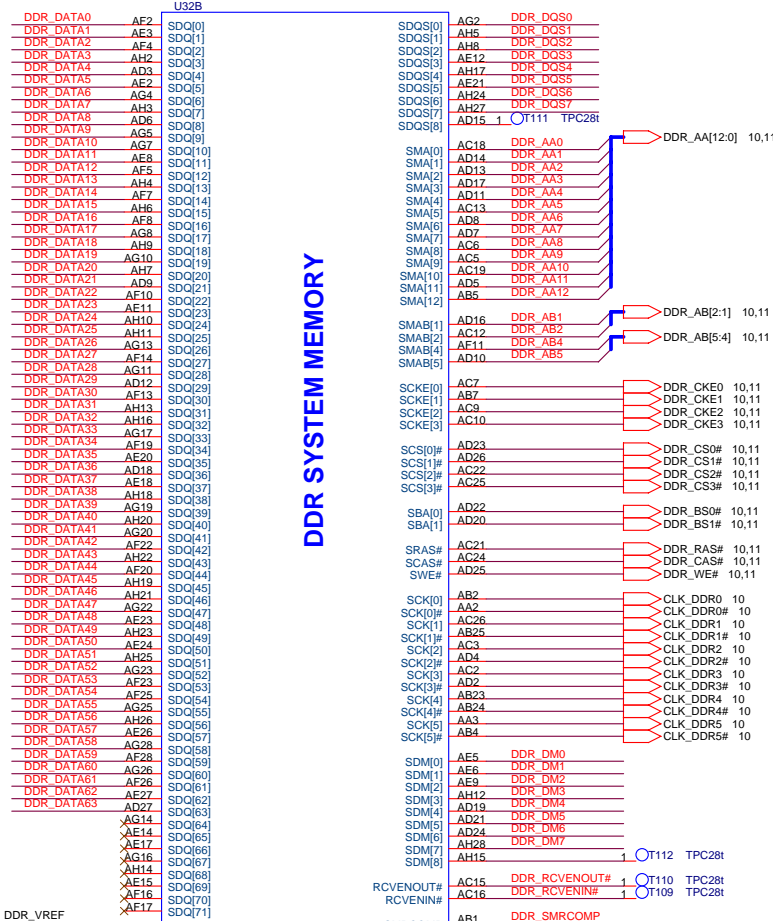
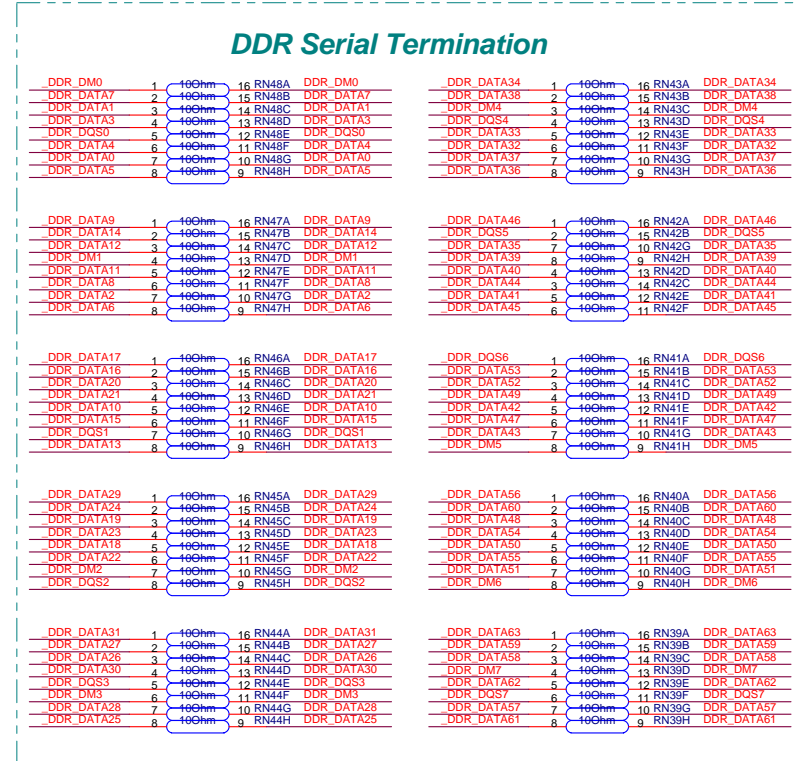
Avoid BPSB,Power



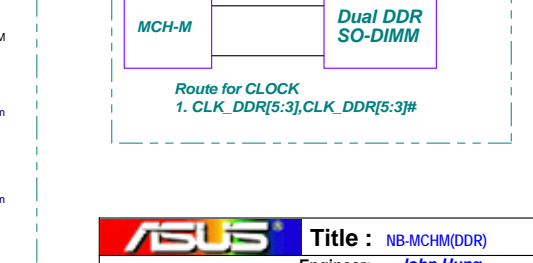
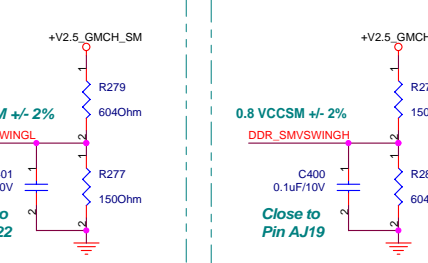
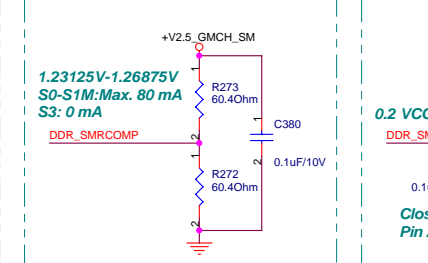
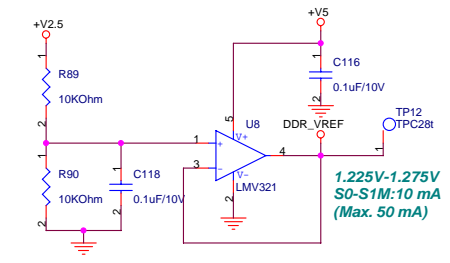
Thermal Power: ~ 3.8W
LxWxH=37.5x37.5x2.58



(MCH-Sighting041)
M-GM system memory interface generates single pulse CKE events which may cause intermittent hangs and display corruptions when using Micron and Infineon SO-DIMMs.



Intel suggested that DDR_VREF should be turned off in S3-S5. But measure the leakage because there is no +V2.5S.

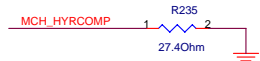


MCH_COMP Signals

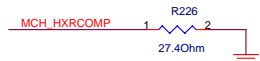
MCH_HLZCOMP :
Length <= 0.5"
Width = 18 mils(L1/L6)
Space >= 20 mils

MCH_HLZCOMP

MCH_HYRCOMP :
Length <= 0.5"
Width = 18 mils(L1/L6)
Space >= 20 mils

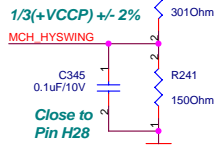


MCH_HXRCOMP :
Length <= 0.5"
Width = 18 mils(L1/L6)
Space >= 20 mils

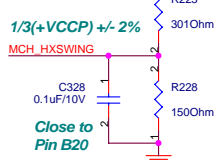


MCH_SWING Signals

MCH_HYSWING :
Length <= 0.5"
Width = 18 mils
Space >= 20 mils



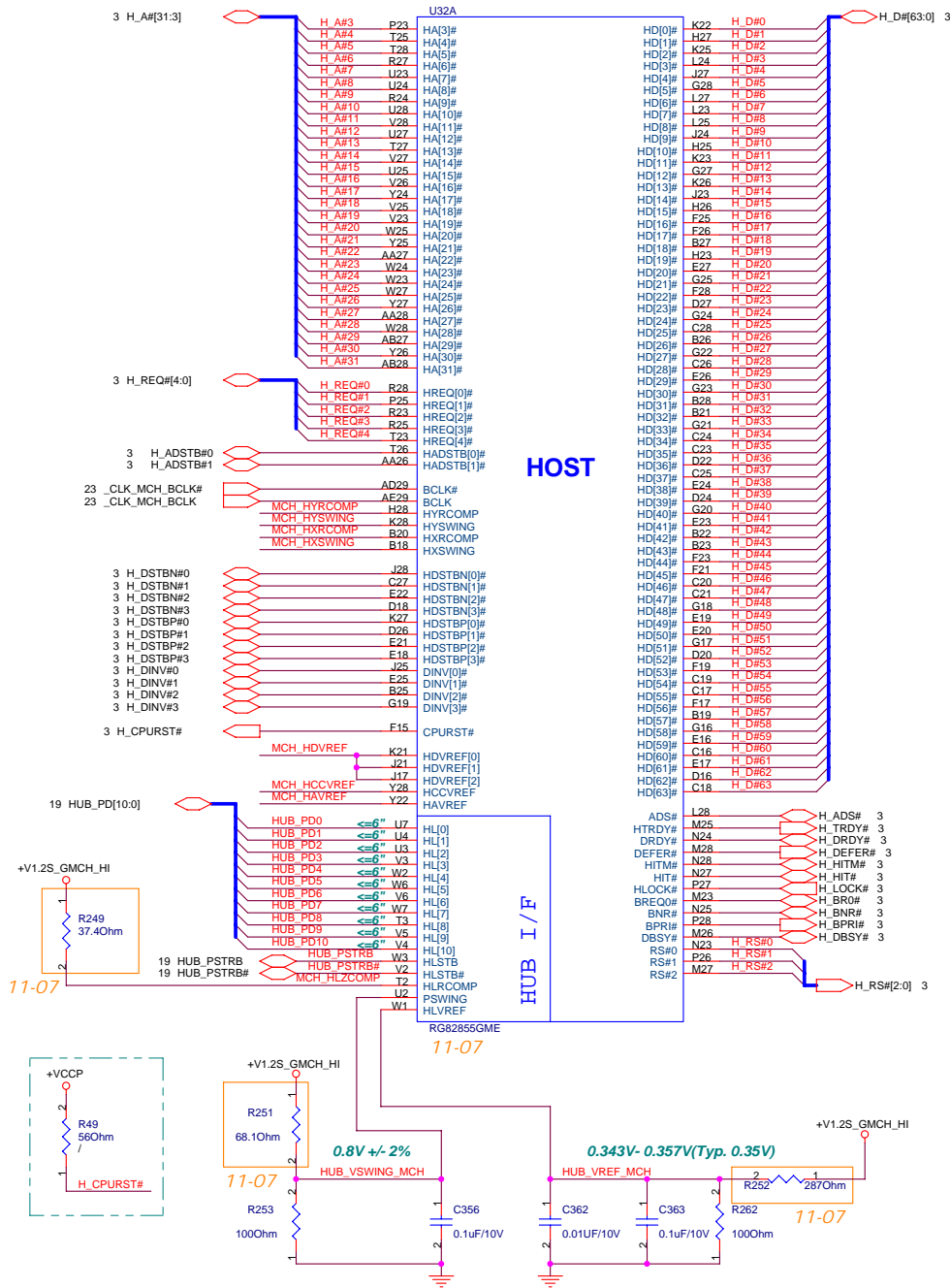
MCH_HXSWING :
Length <= 0.5"
Width = 18 mils
Space >= 20 mils



R249:
27.4 ohm (10-003412704) for 855GM/852GM
37.4 ohm (10-003413704) for 855GME
48.7 ohm (10-003414807) for 852GME/852GMV

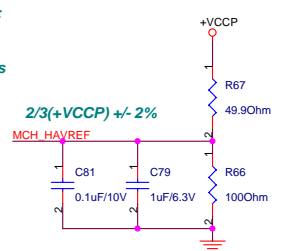
R251:
49.9 ohm (10-003414909) for 855GM/852GM
68.1 ohm (10-003416801) for 855GME
86.6 ohm (10-003418606) for 852GME/852GMV

R252:
240 ohm (10-003412410) for 855GM/852GM
287 ohm (10-003412817) for 855GME
324 ohm (10-003413214) for 852GME/852GMV

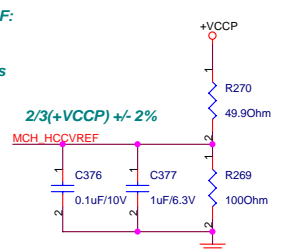


MCH_VREF Signals

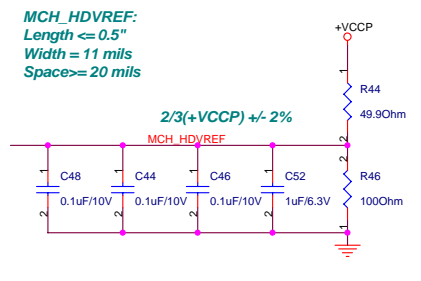
MCH_HAVREF:
Length <= 0.5"
Width = 11 mils
Space >= 20 mils



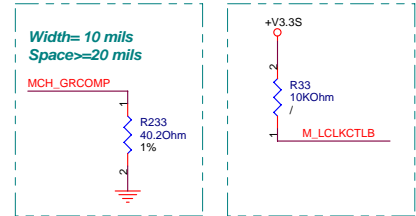
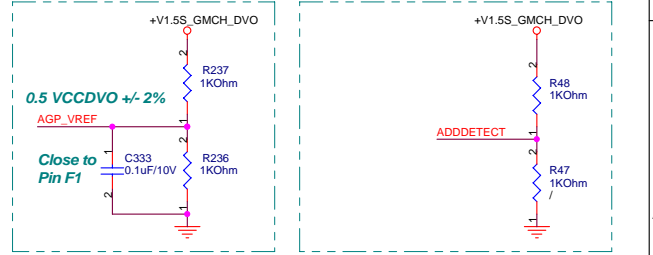
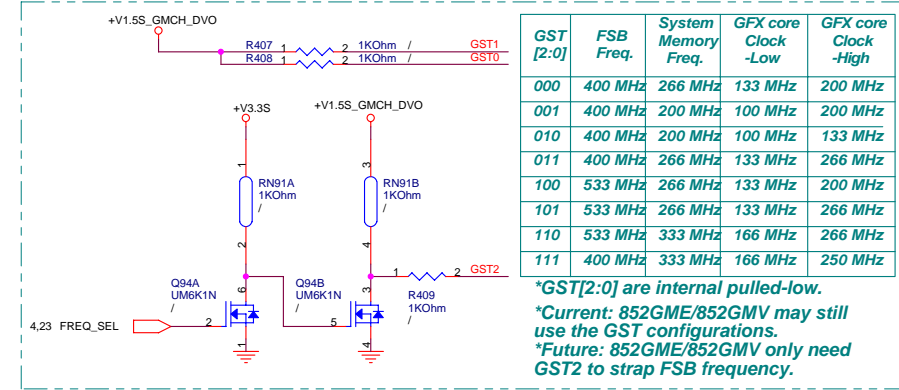
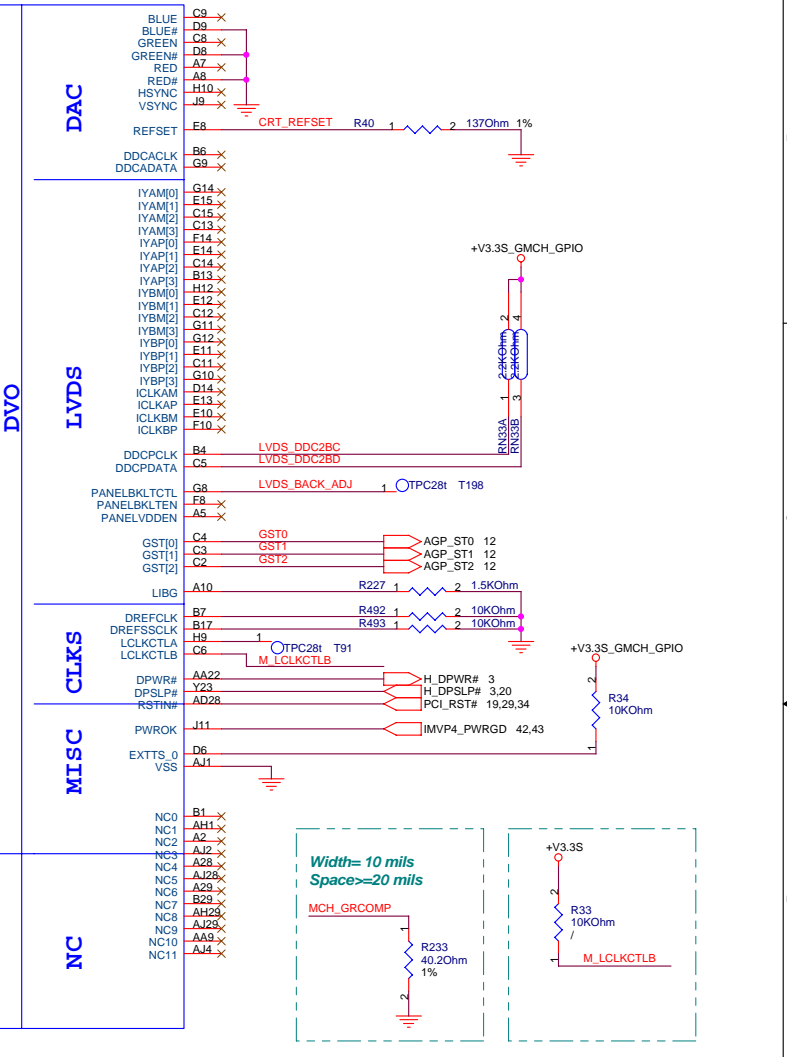
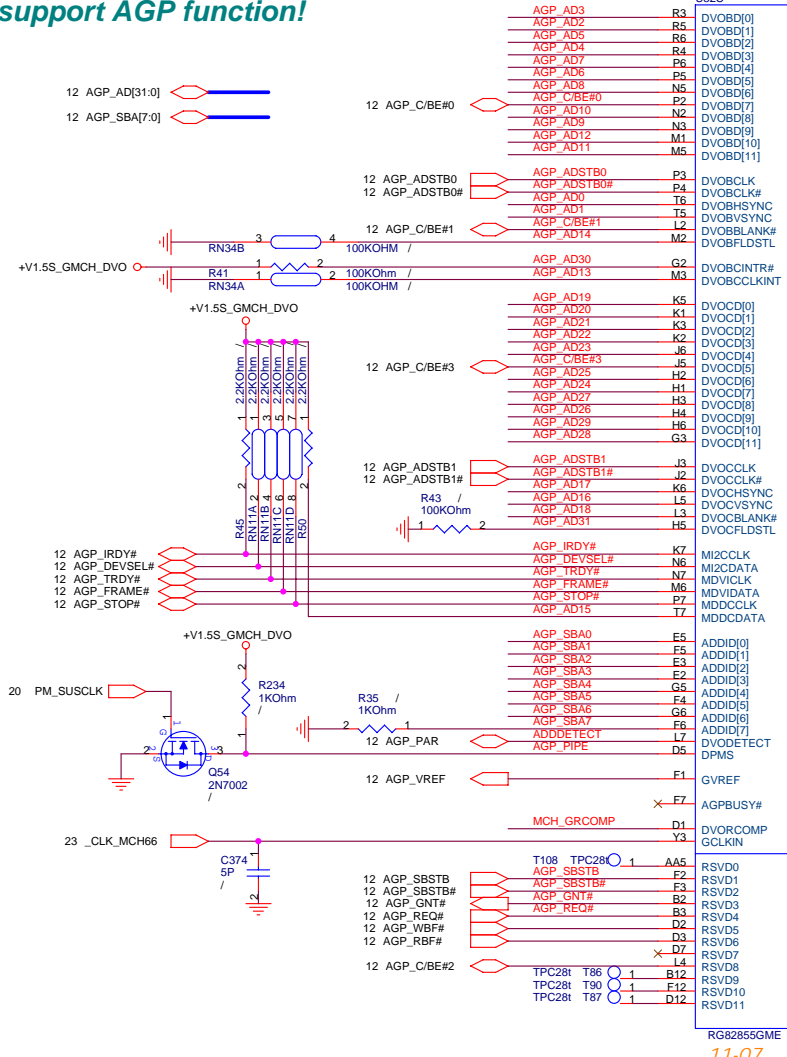
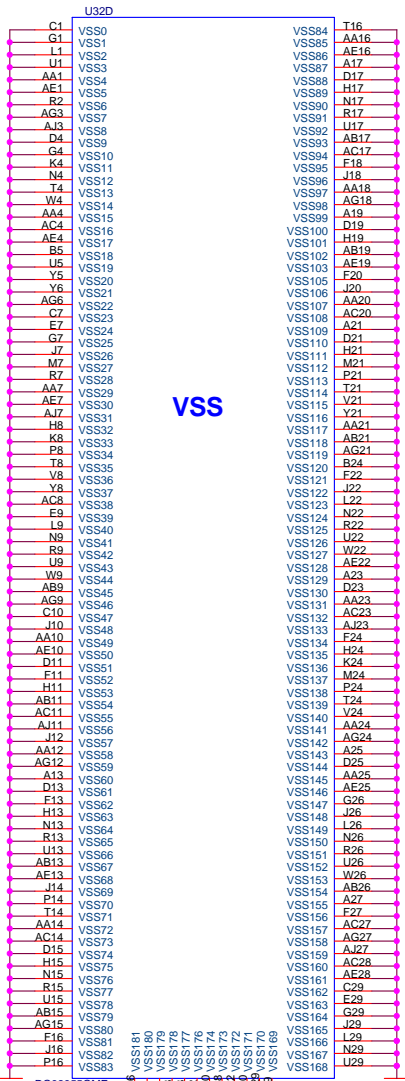
MCH_HCCVREF:
Length <= 0.5"
Width = 10 mils
Space >= 20 mils

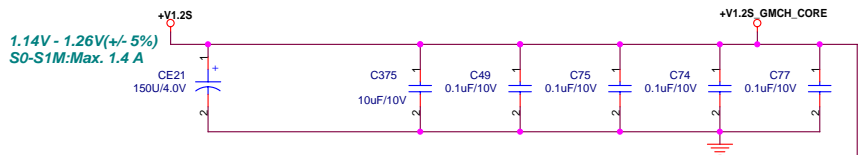


MCH_HDVREF:
Length <= 0.5"
Width = 11 mils
Space >= 20 mils

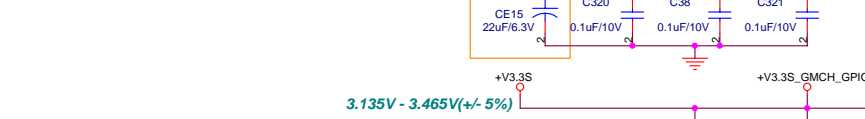
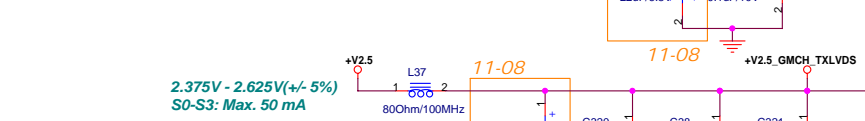
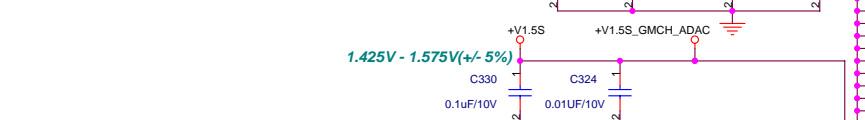
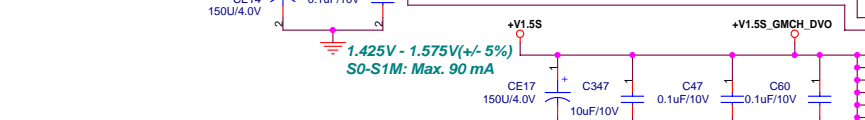
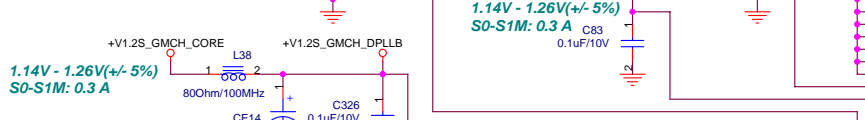
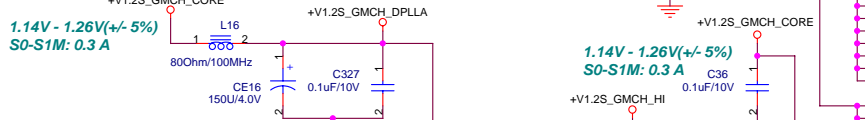
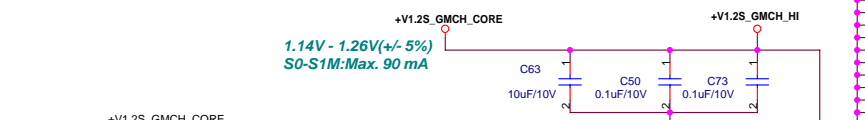


Only 855GME & 852GME can support AGP function!





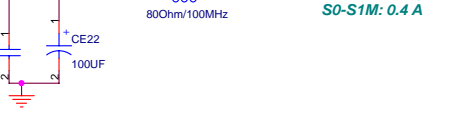
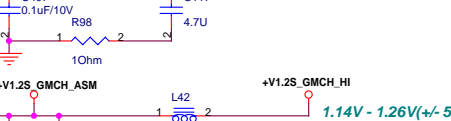
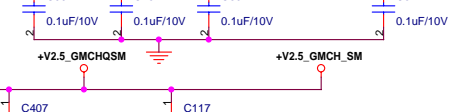
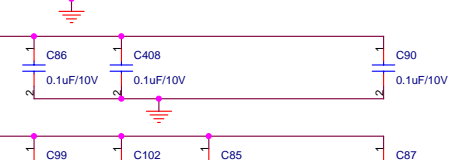
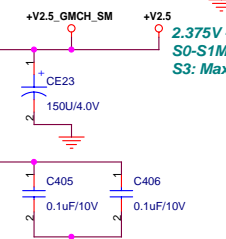
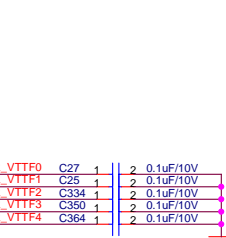
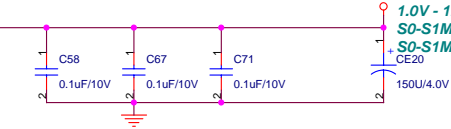
(MCH-Sighting041)
The core supply (1.2V) should be powered up a minimum of 1ms before the DVO and GPIO IO (1.5V and 3.3V) voltage rails.



J15	VCC0
P13	VTTLF0
T13	VCC1
NH4	VCC2
R14	VCC3
U14	VCC4
P15	VCC5
T15	VCC6
AA15	VCC7
N15	VCC8
R16	VCC9
U16	VCC10
P17	VCC11
AA17	VCC12
AA19	VCC13
W21	VCC14
H14	VCC15
	VCC16
	VCC17
V1	VCCHL0
Y1	VCCHL1
W5	VCCHL2
U8	VCCHL3
W8	VCCHL4
V7	VCCHL5
V9	VCCHL6
	VCCHL7
D29	VCCAPLL
Y2	VCCAGPLL
A6	VCCADPLLA
B16	VCCADPLLB
E1	VCCDVO_0
J1	VCCDVO_1
N1	VCCDVO_2
E4	VCCDVO_3
J4	VCCDVO_4
M4	VCCDVO_5
E6	VCCDVO_6
H7	VCCDVO_7
J8	VCCDVO_8
L8	VCCDVO_9
M8	VCCDVO_10
N8	VCCDVO_11
R8	VCCDVO_12
K8	VCCDVO_13
M9	VCCDVO_14
P9	VCCDVO_15
A9	VCCADAC0
B9	VCCADAC1
B8	VSSADAC
A11	VCCALVDS
B11	VSSALVDS
G13	VCCDLVDS0
B14	VCCDLVDS1
J13	VCCDLVDS2
B15	VCCDLVDS3
F9	VCCTXLVDS0
B10	VCCTXLVDS1
D10	VCCTXLVDS2
A12	VCCTXLVDS3
A3	VCCGPIO_0
A4	VCCGPIO_1

POWER

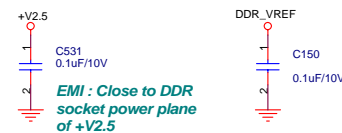
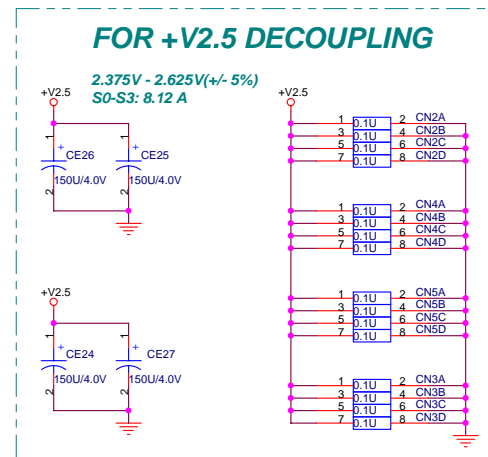
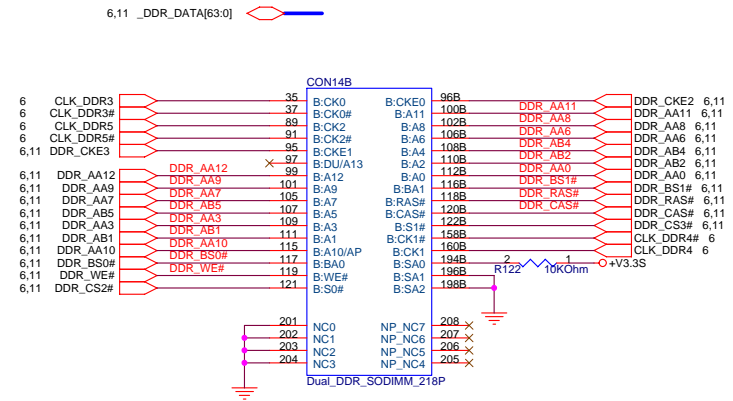
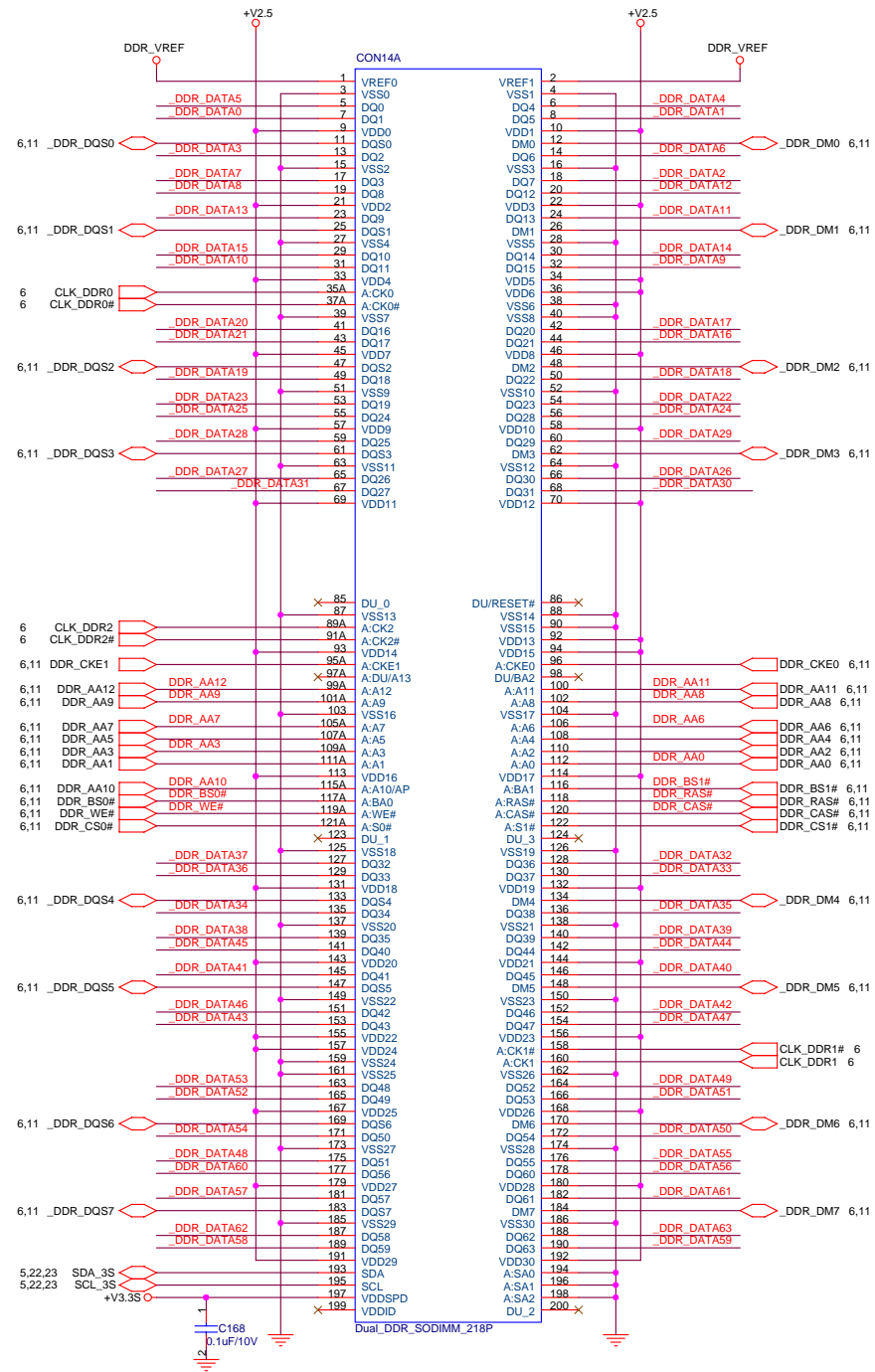
G15	VTTLF0
H16	VTTLF1
H18	VTTLF2
H19	VTTLF3
H20	VTTLF4
L21	VTTLF5
N21	VTTLF6
R21	VTTLF7
U21	VTTLF8
H22	VTTLF9
M22	VTTLF10
P22	VTTLF11
T22	VTTLF12
Y22	VTTLF13
K29	VTTLF14
F29	VTTLF15
AB29	VTTLF16
A26	VTTLF17
A20	VTTLF18
A18	VTTLF19
	VTTLF20



NB

VCC, VCCASM, VCCHL, VCCAGPLL, VCCADPLLA, VCCADPLLB:
855GM/852GM: 1.2V
855GME: 1.35V
852GME/852GMV: 1.5V

ASUS		Title : NB-MCHM(PWR)	
ASUSTek COMPUTER INC. NB1		Engineer: John Hung	
Size	Project Name	Rev	
Custom	A6G	1.1	
Date: Friday, October 15, 2004	Sheet 9	of 54	



6,10 _DDR_DATA[63:0]
 6,10 _DDR_DM[8:0]
 6,10 _DDR_DQS[8:0]
 6,10 DDR_AA[12:0]
 6,10 DDR_AB[2:1]
 6,10 DDR_AB[5:4]

DDR TERMINATION

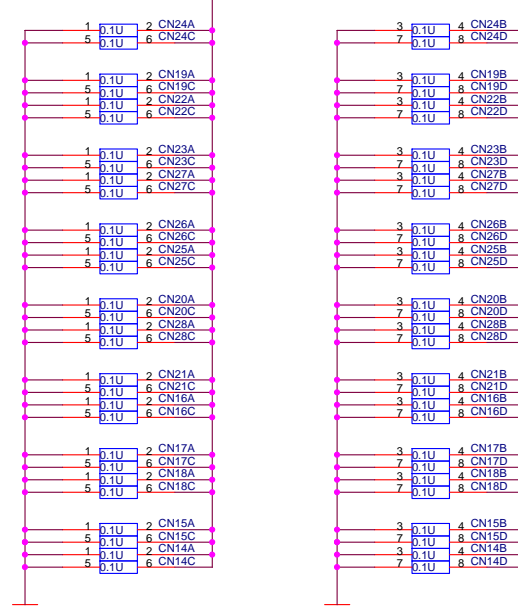
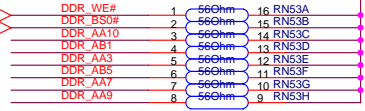
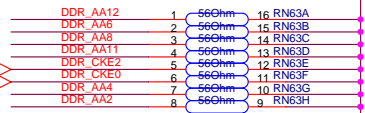
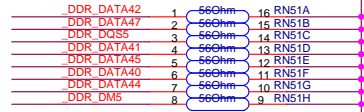
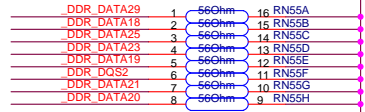
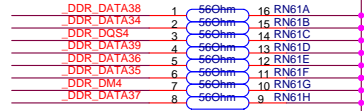
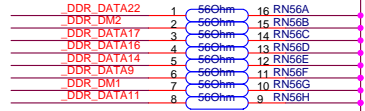
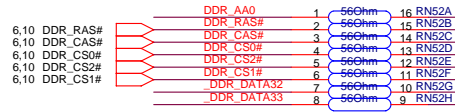
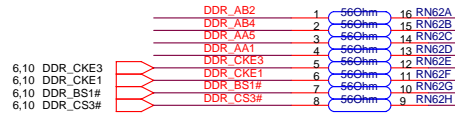
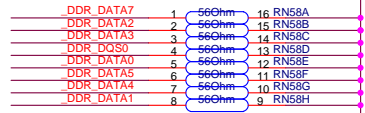
FOR +V1.25S DECOUPLING

+V1.25S

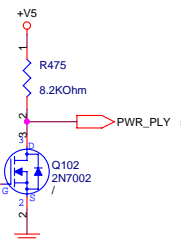
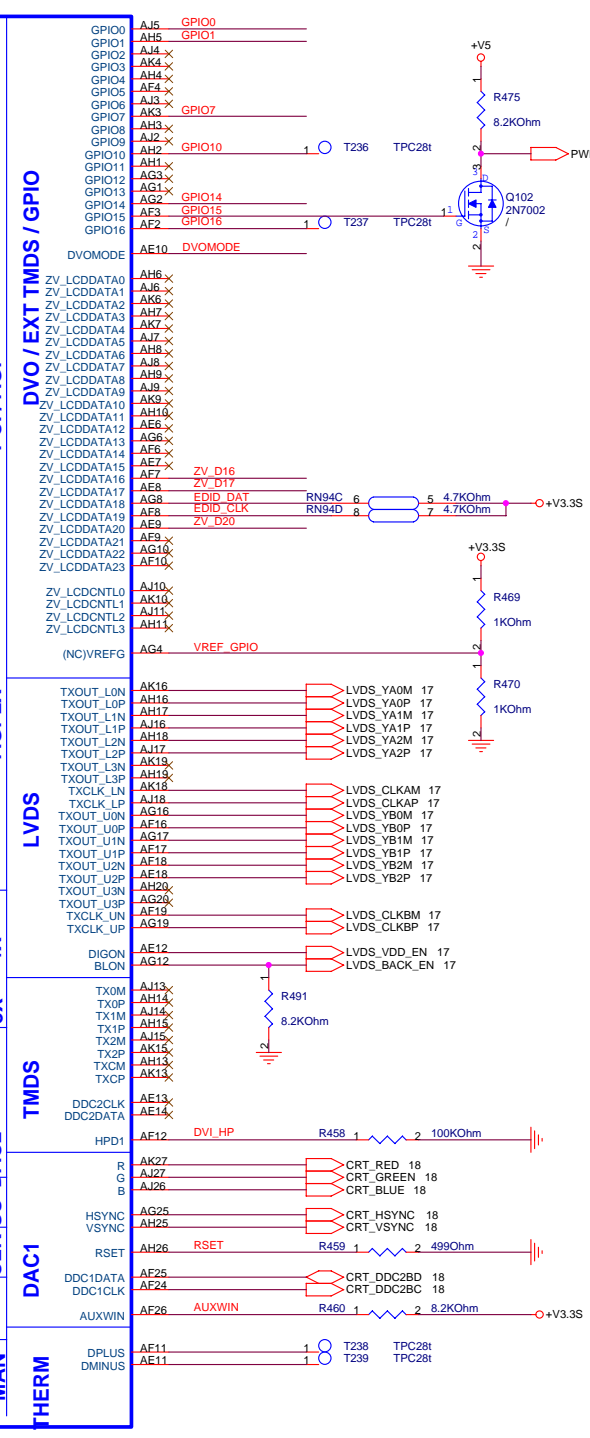
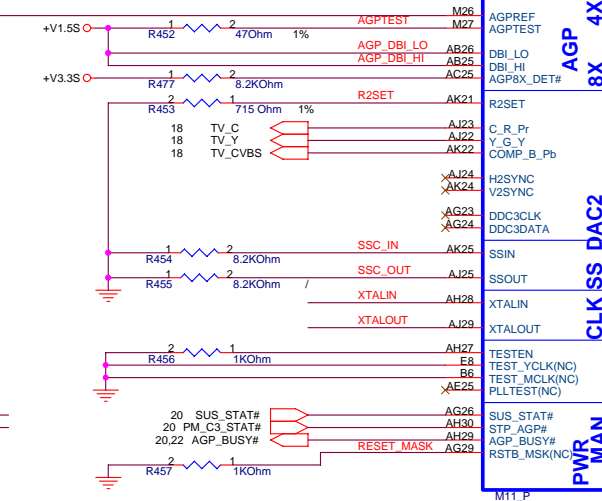
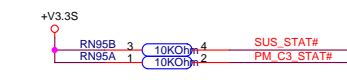
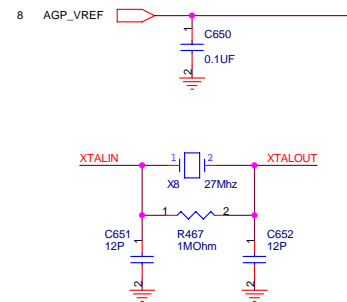
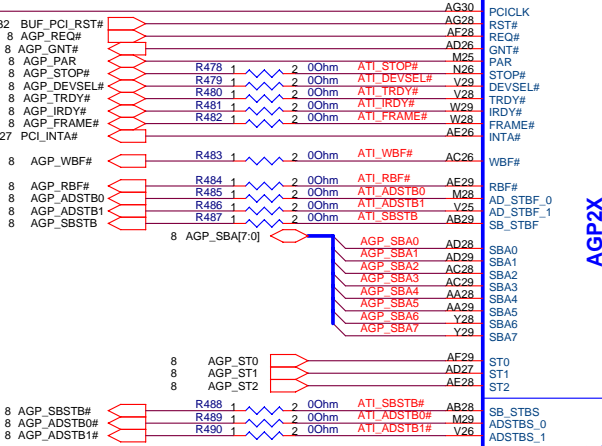
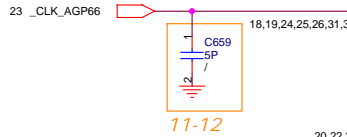
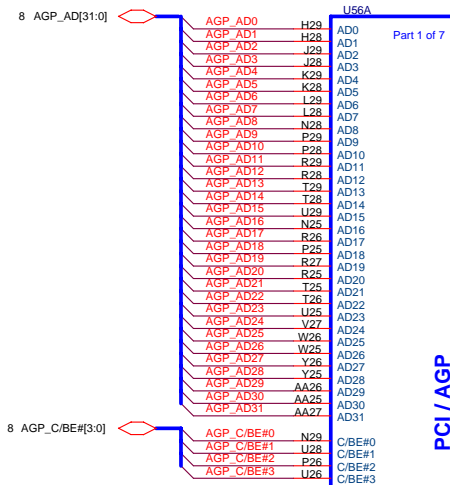
+V1.25S

+V1.25S

+V1.25S



A6G uses M11-CL as external AGP Graphics.
 (M11-CL and M11-P are pin-to-pin compatible!)

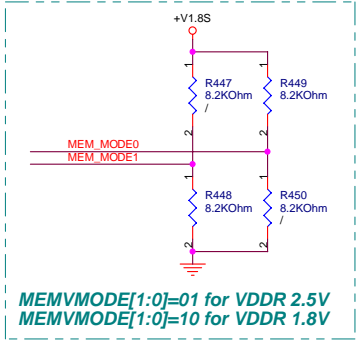
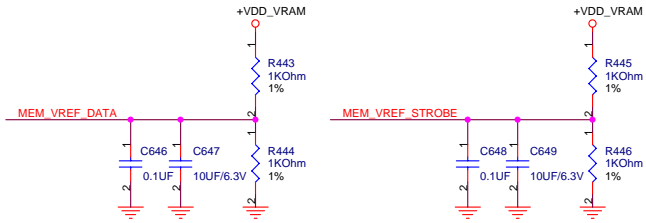
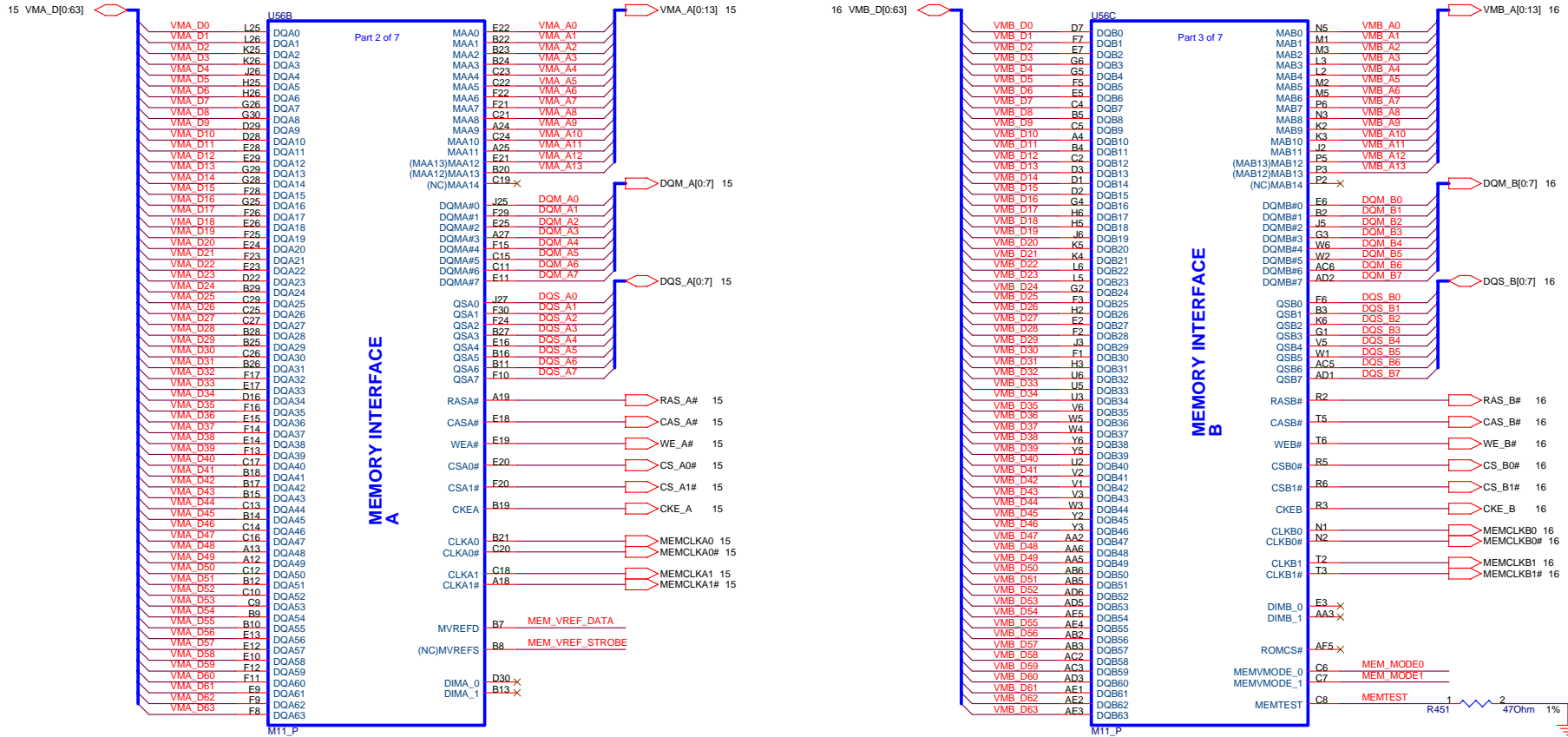


- Strap Option**
- GPIO[1,0] = [1,1] : REFCLK 2 TAPS EARLIER THAN FEEDBACK
- GPIO[3,2] = [0,0] : X1CLK & X2CLK ALIGNED
- GPIO[6,5,4] = [0,0,0] & AGP8X_DET#=1: 1.5V, AGP4X, AD16
- GPIO[8] = 0 : NORMAL OPERATION
- GPIO[9,13,12,11] = [0,0,0,0] : NO EXT ROM
- DVOMODE = 0 : 3.3V ZV SIGNAL
- ZV_LCDDATA[17,16] = [0,0] : SINGLE FUNCTION DEVICE
- ZV_LCDDATA[20] = 1 : NO SLAVE VIP HOST

- Use GPIO to choose VRAM type**
- GPIO[7] = 0 : Samsung 4M*32 VRAM
- RESERVE GPIO10 FOR OTHER USE

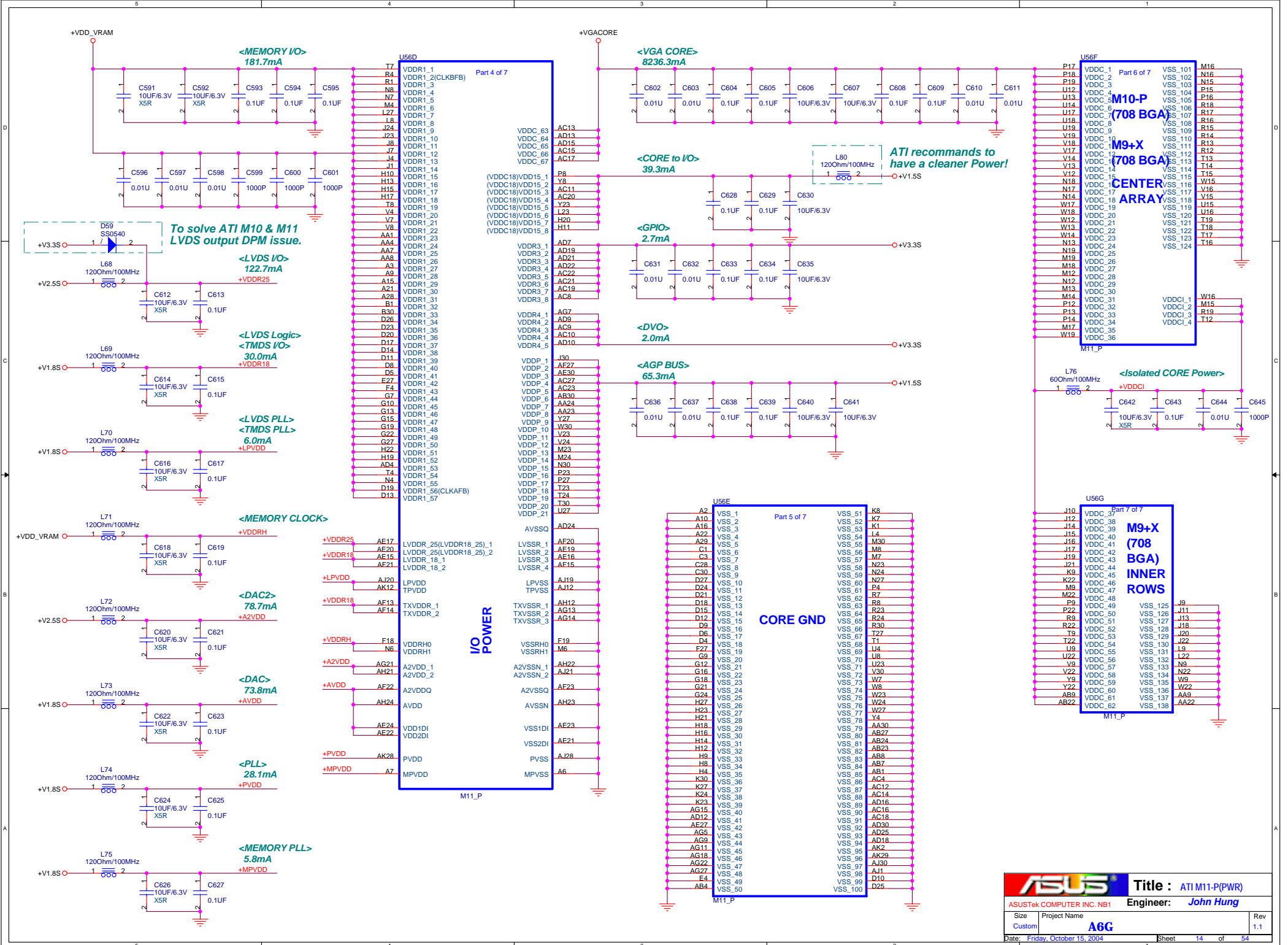
To A CHANNEL VRAM

To B CHANNEL VRAM



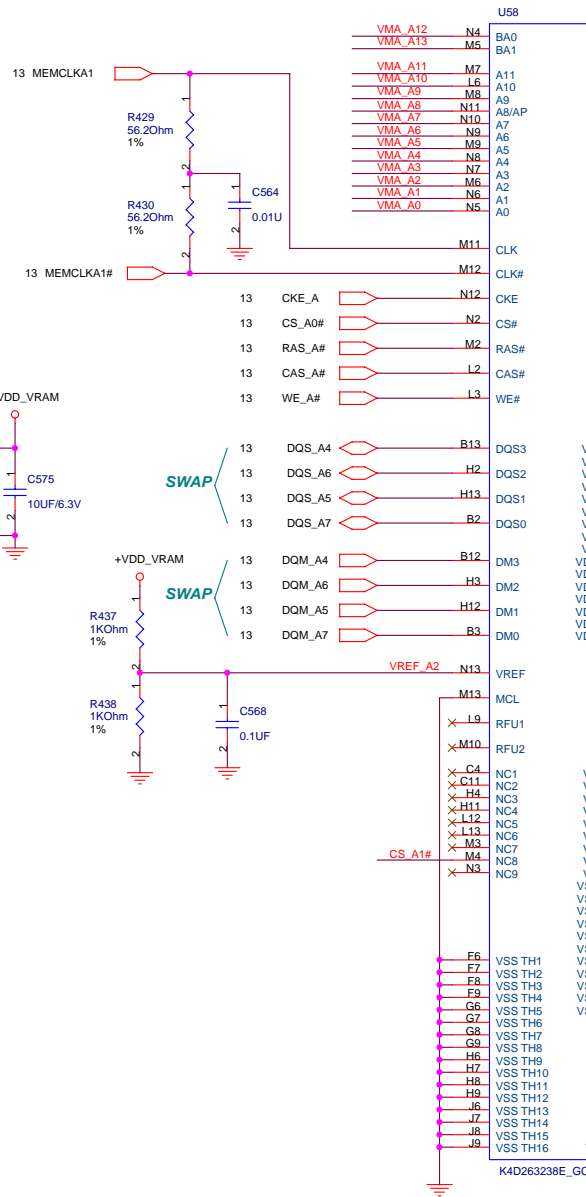
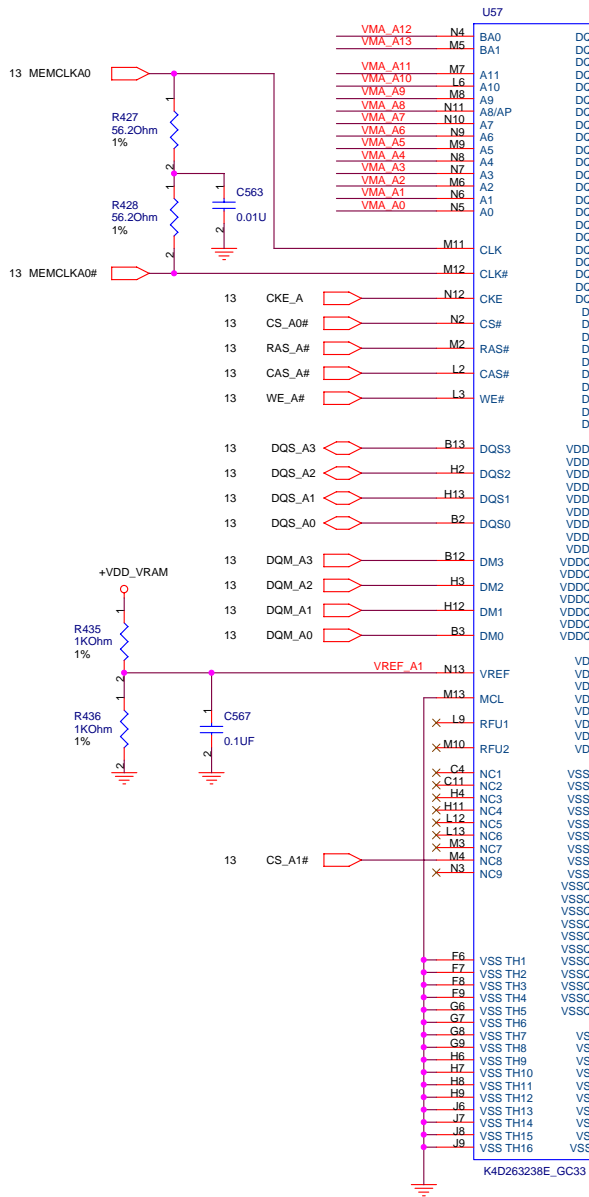
MEMVMODE[1:0]=01 for VDDR 2.5V
MEMVMODE[1:0]=10 for VDDR 1.8V

ASUS Title : ATI M11-P(MEMORY IF)
 ASUSTek COMPUTER INC. NB1 Engineer: John Hung
 Size Project Name
 Custom A6G Rev 1.1
 Date: Friday, October 15, 2004 Sheet 13 of 54



13 VMA_A[13:0]

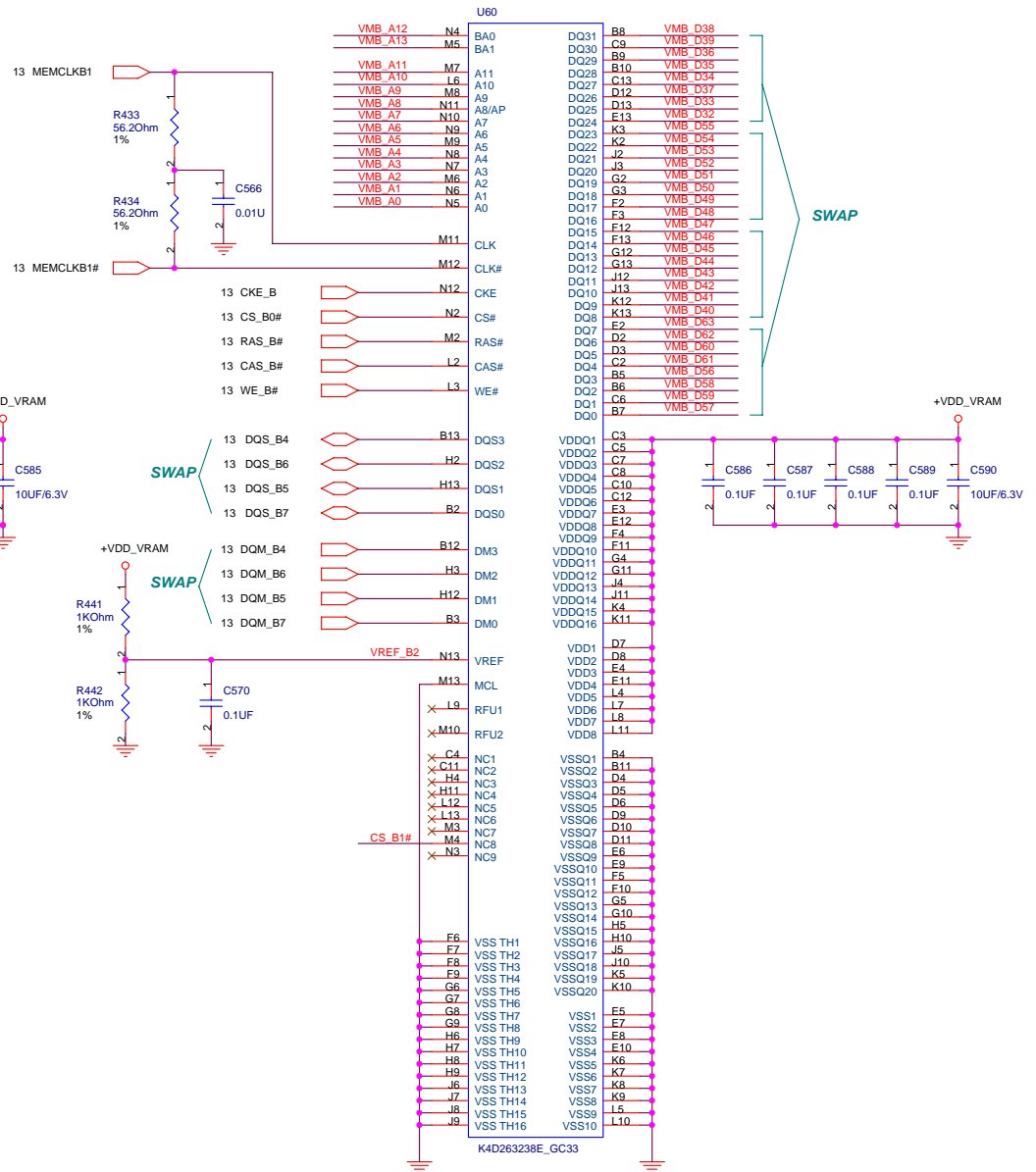
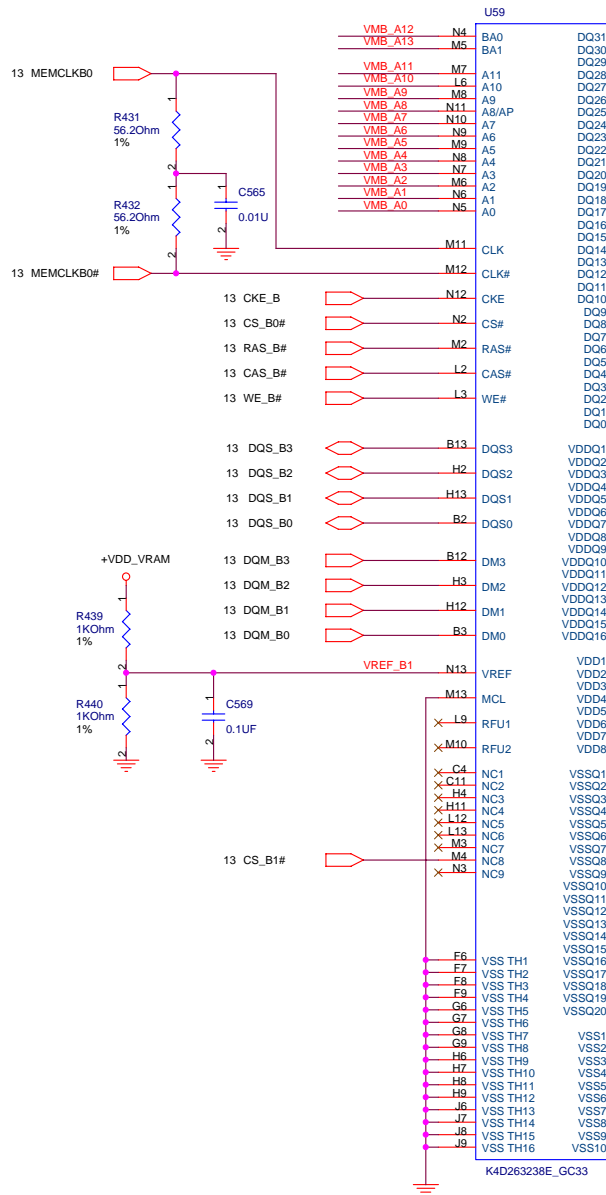
13 VMA_D[0:63]



13 VMB_A[13:0]

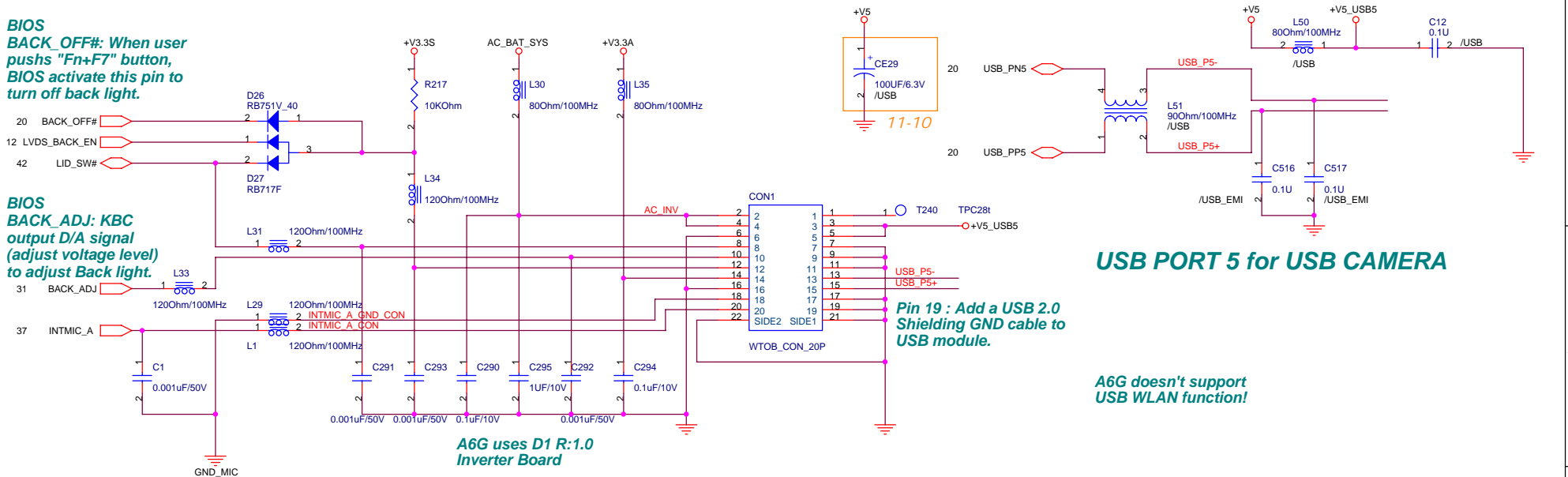
13 VMB_D[0:63]

B_D[0:63]

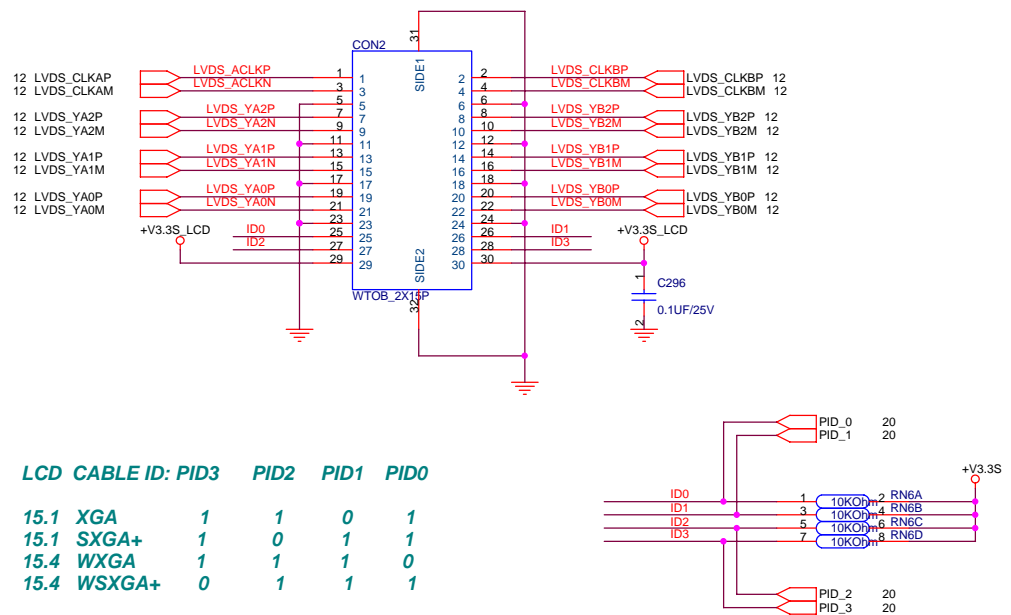


**BIOS
BACK_OFF#:** When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.

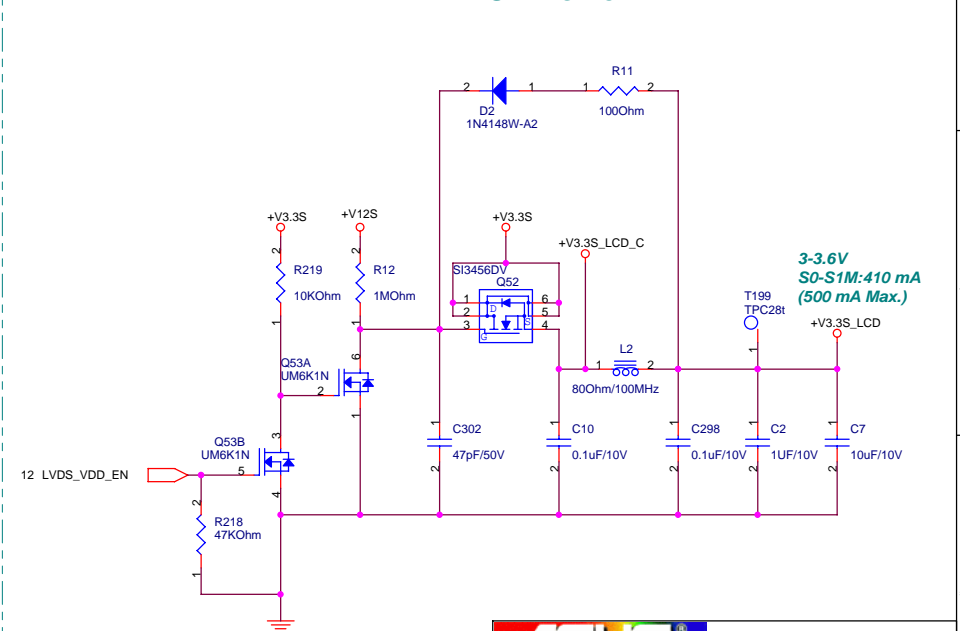
**BIOS
BACK_ADJ:** KBC output D/A signal (adjust voltage level) to adjust Back light.

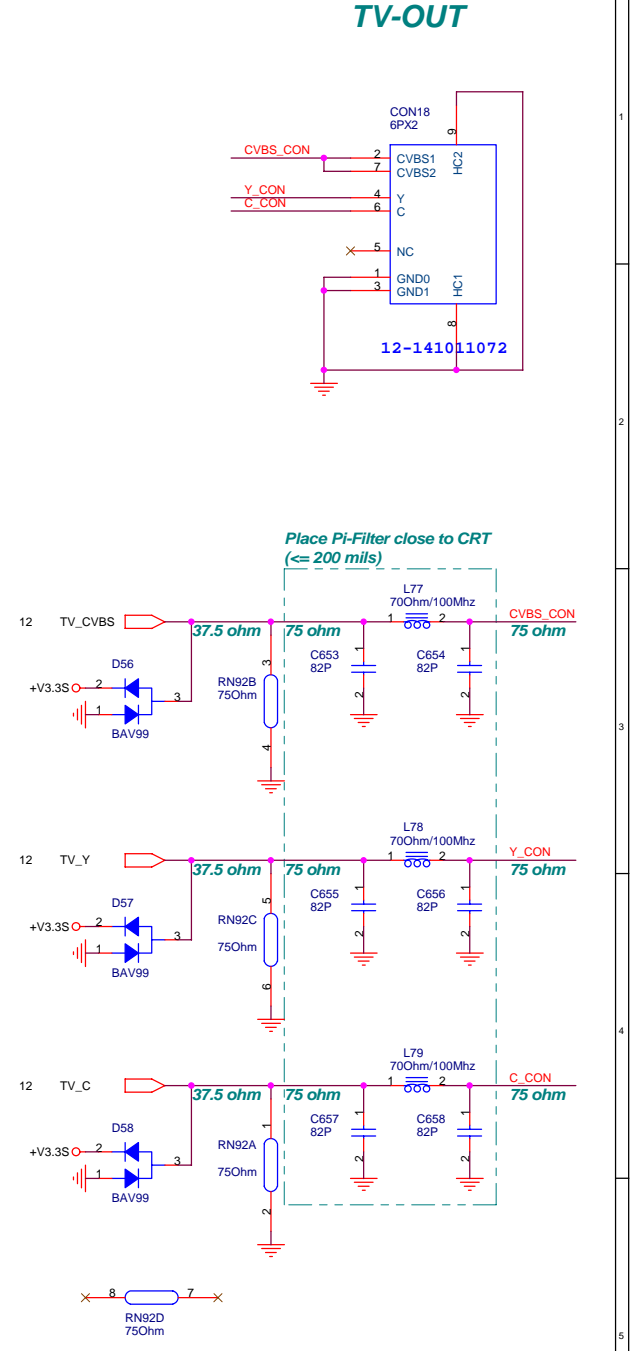
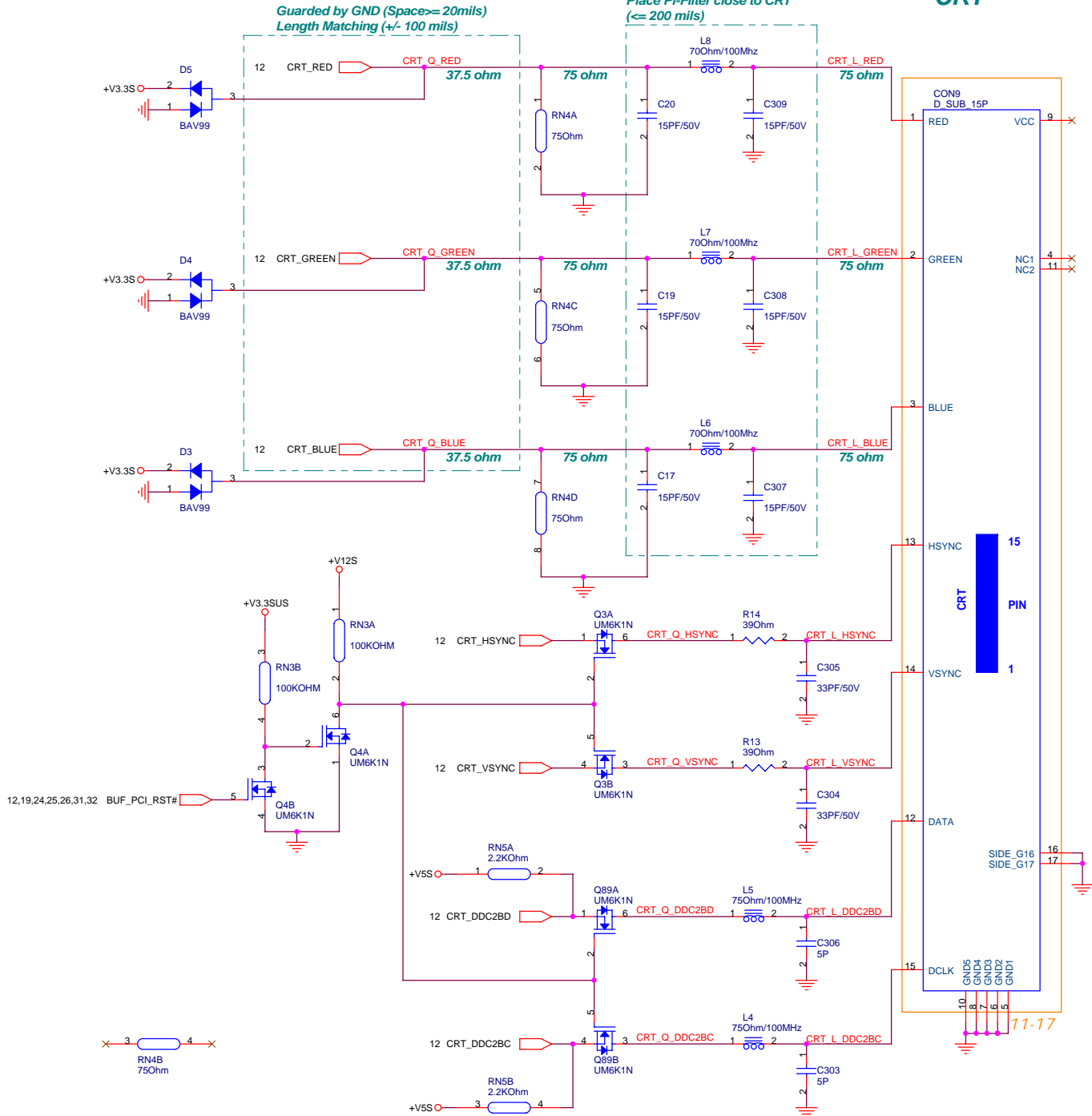


USB PORT 5 for USB CAMERA

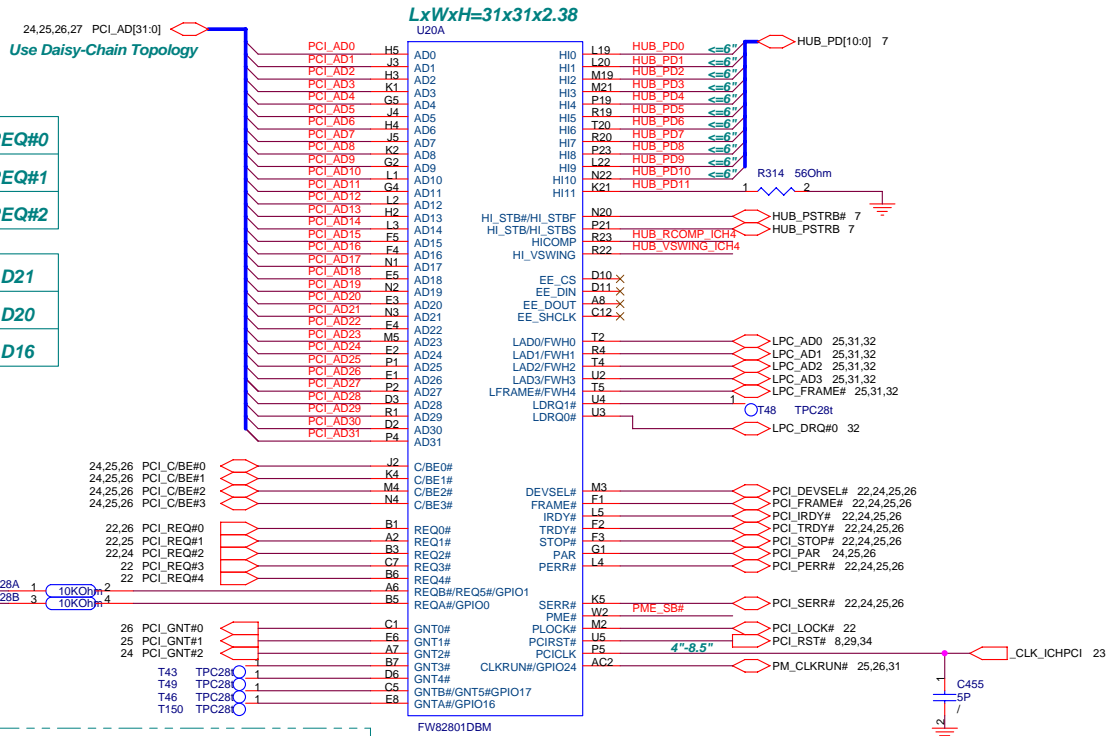


LCD Power





ASUS		Title : CRT & TV-OUT	
ASUSTek COMPUTER INC. NB1		Engineer: John Hung	
Size Custom	Project Name A6G	Rev 1.1	
Date: Friday, October 15, 2004		Sheet 18 of 54	

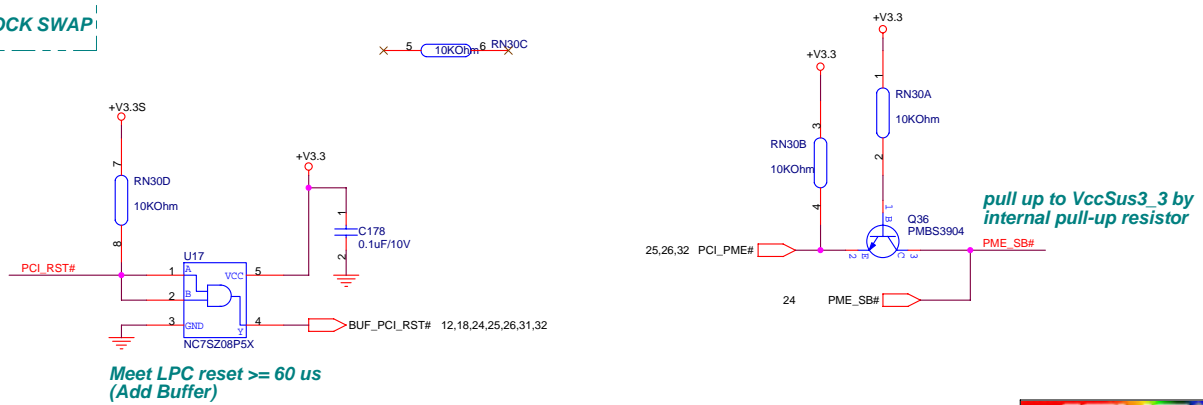
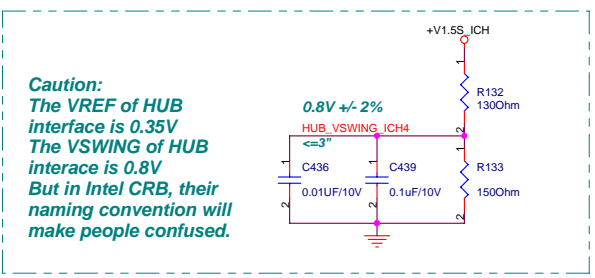
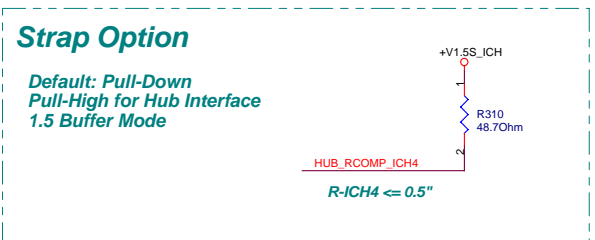


CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

Strap Option

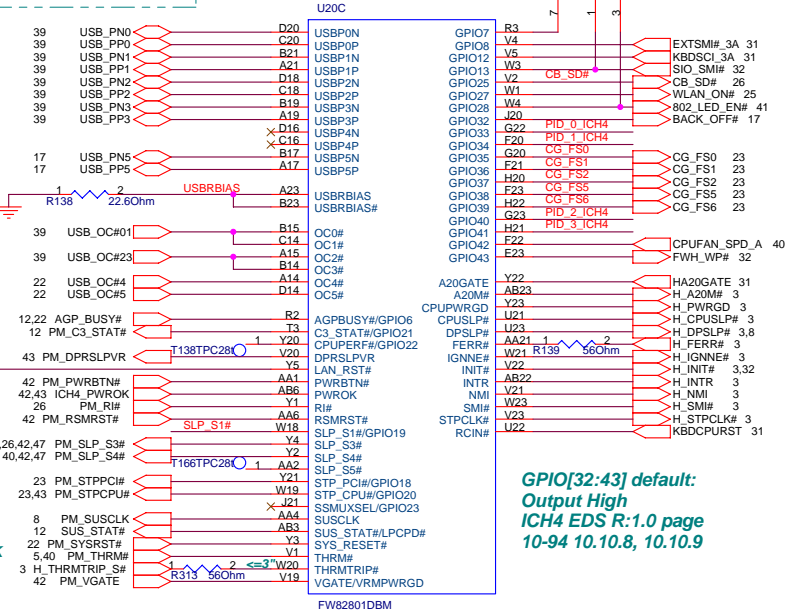
ICH4-M pin E8
Default: Pull-High 20K
Pull-Down for BIOS TOP-BLOCK SWAP



USB SIGNALS
 | USB+ - USB- | <= 50 mils
 Pair Width/Space: 5.5/5 mils (L1/L6)
 4.5/5 mils (L3/L4)
 Impedance: 90 ohm(differential)
 Other Signals Space: >= 20 mils
 Clock Signals Spac: >= 50 mils

USBRBIAS:
 W/S: 5/5 mils
 Length: <= 0.5"

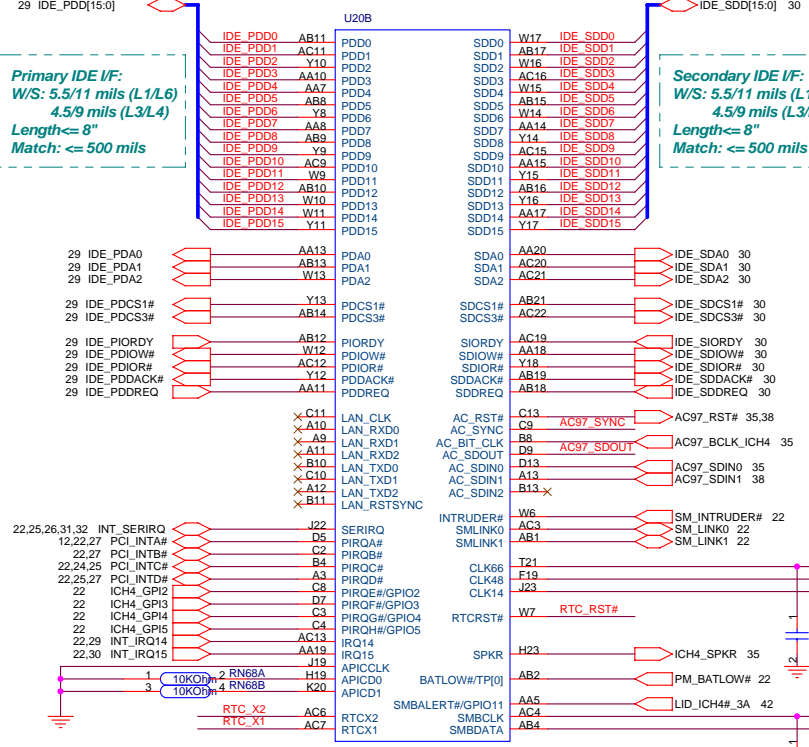
Measure duty-cycle of SUSCLK (Pin A44) must be in 30-70%



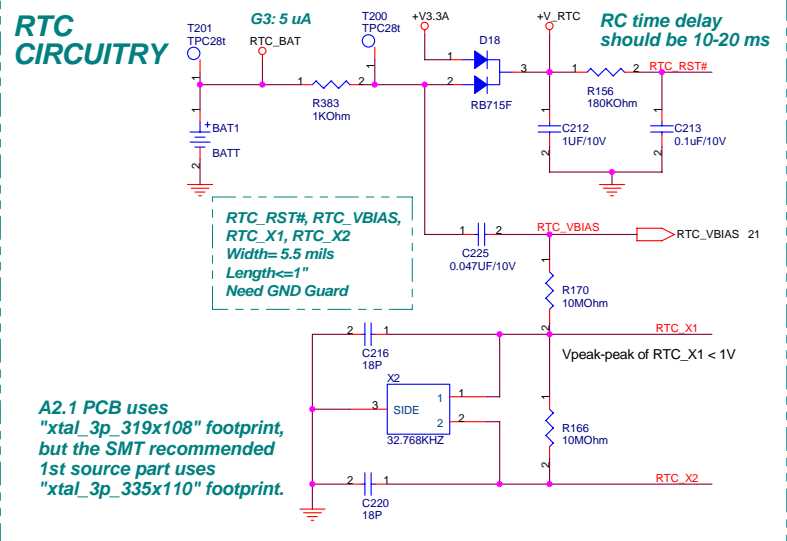
GPIO[32:43] default:
 Output High
 ICH4 EDS R:1.0 page 10-94 10.10.8, 10.10.9

Primary IDE I/F:
 W/S: 5.5/11 mils (L1/L6)
 4.5/9 mils (L3/L4)
 Length <= 8"
 Match: <= 500 mils

Secondary IDE I/F:
 W/S: 5.5/11 mils (L1/L6)
 4.5/9 mils (L3/L4)
 Length <= 8"
 Match: <= 500 mils



CODEC	AC97_SDIN0
MDC	AC97_SDIN1

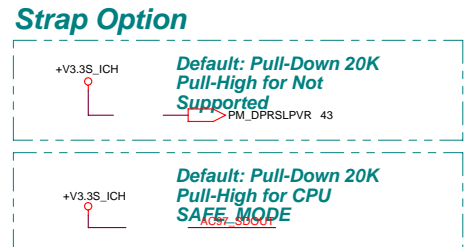
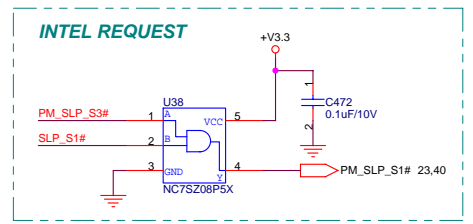
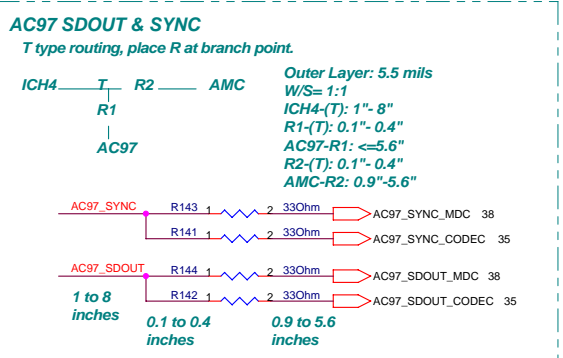
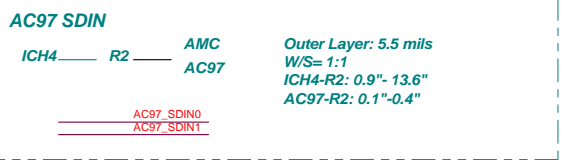


RTC CIRCUITRY

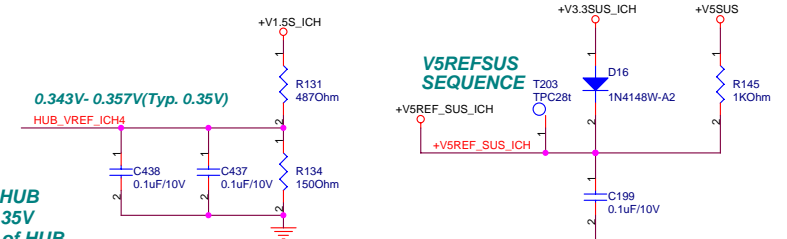
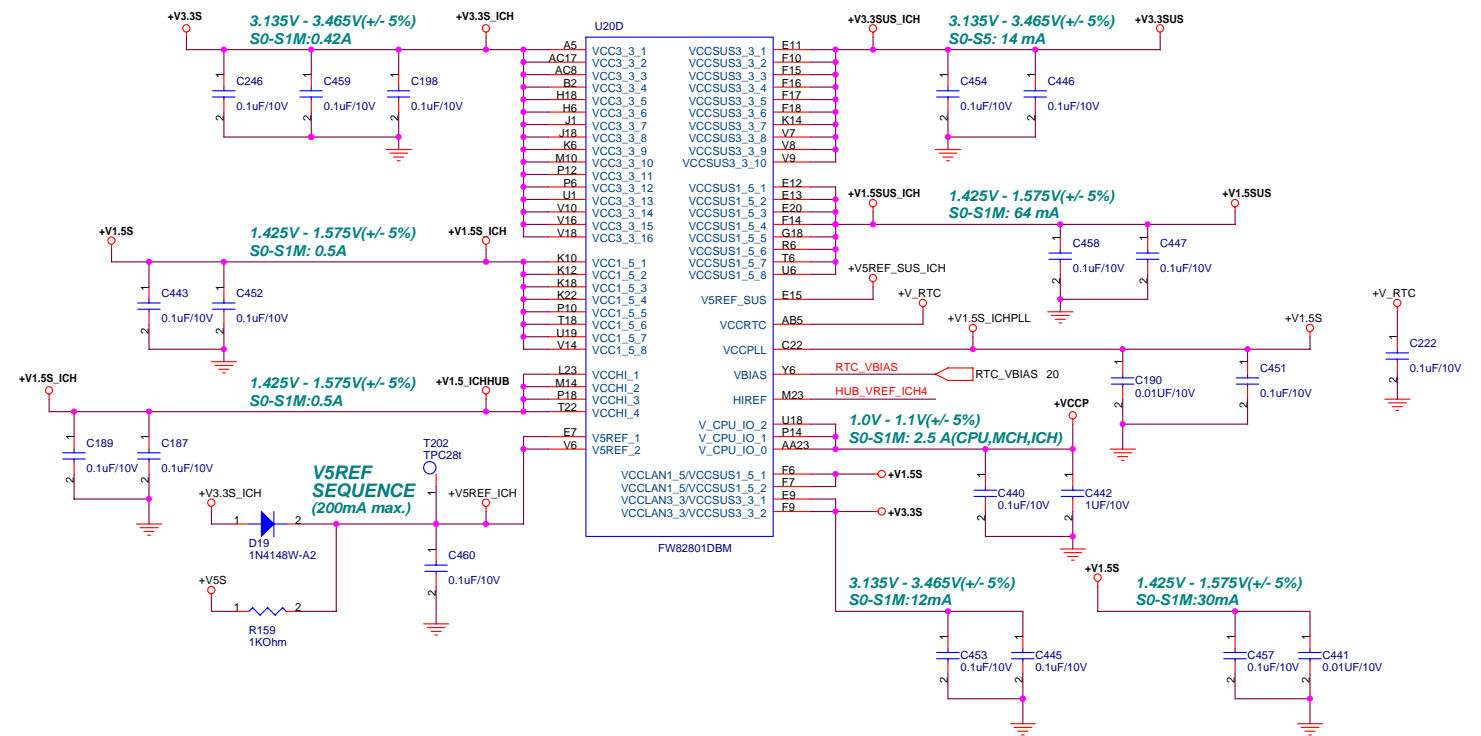
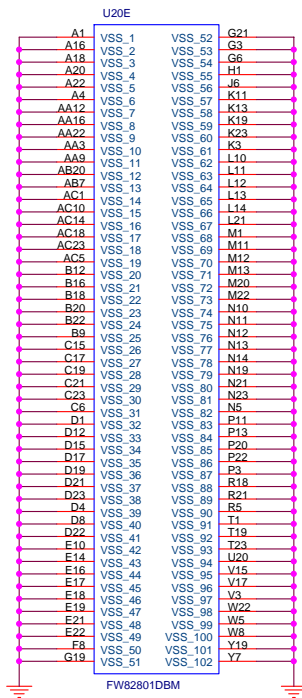
RC time delay should be 10-20 ms

RTC_RST#, RTC_VBIAS, RTC_X1, RTC_X2
 Width= 5.5 mils
 Length <= 1"
 Need GND Guard

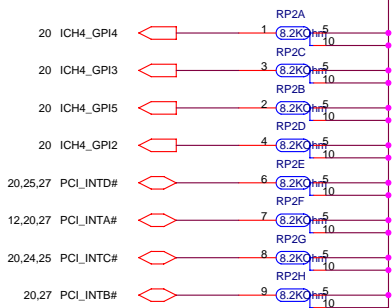
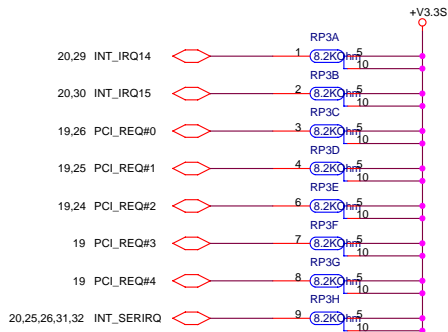
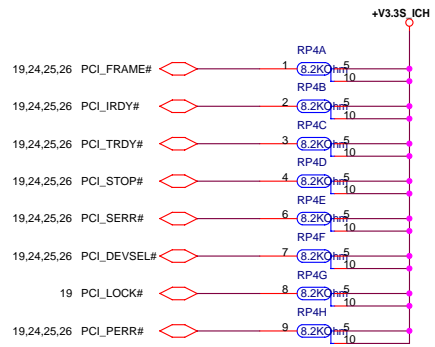
A2.1 PCB uses "xtal_3p_319x108" footprint, but the SMT recommended 1st source part uses "xtal_3p_335x110" footprint.



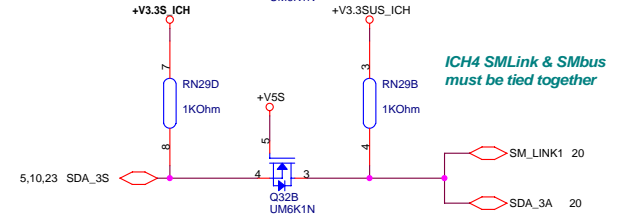
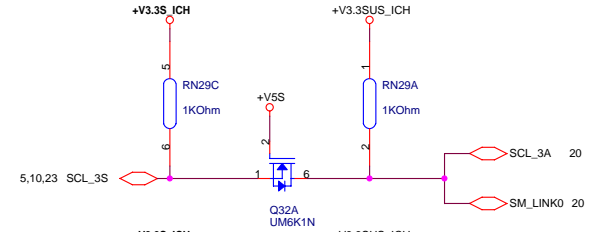
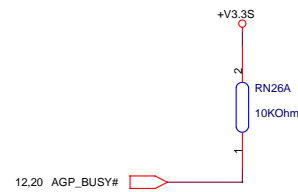
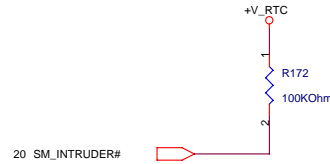
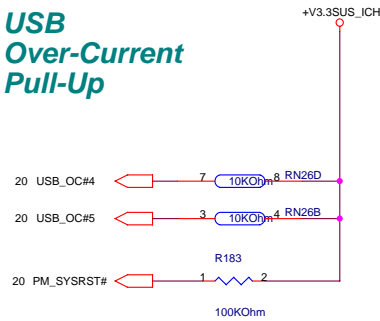
PID_0_ICH4	3	2.2KOhm	RN89B	PID_0	17
PID_1_ICH4	1	2.2KOhm	RN89A	PID_1	17
PID_2_ICH4	5	2.2KOhm	RN89C	PID_2	17
PID_3_ICH4	7	2.2KOhm	RN89D	PID_3	17



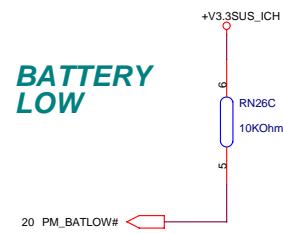
Caution:
The VREF of HUB interface is 0.35V
The VSWING of HUB interface is 0.8V
But in Intel CRB, their naming convention will make people confused.

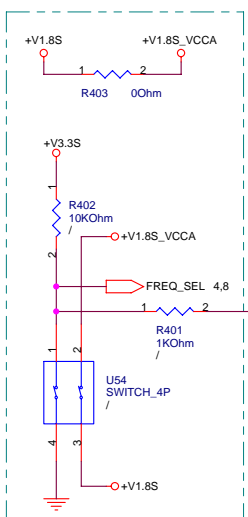


USB Over-Current Pull-Up



BATTERY LOW





CLK_EN# is OD for MAX1987

FS4	FS3	FUNCTION
0	0	100MHz
0	1	133MHz (D)
1	0	200MHz
1	1	166MHz

For 852GMV:
Load R401, R402, U54

For 855GM/ 855GME/ 852GM/ 852GME:
Load R403, R368

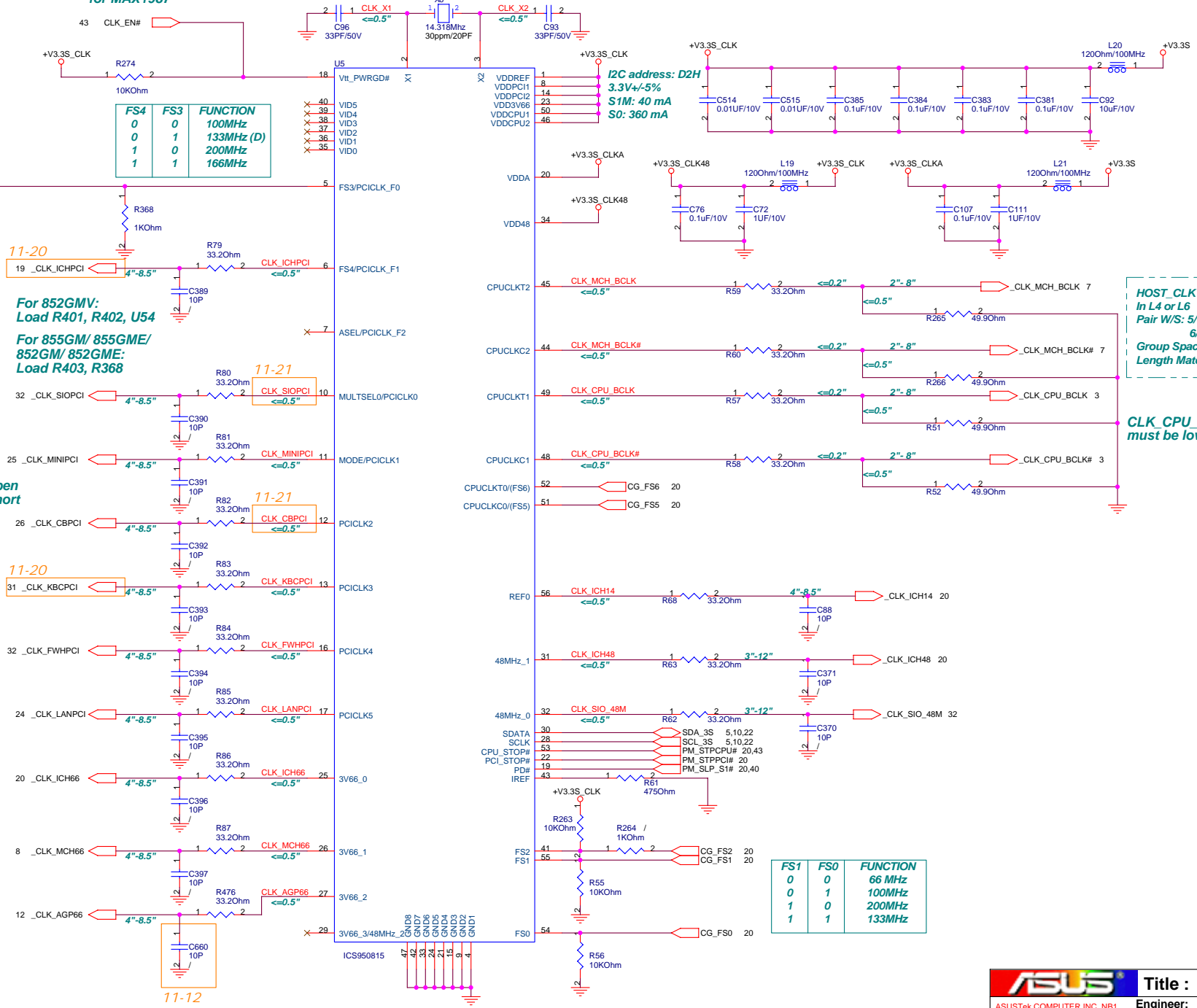
1(H): FSB Freq=133MHz & VCCA[0]=1.5V
4(L): FSB Freq=100MHz & VCCA[0]=1.8V

2: Dothan(533) CPU
3: Celeron/Banias /Dothan(400) CPU

U54 switch to 1: pin1 & 4 open
U54 switch to 4: pin1 & 4 short

CLK33 GROUP:
In L4 or L6
W/S: 5.5/16.5 mils (L4)
4.5/13.5 mils (L6)
Group Space >= 20 mils
Length Match: same as CLK66

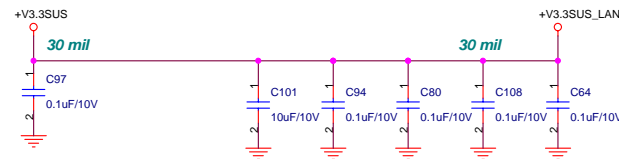
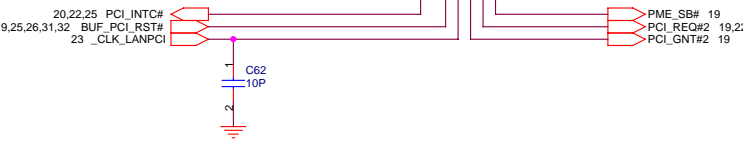
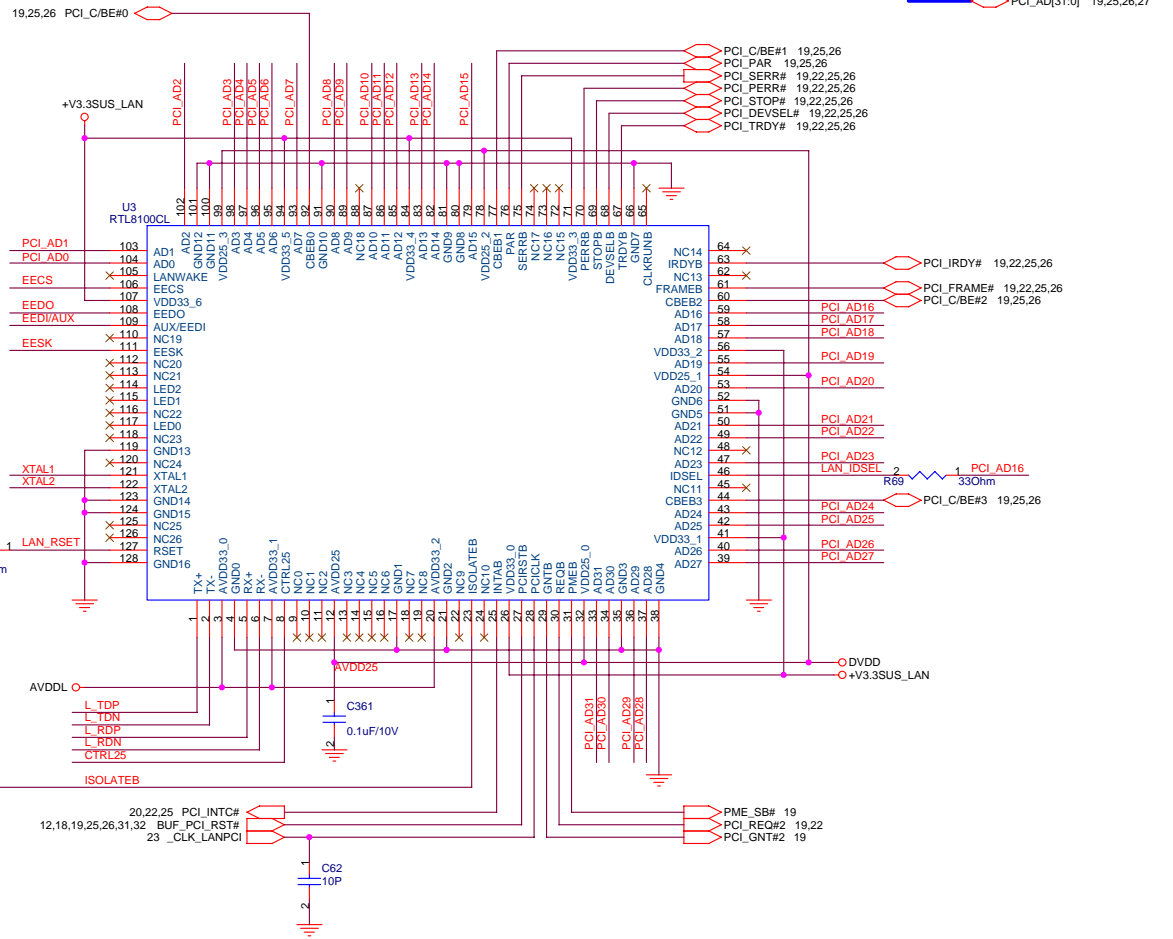
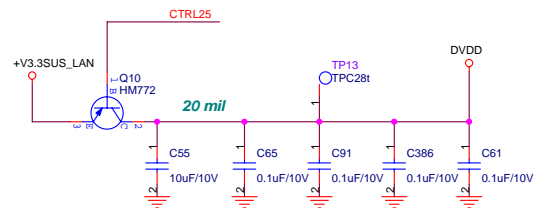
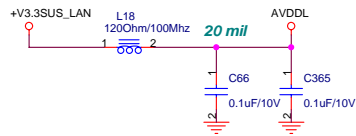
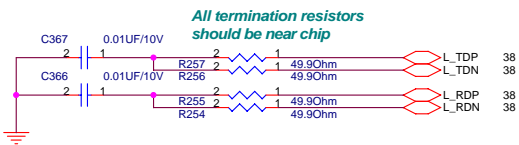
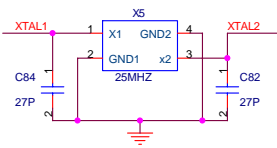
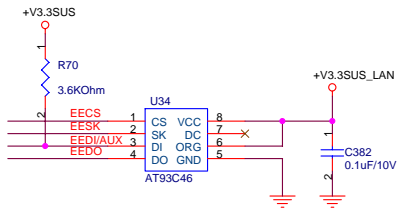
CLK66 GROUP:
In L4 or L6
W/S: 5.5/16.5 mils (L4)
4.5/13.5 mils (L6)
Group Space >= 20 mils
Length Match: +/- 100 mils

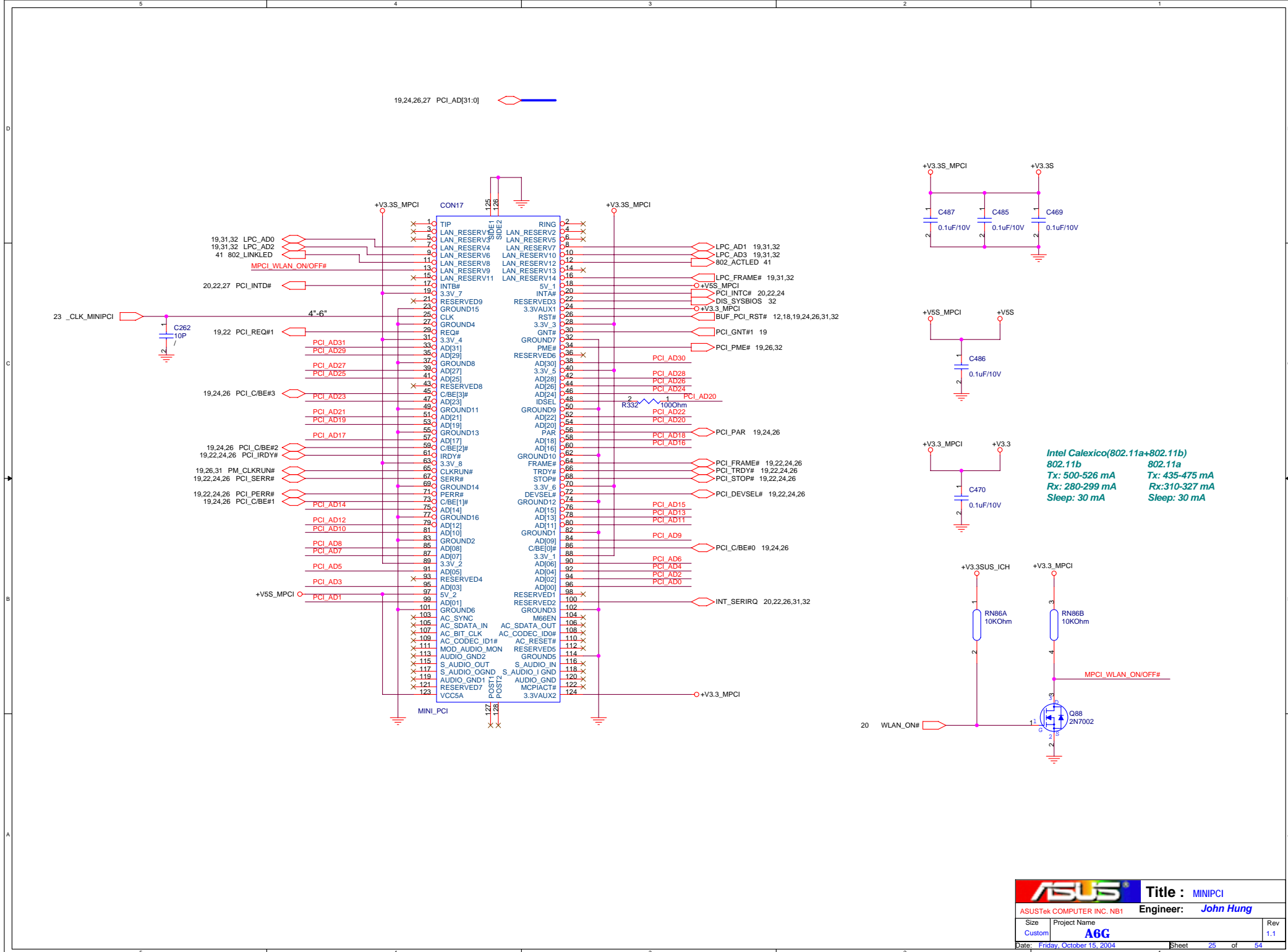


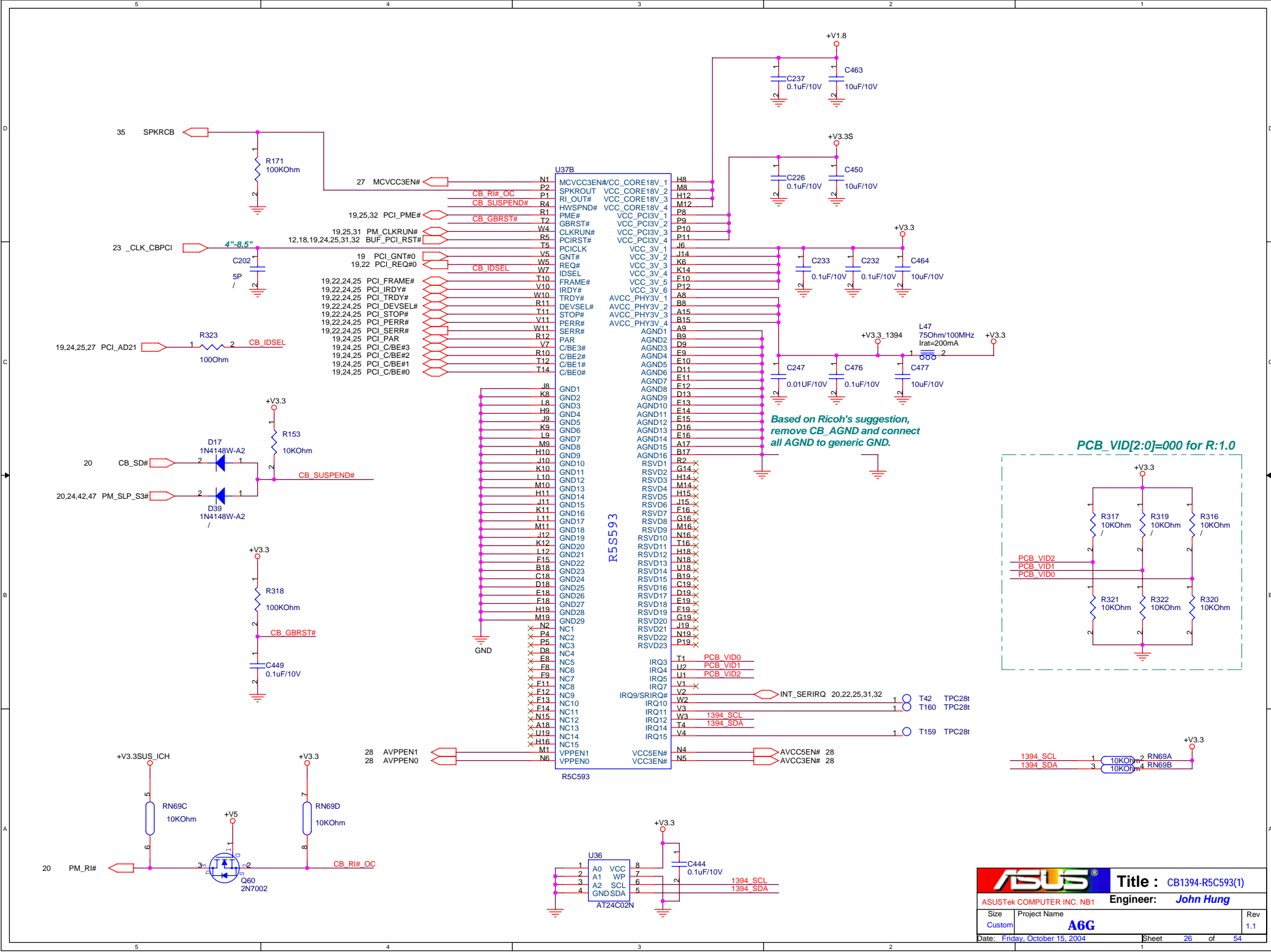
HOST_CLK GROUP
In L4 or L6
Pair W/S: 5/12 mils (L4)
6/11 mils (L6)
Group Space: >= 20 mils
Length Match: +/- 10 mils

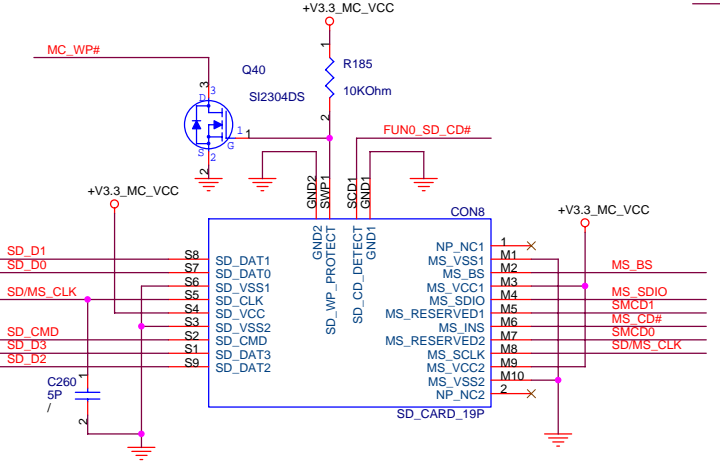
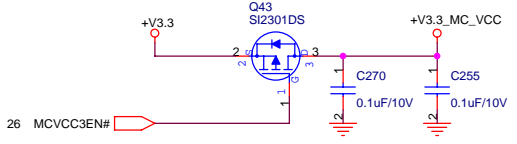
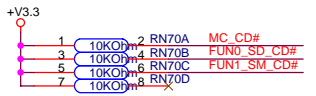
CLK_CPU_BCLK# must be low in C3

FS1	FS0	FUNCTION
0	0	66 MHz
0	1	100MHz
1	0	200MHz
1	1	133MHz





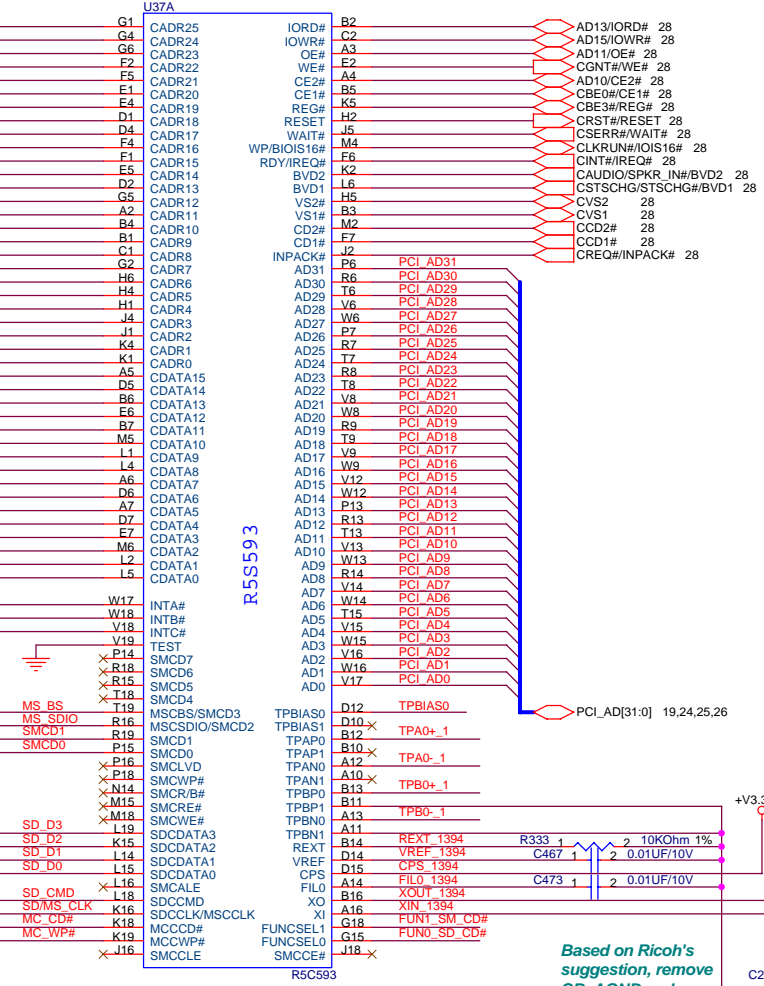
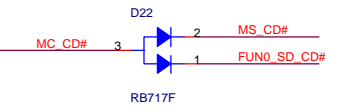




Memory Card Detect

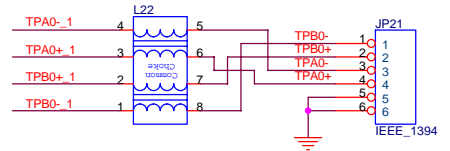
FUNSEL1	FUNSEL0	
0	0	Not Support
0	1	SmartMedia
1	0	MMC/SD
1	1	Memory Stick

MC_CD# : Memory Card Detect
Turn-on voltage: 0.37 V



REXT/VREF/FILO:
To implement as close as possible to R5C593
To apply shield GND

Based on Ricoh's suggestion, remove CB_AGND and connect all AGND to generic GND.



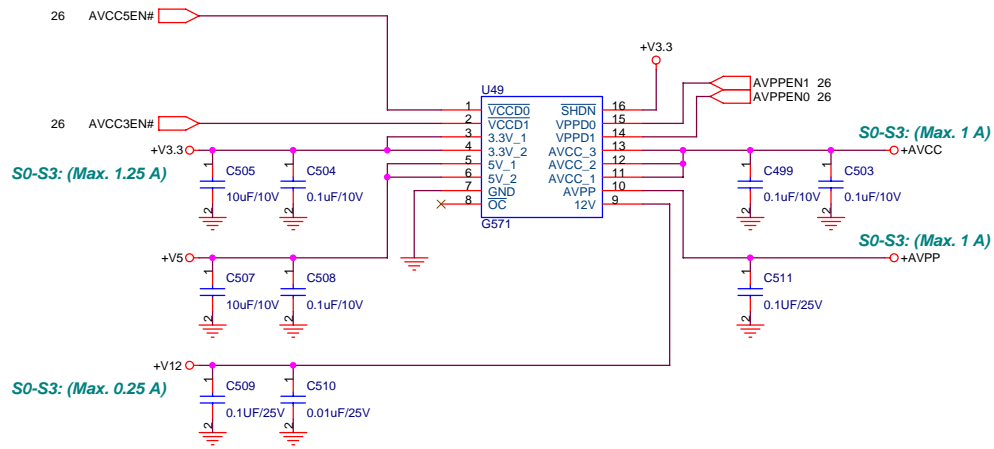
ASUS Title : CB1394-R5C593(2)

ASUSTek COMPUTER INC. NB1 Engineer: John Hung

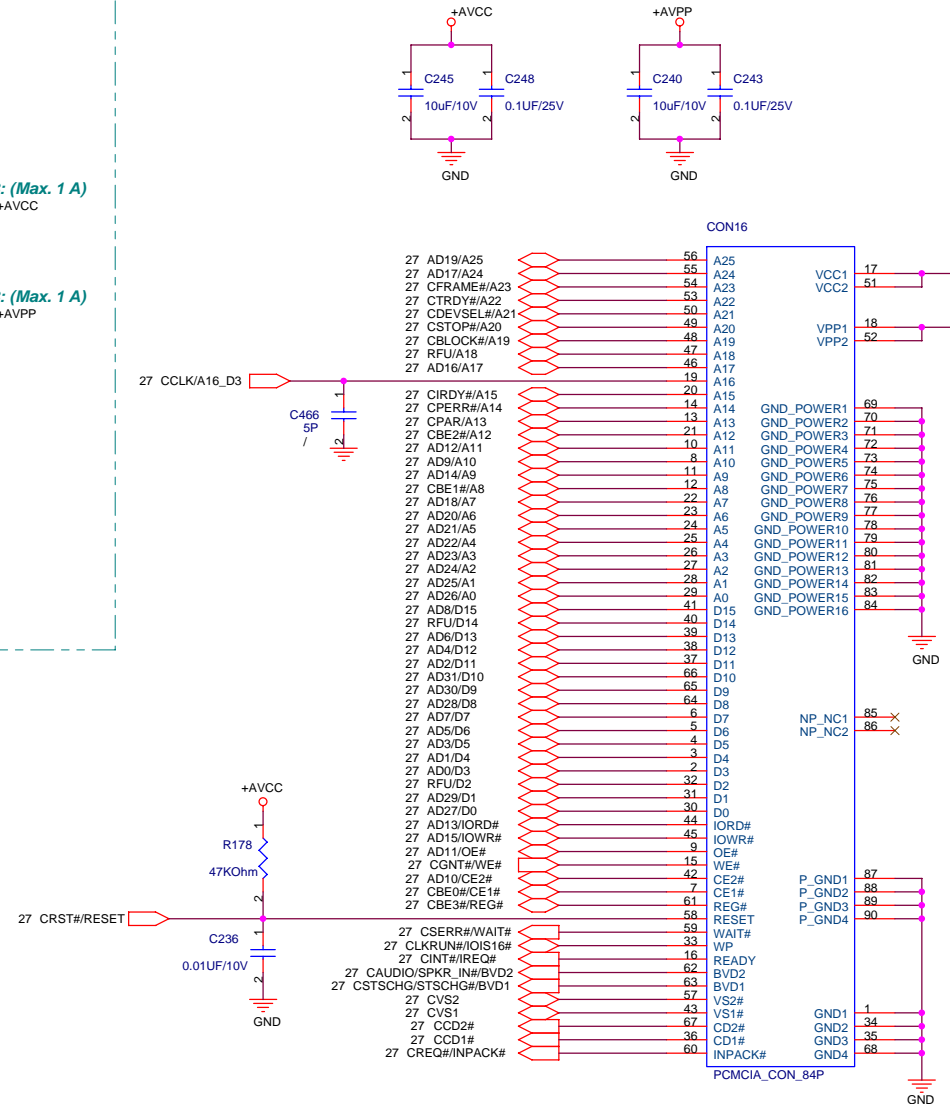
Size	Project Name	Rev
Custom	A6G	1.1

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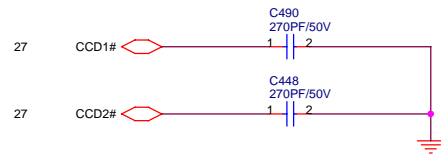
CB POWER SWITCH

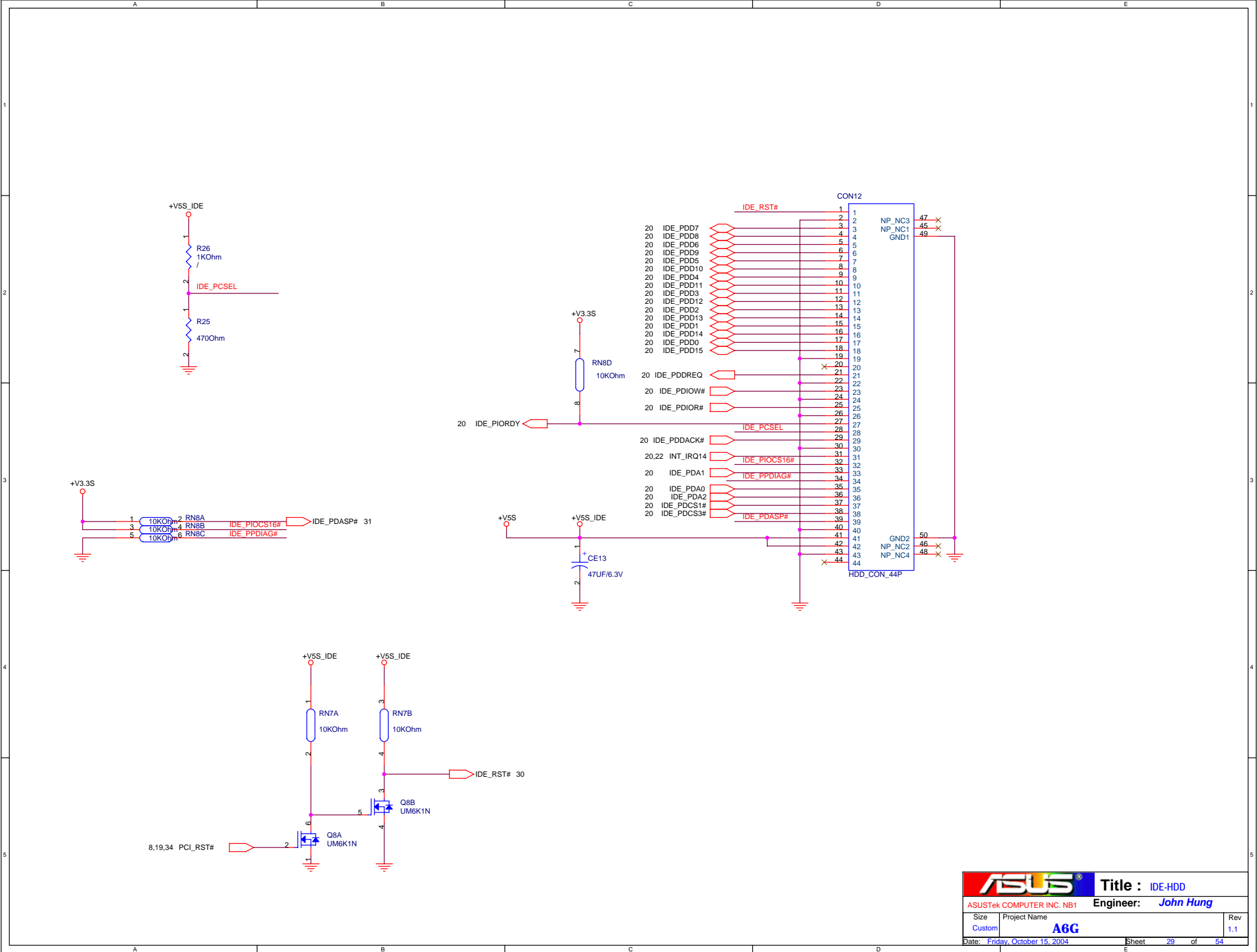


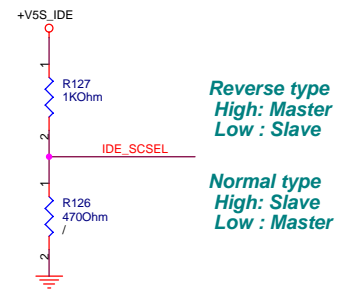
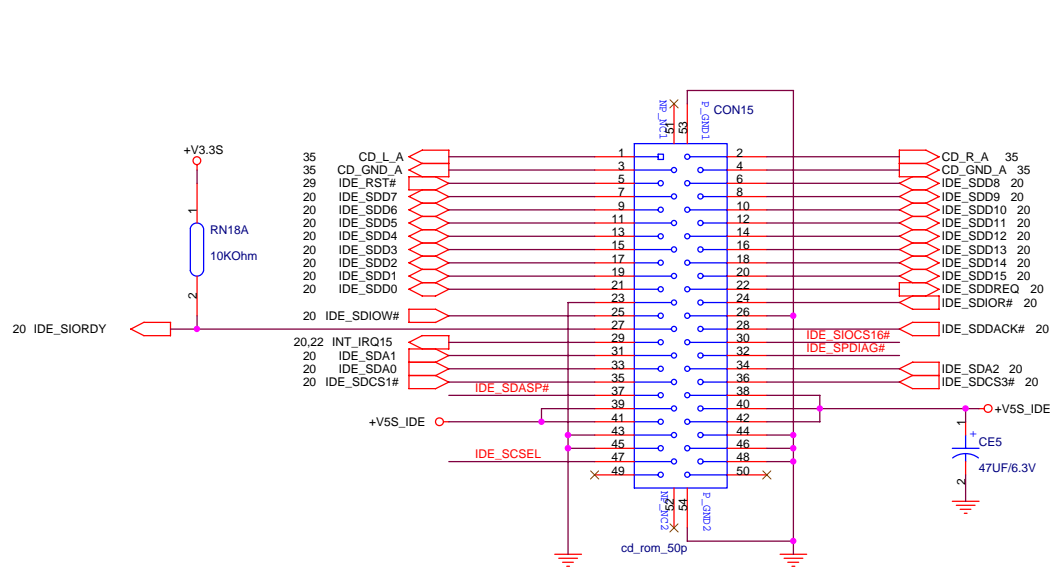
CB SOCKET



CB DE-BOUNCE

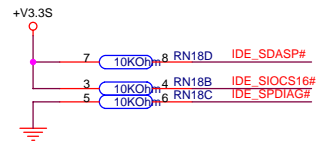


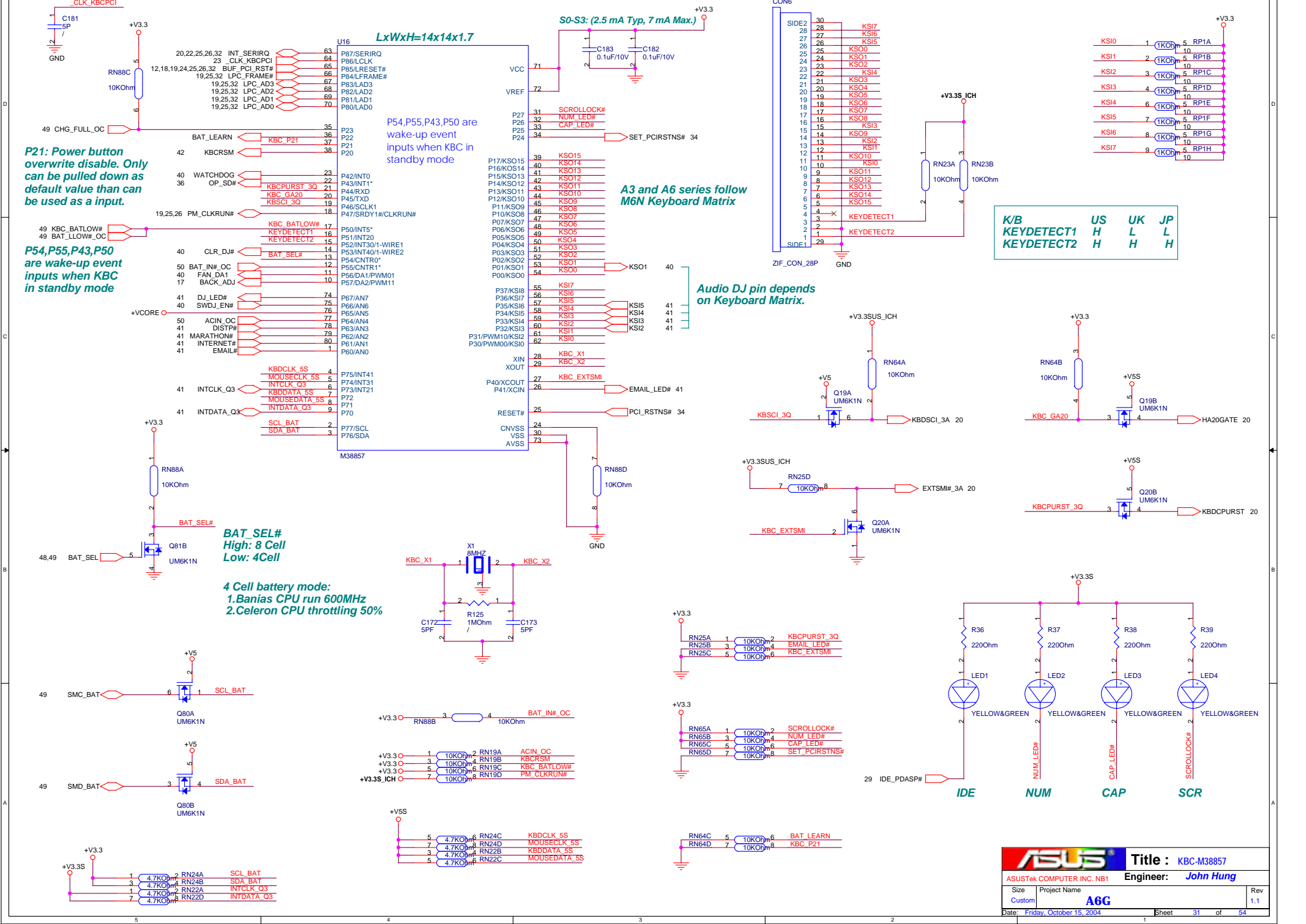




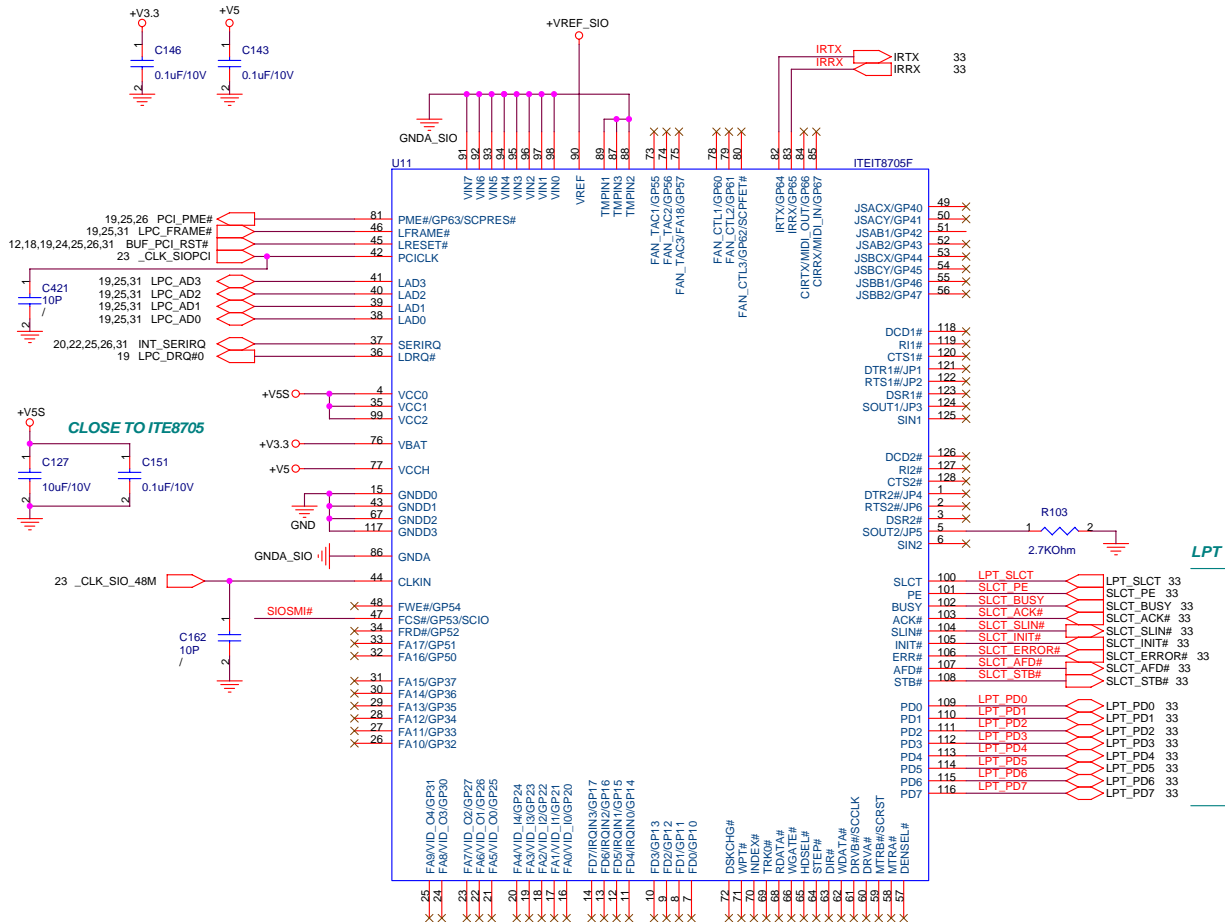
Reverse type
High: Master
Low: Slave

Normal type
High: Slave
Low: Master

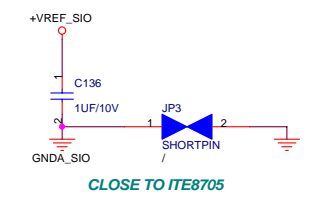
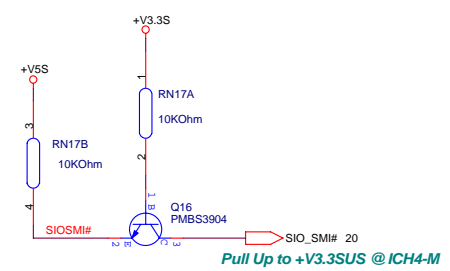
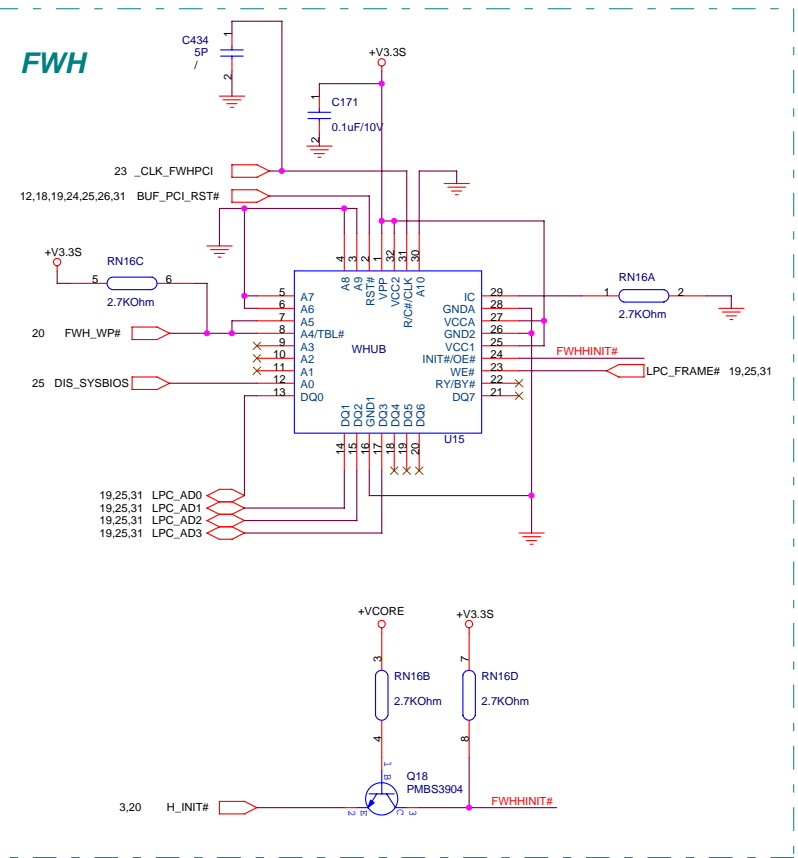


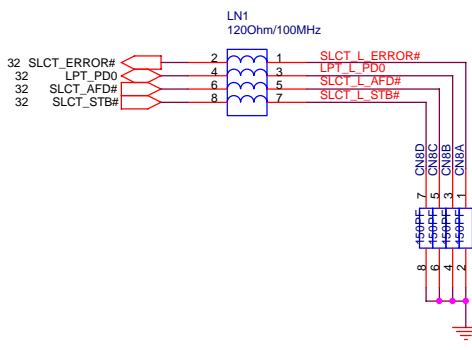
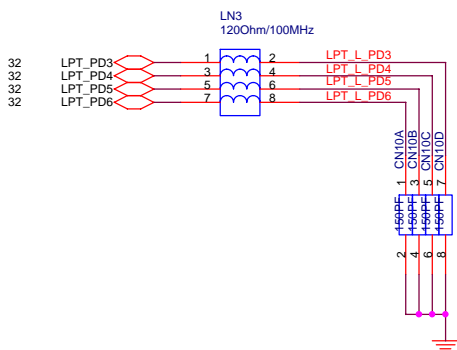
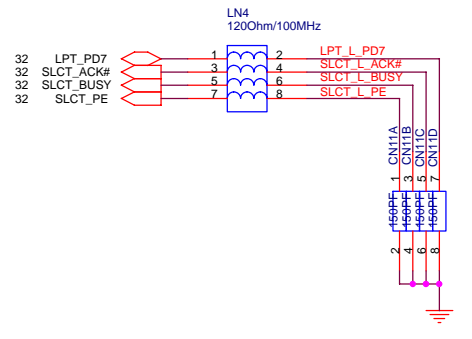
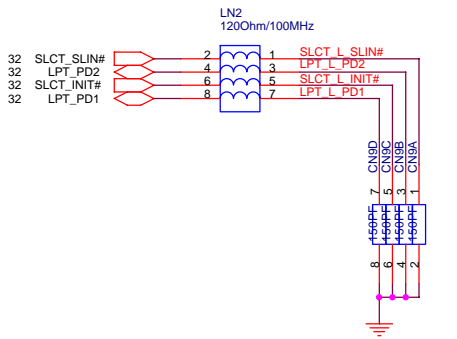


Super I/O

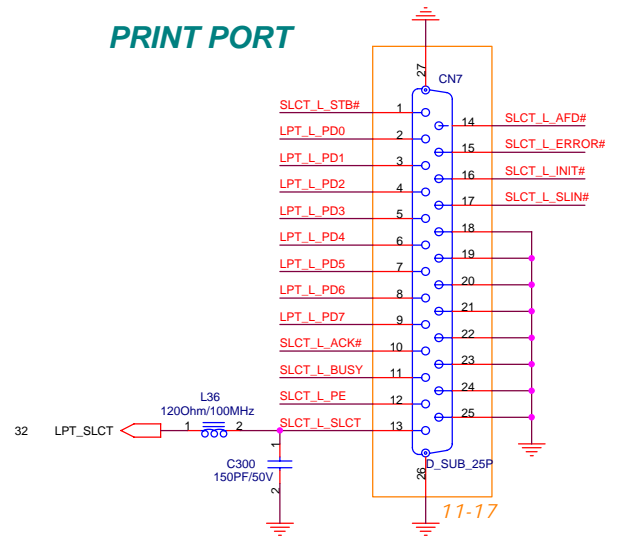


FWH

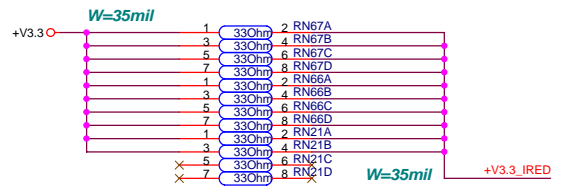
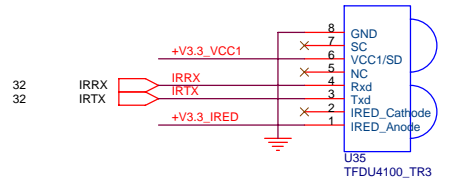
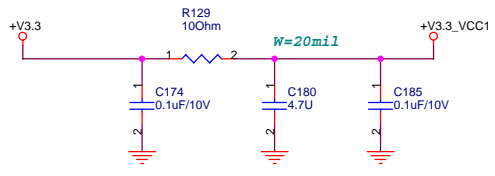




PRINT PORT

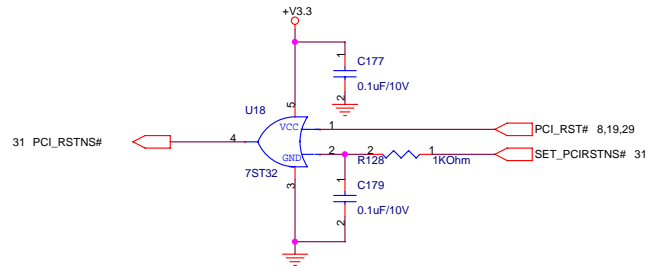


IR

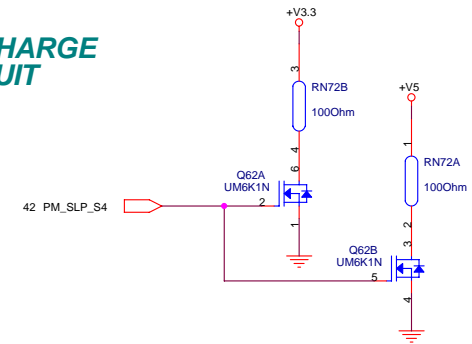


A6G follows A3 to NOT support PCMCIA DEBUG Card Function

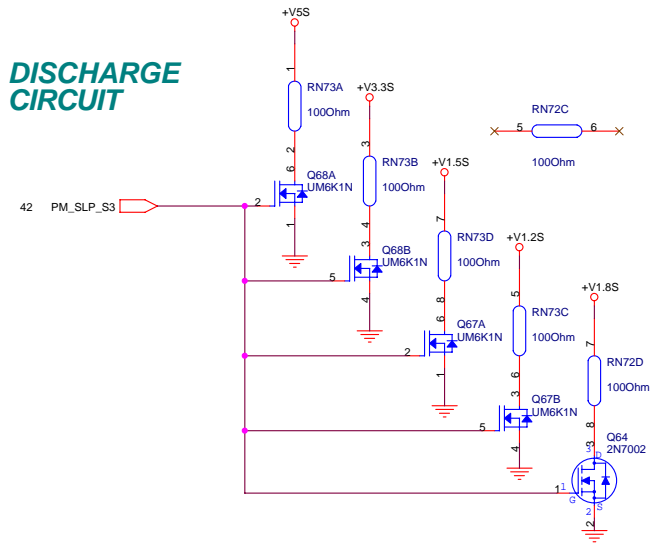
PCI_RSTNS# Gen Circuit



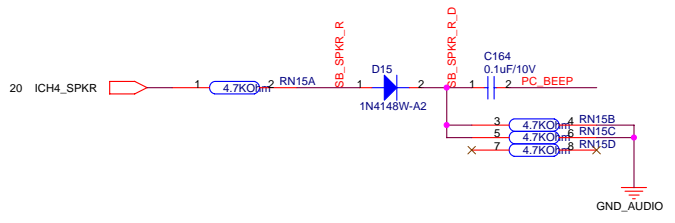
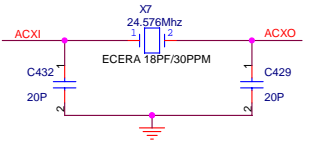
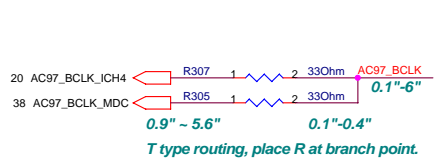
DISCHARGE CIRCUIT



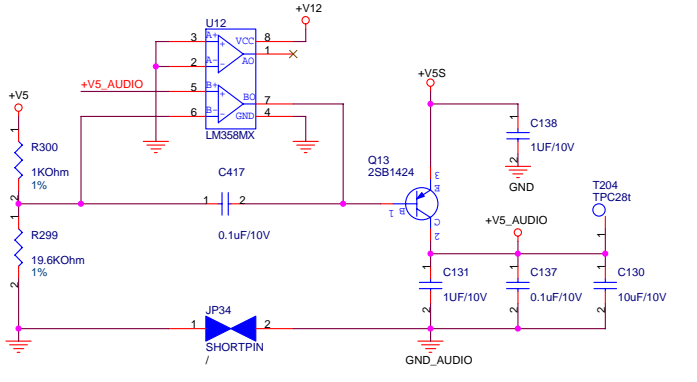
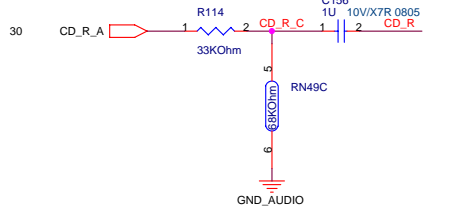
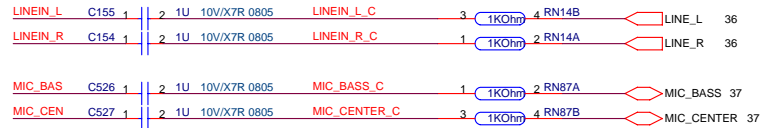
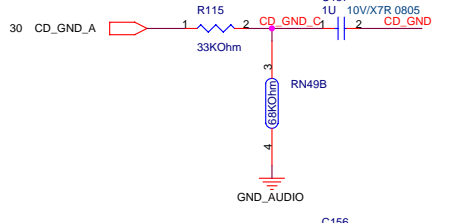
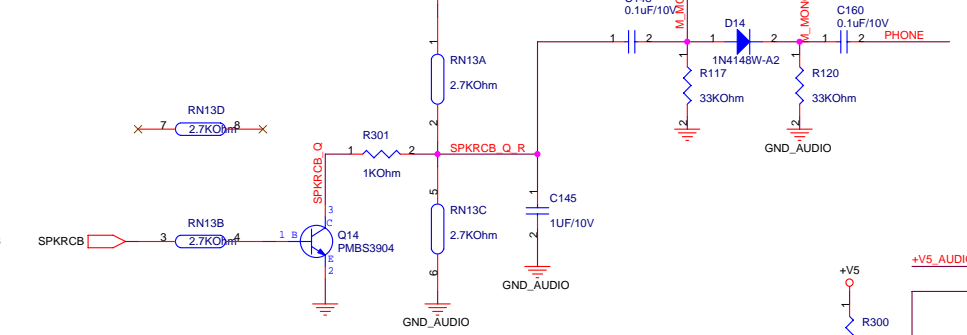
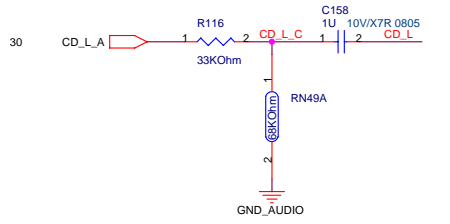
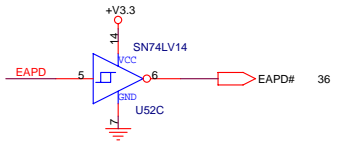
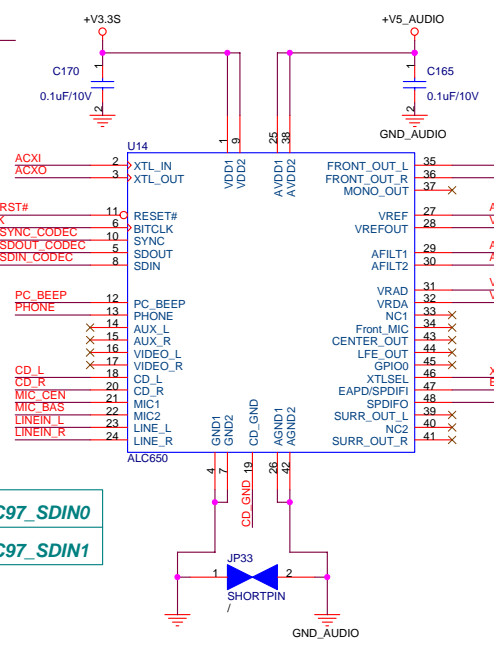
DISCHARGE CIRCUIT

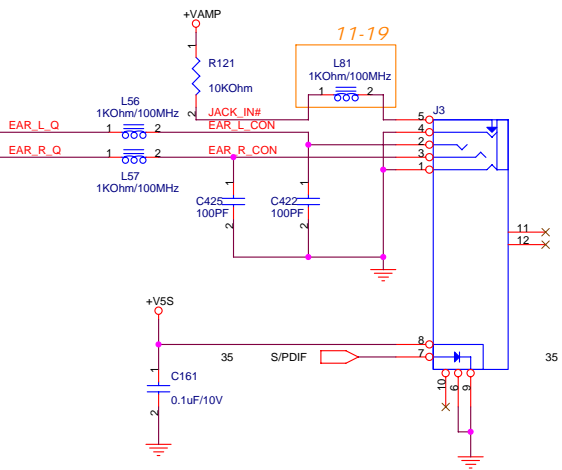
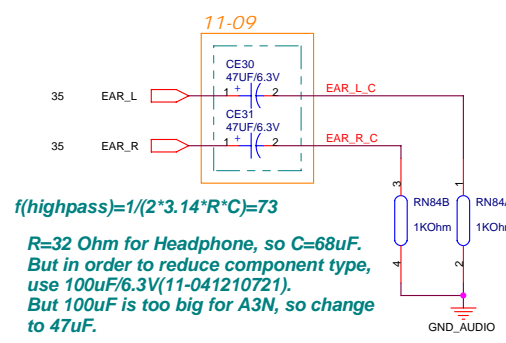
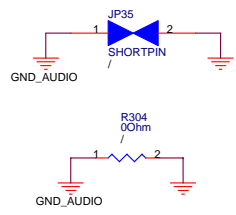
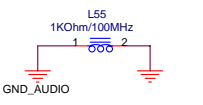


ASUS		Title : DISCHARGE CIRCUIT	
ASUSTek COMPUTER INC. NB1		Engineer: John Hung	
Size	Project Name	Rev	
Custom	A6G	1.1	
Date: Friday, October 15, 2004		Sheet	34 of 54



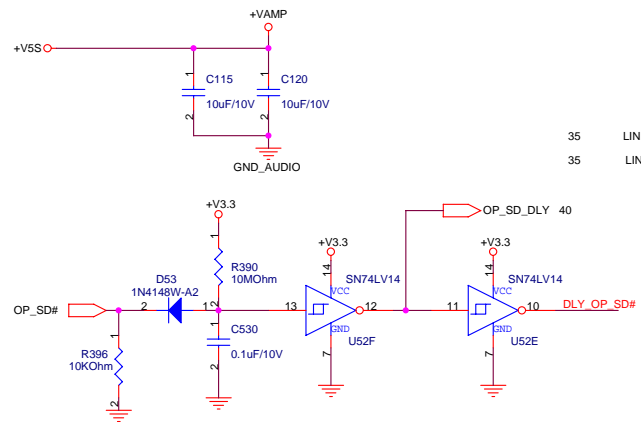
CODEC	AC97_SDINO
MDC	AC97_SDIN1





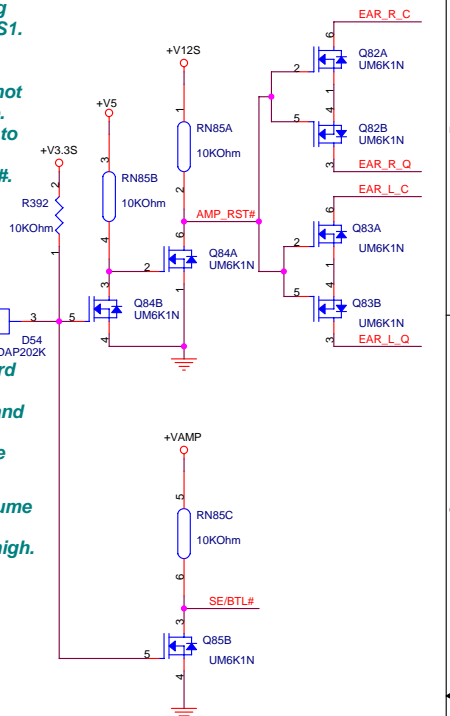
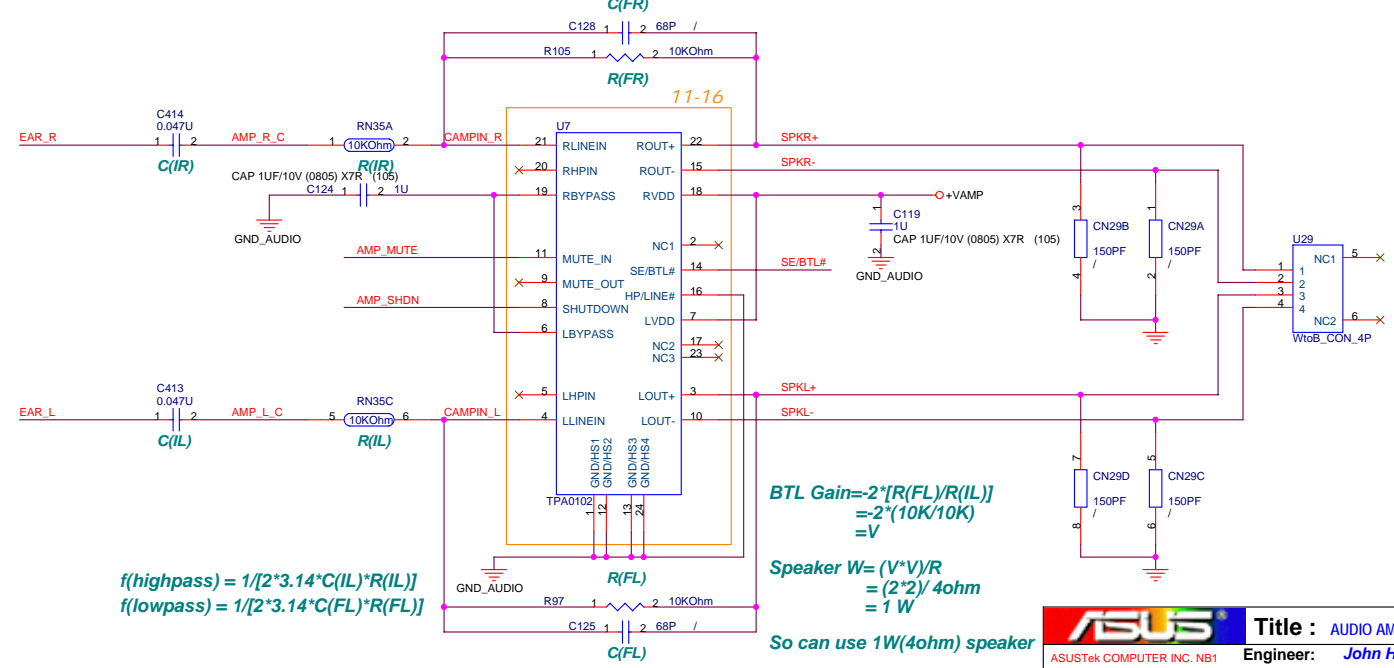
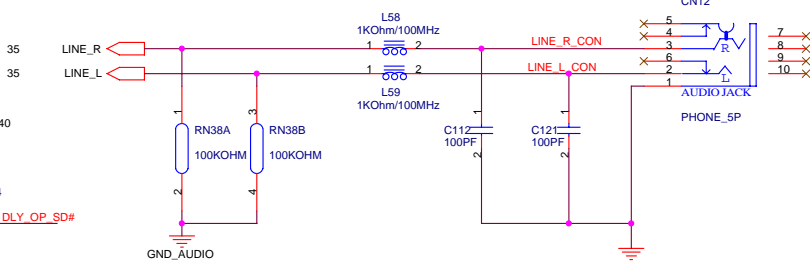
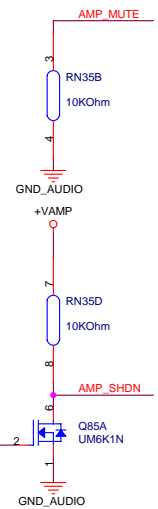
Noise occurred during system resume from S1. The timing of DLY_OP_SD# and AC97_RST# still can not prevent the pop noise. Realtek recommends to use pin47 EAPD to substitute AC97_RST#. This pin can be controlled by codec driver to meet our timing request.

Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing. But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.

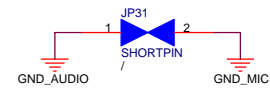
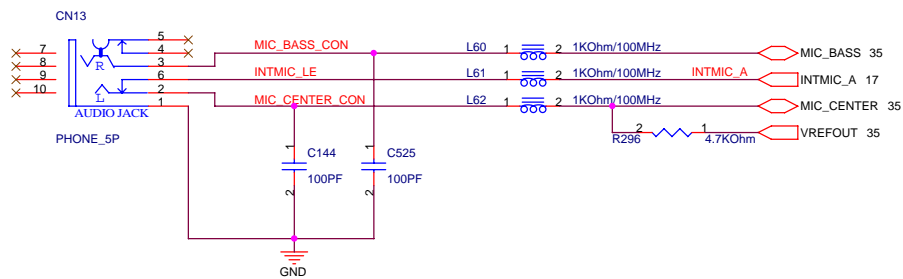


For reduce "POP" noise when system enter S3 (suspend to RAM) or resume from S3. Net "OP_SD#" should be pull low by KBC controller when system at S3 mode.

If using "OP_SD#" to switch AMP_SHDN, speaker will have "POP" noise after logo display when turn on system.



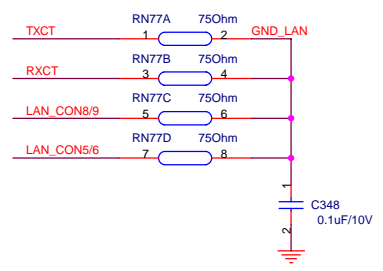
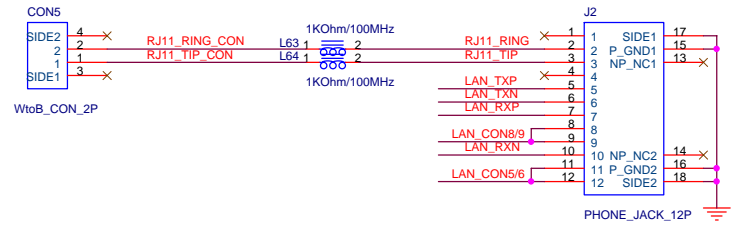
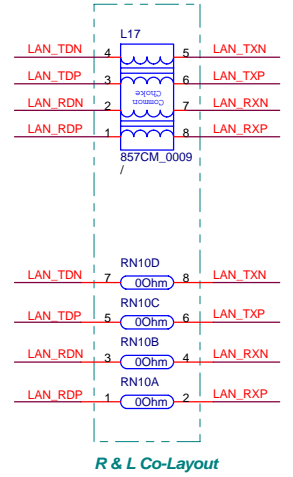
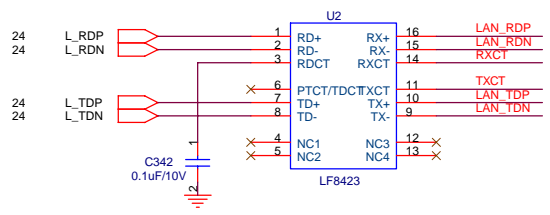
MIC JACK



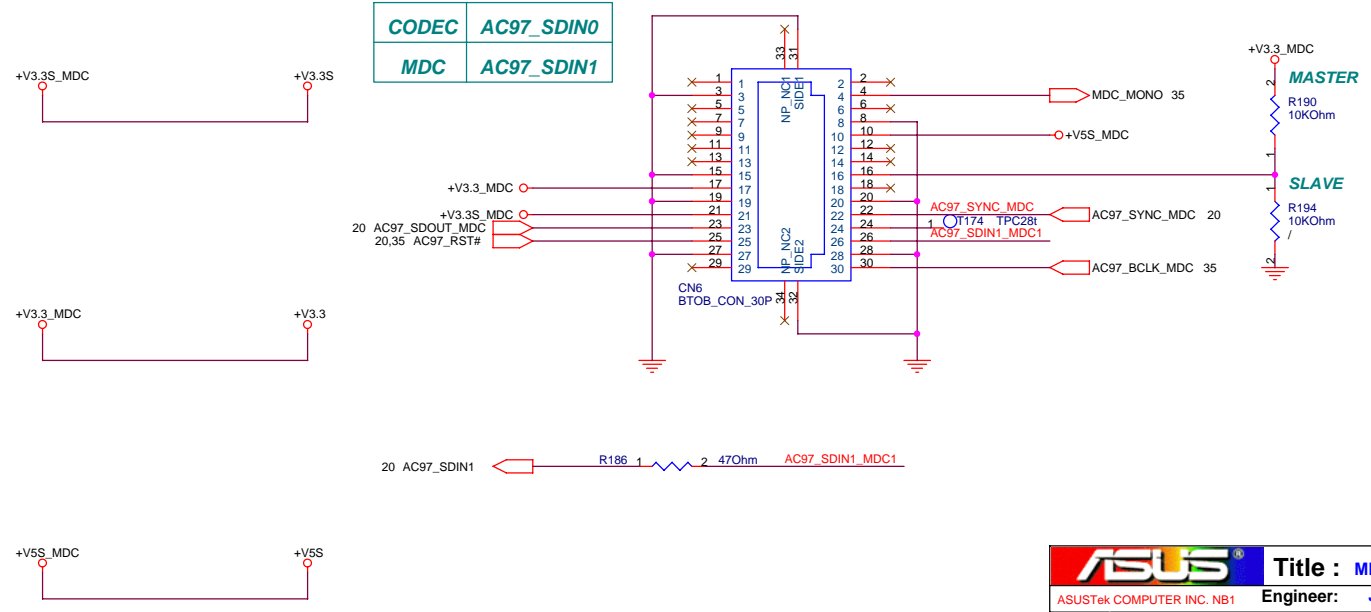
INTMIC_A & GND_AUDIO :
W/P/X = 12/5/15mils

ASUS		Title : MIC	
ASUSTek COMPUTER INC. NB1		Engineer: John Hung	
Size Custom	Project Name A6G	Date: Friday, October 15, 2004	Rev 1.1
		Sheet 37 of 54	

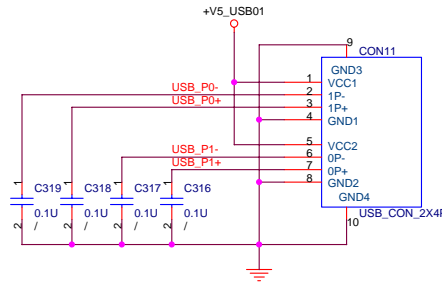
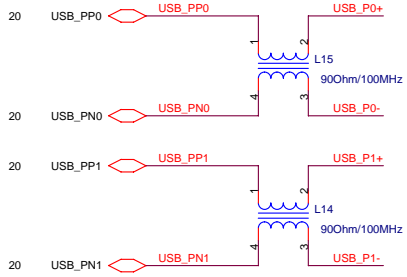
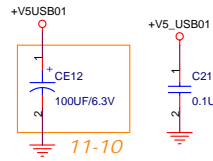
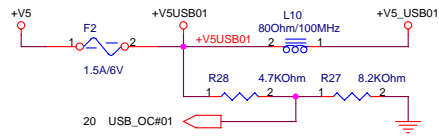
RJ45 & RJ11



MDC

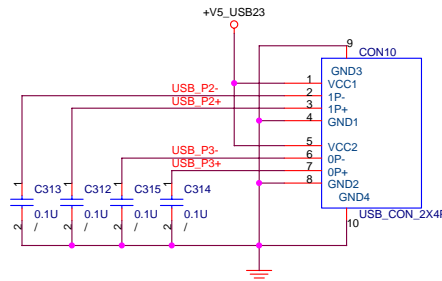
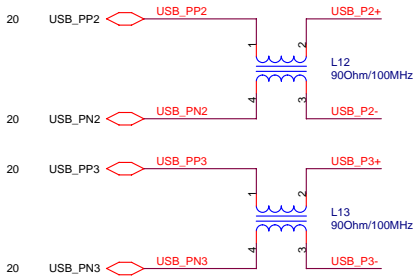
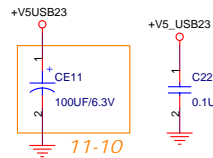
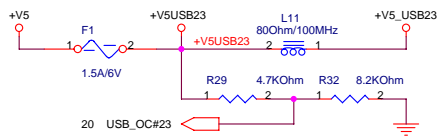


USB PORT 0 & PORT 1



USB PORT 4

USB PORT 2 & PORT 3



USB PORT 5 for USB CEMERA

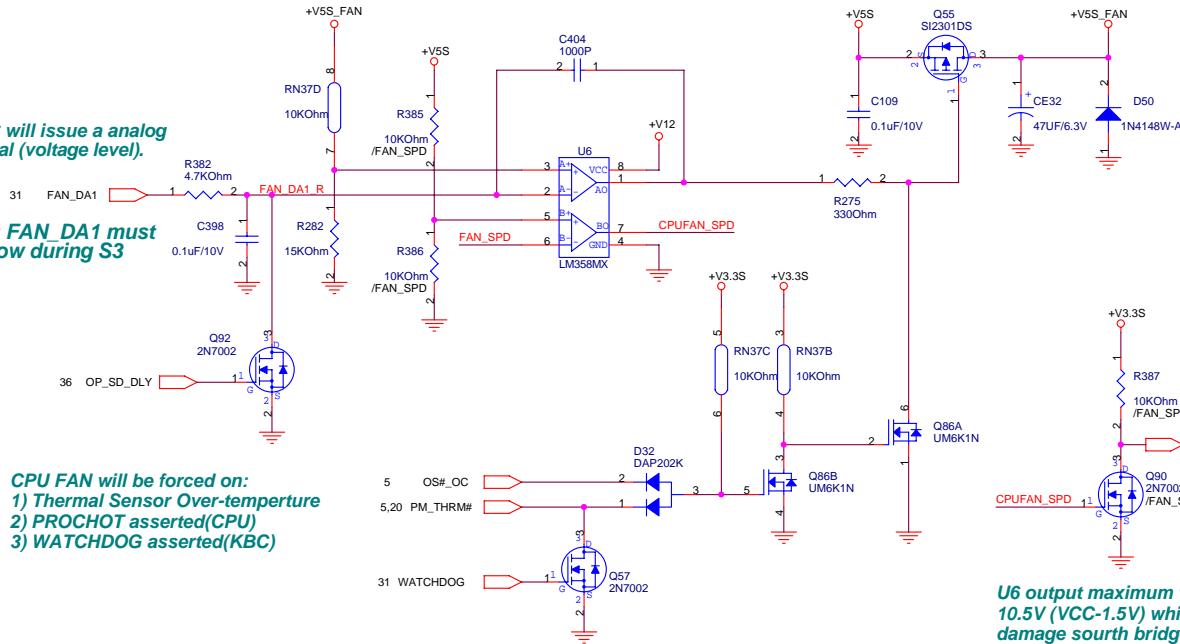
(Move to Page 17)

DC FAN

Using a OP AMP and fine-tuning the level, we can improve the fan ON/OFF detection.

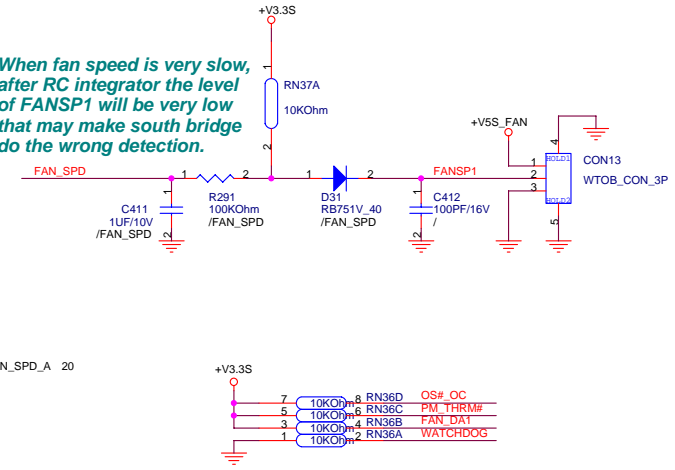
KBC will issue a analog signal (voltage level).

SW: FAN_DA1 must be low during S3



CPU FAN will be forced on:
 1) Thermal Sensor Over-temperature
 2) PROCHOT asserted(CPU)
 3) WATCHDOG asserted(KBC)

When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

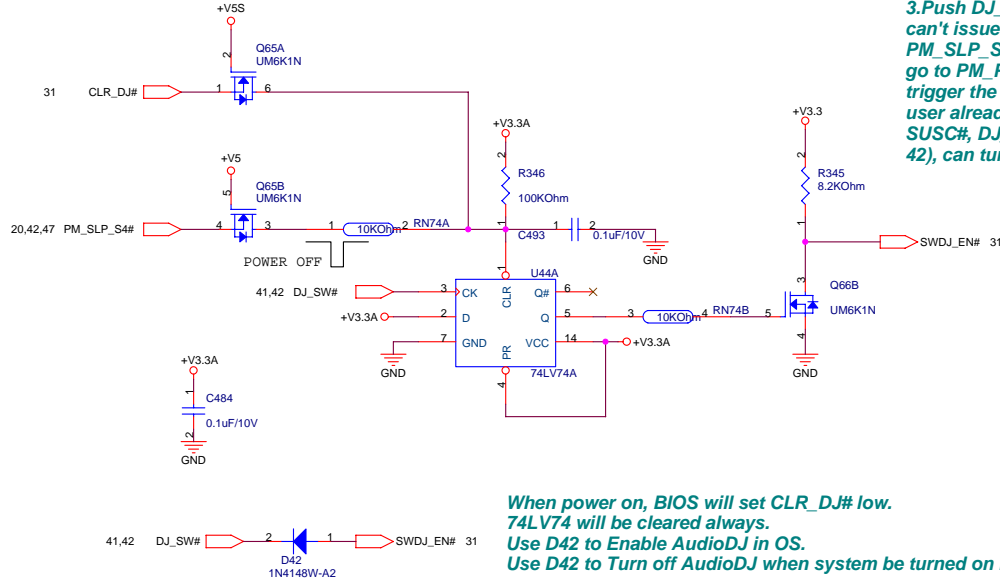


U6 output maximum will be 10.5V (VCC-1.5V) which will damage south bridge. Add a MOS to transfer it to +3V level.

AUDIO DJ

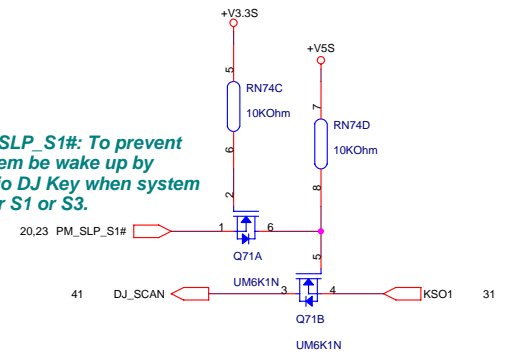
SWDJ_EN# function :

1.Push DJ_SW#, turn on Audio DJ.
 2.PM_SLP_S4# will keep high.
 3.Push DJ_SW# again, KBC will receive SWDJ_EN#. KBC can't issue SUSC# (PM_SLP_S4#) immediately. If KBC do it, PM_SLP_S4# (page 42) will go low, DJ_SW# low signal will go to PM_PWRBTN#, then system will restart. KBC need trigger the righting edge of SWDJ_EN#, for make sure end user already push than remove DJ Switch button than issue SUSC#, DJ_SW# won't initial low to PM_PWRBTN# (page 42), can turn off Audio DJ and won't restart.

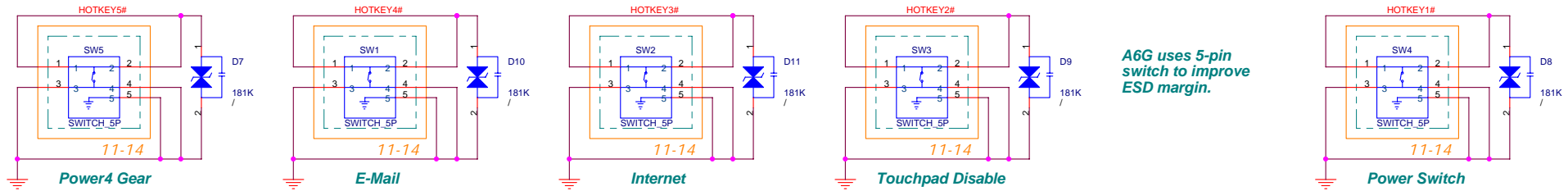


When power on, BIOS will set CLR_DJ# low. 74LV74 will be cleared always.
 Use D42 to Enable AudioDJ in OS.
 Use D42 to Turn off AudioDJ when system be turned on in DJ mode.

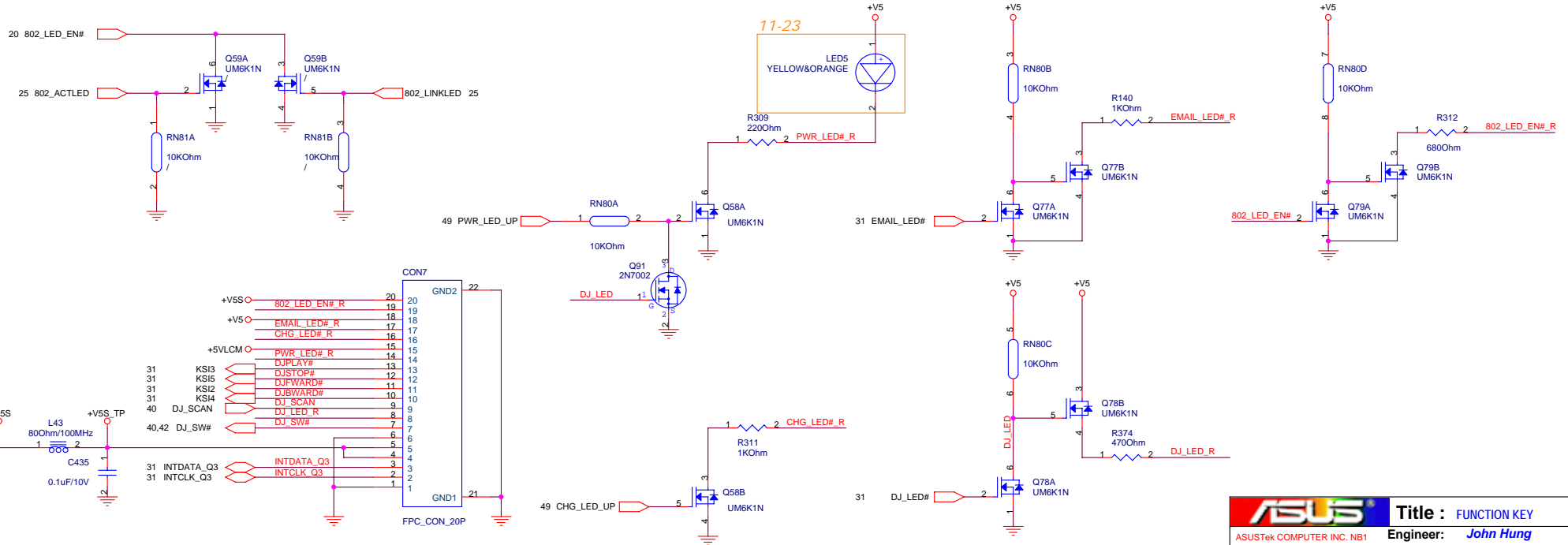
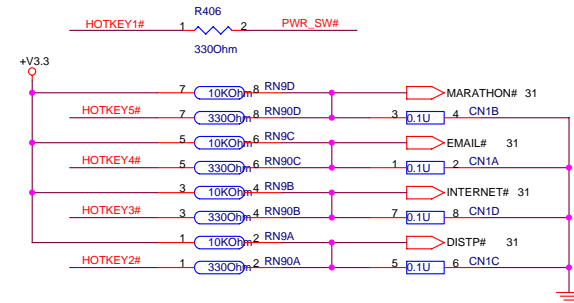
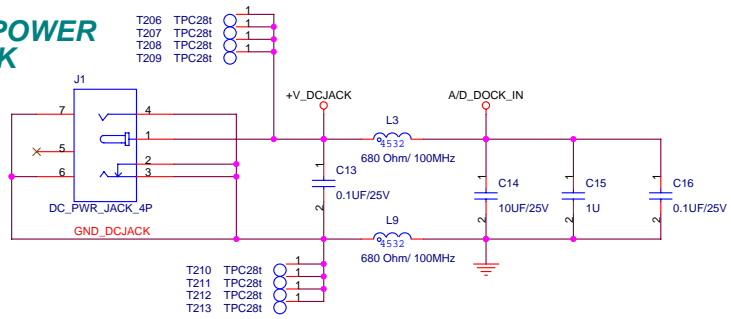
PM_SLP_S1#: To prevent system be wake up by Audio DJ Key when system enter S1 or S3.

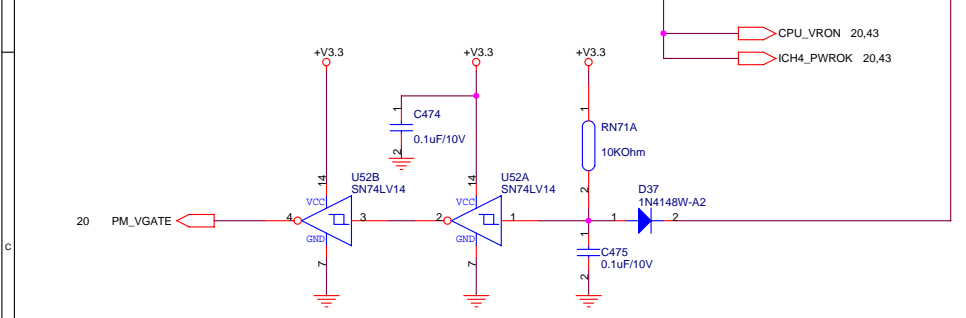
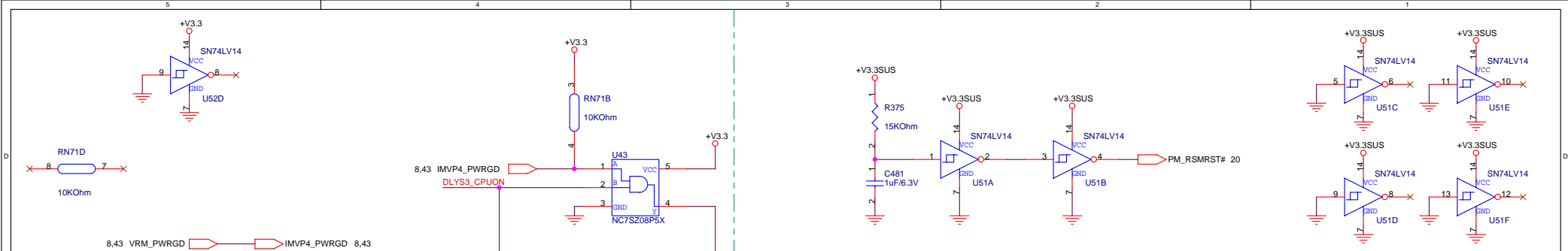


FUNCTION KEY



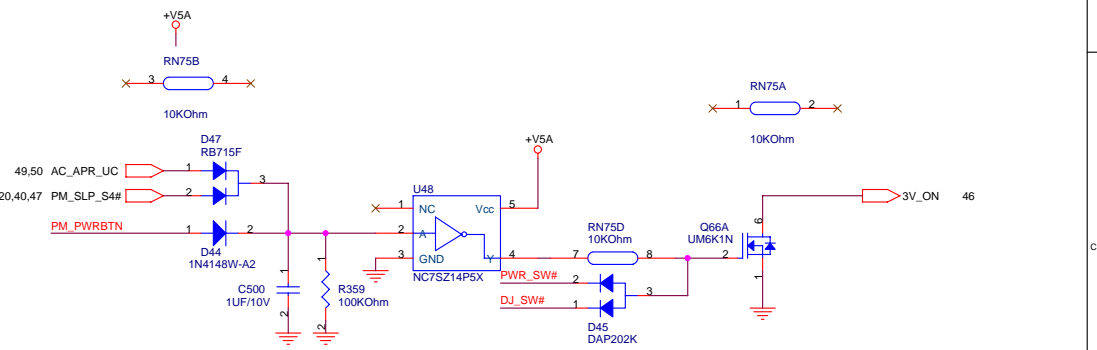
DC POWER JACK



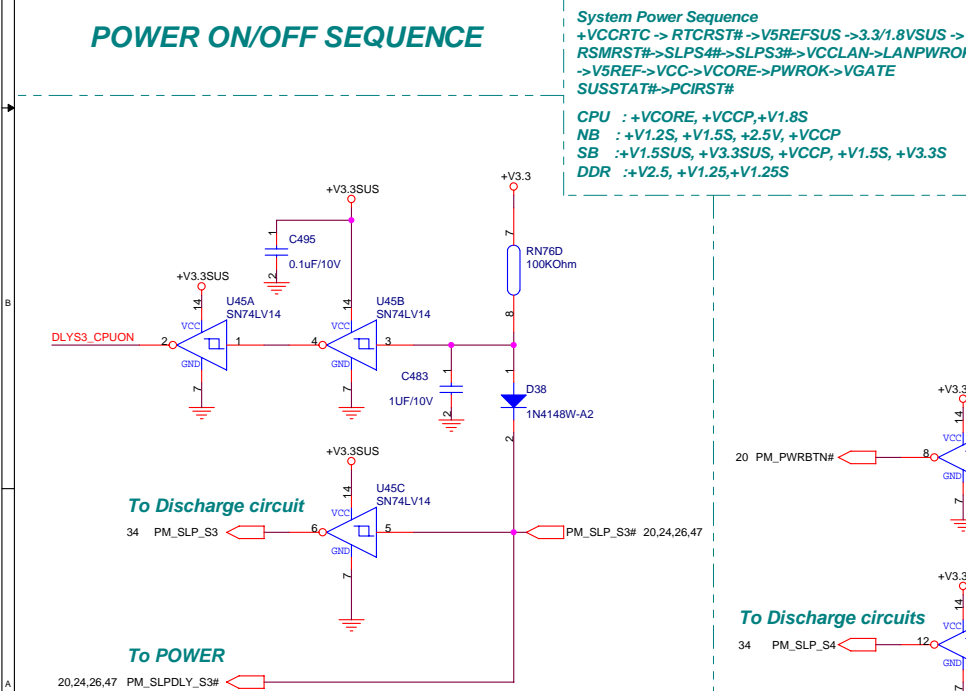
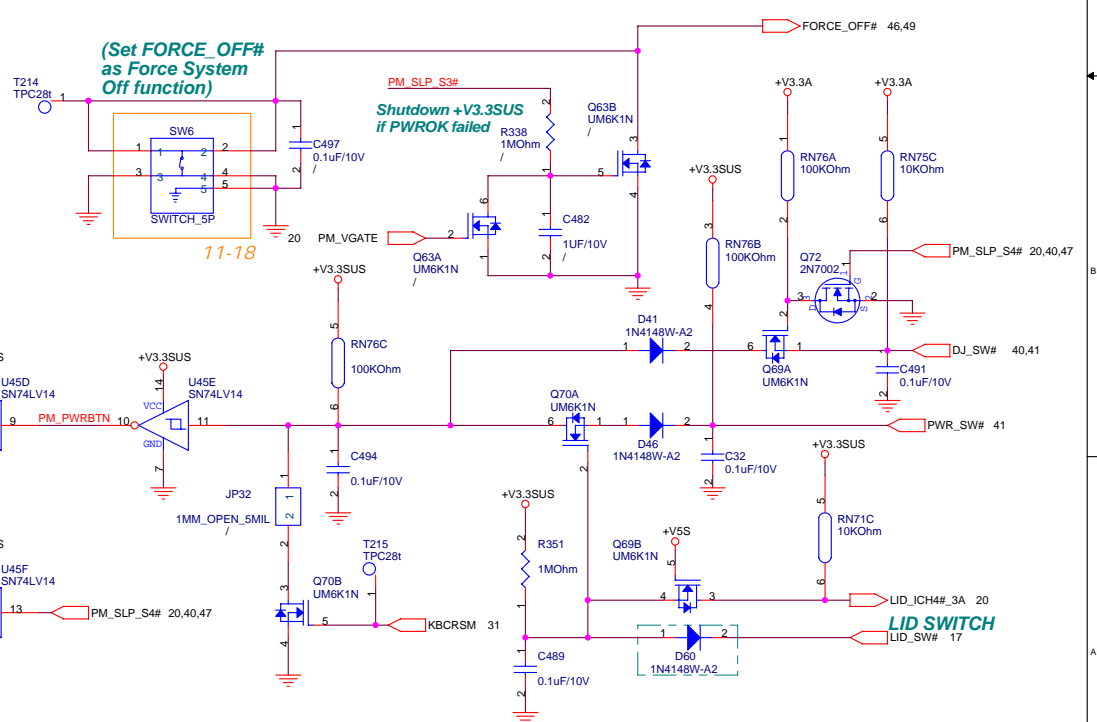


System Power Sequence
 +VCCRTC -> RTCRST# -> V5REFSUS -> 3.3/1.8VSUS ->
 RSMRST# -> SLPS4# -> SLPS3# -> VCCLAN -> LANPWROK
 -> V5REF -> VCC -> VCORE -> PWROK -> VGATE
 SUSSTAT# -> PCIRST#

CPU : +VCCORE, +VCCCP, +V1.8S
NB : +V1.2S, +V1.5S, +2.5V, +VCCCP
SB : +V1.5SUS, +V3.3SUS, +VCCCP, +V1.5S, +V3.3S
DDR : +V2.5, +V1.25, +V1.25S

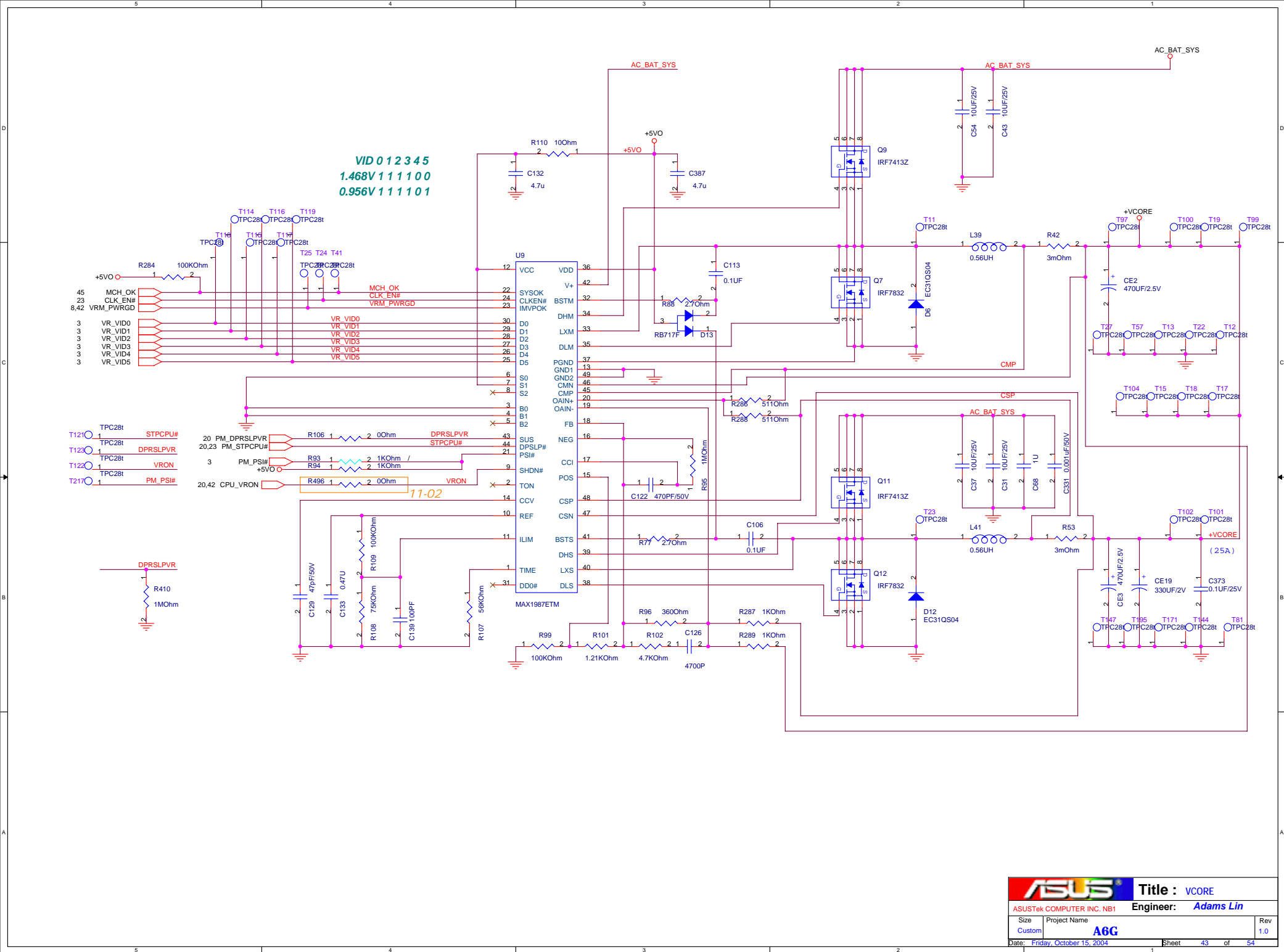


POWER ON/OFF SEQUENCE



To Discharge circuits

KBCRSM will issue low when system on & BIOS work normally.
 Issue high when system on & BIOS don't work, then system will off after 4 seconds to protect system.
 Issue a high pulse to wake up system from S3 state by push any key.

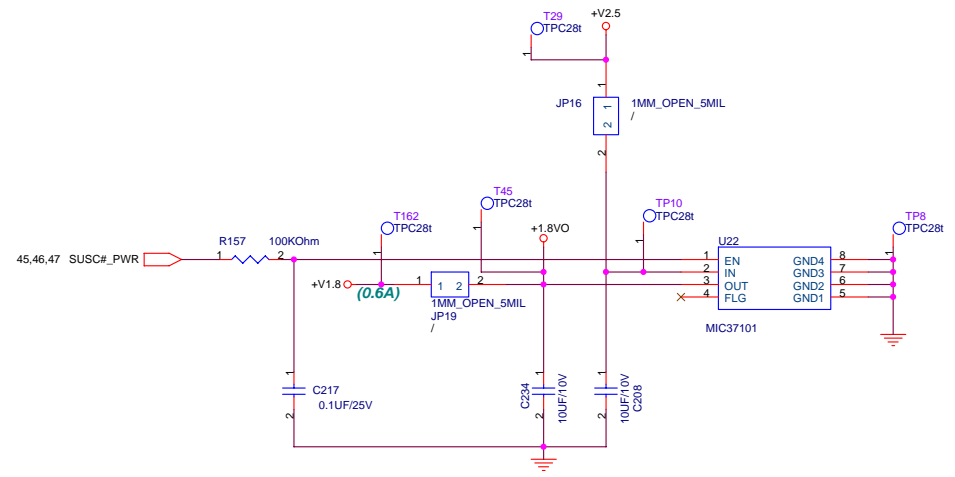
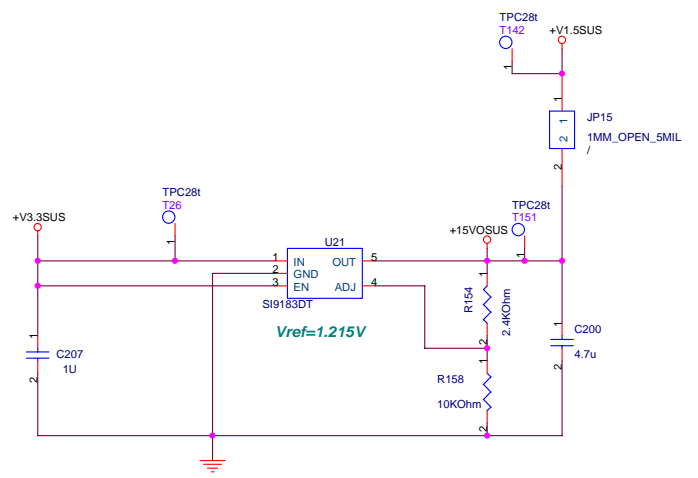
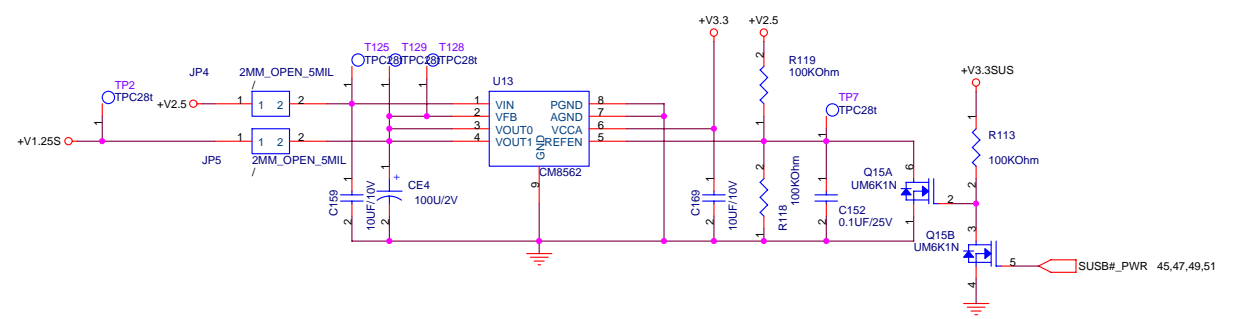
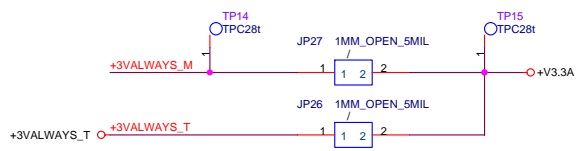
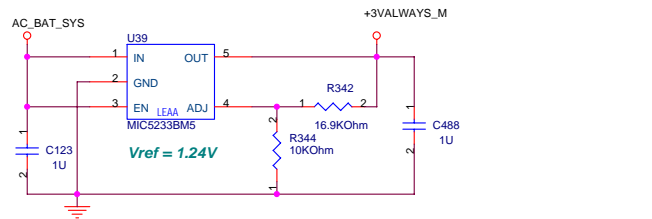


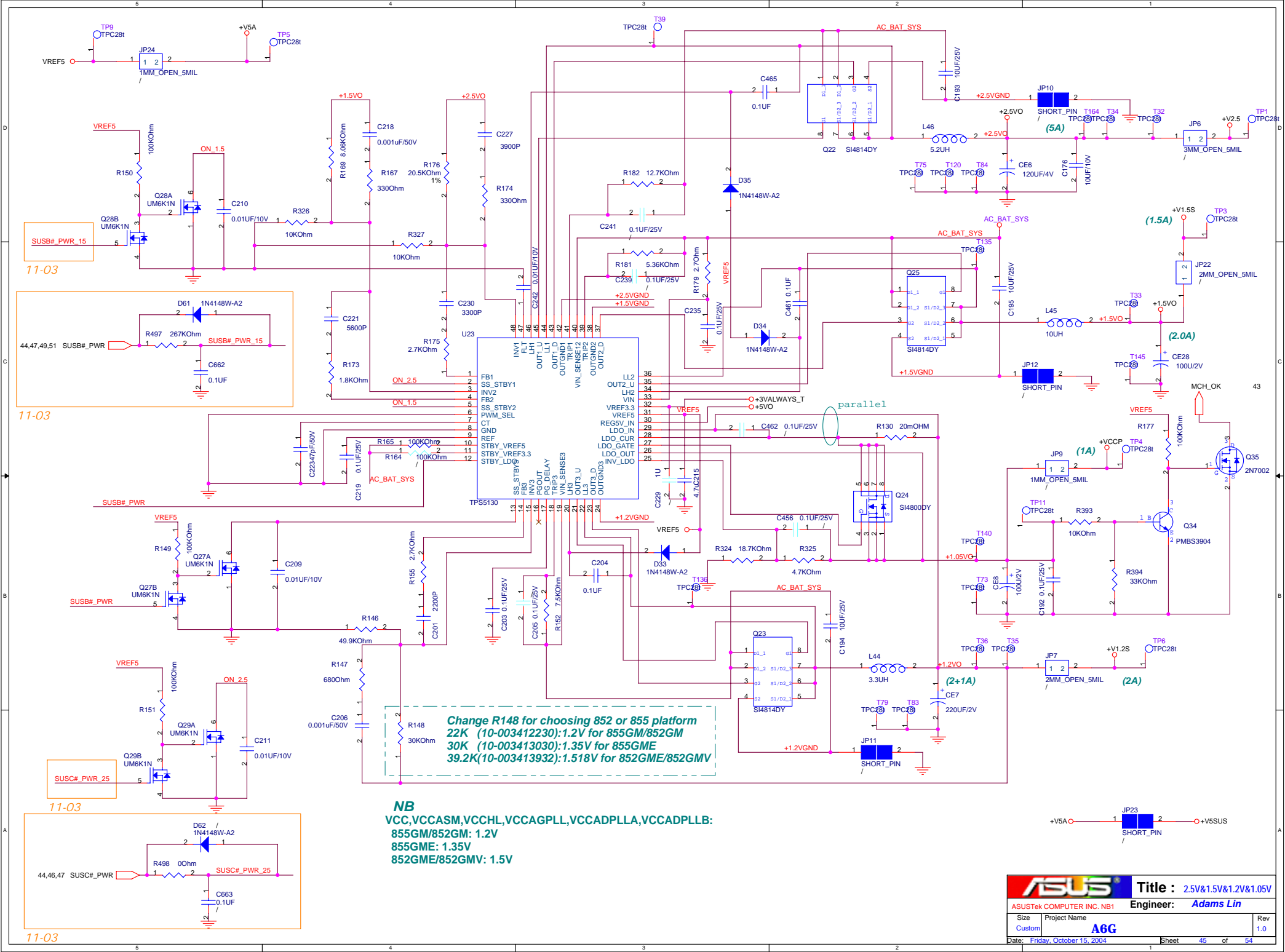
VID 0 1 2 3 4 5
 1.468V 1 1 1 1 0 0
 0.956V 1 1 1 1 0 1

T121 TPC28t STPCPU#
 T120 TPC28t DPRSLPVR
 T122 TPC28t VRON
 T217 TPC28t PM_PSI#

20 PM_DPRSLPVR R106 1 2 00Ohm DPRSLPVR
 20,23 PM_STPCPU# DPRSLPVR STPCPU#
 3 PM_PSI# R93 1 2 1KOhm / VRON
 +5V0 R94 1 2 1KOhm
 20,42 CPU_VRON R496 1 2 00Ohm VRON

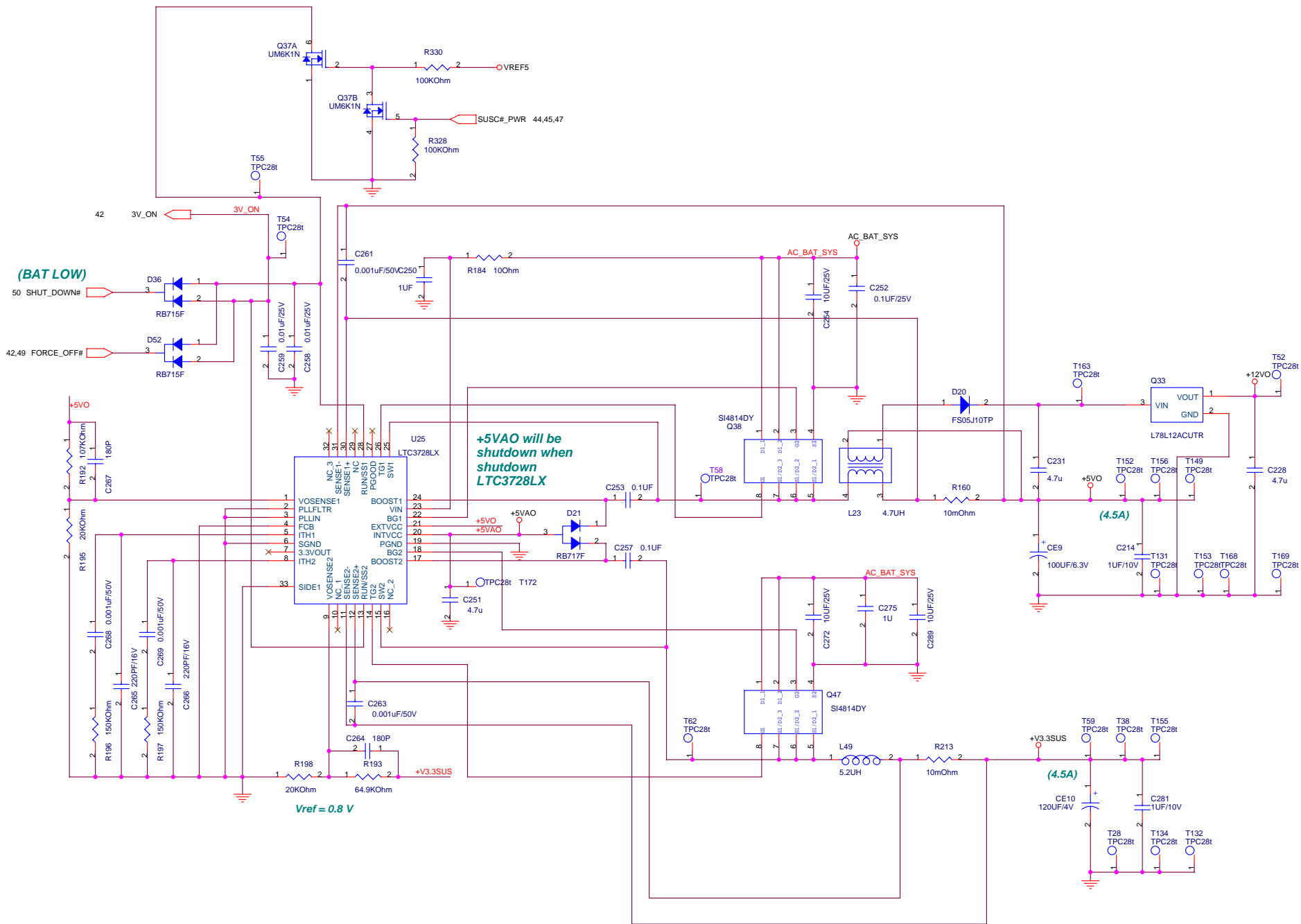
11-02



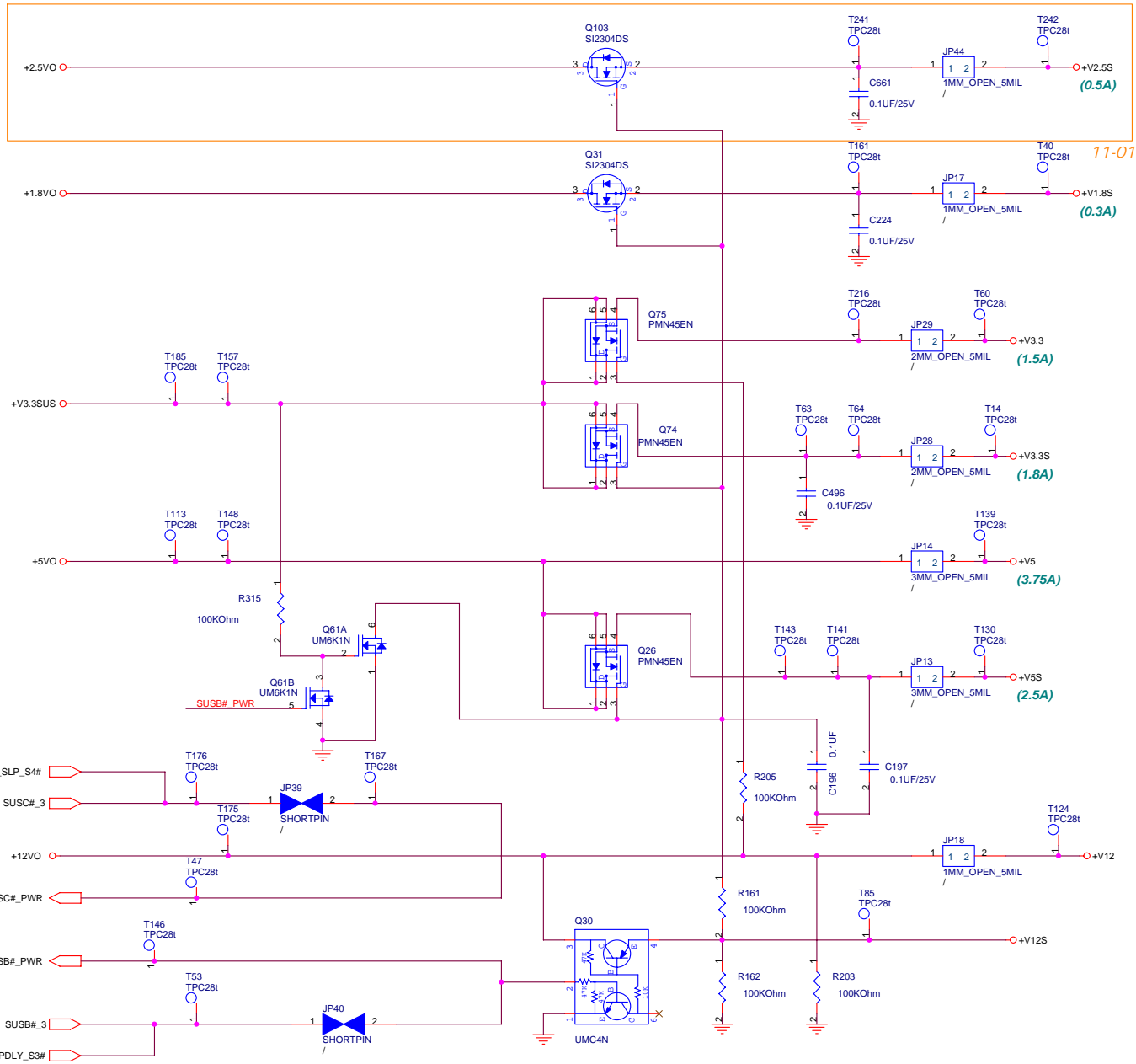


Change R148 for choosing 852 or 855 platform
 22K (10-003412230): 1.2V for 855GM/852GM
 30K (10-003413030): 1.35V for 855GME
 39.2K(10-003413932): 1.518V for 852GME/852GMV

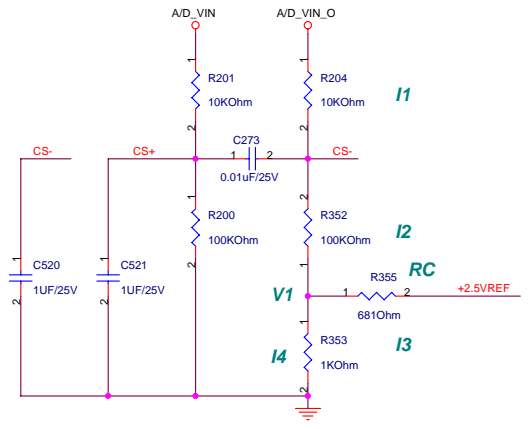
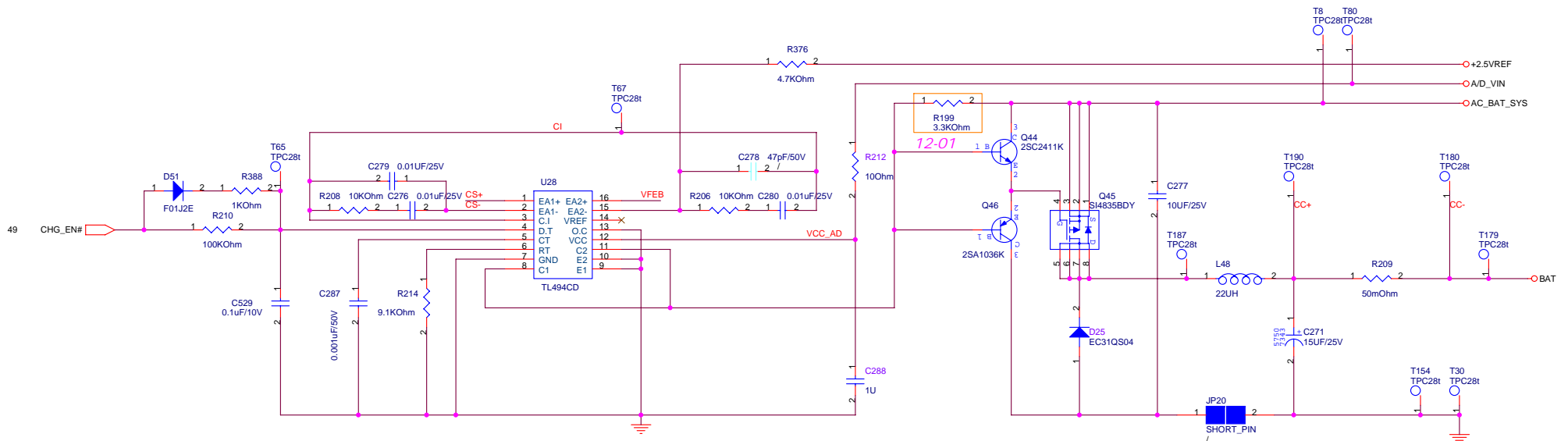
NB
 VCC,VCCASM,VCCHL,VCCAGPLL,VCCADPLLA,VCCADPLLB:
 855GM/852GM: 1.2V
 855GME: 1.35V
 852GME/852GMV: 1.5V



D
C
B
A

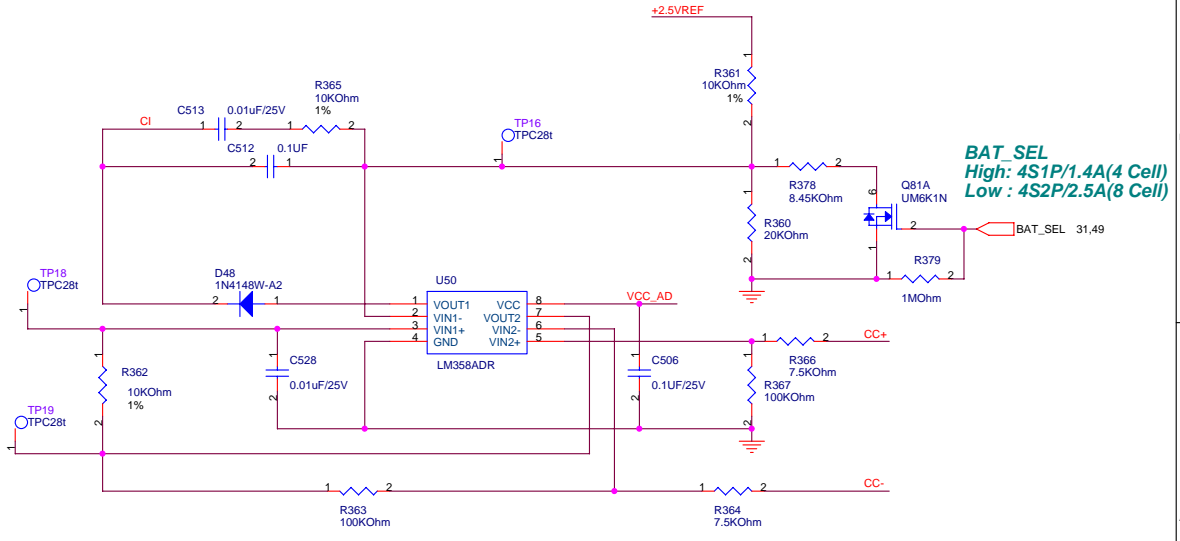
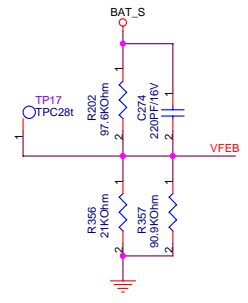


11-01

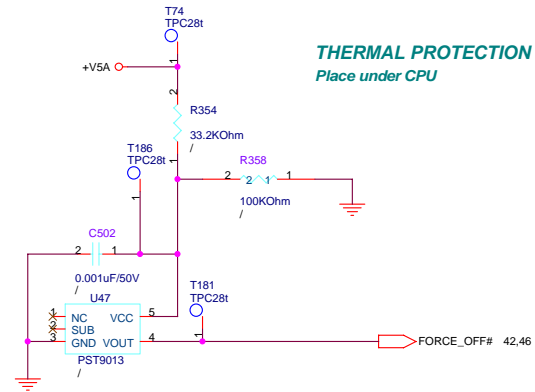
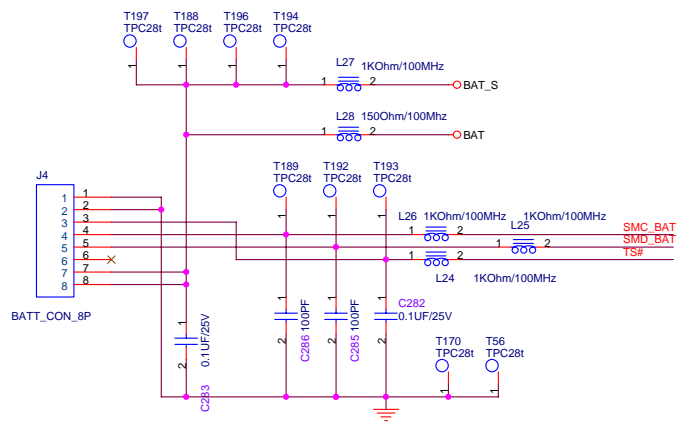
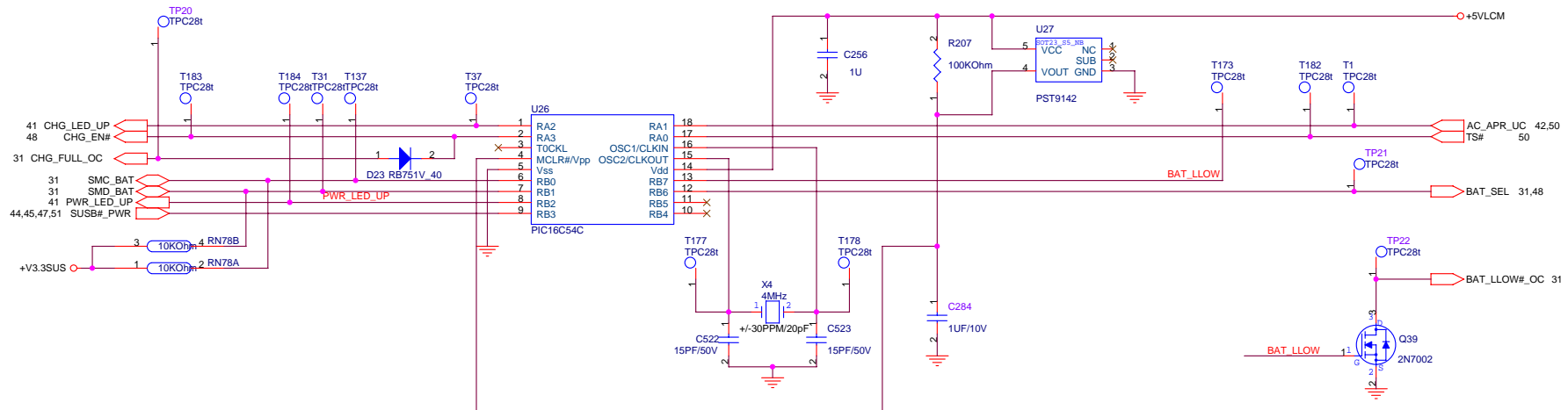


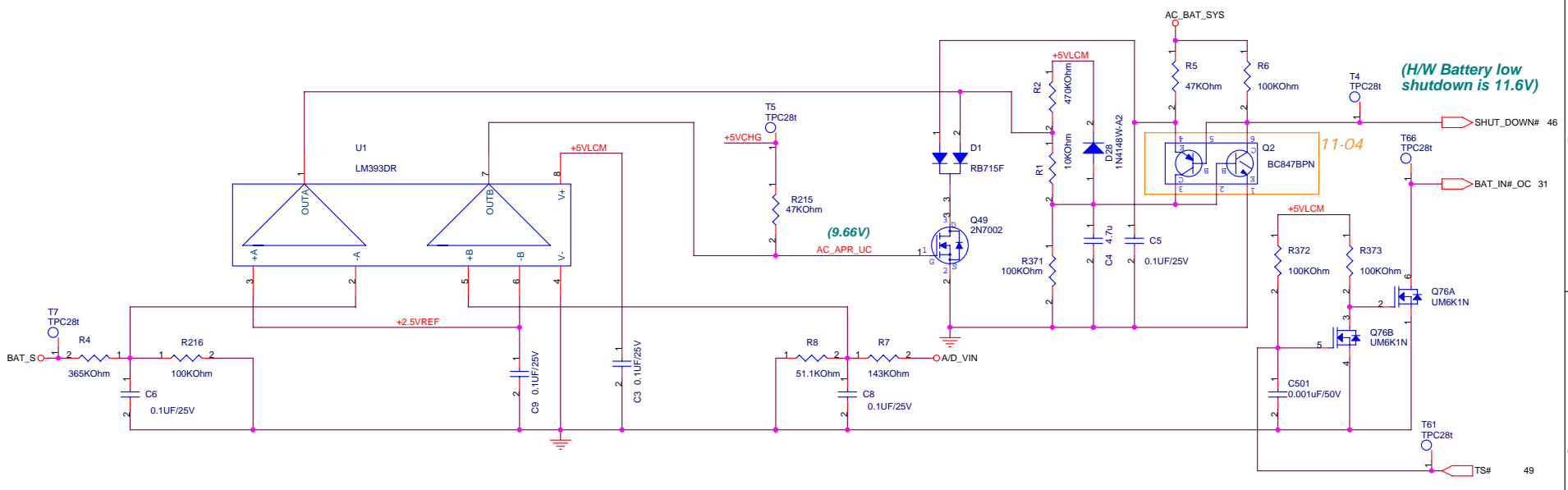
Current sharing = 3.1A

$A/D_VIN=19V$
 $A/D_VIN_O=19V-3.1A*50mohm=18.845V$
 $CS+=CS-=19*(100/110)=17.272727V$
 $I1=(18.845V-17.272727V)/10K=0.15723mA$
 $V1=17.272727V-(0.15723mA*100K)=1.5497V$
 $I4=1.5497V/1K=1.5497mA$
 $I3=1.5497mA-0.15723mA=1.39247mA$
 $RC=(2.5V-1.5497V)/1.39247mA=681\ ohm$

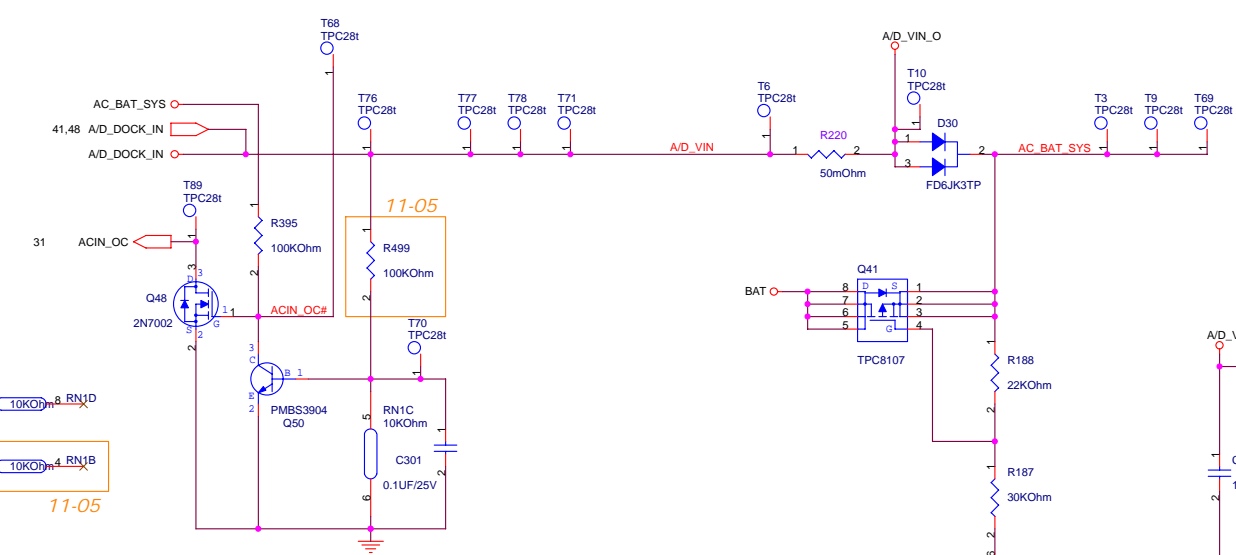


BAT_SEL
 High: 4S1P/1.4A(4 Cell)
 Low: 4S2P/2.5A(8 Cell)

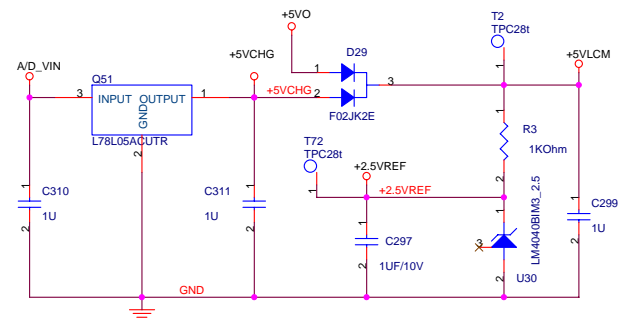


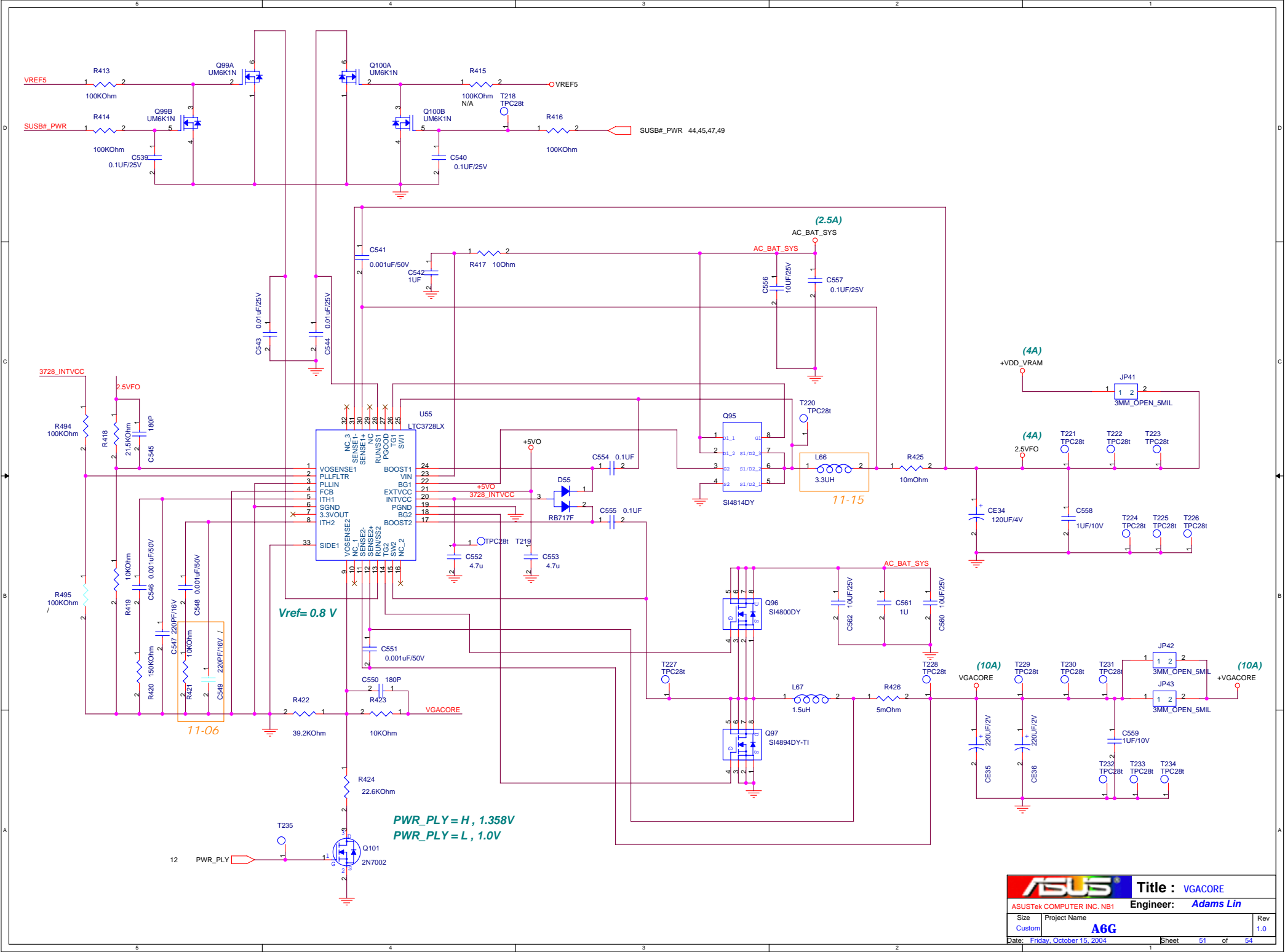


(H/W Battery low shutdown is 11.6V)

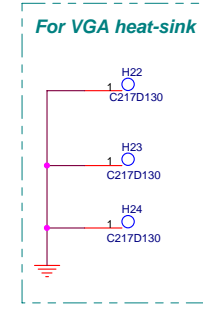
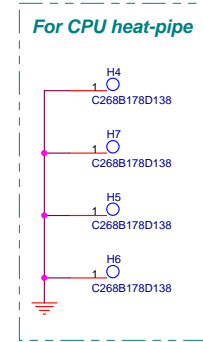
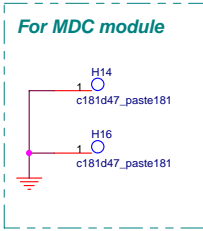
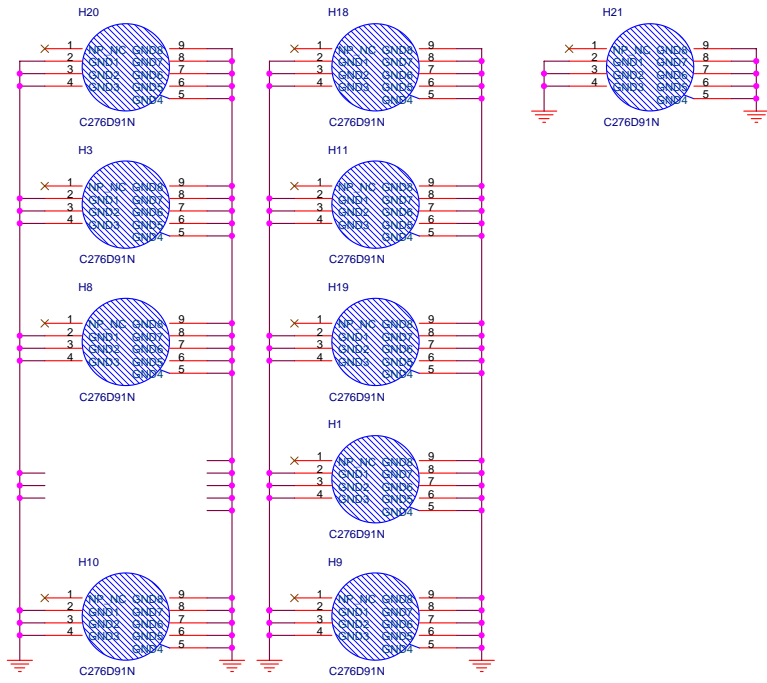


When system turn on by adapter power, "AC_APR_UC" will issue high, turn off Q41, to prevent AC power go into battery.



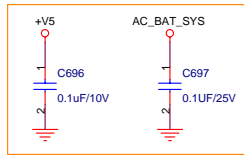


SCREW HOLE



Screw holes for PCMCIA socket are combined to PCMCIA socket footprint!

EMI CAP.



11-19

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 IN1
L4 IN2
L5 GND
L6 BOT

IMPEDENCE

Single-Ended

27.4 OHM WIDTH

TOP/BOT 18 mils

37.5 OHM WIDTH

TOP/BOT 11 mils
IN1/IN2 9.5 mils

42 OHM WIDTH

TOP/BOT 9 mils
IN1/IN2 7.5 mils

50 OHM WIDTH

TOP/BOT 6 mils
IN1/IN2 5 mils

55 OHM WIDTH

TOP/BOT 5.5 mils
IN1/IN2 4.5 mils

75 OHM WIDTH

TOP/BOT 4 mils
IN1/IN3 3.5 mils

Differential

70 OHM WIDTH/SPACE

TOP/BOT 9 mils/ 4 mils
IN1/IN2 7.5 mils/ 4 mils

85 OHM WIDTH/SPACE

TOP/BOT 5.5 mils/ 4 mils
IN1/IN2 4.5 mils/ 4 mils

90 OHM WIDTH/SPACE

TOP/BOT 5.5 mils/ 5 mils
IN1/IN2 4.5 mils/ 5 mils

100 OHM WIDTH/SPACE

TOP/BOT 6 mils/ 11 mils
IN1/IN2 5 mils/ 12 mils

110 OHM WIDTH/SPACE

TOP/BOT 5 mils/ 13 mils
IN1/IN2 4 mils/ 12 mils

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3S_CLK
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+V3.3SUS
VRM_PWRGD	I	+V3.3S
PM_STPCPU#	O	+V3.3S
CHG_LED	I	+5VLCM
RST_BTN#	O	OD
OTP_RESET#	I	+V5
SHUT_DOWN#	I	AC_BAT_SYS
+5VLCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3SUS
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_FULL_OC	I	+V3.3
PM_DPRSLPVR	O	+V3.3S
AC_APR_UC	I	+V5A
+V5A	PWR	VREF5
3V_ON	O	OD
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT	I/O	+V3.3
SMD_BAT	I/O	+V3.3

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	27A
+VCCP	1.05V	3.73A
+VGACORE	1.36V	10A
+VDD_VRAM	2.5V/1.8V	6.1A
+V1.2S	1.2V	3.1A
+V1.25S	1.25V	3A
+V1.5S	1.5V	1.58A
+V1.5SUS	1.5V	0.07A
+V1.8	1.8V	0.14A
+V1.8S	1.8V	0.445 A
+V2.5	2.5V	7.5A
+V2.5S	2.5V	0.384A
+V3.3	3.3V	2.07A
+V3.3S	3.3V	3A
+V3.3SUS	3.3V	0.5A
+V5	5V	1.01A
+V5S	5V	8.63A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

PCI INTERFACE

PCI_REQ#	
CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

PCI_GNT#	
CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL	
CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

PCI_INT#	
CB&1394	PCI_INTB/A/D#
MINIPCI	PCI_INTC/D#
LAN	PCI_INTC#

Power Jumper:

JP4: +V2.5 --Power In
 JP5: +V1.25S
 JP6: +V2.5
 JP7: +V1.2S
 JP9: +VCCP
 JP13: +V5S
 JP14: +V5
 JP15: +V1.5SUS
 JP16: +V2.5 --Power IN
 JP17: +V1.8S
 JP18: +V12
 JP19: +V1.8
 JP22: +V1.5S
 JP24: VREF-->+V5A
 JP26: +3VALWAYS_T-->+V3.3A
 (Don't Short)
 JP27: +3VALWAYS_M-->+V3.3A
 JP28: +V3.3S
 JP29: +V3.3
 JP32: KBCRSM
 JP41: +VDD_VRAM
 JP42: +VGACORE
 JP43: +VGACORE
 JP44: +V2.5S

SSID/SVID

DEVICE	SSID	SVID
LAN	1045	1043
MDC	1826	1043
1394	1897	1043
Audio	1893	1043
CardBUS	1894	1043
VGA (ATI M11-P)	1942	1043
VGA (ATI M11-CL)	1872	1043

Thermal

CPU Throttling(BIOS setting) :
 100 degree C.
 System shutdown(BIOS setting) :
 110 degree C.

Rev	Date	Description
R1.0	09/14 '04	First Release! <i>A6G platform is based on A6NE and adds external Graphics (ATI M11-P).</i>
R1.1 Orange Block	10/05 '04	<p>1. Power: Add +V2.5S power plane for VGA chip. Page 47.</p> <p>2. Power: Add a 0 ohm between signal "CPU_VRON" and U9. Page 43.</p> <p>3. Power: Add +2.5VO & +1.5VO sequence circuit. Page 45.</p> <p>4. Power: The original part (P/N:07-003034010) used for Q2 will be EOL. Change Q2 to new part (P/N:07-003188010). Page 50.</p> <p>5. Power: When the system temperature rise high due to the system running at heavy loading. The leak current(IR) of D30 schottky diode will be increased, the H/W AC detect circuit will make a wrong state. Net " ACIN_OC " will issue " high". To solve this problem, change RN1B (10K ohm) to R499 (100K ohm) to make sure it will issue "low" at this moment. Page 50.</p> <p>6. Power: Fine-tune R421 & C549 for current compensation. Page 51.</p> <p>7. Modify U32, R249, R251, R252 to according part. Page 6,7,8,9.</p> <p>8. Change CE15, CE18 from Tantalum Capacitor to OxiCap. Page 9.</p> <p>9. Factory finds that 47UF/6.3V Aluminum Electrolytic capacitor CE30, CE31 will fail at soldering process in A3 model. Change them to 47UF/6.3V OxiCap. Page 36.</p> <p>10. Factory finds that 100uF/6.3V Aluminum Electrolytic capacitor CE29, CE11, CE12 will fail at soldering process in A3 model. Change them to 100uF/6.3V OxiCap. Page 17,39.</p> <p>11. Reserve C694, C695 to fine-tune SMBUS signal quality. Page 20.</p> <p>12. Change C659 to Page 12, C660 to Page 23 to correspond with their actual layout location. Page 12,23.</p> <p>13. Because M11-P and M11-CL have different Chip ID, we don't need the VGA chip GPIO10 to choose GPU type. Reserve it for other use. Page 12.</p> <p>14. Change SW1-SW5 pad for SMT Manufacturability Improve. Page 41.</p> <p>15. Power: Change L66 to 3.3uH (P/N: 09-02X333C00). Page 51.</p> <p>16. Modify Audio AMP (U7) from GMT G1420 to TI TPA0102 for cost-down. Page 36.</p> <p>17. Base on Factory's request : modify D-SUB CN7, CON9 (only for 1.6mm thickness PCB). Page 18,33.</p> <p>18. To decrease the part type on M/B, change SW6 to 5-pin switch same as SW1-SW5. Page 42.</p> <p>19. EMI: Add L81, C696,C697. Page 36,52.</p> <p>20. BUG: system cannot be turn-off. The reason is that PCI clock for ICH4-M should be Free-Running, but in A6G R1.0 we swap it with PCI clock for KBC. Change it back in A6G R1.0. Page 23.</p> <p>21. Modify net name. Page 23.</p> <p>22. Power: Change R199 from 3.3K ohm/0603 to 3.3K ohm/0805 (P/N: 10-002303320). Page 48.</p> <p>23. Mount LED5 for A6 ID2. Page 41.</p>

Rev	Date	Description
R2.0 Pink Block		1. Power: Change R199 from 3.3K ohm/0603 to 3.3K ohm/0805 (P/N: 10-002303320). Page 48.