

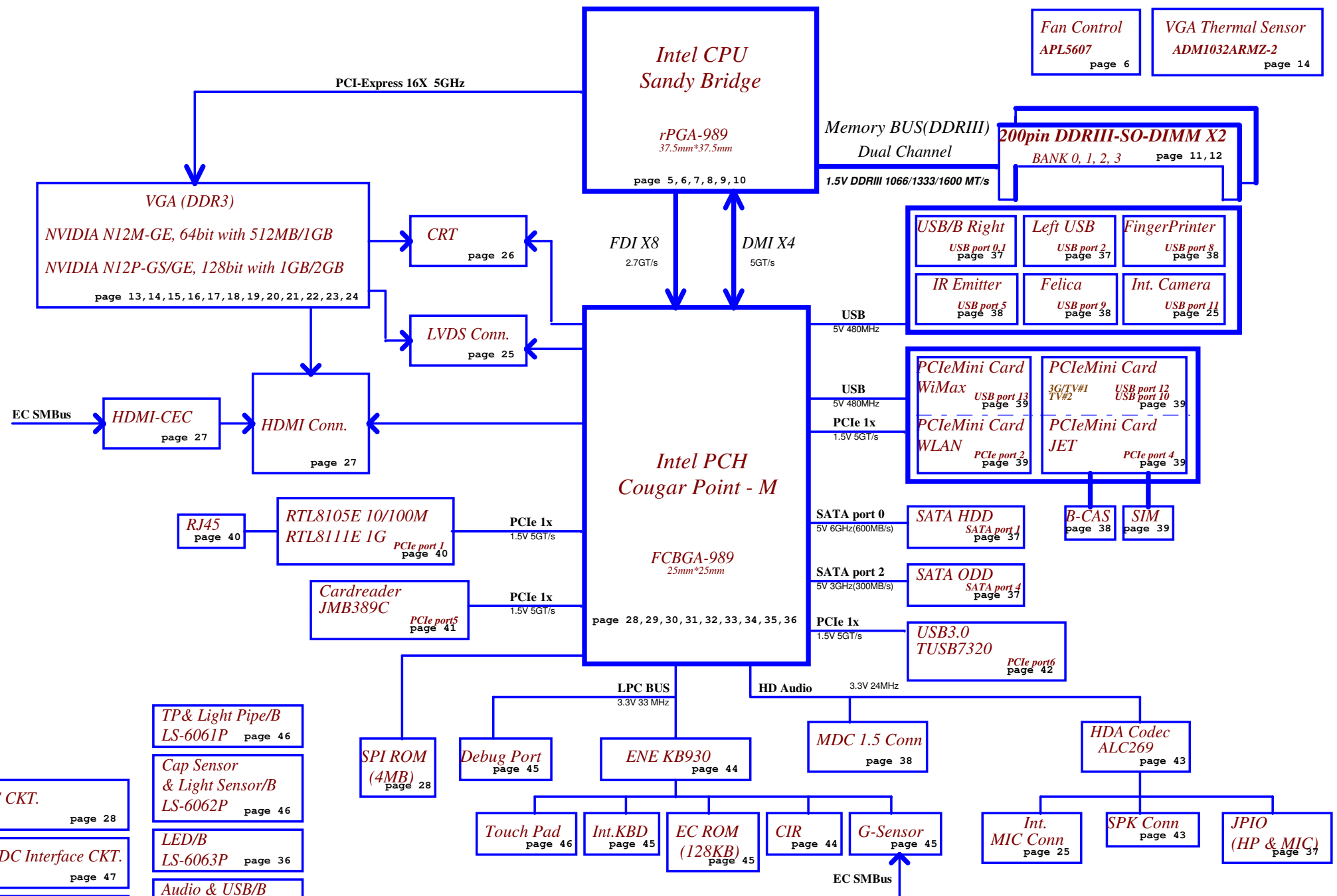
PHQAA

Marseille 10R/10RG

LA-6831P REV 0.3 Schematic

Intel Processor (Sandy Bridge) / PCH (Cougar Point)
2010-07-05 Rev 0.1

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				Cover Page		
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RTC CKT. page 28

DC/DC Interface CKT. page 47

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Cap Sensor & Light Sensor/B LS-6062P page 46

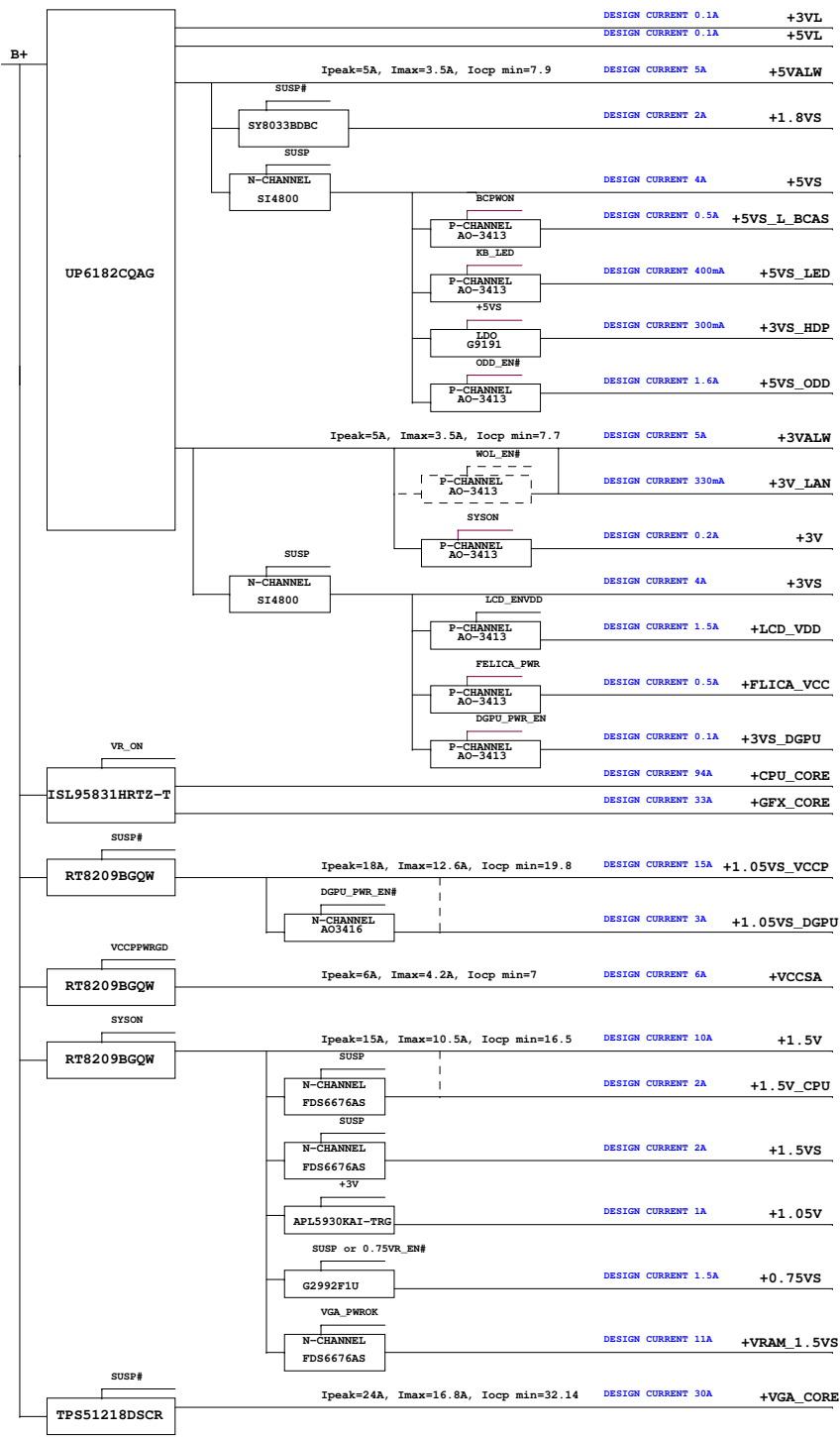
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane	+RTCVC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
State						
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

Platform	SKU	CPU	PCH	VGA
Calpella	UMA (OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

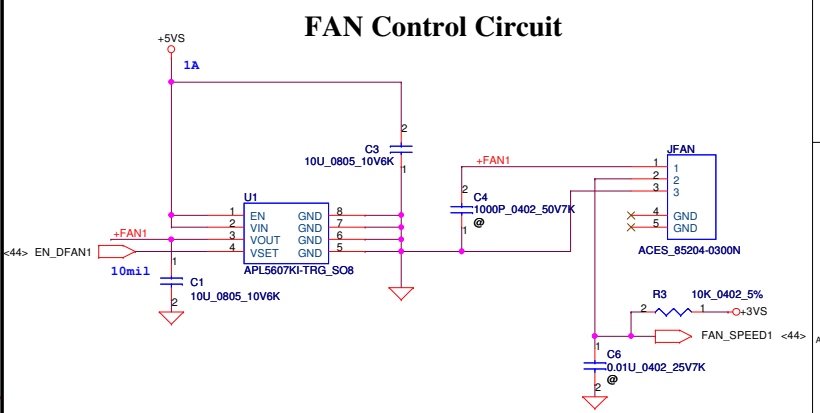
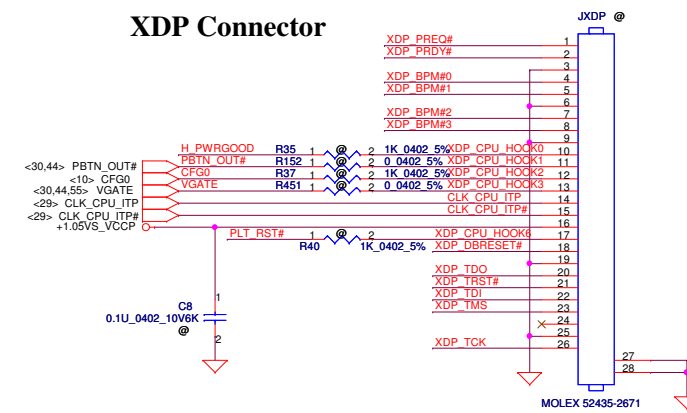
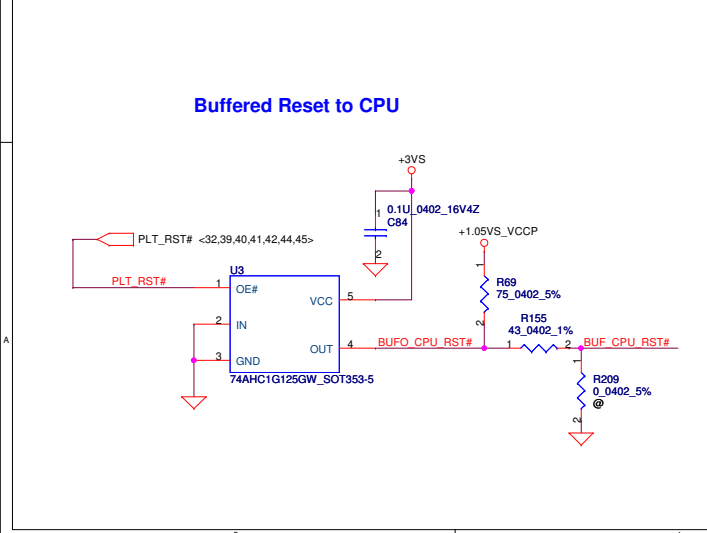
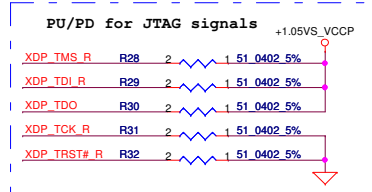
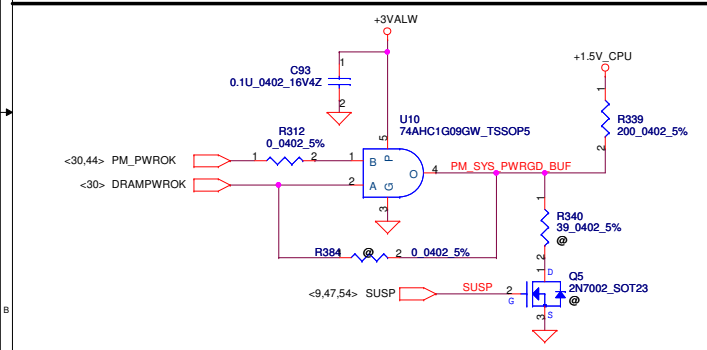
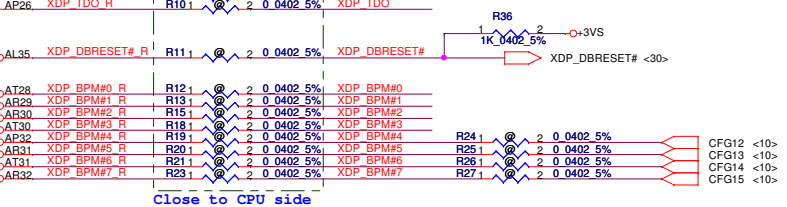
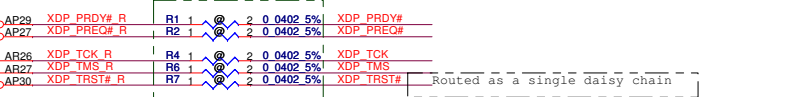
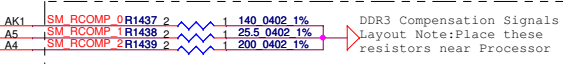
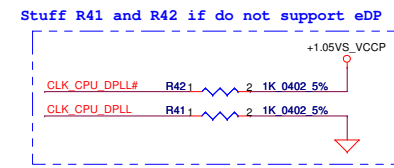
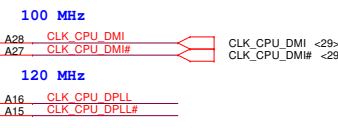
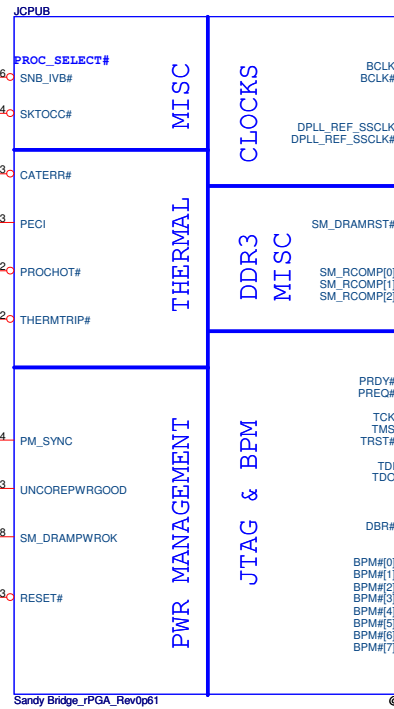
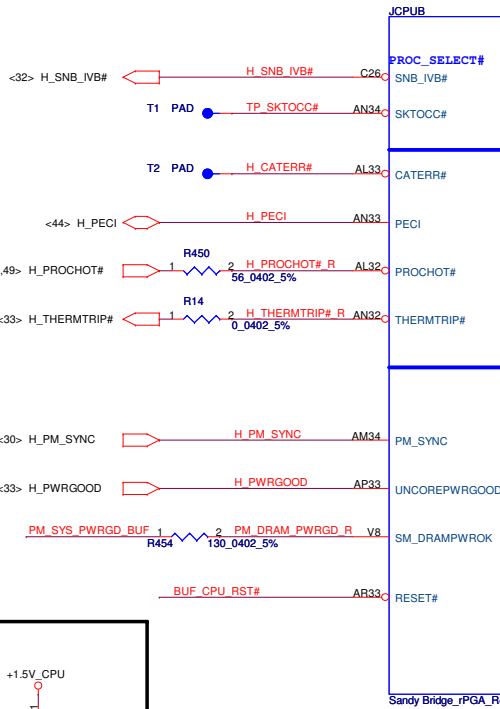
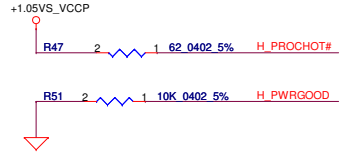
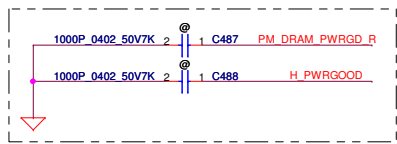
Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete	Optimus	Camera & Mic	
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving			GPU				
description	S3 Power Saving			N11P & N11E			N11M	
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

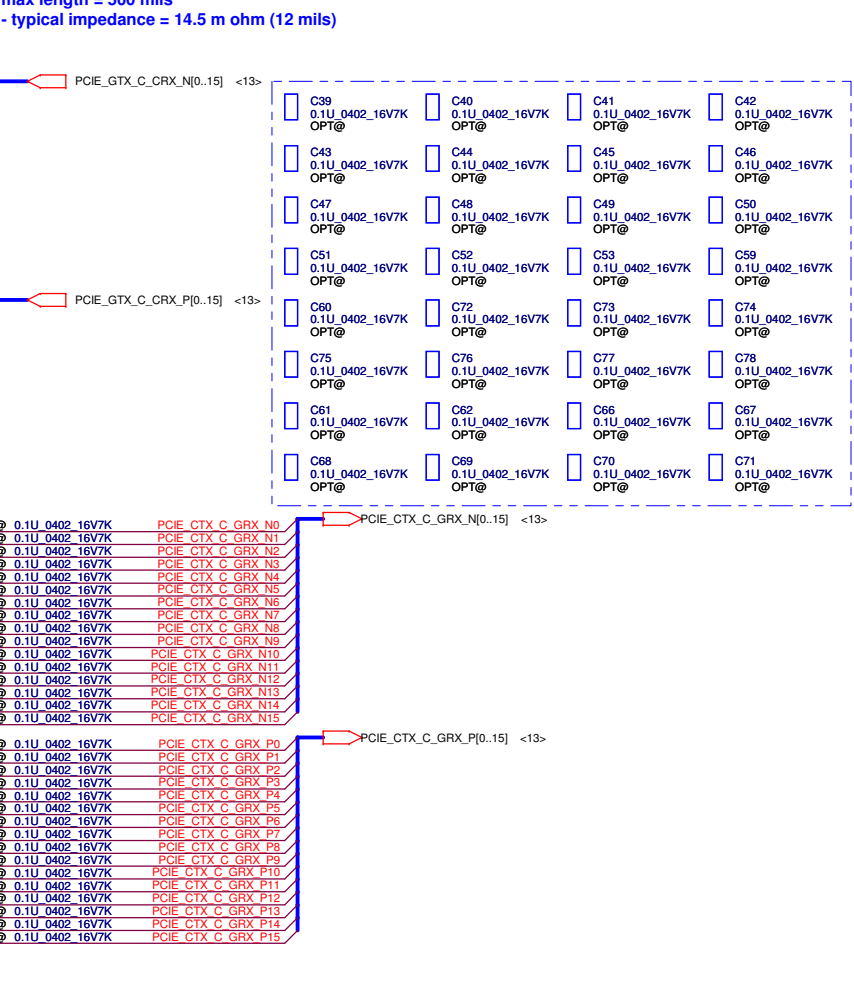
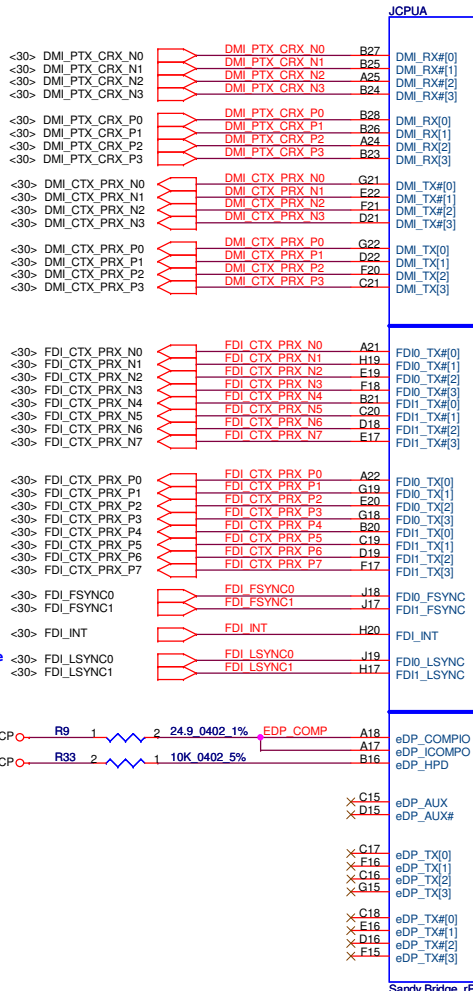
Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

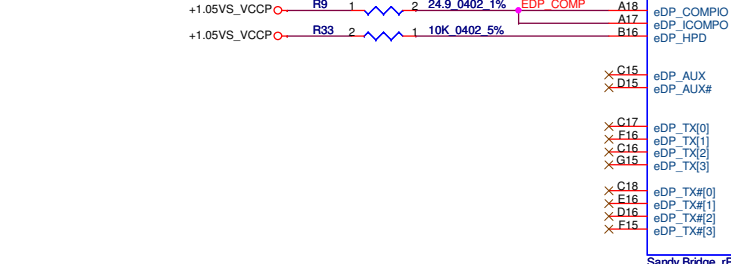


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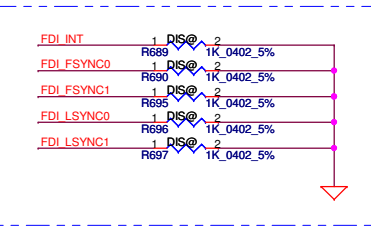
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)



eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm

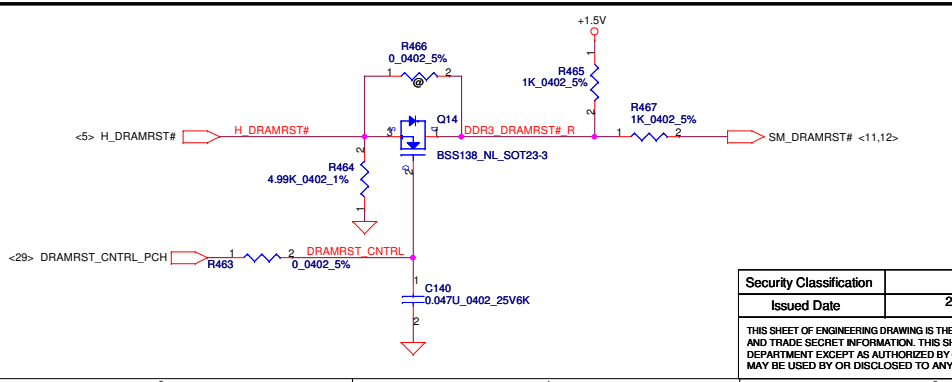
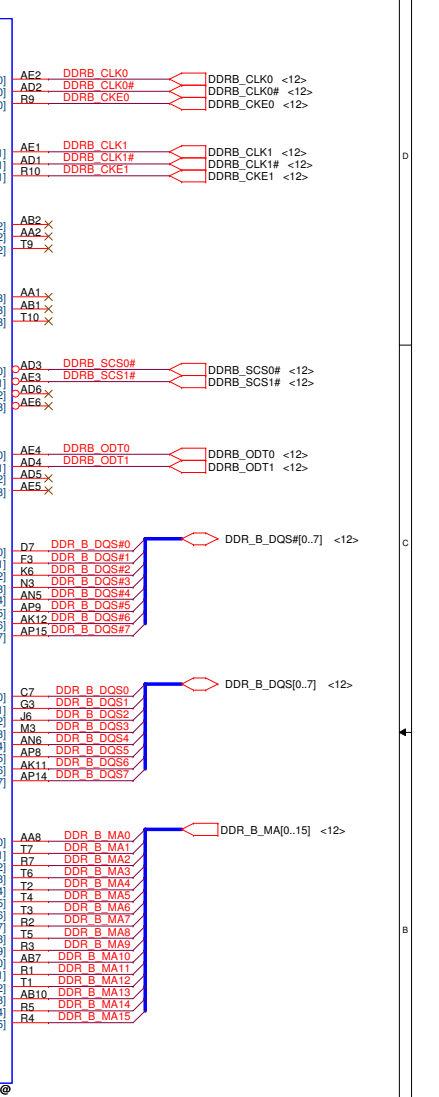
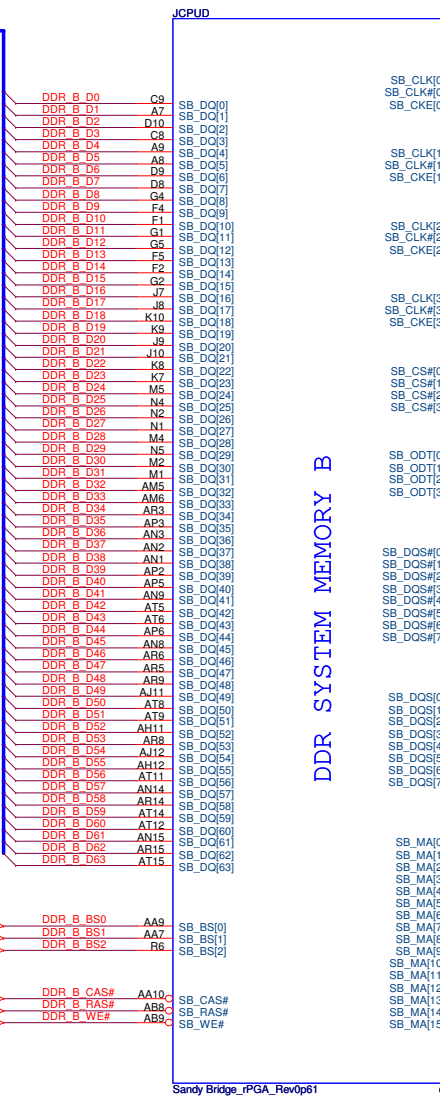
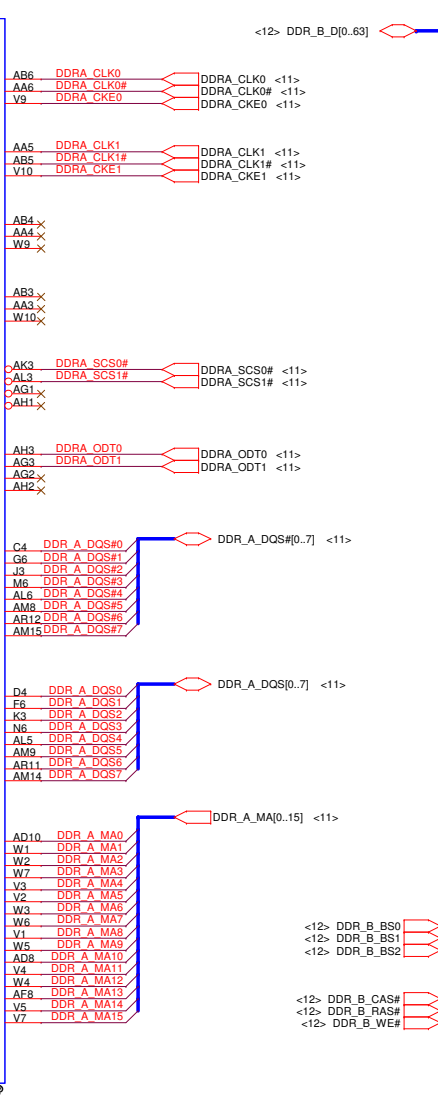
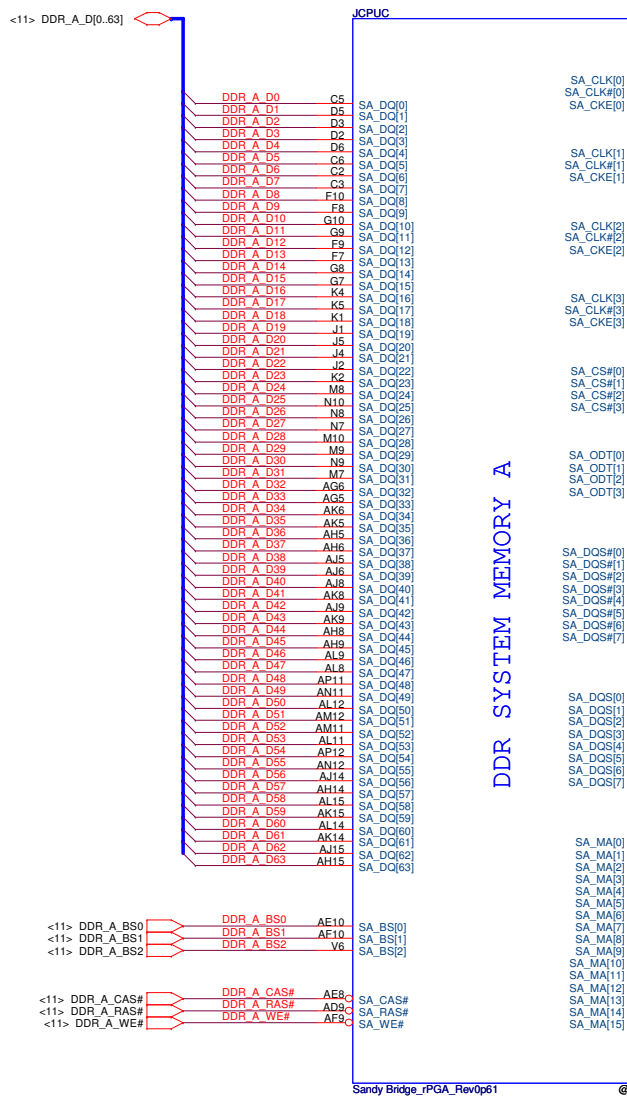


Close to CPU



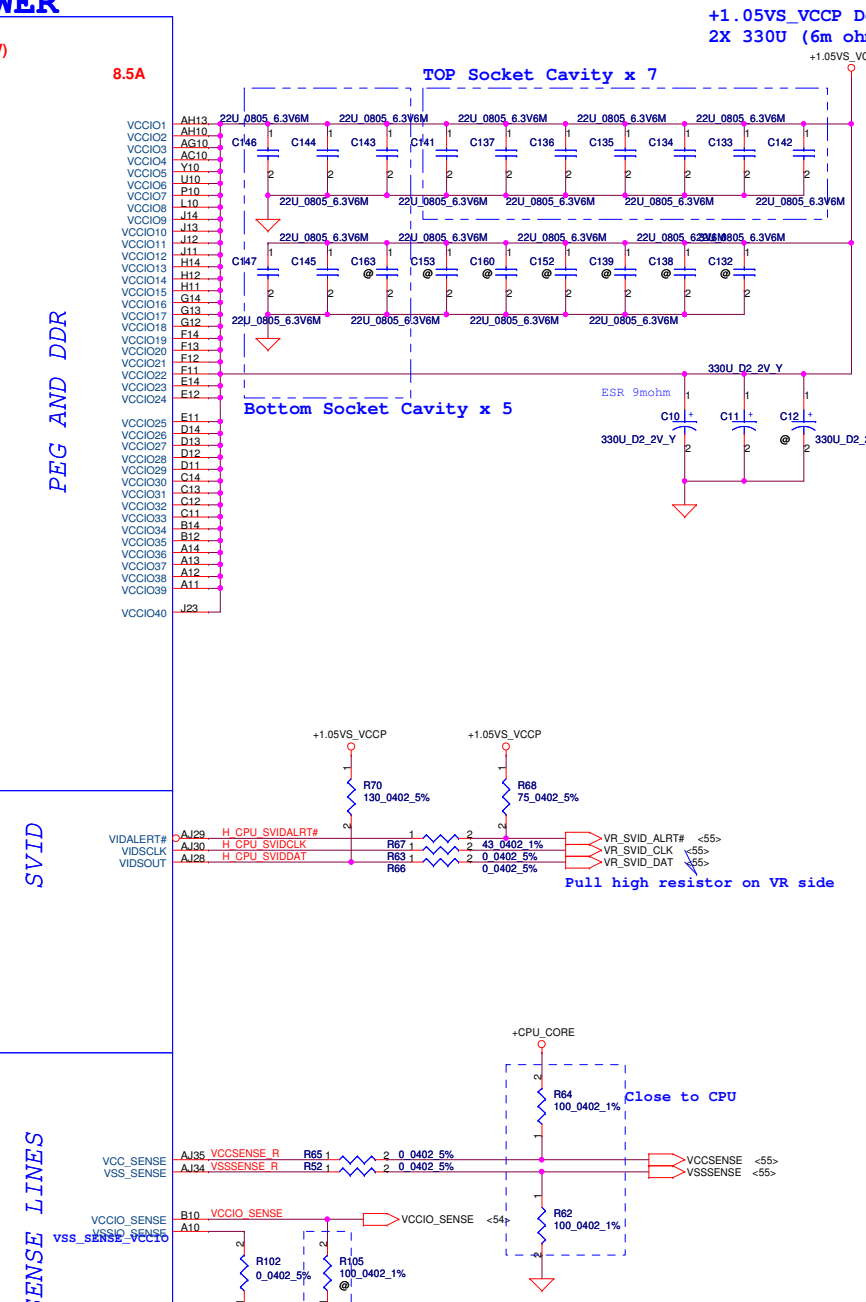
Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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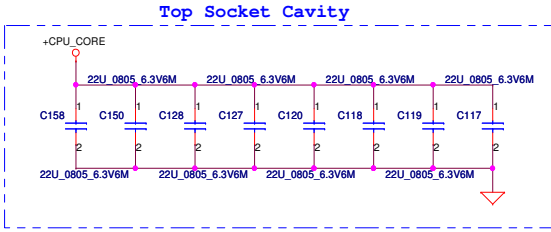
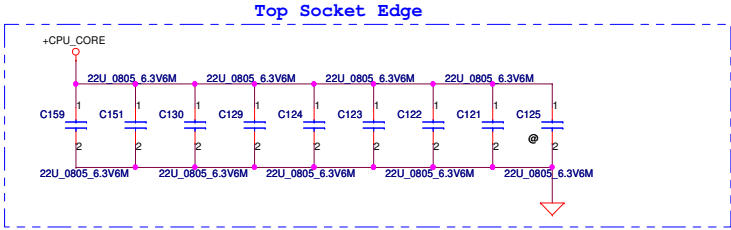
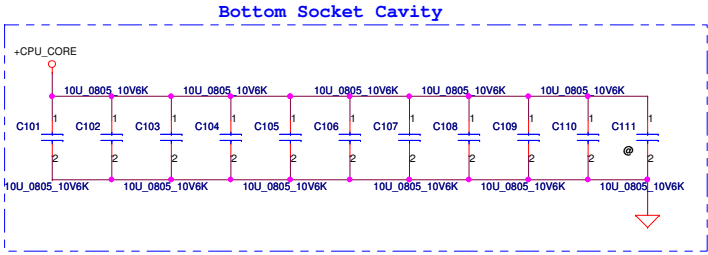
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- POWER**
- 94A (Quad Core 45W)
53A (SV 35W)
- PEG AND DDR**
- CORE SUPPLY**
- SVID**
- SENSE LINES**
- AG35 VCC1
 - AG34 VCC2
 - AG33 VCC3
 - AG32 VCC4
 - AG31 VCC5
 - AG30 VCC6
 - AG29 VCC7
 - AG28 VCC8
 - AG27 VCC9
 - AG26 VCC10
 - AF35 VCC11
 - AF34 VCC12
 - AF33 VCC13
 - AF32 VCC14
 - AF31 VCC15
 - AF30 VCC16
 - AF29 VCC17
 - AF28 VCC18
 - AF27 VCC19
 - AD35 VCC20
 - AD34 VCC21
 - AD33 VCC22
 - AD32 VCC23
 - AD31 VCC24
 - AD30 VCC25
 - AD29 VCC27
 - AD28 VCC28
 - AD27 VCC29
 - AD26 VCC30
 - AC35 VCC31
 - AC34 VCC32
 - AC33 VCC33
 - AC32 VCC34
 - AC31 VCC35
 - AC30 VCC36
 - AC29 VCC37
 - AC28 VCC38
 - AC27 VCC39
 - AC26 VCC40
 - AA35 VCC41
 - AA34 VCC42
 - AA33 VCC43
 - AA32 VCC44
 - AA31 VCC45
 - AA30 VCC46
 - AA29 VCC47
 - AA28 VCC48
 - AA27 VCC49
 - AA26 VCC50
 - Y35 VCC51
 - Y34 VCC52
 - Y33 VCC53
 - Y32 VCC54
 - Y31 VCC55
 - Y30 VCC56
 - Y29 VCC57
 - Y28 VCC58
 - Y27 VCC59
 - Y26 VCC60
 - V35 VCC61
 - V34 VCC62
 - V33 VCC63
 - V32 VCC64
 - V31 VCC65
 - V30 VCC66
 - V29 VCC67
 - V28 VCC68
 - V27 VCC69
 - V26 VCC70
 - U35 VCC71
 - U34 VCC72
 - U33 VCC73
 - U32 VCC74
 - U31 VCC75
 - U30 VCC76
 - U29 VCC77
 - U28 VCC78
 - U27 VCC79
 - U26 VCC80
 - R35 VCC81
 - R34 VCC82
 - R33 VCC83
 - R32 VCC84
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 - R30 VCC86
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 - R27 VCC89
 - R26 VCC90
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 - P34 VCC92
 - P33 VCC93
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 - P29 VCC97
 - P28 VCC98
 - P27 VCC99
 - P26 VCC100

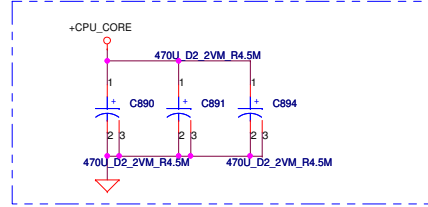


+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

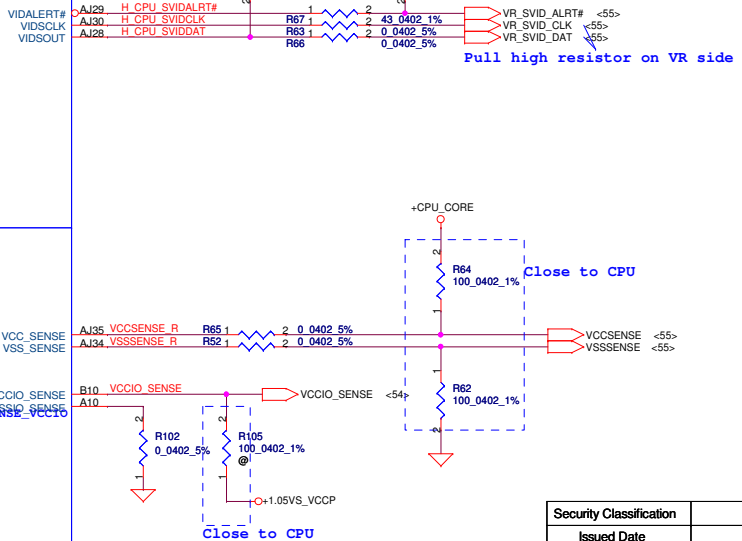
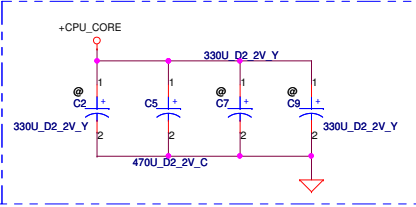
+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U



Co-Lay with C2, C5, C7, C9



Bottom Socket Edge



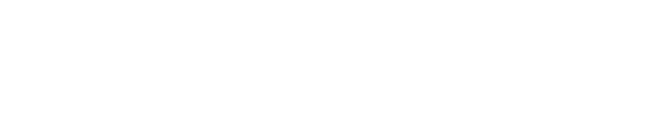
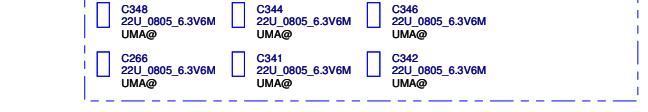
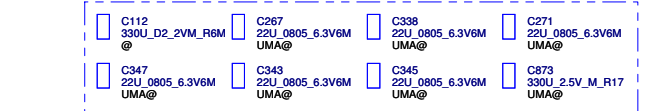
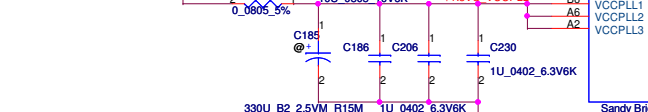
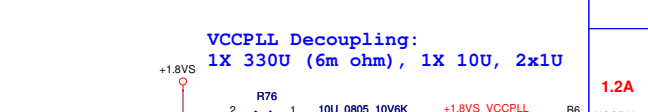
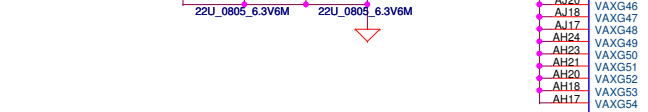
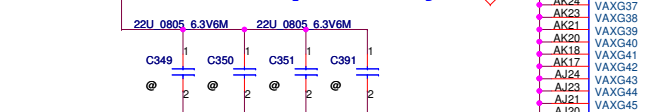
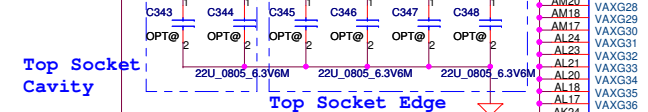
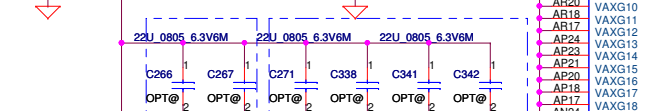
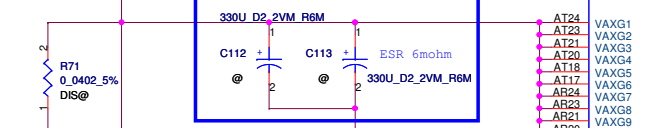
Pull high resistor on VR side

Close to CPU

Close to CPU

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+GFX_CORE Decoupling:
2X 470U (4m ohm), 12X 22U



POWER

SENSE LINES

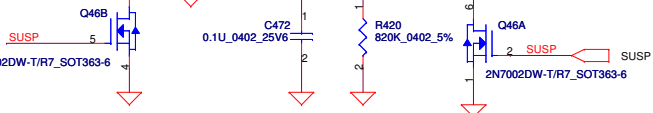
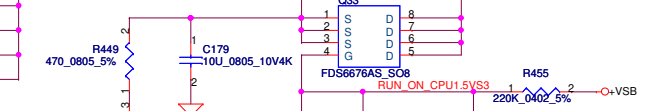
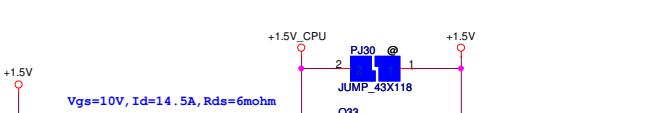
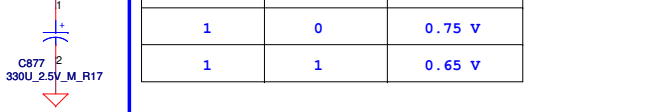
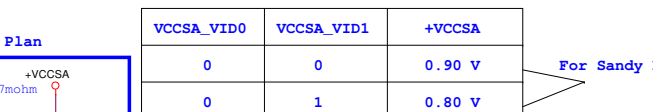
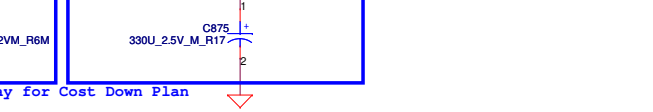
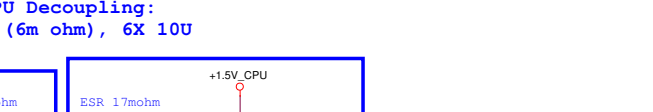
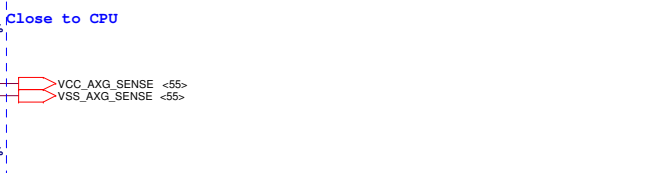
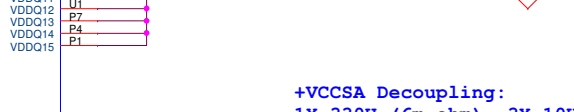
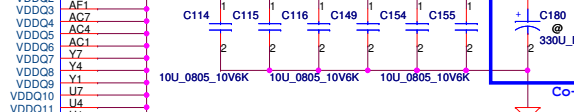
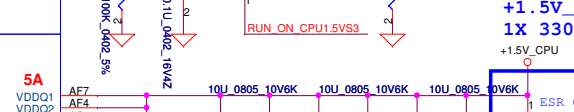
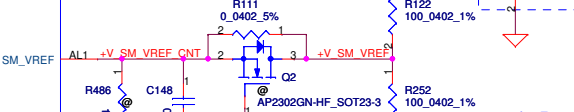
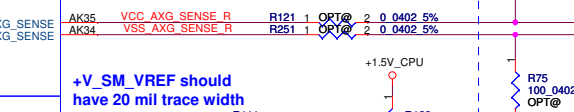
VREF

DDR3 -1.5V RAILS

SA RAIL

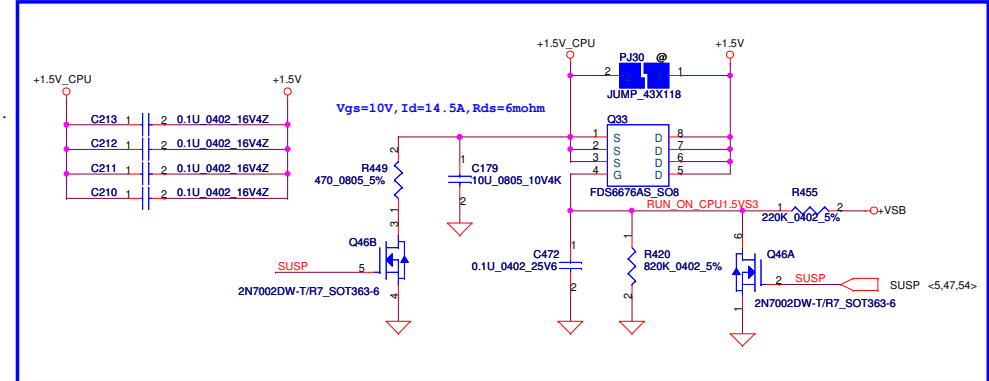
MISC

1.8V RAIL



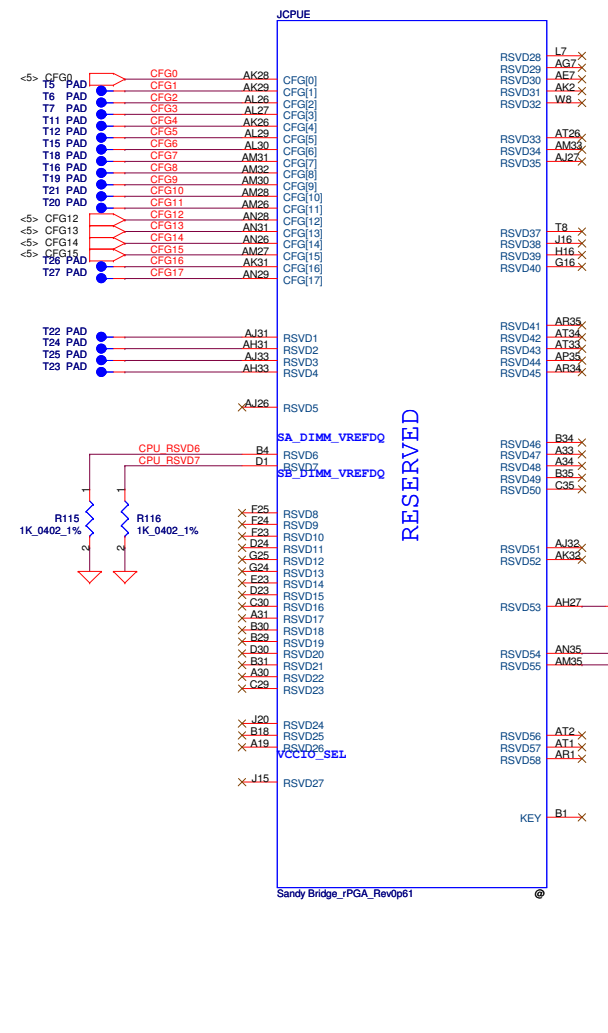
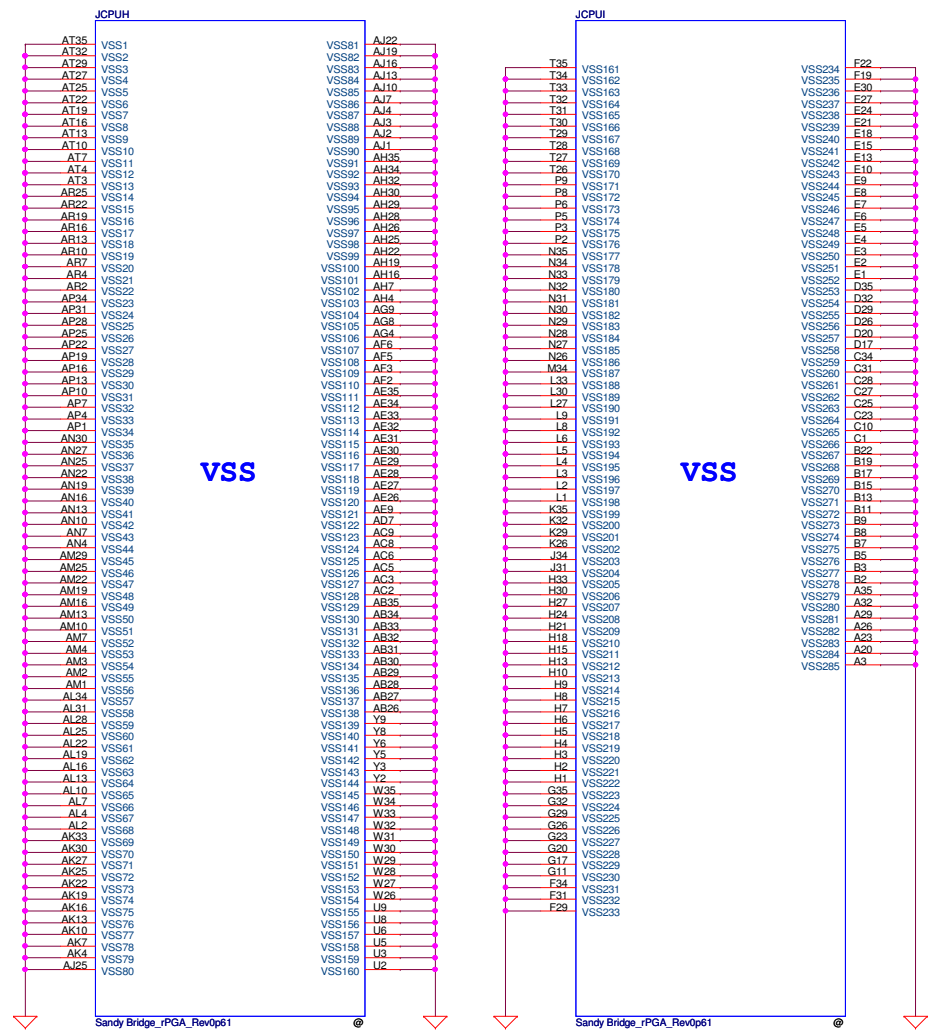
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

For Sandy Bridge



CFG Straps for Processor

(CFG[17:0] internal pull high to VCCIO)



PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	--

Embedded Display Port Presence Strap

CFG4	★ 1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
------	--

PCIE Port Bifurcation Straps

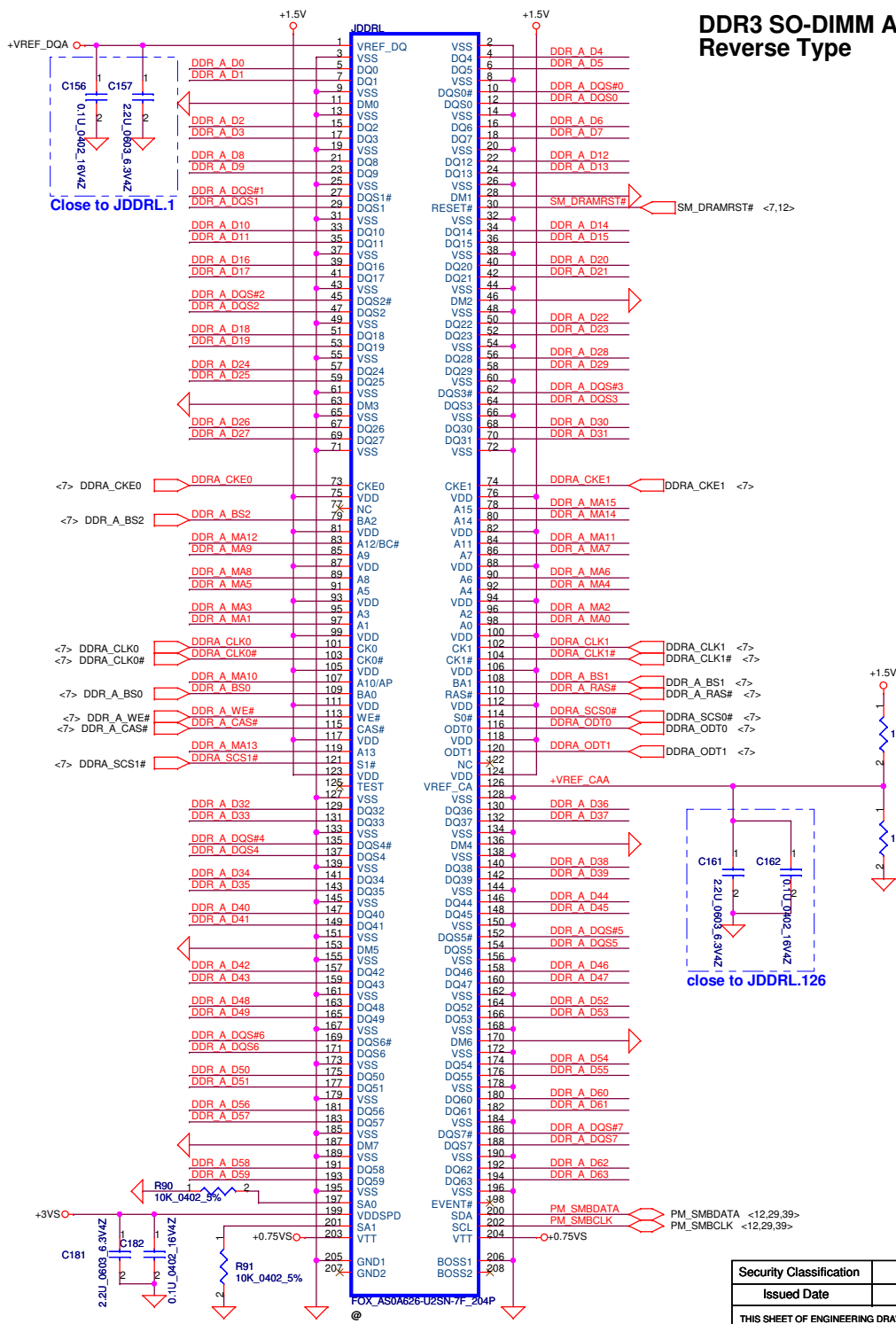
CFG[6:5]	★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
----------	--

PEG DEFER TRAINING

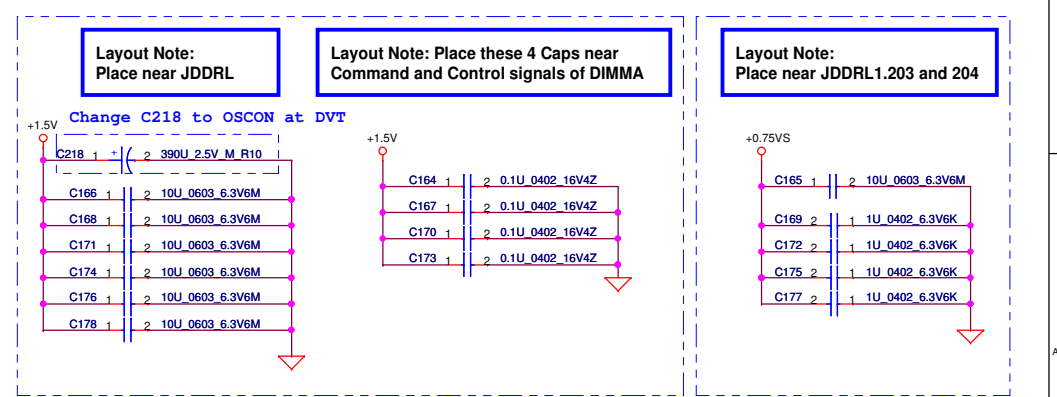
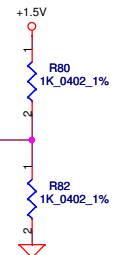
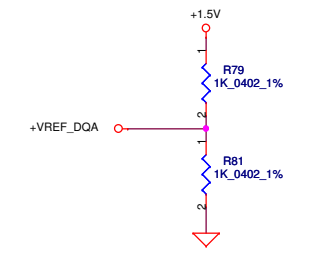
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---

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Date:	Thursday, October 07, 2010	Sheet	10	of 58

DDR3 SO-DIMM A Reverse Type

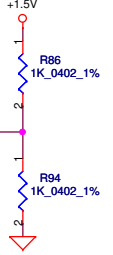
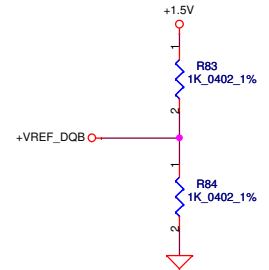
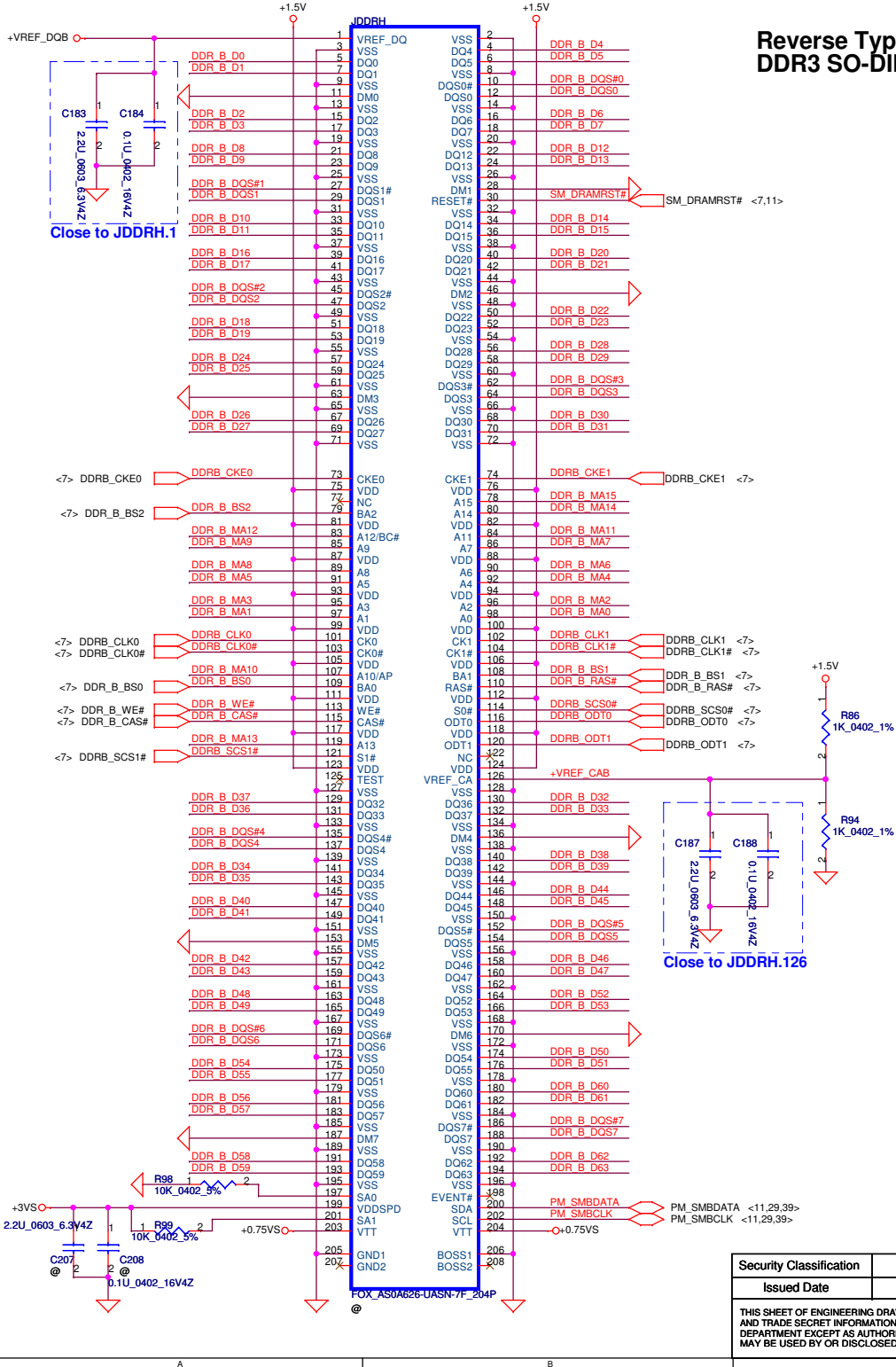


- DDR_A_DQS[0..7] <7>
- DDR_A_DQS#[0..7] <7>
- DDR_A_D[0..63] <7>
- DDR_A_MA[0..15] <7>



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Reverse Type DDR3 SO-DIMM B

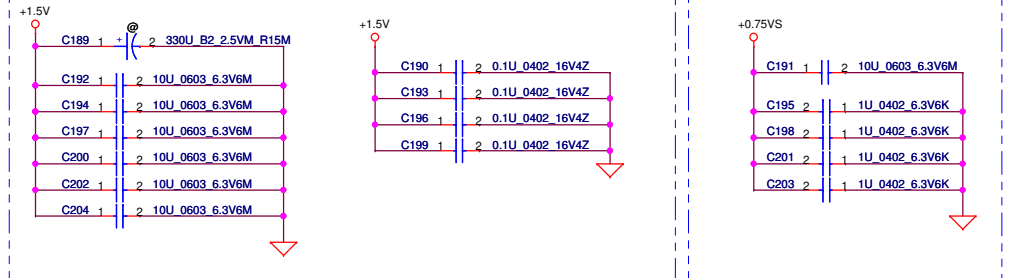


Close to JDDR.H.126

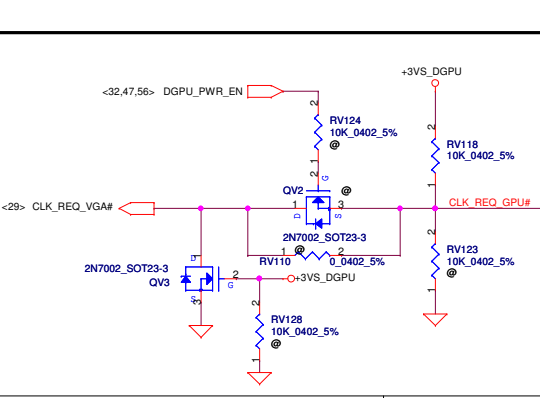
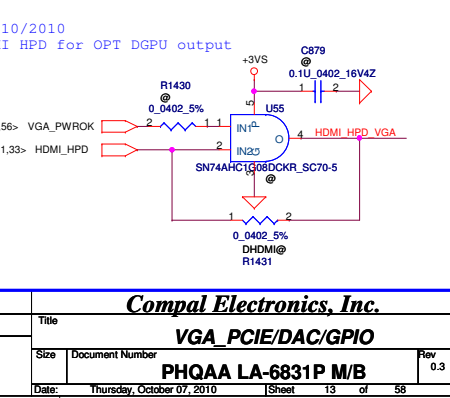
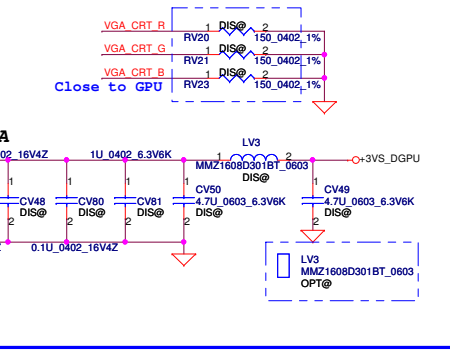
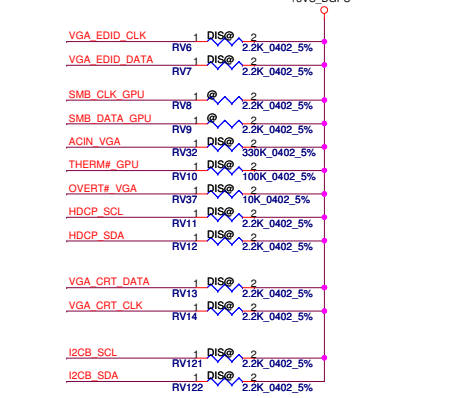
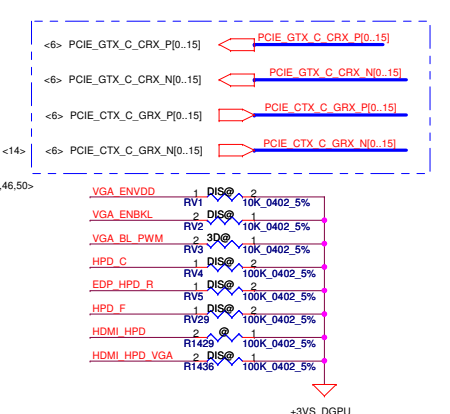
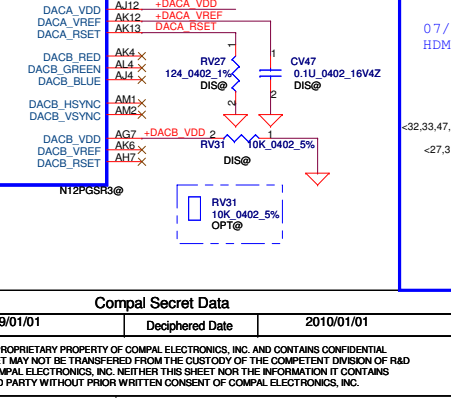
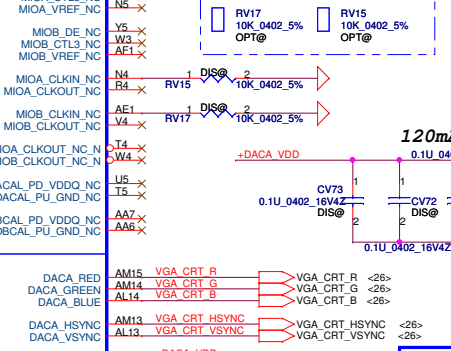
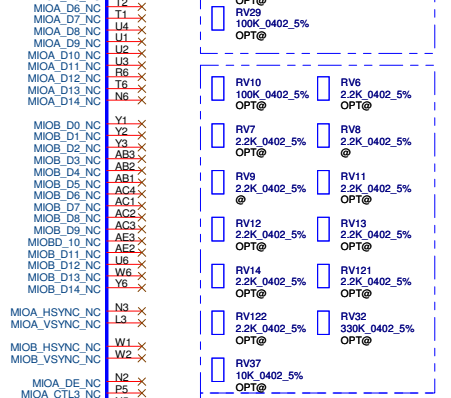
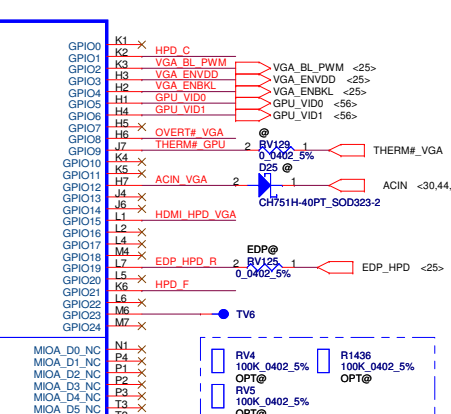
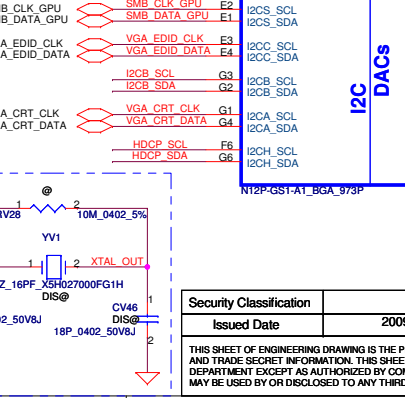
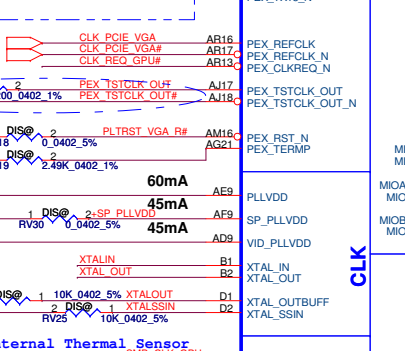
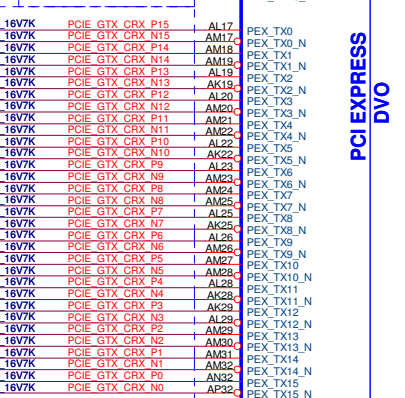
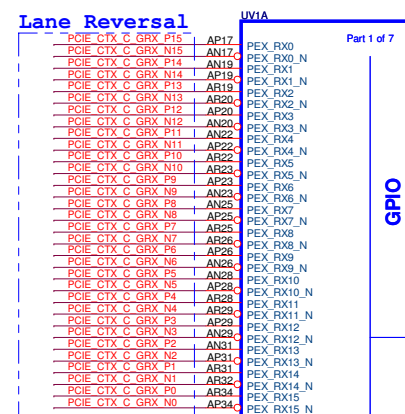
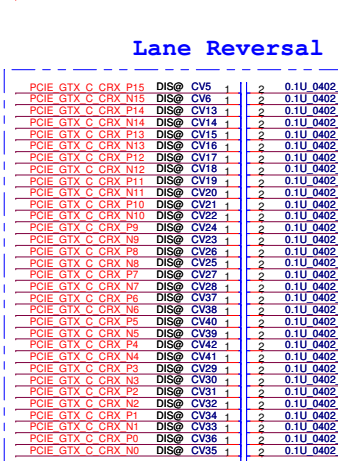
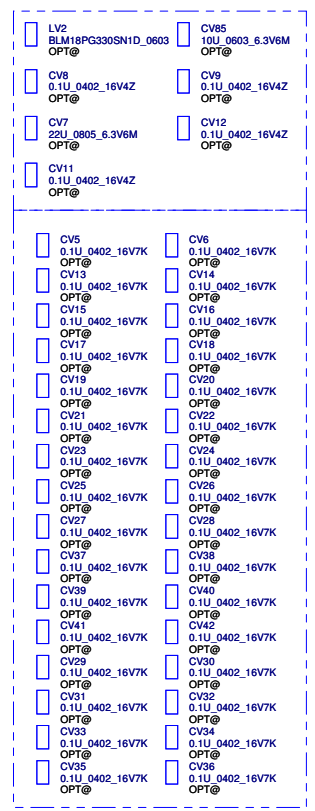
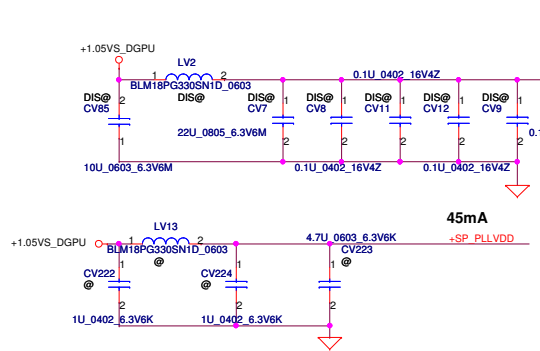
Layout Note:
Place near JDDR.H

Layout Note: Place these 4 Caps near
Command and Control signals of DIMM B

Layout Note:
Place near JDDR.H.203 and 204



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		2010/01/01

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07/10/2010
HDMI HPD for OPT DGPU output

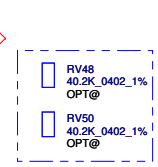
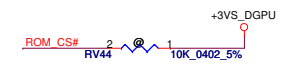
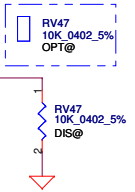
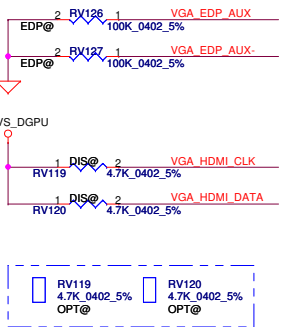
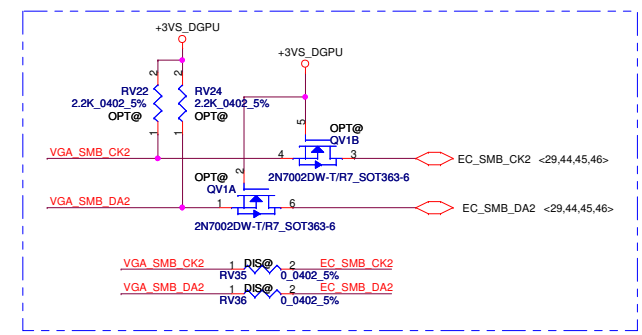
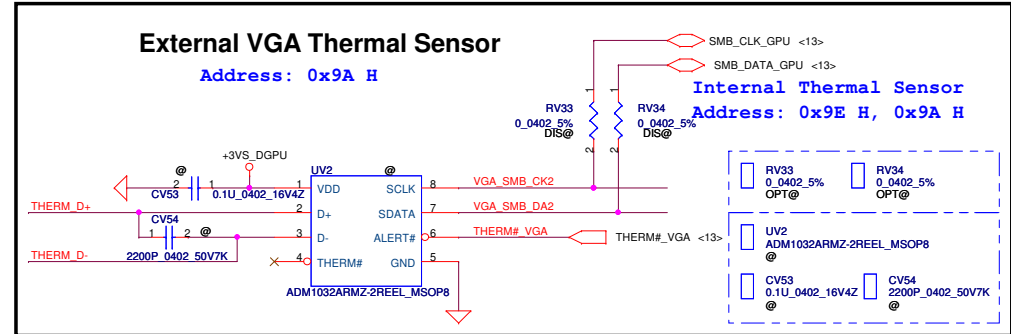
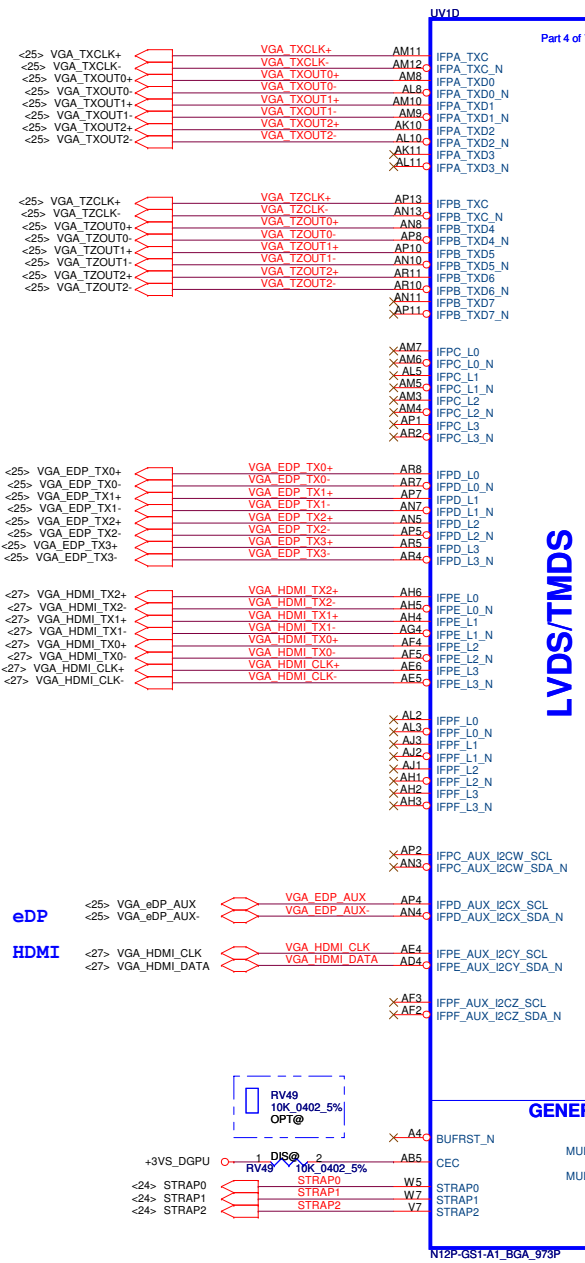
Compal Electronics, Inc.

VGA_PCIE/DAC/GPIO

PHQAA LA-6831P M/B

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For PHQAA EVT Phase only

Mode	VID1	VID0	+VGA_CORE
P0 (Cold)	1	1	0.95 V
P0	0	1	0.950V
P8/P12	0	0	0.825 V

N12M-GE Performance Mode

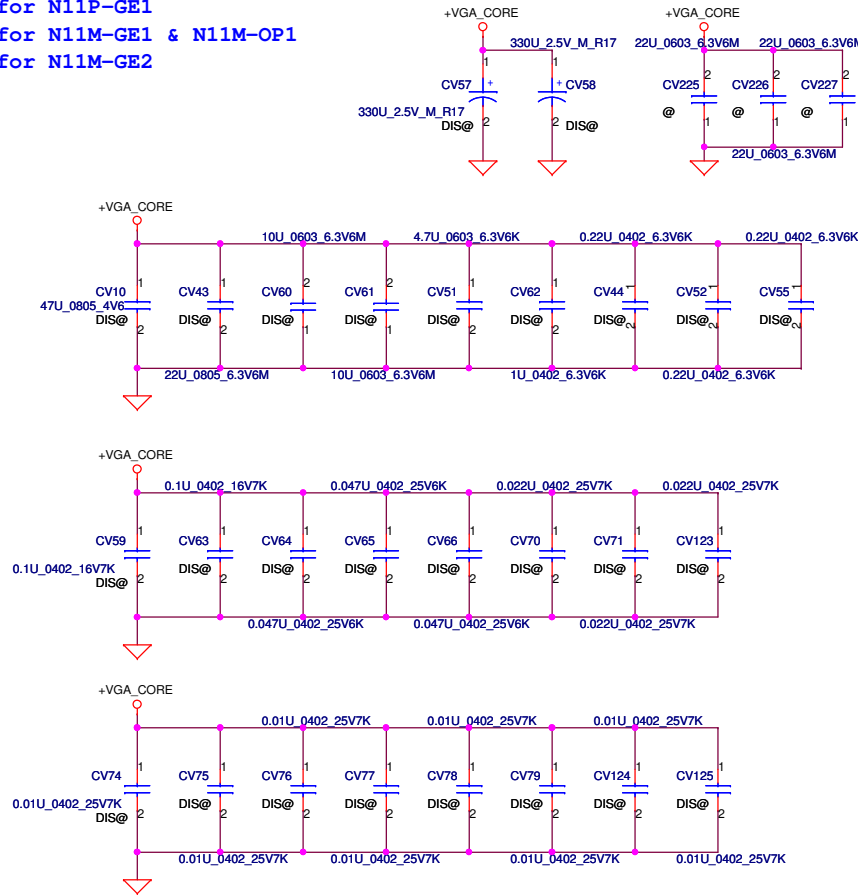
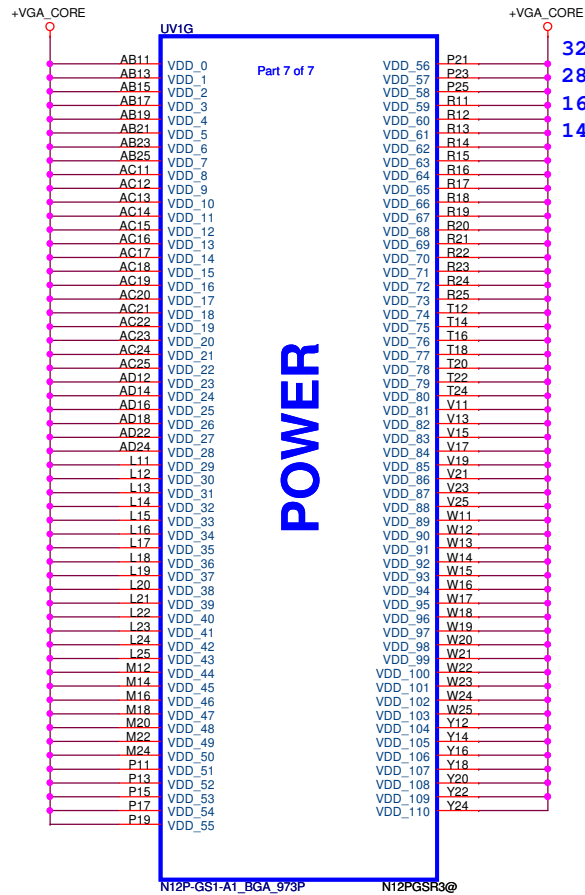
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	606	790	1.00 V
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

N12P-GS Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

N12P-GE Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

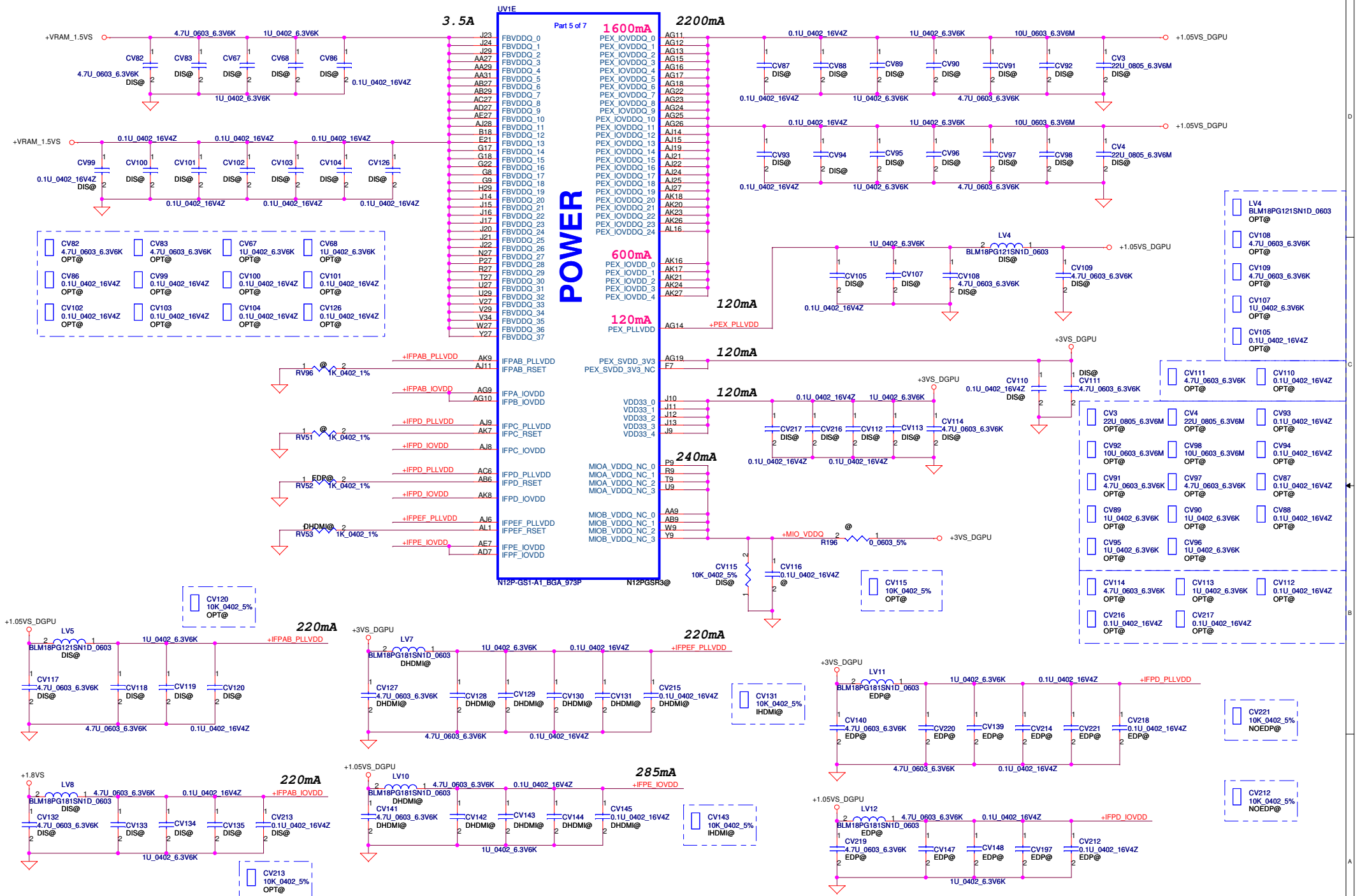


- CV225 22U_0603_6.3V6M @
- CV226 22U_0603_6.3V6M @
- CV57 330U 2.5V_M_R17 OPT@
- CV10 47U_0805_4V6 OPT@
- CV60 10U_0603_6.3V6M OPT@
- CV51 4.7U_0603_6.3V6K OPT@
- CV44 0.22U_0402_6.3V6K OPT@
- CV55 0.22U_0402_6.3V6K OPT@
- CV63 0.1U_0402_16V7K OPT@
- CV85 0.047U_0402_25V6K OPT@
- CV70 0.022U_0402_25V7K OPT@
- CV75 0.01U_0402_25V7K OPT@
- CV77 0.01U_0402_25V7K OPT@
- CV79 0.01U_0402_25V7K OPT@
- CV227 22U_0603_6.3V6M @
- CV58 330U 2.5V_M_R17 OPT@
- CV43 22U_0805_6.3V6M OPT@
- CV61 10U_0603_6.3V6M OPT@
- CV62 1U_0402_6.3V6K OPT@
- CV52 0.22U_0402_6.3V6K OPT@
- CV59 0.1U_0402_16V7K OPT@
- CV64 0.047U_0402_25V6K OPT@
- CV71 0.022U_0402_25V7K OPT@
- CV76 0.01U_0402_25V7K OPT@
- CV78 0.01U_0402_25V7K OPT@
- CV124 0.01U_0402_25V7K OPT@

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Issued Date	2009/01/01	Deciphered Date	2010/01/01

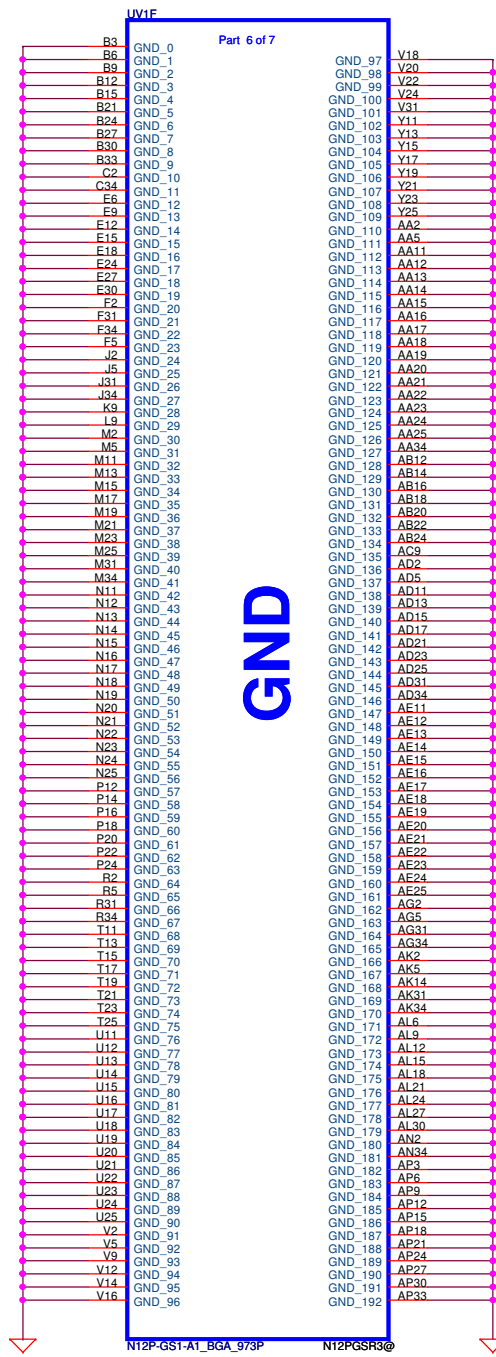
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Title			Rev
<p align="center">Compal Electronics, Inc.</p> <p align="center">VGA_VGA CORE</p>			
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Compal Electronics, Inc.		
VGA_POWER		
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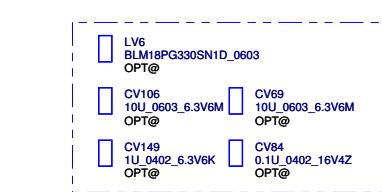
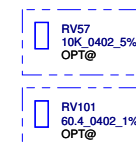
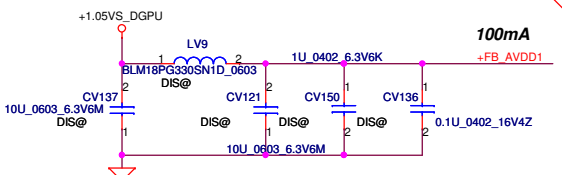
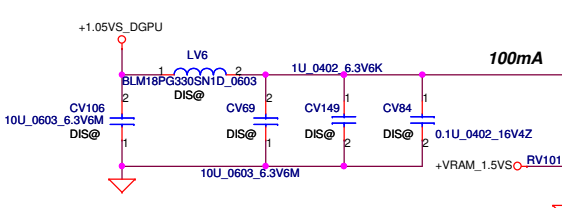
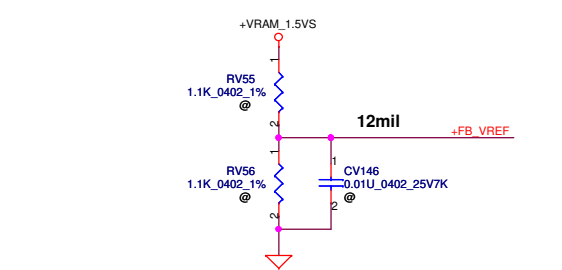
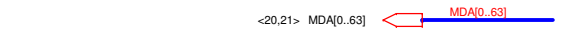


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Title VGA_GND		
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GB2-128 Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	A8
CMD8	A8	A8
CMD2	CS0#_L	A6
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



Security Classification	Compal Secret Data	
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Title			
VGA_MEM Interface A			
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<22,23> MDB[0..63]

MDB[0..63]

- MDB0 B13 FBC_D0
- MDB1 D13 FBC_D1
- MDB2 A13 FBC_D2
- MDB3 C16 FBC_D3
- MDB4 C16 FBC_D4
- MDB5 B16 FBC_D5
- MDB6 A17 FBC_D6
- MDB7 D16 FBC_D7
- MDB8 C13 FBC_D8
- MDB9 B11 FBC_D9
- MDB10 C11 FBC_D10
- MDB11 A11 FBC_D11
- MDB12 C10 FBC_D12
- MDB13 C8 FBC_D13
- MDB14 B8 FBC_D14
- MDB15 A8 FBC_D15
- MDB16 E8 FBC_D16
- MDB17 F8 FBC_D17
- MDB18 F10 FBC_D18
- MDB19 E9 FBC_D19
- MDB20 F12 FBC_D20
- MDB21 D8 FBC_D21
- MDB22 D11 FBC_D22
- MDB23 E11 FBC_D23
- MDB24 D12 FBC_D24
- MDB25 E13 FBC_D25
- MDB26 F13 FBC_D26
- MDB27 F14 FBC_D27
- MDB28 F15 FBC_D28
- MDB29 E16 FBC_D29
- MDB30 F16 FBC_D30
- MDB31 F17 FBC_D31
- MDB32 D29 FBC_D32
- MDB33 F27 FBC_D33
- MDB34 F28 FBC_D34
- MDB35 E28 FBC_D35
- MDB36 D26 FBC_D36
- MDB37 F25 FBC_D37
- MDB38 D24 FBC_D38
- MDB39 E25 FBC_D39
- MDB40 E32 FBC_D40
- MDB41 F32 FBC_D41
- MDB42 D33 FBC_D42
- MDB43 E31 FBC_D43
- MDB44 C33 FBC_D44
- MDB45 F29 FBC_D45
- MDB46 D30 FBC_D46
- MDB47 E29 FBC_D47
- MDB48 B29 FBC_D48
- MDB49 C31 FBC_D49
- MDB50 C29 FBC_D50
- MDB51 B31 FBC_D51
- MDB52 C32 FBC_D52
- MDB53 B32 FBC_D53
- MDB54 B35 FBC_D54
- MDB55 B34 FBC_D55
- MDB56 A29 FBC_D56
- MDB57 B28 FBC_D57
- MDB58 A28 FBC_D58
- MDB59 C28 FBC_D59
- MDB60 C26 FBC_D60
- MDB61 D25 FBC_D61
- MDB62 B25 FBC_D62
- MDB63 A25 FBC_D63

UVIC

Part 3 of 7

MEMORY INTERFACE C

- FBC_CMD0 F18 CMDB0 <22>
- FBC_CMD1 E19 CMDB1 <22>
- FBC_CMD2 D18 CMDB2 <22>
- FBC_CMD3 C17 CMDB3 <22>
- FBC_CMD4 C19 CMDB4 <22,23>
- FBC_CMD5 B17 CMDB5 <22,23>
- FBC_CMD6 E20 CMDB6 <22,23>
- FBC_CMD7 B19 CMDB7 <22,23>
- FBC_CMD8 D20 CMDB8 <22,23>
- FBC_CMD9 A19 CMDB9 <22,23>
- FBC_CMD10 D19 CMDB10 <22,23>
- FBC_CMD11 C20 CMDB11 <22,23>
- FBC_CMD12 F20 CMDB12 <22,23>
- FBC_CMD13 B20 CMDB13 <22,23>
- FBC_CMD14 G21 CMDB14 <22,23>
- FBC_CMD15 F22 CMDB15 <22,23>
- FBC_CMD16 F24 CMDB16 <23>
- FBC_CMD17 E23 CMDB17 <23>
- FBC_CMD18 C25 CMDB18 <23>
- FBC_CMD19 E21 CMDB19 <22,23>
- FBC_CMD20 E22 CMDB20 <22,23>
- FBC_CMD21 D21 CMDB21 <22,23>
- FBC_CMD22 A23 CMDB22 <22,23>
- FBC_CMD23 D22 CMDB23 <22,23>
- FBC_CMD24 D22 CMDB24 <22,23>
- FBC_CMD25 B23 CMDB25 <22,23>
- FBC_CMD26 C22 CMDB26 <22,23>
- FBC_CMD27 B22 CMDB27 <22,23>
- FBC_CMD28 A22 CMDB28 <22,23>
- FBC_CMD29 A20 CMDB29 <22,23>
- FBC_CMD30 G20 CMDB30 <22,23>
- FBC_CMD31

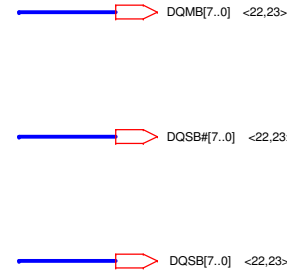
- FBC_DQM0 A16 DQMB0
- FBC_DQM1 F11 DQMB1
- FBC_DQM2 D15 DQMB2
- FBC_DQM3 D27 DQMB3
- FBC_DQM4 D34 DQMB4
- FBC_DQM5 A34 DQMB5
- FBC_DQM6 D28 DQMB6
- FBC_DQM7

- FBC_DQS_RN0 B14 DQSB#0
- FBC_DQS_RN1 C10 DQSB#1
- FBC_DQS_RN2 D9 DQSB#2
- FBC_DQS_RN3 E14 DQSB#3
- FBC_DQS_RN4 E26 DQSB#4
- FBC_DQS_RN5 D31 DQSB#5
- FBC_DQS_RN6 A31 DQSB#6
- FBC_DQS_RN7 A26 DQSB#7

- FBC_DQS_WP0 C14 DQSB0
- FBC_DQS_WP1 A10 DQSB1
- FBC_DQS_WP2 E10 DQSB2
- FBC_DQS_WP3 D14 DQSB3
- FBC_DQS_WP4 E26 DQSB4
- FBC_DQS_WP5 D32 DQSB5
- FBC_DQS_WP6 A32 DQSB6
- FBC_DQS_WP7 B26 DQSB7

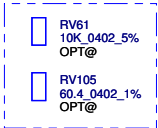
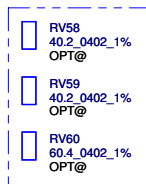
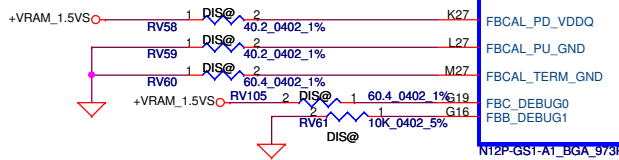
- FBC_WCK0 G14
- FBC_WCK0_N G15
- FBC_WCK1 G11
- FBC_WCK1_N G12
- FBC_WCK2 G27
- FBC_WCK2_N G28
- FBC_WCK3 G24
- FBC_WCK3_N G25

- FBC_CLK0 E17 CLKB0
- FBC_CLK0_N D17 CLKB0#
- FBC_CLK1 D23 CLKB1
- FBC_CLK1_N E23 CLKB1#



GB2-128 Mode E - Mirror Mode Mapping

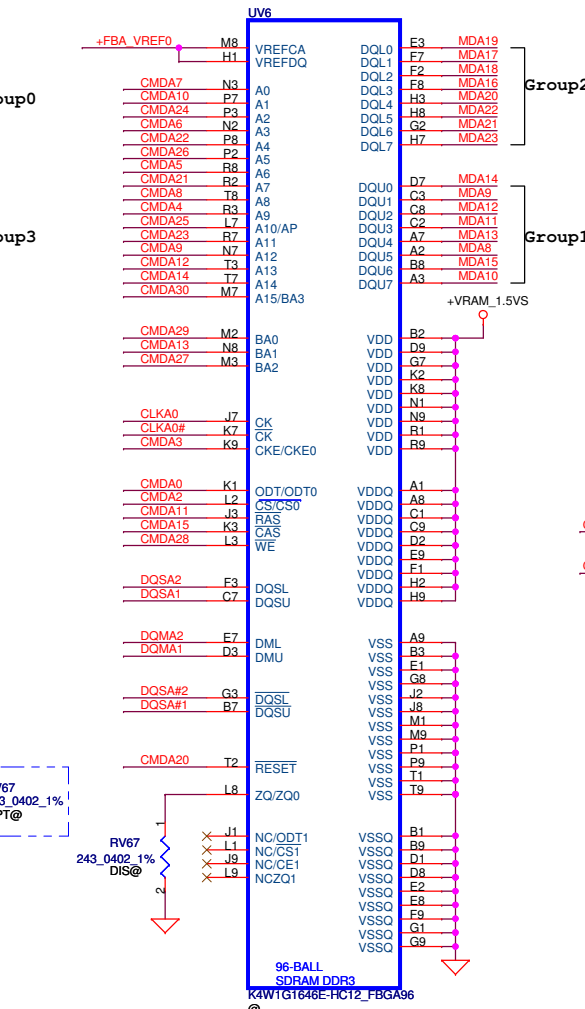
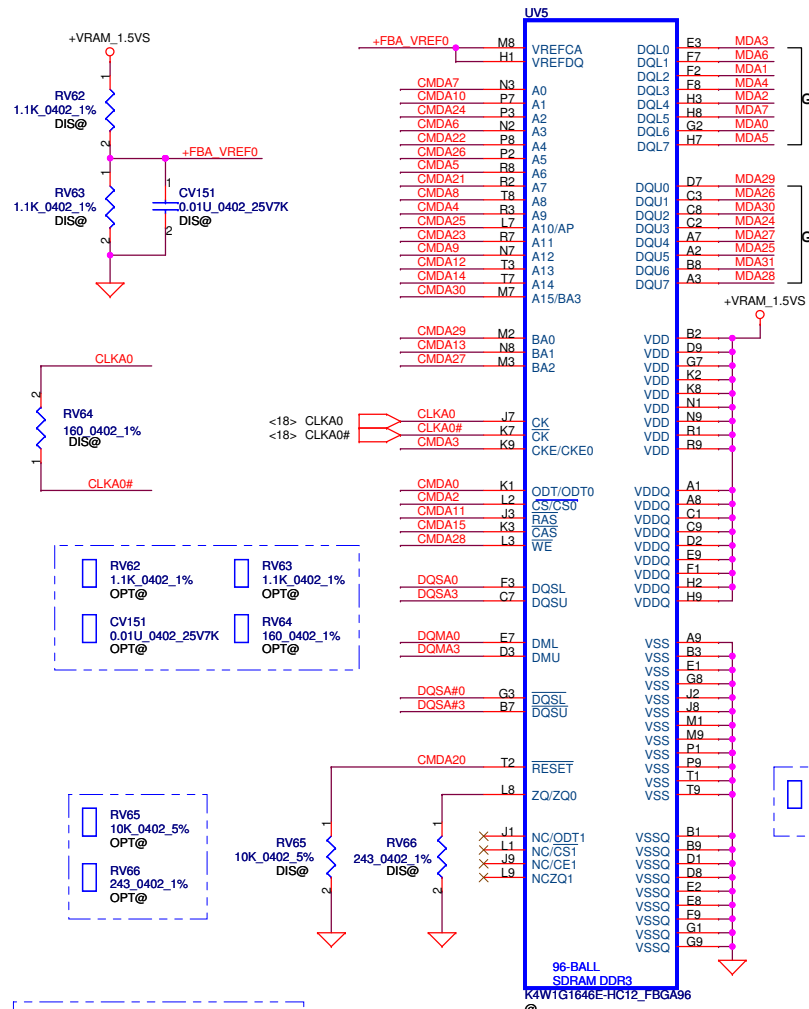
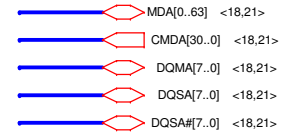
DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



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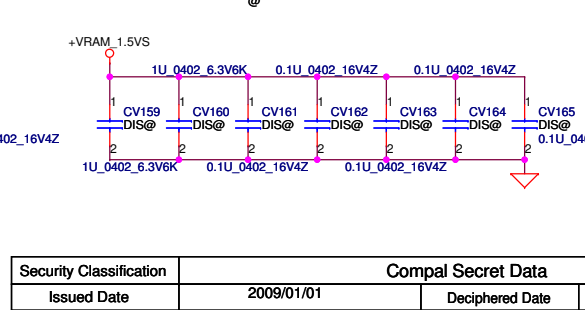
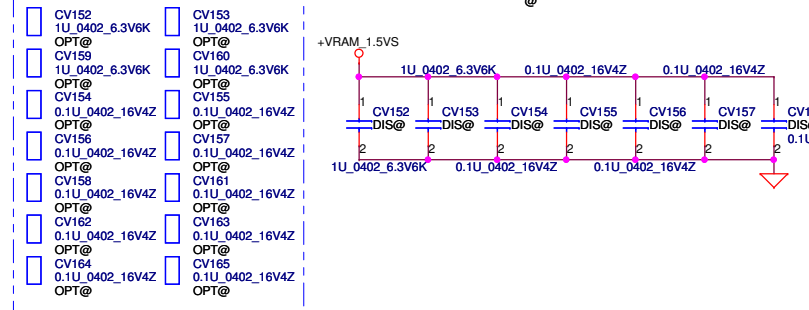
Compal Electronics, Inc.		
VGA_MEM Interface C		
Title	Document Number	Rev
	PHQAA LA-6831P M/B	0.3
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Memory Partition A - Lower 32 bits



GB2-128 Mode E - Mirror Mode Mapping

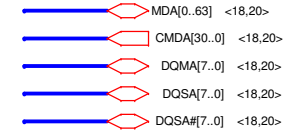
Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	A8
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



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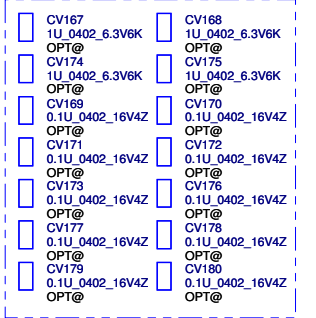
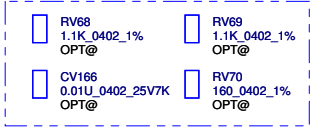
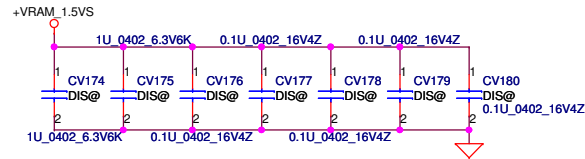
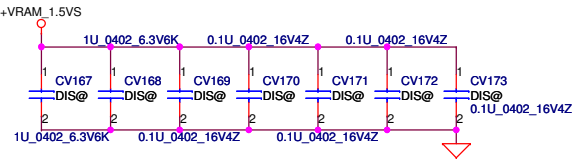
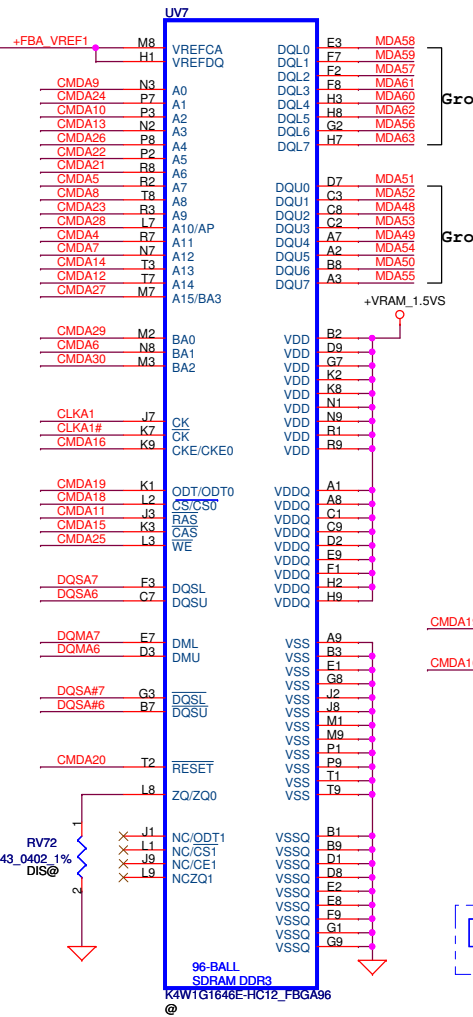
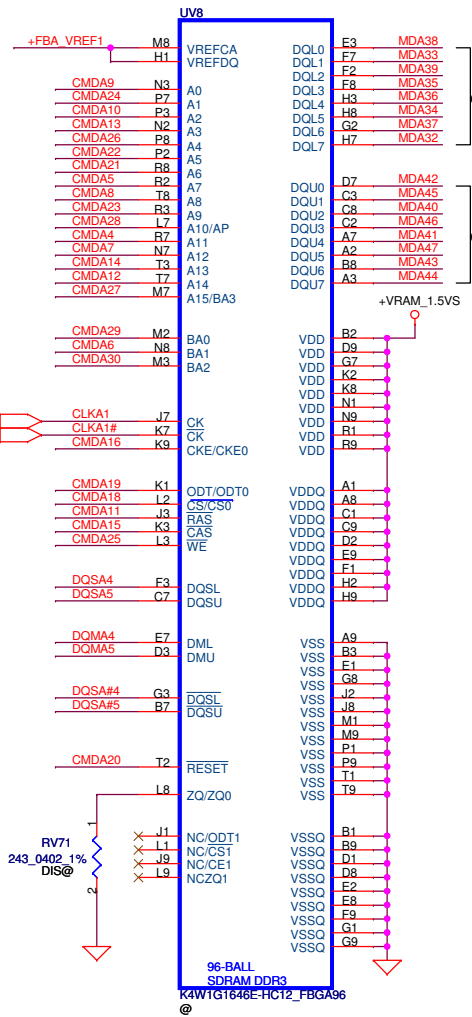
Title			Rev 0.3
Compal Electronics, Inc. VGA_VRAM_A Lower			
Size	Document Number	PHQAA LA-6831P M/B	
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Memory Partition A - Upper 32 bits



GB2-128 Mode E - Mirror Mode Mapping

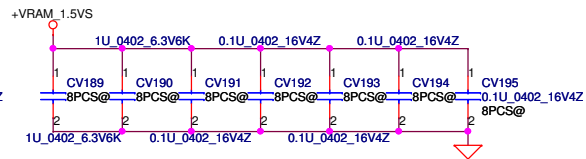
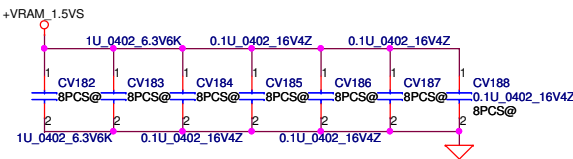
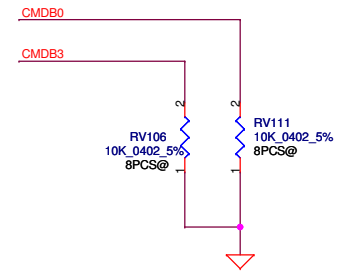
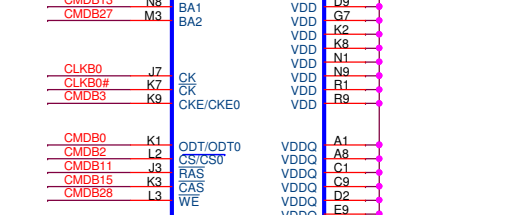
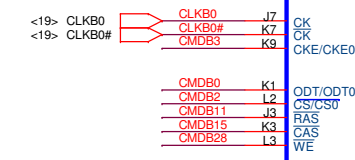
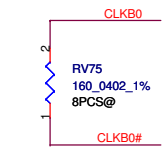
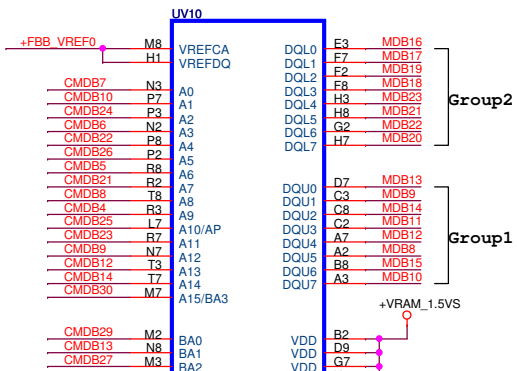
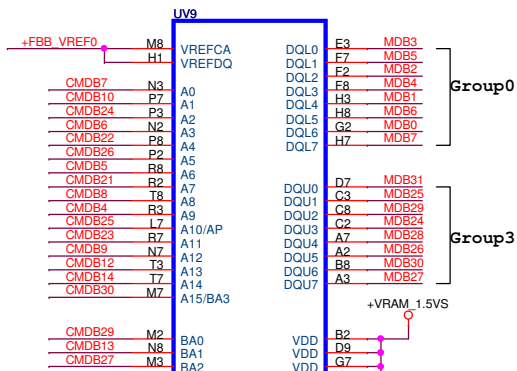
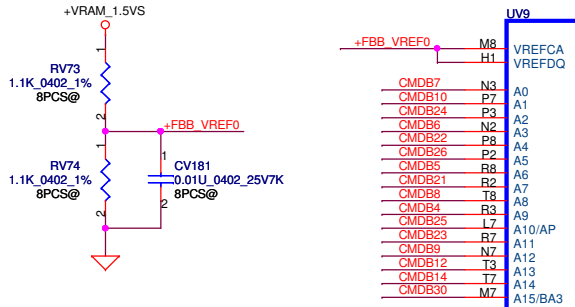
Address	DATA Bus	
CMD3	0..31	32..63
CMD8	CKE_L	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



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Compal Electronics, Inc.			
VGA_VRAM_A Upper			
Title	Document Number	Rev	0.3
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Memory Partition C - Lower 32 bits

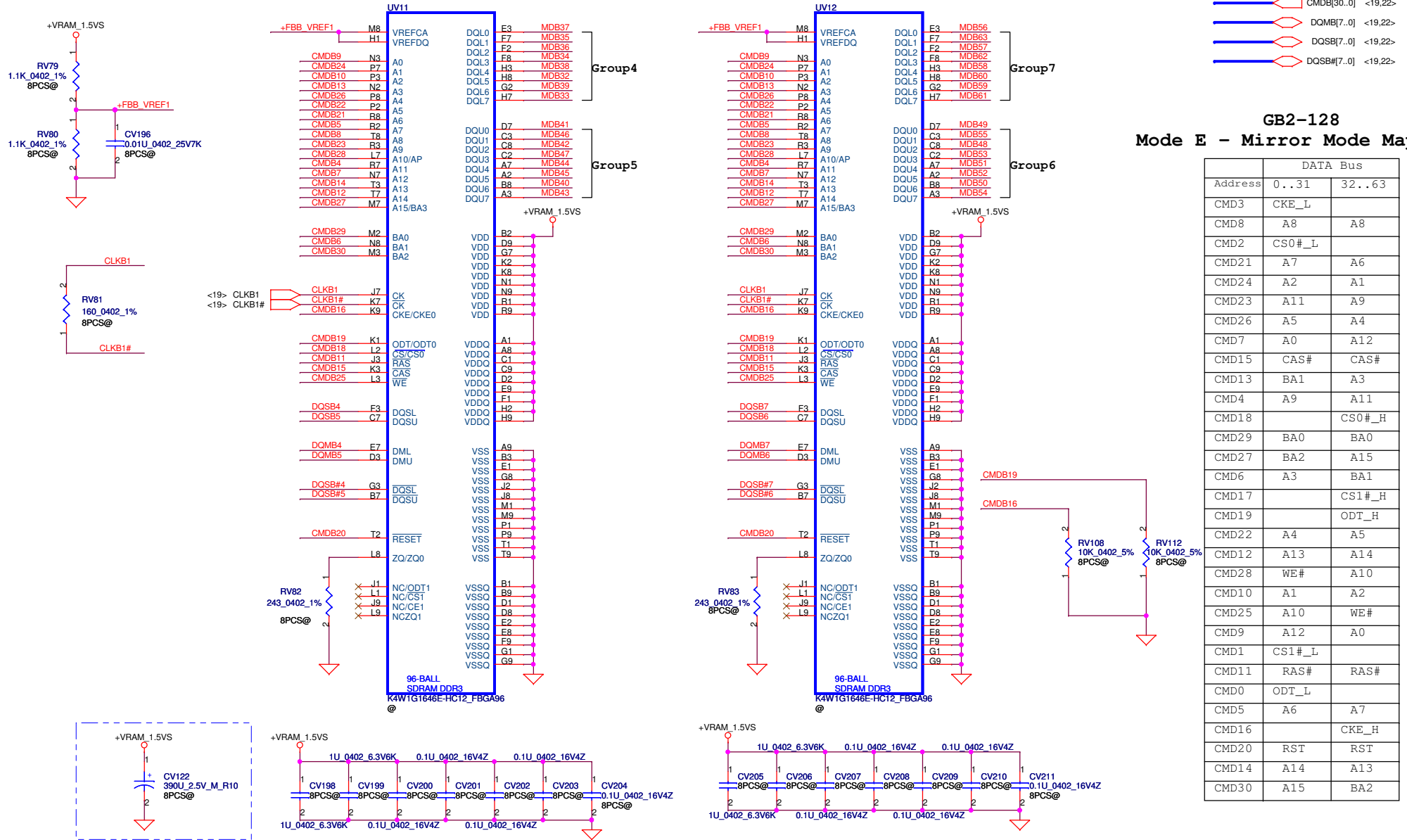


GB2-128 Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD9	A12	A0
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Compal Electronics, Inc. VGA_VRAM_C Lower	
Issued Date	2009/01/01	Deciphered Date	2010/01/01		
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Size	Custom	Document Number	PHQAA LA-6831P M/B		Rev 0.3
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Memory Partition C - Upper 32 bits

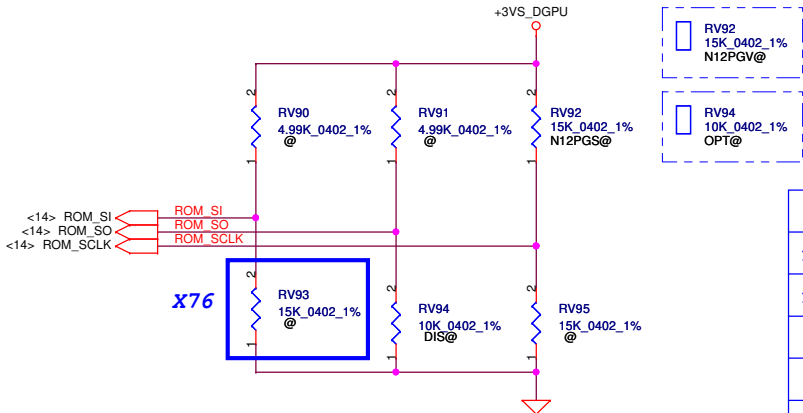
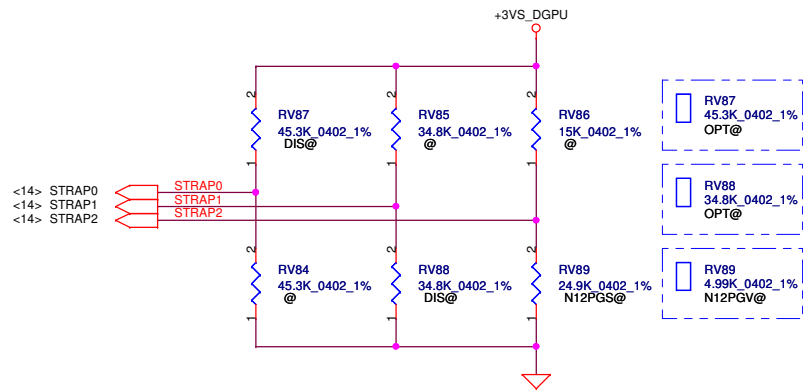


GB2-128
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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Issued Date	2009/01/01	Deciphered Date	2010/01/01
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Compal Electronics, Inc.		
VGA_VRAM_C Upper		
Title	Document Number	Rev
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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XLCK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GV	0x1050	Pull up 15K	Pull down 5K

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XLCK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

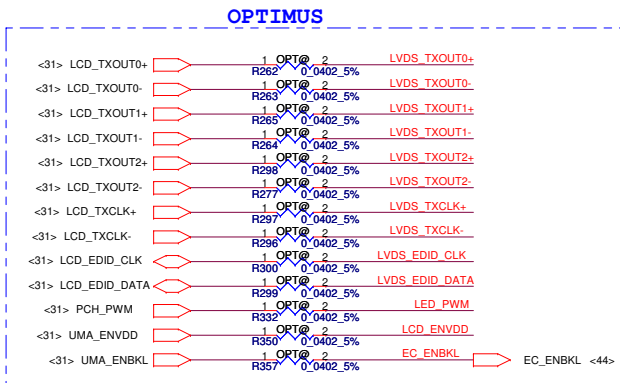
VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	512MB	0010	PD 15K (SD034150280)
	1GB	0010	PD 15K (SD034150280)
Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003Y000	2GB	0110	PD 34.8k (SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646E-HC11 SA000041T00	512MB	0011	PD 20K (SD034200280)
	1GB	0011	PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	PD 45.3K (SD034453280)

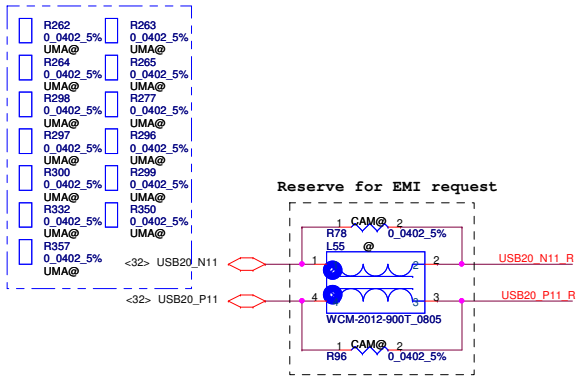
Security Classification	Compal Secret Data	
Issued Date	2009/01/01	Deciphered Date
		2010/01/01

Compal Electronics, Inc.		
Title		
VGA_MSIC		
Size	Document Number	Rev
Custom	PHQAA LA-6831P M/B	0.3
Date:	Thursday, October 07, 2010	Sheet 24 of 58

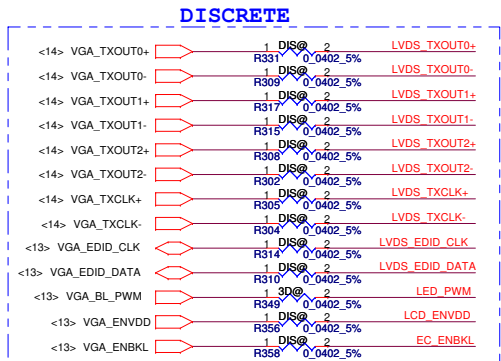
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Close to LVDS Connector

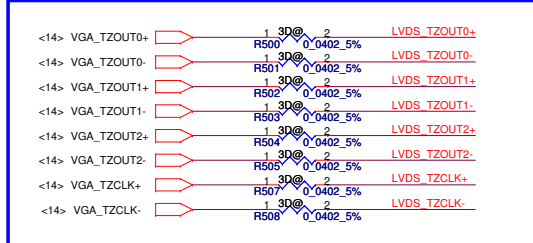


LCD/PANEL BD. Conn.



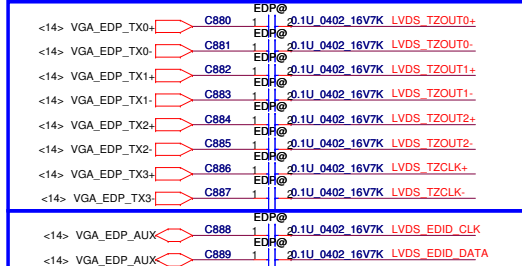
Close to LVDS Connector

DISCRETE for Full-HD and 3D LVDS Panel



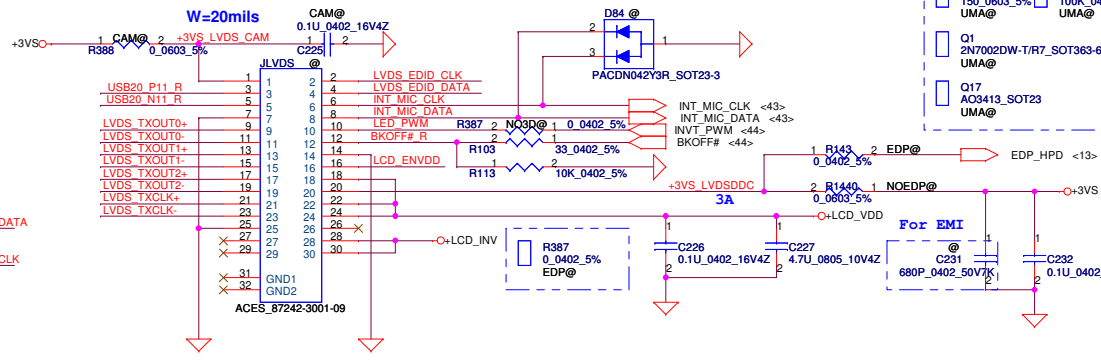
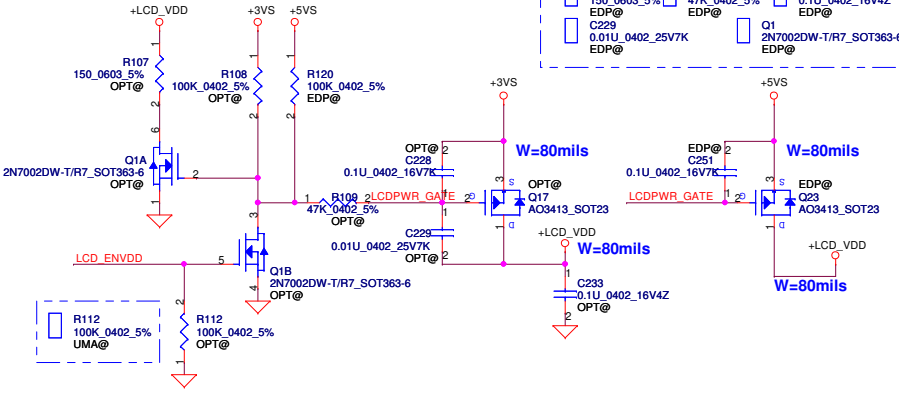
Close to LVDS1 Connector

DISCRETE for Full-HD and 3D eDP Panel

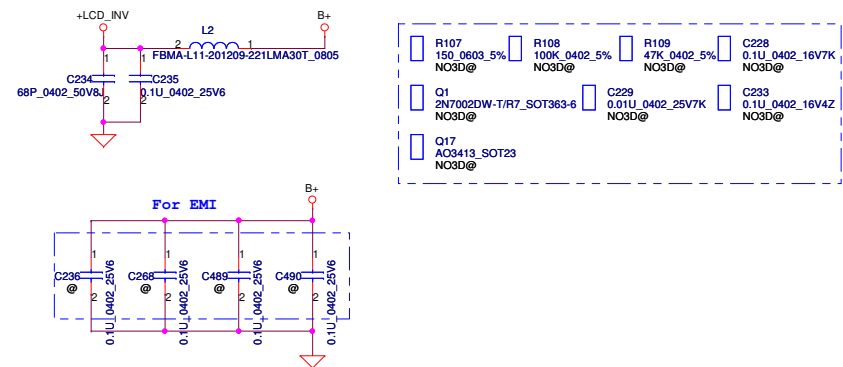
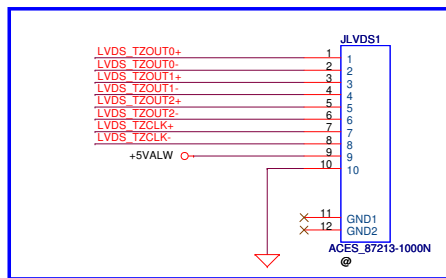


Close to LVDS1 Connector

Close to LVDS Connector



For 3D Panel



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CRT CONNECTOR

OPTIMUS

<31> UMA_CRT_R	1 OPT@ 2	CRT_R
<31> UMA_CRT_G	1 OPT@ 2	CRT_G
<31> UMA_CRT_B	1 OPT@ 2	CRT_B
<31> UMA_CRT_HSYNC	1 OPT@ 2	CRT_HSYNC
<31> UMA_CRT_VSYNC	1 OPT@ 2	CRT_VSYNC
<31> UMA_CRT_CLK	1 OPT@ 2	CRT_CLK
<31> UMA_CRT_DATA	1 OPT@ 2	CRT_DATA

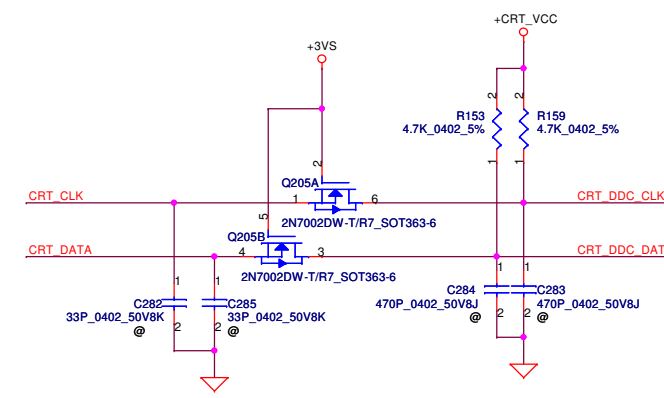
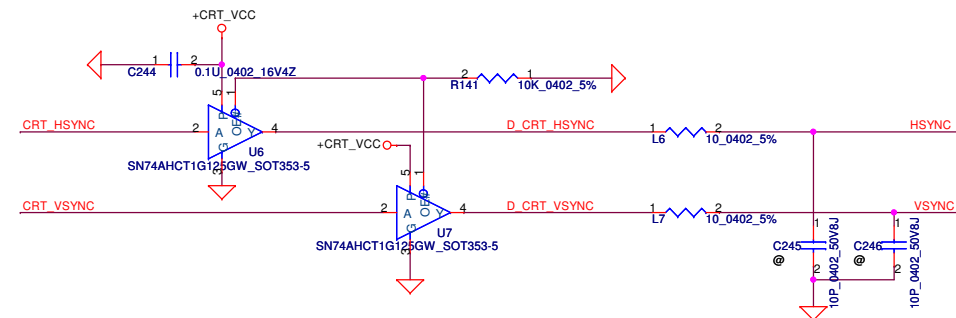
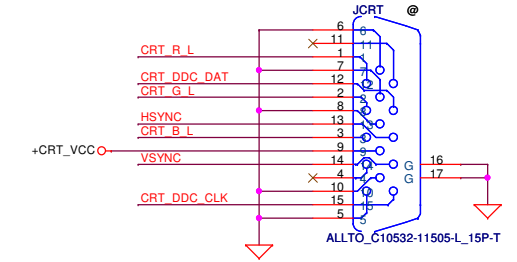
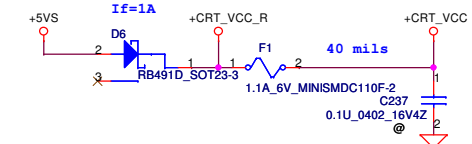
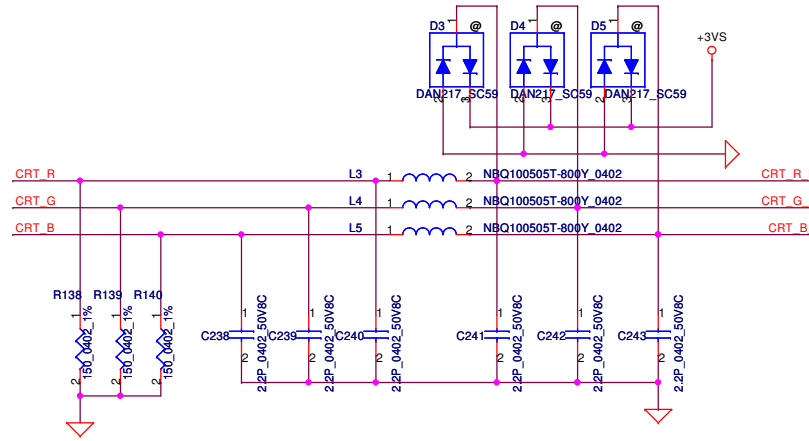
Close to CRT Connector

R200	0.0402_5%	UMA@
R204	0.0402_5%	UMA@
R211	0.0402_5%	UMA@
R213	0.0402_5%	UMA@
R235	0.0402_5%	UMA@
R236	0.0402_5%	UMA@
R261	0.0402_5%	UMA@

DISCRETE

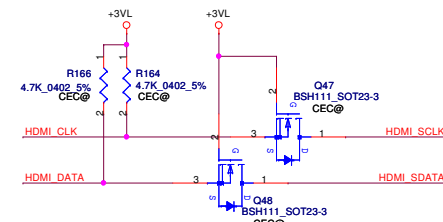
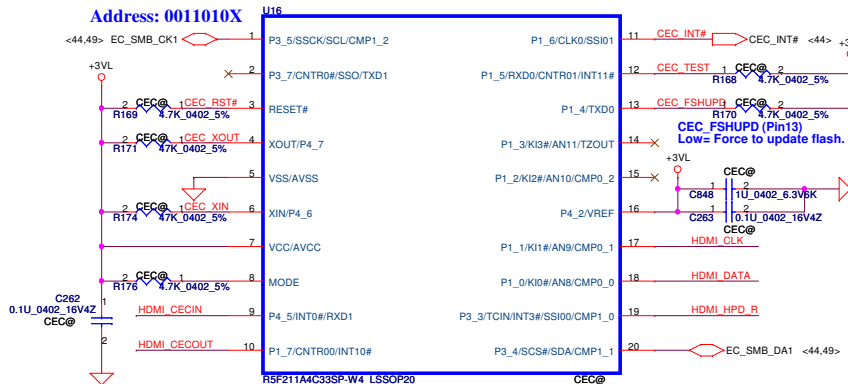
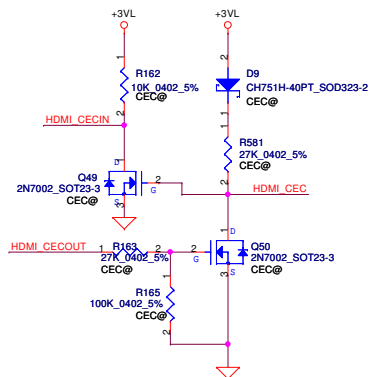
<13> VGA_CRT_R	1 DIS@ 2	CRT_R
<13> VGA_CRT_G	1 DIS@ 2	CRT_G
<13> VGA_CRT_B	1 DIS@ 2	CRT_B
<13> VGA_CRT_HSYNC	1 DIS@ 2	CRT_HSYNC
<13> VGA_CRT_VSYNC	1 DIS@ 2	CRT_VSYNC
<13> VGA_CRT_CLK	1 DIS@ 2	CRT_CLK
<13> VGA_CRT_DATA	1 DIS@ 2	CRT_DATA

Close to CRT Connector



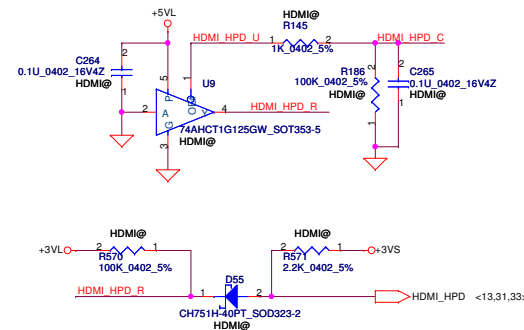
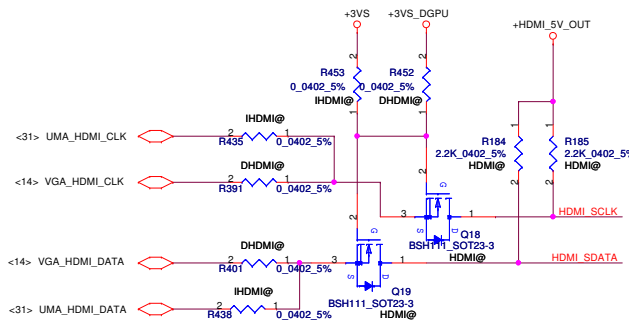
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				CRT	
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HDMI CEC Controller



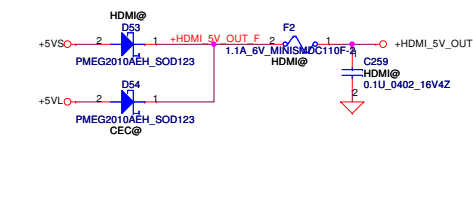
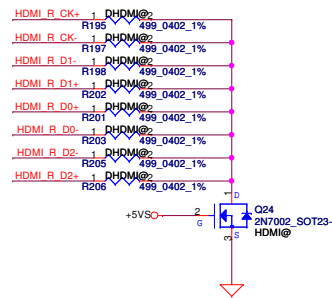
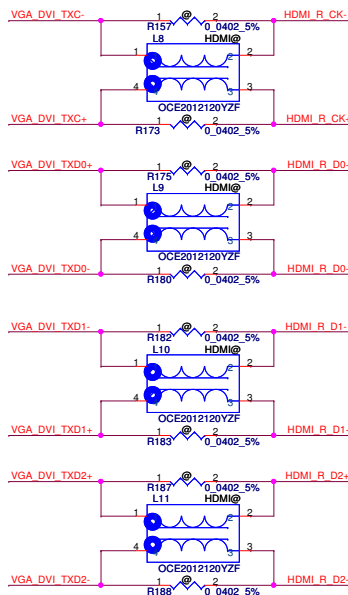
For DISCRETE

<14>	VGA_HDMI_CLK+	CV296	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXC+
<14>	VGA_HDMI_CLK-	CV293	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXC-
<14>	VGA_HDMI_TX0+	CV294	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD0+
<14>	VGA_HDMI_TX0-	CV297	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD0-
<14>	VGA_HDMI_TX1+	CV299	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD1+
<14>	VGA_HDMI_TX1-	CV298	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD1-
<14>	VGA_HDMI_TX2+	CV295	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD2+
<14>	VGA_HDMI_TX2-	CV300	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD2-

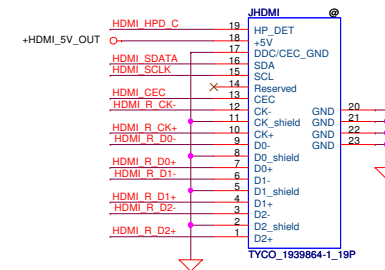


For Optimus

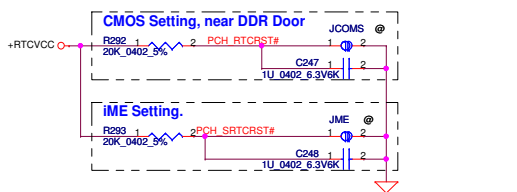
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<31>	UMA_HDMI_TX0+	CV306	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD0+
<31>	UMA_HDMI_TX0-	CV302	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD0-
<31>	UMA_HDMI_TX1+	CV303	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD1+
<31>	UMA_HDMI_TX1-	CV301	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD1-
<31>	UMA_HDMI_TX2+	CV307	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD2+
<31>	UMA_HDMI_TX2-	CV305	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD2-



HDMI Connector

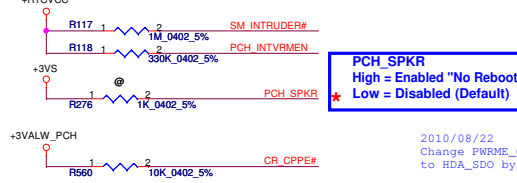


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Rev 0.3				



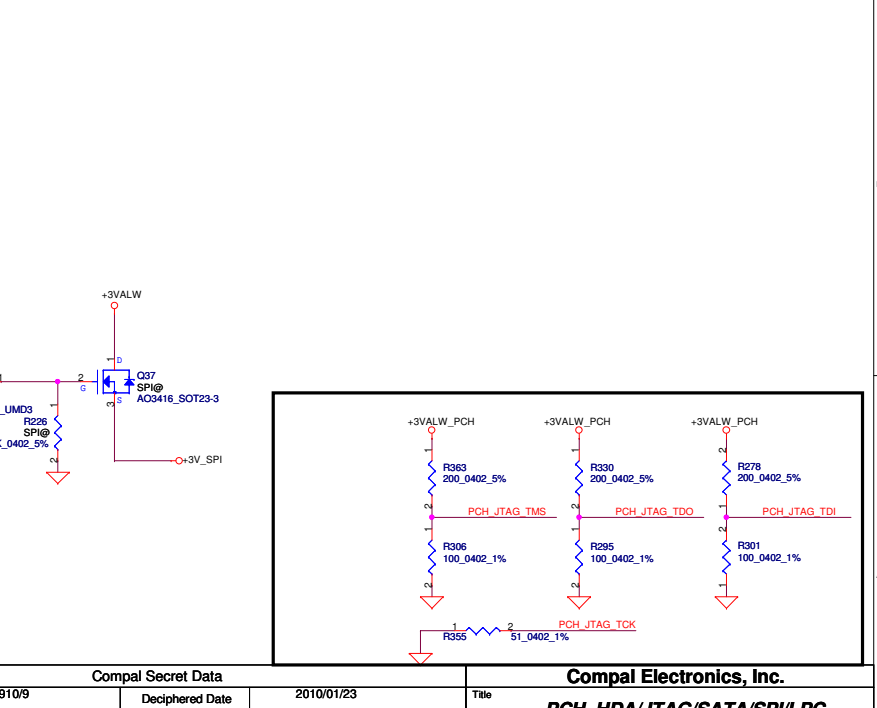
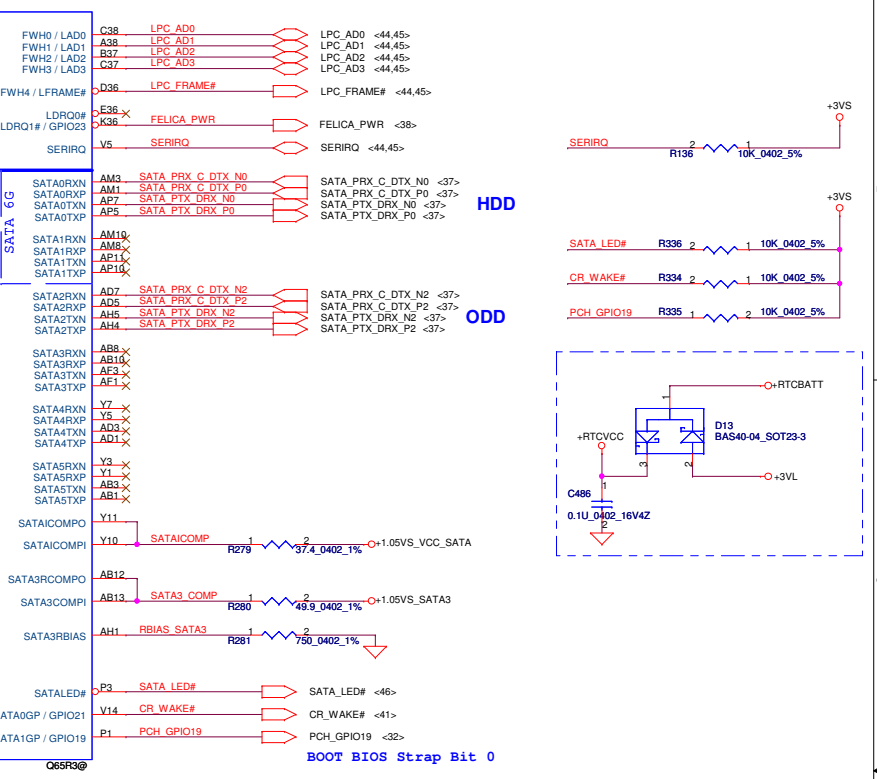
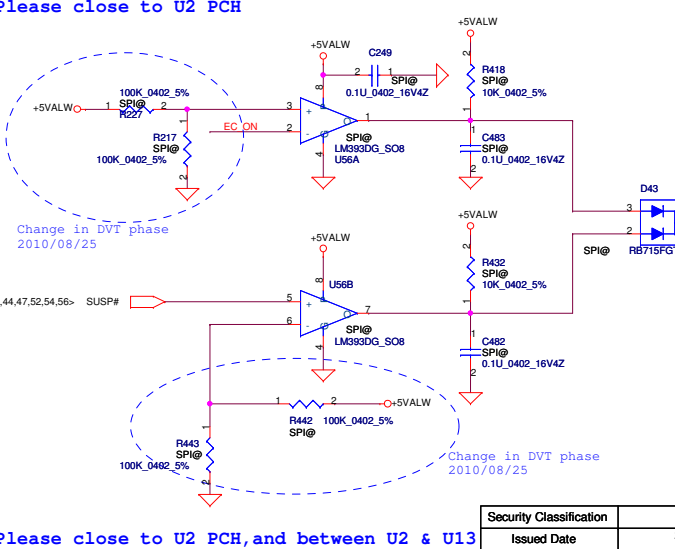
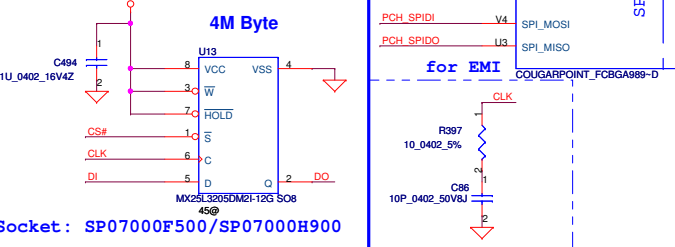
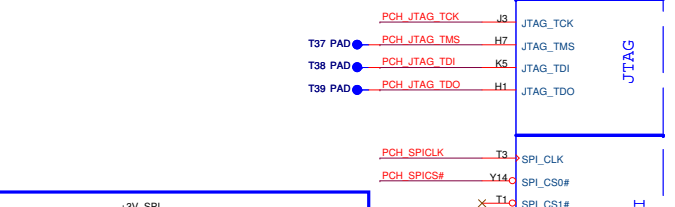
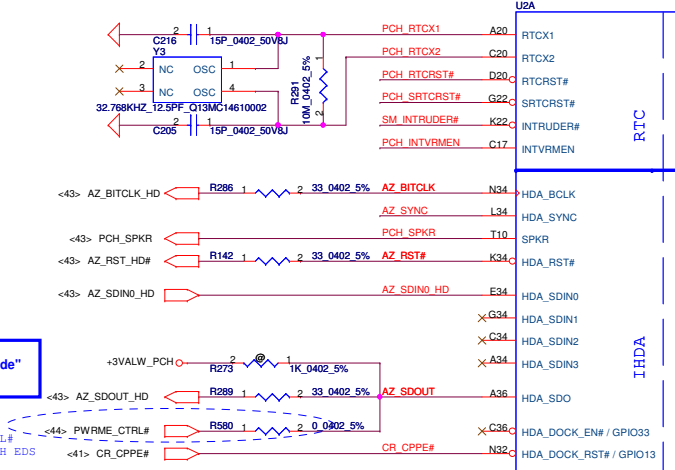
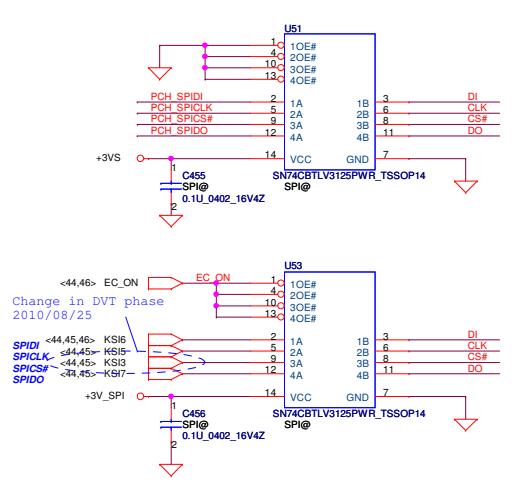
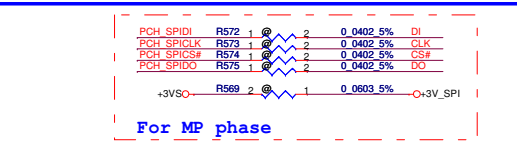
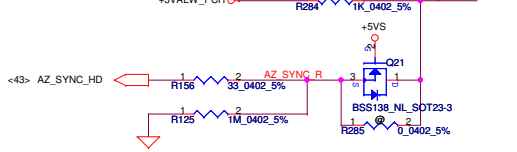
Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)



HDA_SDO
ME debug mode, this signal has a weak internal pull down
★Low = Disable (default)
High = Enable (flash descriptor security override)

HDA_SYNC
★This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform

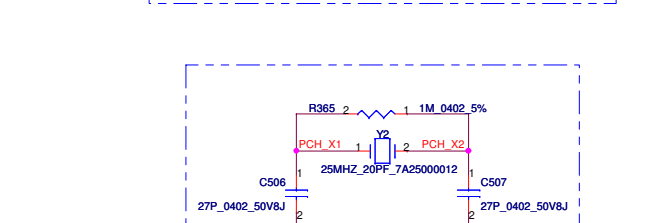
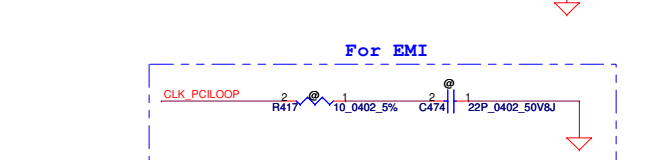
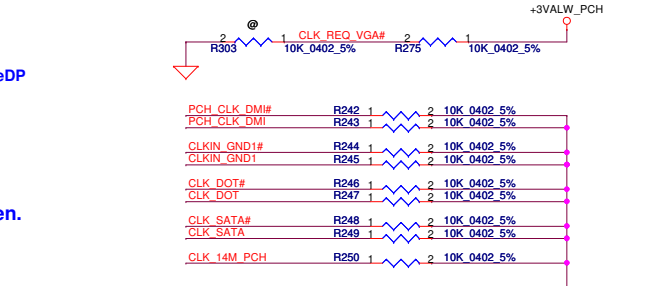
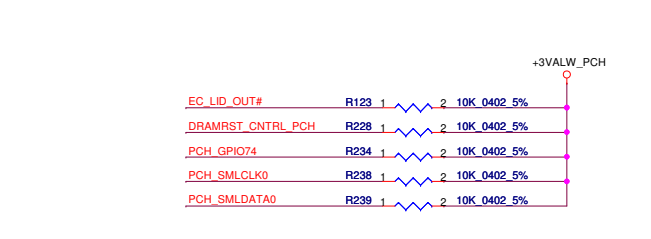
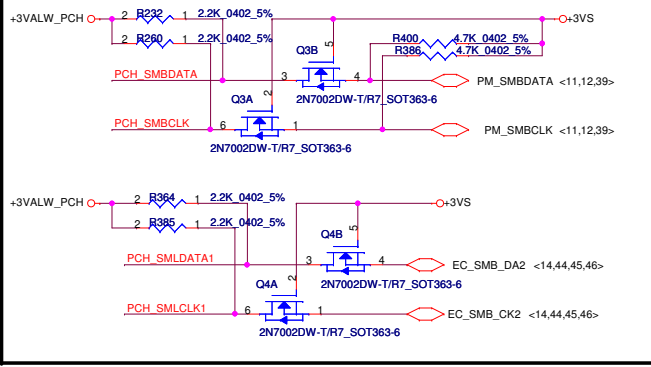
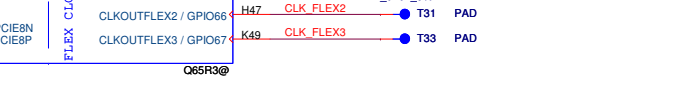
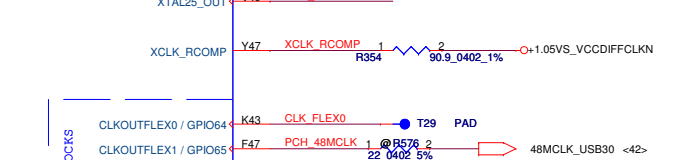
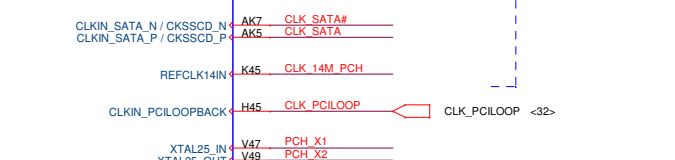
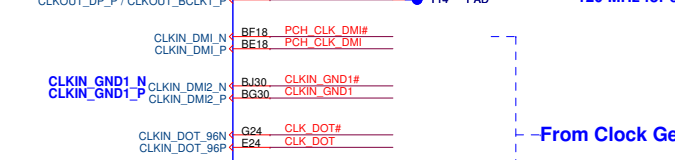
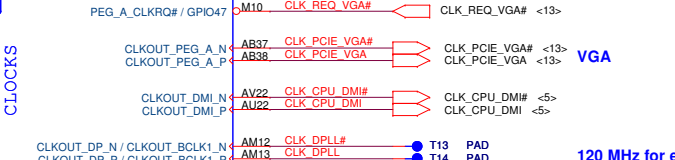
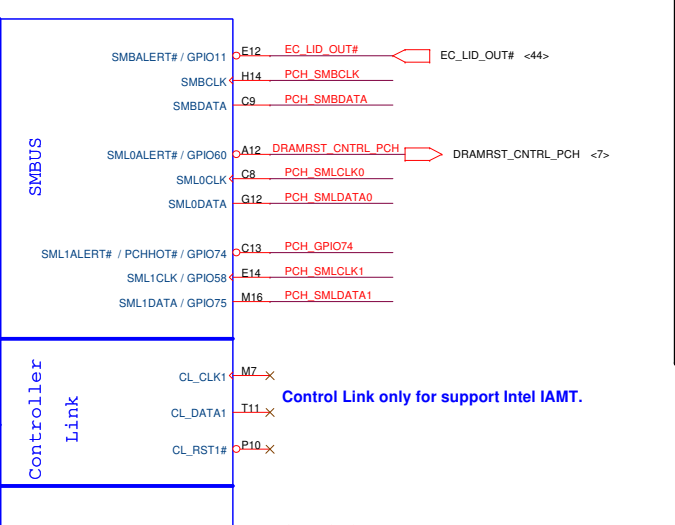
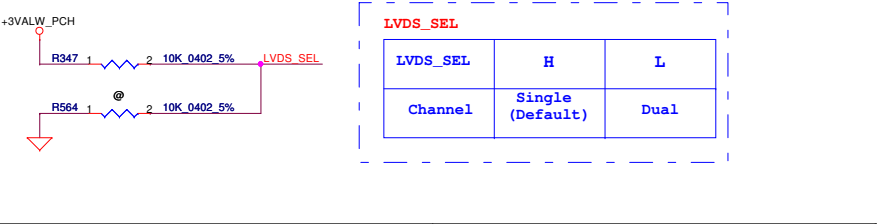
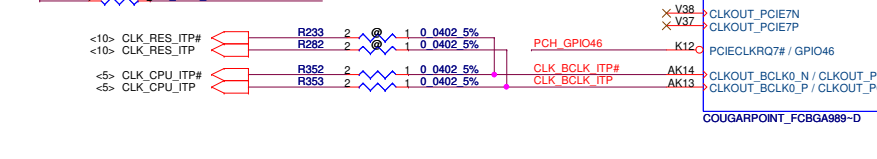
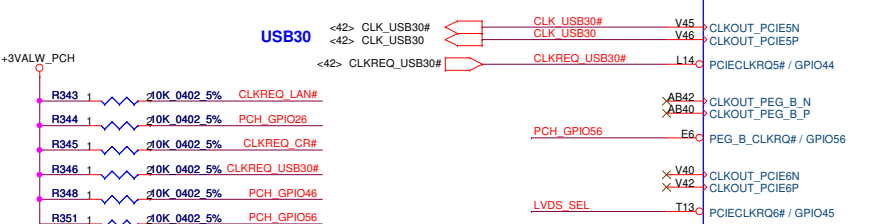
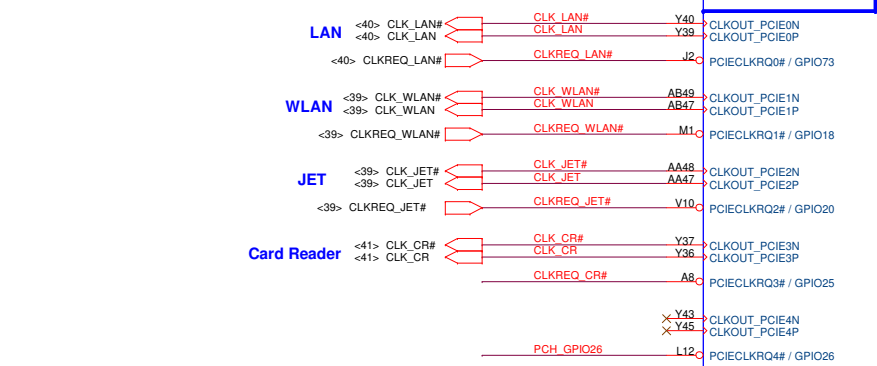
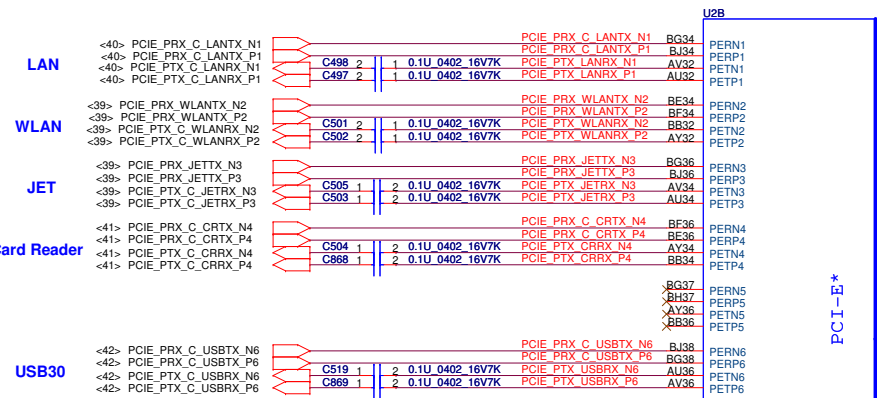


Socket: SP07000F500/SP07000H900

Please close to U2 PCH

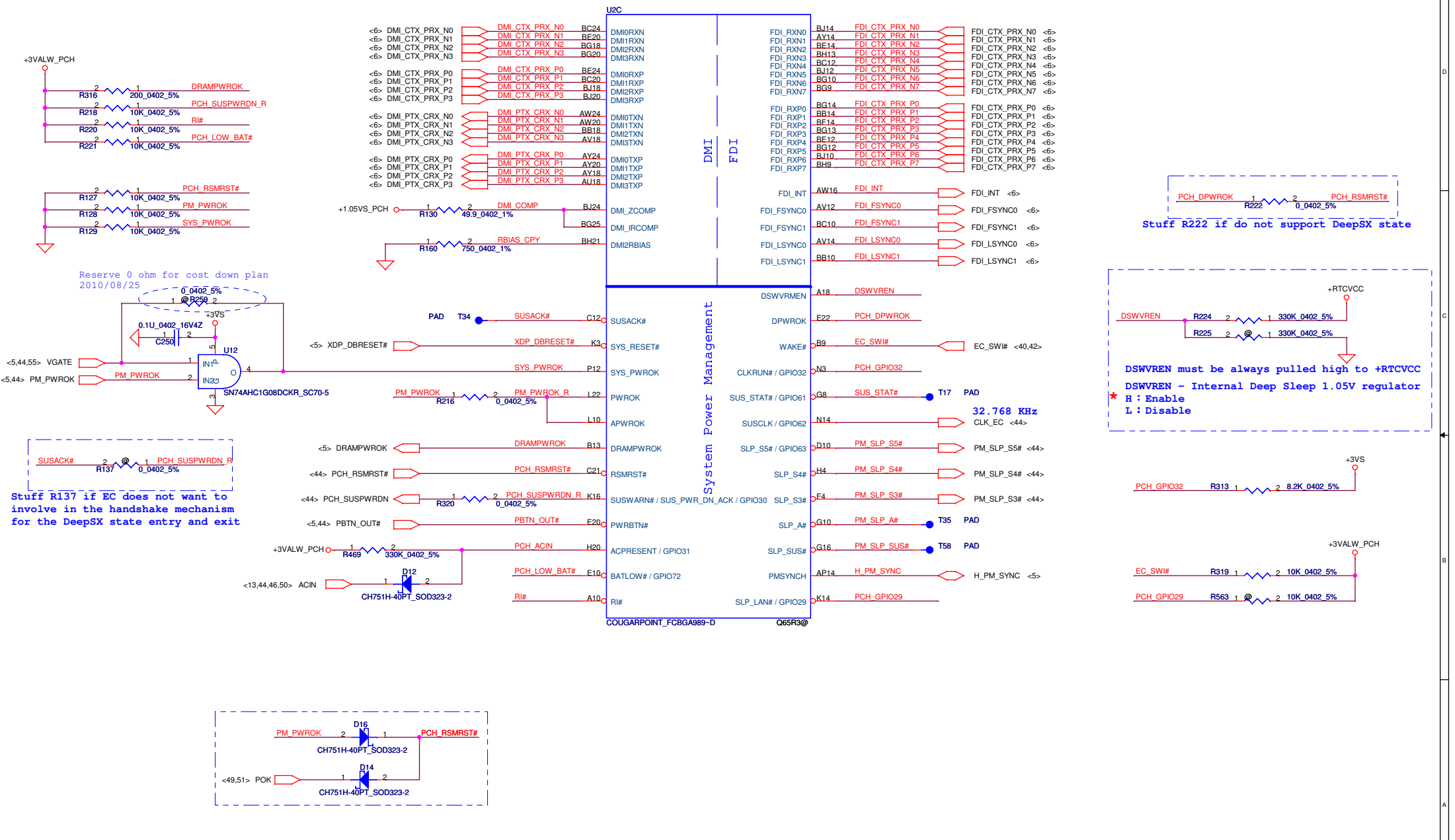
Please close to U2 PCH, and between U2 & U13

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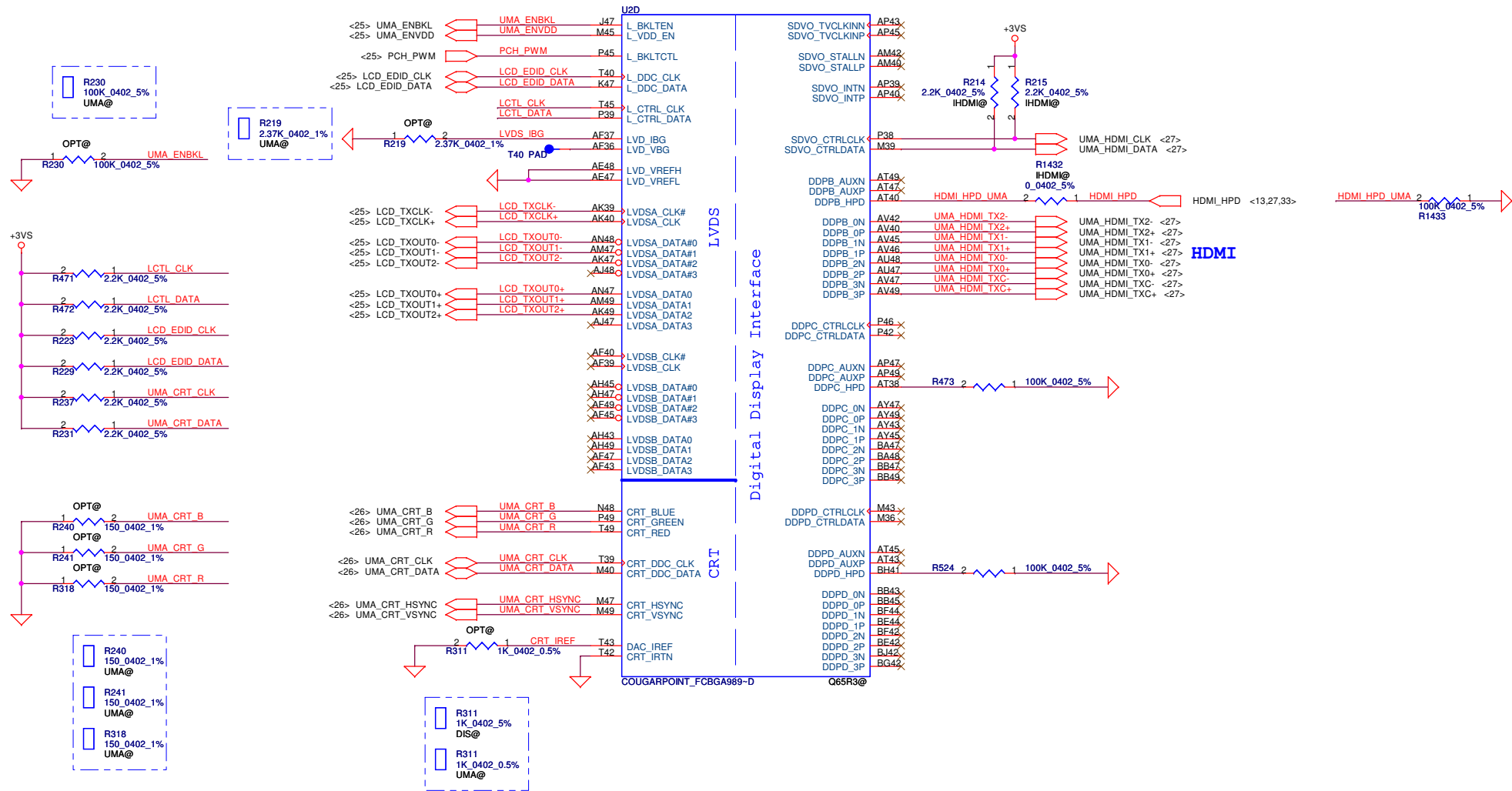


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				PCH_PCI-E/SMBUS/CLK	
Size	Document Number			Rev	0.3
Custom	PHQAA LA-6831P M/B			Date:	Thursday, October 07, 2010
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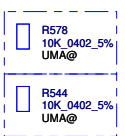
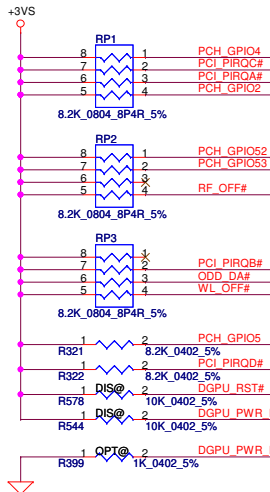
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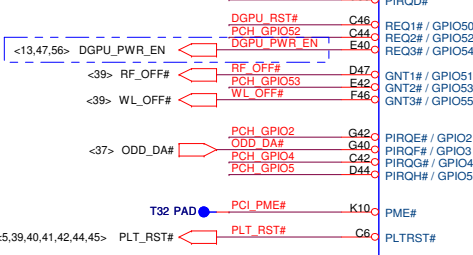
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Size	Document Number			Rev	0.3
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Size	Document Number	Rev		0.3	
Custom	PHQAA LA-6831P M/B	Date:		Thursday, October 07, 2010 Sheet 31 of 58	

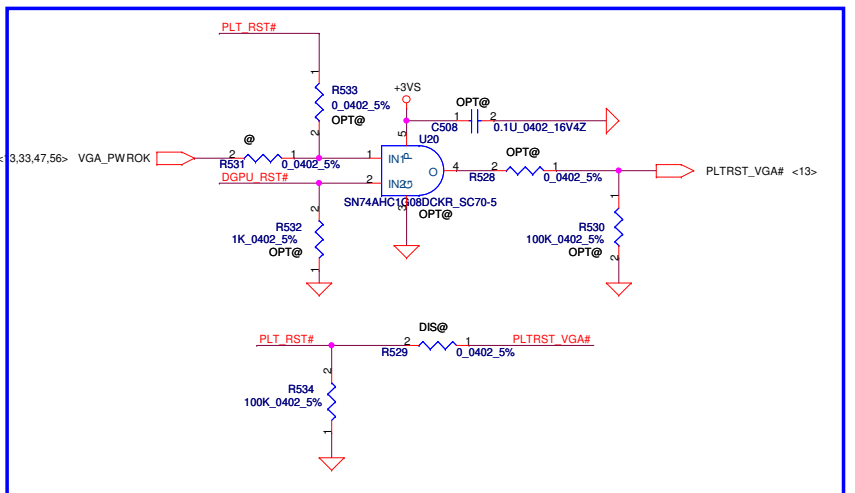
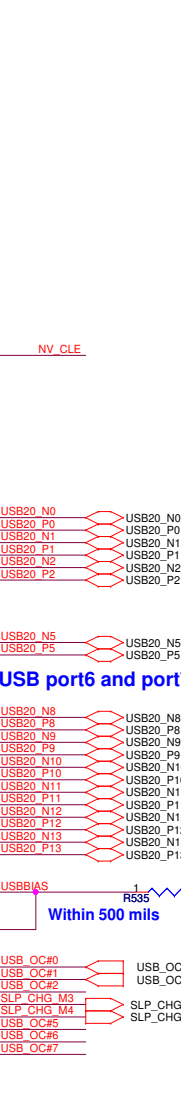
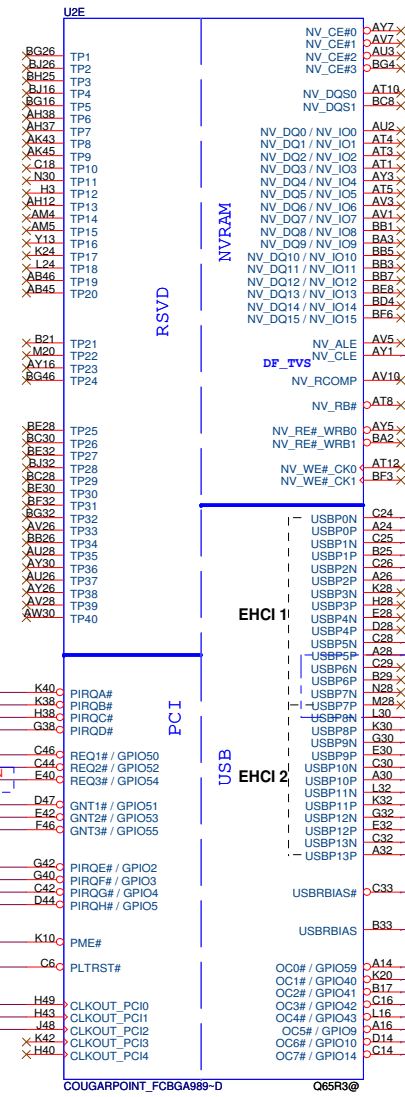
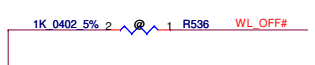
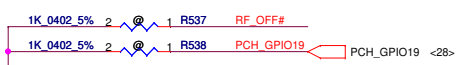


For Optimus



Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	0	Reserved
1	0	PCI
1	1	SPI *

A16 Swap Override Strap	
WL_OFF#	Low= A16 swap override Enable High= A16 swap override Disable
*	

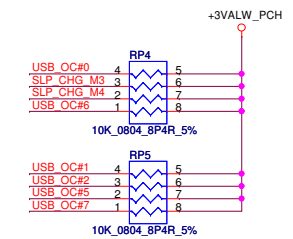
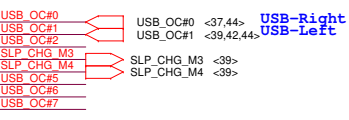
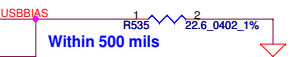
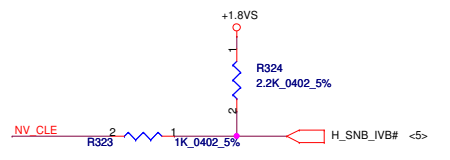


For Optimus

USB-RIGHT1
USB-RIGHT2
USB-Left1

IR Emitter
WIMax
TV Tuner #1
Int. Camera
3G/ TV tuner #2
Felica

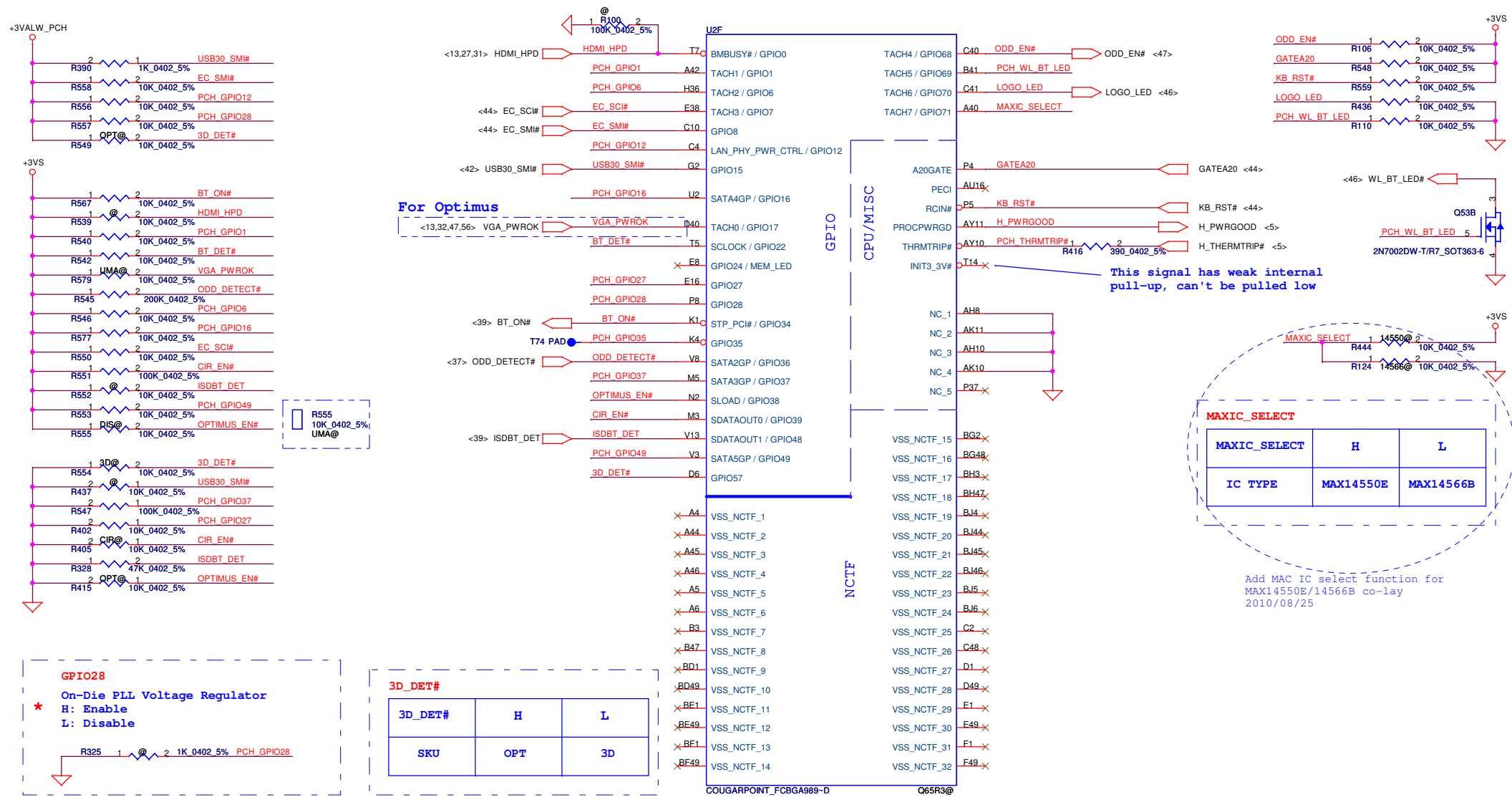
DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH Set to VSS when LOW



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Issued Date	200910/9	Deciphered Date	2010/01/23

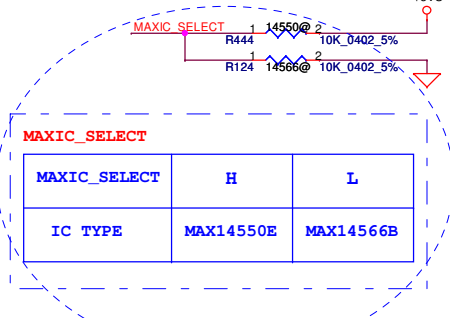
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Compal Electronics, Inc.			
PCH_PCI/USB/NAND			
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For Optimus

This signal has weak internal pull-up, can't be pulled low



Add MAC IC select function for MAX14550E/14566B co-lay 2010/08/25

GPIO28

On-Die PLL Voltage Regulator

H: Enable
L: Disable

R325 1K 0402 5% PCH_GPIO28

3D_DET#

3D_DET#	H	L
SKU	OPT	3D

GPIO8

Integrated Clock Chip Enable (Removed)

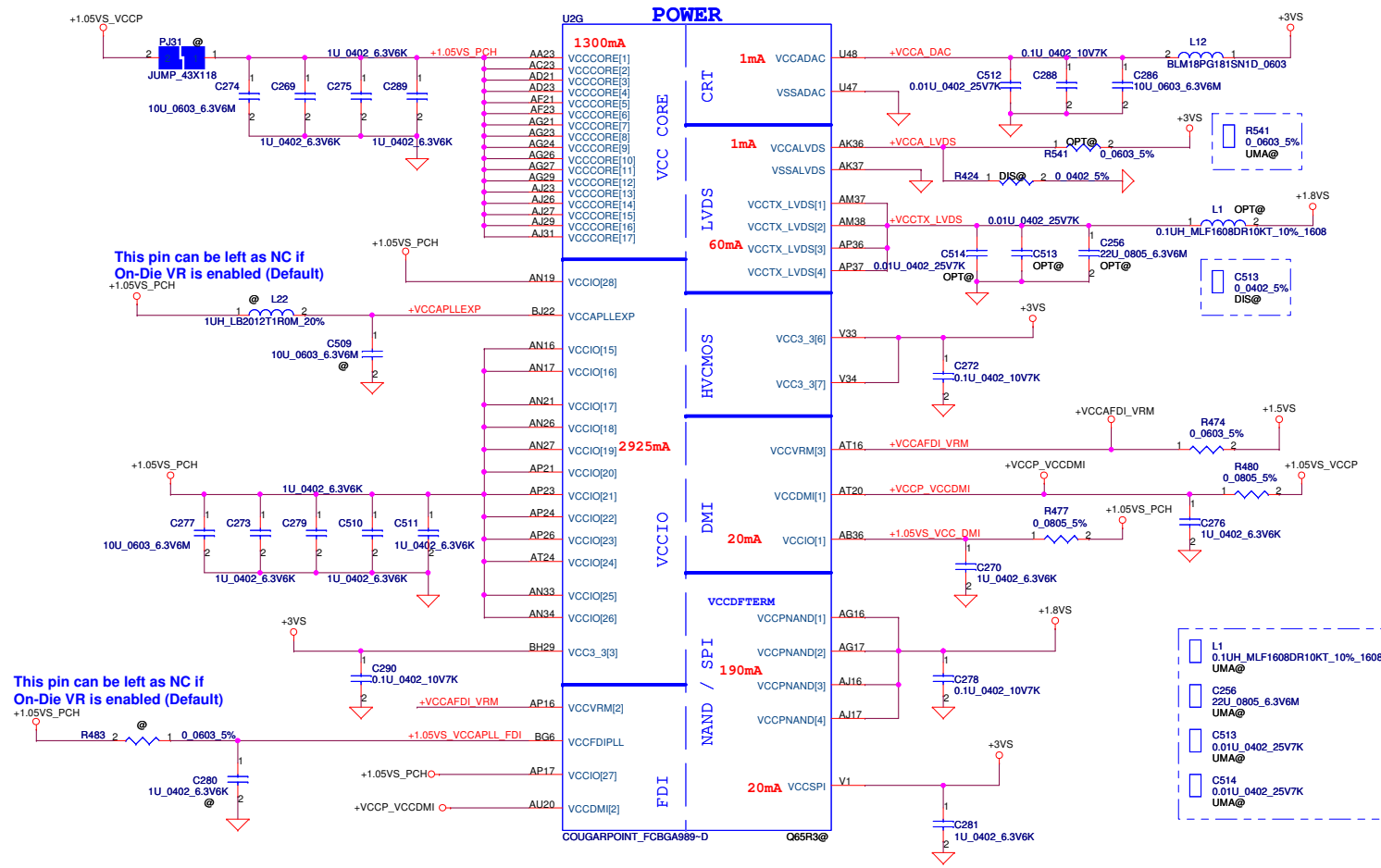
H: Disable
L: Enable

R326 1K 0402 5% EC_SMI#

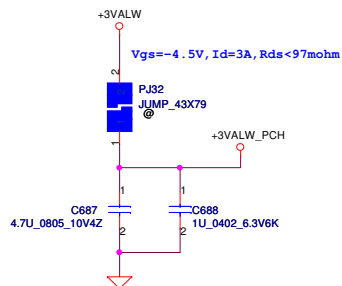
Integrated clock enable functionality is achieved by soft-strap
The current default is clock enable

OPTIMUS_EN#

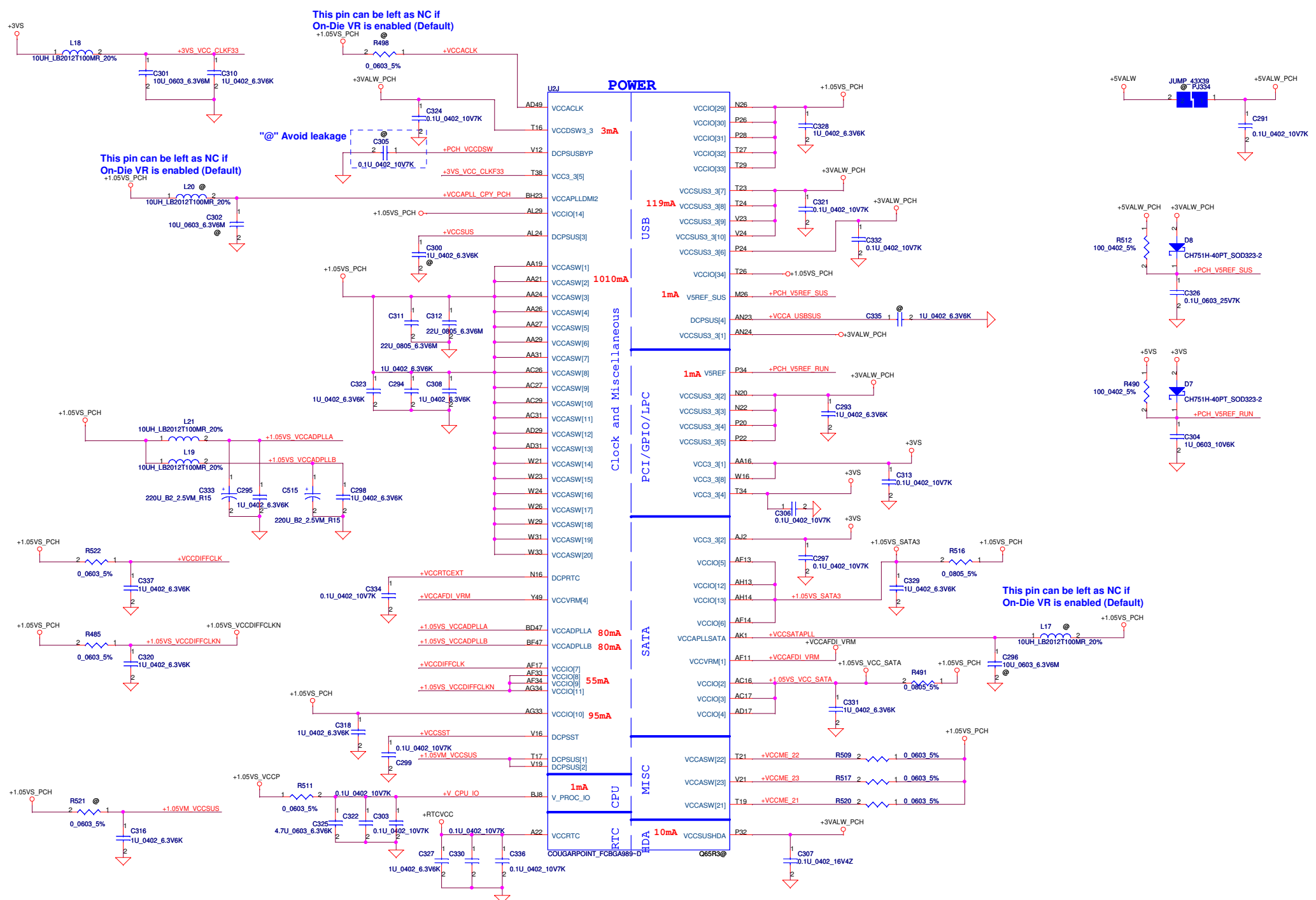
OPTIMUS_EN#	H	L
SKU	Discrete	Optimus



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPILLA	1.05	0.08
VCCADPLL	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSUSHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06

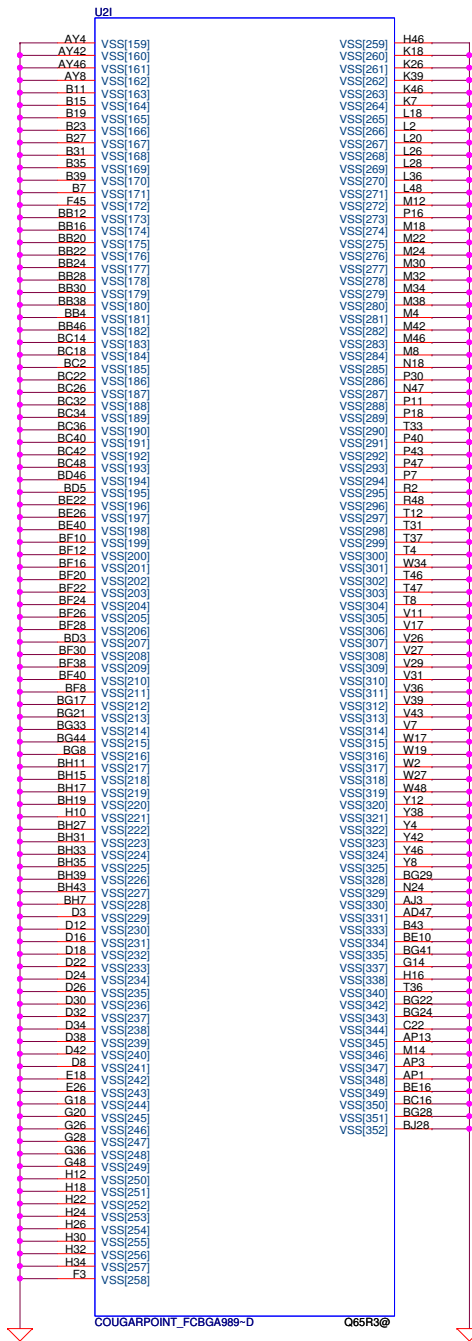
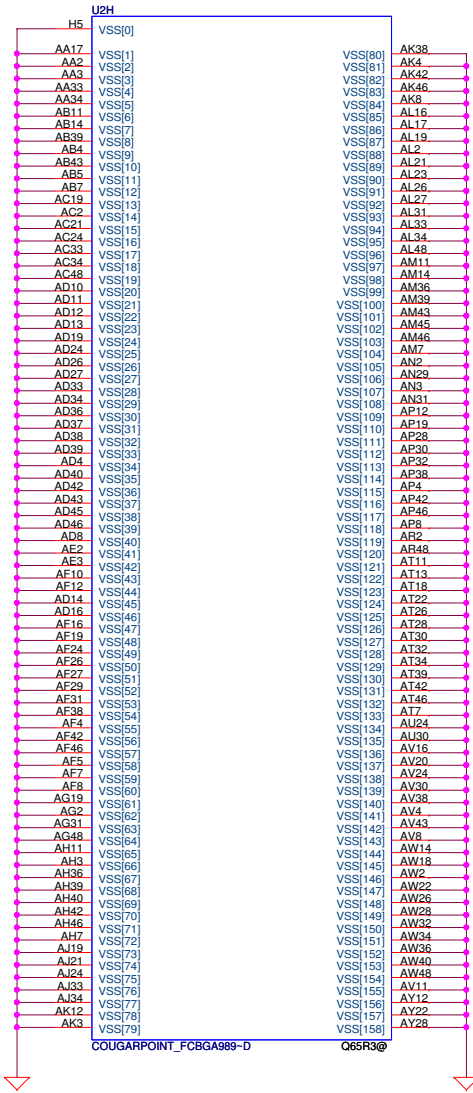


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				PCH_POWER-1		
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			PHQAA LA-6831P M/B	0.3		
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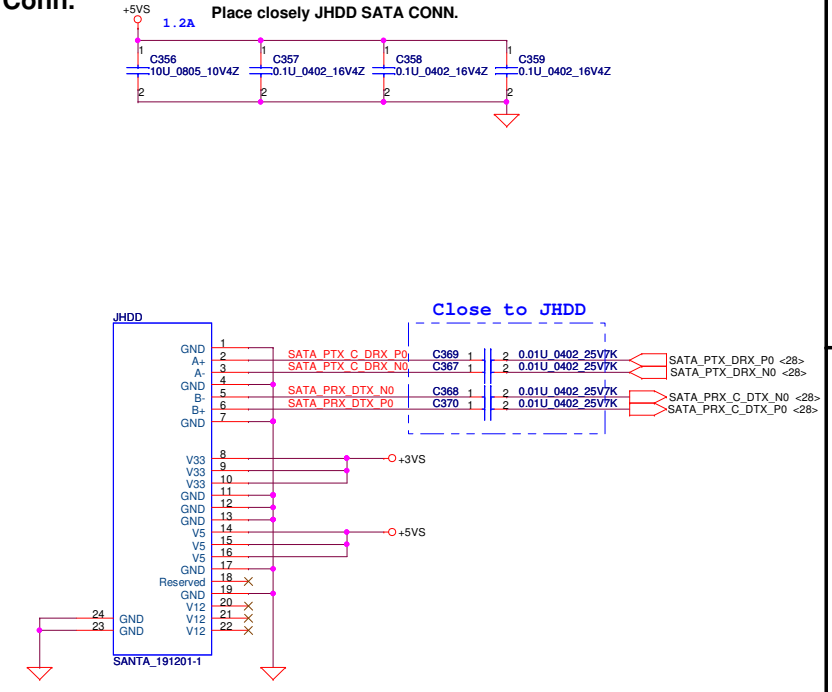
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Compal Electronics, Inc.			
PCH POWER-2			
Size	Document Number	Rev	
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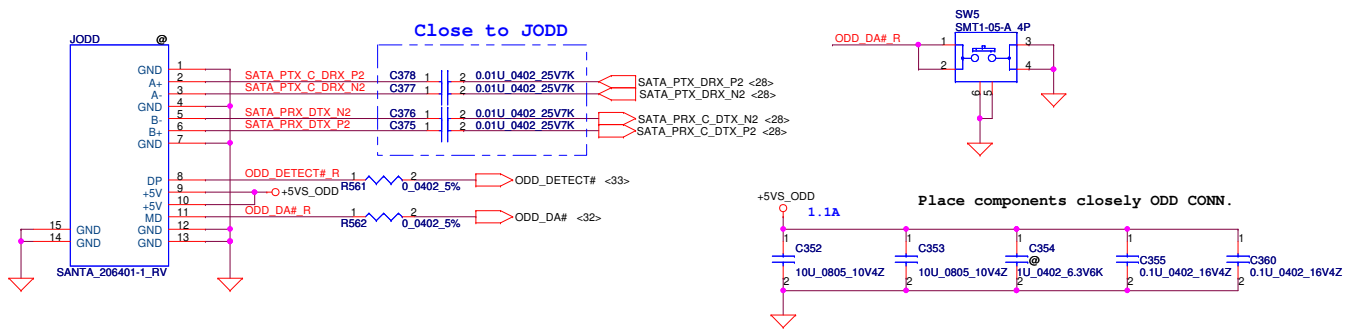


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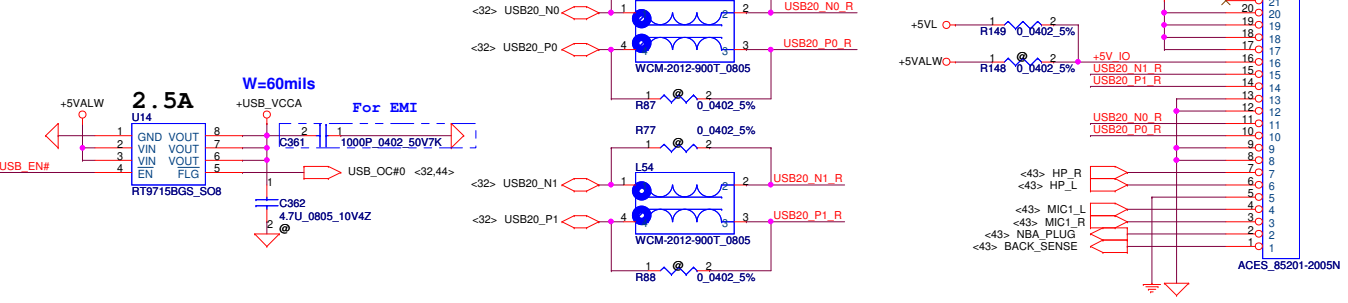
SATA HDD Conn.



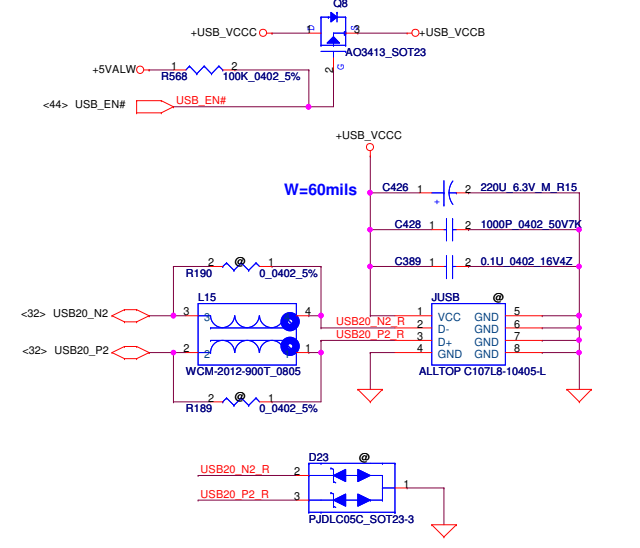
SATA ODD Conn



USB Board@ Right Side

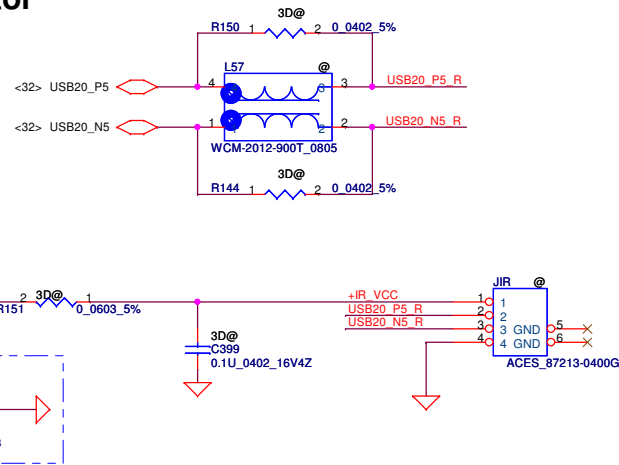


USB Board@ Left Side

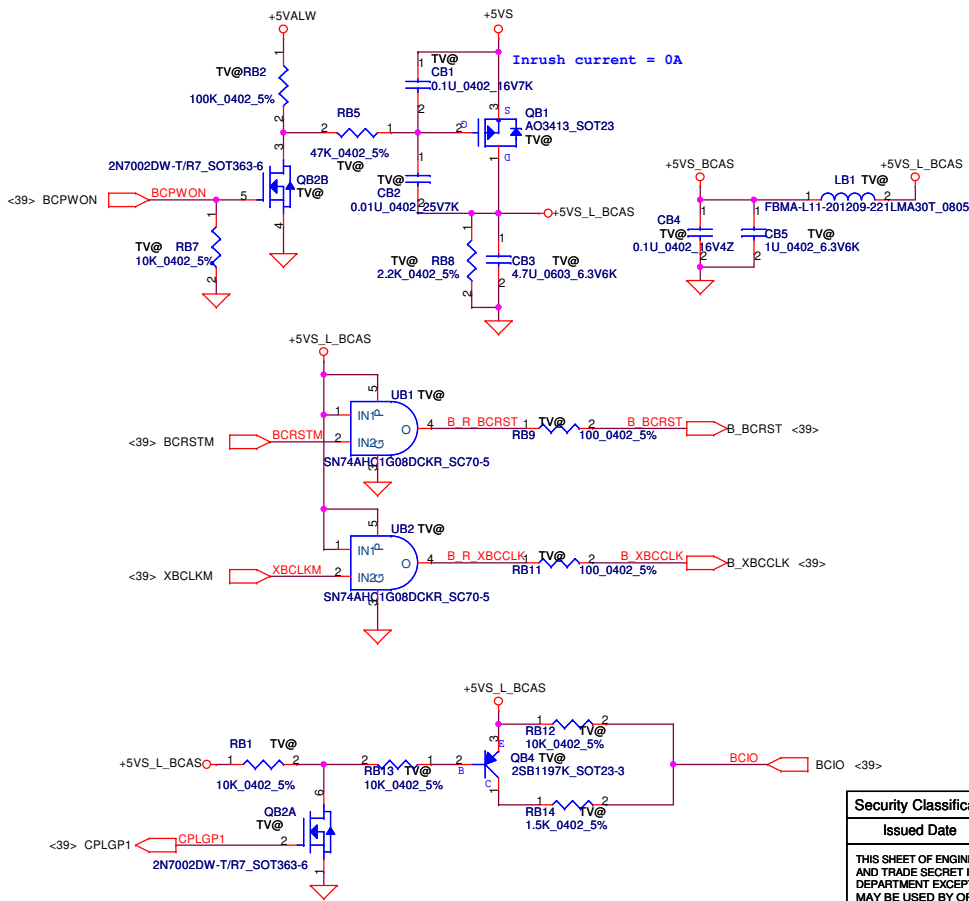


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IR Emitter Connector

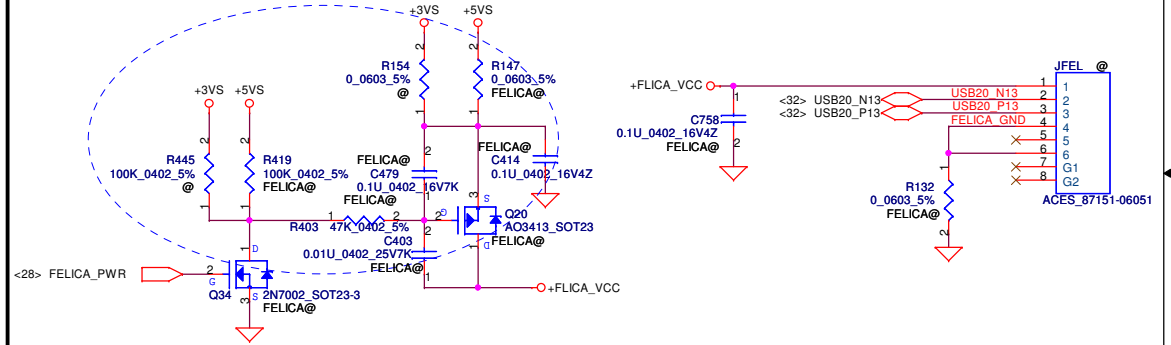


B-CAS Circuit

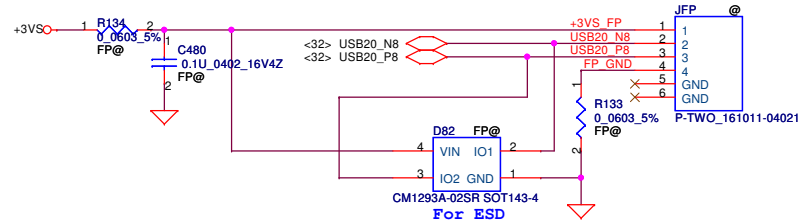


Felica

Reserve +3VS Felica by Customer demand.
2010/09/27

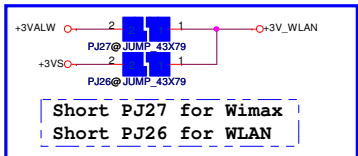


Finger printer



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Size	Document Number	PHQAA LA-6831P M/B		Rev 0.3	
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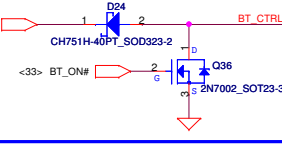
Slot 1 Half PCIe Mini Card-WLAN/ WiMax



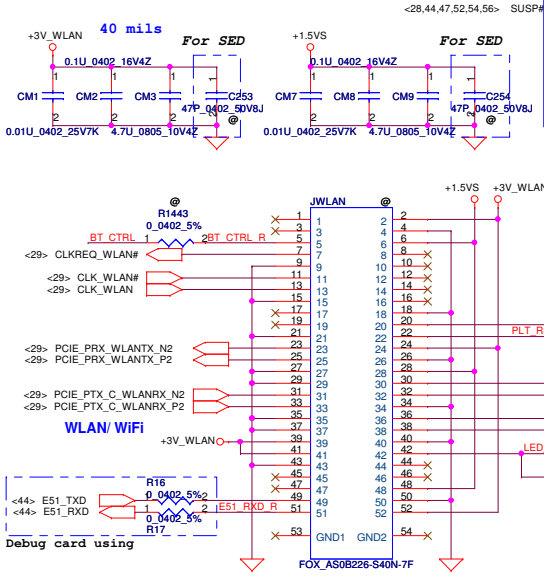
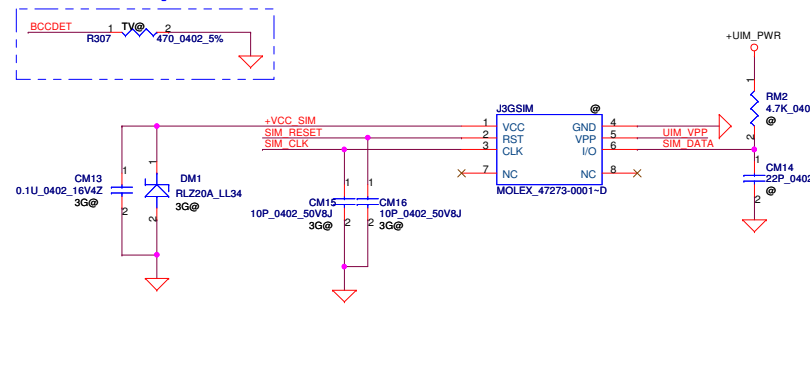
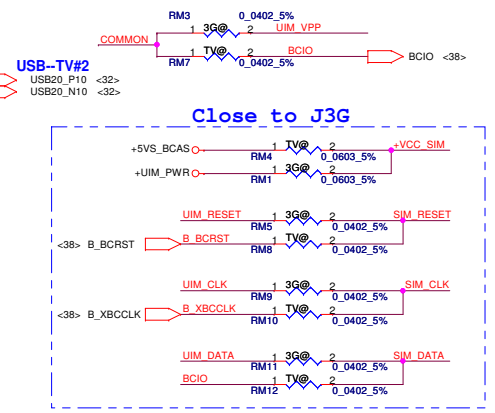
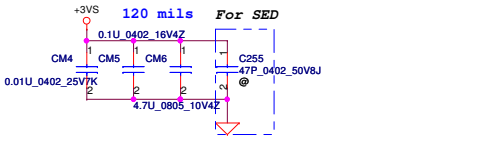
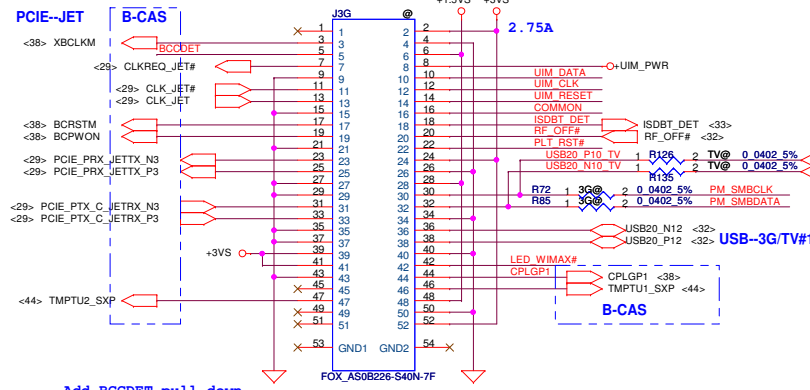
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

**If +3V_WLAN is +3VS, please remove D24



Slot 2 Full PCIe Mini Card- 3G/ TV Tuner Half PCIe Mini Card- JET



USB Sleep & Charge Auto-Mode Mode3/Mode4

MAX14566B

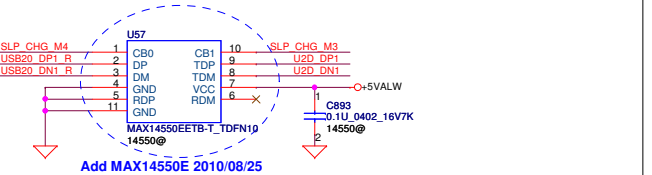
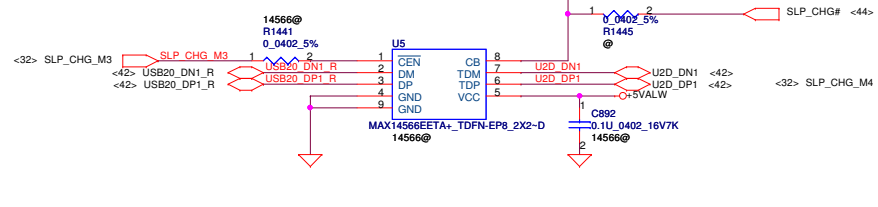
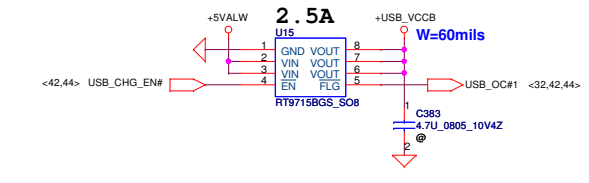
CB0 SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14566E

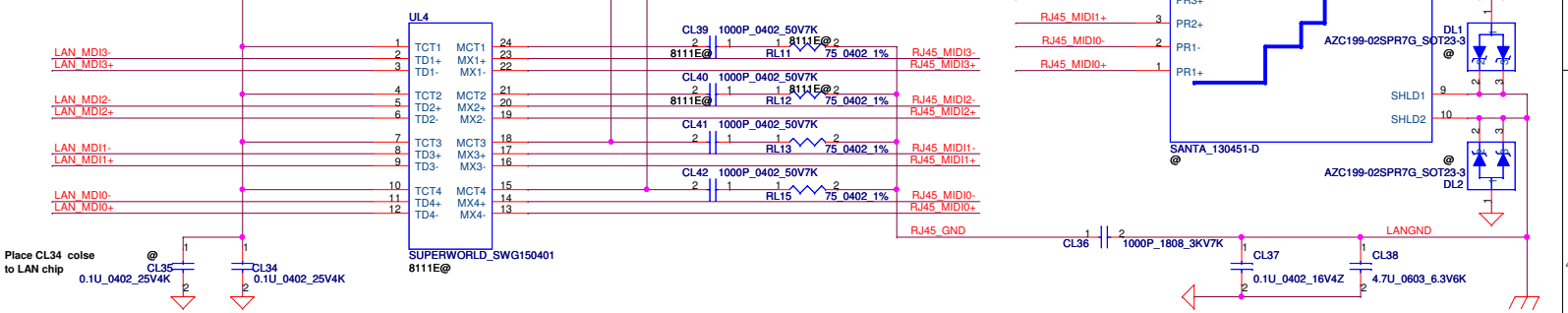
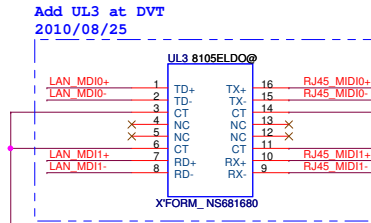
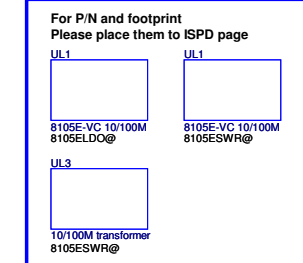
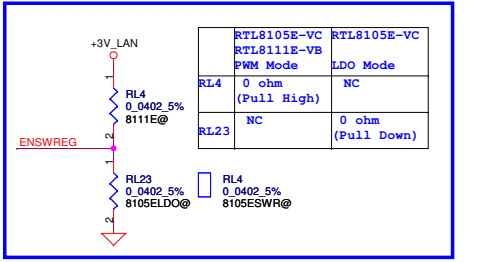
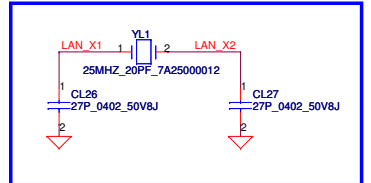
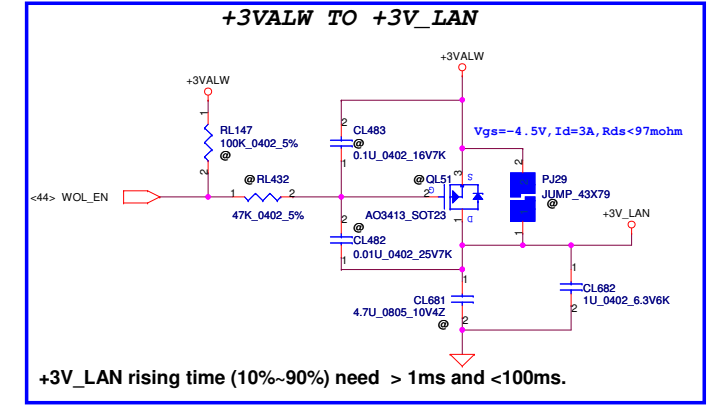
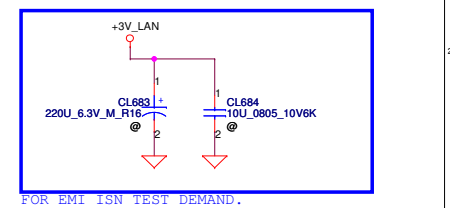
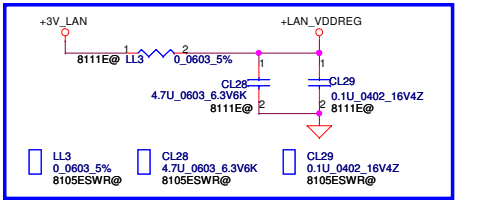
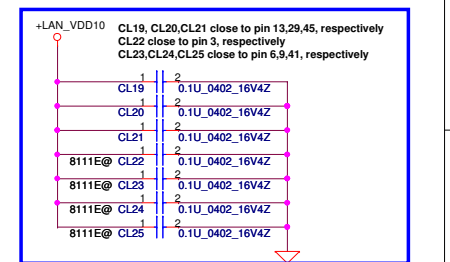
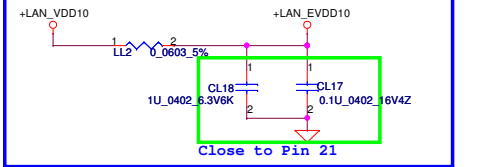
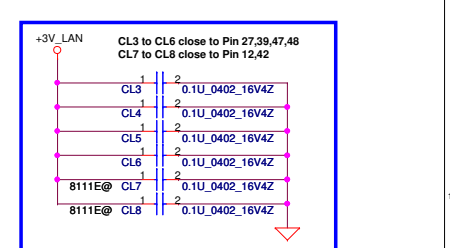
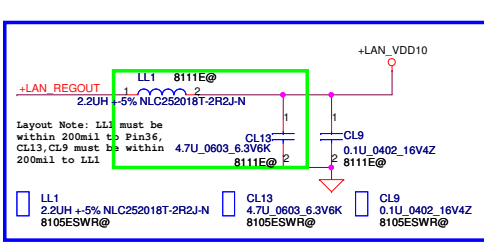
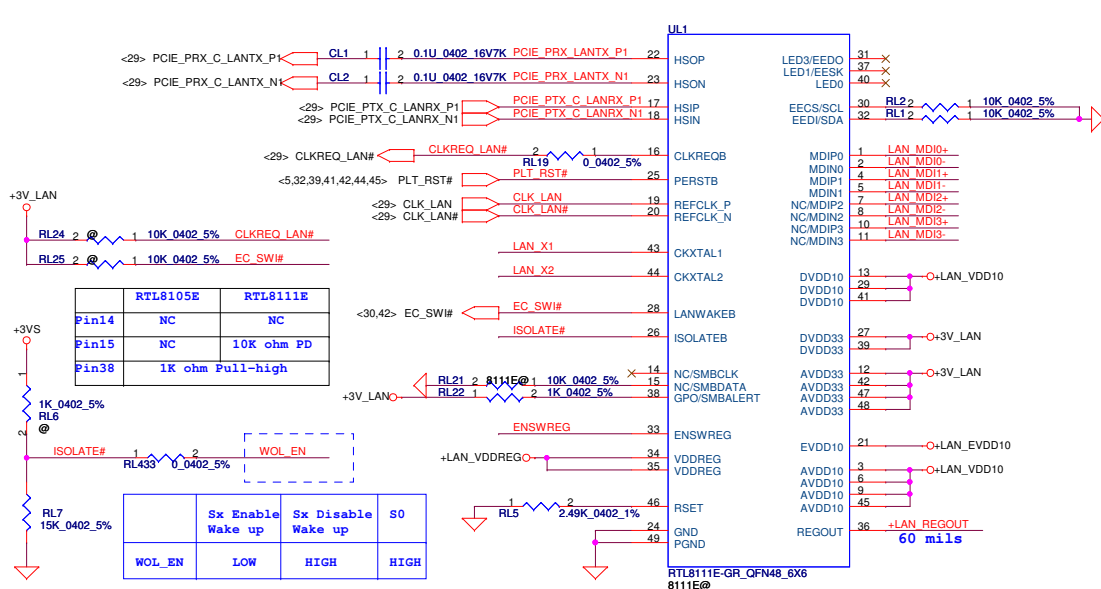
CB0: SLP_CHG_M4	STATUS
0	AUTO MODE
1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14550E

CB0 SLP_CHG_M4	CB1 SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	MODE3
1	0	MODE4
1	1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

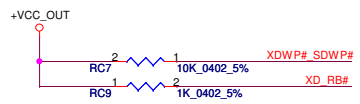
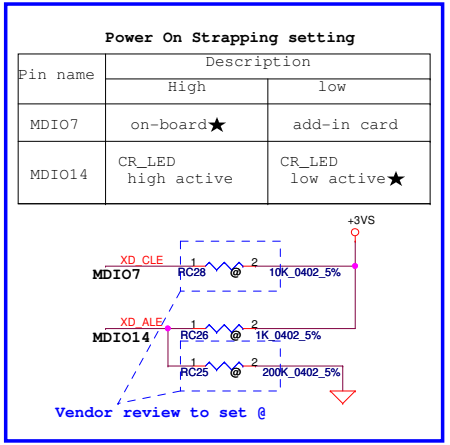
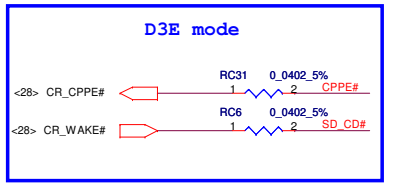
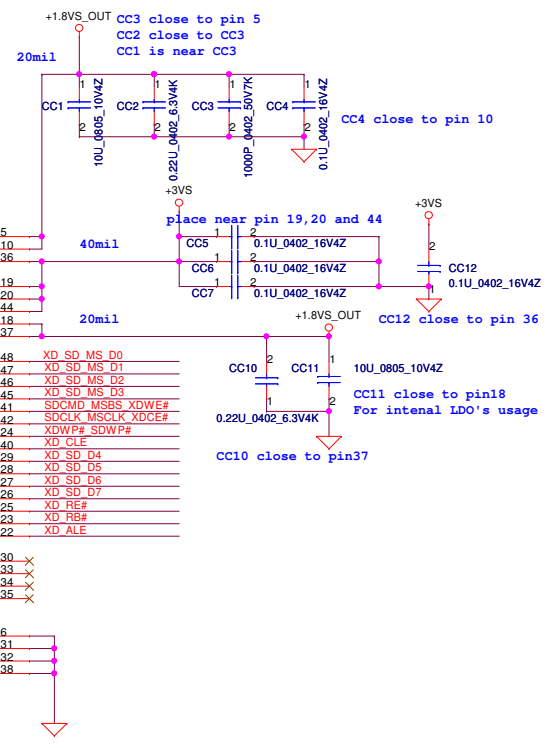


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Size	Document Number	Rev		0.3
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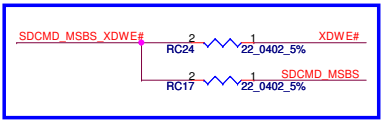


CC16 close to pin43
For internal LDO in SD3.0

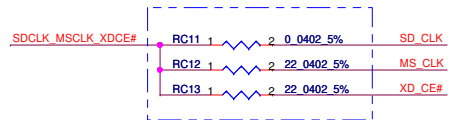
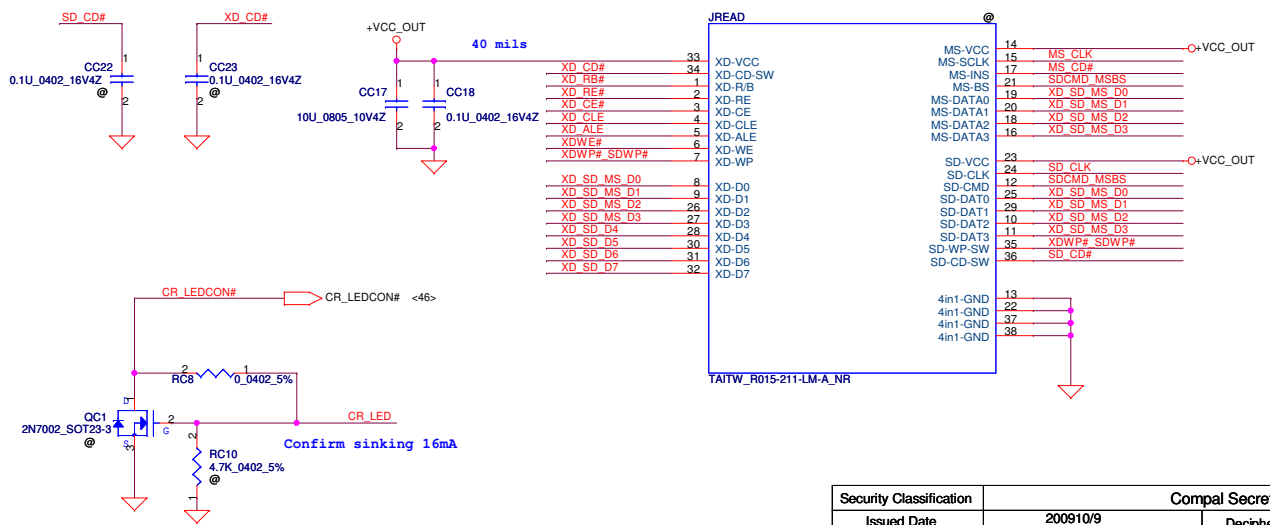
JMB389C



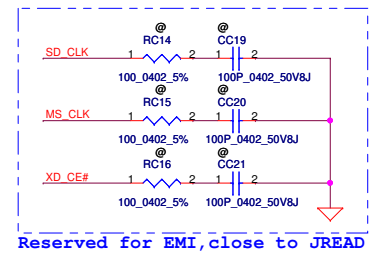
Add RC24 and RC17 close to UC1 for xD issue



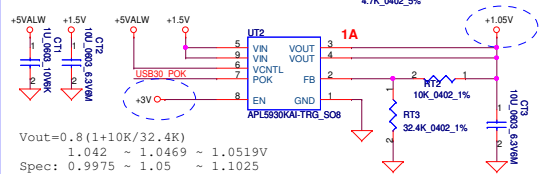
5 in 1 Card Reader



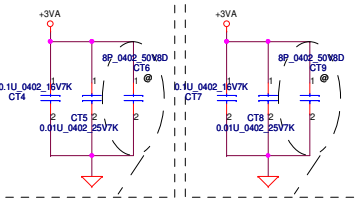
Reserved for EMI, close to UC1.42
Change RC11 from 22ohm to 0ohm
in order fix SDXC performance low.



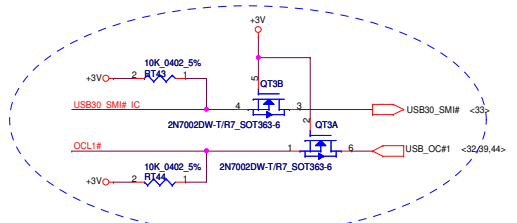
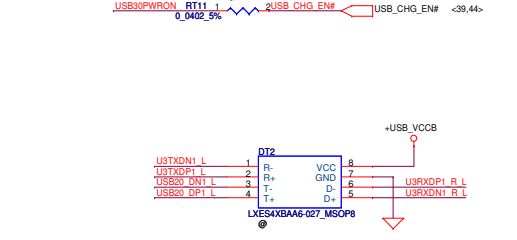
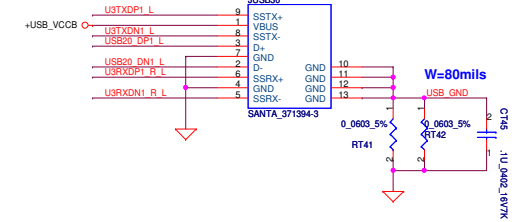
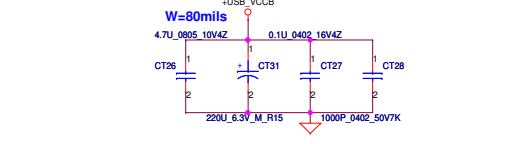
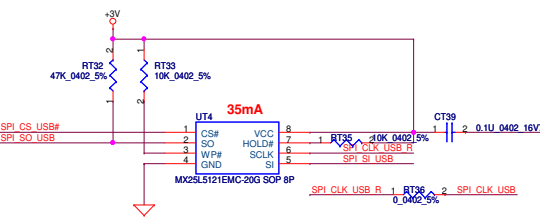
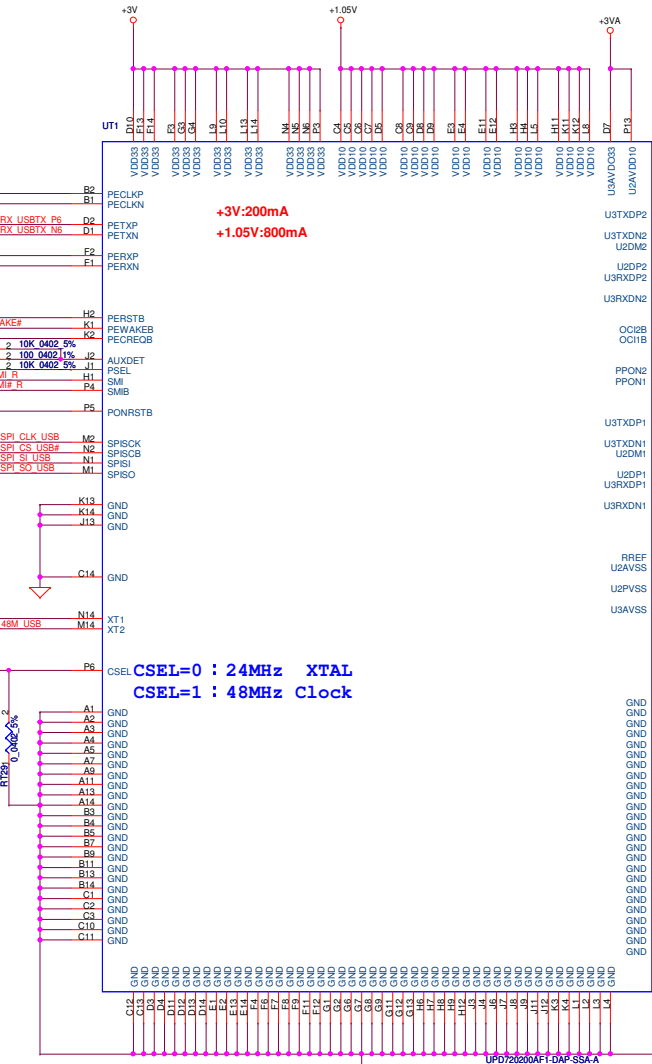
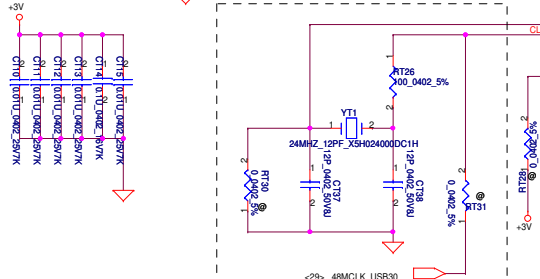
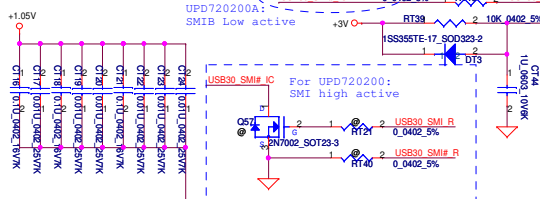
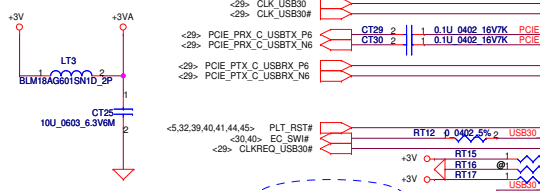
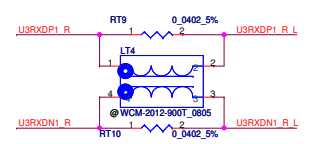
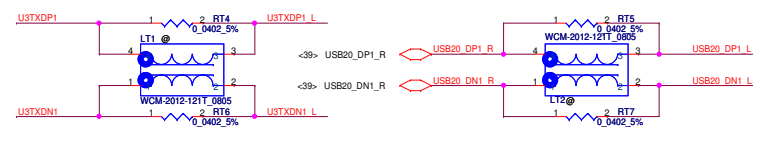
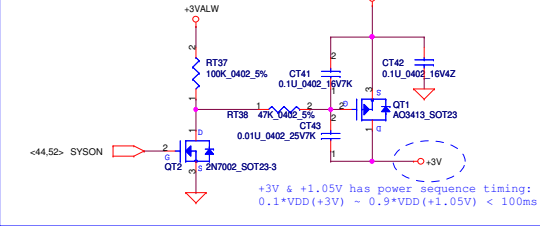
+1.5V to +1.05V Transfer



Close to U102.D7 Close to U102.P13

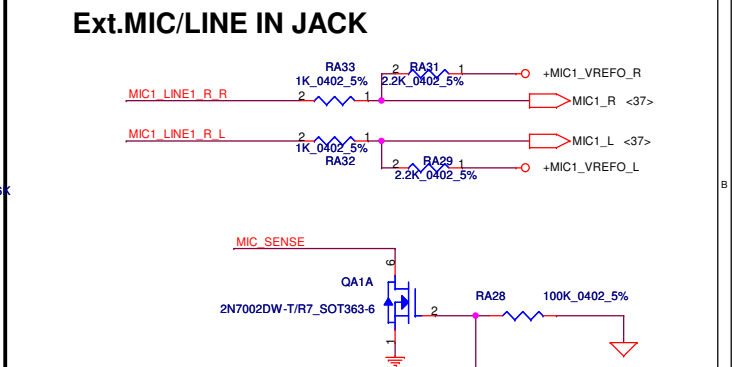
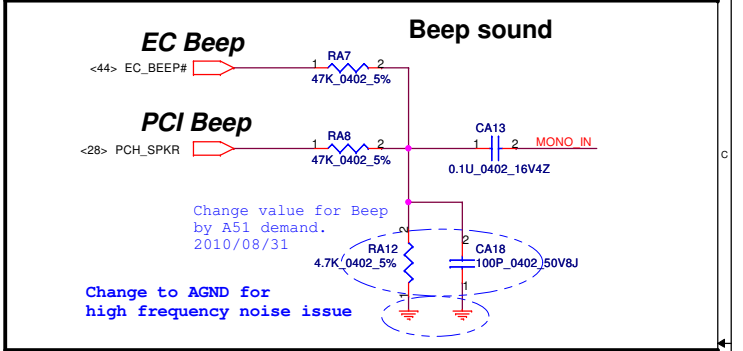
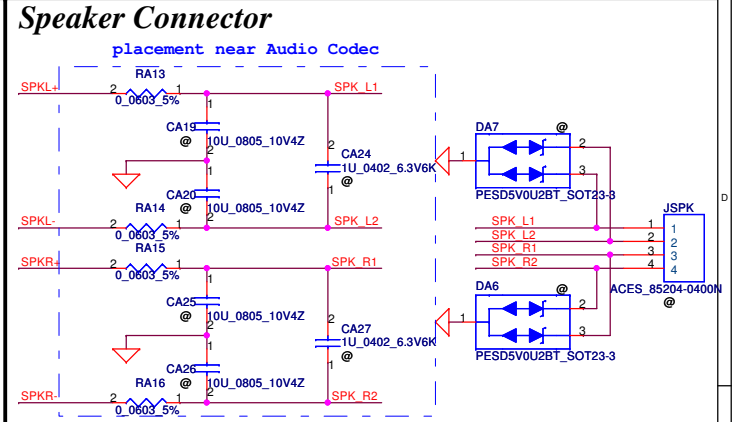
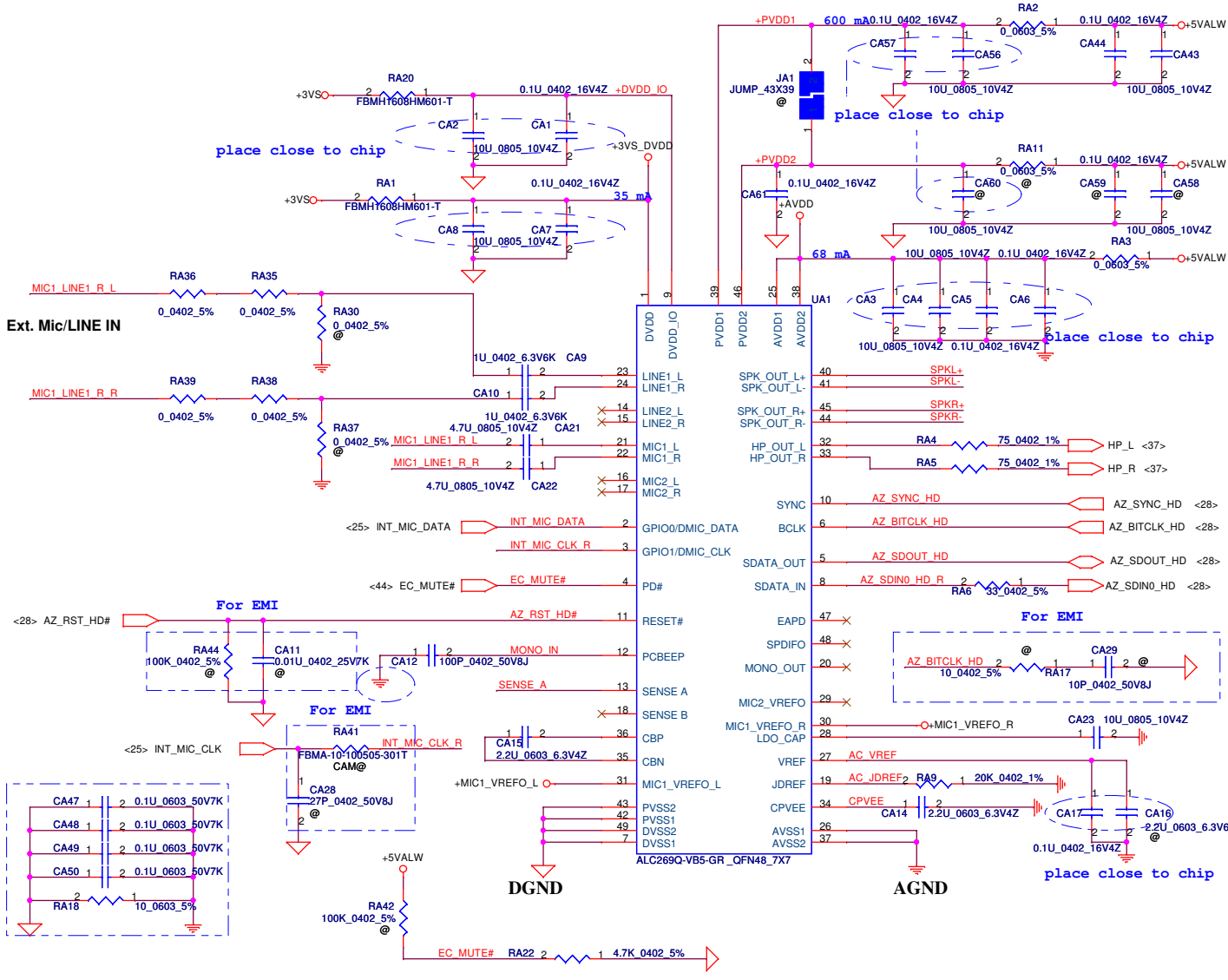


+3VALW to +3V Transfer

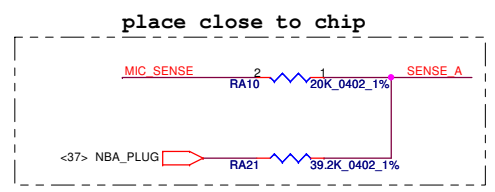


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Issued Date		Deciphered Date		2010/01/23	
200910/9		2010/01/23		PCIE-USB3.0 UPD720200A	
Size		Document Number		Rev	
Custom		PHQAA LA-6831P M/B		0.3	
Date		Thursday, October 07, 2010		Sheet 42 of 58	

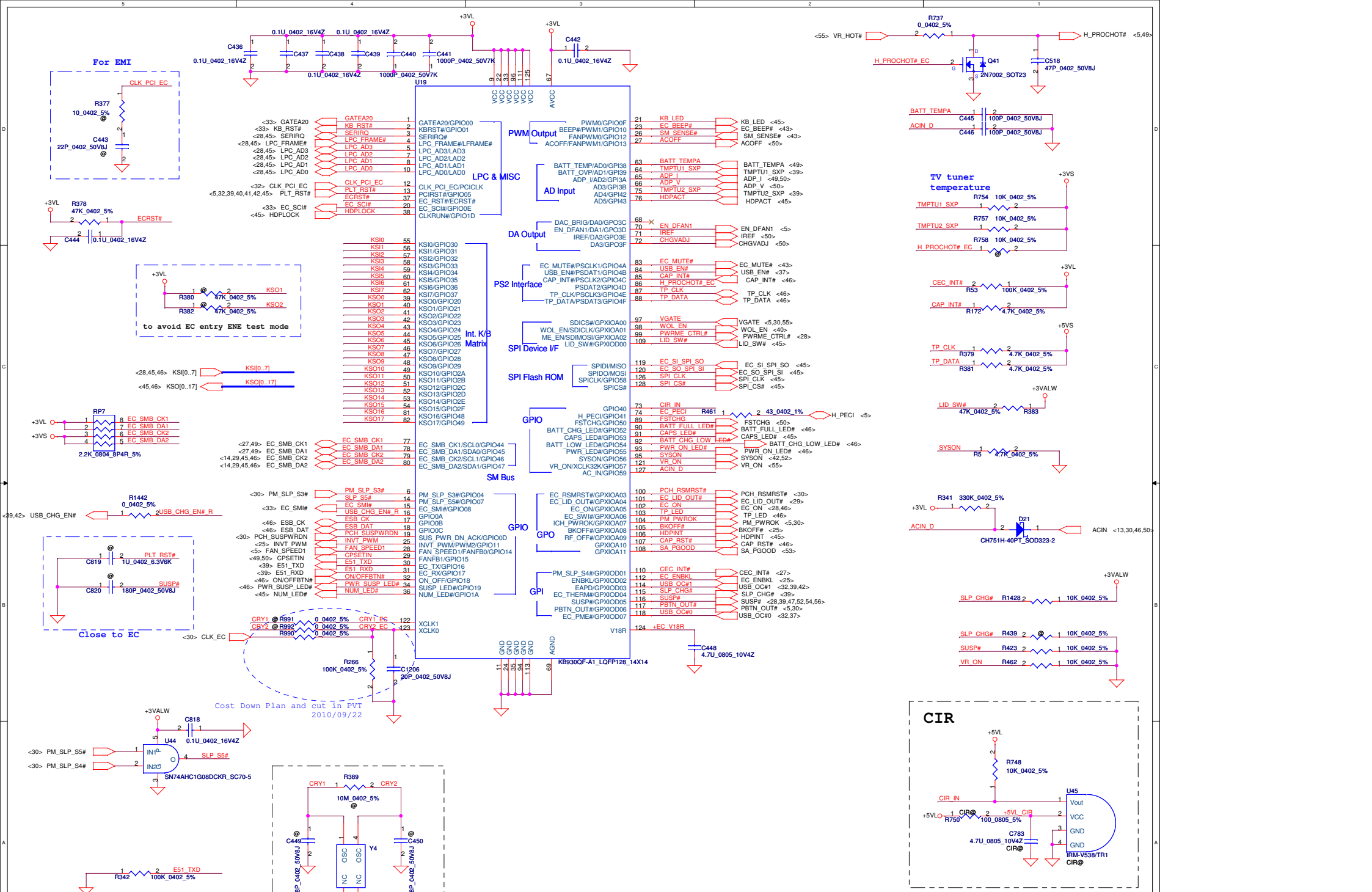
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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



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				PHQAA LA-6831P M/B	
				Date	Thursday, October 07, 2010
				Sheet	43 of 58

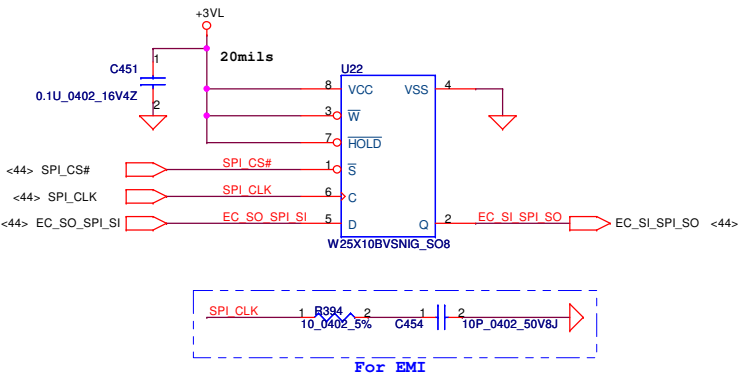


Security Classification	Compal Secret Data	
Issued Date	200910/9	Deciphered Date
		2010/01/23

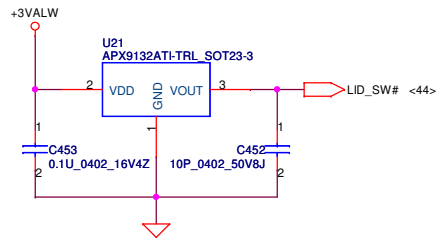
Compal Electronics, Inc.		
LPC-EC-KB930		
Size	Document Number	Rev
	PHQAA LA-6831P M/B	0.3
Date:	Thursday, October 07, 2010	Sheet 44 of 58

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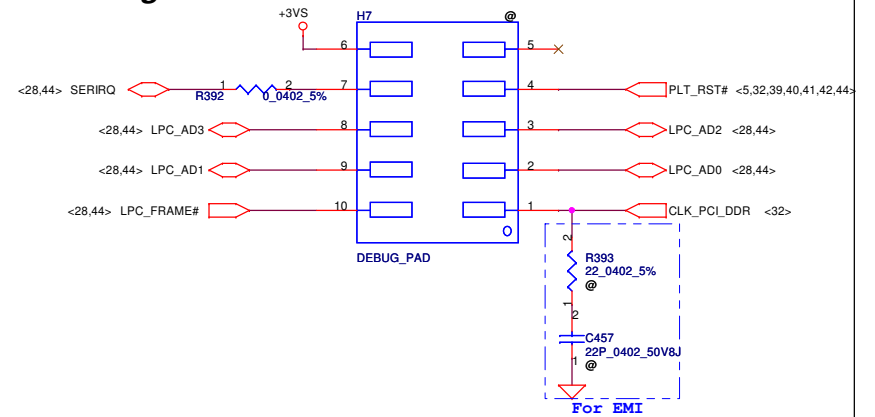
SPI Flash (256KB)



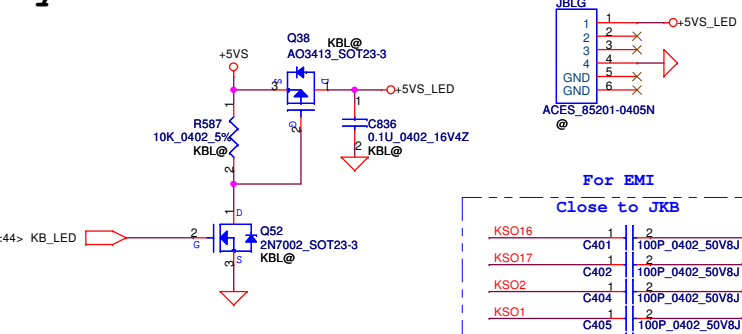
Lid SW



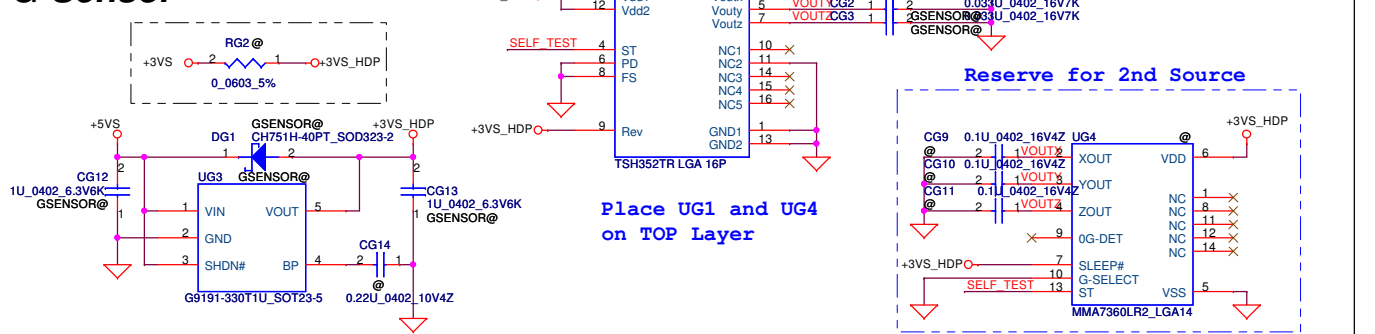
LPC Debug Port



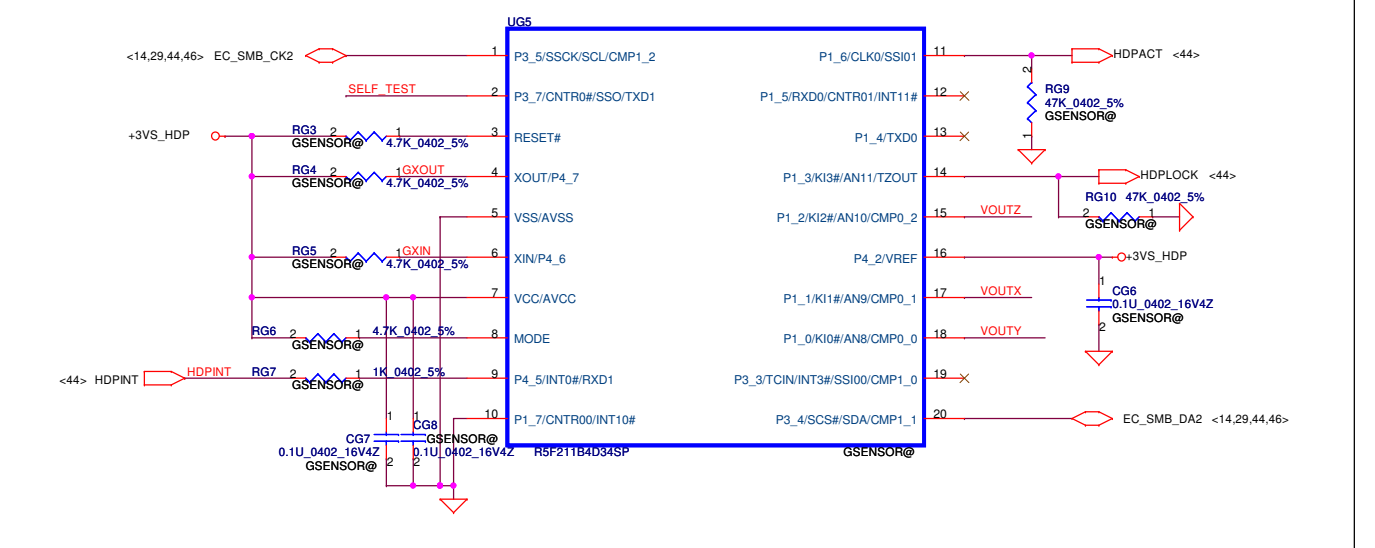
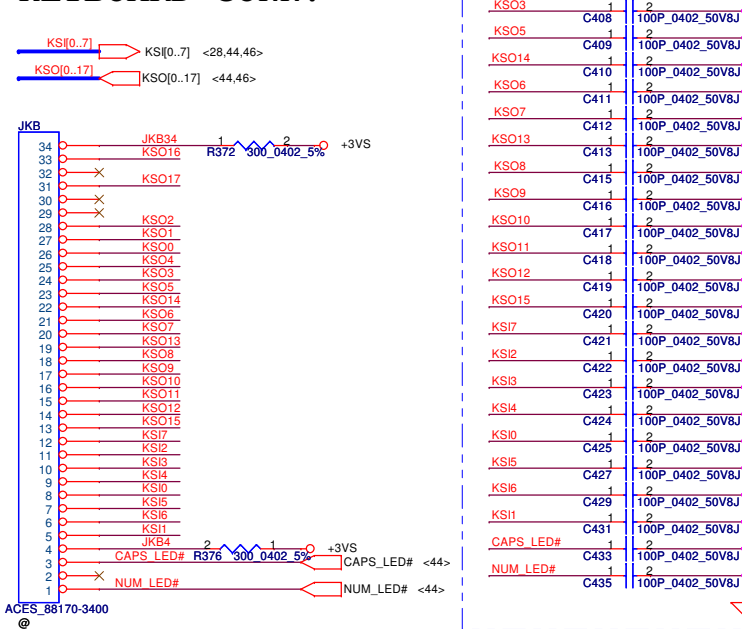
Keyboard LED



G-Sensor

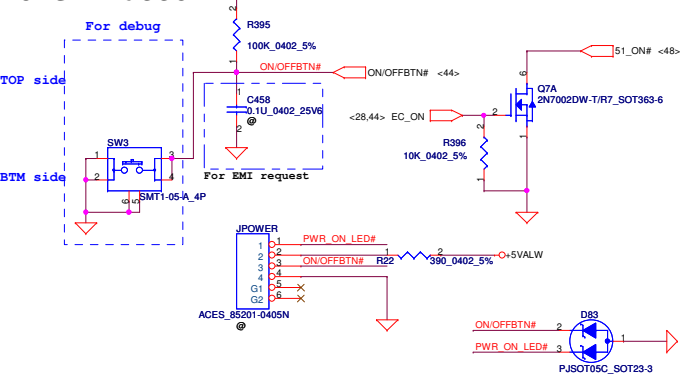


KEYBOARD CONN.

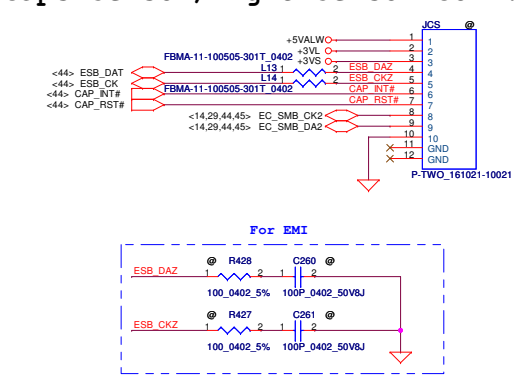


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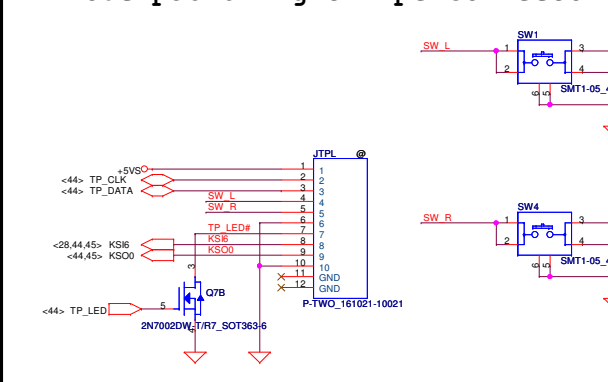
Power Button



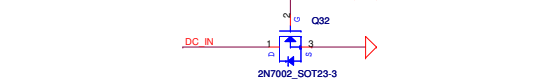
Caps Sensor/Light Sensor Conn.



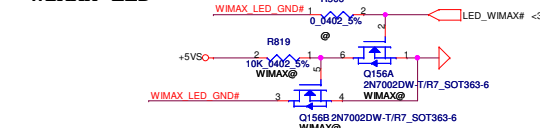
Touchpad & Light Pipe Connector



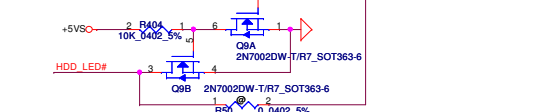
DC-IN LED



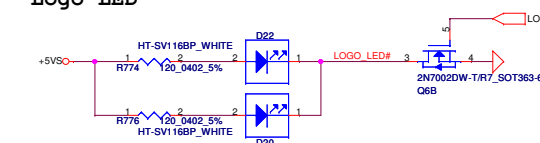
WiMAX LED



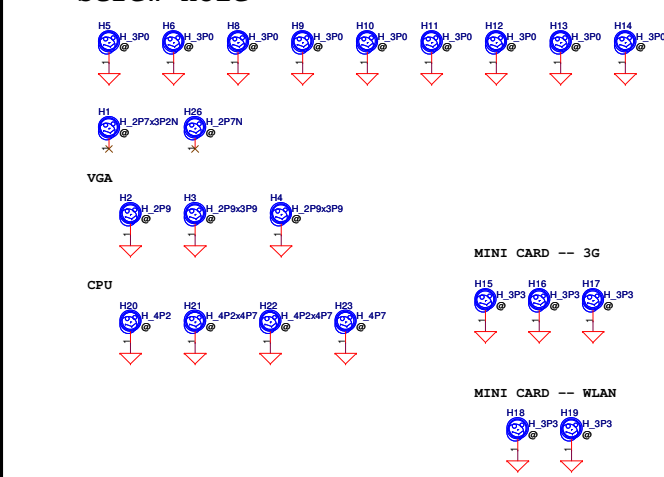
HDD LED



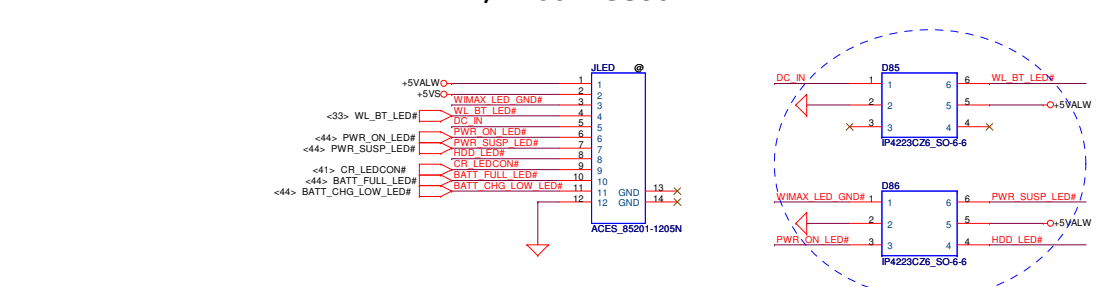
Logo LED



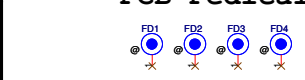
Screw Hole



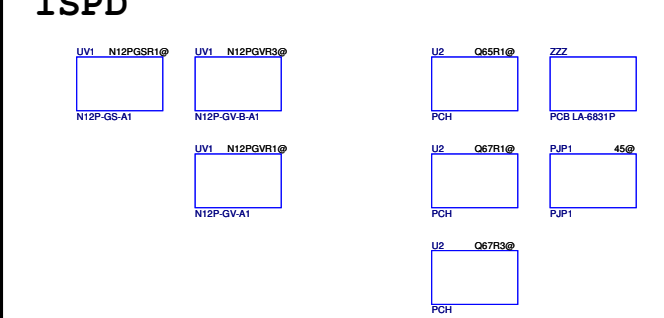
LED/B Connector



PCB Federal Mark PAD

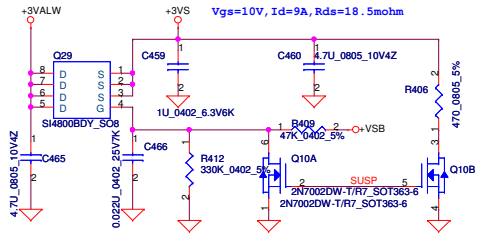


ISPD

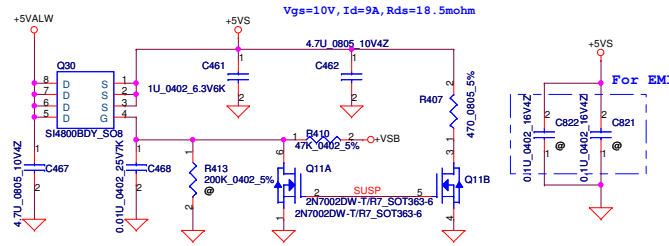


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Date:	Thursday, October 07, 2010	Sheet	46	of 58

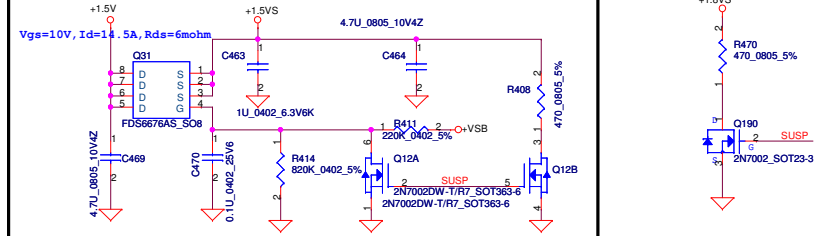
+3VALW TO +3VS



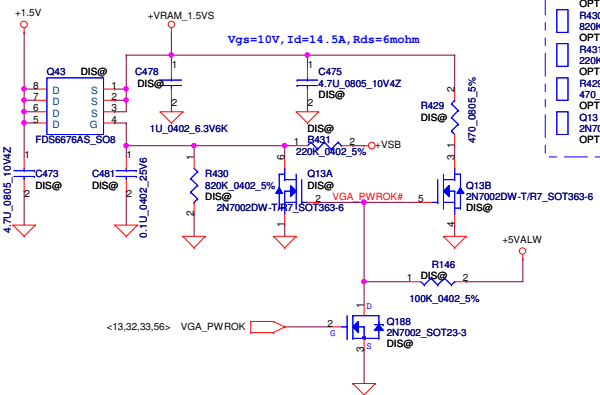
+5VALW TO +5VS



+1.5V to +1.5VS

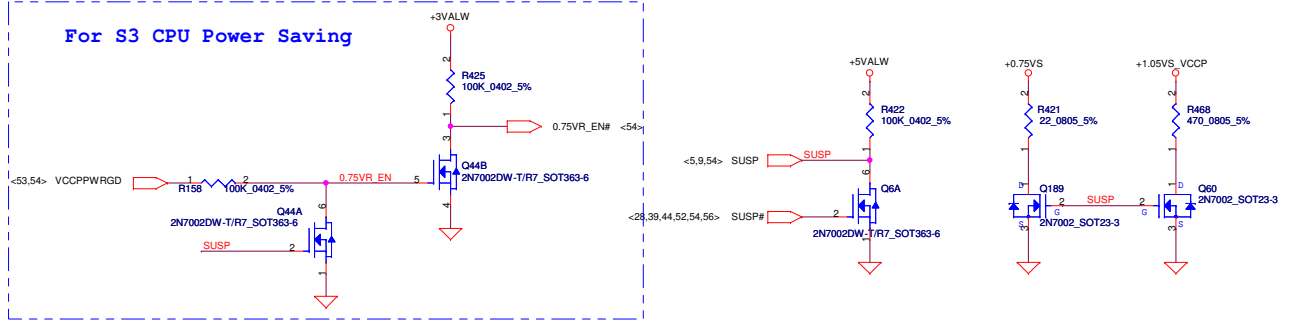


+1.5V to +VRAM_1.5VS

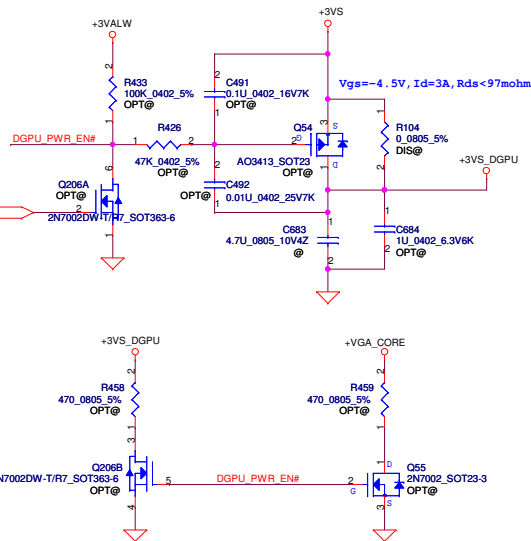


- Q43 FDS5676AS_S08
- C473 4.7U_0805_10V4Z
- C481 1U_0402_25V6
- C475 4.7U_0805_10V4Z
- R430 820K_0402_5%
- R431 220K_0402_5%
- R429 470_0805_5%
- Q13 2N7002DW-T/R7_SOT363-6
- C478 1U_0402_6.3V6K
- C475 4.7U_0805_10V4Z
- R416 100K_0402_5%
- R418 470_0805_5%
- Q188 2N7002_SOT23-3

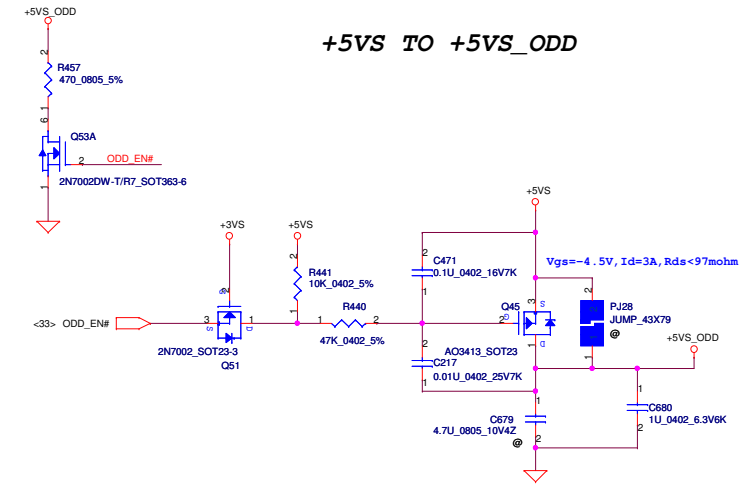
For S3 CPU Power Saving



+3VS to +3VS_DGPU

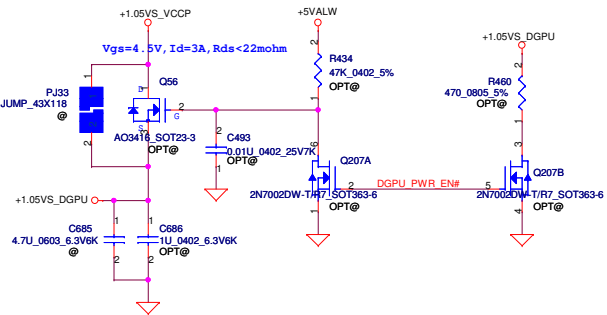


+5VS TO +5VS_ODD



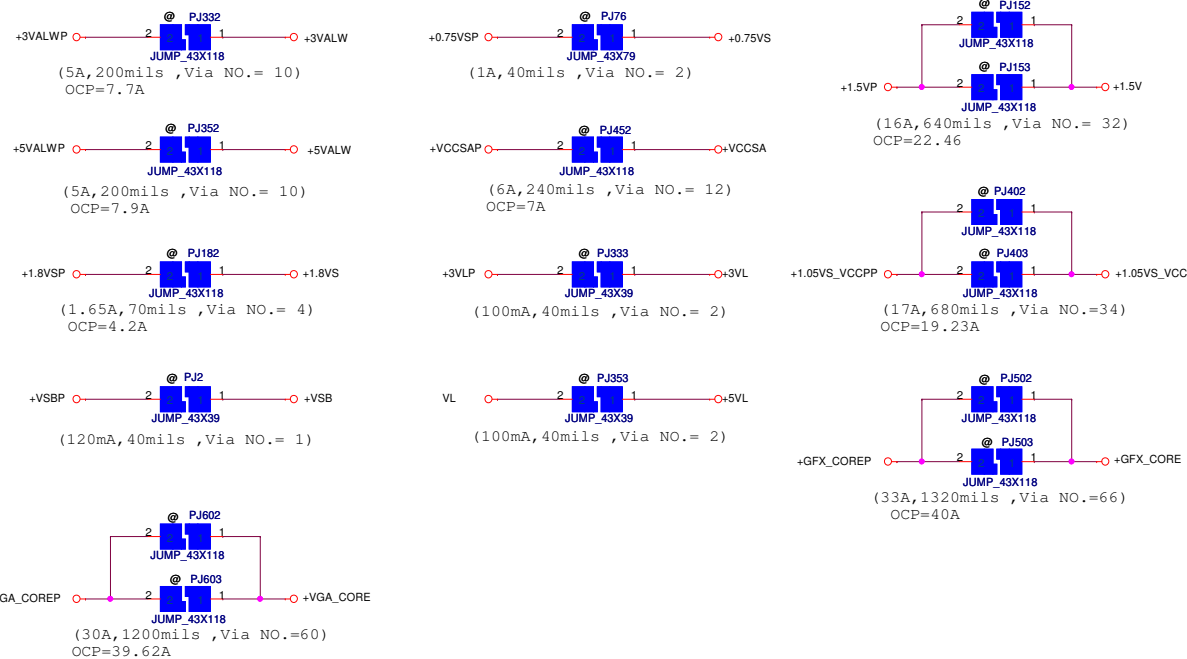
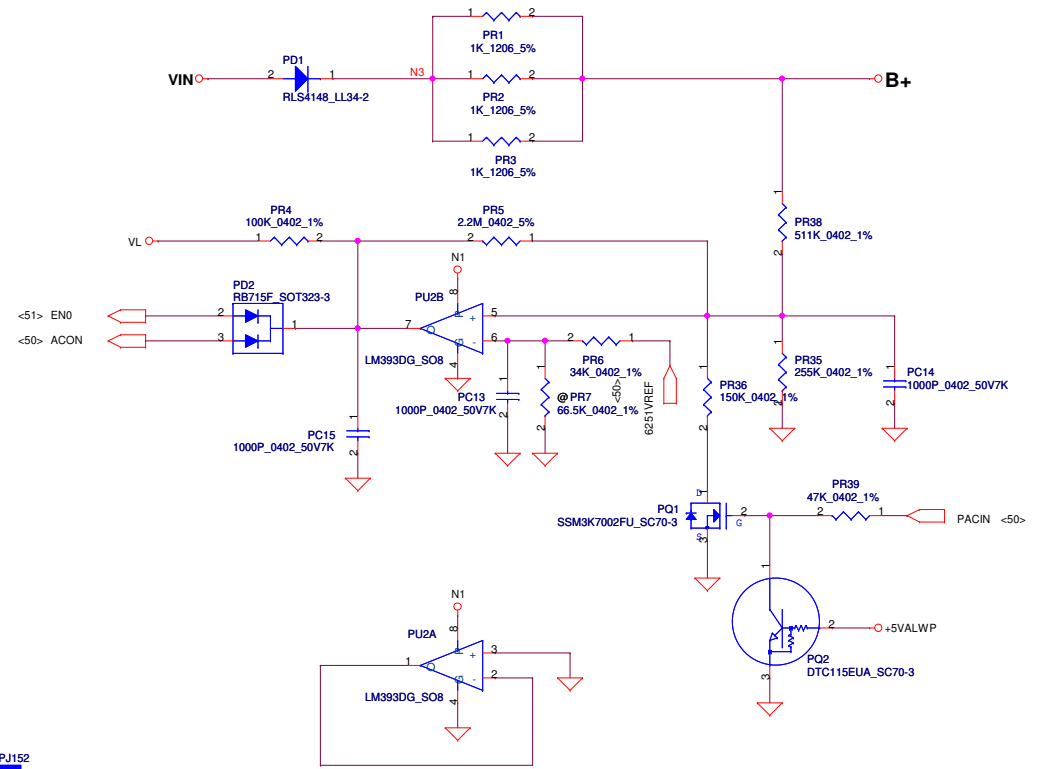
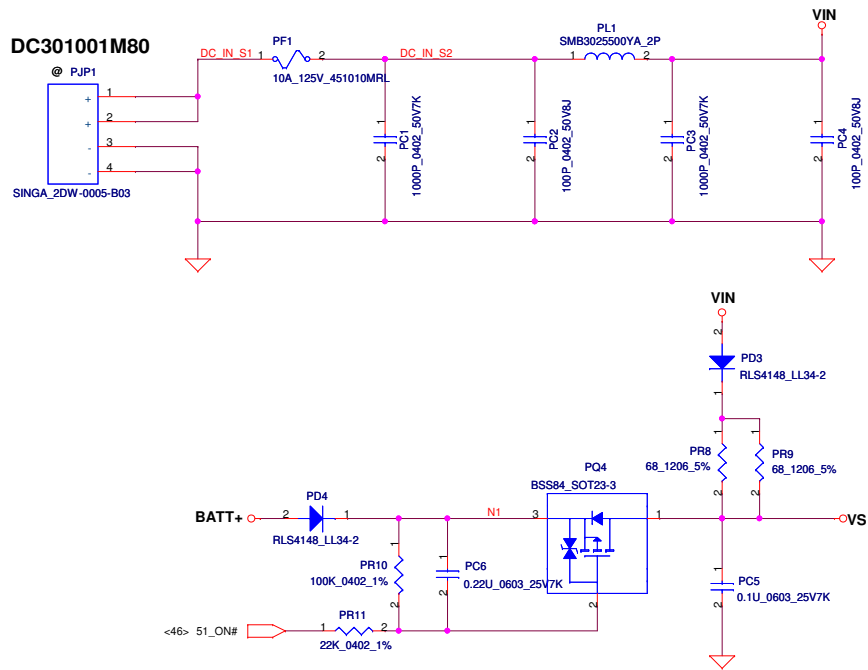
+1.05VS_VCCP to +1.05VS_DGPU

Short PJ33 for Discrete SKUs

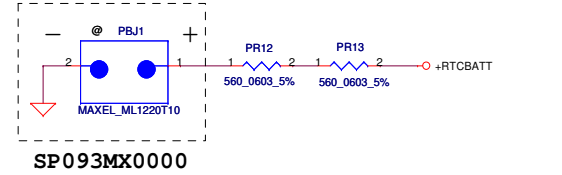


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DC301001M80

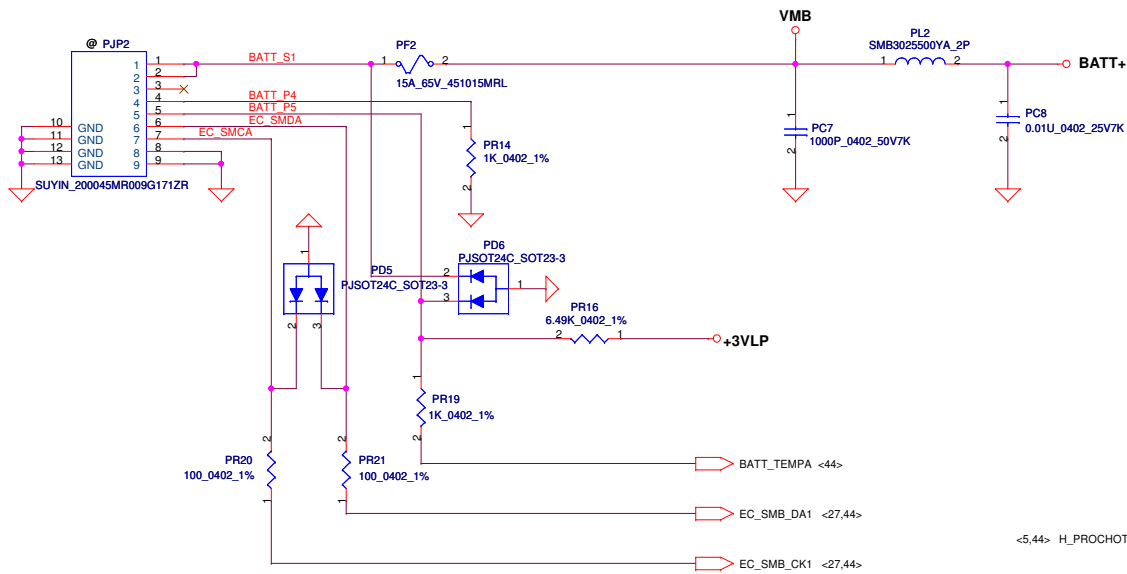


RTC Battery

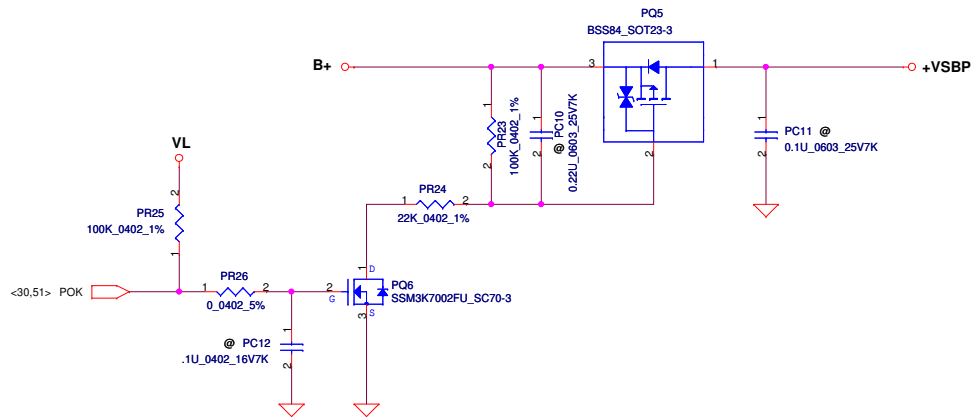
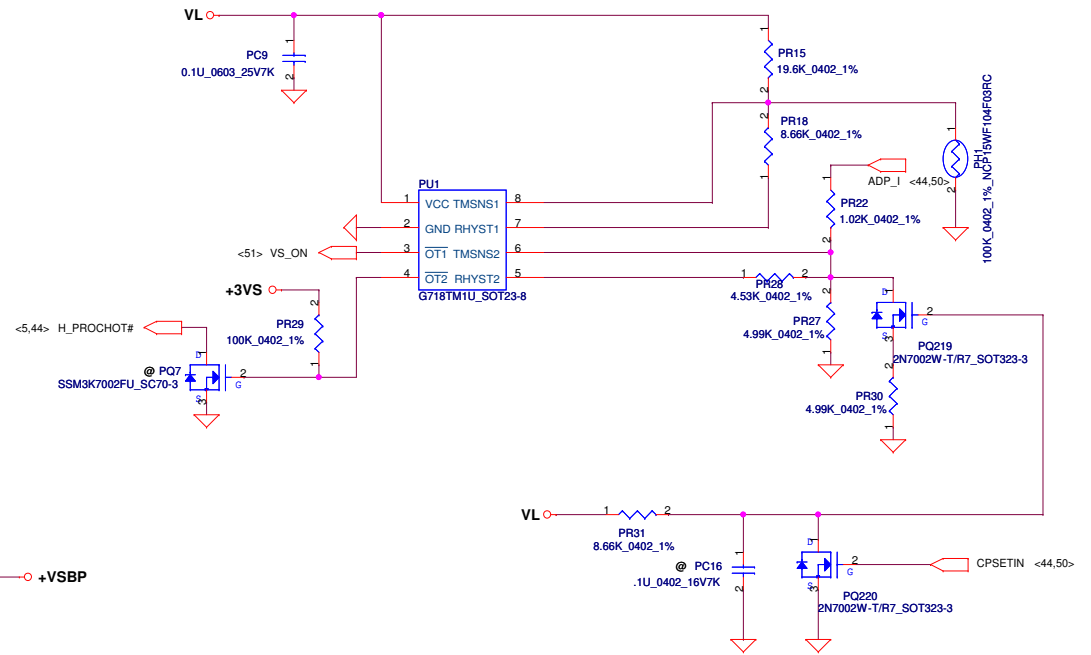


ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.42V	14.74V	15.23V
L->H	15.39V	15.88V	16.39V

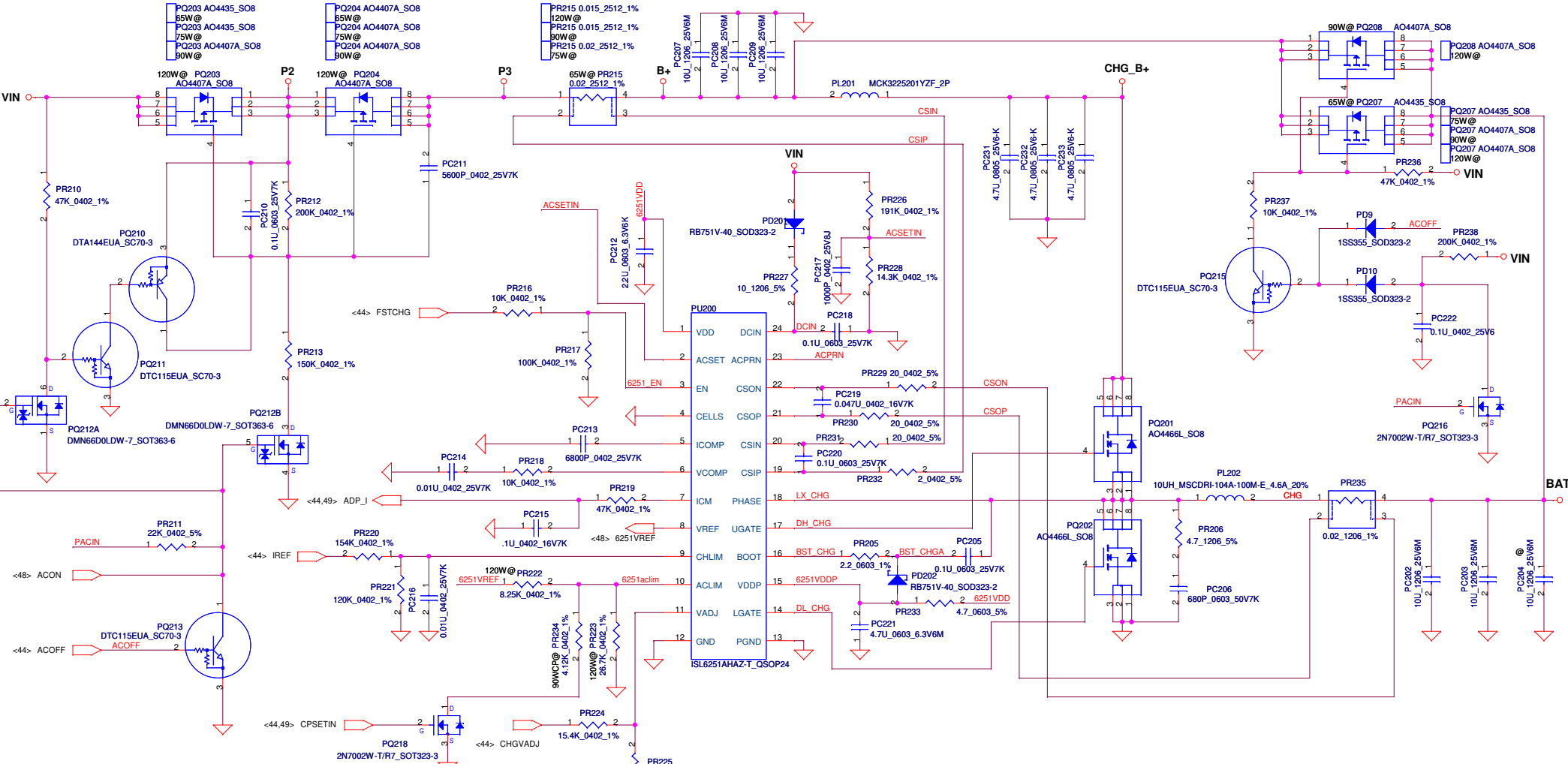
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Issued Date	2009/11/13	Deciphered Date	2009/04/28	Title	
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Size	Document Number	PHQAA LA-6831P M/B		Rev 0.1	
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PH1 under CPU botten side :
 CPU thermal protection at 95 degree C
 Recovery at 56 degree C



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- PR222 75K_0402_1% 65W@
- PR222 24K_0402_1% 75W@
- PR222 53.6K_0402_1% 90W@
- PR223 20K_0402_1% 65W@
- PR223 20K_0402_1% 75W@
- PR223 20K_0402_1% 90W@
- PR234 12.4K_0402_1% 65WCP@
- PR234 4.99K_0402_1% 75WCP@

CP mode

I_{ada}=0~3.42A (65W) CP= 92%*I_{ada}; CP=3.147A
 Vac_{lim}=1.08V (65W) PR222=75k PR223=20k PR45=0.02

I_{ada}=0~3.947A (75W) CP= 92%*I_{ada}; CP=3.63A
 Vac_{lim}=0.736V (75W) PR222=24k PR223=20k PR45=0.02

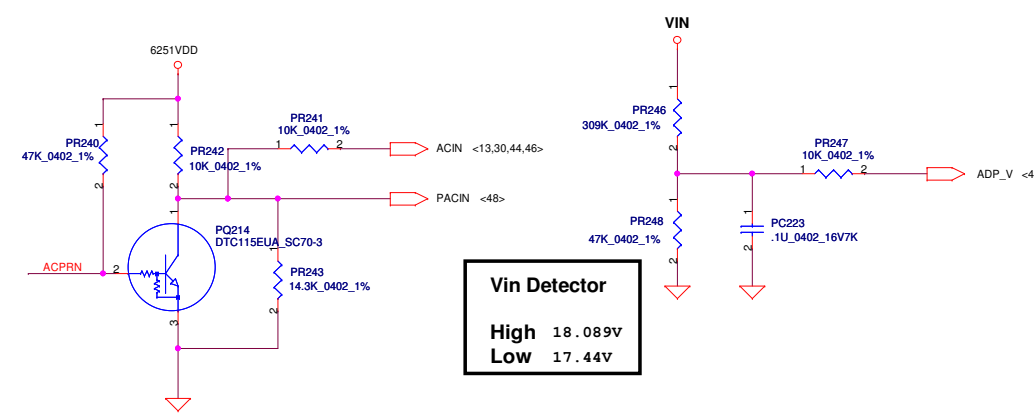
I_{ada}=0~4.737A (90W) CP= 92%*I_{ada}; CP=4.36A
 Vac_{lim}=0.736V (90W) PR222=53.6k PR223=20k PR45=0.015

I_{ada}=0~6.316A (120W) CP= 92%*I_{ada}; CP=5.81A
 Vac_{lim}=0.736V (120W) PR222=8.25k PR223=26.7k PR45=0.015

CC=0.25A-3A

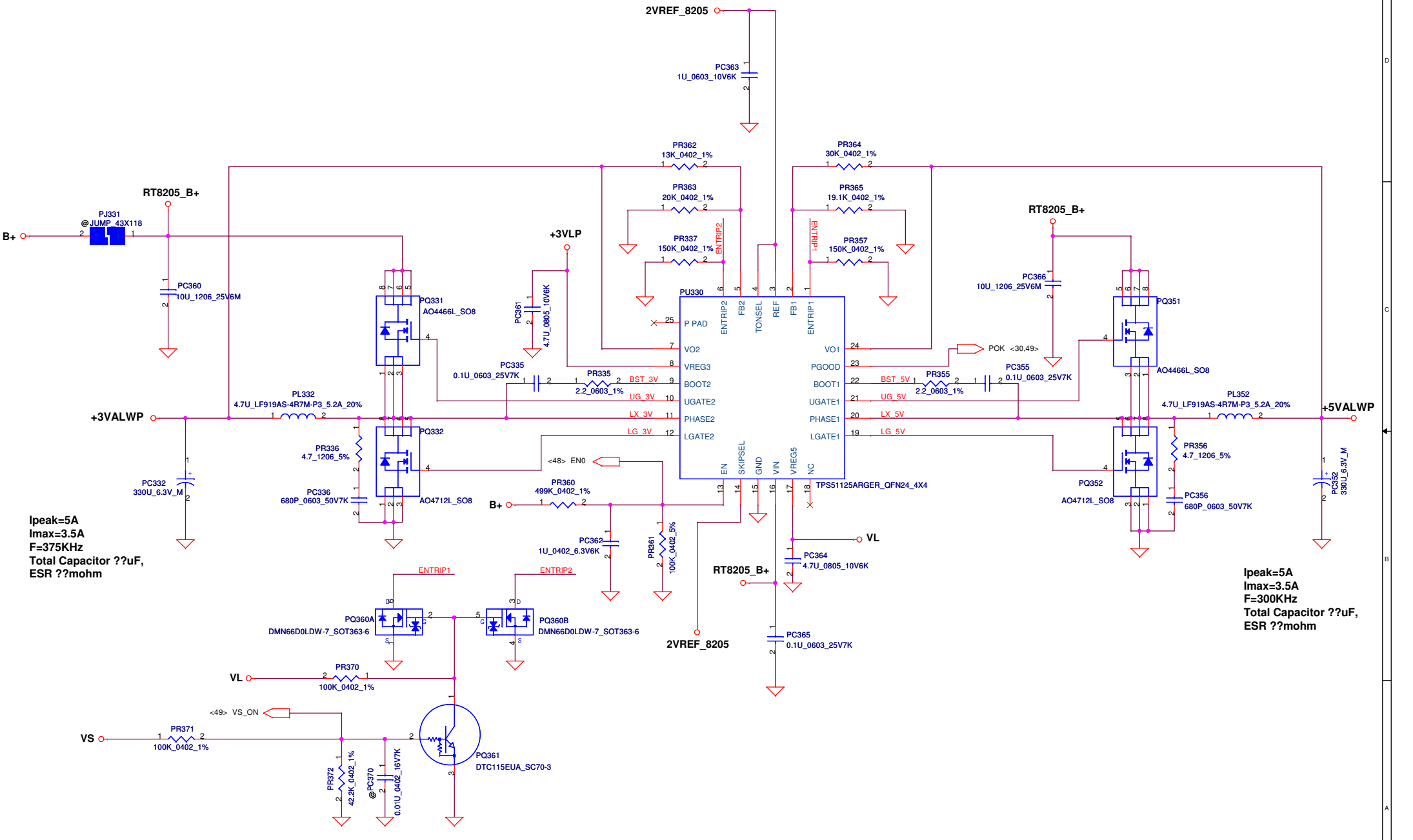
I_{REF}=1.016*I_{charge}
 I_{REF}=0.254V-3.048V
 V_{CHLIM} need over 95mV

CHGVADJ=(V _{cell} -4)*9.445	
V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V



Vin Detector

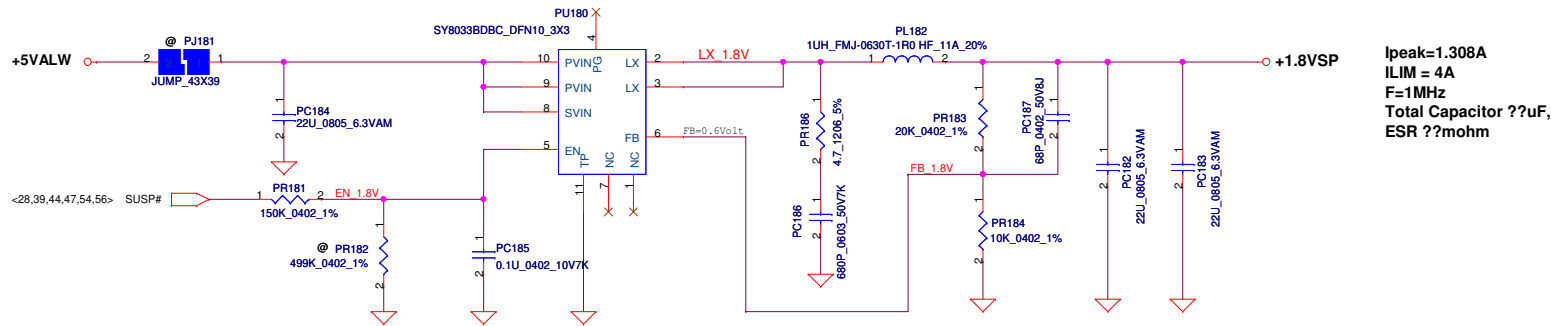
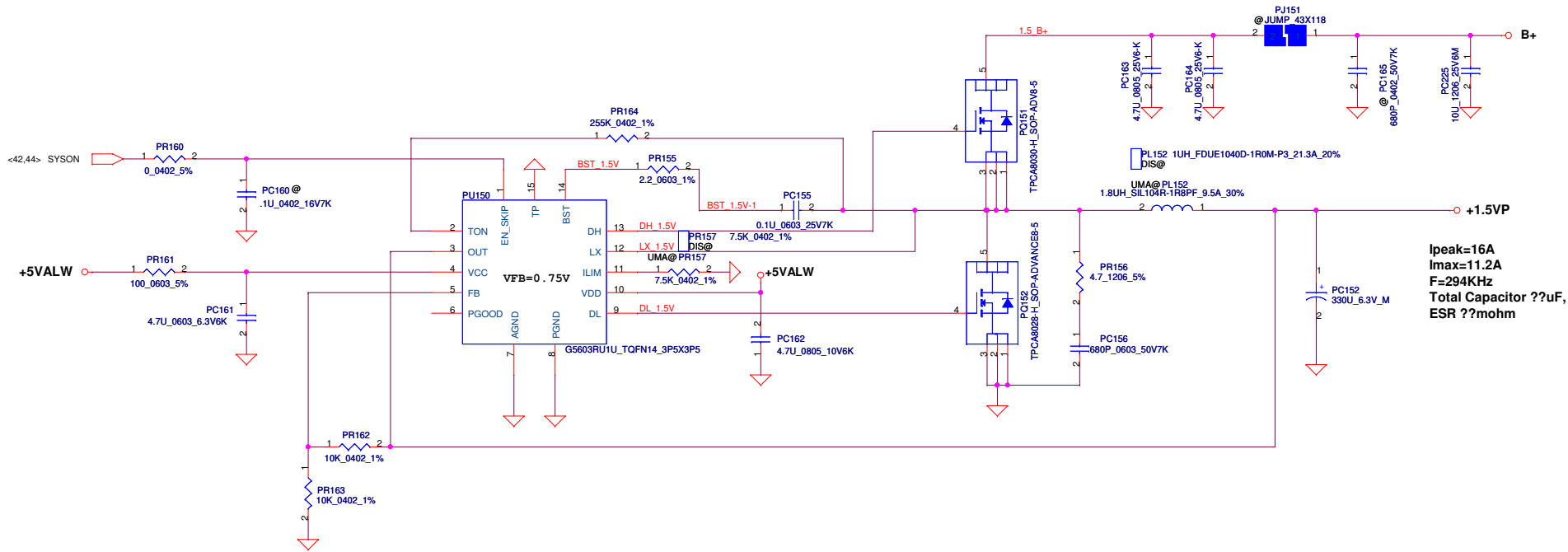
High 18.089V
 Low 17.44V



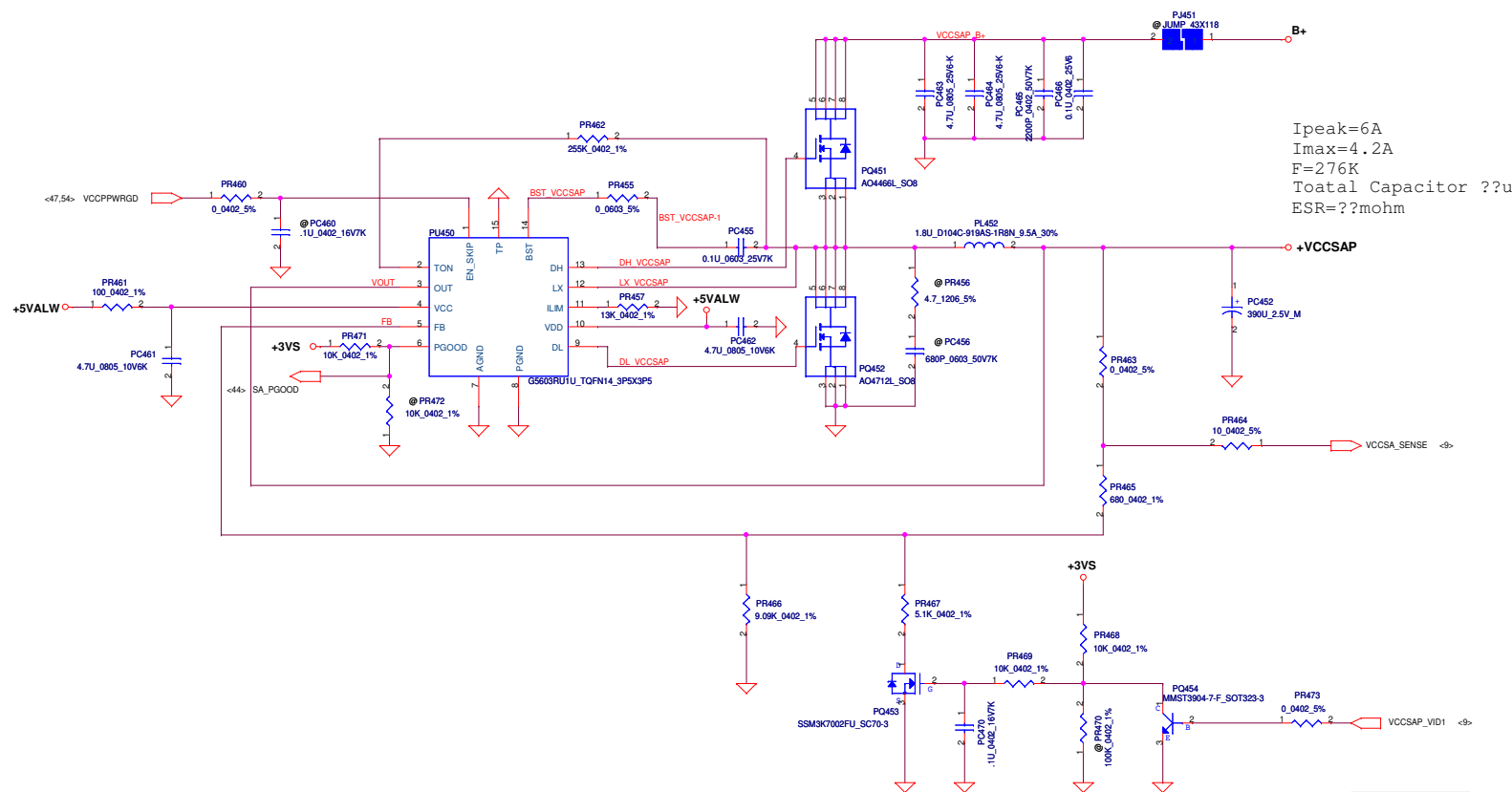
Ipeak=5A
 Imax=3.5A
 F=375KHz
 Total Capacitor ??uF,
 ESR ??mohm

Ipeak=5A
 Imax=3.5A
 F=300KHz
 Total Capacitor ??uF,
 ESR ??mohm

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				3VALWP/5VALWP	
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				PHQAA LA-6831P M/B 0.1	
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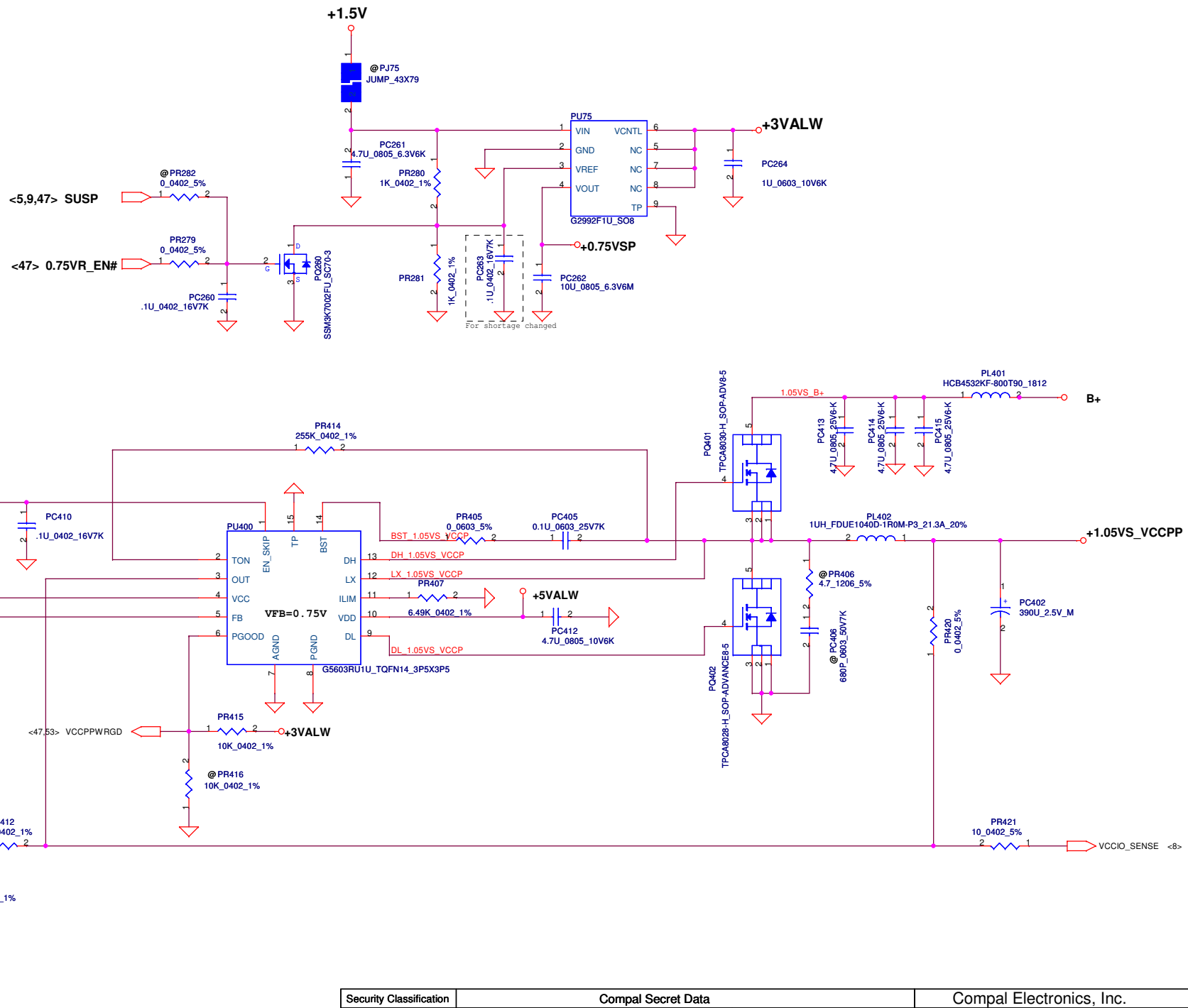


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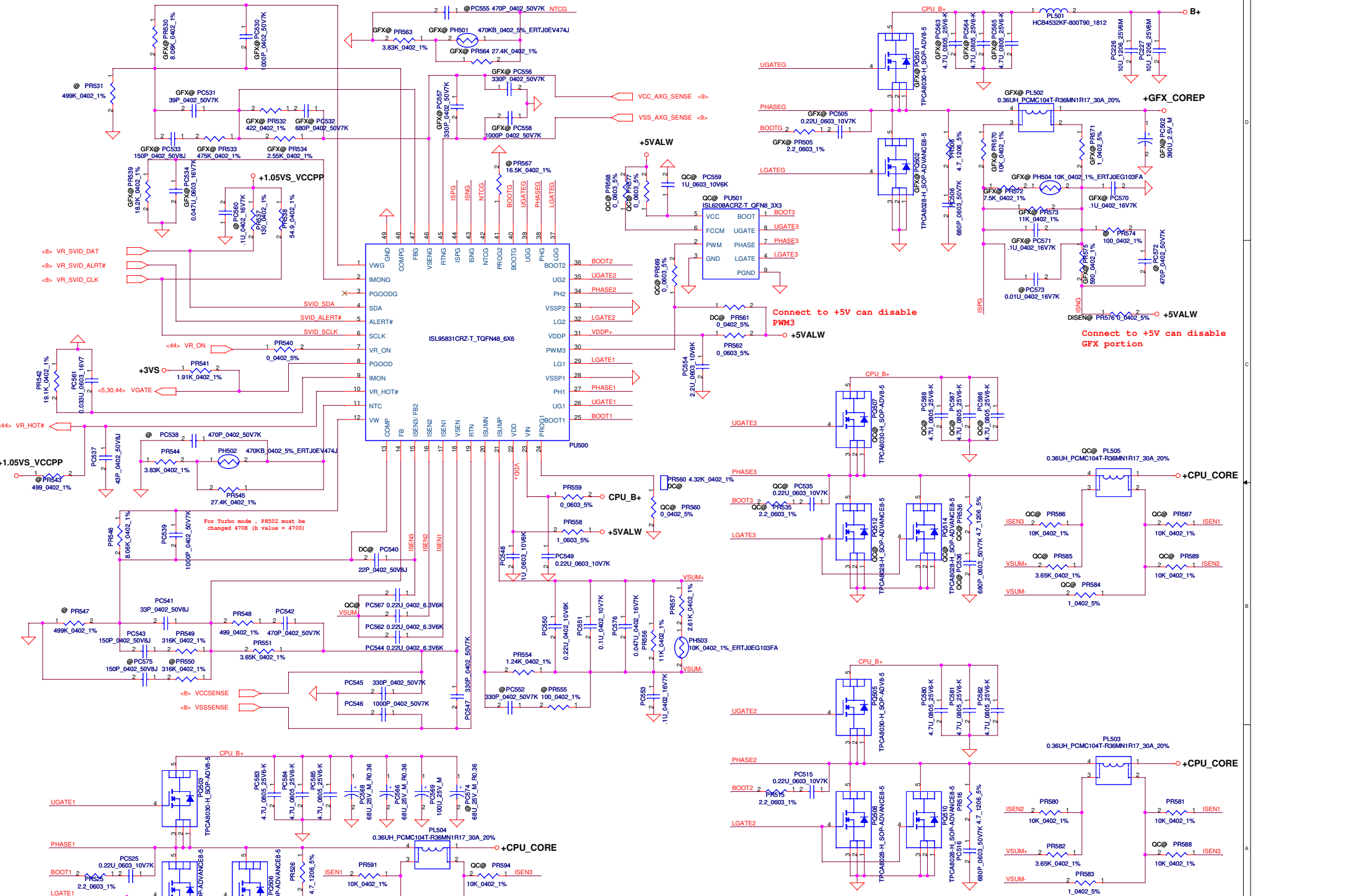
I_{peak}=6A
 I_{max}=4.2A
 F=276K
 Total Capacitor ??u
 ESR=?mohm

VID1	+VCCSAP
1	0.8V
0	0.9V



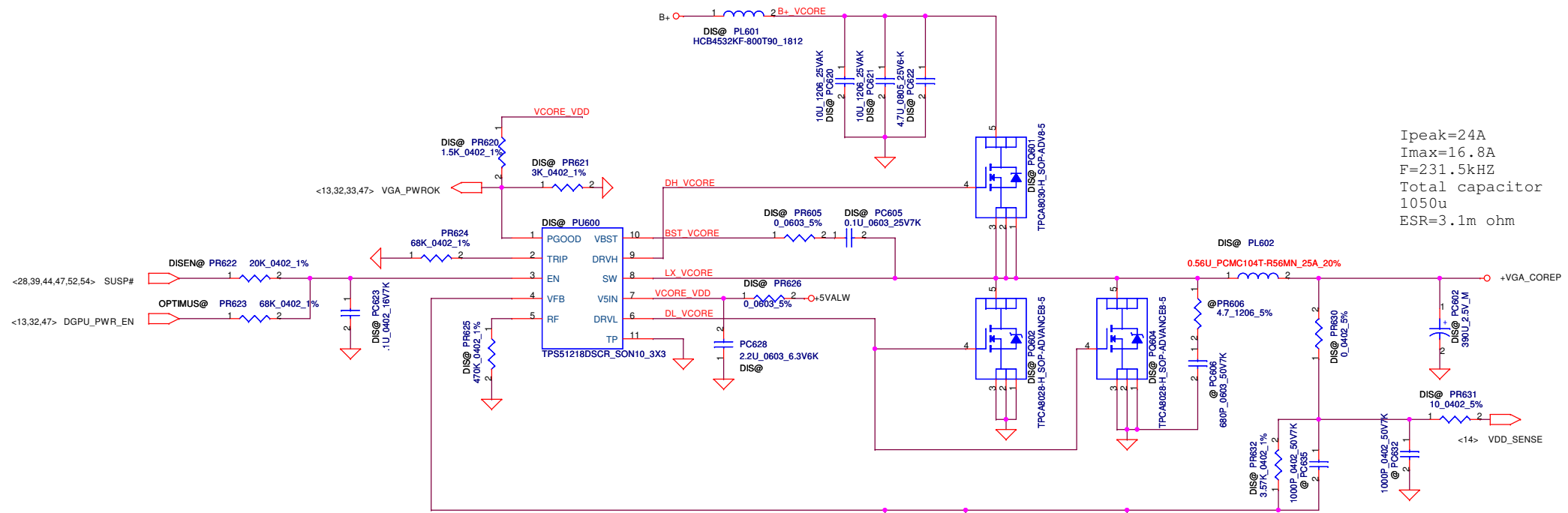
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				+1.05VS_VCCPP/+0.75VSP	
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Compal Electronics, Inc.	
CPU_CORE/GFX	
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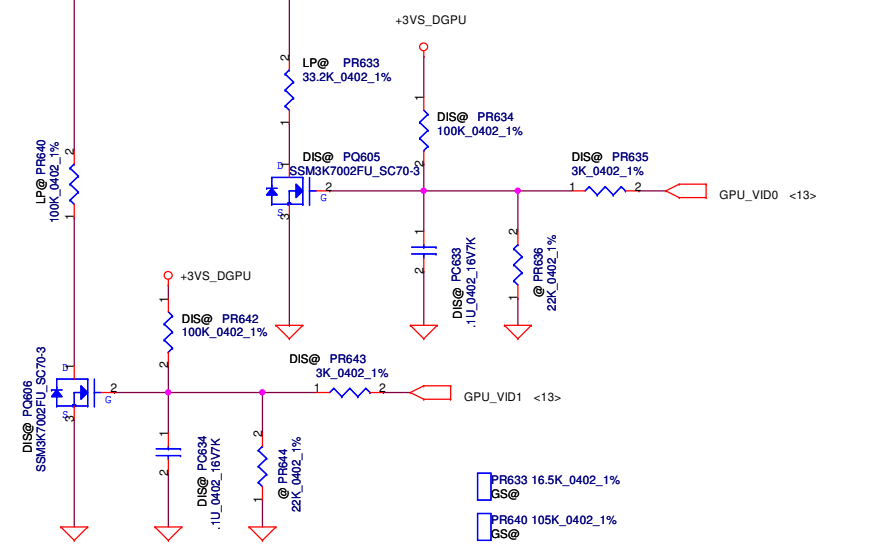
Ipeak=24A
 Imax=16.8A
 F=231.5kHz
 Total capacitor
 1050u
 ESR=3.1m ohm

$FWS=1/(75E-12*57.6K)=231.48KHz$

N12P-GV	N12P-GE	N12P-GS
Imax=16.09A Ipeak=18.19A Iocp=20.72A	Imax=16.8A Ipeak=24A Iocp=29.17A	Imax=16.8A Ipeak=24A Iocp=32.14A
PR607=7.15K PQ604=unpop	PR607=7.15K PQ604=unpop	PR607=7.15K PQ604=unpop

$VFB(0.6)=Vout*Rbottom/(Rtop+Rbottom)$

Pstate	GPU_VID0	GPU_VID1	N12P-GV	N12P-LP	N12P-GS
P8/P12	0	0		0.825V	0.825V
P0 (hot)	1	0		0.9V	0.975V
	0	1			
P0 (cold)	1	1		0.925V	1V
			PR632=7.5K PR641=20K PR633=59K PR640=88.7K	PR632=7.5K PR641=20K PR633=59K PR640=88.7K	



PR633 16.5K_0402_1%
 GS@
 PR640 105K_0402_1%
 GS@

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HW PIR (Product Improve Record)

PHQAA LA-6831P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2010/09/03

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P08.	Sandy Bridge_POWER-1 Remove C126, C131 and add C894 3Pin Bulk Cap Change C890, C891, C894 from SGA00005R00 (S POLY C 330U 2V M D2 LESR6M LX H1.9) to SGA00004X80 (S POLY C 470U 2V M D2 LESR4.5M LX H1.9) by Power demand.	By Power Transient test demand. By Power Transient test demand.
EVT		P13.	VGA_PCIE/DAC/GPIO Change RV8, RV9 to @ due to use internal thermal sensor.	Remove External Thermal and implement NV Internal Thermal sensor.
EVT		P14.	VGA_LVDS/HDMI/THERM/eDP Change External Thermal sensor UV2, CV53, CV54 to @. Change RV33, RV34 to always mount.	Remove External Thermal and implement NV Internal Thermal sensor. Remove External Thermal and implement NV Internal Thermal sensor.
EVT		P16.	VGA_POWER Change External Thermal sensor UV2, CV53, CV54 to @. Change RV33, RV34 to always mount.	Remove External Thermal and implement NV Internal Thermal sensor. Remove External Thermal and implement NV Internal Thermal sensor.
EVT		P28.	PCH_HDA/JTAG/SATA/SPI/LPC Change PWRME_CTRL# from PCH_GPIO33 to HDA_SDO. Remove R274. Change R442, R443 from 10k to 100k. Change U56 Pin3 from KSO6 to +5VALW. Add R227 100k ohm. Change U53 pin9 from KSI4 to KSI3. Change U13 from SA000021A00 to SA00003IN00.	Follow Intel Strap Pin Design Guide. Due to PCH GPIO33 no use. Modify SPI Debug Circuit. Due to EOL of SA000021A00
EVT		P29.	PCH_PCI-E/SMBUS/CLK Remover NEW Card Function: Remove PCIE interface.	A51 changed PRD Spec: remove New Card function
EVT		P30.	PCH_DMI/FDI/PM Reserve R259.	Cost down Plan
EVT		P32.	PCH_PCI/USB/NAND Remover NEW Card Function: Remove EXP_CPPE#	A51 changed PRD Spec: remove New Card function
EVT		P33.	PCH_CPU/GPIO Remove T73. Add USB Sleep & Charge MAXIC_Select pin in GPIO71.	Add USB Sleep & Charge IC detect function Add USB Sleep & Charge IC detect function
EVT		P37.	SATA-HDD/ODD/USB Change C426 to Aluminum Solid Cap 220uF	Cost Down Plan.
EVT		P39.	PCIE-WLAN/JET/3G/TV/S&C Remover NEW Card Function. Add USB Sleep & Charge IC: MAX14550E. Add 14566@ & 14550@. Change U5 Pin8 control pin from SLP_CHG# to SLP_CHG_M4. Reserve R1443 for WLAN Mini PCIE Card Pin5.	A51 changed PRD Spec: remove New Card function Add USB Sleep & Charge IC MAX14550E Set BOM Structure for MAX14550E & MAX14566B The conclusion of discussion with Sw Reserve for Broadcom combo card with BT
EVT		P40.	PCIE-LAN-RTL8105E/8111E Change 8105E-LDO@ to 8105ELDO@. Change 8105E-SWR@ to 8105ESWR@. Reserve DL1, D12 for ISN test by EMI demand. Add LL5 for ISN test by EMI demand. Add 16pin Xform for cost down, and P/N is SP050006E00	Avoid ISPD BOM Error Reserve for ISN Test by EMI demand Cost Down Plan
EVT		P41.	PCIE-CardReader JMB389 Change JMB389@ to always mount.	Reduce BOM Config
EVT		P42.	PCIE-USB3.0 UPD720200A Change USB3.0 Connector Swap LT1 Add net name: SPI_CLK_USB_R.	ME demand. Layout demand. Layout demand.
EVT		P43.	HDA-ALC269/HP/MIC Change RA12 from 10k to 4.7kohm for Beep Change CA18 from 0.1uF tp 100pF for Beep	Let PC Beep to be clearer
EVT		P44.	LPC-EC-KB930 Add CPSETIN function in EC_GPIO15.	Add it to detect QC/DC by Power demand.
EVT		P45.	SPI ROM/LID/Debug/KB/G-Sen Change EC ROM size from 256KB(SA00003GM10) to 128KB(SA00003FL10).	EC Cost down plan.
EVT		P46.	PWR/Cap./TP/LED/LP/LS/Screw Change SW1, SW4 to SN100002Y00.	

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1.	2010/08/12	P54-PWR+1.05VS_VCCP/+0.75VSP	Change PU75 from UP7711 to G2992	Change source
2.	2010/08/12	P55-PWR-CPU_CORE/GFX	Change PU501 to SA000010200	Use Compal part number
3.	2010/08/12	P51-PWR_3VALWP/5VALWP	Change PU330 from UP6182CQAG to TPS51125A	Change source
4.	2010/08/12	P52-PWR+1.5VP/+1.8VSP	Change PU150 from G5603 to RT8209B	Change source
5.	2010/08/12	P53-PWR+VCCSAP	Change PU450 from G5603 to RT8209B	Change source
6.	2010/08/12	P54-PWR+1.05VS_VCCP/+0.75VSP	Change PU400 from G5603 to RT8209B	Change source
7.	2010/08/12	P50-PWR-CHARGER	Change PQ204 from A04435 to A04407	Increase current margin for back to back MOS
8.	2010/08/12	P48-PWR_DCIN/VIN DECTOR	Change PQ1,PQ4 to SB900840003	For shortage issue
9.	2010/08/12	P49-PWR_BATTERY CONN / OTP	Change PQ5 to SB900840003	For shortage issue
10.	2010/08/12	P55-PWR-CPU_CORE/GFX	Add PR544 3.83k,PR545 27.4k,PH502 470k	For CPU NTC function
11.	2010/08/12	P55-PWR-CPU_CORE/GFX	Add PR560 0 Ohm	Set CPU VBOOT to 0V
12.	2010/08/12	P52-PWR+1.5VP/+1.8VSP	Change PR157 10k to 7.5k	For DIS OCP(22.46A)
			Change PR157 10k to 4.7k	For UMA OCP(13.96A)
			Change PR457 10k to 13k	Set OCP(7A)
13.	2010/08/12	P53-PWR+VCCSAP	Change PR407 13.7k to 6.49k	Set OCP(19.23A)
14.	2010/08/12	P54-PWR+1.05VS_VCCP/+0.75VSP	Change PC332, PC352 to 330U	Change source
15.	2010/08/12	P51-PWR_3VALWP/5VALWP	Change PC152 to 330U	Change source
16.	2010/08/12	P52-PWR+1.5VP/+1.8VSP	Change PL182 to SH00000GJ00	For shortage issue
17.	2010/08/12	P52-PWR+1.5VP/+1.8VSP	Add PQ604 TPCA8028	Add 1 low side MOS for VGA_CORE
18.	2010/08/12	P56-PWR_VGA_COREP	Add PR607 3.9k to 4.7k	set OCO to 39.62A
19.	2010/08/12	P56-PWR_VGA_COREP	Add PR622 20k	For non OPTIMUS enable
20.	2010/08/12	P56-PWR_VGA_COREP	Add PR576 0 Ohm	For disable GFX_CORE
21.	2010/08/12	P55-PWR-CPU_CORE/GFX	Change PU200 to ISL6251	Change source
22.	2010/09/08	P50-PWR-CHARGER	Change PU150 to G5603	Change source
23.	2010/09/08	P52-PWR+1.5VP/+1.8VSP	Change PU450 to G5603	Change source
24.	2010/09/08	P53-PWR+VCCSAP	Change PU400 to G5603	Change source
25.	2010/09/08	P54-PWR+1.05VS_VCCP/+0.75VSP	Change OQ454 to MMS13904	Use low Vth transistor
26.	2010/09/08	P53-PWR+VCCSAP	Add PQ217 2N7002W,PR249 10k	For precharge function
27.	2010/09/08	P50-PWR-CHARGER	Add PQ218 2N7002W,PR234 12.4k	For DC,QC CP setting
28.	2010/09/08	P50-PWR-CHARGER	Change PQ452 to A04712L	Use same part number
29.	2010/09/08	P53-PWR+VCCSAP	Change PQ452 to A04712L	Use same part number
30.	2010/09/08	P53-PWR+VCCSAP	Change PQ451 to A04466L	Use same part number
31.	2010/09/08	P53-PWR+VCCSAP	Change PQ201,PQ202 to A04466L	Use same part number
32.	2010/09/08	P50-PWR-CHARGER	Change PQ201,PQ202 to A04466L	Use same part number
33.	2010/09/08	P50-PWR-CHARGER	Change PQ203,PQ207 to A04435L	Change source
34.	2010/09/08	P50-PWR-CHARGER	Add PD5,PD6	For EMI request
35.	2010/09/08	P49-PWR_BATTERY CONN / OTP	Change PR215 current sensor to 2512 size	Add current current sensor rating
36.	2010/09/08	P50-PWR-CHARGER	Change PR551 from 3.83k to 3.65k	For CPU_CORE load line
37.	2010/09/08	P55-PWR-CPU_CORE/GFX	Add PR17 1k	For precharge function
38.	2010/09/08	P48-PWR_DCIN/VIN DECTOR	Add 4.7 Ohm and 680pF	Add snubber
39.	2010/09/08	Many page	Add 2.2 Ohm	Add booster
40.	2010/09/08	Many page	Change PR181 0 to 150k,add PC185 0.1u	For VGA sequence
41.	2010/09/08	P52-PWR+1.5VP/+1.8VSP	Change Pr420 0 ohm to 0402 size	Cost down
42.	2010/09/08	P53-PWR+VCCSAP	Change Pr410 0 ohm to 150k,add PC410 0.1u	For VGA sequence
43.	2010/09/08	P53-PWR+VCCSAP	Change Pr463 0 ohm to 0402 size	Cost down
44.	2010/09/08	P54-PWR+1.05VS_VCCP/+0.75VSP	Add PR29 100k,PR22 1.02k,PR27 4.99k,PR28 4.53k	For adapter protect function
45.	2010/09/08	P49-PWR_BATTERY CONN / OTP	Change PR151 4.7k to 7.5k	For UMA 1.5V OCP
46.	2010/09/08	P52-PWR+1.5VP/+1.8VSP	Add 10u 1206	For EMI ISN request
47.	2010/09/08	Many page	Add PL201	For EMI ISN request
48.	2010/09/08	P50-PWR-CHARGER	Change VGA IC solution(many component)	For cost down
49.	2010/09/08	P50-PWR-CHARGER	Change PR455 2.2 to 0	remove booster
50.	2010/09/08	P53-PWR+VCCSAP		

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