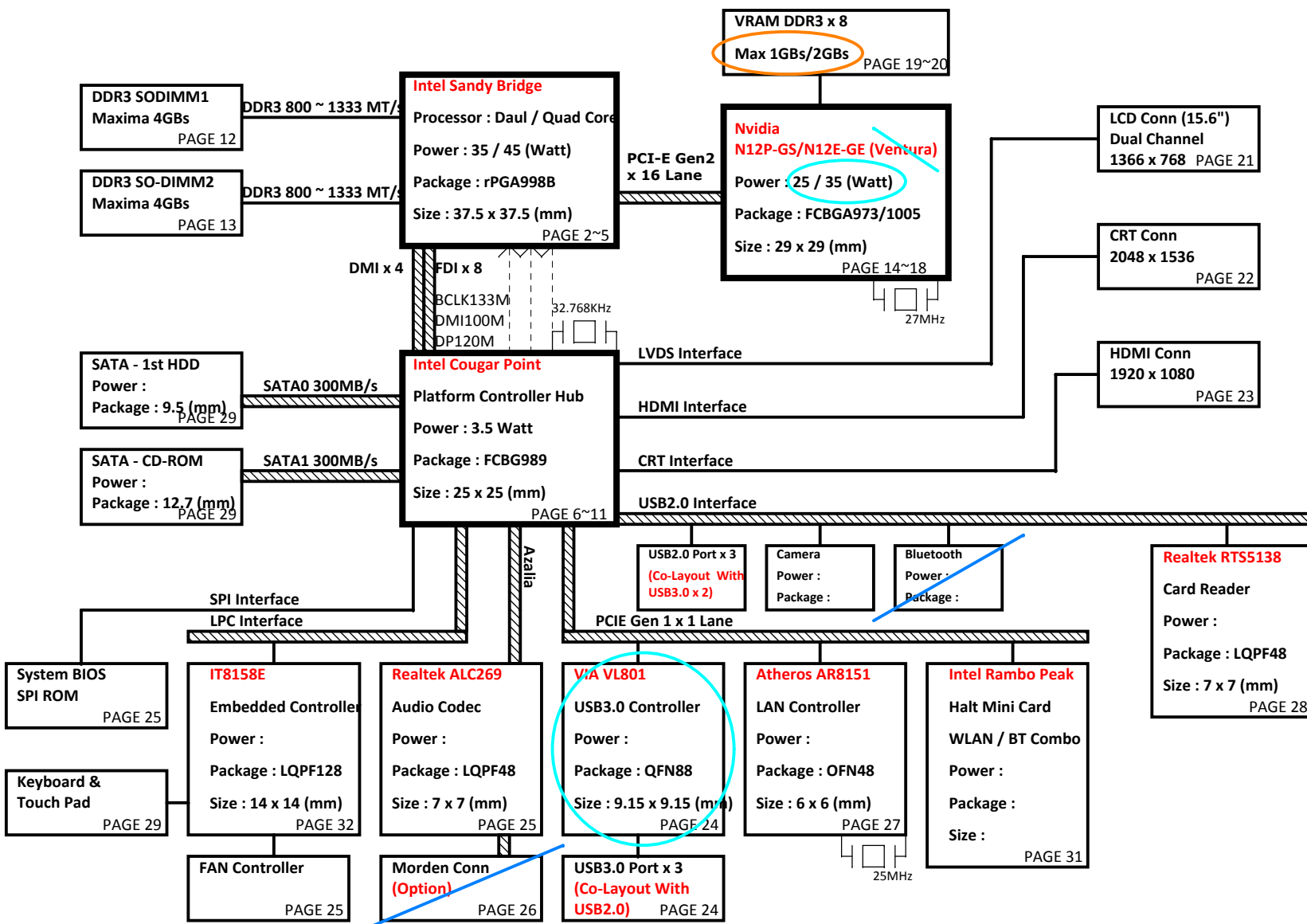


TWH (15.6") Intel Huron River Platform Block Diagram 01

https://t.me/biosarchive

https://t.me/biosarchive

https://t.me/biosarchive



PCB 6L STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1(High)
- LAYER 4 : IN2(Low)
- LAYER 5 : SVCC
- LAYER 6 : BOT

PCB 8L STACK UP

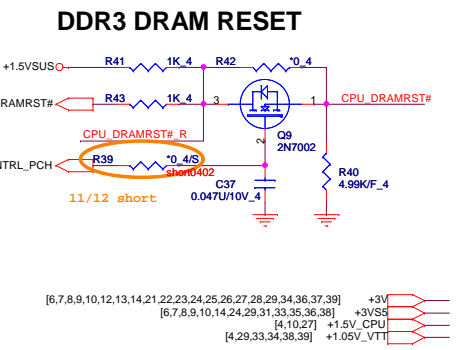
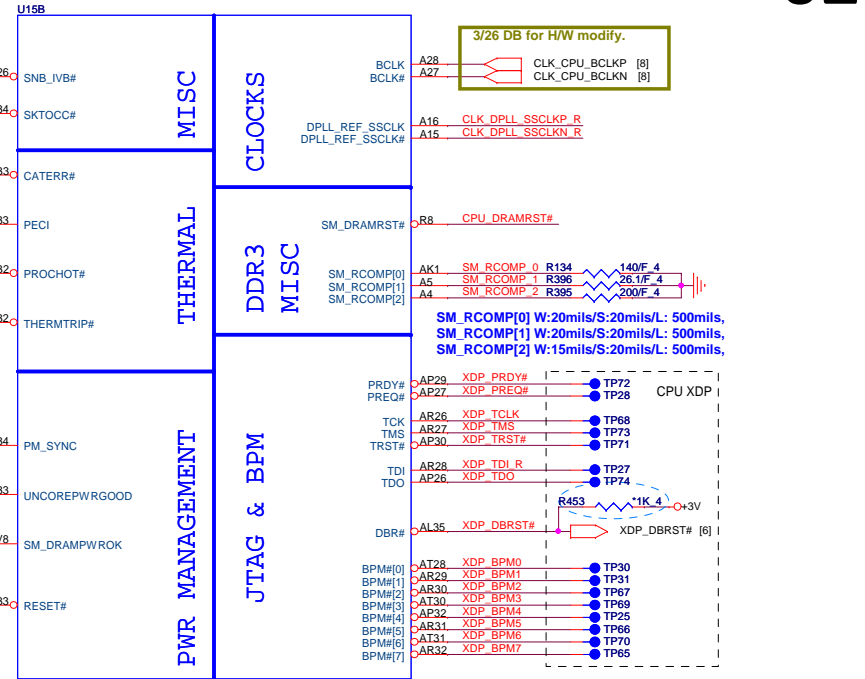
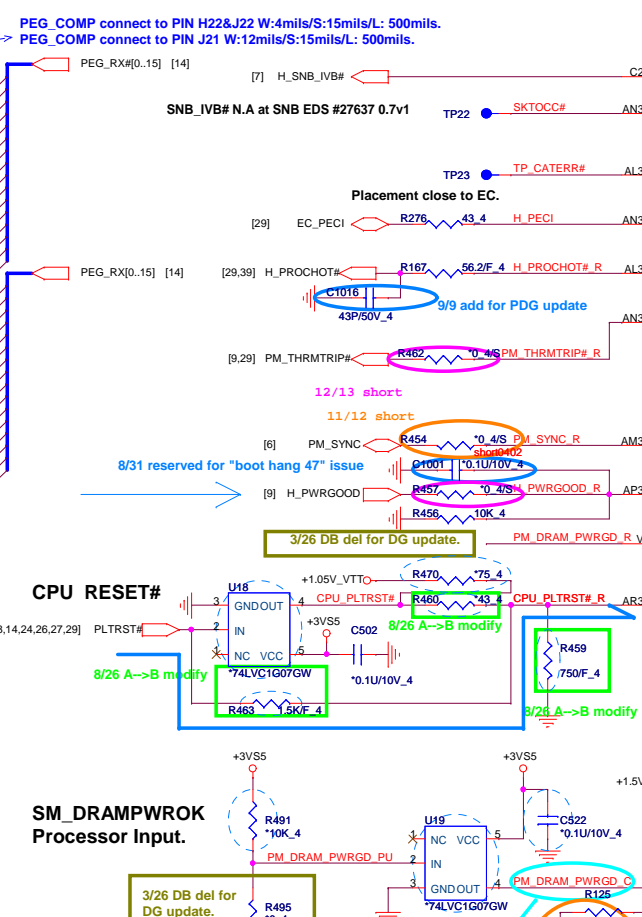
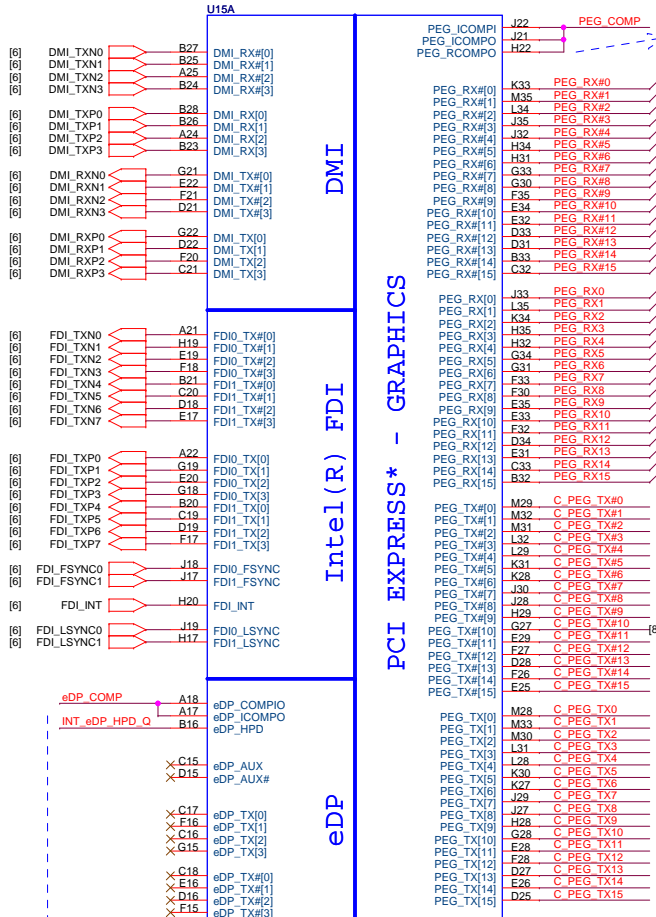
- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1(High)
- LAYER 4 : IN2(Low)
- LAYER 5 : SGND1
- LAYER 6 : SVCC
- LAYER 7 : SGND2
- LAYER 8 : BOT

Power Source

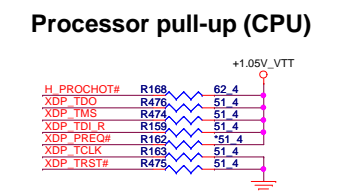
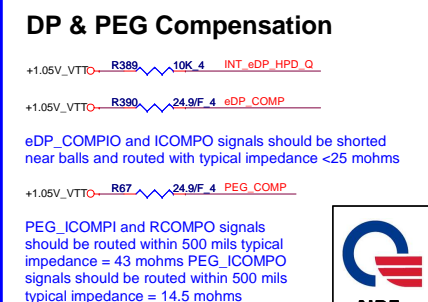
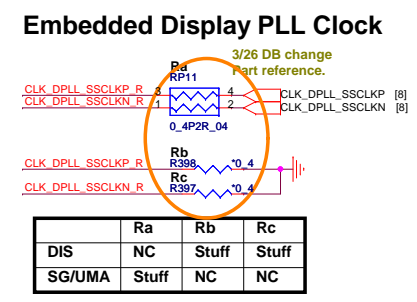
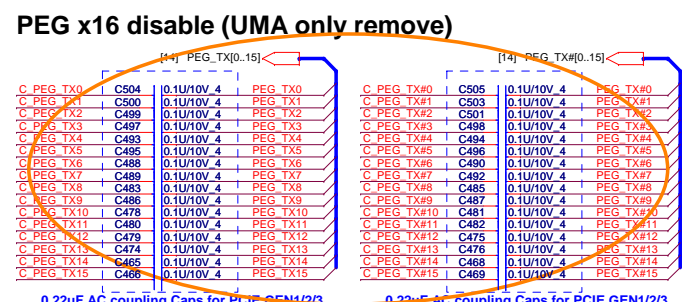
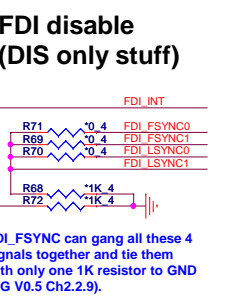
- O2Micro OZ8681**
System Charge Power (+BATCHG)
- P2806**
System Discharge Power (+1.5V/+3V/+5V)
- Richtek RT8205**
System Power (+3VPCU/+5VPCU/+3VSS/+5VSS)
- NCP6131/NCP5911/RT8209/G9334**
Processor Power (+VCC_CORE/+1.05_VTT/+VCCSA)
- Richtek RT8207**
System Memory Power (+1.5VSUS/+0.75V_DDR_VTT)
- Richtek RT8209/RT9025**
PCH Power (+1.05/+1.8V)
- O2Micro OZ8122**
DGPU Power (+VGACORE/+3.3V_GFX/+1.8_VGA/+1.5_GFX/+1.05_GFX)

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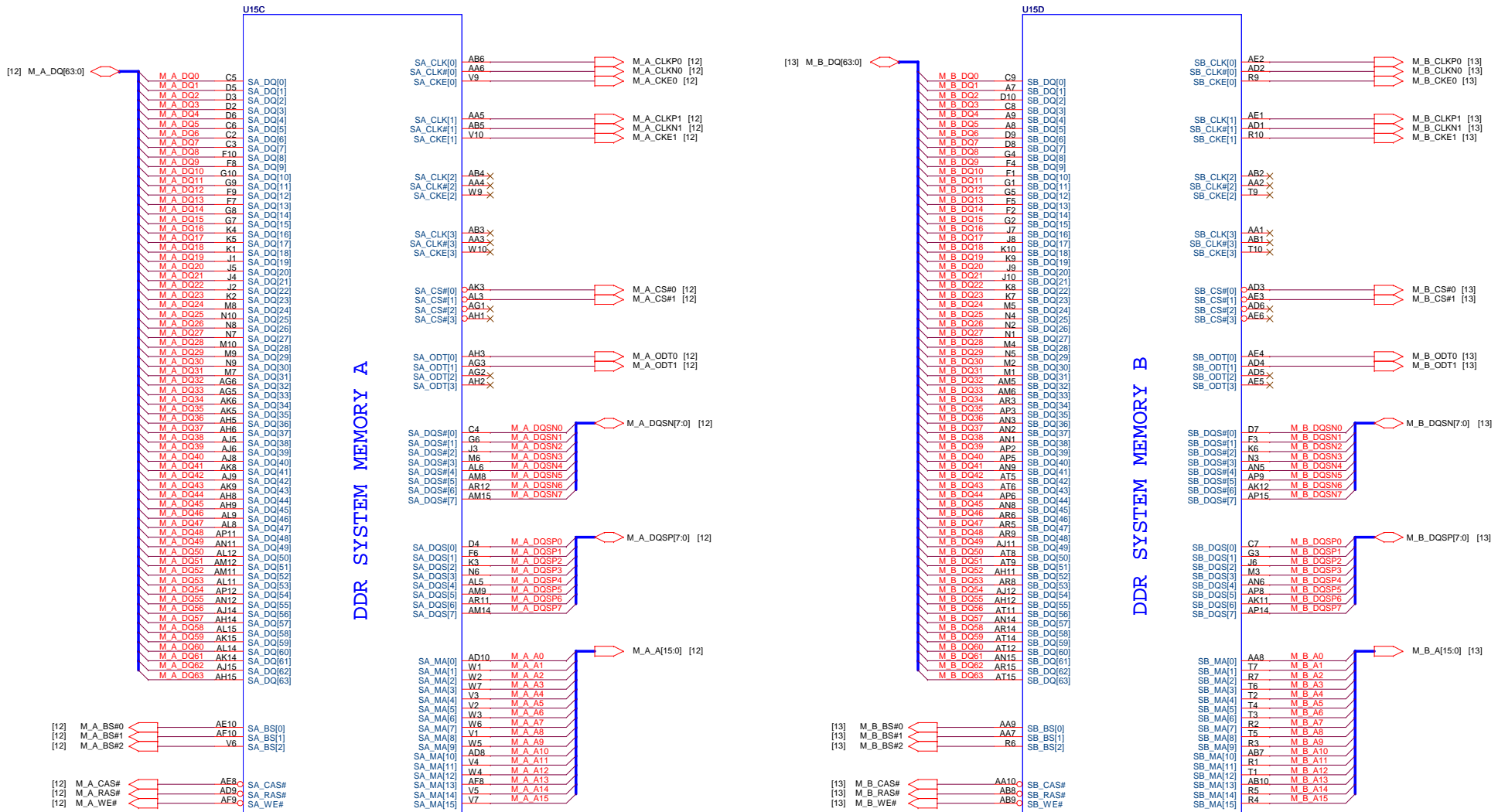
	PROJECT : TWH		Rev A
	Quanta Computer Inc.		
Size A3	Document Number Block Diagram		
Date: Tuesday, December 14, 2010	Sheet 1 of 40		



eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
 eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.



Sandy Bridge Processor (DDR3)



Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG#9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge_rPGA_Rev0p61
 rpg989-47989-socket
 DGG#9000014
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

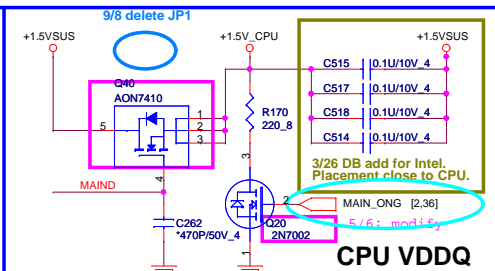
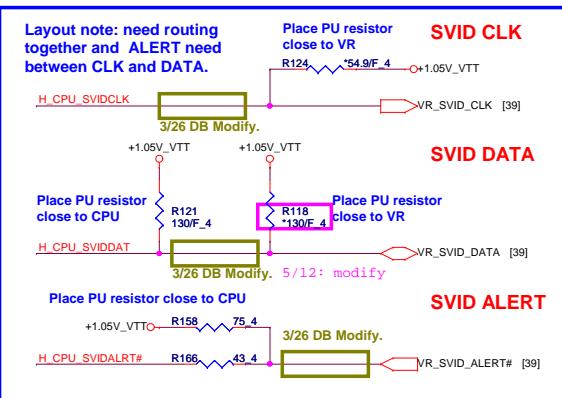
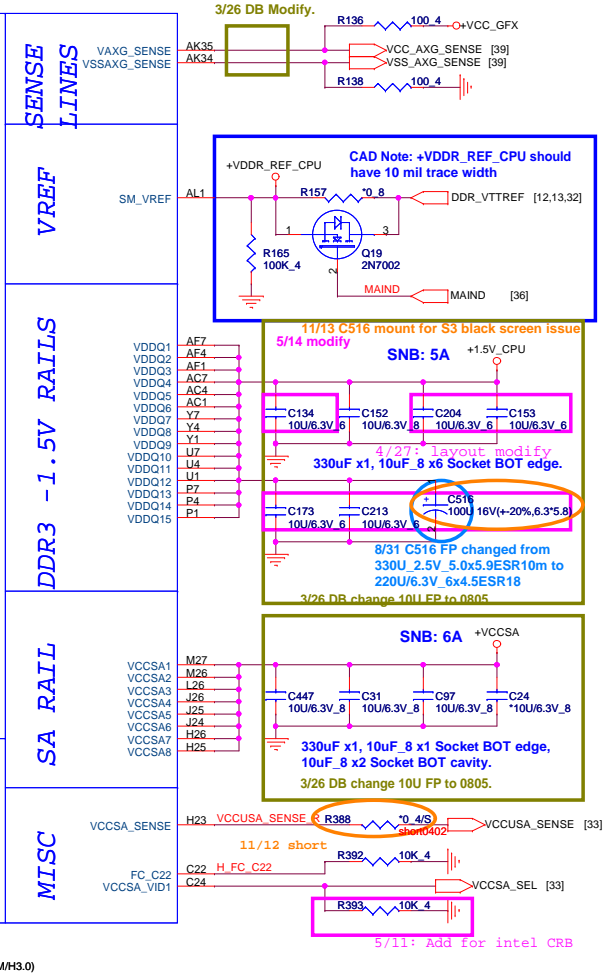
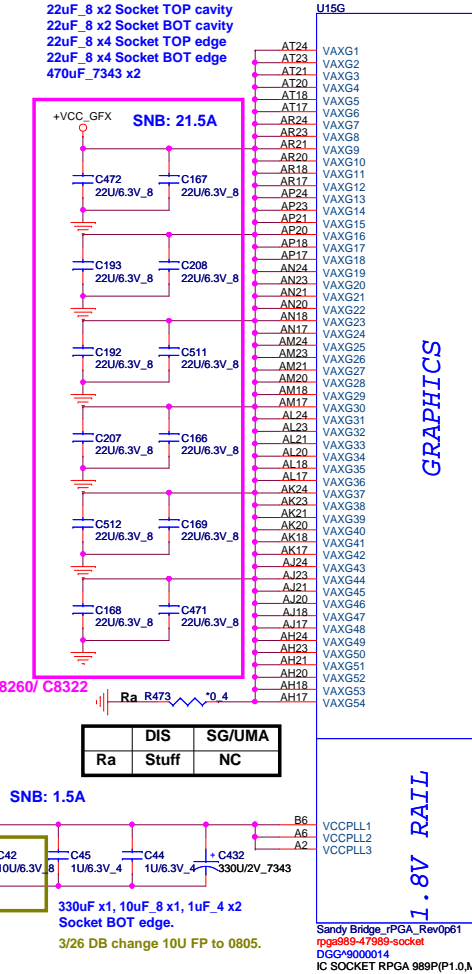
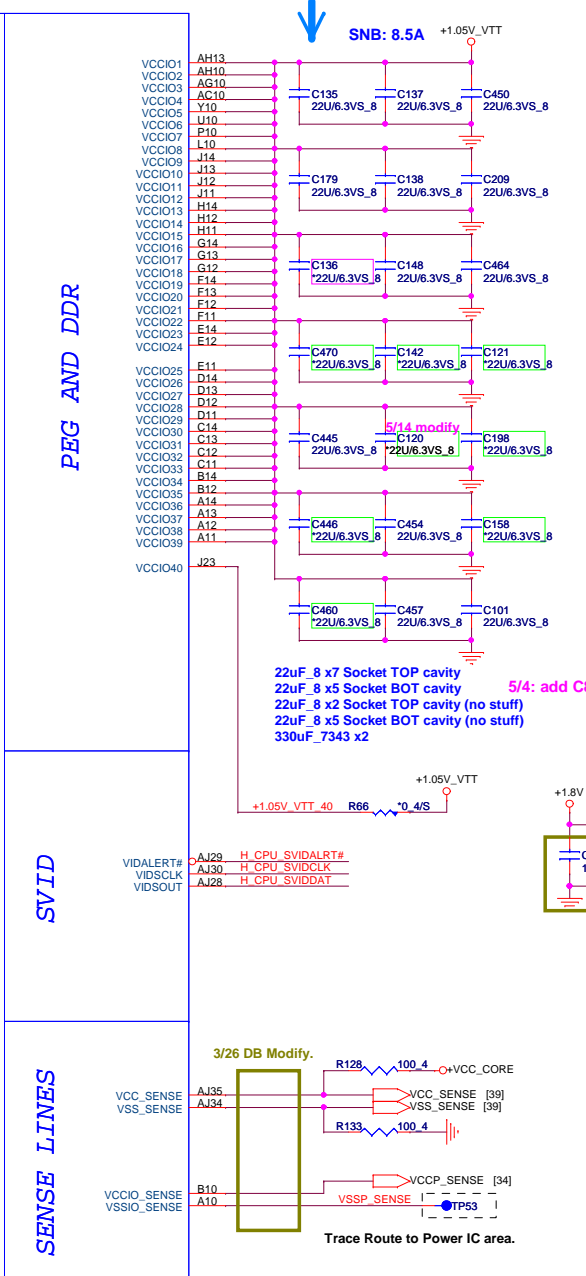
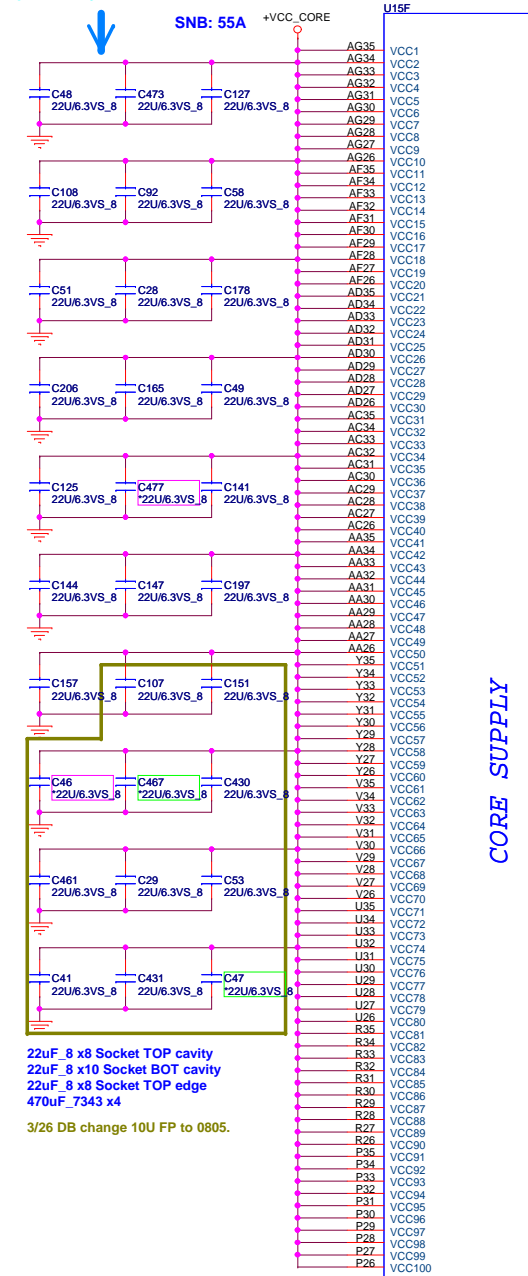
	PROJECT : TWH Quanta Computer Inc.		Rev A
	Size Custom	Document Number Processor 2/4 (Memory)	
Date: Tuesday, December 14, 2010		Sheet 3 of 40	

Sandy Bridge Processor (POWER)

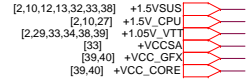
Sandy Bridge Processor (GRAPHIC POWER)

9/4 all of these 22uF/6.3V capacitors are replaced by 10uF/6.3V in BOM

9/4 all of these 22uF/6.3V capacitors are replaced by 10uF/6.3V in BOM



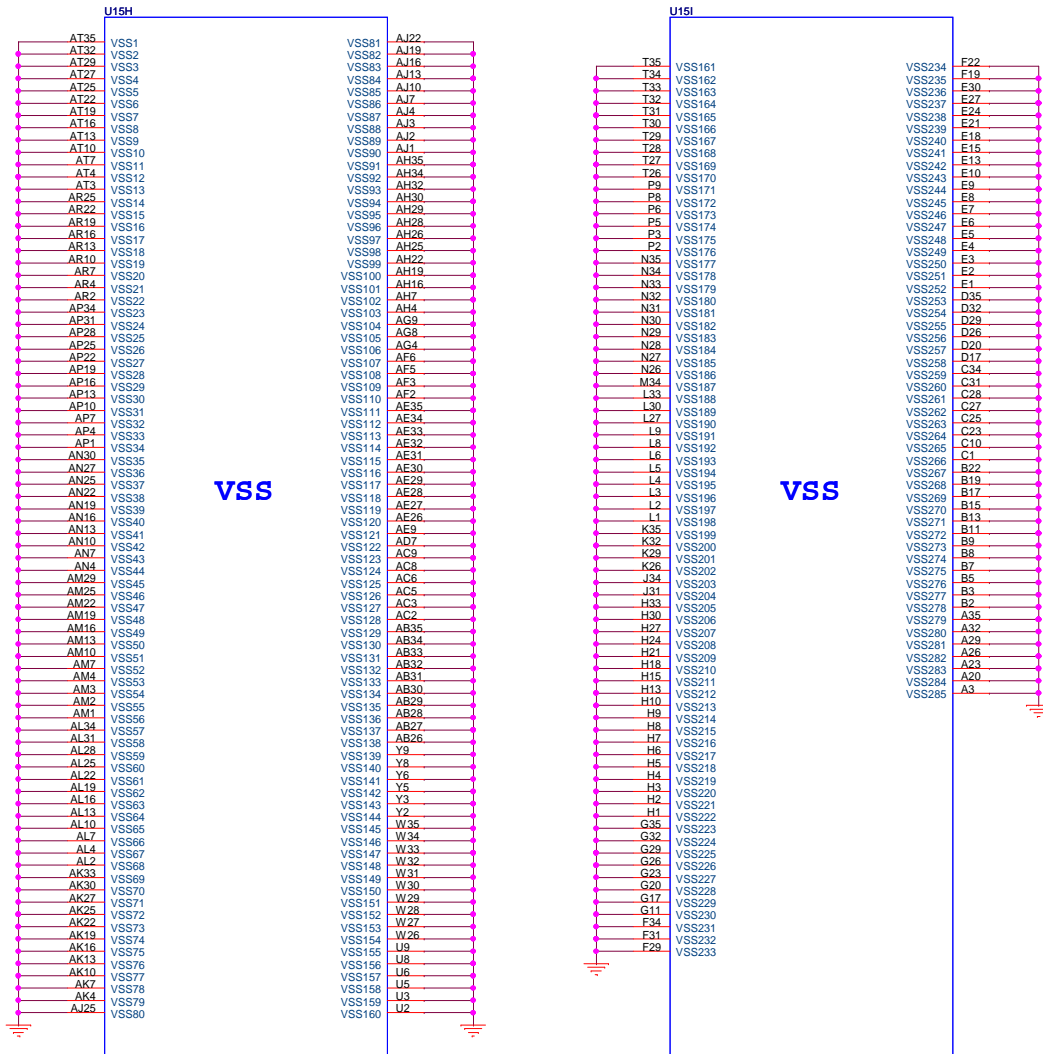
Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)



PROJECT : TWH
Quanta Computer Inc.

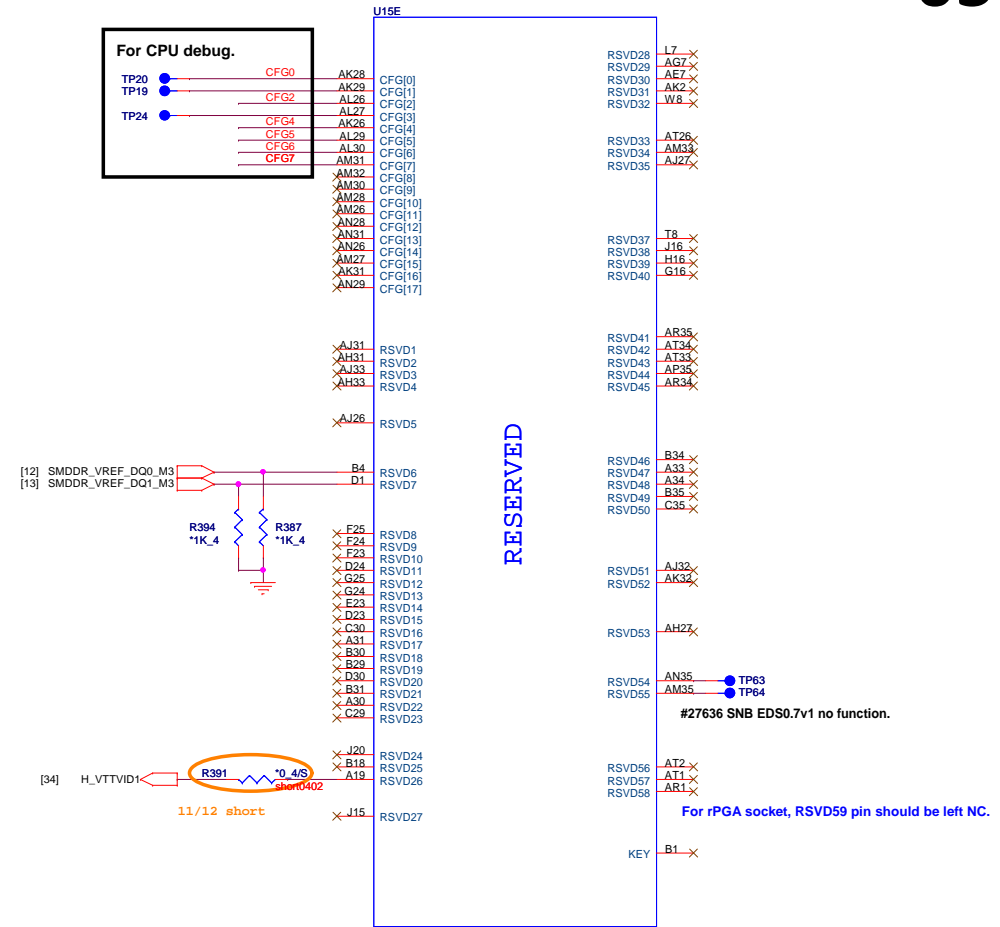
Size	Document Number	Rev
Custom	Processor 3/4 (Power)	A

Date: Tuesday, December 14, 2010 Sheet 4 of 40



Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)

Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)



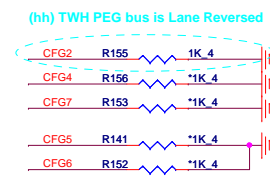
Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG*9000014
IC SOCKET RPGA 989P(P1.0,MH3.0)

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

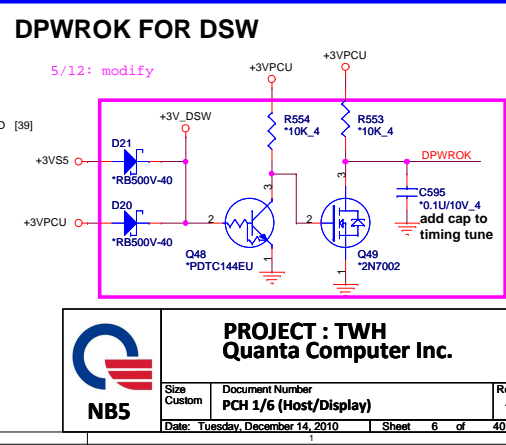
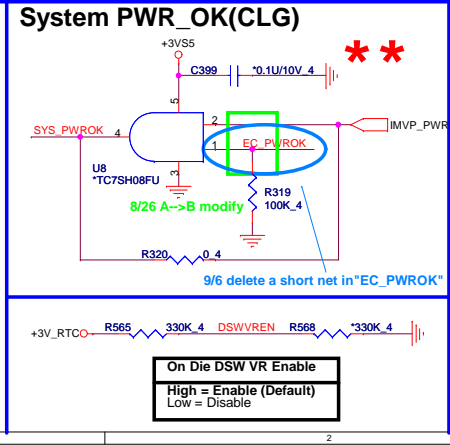
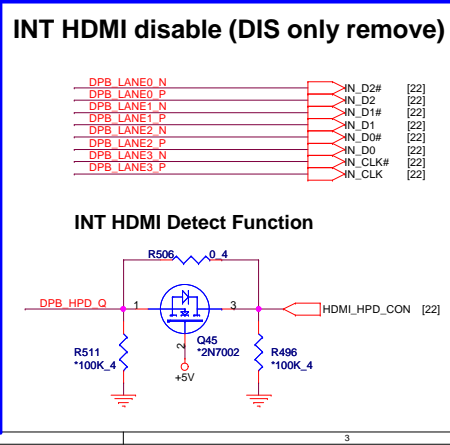
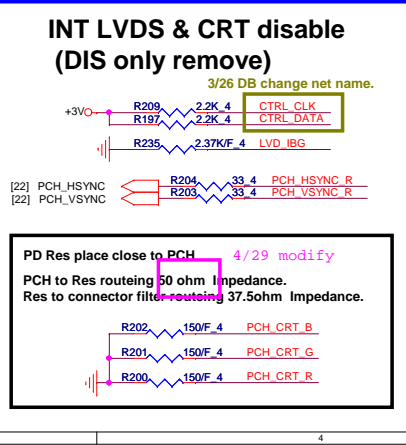
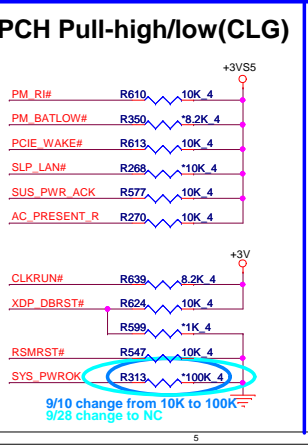
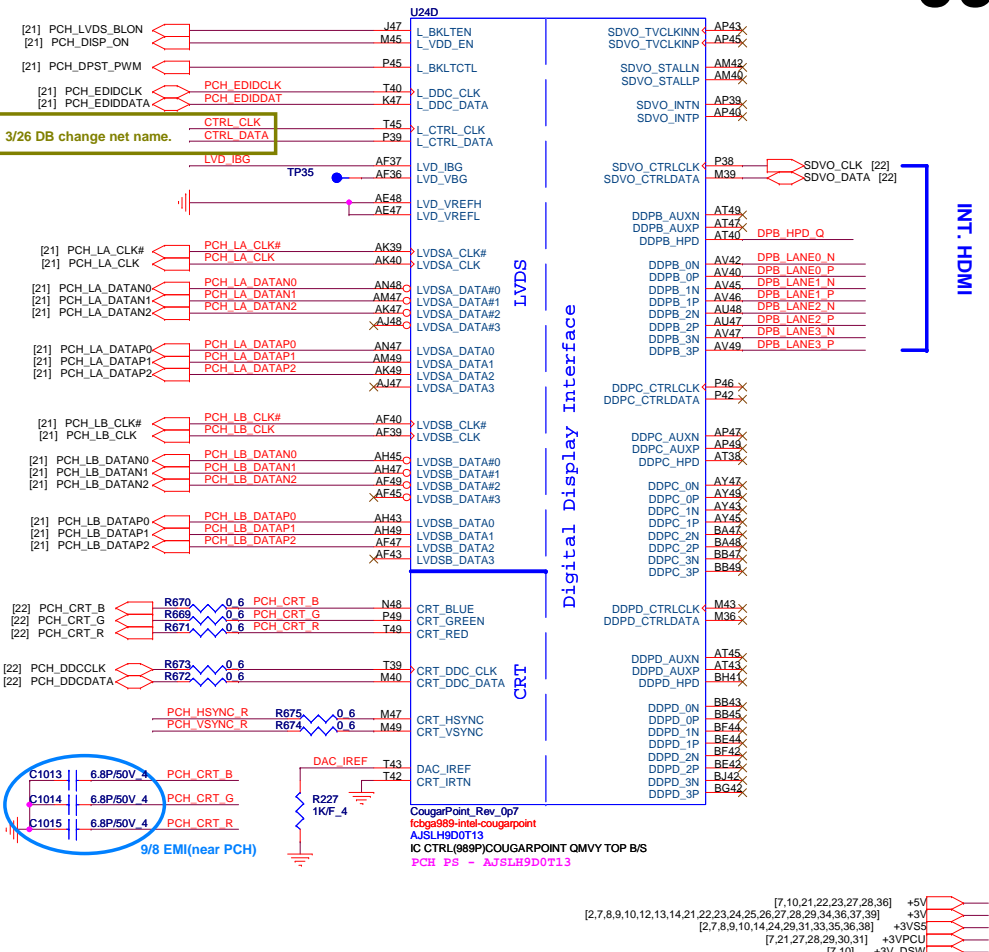
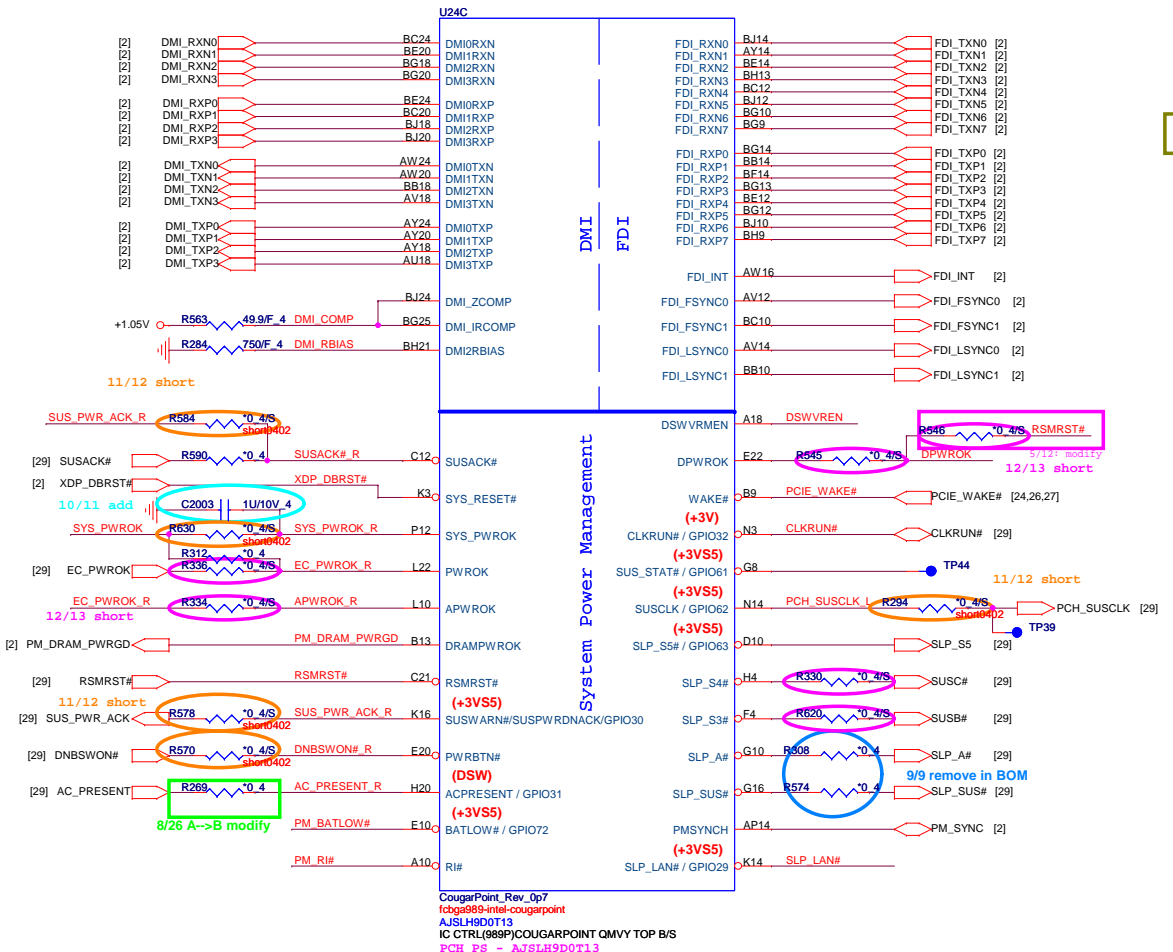
CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



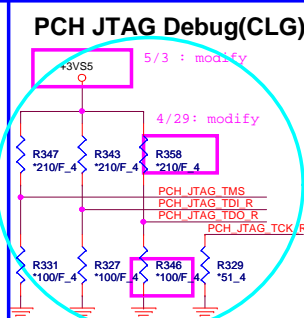
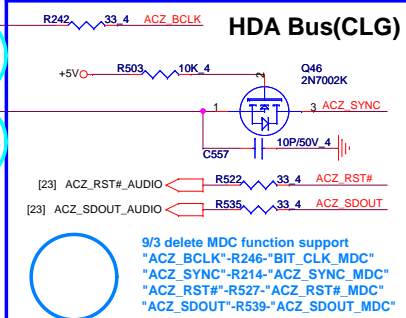
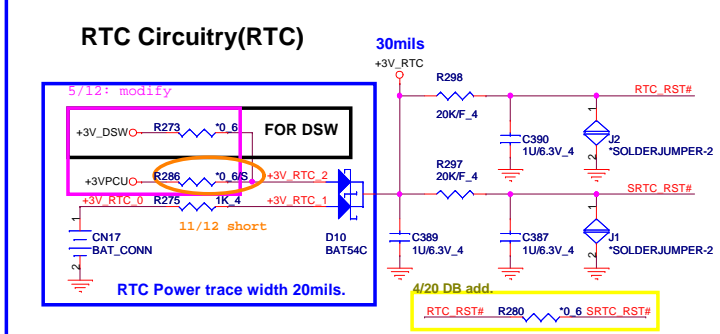
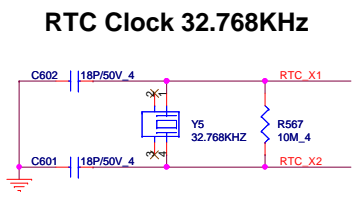
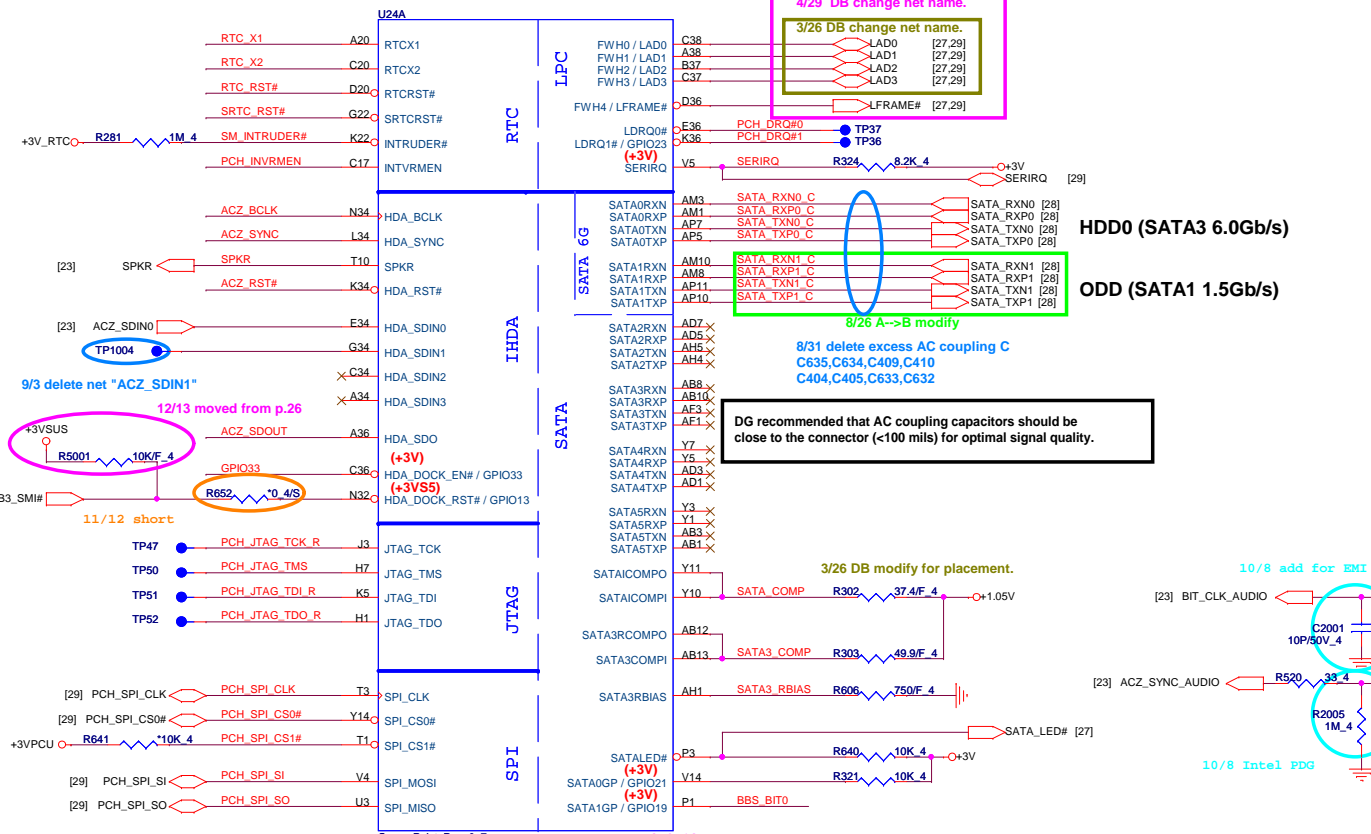
PROJECT : TWH
Quanta Computer Inc.

Size Custom Document Number
Processor 4/4 (Ground)

Date: Tuesday, December 14, 2010 Sheet 5 of 40



Cougar Point (HDA, JTAG, SATA)

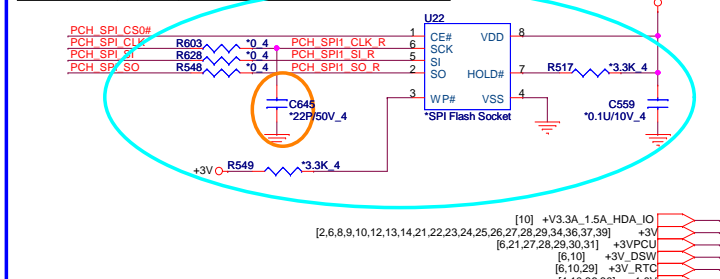


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R636 *1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R518 *1K 4 R514 *10K 4 +3V PCH_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R566 *330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R540 *1K 4 8/26 A-->B modify GPIO33_E [29]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R602 *1K 4 R513 *1K 4 BBS_BIT0 BBS_BIT1 [8]
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R608 *1K 4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm 4/29 modify	+1.8V R616 *2.2K 4 R607 *4.7K 4 NV_CLE [8] N.A at CPT EDS 0.7 H_SNB_IVB# [2]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V5 R215 *1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K) 8/26 A-->B modify	GPIO33_E R544 *1K 4 ACZ_SDOUT R544 *1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R811 *1K 4 4/29 reserve. ICC_EN# [9]
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R817 *1K 4 PLL_OVDR_EN [9]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R604 *1K 4 +3V

Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

11/13 remove all R (Intel confirmed)



PROJECT : TWH
Quanta Computer Inc.

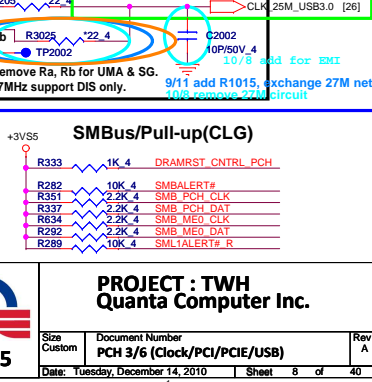
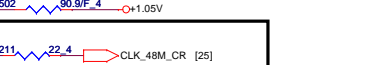
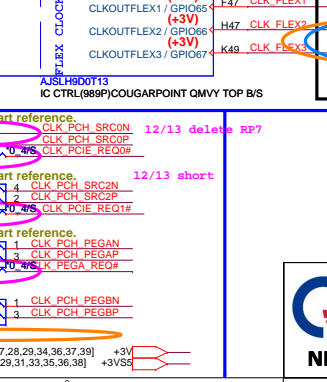
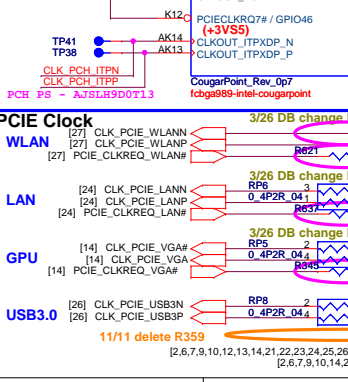
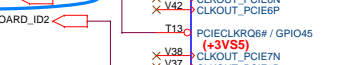
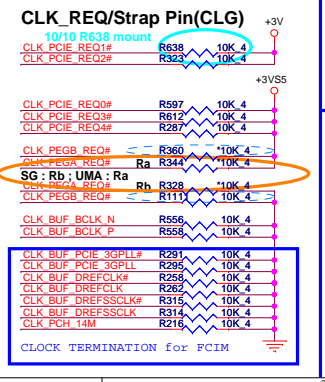
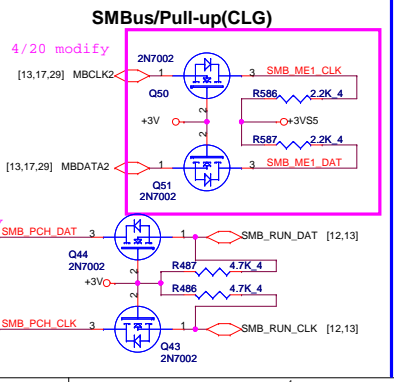
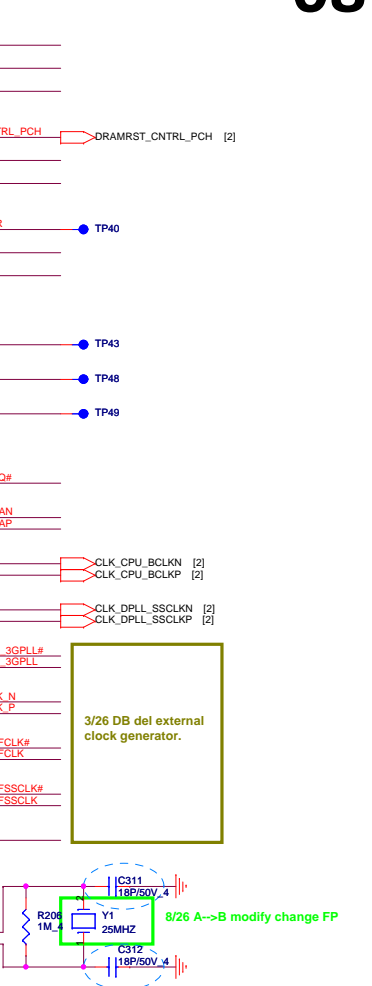
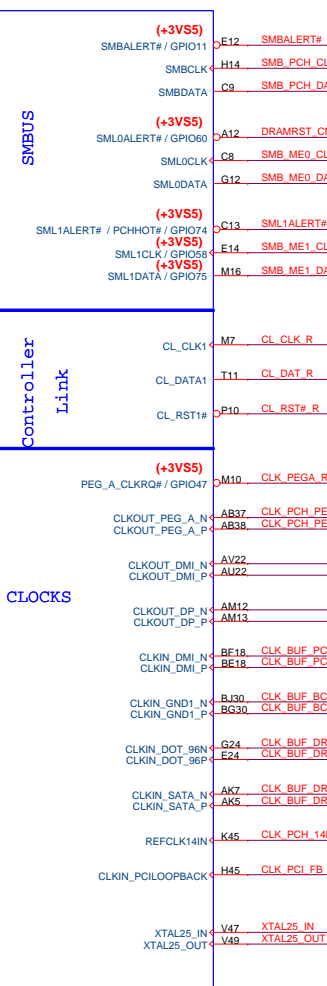
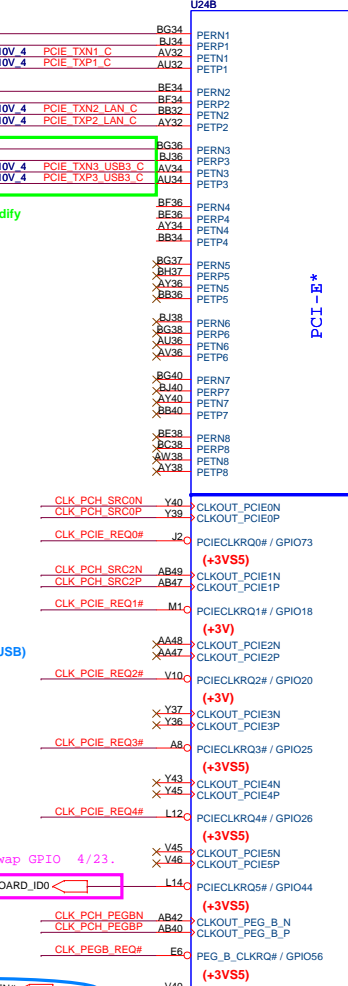
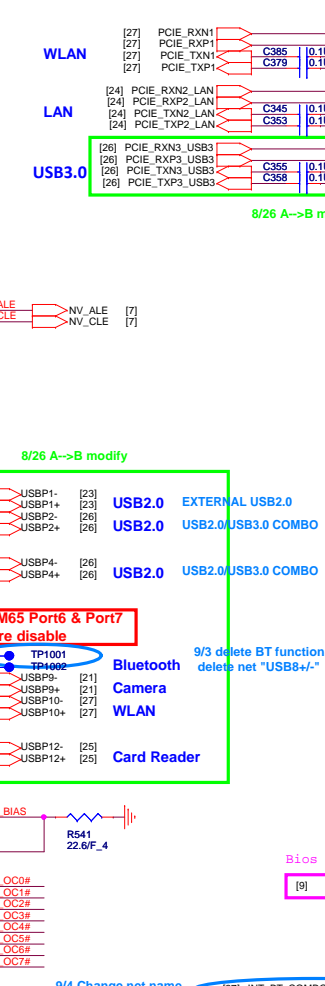
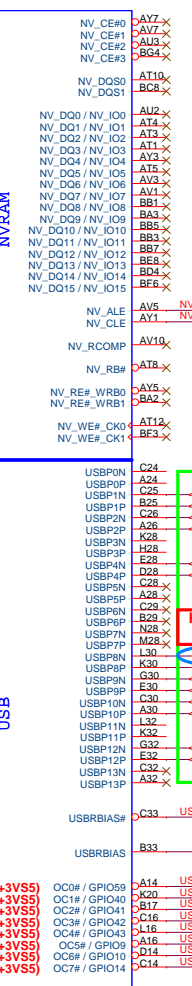
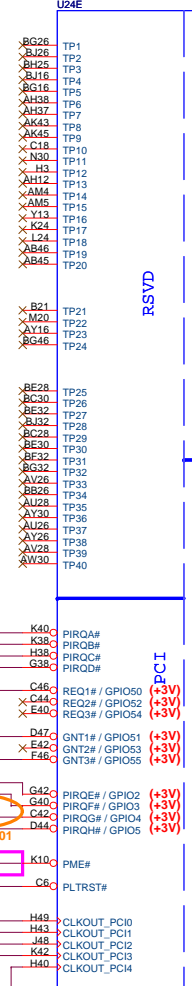
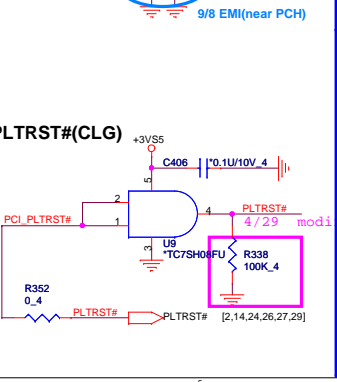
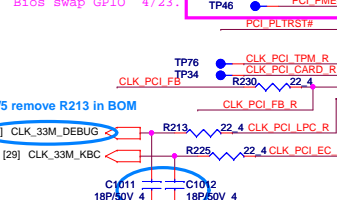
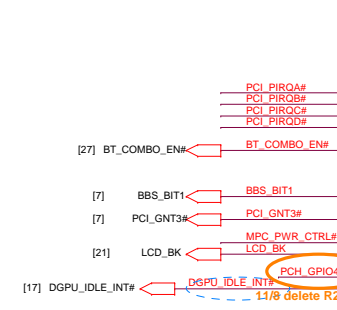
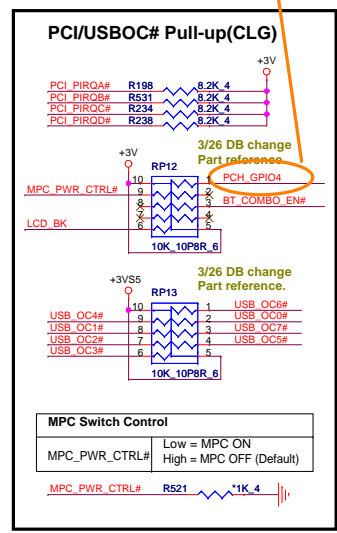
NBS

Size Custom Document Number PCH 2/6 (HDA/RTC/SATA/SPI) Rev A
 Date: Wednesday, December 15, 2010 Sheet 7 of 40

11/8 change net name to "PCH_GPIO4" delete "DGPU_IDLE_INT#" pull-hi

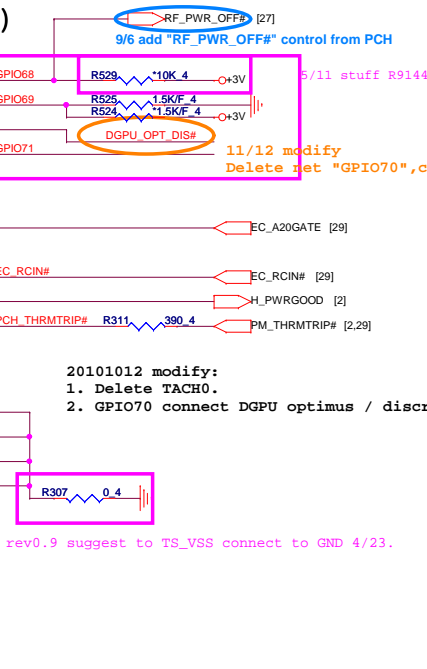
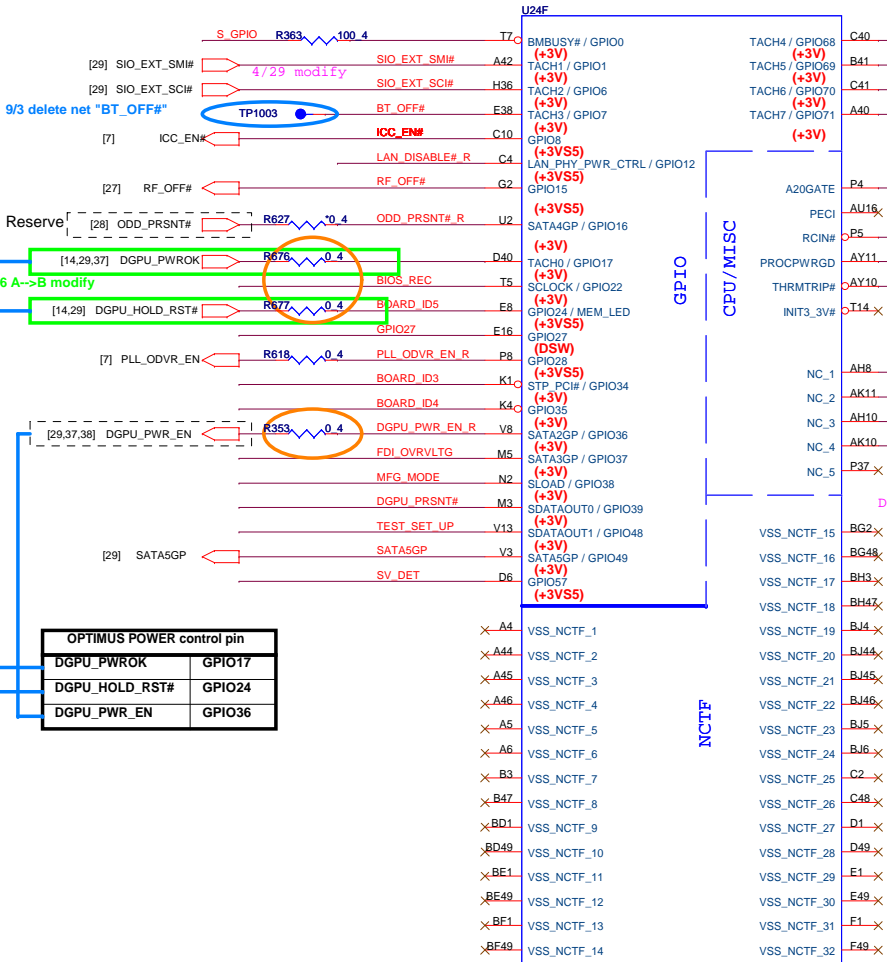
Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)



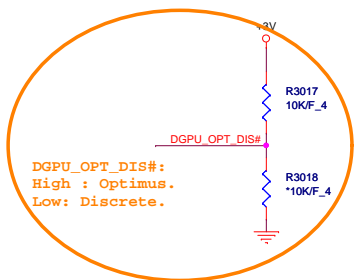
PROJECT : TWH Quanta Computer Inc. NBS Size Custom Document Number PCH 3/6 (Clock/PCI/PCIE/USB) Rev A Date: Tuesday, December 14, 2010 Sheet 8 of 40

Cougar Point (GPIO,VSS_NCTF,RSVD)



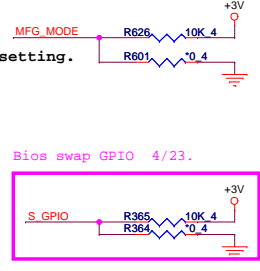
Clock Gen Power OK (CLG)

3/26 DB del external clock generator.

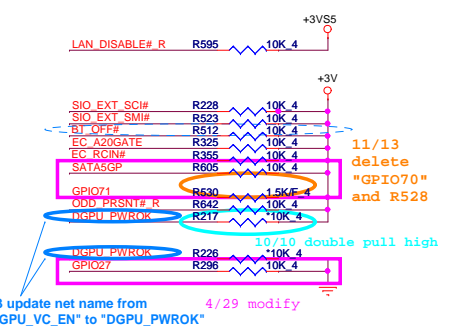


09

MFG-TEST



GPIO Pull-up/Pull-down(CLG)



OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

RF_OFF#
Low = Disable (Default)
High = Enable

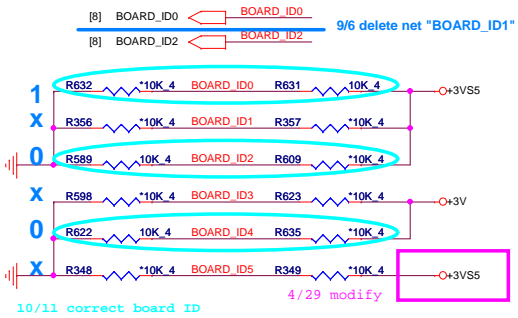
BIOS RECOVERY
High = Disable (Default)
Low = Enable

SV_SET_UP
High = Strong (Default)

TEST DETECT
Low = Default

BOARD ID SETTING

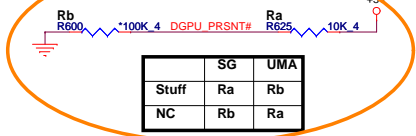
Board ID	ID0	ID1	ID2	ID3	ID4	ID5
LG	0=LG 1=CB					
UMA/Dis.						
15.6"/ 14"			0=QLH/TWH 1=QLC/SWH			
MDC						
Dobly					0=NO 1=YES	
Optiums						1=YES 0=NO



DGPU_PWR_EN R
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE
LOW - Tx, Rx terminated to same voltage

GFX Present



PROJECT : TWH
Quanta Computer Inc.

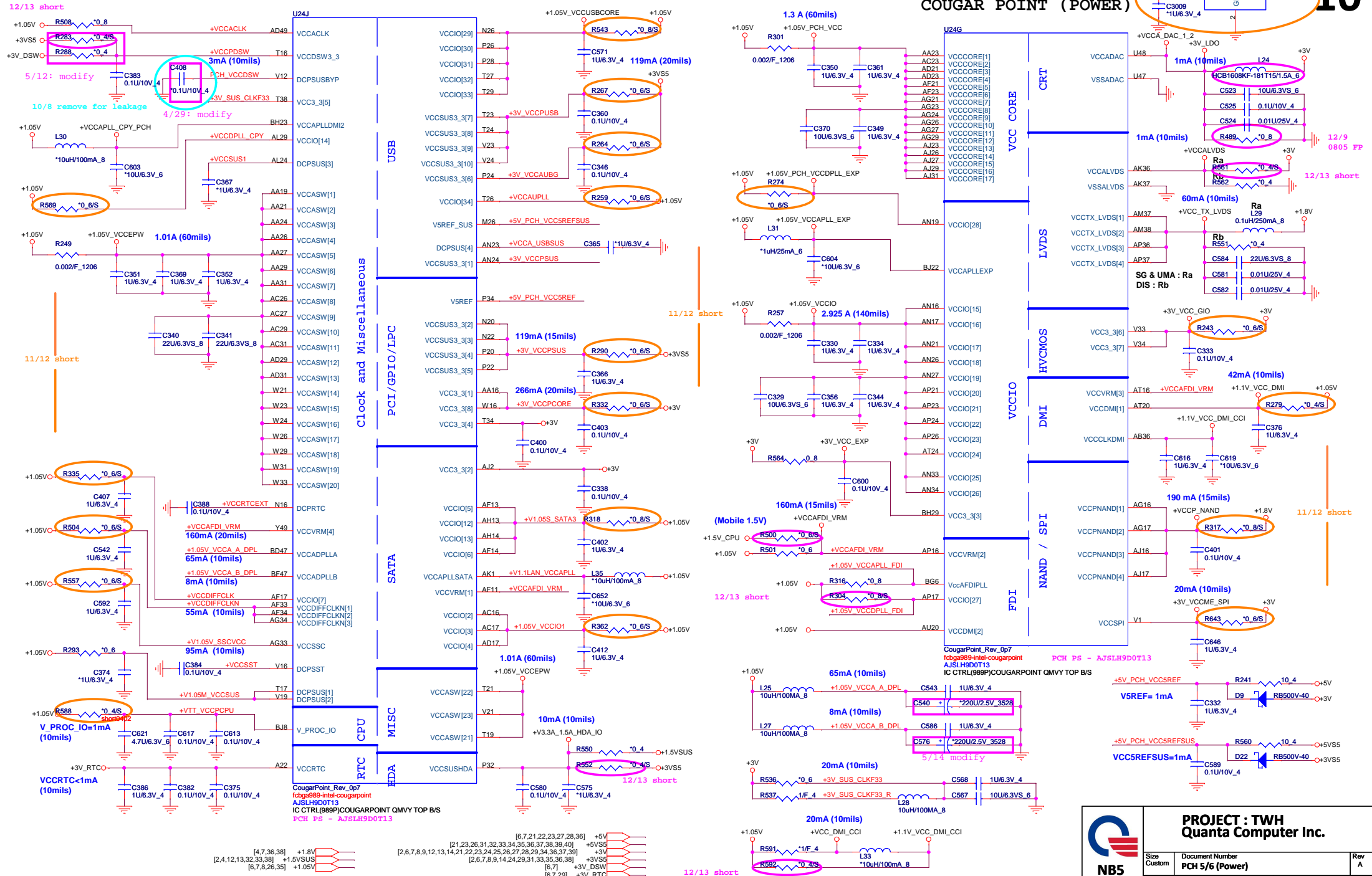
NBS

Size Custom	Document Number PCH 4/6 (GPIO)	Rev A
Date: Wednesday, December 15, 2010	Sheet 9 of 40	

Cougar Point-M (POWER)

COUGAR POINT (POWER)

10



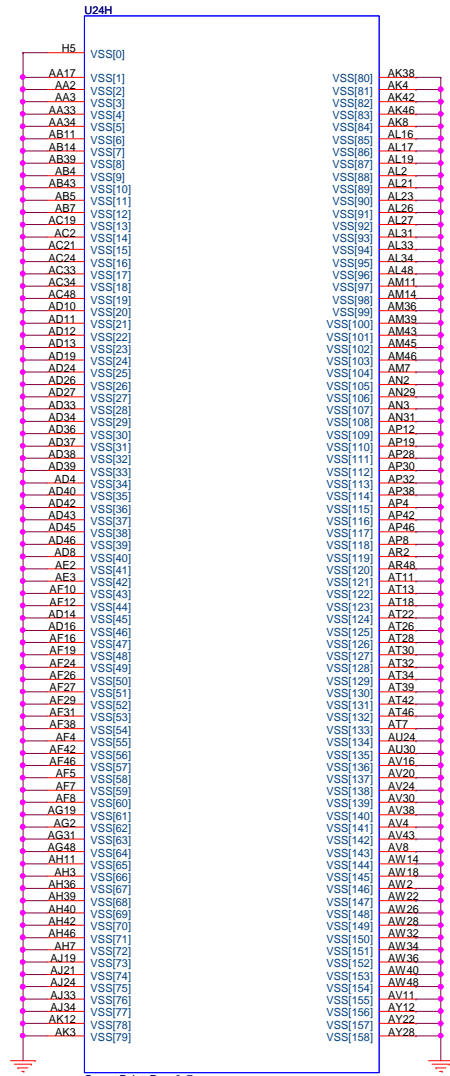
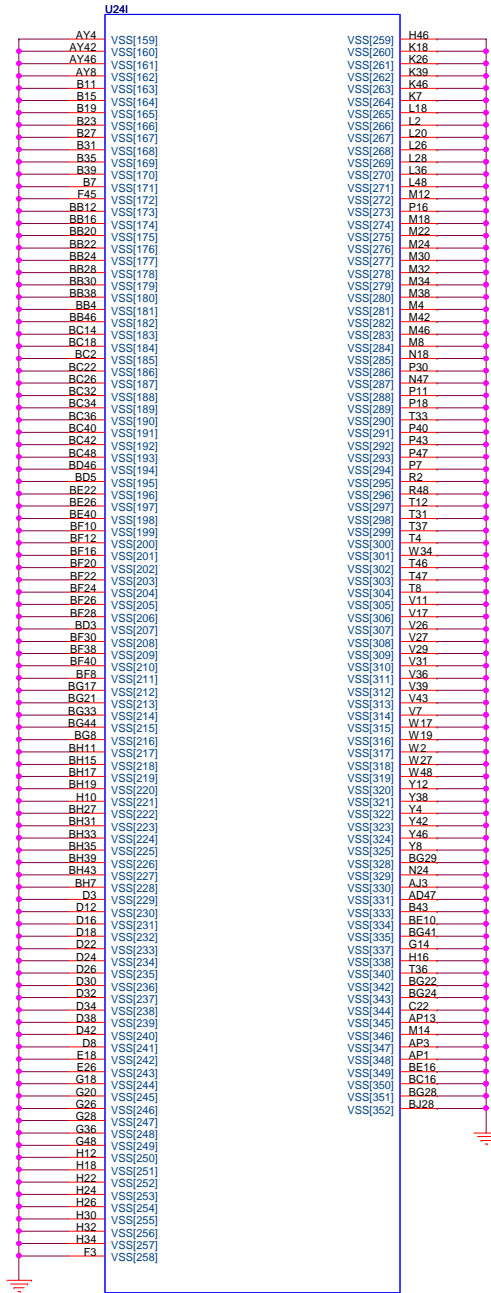
**PROJECT : TWH
Quanta Computer Inc.**

Size	Document Number	Rev
Custom	PCH 5/6 (Power)	A

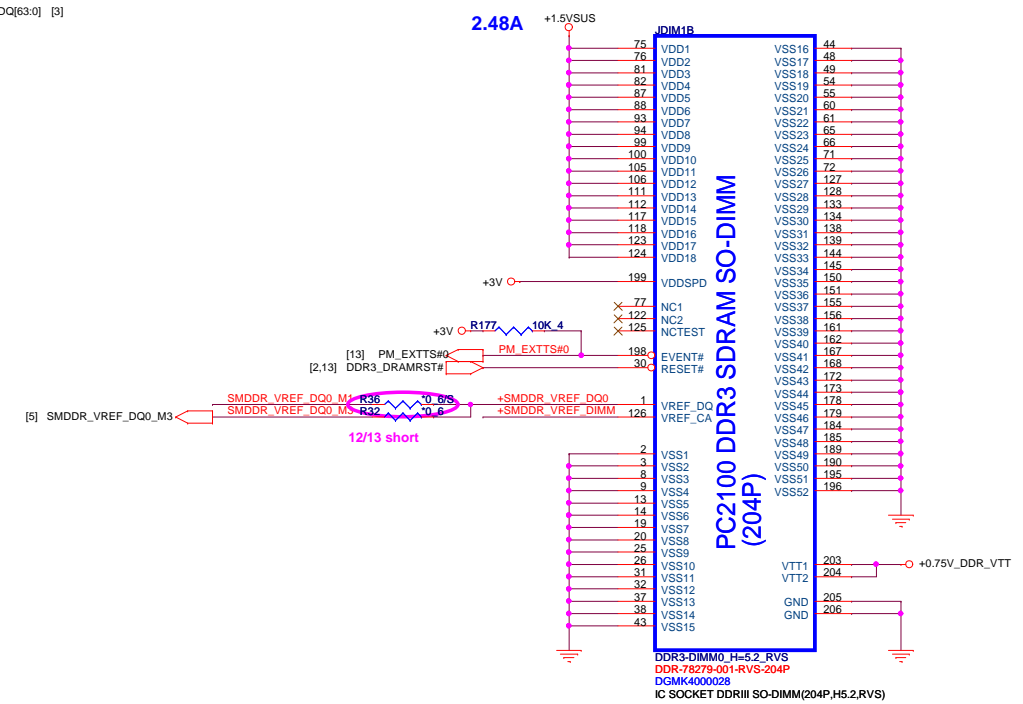
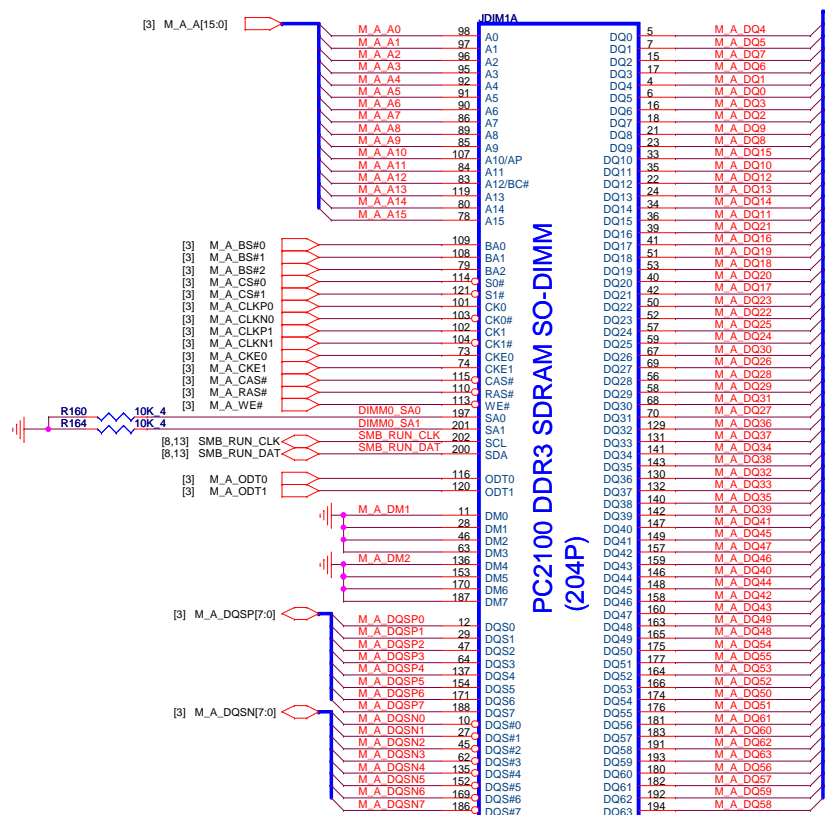
Date: Tuesday, December 14, 2010 Sheet 10 of 40

IBEX PEAK-M (GND)

IBEX PEAK-M (GND)



	PROJECT : TWH Quanta Computer Inc.		Rev A
	Size Custom	Document Number PCH 6/6 (Ground)	
	Date: Tuesday, December 14, 2010	Sheet 11 of 40	

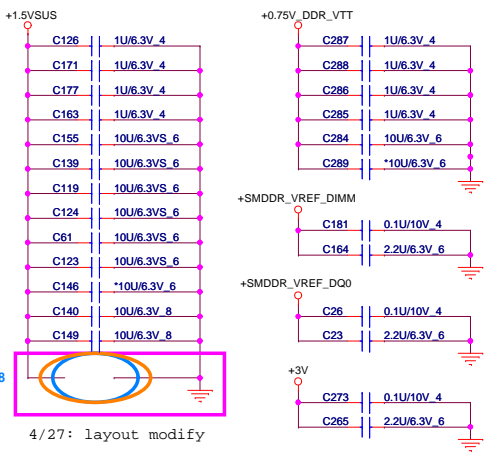


Remove M2 Solution (Intel 436996 Doc)

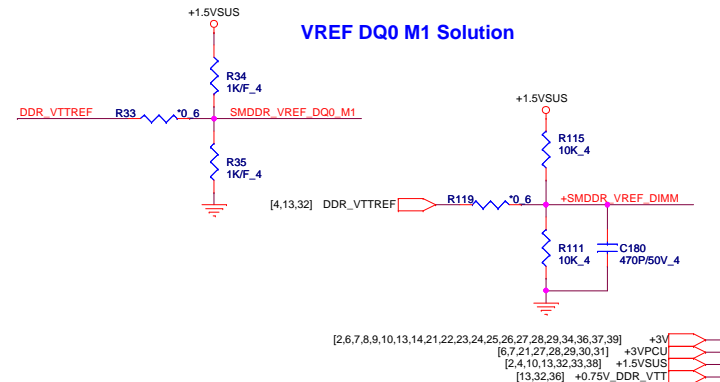
8/31 C513 FP changed from 330U_2.5V_5.0x5.9ESR10m to 220U/6.3V_6x4.5ESR18

11/13 delete C513

Place these Caps near So-Dimm0.

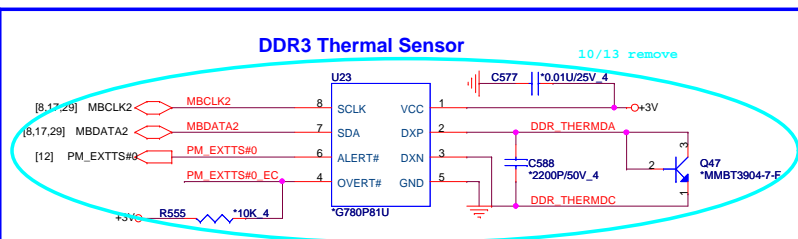
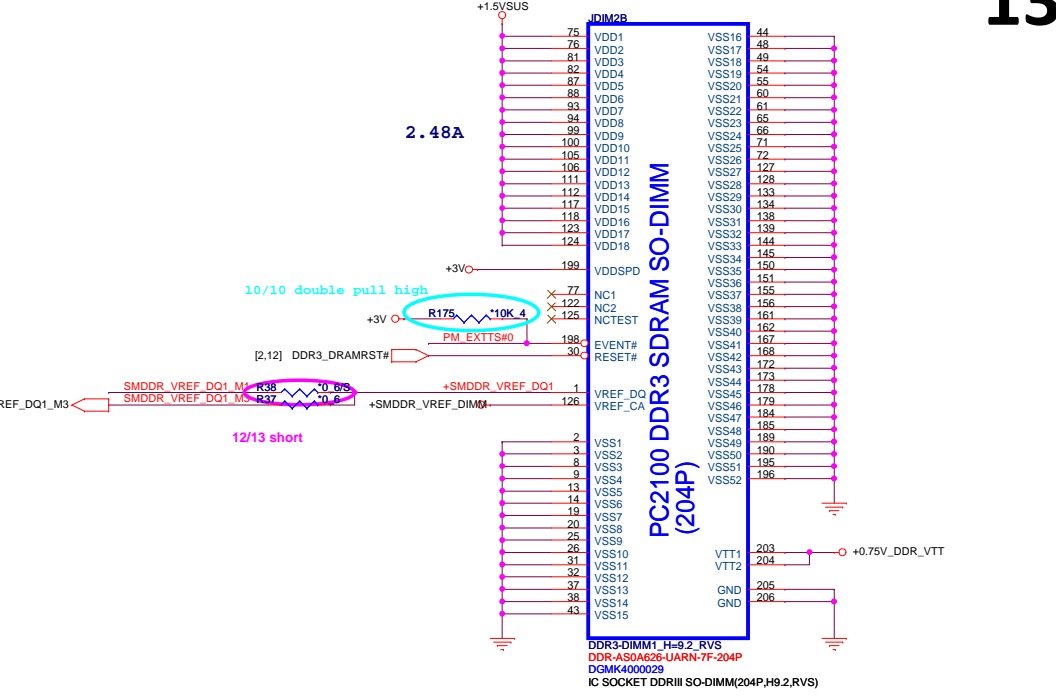
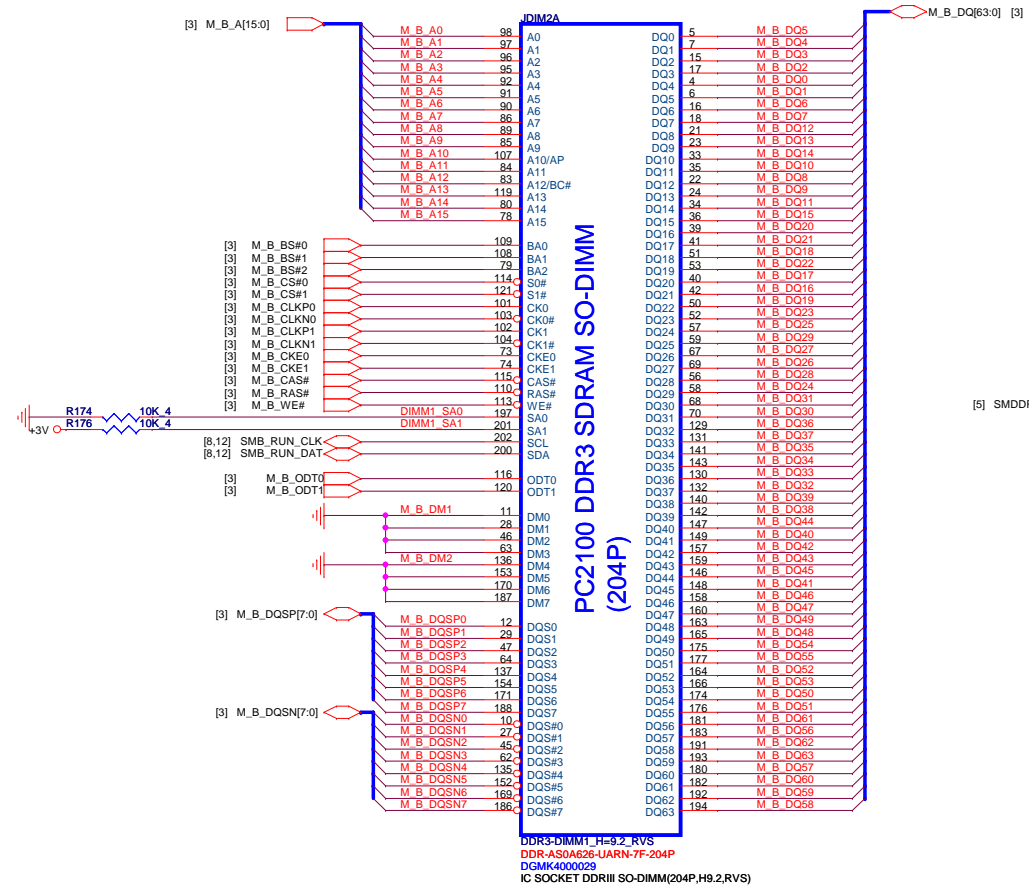


VREF DQ0 M1 Solution

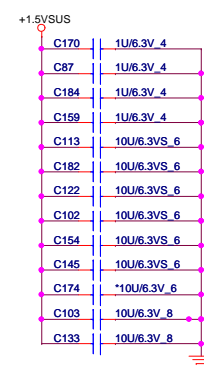


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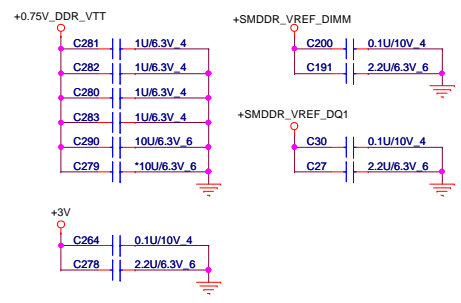
NBS	Size Custom	Document Number System Memory 1/2 (5.2H)	Rev A
	Date: Tuesday, December 14, 2010	Sheet 12 of 40	



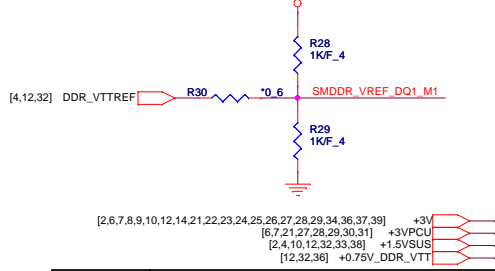
Remove M2 Solution (Intel 436996 Doc)



Place these Caps near So-Dimm1.



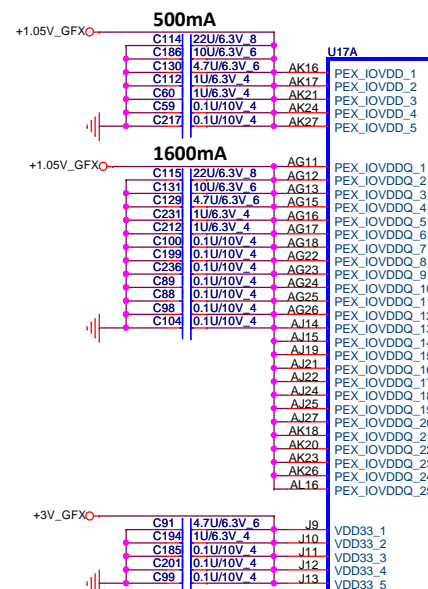
VREF DQ1 M1 Solution



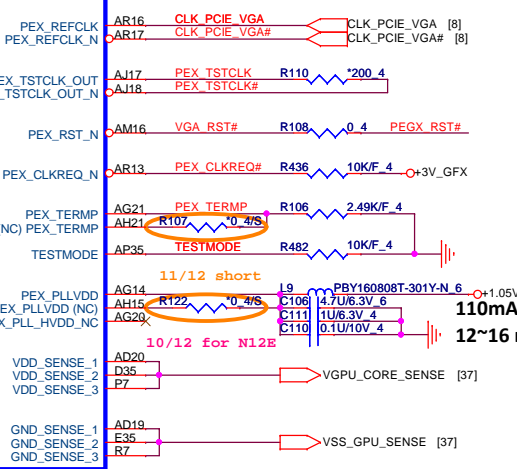
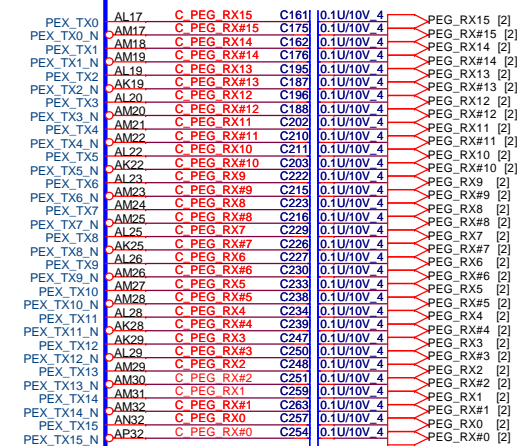
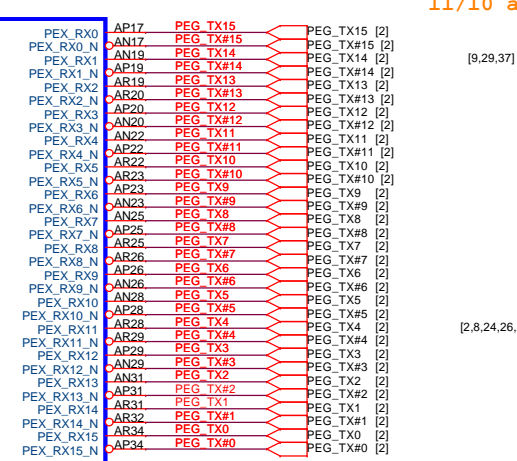
PROJECT : TWH
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NBS

Size: Custom	Document Number: System Memory 2/2 (9.2H)	Rev: A
Date: Tuesday, December 14, 2010	Sheet: 13 of 40	

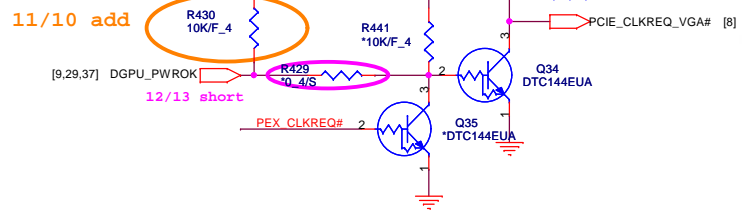


PEG Interface



N12P AJ0N12P0T04

For Discrete



For Discrete

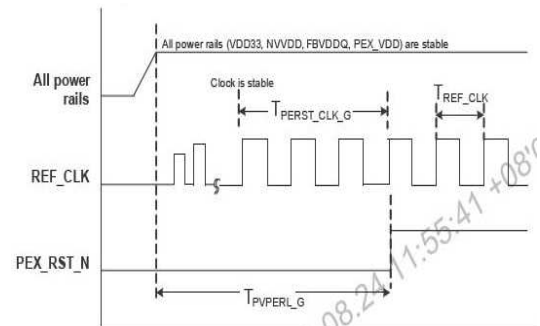
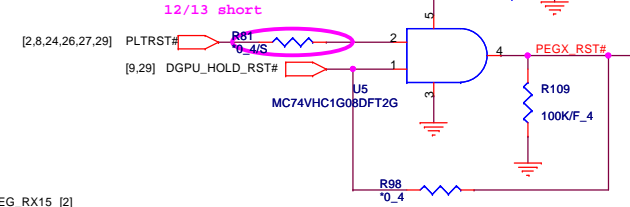


Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL_G} \ge 1\mu s$	
$T_{PPEST_CLK_G}$	$T_{PPEST_CLK_G} \ge 11T_{REF_CLK}$	

Power Sequence

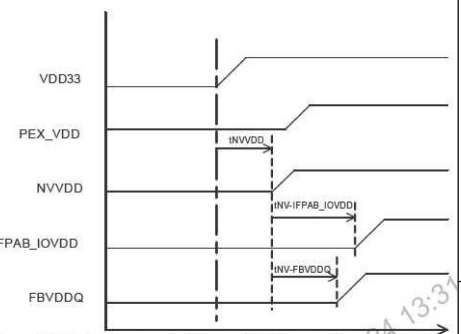


Figure 3-20 Recommended Power On Sequencing Order

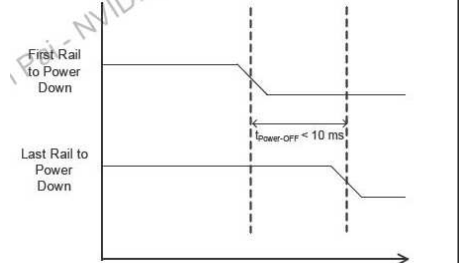


Figure 3-21 Recommended Power Off Sequencing Order

NVDD Settling Time

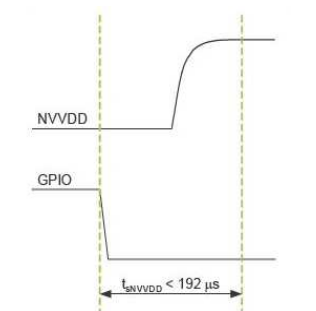
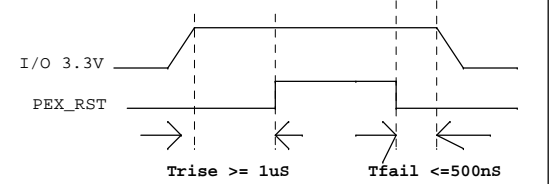


Figure 3-12 NVDD Settling Time

PEG_RST timing

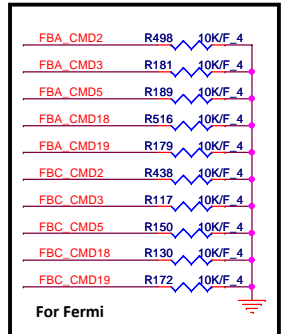
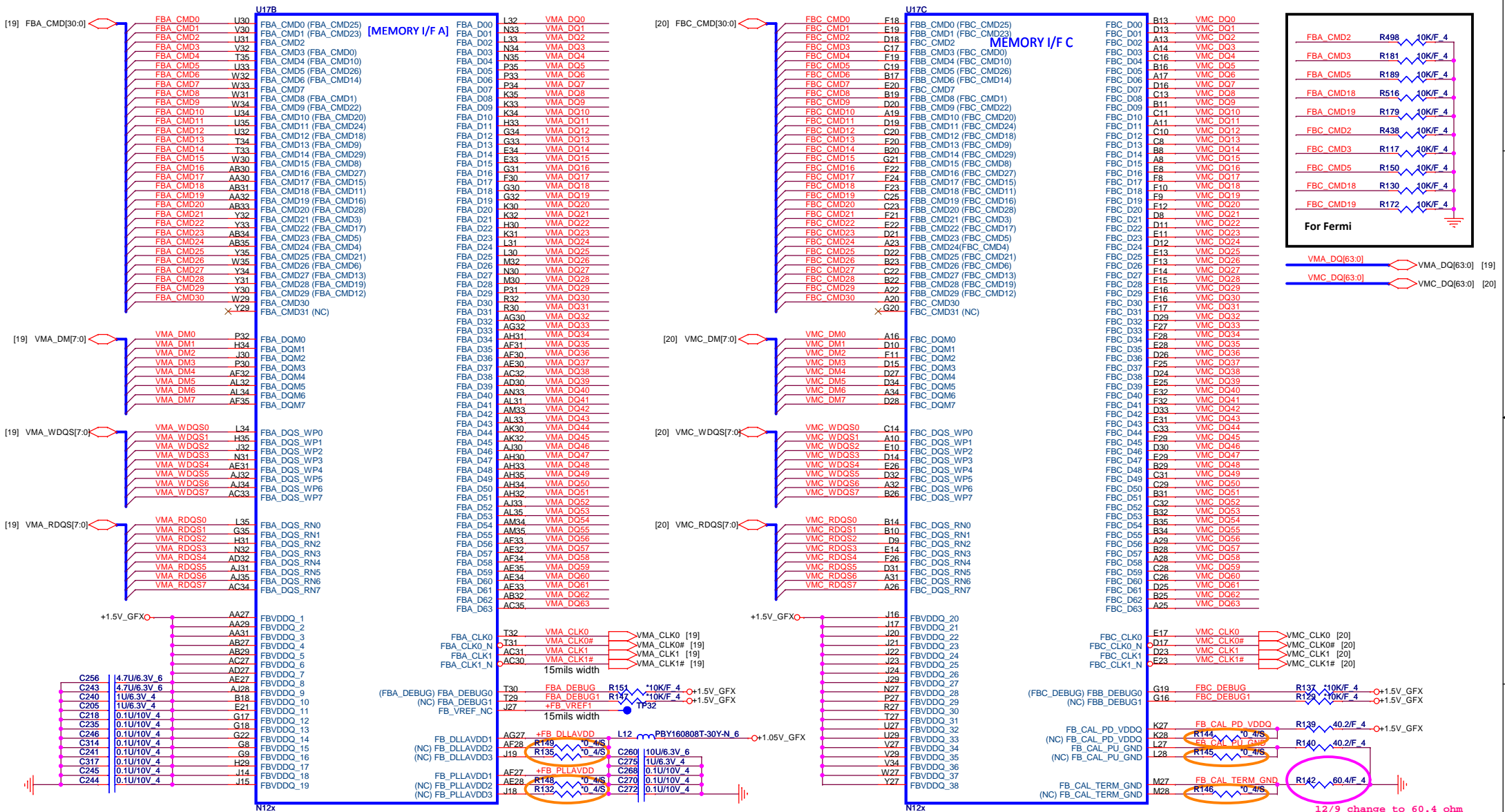


PROJECT : TWH
Quanta Computer Inc.

Rev A

Size A3	Document Number DGPU 1/5 (PEG)	Sheet 14 of 40
Date: Tuesday, December 14, 2010		

[15,16,37,38] +1.05V_GFX
[16,17,22,37,38] +3V_GFX



N12P AJ0N12P0T04

10/12 for N12E
11/12 short

N12P AJ0N12P0T04

10/12 for N12E
11/12 short

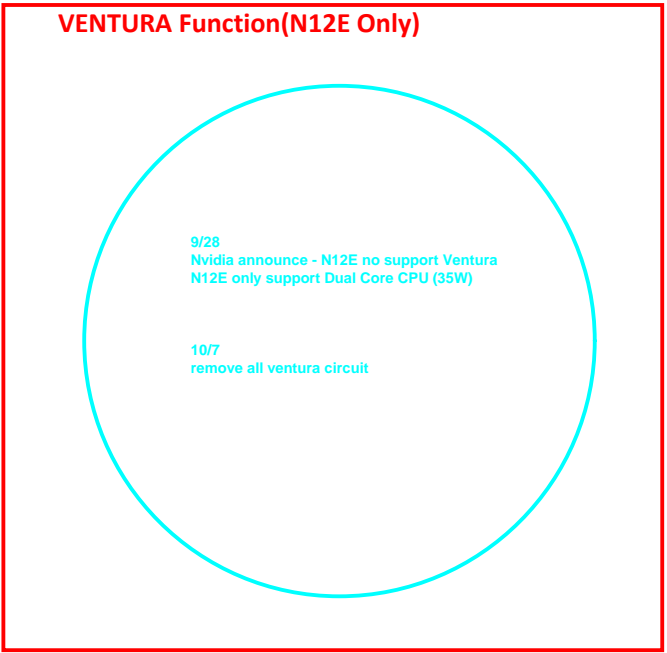
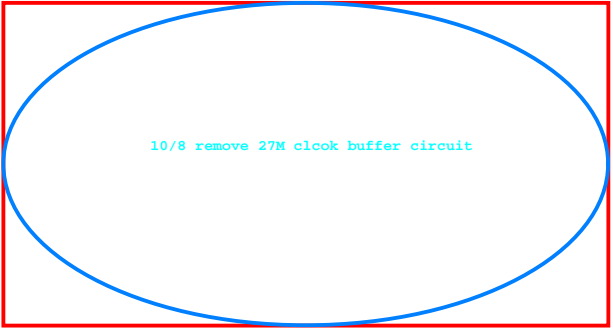
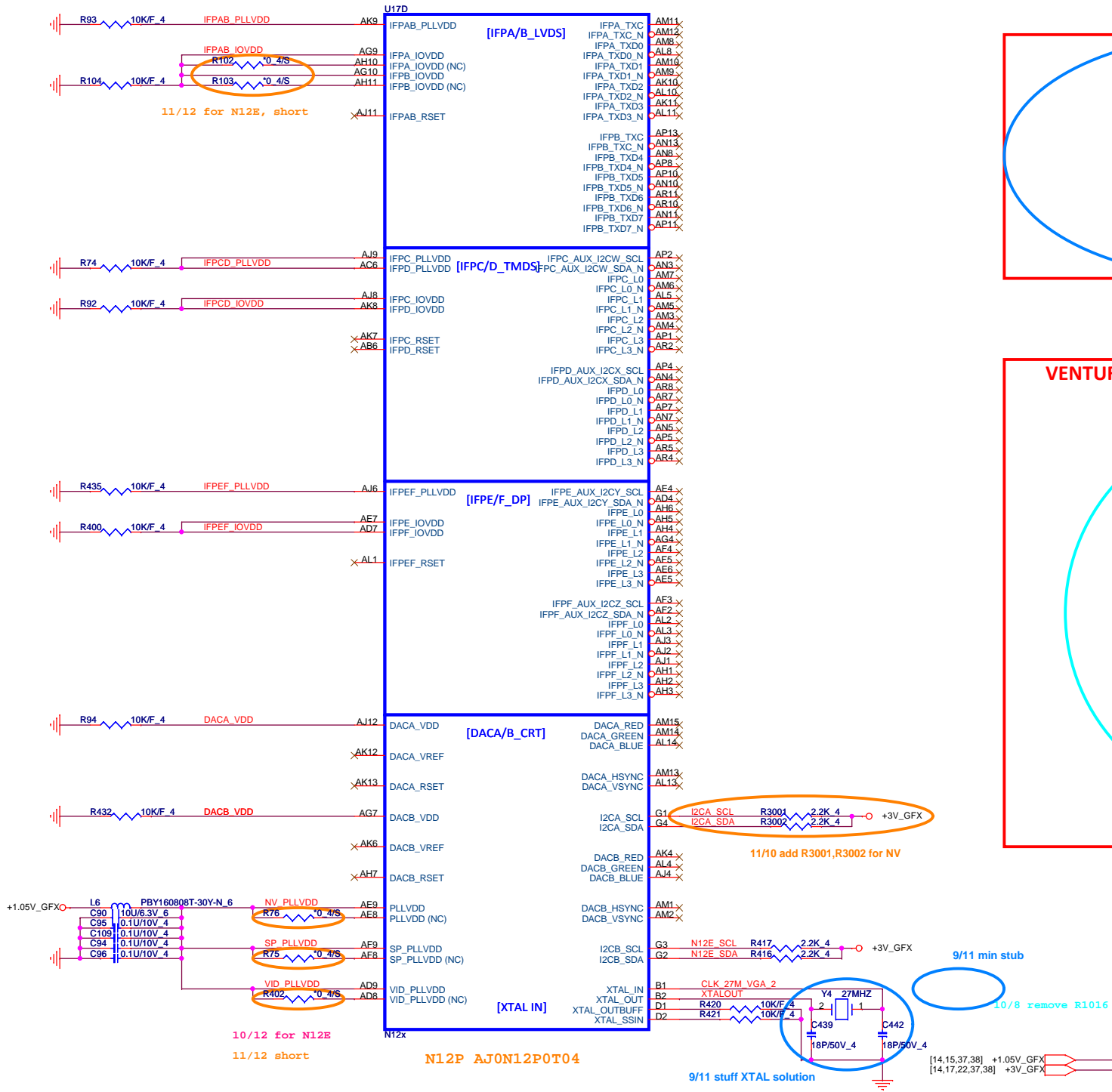
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NBS

Size A3 Document Number **DGPU 2/5 (Memory)** Rev A

Date: Tuesday, December 14, 2010 Sheet 15 of 40

[14,16,37,38] +1.05V_GFX
[19,20,37,38] +1.5V_GFX

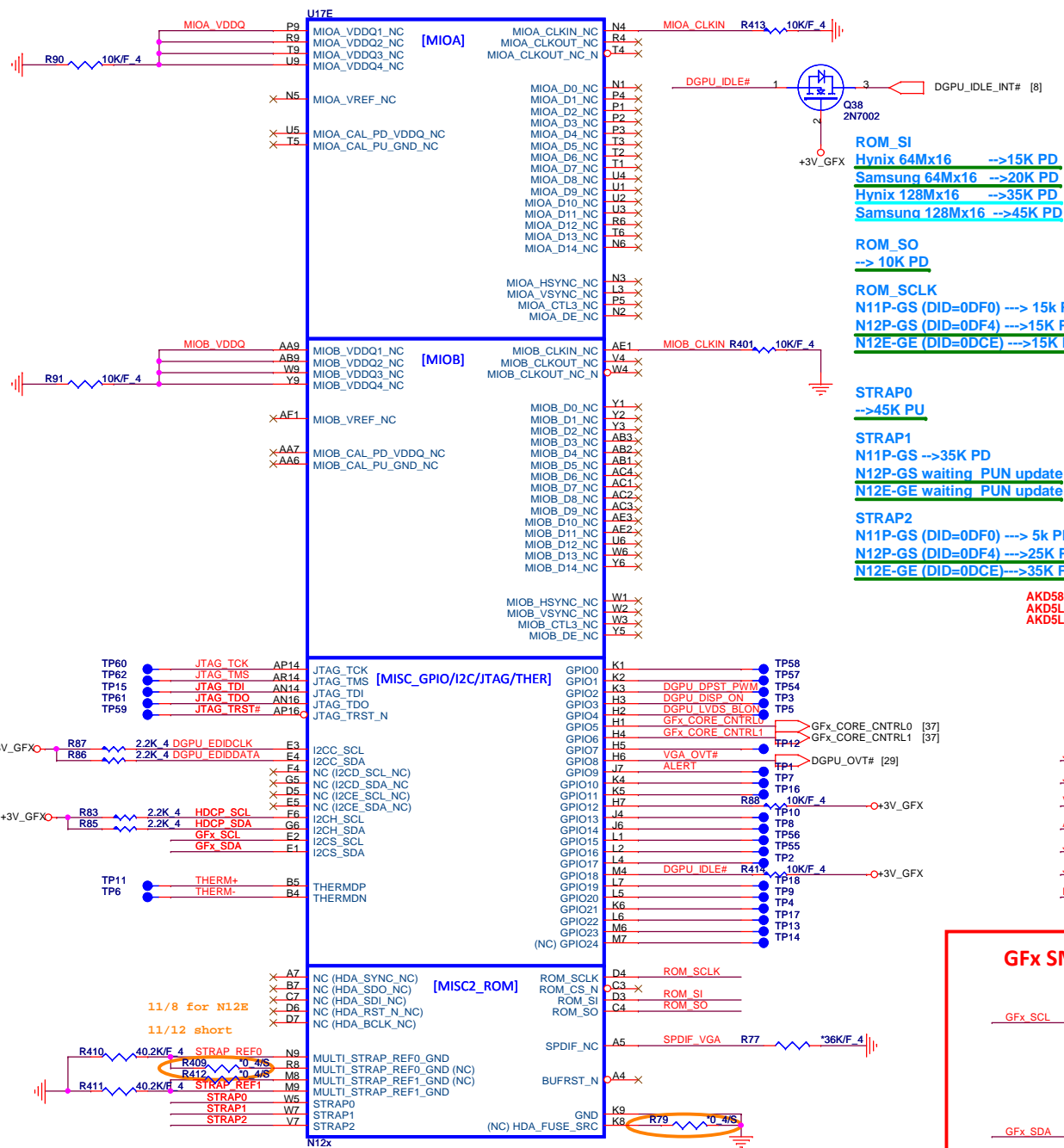


**PROJECT : TWH
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Size A3	Document Number DGPU 3/5 (Display)	Rev A
Date: Tuesday, December 14, 2010	Sheet	16 of 40

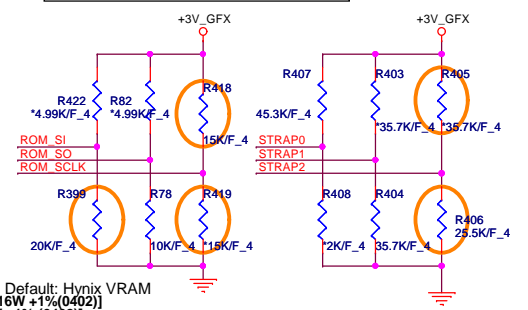
N11P-GS ES
Strap2 = 35K Pull High
ROM_CLK=15k Pull High

N11P-GS QS
Strap2 = 5K Pull High
ROM_CLK=15k Pull High



Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Default: Hynix VRAM
 4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
 10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1%(0402)]
 15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1%(0402)]
 20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +1%(0402)]
 30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1%(0402)]
 35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1%(0402)]
 45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1%(0402)]

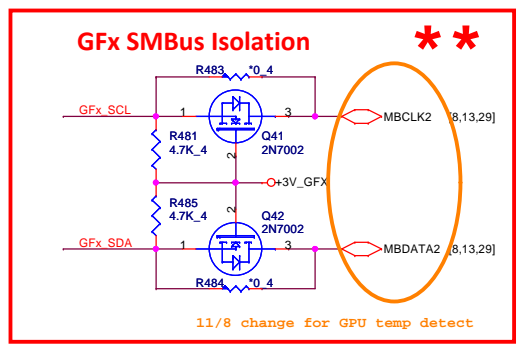
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0		
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK		PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0110		Reserved		
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

GPIO ASSIGNMENTS

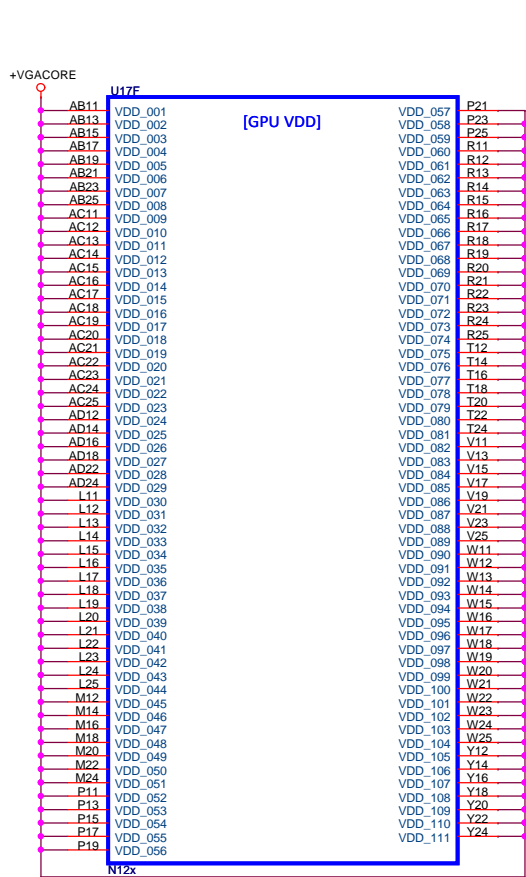
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL



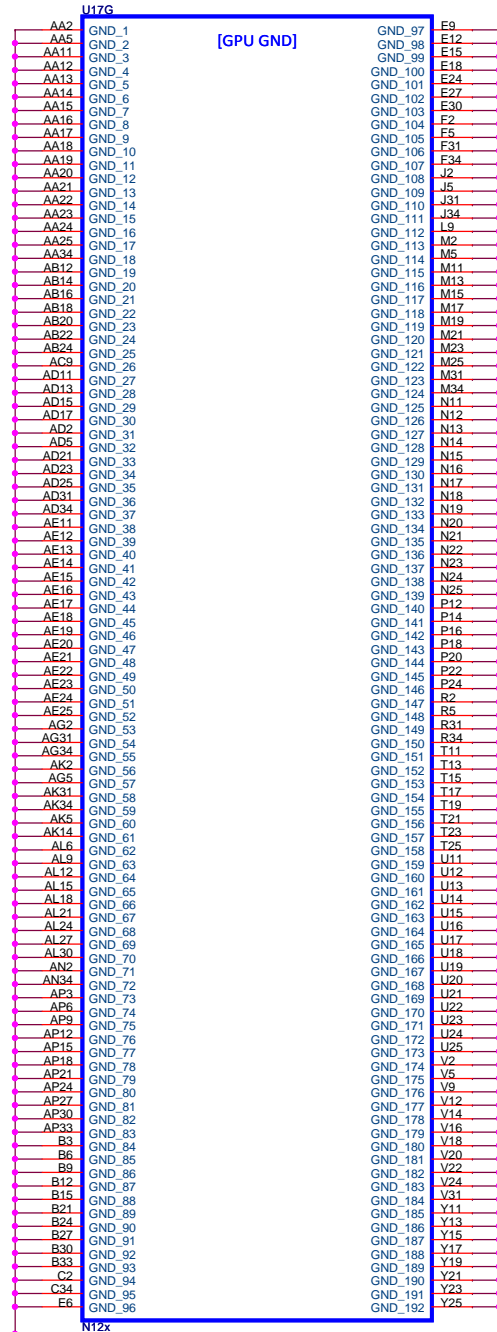
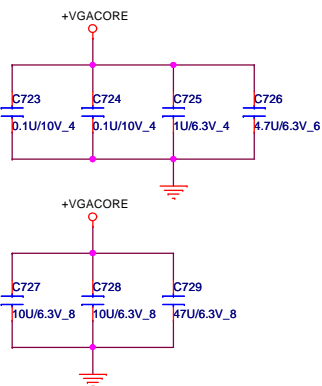
N12P AJ0N12P0T04

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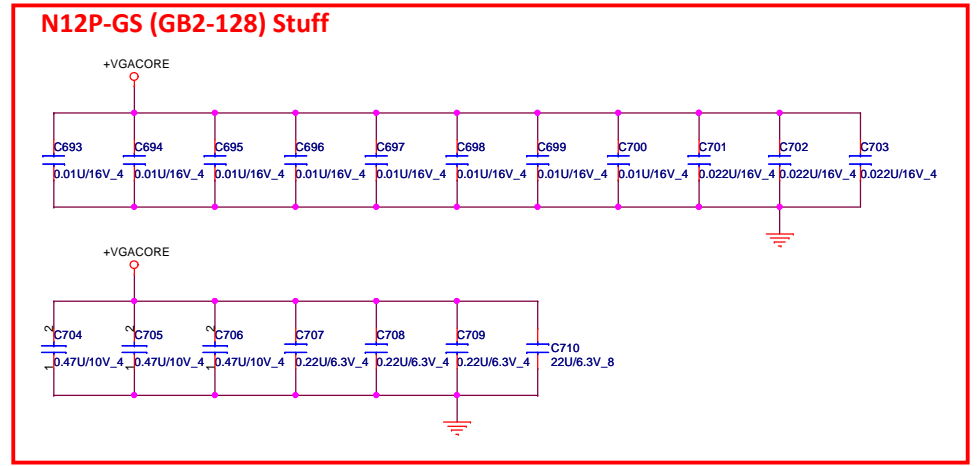
Size Custom	Document Number DGPU 4/5 (MIO/GPIO)	Rev A
Date: Wednesday, December 15, 2010 Sheet 17 of 40		



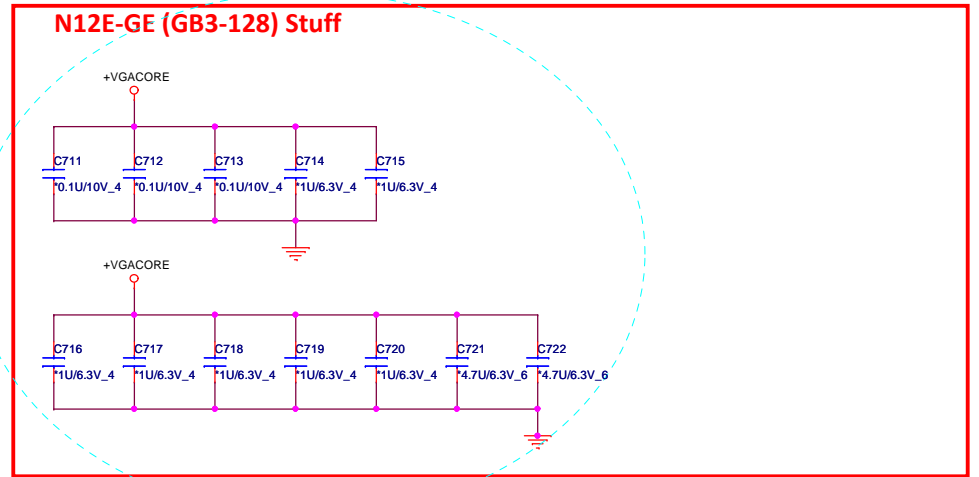
N12P AJ0N12P0T04



N12P AJ0N12P0T04



N12E-GE: C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411 stuff 0.1U/10V_4. N12E-GE: C412 Stuff 47U/6.3V_8

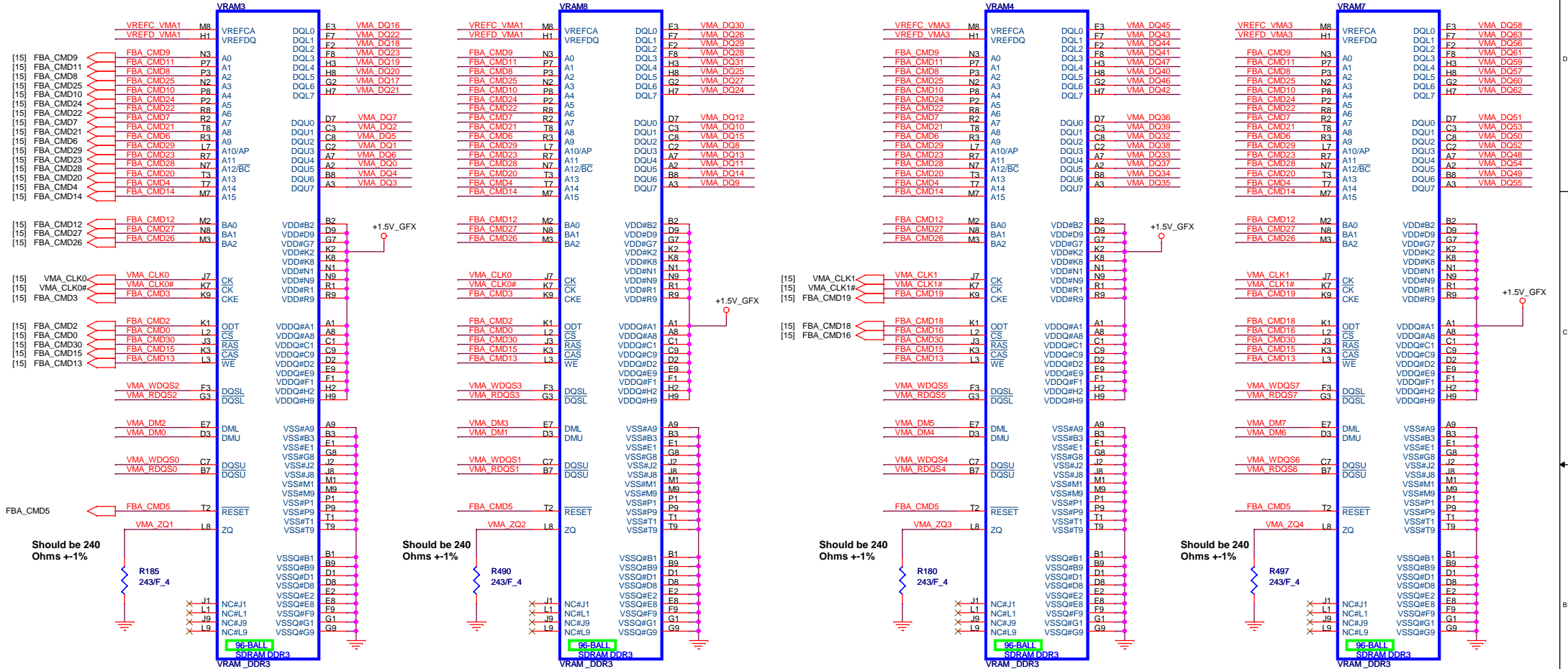


9/28 need check for N12E

[37] +VGACORE

	PROJECT : TWH Quanta Computer Inc.		Rev A
	Size A3	Document Number DGPU 5/5 (Power/Ground)	
		Sheet 18 of 40	

CHANNEL A: 256MB/512MB DDR3

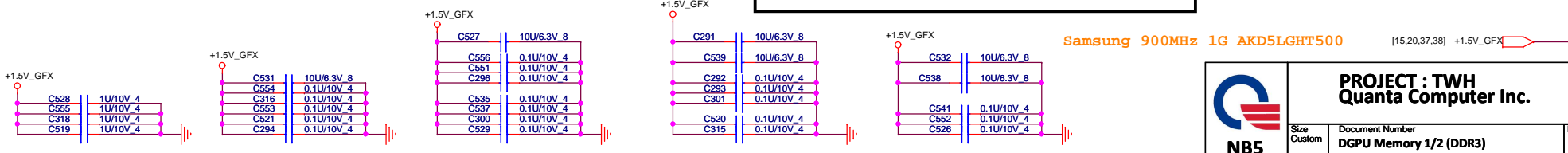


VMA_CLK#
R178
160/F_4
VMA_CLK#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1%(0402)

VMA_CLK1#
R183
160/F_4
VMA_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1%(0402)



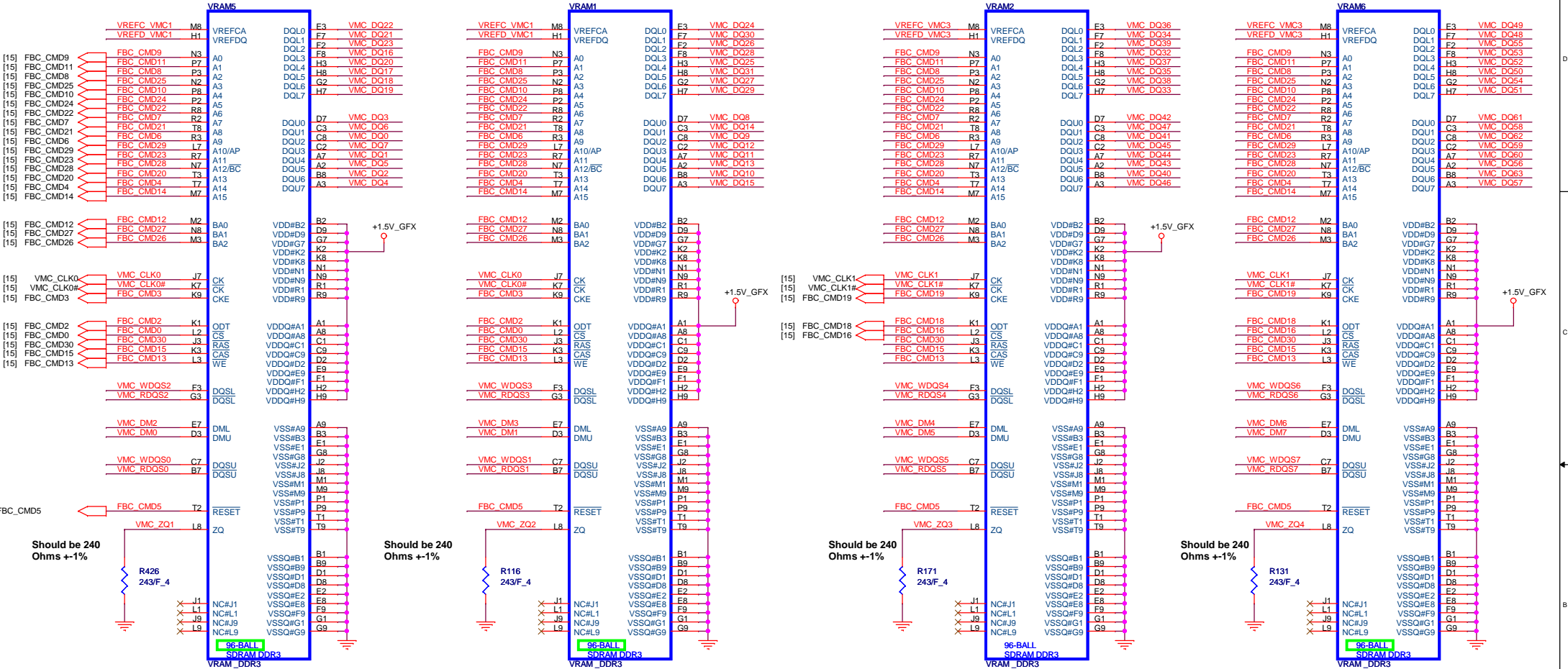
Samsung 900MHz 1G AKD5LGH7500 [15.20.37.38] +1.5V_GFX

PROJECT : TWH Quanta Computer Inc.

Size Custom Document Number **DGPU Memory 1/2 (DDR3)** Rev A

Date: Wednesday, December 15, 2010 Sheet 19 of 40

CHANNEL B: 256MB/512MB DDR3

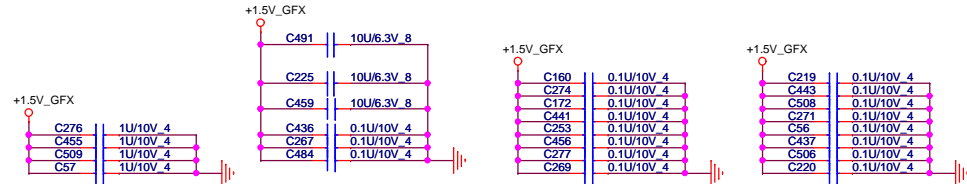


VMC CLK0
 R61 160F_4
 VREFC_VMC1
 VMC_CLK0#

Fermi : Change to 160 ohm
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
 2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

VMC CLK1
 R173 160F_4
 VREFD_VMC1
 VMC_CLK1#

Fermi : Change to 160 ohm
 1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
 2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

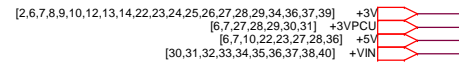
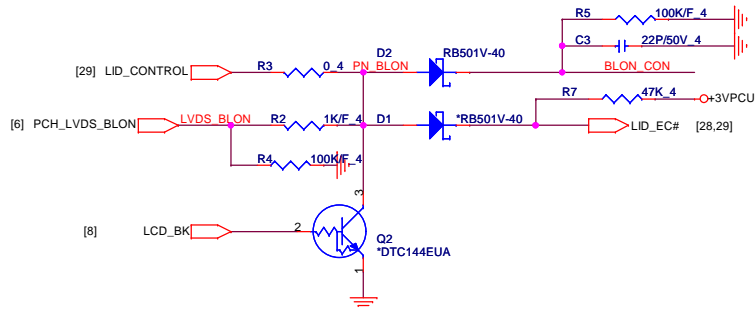
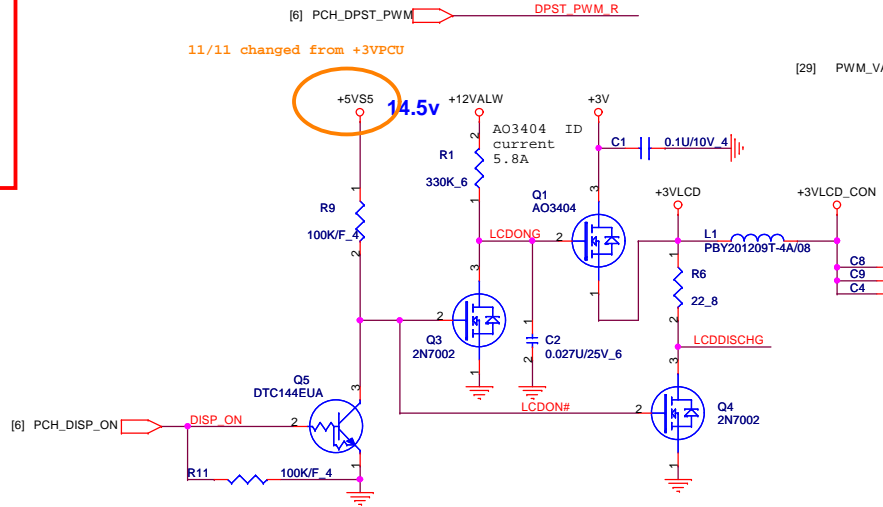
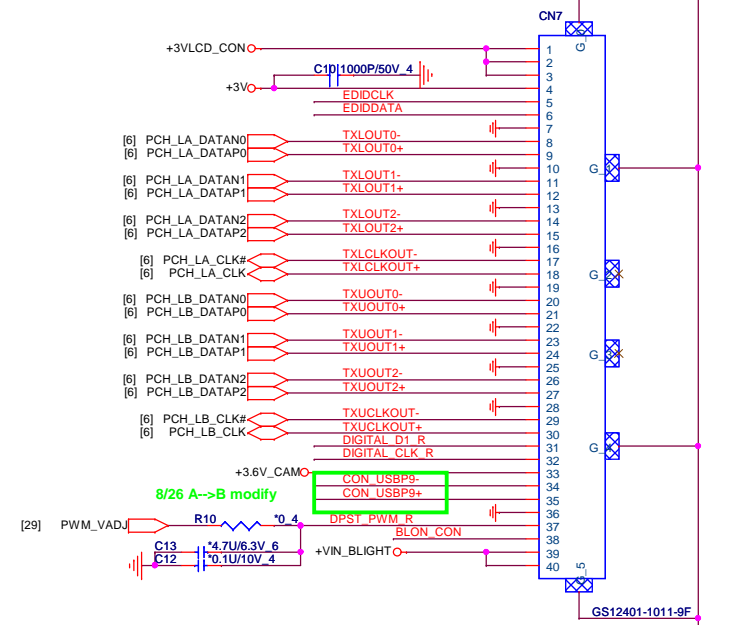
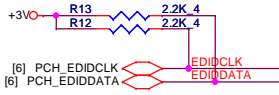
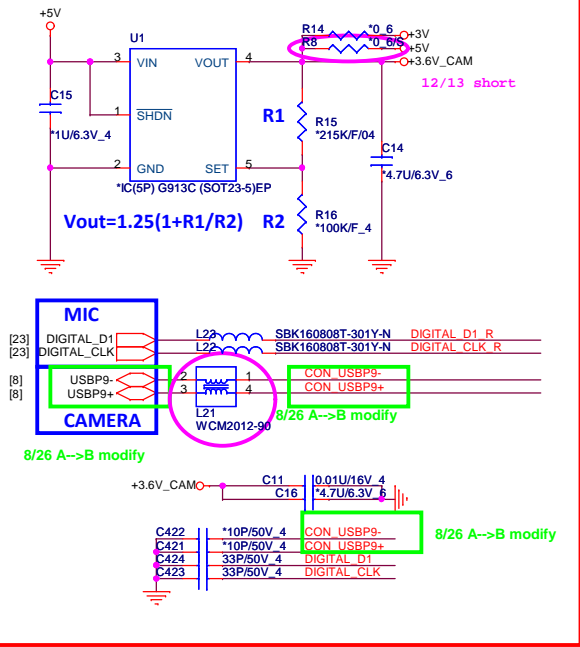


Samsung 900MHz 1G AKD5LGH500

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Size Custom	Document Number DGPU Memory 2/2 (DDR3)	Rev A
Date: Wednesday, December 15, 2010		Sheet 20 of 40

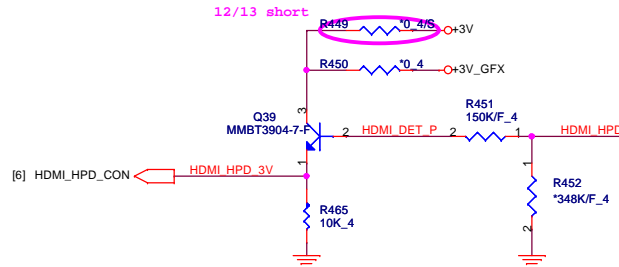
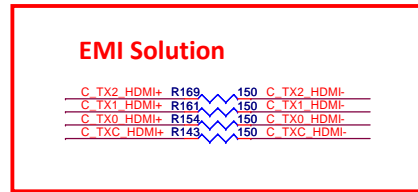
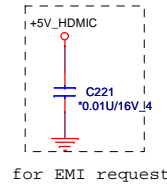
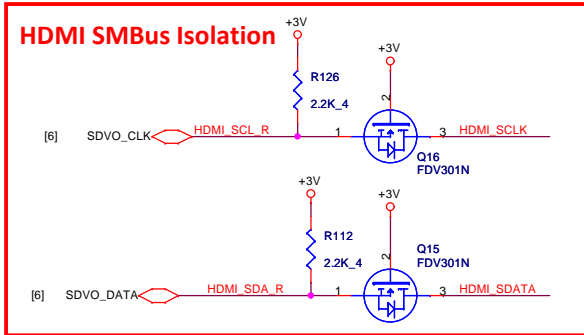
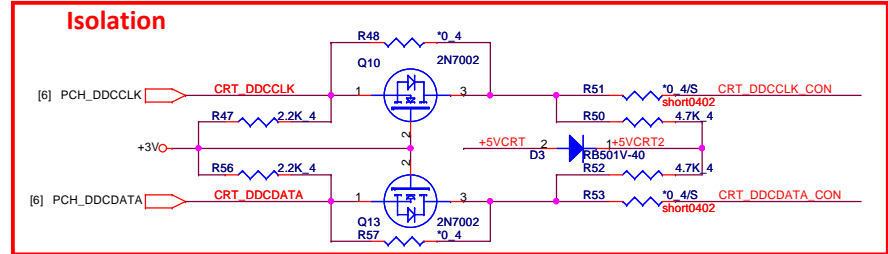
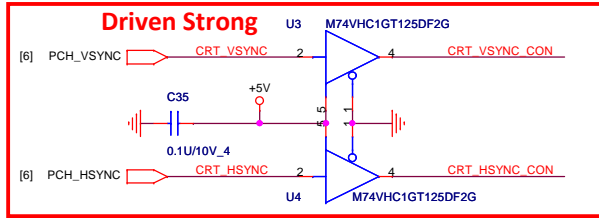
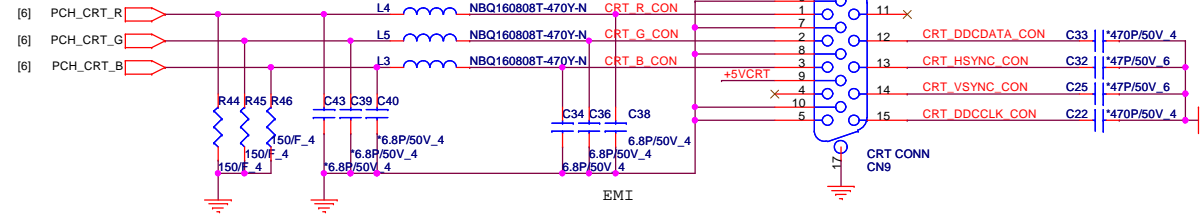
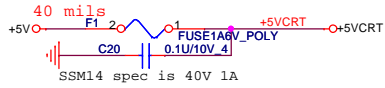
USB Camera Connector



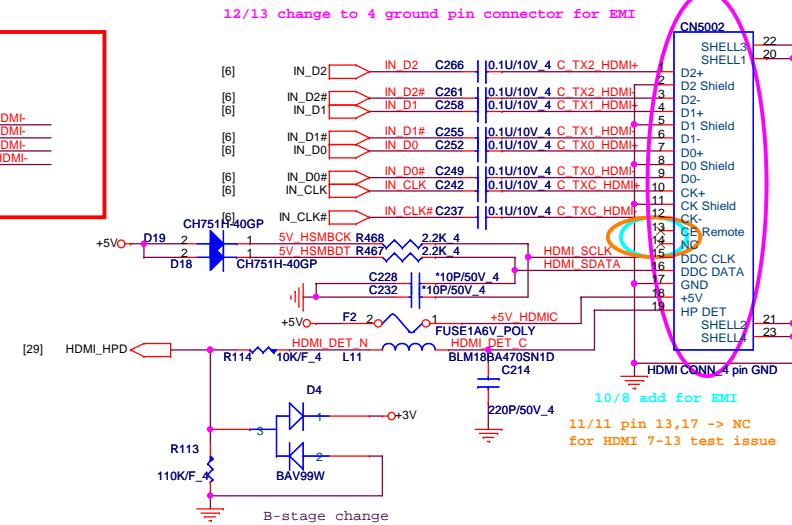
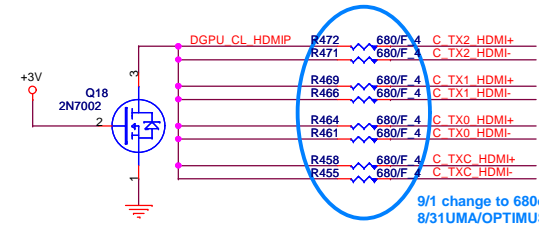
PROJECT : TWH Quanta Computer Inc.		
Size Custom	Document Number LCD Connector (LVDS)	Rev A
Date: Tuesday, December 14, 2010		Sheet 21 of 40

CRT PORT

40 MIL

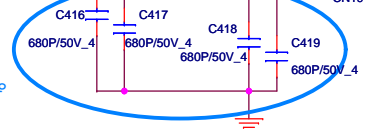
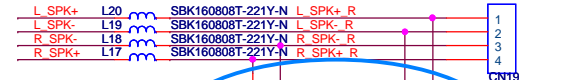


HDMI PORT

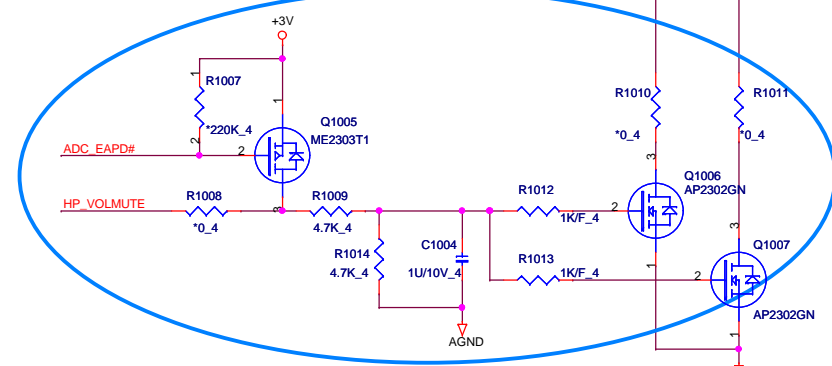


9/1 change to 680ohm
8/31UMA/OPTIMUS-680 ohm, DISCRETE-499 ohm

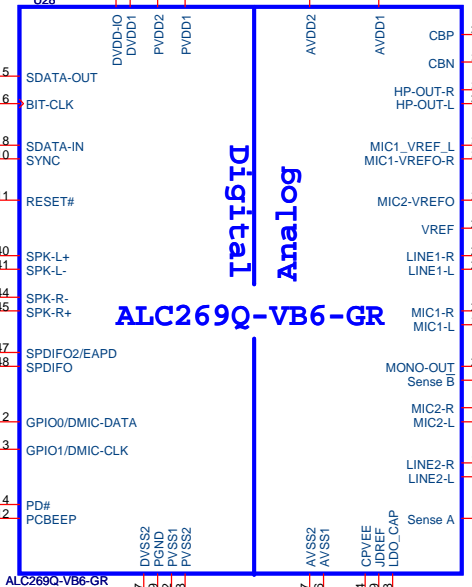
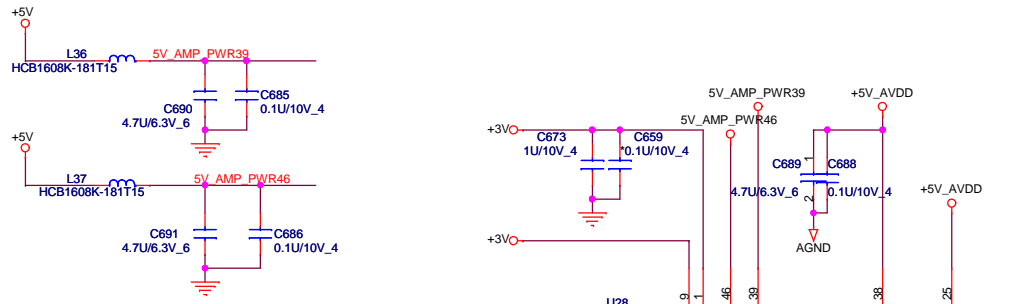
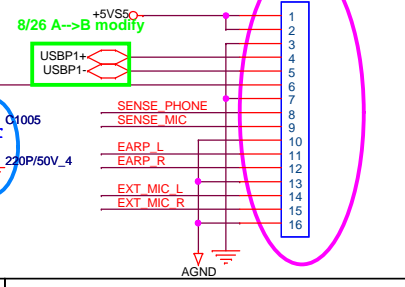
Internal Speaker



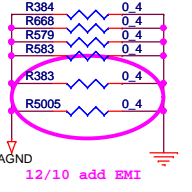
9/5 add de-pop circuit, add C1002, C1003, C1004 Q1005, Q1006, Q1007 R1007, R1008, R1009, R1010, R1011, R1012, R1013, R1014



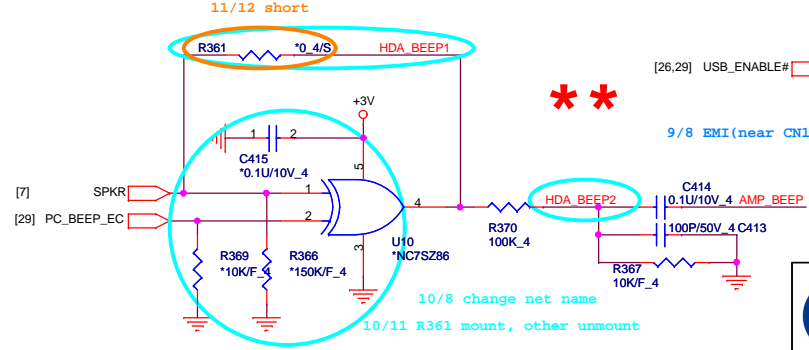
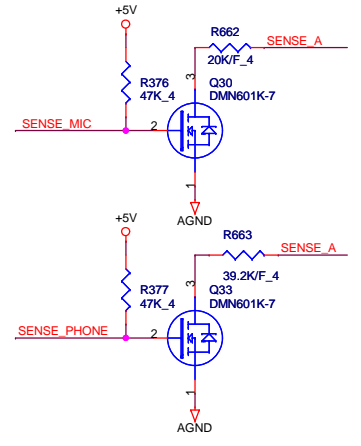
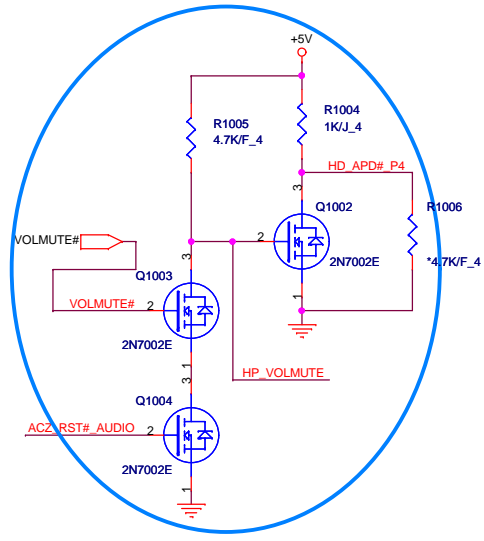
12/8 change to 16 pin connector (add 2 AGND pin)



10/5 change VB6



9/5 "PD#" circuit modify
 1.delete R650, R372, R373, Q27, Q28, D16, D17, D15
 2.add Q1002, Q1003, Q1004, R1004, R1005, R1006



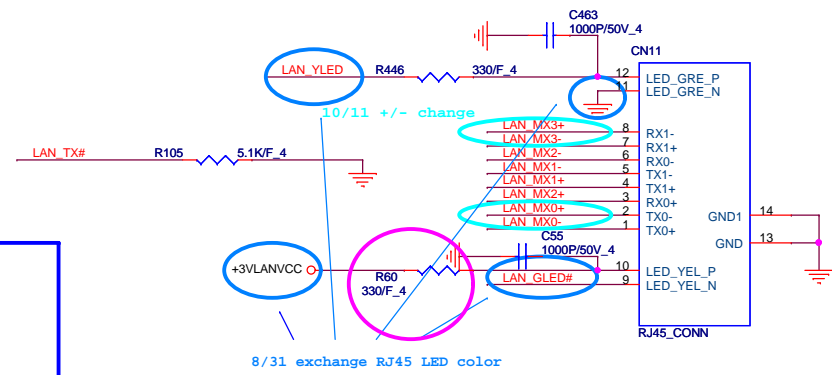
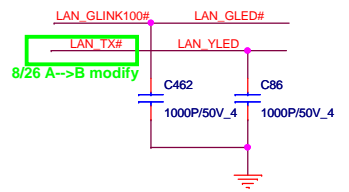
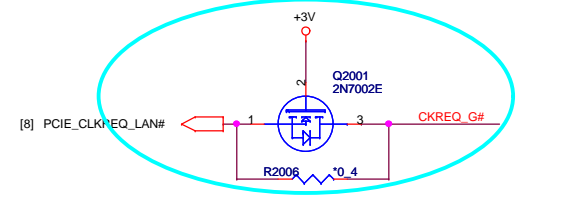
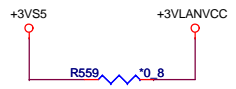
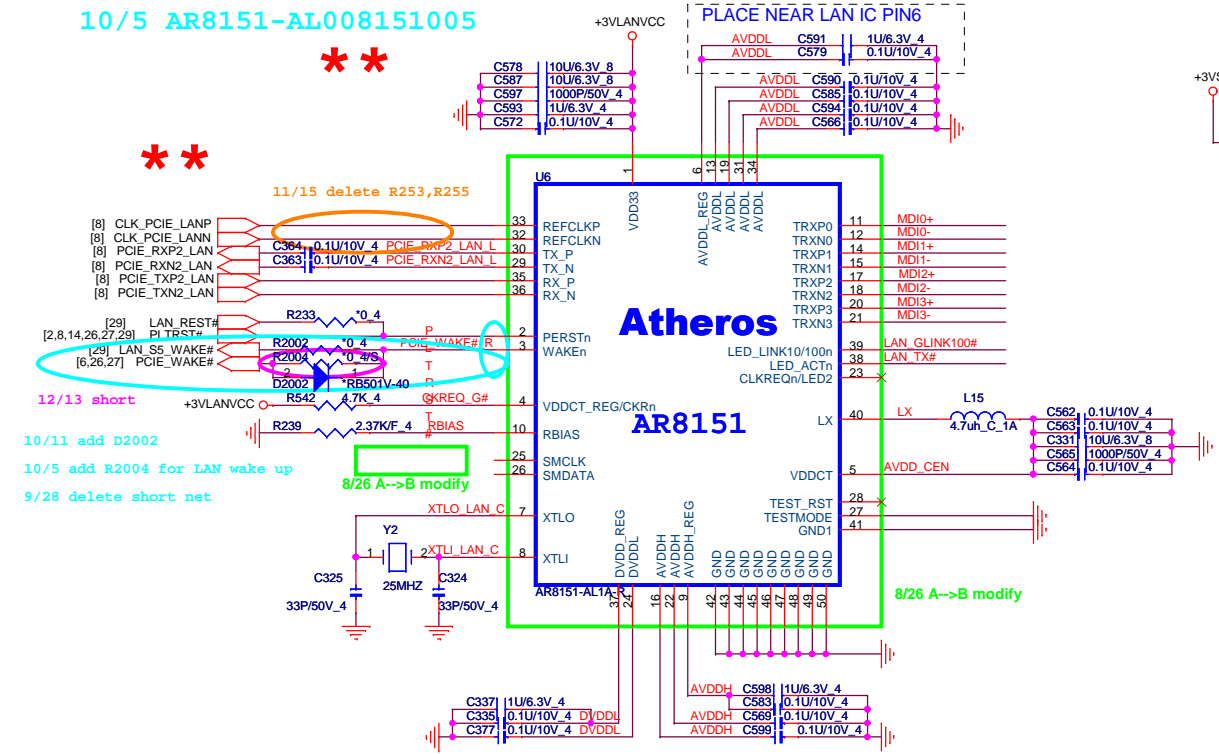
PROJECT : TWH
Quanta Computer Inc.

Size Custom Document Number **Audio Codec (Realtek_ALC269)** Rev A

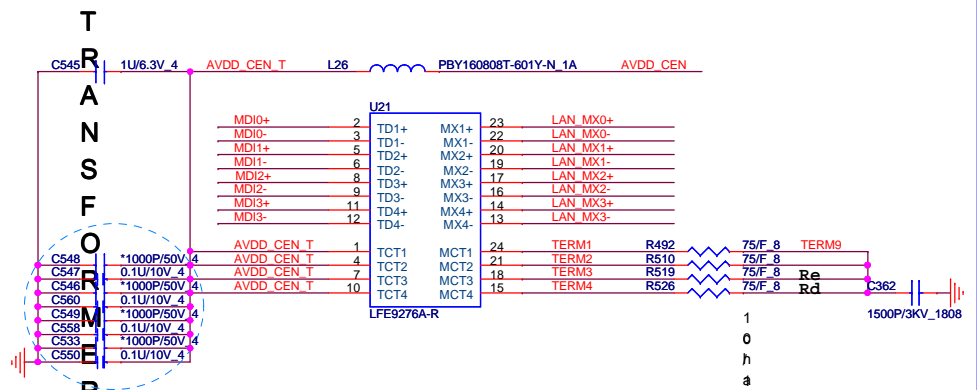
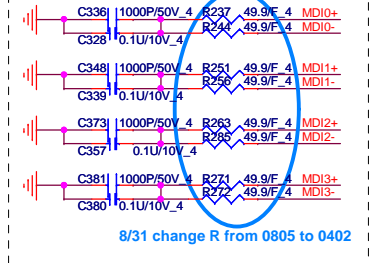
Date: Tuesday, December 14, 2010 Sheet 23 of 40

Atheros Lan

10/5 AR8151-AL008151005



PLACE NEAR LAN IC SIDE

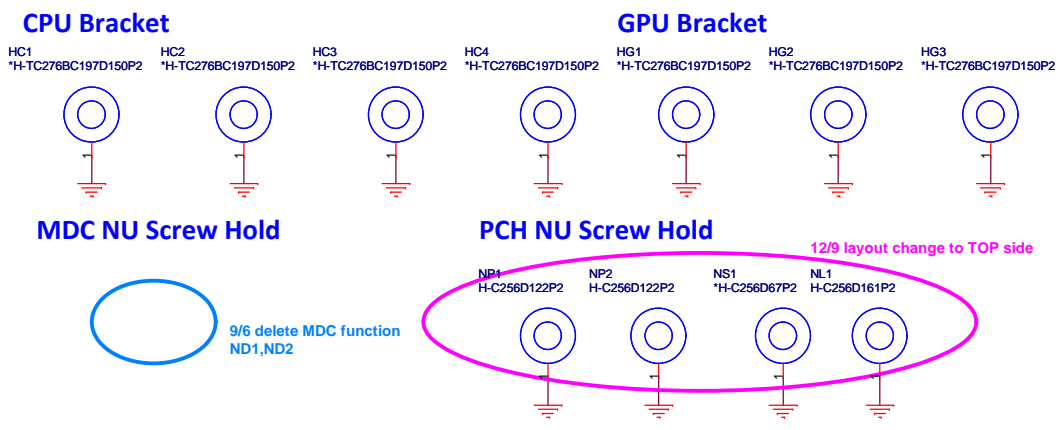
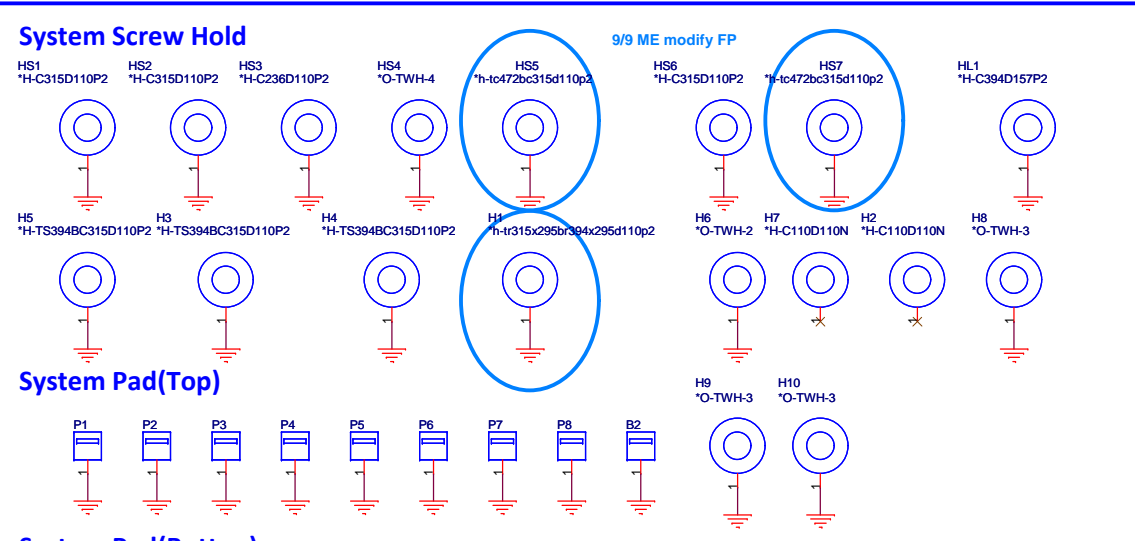
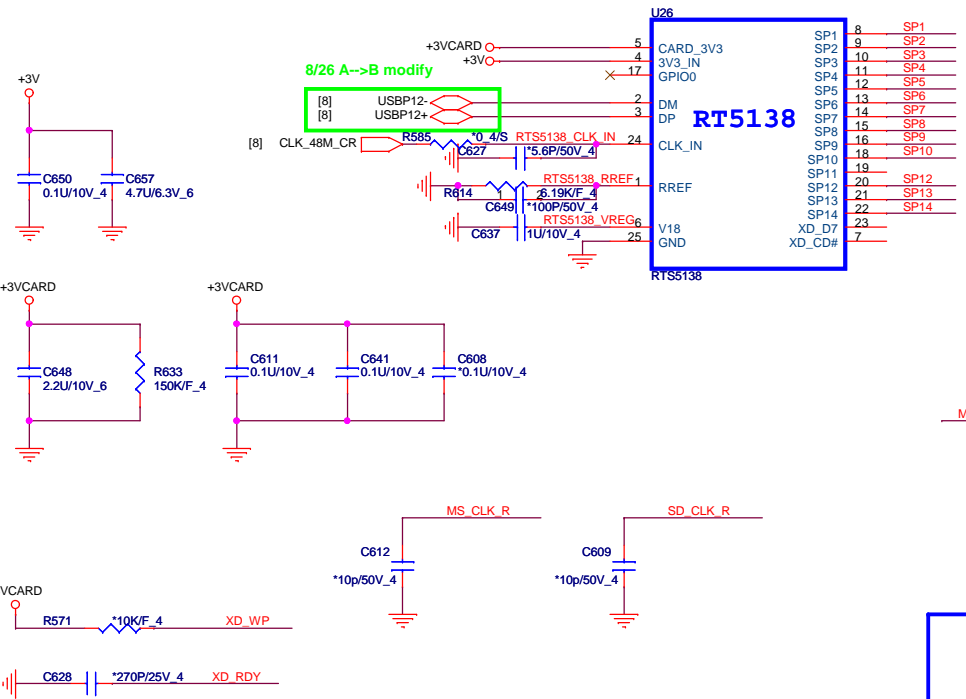
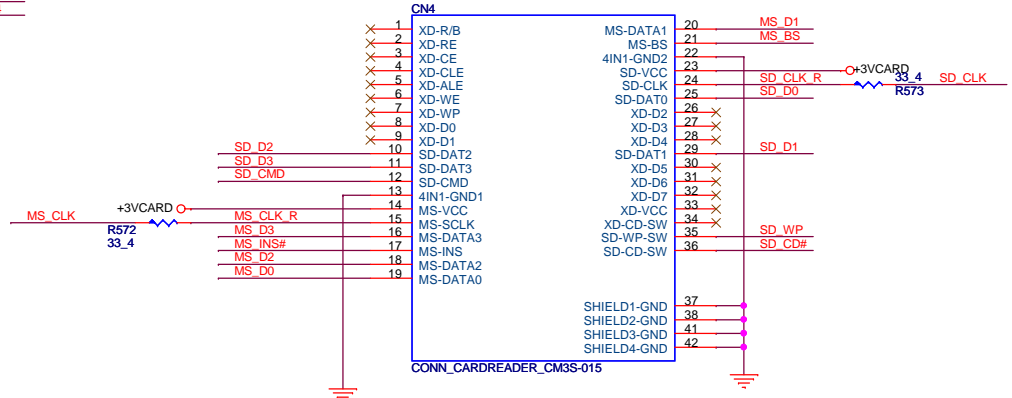


D3A: only UMA sku support 1G, If support 10/100 in UMA SKU, R55,R56 change to 0-ohm

	PROJECT : TWH		Rev A
	Quanta Computer Inc.		
	Size Custom	Document Number LAN Controller (Atheros_AR8151)	
Date: Wednesday, December 15, 2010		Sheet 24 of 40	

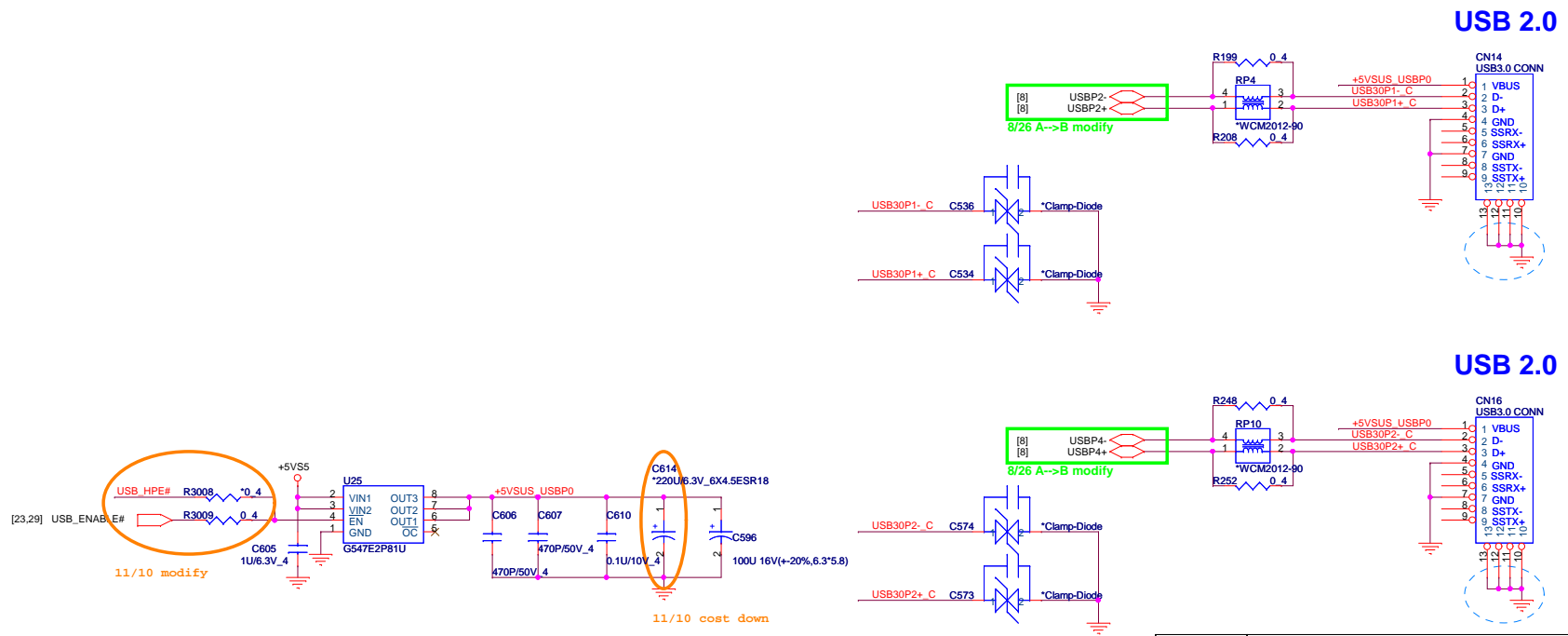
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS

Share Pin



	PROJECT : TWH		Date: Tuesday, December 14, 2010
	Quanta Computer Inc.		
	Size: Custom Document Number: Audio Codec (Realtek_ALC269)	Rev: A	
		Sheet 25 of 40	

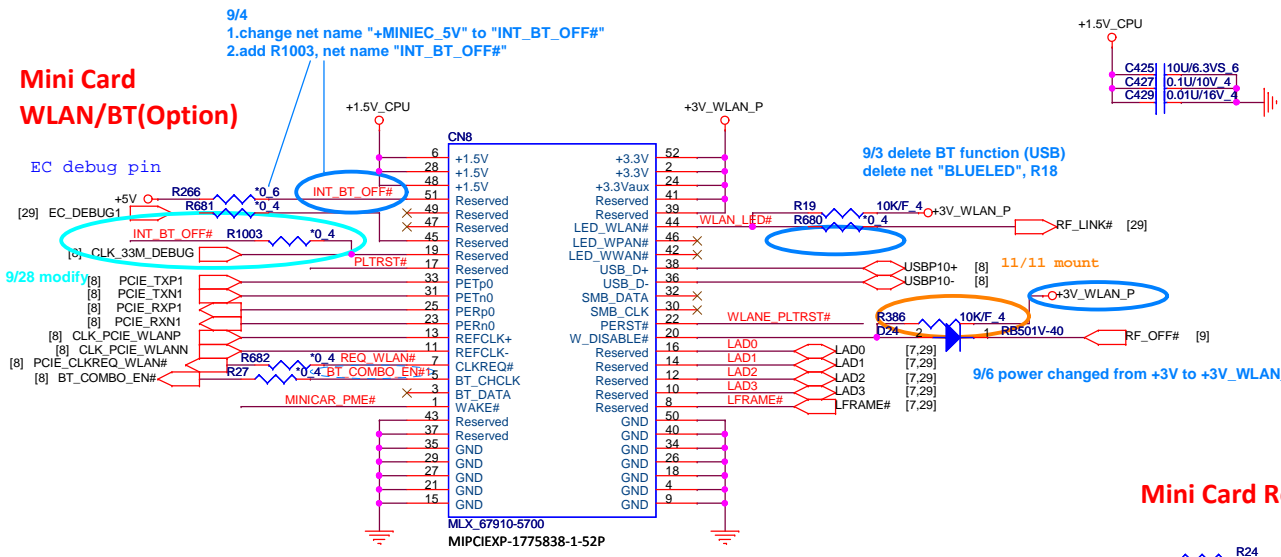
USB3.0 X 2/USB2.0 COMBO



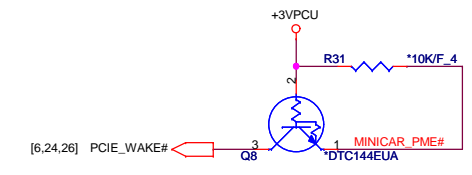
[2,6,7,8,9,10,12,13,14,21,22,23,24,25,27,28,29,34,36,37,39] +3V
 [10,21,23,31,32,33,34,35,36,37,38,39,40] +5VS5
 [36] +3VSUS
 [33] +1.1V_VL801

	PROJECT : TWH Quanta Computer Inc.		Rev A
	Size Custom	Document Number USB 3.0 Controller (T1_TUSB7320)	
		Sheet 26 of 40	

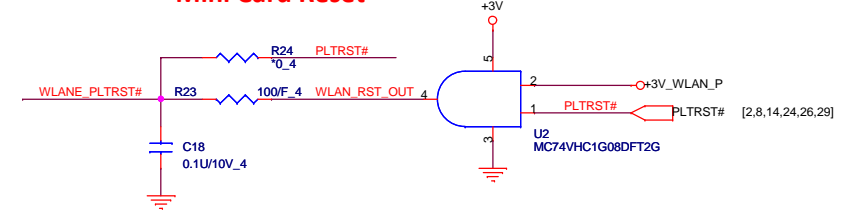
Mini Card WLAN/BT(Optional)



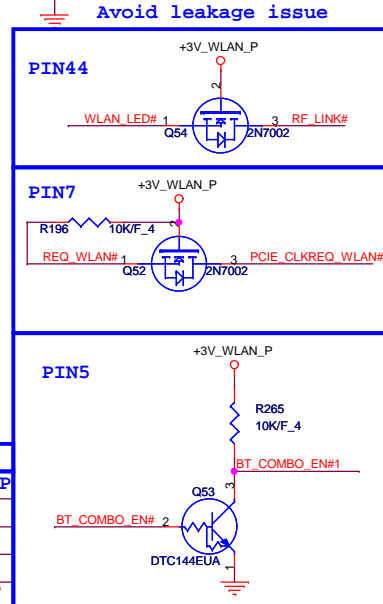
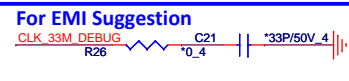
Support Wake Function(Reserve)



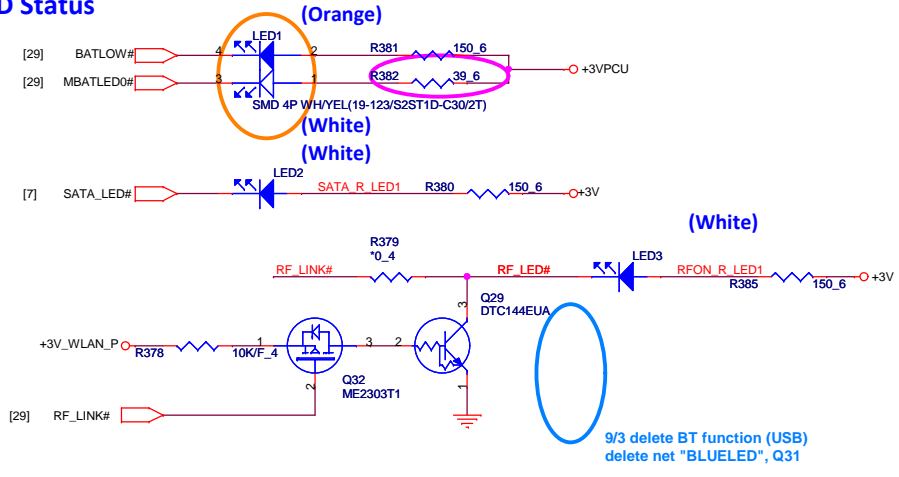
Mini Card Reset



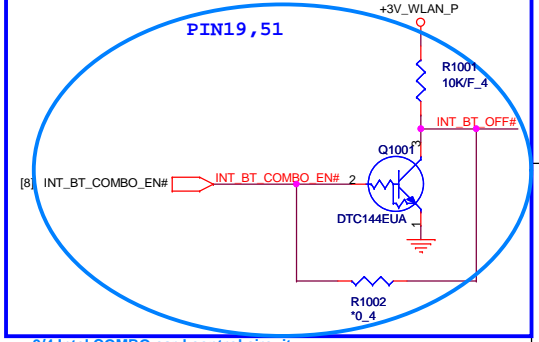
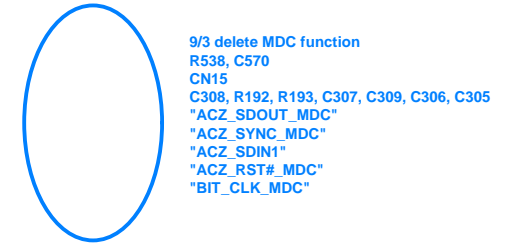
LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF



LED Status



MDC Connector(Optional)



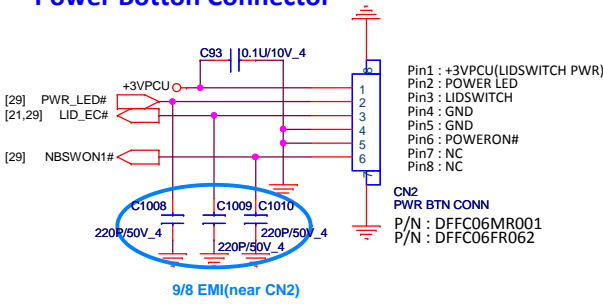
9/4 Intel COMBO card control circuit
 1.add R1001,R1002,Q1001
 2.add net name "INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

NB5

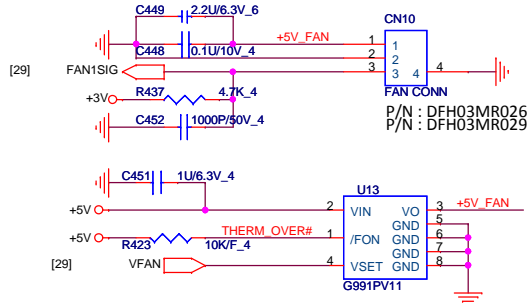
PROJECT : TWH
Quanta Computer Inc.

Size Custom	Document Number Audio Codec (Realtek_ALC269)	Rev A
Date: Tuesday, December 14, 2010		Sheet 27 of 40

Power Button Connector

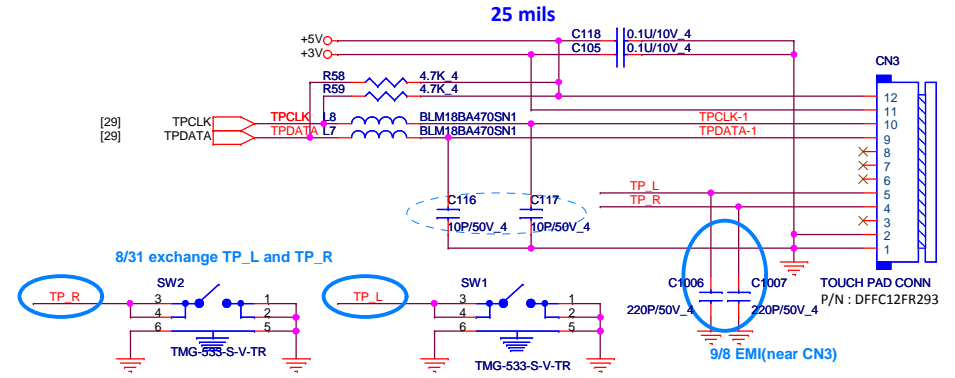


CPU FAN

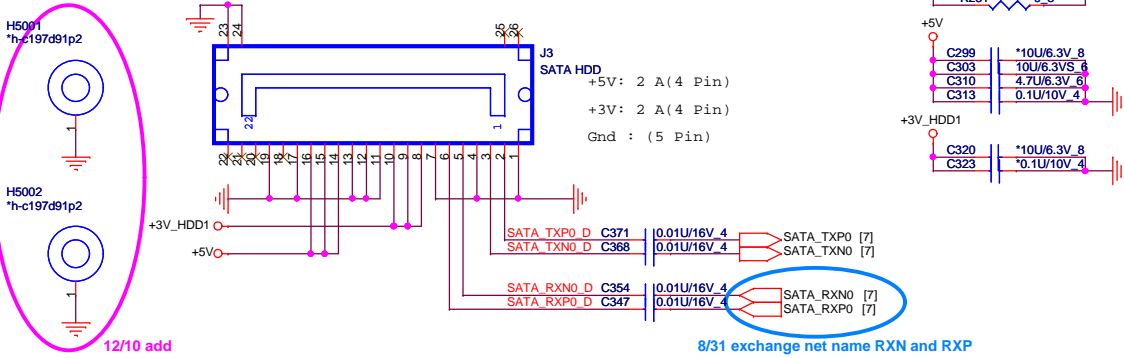


Touch Pad Connector

B-stage change footprint to BL121-12R-TAND-12P-L



SATA HDD Connector

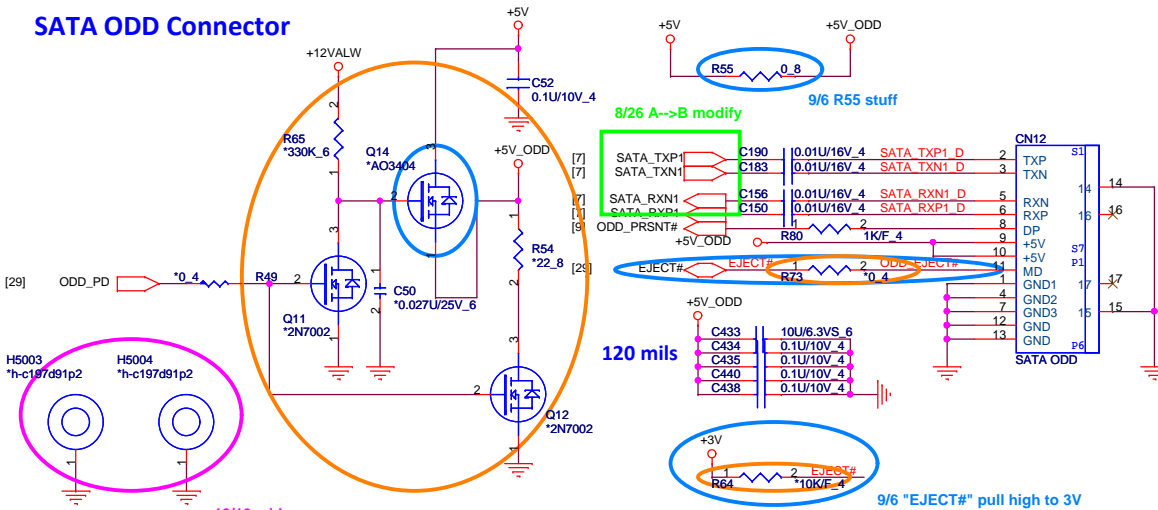


BT Connector

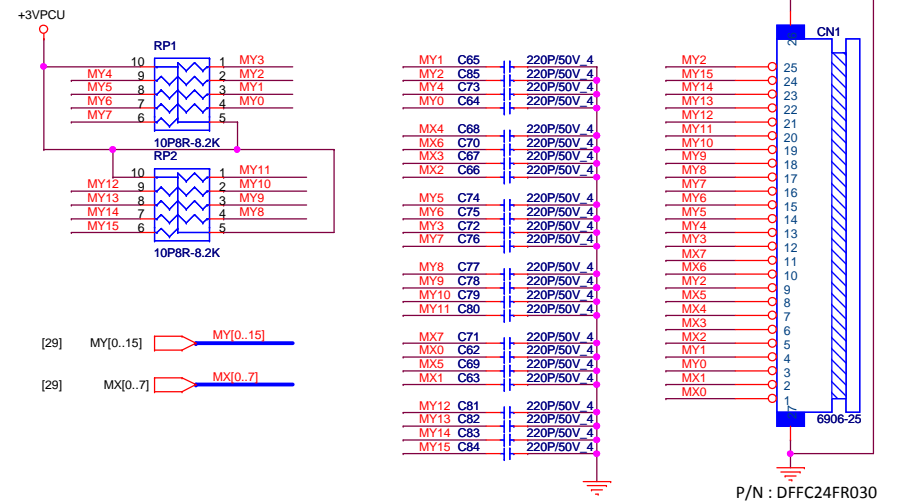


8/31 delete BT function (USB)
 delete CN20, net "BT_OFF#", "BLUELED", "USB8+", "USB8-"

SATA ODD Connector



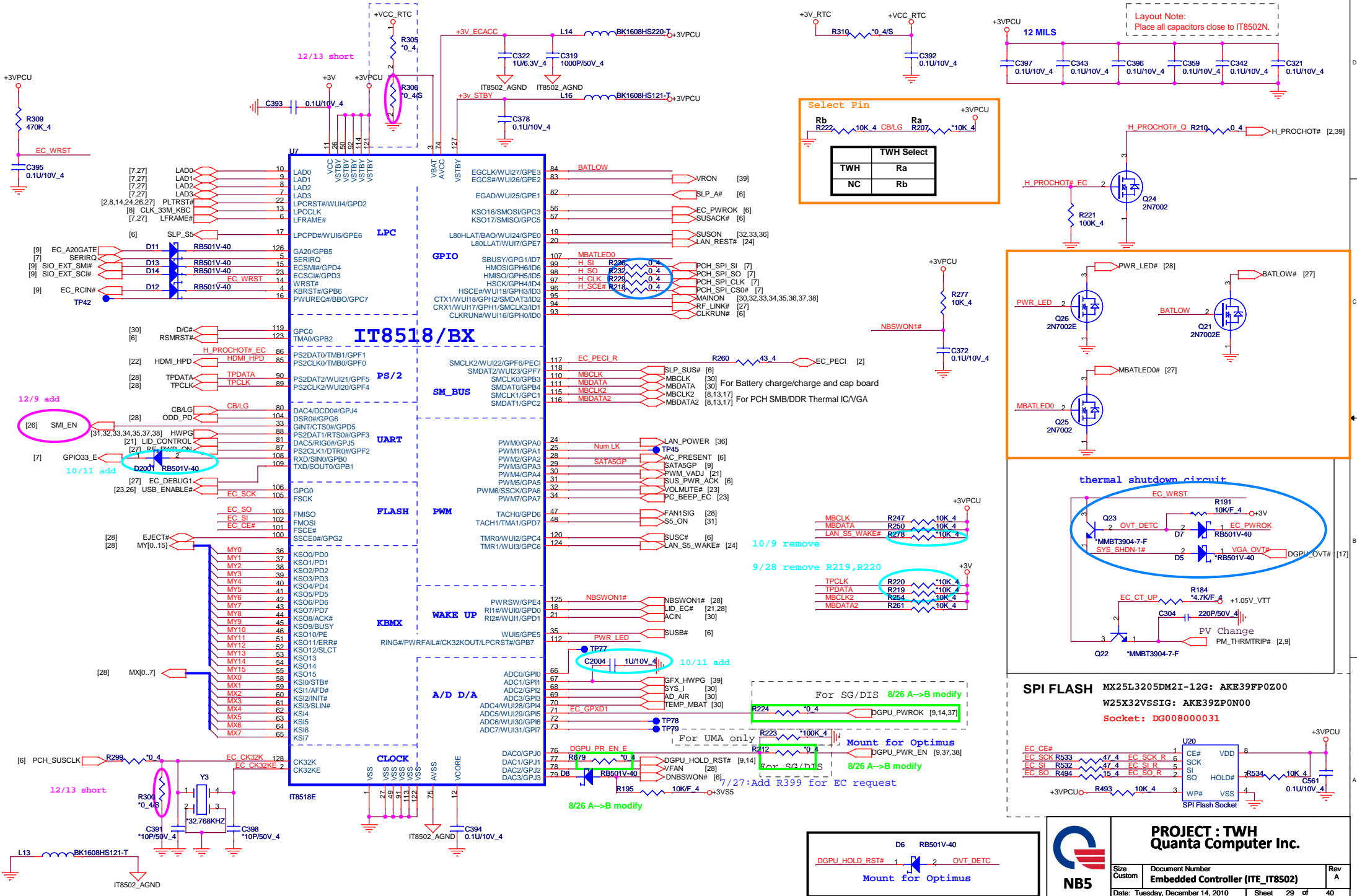
Keyboard Connector



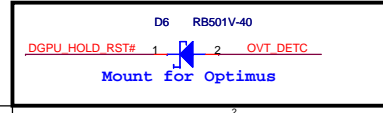
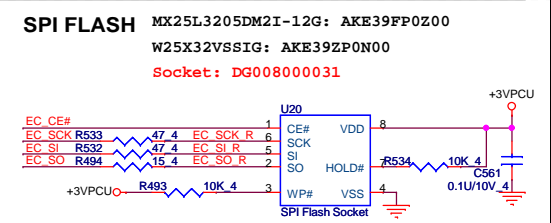
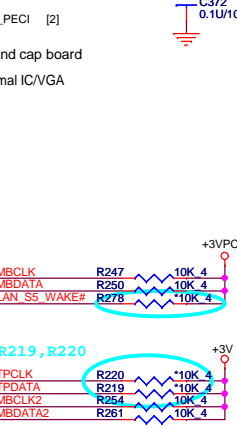
PROJECT : TWH
Quanta Computer Inc.

Size Custom	Document Number Audio Codec (Realtek_ALC269)	Rev A
Date: Tuesday, December 14, 2010		Sheet 28 of 40

[2,4,10,27] +1.5V_CPU
 [6,7,8,9,10,12,13,14,21,22,23,24,25,26,27,28,34,36,37,39] +3V
 [6,7,10,21,22,23,27,36] +5V



Rb R222	10K 4	CB/LG	Ra R207	10K 4
TWHL		TWHL Select		
NC				



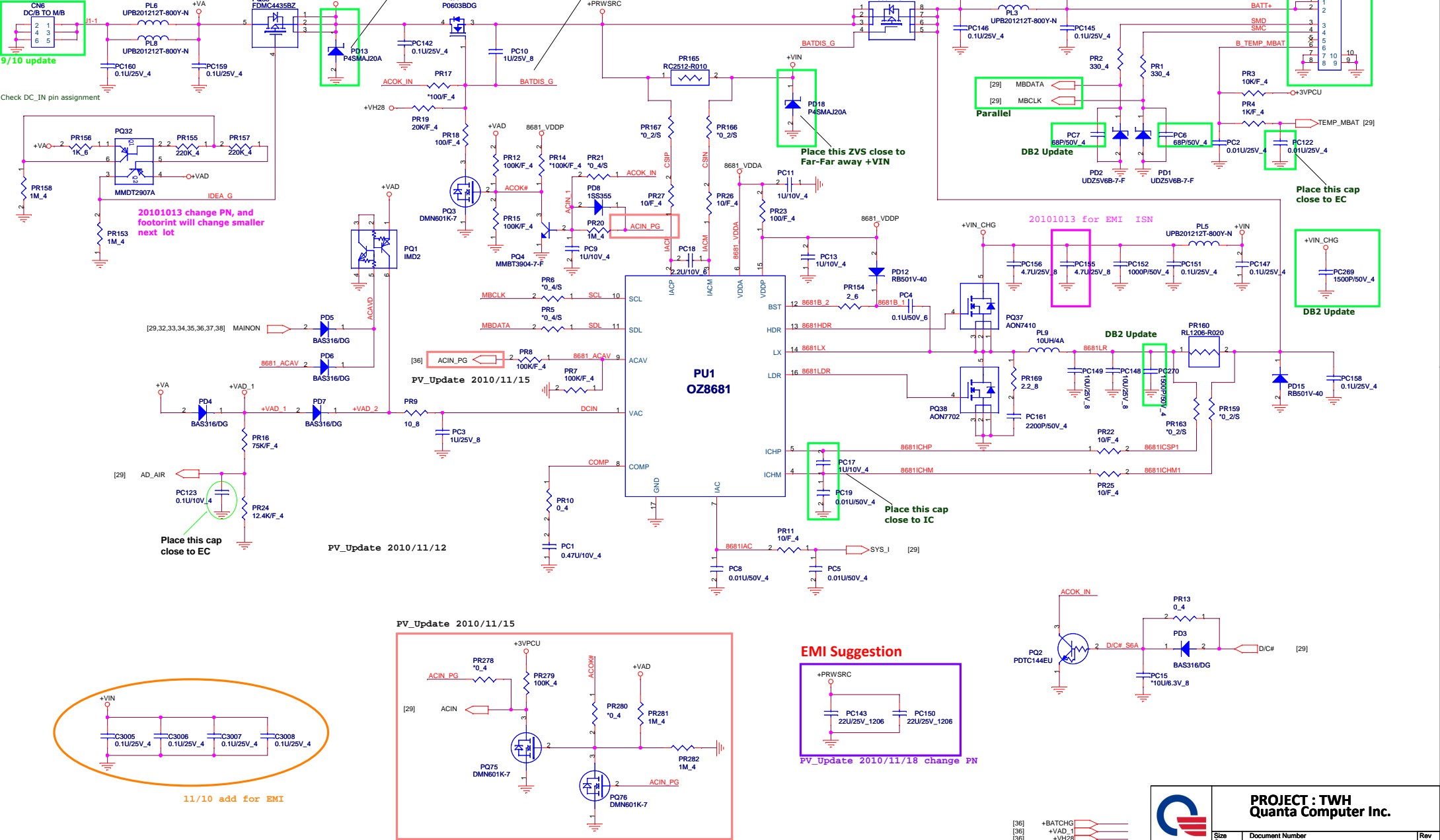
PROJECT : TWH
Quanta Computer Inc.

NBS

Size Custom Document Number Embedded Controller (ITE_IT8502) Rev A

Date: Tuesday, December 14, 2010 Sheet 29 of 40

TOP DC_JACK
65W/90W



+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

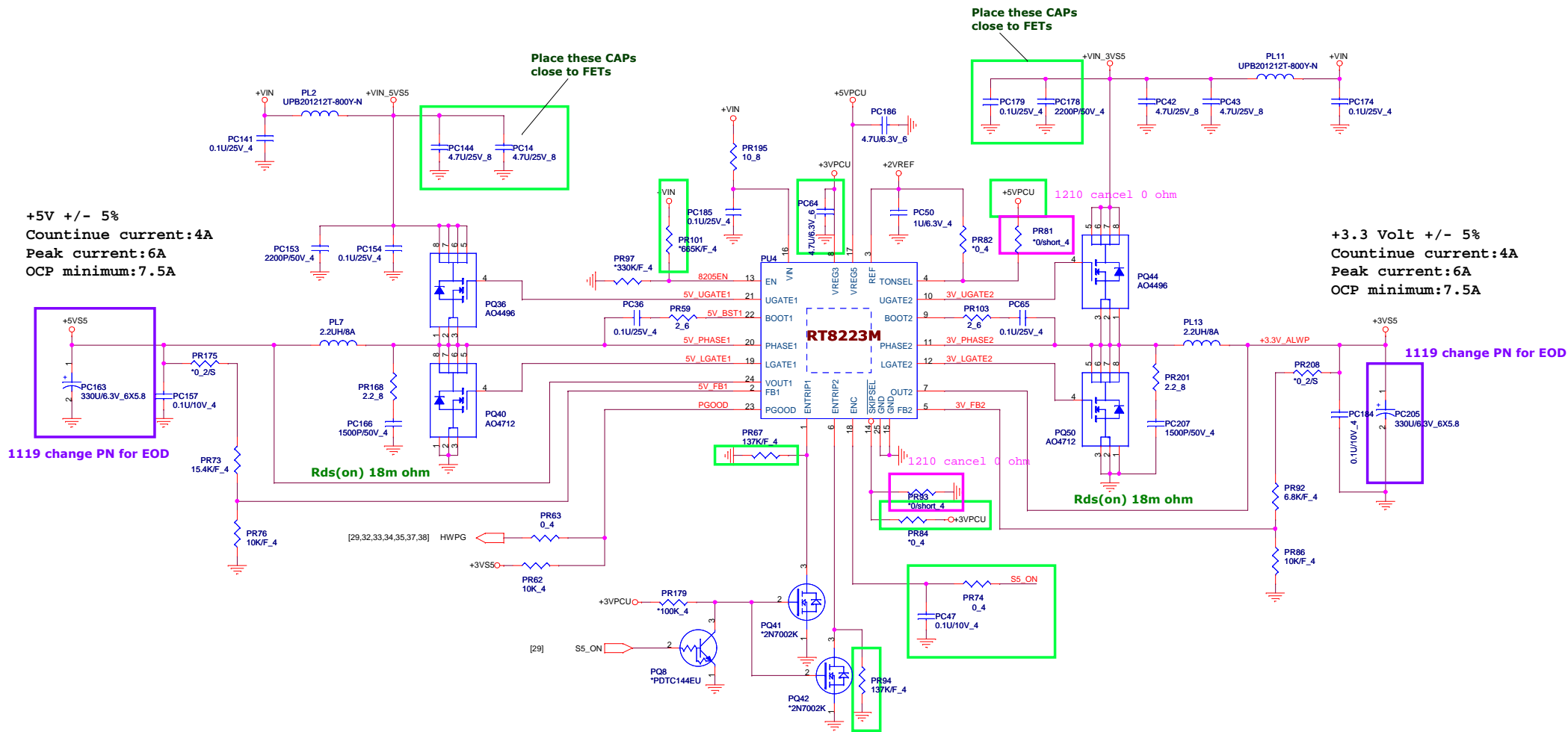
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A


1119 change PN for EOD

Rds(on) 18m ohm

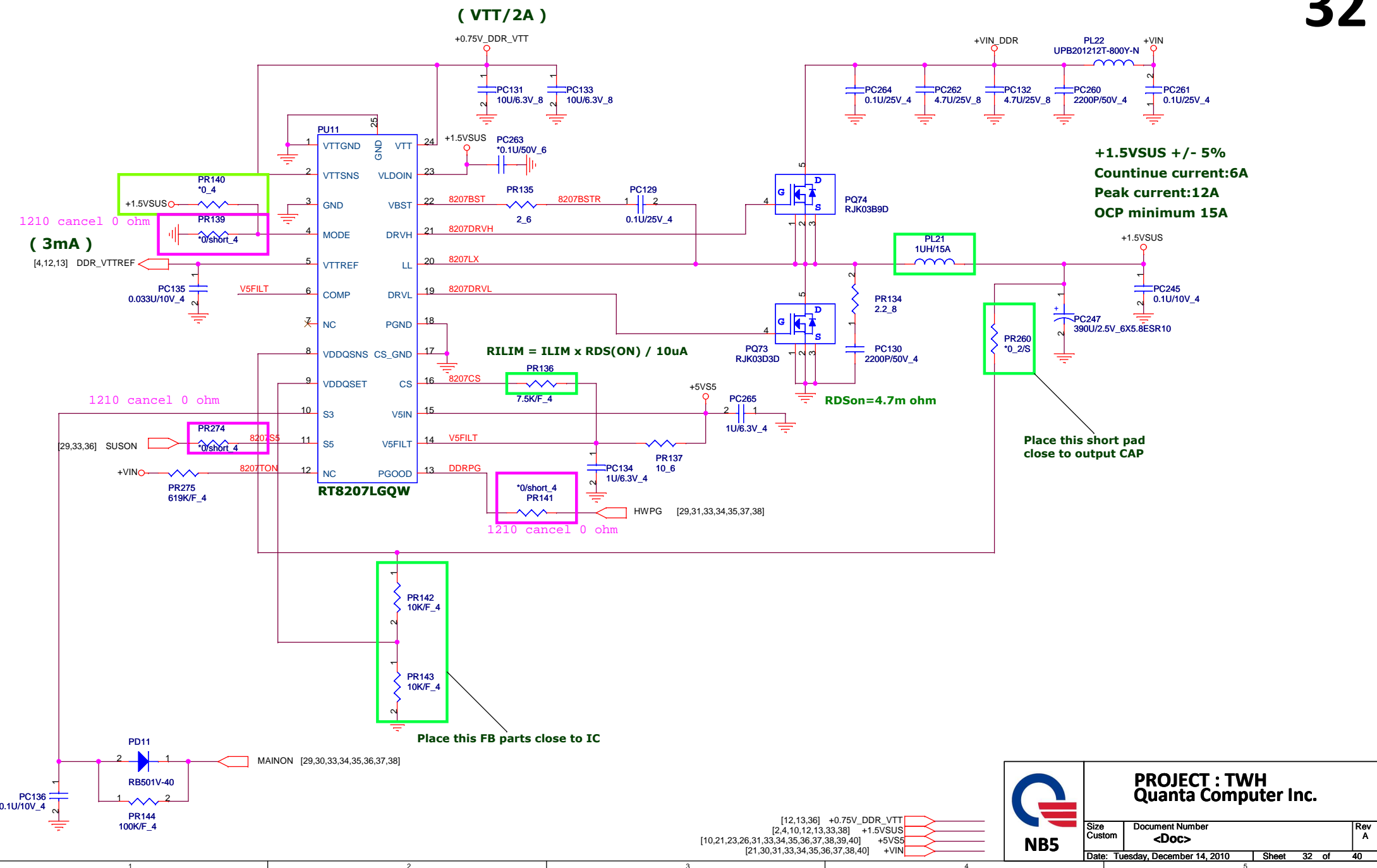
Rds(on) 18m ohm

1119 change PN for EOD



	PROJECT : TWH Quanta Computer Inc.		
	Size Custom	Document Number <Doc>	Rev A
	Date: Tuesday, December 14, 2010	Sheet 31 of 40	

+5VPCU



(VTT/2A)

+0.75V_DDR_VTT

**+1.5VSUS +/- 5%
Continue current:6A
Peak current:12A
OCP minimum 15A**

(3mA)

$$RILIM = ILIM \times RDS(ON) / 10\mu A$$

RDSon=4.7m ohm

Place this FB parts close to IC

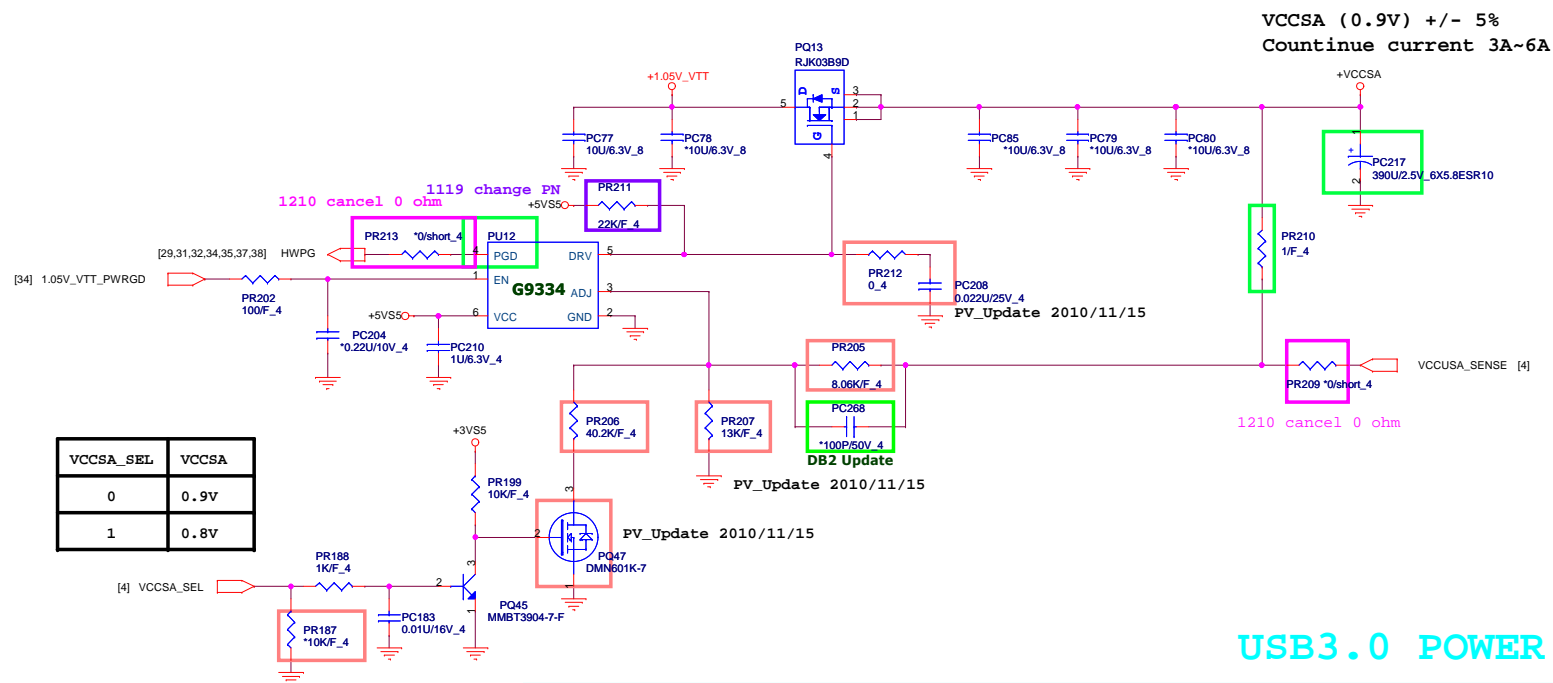
Place this short pad close to output CAP

[12,13,36]	+0.75V_DDR_VTT	
[2,4,10,12,13,33,38]	+1.5VSUS	
[10,21,23,26,31,33,34,35,36,37,38,39,40]	+5VS5	
[21,30,31,33,34,35,36,37,38,40]	+VIN	

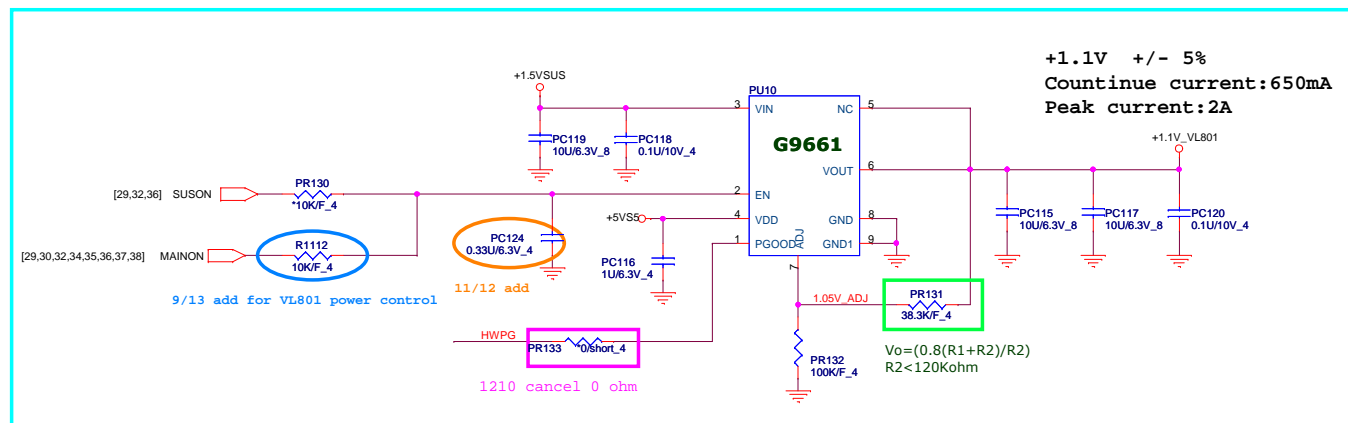
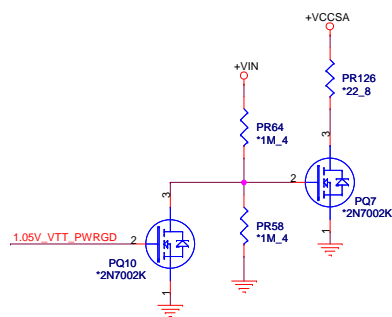


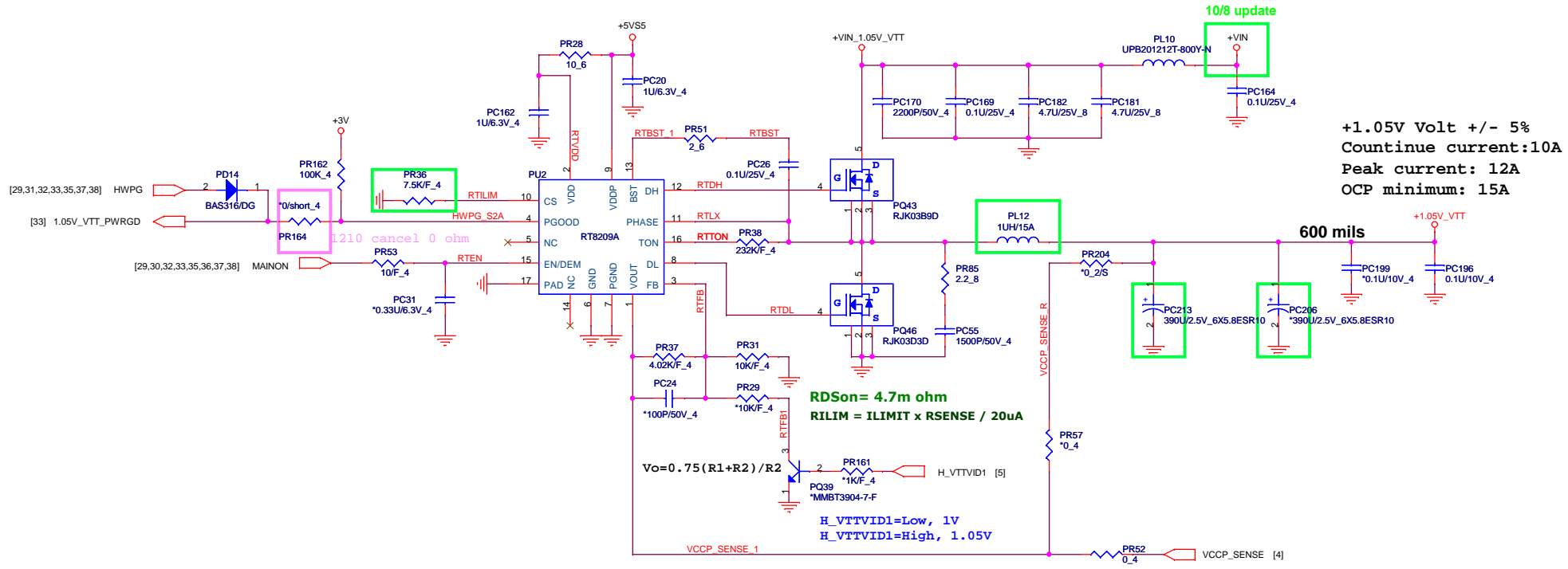
**PROJECT : TWH
Quanta Computer Inc.**

Size Custom	Document Number <Doc>	Rev A
Date: Tuesday, December 14, 2010	Sheet 32 of 40	



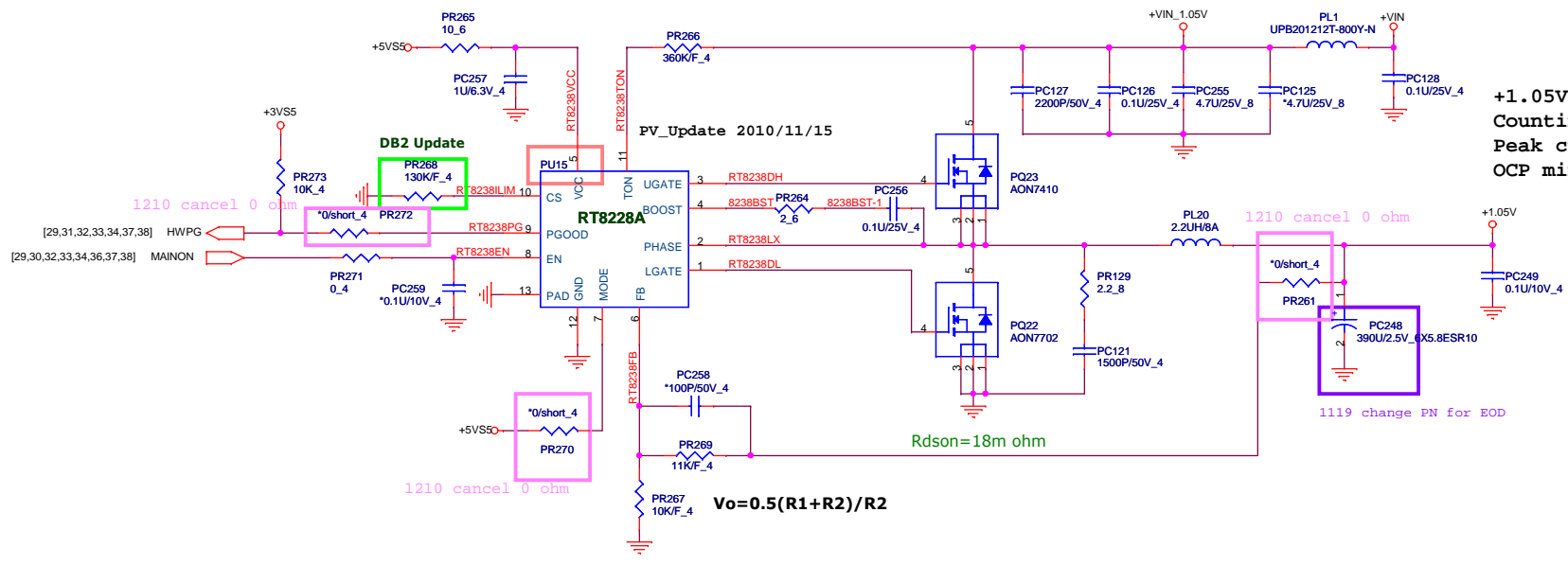
USB3.0 POWER





PROJECT : TWH
Quanta Computer Inc.

Size Custom	Document Number <Doc>	Rev A
Date: Tuesday, December 14, 2010	Sheet 34 of 40	



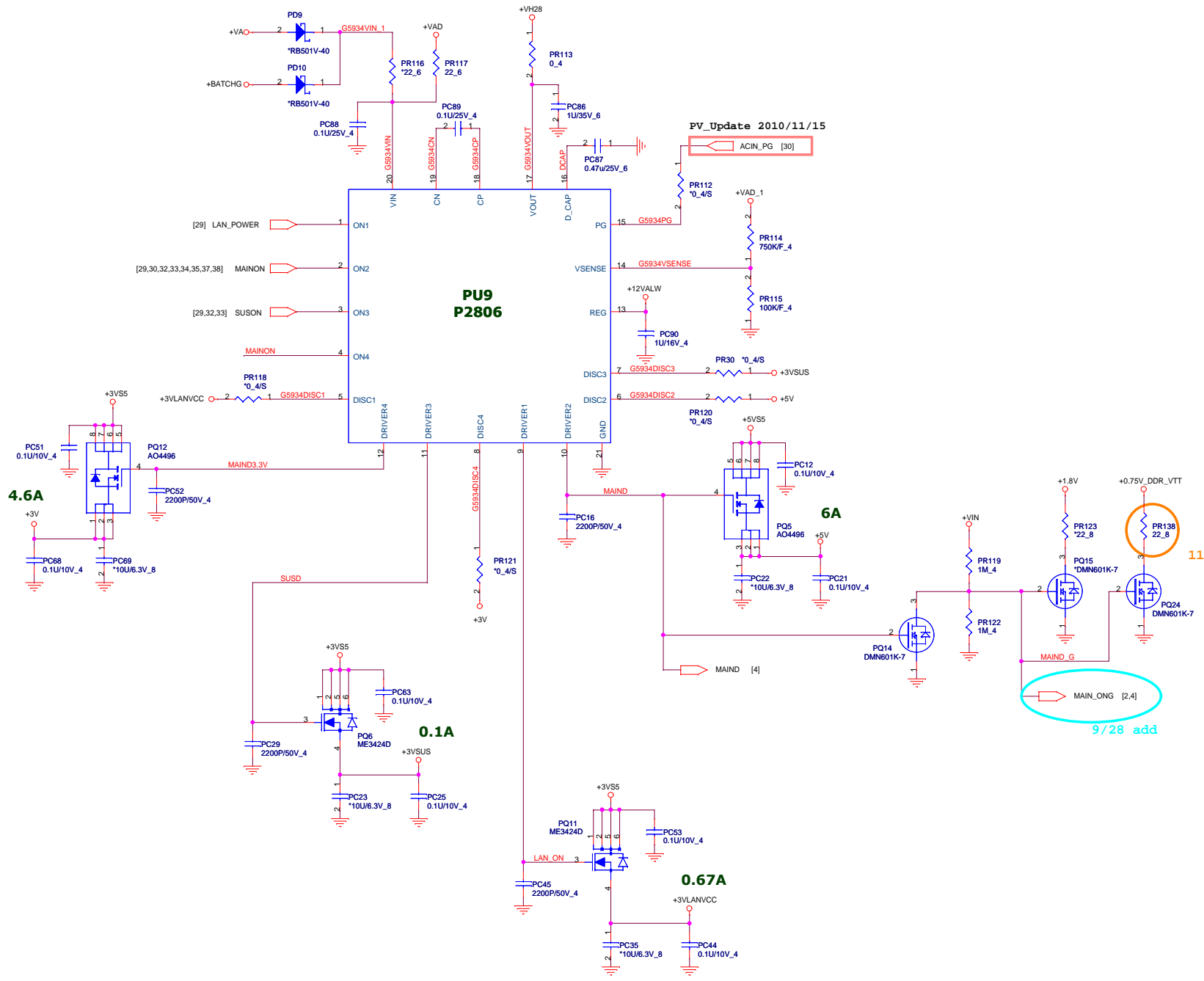
+1.05V +/- 5%
Countinue current:6A
Peak current: 8A
OCP minimum: 10A

$V_o = 0.5(R_1 + R_2) / R_2$




PROJECT : TWH
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Size Custom	Document Number <Doc>	Rev A
Date: Tuesday, December 14, 2010		Sheet 35 of 40



[12,13,32]	+0.75V_DDR_VTT
[24]	+3VLAVCC
[2,4,10,12,13,32,33,38]	+1.5VSUS
[30]	+BATCHG
[21,28,38]	+12VALW
[10,21,23,26,31,32,33,34,35,37,38,39,40]	+5VS5
[2,6,7,8,9,10,14,24,29,31,33,35,38]	+3VS5
[30]	+VAD_1
[30]	+VH28
[4,7,10,38]	+1.8V
[21,30,31,32,33,34,35,37,38,40]	+VIN
[6,7,10,21,22,23,27,28]	+5V
[30]	+VA



NBS

**PROJECT : TWH
Quanta Computer Inc.**

Size Custom	Document Number <Doc>	Rev A
Date: Tuesday, December 14, 2010		Sheet 36 of 40

ciucit default is N12P

VGA type	PQ17 PQ19 PQ16 PQ18	PR252
N12E	POP(SMT)	1.37K
N12P	NA(no SMT)	806 ohm (CS18062FB29)

Nvideo N12E

CNTRL1	CNTRL0	N11E-GE
GPI06	GPI05	
0	0	0.9125V
0	1	0.8625V
1	0	0.8125V
1	1	N/A

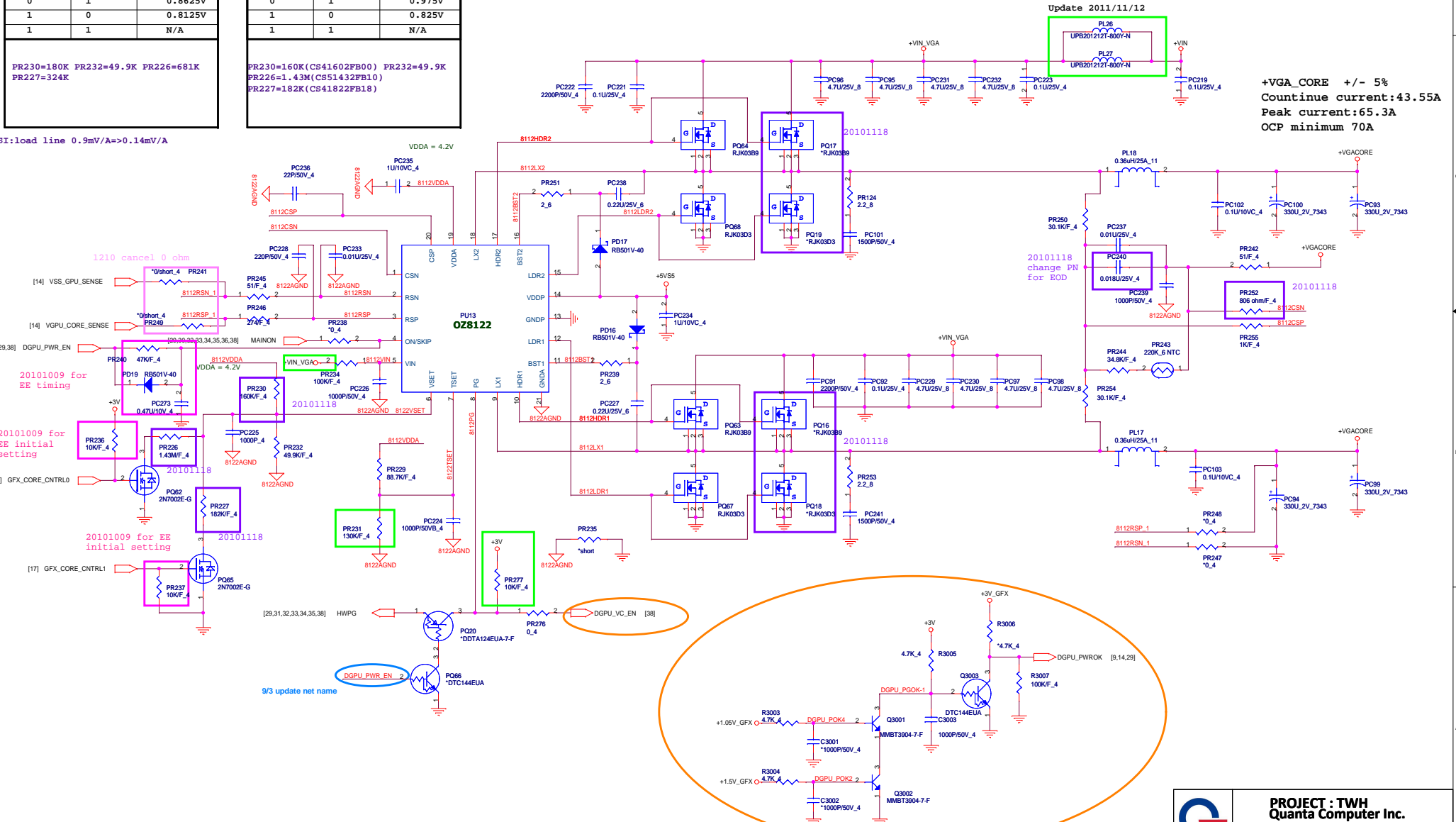
PR230=180K PR232=49.9K PR226=681K
PR227=324K

Nvideo N12P

CNTRL1	CNTRL0	N11E-GE
GPI06	GPI05	
0	0	1V
0	1	0.975V
1	0	0.825V
1	1	N/A

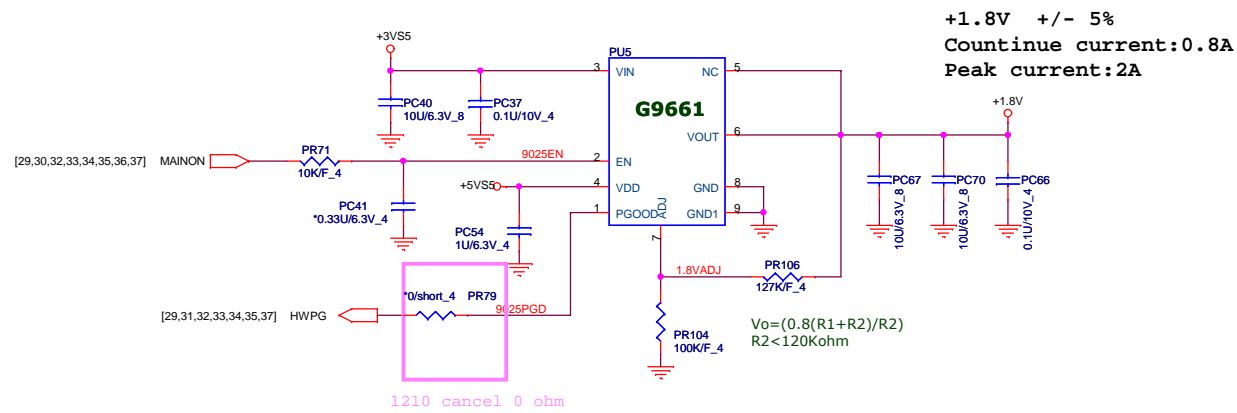
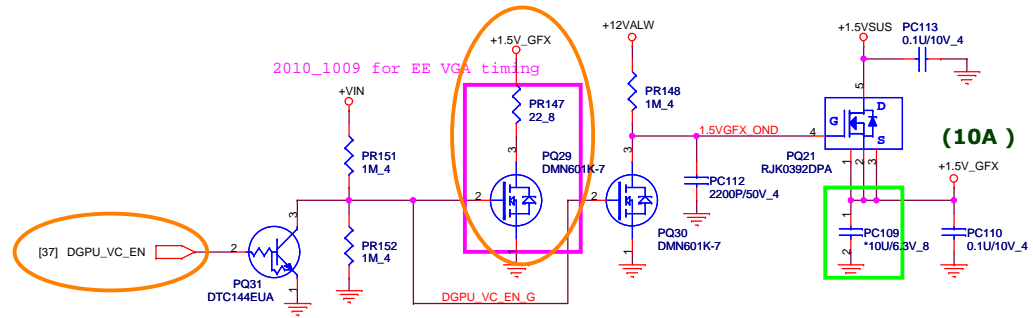
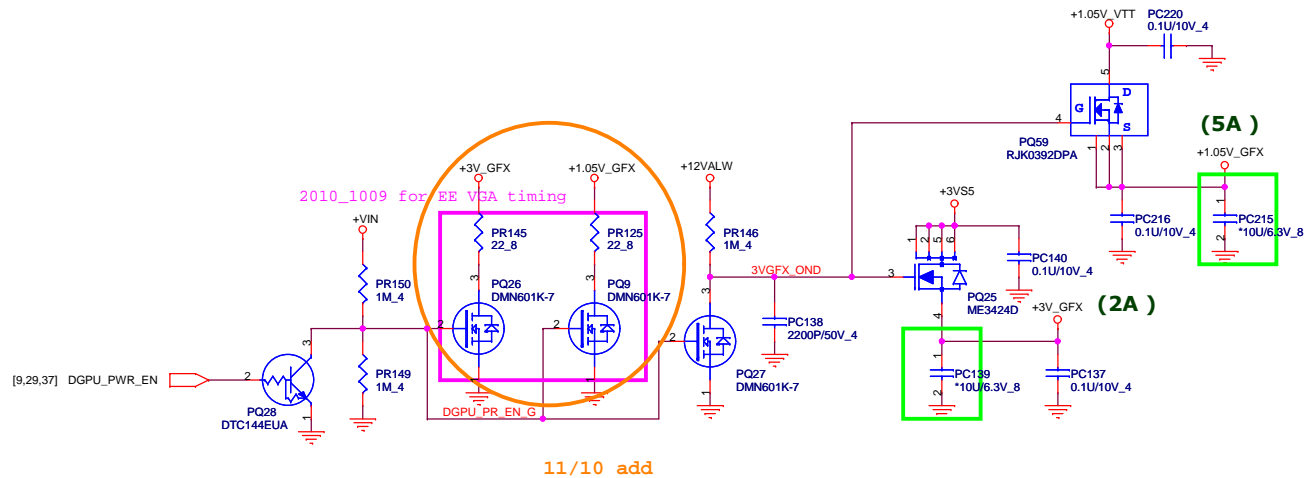
PR230=160K(CS41602FB00) PR232=49.9K
PR226=1.43M(CS51432FB10)
PR227=182K(CS41822FB18)

SI:load line 0.9mV/A=>0.14mV/A

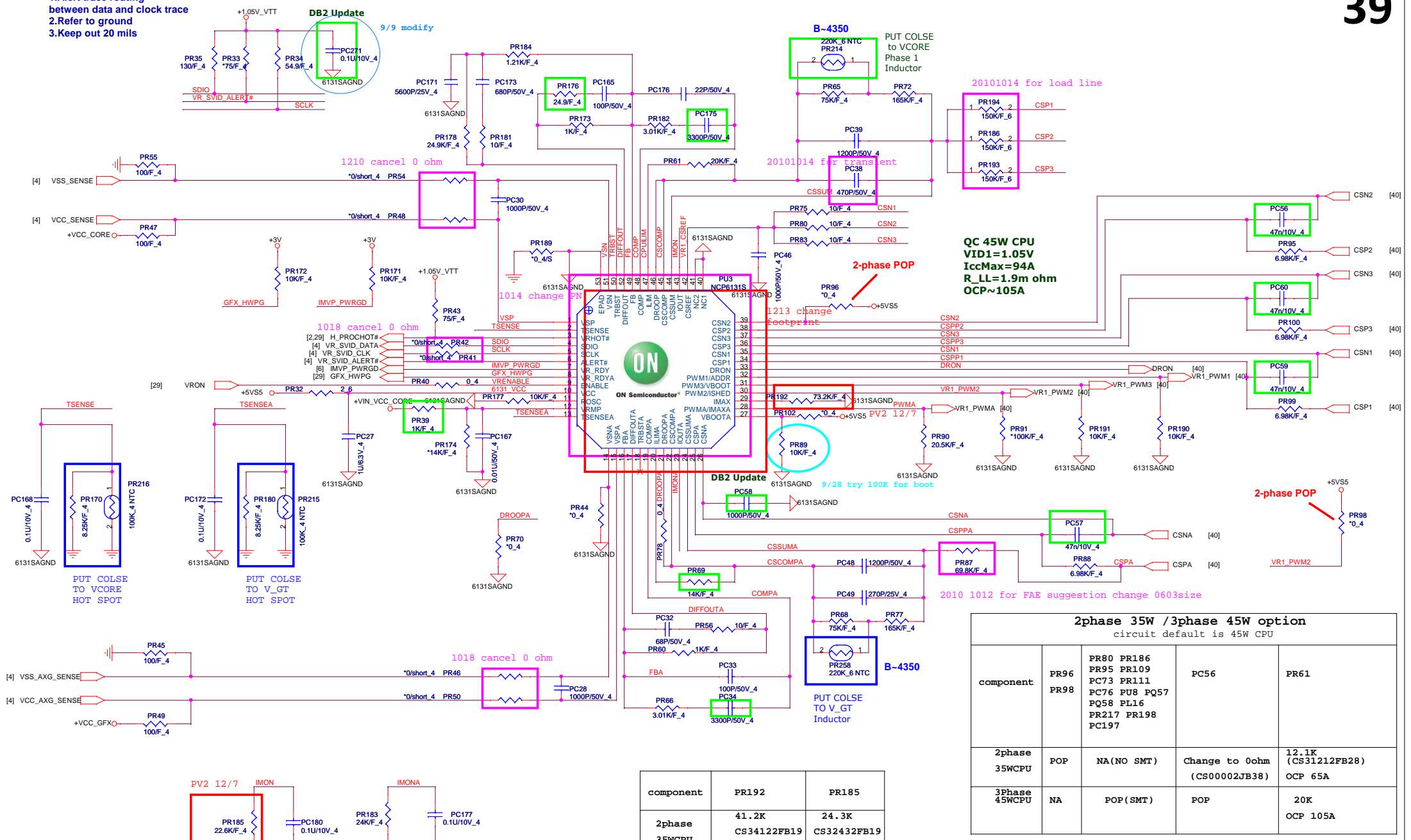


+VGA_CORE +/- 5%
Continue current:43.55A
Peak current:65.3A
OCP minimum 70A

11/10 add for DGPU_PWROK circuit



- Alert trace routing between data and clock trace
- Refer to ground
- Keep out 20 mils



2phase 35W /3phase 45W option
circuit default is 45W CPU

component	PR96 PR98	PR80 PR186 PR95 PR109 PC73 PR111 PC76 PU8 PQ57 PQ58 PL16 PR217 PR198 PC197	PC56	PR61
2phase 35WCPU	POP	NA(NO SMT)	Change to 0ohm (CS00002JB38)	12.1K (CS31212FB28) OCP 65A
3Phase 45WCPU	NA	POP(SMT)	POP	20K OCP 105A

component	PR192	PR185
2phase 35WCPU	41.2K CS34122FB19	24.3K CS32432FB19
3Phase 45WCPU	73.2K CS37322BB00	22.6K CS32262FB15

PROJECT : TWH
Quanta Computer Inc.

NBS

Size Custom Document Number <Doc> Rev A

Date: Tuesday, December 14, 2010 Sheet 39 of 40

