

UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :NotInstalled

UMA:UMA platform installed

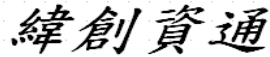
OPS:Optimus

HR:Huron River

CR:Chief River

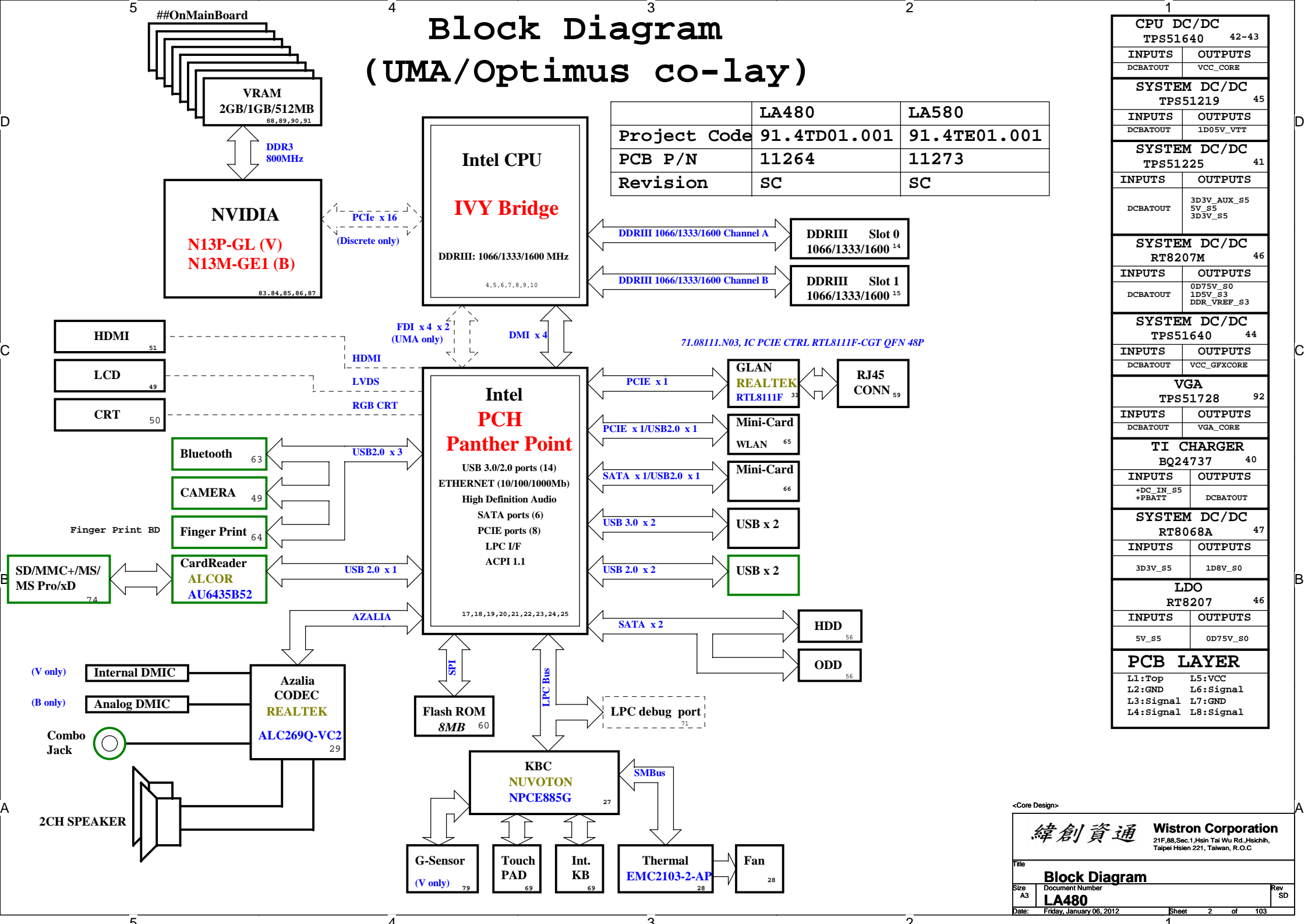
V: V-Series installed

<Core Design>

		Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C
Title		
Cover Page		
Size A4	Document Number LA480	Rev SD
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Block Diagram (UMA/Optimus co-lay)

	LA480	LA580
Project Code	91.4TD01.001	91.4TE01.001
PCB P/N	11264	11273
Revision	SC	SC



CPU DC/DC TPS51640 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC TPS51219 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC TPS51225 41	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC RT8207M 46	
INPUTS	OUTPUTS
DCBATOUT	0D75V_S0 1D5V_S3 DDR_VREF_S3
SYSTEM DC/DC TPS51640 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
VGA TPS51728 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
TI CHARGER BQ24737 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT
SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
LDO RT8207 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0
PCB LAYER	
L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

<Core Design>

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File: **Block Diagram**

Size: A3 Document Number: **LA480** Rev: SD

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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

USB Table port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3		ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN		ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I 2 C / SMBus Addresses	Ref Des	Chief River CRV		
		Address	Hex	Bus
Device				
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Core Design>

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SSID = CPU

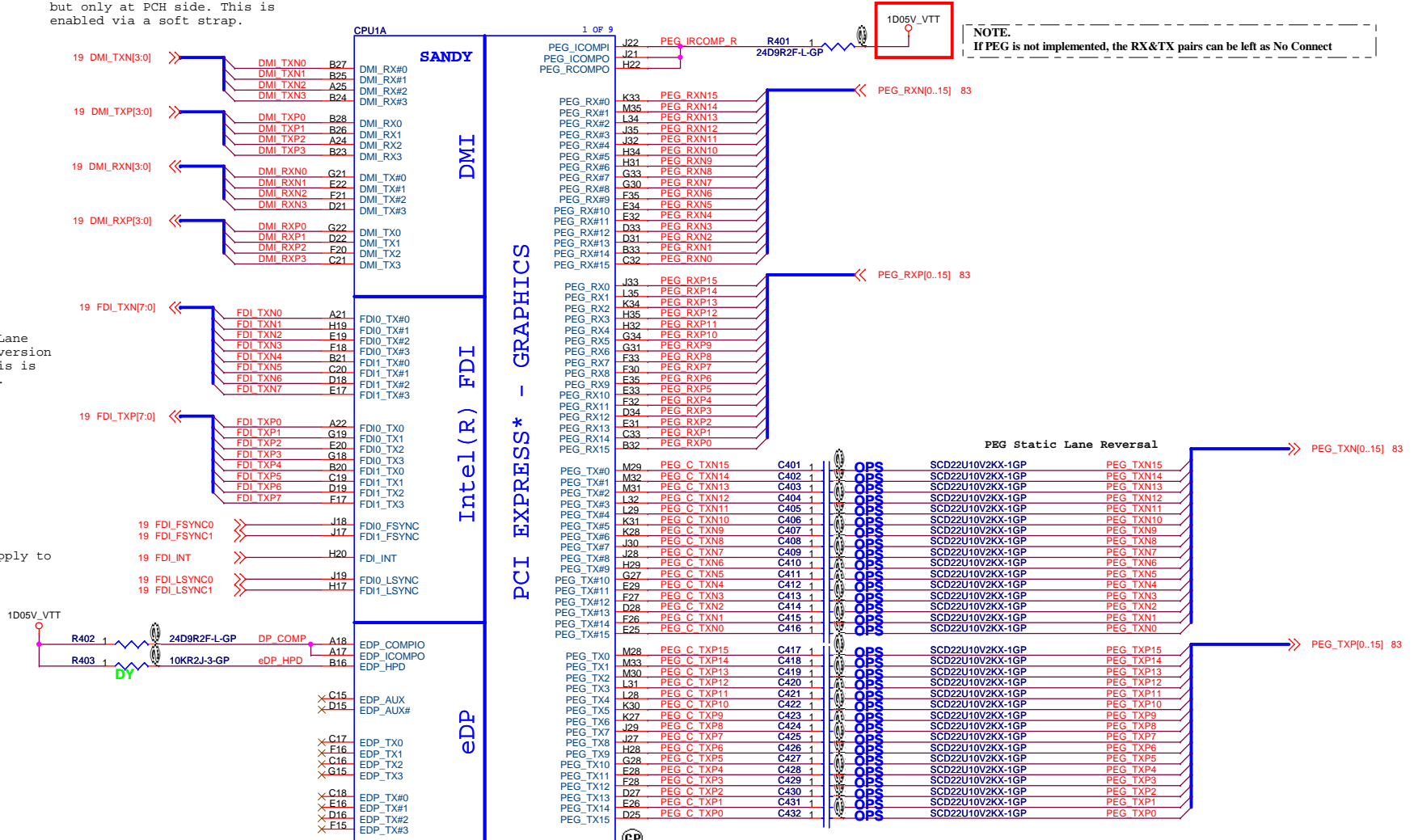
01.001VY.000 IVY BRIDGE ORCAD SYMBOL.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.



NOTE:
If PEG is not implemented, the RX&TX pairs can be left as No Connect

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

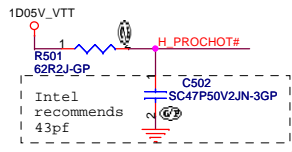
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

<Core Design>

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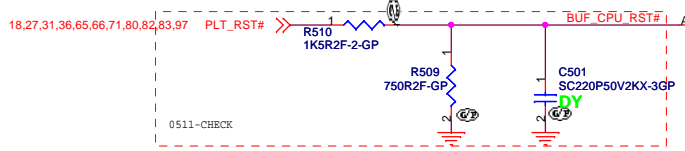
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Size A3 Document Number LA480 Rev SD
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SSID = CPU

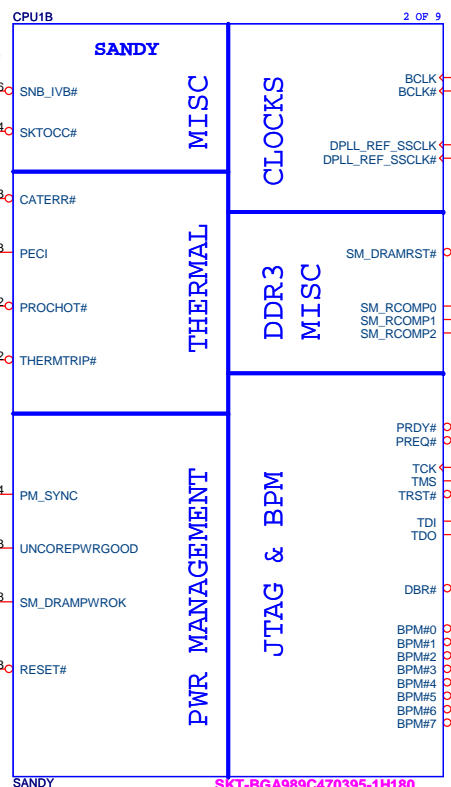


Connect EC to PROCHOT# through inverting OD buffer.

If PROCHOT# is not used, then it must be terminated with a 68ohm ±5% pull-up resistor to VTT.

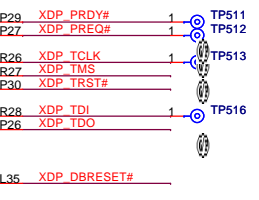
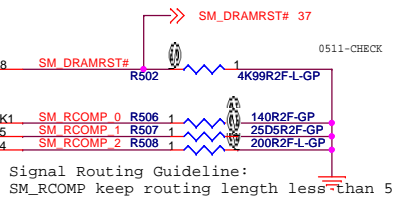
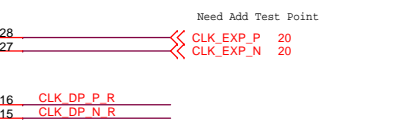


- DEL U501
- DEL R519
- DEL C503
- DEL R517
- DEL R515
- ASM R510
- ASM R509

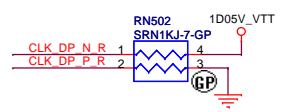


SANDY
62.10055.421
2nd = 62.10040.771

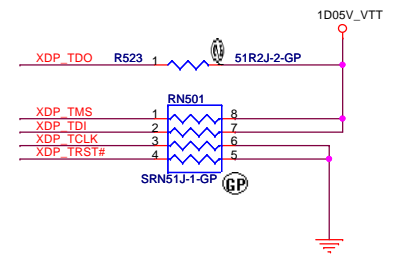
SKT-BGA989C470395-1H180



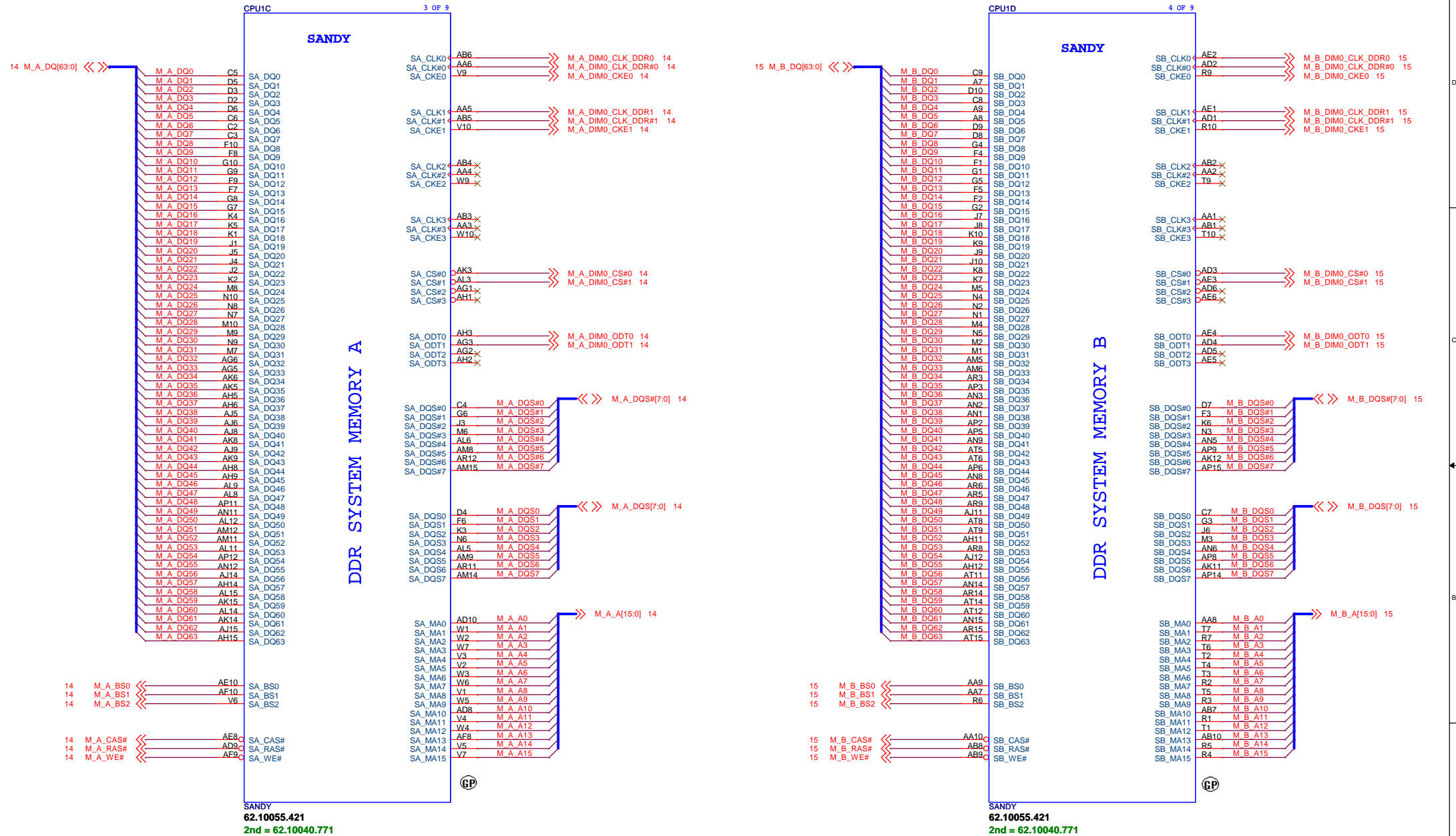
Disabling SDRAM:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor power (~15 mW) may be wasted.



In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils wide trace for routing less than 500 mils, or 20-mils wide trace for routing between 500 mils and 1000 mils. Keep 20-mils spacing to any other signals in order to minimize crosstalk.



SSID = CPU



SANDY
62.10055.421
2nd = 62.10040.771

SANDY
62.10055.421
2nd = 62.10040.771

<Core Design>

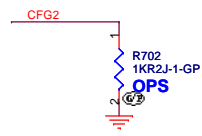
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Title: **CPU (DDR)**

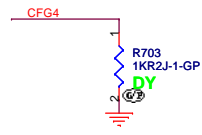
Size A3 Document Number **LA480** Rev SD

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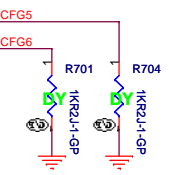
SSID = CPU



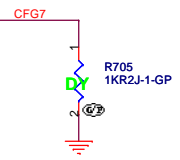
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



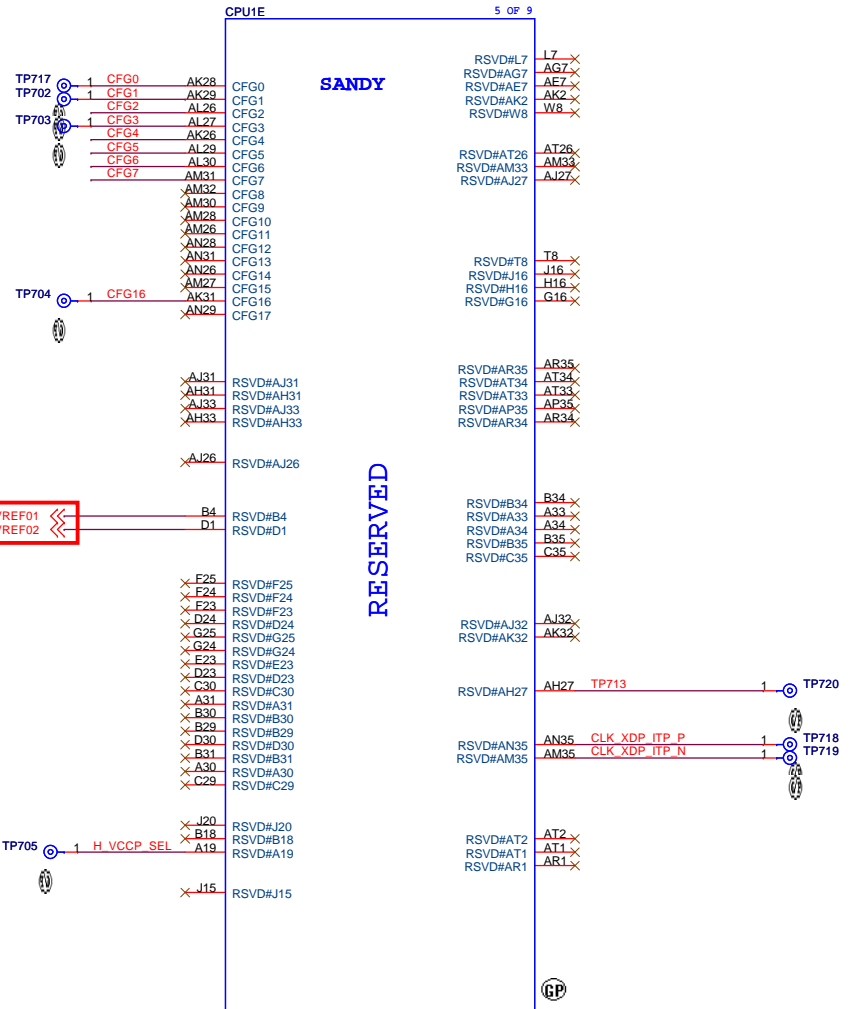
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



12 DDR_WR_VREF01
12 DDR_WR_VREF02

RESERVED

SANDY SKT-BGA989C470395-1H180
62.10055.421
2nd = 62.10040.771

<Core Design>

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Title: **CPU (RESERVED)**

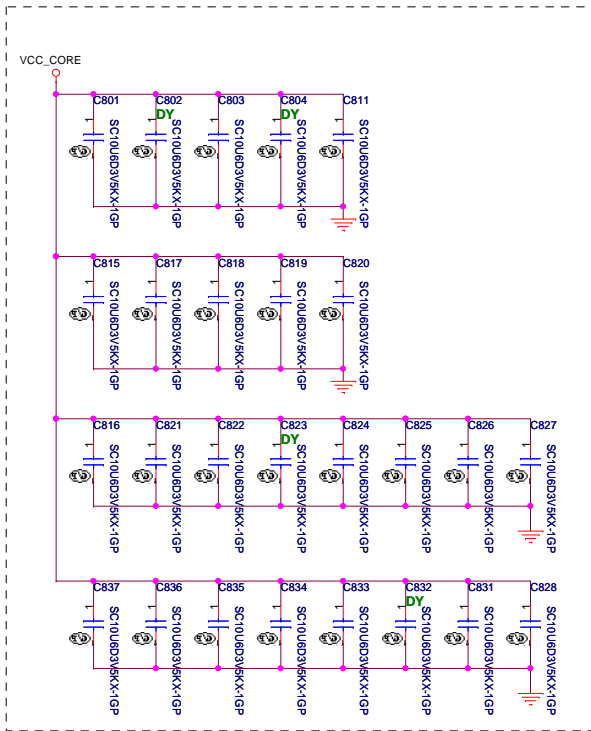
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POWER

VCC CORE: 5.3A

VCCIO: 8.5A



VCC_CORE

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
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- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

SANDY

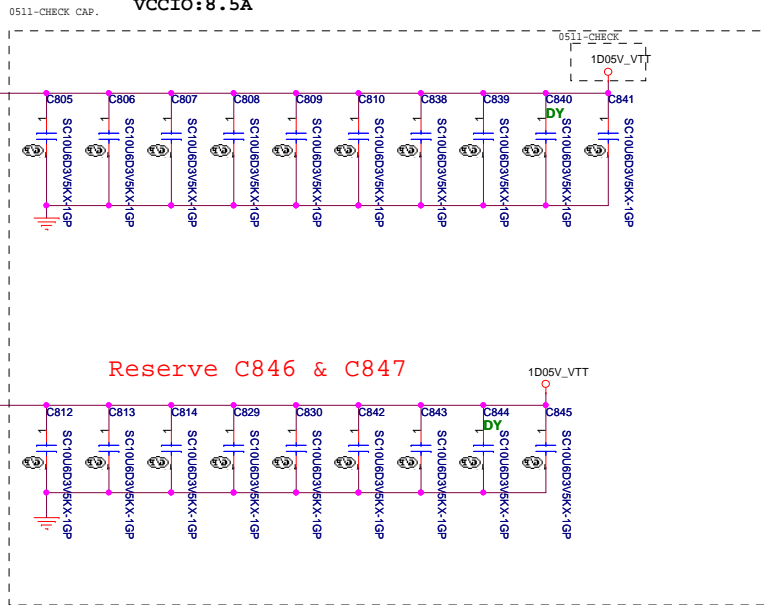
CORE SUPPLY

PEG AND DDR

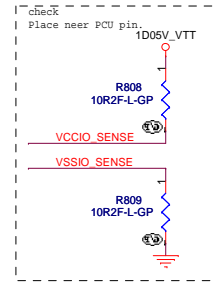
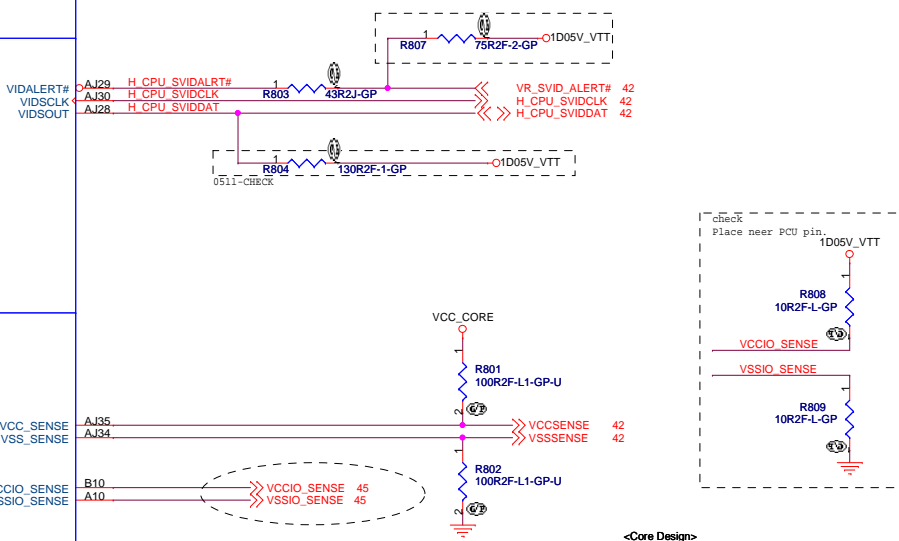
SVID

SENSE LINES

- VCCIO AH13
- VCCIO AH10
- VCCIO AG10
- VCCIO Y10
- VCCIO L10
- VCCIO P10
- VCCIO L14
- VCCIO J13
- VCCIO J12
- VCCIO H14
- VCCIO H12
- VCCIO H11
- VCCIO G14
- VCCIO G13
- VCCIO F14
- VCCIO F13
- VCCIO F12
- VCCIO E11
- VCCIO E14
- VCCIO E12
- VCCIO E11
- VCCIO D14
- VCCIO D13
- VCCIO D12
- VCCIO D11
- VCCIO C14
- VCCIO C13
- VCCIO C12
- VCCIO C11
- VCCIO B14
- VCCIO B12
- VCCIO B11
- VCCIO A13
- VCCIO A12
- VCCIO A11
- VCCIO J23



For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU



SANDY
62.10055.421
2nd = 62.10040.771

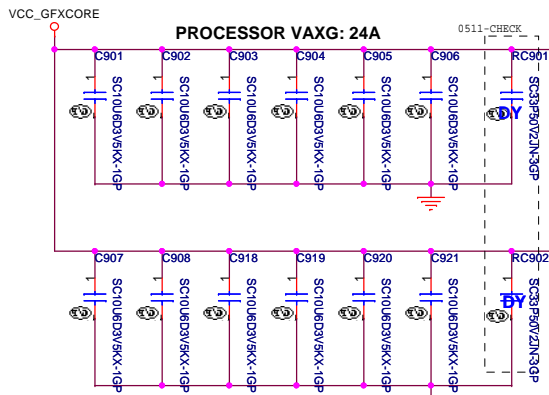
<Core Design>

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Title: **CPU (VCC CORE)**

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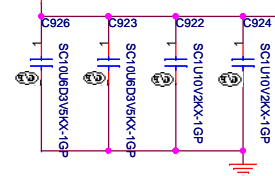
POWER



PROCESSOR VAXG: 24A

0511-CHECK

VCCPLL: 1.2A



CPU1G 7 OF 9	
AT24	VAXG
AT23	VAXG
AT21	VAXG
AT20	VAXG
AT18	VAXG
AT17	VAXG
AR24	VAXG
AR23	VAXG
AR21	VAXG
AR20	VAXG
AR18	VAXG
AR17	VAXG
AP24	VAXG
AP23	VAXG
AP21	VAXG
AP20	VAXG
AP18	VAXG
AP17	VAXG
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AJ17	VAXG
AH24	VAXG
AH23	VAXG
AH21	VAXG
AH20	VAXG
AH18	VAXG
AH17	VAXG
B6	VCCPLL
A6	VCCPLL
A2	VCCPLL

SANDY
62.10055.421
2nd = 62.10040.771

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC

VAXG_SENSE
VSSAXG_SENSE

SM_VREF

VDDQ
AF7
AF4
AF1
AC7
AC4
AC1
Y7
Y4
Y1
LJ7
LJ4
LJ1
P7
P4
P1

VCCSA
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J24
H26
H25

VCCSA_SENSE
FC_C22
VCCSA_VID1

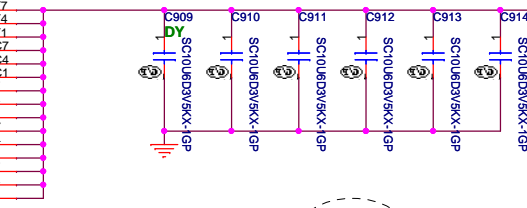
AK35 → VCC_AXG_SENSE 42
AK34 → VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

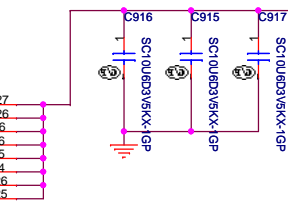
+V_SM_VREF_CNT should have 10 mil trace width

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

VDDQ: 5A

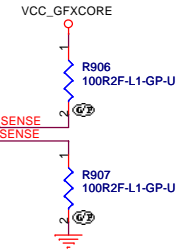
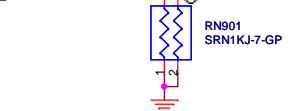


VCCA: 6A



+V0.85S - VCCSA - System Agent rail voltage can be [0.9, 0.725, 0.8, 0.675] V for IVB [0.9, 0.8] V for SNB

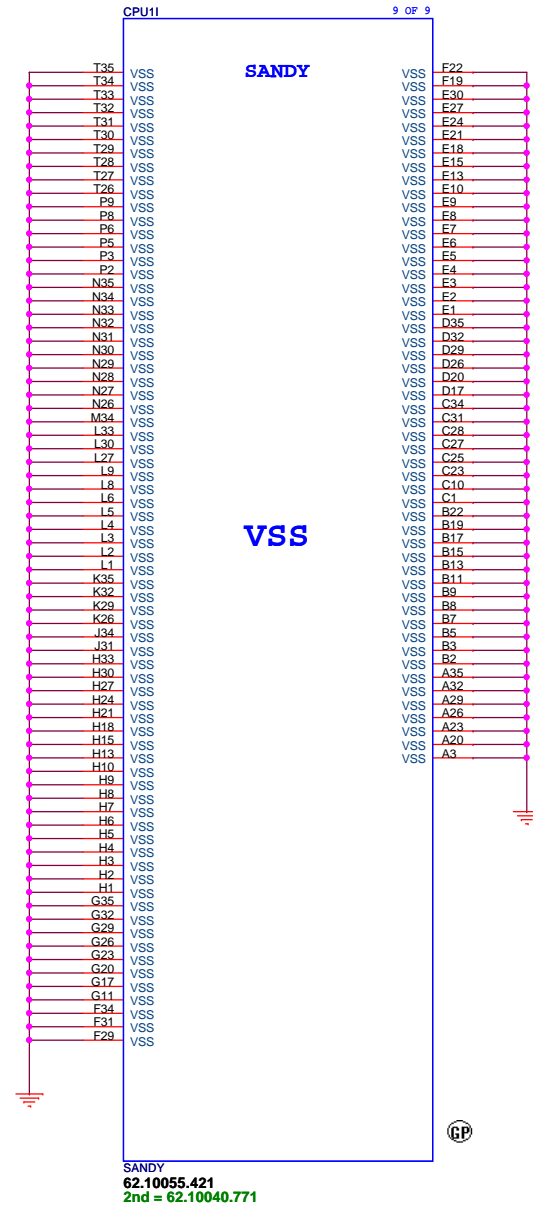
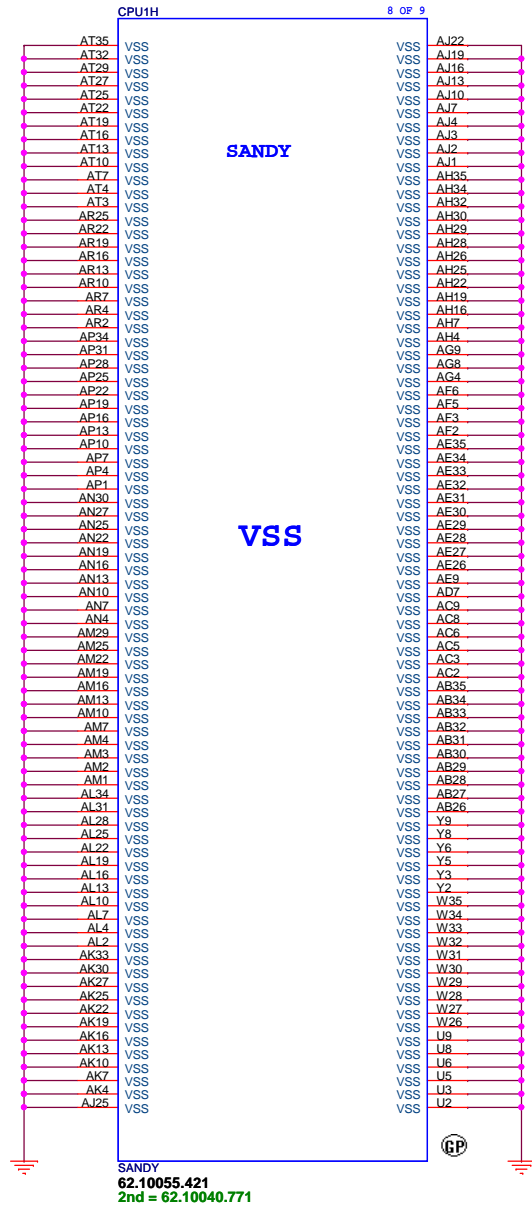
H23 → VCCSA_SENSE 48
C22 → VCCSA_SELECT0 48
C24 → VCCSA_SELECT1 48



<Core Design>

<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title: CPU (VCC GFXCORE)</p>		
Size: A3	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet: 9	of: 103

SSID = CPU



<Core Design>

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
CPU (VSS)		
Title		
Size	Document Number	Rev
A3	LA480	SD
Date:	Friday, January 06, 2012	Sheet 10 of 103

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<Core Design>

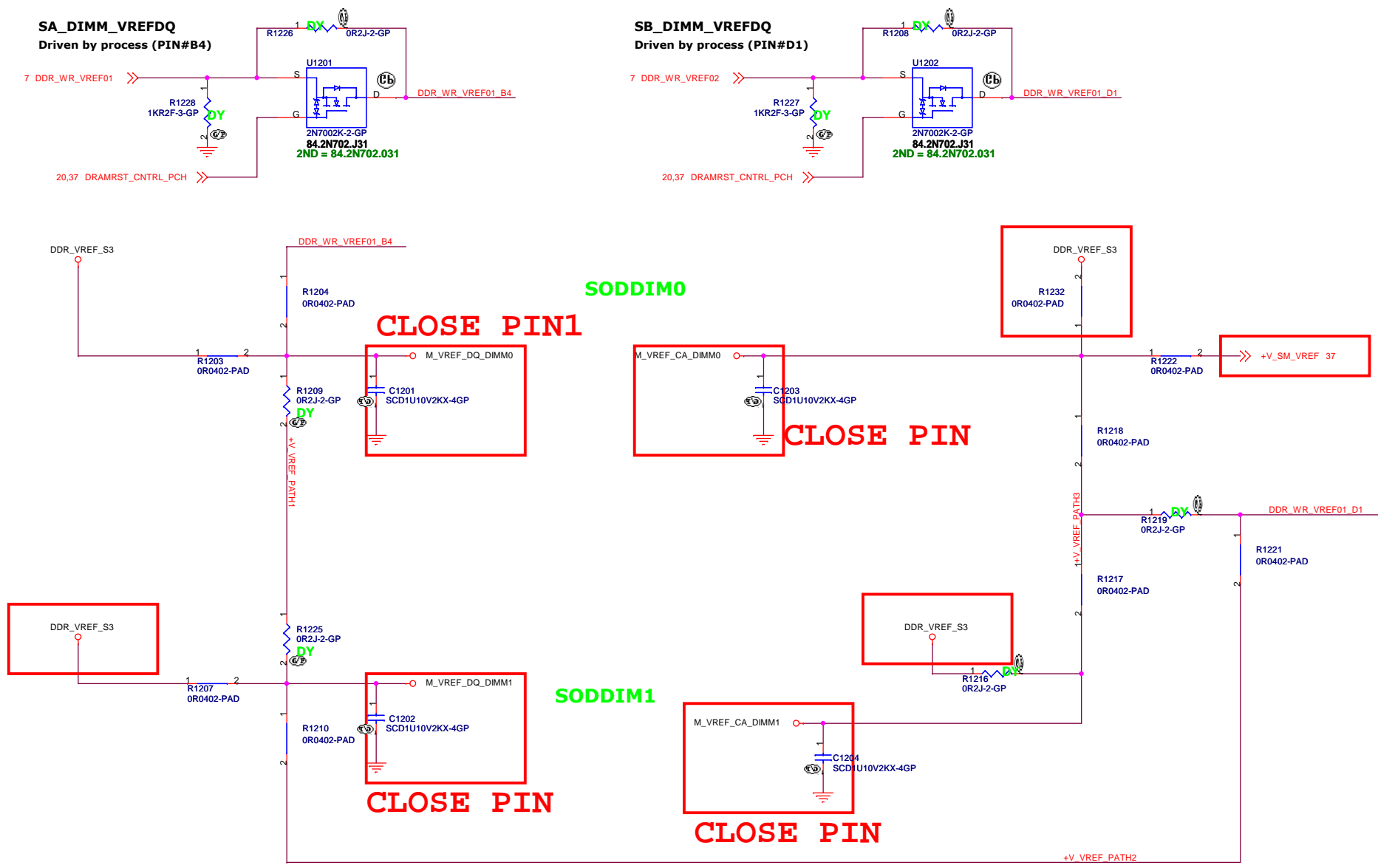
緯創資通		Wistron Corporation	
		<small>21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C</small>	

Title		
<Title>		

Size	Document Number	Rev
A4	LA480	SD

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

CAD Note: All VREF traces should have 20:20 mil trace geometry. Note that while 20 mil trace width is optimal, short violations is acceptable if required due to tight routing constraints.



<Core Design>		
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Title		
M3		
Size	Document Number	Rev
A3	LA480	SD
Date:	Friday, January 06, 2012	Sheet 12 of 103

D

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<Core Design>

緯創資通		Wistron Corporation	
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Title		
<Title>		

Size	Document Number	Rev
A4	LA480	SD

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR3-SODIMM2

Size
A4

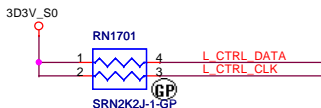
Document Number

LA480

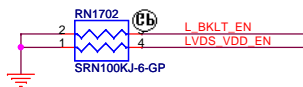
Rev
SD

Date: Friday, January 06, 2012

Sheet 16 of 103

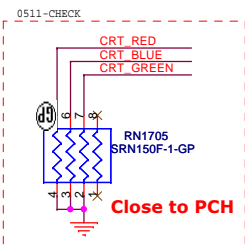


L_DDC_DATA(K47):
 This signal is on the LVDS interface.
 This signal needs to be left NC if eDP is
 used for the local flat panel display

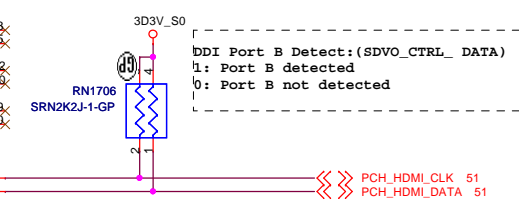
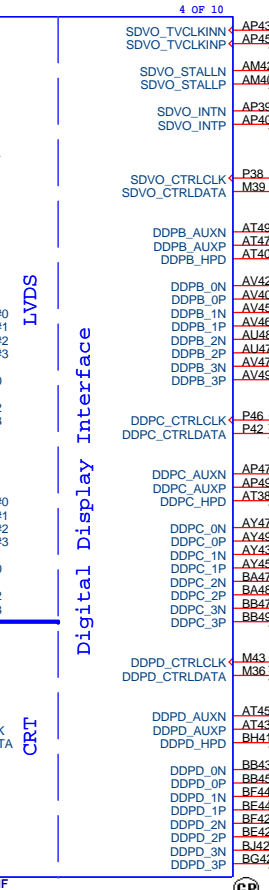
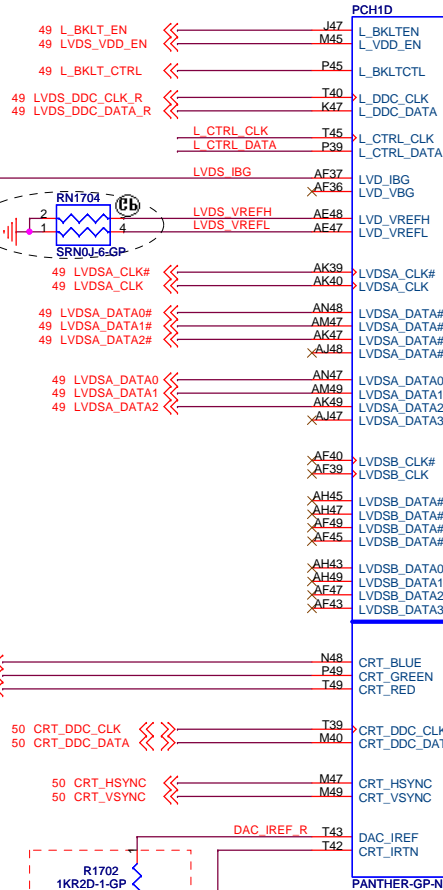
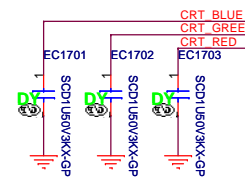


Close to PCH

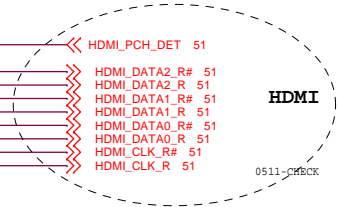
Close to PCH and keep 20mil
 away from other signal.



Close to PCH



DDI Port B Detect: (SDVO_CTRL_DATA)
 1: Port B detected
 0: Port B not detected



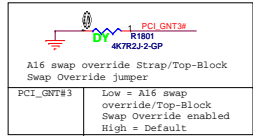
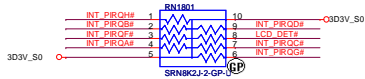
HDMI

PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-B	DDPB_0N	TMDSB_DATA2#
	DDPB_0P	TMDSB_DATA2#
	DDPB_1P	TMDSB_DATA1#
	DDPB_1N	TMDSB_DATA1#
	DDPB_2P	TMDSB_DATA0#
	DDPB_2N	TMDSB_DATA0#
	DDPB_3P	TMDSB_CLK#
	DDPB_3N	TMDSB_CLK#
	DDPB_AUXN	NA
	DDPB_HPD	HDMI_B_HPD
	SDVO_CTRLCLK	HDMI_B_CTRLCLK
	SDVO_CTRLDATA	HDMI_B_CTRLDATA

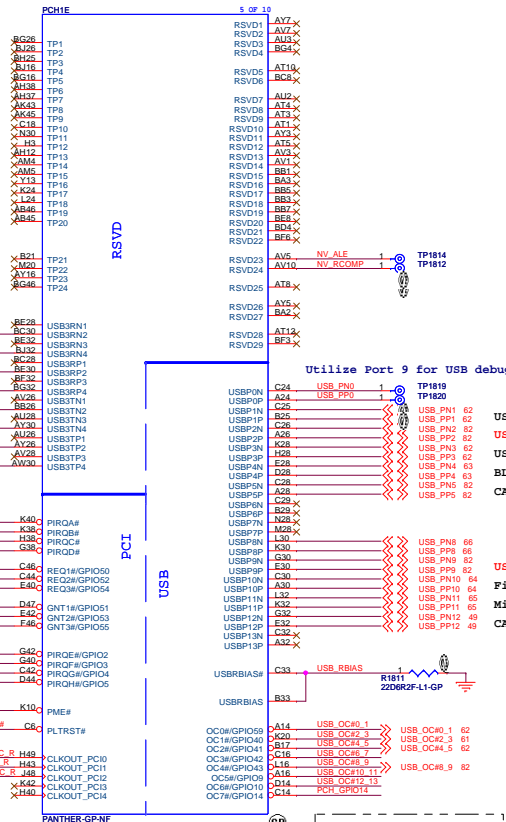
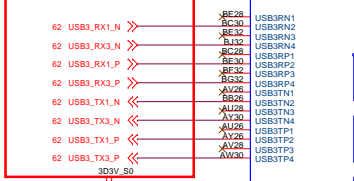
Notes:
1K 0.5% 0402

The recommended value for this external resistor is 1.0 k ±0.5%. The CRT DAC outputs may be measured when the display is completely white. If CRT DAC signal voltage value is between 665 mV to 770 mV, then the video level is within VESA specification and the reference resistor value is optimal for the motherboard design.

SSID = PCH



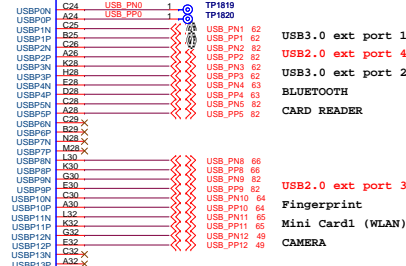
For PPT USB3.0 feature



GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

Mini Card2 (WWAN)

Utilize Port 9 for USB debug

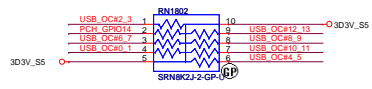
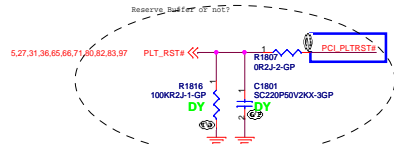


Gx8 USB Table

Pair	Device
0	X
1	USB3.0, ext port1
2	USB2.0, ext port4
3	USB3.0, ext port2
4	Bluetooth
5	CARD READER
6	X
7	X
8	3G
9	USB2.0, ext. port 3
10	Fingerprint
11	Mini Card1 (WLAN)
12	CAMERA
13	X

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 4, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

OC13# for Device 29 (Ports 0-7)
OC17# for Device 26 (Ports 8-13)



For platforms not supporting Deep S4/S5
1.VccSW3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWRN# used as SUSWRDNACK/GPIO30

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

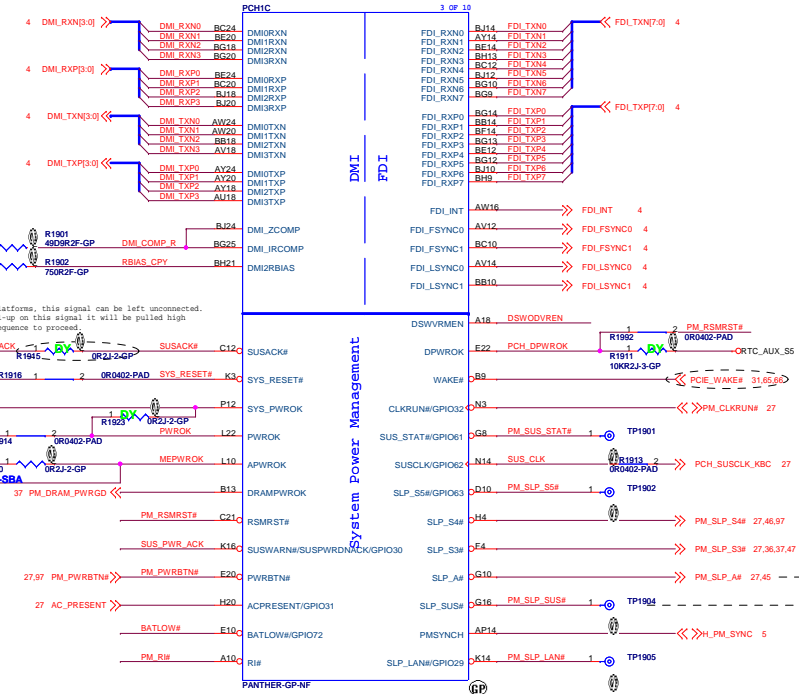
Platforms supporting Deep S4/S5 and not VccDSW3_3 will participate in the handshake during wake and Deep S4/S5 entry may tie SUSACK# to SUSWRN#.

SUS_ACK#! For non-DW platforms, this signal can be left unconnected. Due to the internal pull-up on this signal it will be pulled high in order for the boot sequence to proceed.

SYS_PWROK: the system is ready to start the exit from reset (de-asserts PCH_S0P# to the processor)
PWROK: It indicates to PCH that its CORE well power is stable.
Active Sleep Well (ASW) Power OK

80_PWR_GOOD after PM_SLP_S3# delay 200 ns

SUSWRDNACK: No longer requires a 10-K pull-up to VccSW3 (3.3 V).

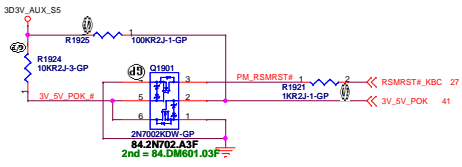
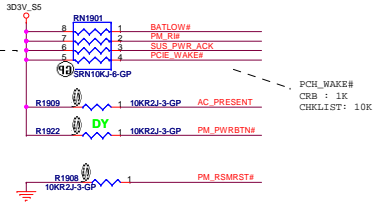


DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled

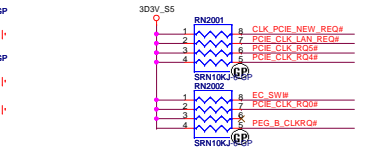
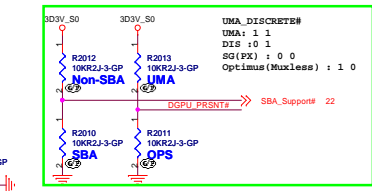
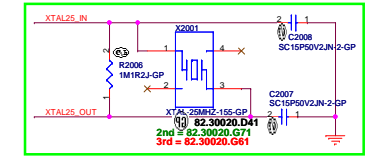
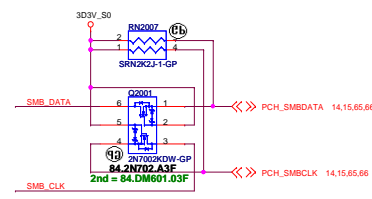
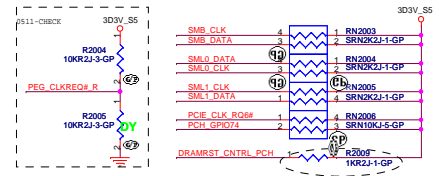
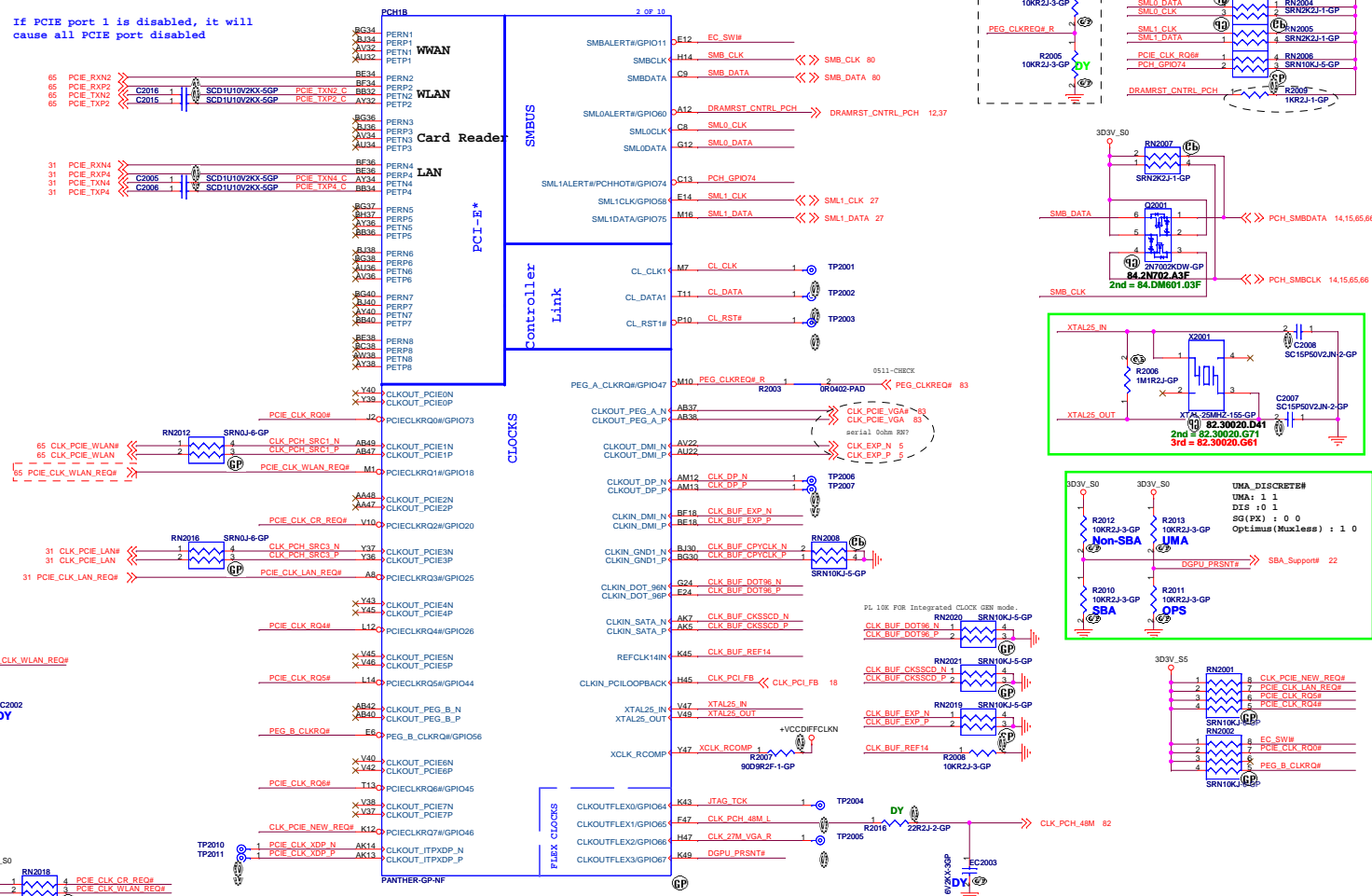
This signal is used to control power planes to the Intel® ME sub-system. This signal will be asserted in M-off state. If M3 is not supported then SLP_A# will have the same timings as SLP_S3#.

For platforms supporting DEEP S4/S5 state, a low on this signal indicates that PCH is in Deep Sleep state and that EC/platform logic does not need to keep the Suspend Rails ON. If high means EC must keep SUS rails ON. If DEEP S4/S5 is not supported, then this pin can be left unconnected.



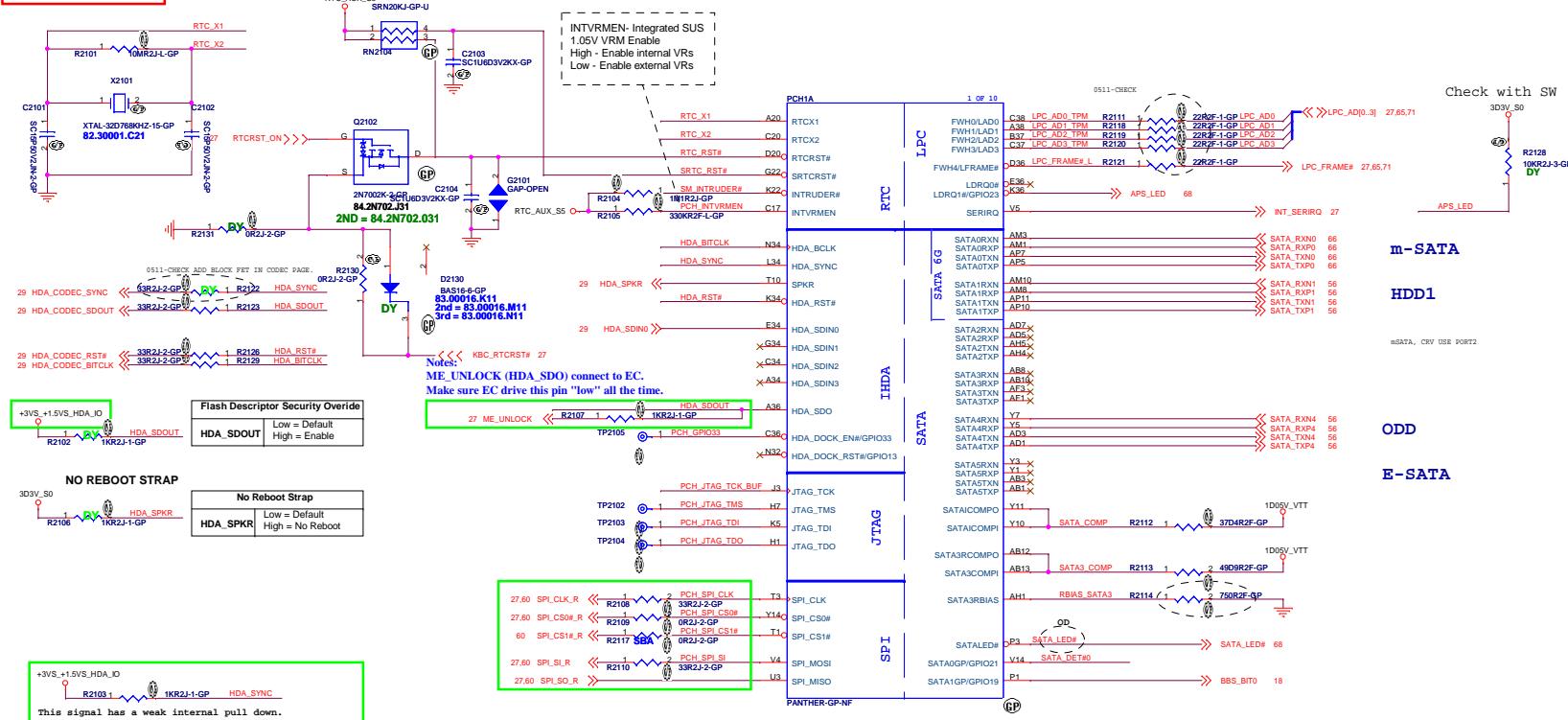
SSID = PCH

If PCIe port 1 is disabled, it will cause all PCIe port disabled



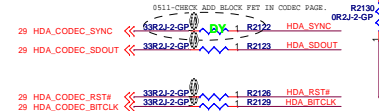
- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

SSID = PCH

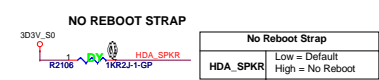


INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

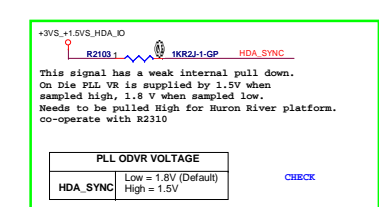
Check with SW



Flash Descriptor Security Override	
HDA_SDOOUT	Low = Default High = Enable



No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot



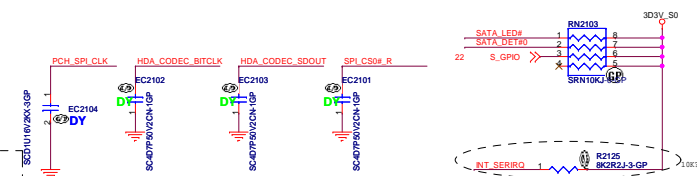
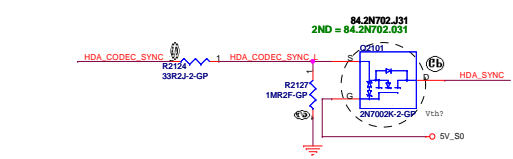
This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.5V (Default) High = 1.5V

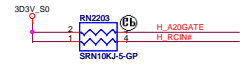
CHECK

This signal has a weak internal pull-down.
On Die PLL VR is supplied by 1.5 V from VccVRM when sampled high, 1.8 V from VccVRM when sampled low.

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

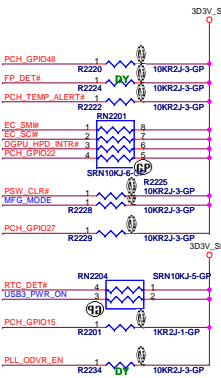


R2202
 HR:200K (64.20035.6DL)
 CRV:10K (63.10334.1DL)

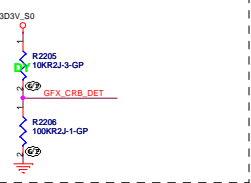


GPIO27 has a weak[20K] internal pull up.
 To enable on-die PLL Voltage regulator,
 should not place external pull down.

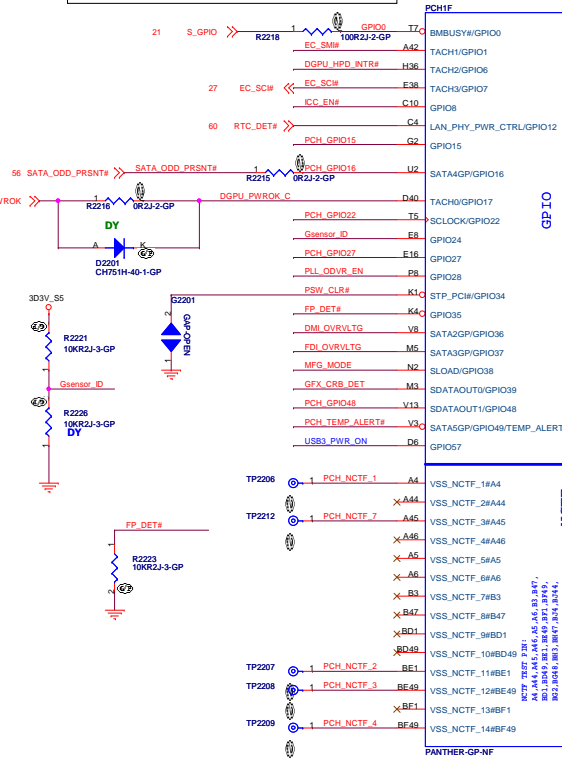
G-Sensor	ST	KIXNOK
R2226	DY	10K
R2221	10K	DY



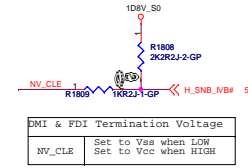
	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



Note:
 For PCH debug with XDP, need to NO STUFF R2218



PLL ON DIE VR ENABLE
 NOTE: This signal has a weak internal pull-up 20K
 ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
 DISABLED -- LOW (R2212 STUFFED)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc when HIGH

TS Signal Disable Guideline:
 TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4
 should not float on the motherboard. They
 should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

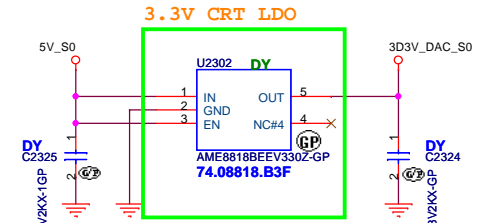
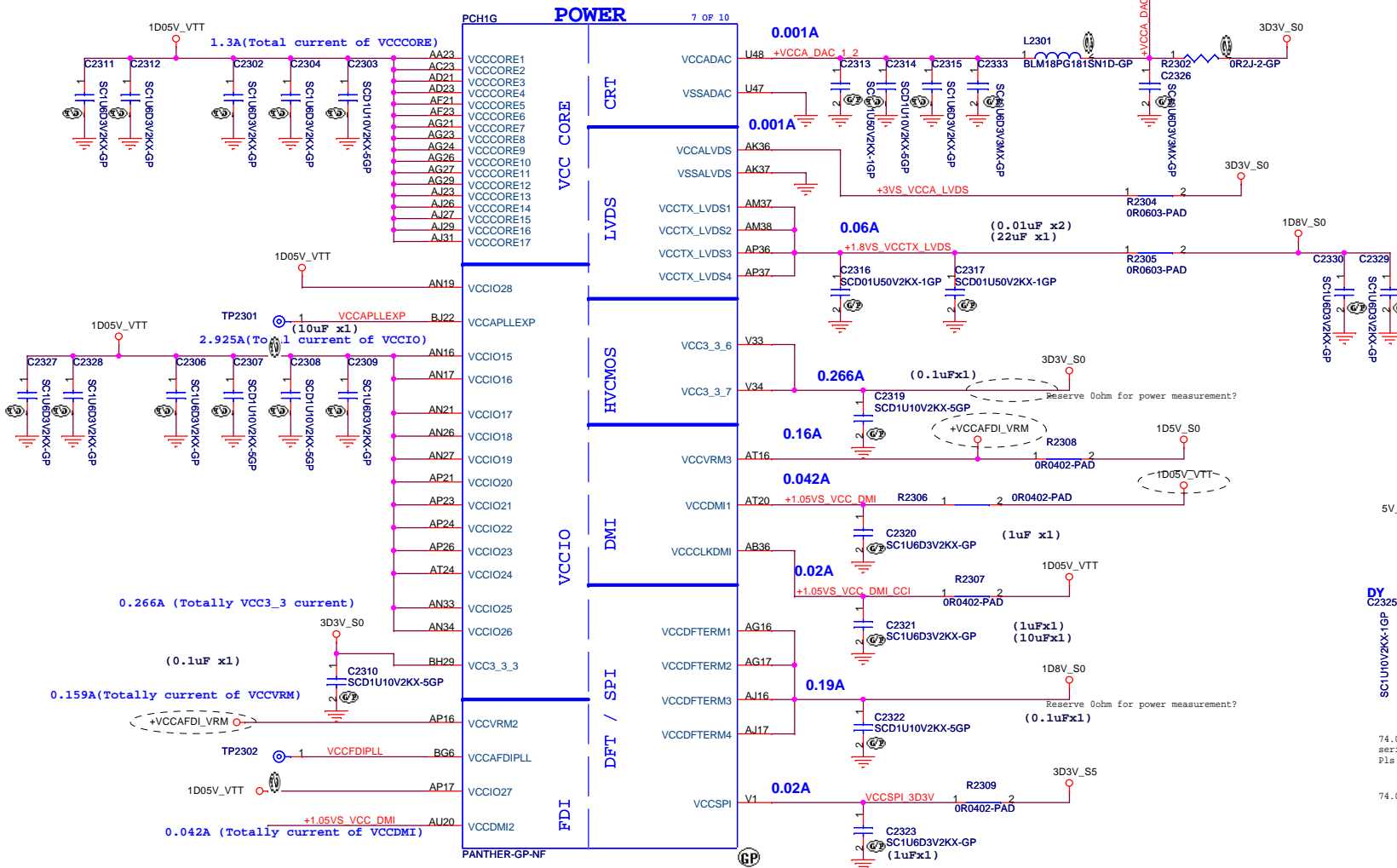
DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved
 via soft-strap. The default is integrated clock
 enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

GPIO15 has a weak[20K] internal pull up.
 Integrated Clock Enable functionality is achieved
 via soft-strap. The default is integrated clock
 enable.

6A



74.09091.J3F GMT OBS REASON:G9091 series is going to EOL and no room for further cost reduction. Pls help to use AME AME8818 , TI TLV702 and GMT G9090 for replacement.

74.09198.G7F OBS

VCCVRM(Internal PLL and VRMs):
 A.1.5V for Mobile
 B.1.8 V for Desktop

Refer to NPCE795 shared SPI flash architecture

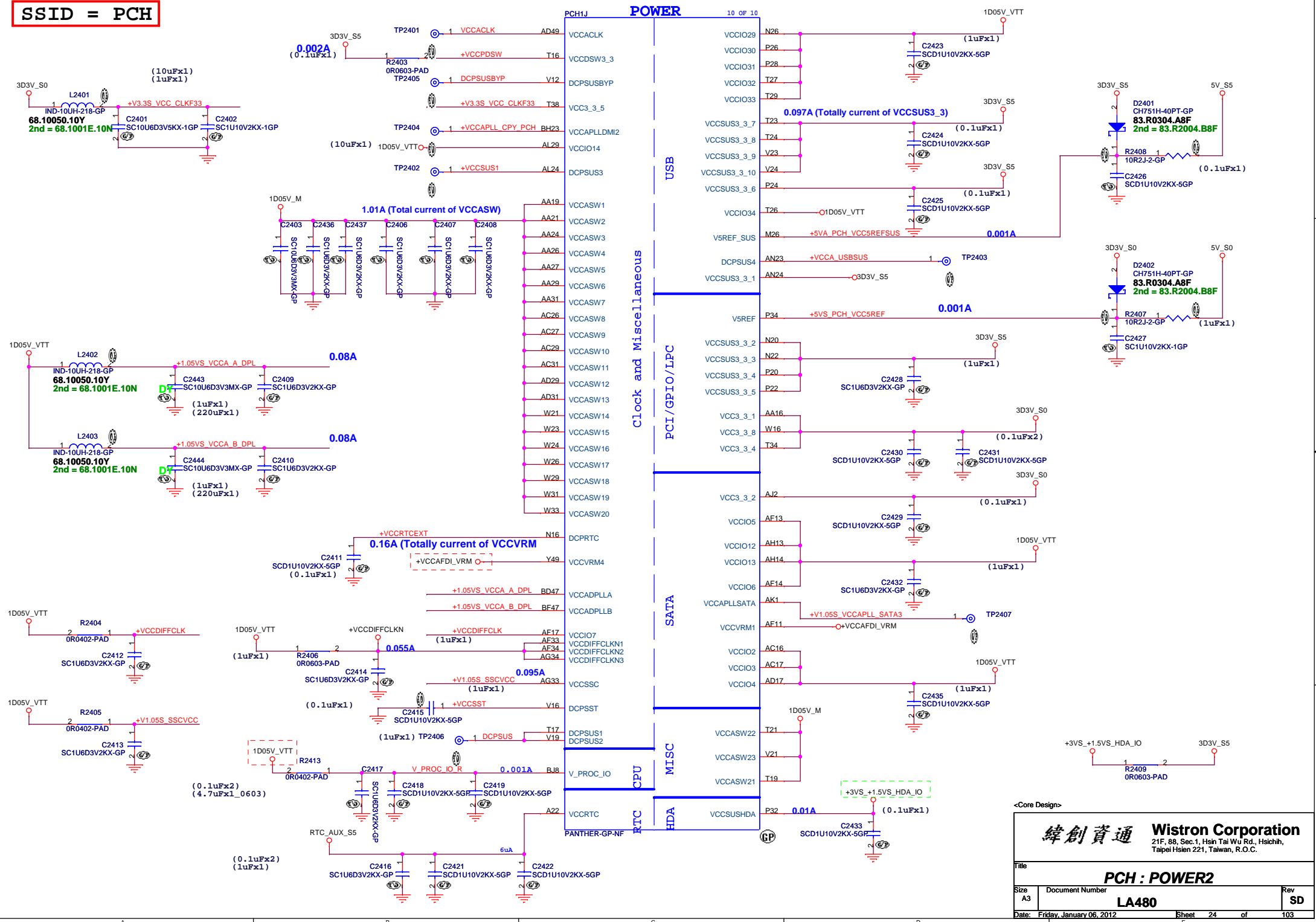
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Title: **PCH : POWER1**

Size A3	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 23	of 103

SSID = PCH

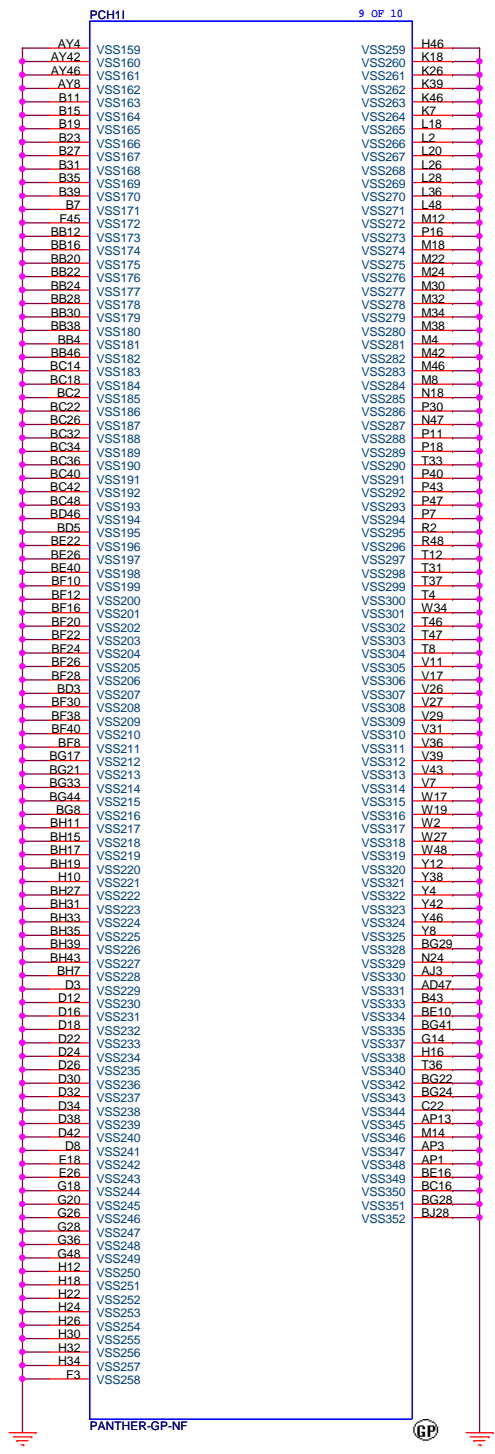
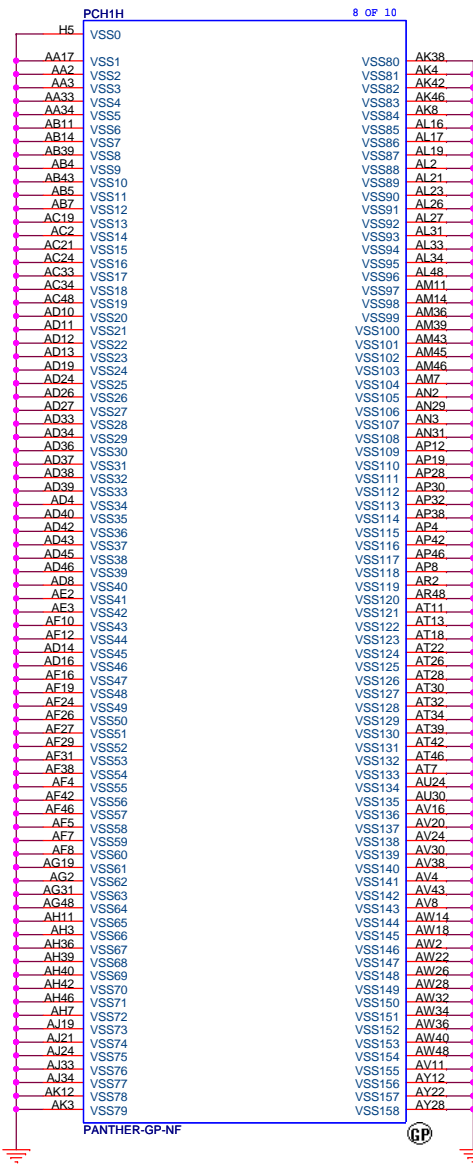


<Core Design>

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Title		SD
PCH : POWER2		SD
Size A3	Document Number	Rev
	LA480	
Date: Friday, January 06, 2012	Sheet 24 of 103	

SSID = PCH



<Core Design>

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Title: **PCH : VSS**

Size: A3 | Document Number: **LA480** | Rev: **SD**

Date: Friday, January 06, 2012 | Sheet: 25 of 103

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

LA480

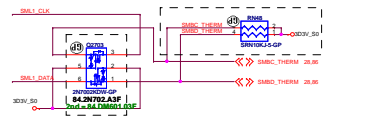
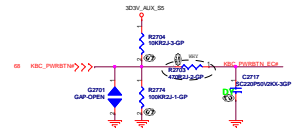
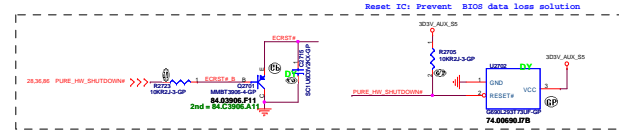
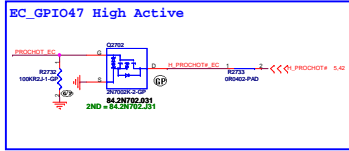
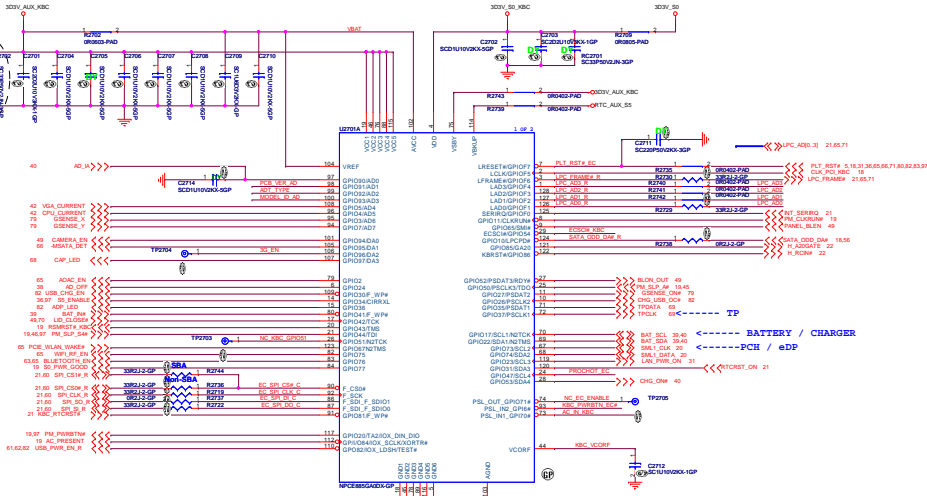
Rev

SD

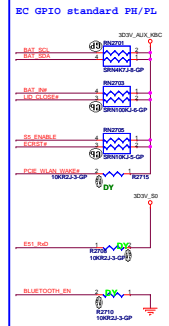
Date: Friday, January 06, 2012

Sheet 26 of 103

SSID = KBC



MODEL_ID_AD (Pin10)	Pull Down	Pull High	Voltage
IMDA	100.0K	33.0K	2.481V
OPTI08	100.0K	47.0K	2.245V

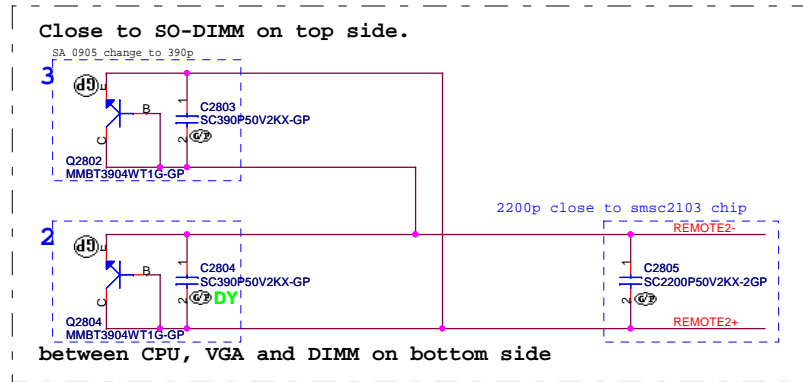


PCB Version A/D (Pin#)	Full-Low Resistor	Full-High Resistor (3.0V_AUX_55)	Voltage
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
+S	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

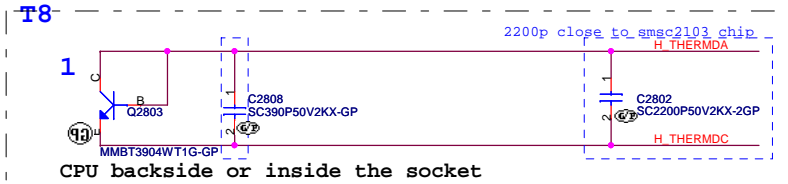
71.00885.A0G
IC EMB CTRL NPCE885PA0DX LQFP 128P

SSID = Thermal

Thermal sensor

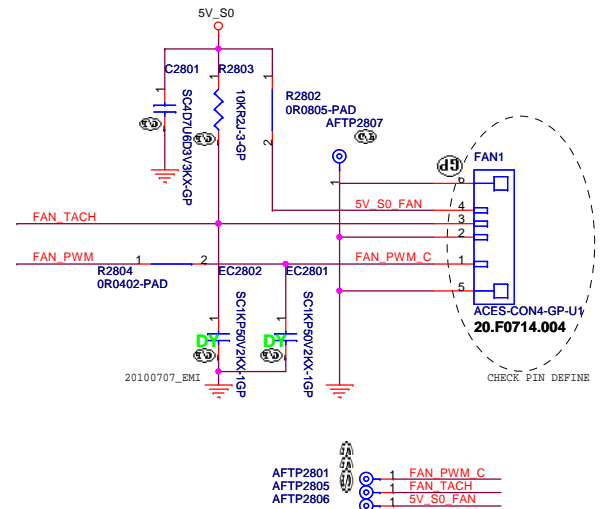


20110718_Carrey:
For Vendor suggestion, add 390pF Cap. as closed to pin B/C and E of Q2803

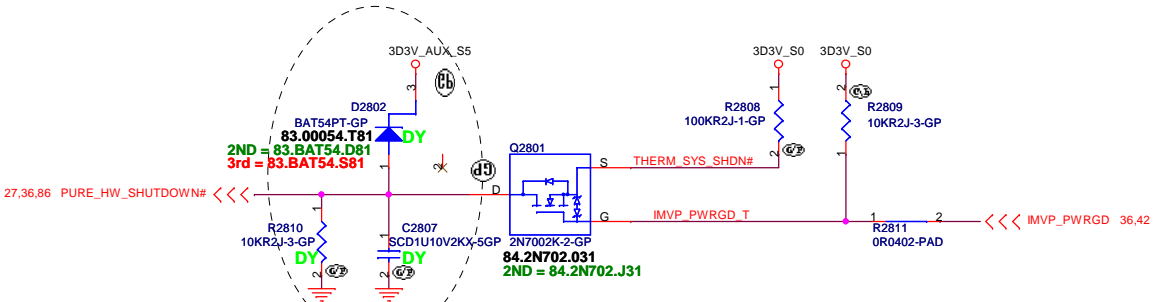
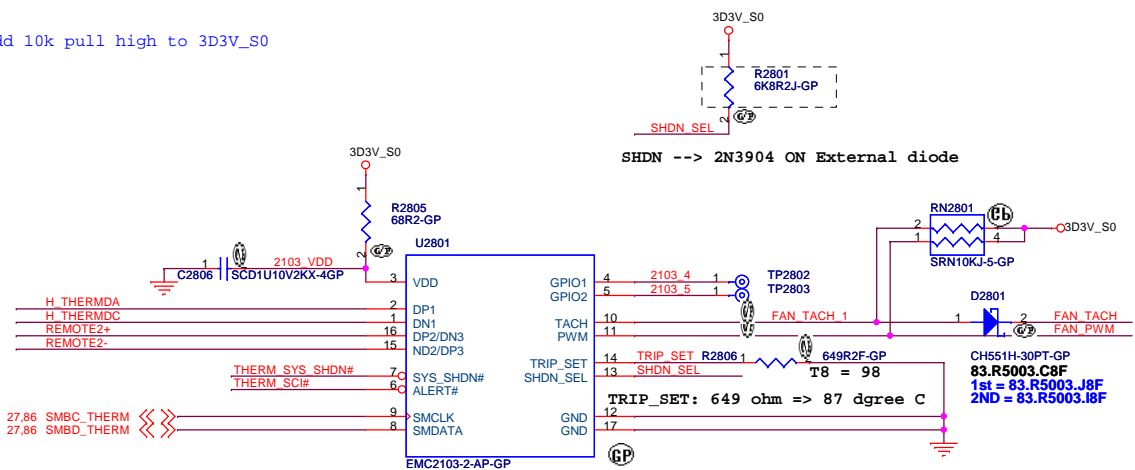
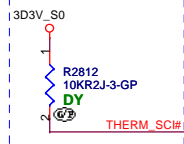


CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

4 WIRE PWM Fan Control circuit



20110718_Carrey:
For Vendor suggestion, add 10k pull high to 3D3V_S0



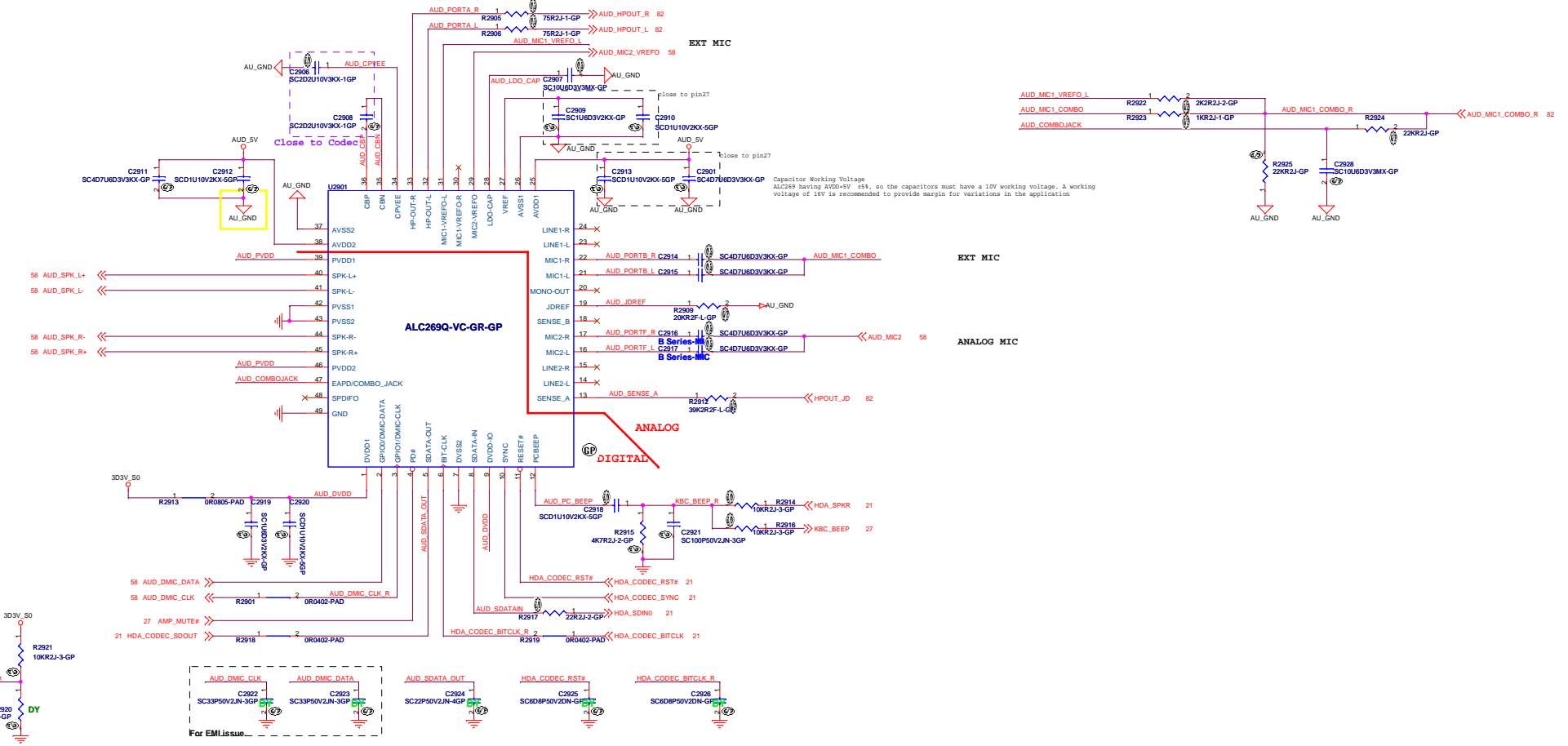
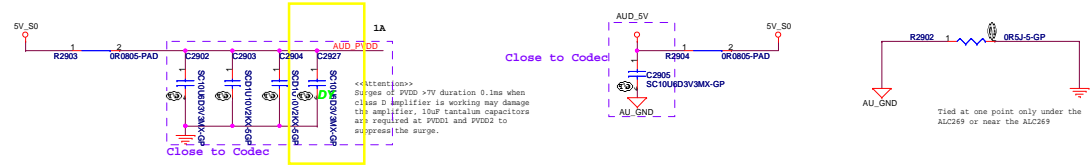
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Title: **THERMAL SENSOR SMSC EMC2103**

Size A3 Document Number **LA480** Rev **SD**

Date: Friday, January 06, 2012 Sheet 28 of 103



20100705_A0D

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<Core Design>

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Title

Reserved

Size
A4

Document Number

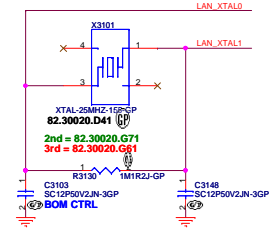
LA480

Rev
SD

Date: Friday, January 06, 2012

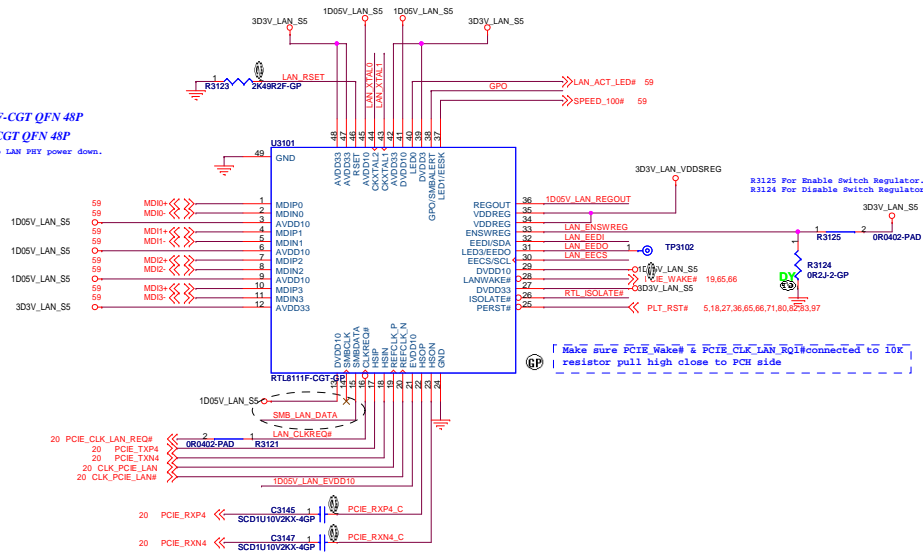
Sheet 30 of 103

25MHz XTAL



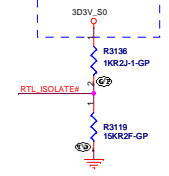
	C3103	C3148
VB480	15pF 78.15034.1FL	12pF
VB580	12pF 78.12034.1FL	12pF

71.08111.N03, IC PCIE CTRL RTL8111F-CGT QFN 48P
 71.08111.J03, IC PCIE RTL8111E-VL-CGT QFN 48P
 8111F can use GPIO to inform system to do LAN PWR power down.



Make sure PCIE_Wake# & PCIE_CLK_LANE_Roll connected to 10k resistor pull high close to PCH side

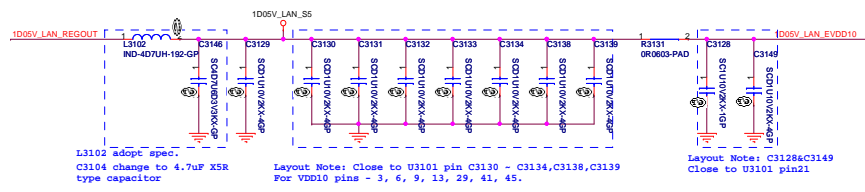
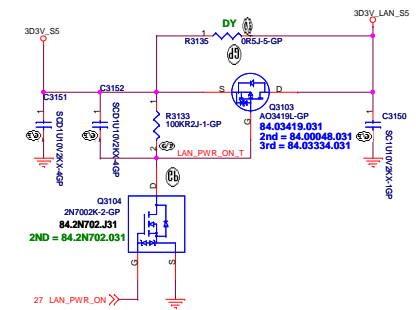
main pwr if have no ASP



High Link up / Low Link down



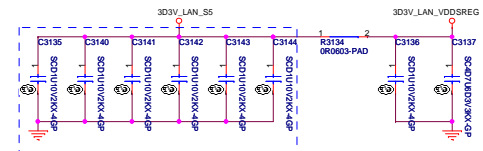
The SM DATA with 10K ohm pull GND.



L3102 3d0pF epec.
 C3104 change to 4.7uF XSR type capacitor

Layout Note: Close to U3101 pin C3130 - C3134, C3138, C3139 For VDD10 pins - 3, 6, 9, 13, 29, 41, 45.

Layout Note: C3128&C3149 Close to U3101 pin21



Layout Note: C3135, C3140-C3144 Close to U3101 pin For VDD33 pins - 12, 27, 39, 42, 47, 48.

<Core Design>

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<Core Design>

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Title

Reserved

Size
A4

Document Number

LA480

Rev
SD

Date: Friday, January 06, 2012

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<Core Design>

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Title

Reserved

Size
A4

Document Number

LA480

Rev
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Date: Friday, January 06, 2012

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB 3.0 Controller

Size
A4

Document Number

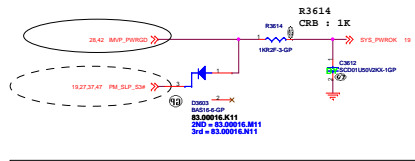
LA480

Rev
SD

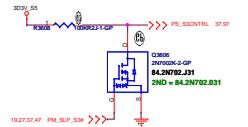
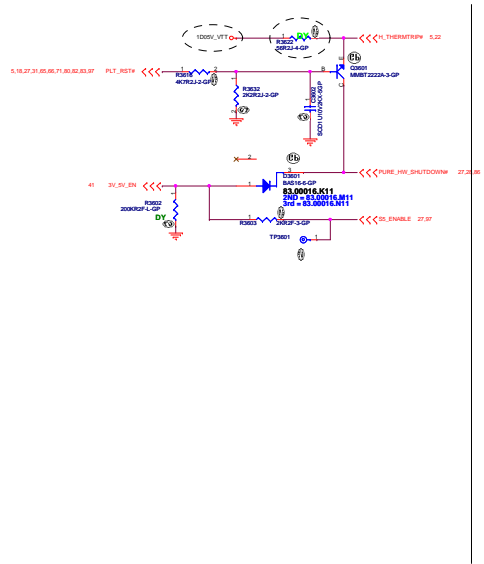
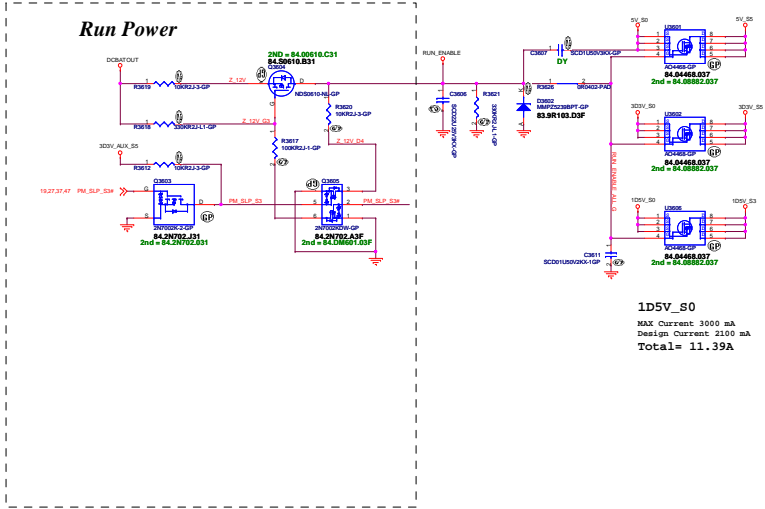
Date: Friday, January 06, 2012

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Power Sequence

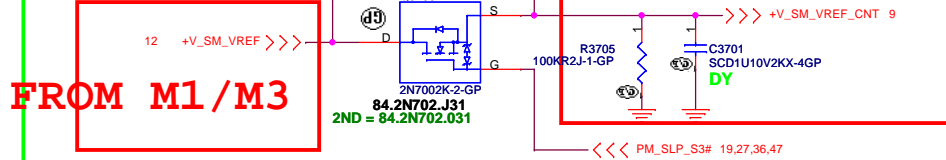


Run Power



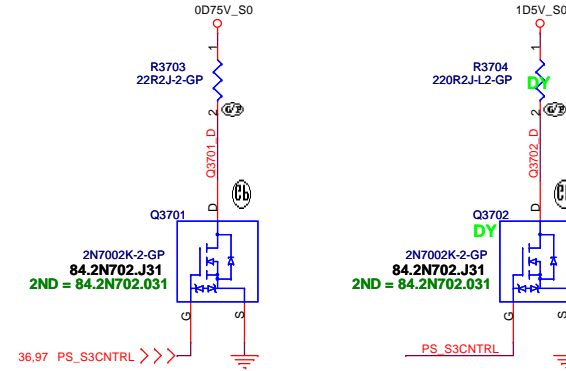
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

DEL R3714
R3705 -> 100K
DY C3701



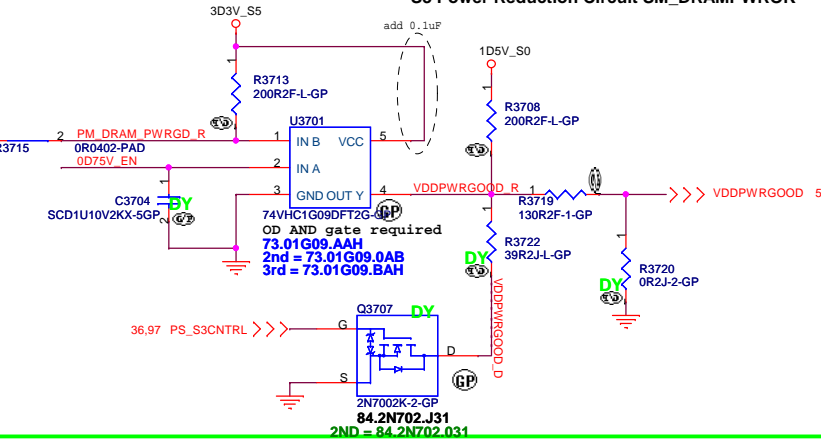
FROM M1/M3

Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

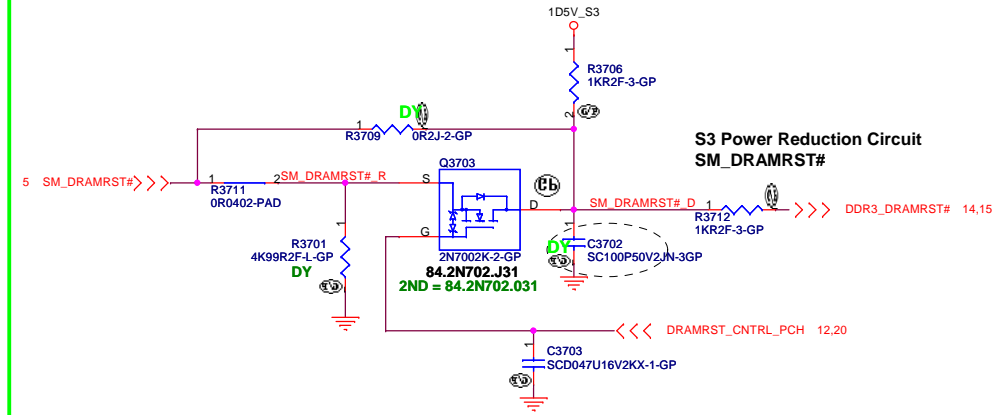


SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

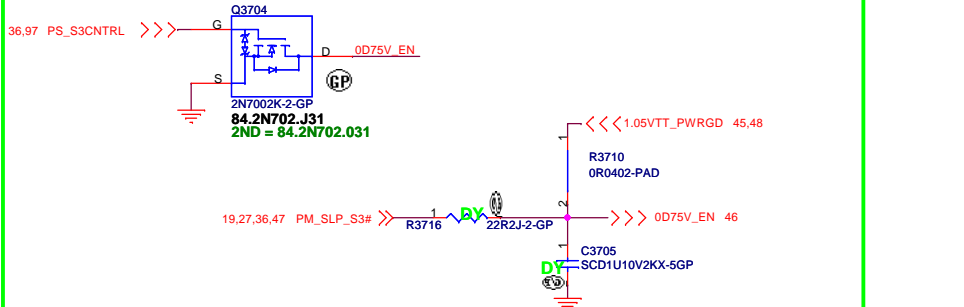
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



5 S3 Power Reduction

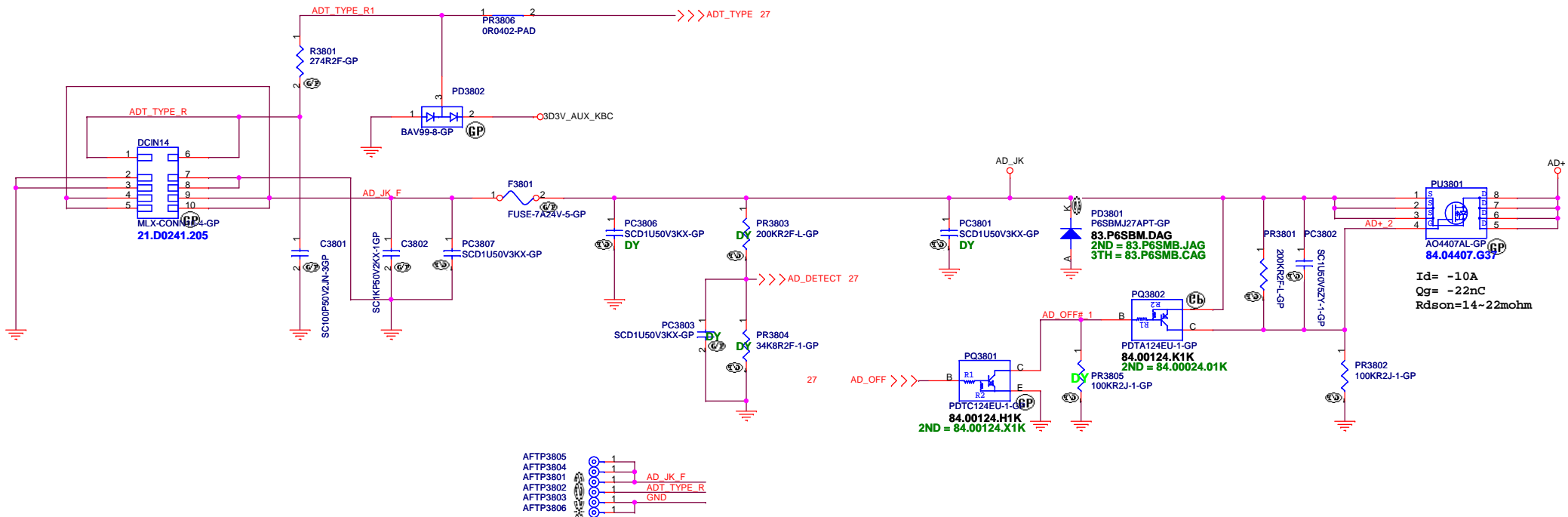


<Core Design>

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Title ADAPTER		
Size A3	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 37	of 103

Adaptor in to generate DCBATOUT

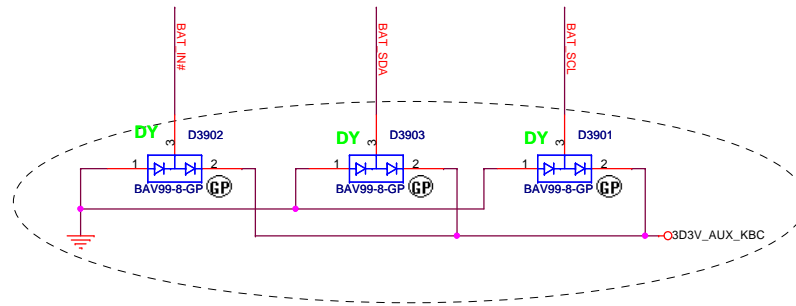
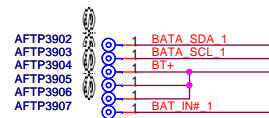
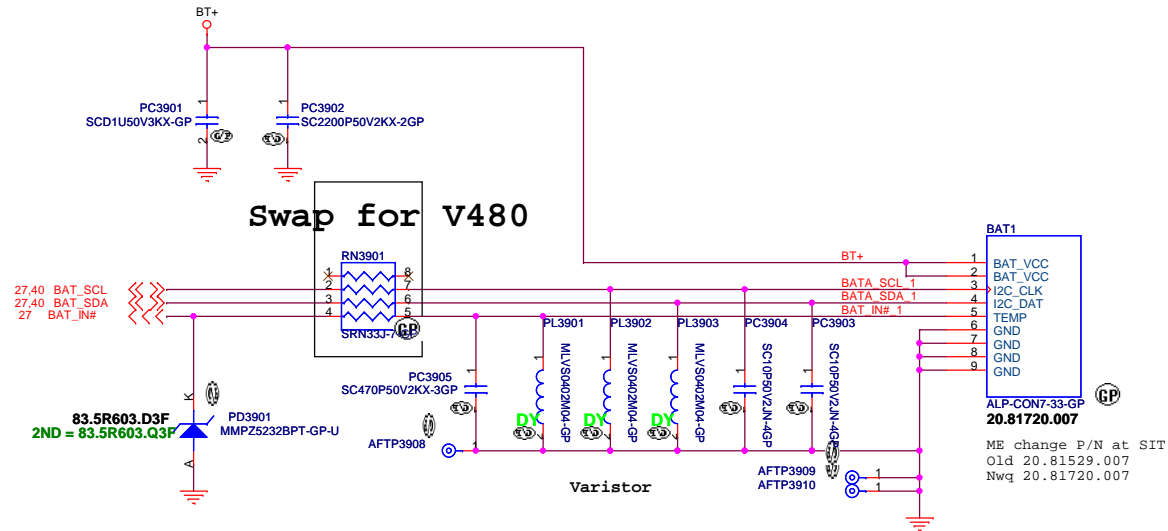


DCIN14 for 14" VB480 & VB485
 DCIN15 for 15" VB580 & VB585

<Core Design>

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DCIN_JACK	
Size A3	Document Number LA480
Date: Friday, January 06, 2012	Rev SD
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BATTERY CONNECTOR



DY on LAB stage

<Core Design>

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Title BATT_CONN	
Size Document Number LA480	Rev SD
Date: Friday, January 06, 2012 Sheet 39 of 103	

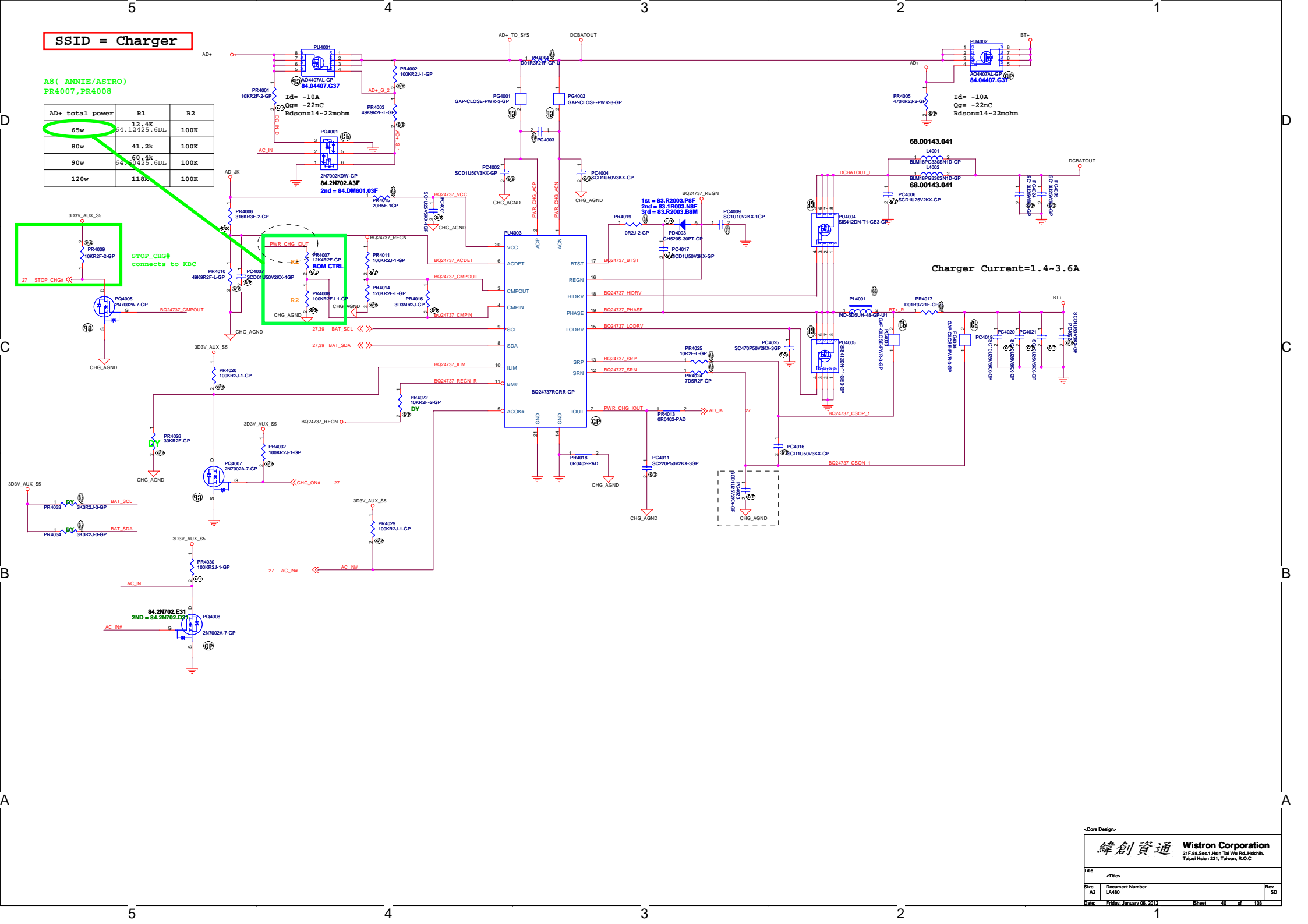
SSID = Charger

A8 (ANNIE/ASTRO)
PR4007, PR4008

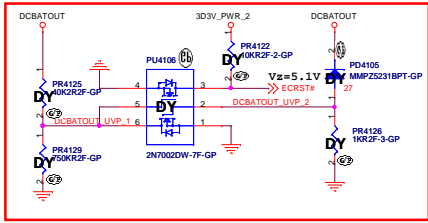
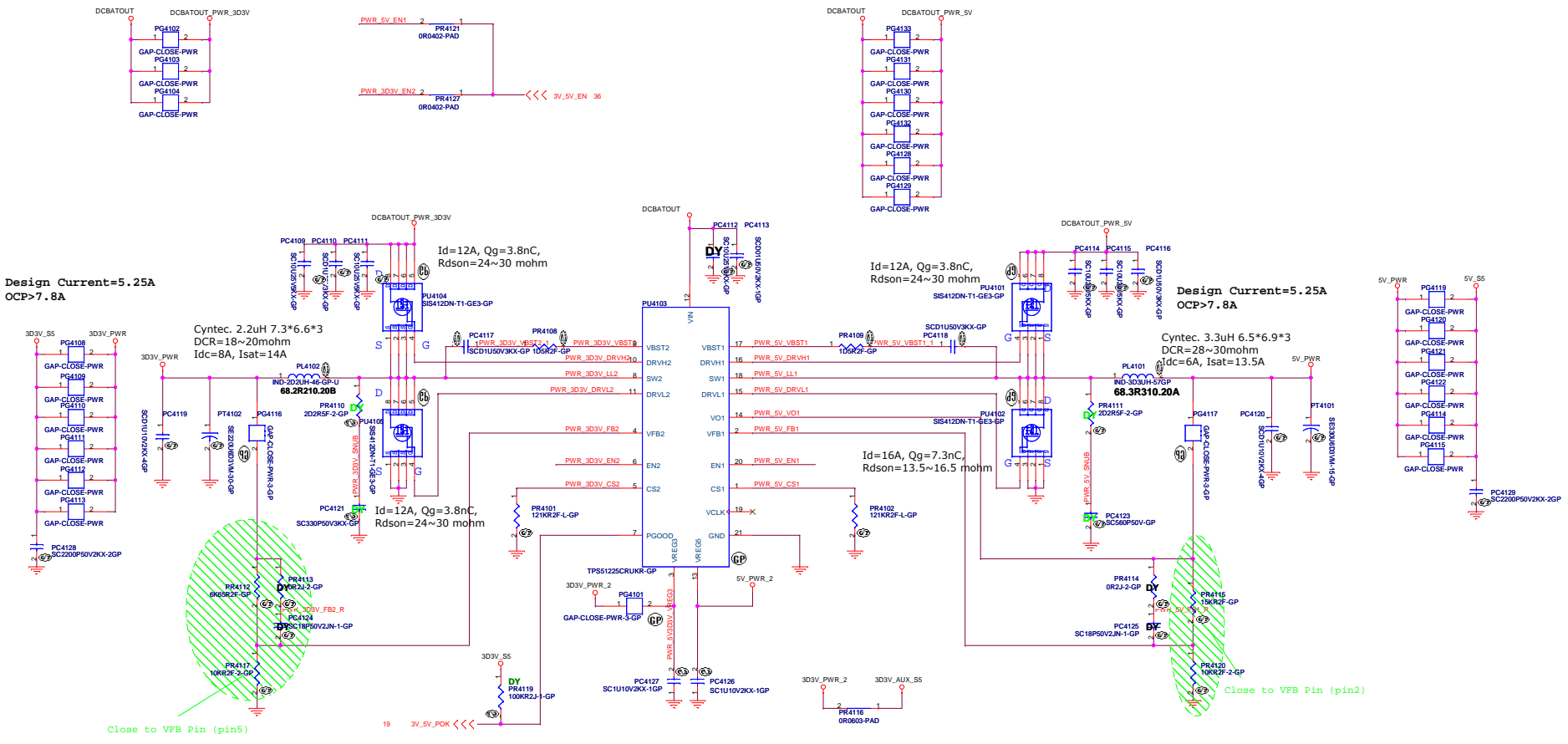
AD+ total power	R1	R2
65w	64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K

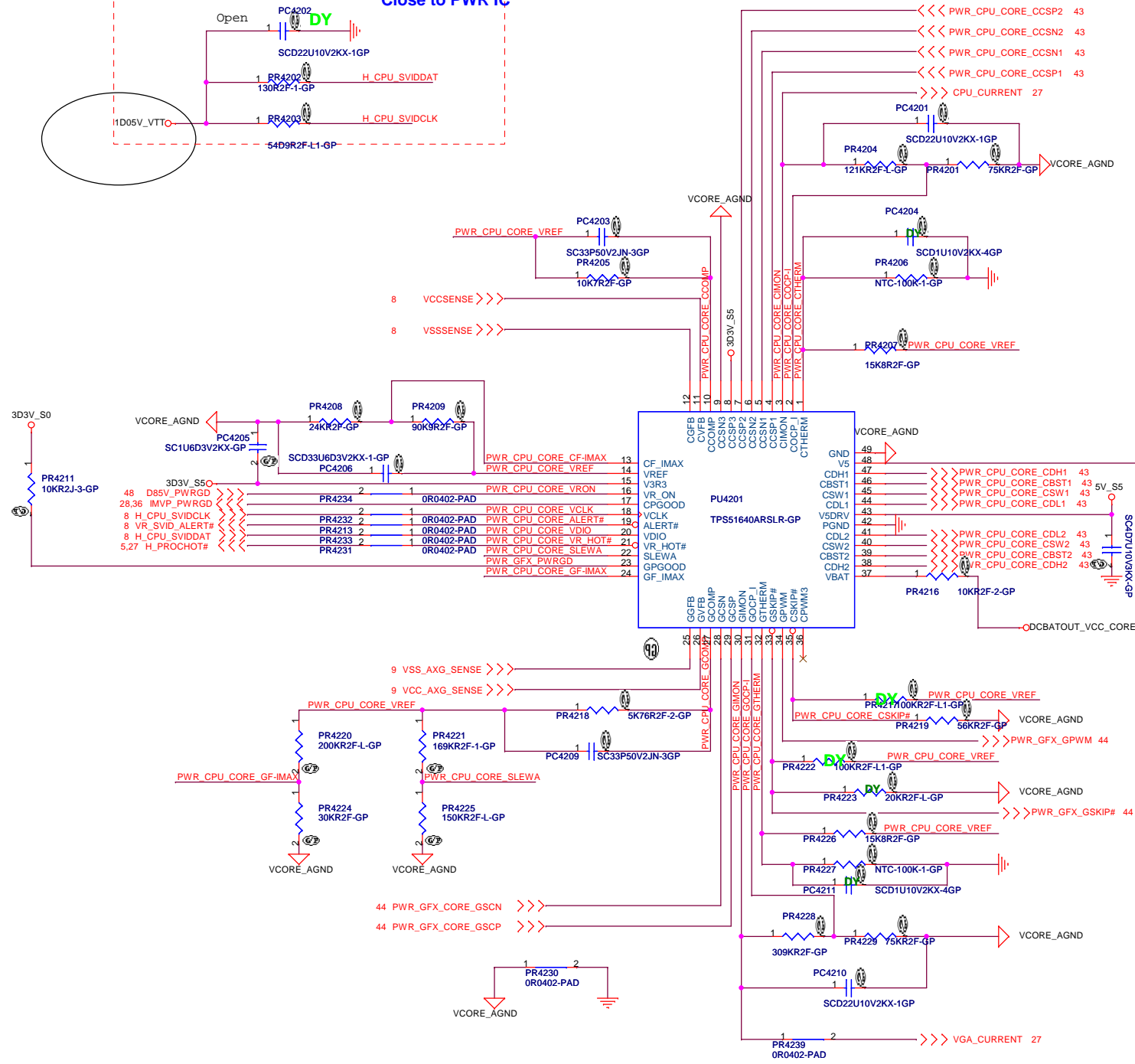
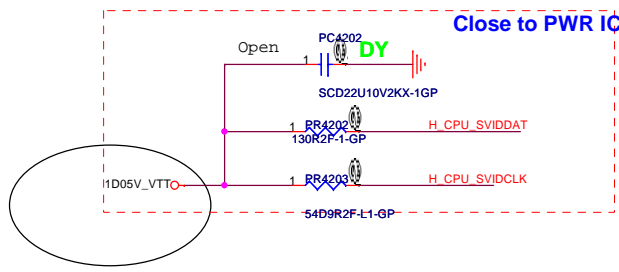
STOP_CHG# connects to KBC

Charger Current=1.4~3.6A



SSID = PWR.Plane.Regulator_5v3p3v





<Core Design>

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Title **TPS51640_CPU_CORE(1/3)**

Size	Document Number	<Doc>	Rev	SD
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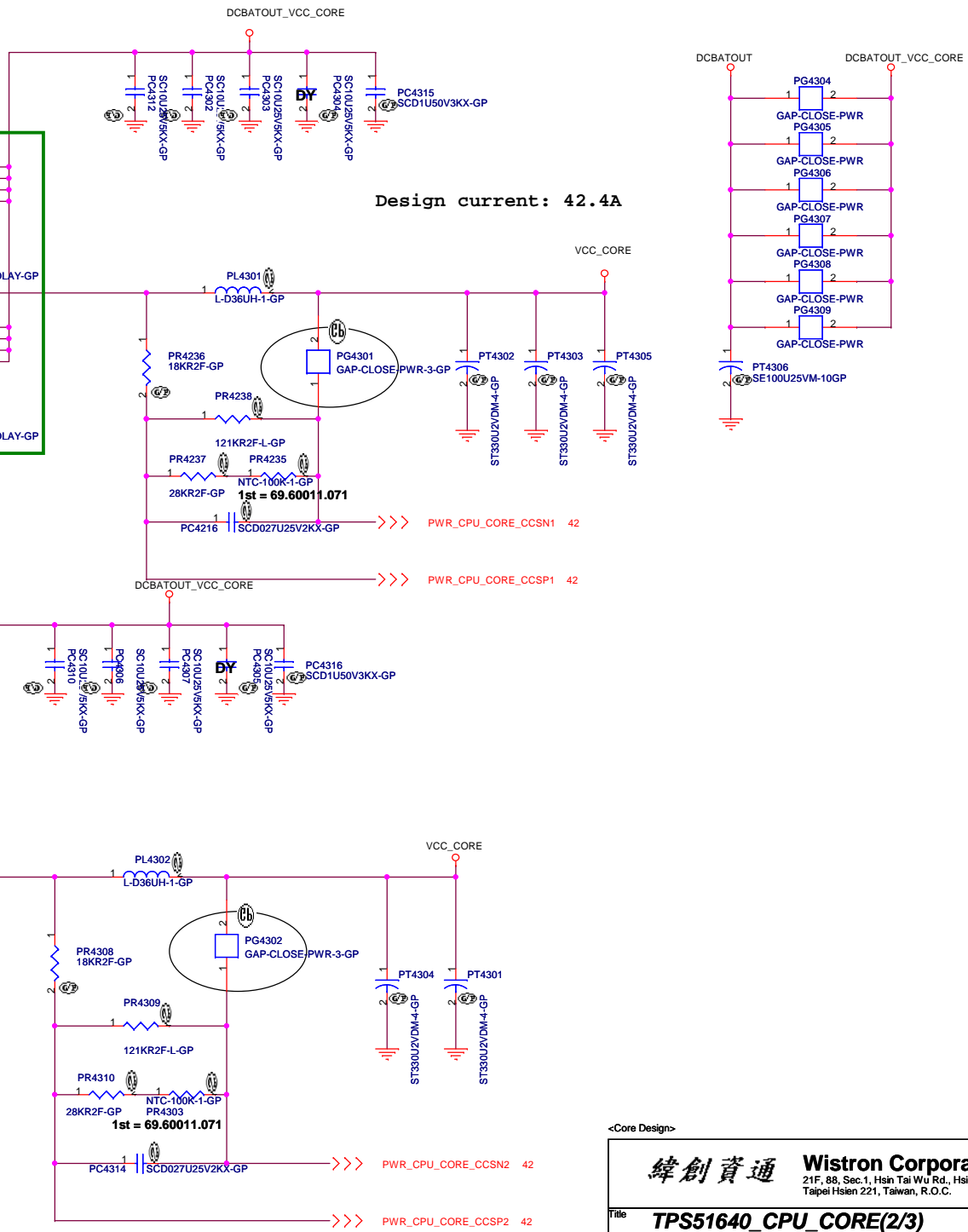
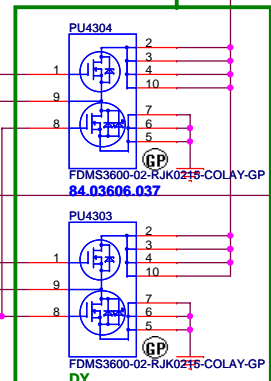
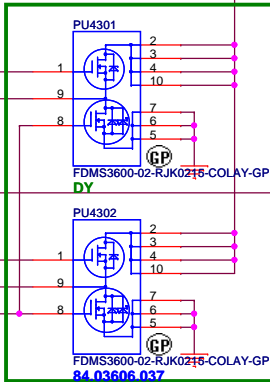
Date: Friday, January 06, 2012 Sheet 42 of 103

42 PWR_CPU_CORE_CDH1 >>>
 42 PWR_CPU_CORE_CSW1 >>>
 PWR_CPU_CORE_CBST1.1
 42 PWR_CPU_CORE_CBST1 >>>
 42 PWR_CPU_CORE_CDL1 >>>

	Main source	2nd source
PU4301	84.03606.037 FDMS3606S-GP-U	
PU4302	84.03606.037 FDMS3606S-GP-U	
PU4303	84.03606.037 FDMS3606S-GP-U	
PU4304	84.03606.037 FDMS3606S-GP-U	

BOM control

42 PWR_CPU_CORE_CDH2 >>>
 42 PWR_CPU_CORE_CSW2 >>>
 PWR_CPU_CORE_CBST2.1
 42 PWR_CPU_CORE_CBST2 >>>
 42 PWR_CPU_CORE_CDL2 >>>



<Core Design>

緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title
TPS51640_CPU_CORE(2/3)

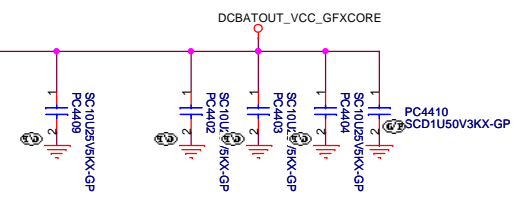
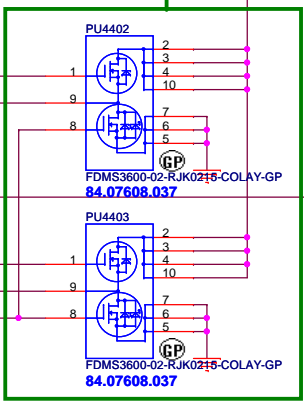
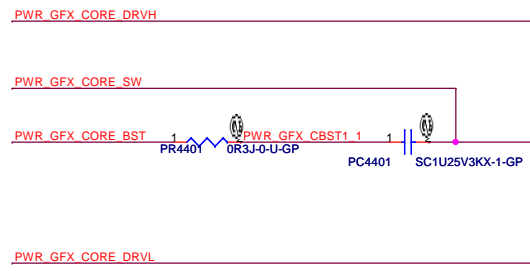
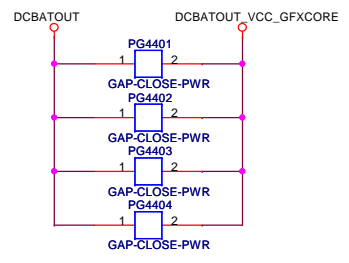
Size Document Number
 <Doc>

Rev
 SD

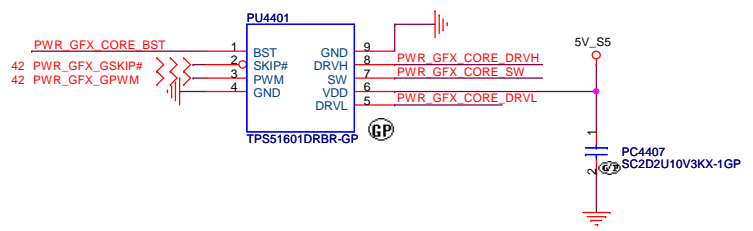
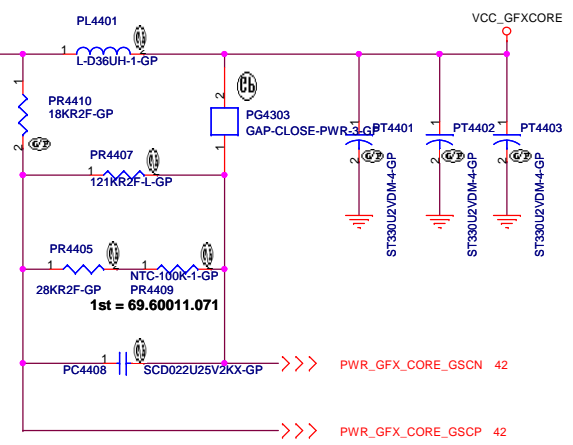
Date: Friday, January 06, 2012 Sheet 43 of 103

	Main source	2nd source
PU4402	84.07608.037 FDMS7608S-GP	
PU4403	84.07608.037 FDMS7608S-GP	

BOM control



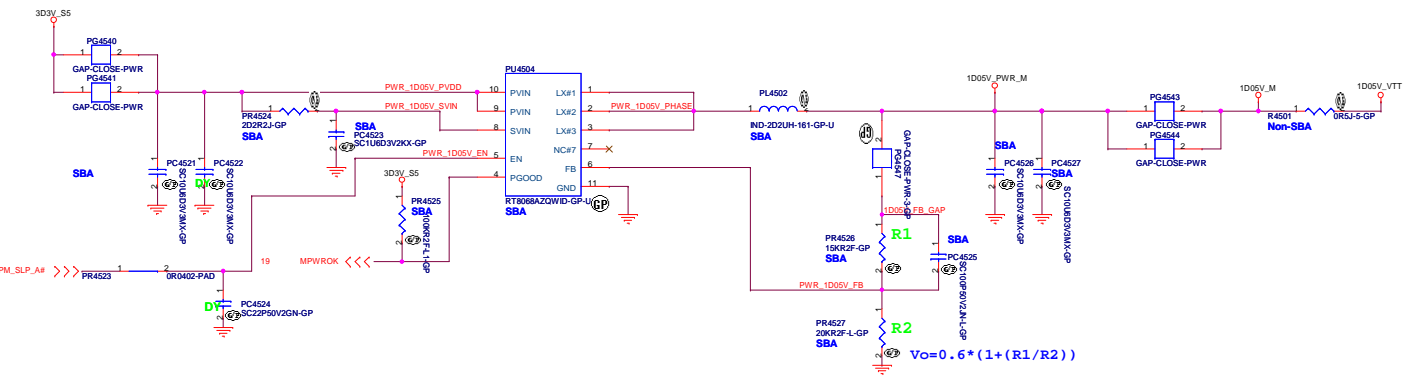
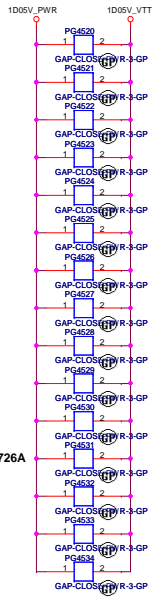
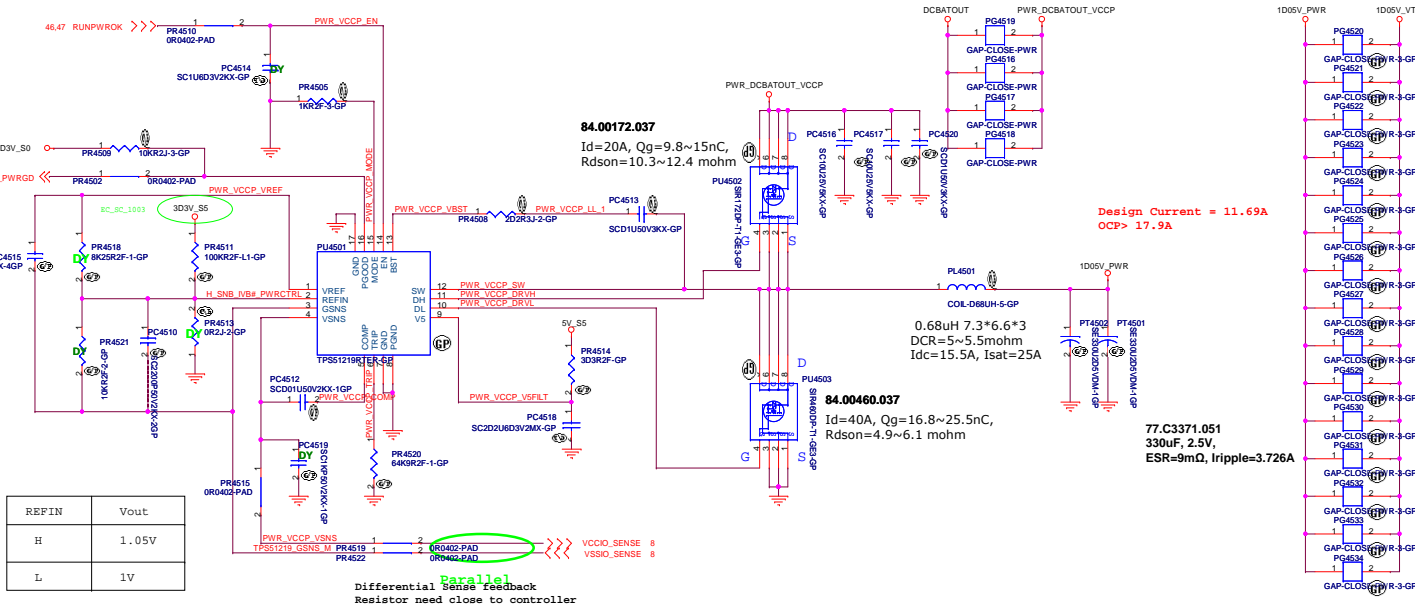
Design current: 22A

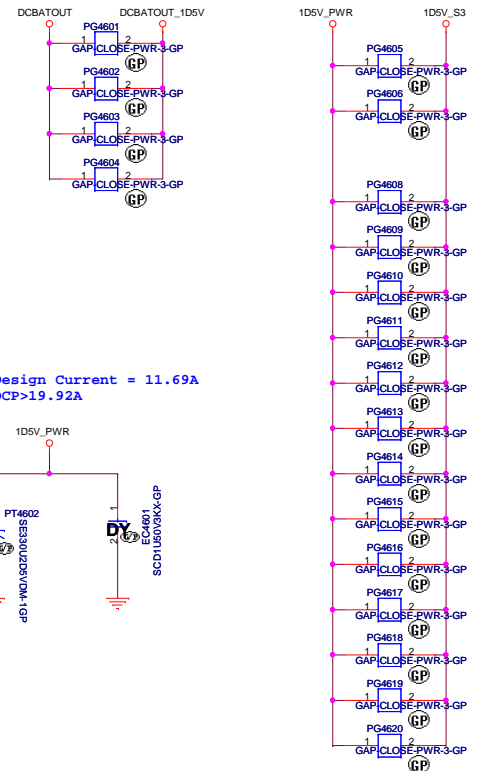
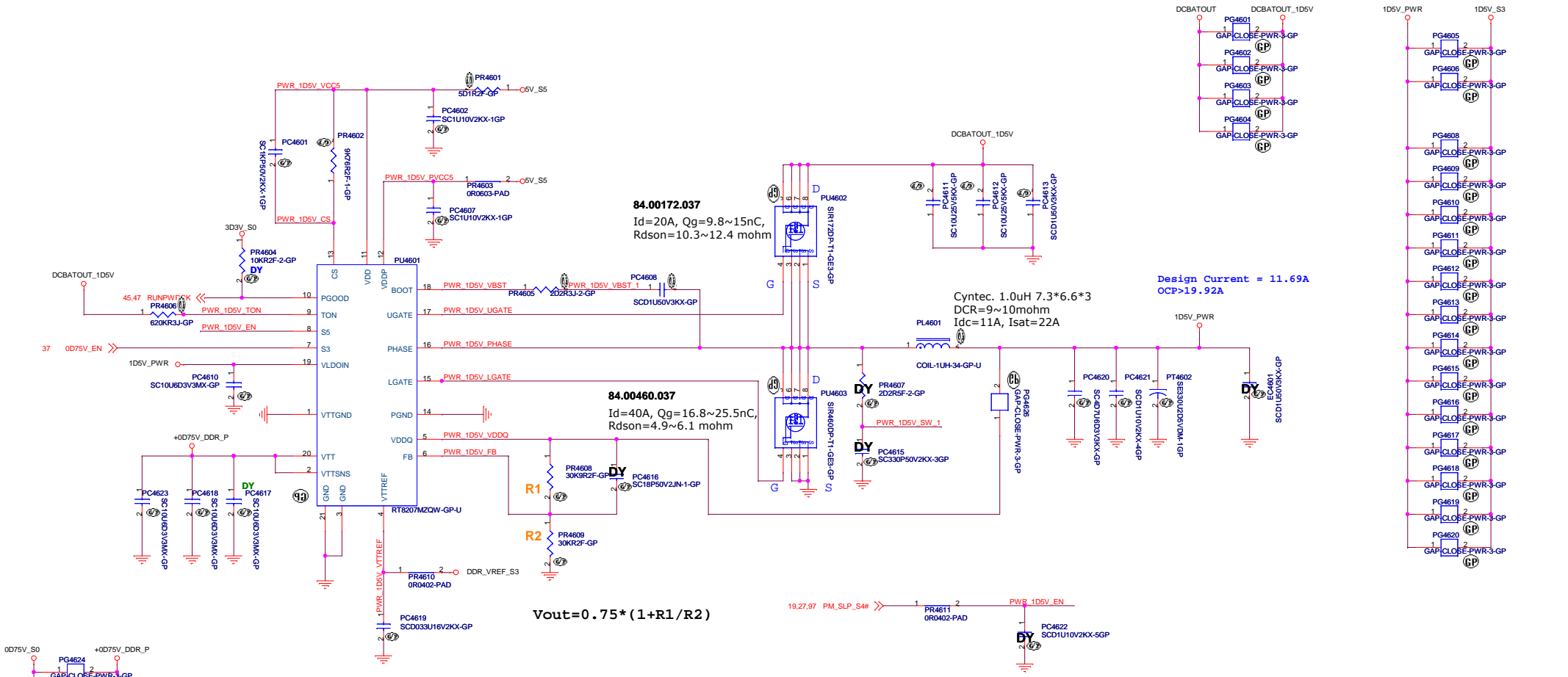


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緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title TPS51640_CPU_CORE(3/3)	
Size	Document Number <Doc>
Date Friday, January 06, 2012	Rev SD
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TPS51219 for 1D05V





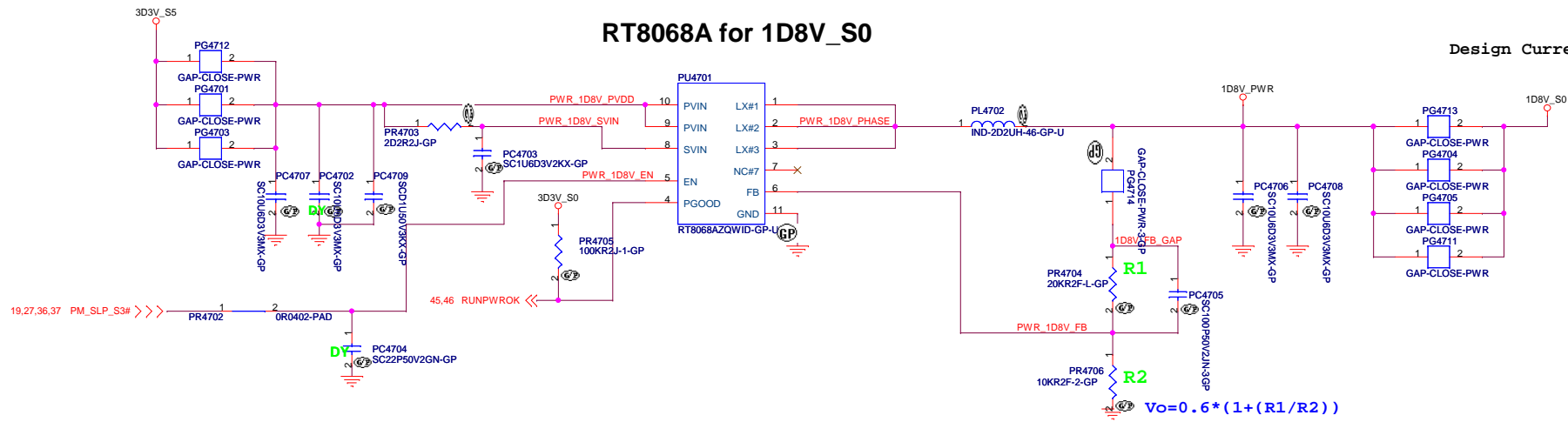
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緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsien Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RT8207M_1D5V_0D75V	
Size	Document Number <Doc> Rev SD
Date: Friday, January 06, 2012	Sheet 46 of 103

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S0

Design Current=1.1A



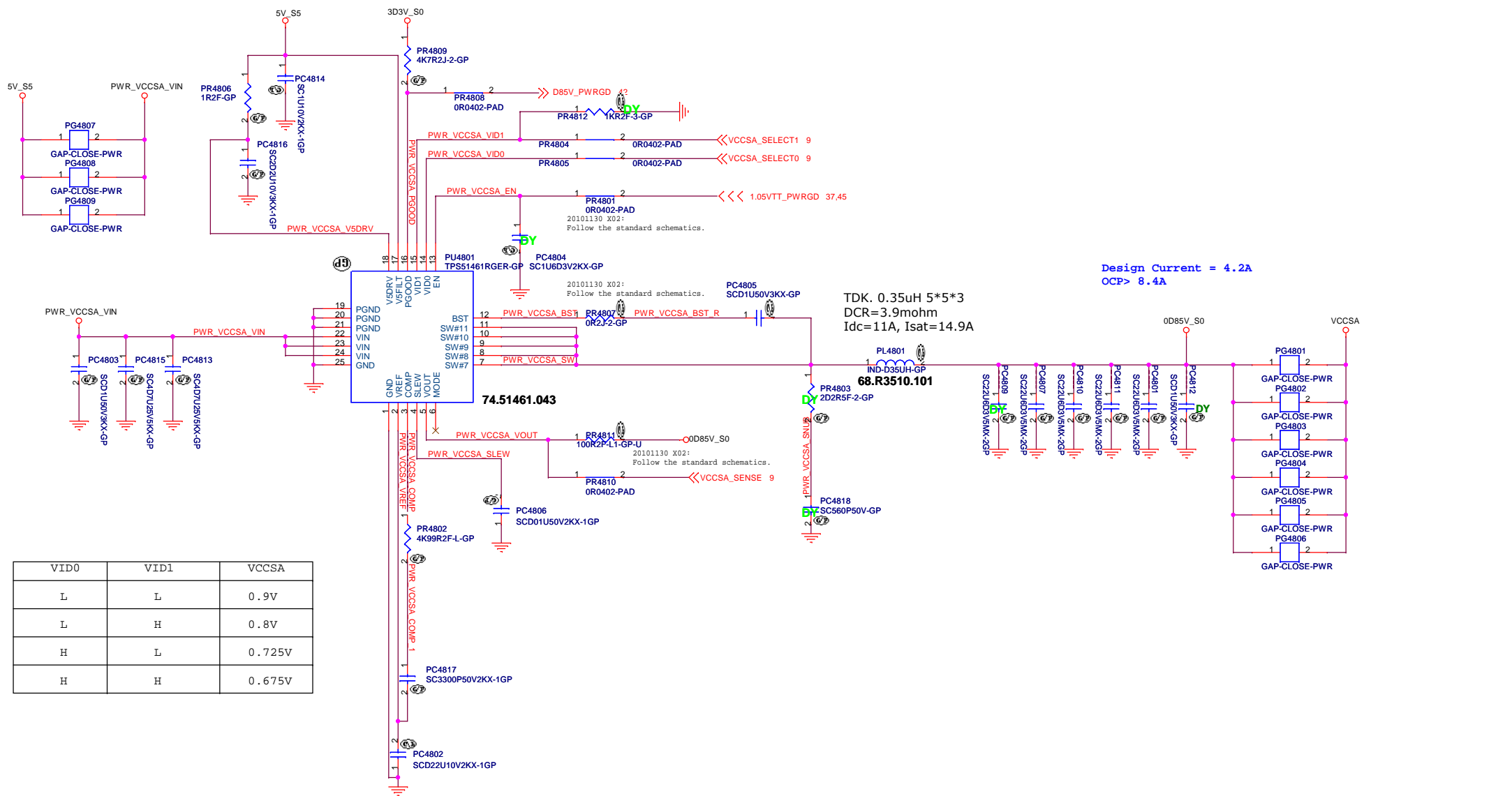
$V_o = 0.6 * (1 + (R1/R2))$

<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title			PWM_1D8V_RT8015B		
Size	Document Number		Rev	SD	
Date:	Friday, January 06, 2012	Sheet	47	of	103

TPS51461 for VCCSA



Design Current = 4.2A
OCP > 8.4A

TDK, 0.35uH 5*5*3
DCR=3.9mohm
Idc=11A, Isat=14.9A

<Core Design>

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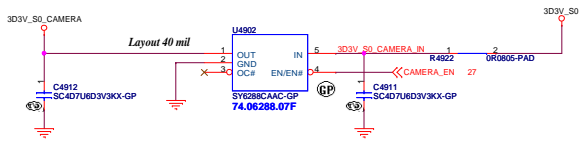
Title: **VCCSA_TPS51461**

Size: Document Number **<Doc>** Rev: **SD**

Date: Friday, January 06, 2012 Sheet 48 of 103

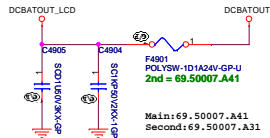
LCD / Inverter Connector

CAMERA POWER

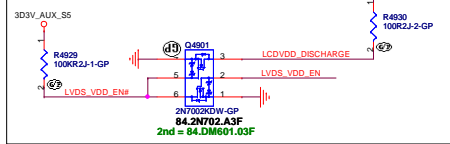


SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
JPI	74.07534.A7F	OBS	High Active
SMT	74.05240.A7F	OBS	High Active

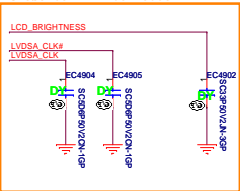
LCD POWER



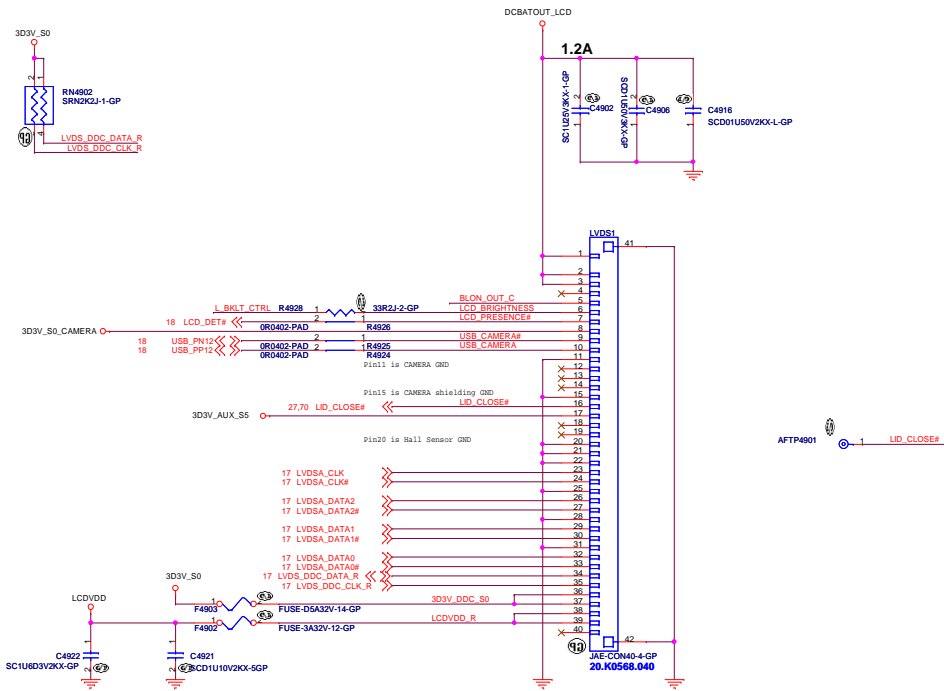
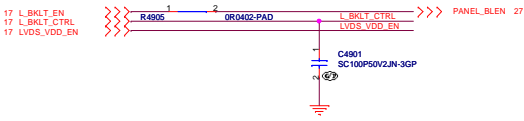
LCDVDD Discharge



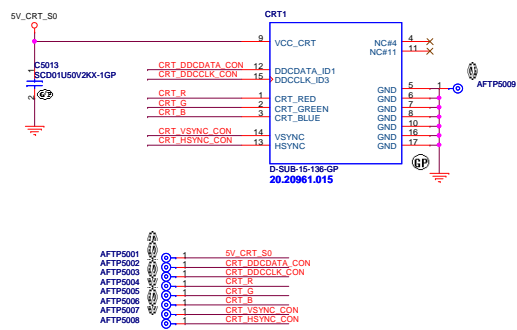
For EMI request
Close to LVDS connector



Panel BL brightness/Power En/BL En

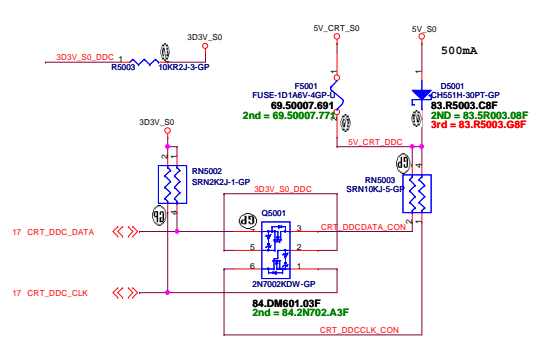


CRT connector

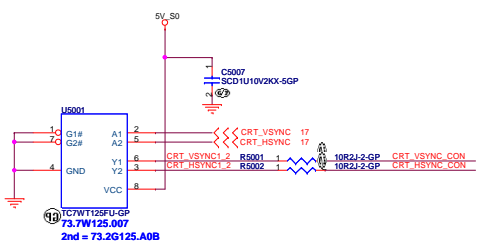


CRT DDCDATA & DDCCLK level shift

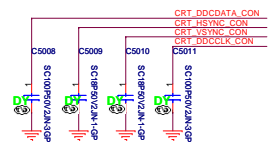
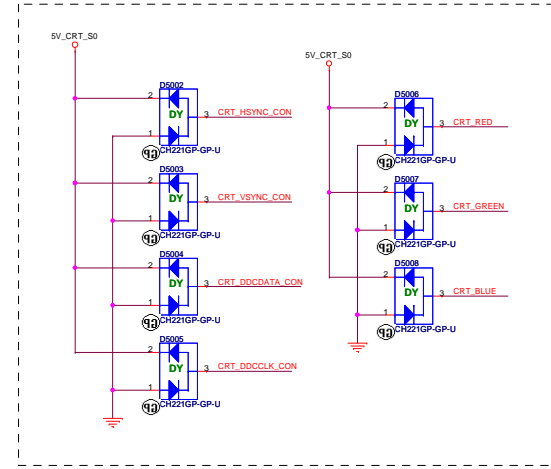
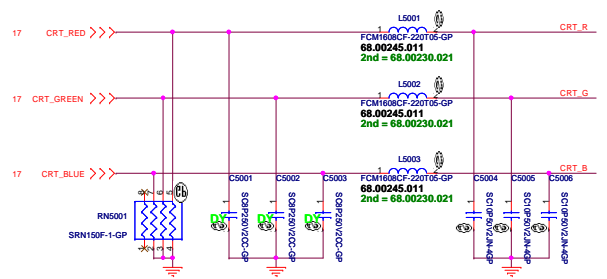
Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift

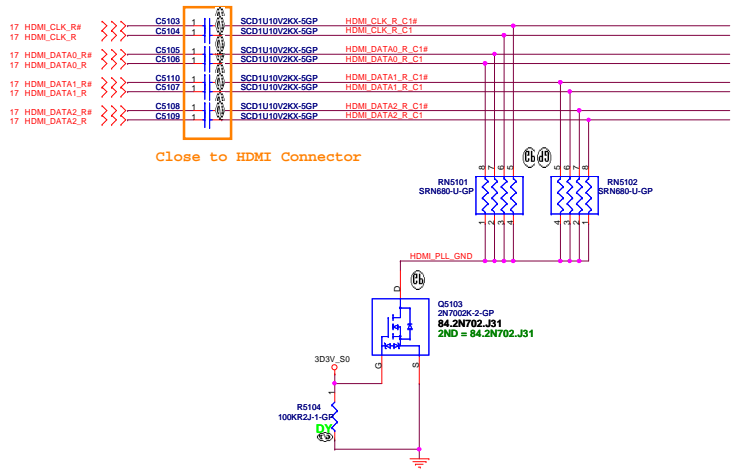


CRT RGB

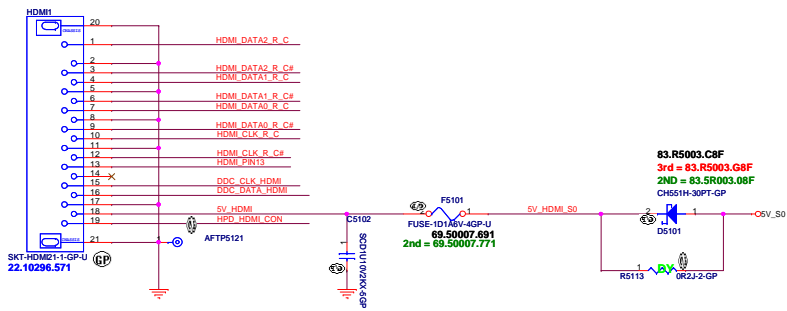


HDMI Passive Level Shifter

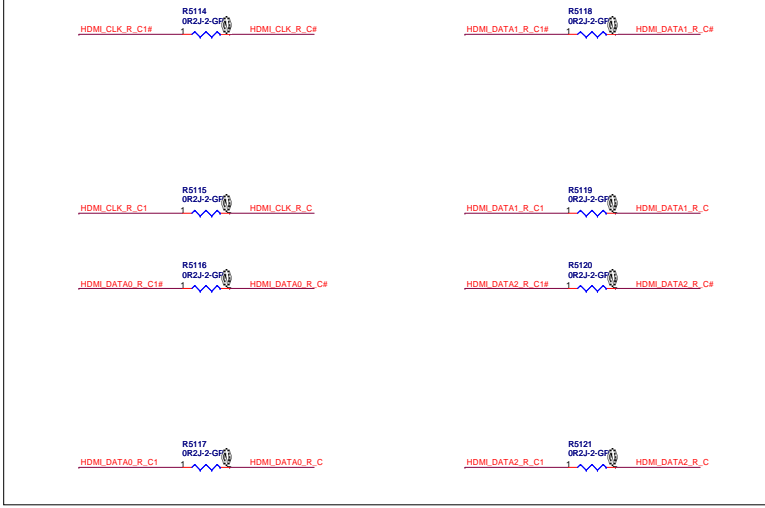
Close to HDMI Connector



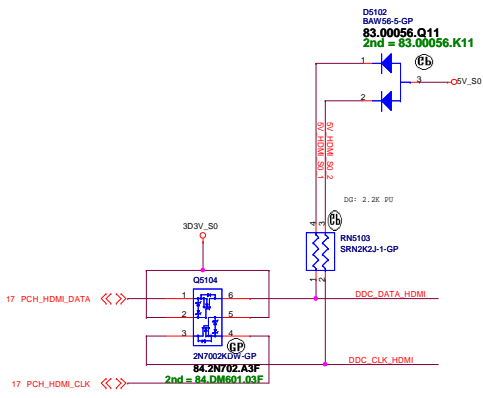
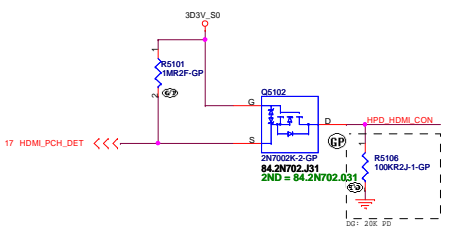
HDMI CONNECTOR



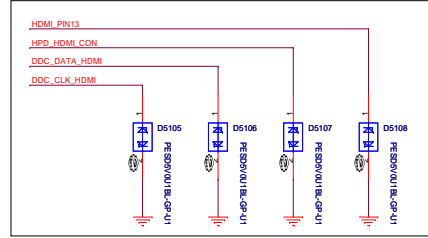
EMI's request



HDMI DDC Passive Level Shifter



ESD Request



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<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

eDP

Size

A4

Document Number

LA480

Rev

SD

Date: Friday, January 06, 2012

Sheet 52 of 103

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<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

S-VIDEO

Size
A4

Document Number

LA480

Rev
SD

Date: Friday, January 06, 2012

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<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

LA480

Rev

SD

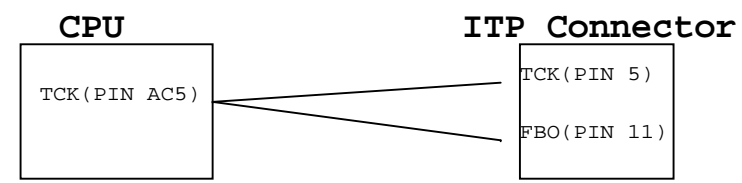
Date: Friday, January 06, 2012

Sheet 54 of 103

SSID = User.Interface

ITP Connector

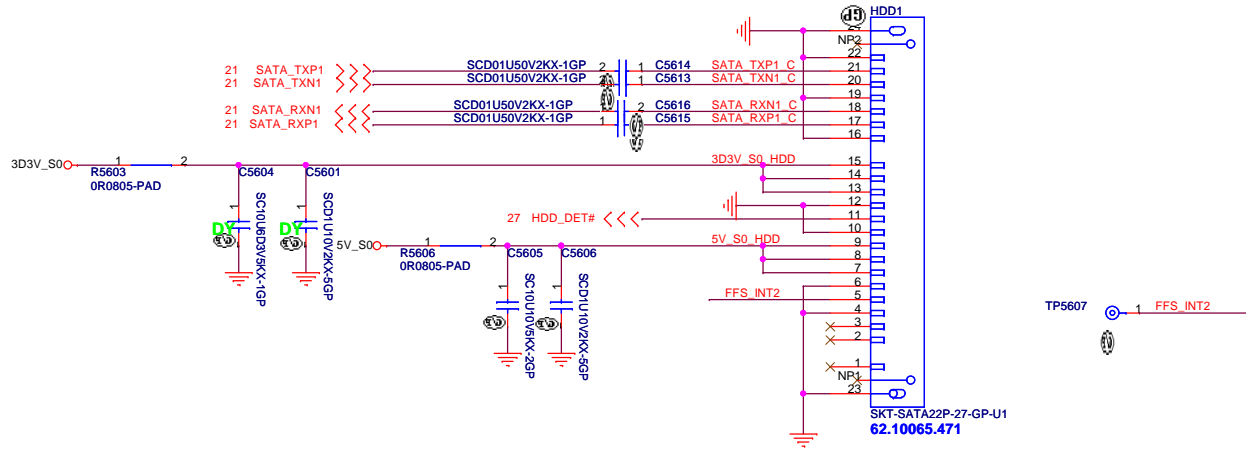
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ITP			
Size	Document Number		Rev
A4	LA480		SD
Date: Friday, January 06, 2012		Sheet 55	of 103

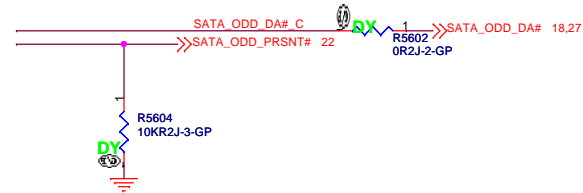
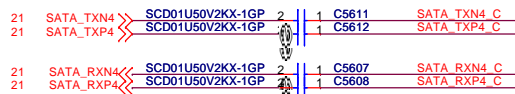
SATA HDD Connector



ODD Connector

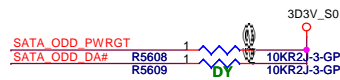
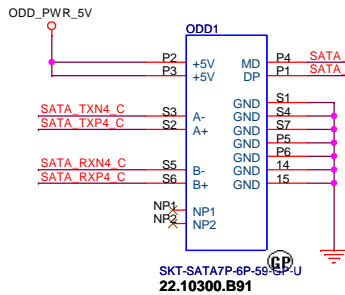
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

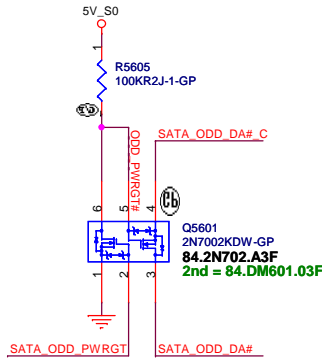


- 74.02069.079 TI TPS2069DGNR MSOP 8P
- 74.07534.D79 UPI UF7534PRA8-15 MSOP 8P
- 74.00547.C79 GMT G547F1P81U MSOP 8P (OBS)
- 74.07534.A79 UPI UF7534ARA8-15 MSOP8P

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



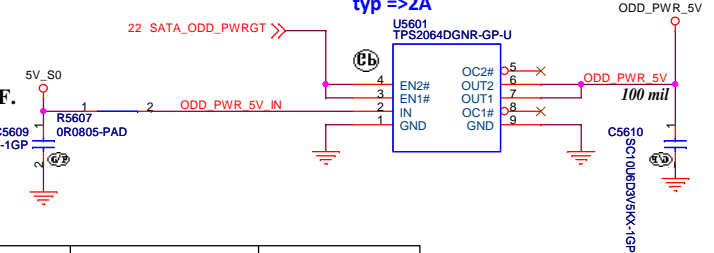
SUPPORT ZERO SATA ODD



TI	74.02069.079	TPS2069DGNR	High Active
DIODES		AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active

SATA Zero Power ODD

Current limit
Active High
typ =>2A



<Core Design>

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Title			HDD/ODD
Size	Document Number	Rev	SD
A3	LA480		
Date:	Friday, January 06, 2012	Sheet	56 of 103

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<Core Design>

緯創資通

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Title

E-SATA+USB

Size
A4

Document Number

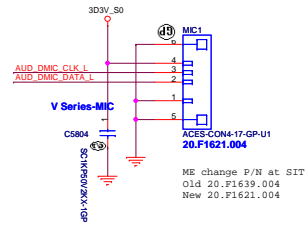
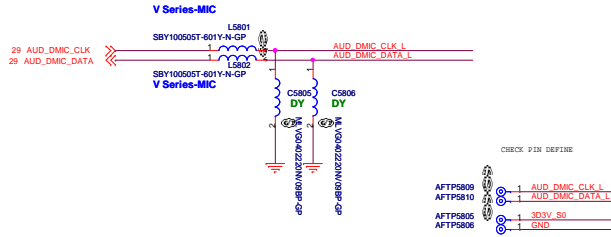
LA480

Rev
SD

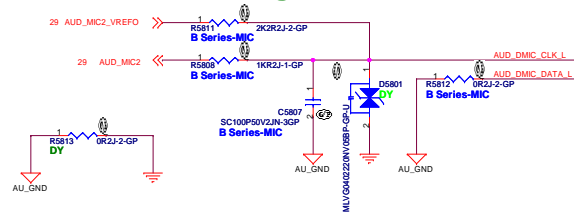
Date: Friday, January 06, 2012

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Int. Digital MIC for V series



Int. Mono Analog MIC for B series



INTERNAL STEREO SPEAKERS

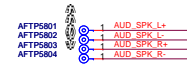
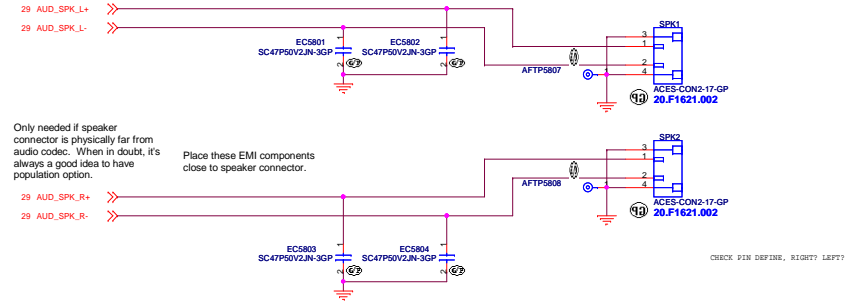


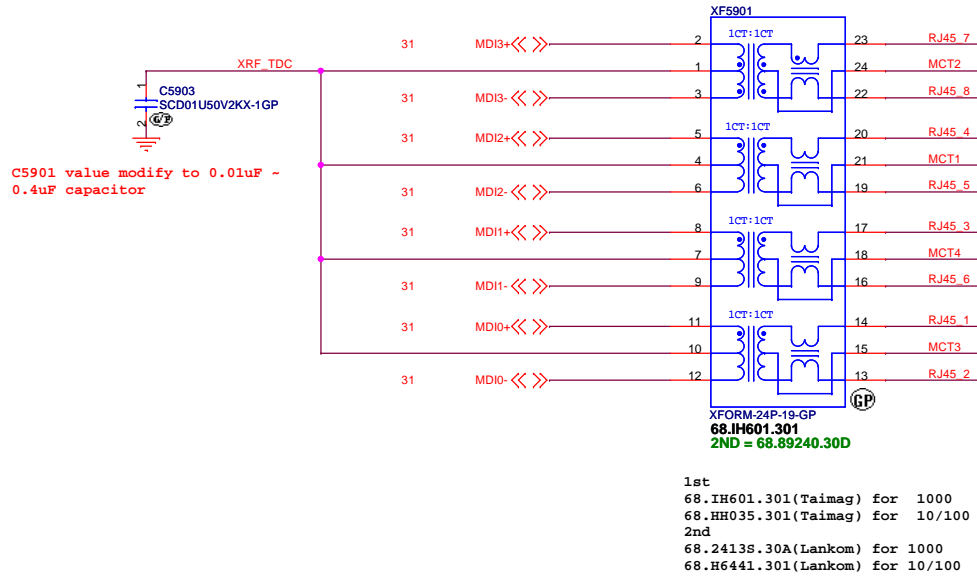
Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

<Core Design>

FOR CO-LAY

GIGA Lan Transformer



TVS

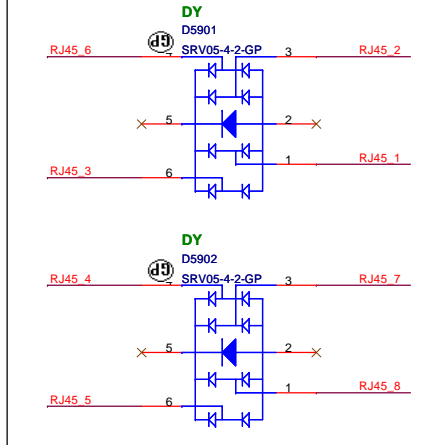
83.00005.BAE

DIODE ARR SRV05-4.TCT SOT-23-6

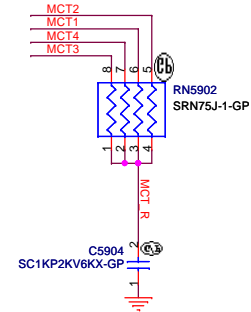
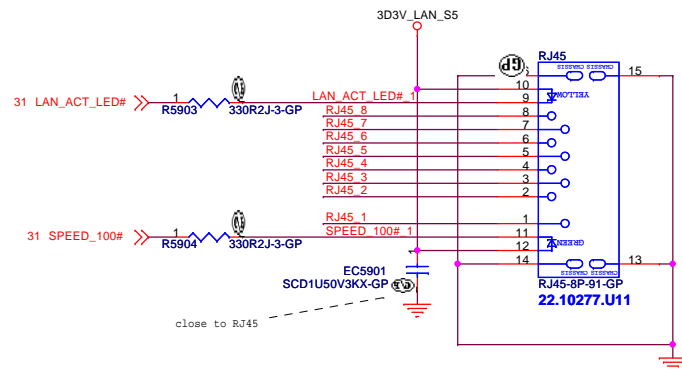
83.09904.AAE

DIODE ESD AZC099-04S SOT23-6L

Swap for V480



LAN Connector



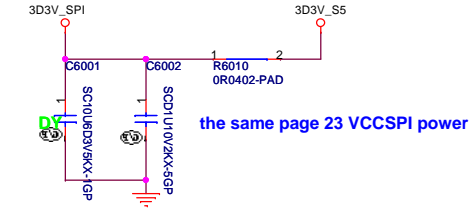
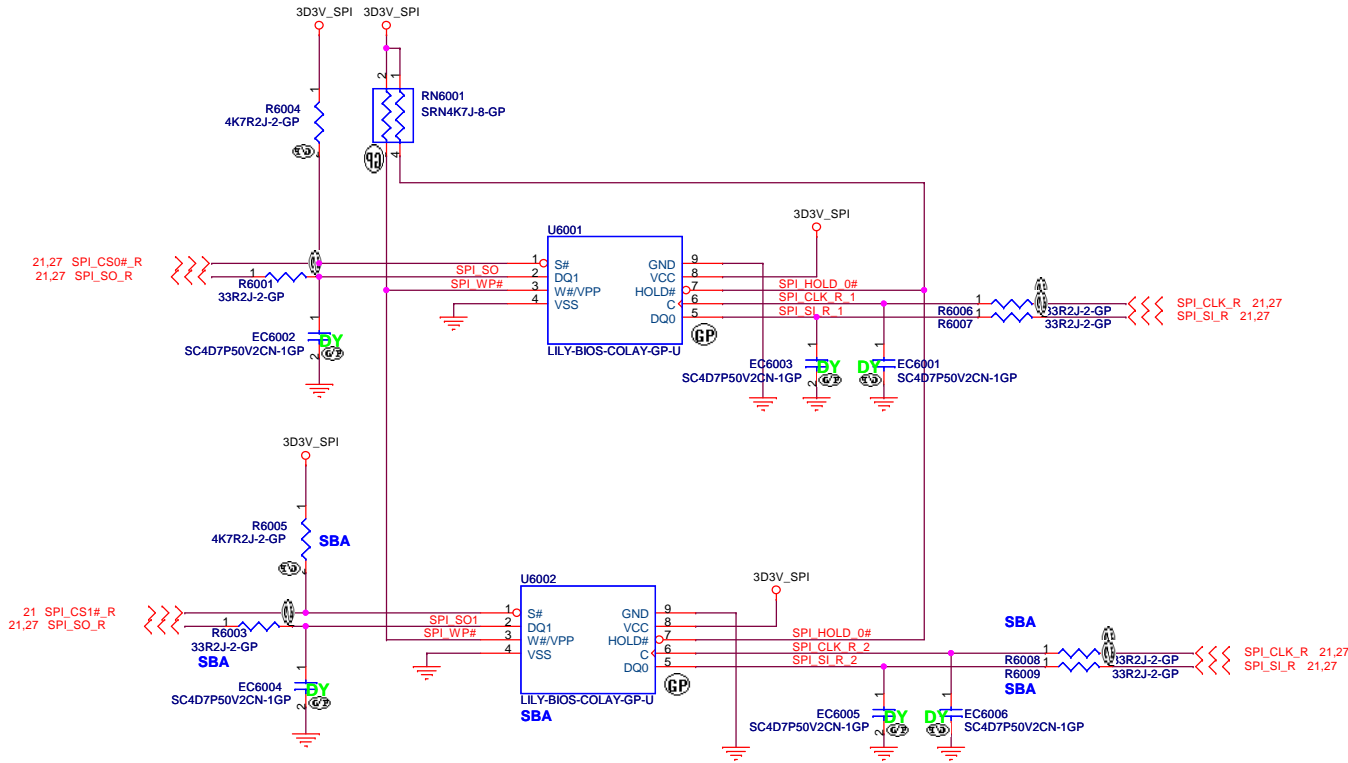
<Core Design>

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Title RJ45 / Transformer		
Size A3	Document Number LA480	Rev SD
Date Friday, January 06, 2012	Sheet 59	of 103

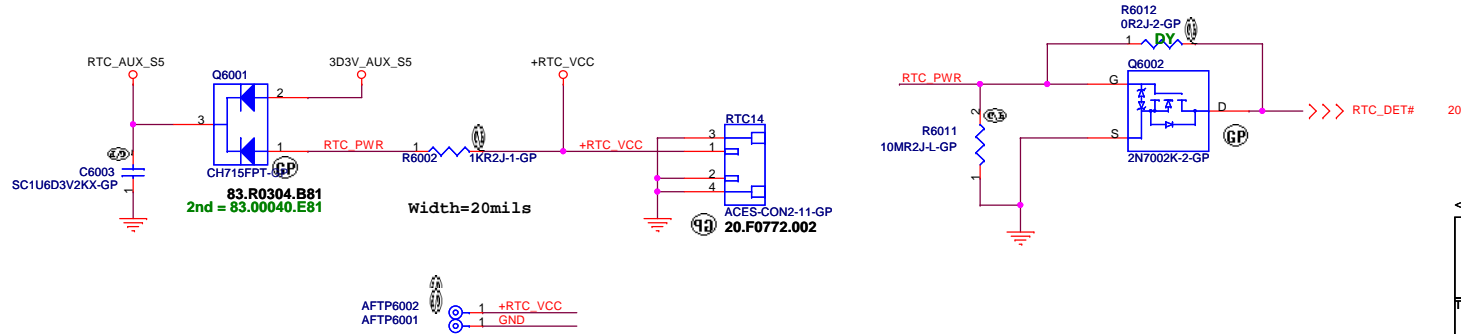
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



4MB			
SO8	Marcronix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Numonyx	N25Q032A13ESE40	72.25032.H01
8MB			
SO8	Marcronix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Numonyx	N25Q064A13ESE40	72.25Q64.D01
16MB			
WSON	Marcronix	MX25L12836EZNI-10G	72.25128.X01
	Marcronix	MX25L12835EZNI-10G	72.25128.Y01
	Winbond	W25Q128BVEIG	72.25128.I01
Numonyx	N25Q128A13EF840	72.25128.B03	

SSID = RBATT



<Core Design>

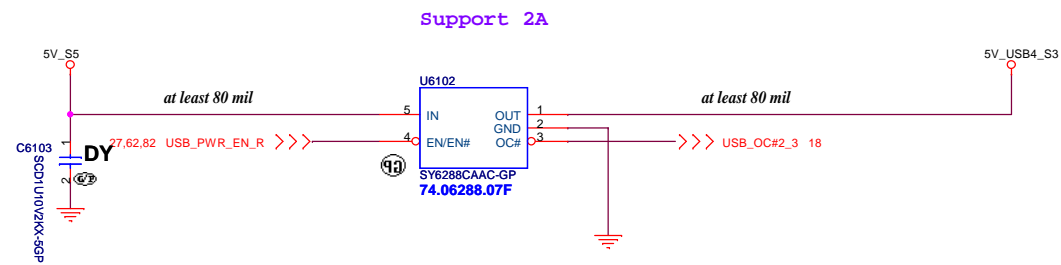
緯創資通 Wistron Corporation
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Title: **Flash/RTC**

Size A3 Document Number: **LA480** Rev: **SD**

Date: Friday, January 06, 2012 Sheet 60 of 103

USB Board CONN.



Place U6102 close to USBCN1

<Core Design>

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB Connector	
Title Size A3	Document Number LA480
Date: Friday, January 06, 2012	Rev SD
Sheet 61 of 103	1

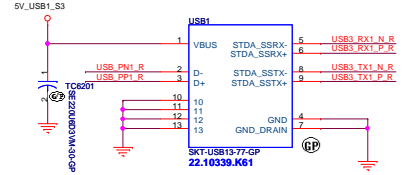
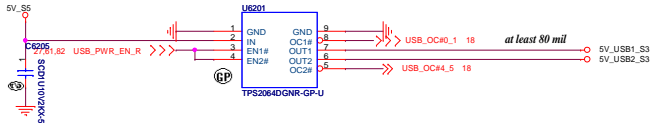
USB3.0 Port1

USB3.0 Port2

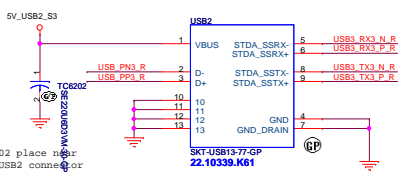
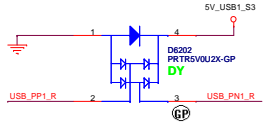
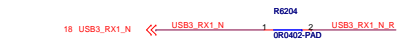
USB3.0 Port3

USB3.0 Port4

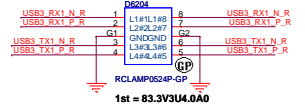
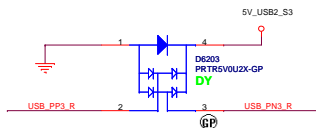
2A



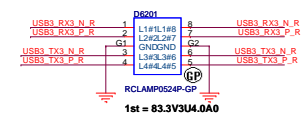
TC6201 place near the USB1 connector



TC6202 place near the USB2 connector



1st = 83.3V3U4.0A0



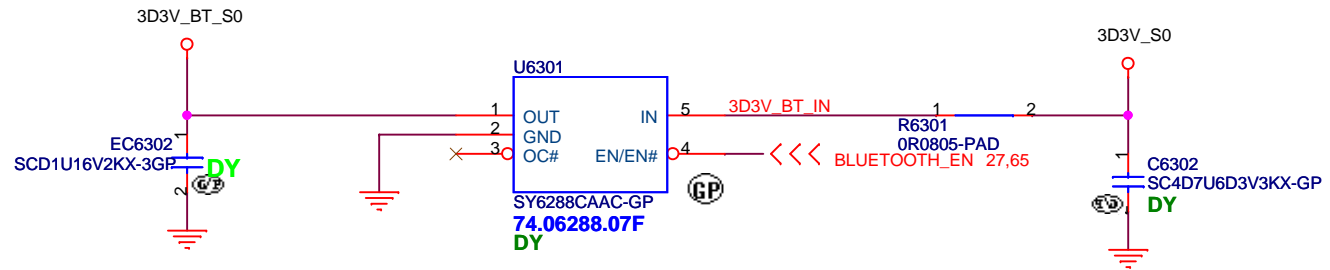
1st = 83.3V3U4.0A0

<Core Design>

		Wistron Corporation 21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsichang, Taipei Hsien 221, Taiwan, R.O.C.
Title: USB 3.0 Port*2		
Size: A2	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet: 62 of 100	1

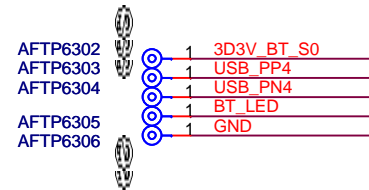
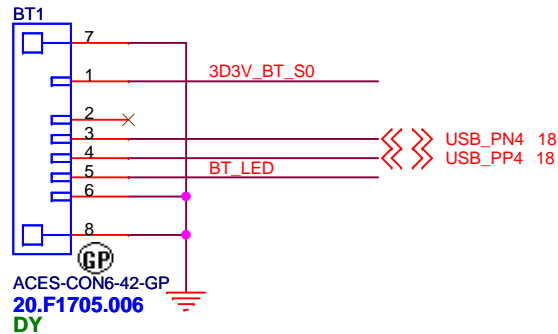
SSID = User.Interface

Bluetooth conn.



SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

BT Module pin definition is same as LA470



<Core Design>

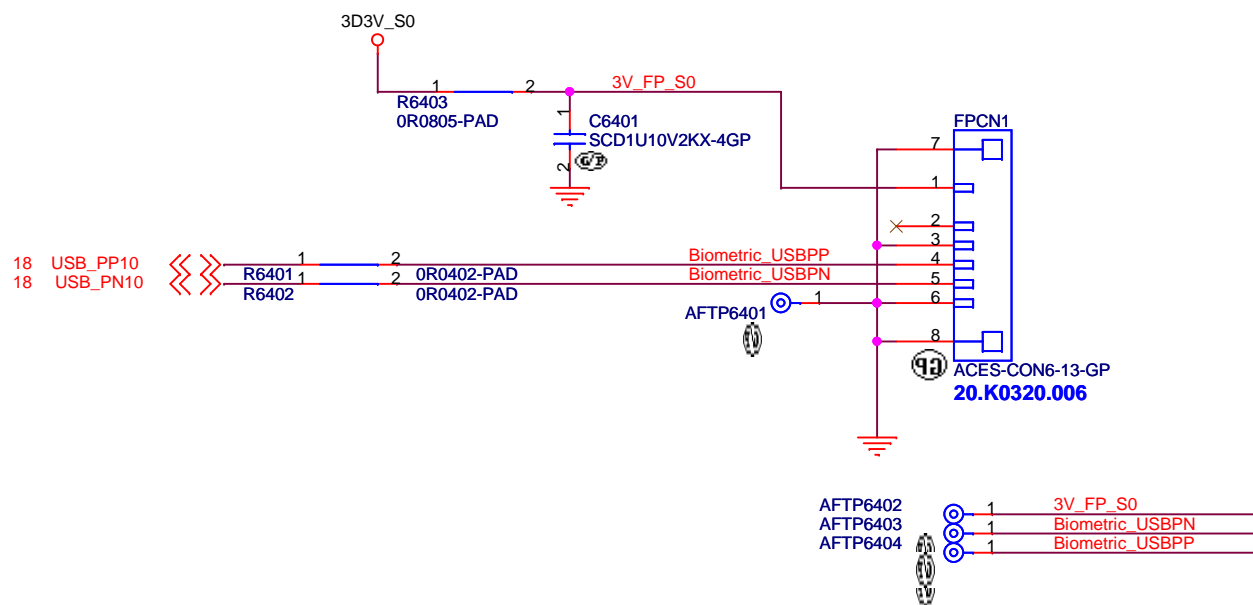

Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Bluetooth**

Size: A4 | Document Number: **LA480** | Rev: **SD**

Date: Friday, January 06, 2012 | Sheet: 63 of 103

Finger Printer Connector

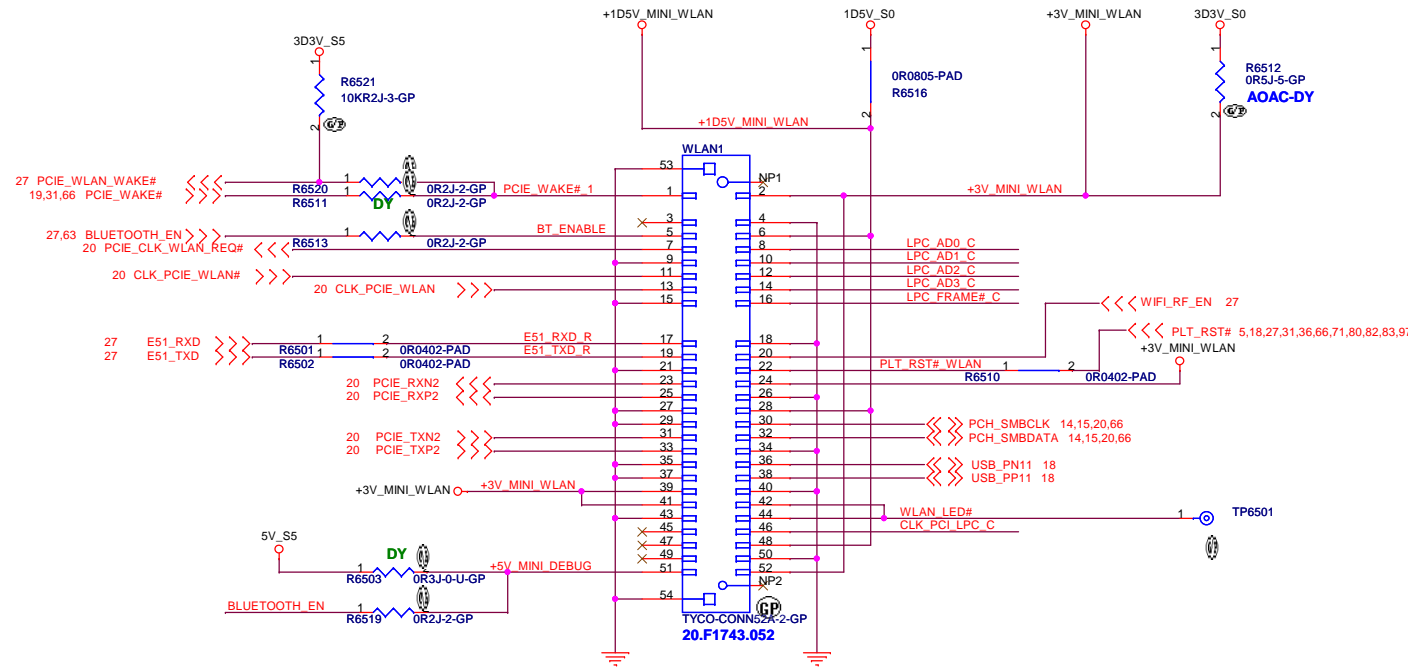


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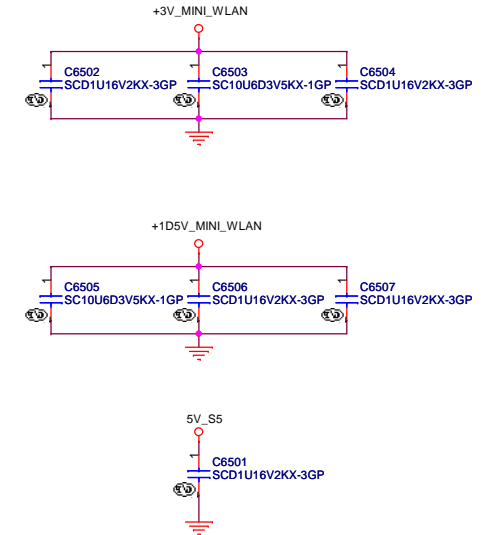
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Finger Printer Connector		
Size A4	Document Number LA480	Rev SD
Date: Friday, January 06, 2012		Sheet 64 of 103

SSID = Wireless

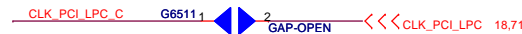
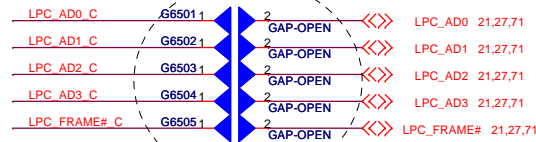
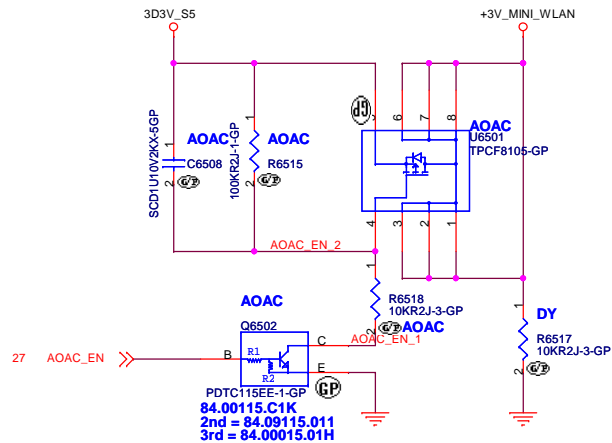
Mini Card Connector(802.11a/b/g/n)



Place near MINI Card CONN



Reserve for AOAC



**G6506~G6511
placement close close WLAN1
in bottom side**

<Core Design>

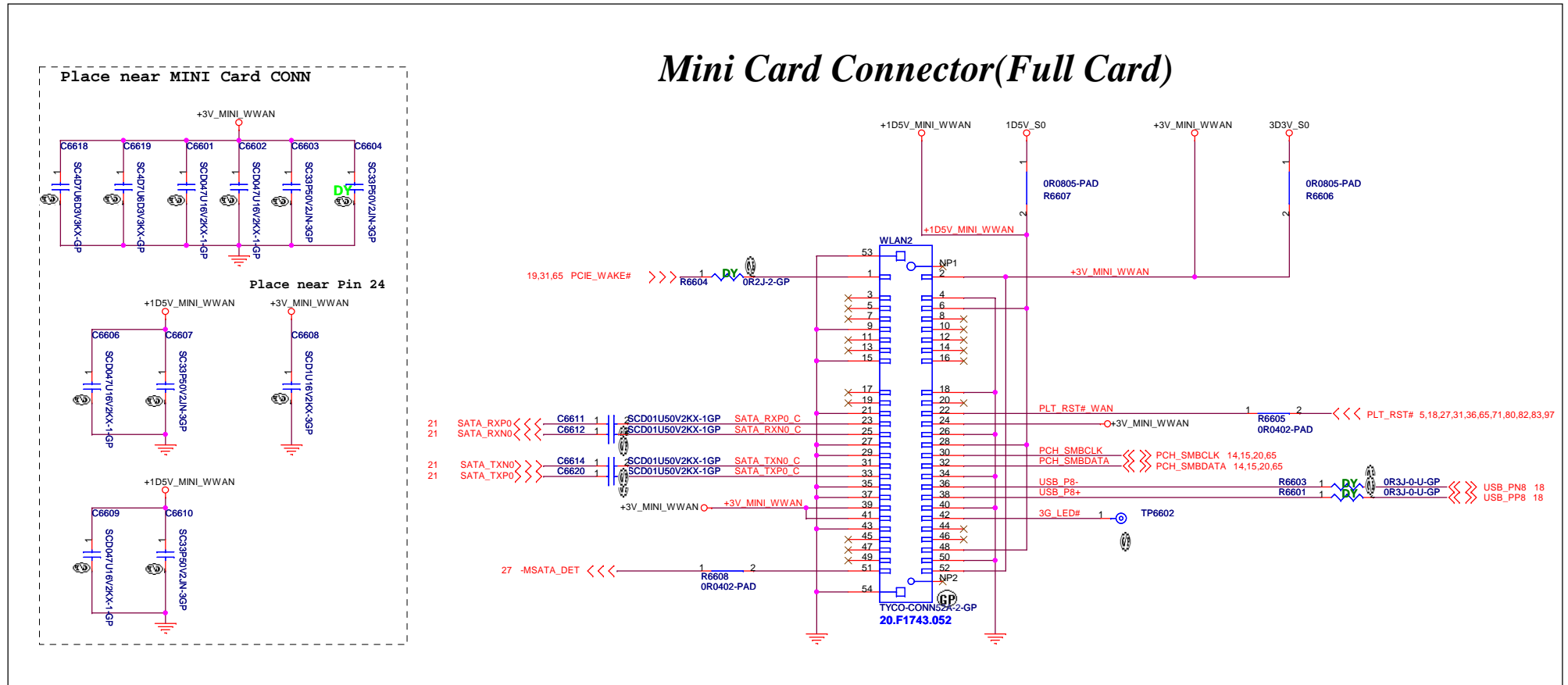
緯創資通 Wistron Corporation
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Title MINICARD(WLAN)/TP CONN		
Size A3	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 65	of 103

SSID = Wireless

mSATA for V Series Only

Mini Card Connector(Full Card)



<Core Design>

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WWAN Connector	
Title LA480	Document Number LA480
Size A3	Rev SD
Date Friday, January 06, 2012	Sheet 66 of 103

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<Core Design>

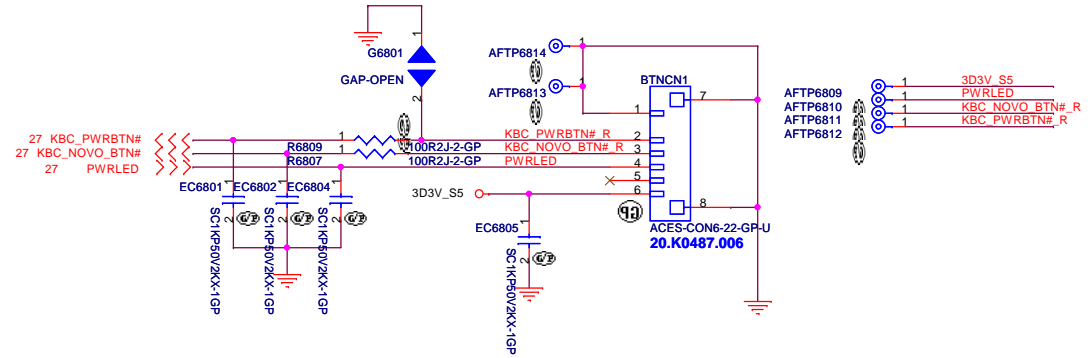
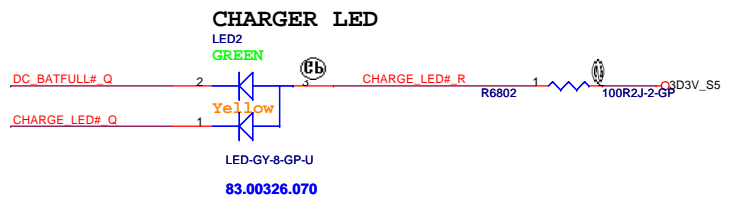
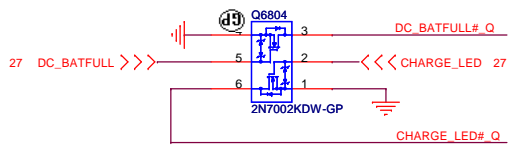
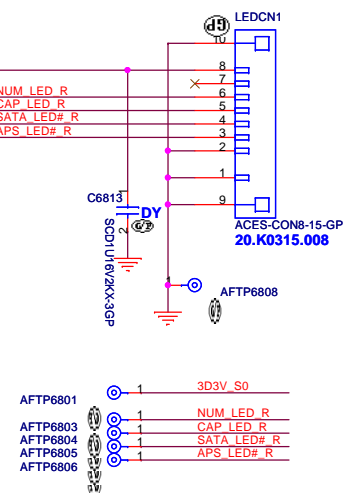
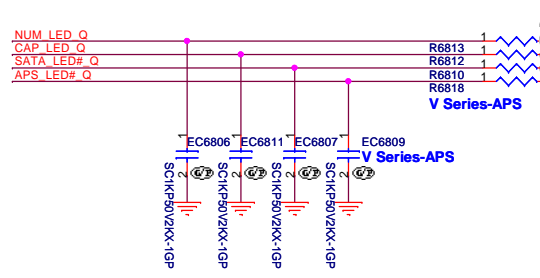
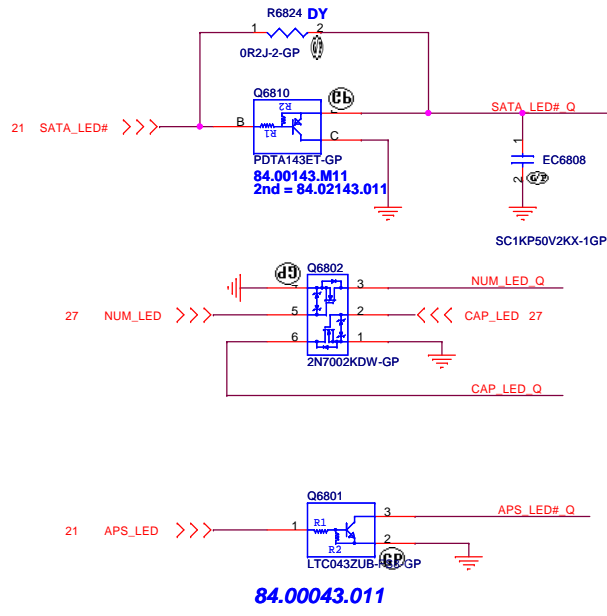
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		
Reserved		

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012	Sheet 67 of	103
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SSID = User.Interface

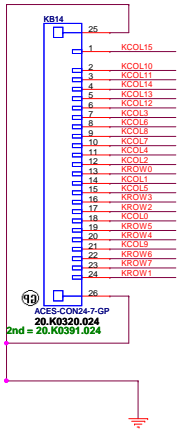


SSID = KBC

Internal Keyboard Connector

<<KROW[8..7] 27
>>KCCL[0..15] 27

- KCCL15 1 AFTP6904
- KCCL10 1 AFTP6905
- KCCL11 1 AFTP6906
- KCCL14 1 AFTP6907
- KCCL13 1 AFTP6908
- KCCL12 1 AFTP6909
- KCCL3 1 AFTP6910
- KCCL5 1 AFTP6911
- KCCL2 1 AFTP6912
- KCCL4 1 AFTP6913
- KCCL1 1 AFTP6914
- KCCL6 1 AFTP6915
- KCCL7 1 AFTP6916
- KCCL8 1 AFTP6917
- KCCL9 1 AFTP6918
- KROW3 1 AFTP6919
- KROW2 1 AFTP6920
- KCCL6 1 AFTP6921
- KCCL9 1 AFTP6922
- KROW5 1 AFTP6923
- KCCL4 1 AFTP6924
- KCCL5 1 AFTP6925
- KROW7 1 AFTP6926
- KCCL1 1 AFTP6927
- KROW1 1 AFTP6928
- GND 1

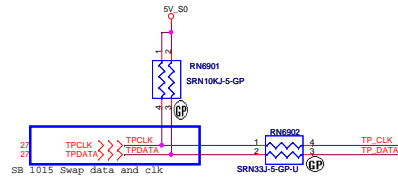


KB14 for 14" VB480 & VB485
KB15 for 15" VB580 & VB585

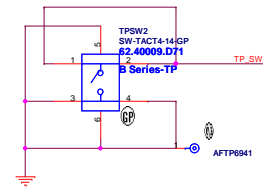
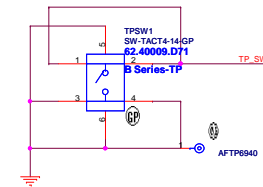
* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

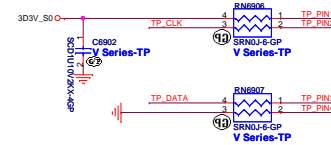
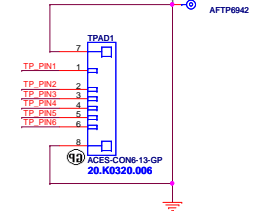
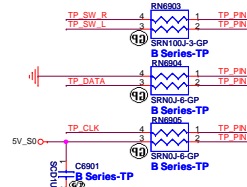
SSID = Touch.Pad



- AFTP6901 1 TP_PIN5
- AFTP6900 1 TP_PIN5
- AFTP6929 1 TP_PIN4
- AFTP6931 1 TP_PIN1
- AFTP6932 1 TP_PIN2
- AFTP6939 1 TP_PIN3
- AFTP6902 1 TP_SW_L
- AFTP6903 1 TP_SW_R



Normal Pad for B Series 5V
ClickPad for V Series 3.3V



	Models			
Synaptics P/N	B480	V480	B580	V580
TM-01146-006	✓			
TM-02022-001		✓		
TM-02060-001			✓	
TM-02045-001				✓
VDD	5V	3.3V	5V	3.3V
Pin 1	VDD	VDD	VDD	VDD
Pin 2	CLK	CLK	CLK	CLK
Pin 3	DAT	DAT	DAT	DAT
Pin 4	Left button	GND	GND	GND
Pin 5	Right button	NC	Left button	NC
Pin 6	GND	NC	Right button	NC

<Core Design>

緯創資通 Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsichang,
Taipei Hsien 221, Taiwan, R.O.C.

Title				Rev
TOUCH PAD CONNECTOR				SD
Size A2	Document Number	LA480		
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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size
A4

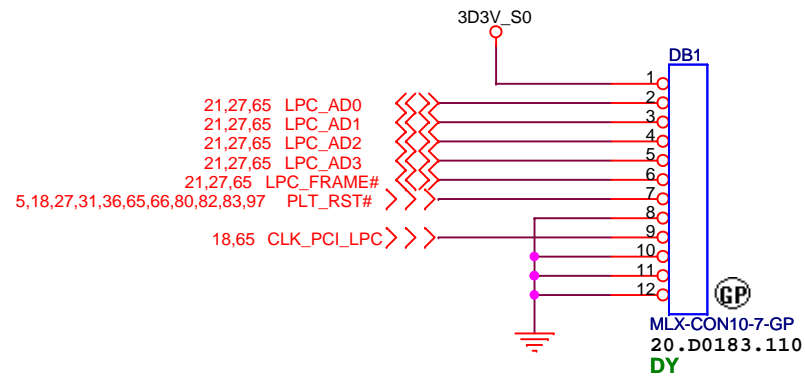
Document Number

LA480

Rev
SD

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<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

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<Core Design>

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Title

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4	Document Number LA480	Rev SD
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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CARD Reader CONN		
Size A2	Document Number LA480	Rev. SD
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<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		
New Card		

Size	Document Number	Rev
A4	LA480	SD

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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<Core Design>

緯創資通

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Title

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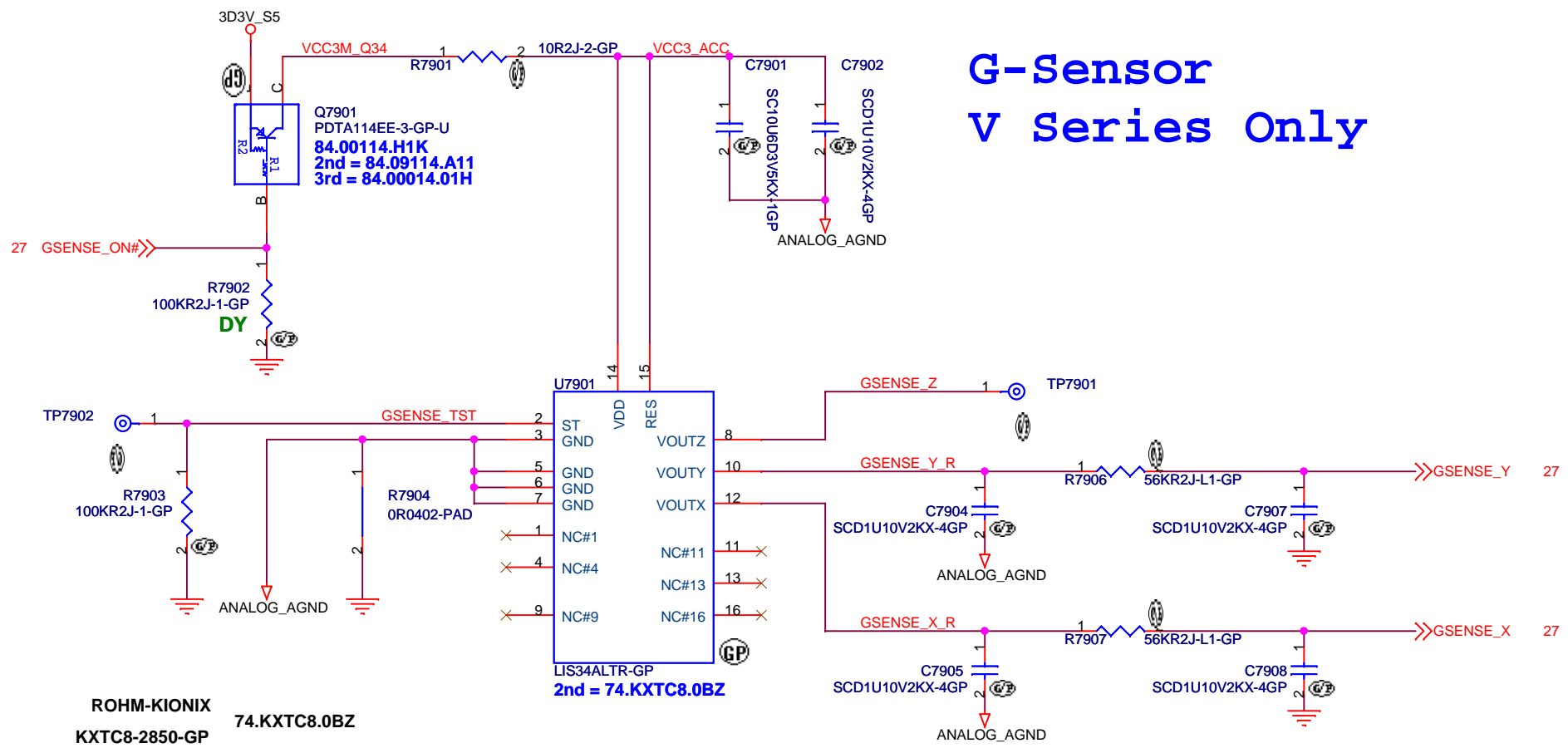
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title	
Reserved	

Size	Document Number	Rev
A4	LA480	SD

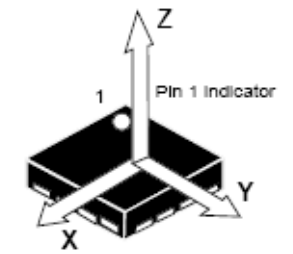
Date: Friday, January 06, 2012	Sheet 78 of 103
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G-Sensor V Series Only



Layout Comment :

- (1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.
- (2) Avoid routing under DCDC switching area.



<Core Design>

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Title

G-Sensor

Size
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SD

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RFID

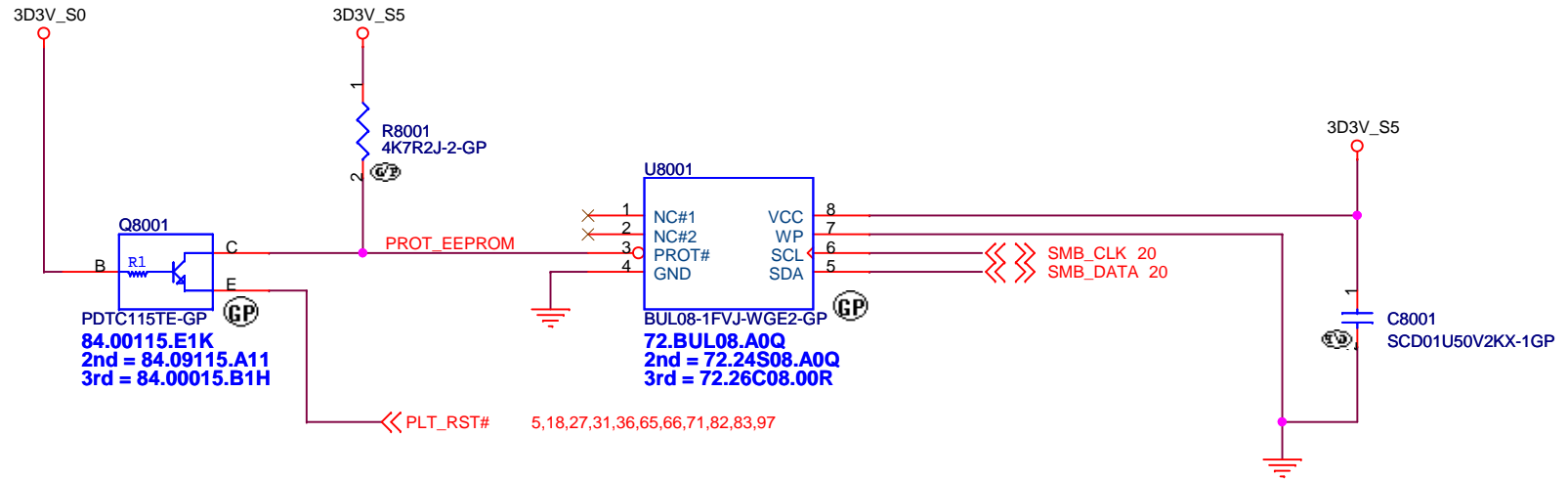



Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
RF ID		
Size A4	Document Number LA480	Rev SD
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size
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Document Number

LA480

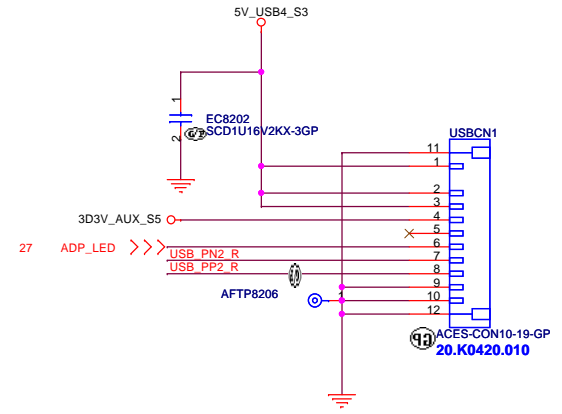
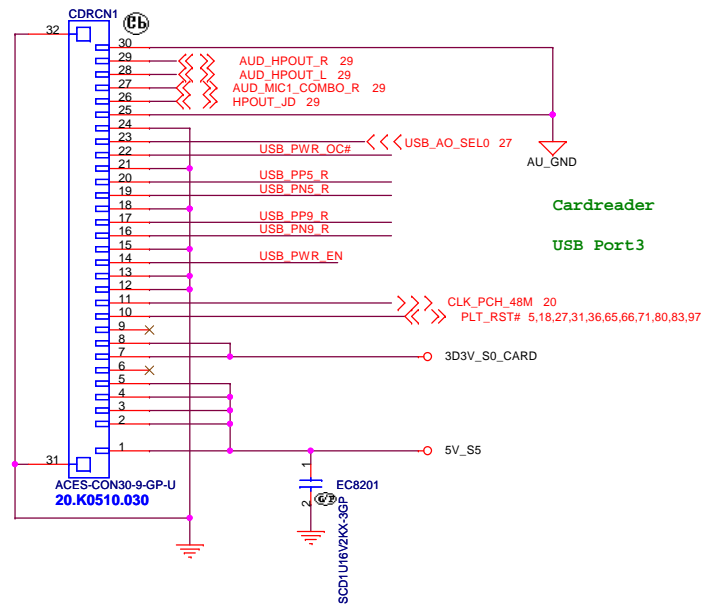
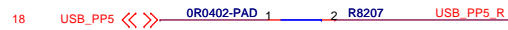
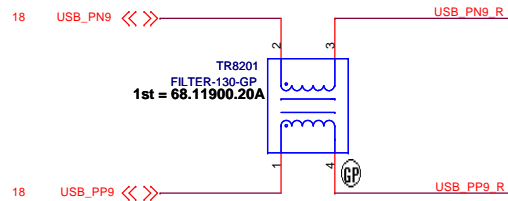
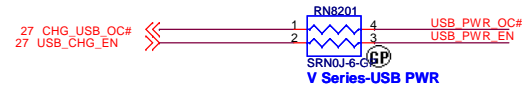
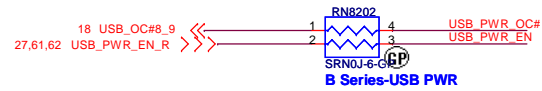
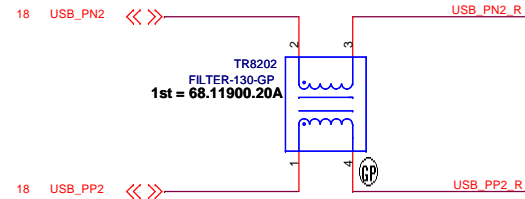
Rev

SD

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R8201 and R8203 Dual layout with TR8201



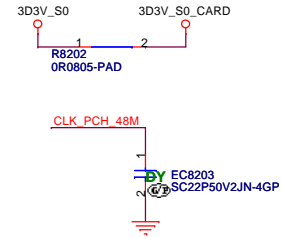
- AFTP8201 1 5V_USB4_S3
- AFTP8202 1 3D3V_AUX_S5
- AFTP8203 1 ADP_LED
- AFTP8204 1 USB_PN2_R
- AFTP8205 1 USB_PP2_R

- AFTP8210 1 HPOUT_JD
- AFTP8213 1 USB_PWR_OC#
- AFTP8223 1 USB_PWR_EN
- AFTP8212 1 USB_AO_SEL0
- AFTP8209 1 AUD_MIC1_COMBO_R

- AFTP8207 1 AUD_HPOUT_R
- AFTP8208 1 AUD_HPOUT_L

- AFTP8211 1 AU_GND

- AFTP8214 1 USB_PP5_R
- AFTP8215 1 USB_PN5_R
- AFTP8216 1 USB_PP9_R
- AFTP8217 1 USB_PN9_R
- AFTP8218 1 CLK_PCH_48M
- AFTP8219 1 PLT_RST#
- AFTP8220 1 3D3V_S0_CARD
- AFTP8221 1 5V_S5
- AFTP8222 1 GND
- AFTP8225 1



<Core Design>

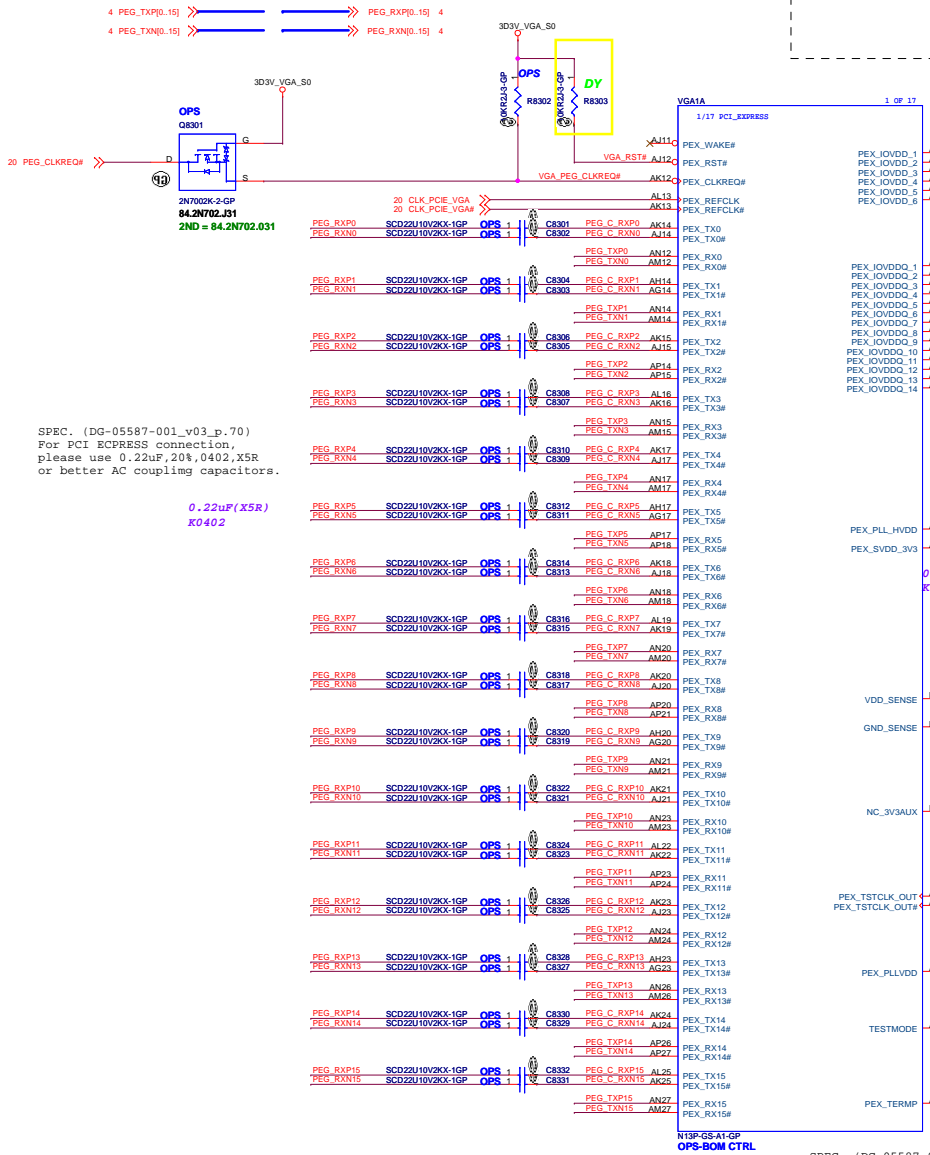
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**

Size A3 Document Number: **LA480** Rev: **SD**

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SPEC. (DG-05587-001_v03_p.70)
 PEX_CLK_REQ_N is an open-drain bi-directional signal;
 by default it should have a 10 kΩ pull-up to 3.3V.
 This signal is an active low signal.



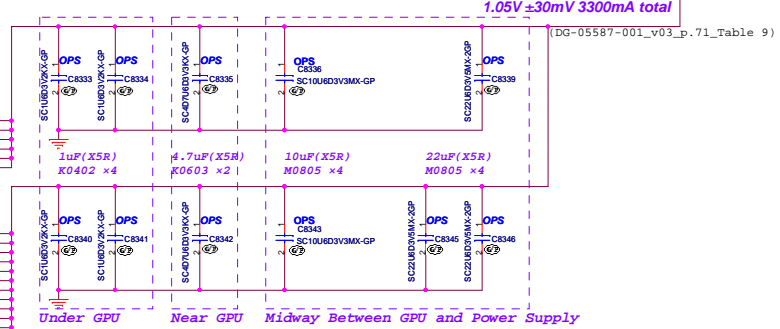
SPEC. (DG-05587-001_v03_p.70)
 For PCI ECPRESS connection,
 please use 0.22uF, 20%, 0402, X5R
 or better AC coupling capacitors.

0.22uF (X5R)
 K0402

PCI Express PEX_IOVVD/Q Combined (DG-05587-001_v03_p.72_Table 10)

Capacitor Type	Footprint	Population	Location
1.0uF	X6S 0402	4	Under GPU
4.7uF	X6S 0603	2	Near GPU
10uF	X5R 0805	4	Midway Between GPU and Power Supply
22uF	X5R 0805	4	Midway Between GPU and Power Supply

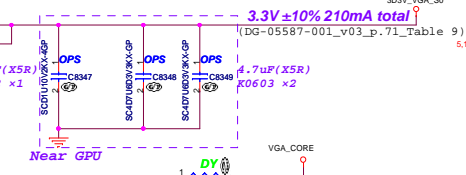
X6S (+/-22% -55-105°C)
 X5R (+/-15% -55-85°C)



PCI Express PEX_SVDD/PLLHVDD Connected to NV3V3 (DG-05587-001_v03_p.72_Table 12)

Capacitor Type	Footprint	Population	Location
0.1uF	X5R 0402	1	Near GPU
4.7uF	X5R 0603	2	Near GPU

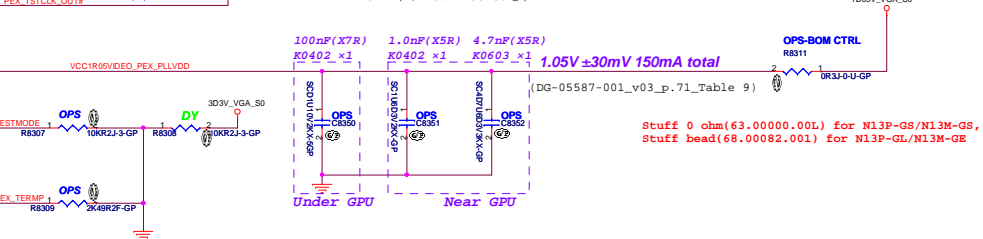
X5R (+/-15% -55-85°C)



PCI Express PEX_PLLVDD (DG-05587-001_v03_p.72_Table 11)

Capacitor Type	Footprint	Population	Location
100mF	X6S 0402	1	Under GPU
1.0uF	X5R 0603	1	Near GPU
4.7uF	X5R 0805	1	Near GPU

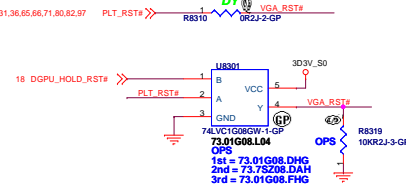
X6S (+/-22% -55-105°C)
 X5R (+/-15% -55-85°C)



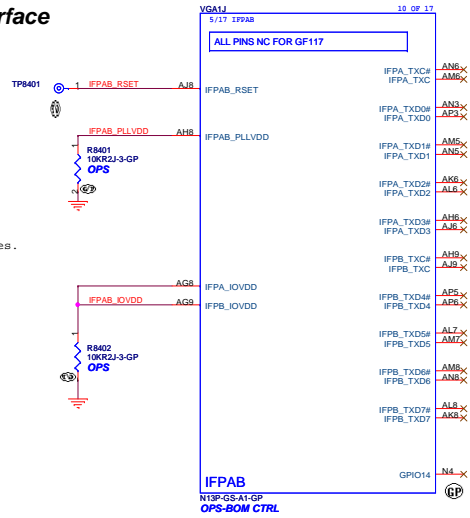
SPEC. (DG-05587-001_v03_p.214)
 By default, pull-down the TESTMODE pin to GND with a 10kΩ resistor.
 For XOR tree testing, TESTMODE should be pulled up to 3v3 with a 10 kΩ resistor.

SPEC. (DG-05587-001_v03_p.70)
 PEX_TERM# is used for internal calibration;
 pull-down this signal with 2.49 kΩ, 1% resistor.

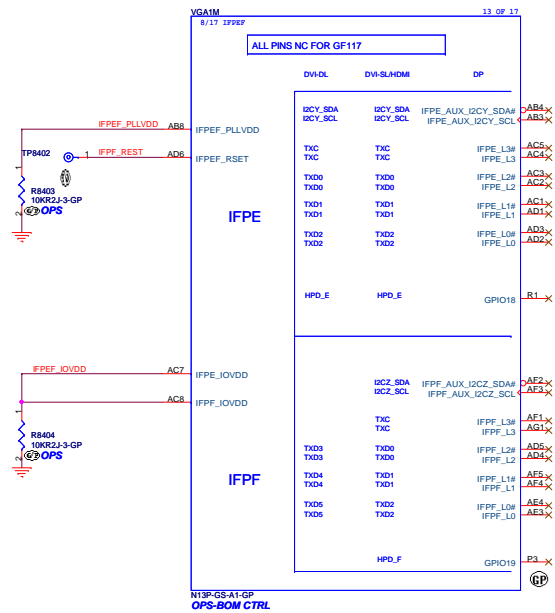
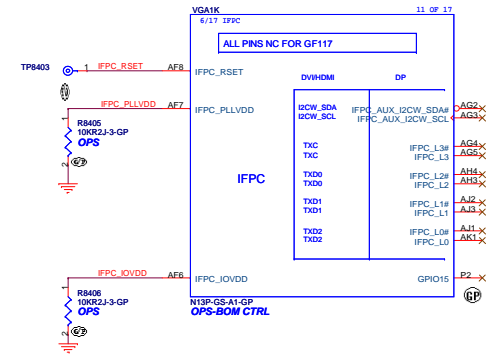
dGPU reset



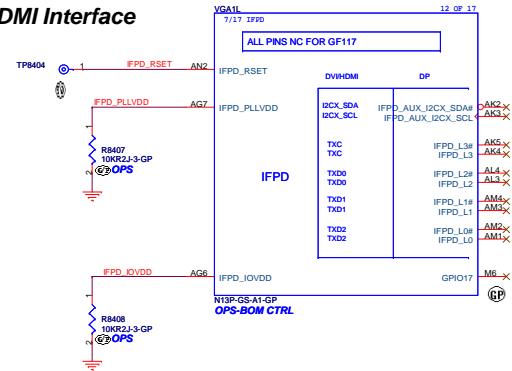
LVDS Interface

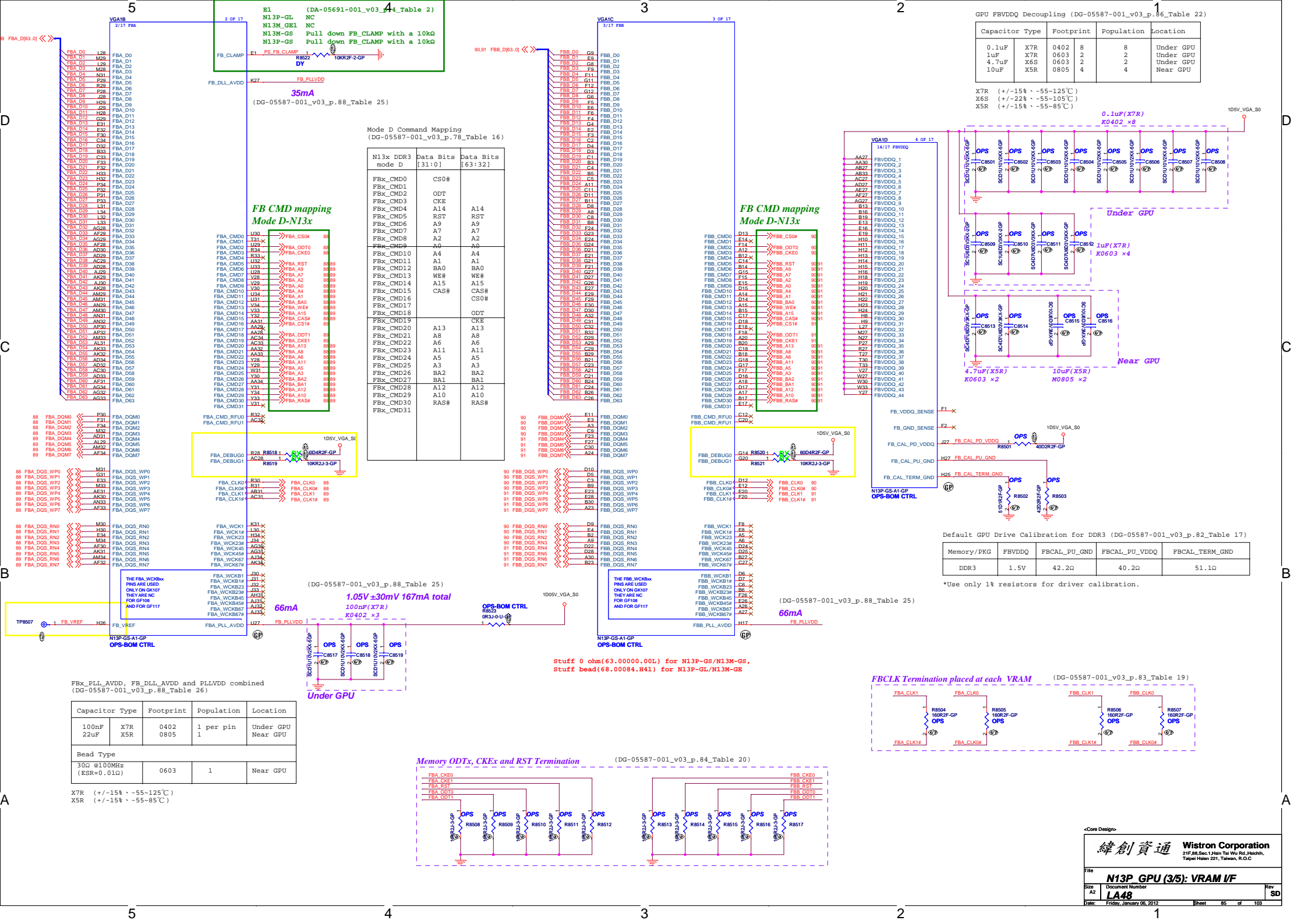


SPEC. (DG-05587-001_v03_p.160)
 Pull down IFPxy IOVDD with 10kΩ resistor.
 Pull down IFPxy PLLVDD with 10kΩ resistor.
 The other IO pins can be NC, this includes unused data lines.



HDMI Interface





GPU FBVDDQ Decoupling (DG-05587-001_v03_p.86_Table 2)

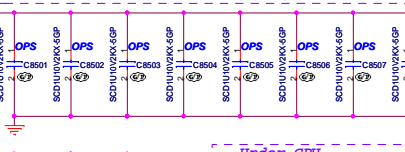
Capacitor Type	Footprint	Population	Location
0.1uF	X7R 0402	8	Under GPU
1uF	X7R 0603	2	Under GPU
4.7uF	X6S 0603	2	Under GPU
10uF	X5R 0805	4	Near GPU

X7R (+/-15% -55-125°C)
 X6S (+/-22% -55-105°C)
 X5R (+/-15% -55-85°C)

Mode D Command Mappings (DG-05587-001_v03_p.78_Table 16)

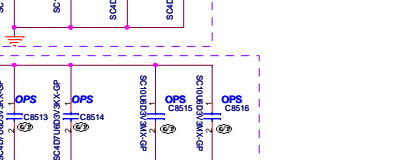
N13x DDR3 mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0#	
FBx_CMD1	ODT	
FBx_CMD2	RST	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A5	A5
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		

0.1uF(X7R) K0402 x8



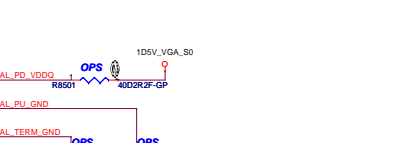
Under GPU

1uF(X7R) K0603 x4



Near GPU

4.7uF(X5R) K0603 x2



10uF(X5R) M0805 x2

Default GPU Drive Calibration for DDR3 (DG-05587-001_v03_p.82_Table 17)

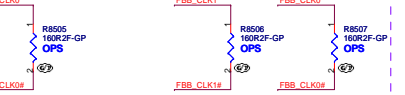
Memory/PKG	FBVDDQ	FBCL_PU_GND	FBCL_PU_VDDQ	FBCL_TERM_GND
DDR3	1.5V	42.2Ω	40.2Ω	51.1Ω

*Use only 1% resistors for driver calibration.

66mA (DG-05587-001_v03_p.88_Table 25)



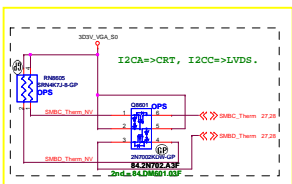
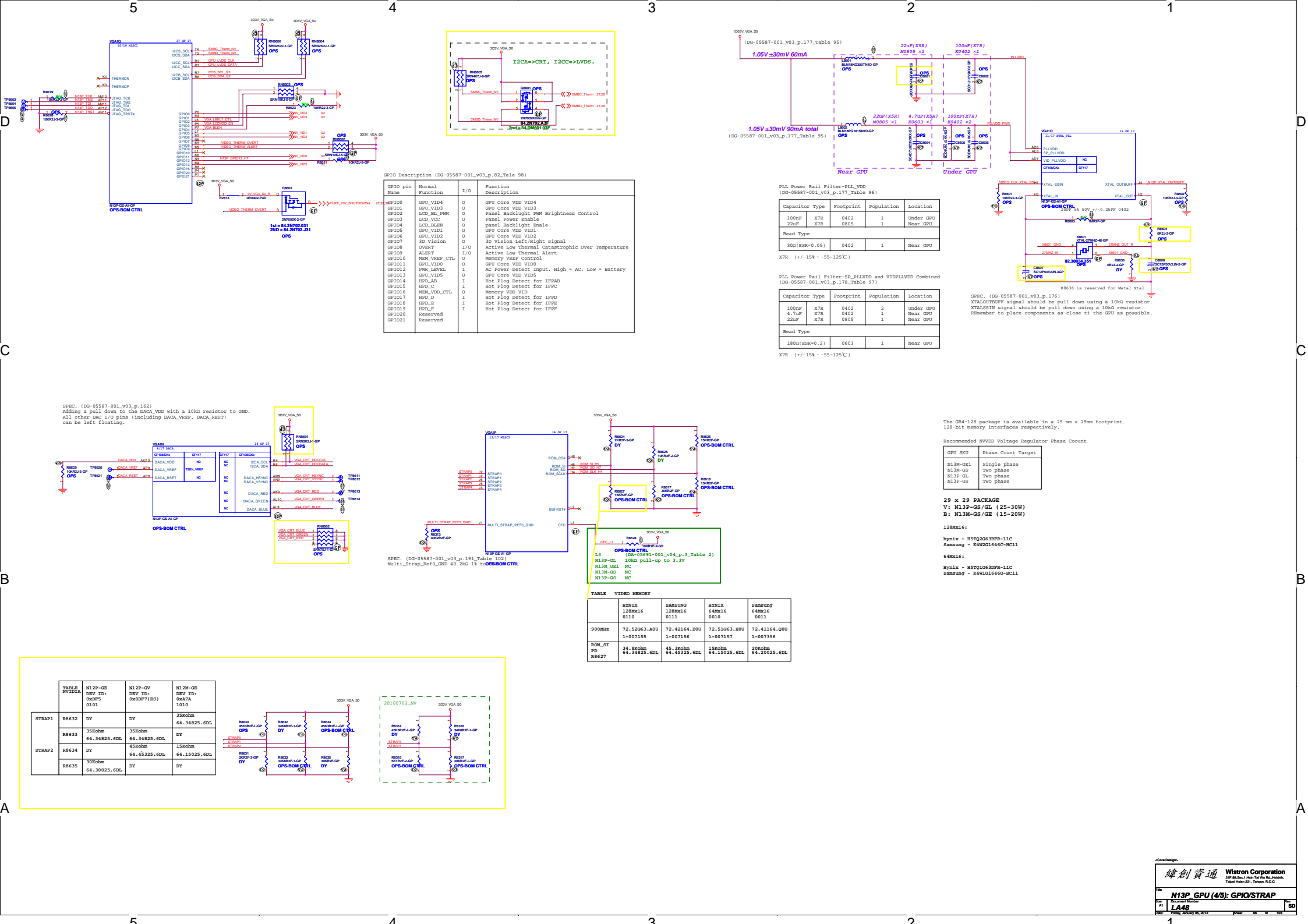
FBCLK Termination placed at each VRAM (DG-05587-001_v03_p.83_Table 19)



Memory ODTx, CKEx and RST Termination (DG-05587-001_v03_p.84_Table 20)



<Core Design>



GPIO Description (DG-05587-001_v03.p.82_Table 98)

GPIO pin Name	Normal Function	I/O	Function Description
GP100	GPU_VID4	0	GPU Core VDD VID4
GP101	GPU_VID3	0	GPU Core VDD VID3
GP102	LCD_BL_PWM	0	Panel backlight PWM Brightness Control
GP103	LCD_VCC	0	Panel Power Enable
GP104	LCD_BLEN	0	Panel Backlight Enable
GP105	GPU_VID1	0	GPU Core VDD VID1
GP106	GPU_VID2	0	GPU Core VDD VID2
GP107	ID_Vision	0	ID Vision Left/Right signal
GP108	OVERT	0	Active Low Thermal Catastrophic Over Temperature
GP109	ALERT	1/0	Active Low Thermal Alert
GP110	MEM_VREF_CTL	0	Memory VREF Control
GP1011	GPU_VDD0	0	GPU Core VDD VID0
GP1012	PMR_LEVEL	0	AC Power Detect Input. High = AC. Low = Battery
GP1013	GPU_VID5	0	GPU Core VDD VID5
GP1014	HDP_DET	1	Hot Plug Detect for IPPAB
GP1015	HDP_C	1	Hot Plug Detect for IPPC
GP1016	MEM_VDD_CTL	0	Memory VDD VID
GP1017	HDP_D	1	Hot Plug Detect for IPPD
GP1018	HDP_E	1	Hot Plug Detect for IPPE
GP1019	HDP_F	1	Hot Plug Detect for IPPF
GP1020	Reserved		
GP1021	Reserved		

PLL Power Rail Filter-PLL_VDD (DG-05587-001_v03.p.177_Table 95)

Capacitor Type	Footprint	Population	Location
100nF	XTR	0402	1
22uF	XTR	0805	1

Bead Type
30G(ESR=0.05) 0402 1 Near GPU

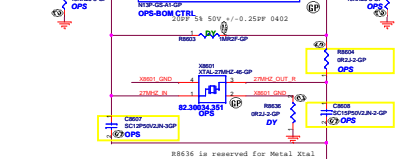
PLL Power Rail Filter-SP_PLLVDD and VIDPLLVD Combined (DG-05587-001_v03.p.178_Table 97)

Capacitor Type	Footprint	Population	Location
100nF	XTR	0402	2
4.7uF	XTR	0402	1
22uF	XTR	0805	1

Bead Type
180G(ESR=0.2) 0603 1 Near GPU

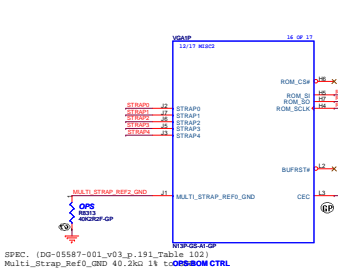
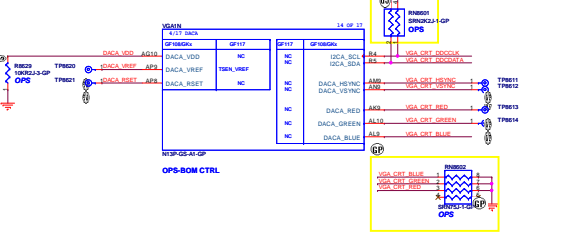
XTR (+/-15% -55-125°C)

PLL Power Rail Filter-PLL_VDD (DG-05587-001_v03.p.177_Table 95)



88636 is reserved for Metal Xtal
SPEC: (DG-05587-001_v03.p.176)
XTALOUTSTRIP signal should be pull down using a 10k resistor.
XTALSSIN signal should be pull down using a 10k resistor.
Remember to place components as close to the GPU as possible.

SPEC: (DG-05587-001_v03.p.162)
Adding a pull down to the DACA_VDD with a 10k resistor to GND.
All other DAC I/O pins (including DACA_VREF, DACA_REST) can be left floating.



SPEC: (DG-05587-001_v03.p.191_Table 102)
Multi_Strap_Ref0_GND 40.2kΩ 1V to OPS-BOM CTRL

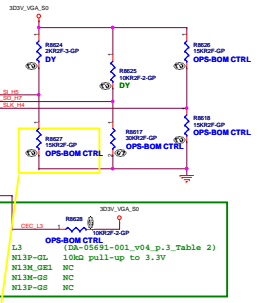


TABLE VIDEO MEMORY

	HYNIX 128Mb16	SAMSUNG 128Mb16	HYNIX 64Mb16	Samsung 64Mb16
300MHz	72.53063.A0U	72.42184.D0U	72.81063.H0U	72.41164.Q0U
ROM_B1	1-007155	1-007156	1-007157	1-007156
PD	34.8900m	45.3600m	1.9000m	2.0000m
R8627	64.34825.6DL	64.45325.6DL	64.30025.6DL	64.40025.6DL

The GB4-128 package is available in a 29 mm x 29mm footprint. 128-bit memory interfaces respectively.

Recommended NVVD Voltage Regulator Phase Count

GPU SKU	Phase Count Target
N13M-GE1	Single phase
N13M-GS	Two phase
N13P-GL	Two phase
N13P-GS	Two phase

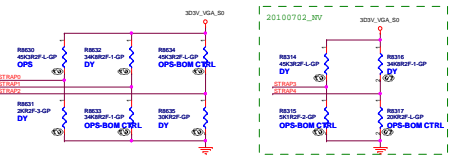
128Mb16:

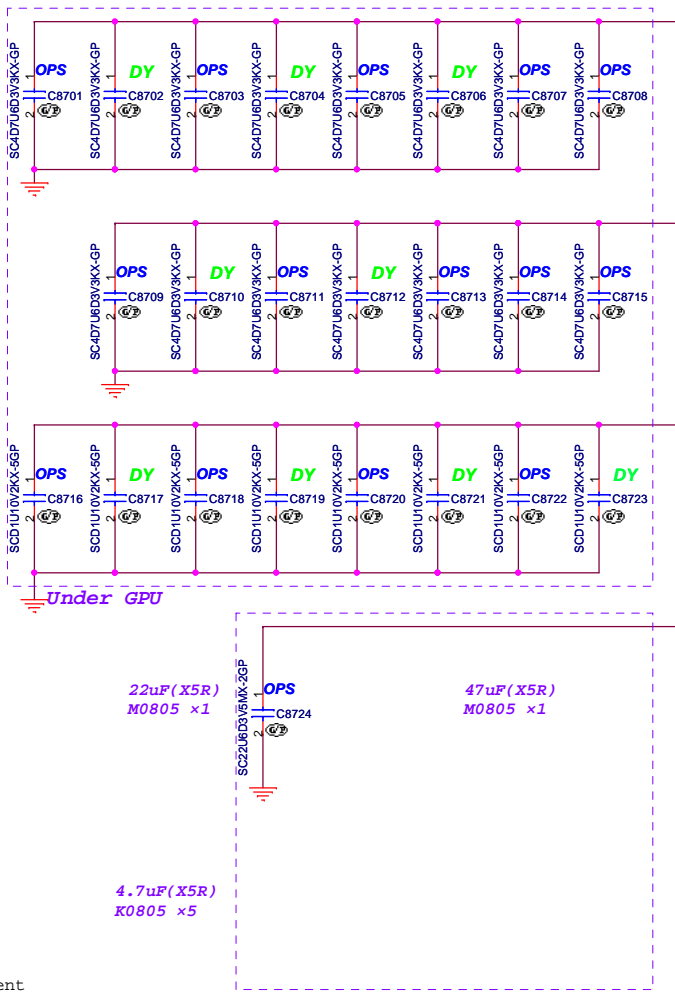
hynix - H57Q206189P-11C
Samsung - K4W031646C-BC11

64Mb16:

Hynix - H57Q106109P-11C
Samsung - K4W01646C-BC11

TABLE N13P	N13P-GE DEV ID: 0x0F5	N13P-GV DEV ID: 0x0F7(ES)	N13M-GE DEV ID: 0x0F7A
STRAP1	R8632 DY	DY	35Kohm
	R8633 35Kohm	35Kohm	64.34825.6DL
	R8634 64.34825.6DL	64.34825.6DL	
STRAP2	R8634 DY	45Kohm	15Kohm
	R8635 45.45325.6DL	45.45325.6DL	64.15025.6DL
	R8635 30Kohm	DY	DY

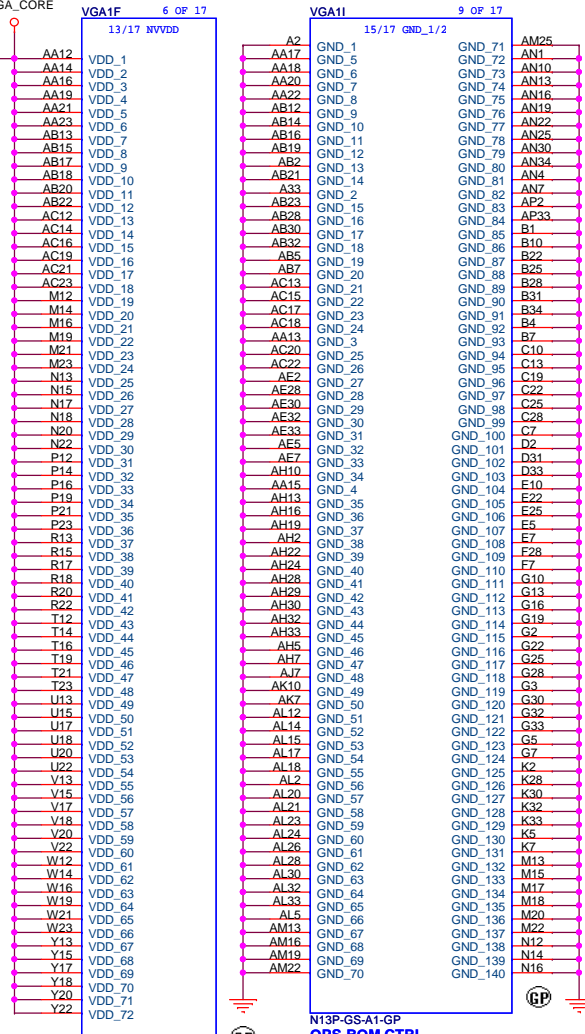




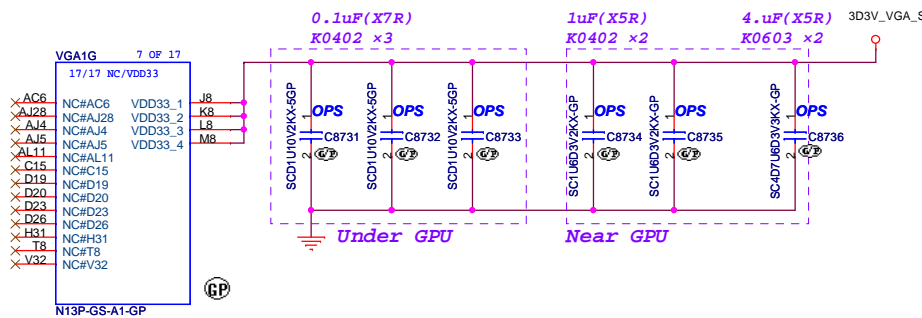
NVDD Decoupling Requirement (DG-05587-001_v03_p.56_Table 7)

Capacitor Type	Footprint	Population	Location
4.7uF	X6S 0603	15	Under GPU
0.1uF	X7R 0402	8	Under GPU
47uF	X5R 0805	1	Near GPU
22uF	X5R 0805	1	Near GPU
4.7uF	X5R 0805	5	Near GPU

- X7R (+/-15%、-55~125°C)
- X6S (+/-22%、-55~105°C)
- X5R (+/-15%、-55~85°C)



N13P-GS-A1-GP OPS-BOM CTRL



VDD33 Decoupling (DG-05587-001_v03_p.57_Table 8)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R 0402	3	Under GPU
1uF	X5R 0402	2	Near GPU
4.7uF	X5R 0603	1	Near GPU

- X7R (+/-15%、-55~125°C)
- X5R (+/-15%、-55~85°C)

<Core Design>

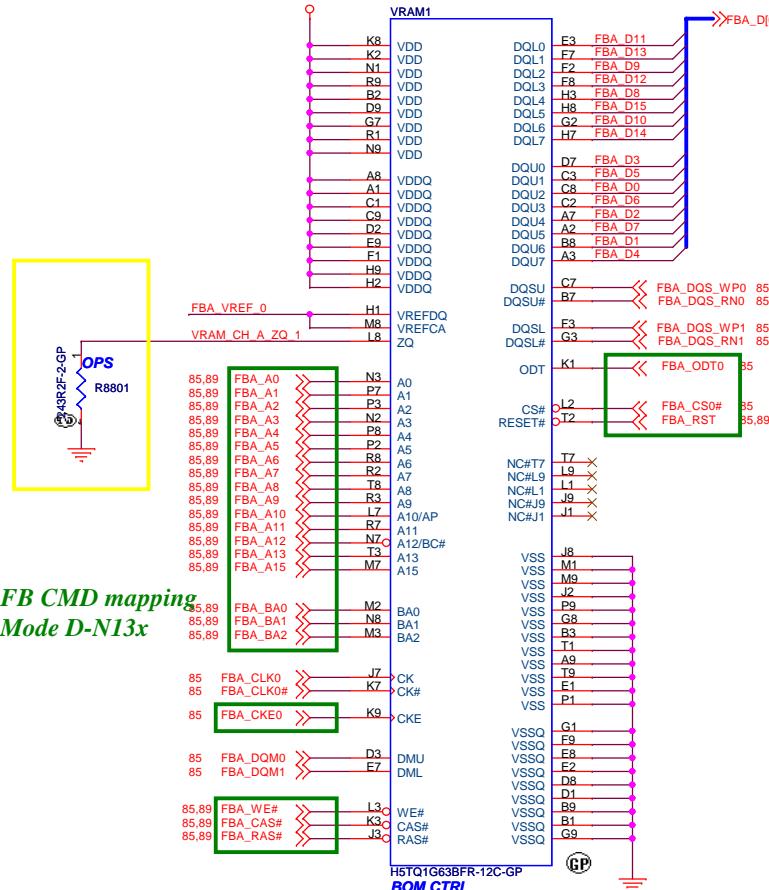
緯創資通 Wistron Corporation
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File	N13P GPU (5/5): PWR/GND			Rev
Size	Document Number	LA48		SD
Date:	Friday, January 06, 2012	Sheet	87	of 103

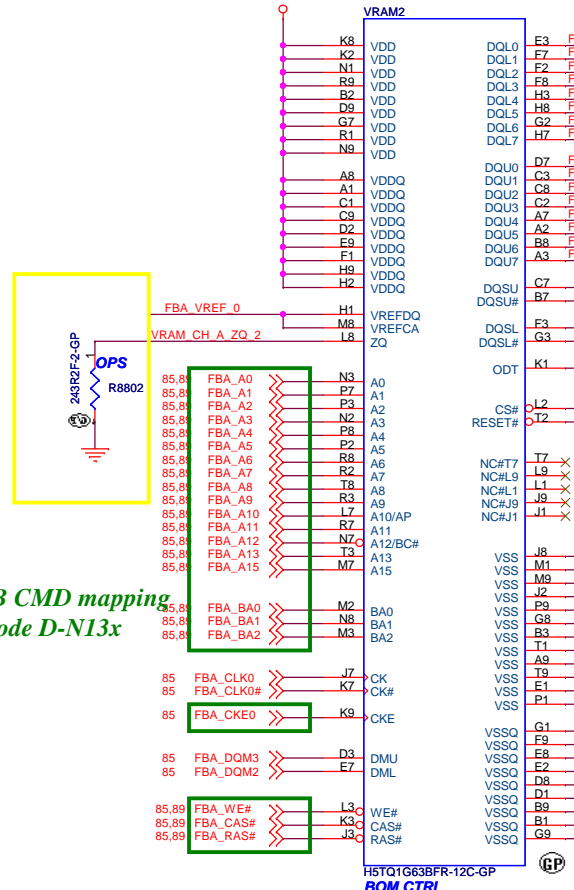
VIDEO FRAME BUFFER PORT A

1D5V_VGA_S0

1D5V_VGA_S0



**FB CMD mapping
Mode D-N13x**



**FB CMD mapping
Mode D-N13x**

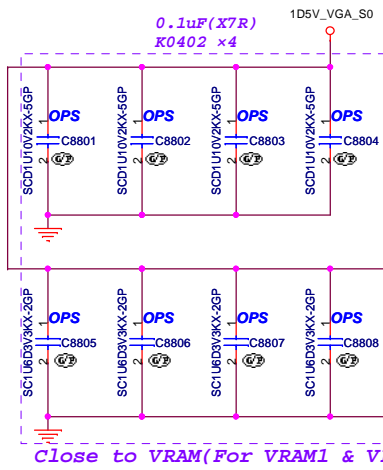
- 128 X 16
72.52G63.A0U IC VRAM K4W2G1646C-HC11 FBGA96
- 64 X 16
72.51G63.H0U IC VRAM H5TQ1G63DFR-11C FBGA 96BALLS
- 72.41646.Q0U IC VRAM K4W1G1646G-BC11 FBGA 96BALLS

- 128Mx16:
hynix - H5TQ2G63BFR-11C
Samsung - K4W2G1646C-HC11
- 64Mx16:
Hynix - H5TQ1G63DFR-11C
Samsung - K4W1G1646G-BC11

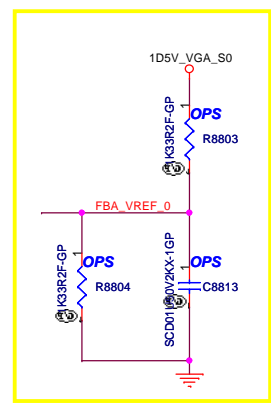
Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout (DG-05587-001_v03_p.87_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

X7R (+/-15%、-55-125°C)
*Per clamshell pair



Close to VRAM(For VRAM1 & VRAM2)



<Core Design>

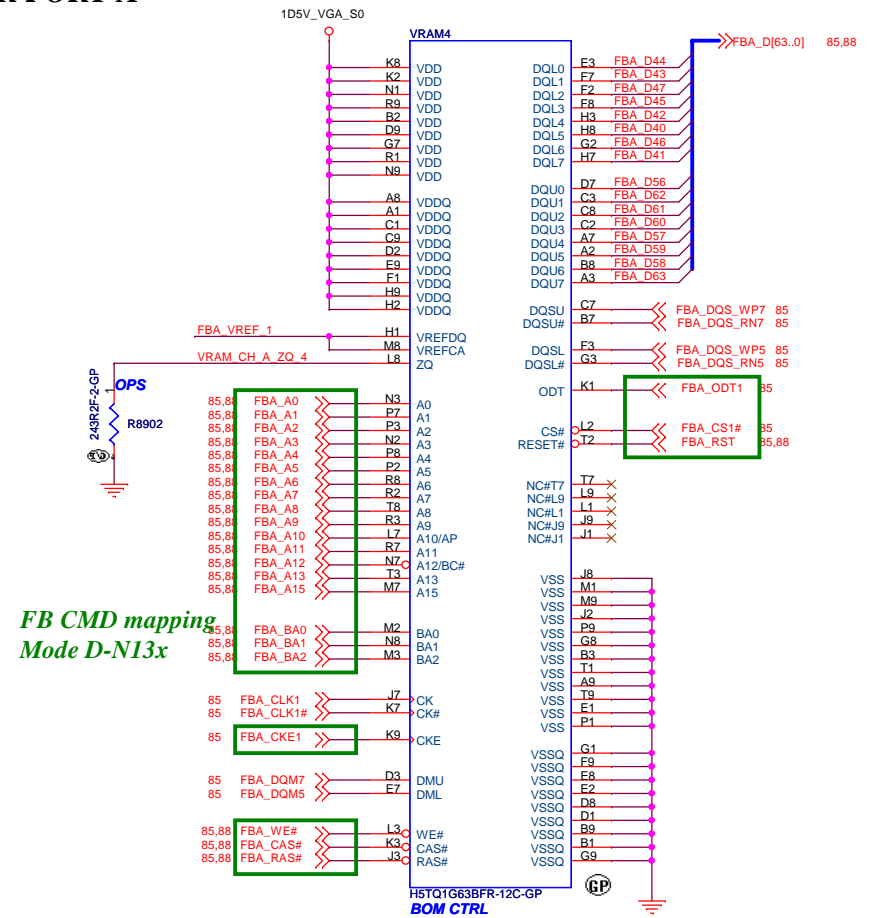
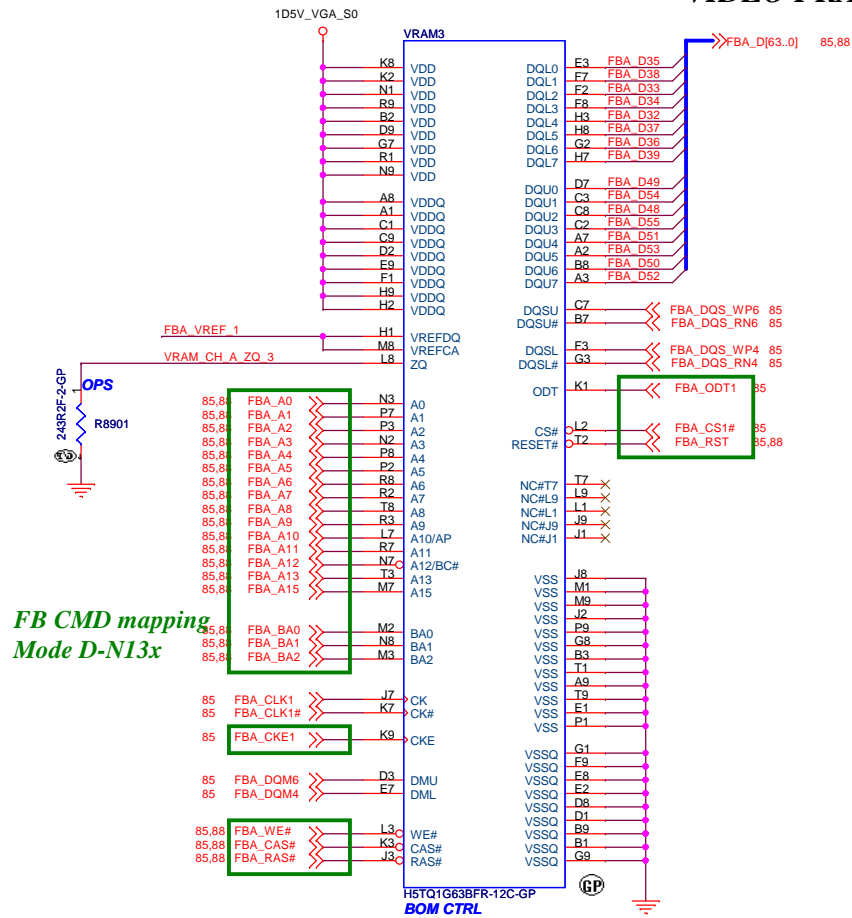
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Title: **CHANNEL-A_VRAM1,2 (1/4)**

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Date: Friday, January 06, 2012 Sheet 88 of 103

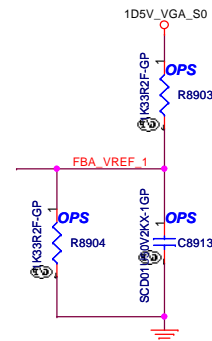
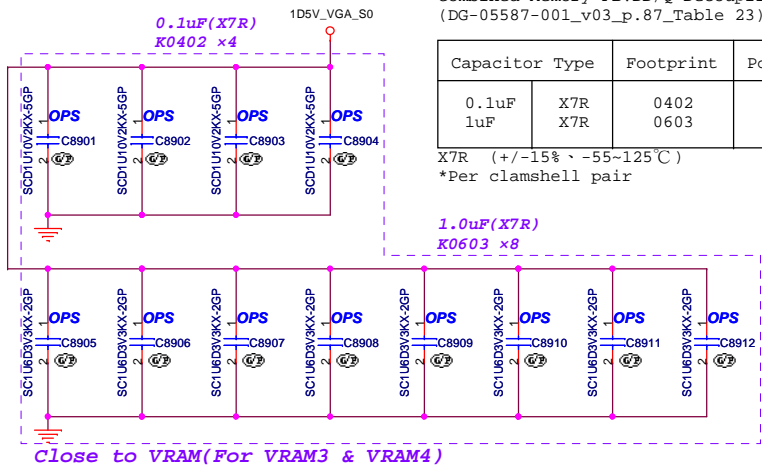
VIDEO FRAME BUFFER PORT A



Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout (DG-05587-001_v03_p.87_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

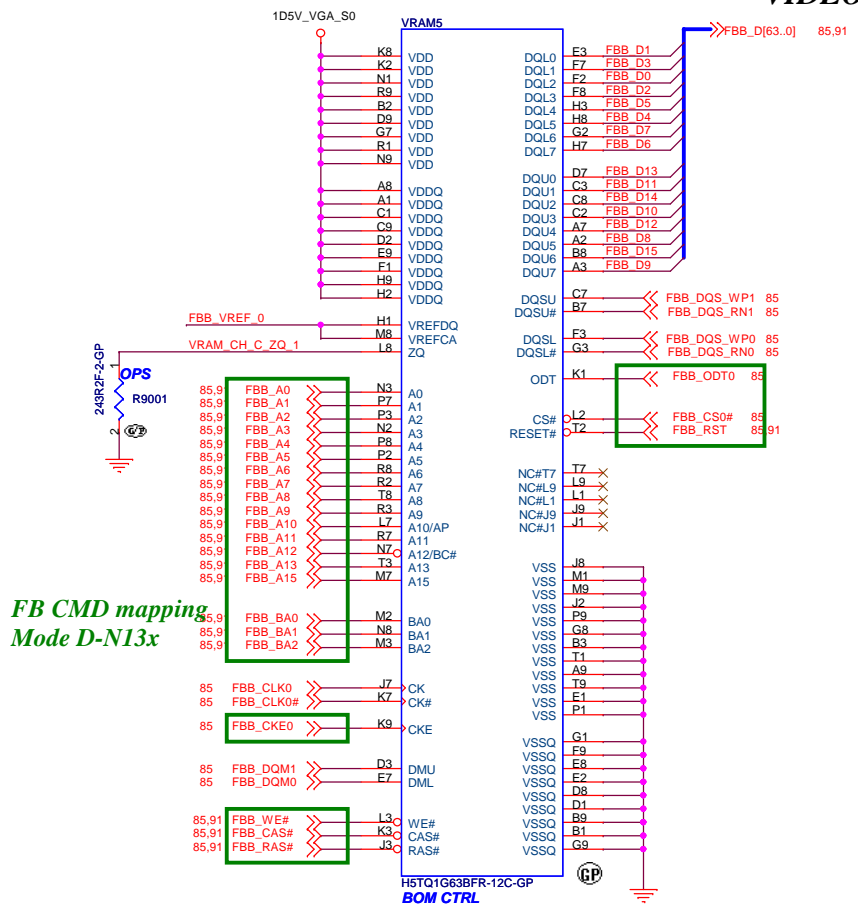
X7R (+/-15%、-55-125°C)
*Per clamshell pair



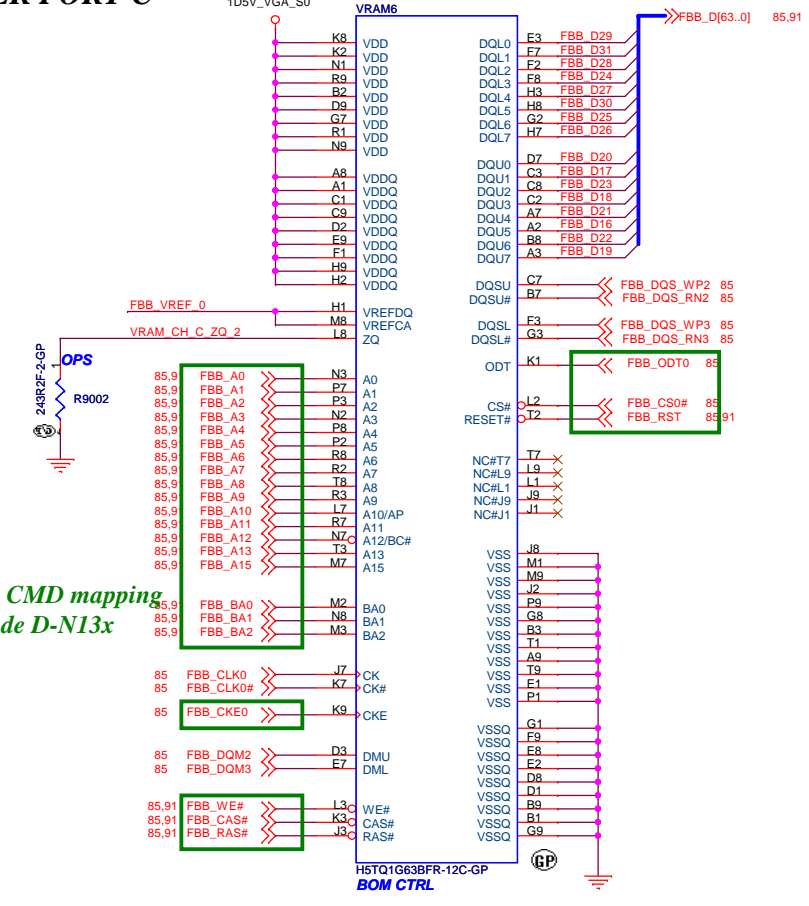
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VIDEO FRAME BUFFER PORT C



**FB CMD mapping
Mode D-N13x**

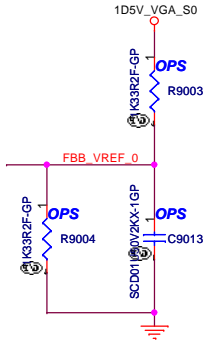
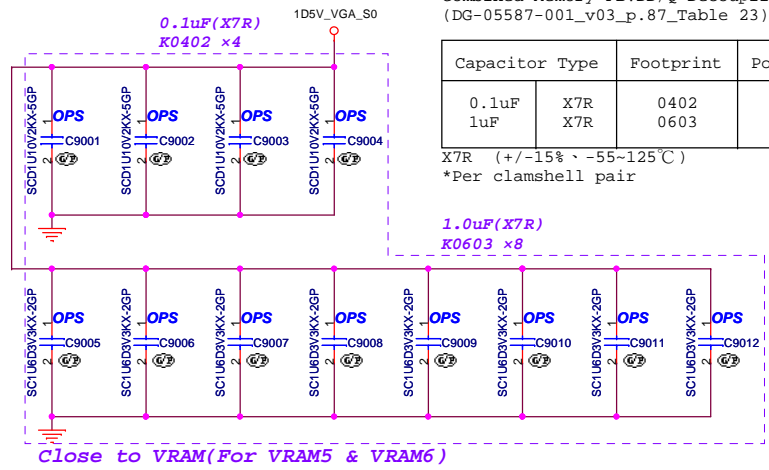


**FB CMD mapping
Mode D-N13x**

Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout (DG-05587-001_v03_p.87_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF X7R	X7R	0402	4
1uF	X7R	0603	8
			Close to VRAM
			Close to VRAM

X7R (+/-15%、-55-125°C)
*Per clamshell pair



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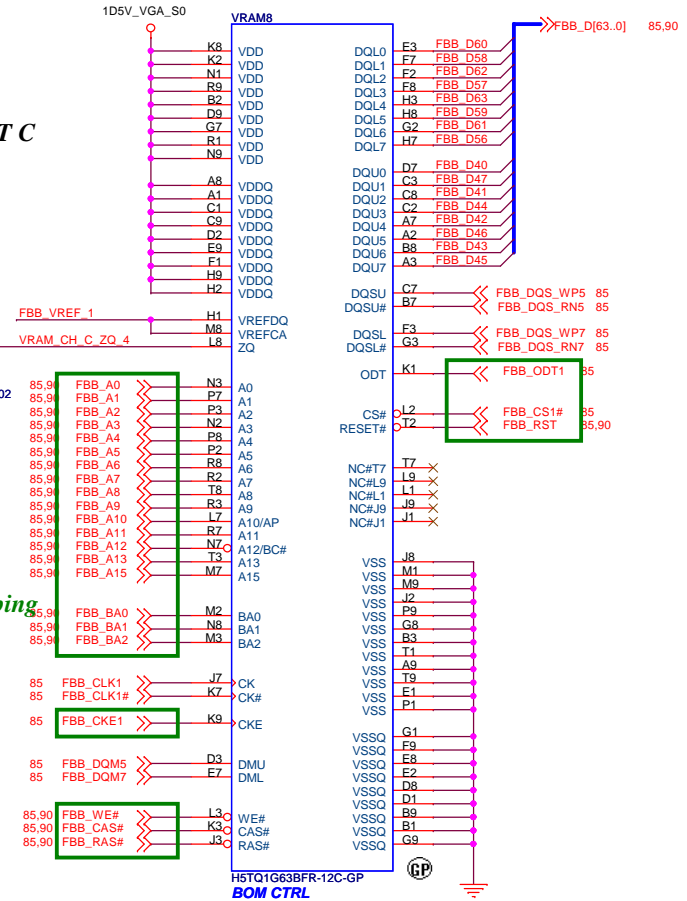
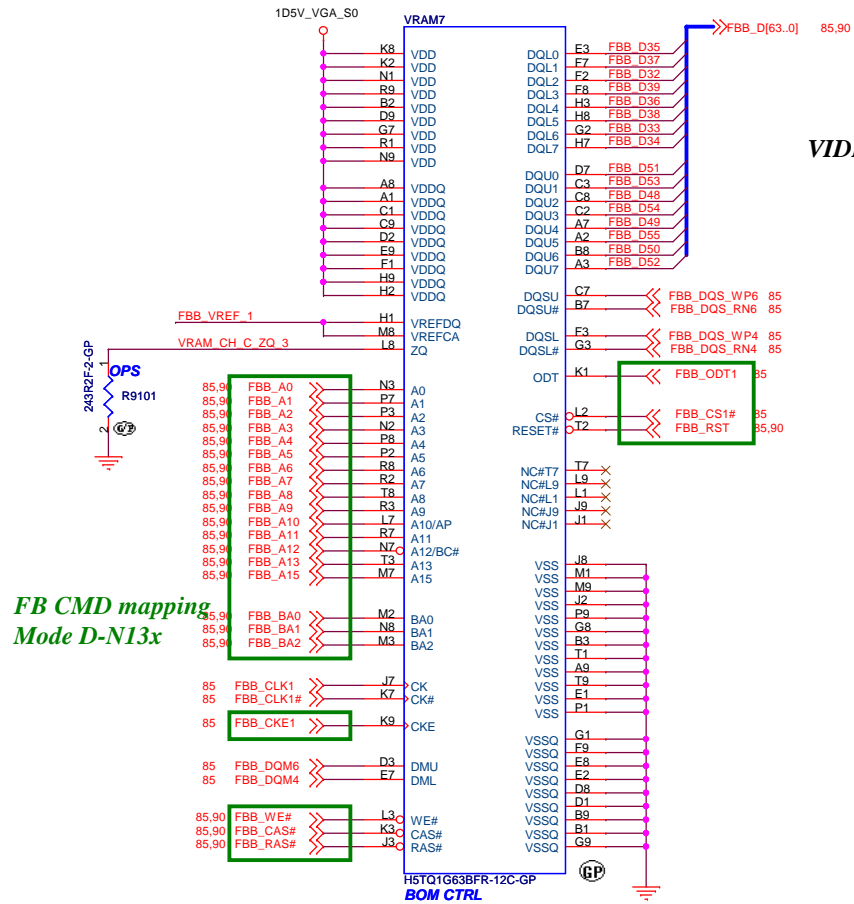
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Title **CHANNEL-C_VRAM5,6 (3/4)**

Size A3 Document Number **LA48** Rev **SD**

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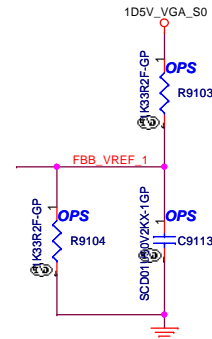
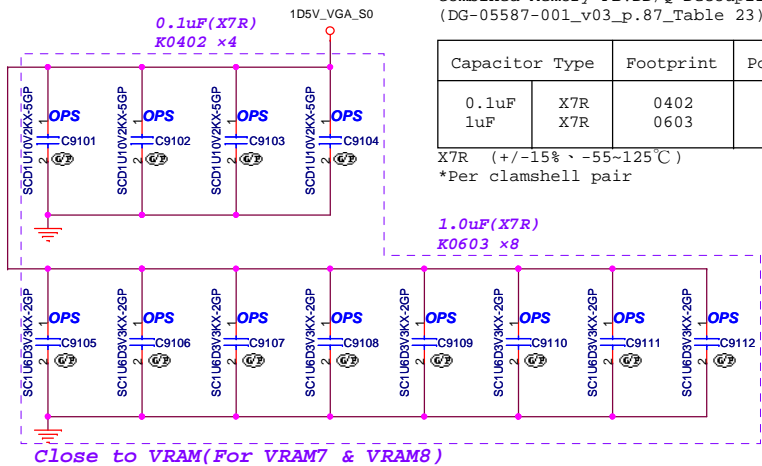
VIDEO FRAME BUFFER PORT C



Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout (DG-05587-001_v03_p.87_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	Close to VRAM
1uF	X7R	0603	Close to VRAM

X7R (+/-15%、-55-125°C)
*Per clamshell pair



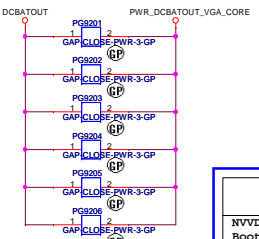
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Title **CHANNEL-C_VRAM7,8 (4/4)**

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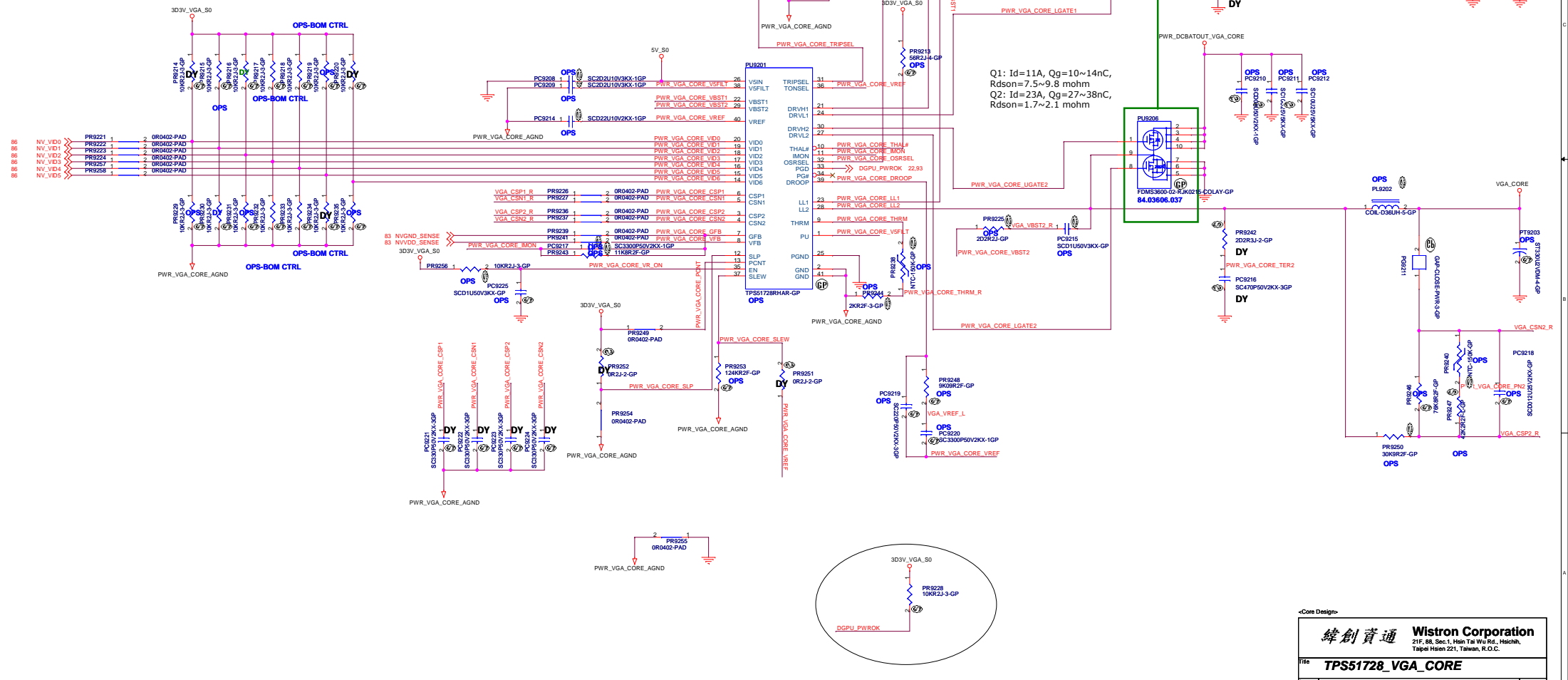
SSID = PWR.Plane.Regulator_GFX



	N13P-GS 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U	N13M-GE1 71.0N13M.C0U
NV_VDD	0.9V	0.975V	0.9V	0.875V
Boot Voltage	VID[6:0]=0110000	VID[6:0]=0101010	VID[6:0]=0110000	VID[6:0]=0110010
NV_VID1	PR9215 DY	63.10334.1DL	DY	63.10334.1DL
	PR9230	63.10334.1DL	DY	63.10334.1DL
NV_VID3	PR9217 DY	63.10334.1DL	DY	63.10334.1DL
	PR9232	63.10334.1DL	DY	63.10334.1DL
NV_VID4	PR9218 DY	63.10334.1DL	DY	63.10334.1DL
	PR9233	63.10334.1DL	DY	63.10334.1DL

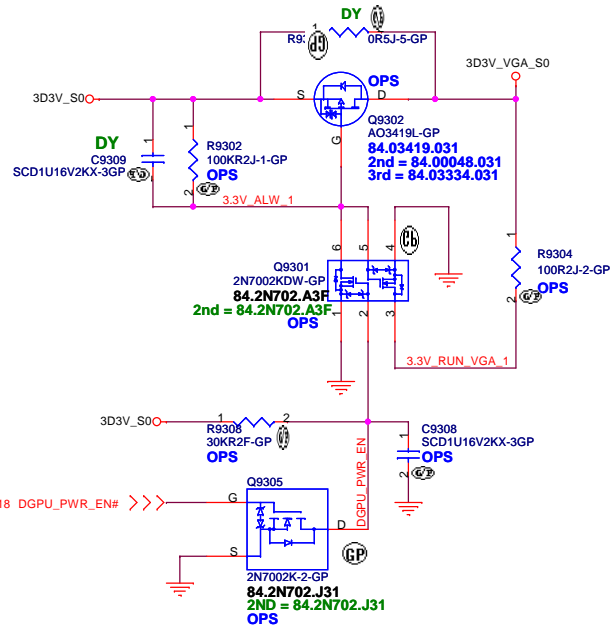
	Main source	2nd source
PU9202	84.03606.037 FDMS3606S-GP-U	
PU9206	84.03606.037 FDMS3606S-GP-U	

BOM control

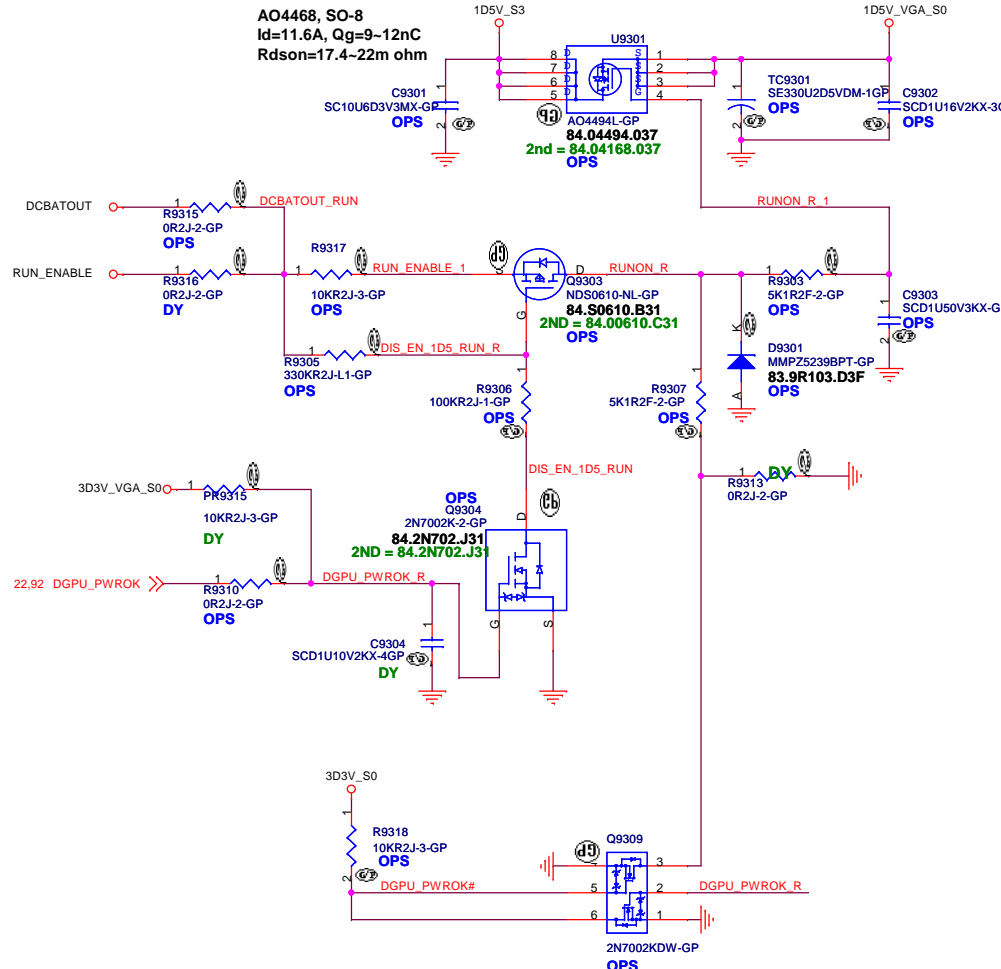


Q1: Id=11A, Qg=10~14nC,
Rdson=7.5~9.8 mOhm
Q2: Id=23A, Qg=27~38nC,
Rdson=1.7~2.1 mOhm

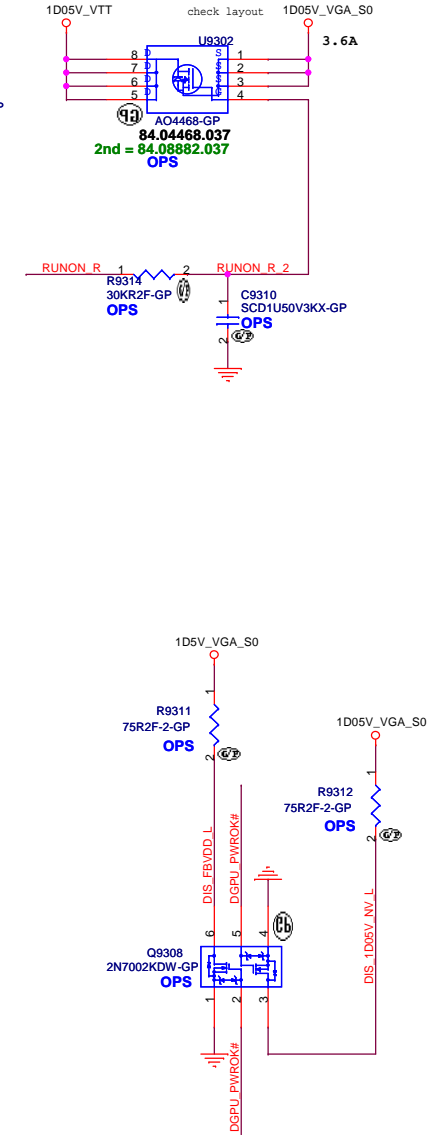
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0



1.05V to 1.05V_VGA_S0 Transfer



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Title: **DISCRETE VGA POWER**

Size A3 Document Number **LA480** Rev **SD**

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緯創資通		Wistron Corporation	
		<small>21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C</small>	

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Size	Document Number	Rev
A4	LA480	SD

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Title

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Document Number

LA480

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Taipei Hsien 221, Taiwan, R.O.C.

Title

TOUCH PANEL

Size
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Document Number

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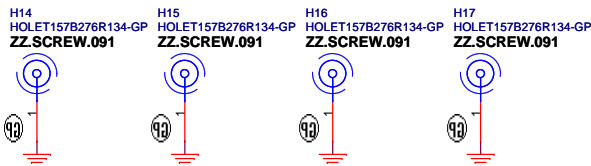
Rev

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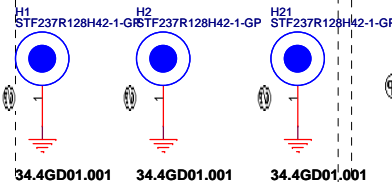
Date: Friday, January 06, 2012

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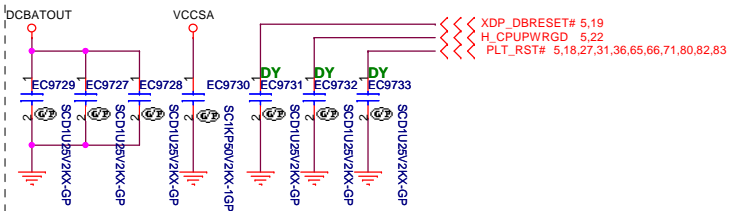
CPU Plate



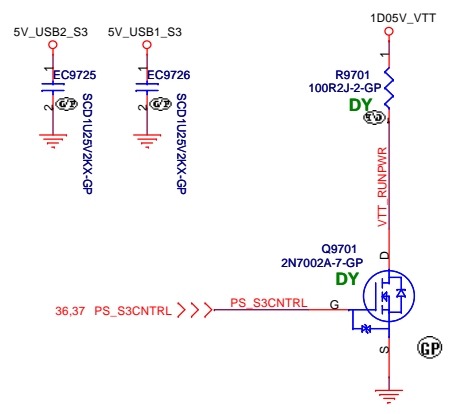
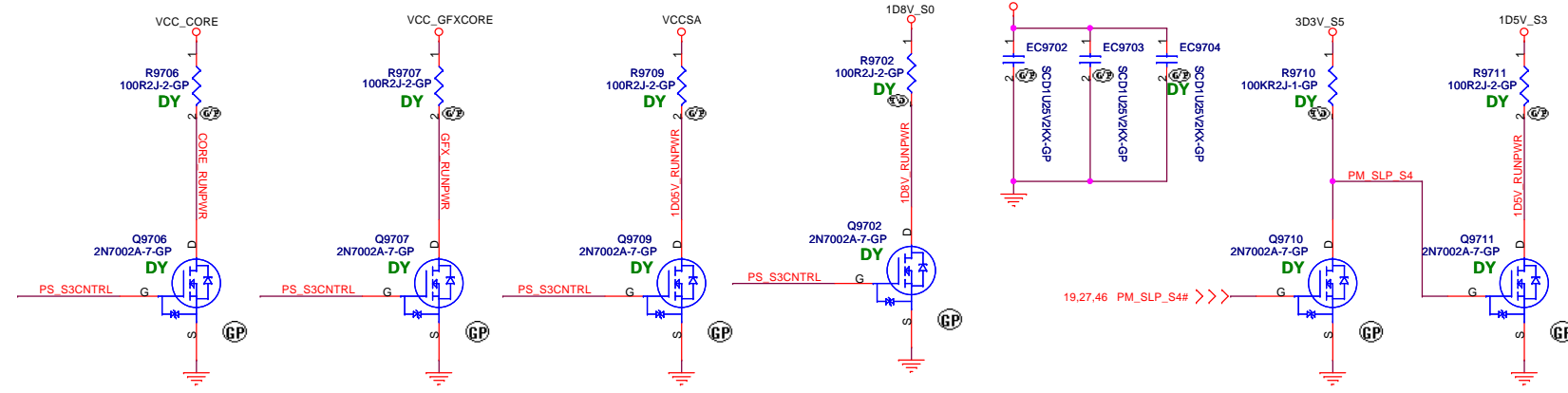
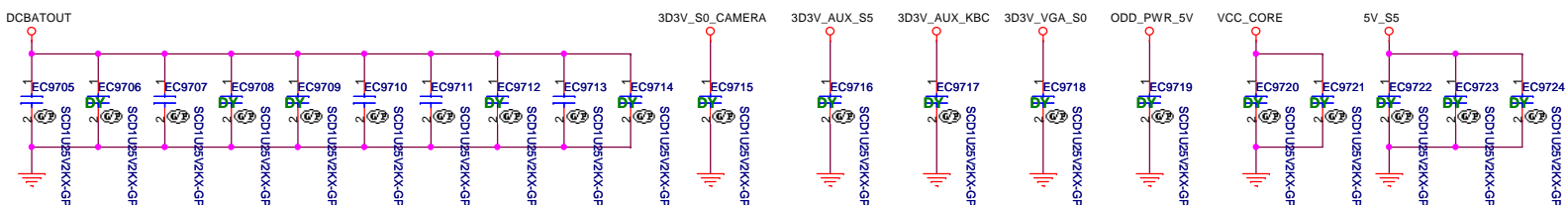
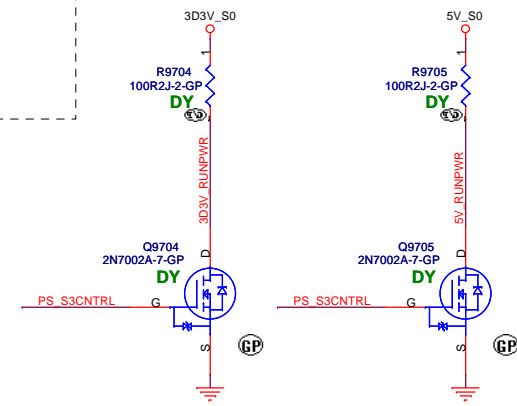
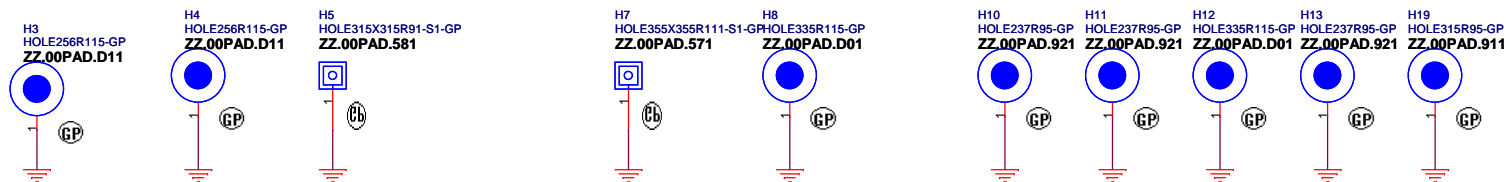
VGA Std-Off



MINI PCIE



14" Structure boss



For Discharge

<Core Design>

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Title	UNUSED PARTS/EMI Capacitors		Rev
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

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A4

Document Number

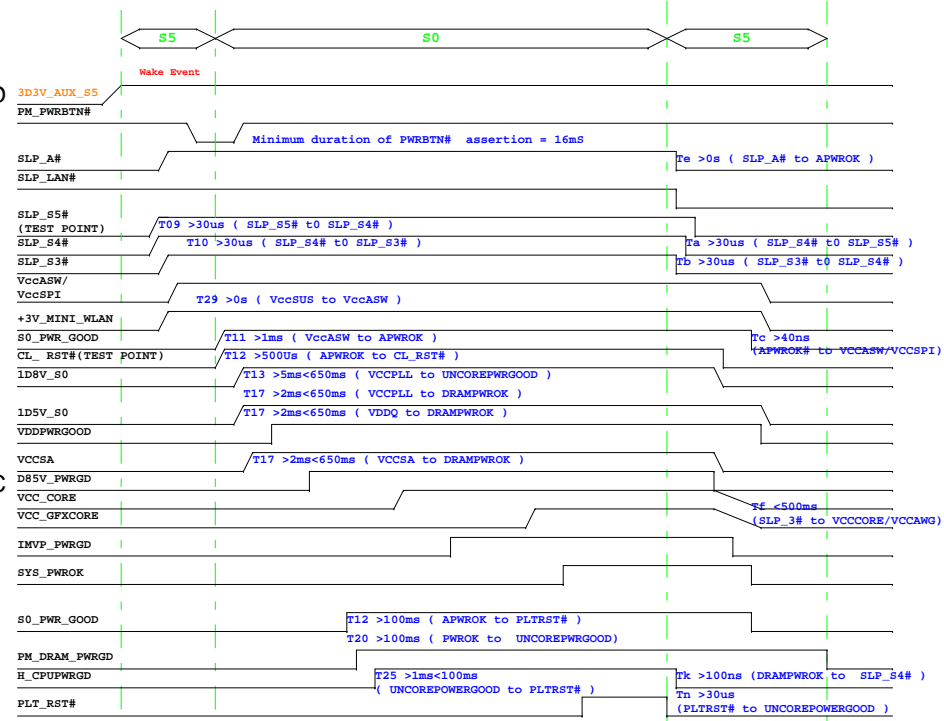
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Rev
SD

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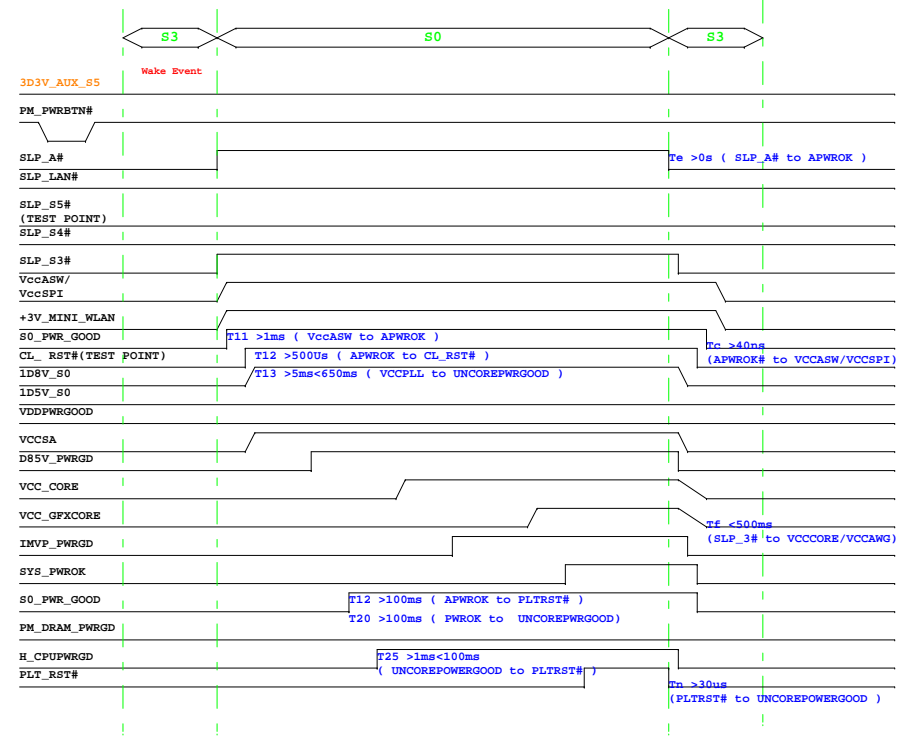
Sheet 98 of 103

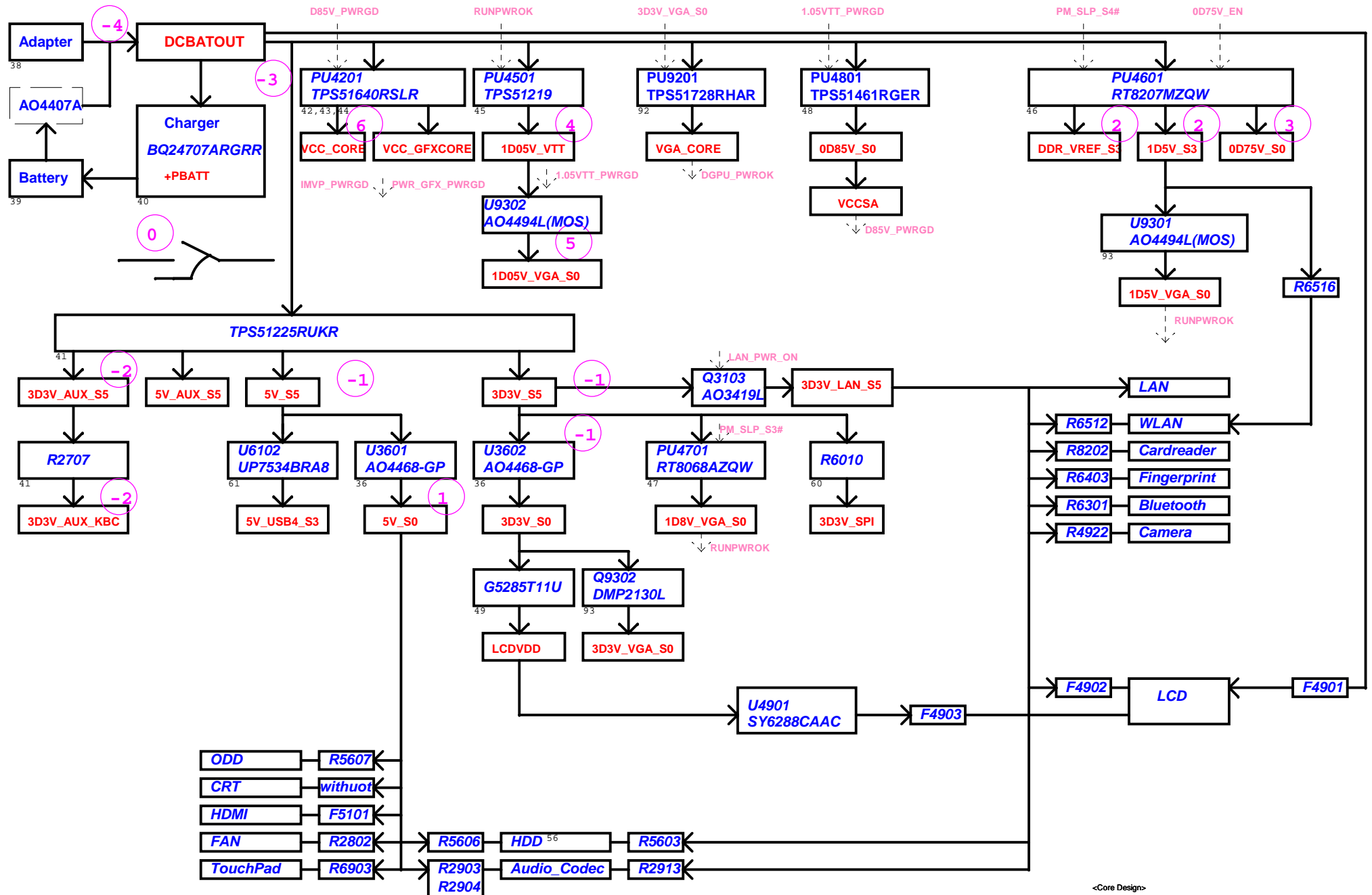
Intel-Power Sequence (S5-to-S0-to-S5)



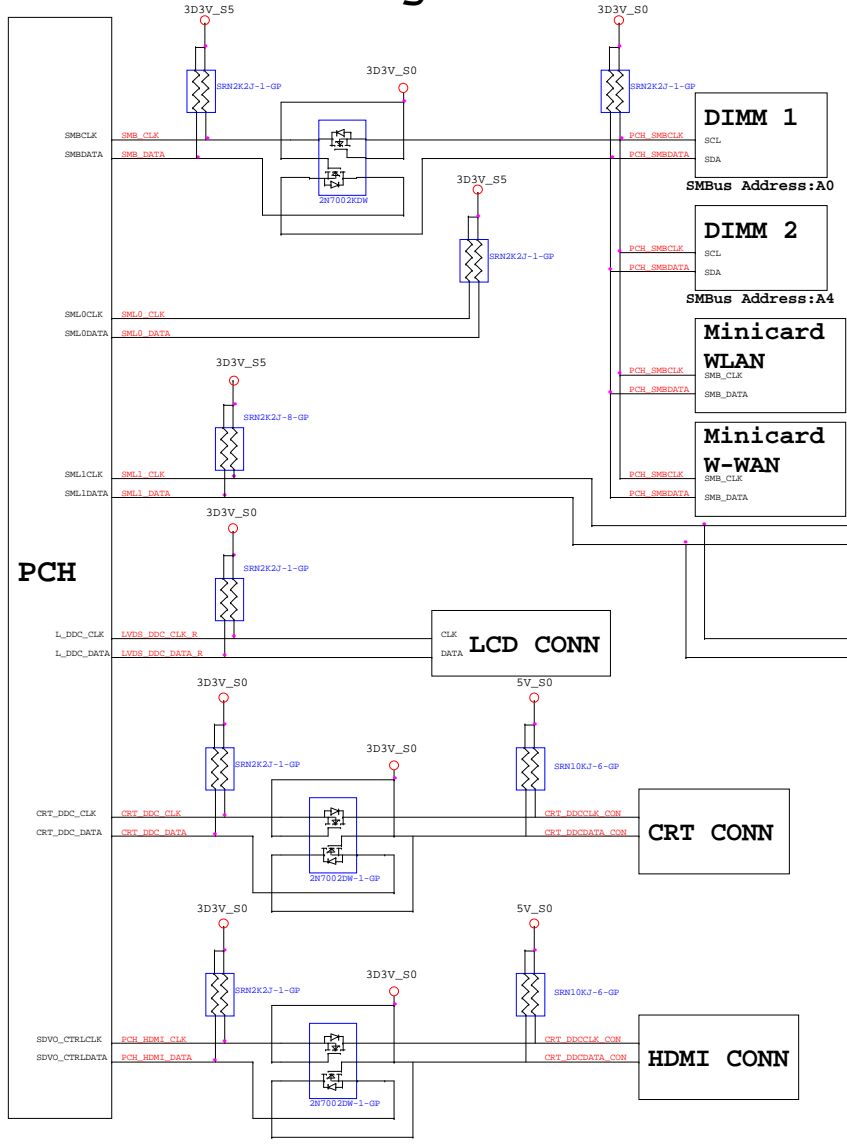
Intel PCH Pin Name	Main board PCH Pin Name
VccSUS (5V/3V)	3D3V_AUX_S5
PWRBTN#	PM_PWRBTN#
SLP_A#	SLP_A#
SLP_LAN#	SLP_LAN#
SLP_S5#	PM_SLP_S5#
SLP_S4#	PM_SLP_S4#
SLP_S3#	PM_SLP_S3#
VccASW/VccSPI	VccASW/VccSPI
Vcc_WLAN	+3V_MINI_WLAN
PWROK/APWROK	S0_PWR_GOOD
CL_RST#	CL_RST#
VCCPLL	ID8V_S0
VDDQ	ID5V_S0
VR_VDDQPWRGOOD	VDDPWRGOOD
VCCSA	VCCSA
IMVP7_VR_EN	D85V_PWRGD
VccCore	VCC_CORE
VccAXG	VCC_GFXCORE
IMVP7_PWRGD	IMVP_PWRGD
SYS_PWRGD	SYS_PWRGD
PWROK	S0_PWR_GOOD
DRAMPWROK	PM_DRAM_PWRGD
UNCOREPWRGOOD	H_CPUPWRGD
PLTRST#	PLT_RST#

(S3-to-S0-to-S3)

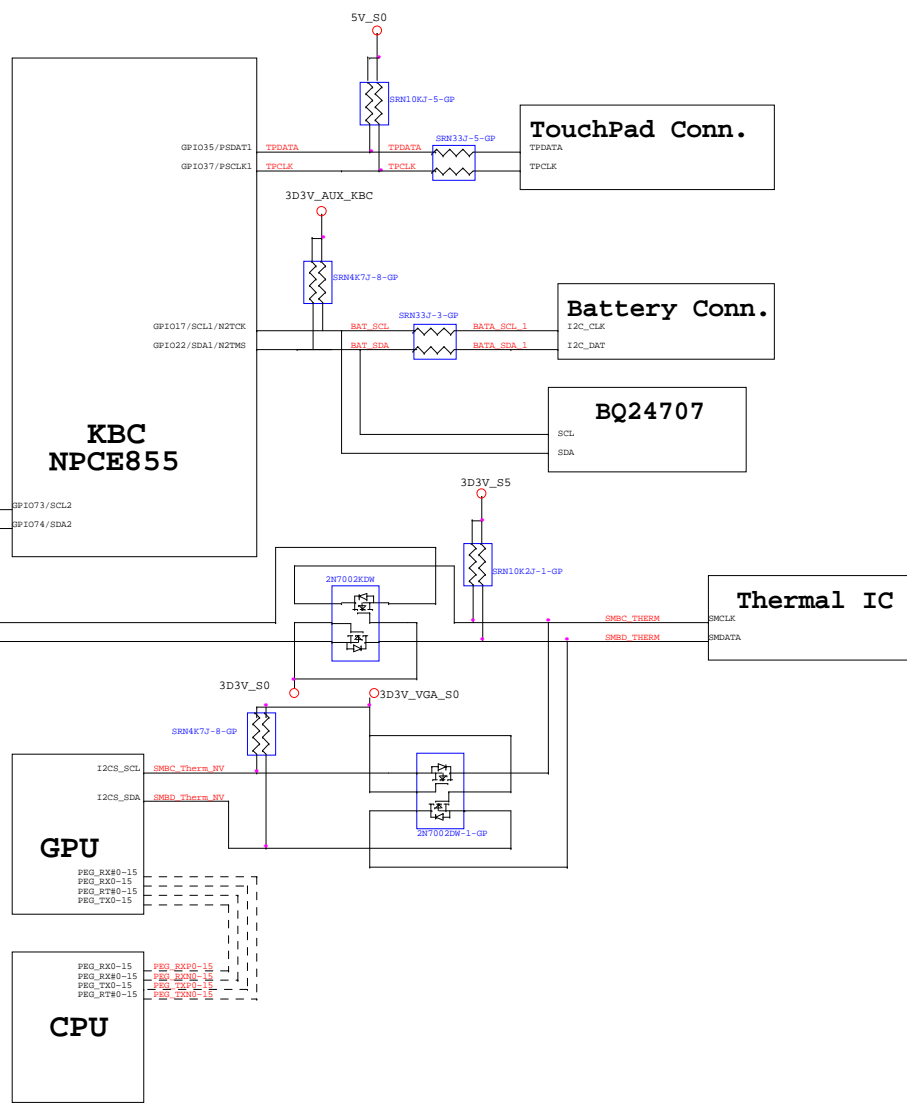




PCH SMBus Block Diagram

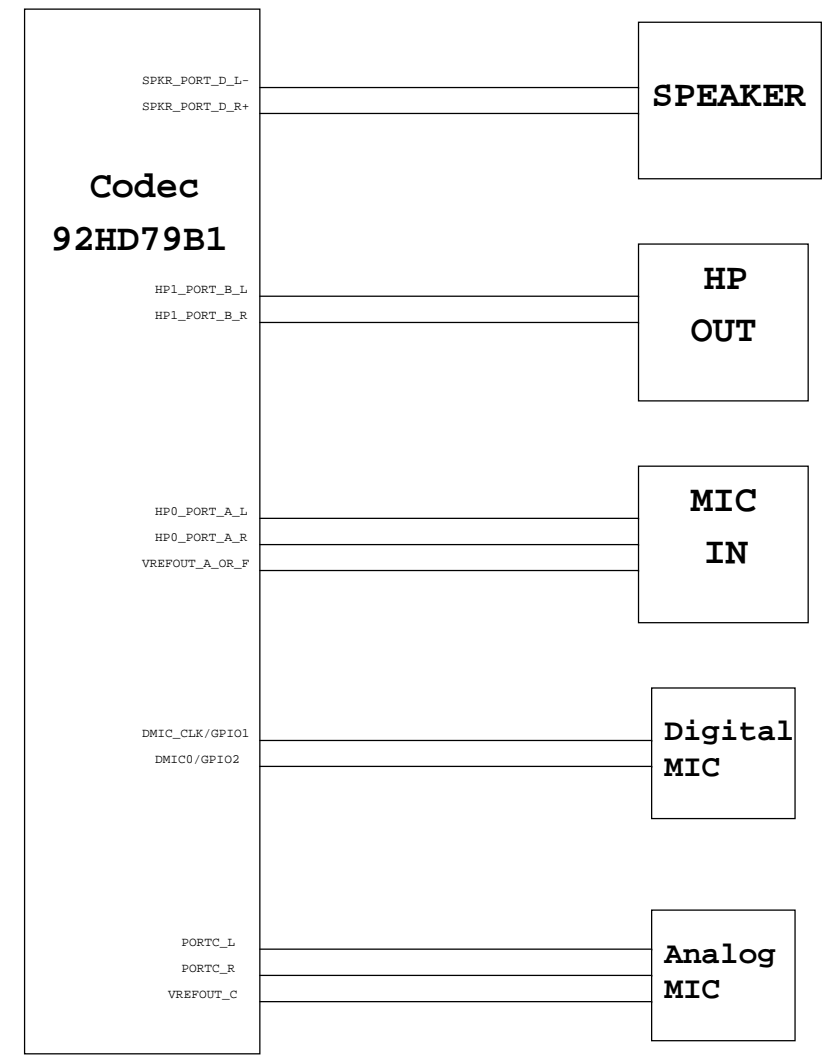
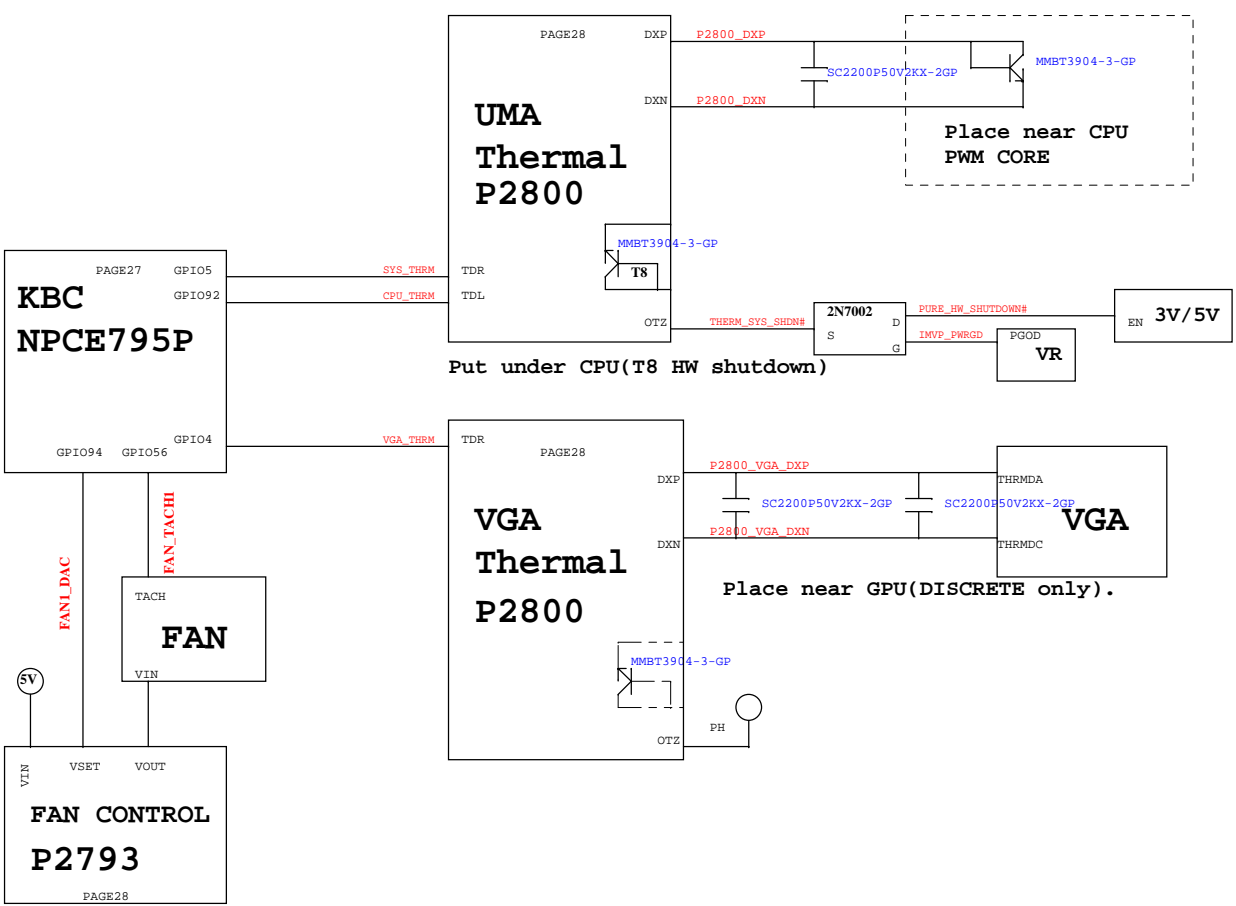


KBC SMBus Block Diagram



Thermal Block Diagram

Audio Block Diagram



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