COMPAL CONFIDENTIAL

MODEL NAME : ***HAL00***

PCB NO : ***LA-2791***

COMPAL P/N : ***45135631L01***

Travis (UMA) Schematics Document

uFCPGA Mobile Yonah
Intel Calistoga + ICH7M

2006-01-20

REV : 1.0 (DELL: A00)

MB PCB

Part Number	Description
DAA0000040L	PCB ZJX LA-2791 REV0 M/B UMA

BOM NO. 45135631L01

PCB P/N: DA800002L1L

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Title: Cover Sheet

Size | Document Number: LA-2791 | Rev: 0.6

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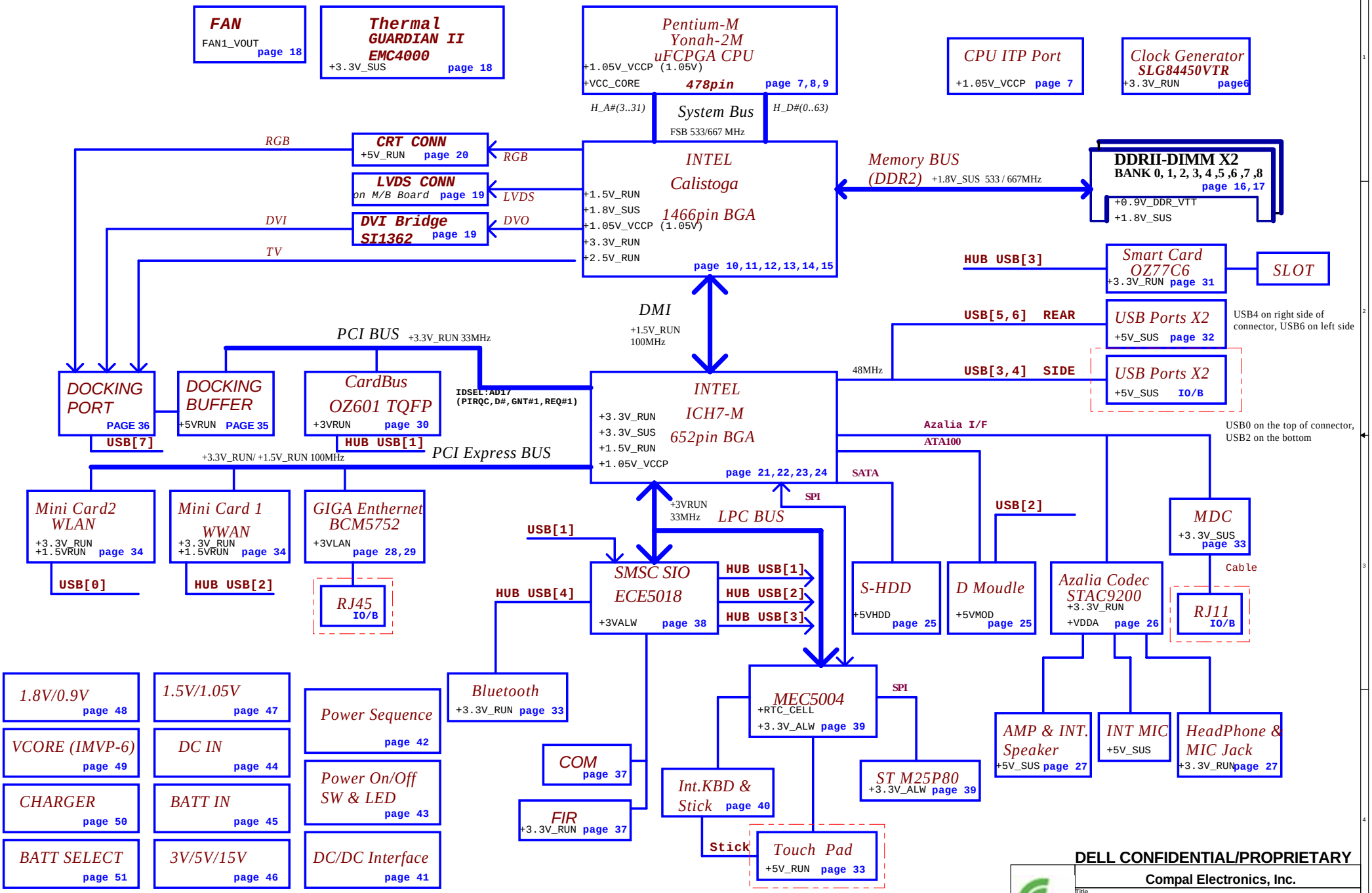
Block Diagram



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Compal Electronics, Inc.		
Title: Block Diagram		
Size	Document Number: LA-2791	Rev: 0.6
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Ceramic Capacitors :

0.1U_0402_6.3VXX

- Tolerance
- Temperature Characteristics
- Rated Voltage
- Package Size
- Value

Tantalum or Polymer Capacitors :

10U_D2_10VX_R45

- Low ESR Mark : 45 m ohm
- Tolerance
- Rated Voltage
- Package Size
- Value

Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

8	9	A	B	C	D	E	F	G
NPO	COG	X6S	BJ	CH	CJ	CK	SH	SJ

H	I	J	K
UJ	UK	SL	X5S

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	+-0.05PF	+-0.1PF	+-0.25PF	+-0.5PF	+-1PF	+-2%	+-3%	+-5%

K	M	N	P	Q	V	X	Z	
+-10%	+-20%	+-30%	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	

NOTE1:

@XX : Depop component

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	C

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW	+3.3V_SRC +15V_SUS +5V_SUS +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +3.3V_RUN_R +1.8V_RUN +0.9V_DDR_VTT +1.5V_RUN +VCC_CORE +1.05V_VCCP +2.5V_RUN
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

USB TABLE

USB PORT#	DESTINATION
0	Mini 2(WLAN)
1	USB Hub (5018)
2	D Moudle
3,4	SIDE
5,6	REAR
7	Docking

USB HUB	DESTINATION
1	PC Card Bay
2	Mini 1(WWAN)
3	Smart Card --> BIO
4	Blue tooth

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Title: Index and Config.

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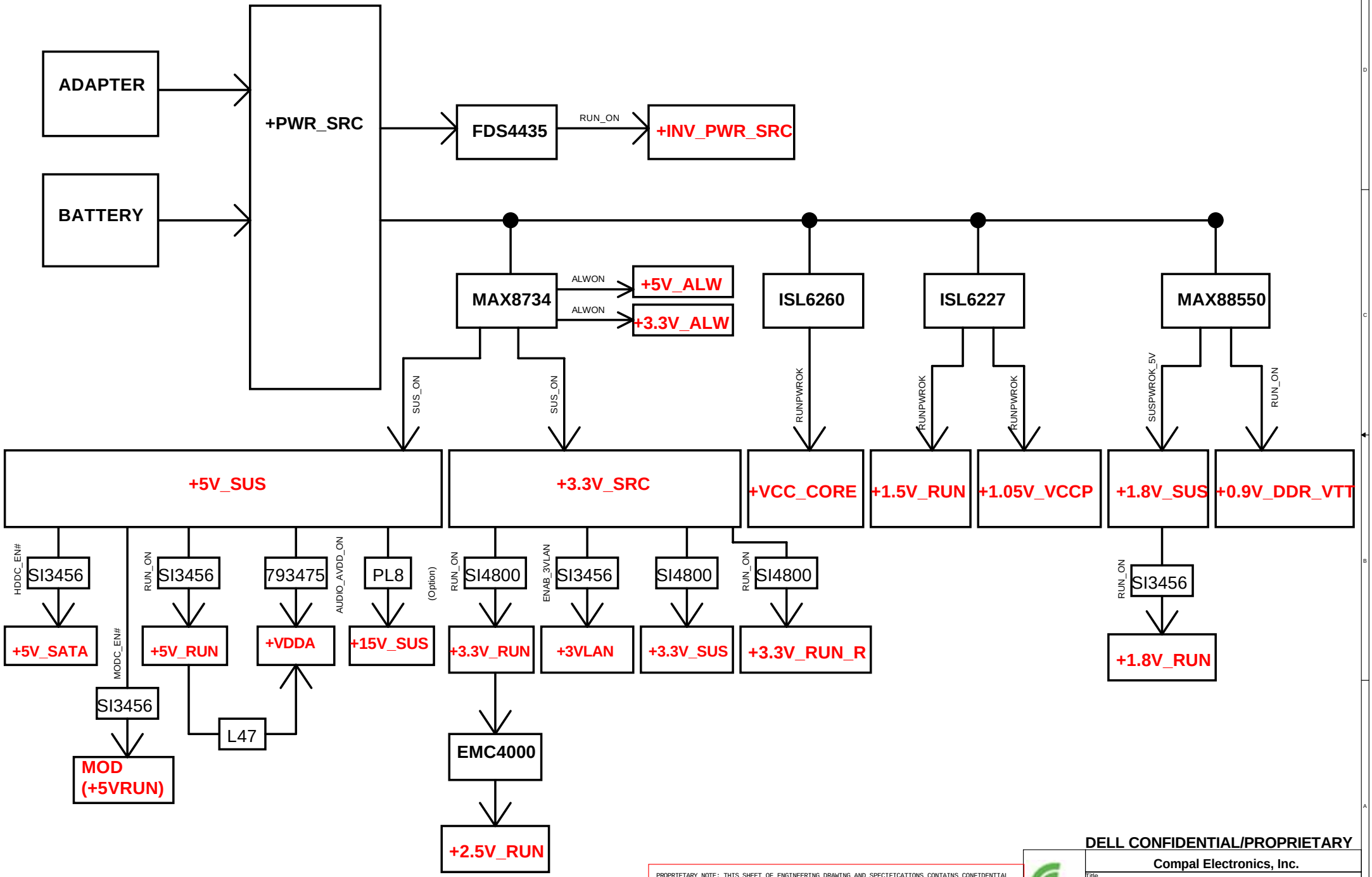

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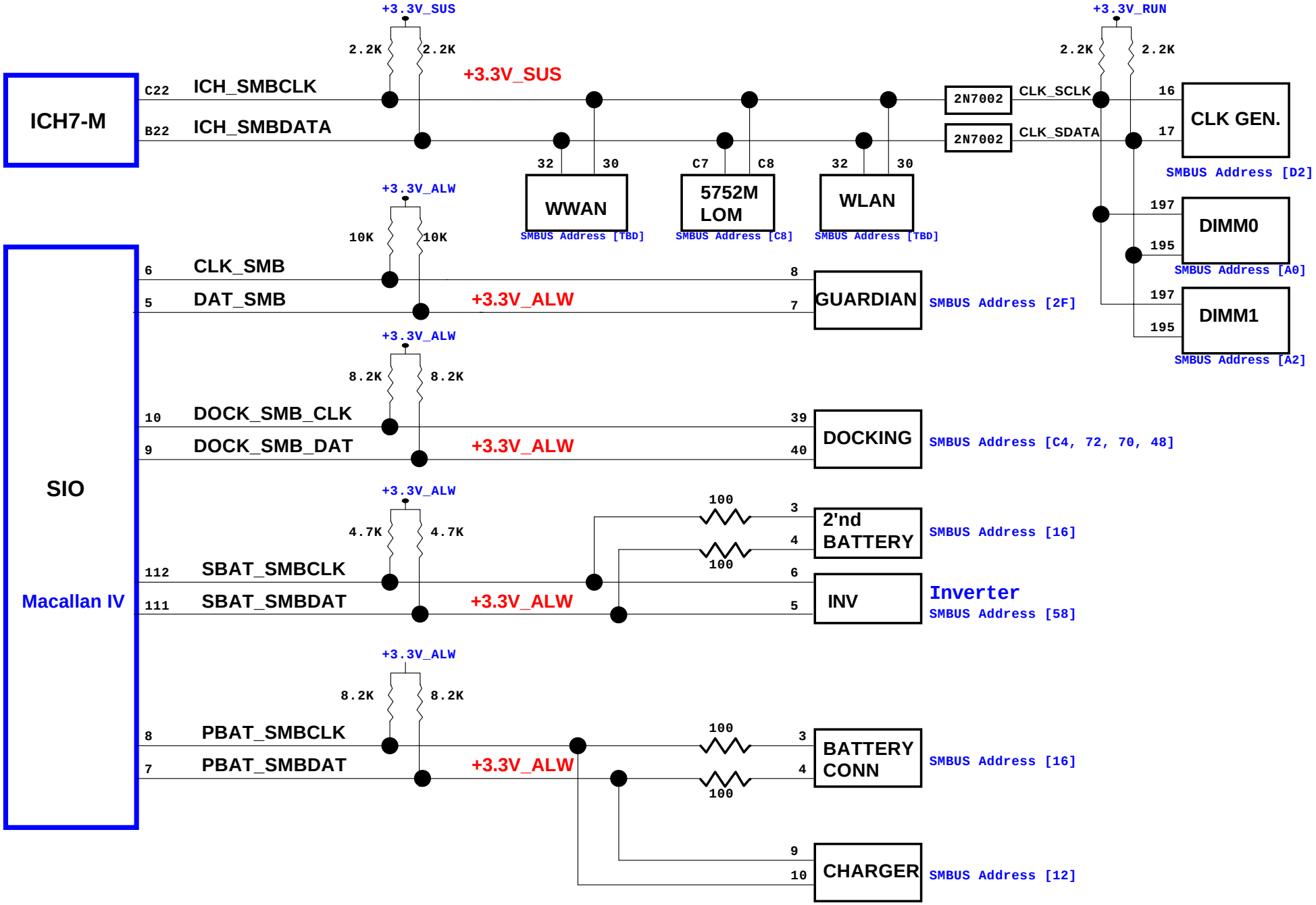
Title: Power Rail

Size | Document Number: LA-2791 | Rev: 0.6

Date: Tuesday, February 07, 2006 | Sheet 4 of 63



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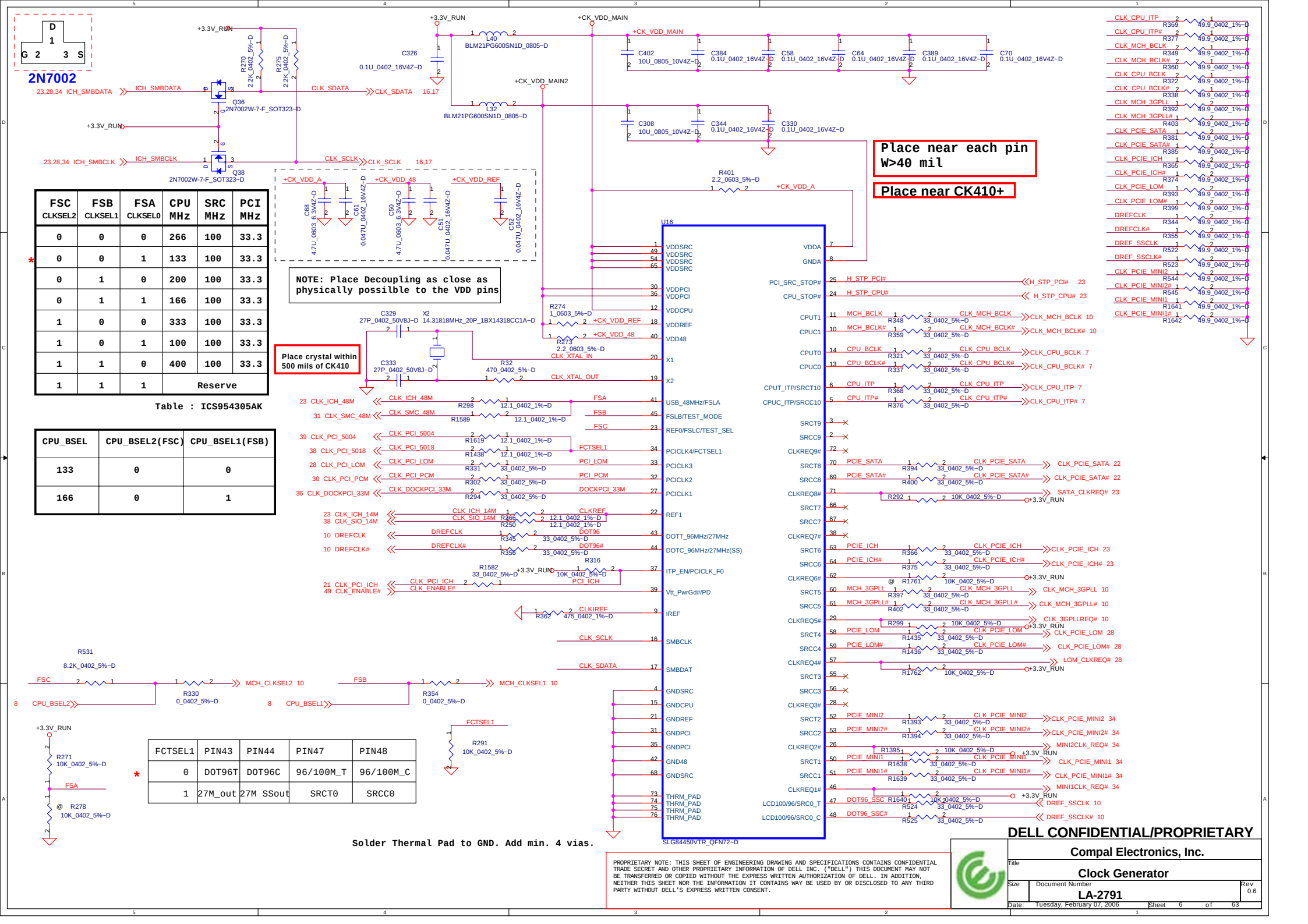
Title: SMBUS TOPOLOGY

Size | Document Number: LA-2791 | Rev: 0.6

Date: Tuesday, February 07, 2006 | Sheet 5 of 63

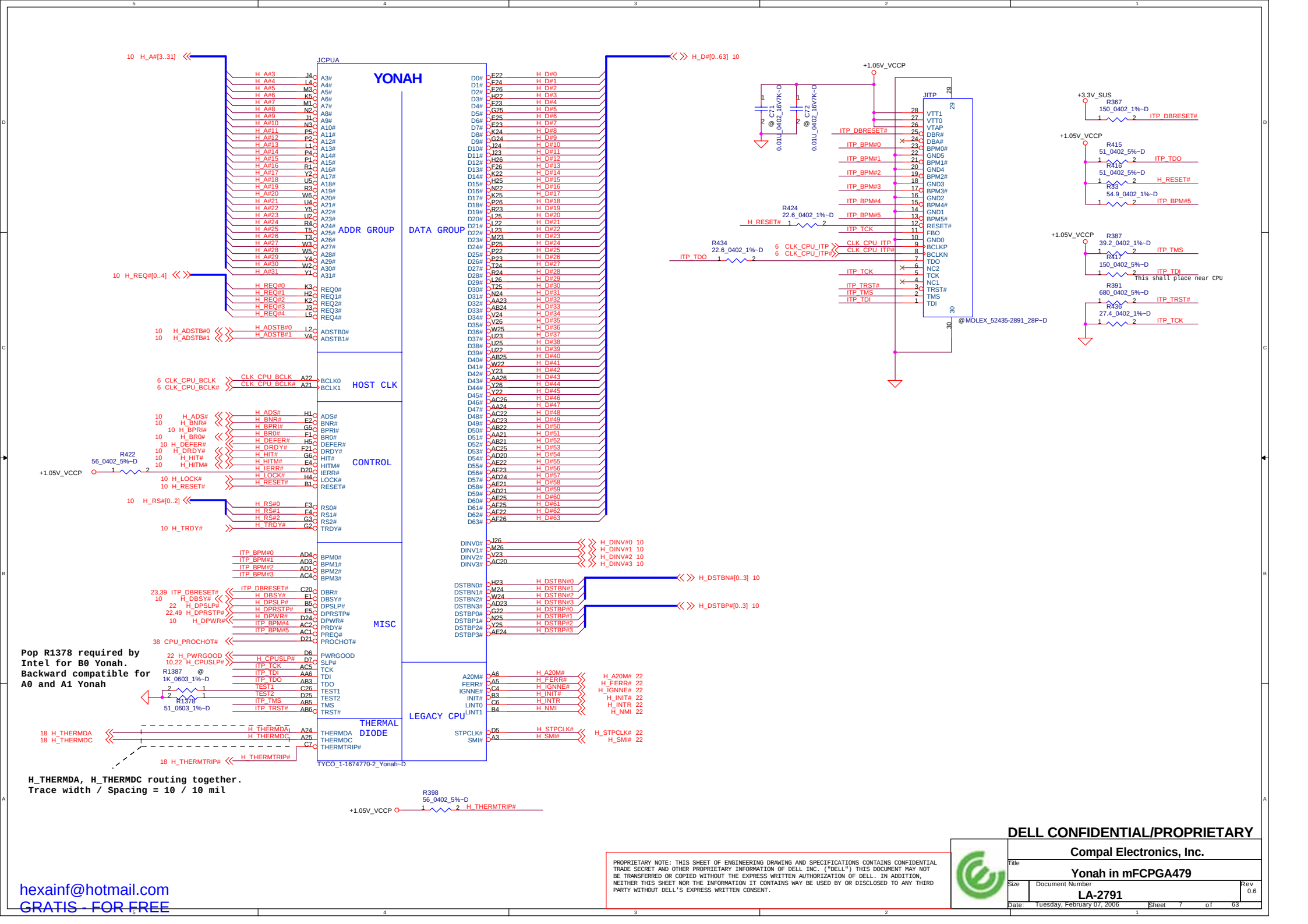


FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
* 0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	Reserve		

Table : ICS954305AK

CPU_BSEL	CPU_BSEL2(FSC)	CPU_BSEL1(FSB)
133	0	0
166	0	1

FCTSEL1	PIN43	PIN44	PIN47	PIN48
* 0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27M_out	27M SSout	SRCT0	SRCC0



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Title: Yonah in mFCPGA479

Size: | Document Number: LA-2791 | Rev: 0.6

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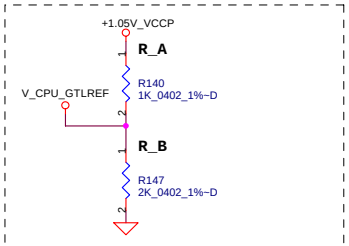
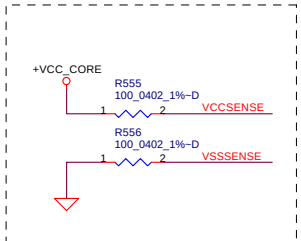
Length match within 25 mils

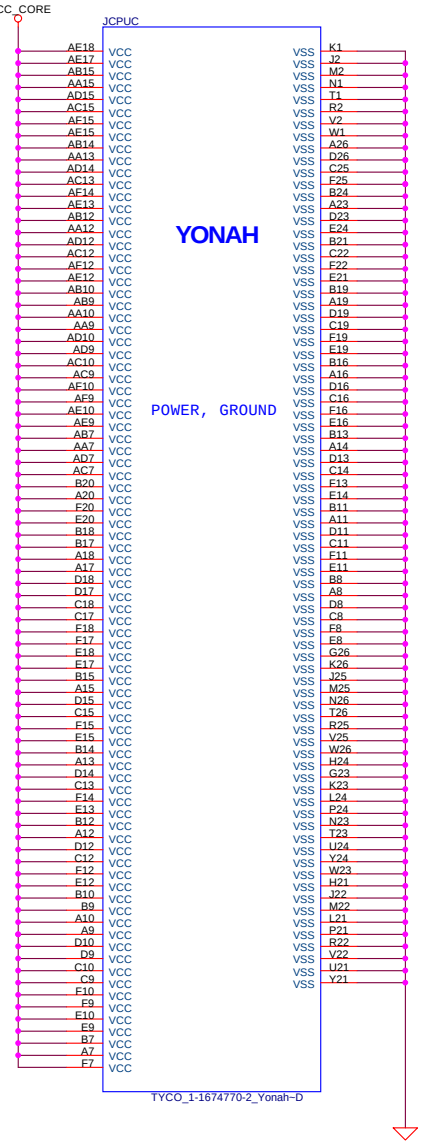


Layout close CPU PIN AD26 0.5 inch (max)



Layout close CPU

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.



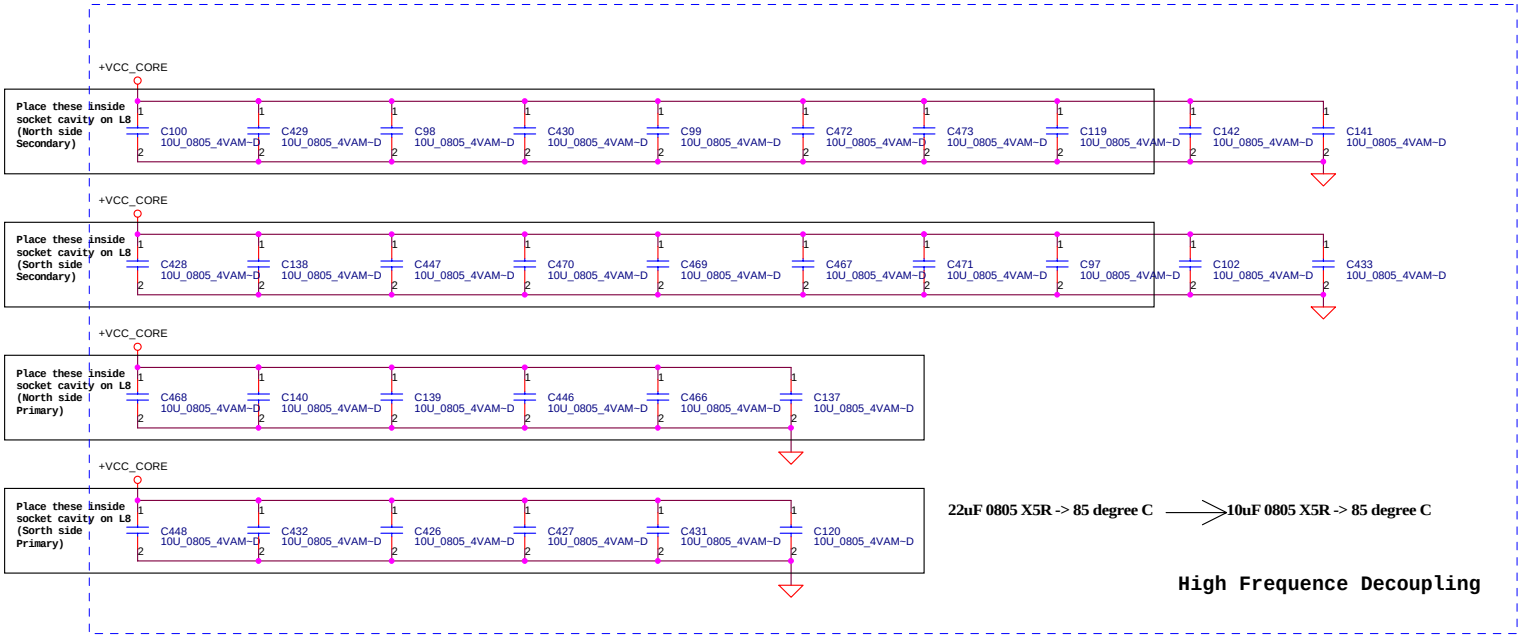
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

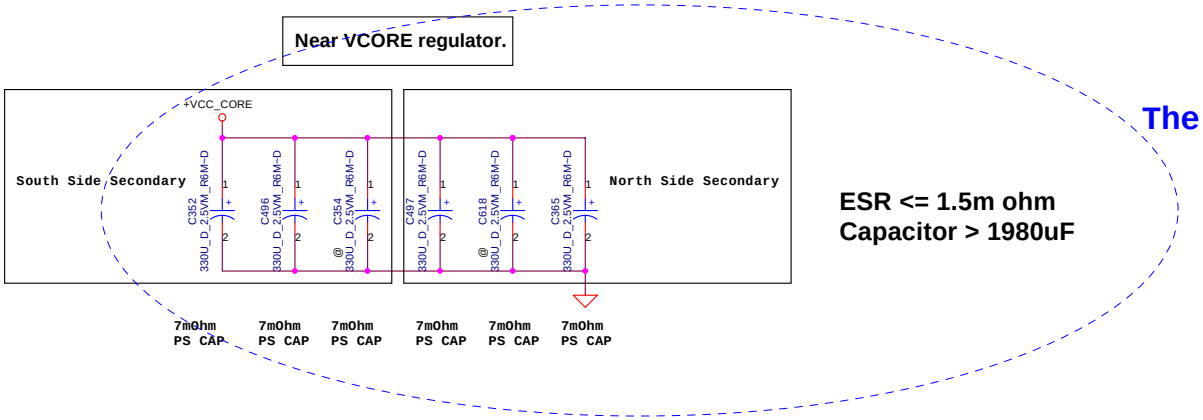
Compal Electronics, Inc.

Title: Yonah in mFCPGA479

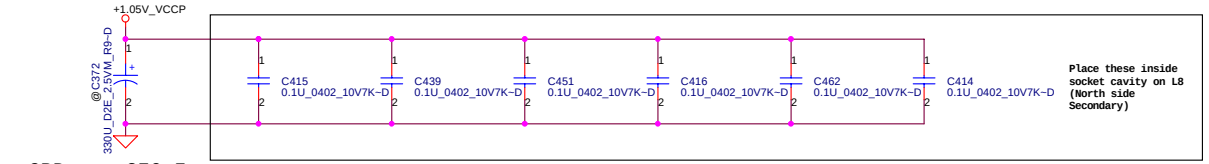
Size: Document Number: LA-2791 Rev: 0.6

Date: Tuesday, February 07, 2006 Sheet 8 of 63





The caps need change to ESR=6m ohms



CRB was 270uF

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Compal Electronics, Inc.
Title: CPU Bypass
Size: Document Number: LA-2791
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Description at page12

Note :
CFG3:17 has internal pullup,
CFG18:19 has internal pulldown

U40A

HOST

CALISTOGA A0_FCBGA1466~D

U40B

DMI

CFG

CLK

DDR MUXING

NC

PM

RESERVED

CALISTOGA A0_FCBGA1466~D

Layout Note:
H_XRCOMP & H_YRCOMP trace width and spacing is 10/20

Layout Note:
Route as short as possible

Stuff R435 & R437 for A1 Calistoga

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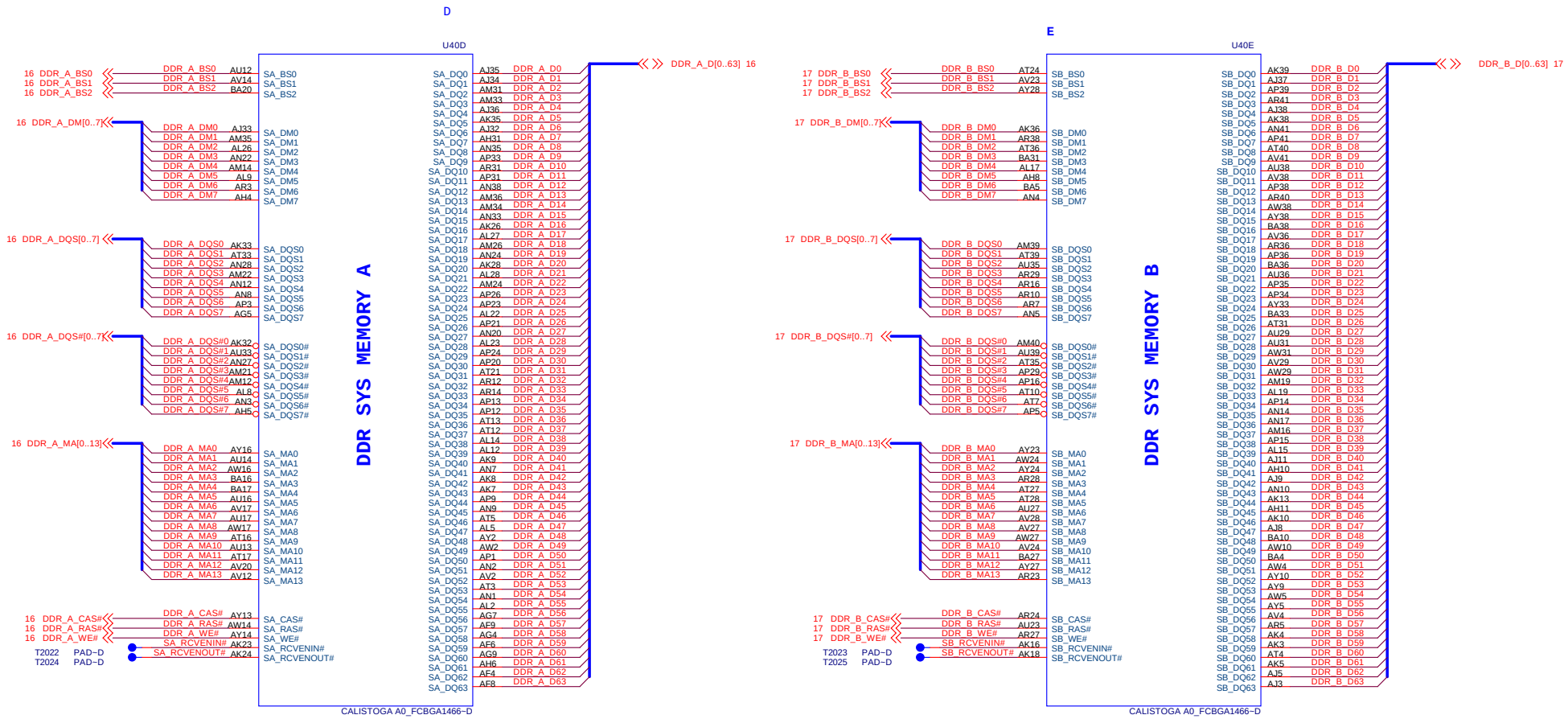
Title: Calistoga(1 of 6)

Size: | Document Number: LA-2791 | Rev: 0.6

Date: Tuesday, February 07, 2006 | Sheet 10 of 63



Compal Electronics, Inc.

Title: Calistogo(2 of 6)

Size | Document Number: LA-2791 | Rev: 0.6

Date: Tuesday, February 07, 2006 | Sheet 11 of 63

LOW = Moby Dick

Strap Pin Table

CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	LOW = Moby Dick HIGH = Calistoga *
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG11	
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (DMI Lane Reversal)	Low = Normal * Operation (Default): Lane number in Order High = Reverse Lane
SDVO_CTRLDATA	Low = No SDVO Device Present (Default)* High = SDVO Device Present
CFG20 (PCIE/SDVO select)	Low = Only PCIE or SDVO is operational. (Default)* High = PCIE/SDVO are operating simu.

CFG[3:17] have internal pullup

CFG[18:20] have internal pulldown

LVREF for Alviso N.C
for Calistoga to GND

Close to U40.J20

Close to U40.J22

CALISTOGA A0_FCBGA1466-D

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Title: Calistoga(3 of 6)

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+3V_TVDAC

U40H

+1.05V_VCCP

CRB 270uF

C411 220U_V_4VM_R45-D

POWER

CALISTOGA A0_FCBGA1466-D

C465 0.1U_0402_16V4Z-D

+2.5V_RUN

Should be placed on top

W=30 mils

+1.5VRUN_PCIE

BLM21PG600SN1D_0805-D

L35

C49 220U_V_4VM_R45-D

C53 10U_0805_4VAM-D

C59 10U_0805_4VAM-D

+1.5V_RUN

C345 0.1U_0402_16V4Z-D

Route +2.5VRUN from GMCH pinG41 to decoupling cap (C345)<200mil to the edge.

+1.5VRUN_3GPLL

+2.5V_RUN

L37 BLM18PG181SN1_0603-D

+2.5V_CRTDAC

C357 0.022U_0402_16V7K-D

C364 0.1U_0402_16V4Z-D

CRTDAC: Route caps within 250mil of Alviso. Route FB within 3" of Calistoga

+1.5VRUN_DPLLA

+1.5VRUN_DPLLB

+1.5VRUN_HPLL

+3.3V_RUN_R

Route VSSACRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

Route VSSA_TVBG GND from GMCH to decoupling cap ground lead and then connect to the GND plane.

+3VRUN_TVDACA

+3VRUN_TVDACB

+3VRUN_TVDACC

+3VRUN_ATVBG

VSSA_TVBG

+2.5V_RUN

C323 0.1U_0402_16V4Z-D

C318 0.01U_0402_16V7K-D

close pin A38

+3V_TVDAC

L9 BLM18PG181SN1_0603-D

+3.3V_RUN_R

C35 22n_0805_25V

C22 0.1U_0402_16V4Z-D

C599 10U_0805_4VAM-D

C306 22n_0805_25V

C239 0.1U_0402_16V4Z-D

R92 0_0603_5%-D

+3VRUN_ATV

C305 22n_0805_25V

C298 0.1U_0402_16V4Z-D

C598 4.7U_0603_6.3V4Z-D

C36 22n_0805_25V

C23 0.1U_0402_16V4Z-D

C35, C305, C306 replace by 0 ohm 0805 resistor

C391 4.7U_0603_6.3V4Z-D

C390 2.2U_0603_6.3V6K-D

U40_A6

C316 0.47U_0402_16V4Z-D

U40_D2

C118 0.22U_0402_10V4Z-D

C164 0.22U_0402_10V4Z-D

C435 0.47U_0402_16V4Z-D

U40_AB1

+1.5V_RUN

C310 10U_0805_4VAM-D

C325 0.01U_0402_16V7K-D

C336 0.1U_0402_16V4Z-D

C385 10U_0805_4VAM-D

C437 0.1U_0402_16V4Z-D

+2.5V_RUN

C314 4.7U_0603_6.3V4Z-D

C324 0.1U_0402_16V4Z-D

close pin B30/C30/A30

+1.5VRUN_QTVDAC

L11 BLM18PG181SN1_0603-D

+1.5V_RUN_TVDAC

C37 0.022U_0402_16V7K-D

C24 0.1U_0402_16V4Z-D

C304 0.022U_0402_16V7K-D

C297 0.1U_0402_16V4Z-D

Should be placed in cavity

+1.5VRUN_3GPLL

R267 0.5_0805_1%-D

+3GPLL_R

L34 BLM18PG181SN1_0603-D

C404 0.1U_0402_16V4Z-D

C511 10U_0805_4VAM-D

C332 0.1U_0402_16V4Z-D

+1.5VRUN_HPLL

45mA Max.

L39 BLM18AG121SN1D_0603-D

C413 0.1U_0402_16V4Z-D

C94 22U_0805_6.3VAM-D

+1.5VRUN_MPLL

45mA Max.

L38 BLM18AG121SN1D_0603-D

C418 0.1U_0402_16V4Z-D

C419 22U_0805_6.3VAM-D

+1.5VRUN_DPLLA

40mA Max.

L28 10U_MLZ2012E100PTAIN_60mA_25%_0805-D

C322 0.1U_0402_16V4Z-D

C294 470U_D2_2.5VM-D

+1.5VRUN_DPLLB

40mA Max.

L33 10U_MLZ2012E100PTAIN_60mA_25%_0805-D

C331 0.1U_0402_16V4Z-D

C335 470U_D2_2.5VM-D

+1.05V_VCCP

R320 10_0402_5%-D

+2.5V_RUN

D14 MMBD4148_SOT23-D

CRT DAC Voltge Follower Circuit - 700mV

+1.5V_RUN

R12 10_0402_5%-D

+3.3V_RUN_R

D8 MMBD4148_SOT23-D

TV DAC Voltge Follower Circuit - 700mV

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Title: Calistoga(4 of 6)

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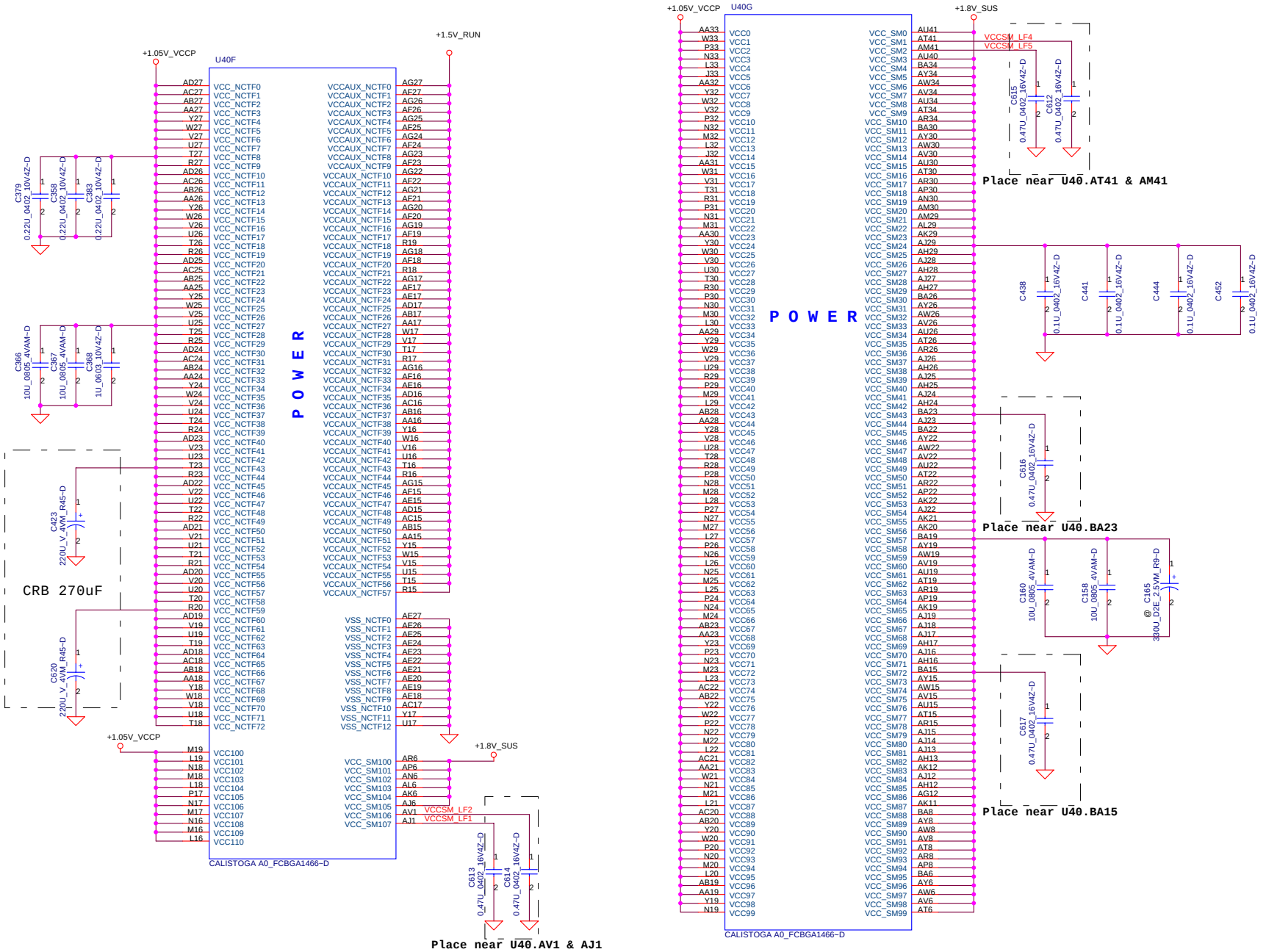

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Title: Calistoga(5 of 6)

Size: | Document Number: LA-2791 | Rev: 0.6

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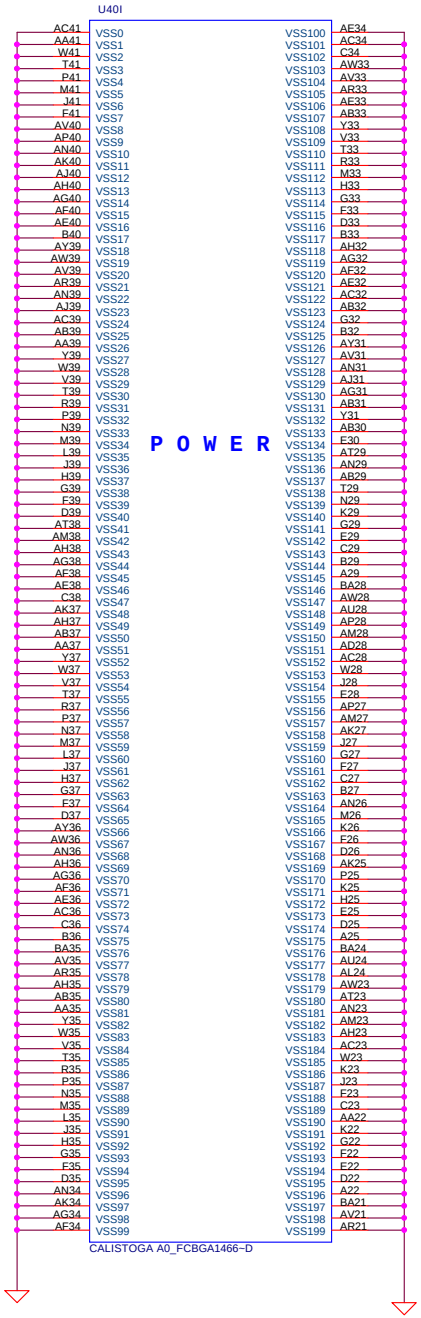

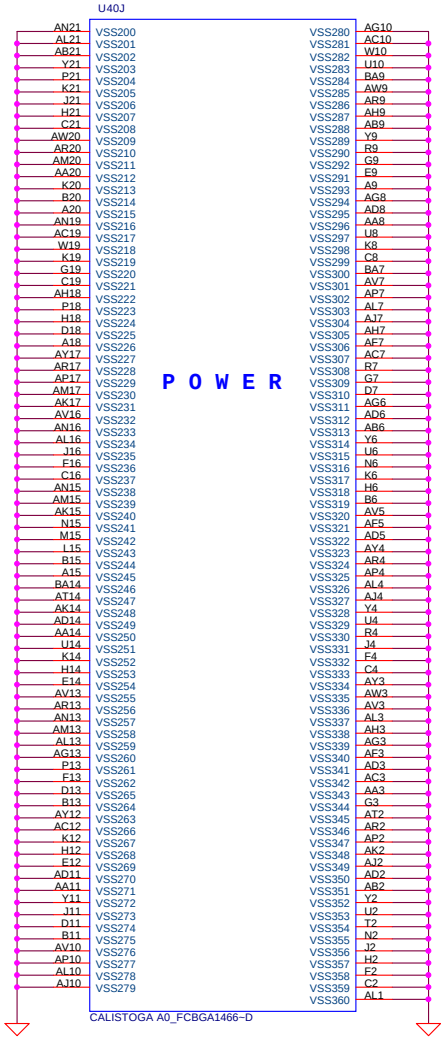

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Title: Calistoga(6 of 6)

Size: | Document Number: LA-2791 | Rev: 0.6

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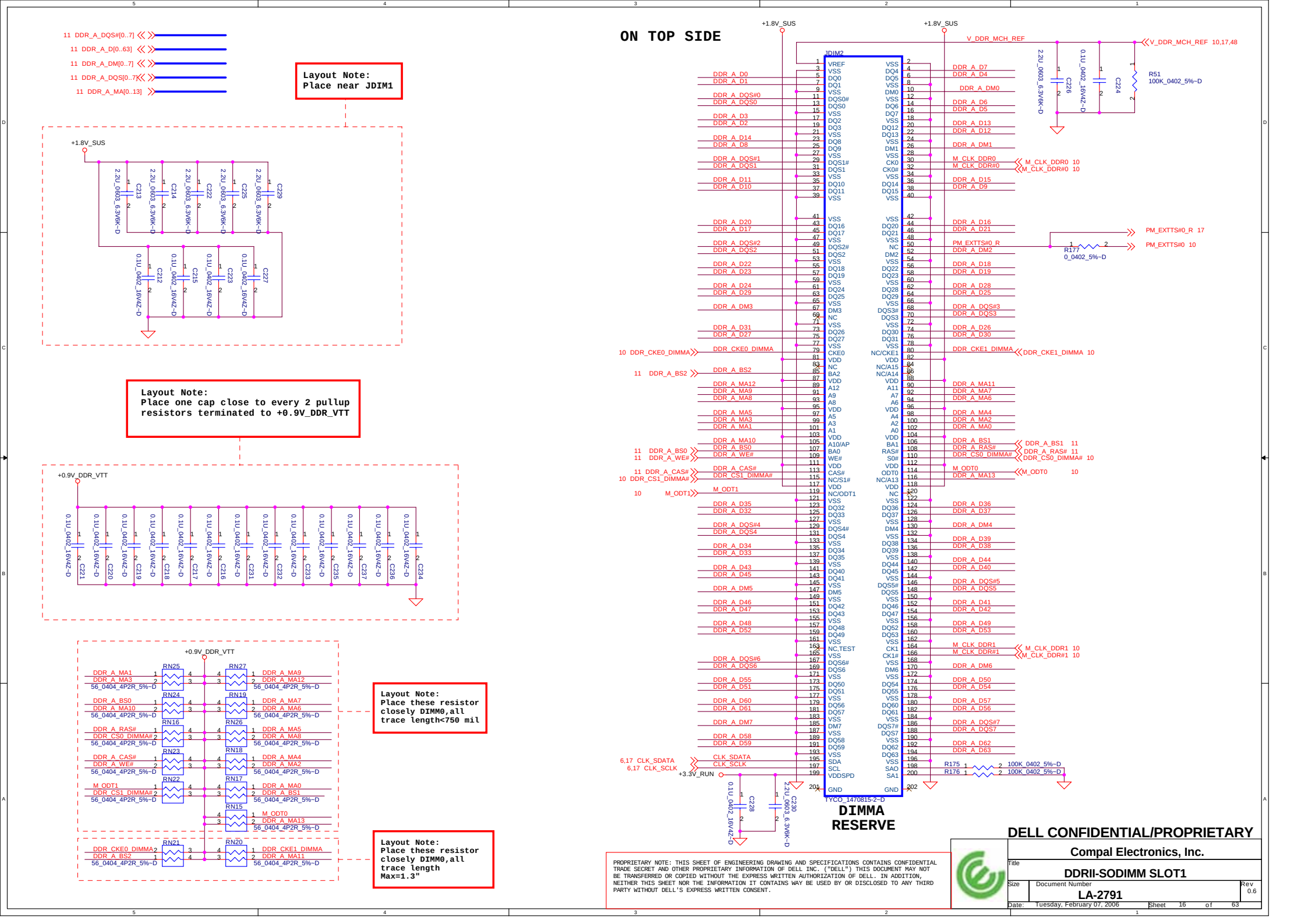
ON TOP SIDE
Layout Note:
Place near JDIM1
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
Layout Note:
Place these resistor
closely DIMM0,all
trace length<750 mil
Layout Note:
Place these resistor
closely DIMM0,all
trace length
Max=1.3"
JDIM2
TYCO_1470815-2-D
DIMMA
RESERVE
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DDRII-SODIMM SLOT1
LA-2791
Rev 0.6
Tuesday, February 07, 2006
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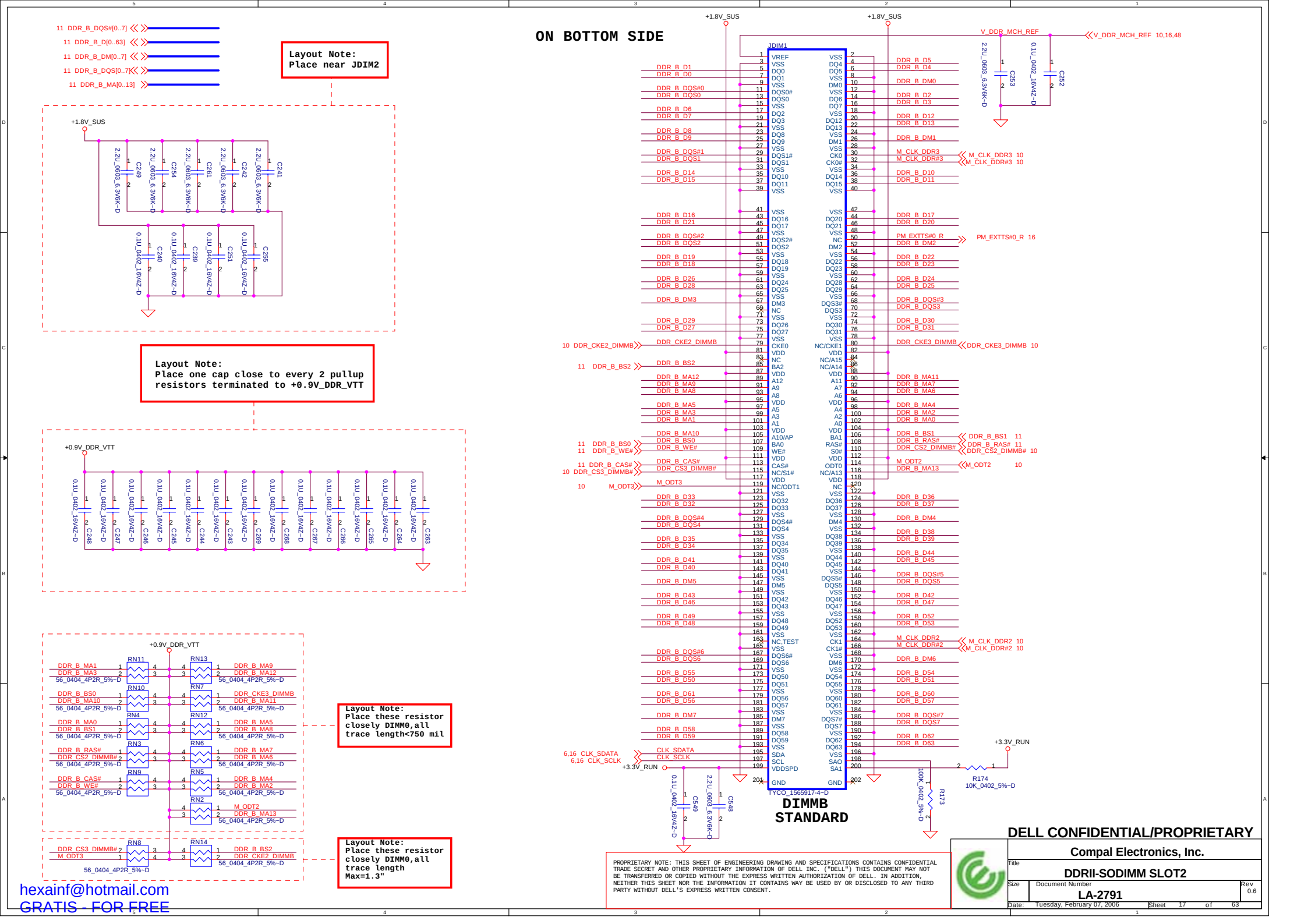
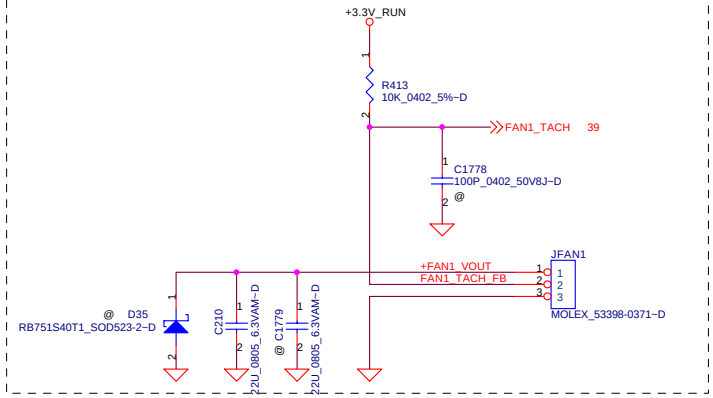
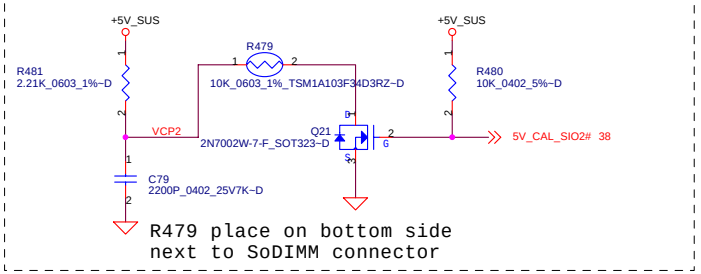


FAN1 Control and Tachometer



Place near the bottom SODIMM

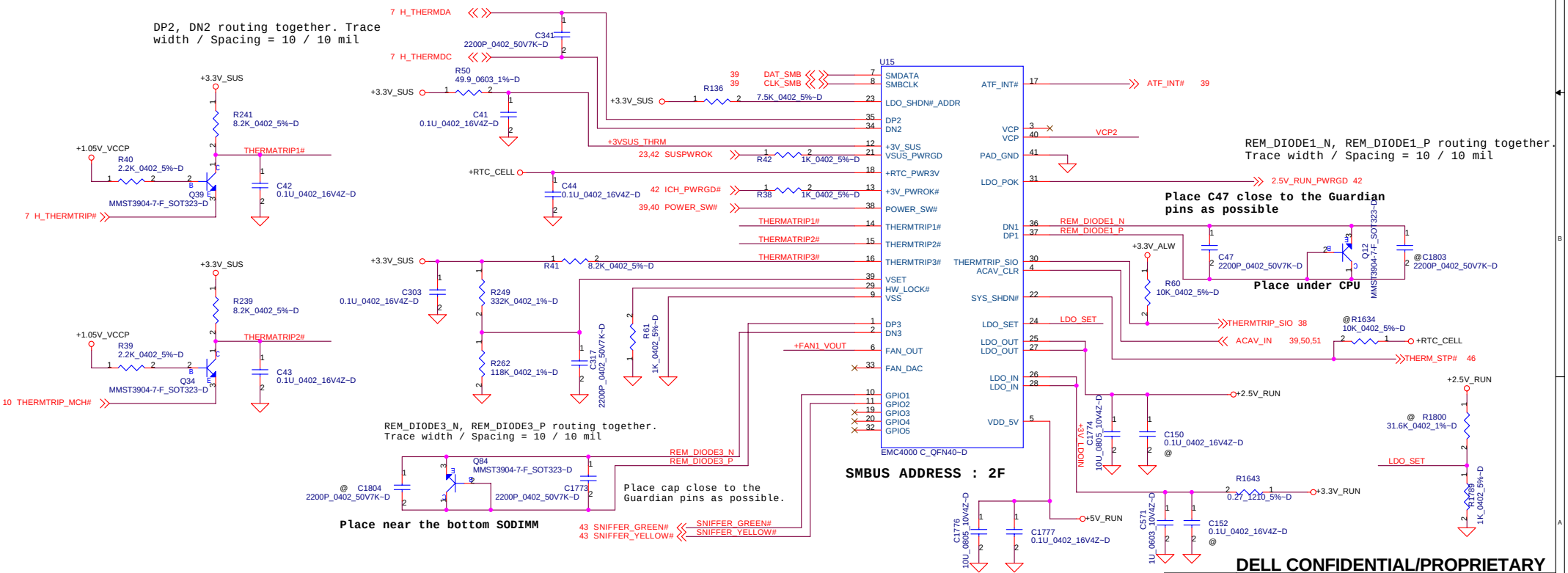


$$VSET = \frac{R262}{R249+R262} \times 3.3V$$

$$VSET = \left(\frac{Tp-70}{21}\right)$$

Place C341 close to the Guardian pins as possible

DP2, DN2 routing together. Trace width / Spacing = 10 / 10 mil



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Compal Electronics, Inc.	
Title	FAN & Thermal Sensor
Size	Document Number: LA-2791
Rev	0.6
Date:	Tuesday, February 07, 2006
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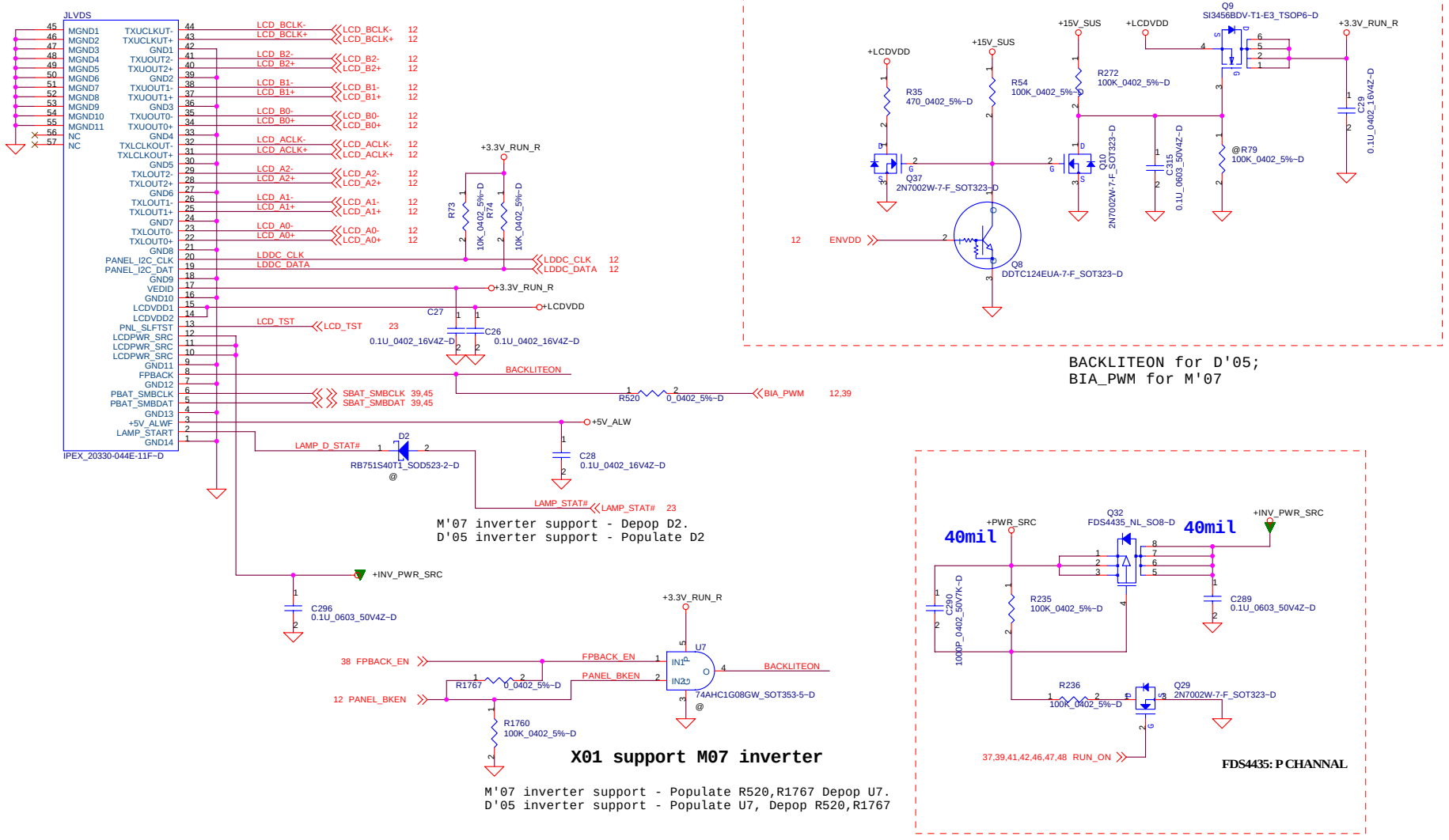

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Compal Electronics, Inc.	
Title	Internal LVDS
Size	Document Number: LA-2791
Rev	0.6
Date:	Tuesday, February 07, 2006
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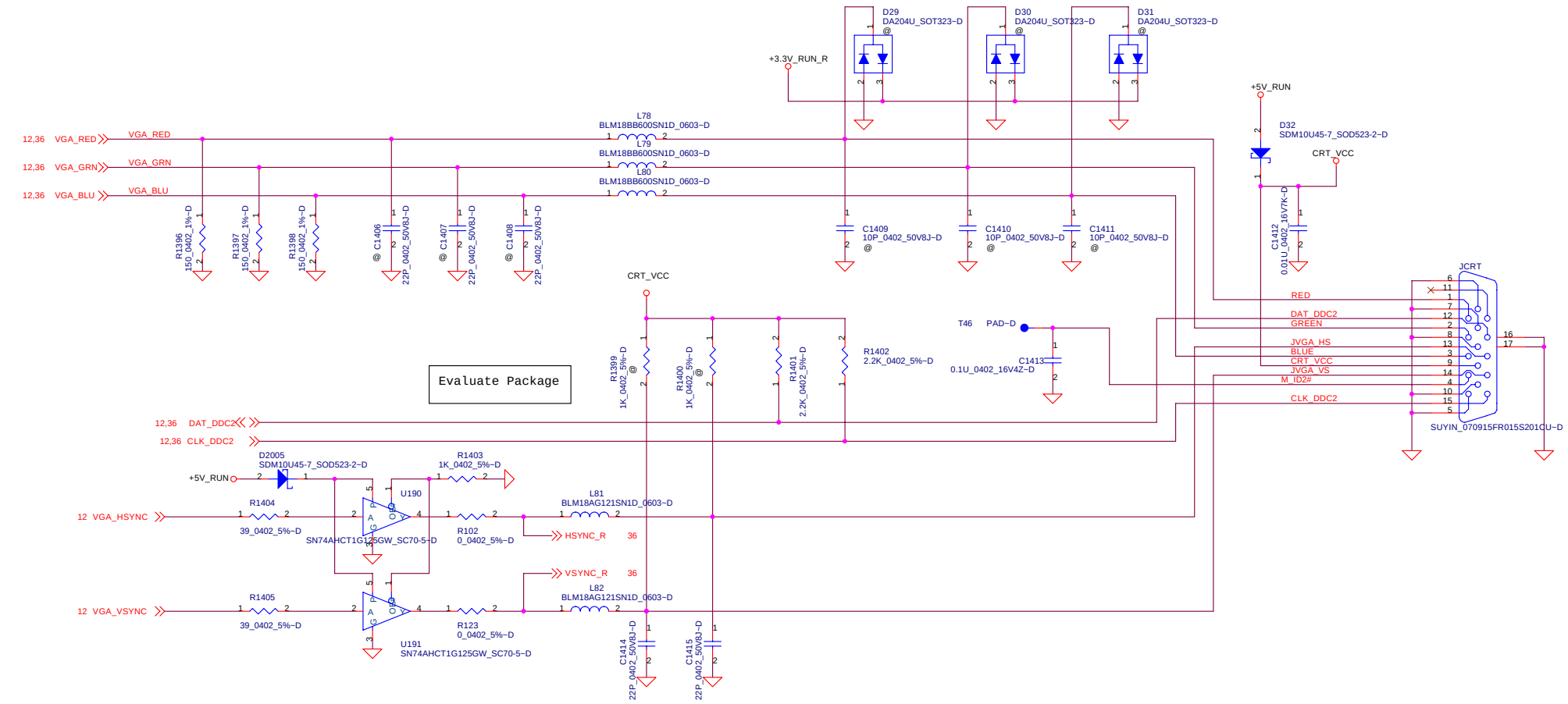

DA204U

K1 A2

A1 K2

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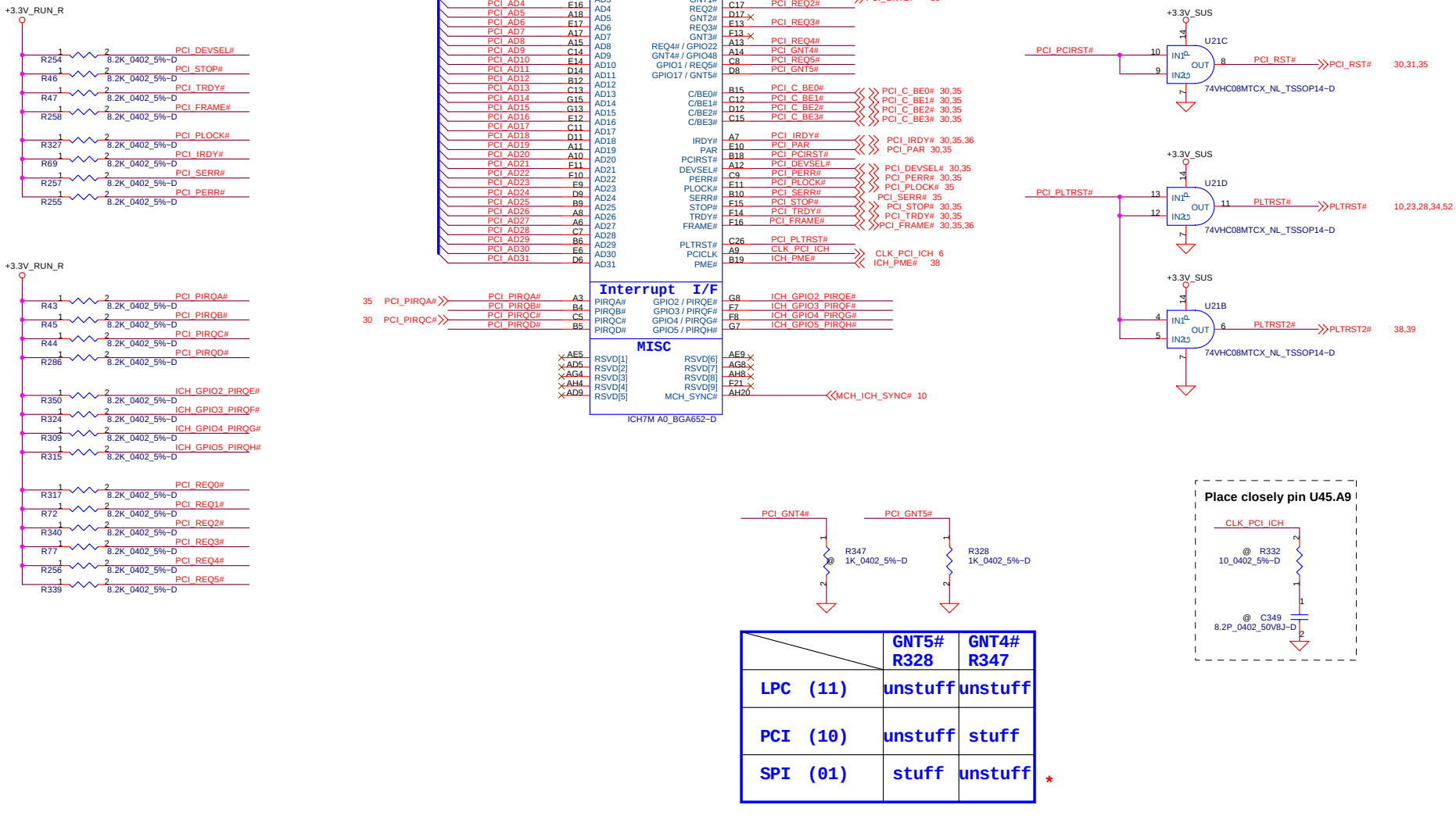
Compal Electronics, Inc.

Title: CRT

Size | Document Number: LA-2791 | Rev: 0.6

Date: Tuesday, February 07, 2006 | Sheet 20 of 63



	GNT5# R328	GNT4# R347
LPC (11)	unstuff	unstuff
PCI (10)	unstuff	stuff
SPI (01)	stuff	unstuff *

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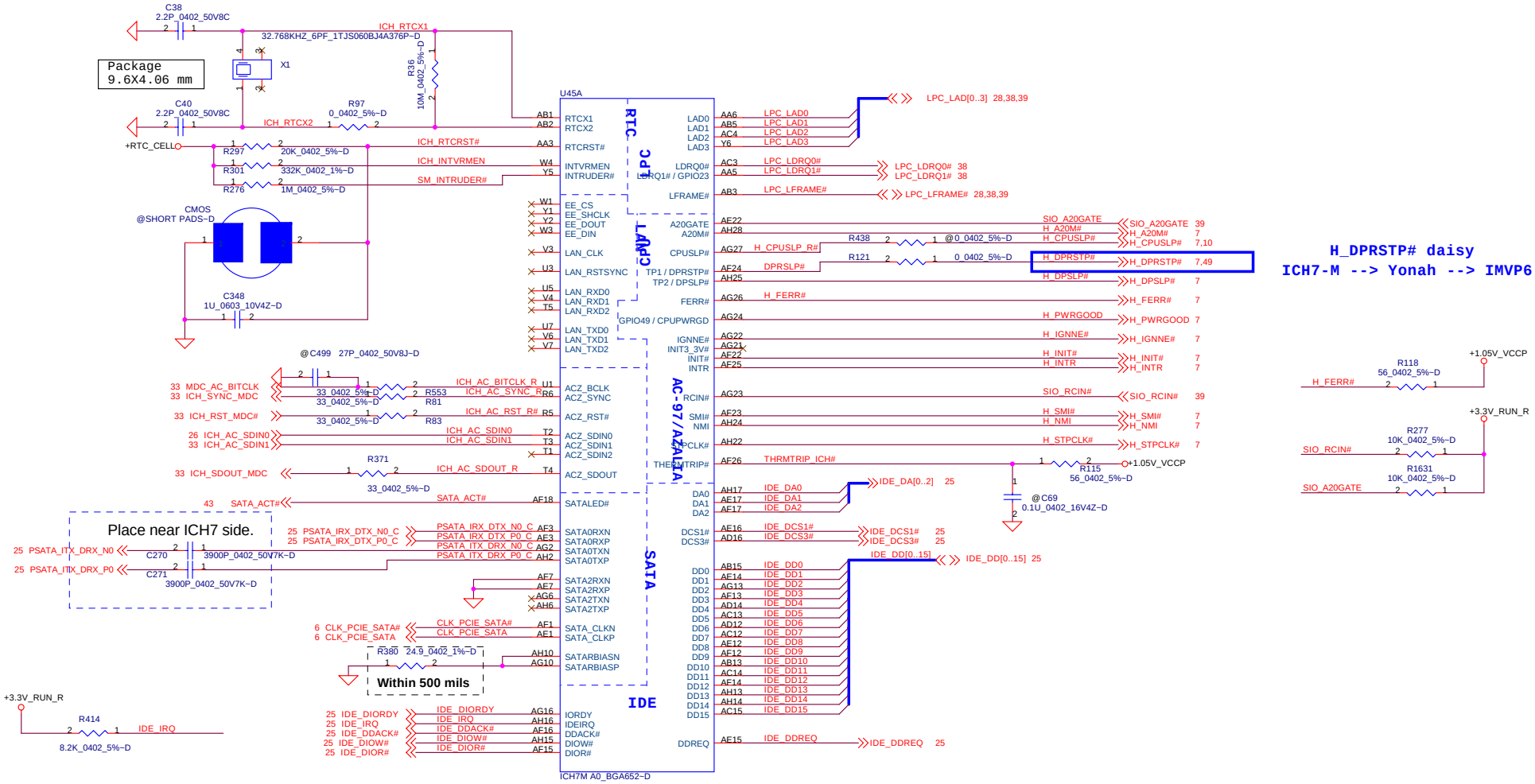
Compal Electronics, Inc.

Title: ICH7(1/4)

Size: | Document Number: LA-2791 | Rev: 0.6

Date: Tuesday, February 07, 2006 | Sheet 21 of 63

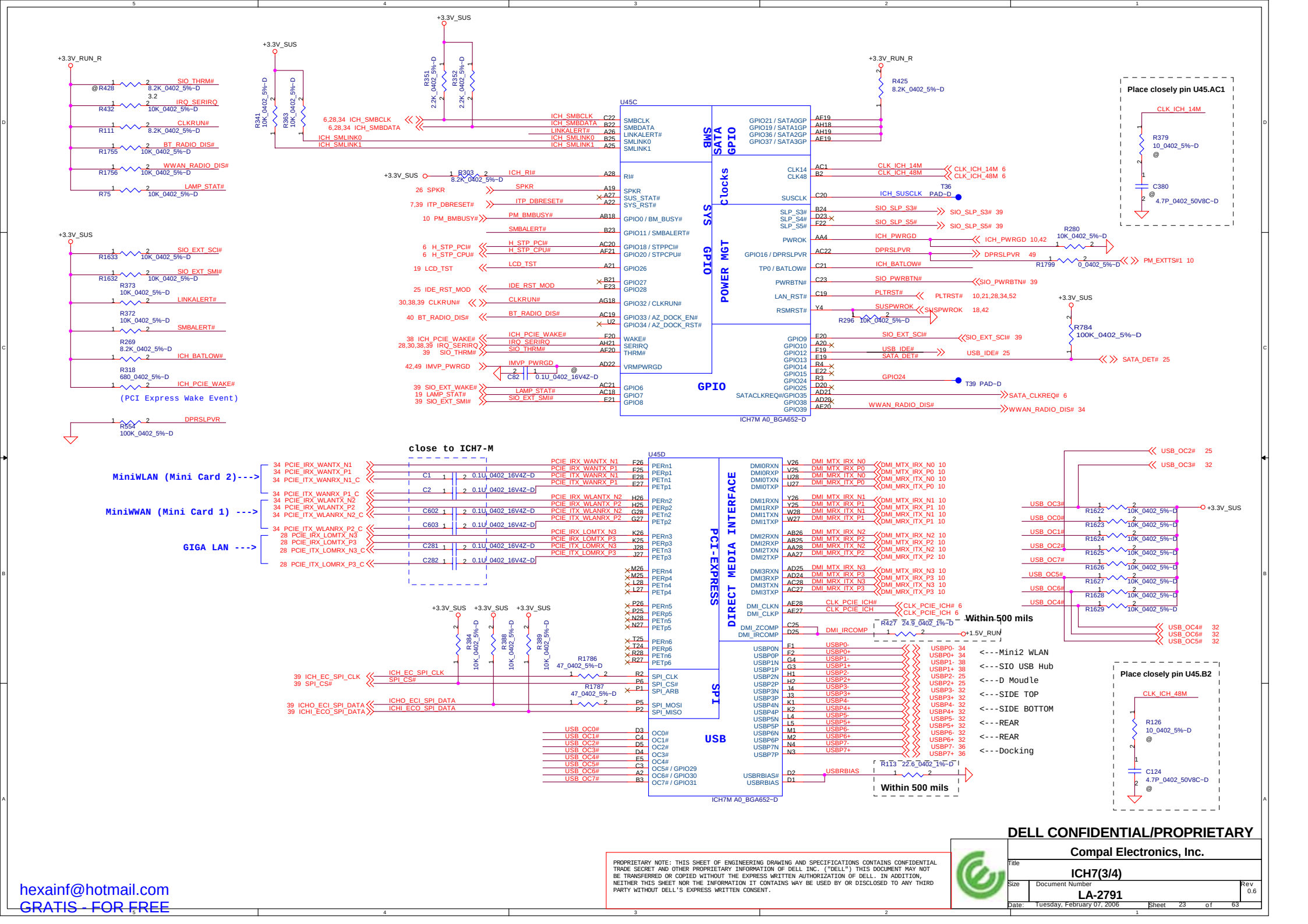


Compal Electronics, Inc.

Title: ICH7(2/4)

Size: | Document Number: LA-2791 | Rev: 0.6

Date: Tuesday, February 07, 2006 | Sheet 22 of 63

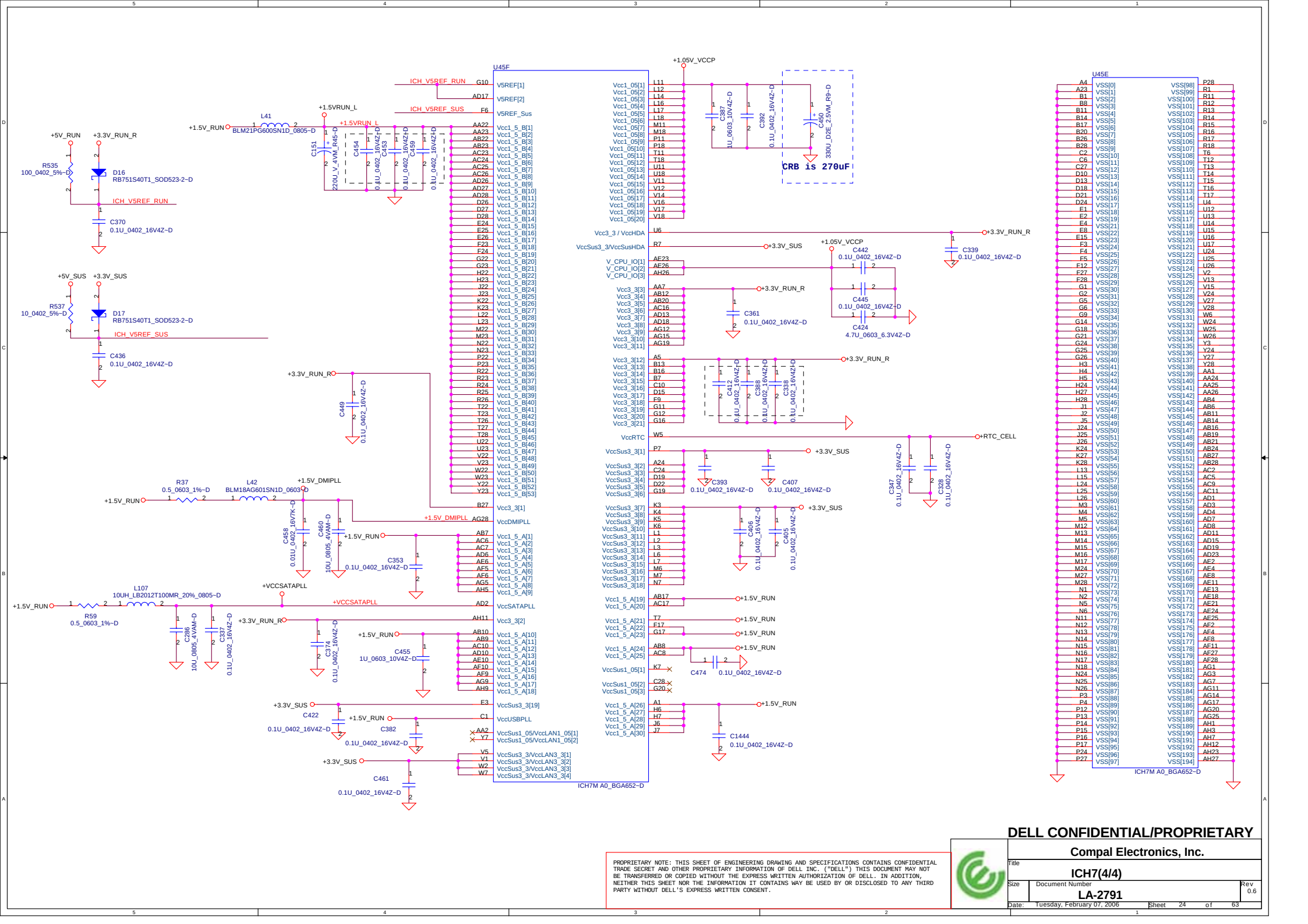


Compal Electronics, Inc.

Title: ICH7(3/4)

Size: | Document Number: LA-2791 | Rev: 0.6

Date: Tuesday, February 07, 2006 | Sheet 23 of 63



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Compal Electronics, Inc.	
Title	ICH7(4/4)
Size	Document Number: LA-2791
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Date:	Tuesday, February 07, 2006
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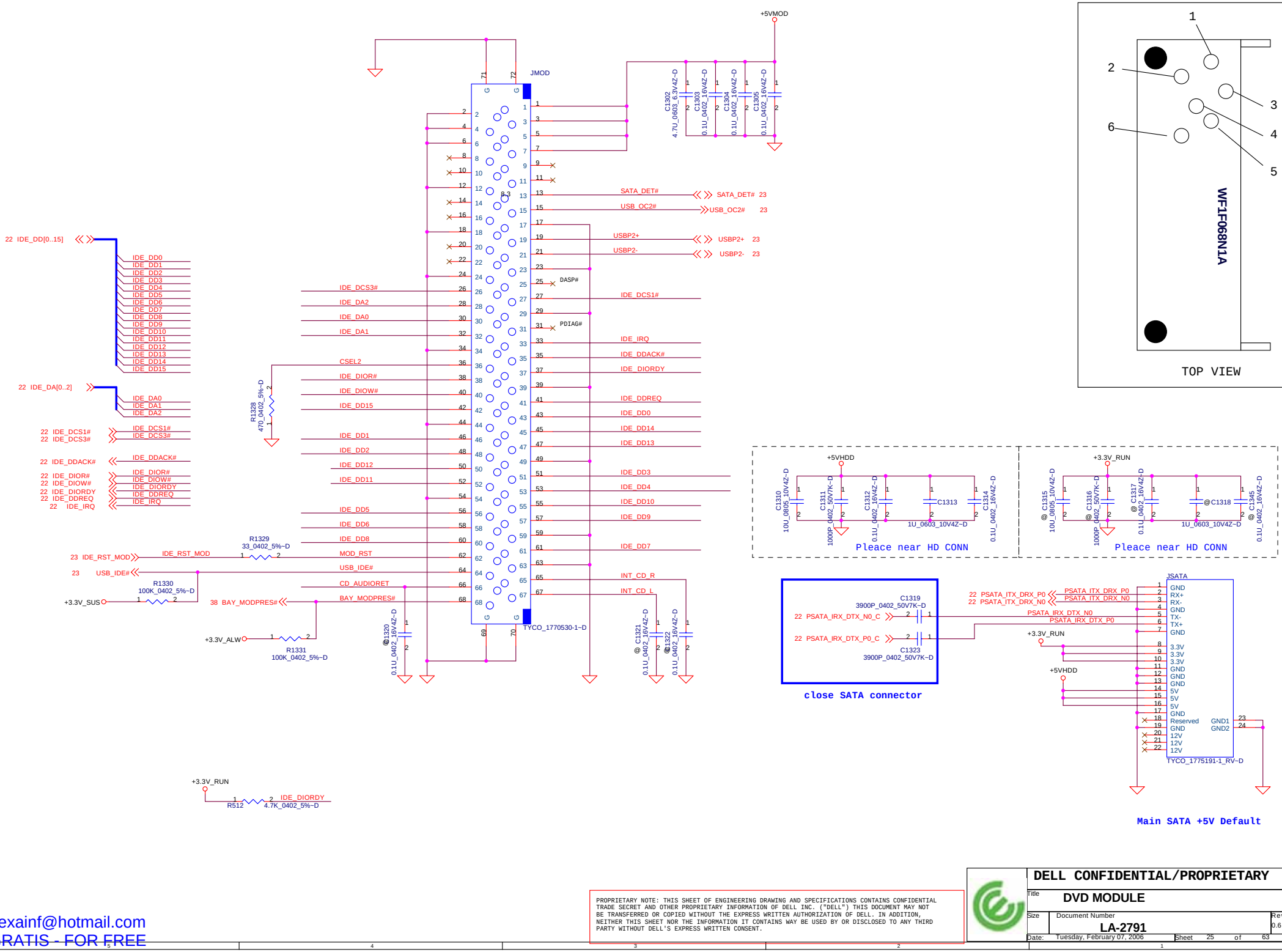

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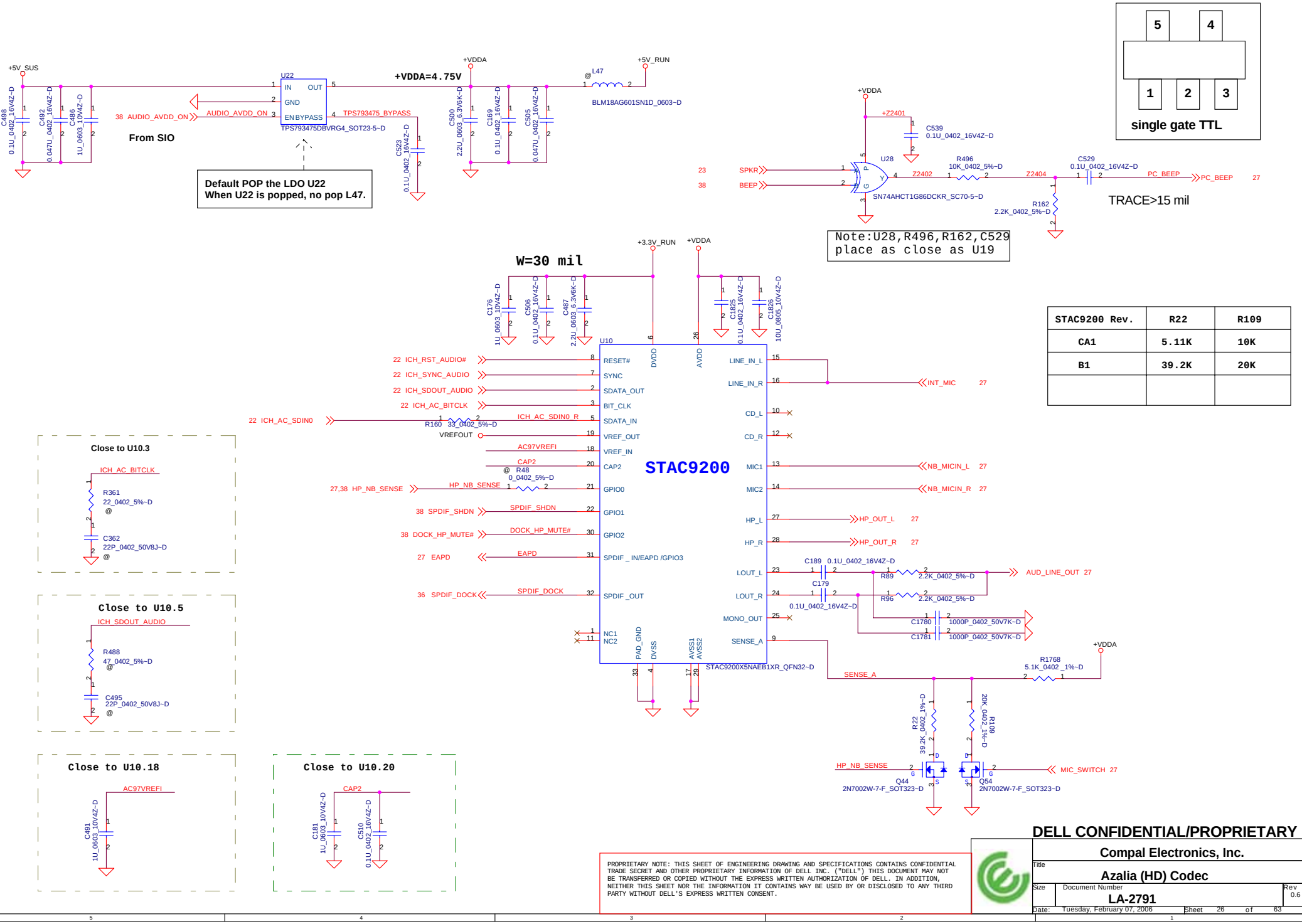
Title: DVD MODULE

Size: | Document Number: LA-2791 | Rev: 0.6

Date: Tuesday, February 07, 2006 | Sheet 25 of 63



STAC9200 Rev.	R22	R109
CA1	5.11K	10K
B1	39.2K	20K

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Title: Azalia (HD) Codec

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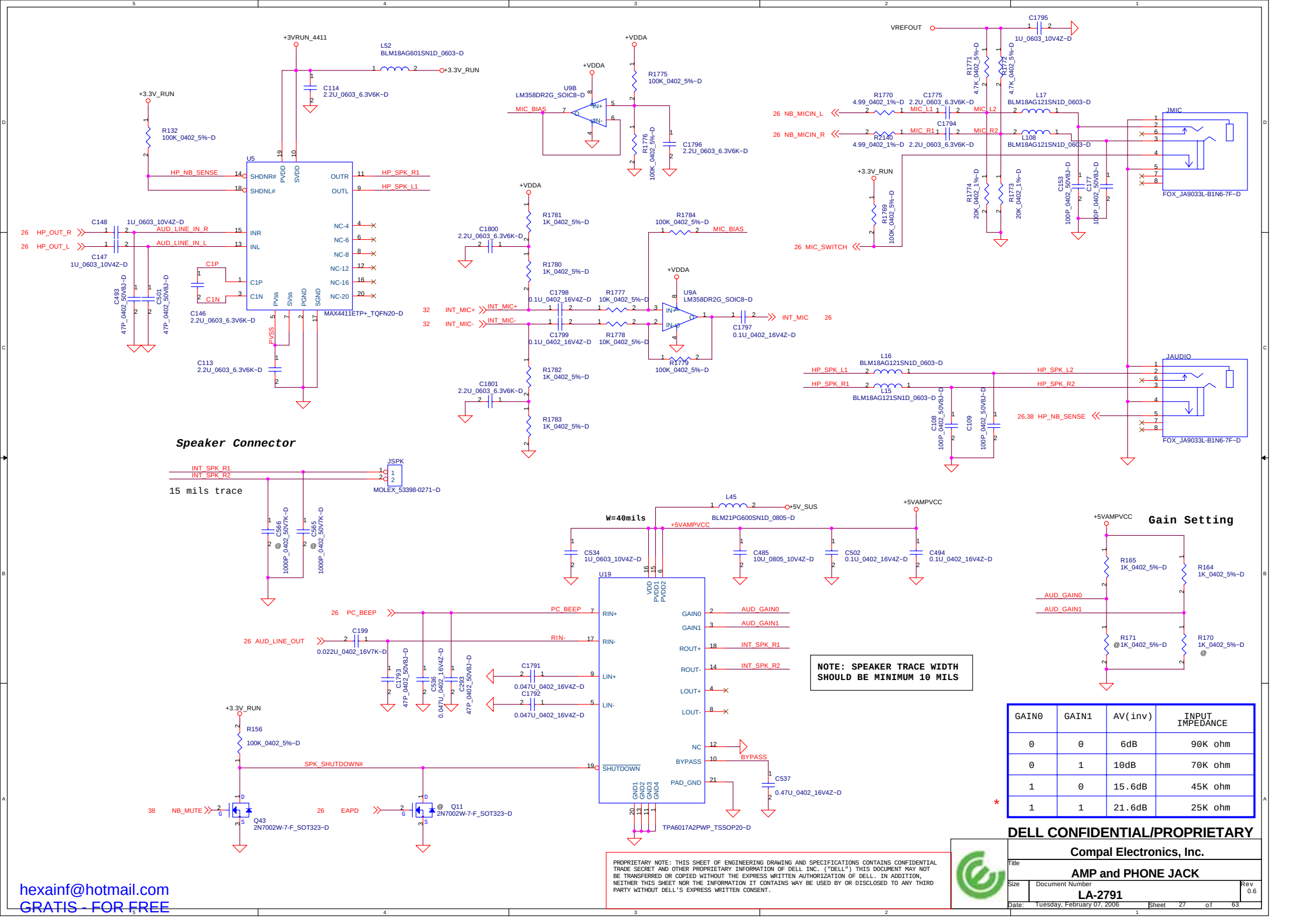

GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm

*

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Compal Electronics, Inc.

Title: AMP and PHONE JACK

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Layout Notice : Place as close chip as possible.

MMJT9435

Layout Notice : 1.2V filter. Place as close chip as possible.

R7, R9 are 1/2 W rating

Pop C1375 for 5752-A0,
De-pop for 5752-A1

Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC

Place closely pin J8

	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1

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Title: BCM5751M

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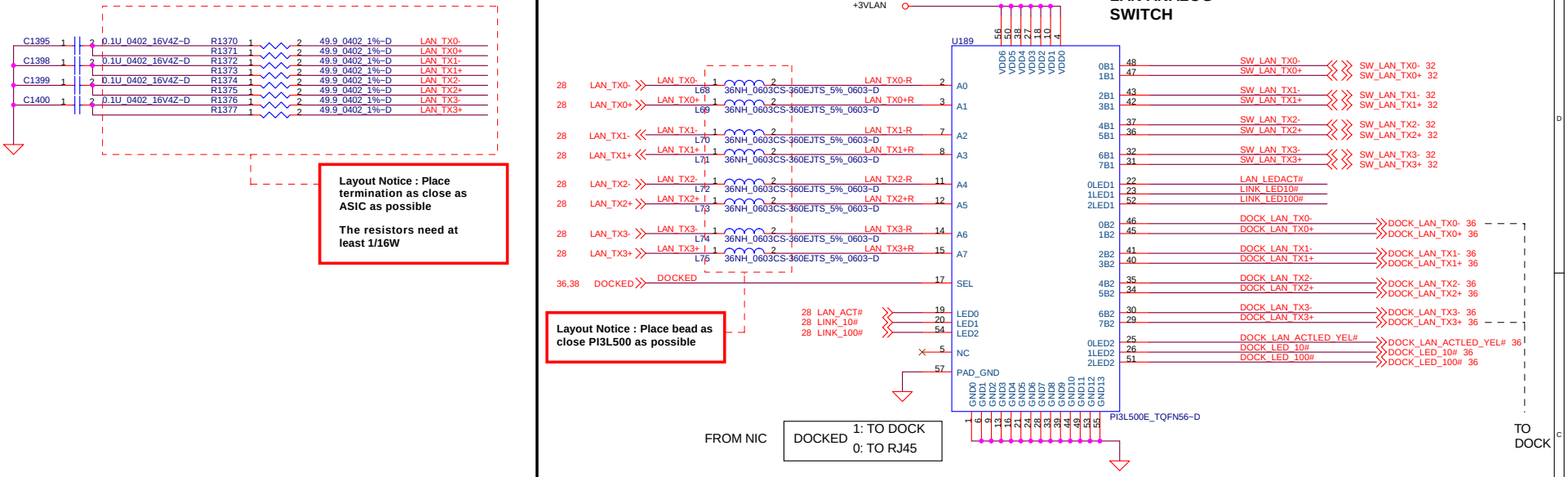

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Title: LAN TRANSFOMER

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NOTE:
THIS PAGE SHOWS THE OZ601B CONFIGURED WITH
EXTERNAL IDSEL AND WITHOUT 12V VPP SUPPORT.

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.
IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE
PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS
FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY
CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST
BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

Place closely pin 26

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Title: Card Bus OZ601

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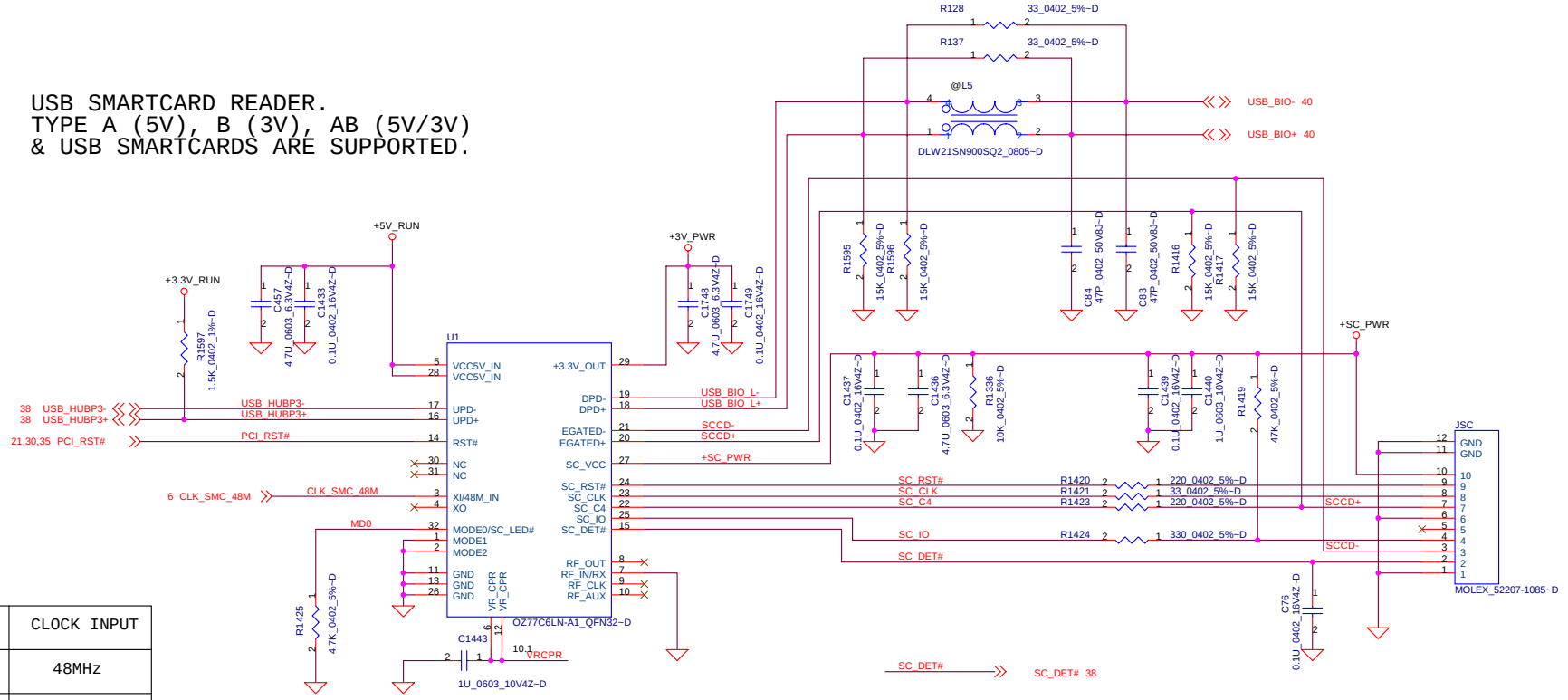
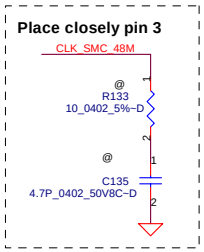
USB SMARTCARD READER.
TYPE A (5V), B (3V), AB (5V/3V)
& USB SMARTCARDS ARE SUPPORTED.



MODE1	CLOCK INPUT
LOW	48MHz
HIGH	6MHz Crystal



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Compal Electronics, Inc.

Title: Smart Card OZ77C6

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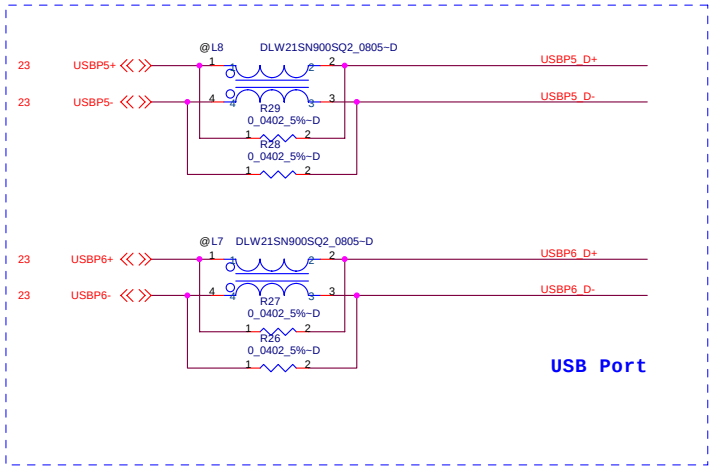

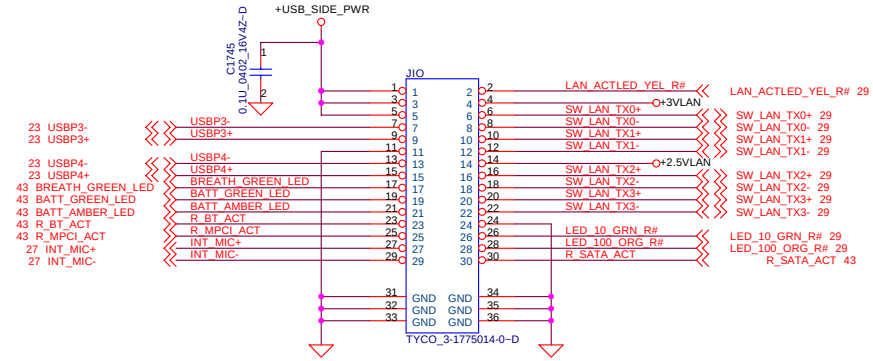

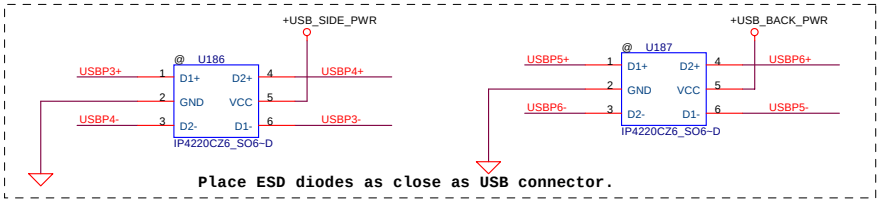

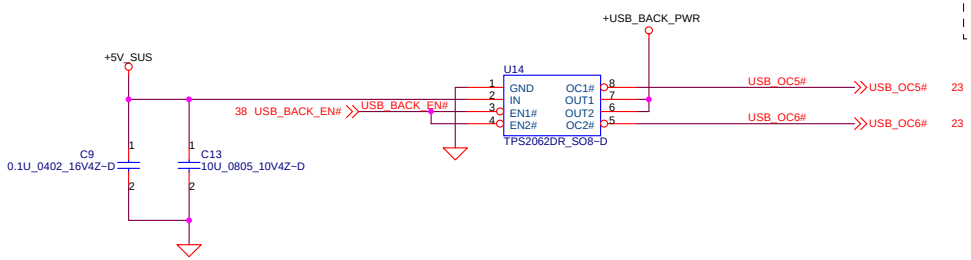

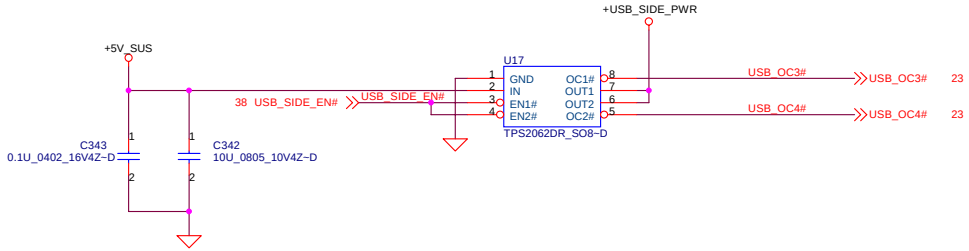

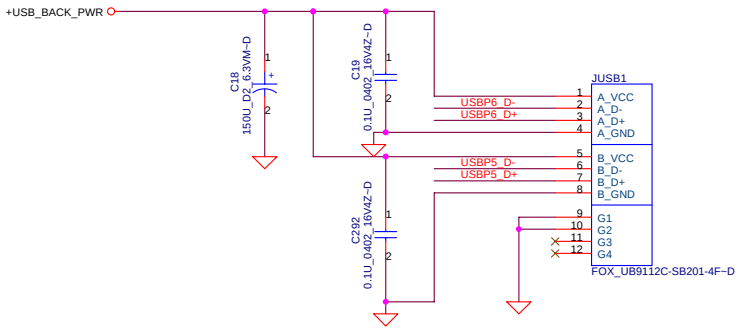

Rear USB Ports

Compal Electronics, Inc.

Title: USB 2.0 Port

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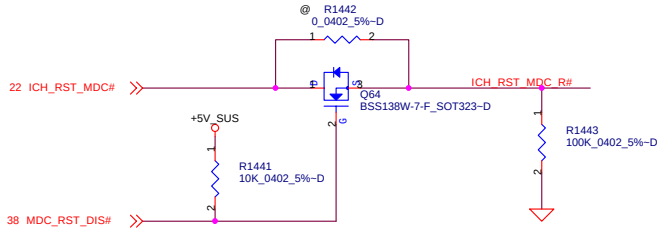
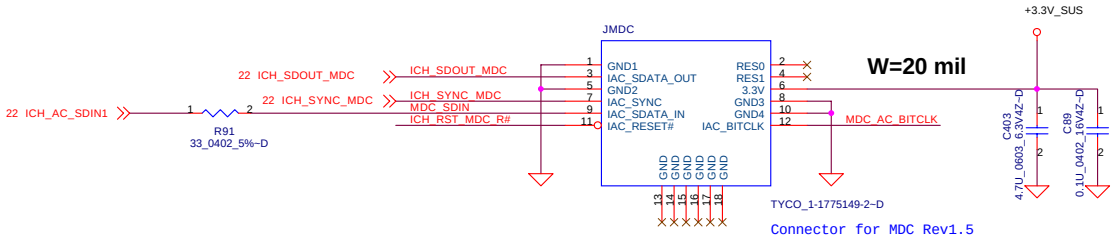
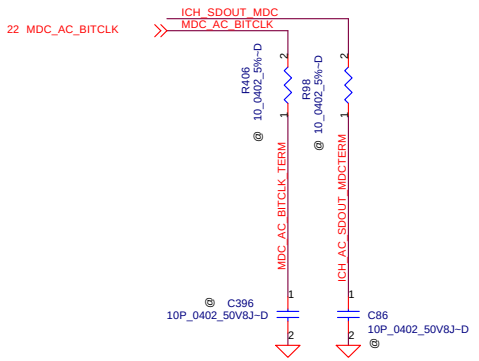


New MDC connector.

1	GND	RES	2
3	IAC_SDATA0	RES	4
5	GND	3.3V	6
7	IAC_SYNC	GND	8
9	IAC_SDATAIN	GND	10
11	IAC_RESET#	IAC_BITCLK	12





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Compal Electronics, Inc.

Title: BT PORT and MDC

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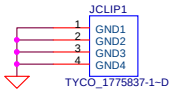
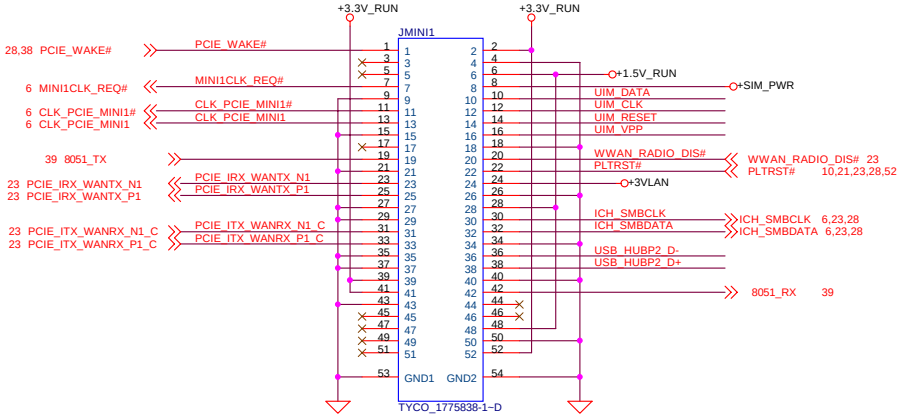
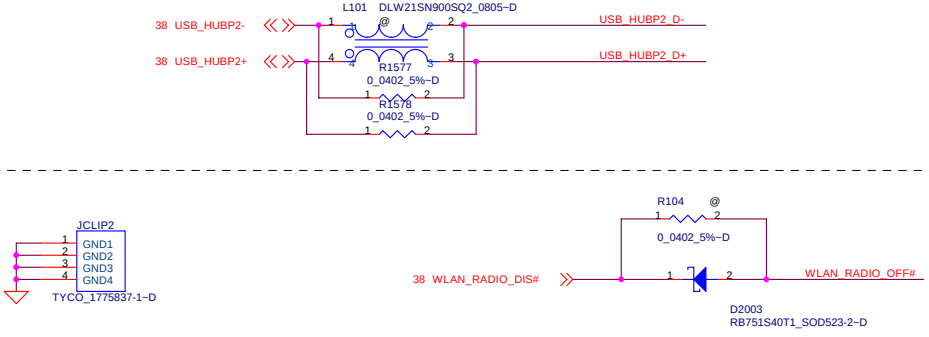
Mini Card
Wire less WAN



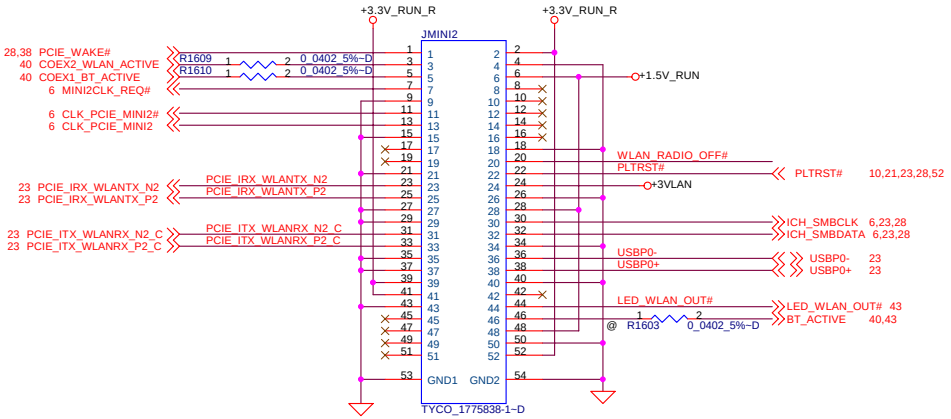
Mini-Card Latch

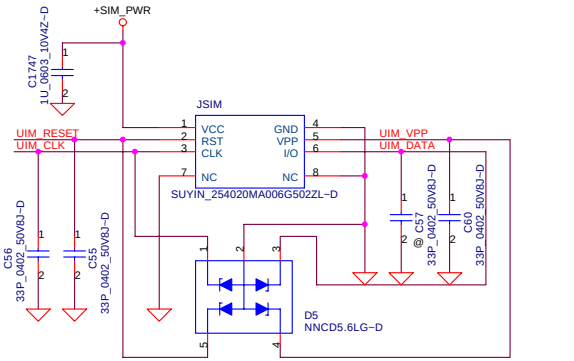


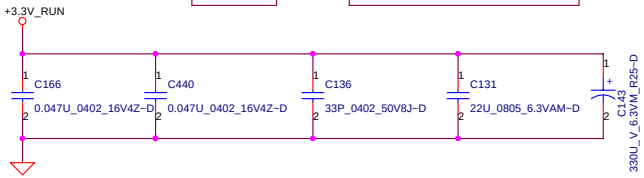


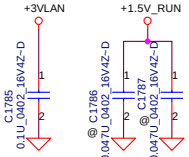
Mini-Card Latch

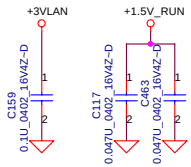
Mini Card
Wire less LAN

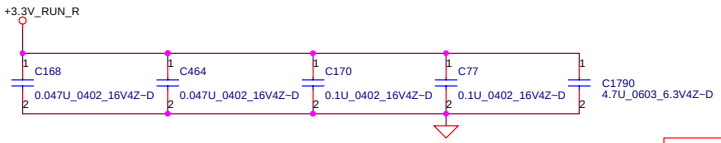












PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

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Title: Mini Card

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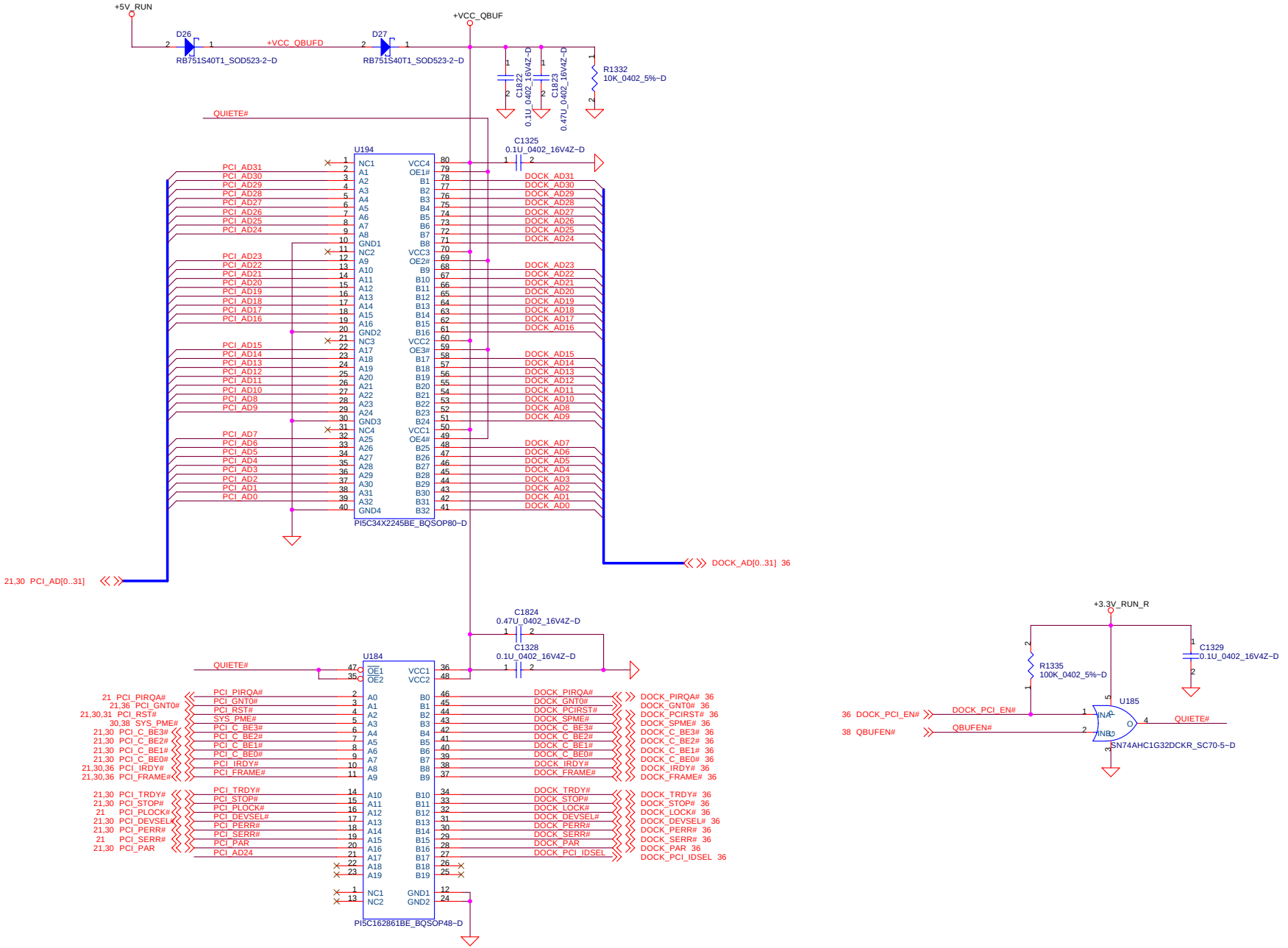

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Title: **DOCKING BUFFER**

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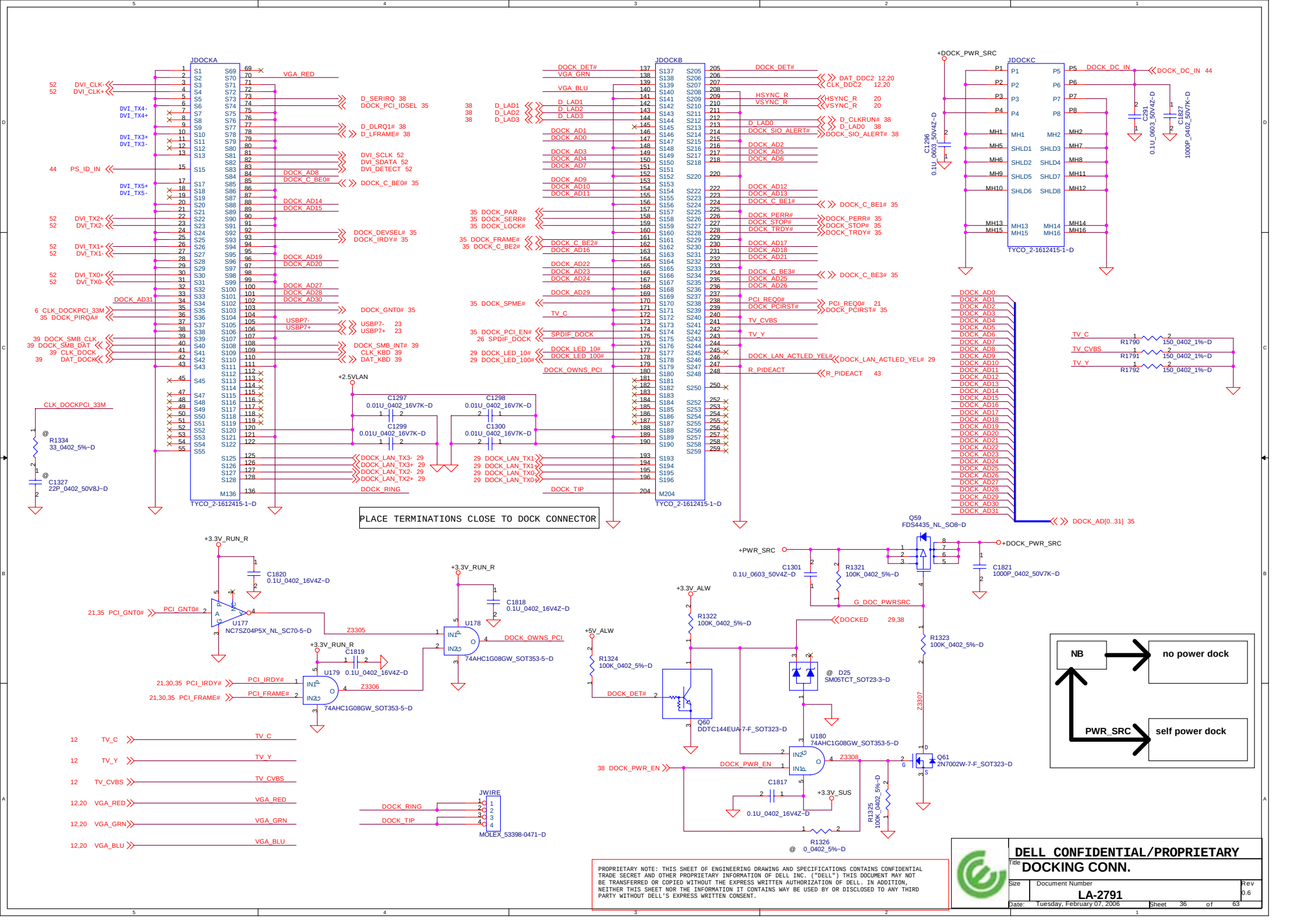
JDOCKA
JDOCKB
JDOCKC
TYCO_2-1612415-1~D
PLACE TERMINATIONS CLOSE TO DOCK CONNECTOR
+2.5VLAN
+3.3V_RUN_R
+3.3V_ALW
+5V_ALW
+DOCK_PWR_SRC
+PWR_SRC
U177 NC7SZ04P5X_NL_SC70-5~D
U178 74AHC1G08GW_SOT353-5~D
U179 74AHC1G08GW_SOT353-5~D
U180 74AHC1G08GW_SOT353-5~D
Q59 FDS4435_NL_SO8~D
Q60 DDTC144EUA-7-F_SOT323~D
Q61 2N7002W-7-F_SOT323~D
@ D25 SM05TCT_SOT23-3~D
JWIRE
MOLEX_53398-0471~D
NB
no power dock
PWR_SRC
self power dock
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Title DOCKING CONN.
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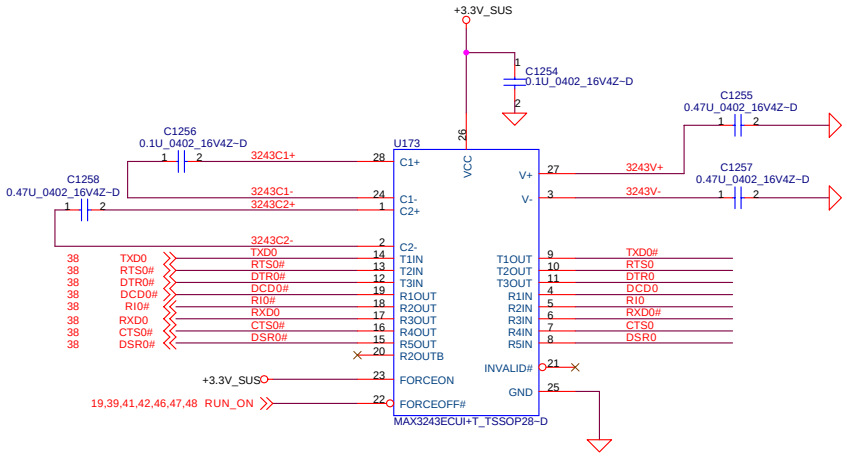

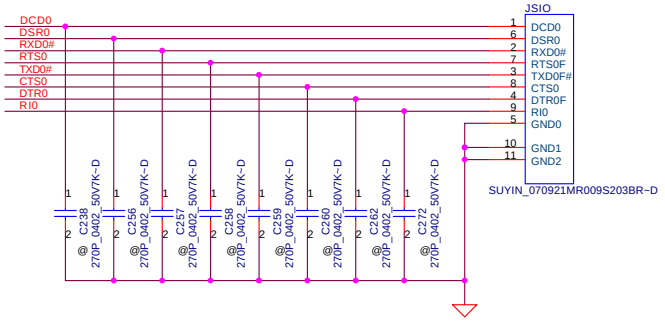

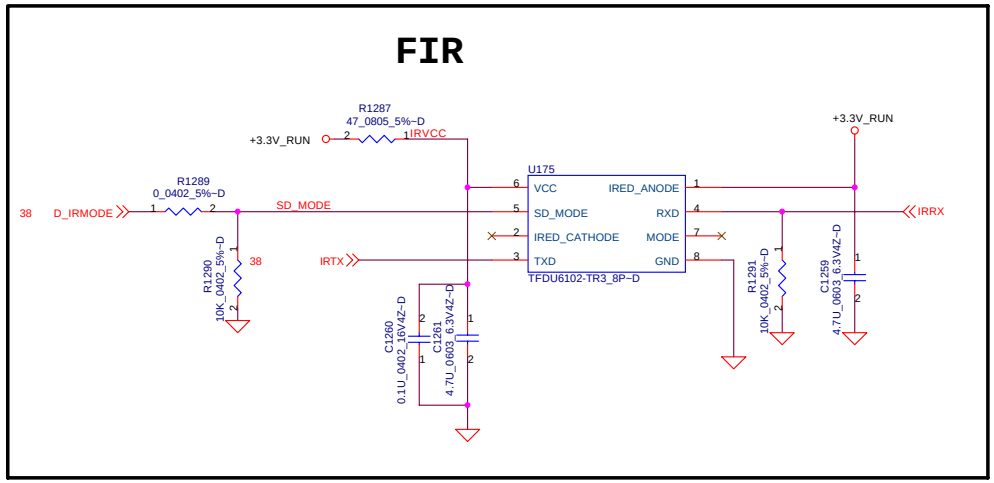

Compal Electronics, Inc.

Title: Serial & FIR

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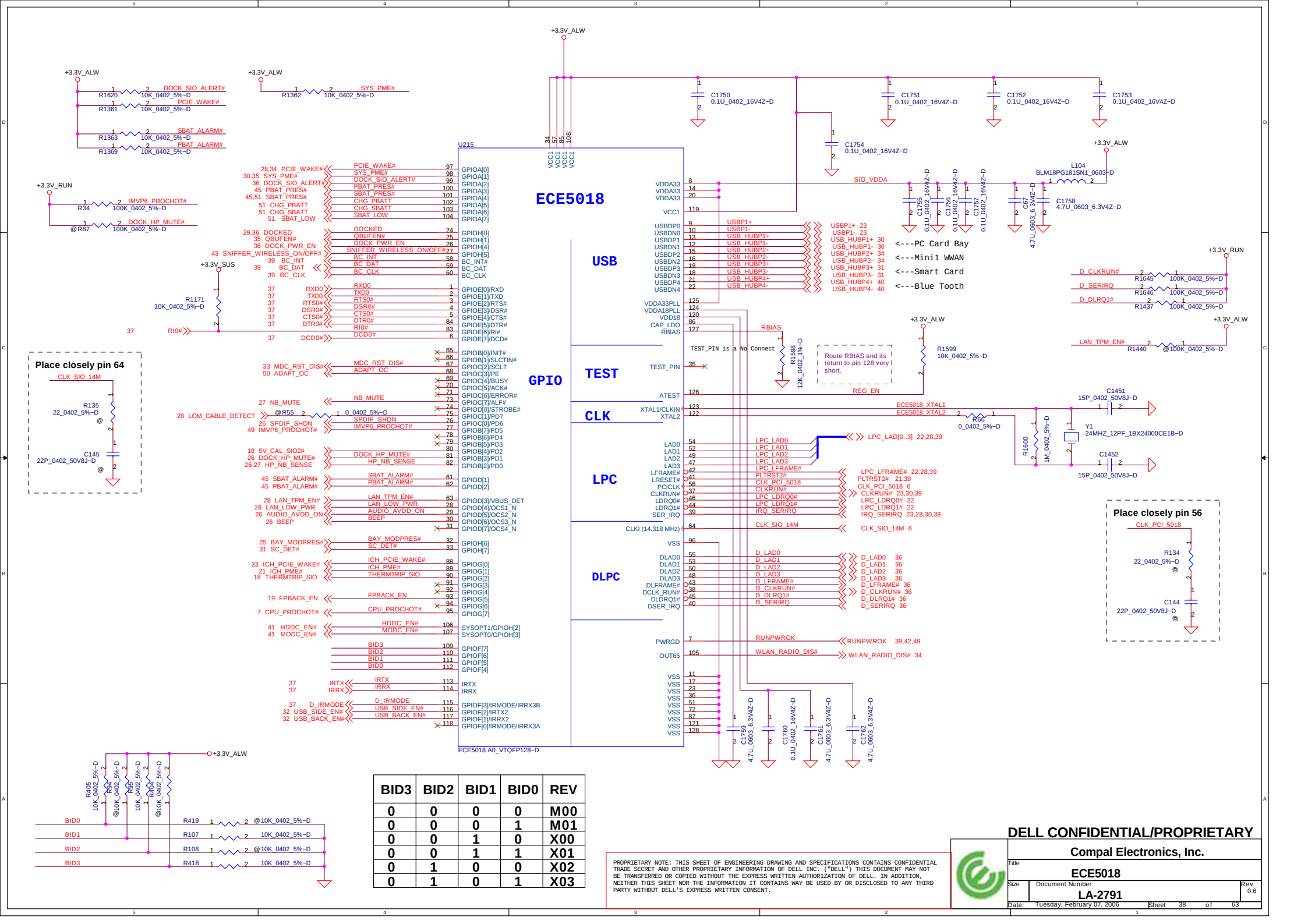
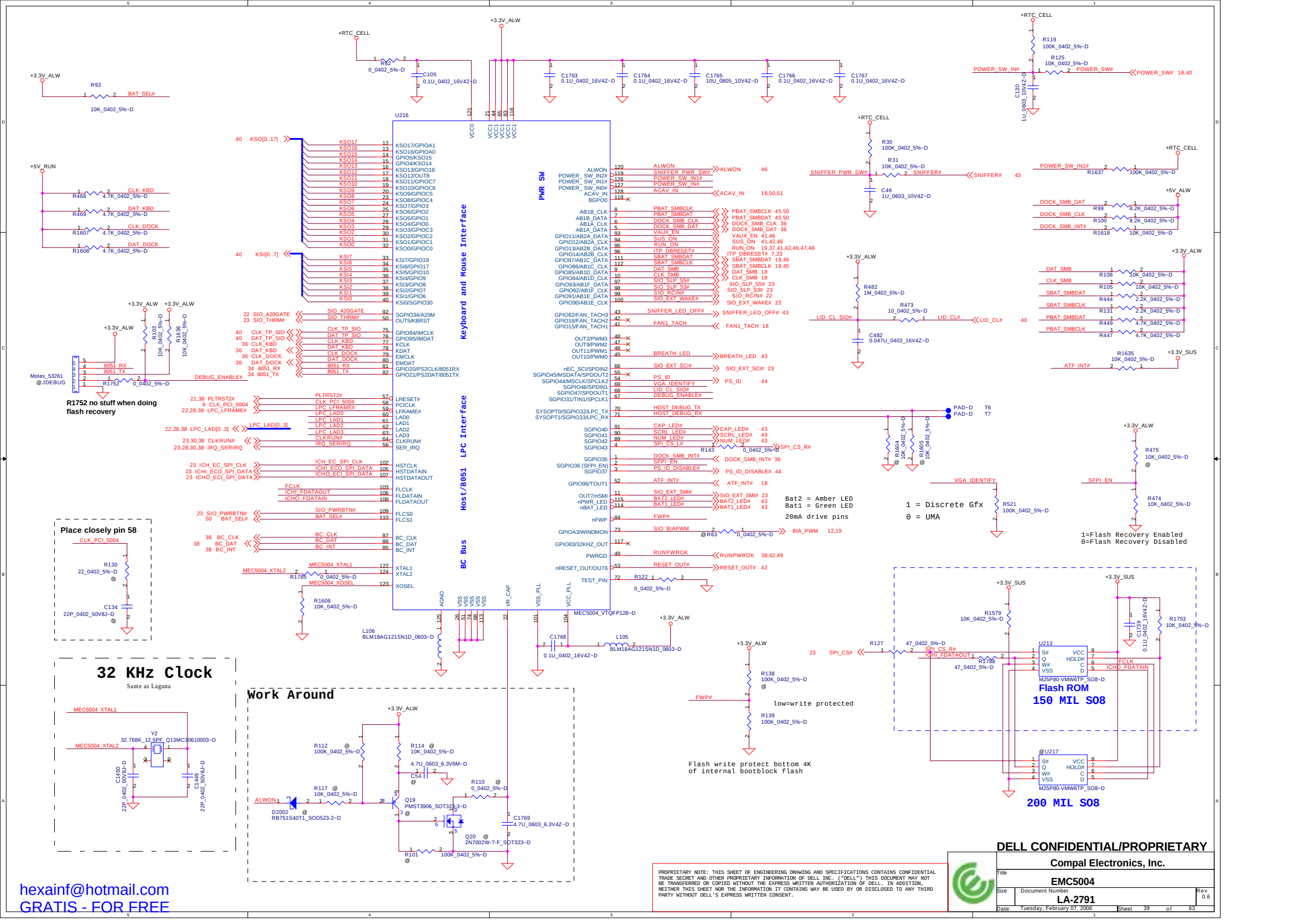


BID3	BID2	BID1	BID0	REV
0	0	0	0	M00
0	0	0	1	M01
0	0	1	0	X00
0	0	1	1	X01
0	1	0	0	X02
0	1	0	1	X03


U216
Keyboard and Mouse Interface
LPC Interface
Host/8051
BC Buss
PWR SW
MEC5004_VTQFP128~D
R1752 no stuff when doing flash recovery
Place closely pin 58
32 KHz Clock
Same as Laguna
Work Around
Bat2 = Amber LED
Bat1 = Green LED
20mA drive pins
1 = Discrete Gfx
0 = UMA
1=Flash Recovery Enabled
0=Flash Recovery Disabled
low=write protected
Flash write protect bottom 4K
of internal bootblock flash
Flash ROM
150 MIL SO8
200 MIL SO8
M25P80-VMW6TP_SO8~D
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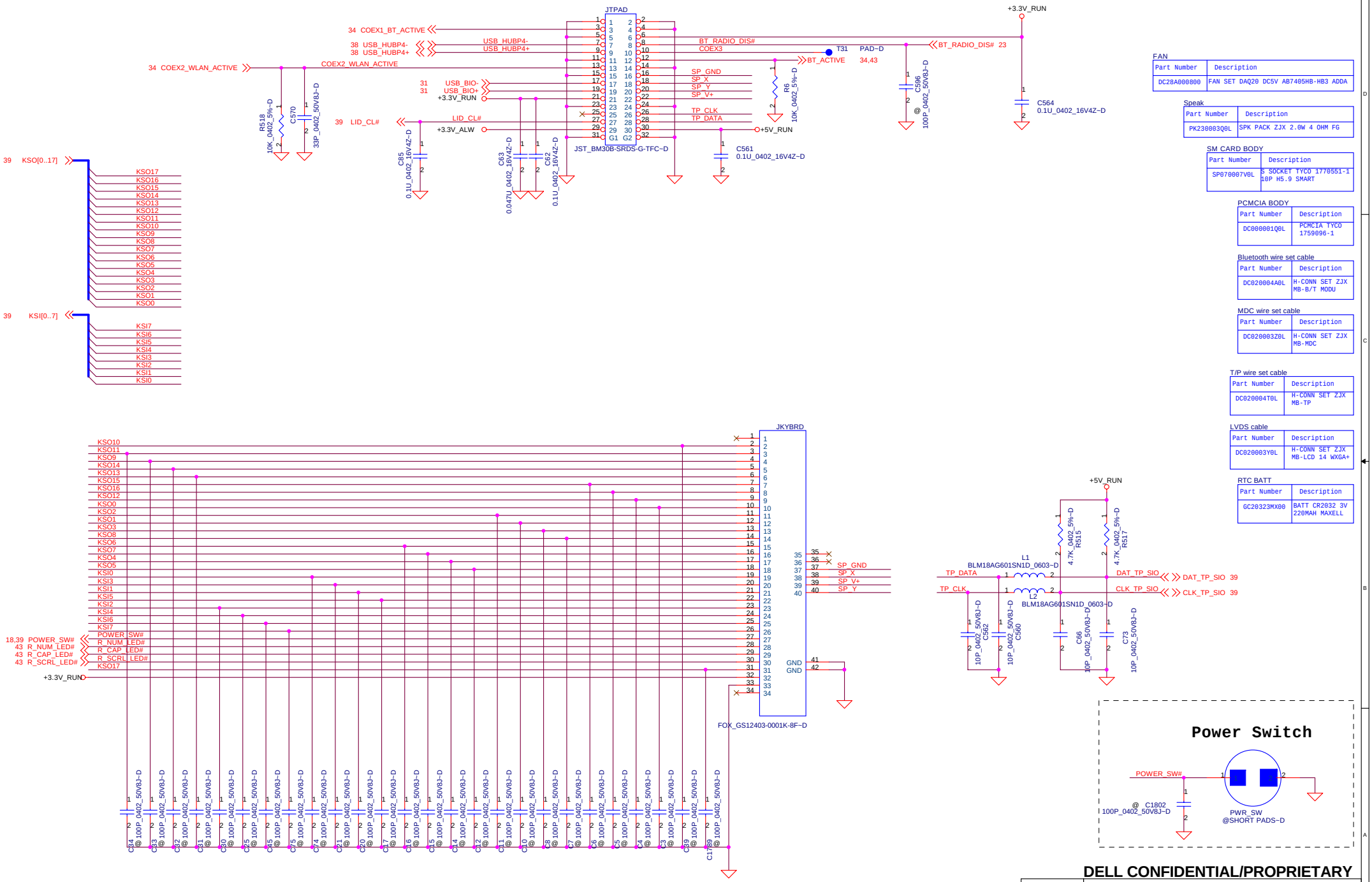
EMC5004
LA-2791
Tuesday, February 07, 2006
hexainf@hotmail.com
GRATIS - FOR FREE

Touch PAD



FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

SM CARD BODY

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

PCMCIA BODY

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

Bluetooth wire set cable

Part Number	Description
DC020004A0L	H-CONN SET ZJX MB-B/T MODU

MDC wire set cable

Part Number	Description
DC020003Z0L	H-CONN SET ZJX MB-MDC

T/P wire set cable

Part Number	Description
DC020004T0L	H-CONN SET ZJX MB-TP

LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+

RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

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Title: INT KB

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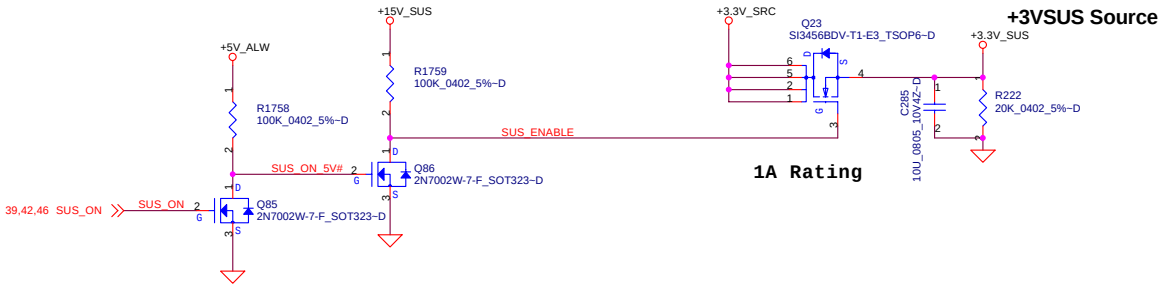
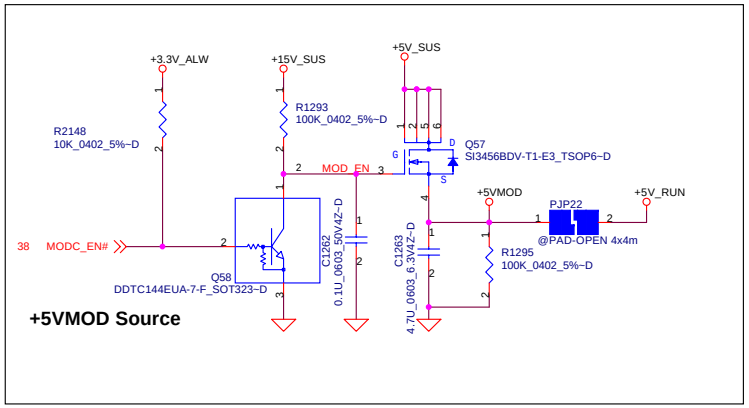
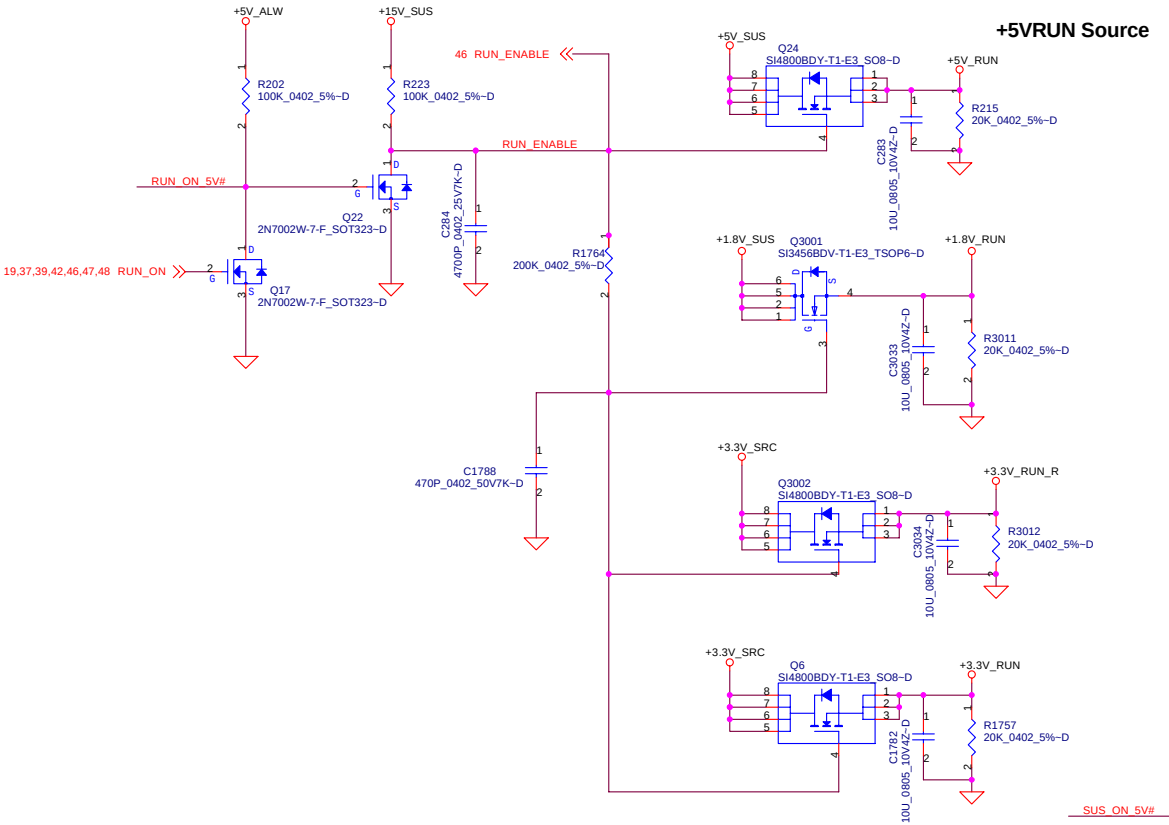
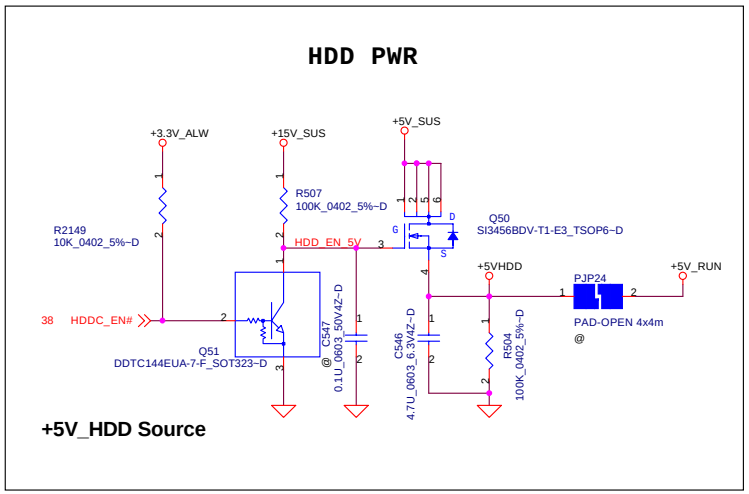
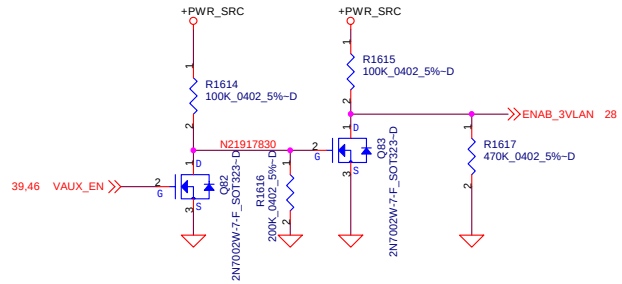
DC/DC Interface



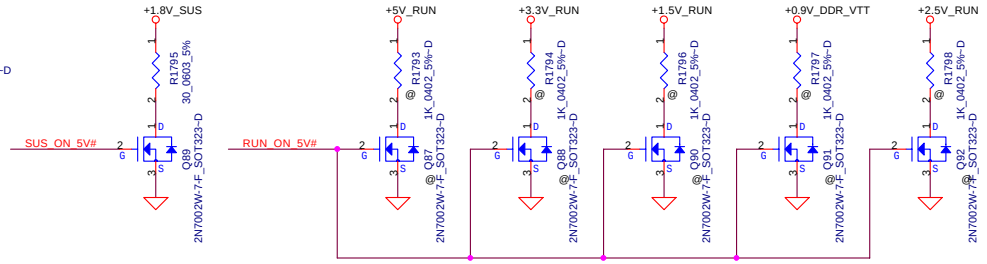








Discharg Circuit



Compal Electronics, Inc.

Title: POWER CONTROL

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For EMI

+3.3V_RUN_R — @C1806 — +3.3V_SRC : 0.047U_0402_16V4Z-D
+3.3V_RUN_R — @C1810 — +SDC_IN : 0.047U_0402_25V4Z-D
+3.3V_SRC — @C1814 — +SDC_IN : 0.047U_0402_25V4Z-D
+1.5V_RUN — @C1807 — +3.3V_SRC : 0.047U_0402_16V4Z-D
+5V_SUS — @ C1811 — +SDC_IN : 0.047U_0402_25V4Z-D
+3.3V_SRC — @C1815 — +1.8V_SUS : 0.047U_0402_25V4Z-D
+1.8V_SUS — @C1808 — +3.3V_SRC : 0.047U_0402_16V4Z-D
+3.3V_SRC — @ C1812 — +SDC_IN : 0.047U_0402_25V4Z-D
+3.3V_RUN — @ C1809 — +3.3V_SRC : 0.047U_0402_16V4Z-D
+3.3V_SRC — @C1813 — +1.5V_RUN : 0.047U_0402_16V4Z-D

+3.3V_RUN
R494 20K_0402_5%-D
3VRUNRC
C520 0.01U_0402_16V7K-D
+3.3V_SUS C483 0.1U_0402_16V4Z-D
U24A 74LVC3G14DC_VSSOP8-D
U24B 74LVC3G14DC_VSSOP8-D
+3.3V_SUS C480 0.1U_0402_16V4Z-D
U26A 74VHC08MTCX_NL_TSSOP14-D

R49 0_0402_5%-D
R313 0_0402_5%-D
R319 0_0402_5%-D
R334 0_0402_5%-D
18 2.5V_RUN_PWRGD
47 1.5V_RUN_PWRGD
47 1.05V_RUN_PWRGD
48 0.9V_DDR_PWRGD

19,37,39,41,46,47,48 RUN_ON
+3.3V_SUS
U26D 74VHC08MTCX_NL_TSSOP14-D
RUNPWROK
RUNPWROK 38,39,49

48 SUSPWROK_1P8V
+3.3V_ALW
R1383 100K_0402_5%-D
R1386 10K_0402_5%-D
C1816 0.1U_0402_16V4Z-D
Q7 2N7002W-7-F_SOT323-D
39,41,46 SUS_ON
U24C 74LVC3G14DC_VSSOP8-D
U26C 74VHC08MTCX_NL_TSSOP14-D
SUSPWROK 18,23

23,49 IMVP_PWRGD
39 RESET_OUT#
IMVP_PWRGD
RESET_OUT#
U26B 74VHC08MTCX_NL_TSSOP14-D
R463 0_0402_5%-D
ICH_PWRGD 10,23

R453 100K_0402_5%-D
ICH_PWRGD#
ICH_PWRGD# 18
ICH_PWRGD
Q41 2N7002W-7-F_SOT323-D

COIN RTC Battery

+COINCELL
R471 1K_0402_5%-D
+3.3VX
Z4012
D15 BAT54CW_SOT323-D
+RTC_CELL
C528 1U_0603_10V4Z-D
COINCELL
JCOIN MOLEX_53398-0271-D

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Compal Electronics, Inc.

Title: Power Good
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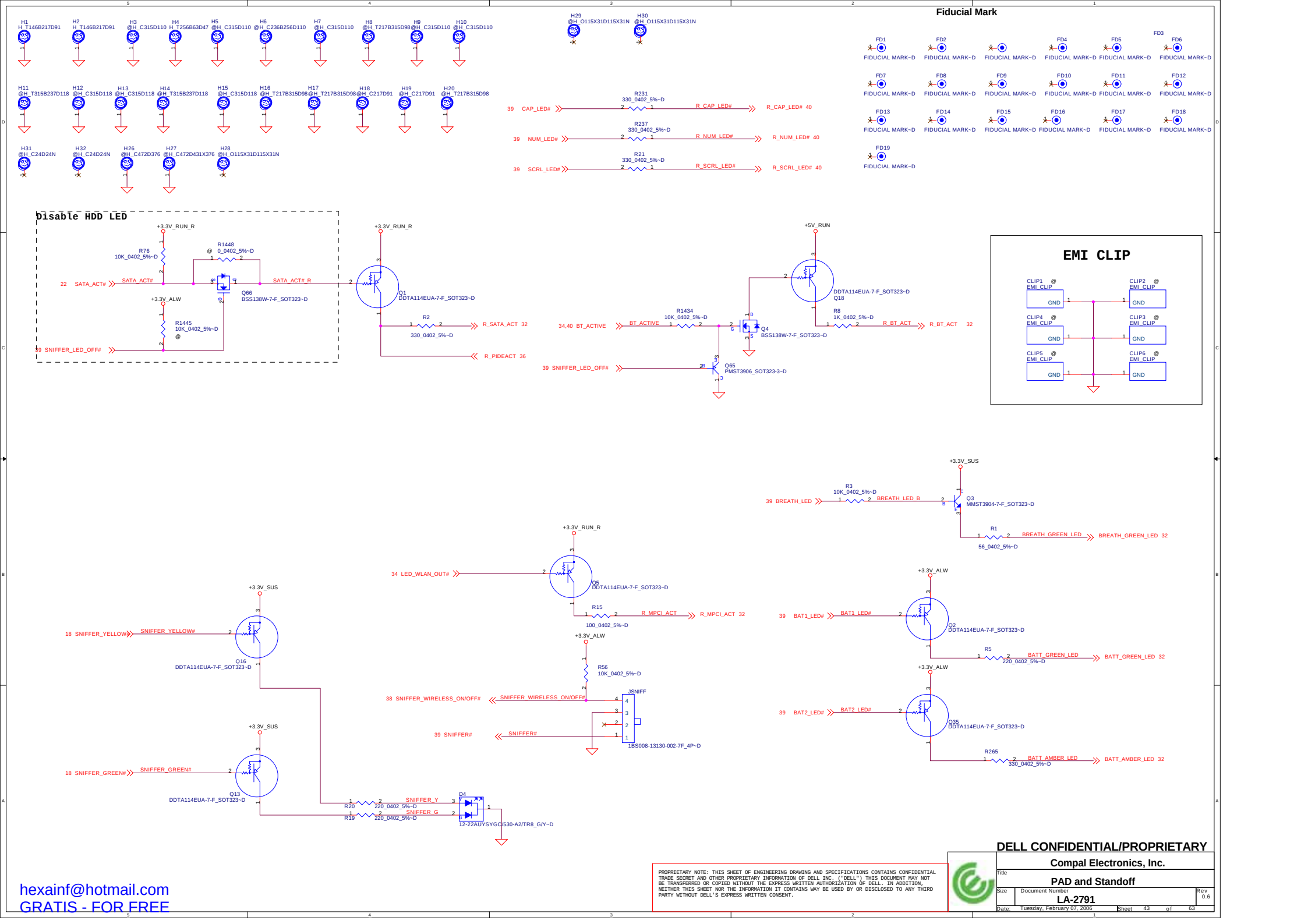

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Compal Electronics, Inc.

Title: PAD and Standoff

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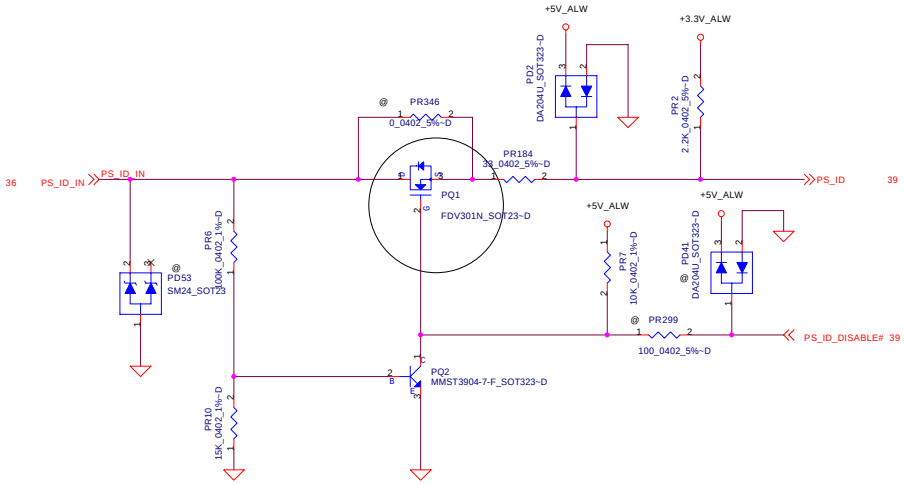

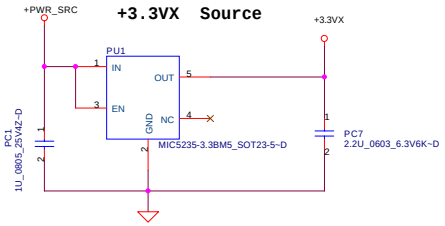

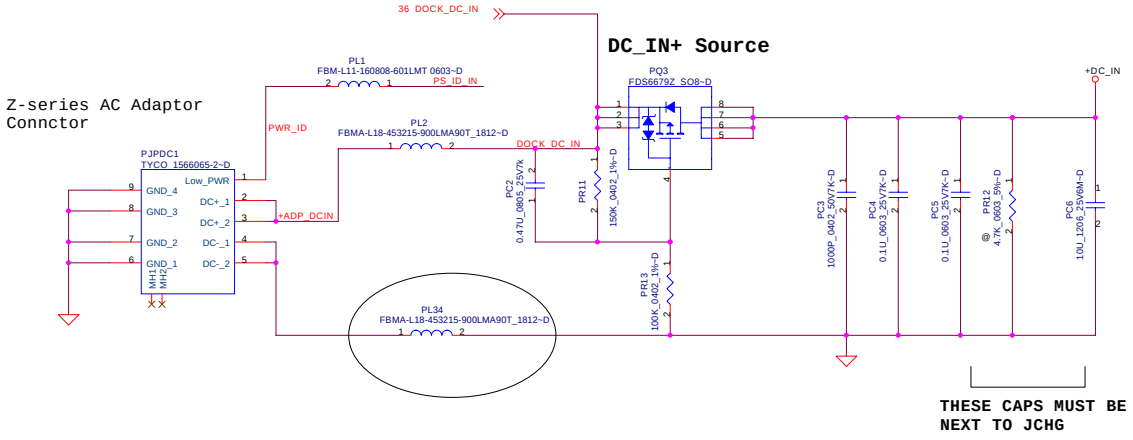

Compal Electronics, Inc.

Title: +DCIN

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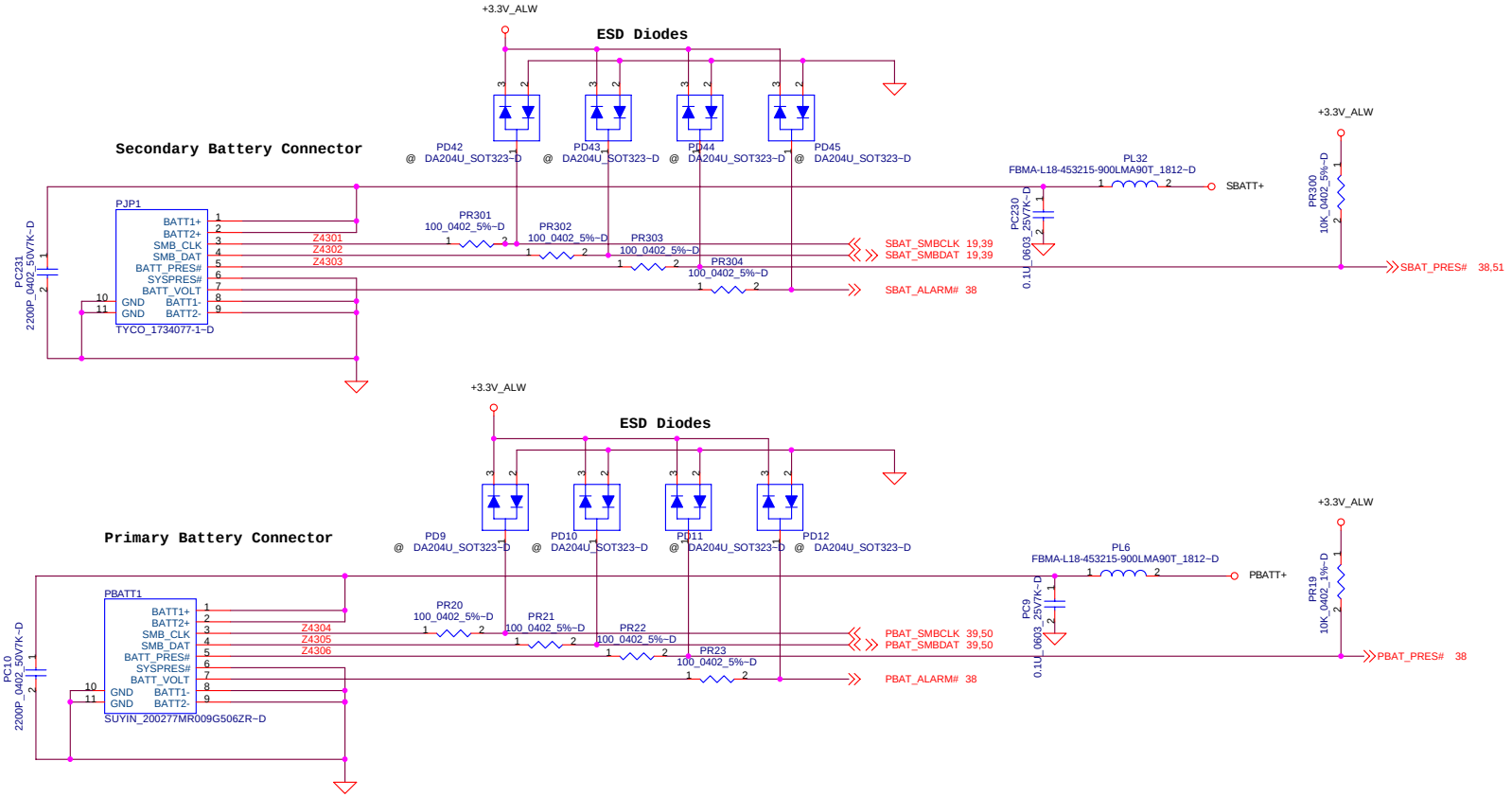

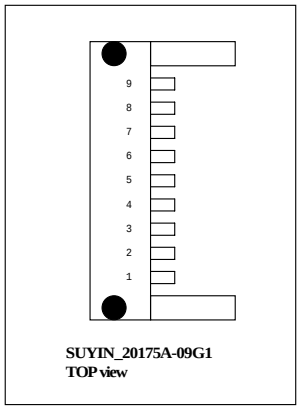

Compal Electronics, Inc.

Title: Battery Conn.

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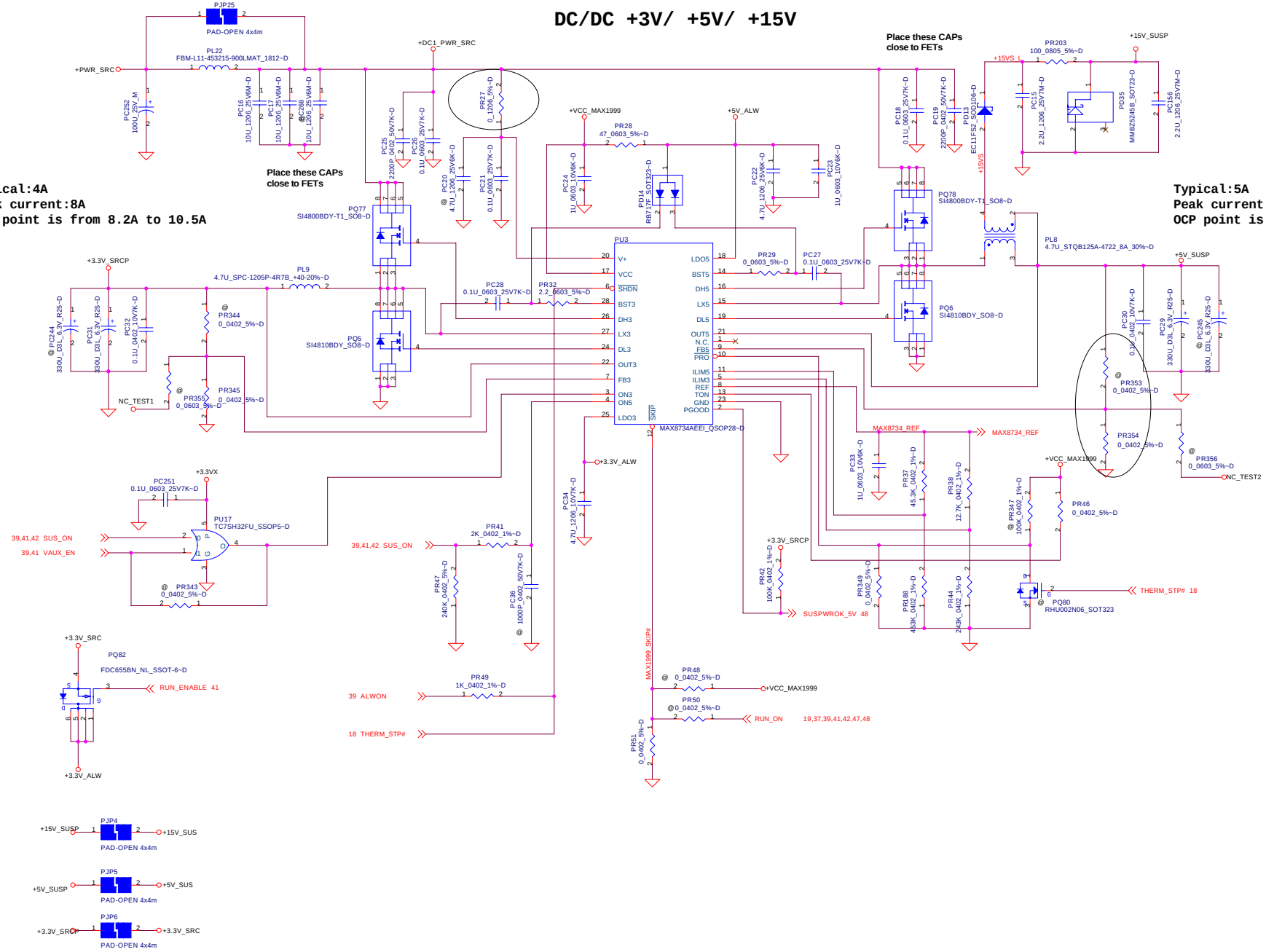
DC/DC +3V/ +5V/ +15V

Typical:4A
Peak current:8A
OCP point is from 8.2A to 10.5A

Typical:5A
Peak current:7A
OCP point is from 8A to 11.2A

Place these CAPs close to FETs

Place these CAPs close to FETs



Compal Electronics, Inc.

Title: +3.3V/+5V/+15V

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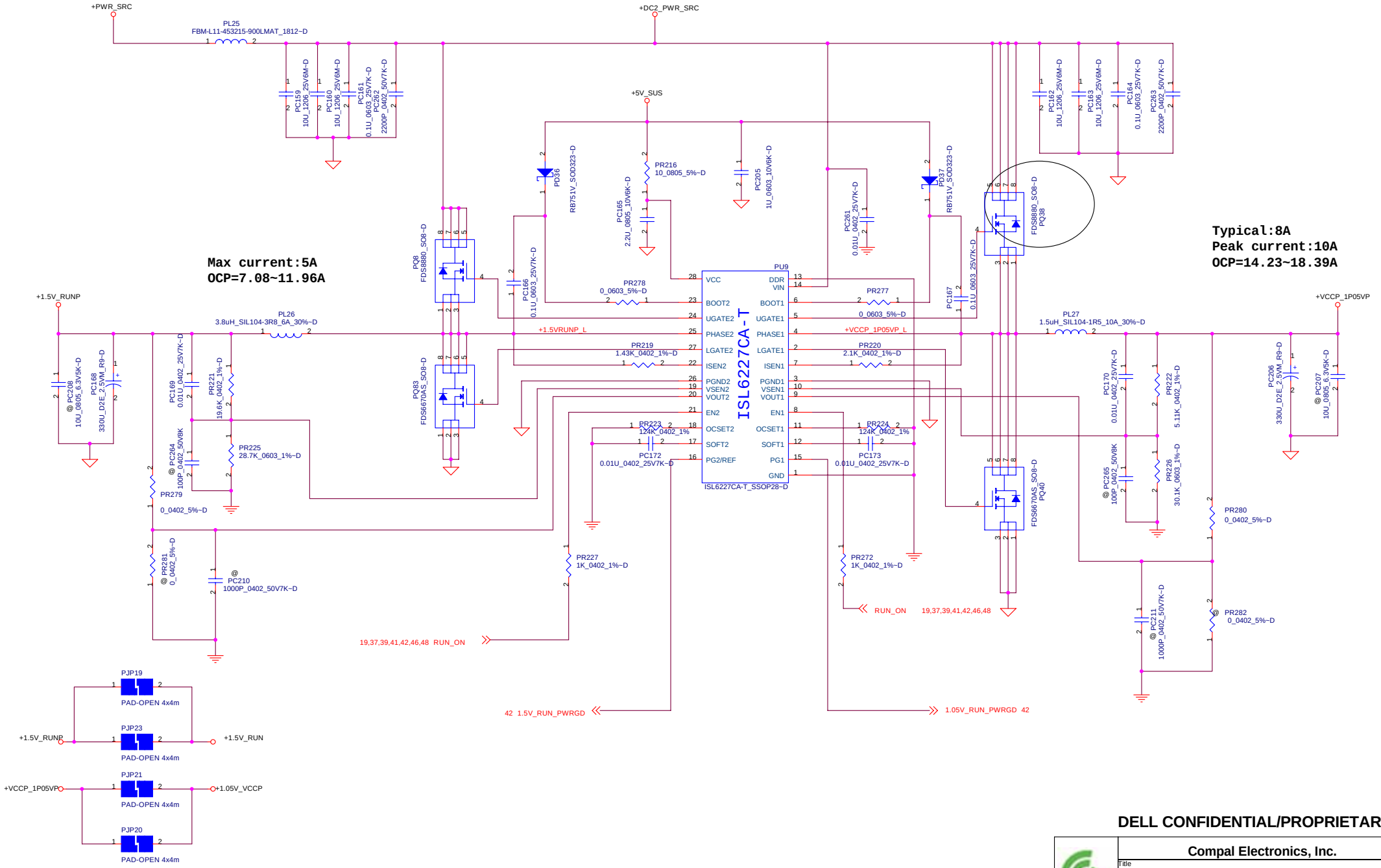
+1.5VRUNP / +VCCP_1P05VP



Compal Electronics, Inc.

Title: +1.5VSUSP /+VCCP_1P05VP

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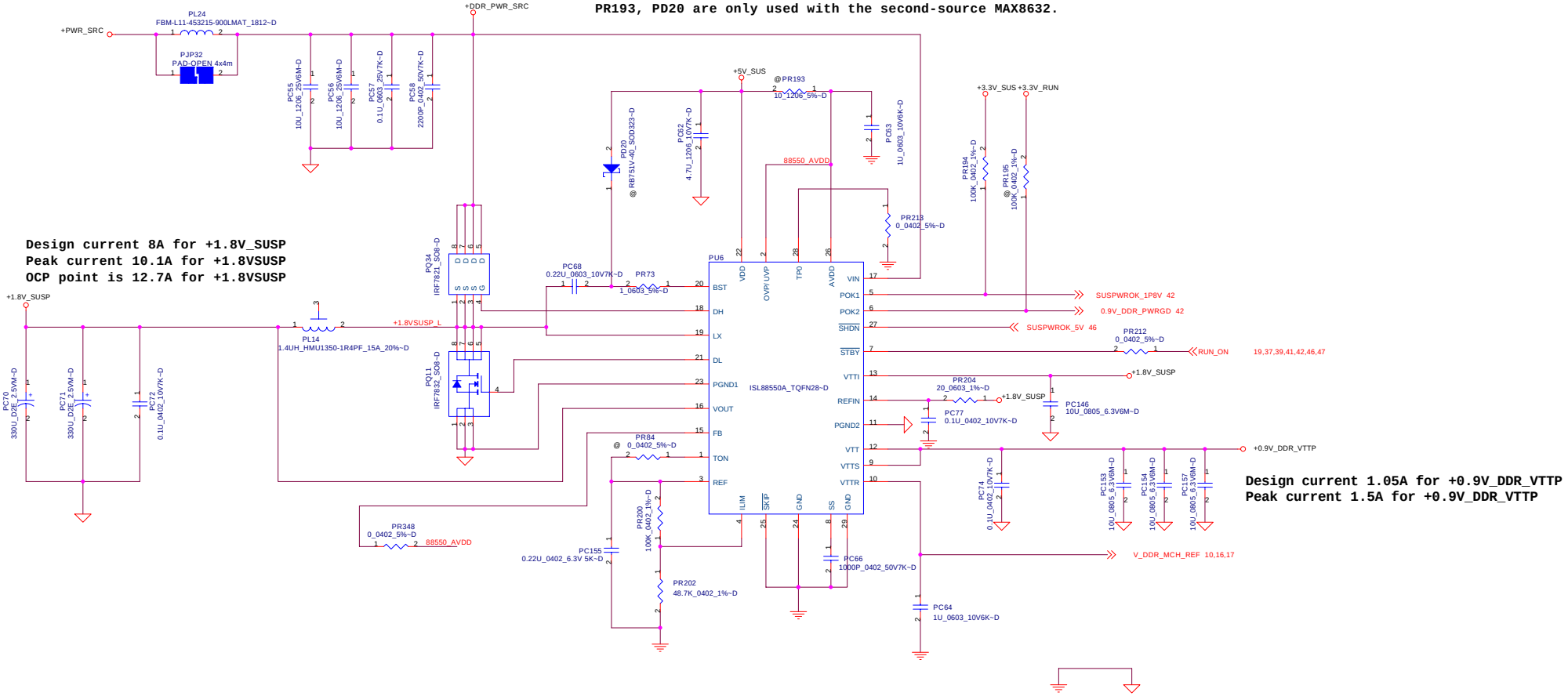
+1.8VSUSP/ +0.9V_DDR_VTT

DDR2 Termination

PR193, PD20 are only used with the second-source MAX8632.



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Compal Electronics, Inc.		
Title	+1.8VSUSP/ +0.9V_DDR_VT	
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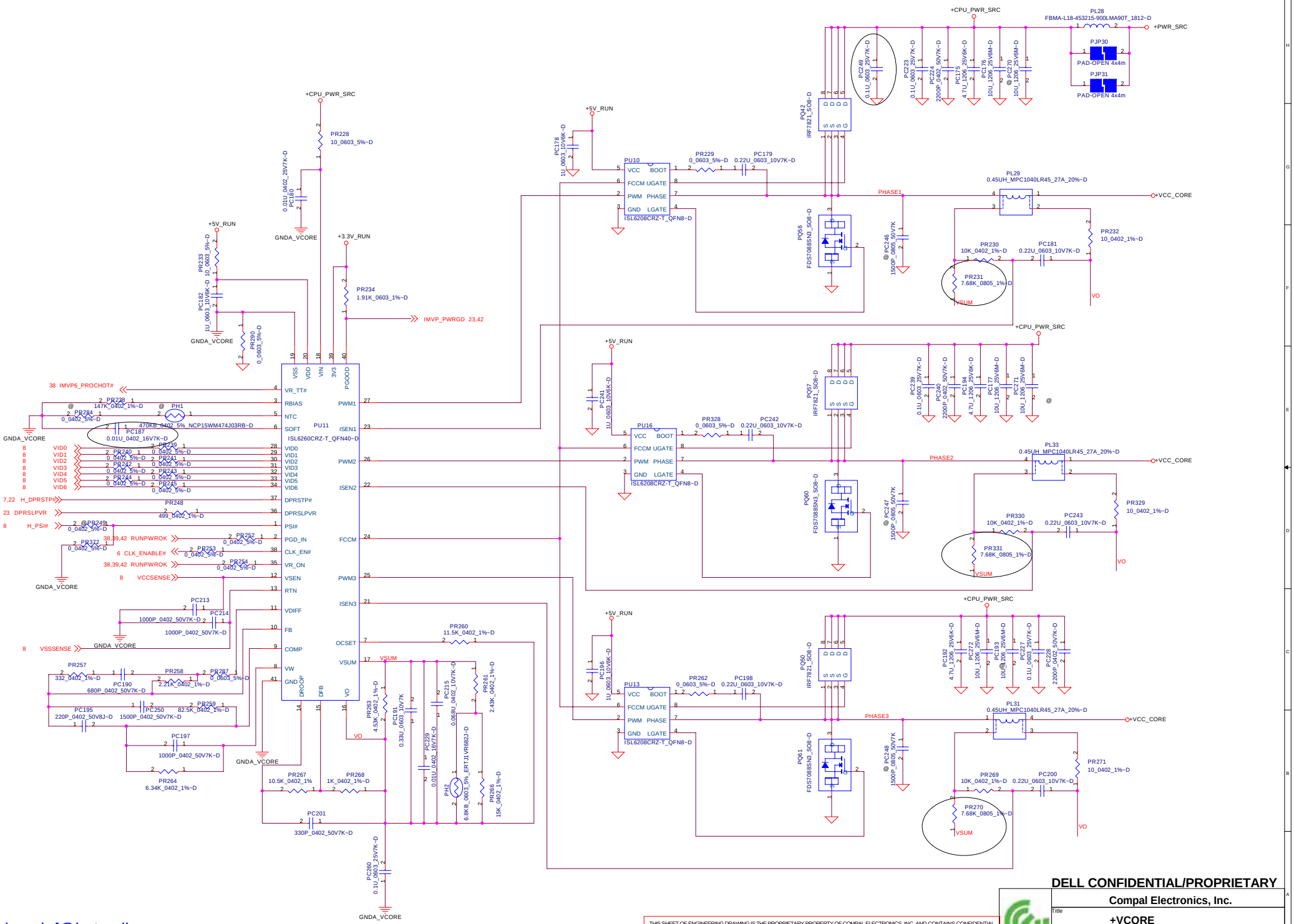

Compal Electronics, Inc.

Title: +VCORE

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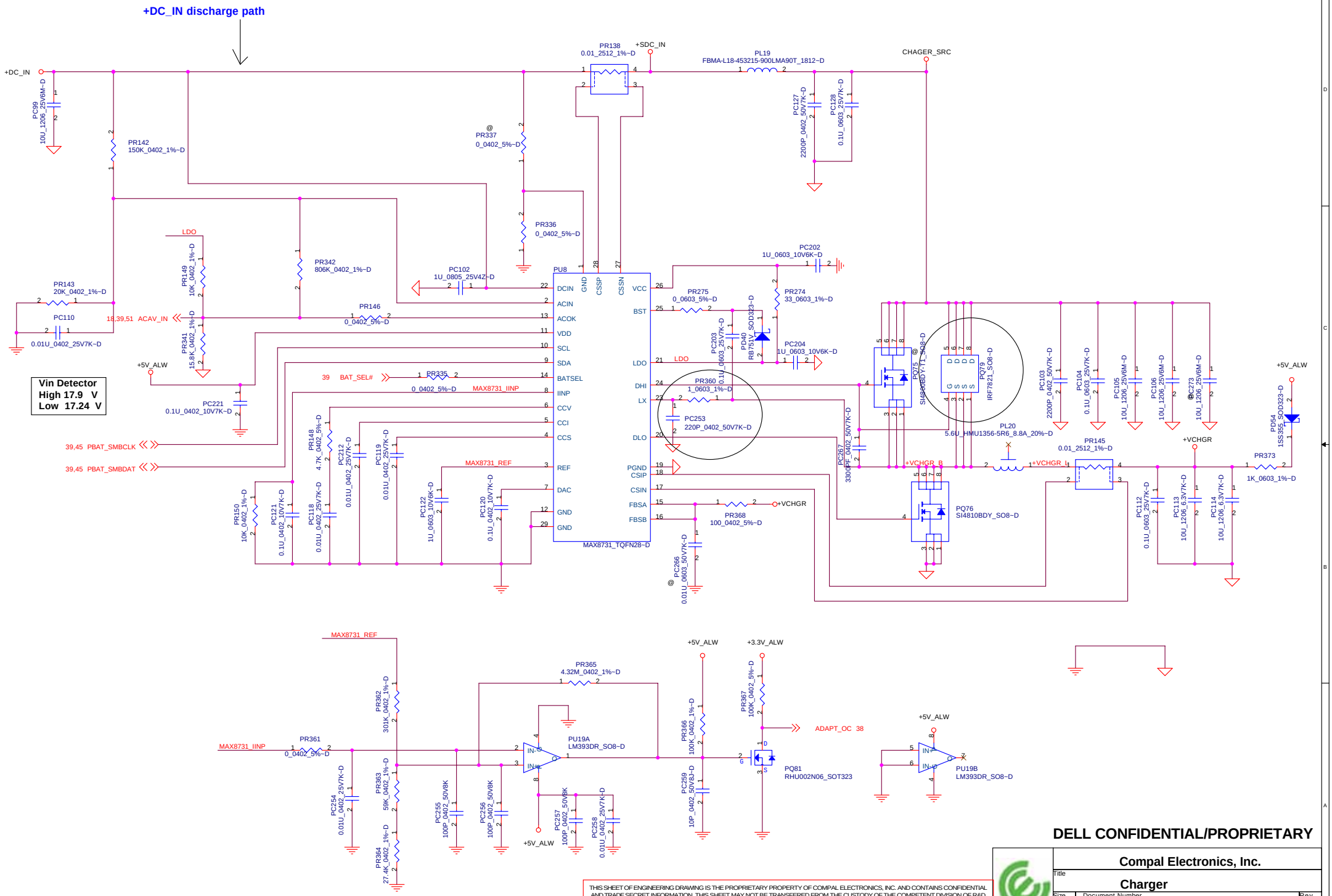

Compal Electronics, Inc.

Title: Charger

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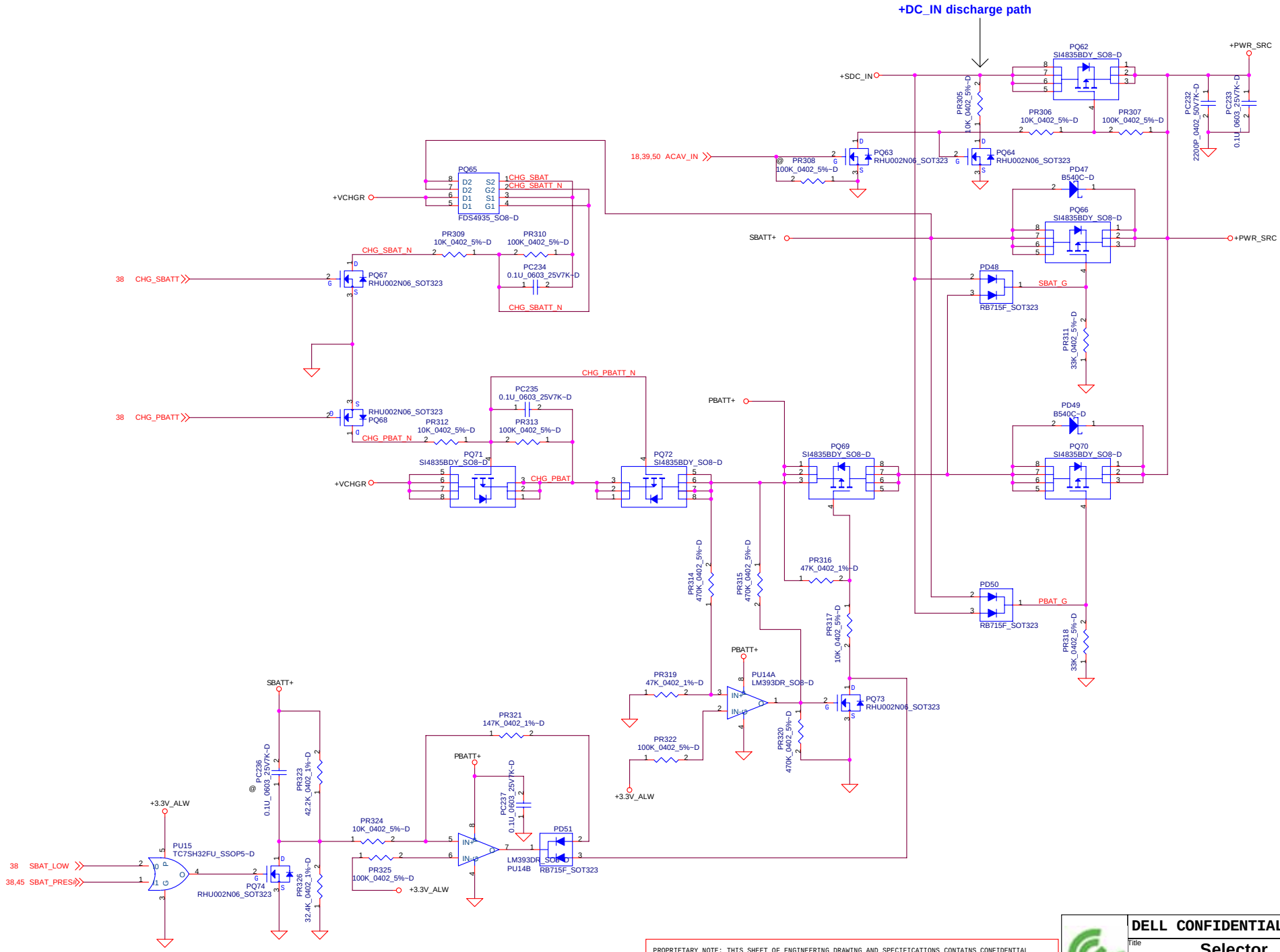

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Title: **Selector**

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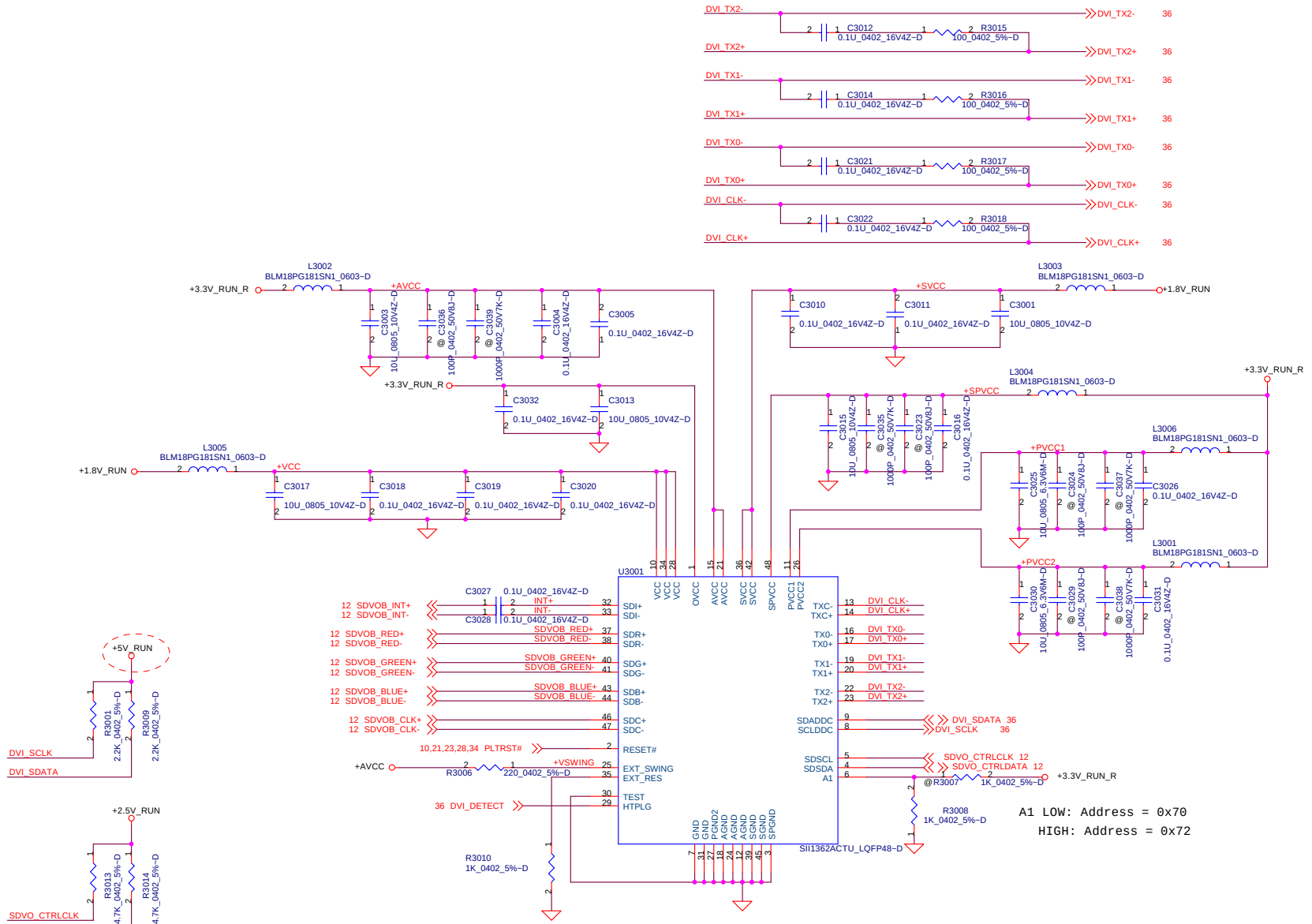

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Compal Electronics, Inc.		
Title: Internal LVDS		
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31	H/W	05/27	Roger	Smart card pin definition not match the cage pin define	Change JSC pin connection, pin1 connect to GND, pin2 connect to SC_DET# ~ pin10 connect to +SC_PWR	0.2
2	12,36	H/W	05/27	Roger	Fix TV out issue	Depop R23,R24,R25. And add R1790,R1791,R1792 75 ohms	0.2
3	40	H/W	05/27	Roger	Remove power switch to save placement spacing	Remove SW1. Reseve R1793 pad for power switch	0.2
4	20	H/W	05/27	Roger	Docking CRT HSYNC, VSYNC connect to the out put side of buffer	DOCK_HSYNC connect from U190 pin4 to docking connector pin 209, DOCK_VSYNC connect from U191 pin4 to docking connector pin 210	0.2
5	32	H/W	05/27	Roger	Improve RJ45 center tap driving	Connect +2.5VLAN to JIO pin 14 for RJ45 center tap	0.2
6	39	H/W	05/27	Roger	SPI ROM pass through mode connect error	Change FDATAIN to ICHO_FDATAIN and connect from U216 pin 106 to U213 pin5. Chagne FDATAOUT to ICHI_FDATAOUT and connect from U216 pin 108 to R1788 pin1	0.2
7	39	H/W	05/27	Roger	Flash Recovery strapping issue	Change R474, R475 from 100K to 10K	0.2
8	ALL	H/W	05/30	Brike	To fix MEC5004 VCC1 power lading	Change net from +3VALW to +3VSRC	0.2
9	43	H/W	05/30	Brike	None	Delete H21 and change H4 footprint from H_C176D122to H_C176D102	0.2
10	39	H/W	06/01	Will	For delay MEC5004 internal 1.8V reg.	Modified C1769 from 4.7UF to 22UF.	0.2
11	23	H/W	06/01	Will	To improve rise time of serial DO from SPI ROM.	Modified R389 from 10K to 1K..	0.2
12	41	H/W	06/01	Will	None	Add pullup to HDDC_EN# and MODC_EN#.	0.2
13	36	H/W	06/01	Will	Fix Docking TV out issue.	Modified R1790,R1791,R1792 from 75 ohms to 150Ohm.	0.2
14	39	H/W	06/01	Will	None	Change power on SPI ROM (pins 3 and 8) from +3VALW to +3VSUS.	0.2
15	38	H/W	06/01	Will	For GPIO control.	Use ECE5018 GPIOC2 (pin 67), pin name MDC_RST_DIS#. Reserve this pin for MDC disable circuit.	0.2
16	12	H/W	06/01	Lester	None	Remove R34, R242, R37, R247, Q7, and Q33 to connect LDDC_CLK, LDDC_DATA directly to LVDS connector.	0.2
17	13	H/W	06/01	Lester	Intel Checklist recommends a 1 nH ferrite which calculates to 200 ohm.	Change L34 to BLM18PG181SN1_0603.	0.2
18	06	H/W	06/01	Lester	Add resistor for cystal drive current limiting	Add R32 0 ohm resistor	0.2
19	39	H/W	06/01	Will	Correct SPI connection for SMSC recommand	ICH7M.P5 connect to MEC 5004.107, MEC5004.108 connect to SPI ROM.5. ICH7M.P2 connect to MEC 5004.105, MEC5004.106 connect to SPI ROM.2	0.2
20	38	H/W	06/02	Roger	SMSC recommond add VBUS_DET pull up resistor	Add R1440 100K for LAN_TPM_EN# (VBUS_DET)	0.2
21	33	H/W	06/02	Roger	Add MDC disable circuit	Add R1441, R1442, R1443, Q64. ECE5018 pin 67 program MDC_RST_DIS#	0.2
22	34	H/W	06/06	Roger	None	Change U8 NNCD6.8RL-A to D5 NNCD5.6LG	0.2
23	3	H/W	06/06	Roger	None	Fixed USB table	0.2
24	3	H/W	06/13	Roger	None	Add PJP22, PJP24 for +5VMOD and +5VHDD. Delete R506	0.3

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Title: Changed-List History 1

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	13	H/W	06/14	Roger	Follow Intel CRB	D14 pin2 connect to +VCCP, pin1 connect to R320 pin1, R320 pin2 connect to +2.5VRUN. D18 pin2 connect to +1.5VRUN, pin2 connect to R12 pin1, R12 pin2 connect to +3VRUN_R	0.3
26	27	H/W	06/14	Roger	U10 (STAC9200) pin21 (GPIO0) is anlog power plane	Change R156 pull up from +3VSUS to +VDDA	0.3
27	7	H/W	06/14	Roger	Change ITP debug to XDP debug definition for Yonah CPU	Change R387, R417, R391, R436, R416, R415 to 56 ohms. Add R33 56 ohms. Change R424 to 1K ohms.	0.3
28	39	H/W	06/14	Roger	For easier flash EC code	Add short pad and change R475 to 1K ohms	0.3
29	40	H/W	06/14	Roger	For easier power switch	Change R1793 to a pad like CMOS pad	0.3
30	34	H/W	06/14	Roger	ME change mini card stand off to Latch	Remove H22,H23,H24,H25. Add JCLIP1,JCLIP2	0.3
31	42	H/W	06/14	Roger	EMI reqest add caps for the splite power plane that PCI bus routed	Add C1806,C1807,C1808,C1809,C1810,C1811	0.3
32	41	H/W	06/16	Roger	Reserve discharg circuit for +5VRUN,+3VRUN, +1.8VRUN,+1.5VRUN,+0.9V_DDR_VTT,+2.5VRUN power rails	Add R1793,R1794,R1795,R1796,R1797,R1798,Q87,Q88,Q89,Q90,Q91,Q92	0.3
33	28	H/W	06/21	Gautam	Reserve ST M45PE20 for LOM EEPROM	Add U3 (ST M45PE20) co-layout with U188 (AT45BCM021B)	0.3
34	42	H/W	06/23	Gary	EMI reqest add caps for the splite power plane that PCI bus routed	Add C1812~C1814 0.047uF_0402. Change C1810~C1813 from 0603 to 0402 package	0.3
35	38	H/W	06/23	Roger	+3VRUN leakage at AC mode in S5	Change R1362 pull up from +3VSRC to +3VRUN	0.3
36	All	H/W	06/24	Roger	Follow Dell USB assignment recommendation	Update USB table, block diagram and connection	0.3
37	39	H/W	06/24	Will	4.7uF cap for VR_Cap pin of REV B 5504	Change C1769 for 22uF 0805 size to 4.7uF 0603 size	0.3
38	All	H/W	06/24	Joey	Change +3V/+5V design to follow Dell recommendation	Change +3VSRC to +3VALW except for LOM	0.3
39	28	H/W	06/24	Gautam	IEEE testing the voltage level are closer to the higher end of IEEE range	Change R1364 from 1.15K to 1.18K_0402_1%	0.3
40	7	H/W	06/24	Lester	Required by Intel for B0 Yonah.	Add R1378 (51_0603_1%) for TEST2 pulldown	0.3
41	39	H/W	06/24	Lester	Required by Intel for B0 Yonah.	Populate R1752 and add note "No stuff when doing flash recovery"	0.3
42	33	H/W	06/28	Rossana	MDC signal by pass caps not require	Delete C93, C82, C73	0.3
43	31,40	H/W	06/28	Rossana	Reseved USB port of OZ77C6 for Biometrics reader	Change JTPAD from 10 pins to 20 pins. Add USB_BIO+/- on U1 pin18,19 connect to JTPAD pin9,11	0.3
44	30	H/W	06/28	Rossana	Request by Dell	Remove C1783, C1784	0.3
45	34	H/W	06/28	Rossana	Request by Dell	Remove L18, R149, and R144 - direct connect USB to Wireless LAN card	0.3
46	34	H/W	06/28	Rossana	Request by Dell	Add R1603 connect to JMINI2 pin46, outgoing signal BT_ACTIVE	0.3
47	34	H/W	06/28	Rossana	Gerber Gate List issue	Add series 0-ohms R1609, R1610 for pins 3 and 5 of JMINI2	0.3

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
48	34	H/W	06/28	Rossana	Gerber Gate List issue	Change C159 and C1785 from 10uF to 0.1uF	0.3
49	34	H/W	06/28	Rossana	Gerber Gate List issue	Add T1 test point for JMINI1 pin 42	0.3
50	36	H/W	06/28	Rossana	Gerber Gate List issue	Add C1817~1820 for U180,U178,U179,U177	0.3
51	39	H/W	06/28	Rossana	Gerber Gate List issue	Change R30 pull up from +3VSRC to +3VALW	0.3
52	43	H/W	06/28	Rossana	Change sniffer switch type, the active direction swap	WIRELESS_ON/OFF# connection from pin1 to pin 4 of JSNIFF, pin3 connect to GND, pin2 NC, pin 1 connect to SNIFFER#	0.3
53	36	H/W	06/28	Rossana	Gerber Gate List issue	Add C1821 1000pF for +DOCK_PWR_SRC, add C1827 1000pF for DOCK_DC_IN	0.3
54	35	H/W	06/28	Rossana	Gerber Gate List issue	Add C1822 0.1uF_0402 and C1823,C1824 .47uF_0402 for QBUF power	0.3
55	26,27	H/W	06/28	Rossana	Gerber Gate List issue	Follow Dell "Travis_Audio_0628" reference circut design	0.3
56	39	H/W	06/29	Scott	Gerber Gate List issue	Change L4 form MURATA BLM11A121S to BLM18PG181SN1	0.3
57	24	H/W	06/30	Scott	Gerber Gate List issue	Remove C375, C37 for ICH_V5REF_RUN, remove C420 for ICH_V5REF_SUS	0.3
58	24	H/W	06/30	Scott	Gerber Gate List issue	Add R37 0.5 ohm 0603 resistor connect to L42 pin1	0.3
59	24	H/W	06/30	Scott	Gerber Gate List issue	Populate C347 and C442	0.3
60	24	H/W	06/30	Scott	Gerber Gate List issue	Change C450 for 220uF to 330uF poly cap	0.3
61	40	H/W	06/30	Roger	Match Dell JTPAD pinout definition	Match Dell JTPAD pinout definition, add C62, C63 for BIO power rail bypass	0.3
62	26,27	H/W	06/30	Rossana	Gerber Gate List issue	R162 change from 8.2K to 2.2K, remove D33, D34, Change C1800, C1801 from 1uF to 2.2uF, change C534 from 0.1uF to 1uF, del C533.	0.3
63	26	H/W	06/30	Rossana	Gerber Gate List issue	HP_NB_SENSE move from GPIO2 to GPIO0 of U10, add series resistor 0 ohm for this signal	0.3
64	7	H/W	07/07	Roger	Support A1 Yanah CPU	De-pop R513, R514 for A1 yanah CPU	0.3
65	7	H/W	08/01	Roger	Gerber Gate List issue item 6	Change Change R417 to 150 ohm, R415 to 51 ohm, R387 to 39.2 ohm, R436 to 27.4 ohm, R391 to 680 ohm, R424 to 22.6 ohm	0.4
66	38	H/W	08/01	Roger	Gerber Gate List issue item 8	Change R110 from 68 ohm to 75 ohm for H_PROCHOT# pull up	0.4
67	43	H/W	08/01	Roger	Gerber Gate List issue item 9	Change the voltage rail on sniffer LED pull-ups (at Q13 and Q16) from +3VALW to +3VSUS	0.4
68	7	H/W	08/01	Roger	None	Remove unnecessary capacitor C1805	0.4
69	40	H/W	08/01	Roger	Hall switch design on touch pad moudle	Depop U46 and C54	0.4
70	38	H/W	08/01	Roger	Gerber Gate List issue item 19	Move NB_MUTE from U215 pin 107 to pin73	0.4
71	16,17	H/W	08/01	Roger	Gerber Gate List issue item 20,21	Remove R178, pop R177	0.4
72	10,23	H/W	08/01	Roger	Gerber Gate List issue item 22,23	Depop R253, populate R1799	0.4

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
73	42	H/W	08/02	Roger	Gerber Gate List issue item3	Connect 2.5V_RUN_PWRGD net to LDO_POK pin. Add depop R49	0.4
74	18	H/W	08/02	Roger	Gerber Gate List issue item11	Add R1800 31.6K ohm resistor for Vmargin circuit.	0.4
75	23	H/W	08/02	Roger	Gerber Gate List issue item5	Change R389 from 1K to 10K	0.4
76	33, 40	H/W	08/04	Steven	Conbine the BT and TP in 30 PIN connector.	Delete JBT and move components to JTAP.	0.4
77	42	H/W	08/04	Steven	Gerber Gate List issue item3	Add Depop resister R3019.	0.4
78	22, 23	H/W	08/04	Steven	For intel NAPA platform check list 1.5 request.	Chnage R425 from 33Ohm pull-down to 8.2KOhm pull-up. And add pull-up resister R3020 in SIO_RCIN#.	0.4
79	19	H/W	08/08	Roger	Follow Intel CRB circuit	Pull up LDDC_CLK, LDDC_DATA to +3VRUN_R by R73, R74	0.4
80	16	H/W	08/09	Roger	V_DDR_MCH_REF discharge issue	Add R51 (100K_0402) connect to V_DDR_MCH_REF	0.4
81	23	H/W	08/09	Roger	Leakage issue when system into S3	Change SIO_EXT_SMI#, SIO_EXT_SCI# pull up to +3VSUS	0.4
82	36	H/W	08/09	Roger	Refer Dell docking reference circuit	Remove R1320, R1319	0.4
83	12	H/W	08/09	Roger	Gerber Gate List issue item 28	Depop R357	0.4
84	28	H/W	08/10	Roger	Gerber Gate List issue item 30	Add R53 4.7K resistor for LOM_SO pull down	0.4
85	28	H/W	08/10	Roger	Gerber Gate List issue item 33	Connect BCM5752 pin C4 to ECE5018 pin75 net name LOM_CABLE_DETECT. Series no stuff resistor R55	0.4
86	38	H/W	08/10	Roger	Gerber Gate List issue item 39	R1171 change pull up from +3VRUN to +3VSUS	0.4
87	38	H/W	08/10	Roger	Gerber Gate List issue item 42	Add a 4.7uF cap for ECE5018 VDDA33 coupling	0.4
88	39	H/W	08/10	Roger	Gerber Gate List issue item 43	Add a 0 Ohm 0402 resistor R62 in series with the RTC_CELL and EMC5004 pin 121	0.4
89	7	H/W	08/10	Roger	Follow Intel CRB circuit	R513, R514 pull up to +VCCP	0.4
90	39	H/W	08/10	Roger	Gerber Gate List issue item 46	Add resistor R63 (0_0402_5%) between the BIA_PWM signal and MEC5004 pin 73	0.4
91	39	H/W	08/10	Roger	Gerber Gate List issue item 47	Change ITP_DBRESET# connection from EMC5004 pin 55 to pin96	0.4
92	22	H/W	08/10	Roger	Gerber Gate List issue item 50	Add no stuff C69 (0.1U_0402_16V4Z) between THRMTRIP_ICH# and GND	0.4
93	41	H/W	08/10	Roger	None	Change R1795 pin 1 connect from +1.8VRUN to +1.8VSUS for discharge	0.4
94	23	H/W	08/10	Roger	Gerber Gate List issue item 51	Move pull-up R388 to pin 1 side of R1787	0.4
95	6	H/W	08/10	Roger	Gerber Gate List issue item 29	Add C70 (0.1U_0402_16V4Z) for +CK_VDD_MAIN decoupling. Remove R290, R343, R329 to save spacing	0.4
96	7	H/W	08/11	Roger	Gerber Gate List issue item 68	Remove R513 and R514 platform no longer use Yonah A00	0.4
97	42	H/W	08/11	Roger	Gerber Gate List issue item 65	Populate 0ohm for R49, R313, R319, R334	0.4

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98	41	H/W	08/11	Roger	Gerber Gate List issue item 67	Change R494 to 20K	0.4
99	7	H/W	08/11	Roger	Gerber Gate List issue item 69	Add no stuff C71 and C72 for +VCCP of JITP	0.4
100	7	H/W	08/11	Roger	Gerber Gate List issue item 70	Change R416 and R33 from 56 ohm to 54.9 ohm	0.4
101	12	H/W	08/11	Roger	Gerber Gate List issue item 72	Delete R333 to follow reference schematics	0.4
102	28	H/W	08/11	Roger	Gerber Gate List issue item 34	Add R68 (20K_0402_5%) and R70 (39K_0402_1%) for LAN_LOW_PWR voltage divider connect to pin K5	0.4
103	26,27,38	H/W	08/12	Roger	Gerber Gate List issue item 75	DOCK_HP_MUTE# for GPIO2 of codec connect to ECE5018 pin 81. EAPD for GPIO3 of codec connect to additional Q11 gate	0.4
104	38	H/W	08/15	Roger	Gerber Gate List issue item 38	Chnge SYS_PME# pull up from +3VRUN to +3VALW. Add no stuff R71 in series	0.4
105	38	H/W	08/15	Roger	Gerber Gate List issue item 41	Remove HP_NB_SENSE from ECE5018 pin 106 to pin 82	0.4
106	23	H/W	08/15	Roger	Gerber Gate List issue item 188,189	Depop R428,Change value of R75 to 10k ohms	0.4
107	40	H/W	08/16	Roger	Gerber Gate List issue item 48	Change R1750 and R1751 to L1 and L2	0.4
108	28	H/W	08/16	Roger	Gerber Gate List issue item 213	Depop U188, R1366 and populate U3, R1267 for ST AT45BCM021B	0.4
109	39	H/W	08/16	Roger	Gerber Gate List issue item 217	Remove R166. Move R1635 for AFT_INT# move to page 39	0.4
110	39	H/W	08/16	Roger	Add pull up for open drain out put	Add R93 pull up to +3VALW for BAT_SEL#	0.4
110	38	H/W	08/16	Roger	Mute internal speaker when docking aduio jack plug in	Add pull down resistor for DOCK_HP_MUTE#	0.4
111	06	H/W	09/07	Roger	Follow Dell CoE schematics	Change C329, C333 from 33pF to 27pF	0.5
112	43	H/W	09/14	Roger	Blue tooth LED too bright	Change R8 from 3.3K to 1K ohms	0.4
113	41	H/W	09/14	Roger	+1.8VSUS discharge low issue	Populate Q89, R1795	0.4
114	39	H/W	09/14	Roger	LID_CL# can't assert low	Change R482 from 100K to 1M ohms	0.4
115	40	H/W	10/04	Brike	Delete U46,C54,SW1	None	0.5
116	34, 39	H/W	10/13	Brike	Connect 8051TX to WWAN Pin 19 and Connect 8051RX to WWAN Pin 42.	Modified.	0.5
117	22	H/W	10/15	Brike	Gerber Gate List issue item 60	Add R97 0-ohm tuning resistor between R36 pin2 and X1 pin1	0.5
118	41	H/W	10/17	Brike	Gerber Gate List issue item 66	Change R1795 to a 30 ohm 0603 resistor	0.5
119	39	H/W	10/18	Brike	MEC5004 per SMSC recommendations to add circuit for improving POR issue.	Add de-pop components R101, R110, R112, R114, R117, Q20, Q19, C54, D2002. And change C1769 to 22U.	0.5
120	38	H/W	10/18	Brike	change board ID to X02	Pop R95, R419 and De-pop R108, R405.	0.5
121	40	H/W	10/18	Brike	Gerber Gate List issue item 77. Add 10pF cap between GND and pin2 of L1/L2.	Add C66, C73.	0.5

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
122	23	H/W	10/18	Brike	Gerber Gate List issue item 78. Pull up LAMP_STAT# to +3VRUN	Change R75 pull-up to +3.3V_RUN.	0.5
123	6	H/W	10/19	Brike	Gerber Gate List issue item 72. Inductor design follow M07 design on L40,L32 (Size:0805).	Change L32, L40 from 0603 to 0805.	0.5
124	23	H/W	10/19	Brike	Gerber Gate List issue item 79. SATA_DET# is pull up to +3.3V_SUS.	Change R784 pull up to +3.3V_SUS.	0.5
125	18	H/W	10/19	Brike	Gerber Gate List issue item 74.Make R1643 prior to bypass caps at +3VRUN.	Change R1643 prior to bypass caps " C152 and C517 " at +3VRUN power rail .	0.5
126	9	H/W	10/20	Brike	Gerber Gate List issue item 84	Change the 32 high frequency decoupling caps, 0805 X5R, from 22uF to 10uF. Depop C354 and C618.Change C352, C496, C497, and C365 from 330uF/7mOhm to 330uF/6mOhm SP caps.	0.5
127	34	H/W	10/20	Brike	Gerber Gate List issue item 82	Connect PLTRST# instead of PLTRST_DELAY# to WLAN and WWAN connectors.	0.5
128	23	H/W	10/20	Brike	IMVP_PWRGD glitch issue	Add C79 0.1uF cap on IMVP_PWRGD to filter the glitch	0.5
129	28	H/W	10/21	Brike	Q68 surge current	Add R102 (0603) and C80 0.1uF cap Q68 pin1 for reduce surge current	0.5
130	40,43	H/W	10/21	Brike	BT & HDD LED is on when the SNIFFER is turned on.	Added a circuit (FET and Resistors) to keep the BT LED & HDD LED off when the SNIFFER is turned on	0.5
131	38	H/W	10/21	Brike	Gerber Gate List issue item 81	Depop R1440	0.5
132	34	H/W	10/22	Brike	Add Intel WoWLAN Support Circuit	Add pop components Q21 and R101, and un-pop componet R24.	0.5
133	18	H/W	10/24	Brike	Gerber Gate List issue item 89. Change OTP trip temperature to 88 deg C.	Change R249 to 332K and R262 to 118K.	0.5
134	39	H/W	10/24	Brike	Gerber Gate List issue item 90. Pop SMSC workround circuit for 11/7 build.	Pop R101, R110, R112, R114, R117, Q20, Q19, C54, D2002.	0.5
135	39	H/W	10/24	Brike	Gerber Gate List issue item 91. Add a 0 ohm pulldown resistor on TEST_PIN.	Add R122 0Ohm resister.	0.5
136	43	H/W	10/24	Brike	Gerber Gate List issue item 111. Remove one of the pull-ups on SNIFFER_LED_OFF#.	Remove Pull up resister R1447.	0.5
137	43	H/W	10/24	Brike	Gerber Gate List issue item 110.	More R76 to pin 1 of Q66 and populate it.	0.5
138	34	H/W	10/24	Brike	Add Intel WoWLAN Support Circuit	Replace Q21 and R101 to D2003	0.5
139	20	H/W	10/24	Brike	Gerber Gate List issue item 108. Add 39 ohm resistors at output of U190 and U191.	Add resister R102 and R123.	0.5
140	18	H/W	10/24	Brike	Gerber Gate List issue item 92. Add thermistor circuit to VCP2 (pin 40) of EMC4000. Please route to 5V_CAL_SIO2# (pin 80, GPIO B4 on ECE5018).	Add thermistor circuit R479, R480, R481, C79, Q21.	0.5
141	43	H/W	10/24	Brike	Gerber Gate List issue item 114. Modified SATA_ACT# LED sniffer disable circuit.	Modified the circuit and Add and D2004. Chnage Q1 to 3904, R1449/1448 change to 10K and 1K.	0.5
142	40	H/W	10/25	Brike	Gerber Gate List issue item 119. For fix the IMVP_PWRGOOD glitch issue.	Change delay circuit R1764 from 200KOhm, C1788 to 470PF to +1.8V_run and +3V_run.	0.5

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143	38	H/W	10/25	Brike	Gerber Gate List issue item 104. Modified the SATA_ACT# circuit.	Modified the circuit Pull up R1449 to +5V_SUS and R1445 to +5V_run. R2 move to Q1 pin 3, SNIFFER_LED change to GPIO82.	0.5
144	20	H/W	10/25	Brike	Gerber Gate List issue item 116. Add diode HSYNC and VSYNC buffers.	Add D2005 (RB751) in U190, U191 Pin 5.	0.5
145	40, 43	H/W	10/26	Brike	Modified HDD/BT disable circuit.	Move 40 BT Disable circuit to 43.	0.5
146	19	H/W	10/26	Brike	Add level shit circuit for BIA_PWM.	Delete R520 and Add U8.	0.5
147	23	H/W	11/03	Brike	the delay circuit on +3.3V should get rid of the glitch	Depop C82.	0.5
148	41	H/W	11/03	Brike	Populate the HDD power switch circuit	Pop Q51, R507, Q50 and Depop PJP24.	0.5
149	31	H/W	11/03	Brike	For passing EMVCo test.	Change R1424 from 220 to 330Ohm.	0.5
150	43	H/W	11/03	Brike	SNIFFER_LED_OFF# is a push/pull signal.	De-pop R1445.	0.5
151	27	H/W	11/03	Brike	To improve audio quality	Change C199 to 0.022uF and pop R164, depop R170.	0.5
152	39	H/W	11/11	Brike	Change SMSC MEC5004 from version C to D.	Change U216 P/N to D version. Depop R117, R114, R110, R101, R104, D2002, Q19, Q20, C54. And chnage C1769 value from 22UF to 4.7UF.	0.5
153	39	H/W	11/11	Brike	Change DOCK_SMB_CLK and DOCK_SMB_DAT for consistent with other M07 platforms.	Change R99 and R100 resister from 100K to 8.2K Ohm. And R1618 change to 10KOhm.	0.5
154	43	H/W	11/11	Brike	For improve LED brightness issue.	Change R2 value from 56Ohm to 330Ohm. And modified R15 from 150Ohm to 100Ohm.	0.5
155	28	H/W	11/12	Brike	For Q68 broken issue. Modified R120 value for protect base pin.	ChangeR120 from 0Ohm to 2KOhm.	0.5
156	20	H/W	11/12	Brike	For Dell request change D32, D2005 to RB500.	Change D32 and D2005 from RB751 to RB500	0.5
157	27	H/W	11/12	Brike	For improve Audio THD+n performance.	Change C113, C114 and C146 from 1UF to 2.2U.	0.5
158	27	H/W	11/27	Brike	For adjust Audio gain to 15.6DB.	Pop R170, De-pop R164.	0.5
159	42	H/W	12/06	Brike	For improving SUSPWROK turn on issue.	Modified Q7 to 2N7002.	0.6
160	52	H/W	12/06	Brike	For solving DVI eye diagram issue.	Change C3030, C3025 from 1uF to 10uF; R3006 to 220Ohm; R3015, R3016, R3017, R3018 to 100Ohm.	0.6
161	23, 38	H/W	12/06	Brike	For solving HD warn boot parking sound issue.	Change HDDC_EN#, MODC_EN# from ICH7 to ECE5018 Pin 106, 107 (GPIOH2/3), and Depop R2148, R2149.	0.6
162	7	H/W	12/06	Brike	Add a De-pop resister for CPU test 1 PIN.	Add De-pop resister R1387.	0.6
163	39	H/W	12/07	Brike	Add an damping resister for improving SPI_CS# overshoot issue.	Add 47Ohm resister R127.	0.6
164	39	H/W	12/07	Brike	For solving SBAT_SMBDAT rising time over spec issue.	Change R444 to 4.7KOhm resister.	0.6
165	6	H/W	12/12	Brike	For Gerber Gating list item 14 Depop pullup resistor on ICH_CLKREQ#.	Depop resister R1761.	0.6
166	38	H/W	12/12	Brike	For Gerber Gating list item 17 Update board ID to A00	Pop R405, depop R419.	0.6
167	31	H/W	12/12	Brike	For Gerber Gating list item 11 add 47pF capacitors to the USB_BIO+/- pins to fix bio sensor ESD issue.	Add 2 capaciotr C83, C84 in USB_BIO+/-.	0.6

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
168	41	H/W	12/14	Brike	For GPIOH[3:2] need, chnage pullup resister power plane to always.	Change pullup resister R2148, R2149 for +3.3V_SUS to +3.3V_ALW.	0.6
169	41	H/W	12/15	Brike	For Gerber Gating list item 18. Change pullup resister to 10K.	Change pullup resister R2148, R2149 for 100K to 10KOhm.	0.6
170	18	H/W	12/15	Brike	For Gerber Gating list item 1. Remove pullup resister from 2.5V_RUN_PWRGD.	Remove R116.	0.6
171	39	H/W	12/19	Brike	For Gerber Gating list item 21. Add 0 ohm series resistor to SPI_CS# at MEC5004.	Add series resister R143 at MEC5004 side.	0.6
172	31	H/W	12/19	Brike	For improving USB BIO sensor EMI issue.	Add Pop L5, and depop resister R128, R137.	0.6
173	40	H/W	12/20	Steven	For DELL EMI request for add a 0.1uF capacitor in JTPAD.	Add 0.1uF capacitor C85.	0.6
174	28	H/W	12/30	Steven	For Q68 damage issue change form BCP69 to MBT35200 as ZRS solution.	Use MBT35200 to replace Q68. Modified.	0.6
175	7	H/W	12/31	Brike	Intel Design Guide 1.0 to change H_RESET pull-up resister to 51Ohm.	Change resister R416 to 51Ohm.	0.6
176	39	H/W	01/04	Brike	For enable MEC5004 BIOS write protect function.	Pop R139 and de-pop R138.	0.6
177	27	H/W	01/07	Benson	For adjust Audio gain to 21.6 DB.	DePop R170, pop R164.	0.6
178	28	H/W	01/09	Brike	For Q68 issue to reserve soft start circuit.	Change R120 to 0Ohm, and depop C80.	0.6
179	20	H/W	01/20	Brike	For fixing issue with projector using long cable.	Change R102,R123 from 39 ohm to 0 ohm	**0.6**
180	19	H/W	01/20	Brike	For stronger the VGS driving in Battery Mode	Change R235 from 200K ohm to 100K ohm	**0.6**
181	6	H/W	01/20	Brike	The Drive Level too high	Change R32 from 0 ohm to 470 ohm	**0.6**
182	22	H/W	01/20	Brike	The Negative Resistance too low	Change X1 spec from CL=20pF to 6 pF and C38,C40 from 12pF to 2.2pF	**0.6**
183	38	H/W	01/20	Brike	The Frequency too high & Drive Level too high	Change Y1 spec from CL=20pF to 12pF and C1451,C1452 from 22P to 15P	**0.6**
184	31	H/W	01/20	Steven	None	Depop L5 ,pop R128,R137 33 ohm	**0.6**
185	39	H/W	02/07	Steven	For solving primary battery hand issue.	Change R447, R449 to 4.7KOHm; R444, R131 to 2.2KOhm.	**0.6**

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	PWR	06/01	Saha	M4 input current more than MAX8734 LDO3 output 100mA	Delete PU17 SN74AHC1G32DCKR OR GATE(SA00732018L), PR49 1K_0402_1%(SD03410018L) Add PR350 0_0402_5%(SD02800008L) connact LDO3 to ON3 PU18 74AHCT1G08GW AND GATE(SA00000L30L) PR352 1K_0402_1%(SD03410018L) PR351 0_0402_5%(SD02800008L)	0.2 0.2
2	46	PWR	06/01	Saha	MAX8734 LDO soft start issue.	Delete PR27 4.7_1210_5%(SD000007E8L) Un-pop PC20 4.7U_1206_25V6K(SE093106M8L)	0.2
3	46	PWR	06/01	Saha	PWR_SRC noise issue	Un-pop PC252 100U_25V_M(SF10004M008)	0.2
4	44/45	PWR	06/01	Saha	+3VALW change to +3VSRC	Rename net +3VALW to +3VSRC	0.2
5	47	PWR	06/01	Saha	VCCP high/low side MOSFET change from IR to Infineon No-stuff PC207 and PC208	PQ38 change from IR7821(SB57821008L) to BSO072N03S(SB00000418L) PQ40 change from IR7832(SB57832008L) to BSO072N03S(SB00000418L) Un-pop PC207 and PC208 10U_0805_6.3V5K(SE093106M8L)	0.2
6	47	PWR	06/01	Saha	VCCP_1P05VP OCP issue(5A)	PR224 change from 124K_0402_1%(SD03412438L) to 60.4K_0402_1%(SD03460428L)	0.2
7	47/48	PWR	06/01	Saha	Choke height issue.(5.6mm change to 5.0mm)	PL14 and PL27 change from 1.4U_HMU1356-1R4_15.5A H5.6mm(SH04814AM8L) to 1.4U_HMU1350-1R4_15A H5.0mm(SH000004H8L)	0.2
8	44	PWR	06/01	Saha	PSID materiel change by Dell	PQ1 change from BSS138_SOT23(SB50138008L) to FDV301_SOT23(SB50301008L)	0.2
9	50	PWR	06/01	Saha	New version MAX8731 PIN1 define GND	Un-pop PR337 0_0402_5%(SD02800008L),Pop PR336 0_0402_5%(SD02800008L)	0.2
10	50	PWR	06/02	Saha	Add RC filter at pin 23 of MAX8731	Add PR360 1_0603_1%(SD014100B8L) PC253 220P_0402_50V7K(SE074221K8L)	0.2
11	46/48	PWR	06/02	Saha	Add support for Reliability voltage margining tests	Add PR356, PR355 and PR359 0_0603_5%(SD01300008L) PR353 and PR354 0_0402_5%(SD02800008L)	0.2
12	48	PWR	06/16	Saha	Change output capactior rating voltage from 6.3V to 2.5V	PC70 and PC71 change from 330U_D3L_6.3V_R25(SGA00000N8L) to 330U_D2E_2.5VM_R15(SGA19331D0L)	0.3
13	49	PWR	06/22	Saha	Change VCORE DPRSLPVR input resistor value	PR248 change from 0_0402_5%(SD02800008L) to 499_0402_1%(SD03449900L)	0.3
14	50	PWR	06/22	Saha	Add power limit schematic	Depop PR361 80.6K_0402_1%, PR362 200K_0402_1%, PR363 121K_0402_1%, PR364 3.01K_0402_1%, PR365 499K_0402_1%, PR366 100K_0402_1%, PR367 100K_0402_1%, PC254 0.01U_0402_25V8K, PC255 100P_0402_50V8K, PC256 100P_0402_50V8K, PC257 100P_0402_50V8K, PC258 0.01U_0402_25V8K, PC259 10P_0402_50J8K, PQ81 RHU002N06_SOT323, PU19 LM393DR_SO8	0.3
15	46	PWR	06/29	Saha	Discreate 3VALW and 3VSRC.	Add PU17 SN74AHC1G32DCKR OR GATE(SA00732018L), PR49 1K_0402_1%(SD03410018L) PQ82 FDC655BN_NL(SB000004P8L) Delete PR352 1K_0402_1%(SD03410018L) PR351 0_0402_5%(SD02800008L) PR350 0_0402_5%(SD02800008L) PU18 74AHCT1G08GW AND GATE(SA00000L30L)	0.3

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16	46	PWR	06/29	Saha	Add V+ input Resistor	Add PR27 0_1206_5%(SD00100000L)	0.3
17	45/51	PWR	06/29	Saha	Battery conn. and battery selector +3VSRC change to +3VALW	Rename +3VSRC to +3VALW	0.3
18	47	PWR	06/29	Saha	ISL6227 Issue change 1.05V/1.5VHigh/Low side MOSFET change 1.05V choke adjust OCP and ISEN value	VCC Change from +5VRUN to +5VSUS. EN1 and EN2 change from RUNPWROK to RUN_ON. PR221 change from 20K_04-2_1%(SD03420028L) to 19.6K_0402_1%(SD00000358L) PQ8 change from FDS6994S(SB56994008L) to FDS8880(SB000004U8L) Add PQ83 FDS6670AS(SB000004T8L) PQ38 change from BSO072N03S(SB00000418L) to FDS8880(SB000004U8L) PQ40 change from BSO072N03S(SB00000418L) to FDS6670AS(SB000004T8L) PL27 change from 1.4U_HMU1350(SH000004H8L) to 1.5U_SIL104(SH04215A08L) Add PC261 0.01U_0402(SE068103K8) Add PC262 and PC263 2200P_0402(SE074222K8L) PR219 change from 825_0402_1%(SD03482508L) to 1.43K_0402_1%(SD03414318L) PR220 change from 825_0402_1%(SD03482508L) to 2.1K_0402_1%(SD03421018L) PR223 change from 69.8K_0402_1%(SD03469828L) to 124K_0402_1%(SD03412438L) PR224 change from 60.4K_0402_1%(SD03460428L) to 124K_0402_1%(SD03412438L)	0.3
19	49	PWR	06/29	Saha	ISL6260 Issue	Delete PR338, PR339 and PR340 2.7_0603_5% Change PC246, PC247, PC248 to 1500P_0805-----Unpop Change PH1 from ERTJ1VR103J(SL20000020L) to NCP15WM474J03RB(SL20000098L) PR284 change from 15.8K_0402_1%(SD03415828L) to 0_0402_5%(SD02800008L) Add PC260 0.1U_0603(SE042104K8L)	0.3
20	50	PWR	06/29	Saha	Change +VCHGR output CAP from 1206 to 1210	PC113 and PC114 change from 10U_1206(SE142106M8L) to 10U_1210(SE056106K8L)	0.3
21	47	PWR	08/12	Saha	Add VSEN capacitor	Add PC265 and PC264 100P_0402_50V8K(SE071101K8L)	0.4
22	47	PWR	08/12	Saha	Delete PGOOD pull high resistor	Delete PR283 100K_0402_1%(SD03410038L) De-pop PR195 100K_0402_1%(SD03410038L)	0.4
23	48	PWR	08/12	Saha	Delete reliability test resistor	Delete PR283 110K_0603_1%, PR359 0_0603_1%, and PR82 59.6K_0603_1%	0.4
24	49	PWR	08/12	Saha	Adjust VCORE load line	PR267 change from 7.87K_0402_1%(SD03478718L) to 9.09K_0402_1%(SD034909100) PR231, PR331, and PR270 change from 7.68K_0402_1%(SD00000238L) to 7.68K_0805_1%(SD00000B08L)	0.4
25	49	PWR	08/12	Saha	Delete H_PROCHOT# resistor	Delete PR235 0_0402_5%(SD02800008L)	0.4
26	50	PWR	10/17	Saha	Add RC filter in FBSA/B PIN	Add PR368 and PR369 100_0402_5%(SD02810008L) Add PC266 and PC267 0.01U_0603_50V7K(SE025103K8L) Un-pop PR371 and PR370 0_0402_5%	0.5
27	46	PWR	10/17	Saha	EMI request: change BST3 resestor	Change PR32 from 0_0603_5%(SD01300008L) to 2.2_0603_5%(SD013220B8L)	0.5
28	46	PWR	10/17	Saha	change 3V out put CAP height	change PC31 from 330U_6.3V_R25 H1.9(SGA00001C8L) to 330U_6.3V_R25 H2.8(SGA0000089L)	0.5

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
29	50	PWR	10/17	Saha	Populate UL circuit	Populate PR361-PR367, PC254-259, PU19, PQ81. Change PR361 from 80.6k to 0. Change PR362 from 200k to 301k. Change PR363 from 121k to 59k. Change PR364 from 3.01k to 27.4k. Change PR365k from 499k to 4.32Meg.	0.5
30	49	PWR	10/20	Saha	Change VCC_CORE OCP, SOFT, and DPRSTP# value	PR260 change from 20K_0402_1%(SD03420028L) to 11.5K_0402_1%(SD03411520L) PC187 change from 0.022U_0402_16V7K(SE076223K8L) to 0.01U_0402_16V7K(SE076103K8L) Add PR372 0_0402_5%(SD02800008L) Delete PR246 0_0402_5%(SD02800008L) Un-pop PR249 0_0402_5%(SD02800008L)	0.5
31	48	PWR	10/20	Saha	Change PU6 BST resistor	PR73 change from 0_0603_5%(SD01300008L) to 1_0603_5%(SD013100B8L)	0.5
32	44	PWR	10/20	Saha	Change PQ2 from RUH002N06 to 3904	PQ2 change from RHU002N06(SB50206008L) to MMST3904(SB000002R0L)	0.5
33	49	PWR	11/12	Saha	Adjust CPU Load Line	PR267 change from 9.09K_0402_1%(SD03490918L) to 10.5K_0402 _1%(SD03410528L) PR261 change from 3.57K_0402_1%(SD03435718L) to 2.47K_0402 _1%(SD03424318L) Add PC252 100U_25V_(6.3X7.7)(SF10004M08L) Add PC215 0.068U_10VX7R_0402 (SE102683K8L)	0.5
34	50	PWR	12/6	Saha	Deeply dischargered battery problem.	Add PD54 1SS355_sod323(SC1SS35500L) Add PR373 1K_0603_1%(SD01410018L)	0.5
35	50	PWR	12/6	Saha	Follow Coe A09 schematic	Add PC267 3300PF_0402_50V7K(SE074332K8L) Depop PC266 0.01U_0603_50V7K(SE025103K8L)	0.5
36	47	PWR	12/15	Saha	Follow GGL 1214 item19.	Depop PR12	0.6
37	49 50 46	PWR	1/7	Saha	For acoustical issue	Add PC270~PC273 and PC268 10U_1206_25V6M(SE142106M8L)	0.6