8 7 6 5 4 3 2 1

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REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
				2010-10-12

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,FLYING_DUTCHMAN,MLB,K91F

REV B RELEASE, 01/31/11

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8620	1	SCHEM,MLB,K91	SCH	CRITICAL	
820-2915	1	PCBF,MLB,K91	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Jan 31 12:49:37 2011

DRAWING TITLE: SCHEM,MLB,K91

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DRAWING NUMBER | SIZE: D

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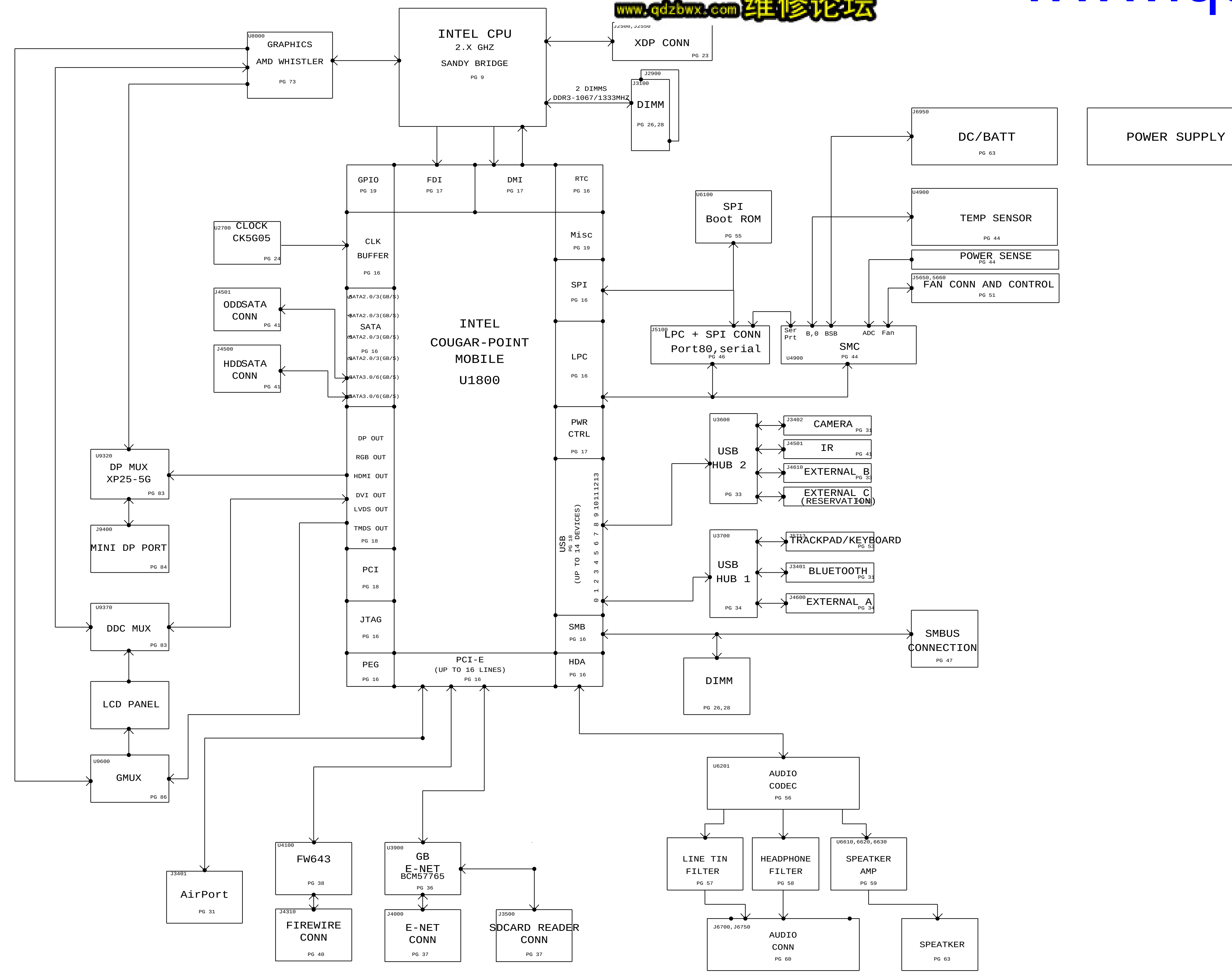

SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE

System Block Diagram

DRAWING NUMBER SIZE D

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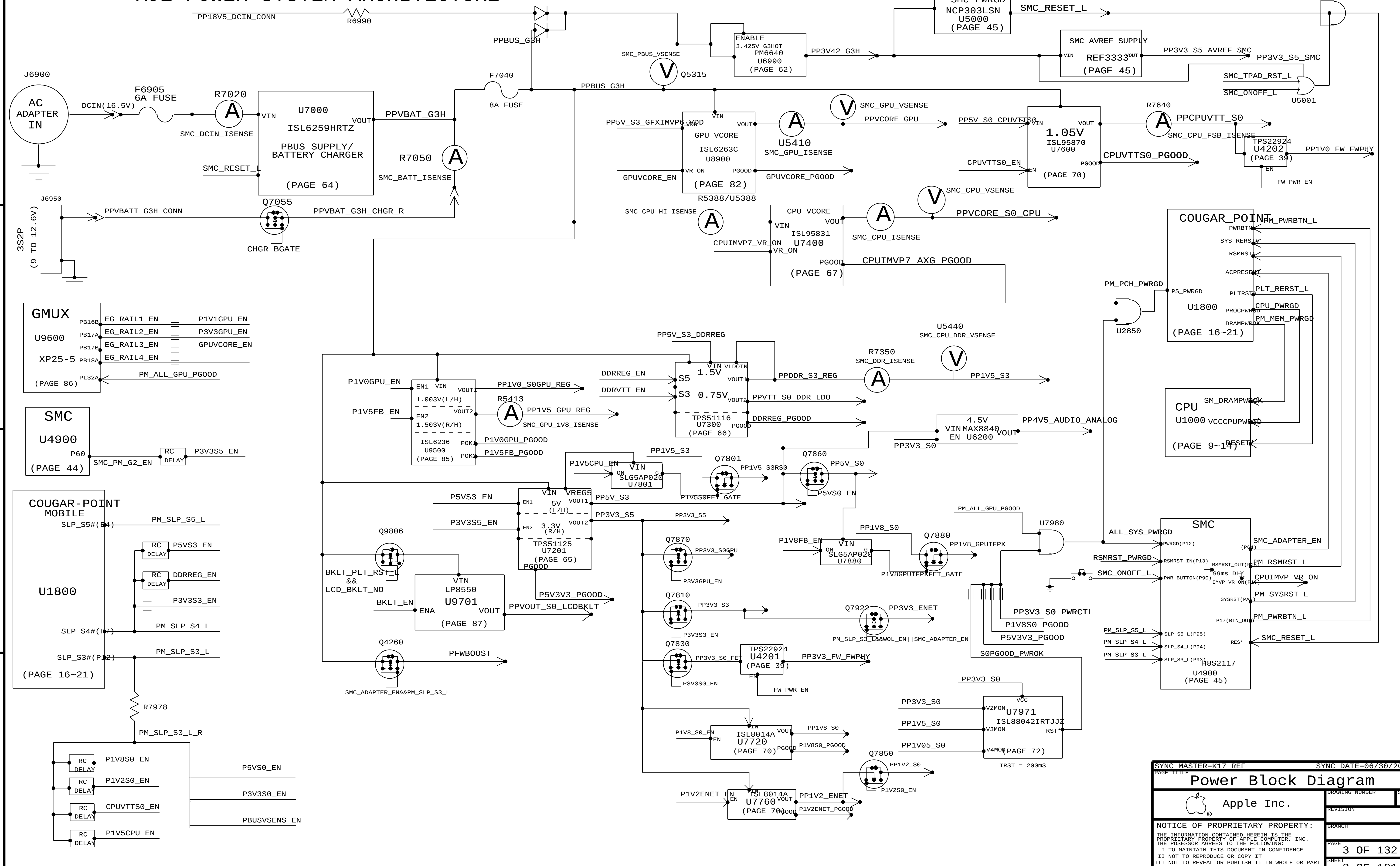
K91 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE

Power Block Diagram

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PAGE 3 OF 132

SHEET 3 OF 101

8 7 6 5 4 3 2 1

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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Revision History

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1468	PCBA,MLB,K91F,DG64	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG64
639-1972	PCBA,MLB,K91F,DL83	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL83
639-1971	PCBA,MLB,K91F,DL82	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL82
639-1469	PCBA,MLB,K91F,DG65	K91_COMMON,SODIMM:FOXCONN,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG65
639-1970	PCBA,MLB,K91F,DL86	K91_COMMON,SODIMM:HYBRID,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL86
639-1956	PCBA,MLB,K91F,DL7W	K91_COMMON,SODIMM:MOLEX,CPU:2_2GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7W
639-1470	PCBA,MLB,K91F,DG66	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DG66
639-1974	PCBA,MLB,K91F,DL87	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL87
639-1976	PCBA,MLB,K91F,DL88	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_HYNIX,VRAM_DVP1,VRAM_DVP0,EEEE:DL88
639-1471	PCBA,MLB,K91F,DG67	K91_COMMON,SODIMM:FOXCONN,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DG67
639-1973	PCBA,MLB,K91F,DL81	K91_COMMON,SODIMM:HYBRID,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL81
639-1954	PCBA,MLB,K91F,DL7T	K91_COMMON,SODIMM:MOLEX,CPU:2_3GHZ,GPU:WHISTLER,FB_1G_SAMSUNG,VRAM_DVP0,EEEE:DL7T
639-1573	PCBA,MLB,K91,DHMV	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DHMV
639-1945	PCBA,MLB,K91,DL7Q	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7Q
639-1953	PCBA,MLB,K91,DL7R	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_HYNIX,EEEE:DL7R
639-1574	PCBA,MLB,K91,DHMW	K91_COMMON,SODIMM:FOXCONN,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DHMW
639-1959	PCBA,MLB,K91,DL80	K91_COMMON,SODIMM:HYBRID,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL80
639-1960	PCBA,MLB,K91,DL7Y	K91_COMMON,SODIMM:MOLEX,CPU:2_0GHZ,GPU:SEYMOUR,FB_256_SAMSUNG,EEEE:DL7Y
085-1901	K91/K91F DEVELOPMENT BOM	K91_DEVEL:ENG

K91 BOM GROUPS

BOM GROUP	BOM OPTIONS
K91_COMMON	ALTERNATE,COMMON,K91_COMMON1,K91_COMMON2,K91_PROGPARTS,K91_PROGPARTS1,UVGLUE_K91_K91F,K91_PVT
K91_COMMON1	CPUMEM_S0,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_2NONREM,USBHUB_2513B
K91_COMMON2	GPUVID_1P11V,KB_BL,T29:YES,ENET_SD:B0,T29BST:Y,SDRV_PD,SDRVI2C:MCU,T29_DP_HPD:ALL_OR
K91_PVT	BMON:PROD,VREFMRGN_NOT,XDP,XDP_CPU_BPM,BKLT:PROD,ISNS_ON:NO,LPCPLUS_R:YES
K91_PROGPARTS	GMUX_PROG,IR_PROG,TPAD_PROG:PVT,ENETROM_PROG:PVT,T29ROM:PROG,T29MCU:PROG
K91_PROGPARTS1	SMC_PROG:PVT,BOOTROM_PROG:PVT
K91_DEVEL:ENG	SNB_CPT_XDP,BMON:ENG,GMUX_JTAG_CONN,VREFMRGN,LPCPLUS_CONN:YES,LPCPLUS_R:YES,BKLT:ENG,S0PGOOD_ISL,CPURIPPLE_ENG,IMVPISNS_ENG,ISNS_ON:YES,DEBUG_ADC,DIGI_MIC
K91_DEVEL:PVT	SNB_CPT_XDP,LPCPLUS_CONN:YES,LPCPLUS_R:YES
SNB_CPT_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4031	1	IC,CPU,SNB,SR030,PRQ,D2,2.0,45W,4+2,1.20,6M,BGA	U1000	CRITICAL	CPU:2_0GHZ
337S4032	1	IC,CPU,SNB,SR00W,PRQ,D2,2.2,45W,4+2,1.30,6M,BGA	U1000	CRITICAL	CPU:2_2GHZ
337S4033	1	IC,CPU,SNB,SR00U,PRQ,D2,2.3,45W,4+2,1.30,8M,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4029	1	IC,PCH,COUGARPOINT,SLH9D,PRQ,BD82HM65	U1800	CRITICAL	
337S3936	1	IC,GPU,AMD,WHISTLER,962FCBGA,40NM,ES	U8000	CRITICAL	GPU:WHISTLER
337S3979	1	IC,GPU,AMD,SEYMOUR,M2 LP,ES1,962BGA	U8000	CRITICAL	GPU:SEYMOUR
338S0945	1	IC,ASSP,LIGHTRIDGE,S LHAJ,PRQ,FCBGA,15X15MM	U3600	CRITICAL	T29:YES
343S0534	1	IC,ASIC,GBIT ETHERNET&SD CTRLR,686 QFN8X8,B0	U3900	CRITICAL	ENET_SD:B0
343S0494	1	IC,ASIC,GBIT ETHERNET&SD CTRLR,686 QFN8X8,A0	U3900	CRITICAL	ENET_SD:A0
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
333S0543	4	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0564	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0571	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,C-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0572	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX
333S0543	2	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8500,U8550	CRITICAL	FB_256_SAMSUNG
333S0564	2	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8500,U8550	CRITICAL	FB_256_HYNIX
353S3055	1	IC,PI3VEDP212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	
725-1479	1	MLB LOCTITE UV EB CPU,PCH,T29,GPU,K91	UV_GLUE_K91_K91F	CRITICAL	UVGLUE_K91_K91F
516S0806	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,FOXCONN	J3100	CRITICAL	SODIMM:FOXCONN
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:FOXCONN
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:MOLEX
516-0245	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,MOLEX	J2900	CRITICAL	SODIMM:MOLEX
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:HYBRID
516-0246	1	CONN,204P,SODIMM,SOCKET,DDR3,p=0.6M,FOXCONN	J2900	CRITICAL	SODIMM:HYBRID

ETHERNET ROM

335S0663	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S2685	1	IC,ENET,1MBITFLASH,CIV REV01,K74/K75,K40	U3990	CRITICAL	ENETROM_PROG:A0_SD
341S2973	1	IC,ENET,1MBITFLASH,CIV REV01,K60/K62	U3990	CRITICAL	ENETROM_PROG:B0_SD
341S3026	1	IC,ENET,1MBITFLASH,CIV REV01,K90i/K91/K92	U3990	CRITICAL	ENETROM_PROG:EVT
341S3096	1	IC,ENET ROM,1MBIT,DVT,PVT,K90i/K91x	U3990	CRITICAL	ENETROM_PROG:PVT

Alternate Parts
(Alternate) (Primary)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA
353S2805	353S2603		ALL	Fairchild wafer option
128S0264	128S0257		ALL	Sanyo alt to Kemet
128S0303	128S0282		ALL	Panasonic alt to Sanyo
353S3085	353S1658		ALL	ST Micro alt to LT
376S0972	376S0612		ALL	ROHM alt to Toshiba N-FET
376S0855	376S0613		ALL	Diodes alt to Toshiba dual N-FET
138S0676	138S0691		ALL	Murata alt to Samsung cap
138S0652	138S0648		ALL	Samsung / Murata alt for Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt for Samsung
152S0685	152S0796		ALL	Dale/Vishay/TDK alt for Cyntec
376S0977	376S0859		ALL	Diodes alt for Rohm
353S2592	353S3199		ALL	U6201 AUDIO CODEC OLD REV IS ALTERNATE FOR NEW REV
335S0550	335S0777		ALL	add 4K byte as alternative to 2K
371S0679	371S0652		ALL	NXP alternate for pin diodes
138S0671	138S0673		ALL	Taiyo Yuden alt for Murata 10 uF caps

EFI ROM

335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S2893	1	IC,EFI,ROM,PROTO0, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S2934	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S2991	1	IC,EFI,ROM,PROTO2, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S2894	1	IC,EFI,ROM,EVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:EVT
341S2895	1	IC,EFI,ROM,DVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:DVT
341S2896	1	IC,EFI,ROM,PVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PVT

PSOC

341S2902	1	IC,TP PSOC,K9x,PROTO0	U5701	CRITICAL	TPAD_PROG:PROTO0
341S2940	1	IC,TP PSOC,K9x,PROTO1	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3001	1	IC,TP PSOC,K9x,PROTO2	U5701	CRITICAL	TPAD_PROG:PROTO2
341S3024	1	IC,TP PSOC,K9x,EVT	U5701	CRITICAL	TPAD_PROG:EVT
341S3099	1	IC,TP PSOC,K9x,DVT,PVT	U5701	CRITICAL	TPAD_PROG:PVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DDKG]	CRITICAL	EEEE:DDKG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG63]	CRITICAL	EEEE:DG63
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG64]	CRITICAL	EEEE:DG64
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG65]	CRITICAL	EEEE:DG65
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG66]	CRITICAL	EEEE:DG66
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG67]	CRITICAL	EEEE:DG67
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMV]	CRITICAL	EEEE:DHMV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DHMW]	CRITICAL	EEEE:DHMW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL81]	CRITICAL	EEEE:DL81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL82]	CRITICAL	EEEE:DL82
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL83]	CRITICAL	EEEE:DL83
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL84]	CRITICAL	EEEE:DL84
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL85]	CRITICAL	EEEE:DL85
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL86]	CRITICAL	EEEE:DL86
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL87]	CRITICAL	EEEE:DL87
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL88]	CRITICAL	EEEE:DL88
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL89]	CRITICAL	EEEE:DL89
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Q]	CRITICAL	EEEE:DL7Q
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7R]	CRITICAL	EEEE:DL7R
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7T]	CRITICAL	EEEE:DL7T
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7V]	CRITICAL	EEEE:DL7V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7W]	CRITICAL	EEEE:DL7W
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL7Y]	CRITICAL	EEEE:DL7Y
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DL80]	CRITICAL	EEEE:DL80

Programmables - All Builds

341S2830	1	IC,CPLD,LATTICE,GMUX,K91/K91F	U9600	CRITICAL	GMUX_PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2384	1	IR,ENCORE II,CY7C63833-LFXC	U4800	CRITICAL	IR_PROG
341S3129	1	IC,T29 EEPROM,PVT,K9x	U3690	CRITICAL	T29ROM:PROG
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S3128	1	IC,PROGRMD,LPC1112A,T29 PORT MCU,PVT,HVQFN25	U9330	CRITICAL	T29MCU:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2957	1	IC,GPU ROM,K91/F,K92,PROG	U8701	CRITICAL	GPUROM:PROG
335S0724	1	IC,GPU ROM,K91/F,K92,BLANK	U8701	CRITICAL	GPUROM:BLANK

SMC

338S0895	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2854	1	IC,SMC,DEVELOPMENT-PROTO0,K91	U4900	CRITICAL	SMC_PROG:PROTO0
341S2935	1	IC,SMC,DEVELOPMENT-PROTO1,K91	U4900	CRITICAL	SMC_PROG:PROTO1
341S2994	1	IC,SMC,DEVELOPMENT-PROTO2,K91	U4900	CRITICAL	SMC_PROG:PROTO2
341S2861	1	IC,SMC,DEVELOPMENT-EVT,K91	U4900	CRITICAL	SMC_PROG:EVT
341S2864	1	IC,SMC,DEVELOPMENT-DVT,K91	U4900	CRITICAL	SMC_PROG:DVT
341S2867	1	IC,SMC,DEVELOPMENT-PVT,K91	U4900	CRITICAL	SMC_PROG:PVT

SYNC_MASTER=K17_REF SYNC_DATE=05/28/2009

PAGE TITLE
BOM Configuration

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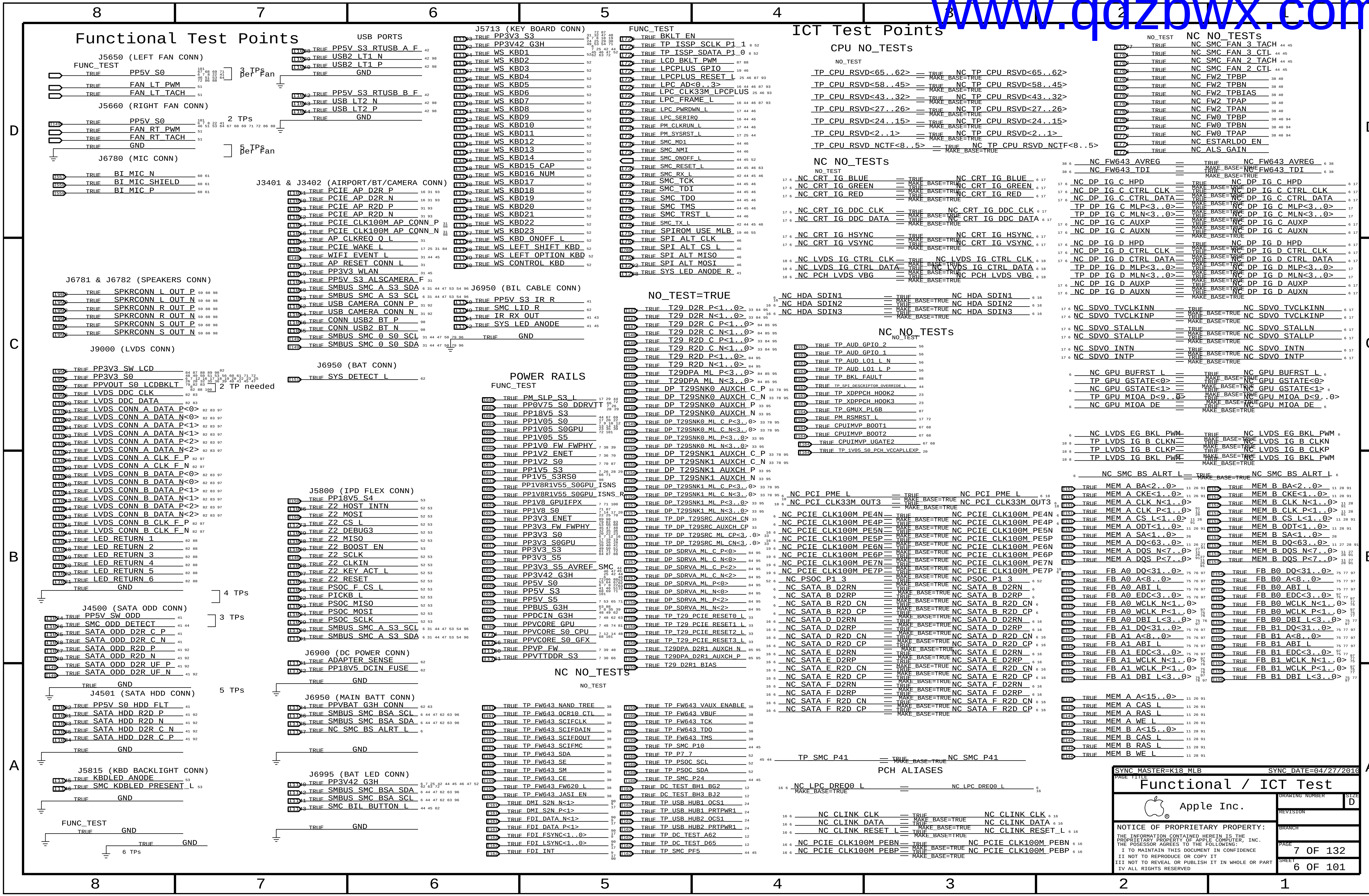

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Functional Test Points
FUNC_TEST
J5650 (LEFT FAN CONN)
3 TPs per Fan
J5660 (RIGHT FAN CONN)
2 TPs
5 TPs per Fan
J6780 (MIC CONN)
J6781 & J6782 (SPEAKERS CONN)
J9000 (LVDS CONN)
2 TP needed
4 TPs
3 TPs
J4500 (SATA ODD CONN)
J4501 (SATA HDD CONN)
5 TPs
J5815 (KBD BACKLIGHT CONN)
6 TPs
USB PORTS
J3401 & J3402 (AIRPORT/BT/CAMERA CONN)
J5800 (IPD FLEX CONN)
J6900 (DC POWER CONN)
J6950 (MAIN BATT CONN)
J6995 (BAT LED CONN)
J5713 (KEY BOARD CONN)
J6950 (BIL CABLE CONN)
J6950 (BAT CONN)
POWER RAILS
NC NO_TESTS
NO_TEST=TRUE
ICT Test Points
CPU NO_TESTs
NC NO_TESTs
PCH ALIASES
SYNC_MASTER=K18_MLB
SYNC_DATE=04/27/2010
PAGE TITLE
Functional / ICT Test
Apple Inc.
DRAWING NUMBER
SIZE
D
REVISION
BRANCH
PAGE
7 OF 132
SHEET
6 OF 101
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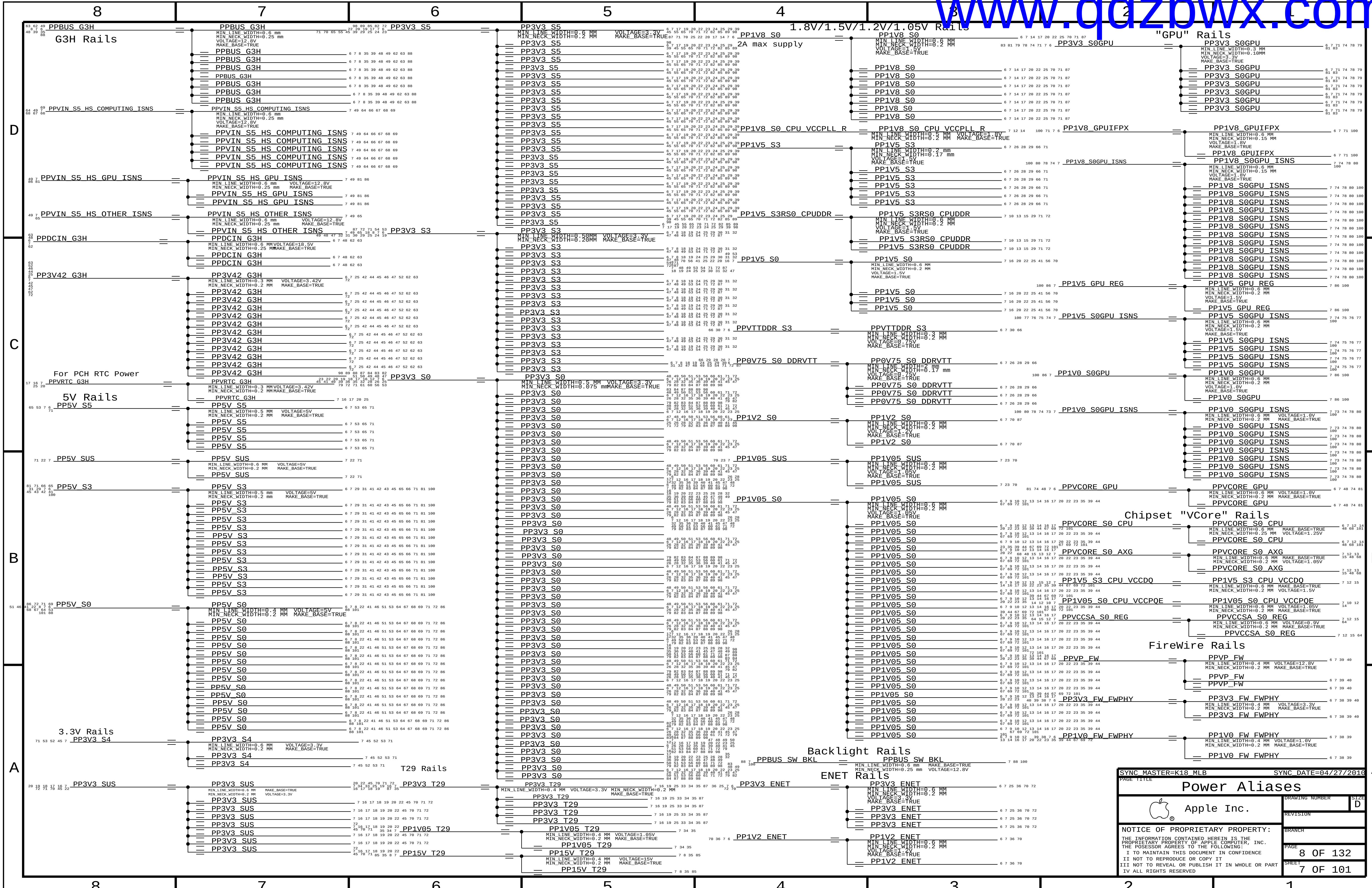

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PAGE TITLE

Power Aliases

Apple Inc.

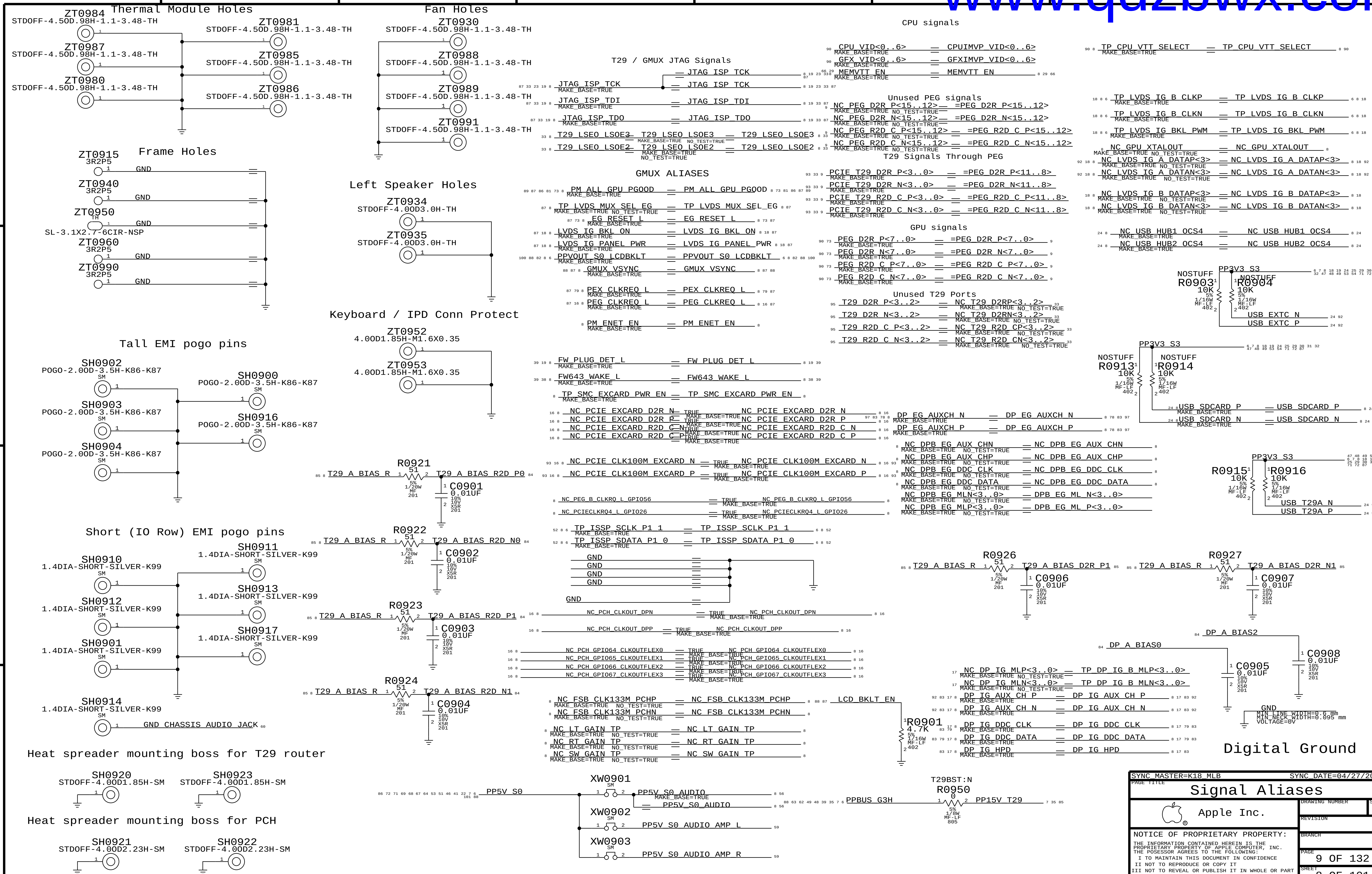
DRAWING NUMBER

SIZE D

REVISION

BRANCH

PAGE 8 OF 132



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

Signal Aliases

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DRAWING NUMBER | SIZE D

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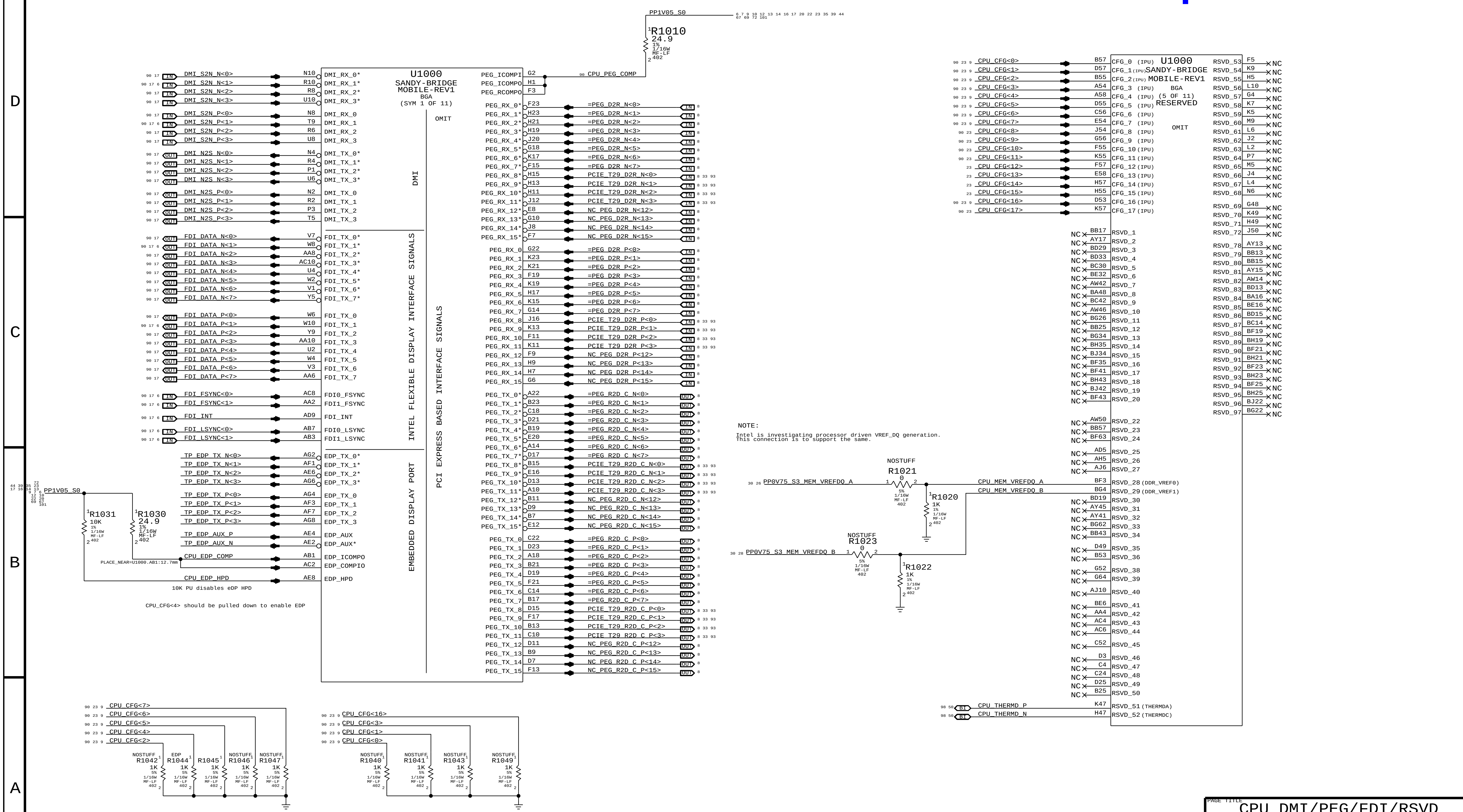

FOR SANDYBRIDGE PROCESSOR

CFG [7]	:PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5]	:PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4]	:eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3]	:PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2]	:PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

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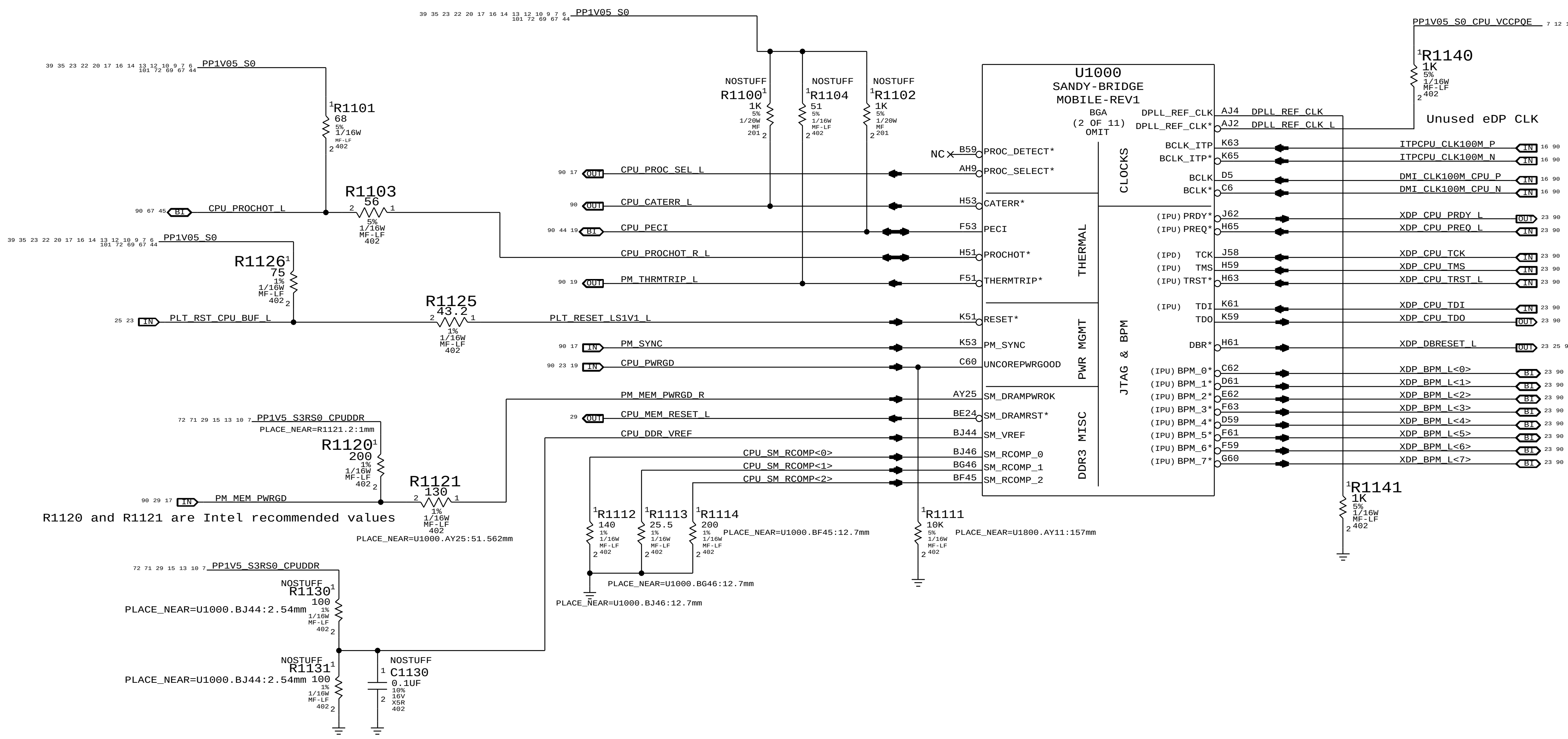

CPU CLOCK/MISC/JTAG

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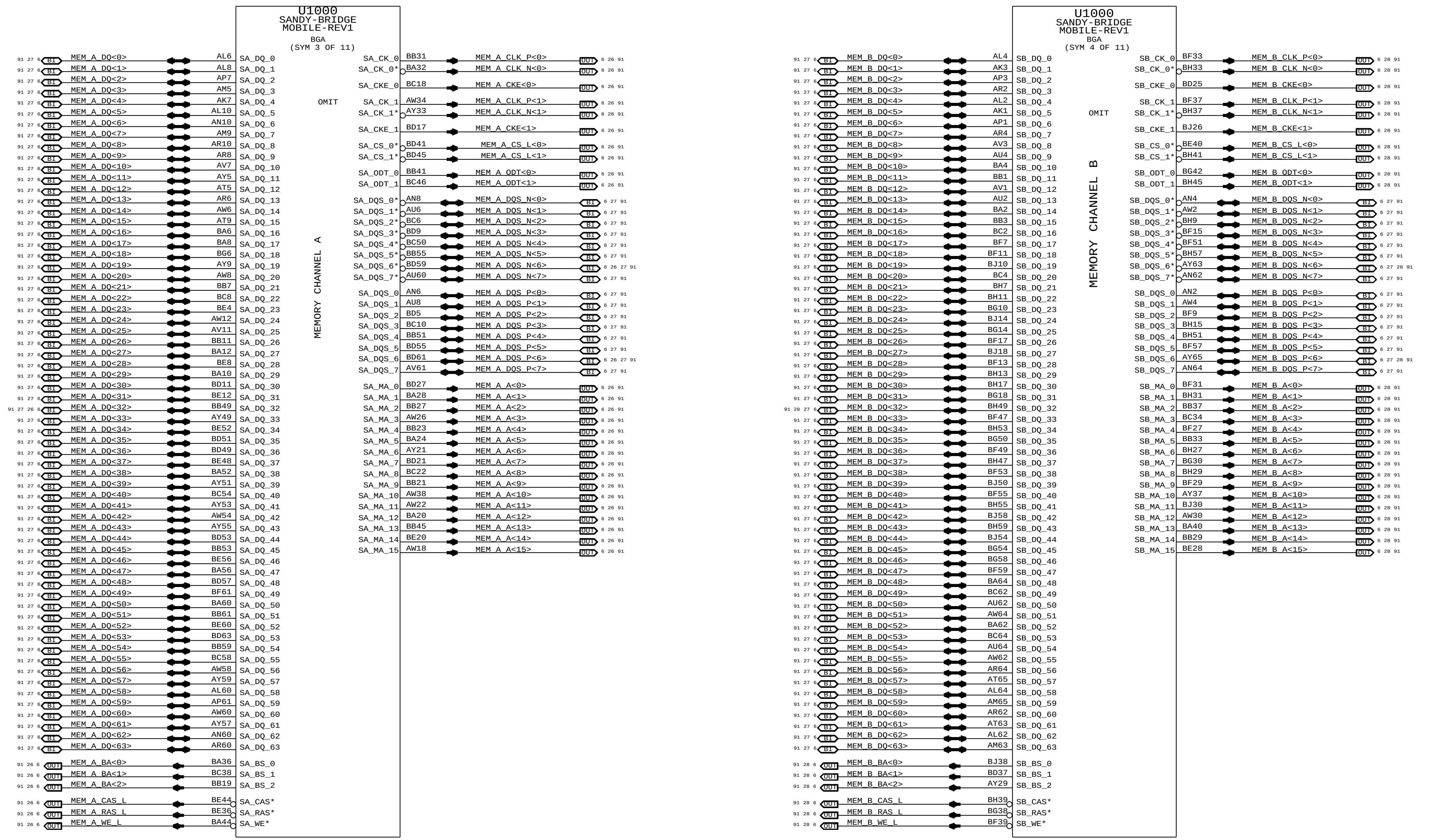

SYNC_DATE=06/15/2010

PAGE TITLE

CPU DDR3 INTERFACES

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REVISION

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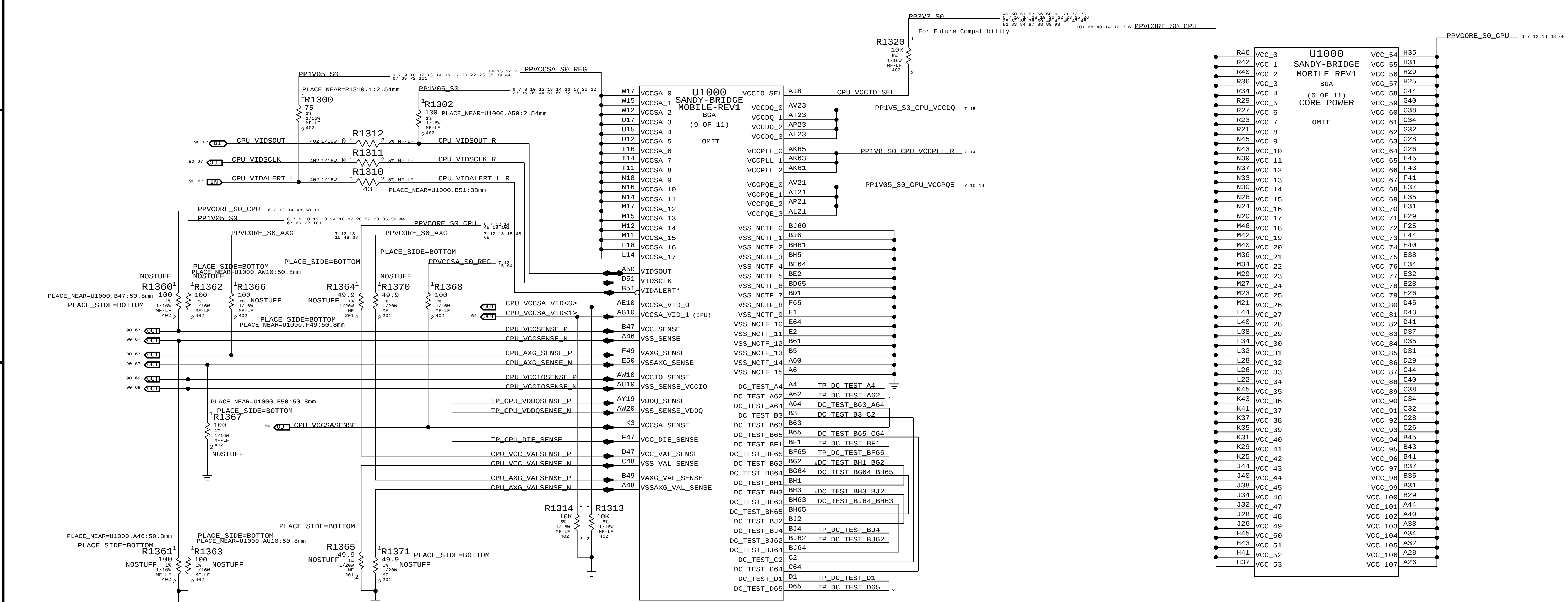
PAGE 12 OF 132

SHEET 11 OF 101



PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

SYNC_MASTER=K92_MLB SYNC_DATE=08/03/2010

PAGE TITLE
CPU POWER

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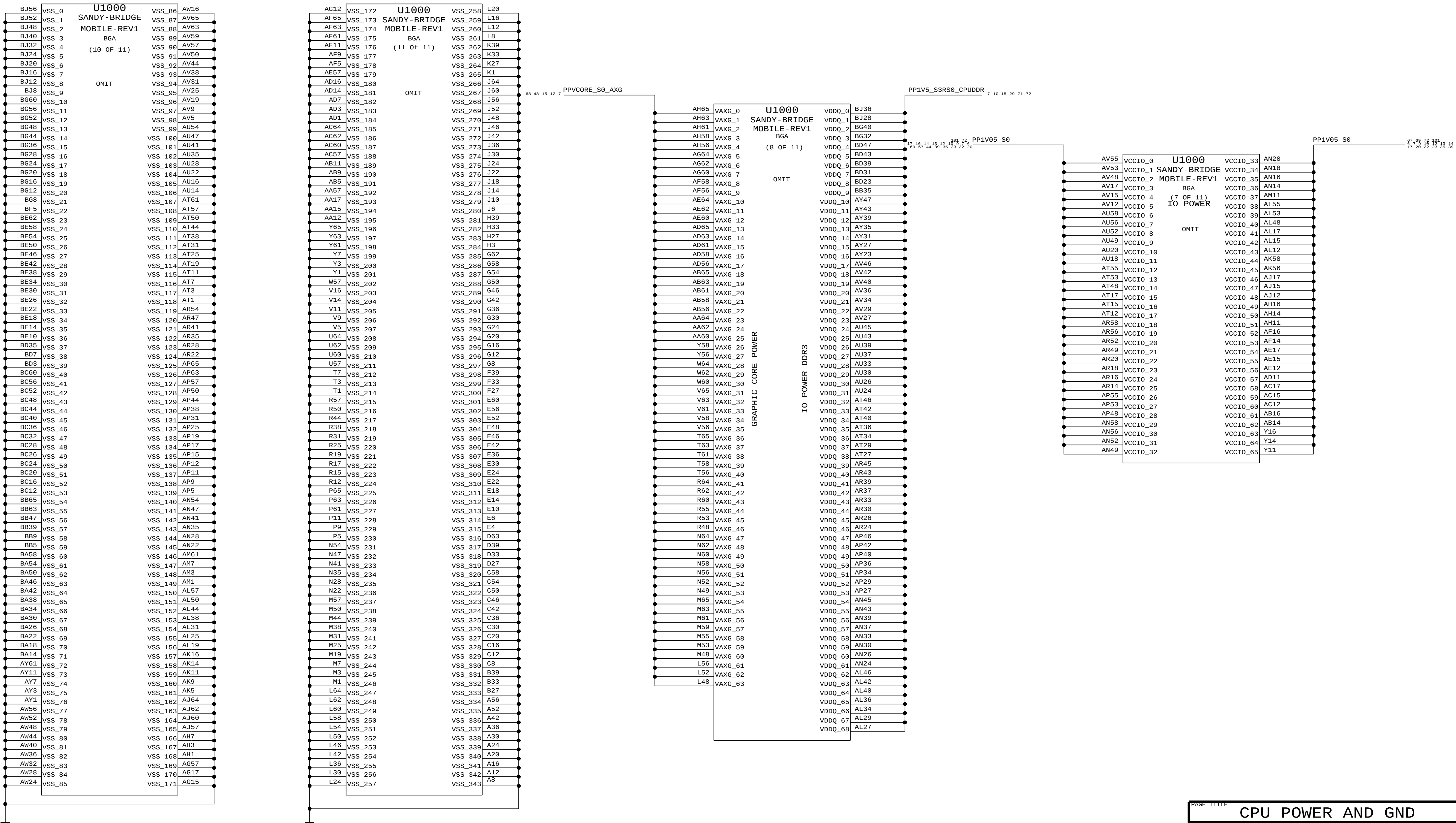

CPU POWER AND GND

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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

PLACEMENT_NOTE (C1620-C1623):
Place near U1000 on bottom side

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

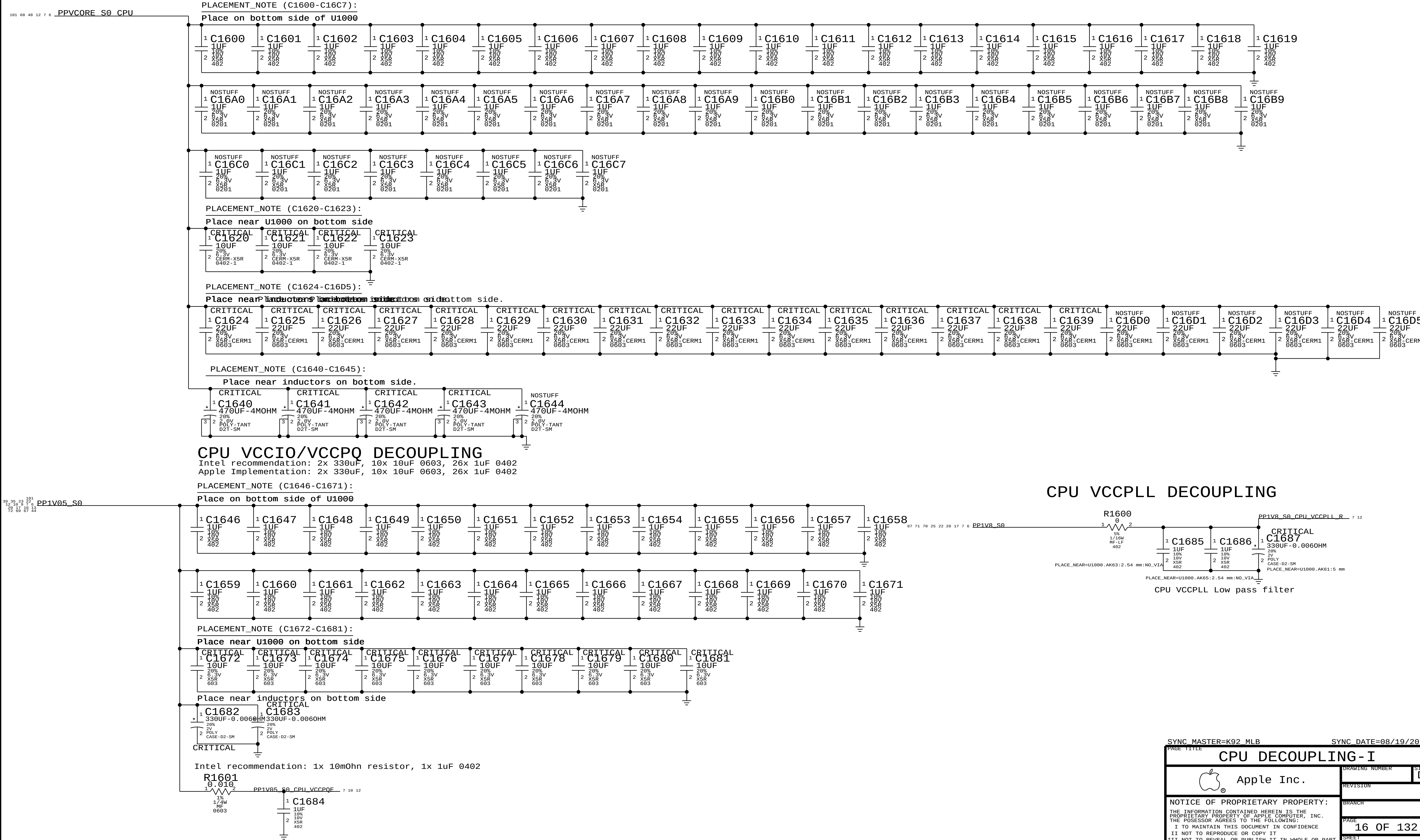
PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

Place near inductors on bottom side

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

CPU VCCPLL DECOUPLING

CPU VCCPLL Low pass filter



SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2010

PAGE TITLE: CPU DECOUPLING-I

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www.qdzbwx.com

VAXG DECOUPLING

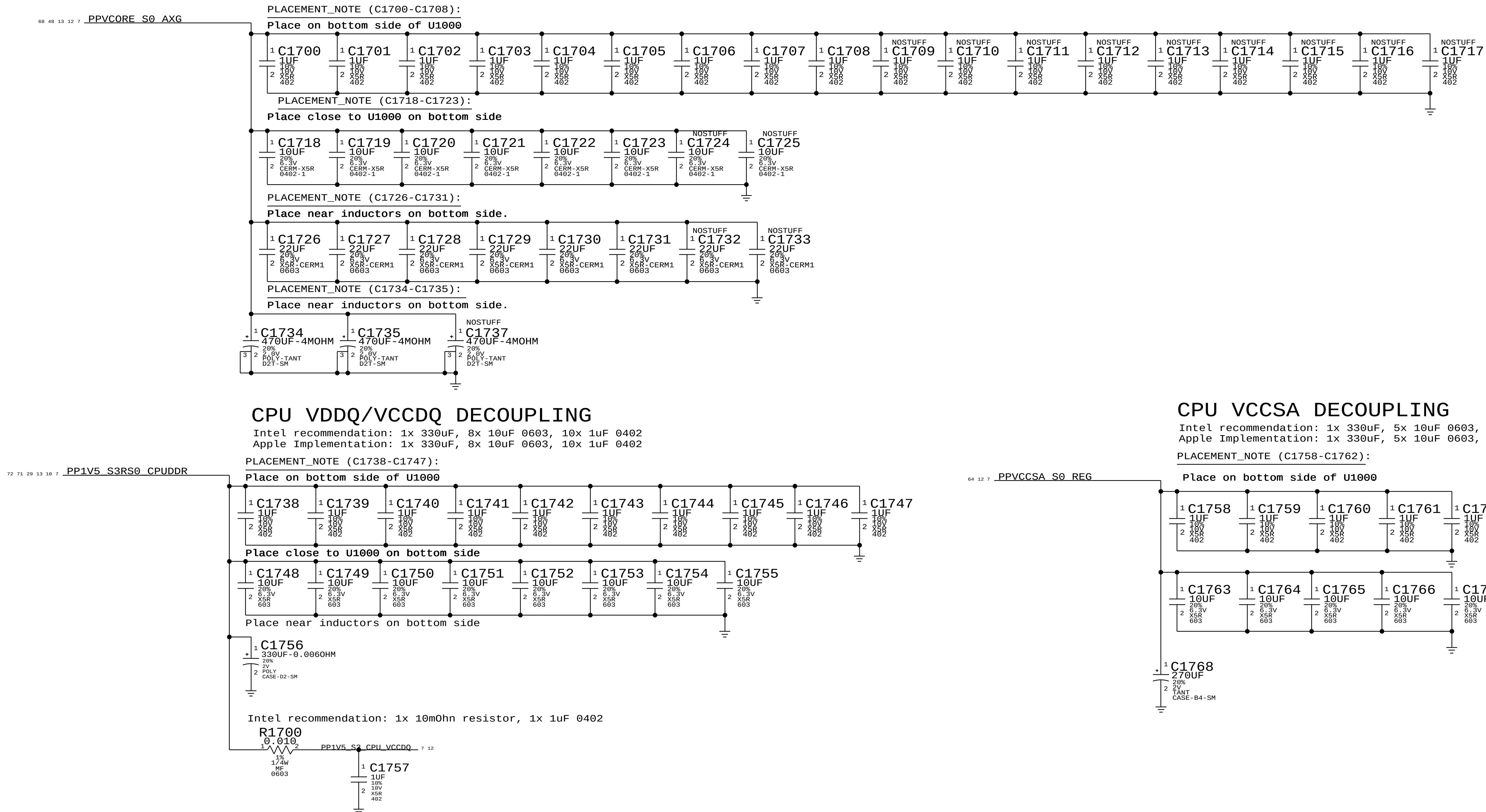
Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402



SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2010

PAGE TITLE: CPU DECOUPLING-II

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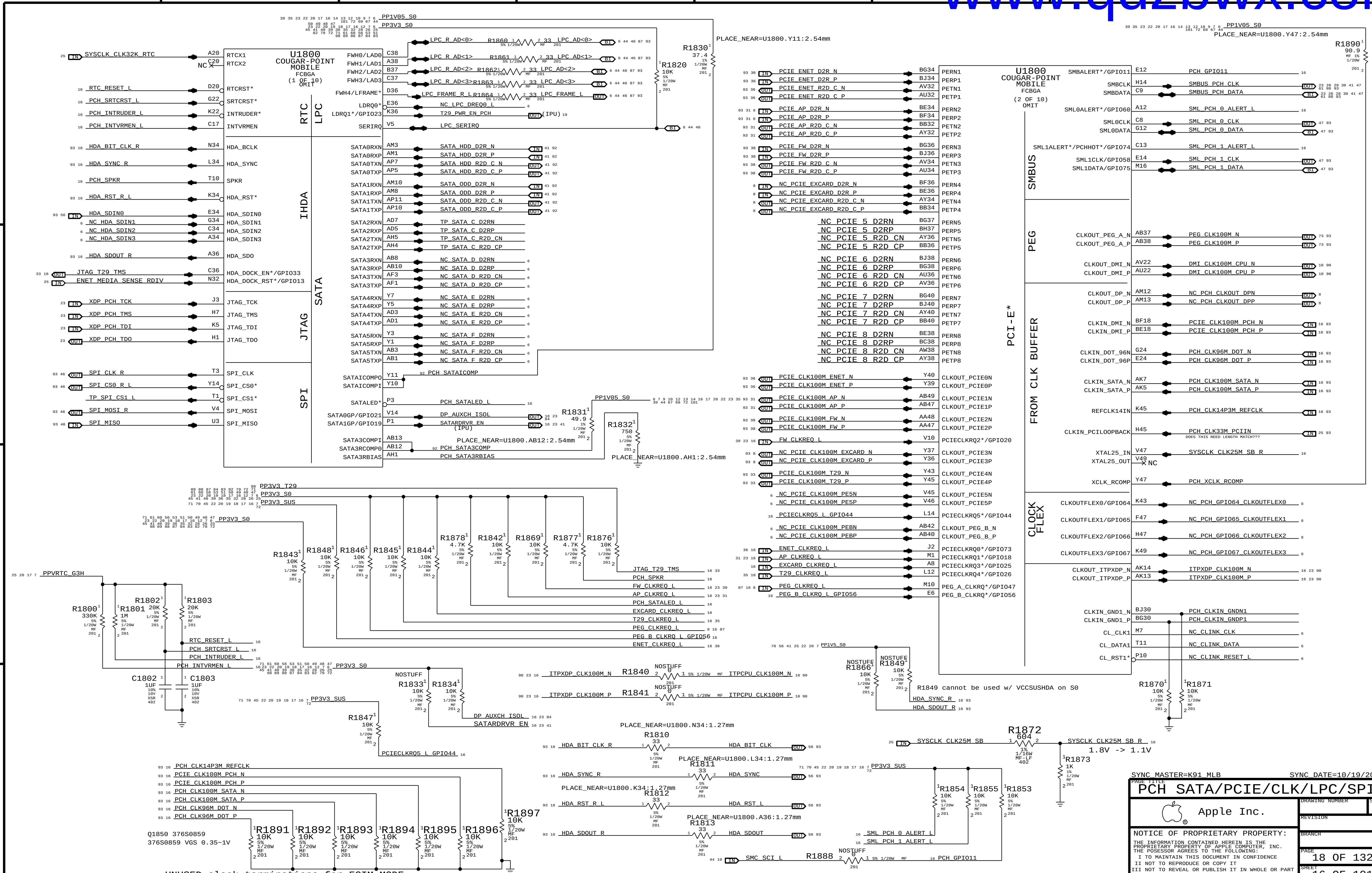

SYNC_MASTER=K91_MLB SYNC_DATE=10/19/2010

PAGE TITLE

PCH SATA/PCIE/CLK/LPC/SPI

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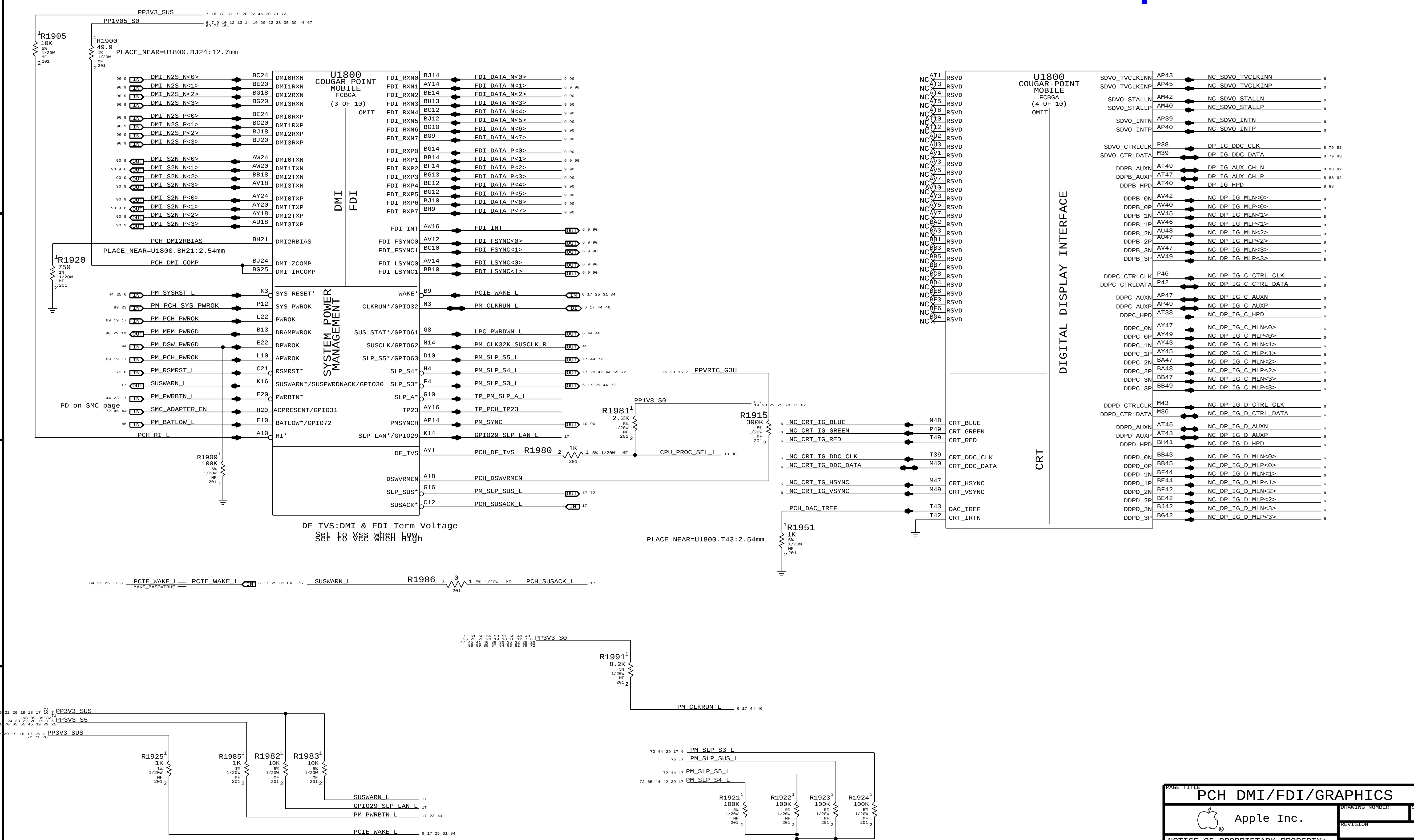
PAGE 18 OF 132

SHEET 16 OF 101



PAGE TITLE
PCH DMI/FDI/GRAPHICS

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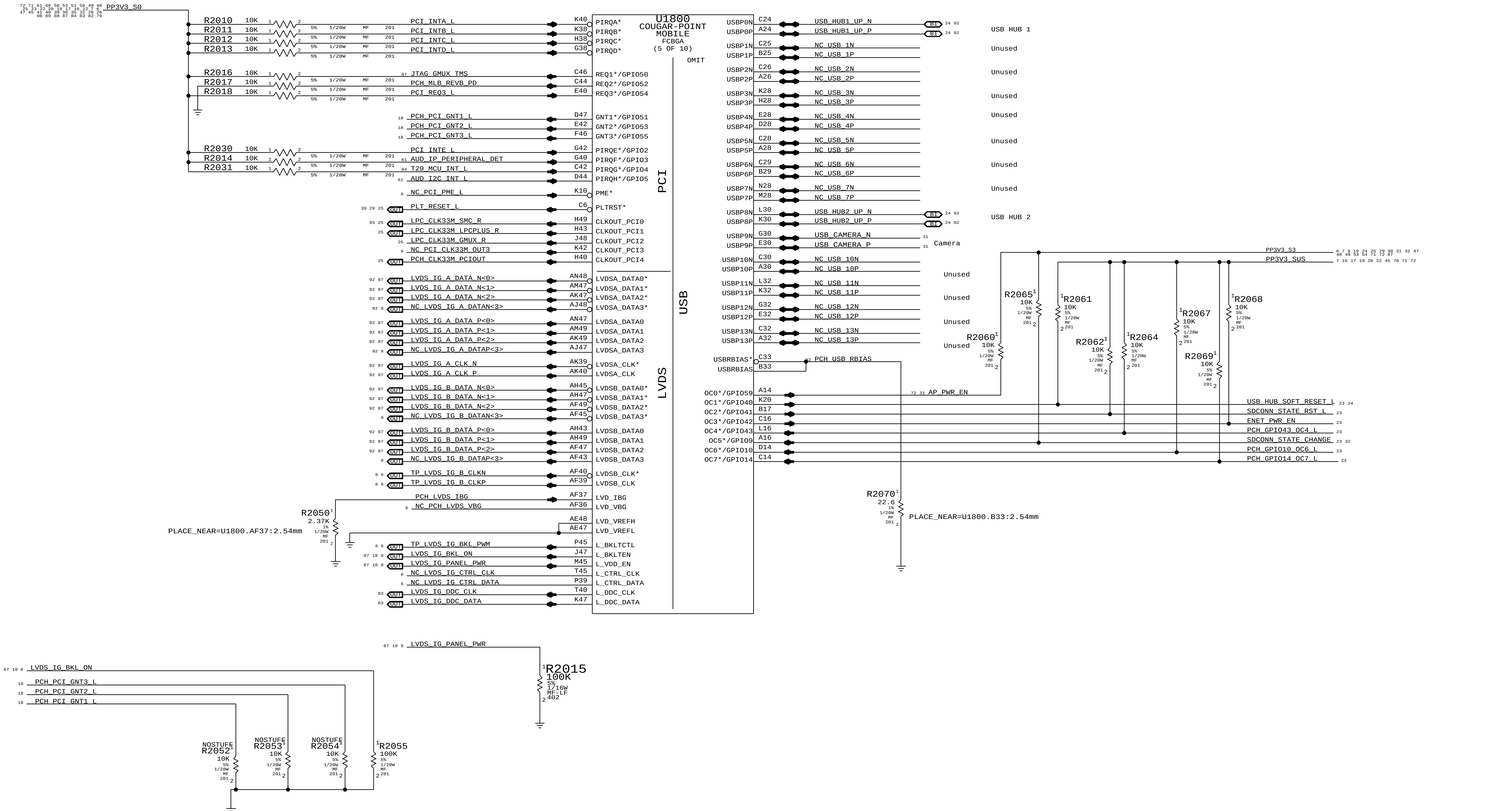

SYNC_MASTER=K92_MLB SYNC_DATE=07/06/2010

PAGE TITLE

PCH PCI/FLASHCACHE/USB

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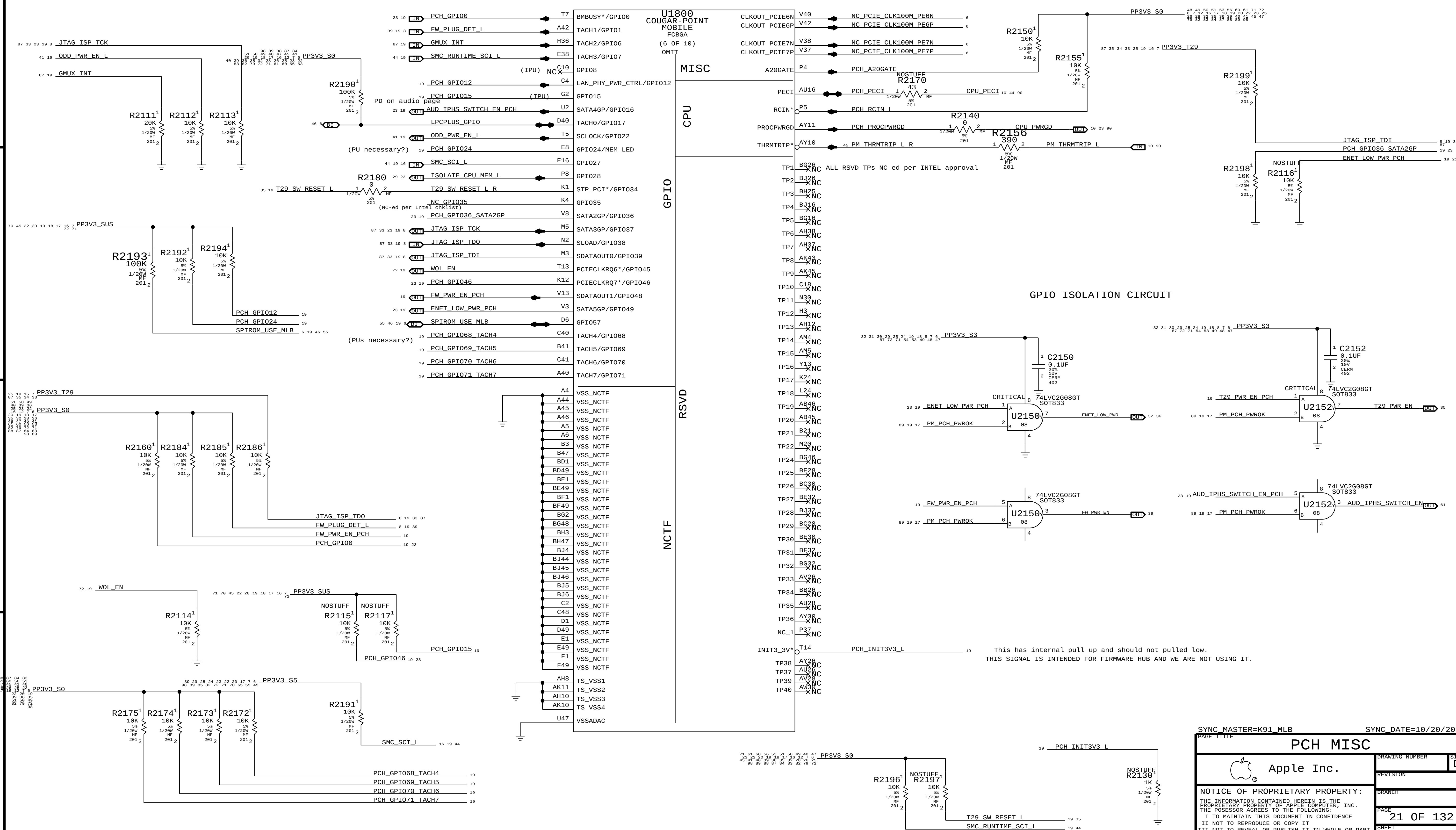

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PAGE TITLE

PCH MISC

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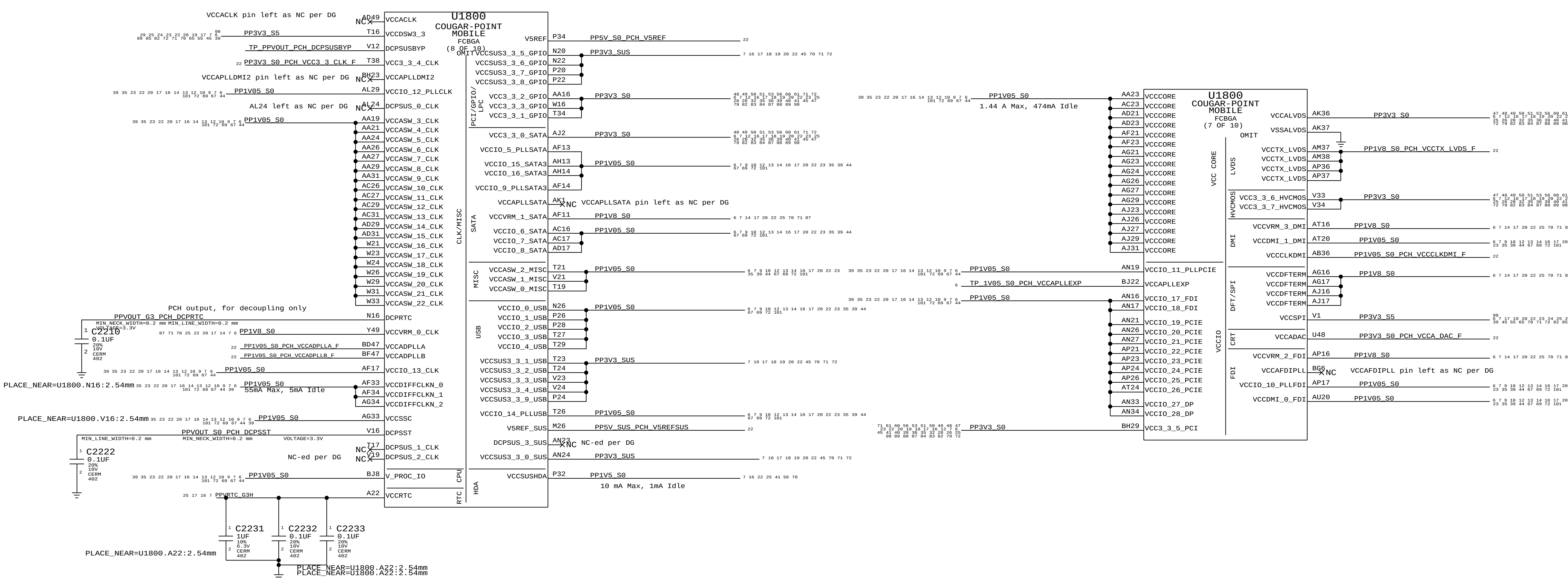

PAGE TITLE

PCH POWER

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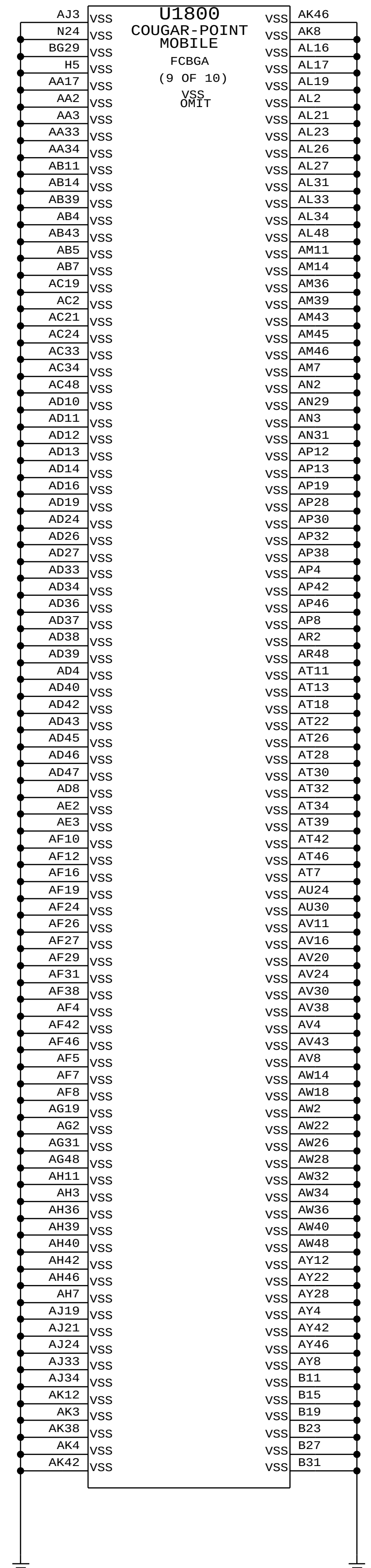

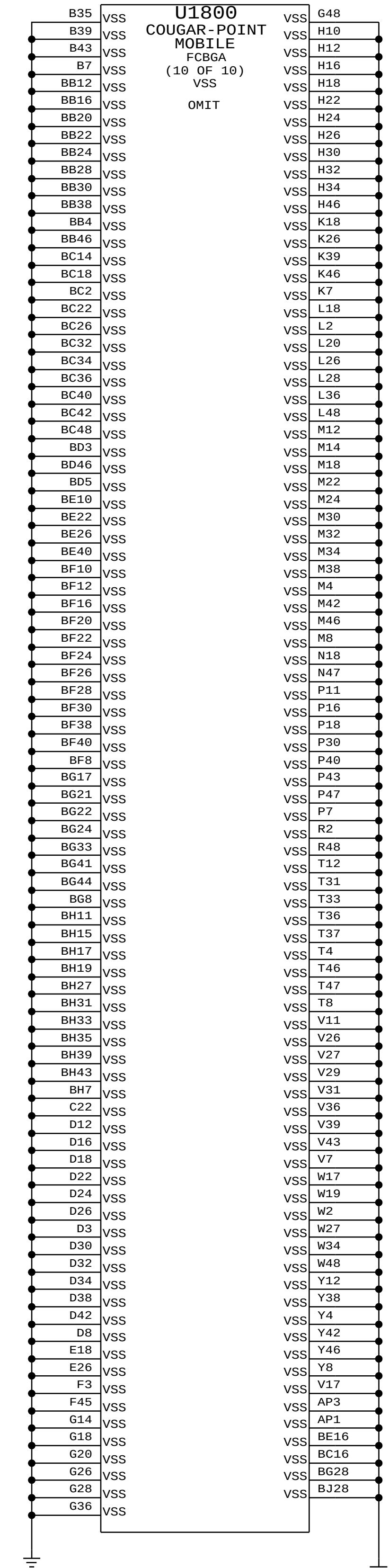

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PCH GROUNDS

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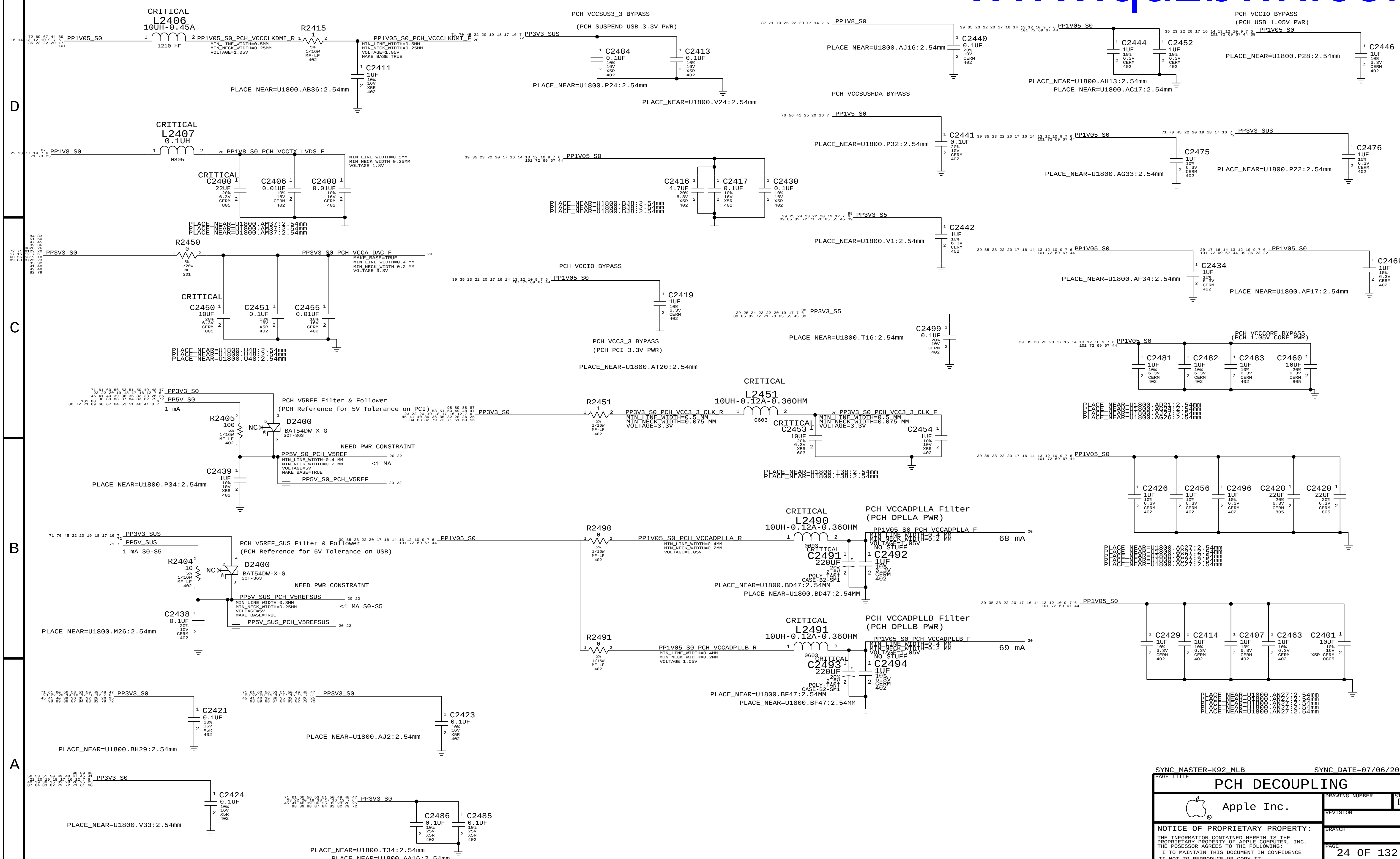

SYNC_MASTER=K92_MLB SYNC_DATE=07/06/2010

PAGE TITLE

PCH DECOUPLING

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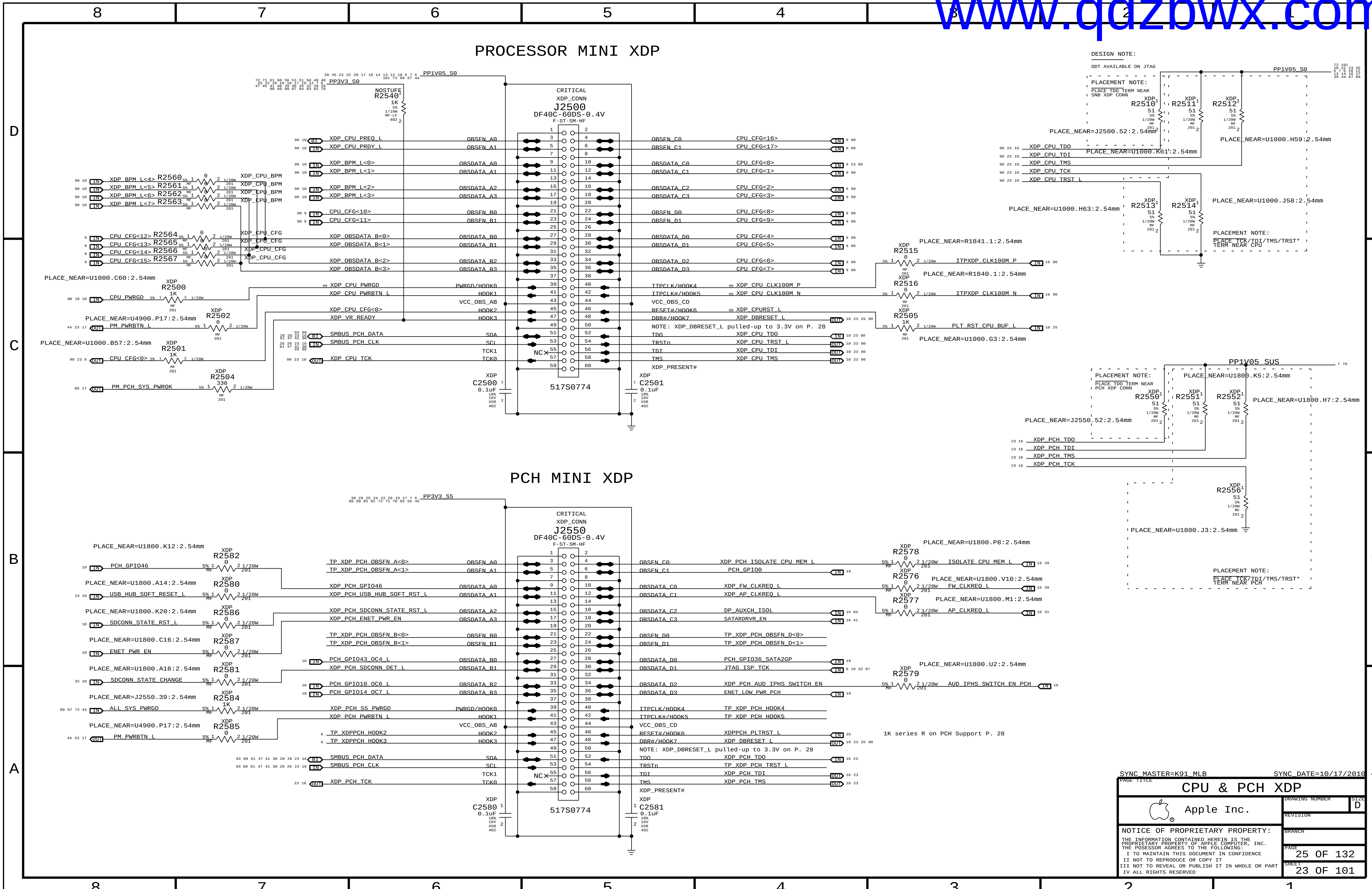
PROCESSOR MINI XDP
PCH MINI XDP
CRITICAL
XDP_CONN
J2500
DF40C-60DS-0.4V
F-ST-SM-HF
517S0774
J2550
PP1V05_S0
PP3V3_S0
PP3V3_S5
PP1V05_SUS
NOSTUFF
R2540
DESIGN NOTE:
ODT AVAILABLE ON JTAG
PLACEMENT NOTE:
PLACE TDO TERM NEAR SNB XDP CONN
PLACE TCK/TDI/TMS/TRST* TERM NEAR CPU
PLACE TDO TERM NEAR PCH XDP CONN
PLACE TCK/TDI/TMS/TRST* TERM NEAR PCH
NOTE: XDP_DBRESET_L pulled-up to 3.3V on P. 28
1K series R on PCH Support P. 28
XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
XDP_CPU_PWRGD
XDP_CPU_PWRBTN_L
XDP_VR_READY
XDP_CPU_TCK
XDP_CPU_TDO
XDP_CPU_TDI
XDP_CPU_TMS
XDP_CPU_TRST_L
XDP_DBRESET_L
XDP_CPURST_L
XDP_CPU_CLK100M_P
XDP_CPU_CLK100M_N
ITPXDP_CLK100M_P
ITPXDP_CLK100M_N
PLT_RST_CPU_BUF_L
SMBUS_PCH_DATA
SMBUS_PCH_CLK
XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_PCH_TCK
XDP_PCH_TRST_L
SYNC_MASTER=K91_MLB
SYNC_DATE=10/17/2010
PAGE TITLE
CPU & PCH XDP
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DRAWING NUMBER
SIZE
D
REVISION
BRANCH
PAGE
25 OF 132
SHEET
23 OF 101
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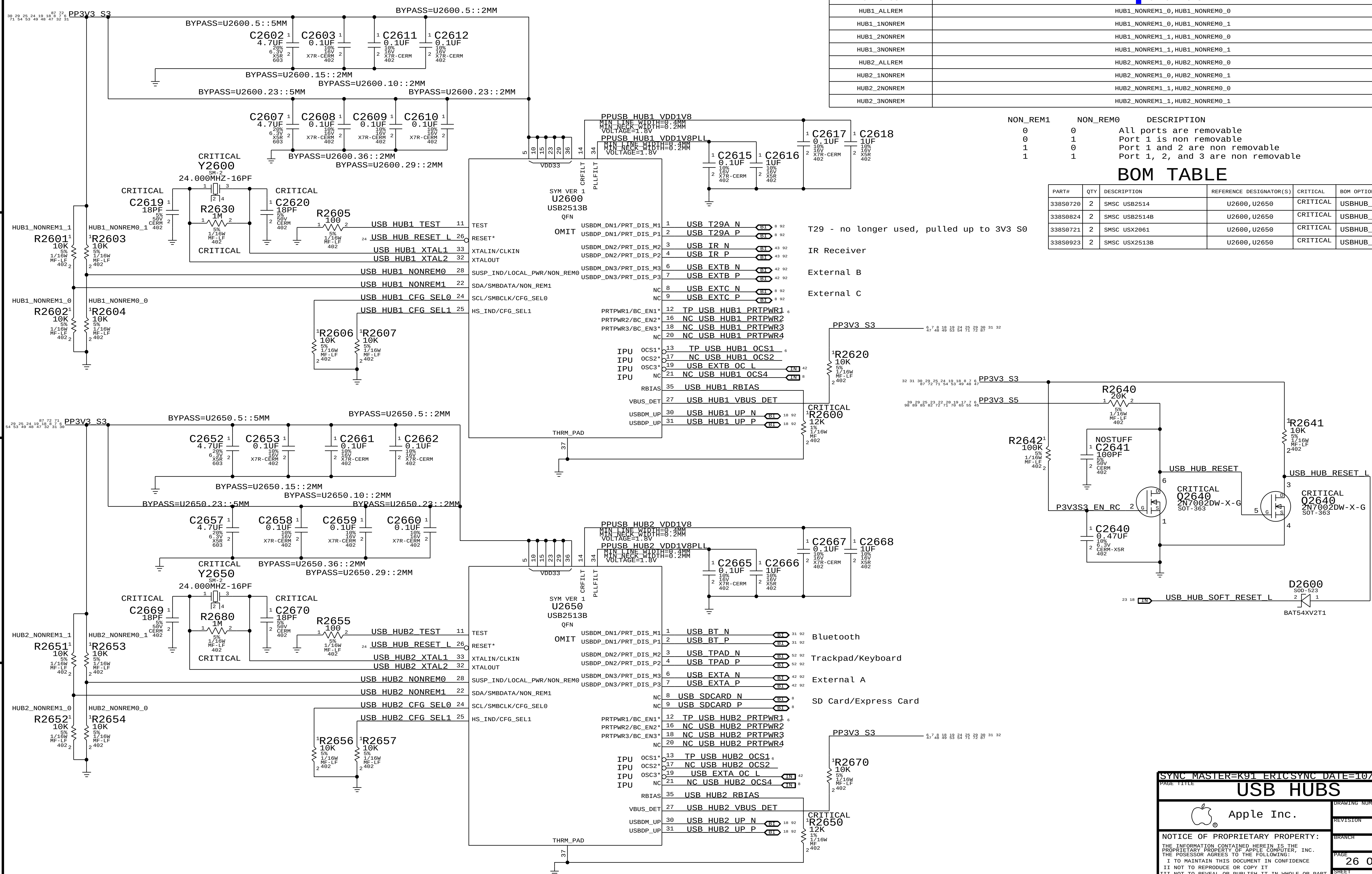
BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600,U2650	CRITICAL	USBHUB_2061
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B



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USB HUBS

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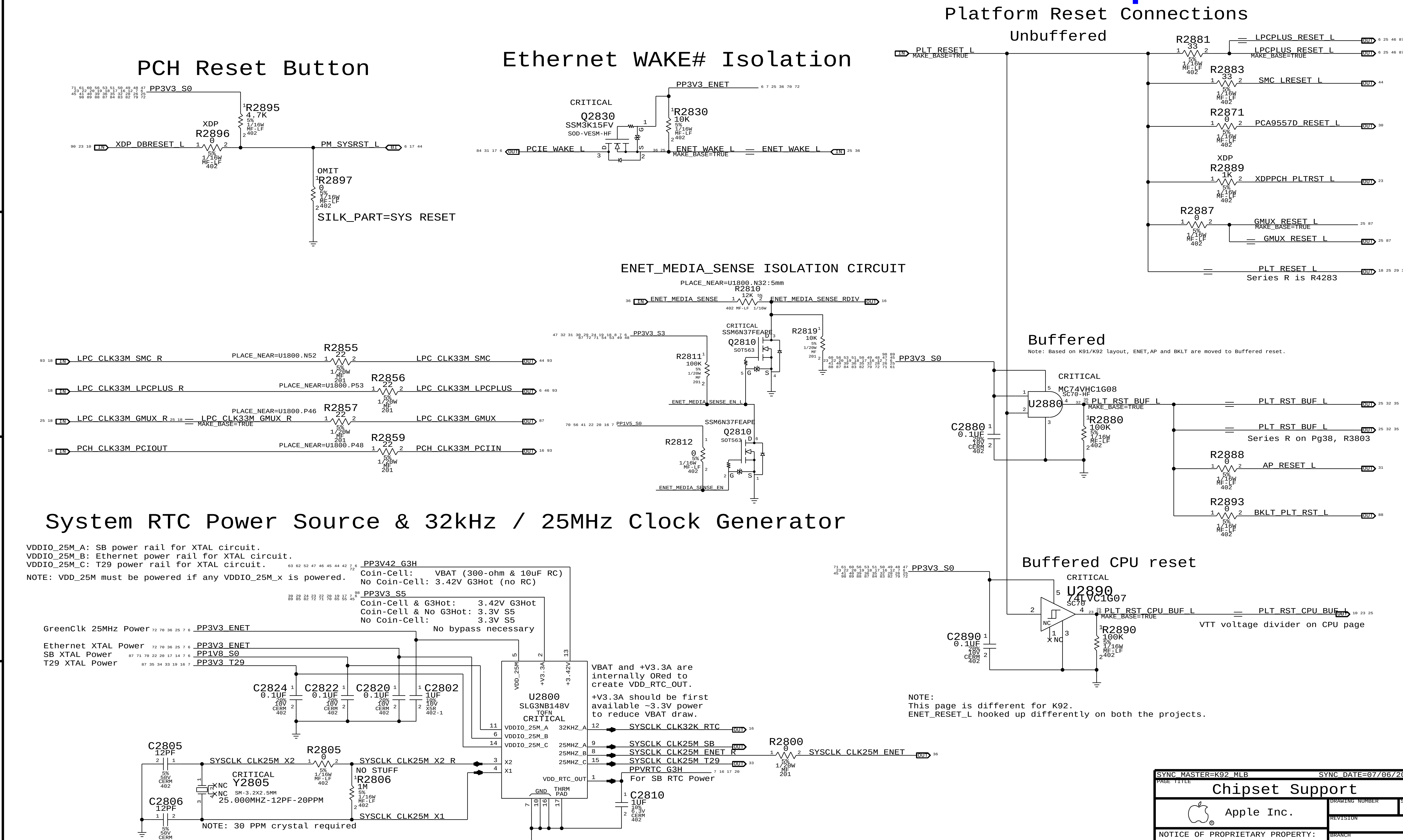

SYNC_MASTER=K92_MLB SYNC_DATE=07/06/2010

PAGE TITLE

Chipset Support

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PAGE 28 OF 132

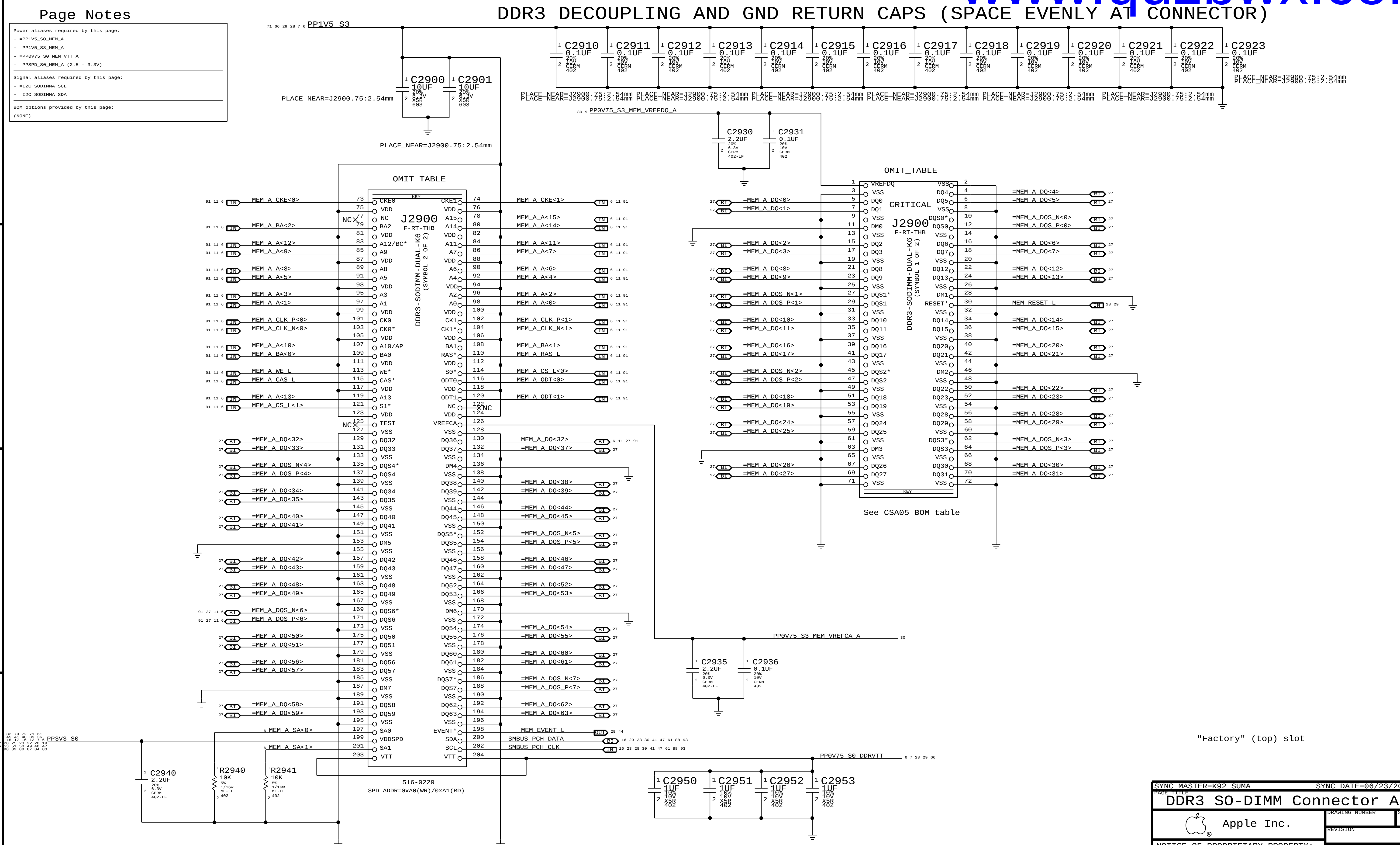
SHEET 25 OF 101

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)



SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE

DDR3 SO-DIMM Connector A

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8 7 6 5 4 3 2 1

D C B A

CPU CHANNEL A DQS 0 -> DIMM A DQS 0

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_A_DQS_N<0>	=MEM_A_DQS_N<0>	26
91 11 6	MEM_A_DQS_P<0>	=MEM_A_DQS_P<0>	26
91 11 6	MEM_A_DQ<7>	=MEM_A_DQ<3>	26
91 11 6	MEM_A_DQ<6>	=MEM_A_DQ<6>	26
91 11 6	MEM_A_DQ<5>	=MEM_A_DQ<5>	26
91 11 6	MEM_A_DQ<4>	=MEM_A_DQ<4>	26
91 11 6	MEM_A_DQ<3>	=MEM_A_DQ<7>	26
91 11 6	MEM_A_DQ<2>	=MEM_A_DQ<0>	26
91 11 6	MEM_A_DQ<1>	=MEM_A_DQ<1>	26
91 11 6	MEM_A_DQ<0>	=MEM_A_DQ<2>	26

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_B_DQS_N<0>	=MEM_B_DQS_N<0>	28
91 11 6	MEM_B_DQS_P<0>	=MEM_B_DQS_P<0>	28
91 11 6	MEM_B_DQ<7>	=MEM_B_DQ<6>	28
91 11 6	MEM_B_DQ<6>	=MEM_B_DQ<3>	28
91 11 6	MEM_B_DQ<5>	=MEM_B_DQ<5>	28
91 11 6	MEM_B_DQ<4>	=MEM_B_DQ<4>	28
91 11 6	MEM_B_DQ<3>	=MEM_B_DQ<1>	28
91 11 6	MEM_B_DQ<2>	=MEM_B_DQ<7>	28
91 11 6	MEM_B_DQ<1>	=MEM_B_DQ<2>	28
91 11 6	MEM_B_DQ<0>	=MEM_B_DQ<0>	28

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_A_DQS_N<1>	=MEM_A_DQS_N<1>	26
91 11 6	MEM_A_DQS_P<1>	=MEM_A_DQS_P<1>	26
91 11 6	MEM_A_DQ<15>	=MEM_A_DQ<15>	26
91 11 6	MEM_A_DQ<14>	=MEM_A_DQ<14>	26
91 11 6	MEM_A_DQ<13>	=MEM_A_DQ<12>	26
91 11 6	MEM_A_DQ<12>	=MEM_A_DQ<13>	26
91 11 6	MEM_A_DQ<11>	=MEM_A_DQ<10>	26
91 11 6	MEM_A_DQ<10>	=MEM_A_DQ<11>	26
91 11 6	MEM_A_DQ<9>	=MEM_A_DQ<9>	26
91 11 6	MEM_A_DQ<8>	=MEM_A_DQ<8>	26

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_B_DQS_N<1>	=MEM_B_DQS_N<1>	28
91 11 6	MEM_B_DQS_P<1>	=MEM_B_DQS_P<1>	28
91 11 6	MEM_B_DQ<15>	=MEM_B_DQ<15>	28
91 11 6	MEM_B_DQ<14>	=MEM_B_DQ<14>	28
91 11 6	MEM_B_DQ<13>	=MEM_B_DQ<13>	28
91 11 6	MEM_B_DQ<12>	=MEM_B_DQ<12>	28
91 11 6	MEM_B_DQ<11>	=MEM_B_DQ<11>	28
91 11 6	MEM_B_DQ<10>	=MEM_B_DQ<10>	28
91 11 6	MEM_B_DQ<9>	=MEM_B_DQ<9>	28
91 11 6	MEM_B_DQ<8>	=MEM_B_DQ<8>	28

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_A_DQS_N<2>	=MEM_A_DQS_N<2>	26
91 11 6	MEM_A_DQS_P<2>	=MEM_A_DQS_P<2>	26
91 11 6	MEM_A_DQ<23>	=MEM_A_DQ<23>	26
91 11 6	MEM_A_DQ<22>	=MEM_A_DQ<22>	26
91 11 6	MEM_A_DQ<21>	=MEM_A_DQ<17>	26
91 11 6	MEM_A_DQ<20>	=MEM_A_DQ<20>	26
91 11 6	MEM_A_DQ<19>	=MEM_A_DQ<19>	26
91 11 6	MEM_A_DQ<18>	=MEM_A_DQ<18>	26
91 11 6	MEM_A_DQ<17>	=MEM_A_DQ<16>	26
91 11 6	MEM_A_DQ<16>	=MEM_A_DQ<21>	26

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_B_DQS_N<2>	=MEM_B_DQS_N<2>	28
91 11 6	MEM_B_DQS_P<2>	=MEM_B_DQS_P<2>	28
91 11 6	MEM_B_DQ<23>	=MEM_B_DQ<23>	28
91 11 6	MEM_B_DQ<22>	=MEM_B_DQ<22>	28
91 11 6	MEM_B_DQ<21>	=MEM_B_DQ<21>	28
91 11 6	MEM_B_DQ<20>	=MEM_B_DQ<20>	28
91 11 6	MEM_B_DQ<19>	=MEM_B_DQ<19>	28
91 11 6	MEM_B_DQ<18>	=MEM_B_DQ<18>	28
91 11 6	MEM_B_DQ<17>	=MEM_B_DQ<17>	28
91 11 6	MEM_B_DQ<16>	=MEM_B_DQ<16>	28

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_A_DQS_N<3>	=MEM_A_DQS_N<3>	26
91 11 6	MEM_A_DQS_P<3>	=MEM_A_DQS_P<3>	26
91 11 6	MEM_A_DQ<31>	=MEM_A_DQ<31>	26
91 11 6	MEM_A_DQ<30>	=MEM_A_DQ<30>	26
91 11 6	MEM_A_DQ<29>	=MEM_A_DQ<29>	26
91 11 6	MEM_A_DQ<28>	=MEM_A_DQ<28>	26
91 11 6	MEM_A_DQ<27>	=MEM_A_DQ<27>	26
91 11 6	MEM_A_DQ<26>	=MEM_A_DQ<26>	26
91 11 6	MEM_A_DQ<25>	=MEM_A_DQ<25>	26
91 11 6	MEM_A_DQ<24>	=MEM_A_DQ<24>	26

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_B_DQS_N<3>	=MEM_B_DQS_N<3>	28
91 11 6	MEM_B_DQS_P<3>	=MEM_B_DQS_P<3>	28
91 11 6	MEM_B_DQ<31>	=MEM_B_DQ<31>	28
91 11 6	MEM_B_DQ<30>	=MEM_B_DQ<30>	28
91 11 6	MEM_B_DQ<29>	=MEM_B_DQ<29>	28
91 11 6	MEM_B_DQ<28>	=MEM_B_DQ<28>	28
91 11 6	MEM_B_DQ<27>	=MEM_B_DQ<27>	28
91 11 6	MEM_B_DQ<26>	=MEM_B_DQ<26>	28
91 11 6	MEM_B_DQ<25>	=MEM_B_DQ<25>	28
91 11 6	MEM_B_DQ<24>	=MEM_B_DQ<24>	28

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_A_DQS_N<4>	=MEM_A_DQS_N<4>	26
91 11 6	MEM_A_DQS_P<4>	=MEM_A_DQS_P<4>	26
91 11 6	MEM_A_DQ<39>	=MEM_A_DQ<38>	26
91 11 6	MEM_A_DQ<38>	=MEM_A_DQ<37>	26
91 11 6	MEM_A_DQ<37>	=MEM_A_DQ<39>	26
91 11 6	MEM_A_DQ<36>	=MEM_A_DQ<33>	26
91 11 6	MEM_A_DQ<35>	=MEM_A_DQ<35>	26
91 11 6	MEM_A_DQ<34>	=MEM_A_DQ<34>	26
91 11 6	MEM_A_DQ<33>	=MEM_A_DQ<32>	26
91 27 26 11 6	MEM_A_DQ<32>	MEM_A_DQ<32>	6 11 26 27 91

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_B_DQS_N<4>	=MEM_B_DQS_N<4>	28
91 11 6	MEM_B_DQS_P<4>	=MEM_B_DQS_P<4>	28
91 11 6	MEM_B_DQ<39>	=MEM_B_DQ<39>	28
91 11 6	MEM_B_DQ<38>	=MEM_B_DQ<38>	28
91 11 6	MEM_B_DQ<37>	=MEM_B_DQ<37>	28
91 11 6	MEM_B_DQ<36>	=MEM_B_DQ<36>	28
91 11 6	MEM_B_DQ<35>	=MEM_B_DQ<35>	28
91 11 6	MEM_B_DQ<34>	=MEM_B_DQ<34>	28
91 11 6	MEM_B_DQ<33>	=MEM_B_DQ<33>	28
27 11 6 91 28	MEM_B_DQ<32>	MEM_B_DQ<32>	6 11 27 28 91

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_A_DQS_N<5>	=MEM_A_DQS_N<5>	26
91 11 6	MEM_A_DQS_P<5>	=MEM_A_DQS_P<5>	26
91 11 6	MEM_A_DQ<47>	=MEM_A_DQ<47>	26
91 11 6	MEM_A_DQ<46>	=MEM_A_DQ<41>	26
91 11 6	MEM_A_DQ<45>	=MEM_A_DQ<43>	26
91 11 6	MEM_A_DQ<44>	=MEM_A_DQ<44>	26
91 11 6	MEM_A_DQ<43>	=MEM_A_DQ<40>	26
91 11 6	MEM_A_DQ<42>	=MEM_A_DQ<46>	26
91 11 6	MEM_A_DQ<41>	=MEM_A_DQ<42>	26
91 11 6	MEM_A_DQ<40>	=MEM_A_DQ<45>	26

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_B_DQS_N<5>	=MEM_B_DQS_N<5>	28
91 11 6	MEM_B_DQS_P<5>	=MEM_B_DQS_P<5>	28
91 11 6	MEM_B_DQ<47>	=MEM_B_DQ<47>	28
91 11 6	MEM_B_DQ<46>	=MEM_B_DQ<46>	28
91 11 6	MEM_B_DQ<45>	=MEM_B_DQ<45>	28
91 11 6	MEM_B_DQ<44>	=MEM_B_DQ<44>	28
91 11 6	MEM_B_DQ<43>	=MEM_B_DQ<43>	28
91 11 6	MEM_B_DQ<42>	=MEM_B_DQ<42>	28
91 11 6	MEM_B_DQ<41>	=MEM_B_DQ<41>	28
91 11 6	MEM_B_DQ<40>	=MEM_B_DQ<40>	28

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

Refs	CPU net	DIMM net	Refs
91 27 26 11 6	MEM_A_DQS_N<6>	MEM_A_DQS_N<6>	6 11 26 27 91
91 27 26 11 6	MEM_A_DQS_P<6>	MEM_A_DQS_P<6>	6 11 26 27 91
91 11 6	MEM_A_DQ<55>	=MEM_A_DQ<49>	26
91 11 6	MEM_A_DQ<54>	=MEM_A_DQ<54>	26
91 11 6	MEM_A_DQ<53>	=MEM_A_DQ<55>	26
91 11 6	MEM_A_DQ<52>	=MEM_A_DQ<52>	26
91 11 6	MEM_A_DQ<51>	=MEM_A_DQ<51>	26
91 11 6	MEM_A_DQ<50>	=MEM_A_DQ<50>	26
91 11 6	MEM_A_DQ<49>	=MEM_A_DQ<53>	26
91 11 6	MEM_A_DQ<48>	=MEM_A_DQ<48>	26

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

Refs	CPU net	DIMM net	Refs
27 11 6 91 28	MEM_B_DQS_N<6>	MEM_B_DQS_N<6>	6 11 27 28 91
27 11 6 91 28	MEM_B_DQS_P<6>	MEM_B_DQS_P<6>	6 11 27 28 91
91 11 6	MEM_B_DQ<55>	=MEM_B_DQ<55>	28
91 11 6	MEM_B_DQ<54>	=MEM_B_DQ<54>	28
91 11 6	MEM_B_DQ<53>	=MEM_B_DQ<53>	28
91 11 6	MEM_B_DQ<52>	=MEM_B_DQ<52>	28
91 11 6	MEM_B_DQ<51>	=MEM_B_DQ<51>	28
91 11 6	MEM_B_DQ<50>	=MEM_B_DQ<50>	28
91 11 6	MEM_B_DQ<49>	=MEM_B_DQ<49>	28
91 11 6	MEM_B_DQ<48>	=MEM_B_DQ<48>	28

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_A_DQS_N<7>	=MEM_A_DQS_N<7>	26
91 11 6	MEM_A_DQS_P<7>	=MEM_A_DQS_P<7>	26
91 11 6	MEM_A_DQ<63>	=MEM_A_DQ<59>	26
91 11 6	MEM_A_DQ<62>	=MEM_A_DQ<58>	26
91 11 6	MEM_A_DQ<61>	=MEM_A_DQ<56>	26
91 11 6	MEM_A_DQ<60>	=MEM_A_DQ<61>	26
91 11 6	MEM_A_DQ<59>	=MEM_A_DQ<63>	26
91 11 6	MEM_A_DQ<58>	=MEM_A_DQ<62>	26
91 11 6	MEM_A_DQ<57>	=MEM_A_DQ<57>	26
91 11 6	MEM_A_DQ<56>	=MEM_A_DQ<60>	26

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

Refs	CPU net	DIMM net	Refs
91 11 6	MEM_B_DQS_N<7>	=MEM_B_DQS_N<7>	28
91 11 6	MEM_B_DQS_P<7>	=MEM_B_DQS_P<7>	28
91 11 6	MEM_B_DQ<63>	=MEM_B_DQ<63>	28
91 11 6	MEM_B_DQ<62>	=MEM_B_DQ<62>	28
91 11 6	MEM_B_DQ<61>	=MEM_B_DQ<61>	28
91 11 6	MEM_B_DQ<60>	=MEM_B_DQ<60>	28
91 11 6	MEM_B_DQ<59>	=MEM_B_DQ<59>	28
91 11 6	MEM_B_DQ<58>	=MEM_B_DQ<58>	28
91 11 6	MEM_B_DQ<57>	=MEM_B_DQ<57>	28
91 11 6	MEM_B_DQ<56>	=MEM_B_DQ<56>	28

SYNC_MASTER=K92_SUMA SYNC_DATE=05/10/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

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BRANCH

8 7 6 5 4 3 2 1

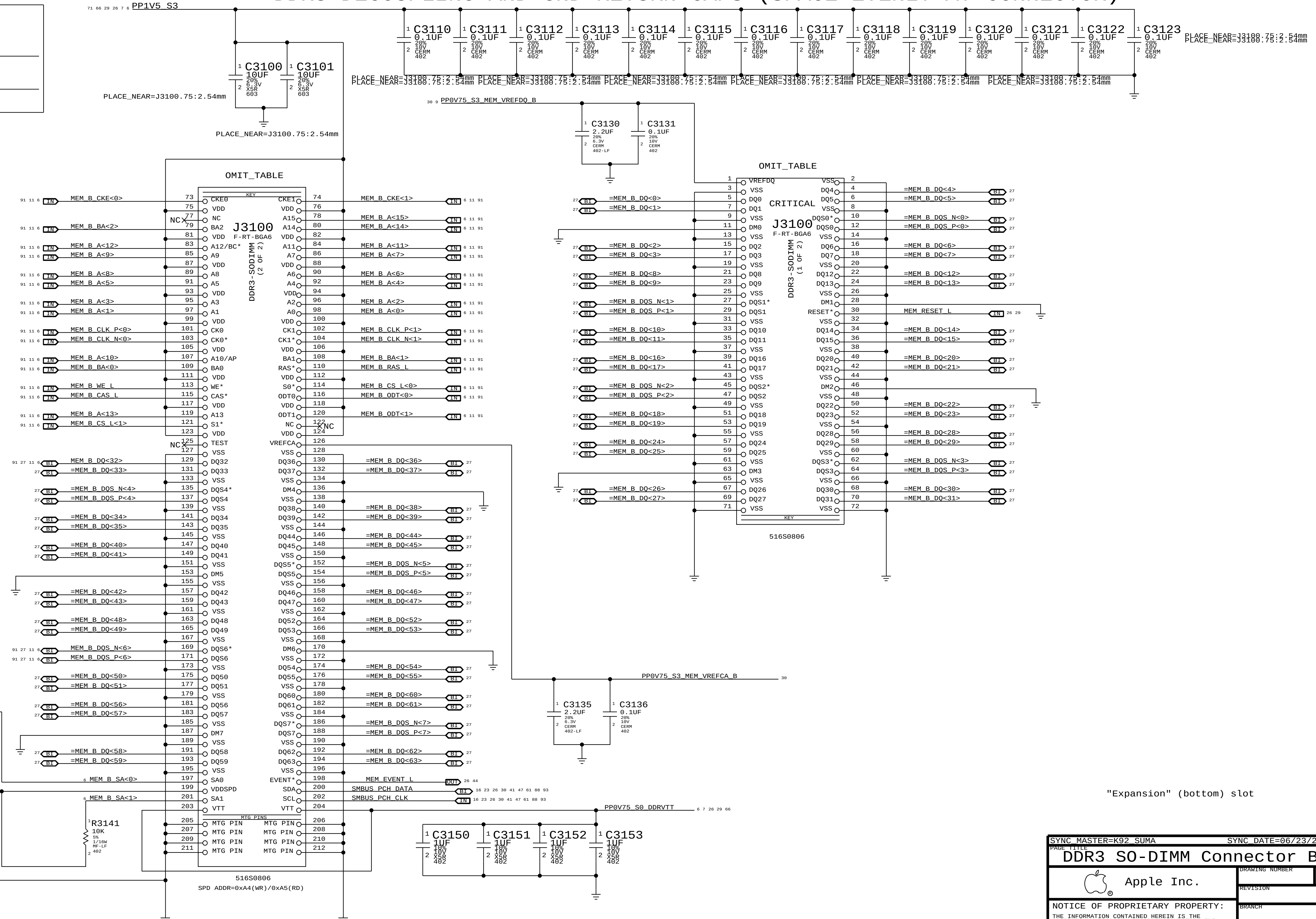
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)



SYNC_MASTER=K92_SUMA SYNC_DATE=06/23/2010

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

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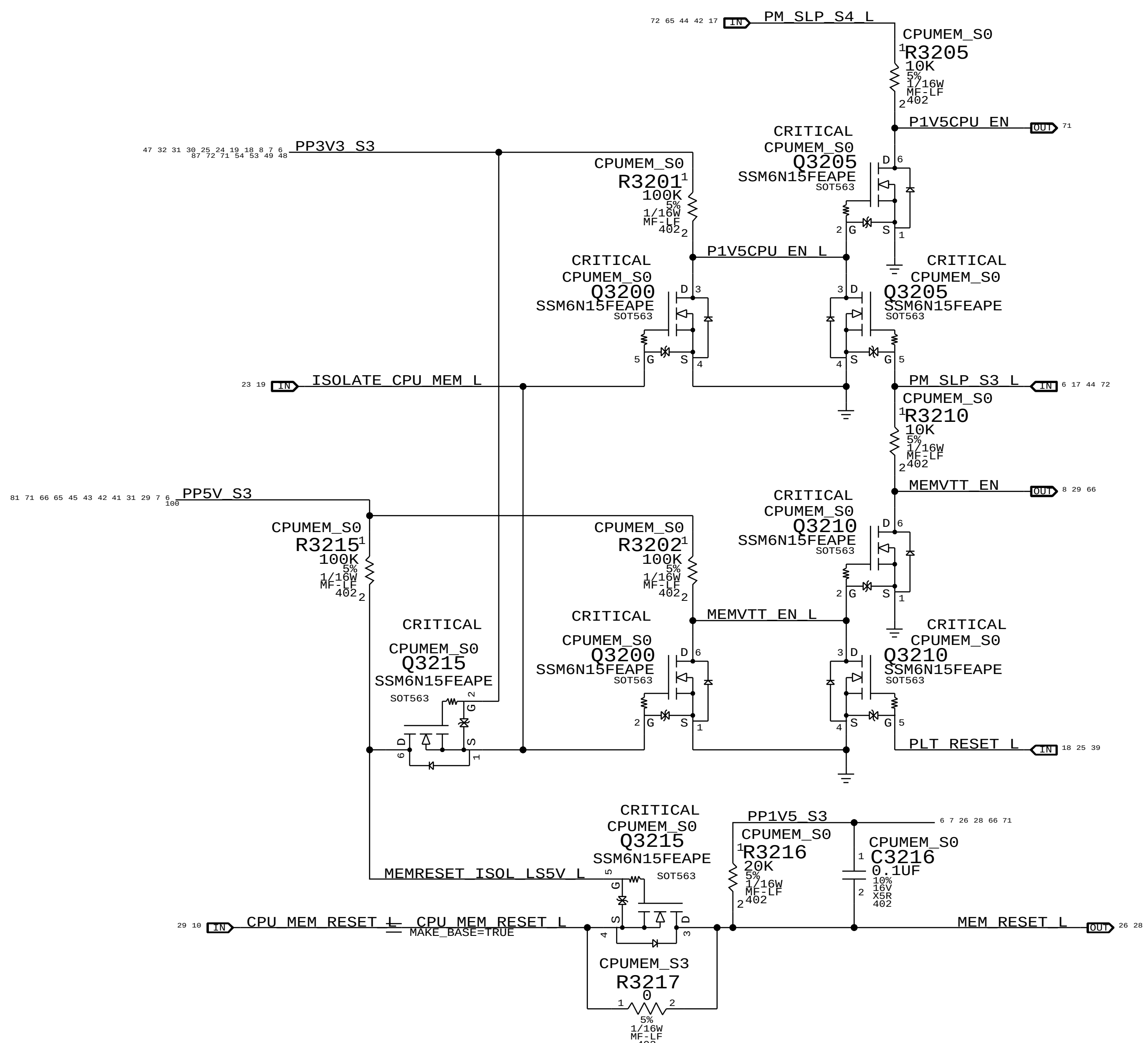
PAGE 31 OF 132

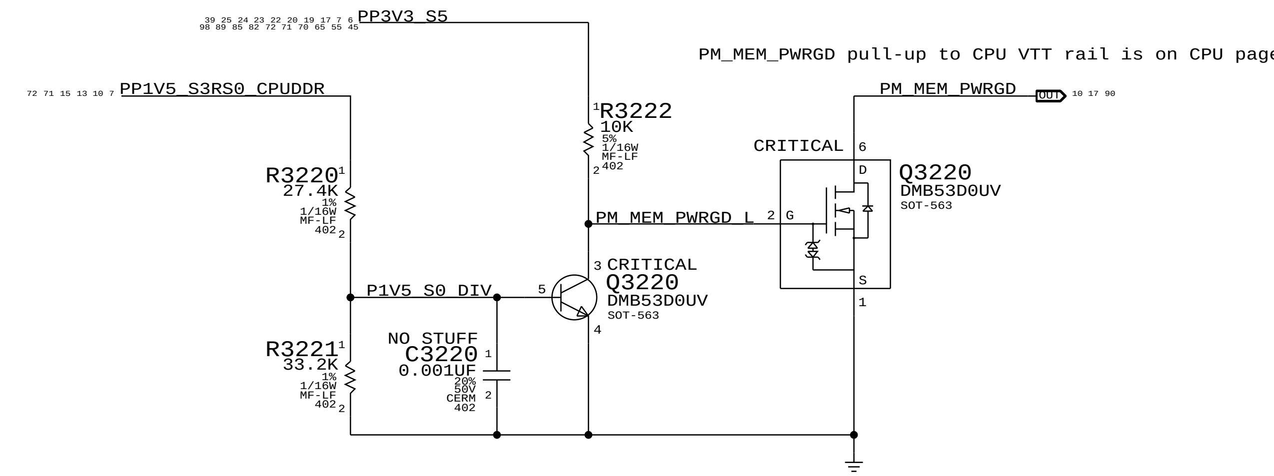
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

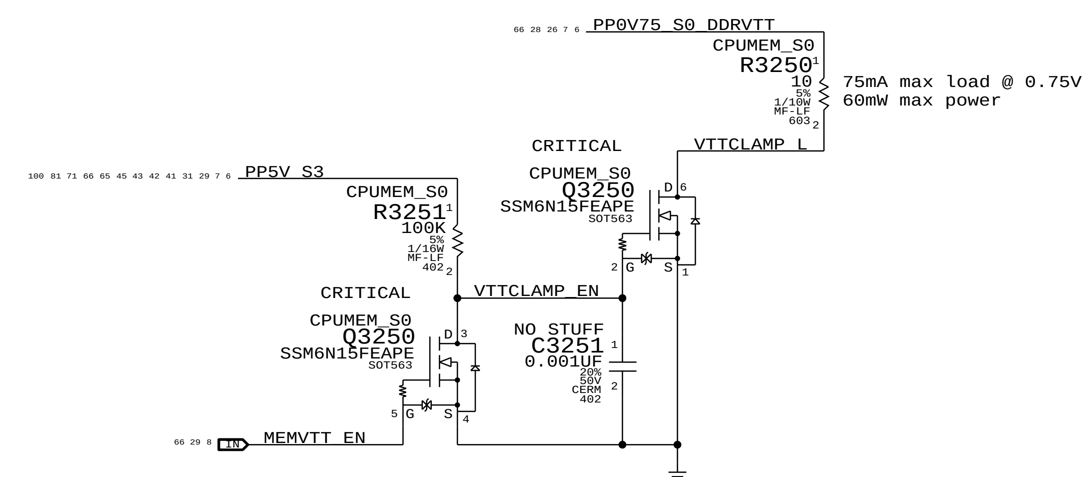


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0 to S3	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
S3 to S0	4	0	0	1	1	X	1	0	1
	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE: CPU Memory S3 Support

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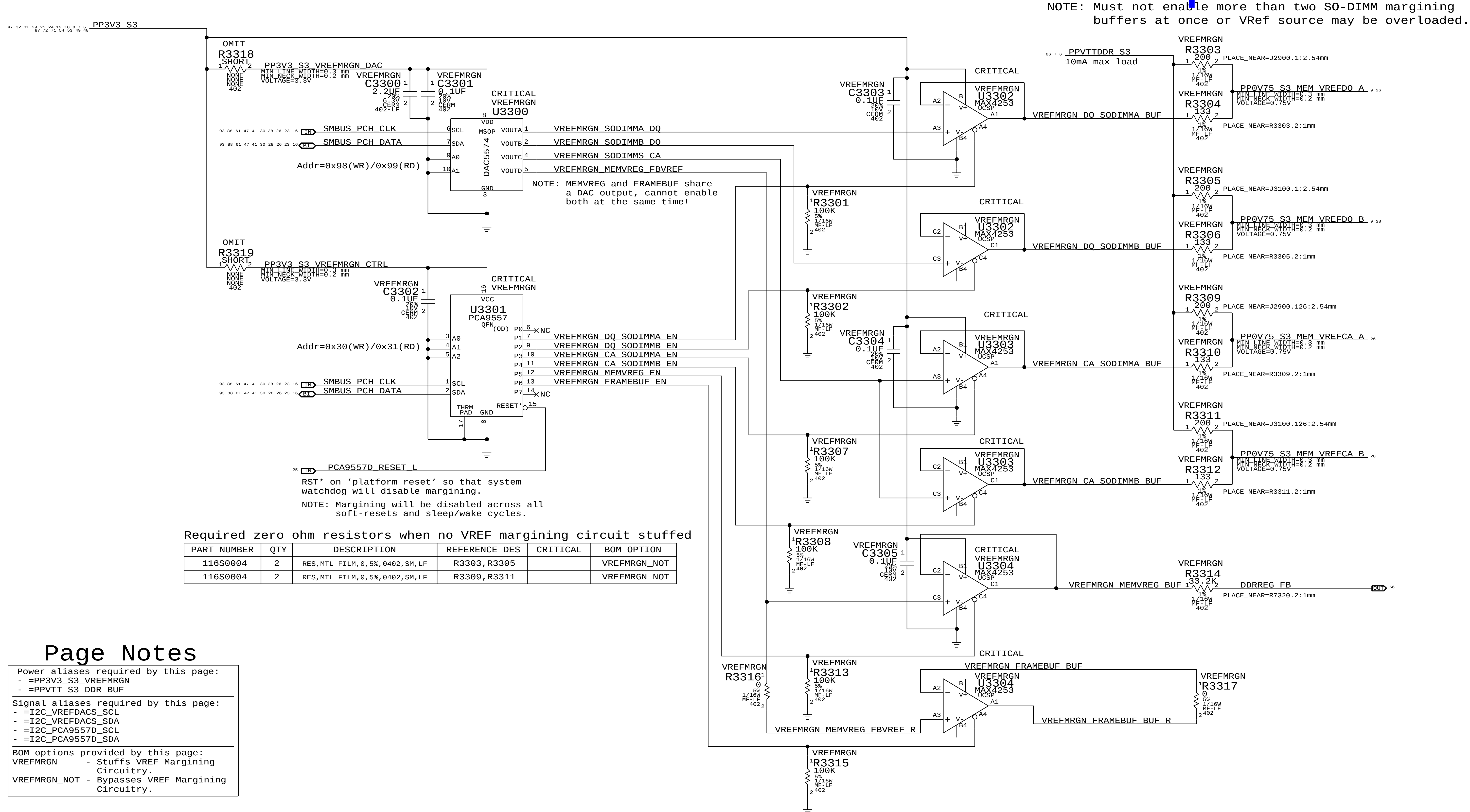

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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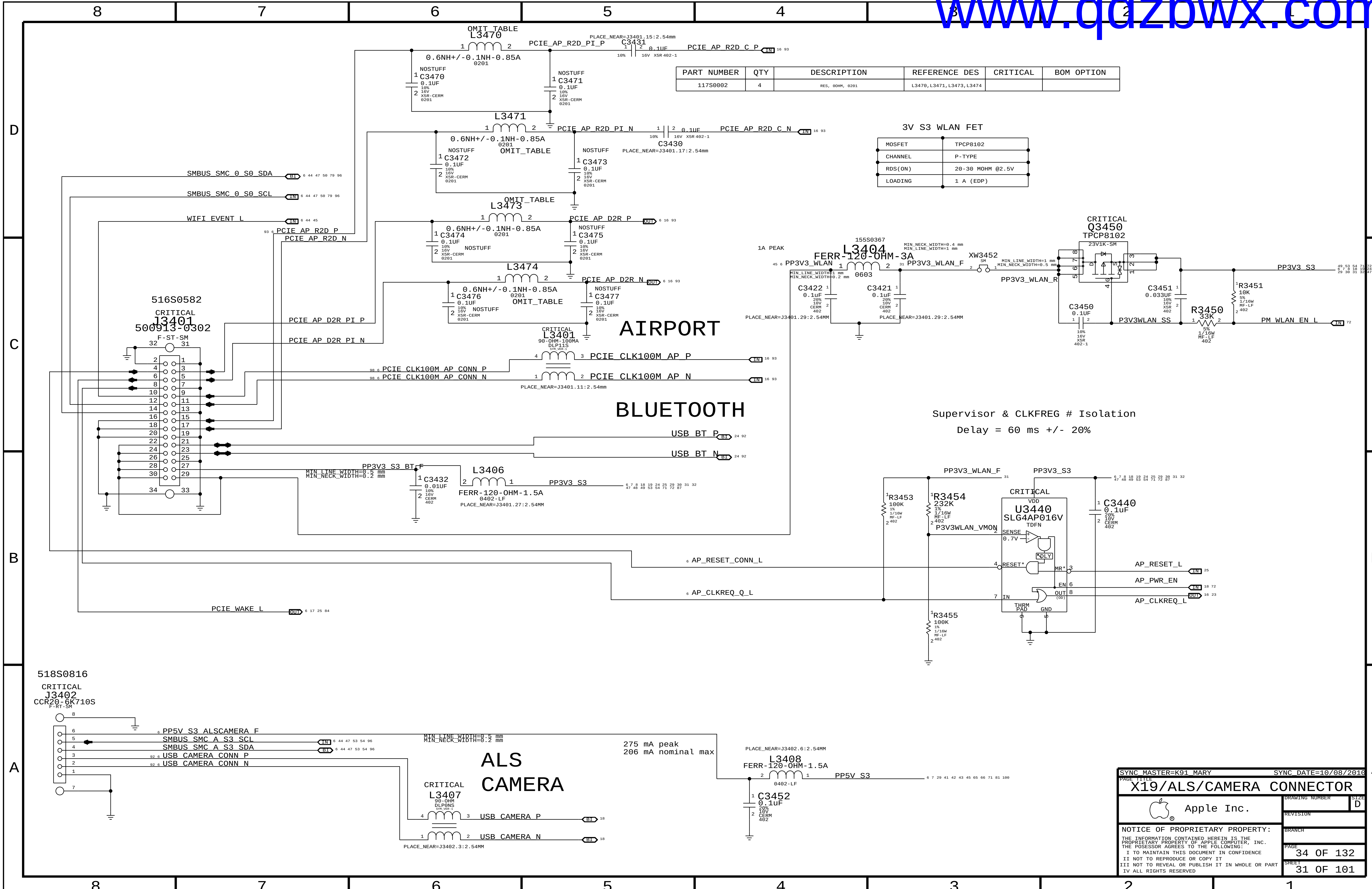

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L3470,L3471,L3473,L3474		

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

SYNC_MASTER=K91_MARY SYNC_DATE=10/08/2010

PAGE TITLE

X19/ALS/CAMERA CONNECTOR

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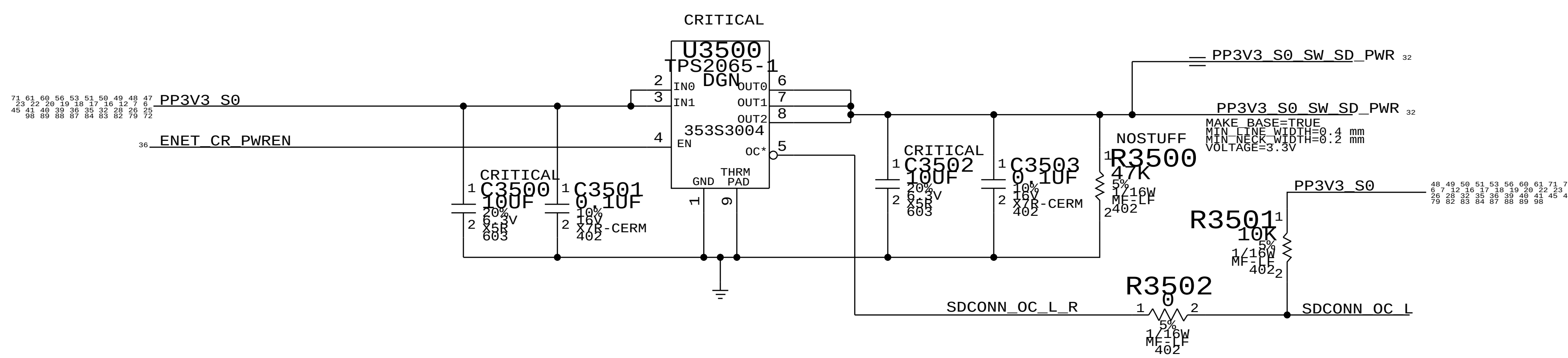
www.qdzbwx.com

SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.

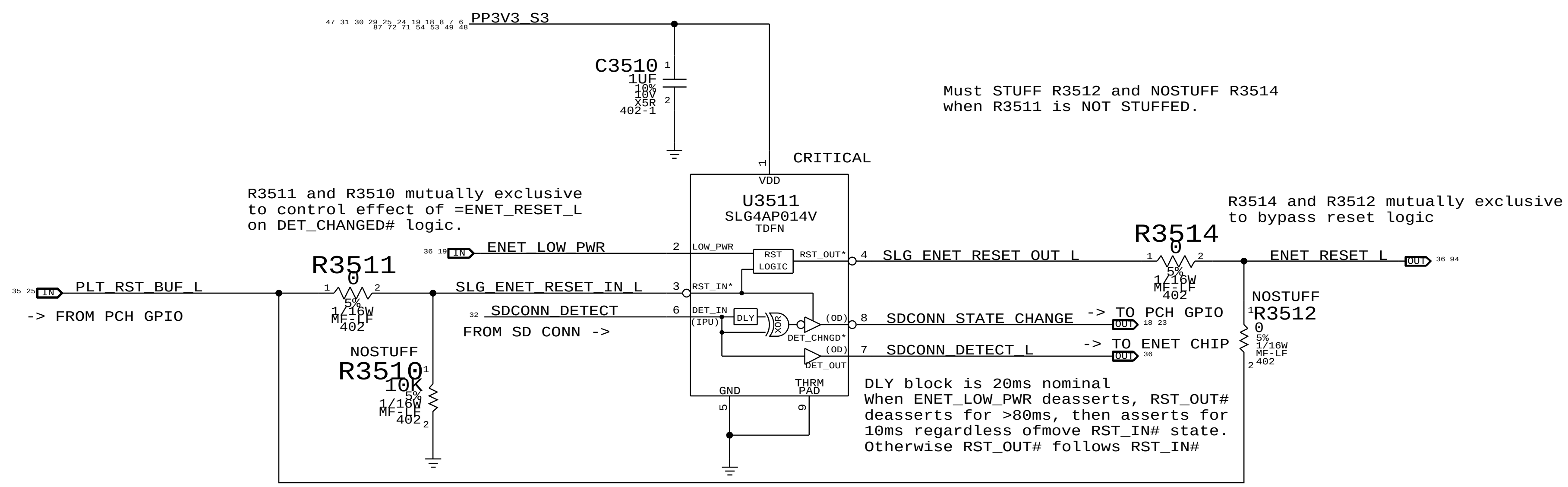


SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO LATCH CIRCUIT

Must STUFF R3512 and NOSTUFF R3514 when R3511 is NOT STUFFED.

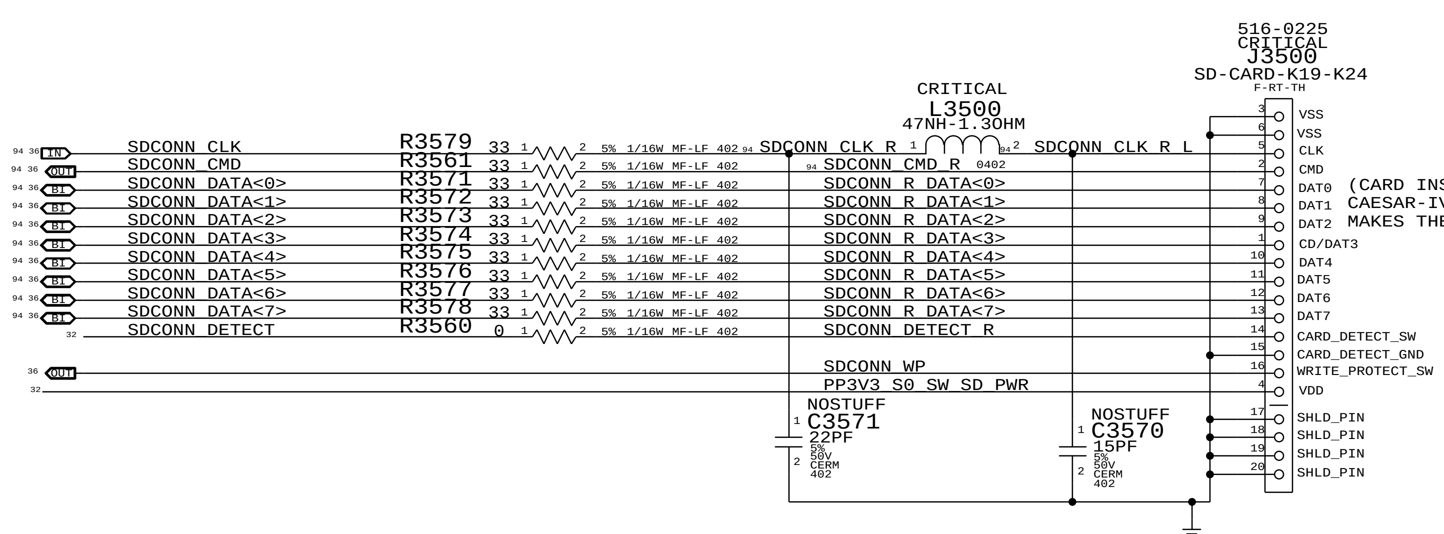
R3511 and R3510 mutually exclusive to control effect of =ENET_RESET_L on DET_CHANGED# logic.

R3514 and R3512 mutually exclusive to bypass reset logic



DLY block is 20ms nominal
When ENET_LOW_PWR deasserts, RST_OUT# deasserts for >80ms, then asserts for 10ms regardless ofmove RST_IN# state.
Otherwise RST_OUT# follows RST_IN#

SD CARD CONNECTOR



(CARD INSERTED = OPEN)
CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG MAKES THE ACTIVE-HIGH CASE UNUSABLE.

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE
SD READER CONNECTOR

Apple Inc.

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SIZE D
REVISION
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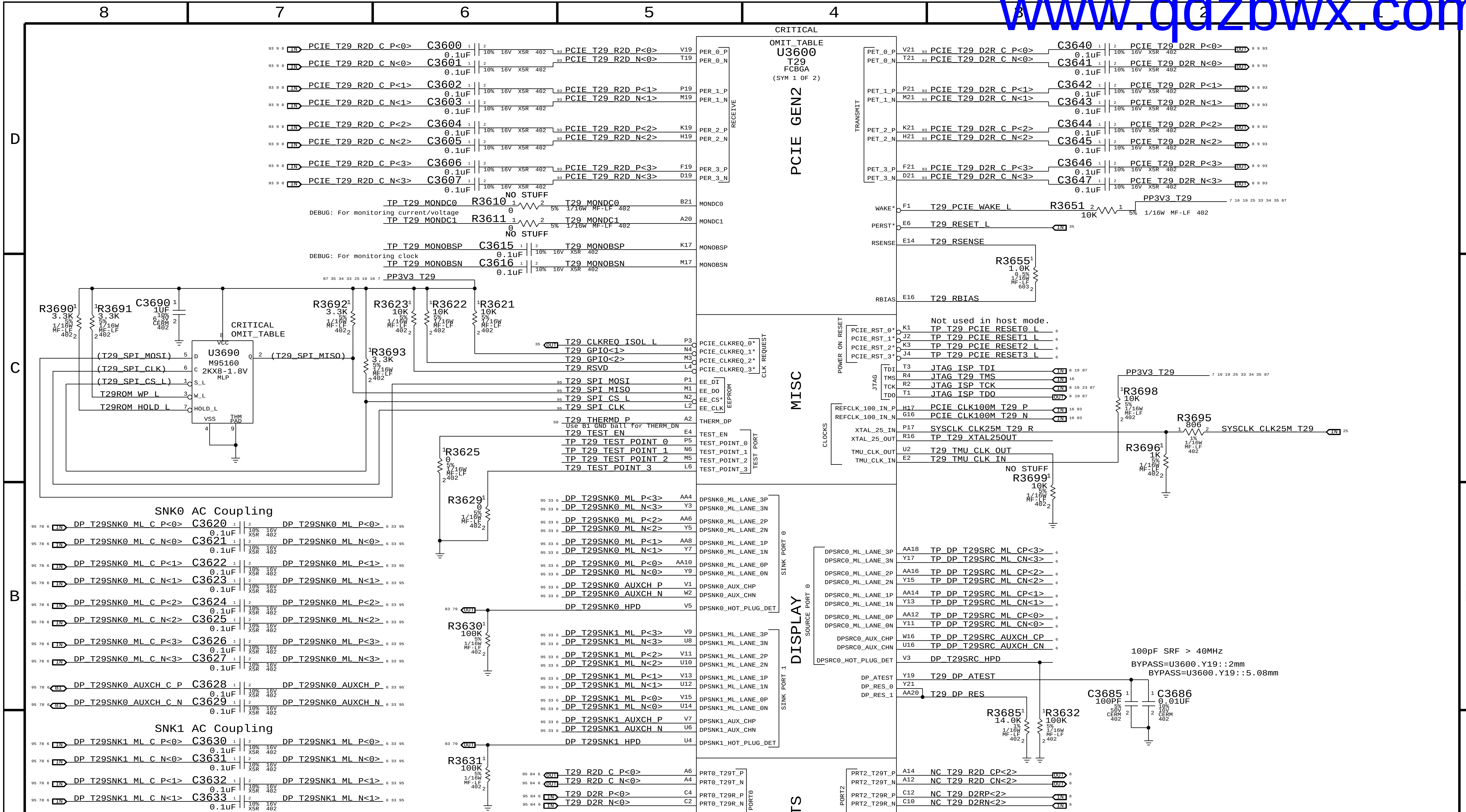

SYNC_MASTER=T29_REF SYNC_DATE=10/12/2010

PAGE TITLE

T29 Host (1 of 2)

Apple Inc.

DRAWING NUMBER

SIZE D

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PAGE 36 OF 132

SHEET 33 OF 101

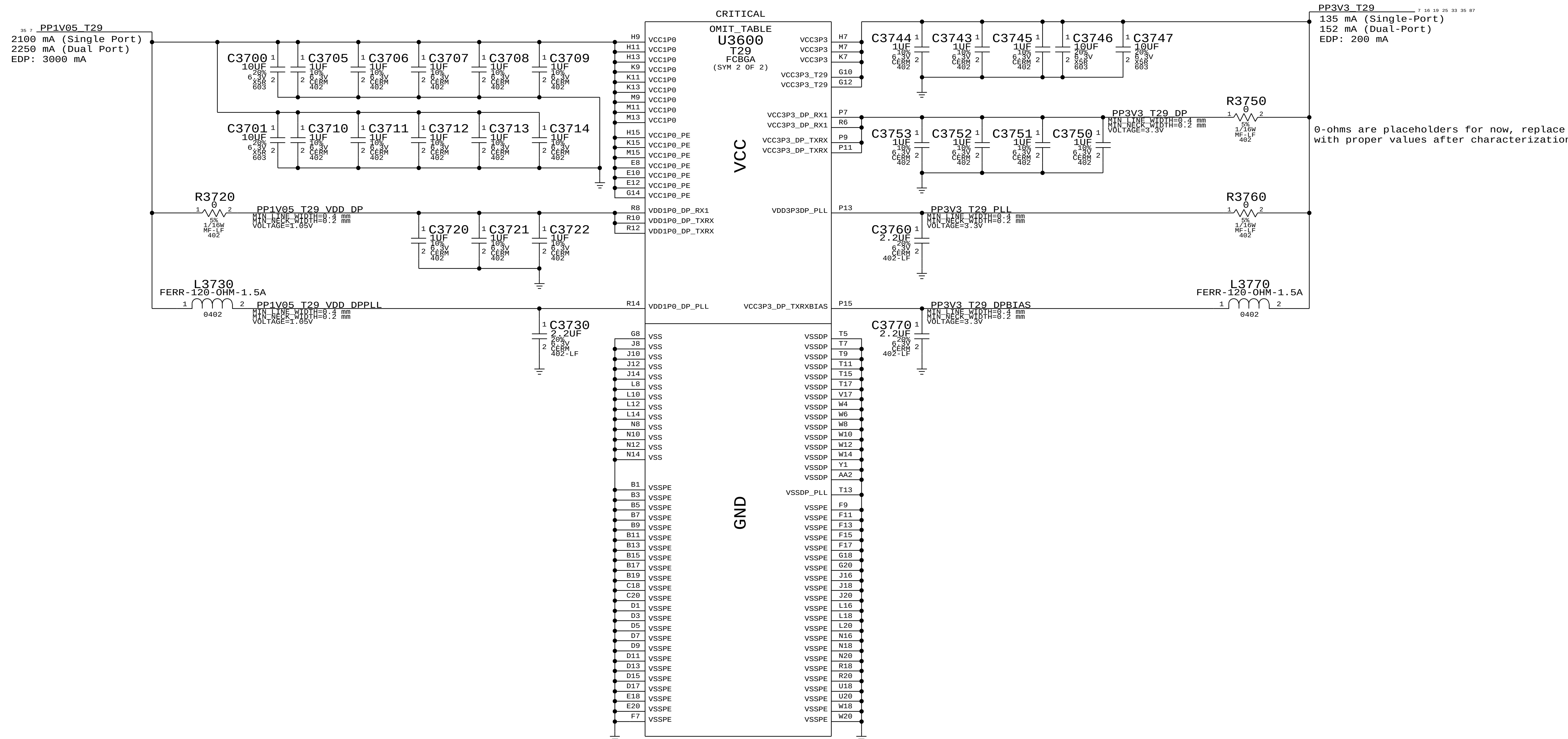
8 7 6 5 4 3 2 1

D

C

B

A



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=10/12/2010

PAGE TITLE

T29 Host (2 of 2)

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

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8 7 6 5 4 3 2 1

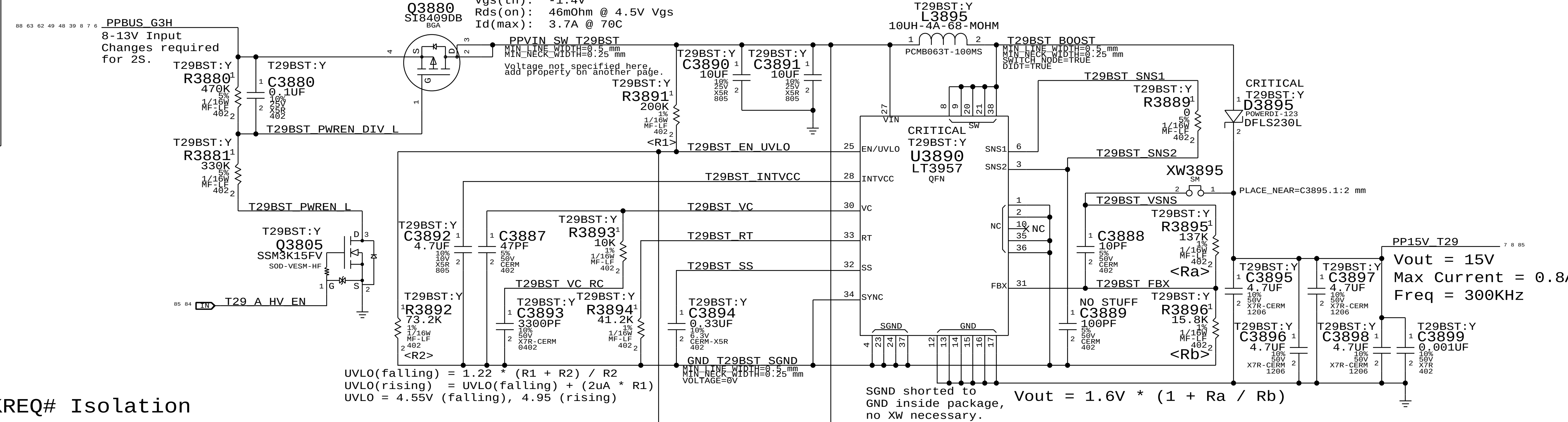
T29 15V Boost Regulator

Page Notes

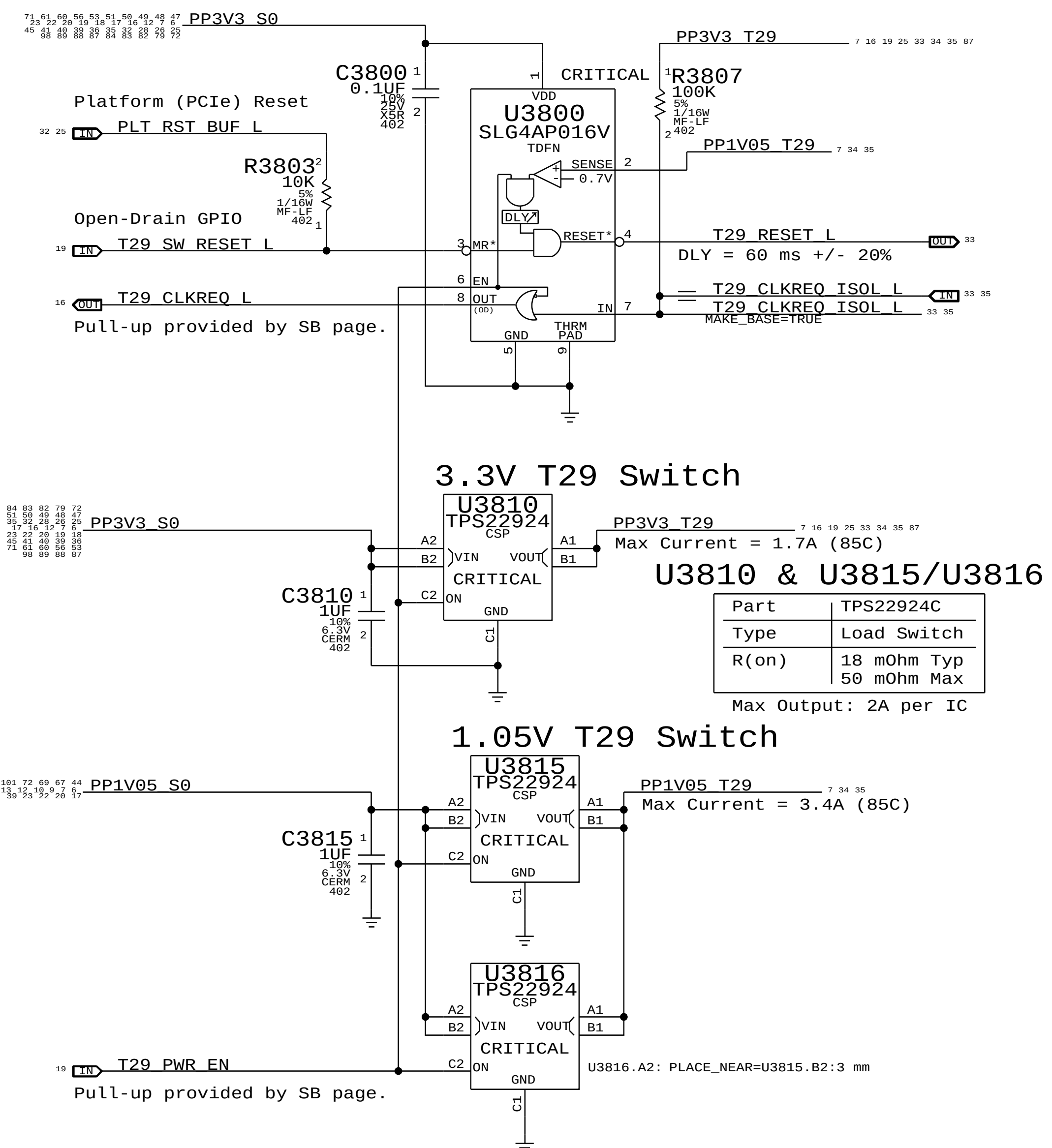
Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.



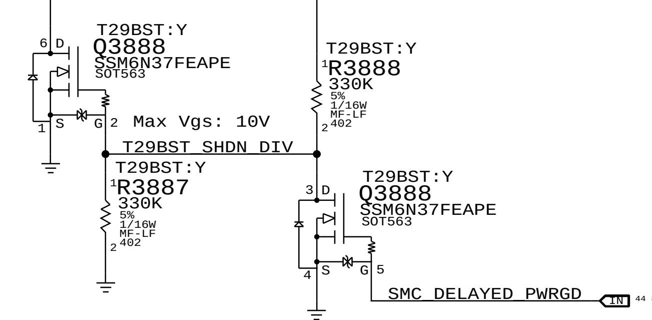
Supervisor & CLKREQ# Isolation



U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC



SYNC_MASTER=T29_REF SYNC_DATE=10/12/2010

PAGE TITLE: T29 Power Support

Apple Inc.

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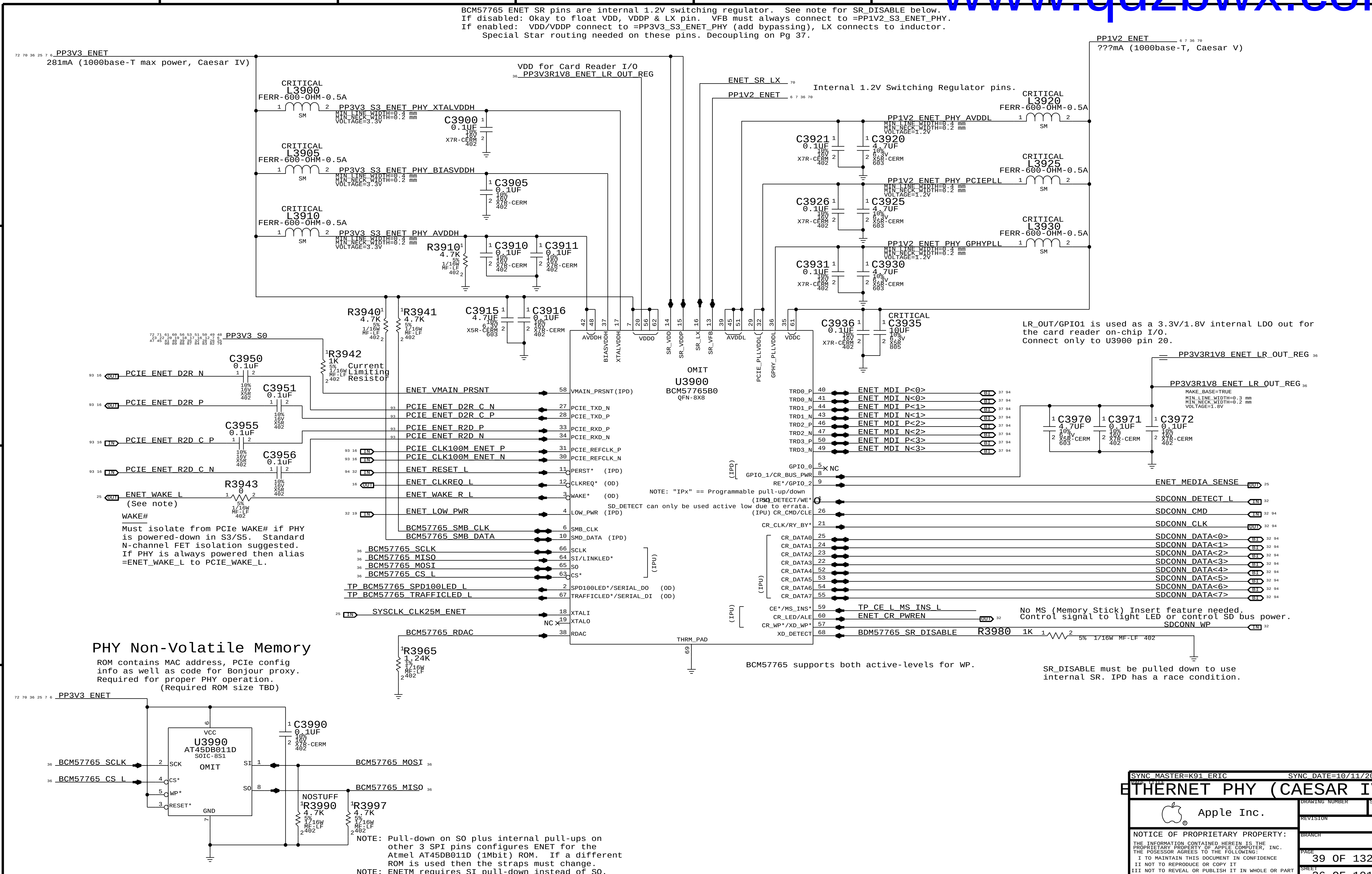


SYNC_MASTER=K91_ERIC SYNC_DATE=10/11/2010

ETHERNET PHY (CAESAR IV)

Apple Inc.

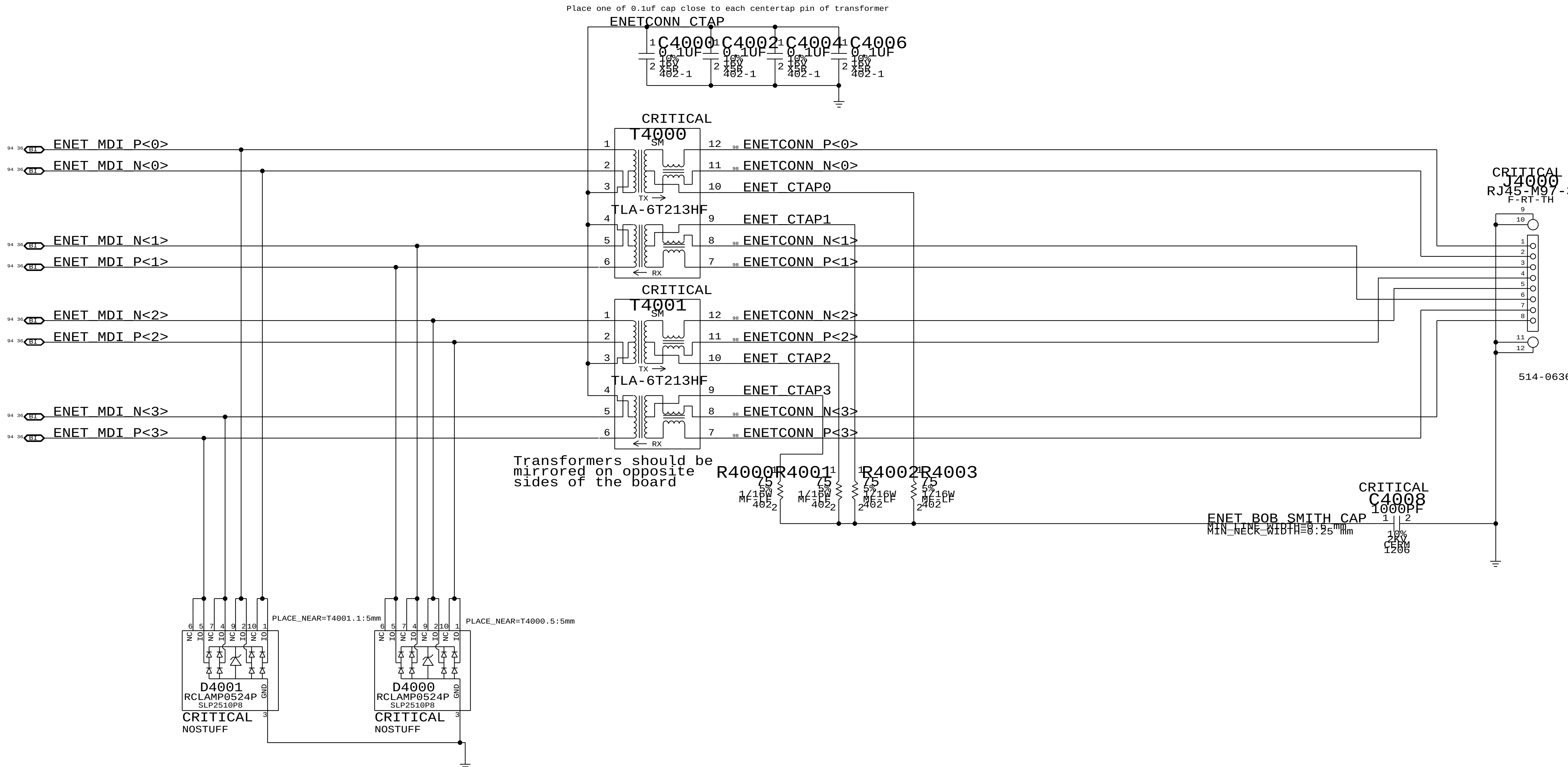
DRAWING NUMBER SIZE D

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_TRINHNI SYNC_DATE=05/26/2010

PAGE TITLE
Ethernet Connector

Apple Inc.

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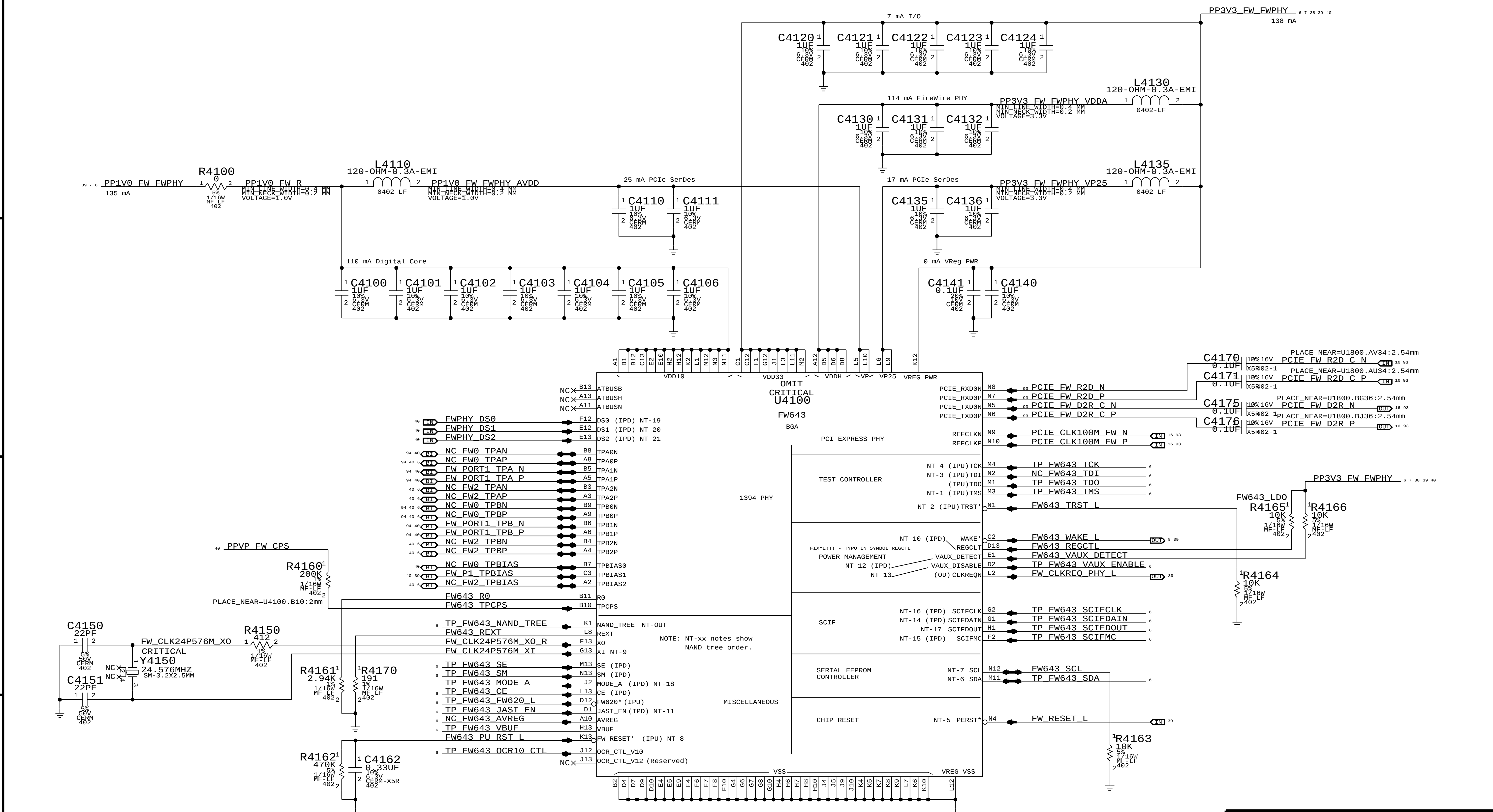


SYNC_MASTER=K18_MLB	SYNC_DATE=04/27/2010

PAGE TITLE

FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER — SIZE D

REVISION

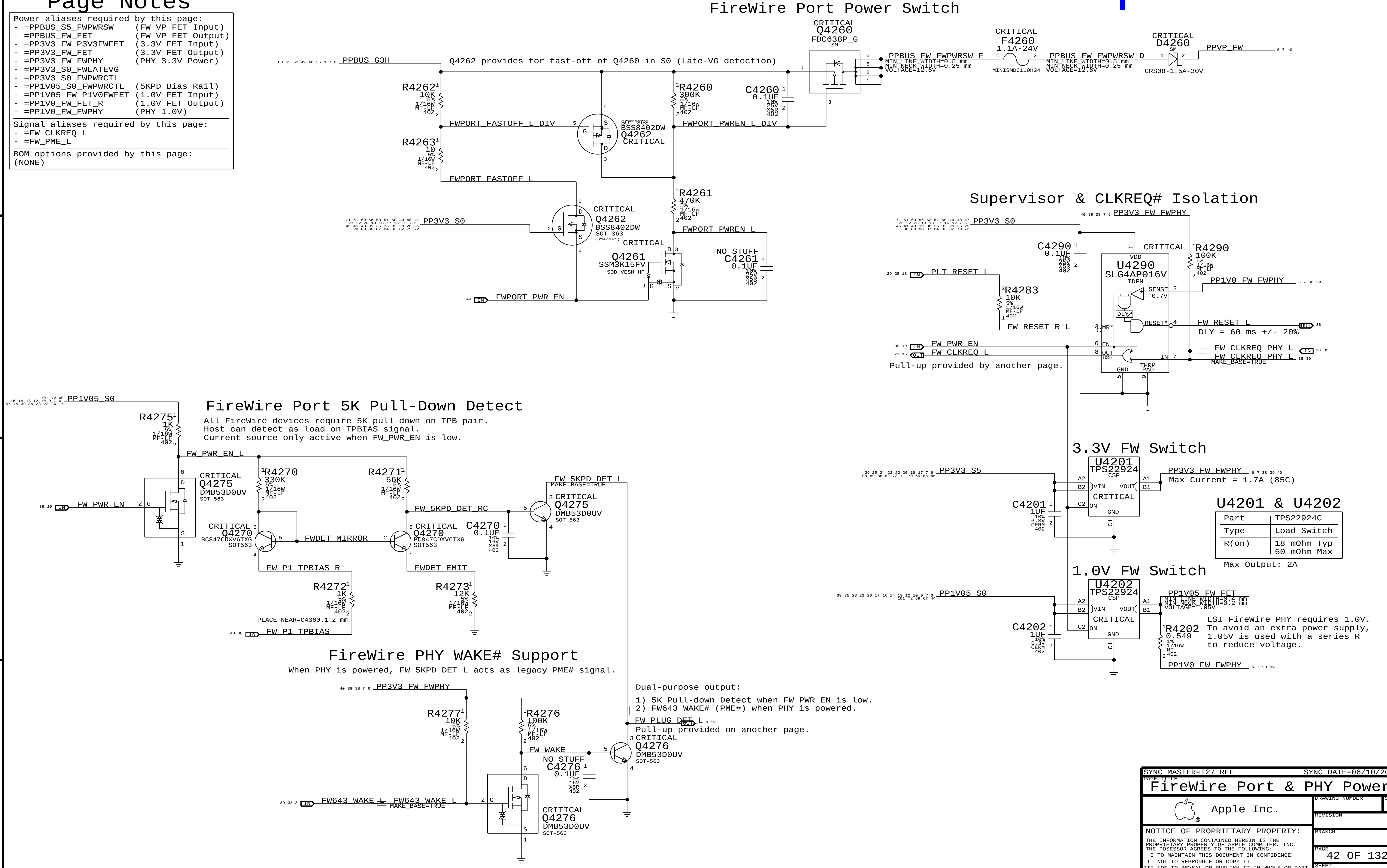
BRANCH

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)



U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

SYNC_MASTER=T27_REF SYNC_DATE=06/10/2010

PAGE TITLE: FireWire Port & PHY Power

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.

Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)

FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

Termination

Place close to FireWire PHY

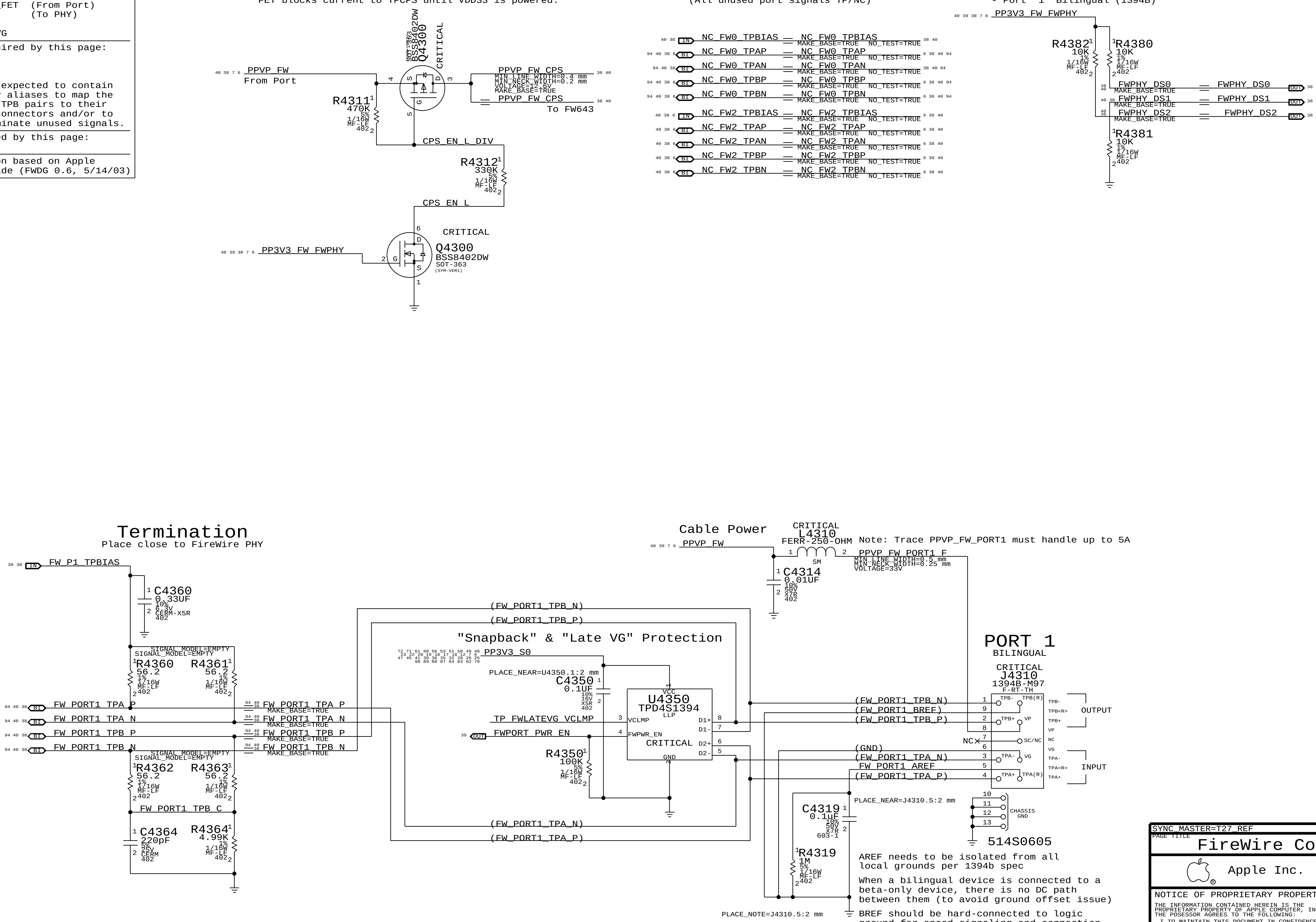
Cable Power

Note: Trace PPVP_FW_PORT1 must handle up to 5A

"Snapback" & "Late VG" Protection

PORT 1

BILINGUAL



AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

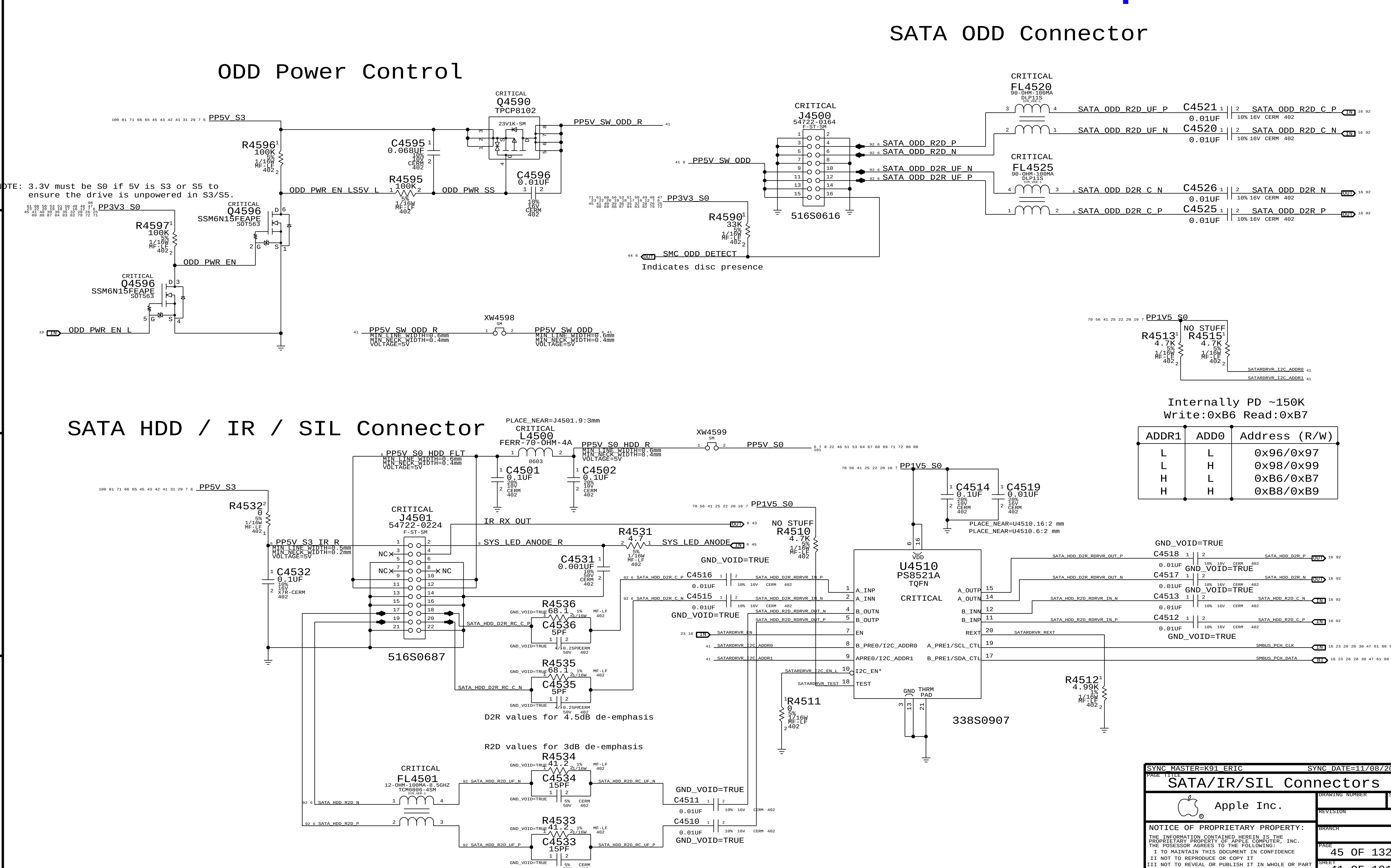
BREF should be hard-connected to logic ground for speed signaling and connection

SYNC_MASTER=T27_REF SYNC_DATE=06/10/2010

PAGE TITLE: FireWire Connector

Apple Inc.

DRAWING NUMBER SIZE D



ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SYNC_MASTER=K91_ERIC SYNC_DATE=11/08/2010

PAGE TITLE

SATA/IR/SIL Connectors

Apple Inc.

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SIZE D

REVISION

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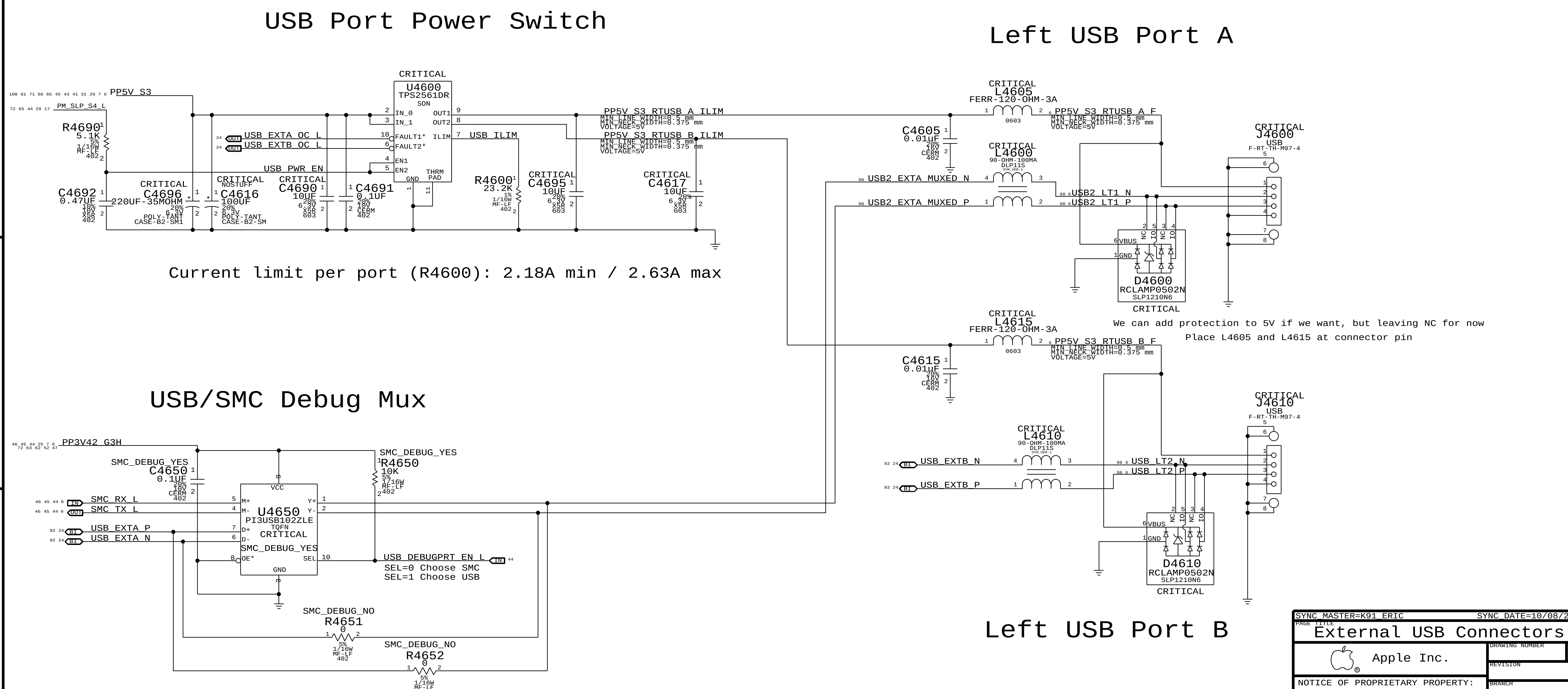

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: External USB Connectors

Apple Inc.

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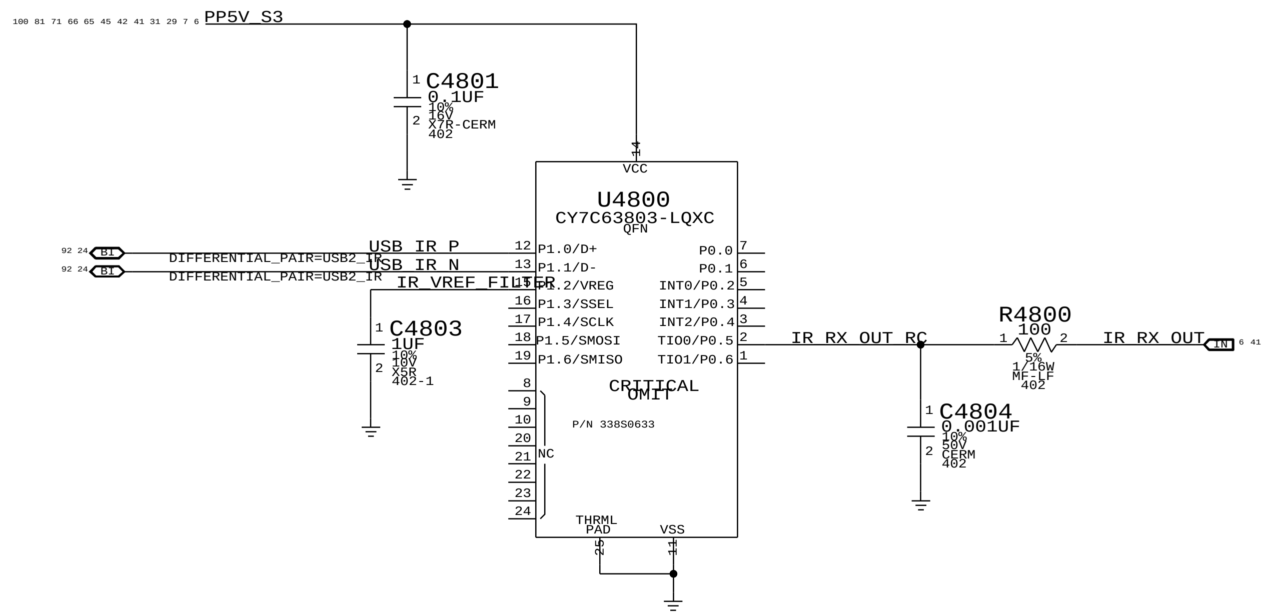
IR SUPPORT



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

Front Flex Support

Apple Inc.

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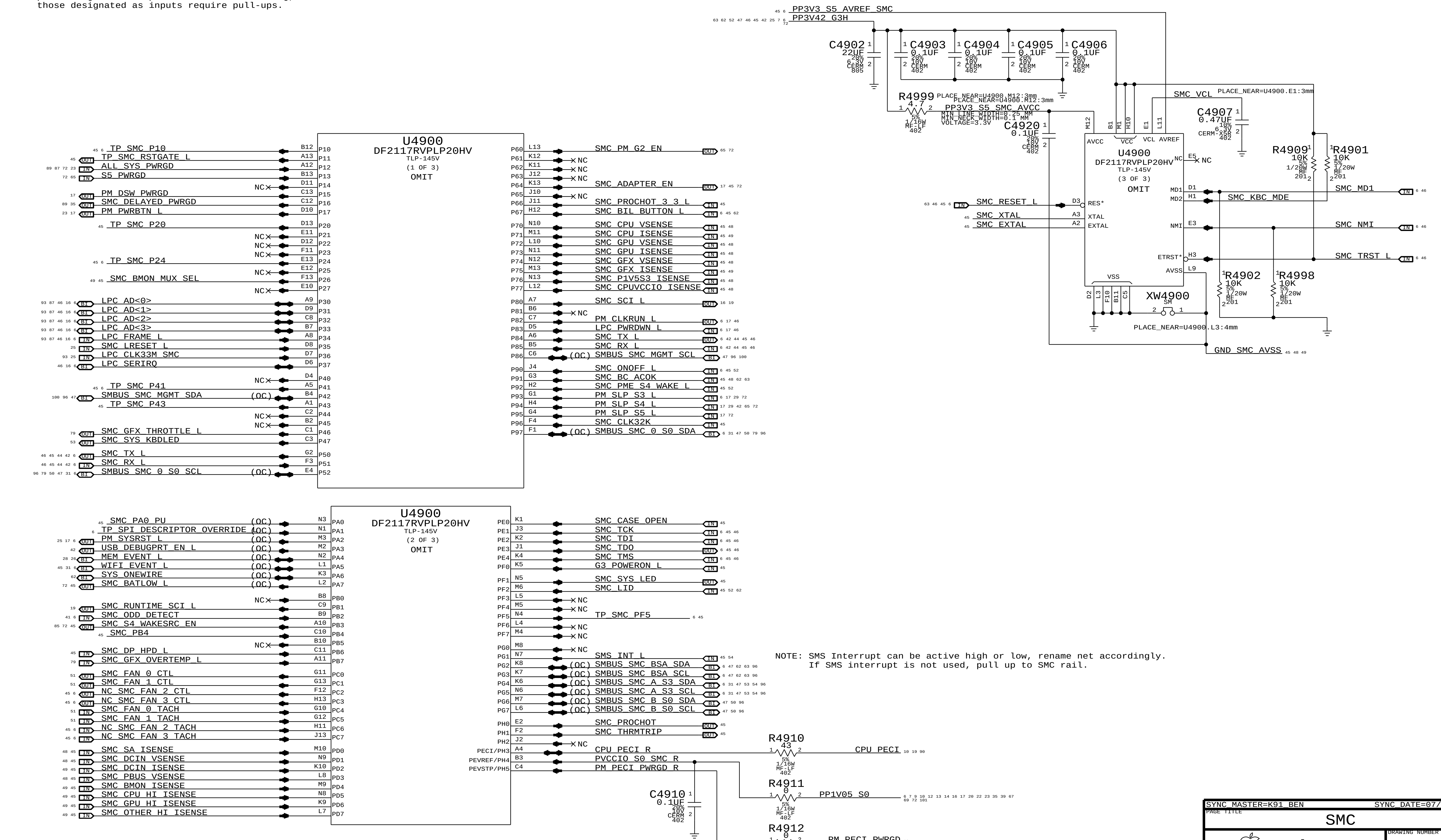
www.qdzbwx.com

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

PAGE TITLE
SMC

DRAWING NUMBER SIZE D

Apple Inc.

REVISION

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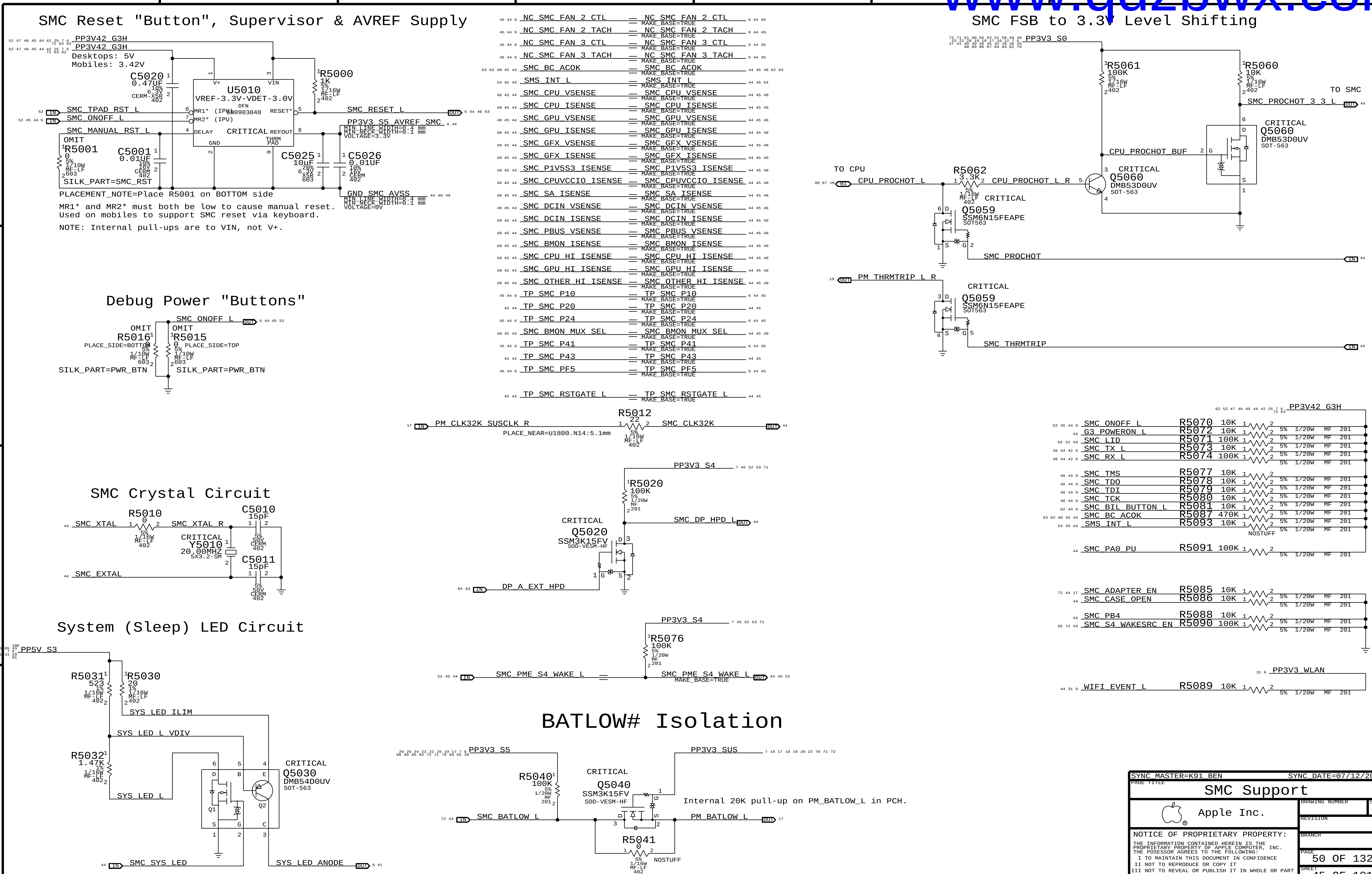


SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

PAGE TITLE

SMC Support

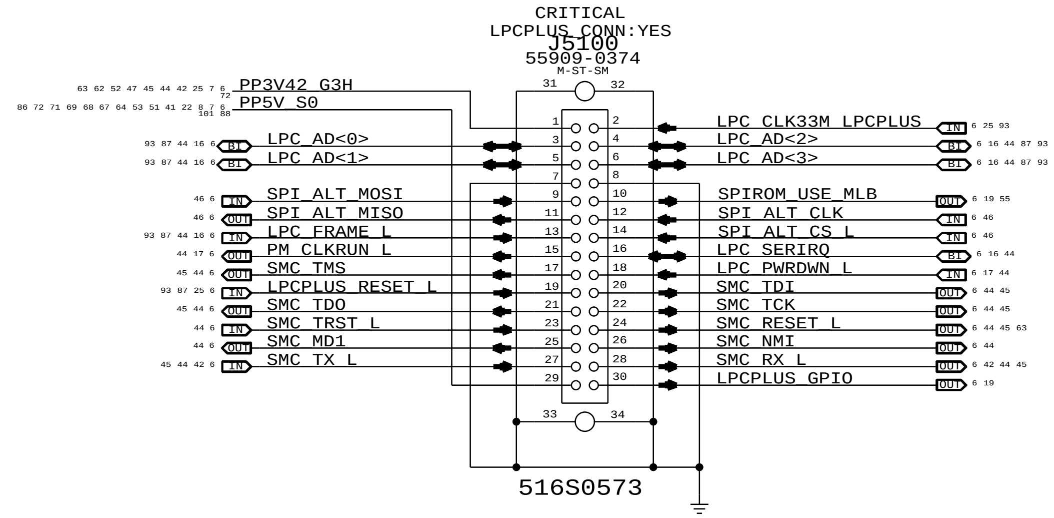
Apple Inc.

DRAWING NUMBER SIZE D

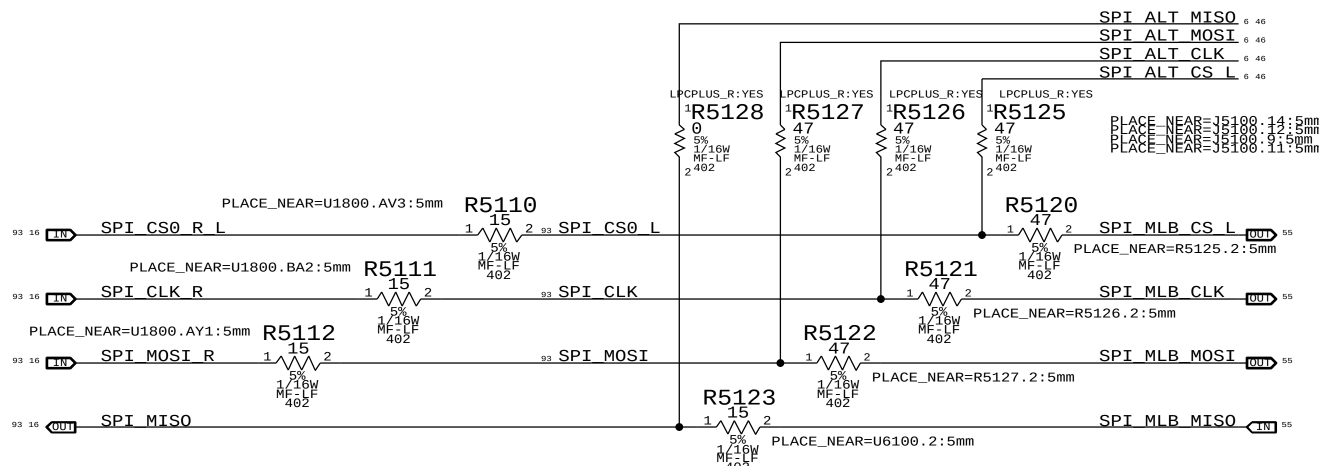
REVISION

BRANCH

LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

LPC+SPI Debug Connector

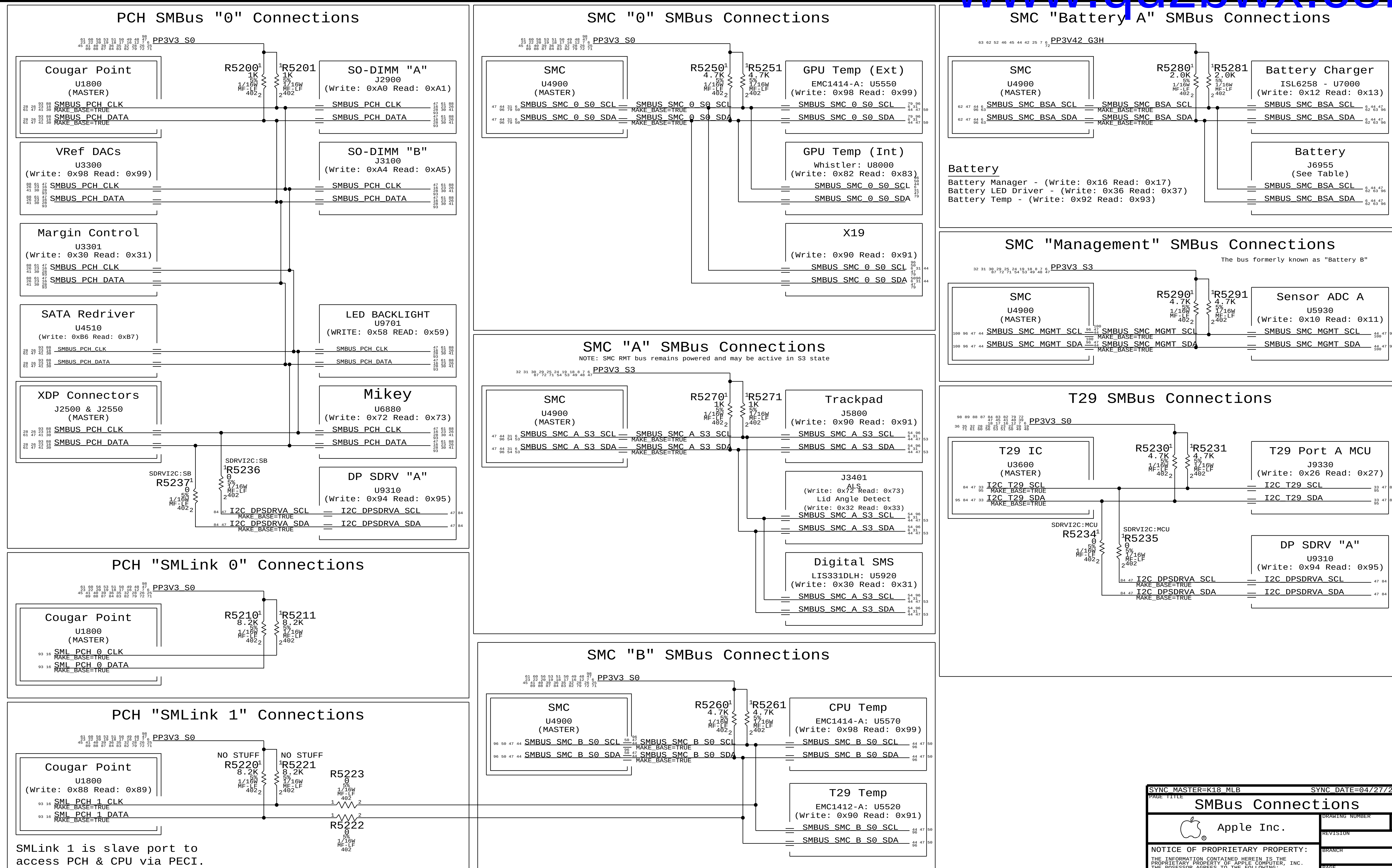
Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH

NOTICE OF PROPRIETARY PROPERTY:

PAGE 51 OF 132

SHEET 46 OF 101



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

SMBus Connections

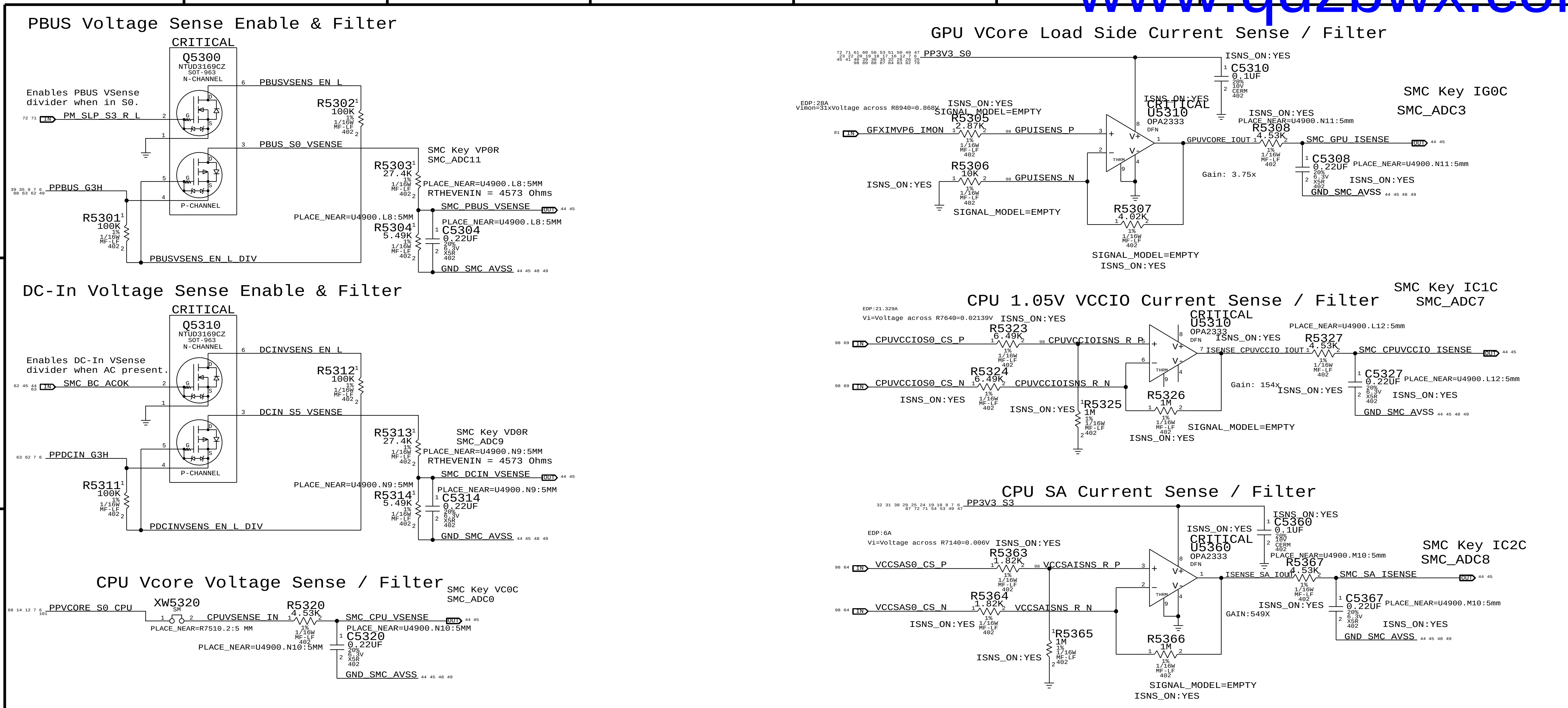
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	4	RES, 0OHM, 0402	C5308,C5327,C5367,C5377		ISNS_ON:NO

SYNC_MASTER=K91_DINESH SYNC_DATE=08/16/2010

PAGE TITLE

Voltage & Load Side Current Sensing

Apple Inc.

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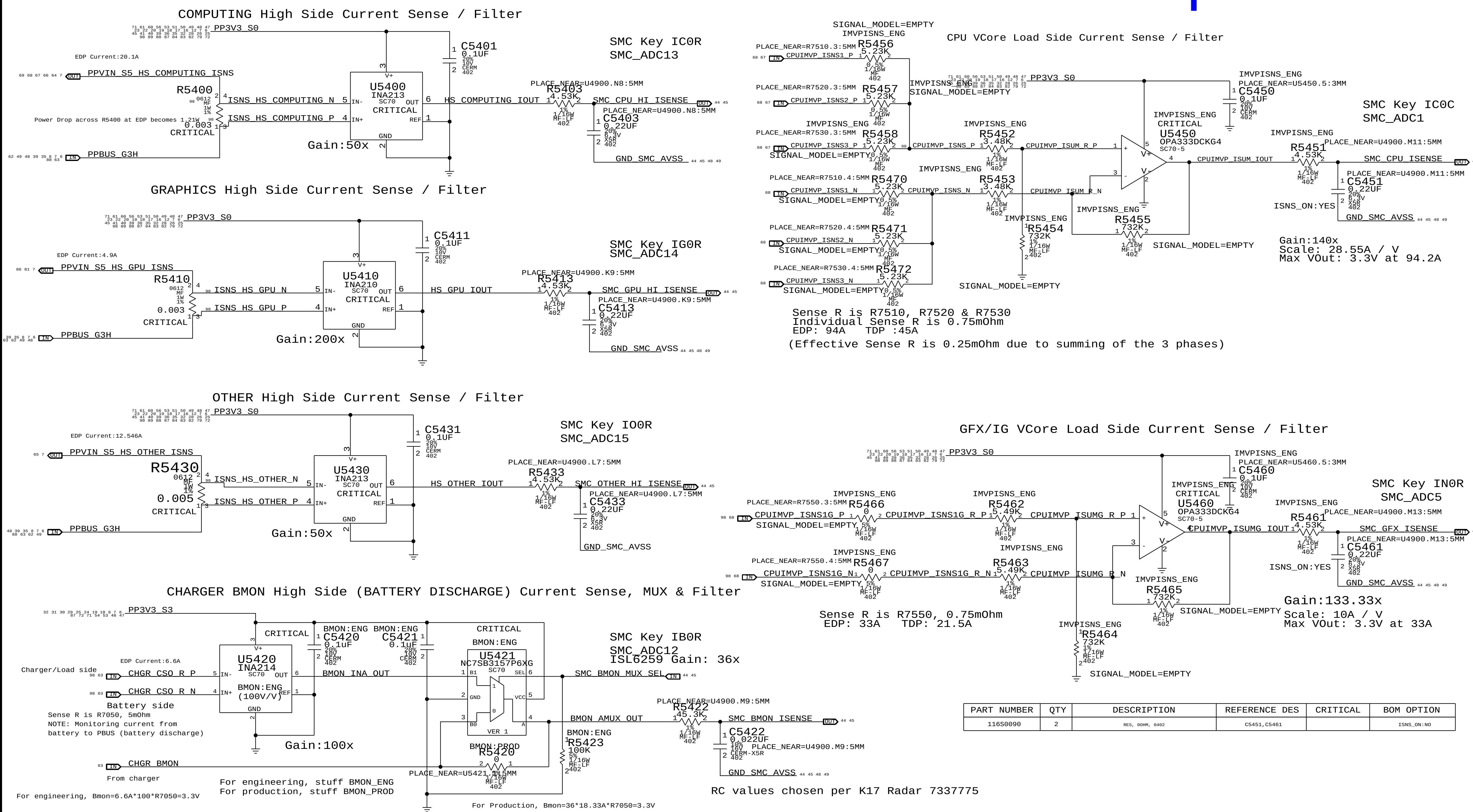
REVISION

BRANCH



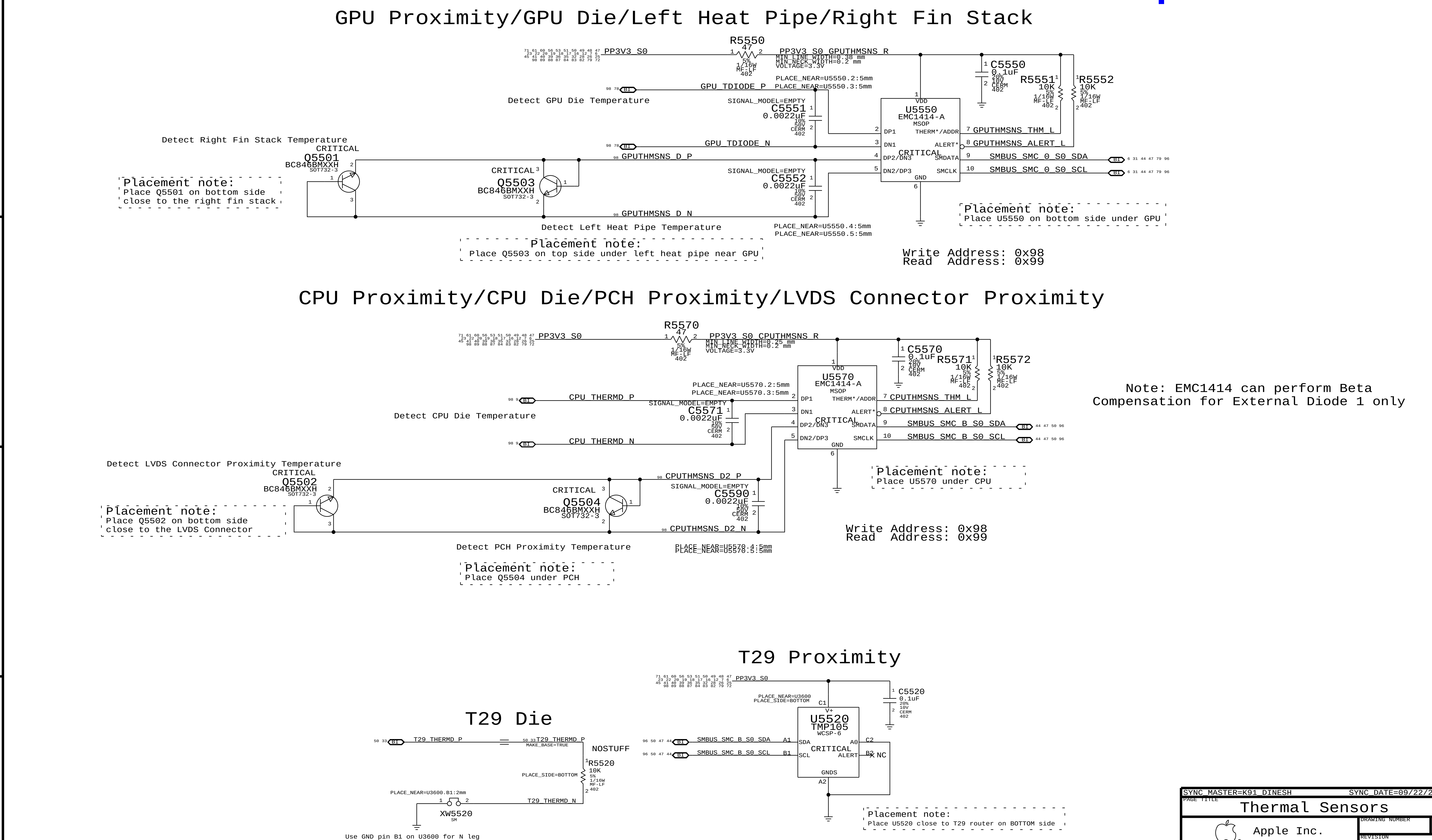
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0090	2	RES, 0OHM, 0402	C5451,C5461		ISNS_ON:NO

SYNC_MASTER=K91_DINESH SYNC_DATE=10/29/2010

PAGE TITLE: High Side and CPU/AXG Current Sensing

Apple Inc.

SIZE: D



SYNC_MASTER=K91_DINESH SYNC_DATE=09/22/2010

PAGE TITLE

Thermal Sensors

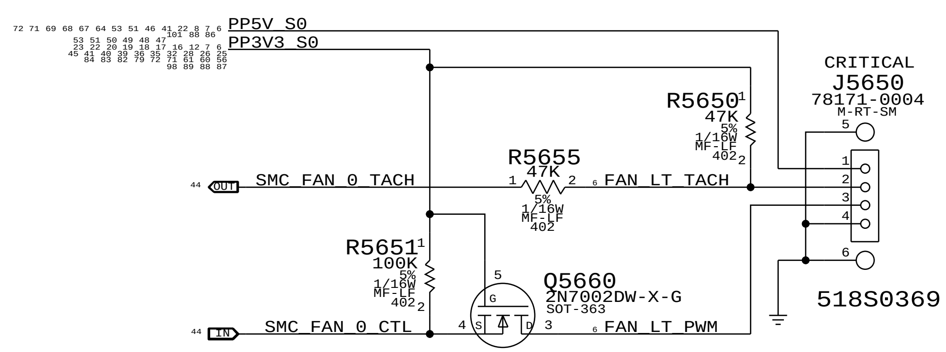
Apple Inc.

DRAWING NUMBER SIZE D

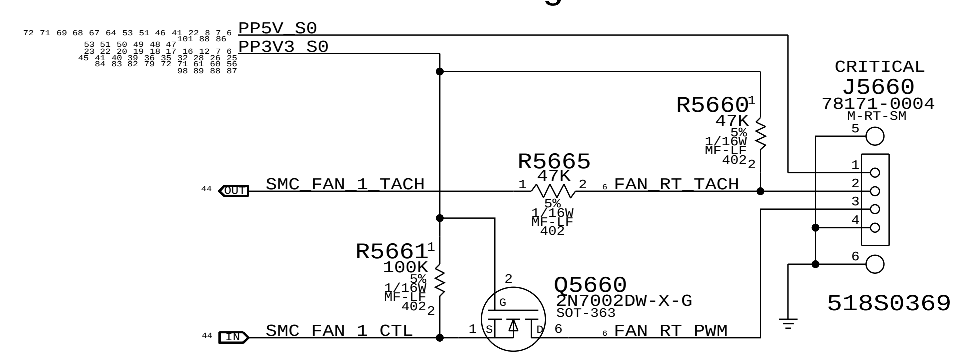
REVISION

BRANCH

Left Fan



Right Fan



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER

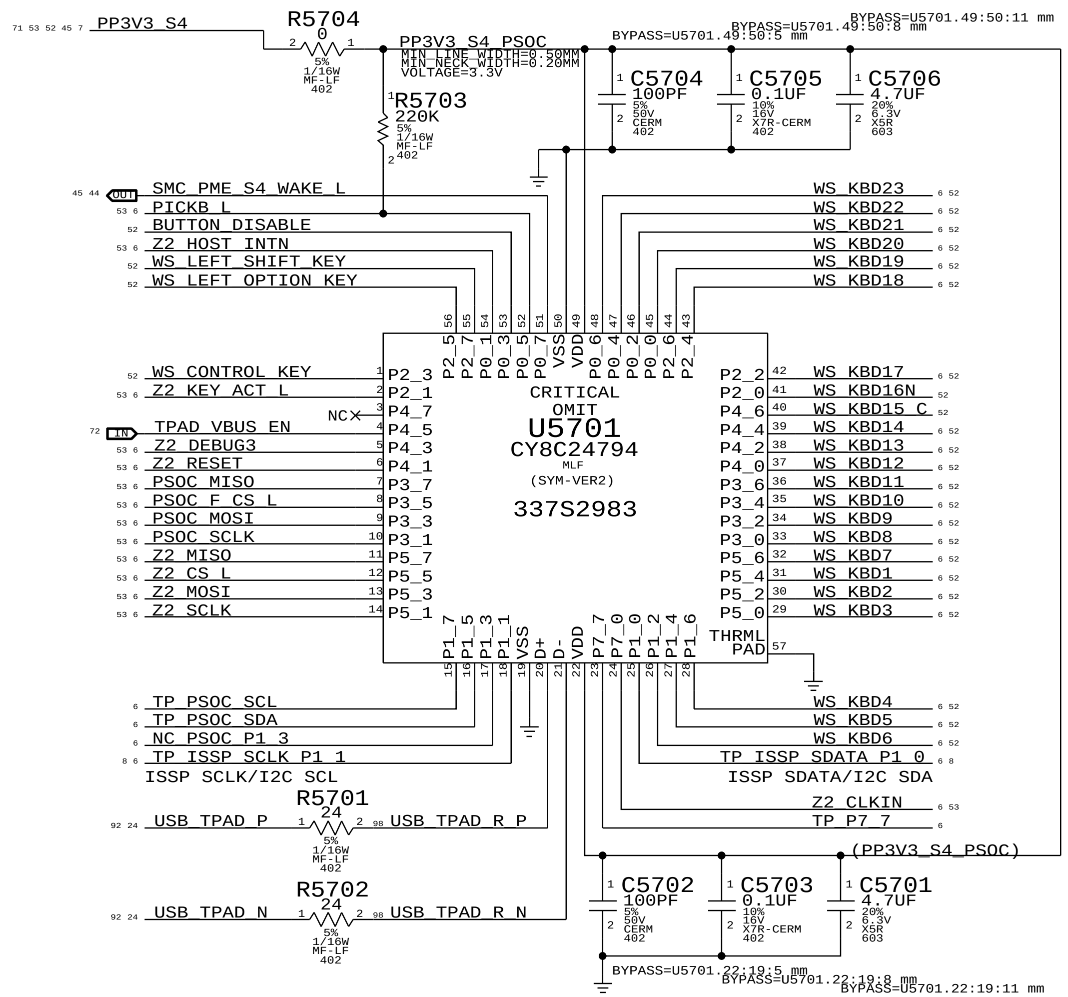
SIZE D

REVISION

BRANCH

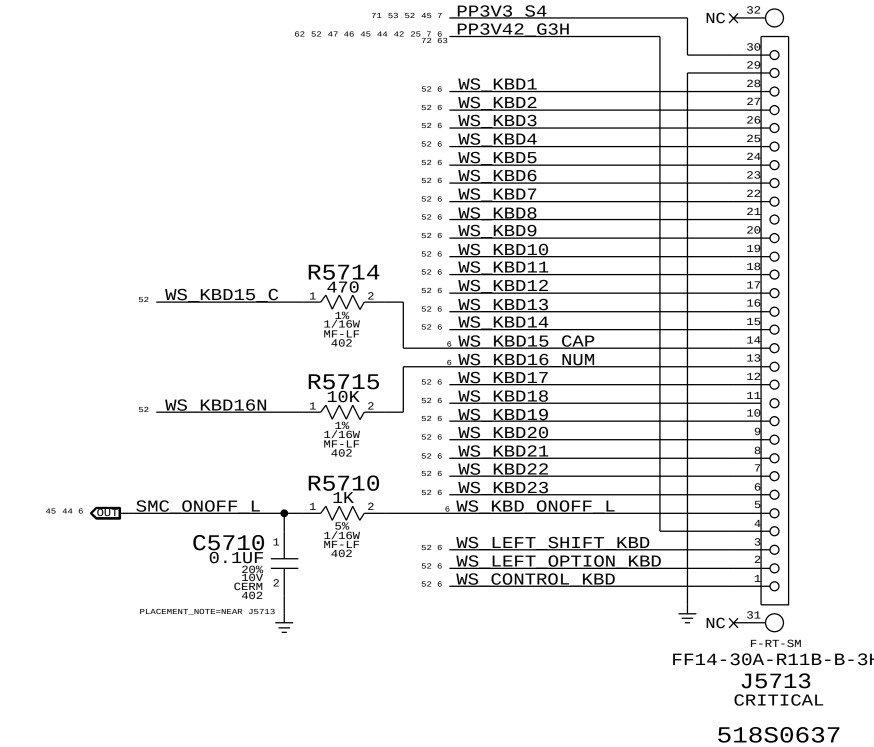
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA 80UA	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60MA (MAX) 60MA (MAX)	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

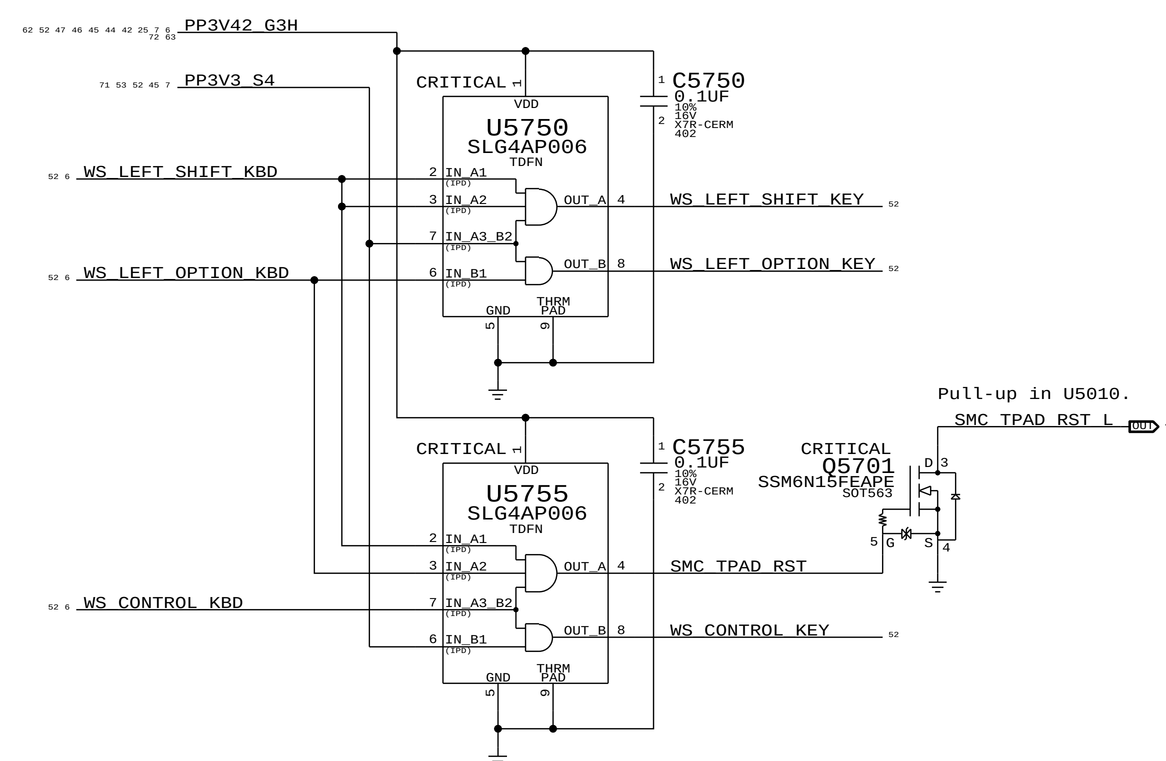
Keyboard Connector



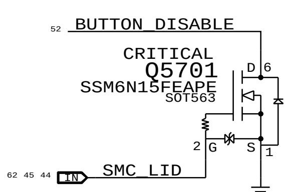
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys ANDed with PSOC power to isolate when PSOC is not powered.



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE
WELLSPRING 1

Apple Inc.

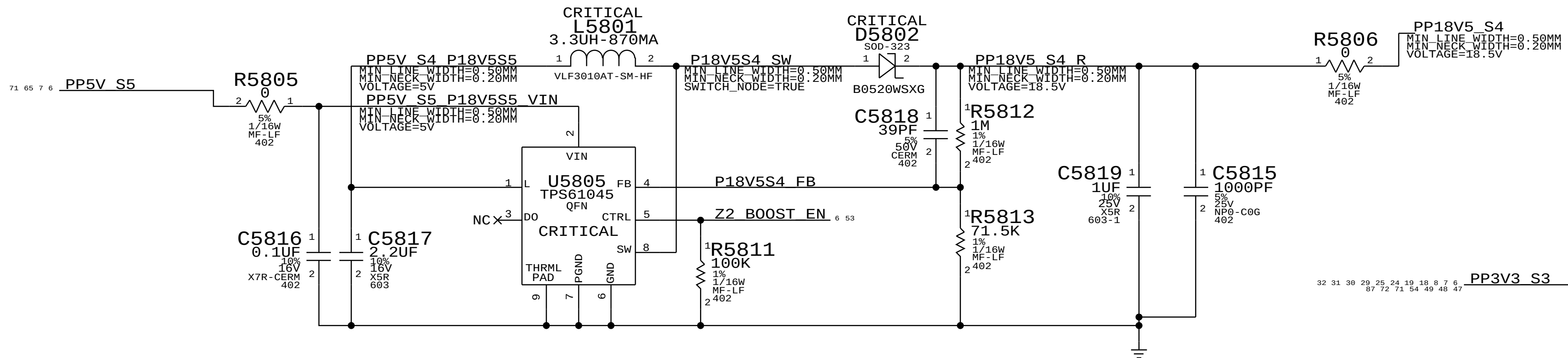
DRAWING NUMBER SIZE D

REVISION

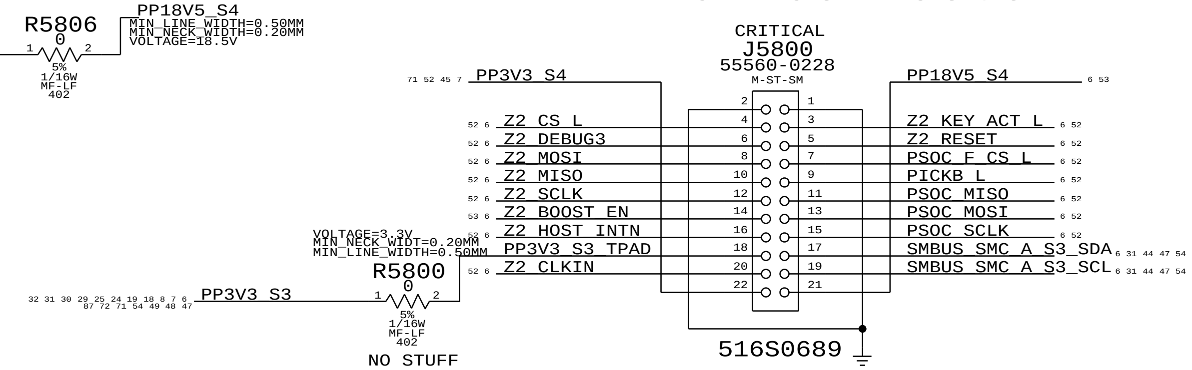
BRANCH

BOOSTER +18.5VDC FOR SENSORS

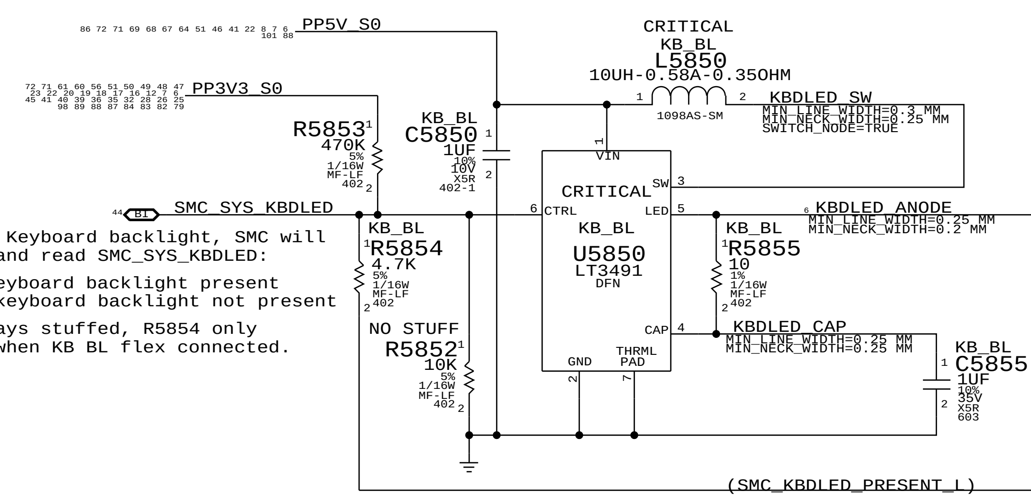
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

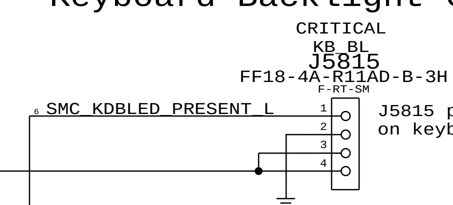


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



J5815 pin 1 is grounded on keyboard backlight flex

SYNC_MASTER=K91_ERIC SYNC_DATE=07/14/2010

PAGE TITLE: WELLSPRING 2

Apple Inc.

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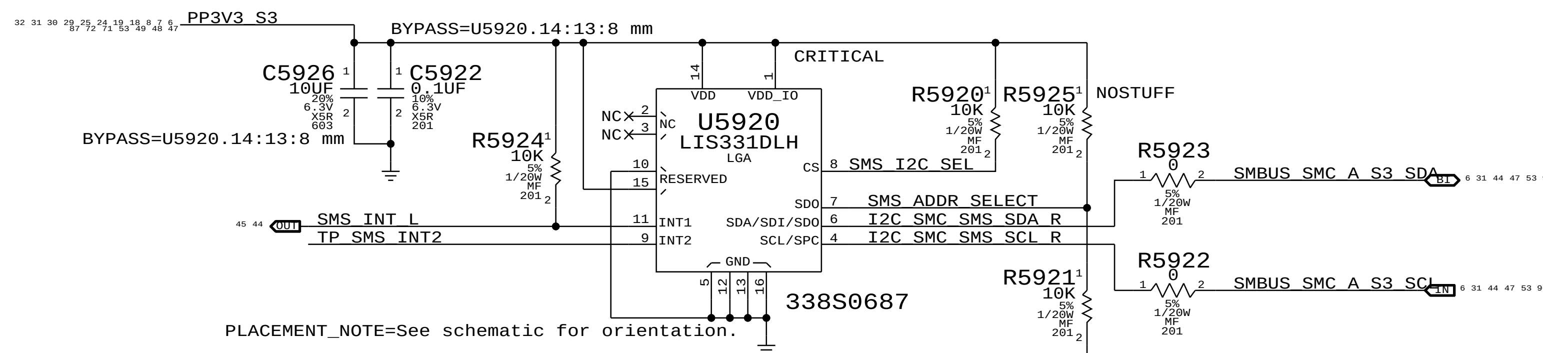
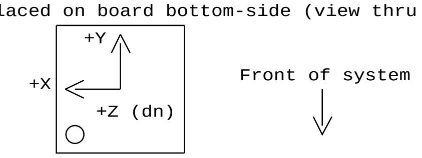


PLACEMENT_NOTE=See schematic for orientation.

SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

NOTE: SDA and SCL have internal pull-ups to VDD_IO.

Desired orientation when
placed on board bottom-side (view thru top):



Circle indicates pin 1 location when placed
in correct orientation

SYNC_MASTER=K91_DINESH SYNC_DATE=08/06/2010

PAGE TITLE

Digital Accelerometer

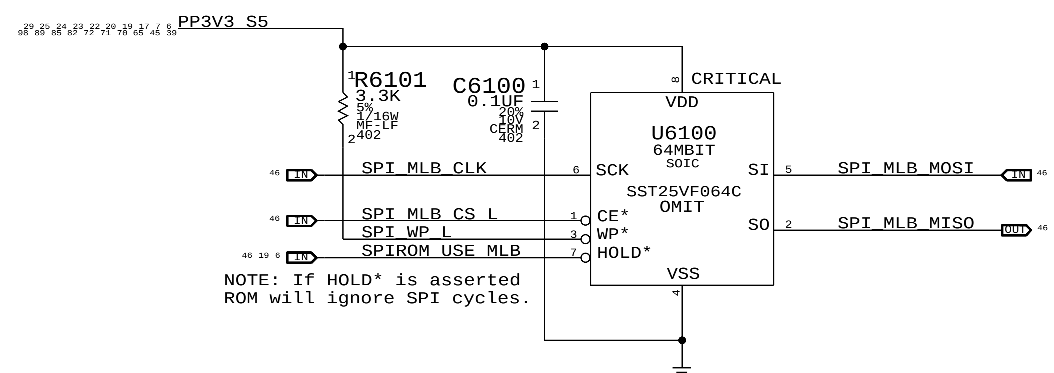
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=K91_BEN SYNC_DATE=06/08/2010

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

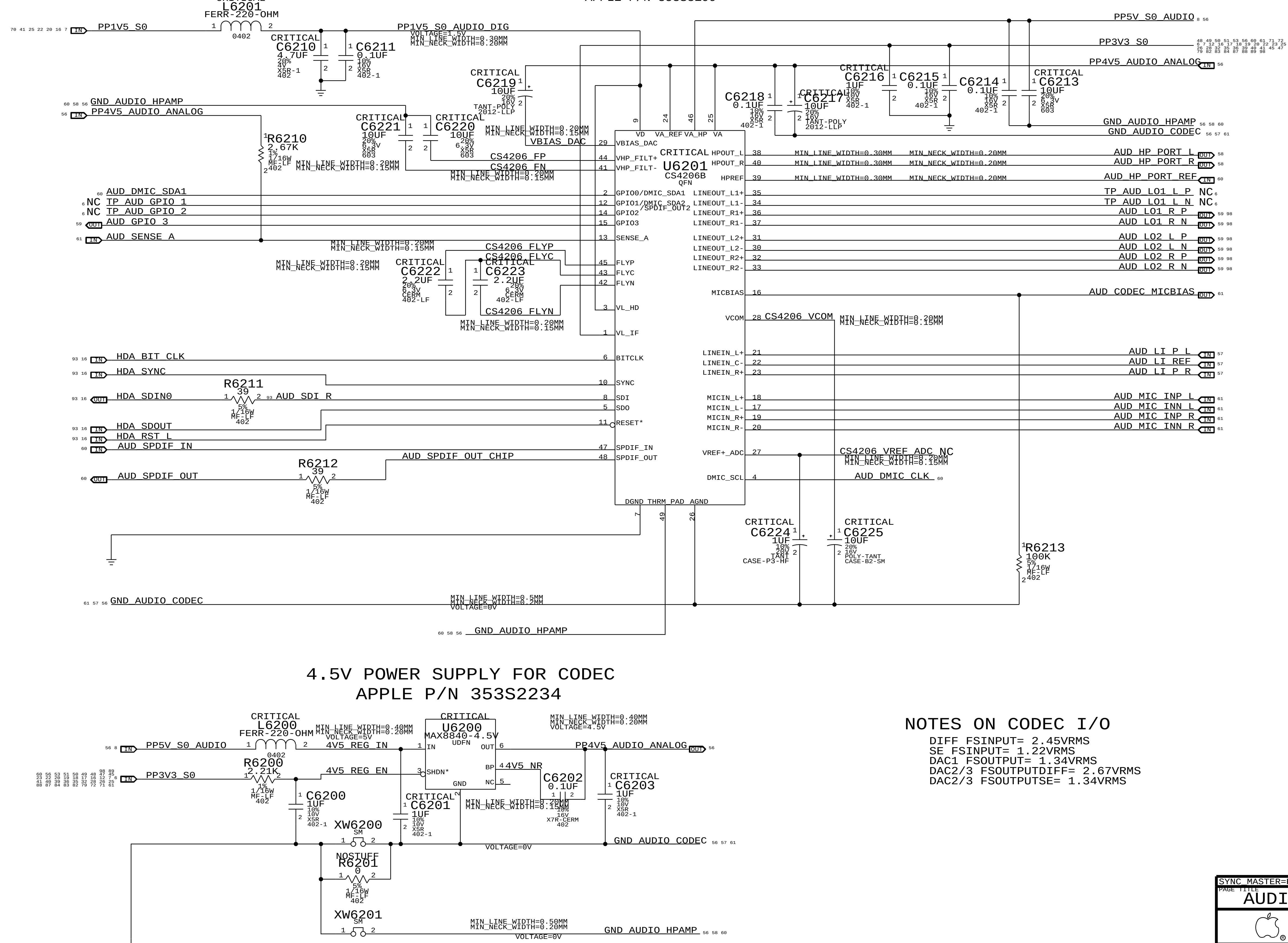
BRANCH

PAGE 61 OF 132

SHEET 55 OF 101

AUDIO CODEC

APPLE P/N 353S3199



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=K91_AUDIO SYNC_DATE=09/30/2010

PAGE TITLE

AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

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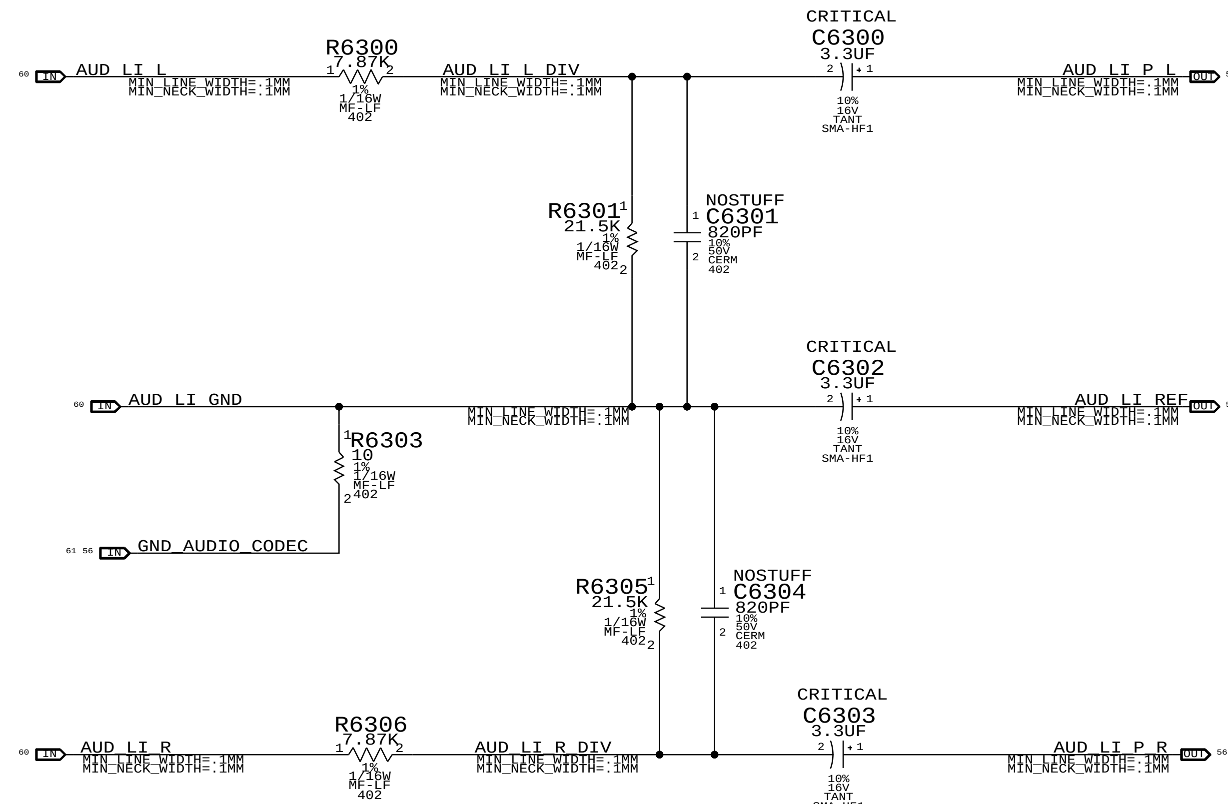
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 18K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE

AUDIO: LINE INPUT FILTER

Apple Inc.

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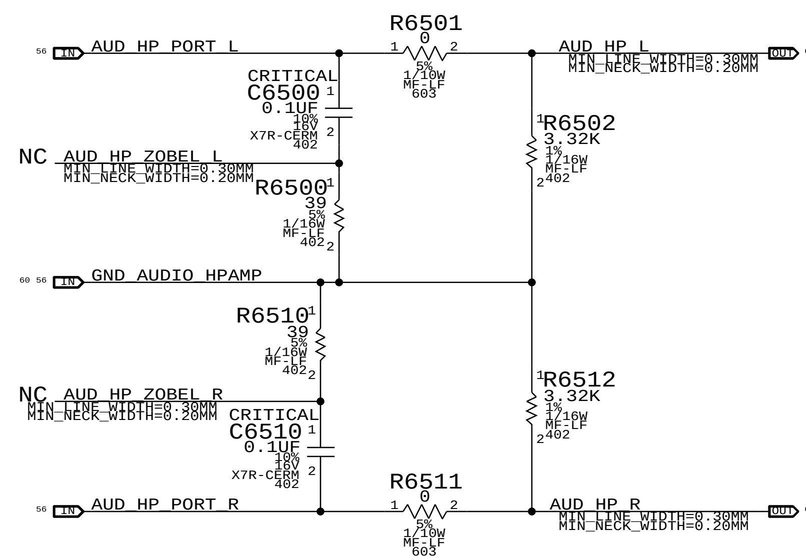
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

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REVISION

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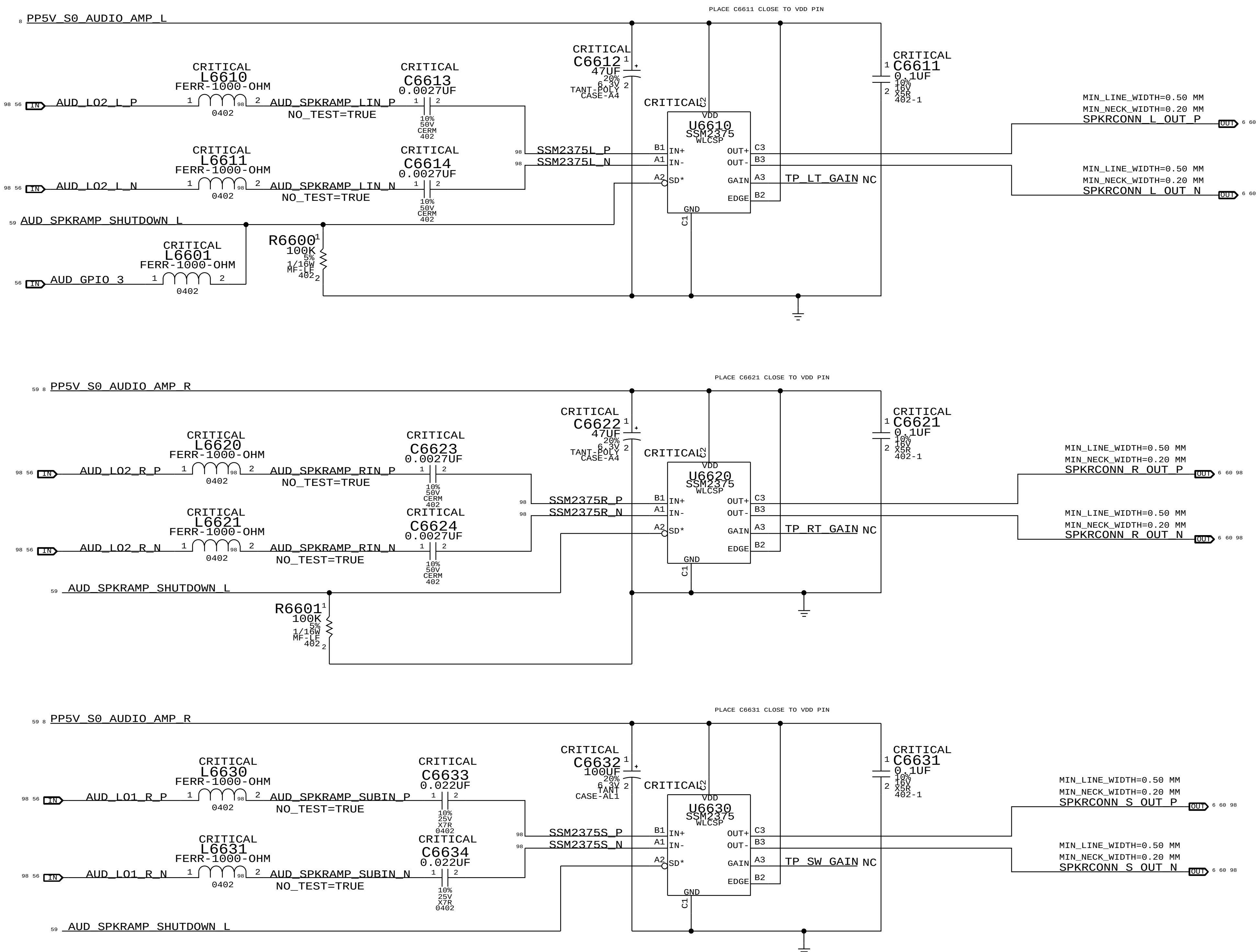
3X MONO SPEAKER AMPLIFIERS (SSM2375)
APN: 353S2958

GAIN = +3 DB
1ST ORDER FC (L&R) = ~737 HZ
1ST ORDER FC (SUB) = ~90 HZ



SYNC_MASTER=K91_AUDIO SYNC_DATE=07/12/2010

PAGE TITLE

AUDIO: SPEAKER AMP

DRAWING NUMBER | SIZE D

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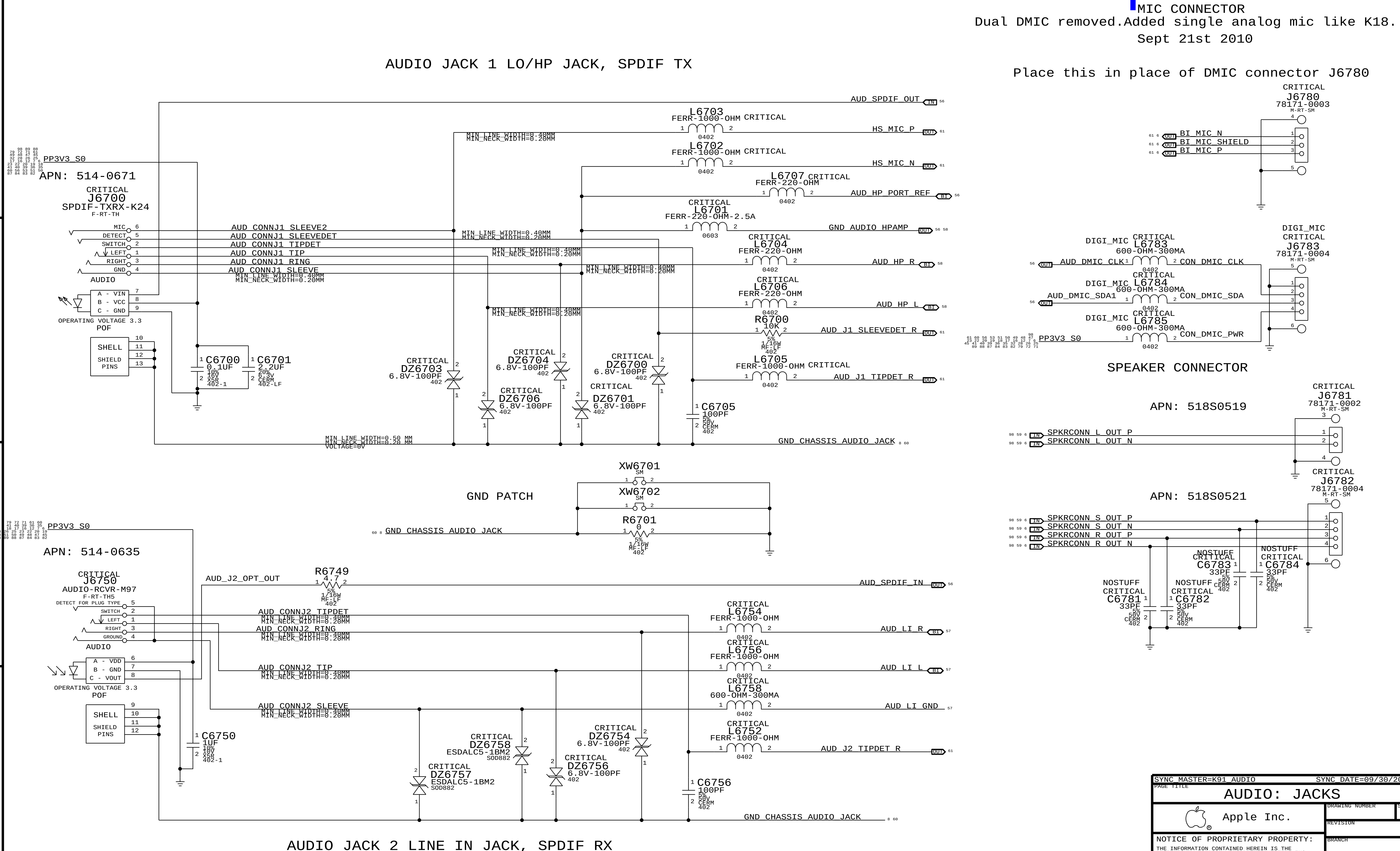

SYNC_MASTER=K91_AUDIO SYNC_DATE=09/30/2010

PAGE TITLE

AUDIO: JACKS

Apple Inc.

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REVISION

BRANCH

CODEC OUTPUT SIGNAL PATHS

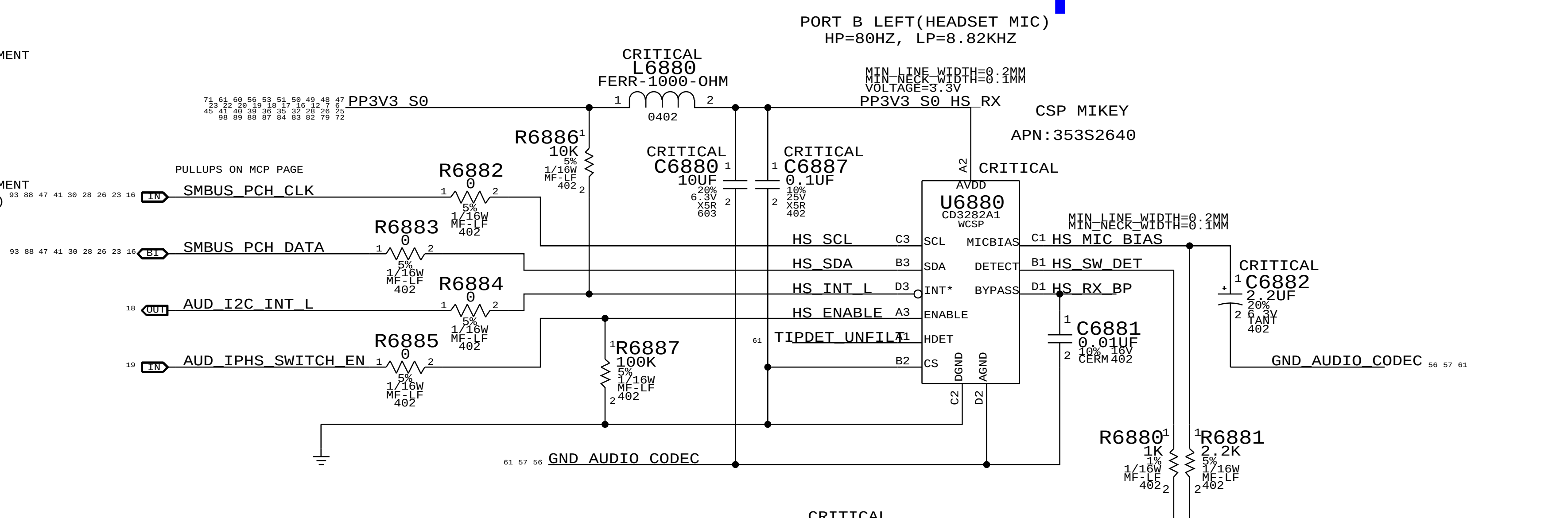
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

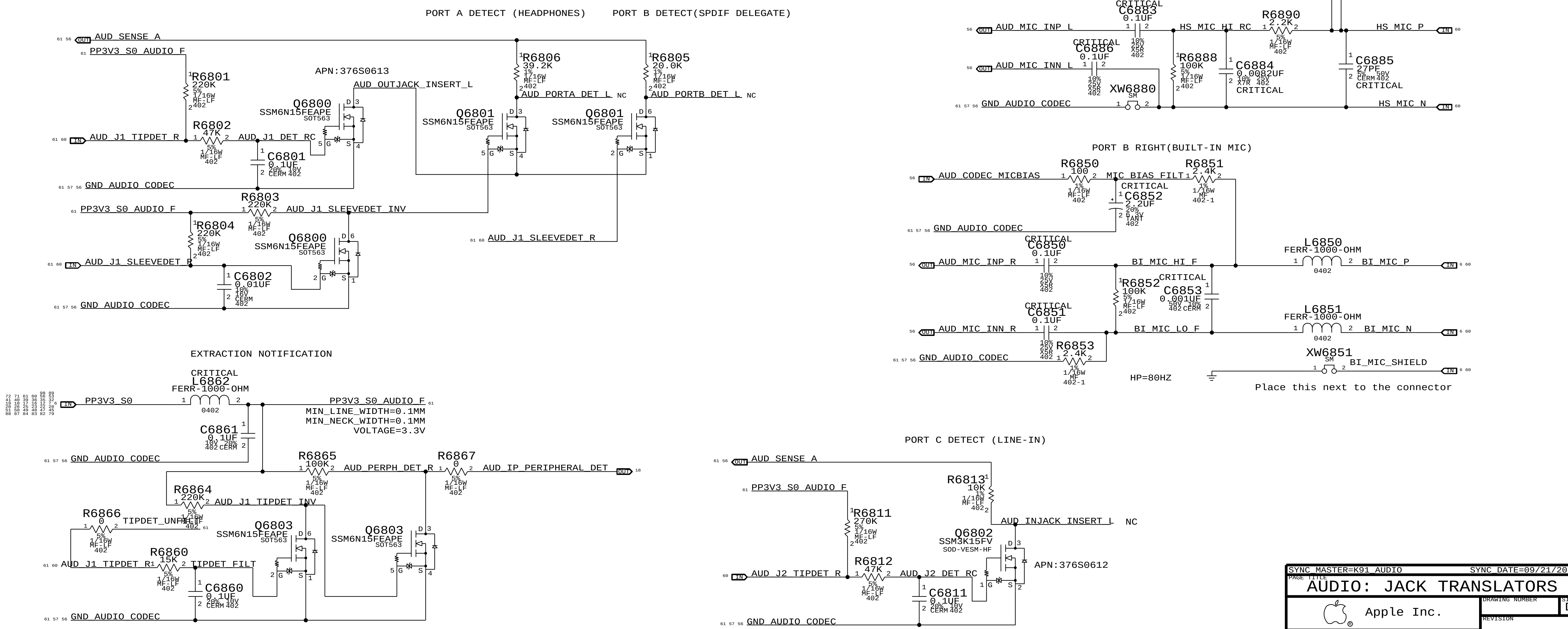
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3





SYNC_MASTER=K91_AUDIO SYNC_DATE=09/21/2010

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

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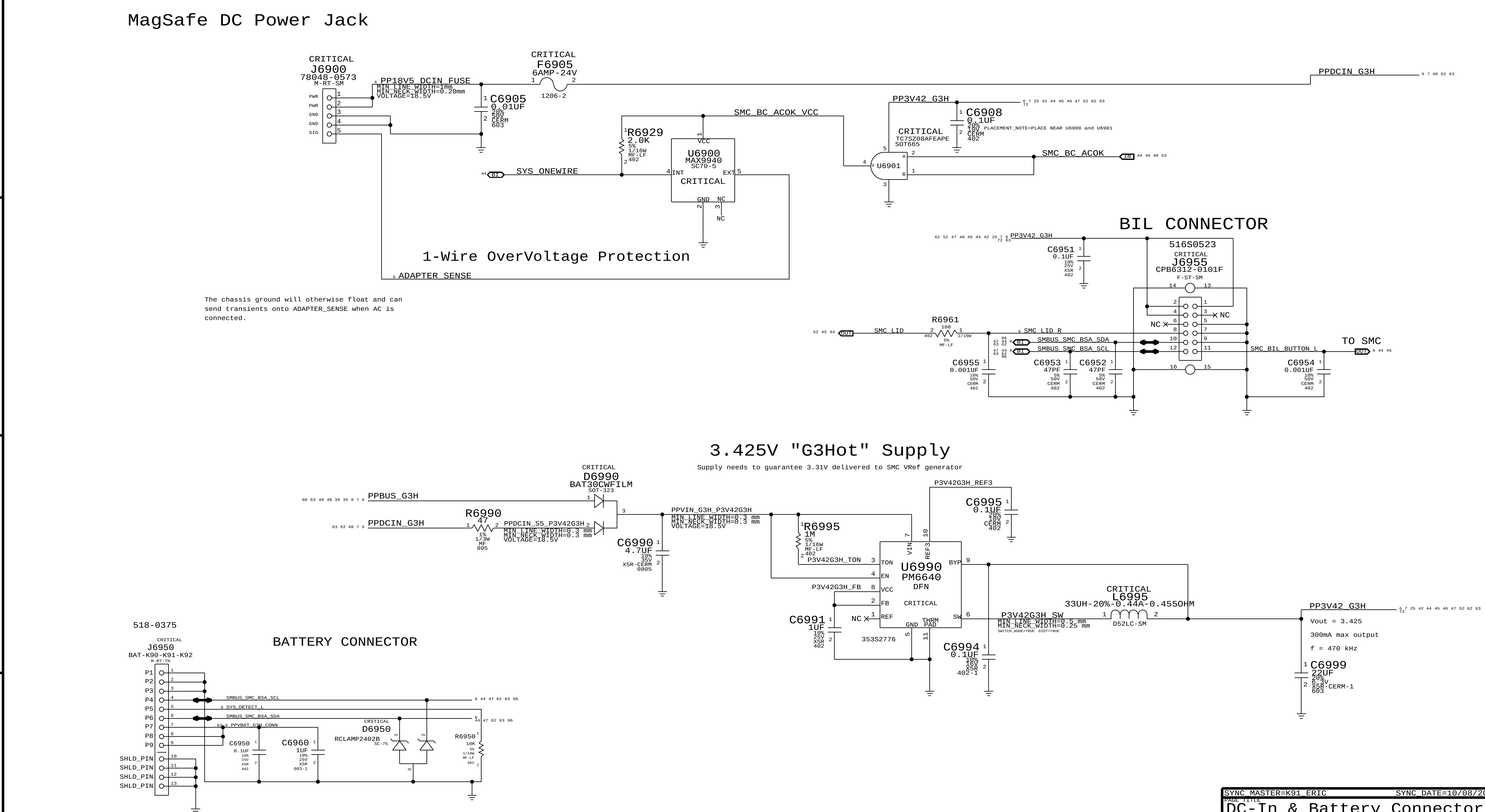
NOTICE OF PROPRIETARY PROPERTY:



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

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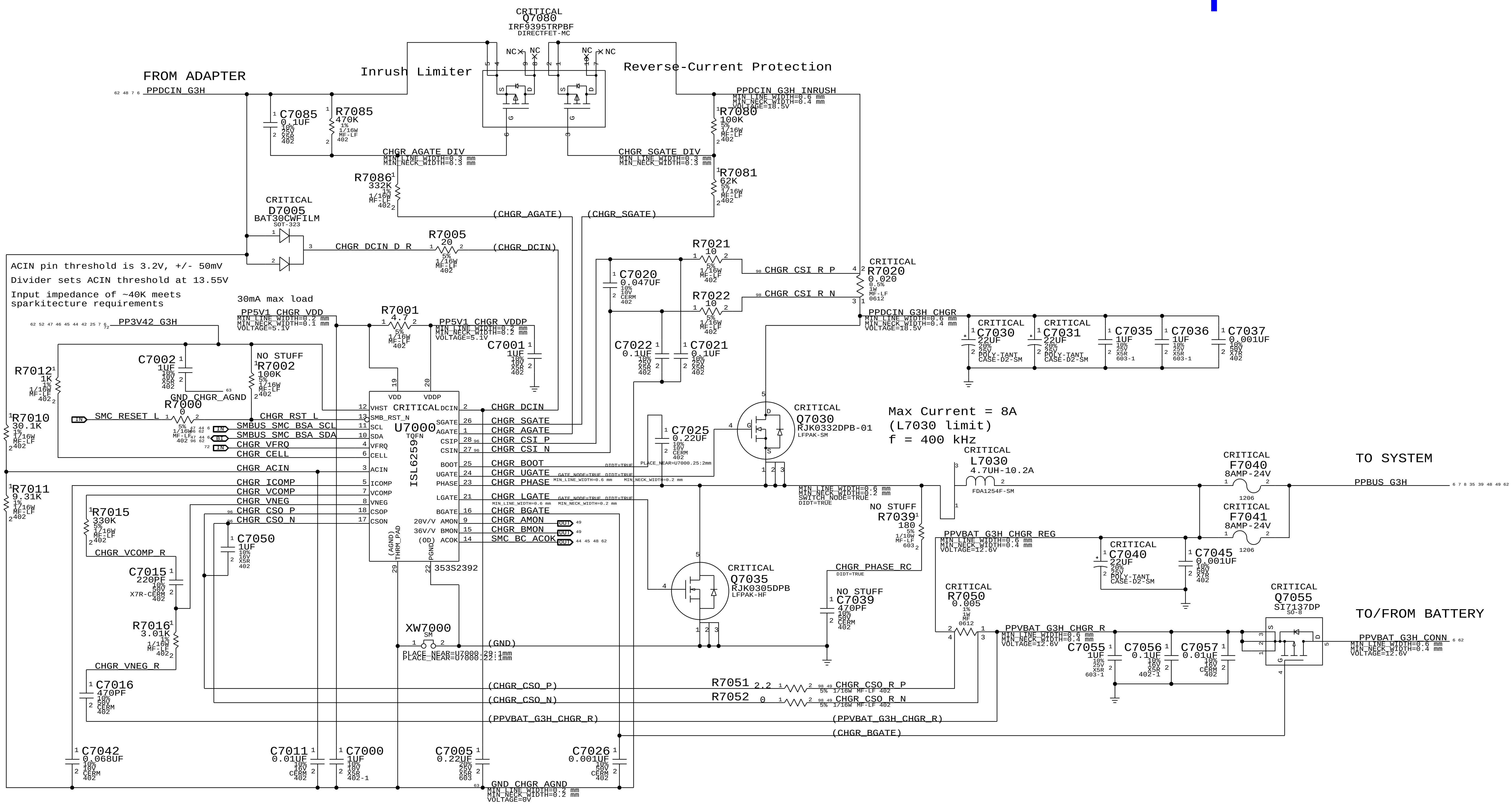


SYNC_MASTER=K91_CHANG SYNC_DATE=07/20/2010

PAGE TITLE

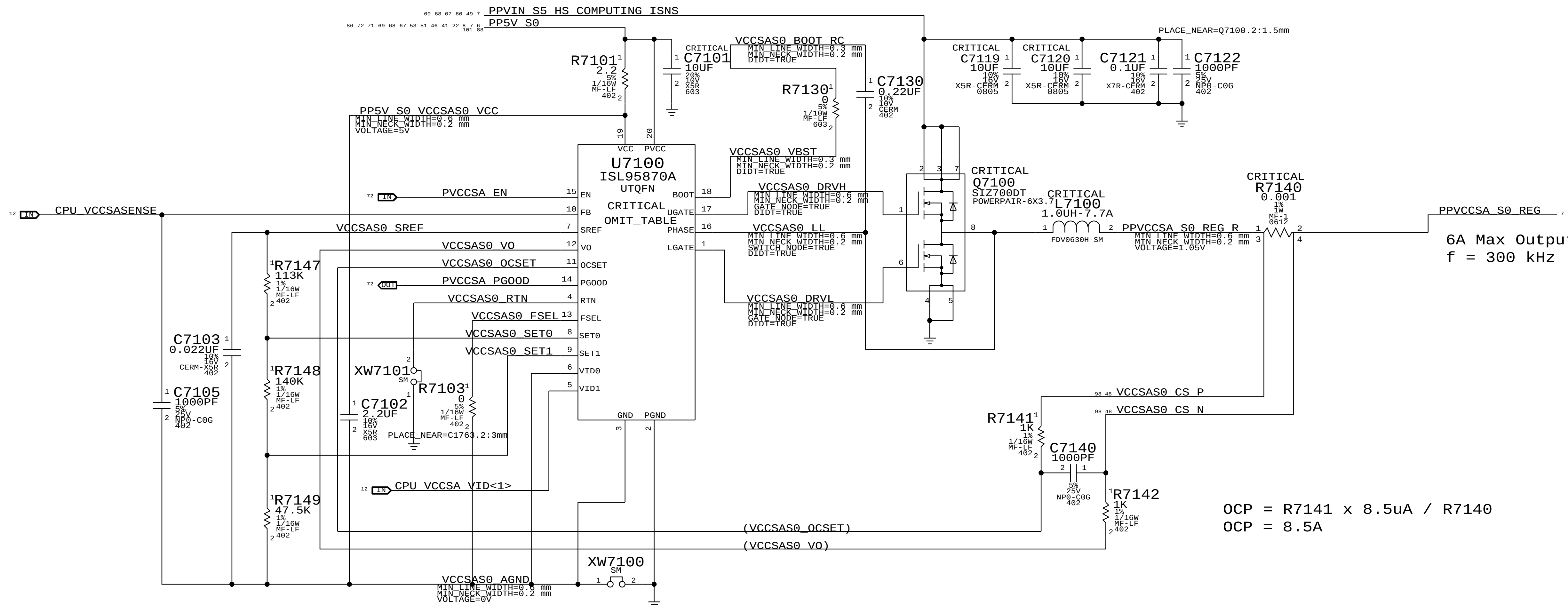
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20P	U7100	CRITICAL	

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

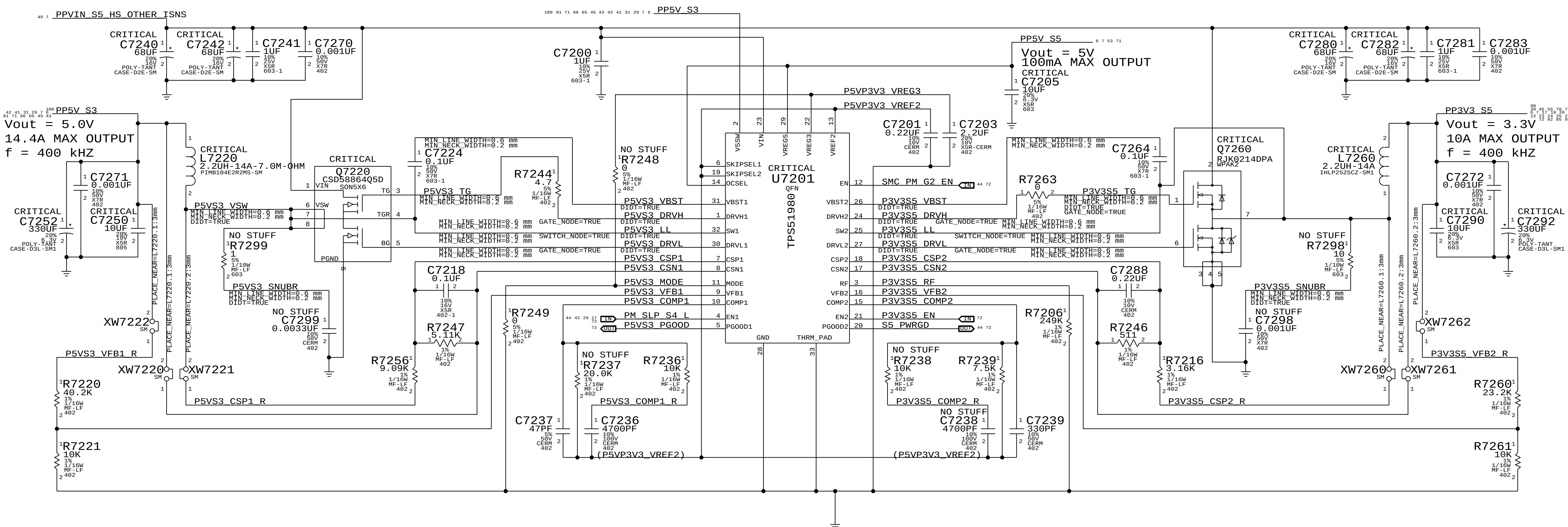
PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER / SIZE: D

REVISION

BRANCH



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE

5V / 3.3V Power Supply

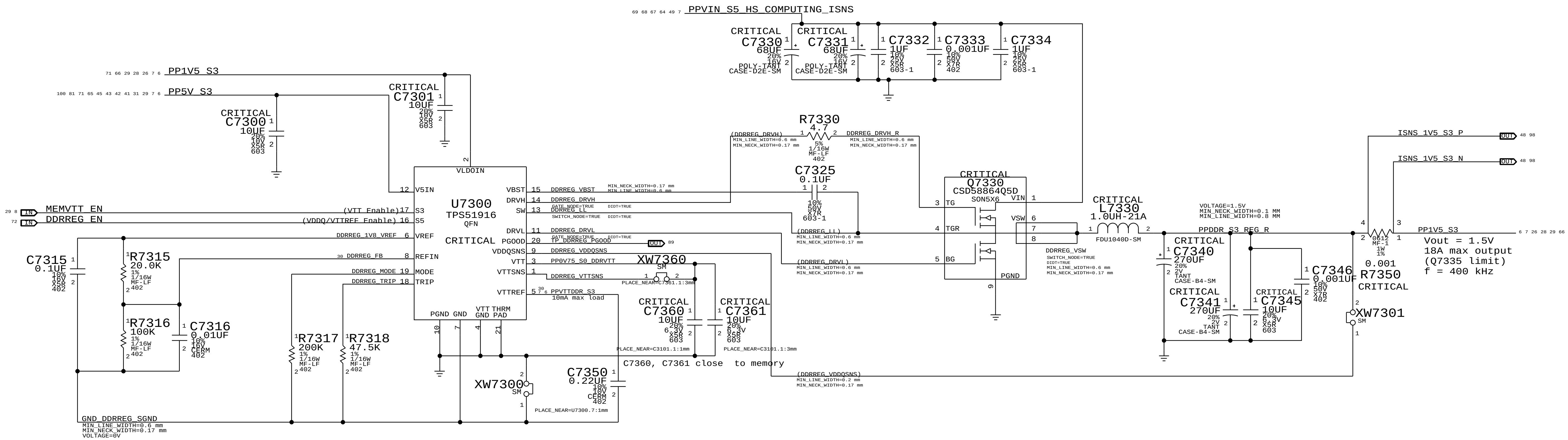
Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER

SIZE D

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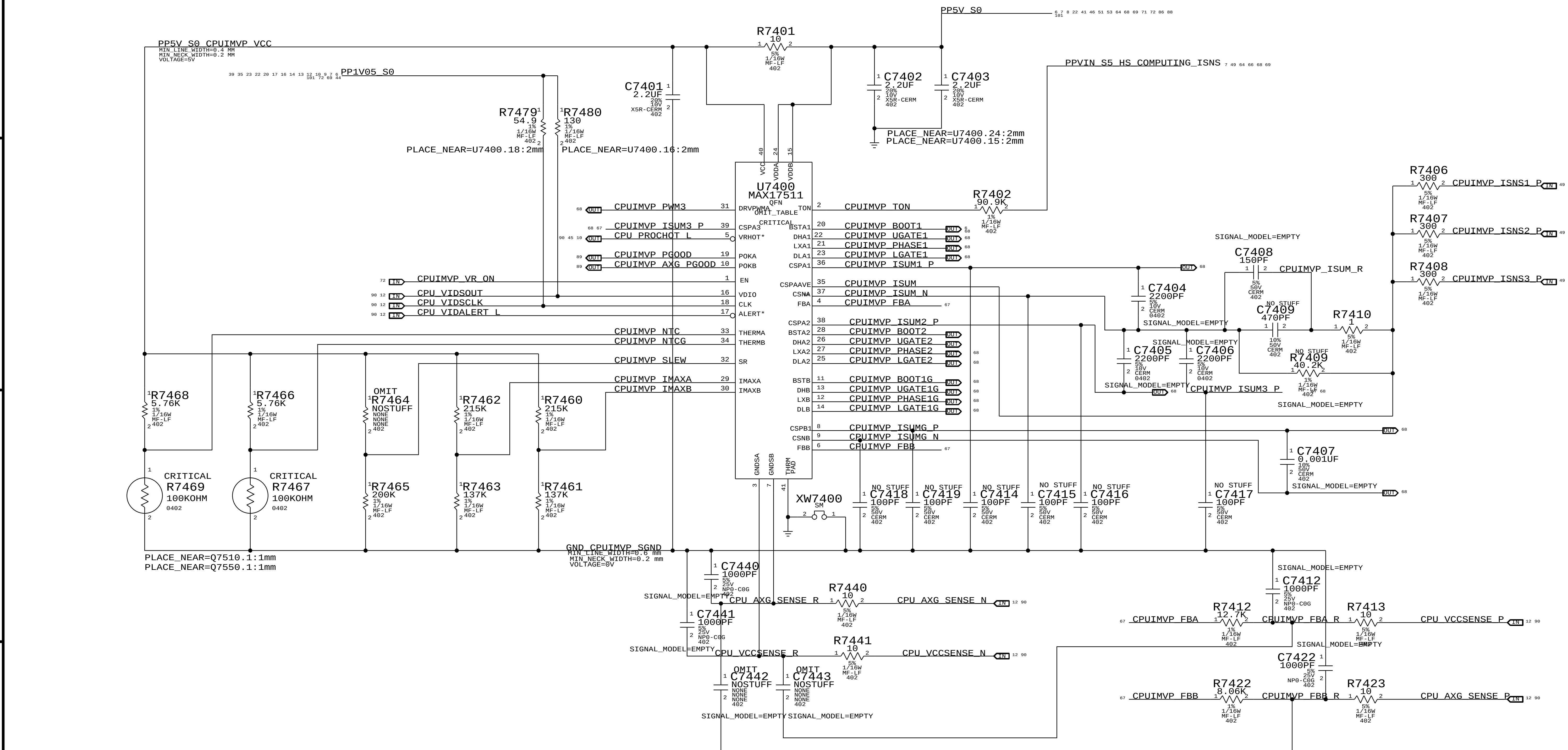
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3259	1	IC,MAX15092,3+1PH CPU REG,IMVP7,5X5QFN40	U7400	CRITICAL	



SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

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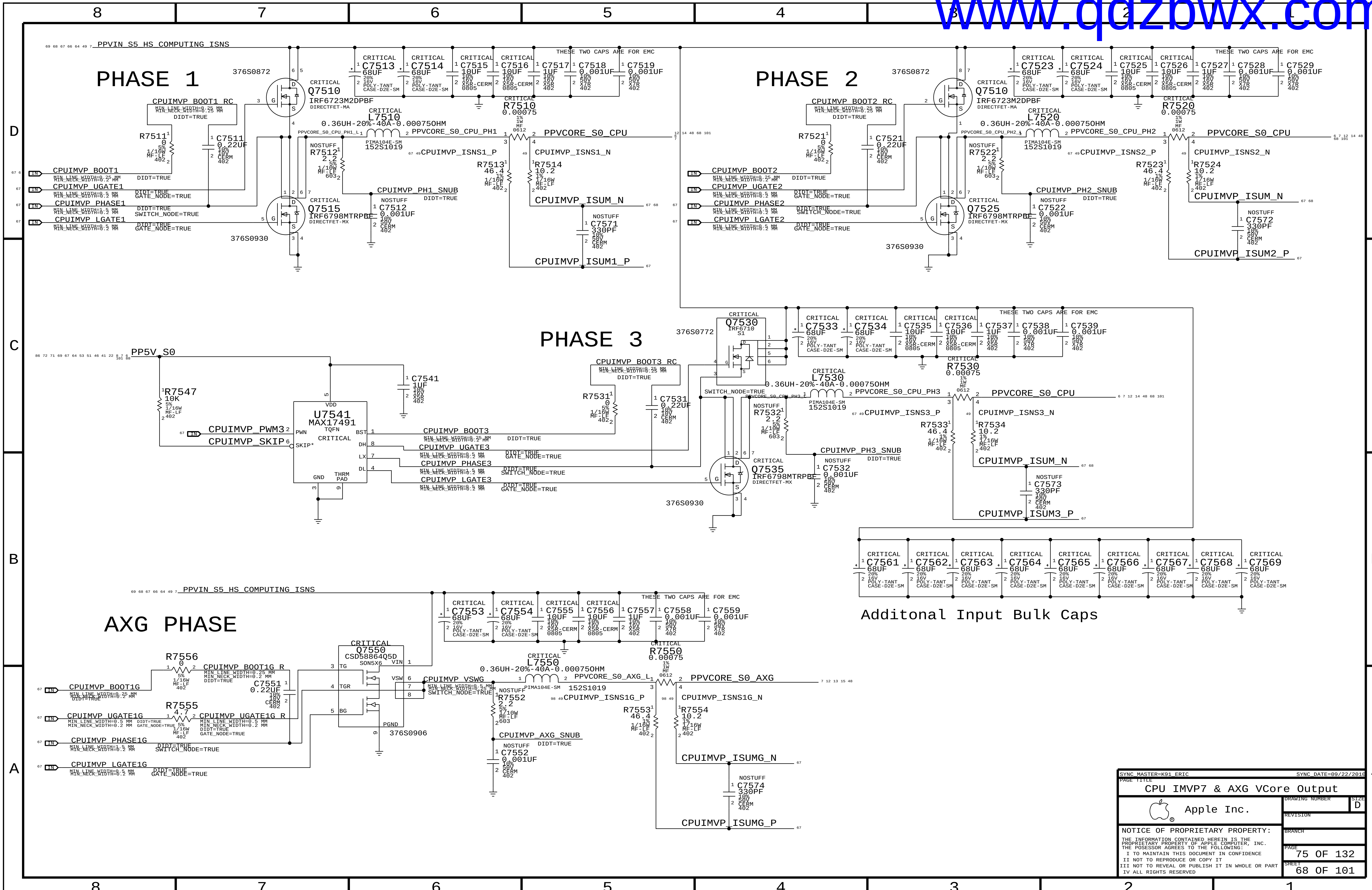
PAGE 74 OF 132

SHEET 67 OF 101


www.qdzbwx.com
PHASE 1
PHASE 2
PHASE 3
AXG PHASE
PPVIN_S5_HS_COMPUTING_ISNS
THESE TWO CAPS ARE FOR EMC
CPUIMVP_BOOT1_RC
Q7510 IRF6723M2DPBF DIRECTFET-MA
Q7515 IRF6798MTRPBF DIRECTFET-MX
L7510 0.36UH-20%-40A-0.00075OHM PIMA104E-SM 152S1019
R7510 0.00075
PPVCORE_S0_CPU_PH1
PPVCORE_S0_CPU
CPUIMVP_ISNS1_P
CPUIMVP_ISNS1_N
CPUIMVP_PH1_SNUB
CPUIMVP_ISUM_N
CPUIMVP_ISUM1_P
CPUIMVP_BOOT1
CPUIMVP_UGATE1
CPUIMVP_PHASE1
CPUIMVP_LGATE1
CPUIMVP_BOOT2_RC
Q7525 IRF6798MTRPBF
L7520
R7520 0.00075
PPVCORE_S0_CPU_PH2
CPUIMVP_ISNS2_P
CPUIMVP_ISNS2_N
CPUIMVP_PH2_SNUB
CPUIMVP_ISUM2_P
CPUIMVP_BOOT2
CPUIMVP_UGATE2
CPUIMVP_PHASE2
CPUIMVP_LGATE2
PP5V_S0
U7541 MAX17491 TQFN
CPUIMVP_PWM3
CPUIMVP_SKIP
CPUIMVP_BOOT3
CPUIMVP_UGATE3
CPUIMVP_PHASE3
CPUIMVP_LGATE3
CPUIMVP_BOOT3_RC
Q7530 IRF6710 S1
Q7535 IRF6798MTRPBF
L7530
R7530 0.00075
PPVCORE_S0_CPU_PH3
CPUIMVP_ISNS3_P
CPUIMVP_ISNS3_N
CPUIMVP_PH3_SNUB
CPUIMVP_ISUM3_P
Additonal Input Bulk Caps
Q7550 CSD58864Q5D SON5X6
CPUIMVP_BOOT1G
CPUIMVP_BOOT1G_R
CPUIMVP_UGATE1G
CPUIMVP_UGATE1G_R
CPUIMVP_PHASE1G
CPUIMVP_LGATE1G
CPUIMVP_VSWG
L7550
R7550 0.00075
PPVCORE_S0_AXG_L
PPVCORE_S0_AXG
CPUIMVP_ISNS1G_P
CPUIMVP_ISNS1G_N
CPUIMVP_AXG_SNUB
CPUIMVP_ISUMG_N
CPUIMVP_ISUMG_P
SYNC_MASTER=K91_ERIC
SYNC_DATE=09/22/2010
CPU IMVP7 & AXG VCore Output
Apple Inc.
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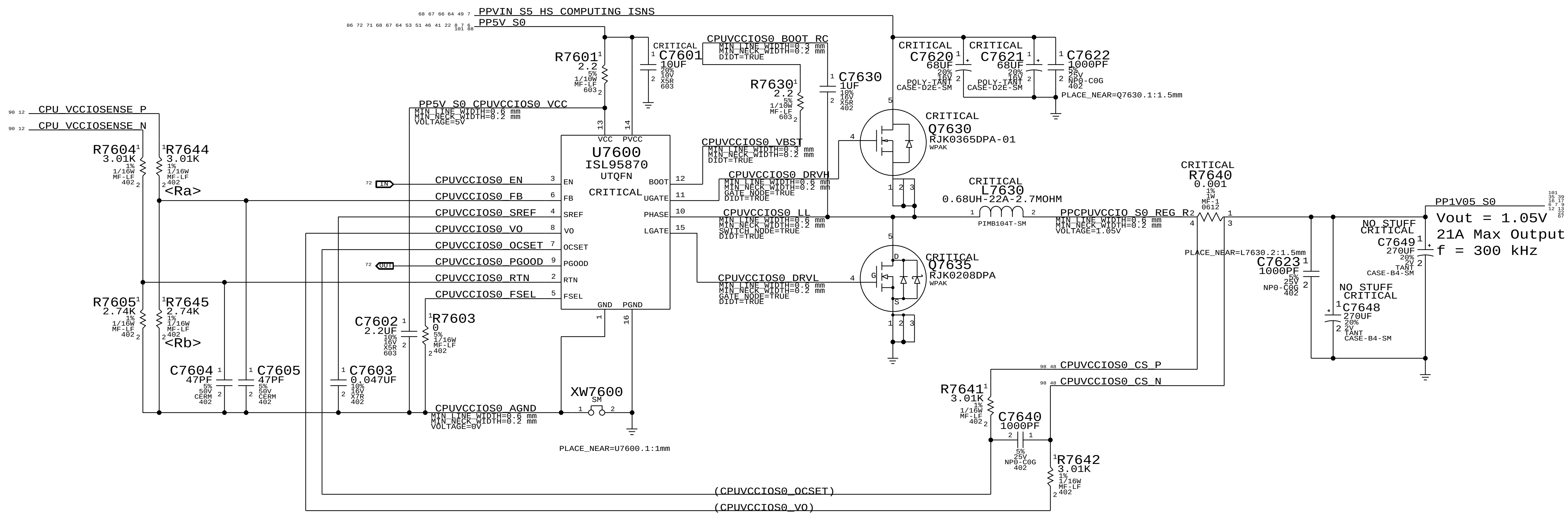
SIZE D
75 OF 132
68 OF 101

CPU VCCIO (1.05V S0) Regulator



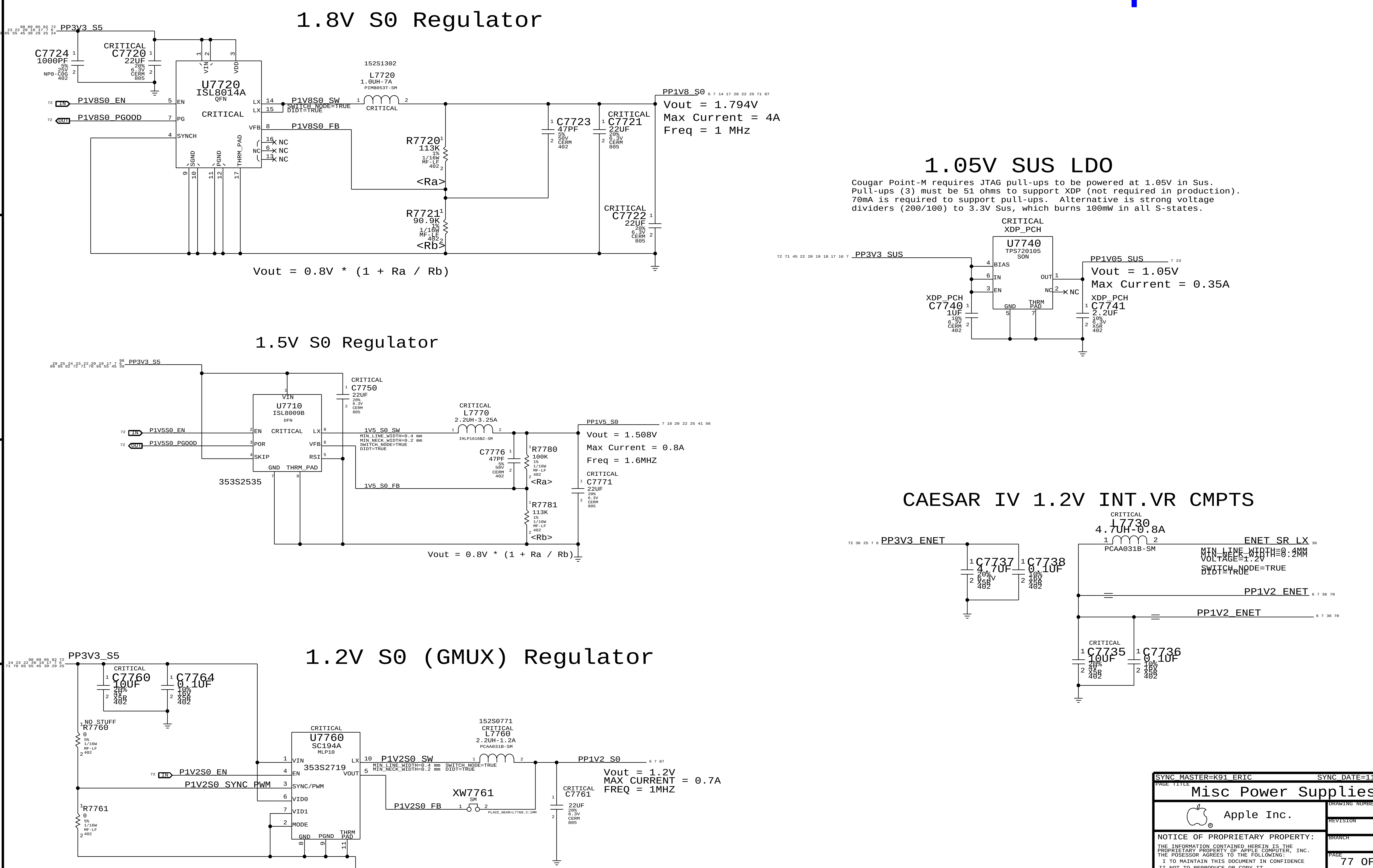
OCP = R7641 x 8.5uA / R7640
OCP = 25.6A
Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE: CPU VCCIO (1.05V) Power Supply

Apple Inc.

SIZE D



SYNC_MASTER=K91_ERIC SYNC_DATE=11/01/2010

PAGE TITLE

Misc Power Supplies

Apple Inc.

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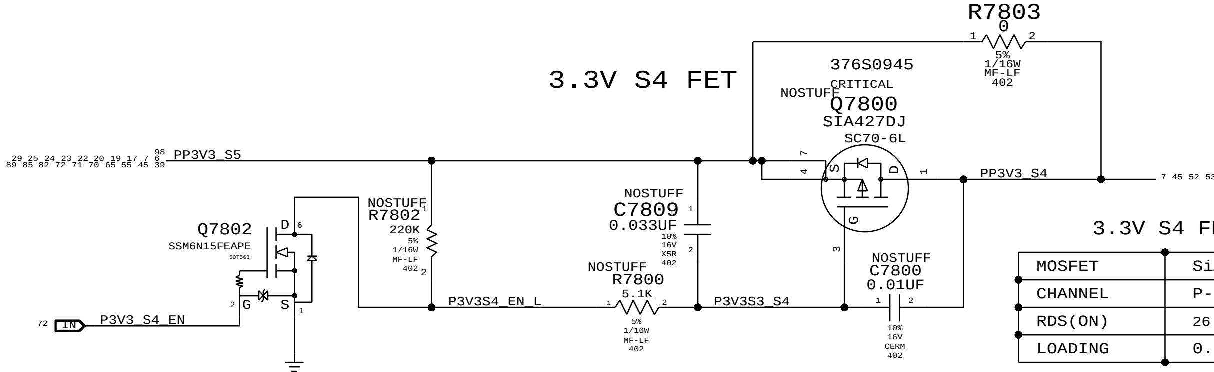
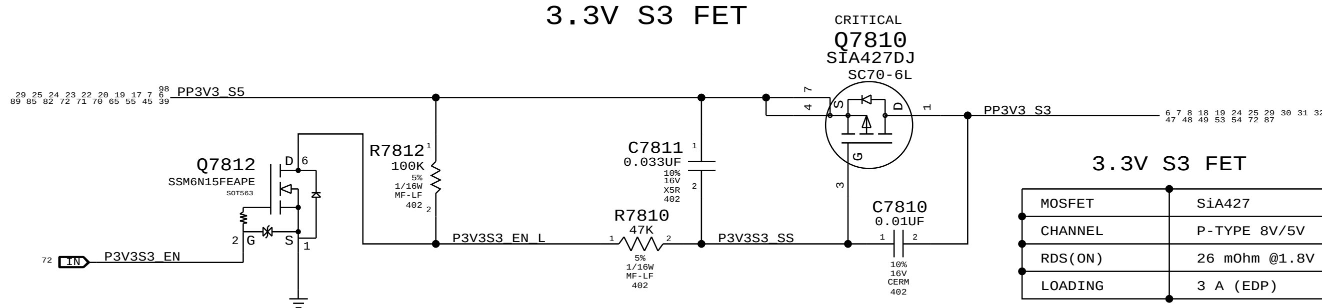
3.3V S4 FET



3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

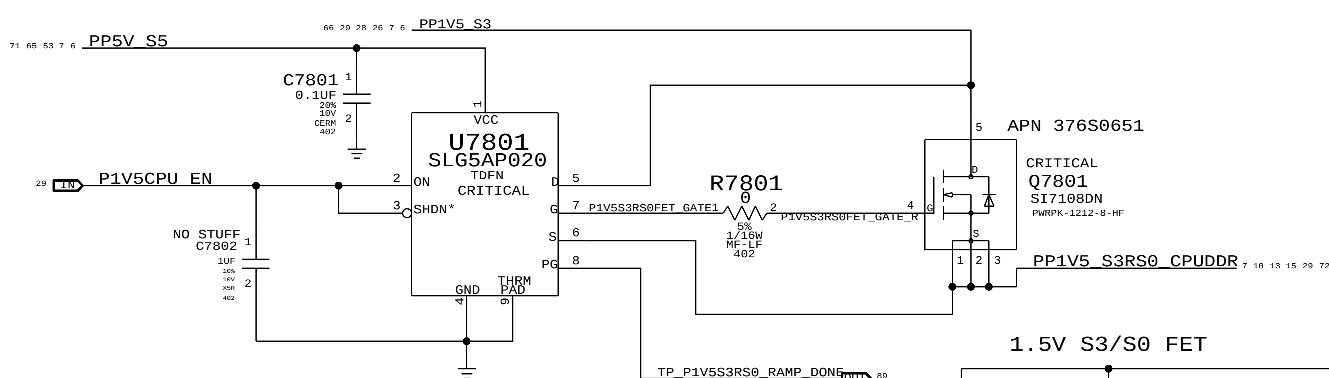
3.3V S3 FET



3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

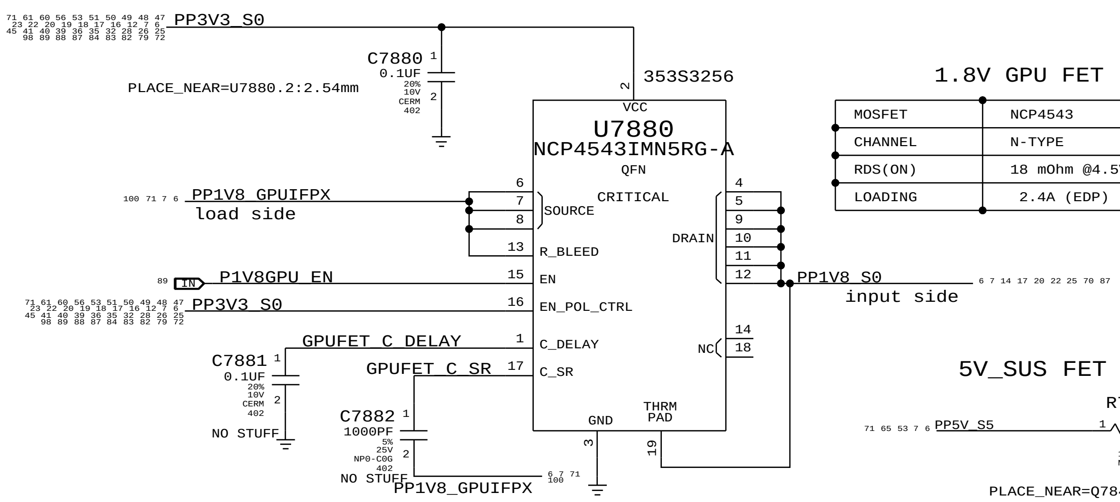
1.5V S3/S0 FET



1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

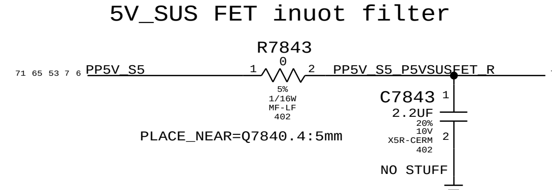
1.8V GPU FET



1.8V GPU FET

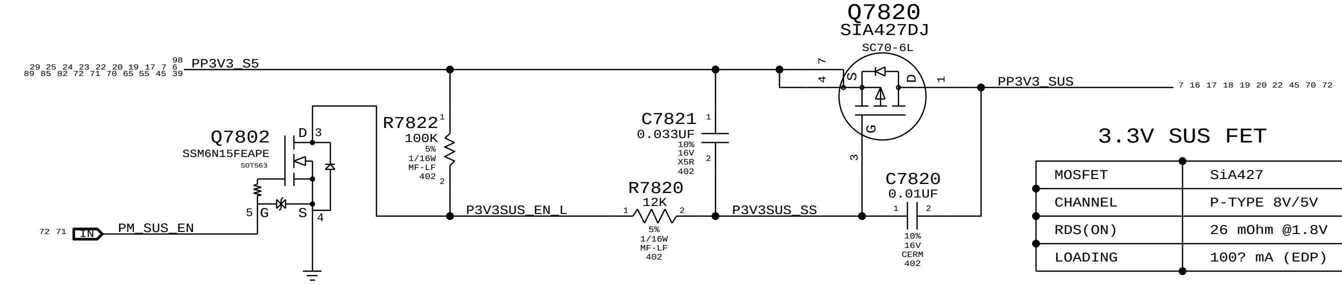
MOSFET	NCP4543
CHANNEL	N-TYPE
RDS(ON)	18 mOhm @4.5V
LOADING	2.4A (EDP)

5V_SUS FET inuot filter



U7880 default Turn on delay EN--> on is 200~650us.

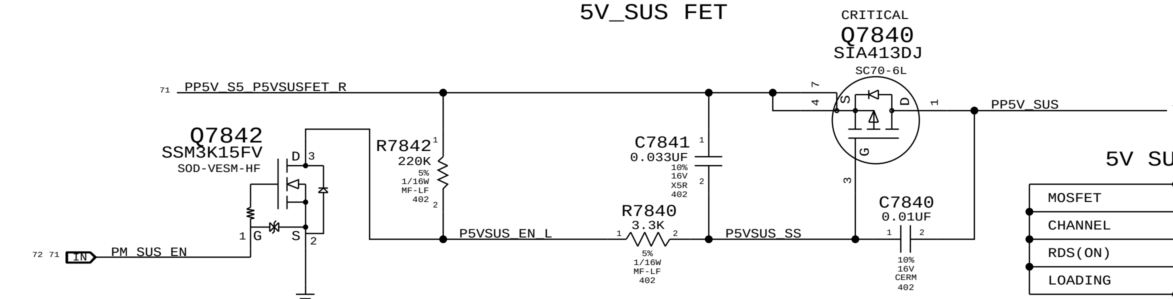
3.3V_SUS FET



3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

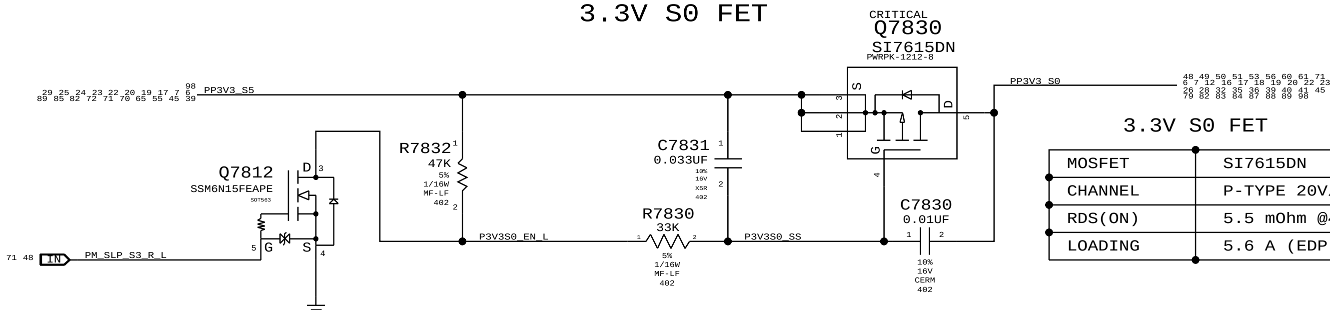
5V_SUS FET



5V SUS FET

MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

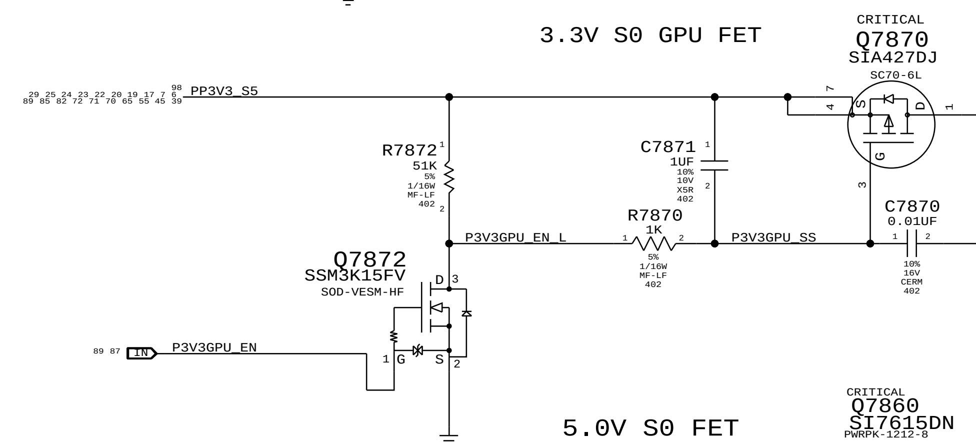
3.3V S0 FET



3.3V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

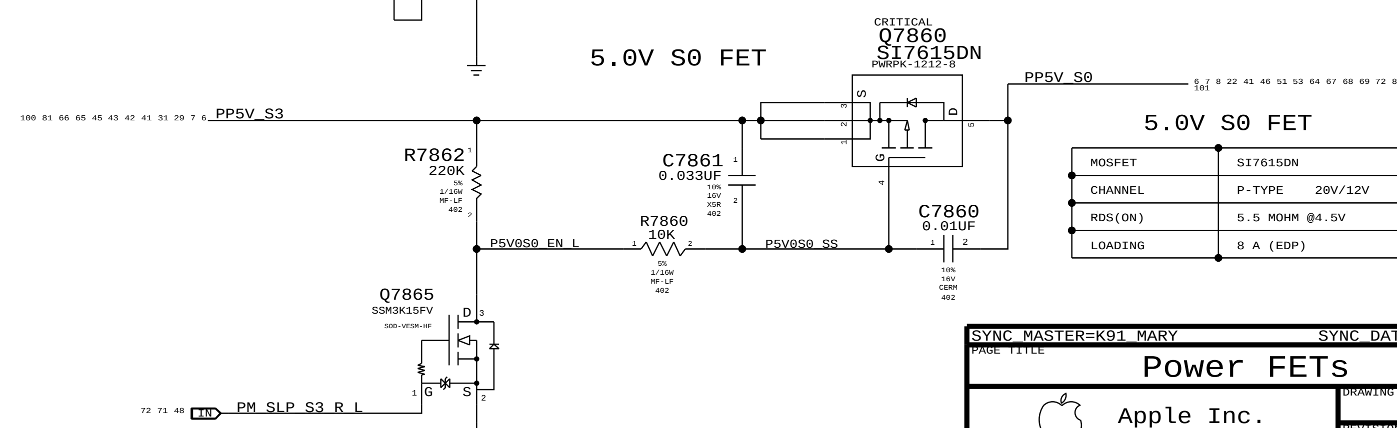
3.3V S0 GPU FET



3.3V S0 GPU FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



5.0V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	8 A (EDP)

SYNC_MASTER=K91_MARY SYNC_DATE=10/14/2010

PAGE TITLE

Power FETs

Apple Inc.

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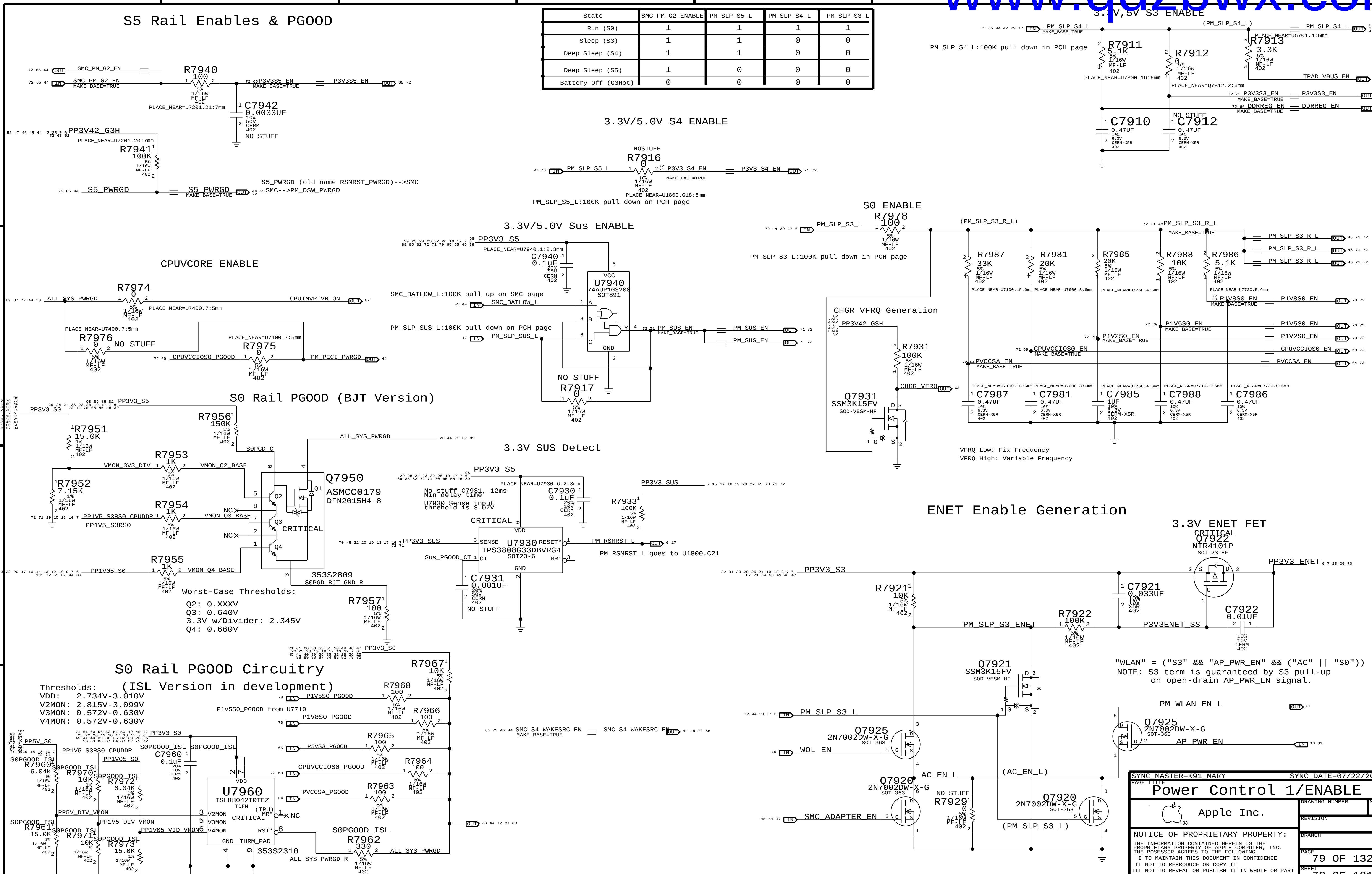

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

SYNC_MASTER=K91_MARY SYNC_DATE=07/22/2010

PAGE TITLE

Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER

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8 7 6 5 4 3 2 1

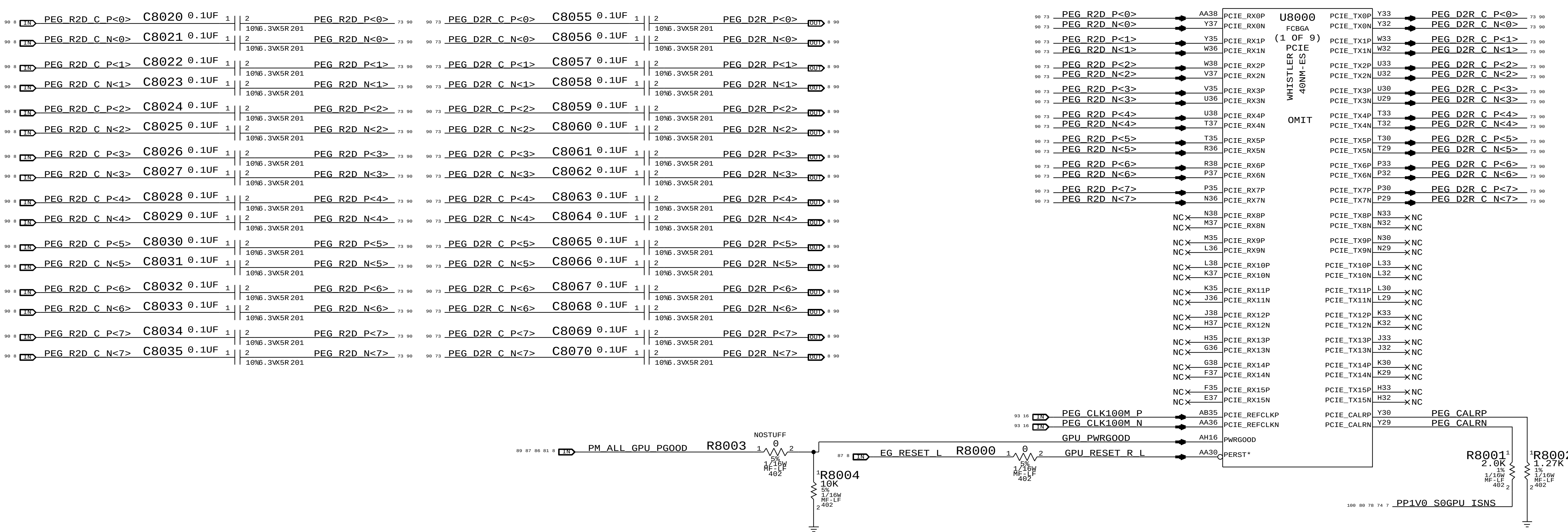
D

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



C

B

A

SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010

PAGE TITLE

Whistler PCI-E

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

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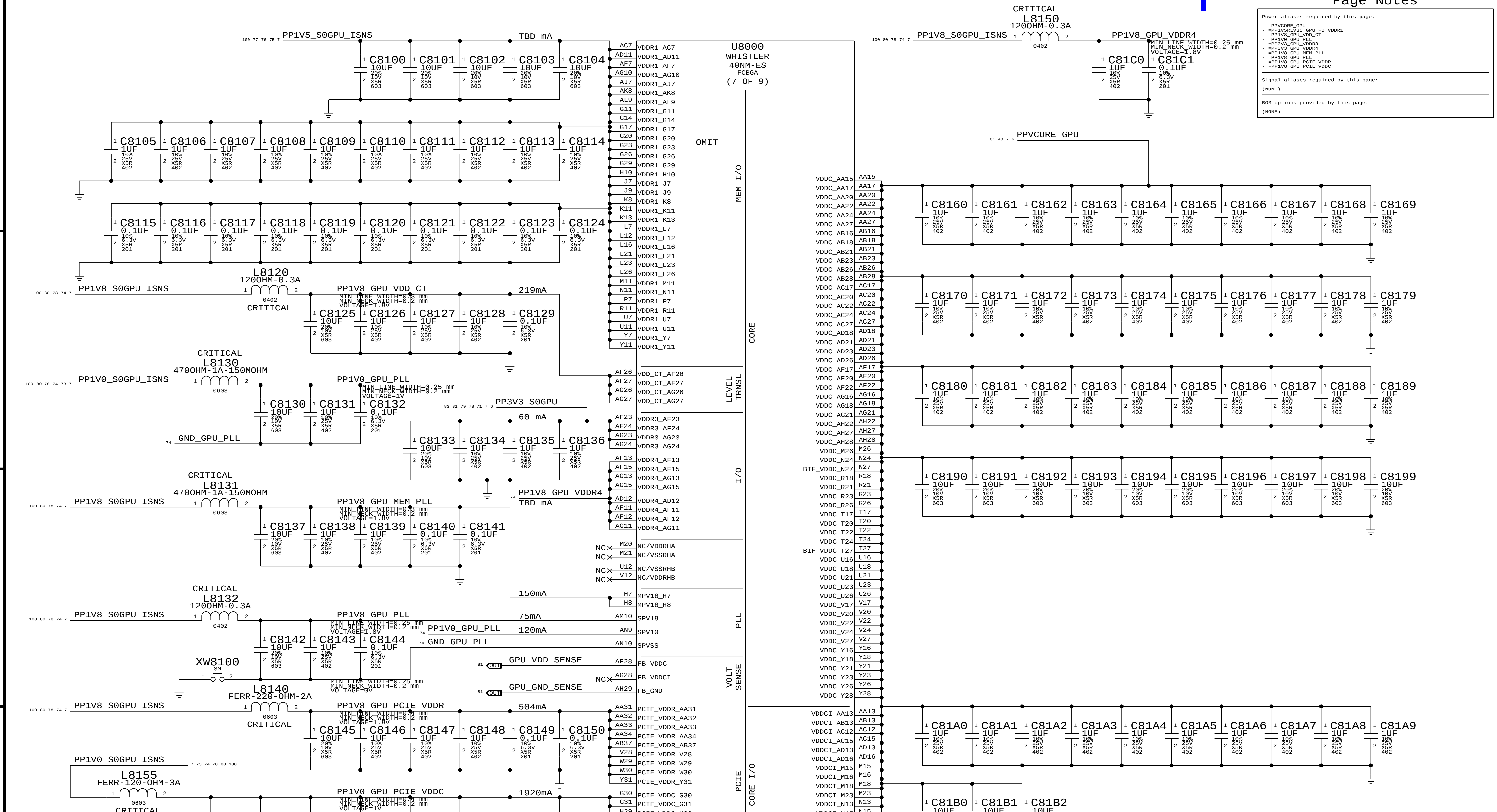
8 7 6 5 4 3 2 1



SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010

PAGE TITLE

Whistler CORE/FB POWER

Apple Inc.

DRAWING NUMBER

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REVISION

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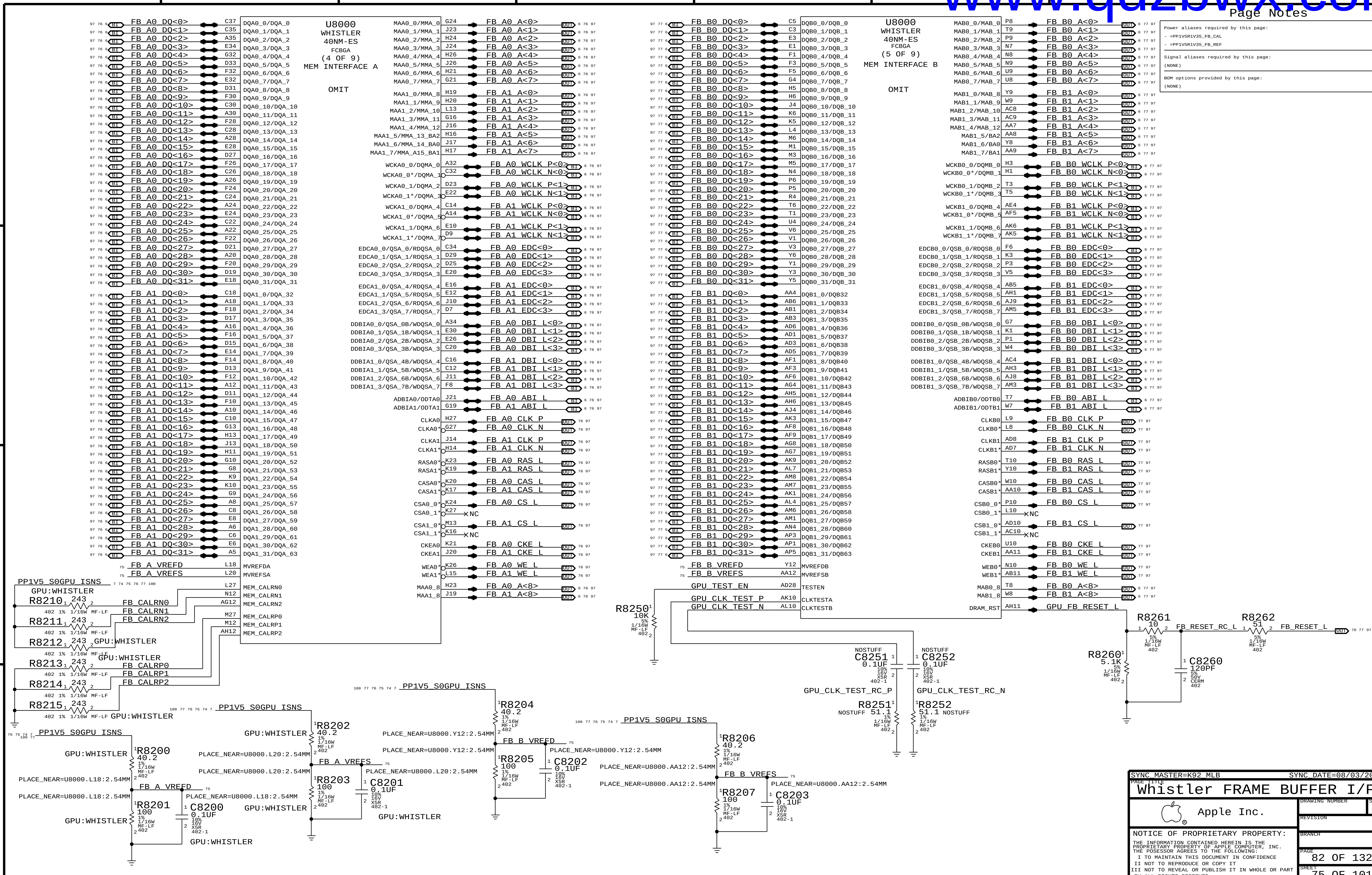

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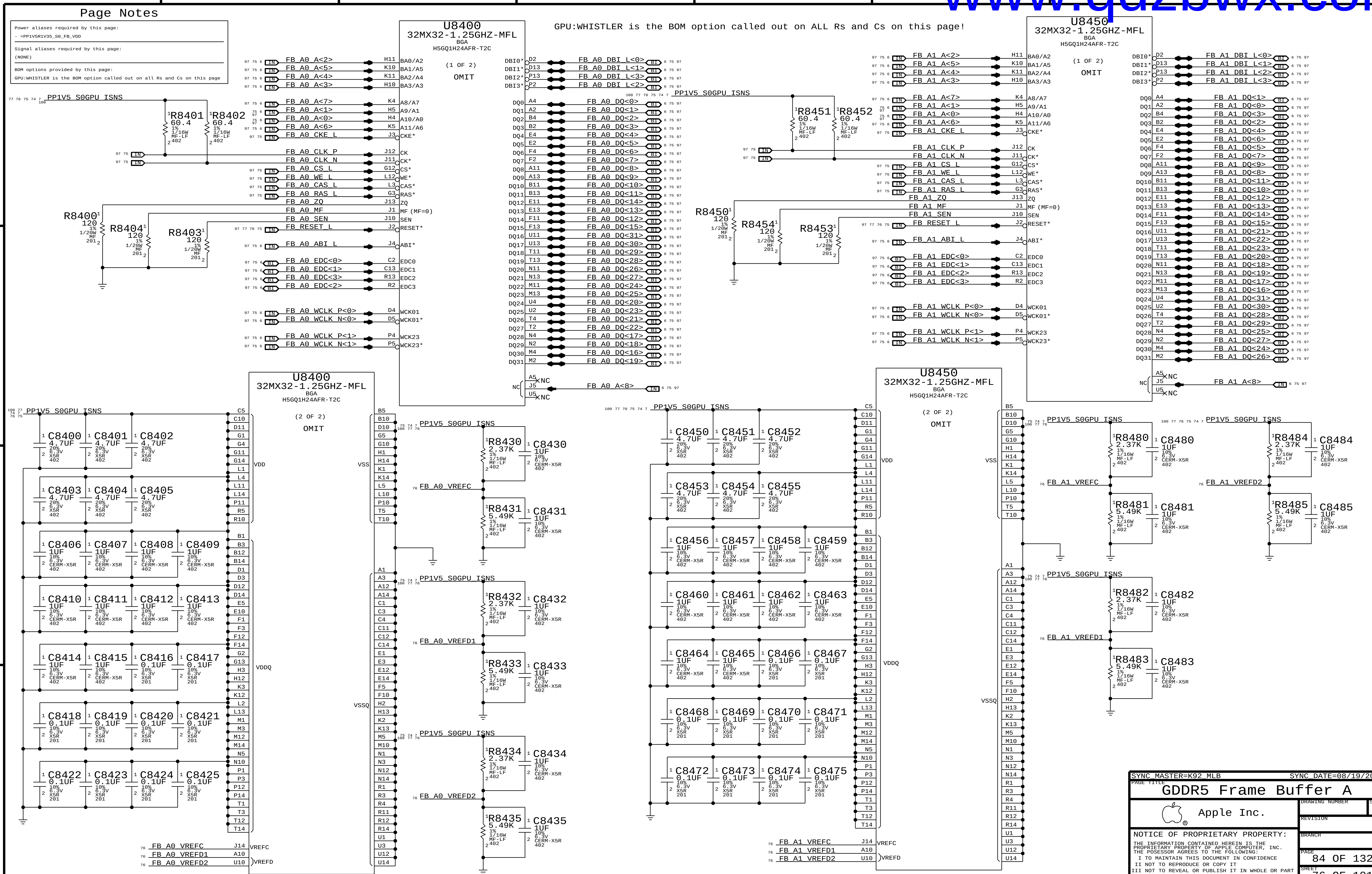
Page Notes
Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
GPU:WHISTLER is the BOM option called out on all Rs and Cs on this page
GPU:WHISTLER is the BOM option called out on ALL Rs and Cs on this page!
U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT
U8400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT
U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT
U8450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT
PP1V5_S0GPU_ISNS
FB_A0_VREFC
FB_A0_VREFD1
FB_A0_VREFD2
FB_A1_VREFC
FB_A1_VREFD1
FB_A1_VREFD2
R8400 120 1% 1/20W MF 201
R8401 60.4 1% 1/16W MF-LF 402
R8402 60.4 1% 1/16W MF-LF 402
R8403 120 1% 1/20W MF 201
R8404 120 1% 1/20W MF 201
R8430 2.37K 1% 1/16W MF-LF 402
R8431 5.49K 1% 1/16W MF-LF 402
R8432 2.37K 1% 1/16W MF-LF 402
R8433 5.49K 1% 1/16W MF-LF 402
R8434 2.37K 1% 1/16W MF-LF 402
R8435 5.49K 1% 1/16W MF-LF 402
R8450 120 1% 1/20W MF 201
R8451 60.4 1% 1/16W MF-LF 402
R8452 60.4 1% 1/16W MF-LF 402
R8453 120 1% 1/20W MF 201
R8454 120 1% 1/20W MF 201
R8480 2.37K 1% 1/16W MF-LF 402
R8481 5.49K 1% 1/16W MF-LF 402
R8482 2.37K 1% 1/16W MF-LF 402
R8483 5.49K 1% 1/16W MF-LF 402
R8484 2.37K 1% 1/16W MF-LF 402
R8485 5.49K 1% 1/16W MF-LF 402
C8400 C8401 C8402 C8403 C8404 C8405 4.7UF 20% 6.3V X5R 402
C8406 C8407 C8408 C8409 C8410 C8411 C8412 C8413 C8414 C8415 1UF 10% 6.3V CERM-X5R 402
C8416 C8417 C8418 C8419 C8420 C8421 C8422 C8423 C8424 C8425 0.1UF 10% 6.3V X5R 201
C8430 C8431 C8432 C8433 C8434 C8435 1UF 10% 6.3V CERM-X5R 402
C8450 C8451 C8452 C8453 C8454 C8455 4.7UF 20% 6.3V X5R 402
C8456 C8457 C8458 C8459 C8460 C8461 C8462 C8463 C8464 C8465 1UF 10% 6.3V CERM-X5R 402
C8466 C8467 C8468 C8469 C8470 C8471 C8472 C8473 C8474 C8475 0.1UF 10% 6.3V X5R 201
C8480 C8481 C8482 C8483 C8484 C8485 1UF 10% 6.3V CERM-X5R 402
FB_A0_A<0>…FB_A0_A<8>
FB_A0_CKE_L FB_A0_CLK_P FB_A0_CLK_N FB_A0_CS_L FB_A0_WE_L FB_A0_CAS_L FB_A0_RAS_L FB_A0_ZQ FB_A0_MF FB_A0_SEN FB_A0_RESET_L FB_A0_ABI_L
FB_A0_EDC<0>…FB_A0_EDC<3>
FB_A0_WCLK_P<0> FB_A0_WCLK_N<0> FB_A0_WCLK_P<1> FB_A0_WCLK_N<1>
FB_A0_DBI_L<0>…FB_A0_DBI_L<3>
FB_A0_DQ<0>…FB_A0_DQ<31>
FB_A1_A<0>…FB_A1_A<8>
FB_A1_CKE_L FB_A1_CLK_P FB_A1_CLK_N FB_A1_CS_L FB_A1_WE_L FB_A1_CAS_L FB_A1_RAS_L FB_A1_ZQ FB_A1_MF FB_A1_SEN FB_A1_RESET_L FB_A1_ABI_L
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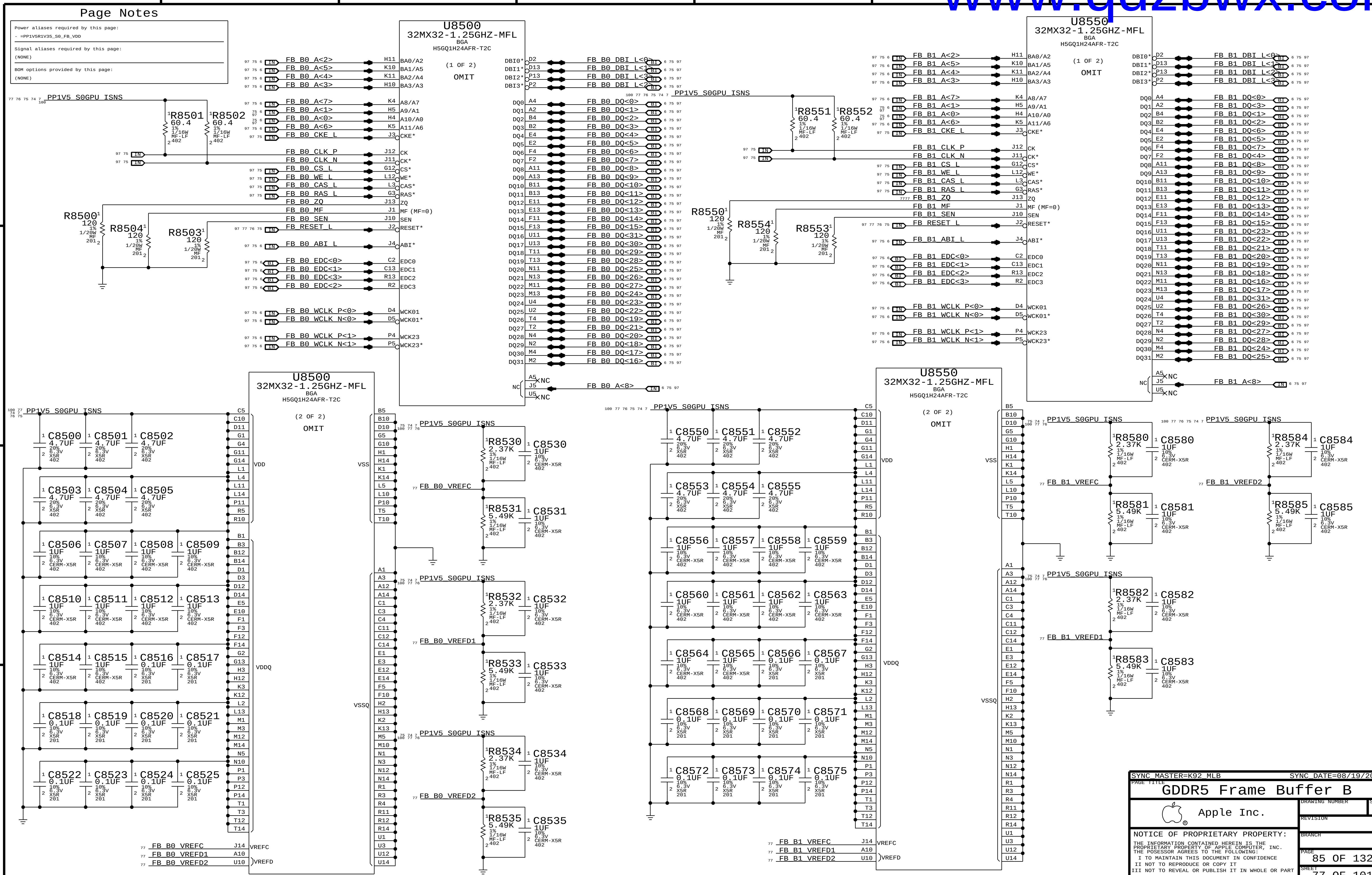
FB_A1_WCLK_P<0> FB_A1_WCLK_N<0> FB_A1_WCLK_P<1> FB_A1_WCLK_N<1>
FB_A1_DBI_L<0>…FB_A1_DBI_L<3>
FB_A1_DQ<0>…FB_A1_DQ<31>
VDD VDDQ VSS VSSQ VREFC VREFD
SYNC_MASTER=K92_MLB
SYNC_DATE=08/19/2010
PAGE TITLE
GDDR5 Frame Buffer A
DRAWING NUMBER
SIZE D
Apple Inc.
REVISION
BRANCH
PAGE 84 OF 132
SHEET 76 OF 101



SYNC_MASTER=K92_MLB SYNC_DATE=08/19/2010

PAGE TITLE

GDDR5 Frame Buffer B

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VRAM BOM OPTION TABLE

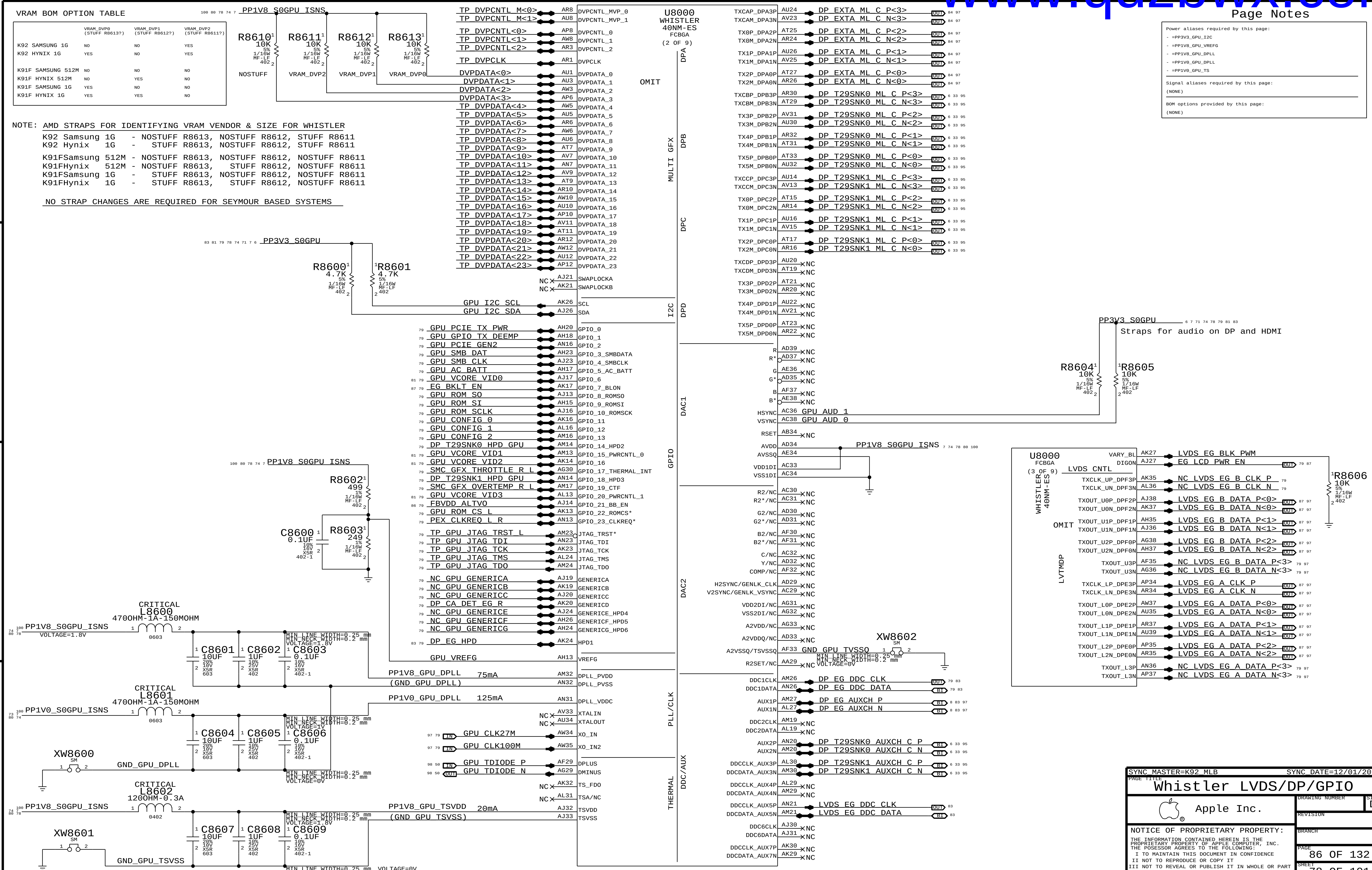
	VRAM_DVP0 (STUFF R8613?)	VRAM_DVP1 (STUFF R8612?)	VRAM_DVP2 (STUFF R8611?)
K92 SAMSUNG 1G	NO	NO	YES
K92 HYNIX 1G	YES	NO	YES
K91F SAMSUNG 512M	NO	NO	NO
K91F HYNIX 512M	NO	YES	NO
K91F SAMSUNG 1G	YES	NO	NO
K91F HYNIX 1G	YES	YES	NO

NOTE: AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611
K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611

K91FSamsung 512M - NOSTUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 512M - NOSTUFF R8613, STUFF R8612, NOSTUFF R8611
K91FSamsung 1G - STUFF R8613, NOSTUFF R8612, NOSTUFF R8611
K91FHynix 1G - STUFF R8613, STUFF R8612, NOSTUFF R8611

NO STRAP CHANGES ARE REQUIRED FOR SEYMOUR BASED SYSTEMS



Page Notes

Power aliases required by this page:

- =PP3V3_GPU_I2C
- =PP1V8_GPU_VREFG
- =PP1V8_GPU_DPLL
- =PP1V0_GPU_DPLL
- =PP1V0_GPU_TS

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC_MASTER=K92_MLB SYNC_DATE=12/01/2010

PAGE TITLE

Whistler LVDS/DP/GPIO

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SIZE D

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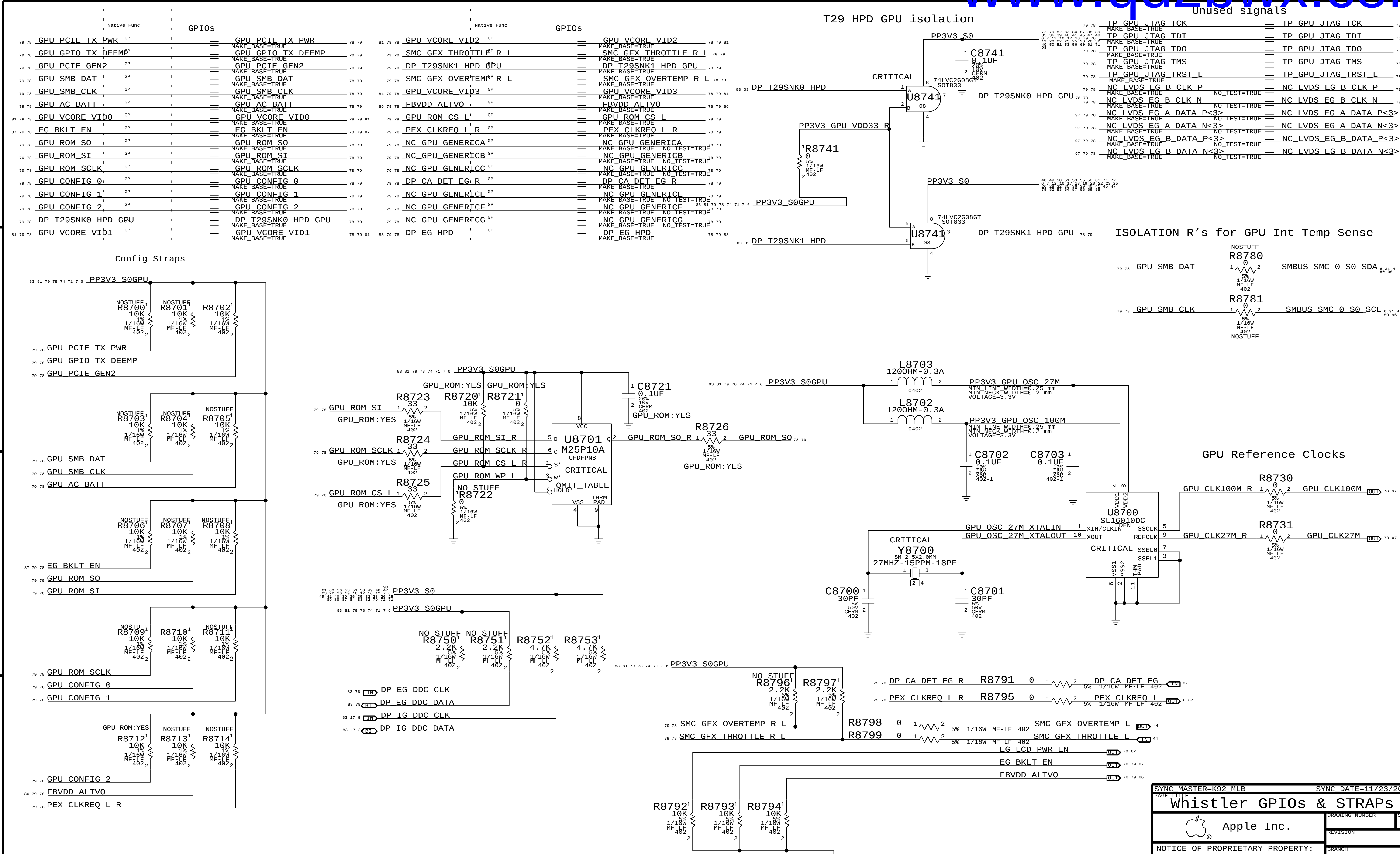
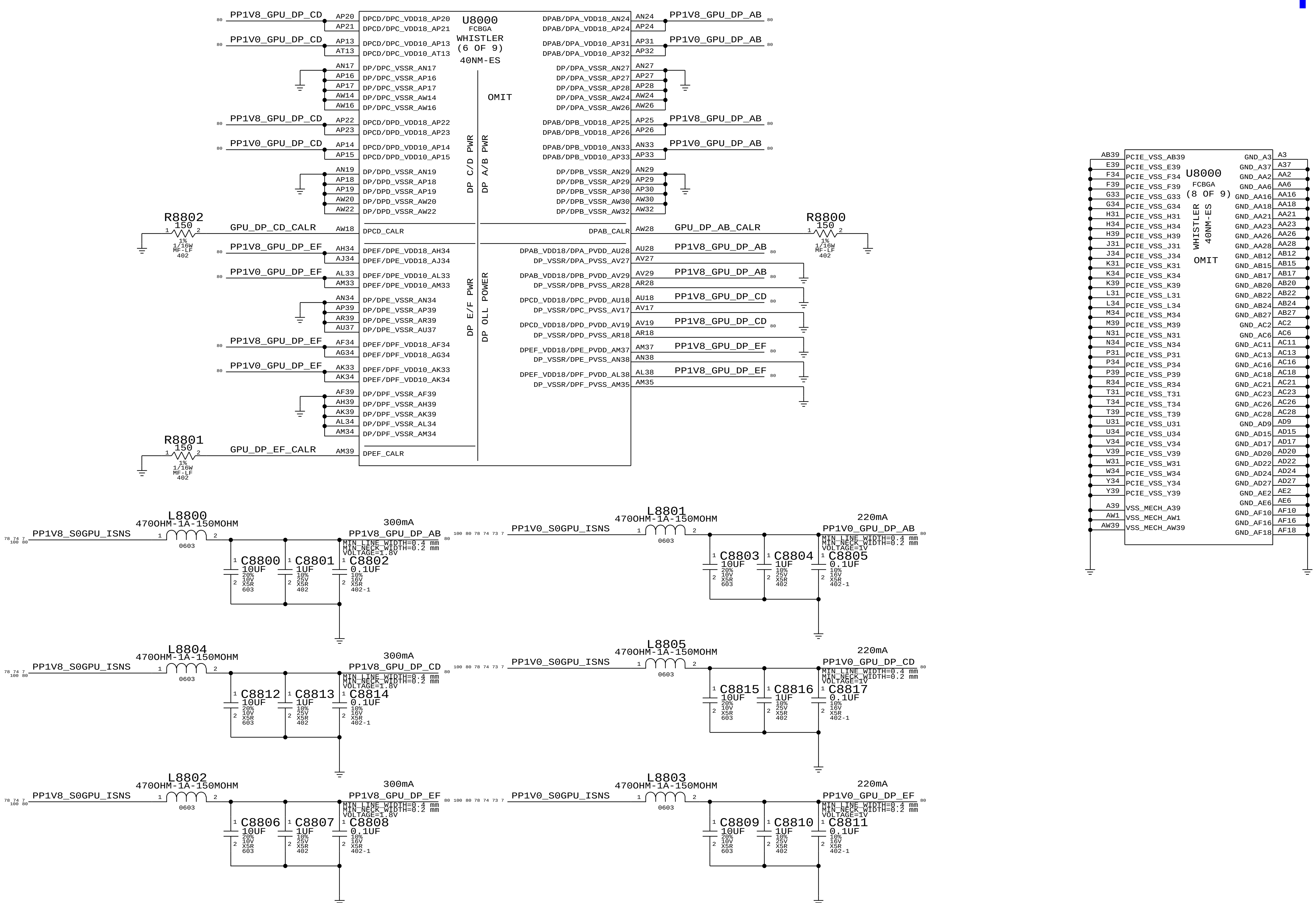


SYNC_MASTER=K92_MLB SYNC_DATE=11/23/2010

Whistler GPIOs & STRAPS

Apple Inc.

SIZE D



Page Notes

Power aliases required by this page:

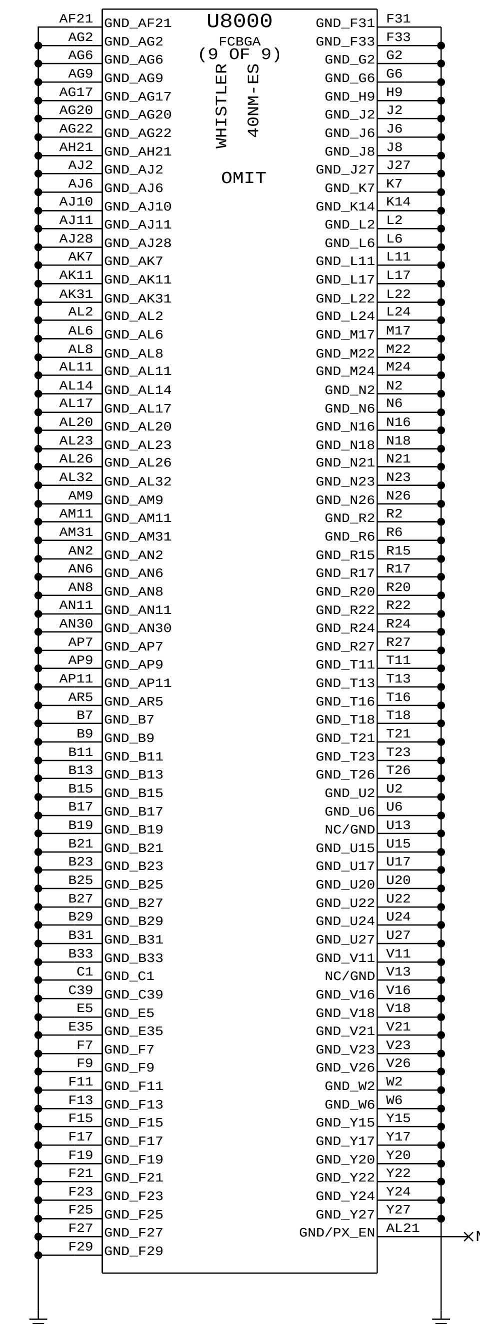
- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



SYNC_MASTER=K92_SUMA SYNC_DATE=06/15/2010

PAGE TITLE

Whistler DP PWR/GNDs

Apple Inc.

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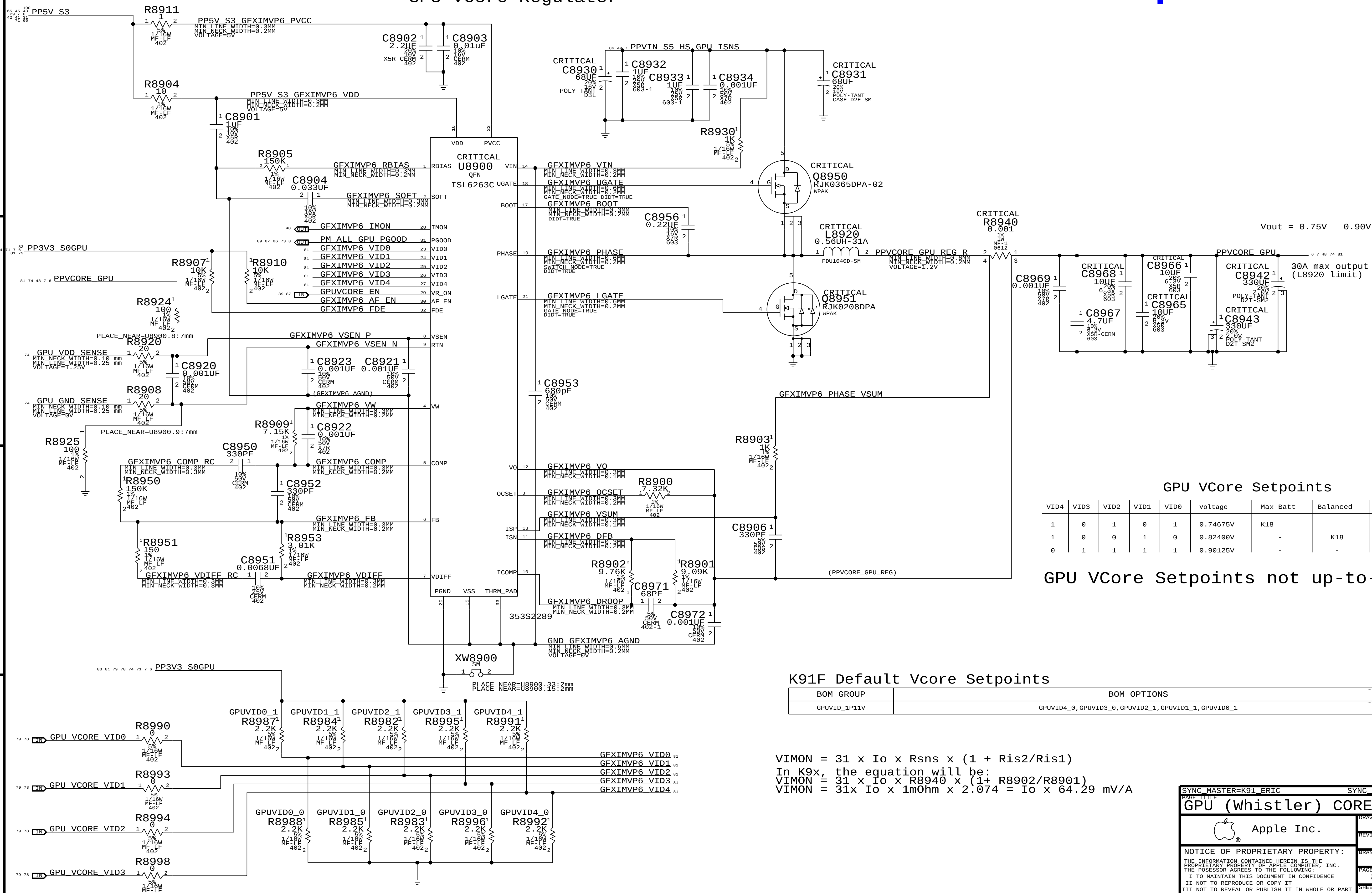
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

GPU VCore Setpoints not up-to-date!

K91F Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0,GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_1

VIMON = 31 x Io x Rsns x (1 + Ris2/Ris1)

In K9x, the equation will be:

VIMON = 31 x Io x R8940 x (1+ R8902/R8901)

VIMON = 31x Io x 1mOhm x 2.074 = Io x 64.29 mV/A

SYNC_MASTER=K91_ERIC SYNC_DATE=12/21/2010

PAGE TITLE

GPU (Whistler) CORE SUPPLY

Apple Inc.

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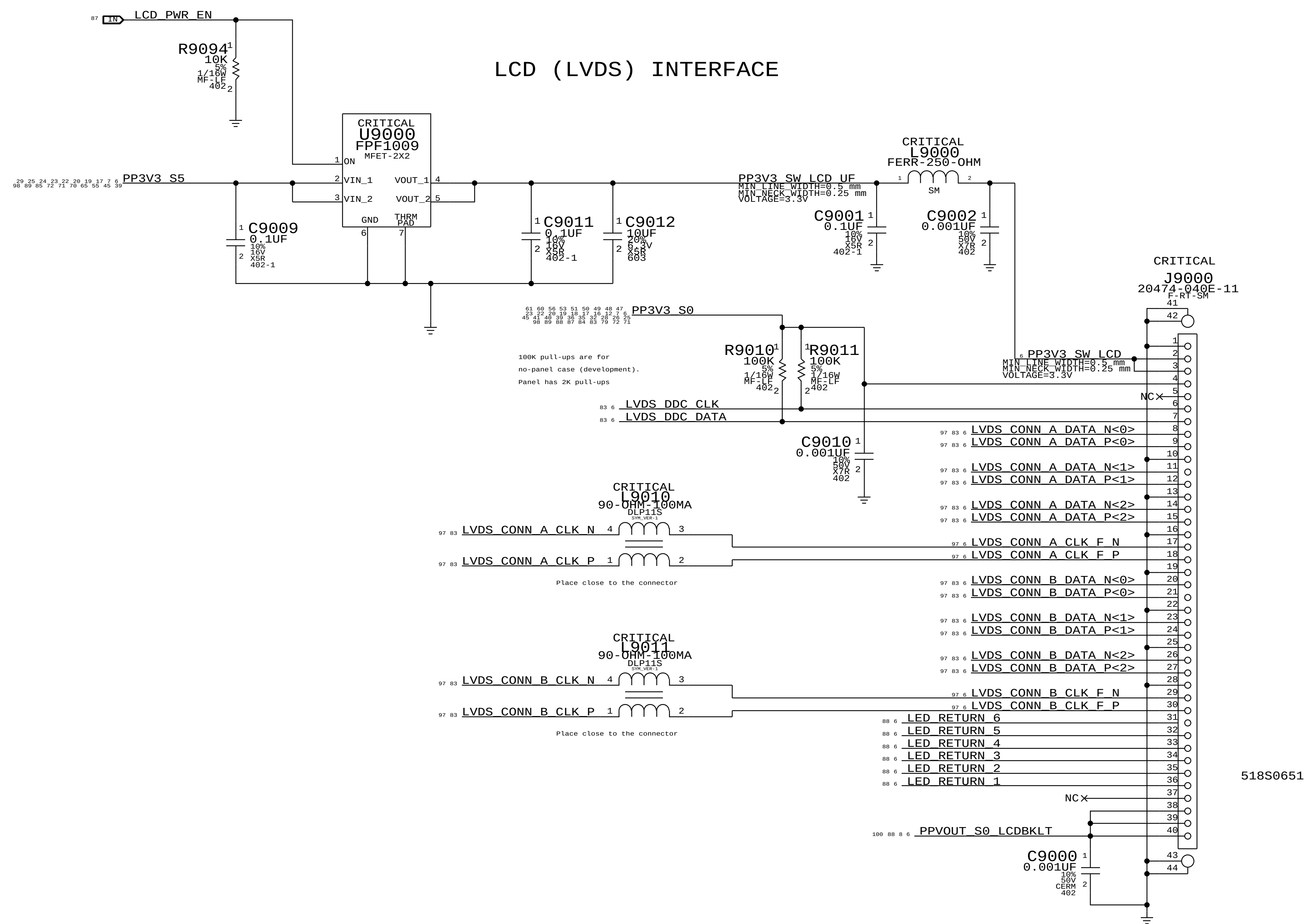
NOTICE OF PROPRIETARY PROPERTY:

LCD (LVDS) INTERFACE



SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

LVDS Display Connector

Apple Inc.

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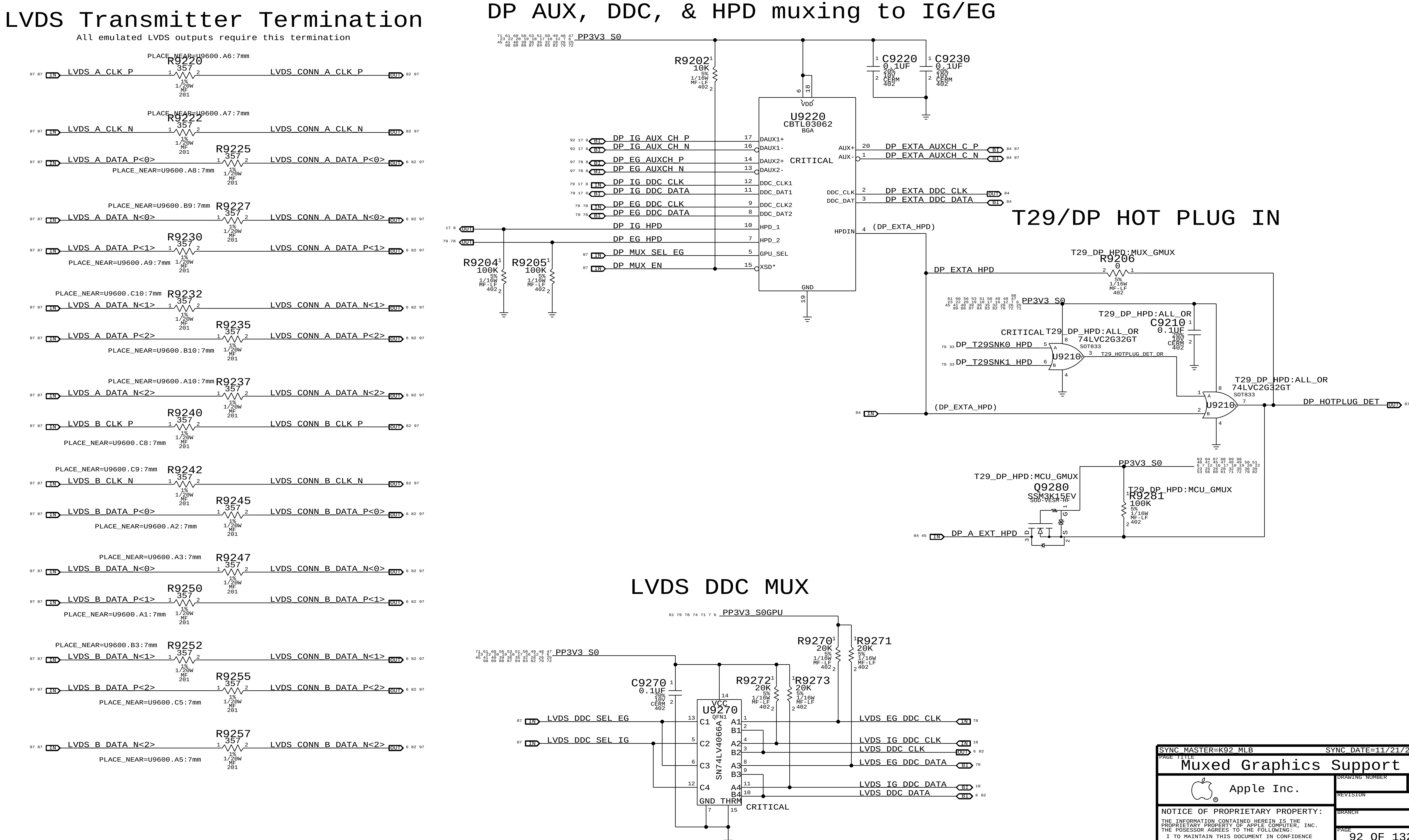


SYNC_MASTER=K92_MLB SYNC_DATE=11/21/2010

PAGE TITLE

Muxed Graphics Support

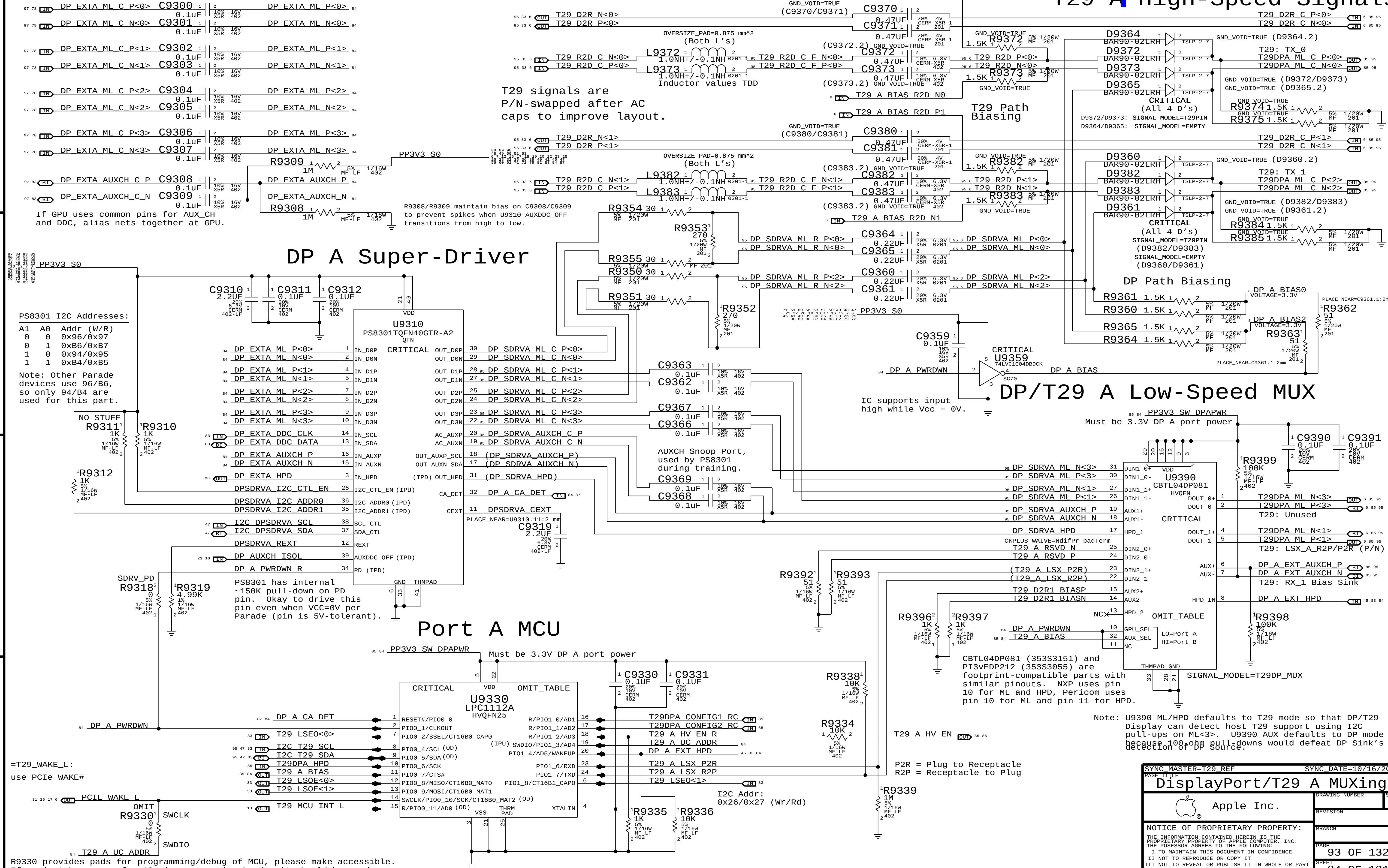
Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

BRANCH

T29 A High-Speed Signals



SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

PAGE TITLE: DisplayPort/T29 A MUXing

Apple Inc.

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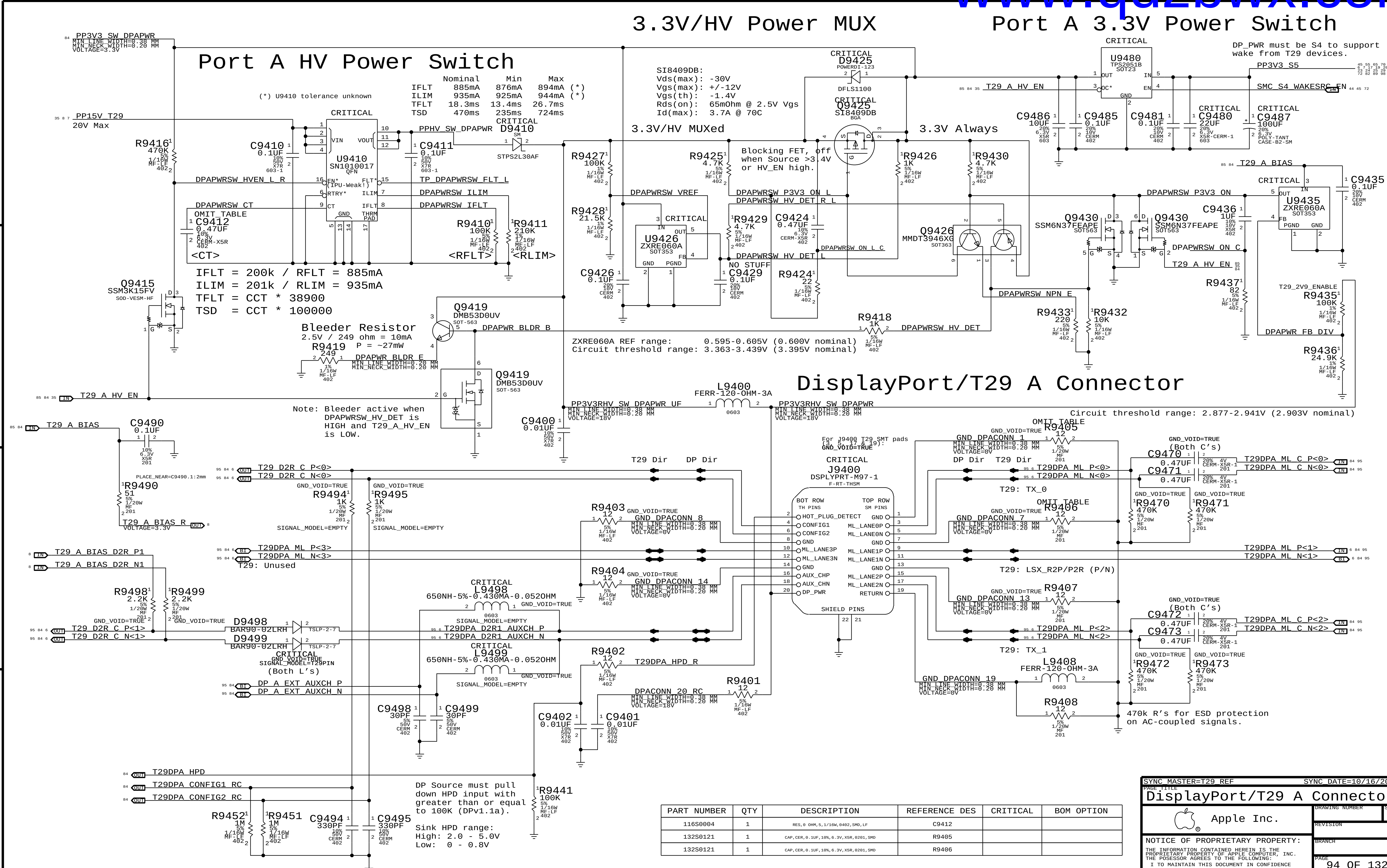

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0 OHM,5,1/16W,0402,SMD,LF	C9412		
132S0121	1	CAP,CER,0.1UF,10%,6.3V,X5R,0201,SMD	R9405		
132S0121	1	CAP,CER,0.1UF,10%,6.3V,X5R,0201,SMD	R9406		

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

PAGE TITLE

DisplayPort/T29 A Connector

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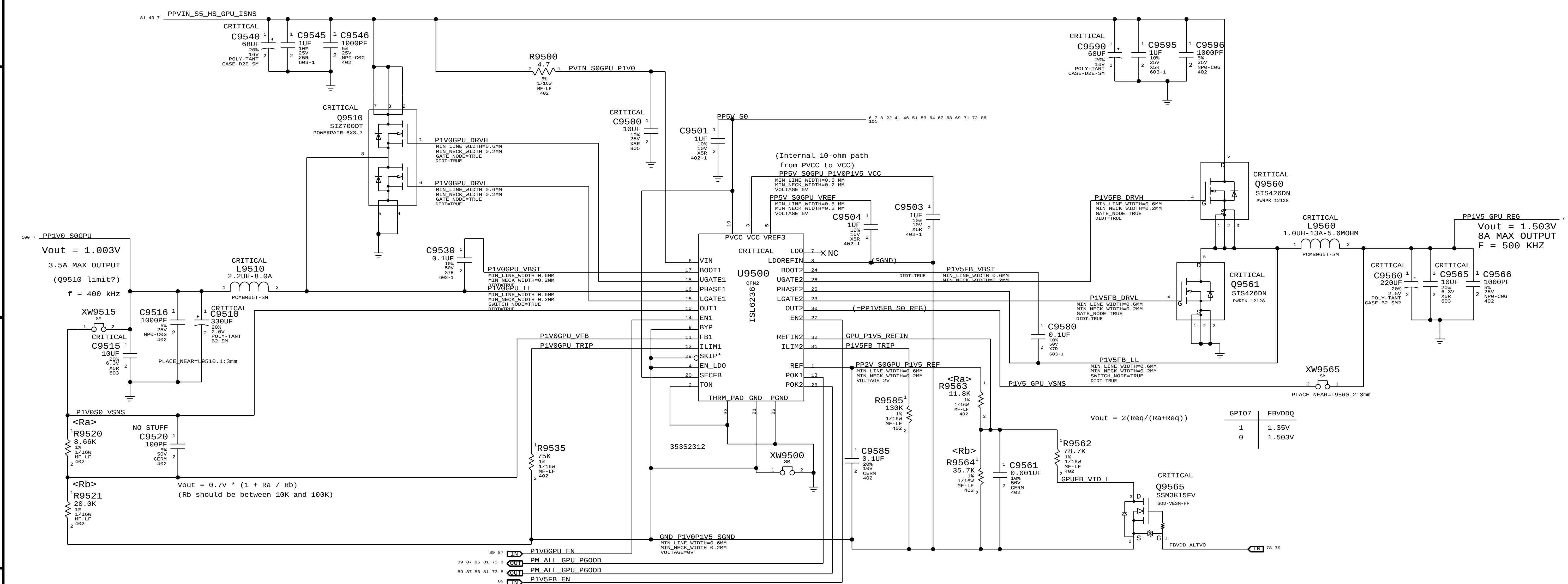

SYNC_MASTER=K91_ERIC SYNC_DATE=10/08/2010

PAGE TITLE

1V0 GPU / 1V5 FB Power Supply

Apple Inc.

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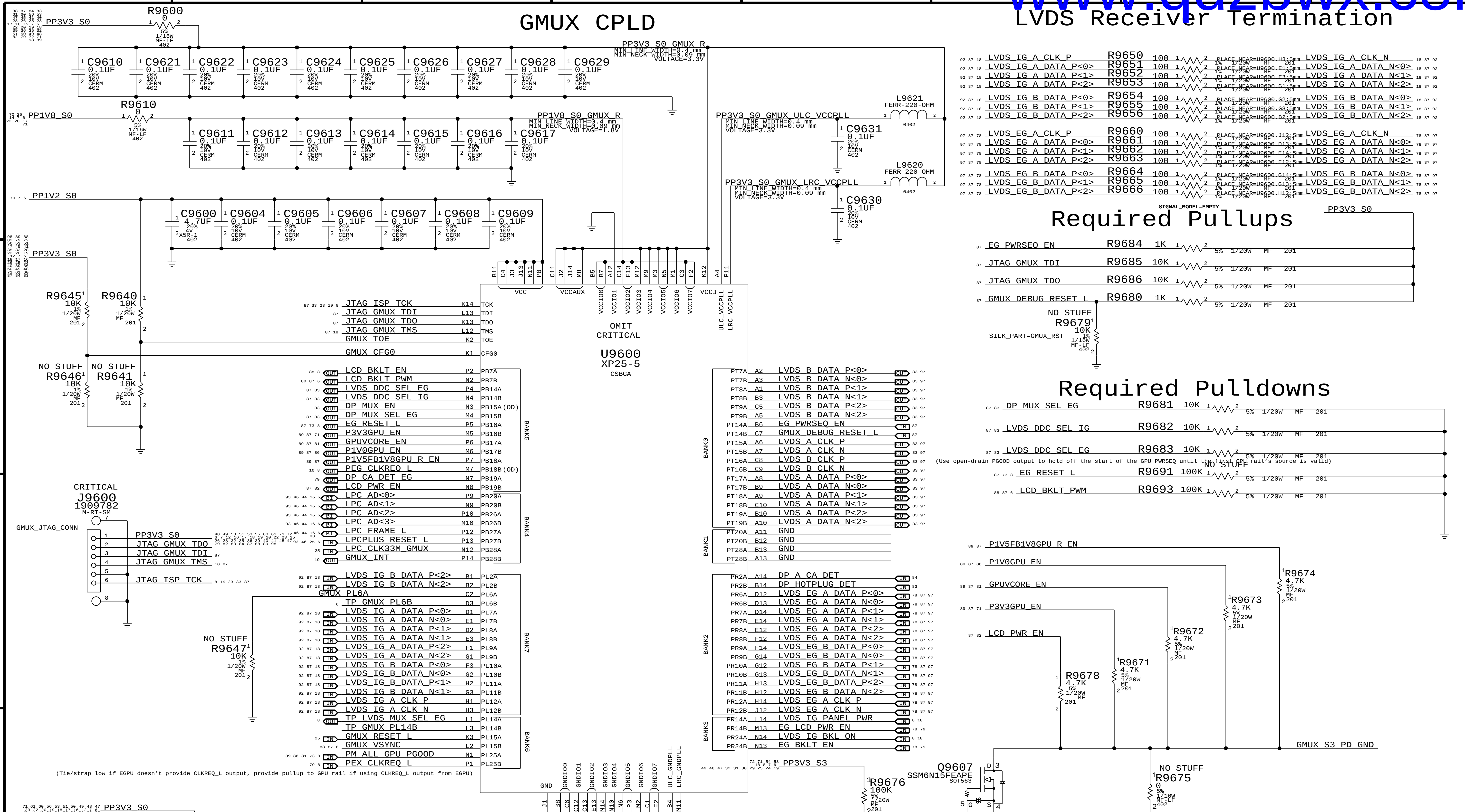

SYNC_MASTER=K91_MARY SYNC_DATE=08/03/2010

PAGE TITLE

Graphics MUX (GMUX)

Apple Inc.

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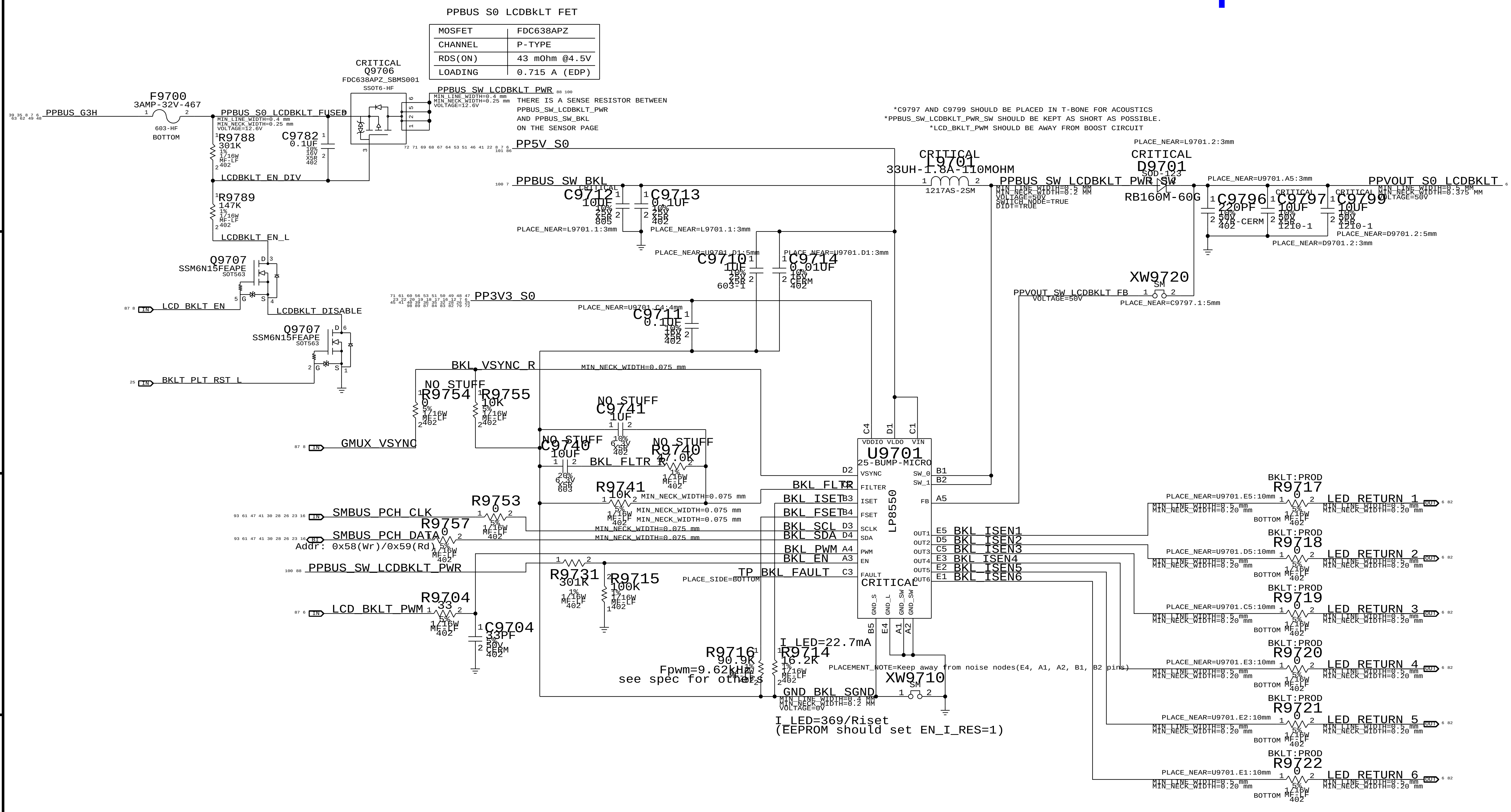

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=K901_KIRAN SYNC_DATE=06/25/2010

LCD Backlight Driver

Apple Inc.

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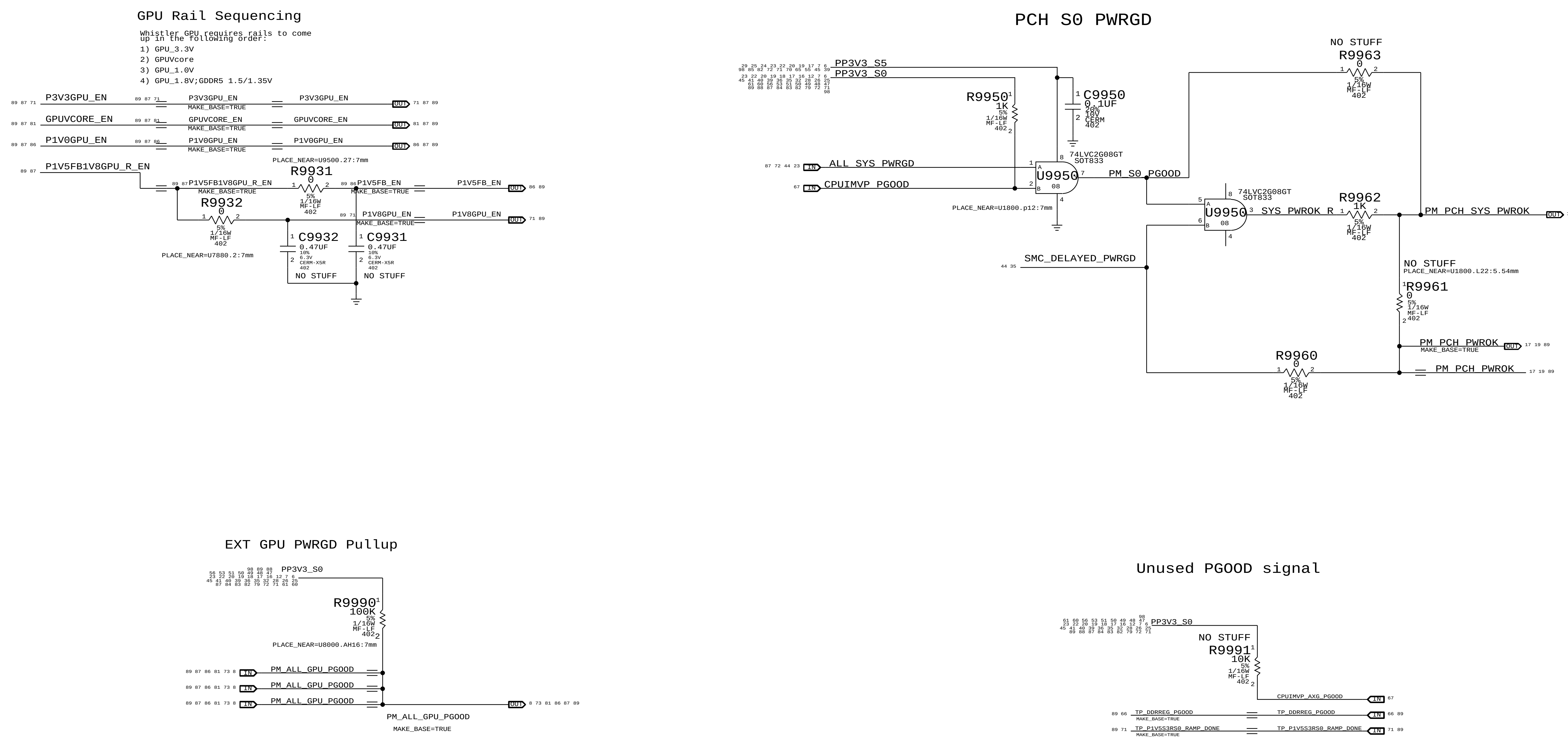

SYNC_MASTER=K91_MARY SYNC_DATE=08/03/2010

PAGE TITLE

Power Sequencing EG/PCH S0

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
	DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
	DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
	DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
	FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	6 9 17
	FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	6 9 17
		CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	6 9 17
		CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	6 9 17
I125	DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
I126		CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
		CPU_50S	CPU_AGTL	FDI_INT	6 9 17
	CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 44
	PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
	PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 29
	XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
	XDP_BDRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
	XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	XDP_PREQ_l	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	
	CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
I124	CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	9 23
	CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
I115		CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 17
		CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 45 67
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
	XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
	XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
	XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
	XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
	XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
	XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
		CPU_55S	CPU_8MIL	CPU_PSI_L	
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
		CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
		CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
	XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
	XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
	XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
	XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
	XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
		CPU_55S	CPU_8MIL	CPU_VID<6..0>	8
		CPU_50S	CPU_AGTL	CPUIMVP_IMON	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 67
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 67
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 69
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 69
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 67
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 67
I120		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	12
I121		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	12
I122		CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	12
I123		CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	12
		CPU_55S	CPU_8MIL	GFX_VID<6..0>	8
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
		CPU_50S	CPU_AGTL	GFX_VR_EN	
		CPU_50S	CPU_AGTL	GFXIMVP_IMON	
		PCIE_85D	PCIE	PEG_R2D_P<7..0>	73
		PCIE_85D	PCIE	PEG_R2D_N<7..0>	73
	PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	8 73
		PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	8 73
	PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	8 73
		PCIE_85D	PCIE	PEG_D2R_N<7..0>	8 73
		PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	73
		PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	73
		CPU_50S	CPU_VID	CPU_VIDSOUT	12 67
		CPU_50S	CPU_VID	CPU_VIDSCLK	12 67
		CPU_50S	CPU_VID	CPU_VIDALERT_L	12 67

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE
CPU Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	6 11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	6 11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	6 11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	6 11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	6 11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	6 11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	6 11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	6 11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	6 11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	6 11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	6 11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	6 11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	6 11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	6 11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	6 11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	6 11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	6 11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	6 11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	6 11 26 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	6 11 26 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	6 11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	6 11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	6 11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	6 11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	6 11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	6 11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	6 11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	6 11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	6 11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	6 11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	6 11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	6 11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	6 11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	6 11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	6 11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	6 11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	6 11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	6 11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	6 11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	6 11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	6 11 27 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	6 11 27 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	6 11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	6 11 27

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE
Memory Constraints

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION
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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
LVDS	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	ISL3,ISL4,ISL9,ISL10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8 17 83
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8 17 83
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	18 87
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 87
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 87
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 87
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 87
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	16 41
	SATA_90D	SATA	SATA_HDD_R2D_C_N	16 41
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_N	6 41
I218 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P	41
I219	SATA_90D	SATA	SATA_HDD_R2D_UF_N	41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	16 41
	SATA_90D	SATA	SATA_HDD_D2R_N	16 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 41
	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N	16 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	6 41
	SATA_90D	SATA	SATA_ODD_R2D_N	6 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	16 41
	SATA_90D	SATA	SATA_ODD_D2R_N	16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P	6 41
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	6 41
I213 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP	16
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	18 24
	USB_85D	USB	USB_HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	18 24
	USB_85D	USB	USB_HUB2_UP_N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P	24 42
	USB_85D	USB	USB_EXTA_N	24 42
USB_EXTB	USB_85D	USB	USB_EXTB_P	24 42
	USB_85D	USB	USB_EXTB_N	24 42
USB_EXTC	USB_85D	USB	USB_EXTC_P	8 24
	USB_85D	USB	USB_EXTC_N	8 24
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 31
	USB_85D	USB	USB_CAMERA_CONN_N	6 31
USB_BT	USB_85D	USB	USB_BT_P	24 31
	USB_85D	USB	USB_BT_N	24 31
USB_TPAD	USB_85D	USB	USB_TPAD_P	24 52
	USB_85D	USB	USB_TPAD_N	24 52
USB_IR	USB_85D	USB	USB_IR_P	24 43
	USB_85D	USB	USB_IR_N	24 43
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	18
I214 USB_T29A	USB_85D	USB	USB_T29A_P	8 24
I215	USB_85D	USB	USB_T29A_N	8 24

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 44 46 87
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 44 46 87
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 25 46 87
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	25 44
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 46
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 23 26 28 30 41 47 61 88
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 23 26 28 30 41 47 61 88
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 47
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 47
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 47
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 47
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 56
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 56
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 56
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 56
	HDA_50S	HDA	AUD_SDI_R	56
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 56
	HDA_50S	HDA	HDA_SDOUT_R	16
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 46
	SPI_55S	SPI	SPI_CLK	46
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 46
	SPI_55S	SPI	SPI_MOSI	46
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 46
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 46
	SPI_55S	SPI	SPI_CS0_L	46
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	36
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	36
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	36
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 31
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 31
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	6 16 31
	PCIE_85D	PCIE	PCIE_AP_D2R_N	6 16 31
	PCIE_85D	PCIE	PCIE_FW_R2D_P	38
	PCIE_85D	PCIE	PCIE_FW_R2D_N	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 38
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	38
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	38
I253	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
I254	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
I262 PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
I261	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33
I255	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
I257	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
I256	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
I259	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
I258	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
I260	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	16 73
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	16 73
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 31
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARD_N	8 16
I263 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 9 33
I264 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 9 33
I265 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	33
I267 PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	33
I266 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 9 33
I268 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 9 33
I270 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	33
I269 PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	33

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE

PCH Constraints 2

Apple Inc.

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR	*	=3X_DIELECTRIC	?

SOURCE: Attila Farkas Email - 8/2/10

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
		ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
		ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
		ENET_50S	ENET_3X	ENET_RESET_L	32 36
	ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
		ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
I166	CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_DATA_R<7..0>	
I167	CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD_R	32
I168	CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK_R	32
I169	CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_DATA<7..0>	32 36
I170	CR_DATA_A0	ENET_50S	ENET_CR	SDCONN_CMD	32 36
I171	CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK	32 36
I172	CR_CLK	ENET_50S	ENET_CR	SDCONN_CLK_R_L	32

FireWire Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
I158	FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 38 40
I159	FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	38 40
I160	FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 38 40
I161	FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 38 40
I162	FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	38 40
I163	FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	38 40
I164	FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	38 40
I165	FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	38 40

Port 2 Not Used

SYNC_MASTER=K91_ERIC SYNC_DATE=08/03/2010

PAGE TITLE: Ethernet/FW Constraints

Apple Inc.

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	6 33 78
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	6 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	6 33 78
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	6 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	6 33 78
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	6 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	6 33 78
	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	6 33 78
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	6 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	6 33
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
	T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 47 84
	T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 47 84
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
	T29DP_80D	T29DP	T29_R2D_C_P<3..0>	6 8 33 84
	T29DP_80D	T29DP	T29_R2D_C_N<3..0>	6 8 33 84
	T29DP_100D	T29DP	T29_D2R_P<3..0>	6 8 33 84
	T29DP_100D	T29DP	T29_D2R_N<3..0>	6 8 33 84

Only used on hosts supporting T29 video-in

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	6 84
T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	6 84
T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	6 84
	T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	84
	T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	84
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	6 84 85
T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	6 84 85
T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	6 84 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	6 85
	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	6 85
	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	6 84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	84
	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	84
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	6 84 95
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	6 84 95
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	84
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	84
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	84
	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	84
	T29DP_80D	T29DP	T29DPA_ML_P<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_N<3..0>	6 84 85
	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	84 85
	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	84 85
	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	84 85
T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
	T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
	T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	95
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	95
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
	T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

SYNC_MASTER=T29_REF SYNC_DATE=10/16/2010

PAGE TITLE

T29 Constraints

Apple Inc.

DRAWING NUMBER | SIZE D | REVISION | BRANCH

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	6 31 44 47 53 54
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	6 31 44 47 53 54
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	44 47 50
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	44 47 50
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	6 31 44 47 50 79
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	6 31 44 47 50 79
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 44 47 62 63
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 44 47 62 63
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	44 47 100
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	44 47 100

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	63
	1TO1_DIFFPAIR		CHGR_CSI_N	63
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	63
	1TO1_DIFFPAIR		CHGR_CSO_N	63

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE

SMC Constraints

DRAWING NUMBER

SIZE D

Apple Inc.

REVISION

BRANCH

GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	75 76
	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	75 76
	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	75 76
	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_A<8..0>	6 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_A<8..0>	6 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_ABI_L	6 75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_ABI_L	6 75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_RAS_L	75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_RAS_L	75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CAS_L	75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CAS_L	75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_WE_L	75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_WE_L	75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CKE_L	75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CKE_L	75 76
	FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A0_CS_L	75 76
	FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_A1_CS_L	75 76
	FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	6 75 76
I293	FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	6 75 76
I294	FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	6 75 76
I295	FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	6 75 76
I296	FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	6 75 76
I297	FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	6 75 76
I298	FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	6 75 76
	FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	6 75 76
	FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	6 75 76
I299	FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	6 75 76
I300	FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	6 75 76
I301	FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	6 75 76
I302	FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	6 75 76
I303	FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	6 75 76
I304	FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	6 75 76
	FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	6 75 76
	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>	6 75 76
	FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>	6 75 76
	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>	6 75 76
	FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>	6 75 76
	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>	6 75 76
	FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>	6 75 76
	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>	6 75 76
	FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>	6 75 76
	FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	6 75 76
	FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	6 75 76
	FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	6 75 76
	FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	6 75 76
	FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	6 75 76
	FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	6 75 76
	FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	6 75 76
	FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	6 75 76
	FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB_RESET_L	75 76 77

GDDR5 FB B Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	75 77
	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	75 77
	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	75 77
	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>	6 75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>	6 75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABI_L	6 75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABI_L	6 75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L	75 77
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L	75 77
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L	75 77
	FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	6 75 77
I305	FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	6 75 77
I306	FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	6 75 77
I307	FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	6 75 77
I310	FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	6 75 77
I309	FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	6 75 77
I308	FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	6 75 77
	FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	6 75 77
	FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	6 75 77
I311	FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	6 75 77
I312	FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	6 75 77
I313	FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	6 75 77
I316	FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	6 75 77
I315	FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	6 75 77
I314	FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	6 75 77
	FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	6 75 77
	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>	6 75 77
	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>	6 75 77
	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>	6 75 77
	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>	6 75 77
	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>	6 75 77
	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>	6 75 77
	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>	6 75 77
	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>	6 75 77
	FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	6 75 77
	FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	6 75 77
	FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	6 75 77
	FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	6 75 77
	FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	6 75 77
	FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	6 75 77
	FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	6 75 77
	FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	6 75 77

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_P	83 87
LVDS_A_CLK	LVDS_85D	LVDS	LVDS_A_CLK_N	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_P<2..0>	83 87
LVDS_A_DATA	LVDS_85D	LVDS	LVDS_A_DATA_N<2..0>	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_P	83 87
LVDS_B_CLK	LVDS_85D	LVDS	LVDS_B_CLK_N	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_P<2..0>	83 87
LVDS_B_DATA	LVDS_85D	LVDS	LVDS_B_DATA_N<2..0>	83 87
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_P	6 82
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_F_N	6 82
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_P	6 82
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_F_N	6 82
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_P	82 83
	LVDS_85D	LVDS	LVDS_CONN_A_CLK_N	82 83
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_A_DATA_N<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_P	82 83
	LVDS_85D	LVDS	LVDS_CONN_B_CLK_N	82 83
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_P<2..0>	6 82 83
	LVDS_85D	LVDS	LVDS_CONN_B_DATA_N<2..0>	6 82 83

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	78 79
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M	78 79
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_P	78 87
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS_EG_A_CLK_N	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_P<2..0>	78 87
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS_EG_A_DATA_N<2..0>	78 87
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>	78 79
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>	78 79
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_P<2..0>	78 87
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS_EG_B_DATA_N<2..0>	78 87
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>	78 79
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>	78 79
DP_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	78 84
	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	78 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	83 84
	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	83 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_EG_AUXCH_P	6 78 83
	DP_85D	DISPLAYPORT	DP_EG_AUXCH_N	6 78 83

SYNC_MASTER=K92_MLB SYNC_DATE=08/09/2010

PAGE TITLE
GPU (Whistler) CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K91 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)	NET	PAGES
		ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
		ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	50
		THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	50
I287	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 50
I288		THERM_1TO1_55S	THERM	CPU_THERMD_N	9 50
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	50
		THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	50
	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	50 78
		THERM_1TO1_55S	THERM	GPU_TDIODE_N	50 78
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	48 64
		SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	48 64
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	48
		SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	48
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	48
		SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	48
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	48 69
		SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	48 69
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	48
		SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	48
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	48
		SENSE_1TO1_55S	SENSE	GPUISENS_P	48
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	48 66
		SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	48 66
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	98
		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	98
I249	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	98
I250		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	98
I252	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	100
I251		SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	100
I256	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	
I255		SENSE_1TO1_55S	SENSE	ISNS_HDD_P	
I281	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	100
I282		SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	100
I283	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
I284		SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
I285	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
I286		SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	100
		SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	100
I292	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	
I291		SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	
I299	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	100
I300		SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	100
I301	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_P	
I302		SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_N	
I303	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_R_P	100
I304		SENSE_1TO1_55S	SENSE	PP1V8_S0GPU_R_N	100
I305	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_P	
I306		SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_N	
I308	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_R_P	100
I307		SENSE_1TO1_55S	SENSE	PP1V5_S0GPU_R_N	100
I329	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	49 68
I330		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	49 68
I337	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	49
I338		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	49
I331	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	49
I332		SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	49
I333	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	49
I334		SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	49
I335	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	49
I336		SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	49
I342	SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	49
I341		SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	49
I312	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 59
I311		AUDIODIFF	AUDIO	AUD_LO1_R_N	56 59
I314	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
I313		AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
I316	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 59
I315		AUDIODIFF	AUDIO	AUD_LO2_R_N	56 59
I317	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	59
I318		AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	59
I319	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	59
I320		AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	59
I321	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_P	59
I322		AUDIODIFF	AUDIO	AUD_SPKRAMP_SUBIN_N	59

K91 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)	NET	PAGES
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 31
	1TO1_DIFFPAIR		CHGR_CSI_R_P	63
	1TO1_DIFFPAIR		CHGR_CSI_R_N	63
	1TO1_DIFFPAIR		CHGR_CSO_R_P	49 63
	1TO1_DIFFPAIR		CHGR_CSO_R_N	49 63
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	42
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	6 42
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	6 42
	USB_85D	USB	CONN_USB2_BT_P	6
	USB_85D	USB	CONN_USB2_BT_N	6
	USB_85D	USB	USB_LT2_P	6 42
	USB_85D	USB	USB_LT2_N	6 42
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375L_P	59
	AUDIODIFF	AUDIO	SSM2375L_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375R_P	59
	AUDIODIFF	AUDIO	SSM2375R_N	59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375S_P	59
	AUDIODIFF	AUDIO	SSM2375S_N	59
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	6 59 60
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	6 59 60
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	6 59 60
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	6 59 60
	USB_85D	USB	USB_TPAD_R_P	52
	USB_85D	USB	USB_TPAD_R_N	52
		SB_POWER	PP3V3_S5	45 55 65 70 71 72 82 85 89 6 7 17 19 20 22 23 24 25 29 39
		SB_POWER	PP3V3_S0	48 49 50 51 53 56 60 61 71 72 6 7 12 16 17 18 19 20 22 23 25 26 28 32 35 36 39 40 41 45 47
		SB_POWER	PP1V5_S3RS0	79 82 83 84 87 88 89 6
		GND	GND	

SYNC_MASTER=K18_MLB SYNC_DATE=04/27/2010

PAGE TITLE
Project Specific Constraints

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K91 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.2 MM	0.2 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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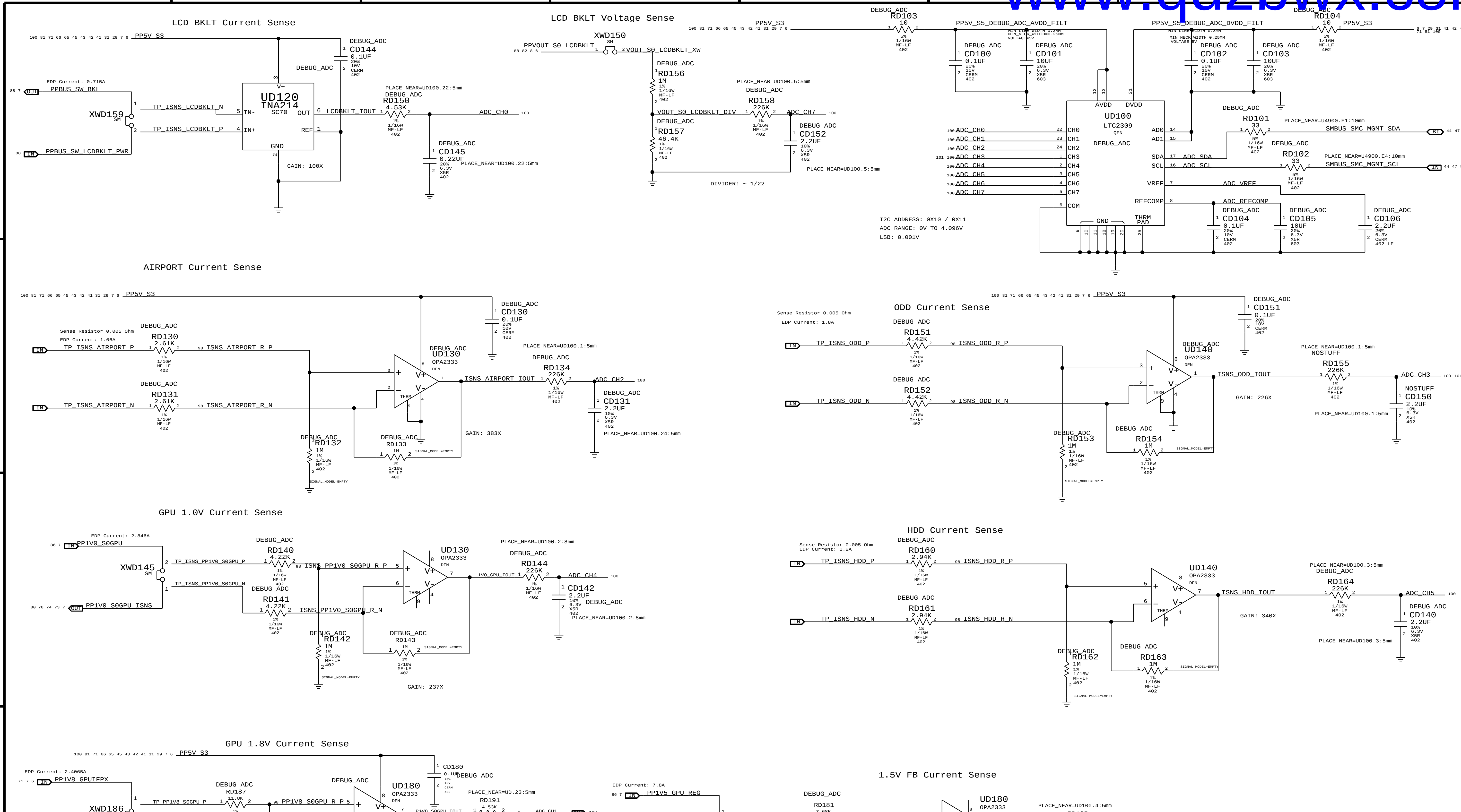

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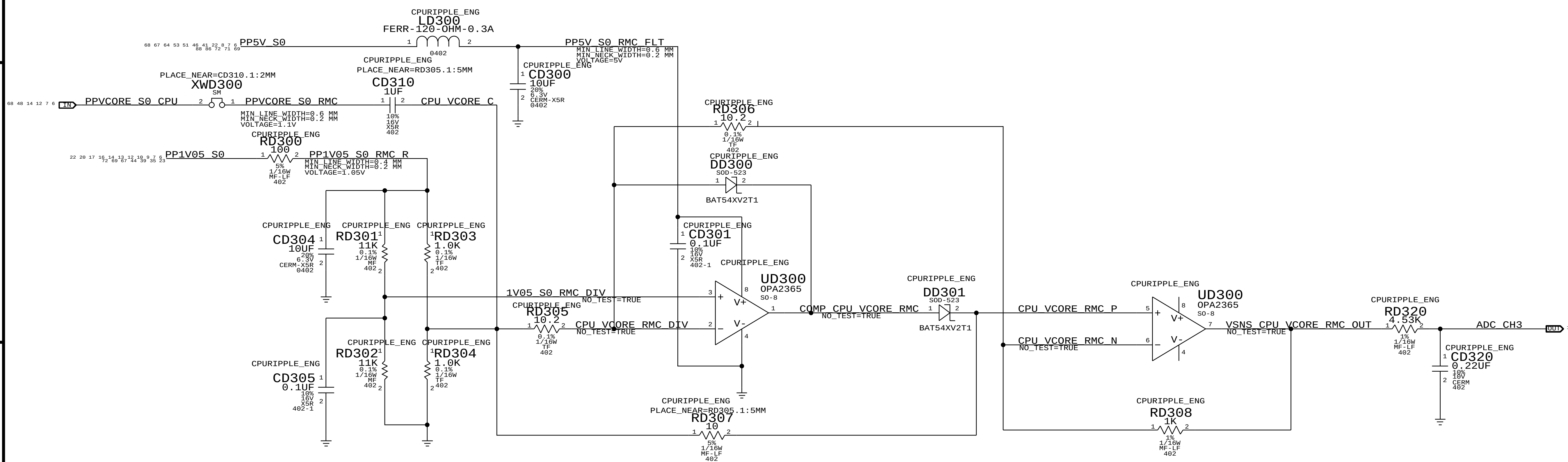

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PAGE 132 OF 132

SHEET 101 OF 101