MODEL NAME : *QCL00_QCL20*

PCB NO : *LA-8241P*

BOM P/N :
4619GP31L21 Inspiron DIS
4619GQ31L21 Inspiron UMA
4619GP31L01 Vostro DIS
4619GQ31L01 Vostro UMA

Dell / Compal Confidential

Schematic Document

Inspron A5 & Vostro 3560 (Intel Chief River)
Ivy Bridge(rPGA) + Panther Point(mainstream)

Discrete AMD Thames-XT

2012-02-01

Rev: 1.0

MB Type	BOM P/N	Config

46@ : for 46 level
@ : Nopop Component
CONN@ : Connector Component
KB930@ : ENE KB930 Implemented
KB9012@ : ENE KB9012 Implemented
EXP@ : Express Card Implemented
FFS@ : Only for Free Fall Sensor
VOS@ : Only for Vostro
INS@ : Only for Inspiron
UMA@ : Only for UMA
GCLK@ : Green CLK implemented
AMP@ : External Amplifier implemented
KBBL@ : Keyboard Back Light implemented

X76@ : VRAM Group
CH@ : Chelsea M2
SE@ : Seymour M2
TH@ : Thames-XT
DIS@ : Only for Discrete

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

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Title: *Cover Page*

Size | Document Number: *LA-8241P* | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 1 of 56

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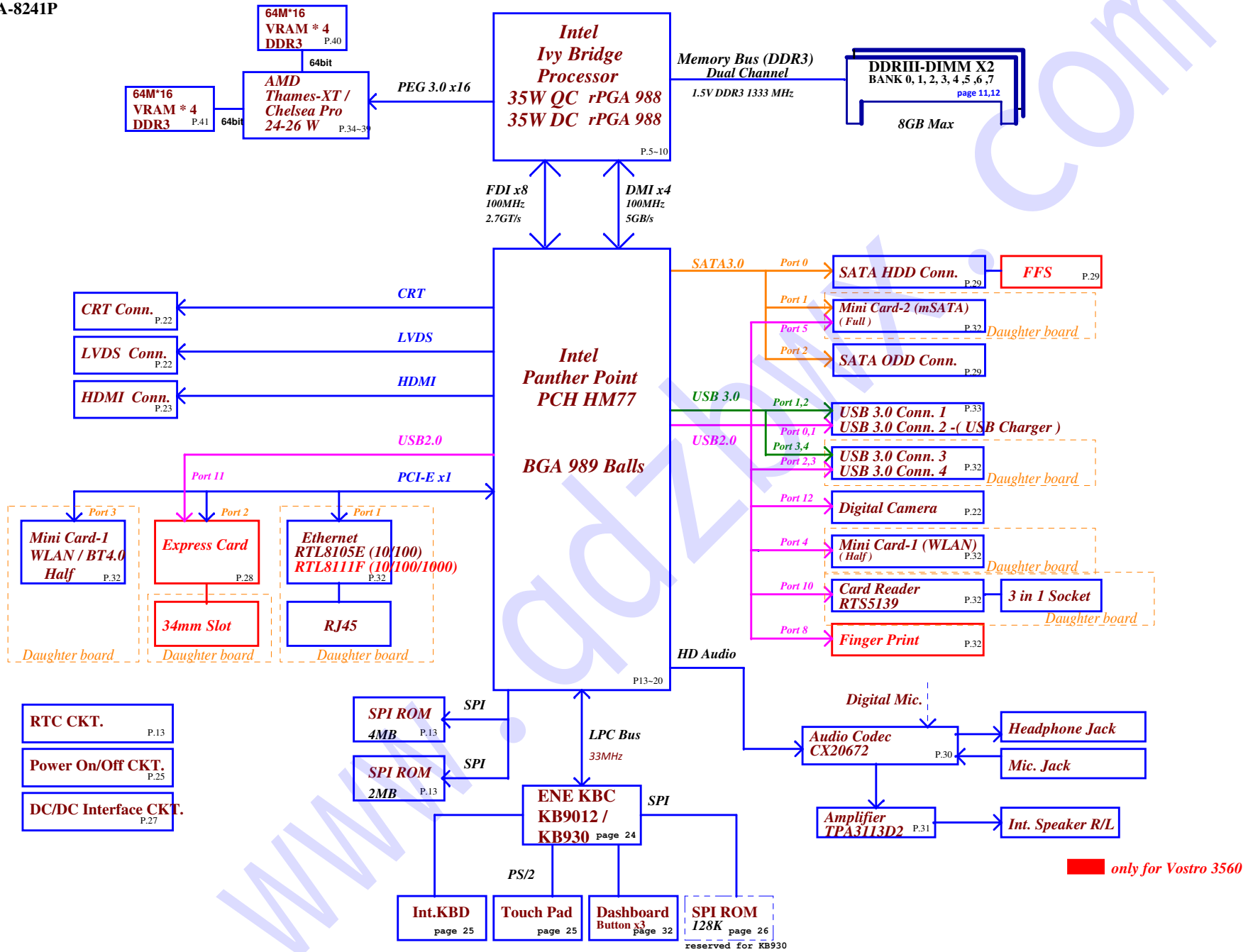
Project Code : QCL00 / QCL20
File Name : LA-8241P



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
	LA-8241P	1.0

Date: Wednesday, February 01, 2012 Sheet 2 of 56

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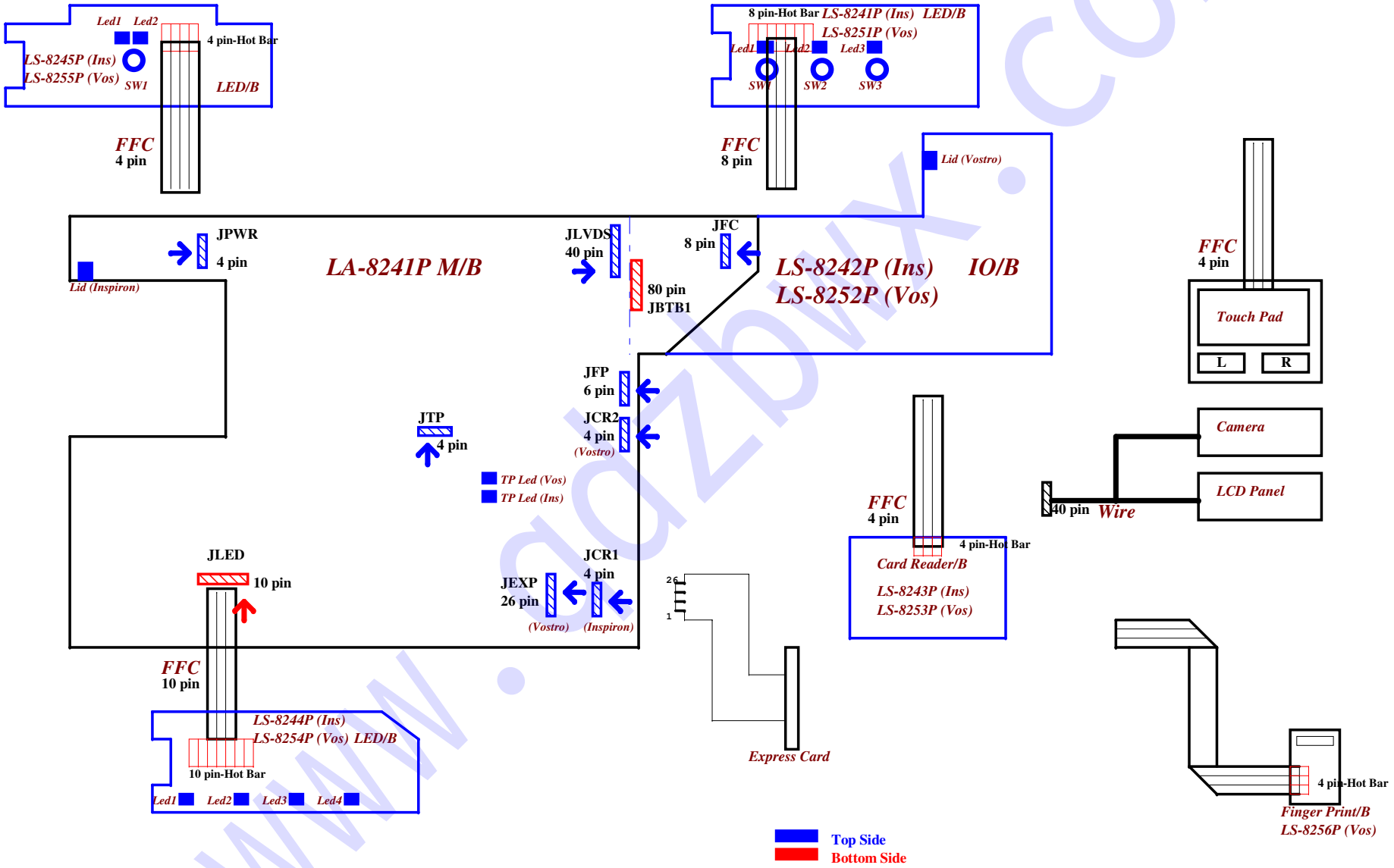
Project Code : QCL00 / QCL20
File Name : LA-8241P



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	Block Diagram		
Size	Document Number		Rev 1.0
Date: Wednesday, February 01, 2012	Sheet 3 of 56		

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision			
0	0.1			
1		0.1		
2	0.2			
3		0.2		
4	0.3			0.2
5		0.3		0.3
6	1.0			1.0
7		1.0		
	QCL00	QCL20		QCL01

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	

Link

PCH	USB PORT#	DESTINATION
	0	USB conn.1
	1	USB conn.2 - Power Share
	2	USB conn.3
	3	USB conn.4
	4	MINI CARD-1 (WLAN)
	5	NC
	6	NC
	7	NC
	8	Finger Print
	9	NC
	10	Card Reader
	11	Express Card
	12	Camera
	13	NC

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-1 WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	Express Card	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

SATA	DESTINATION
SATA0	HDD
SATA1	SSD
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-1 (WLAN)
Lane 3	Express Card
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

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Issued Date	2012/01/17	Deciphered Date	2013/01/16

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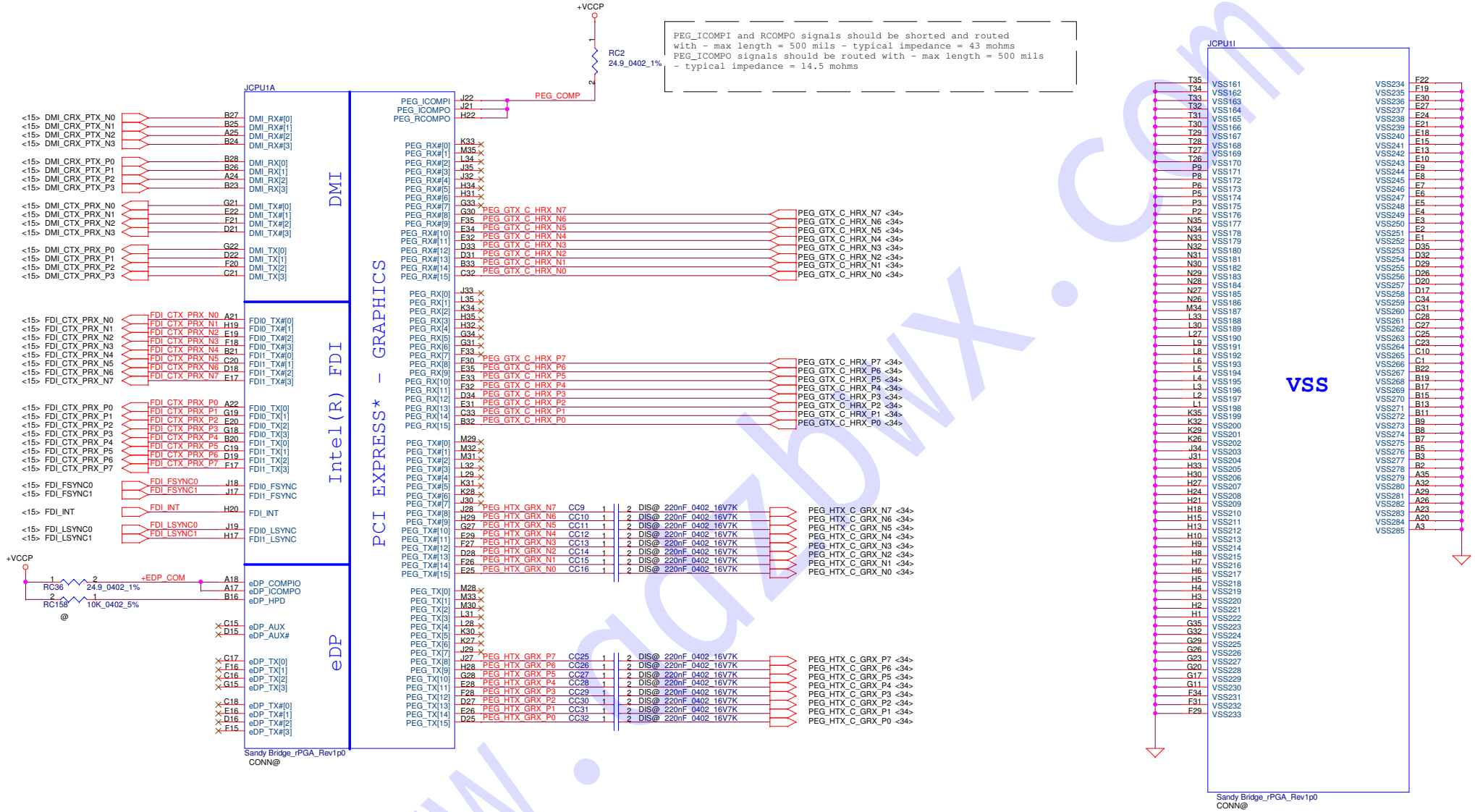
Title: Notes List

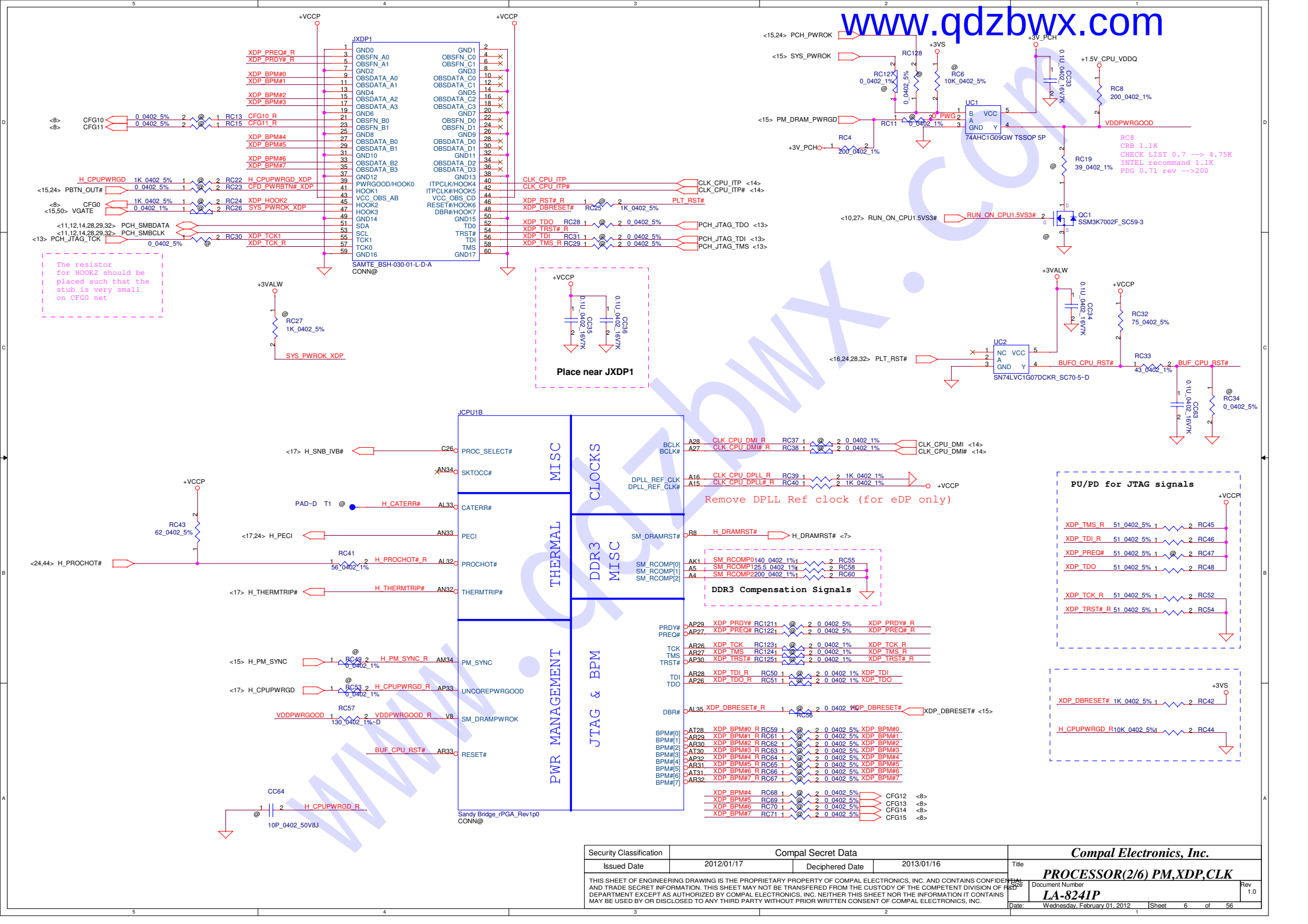
Size: B | Document Number: LA-8241P | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 4 of 56



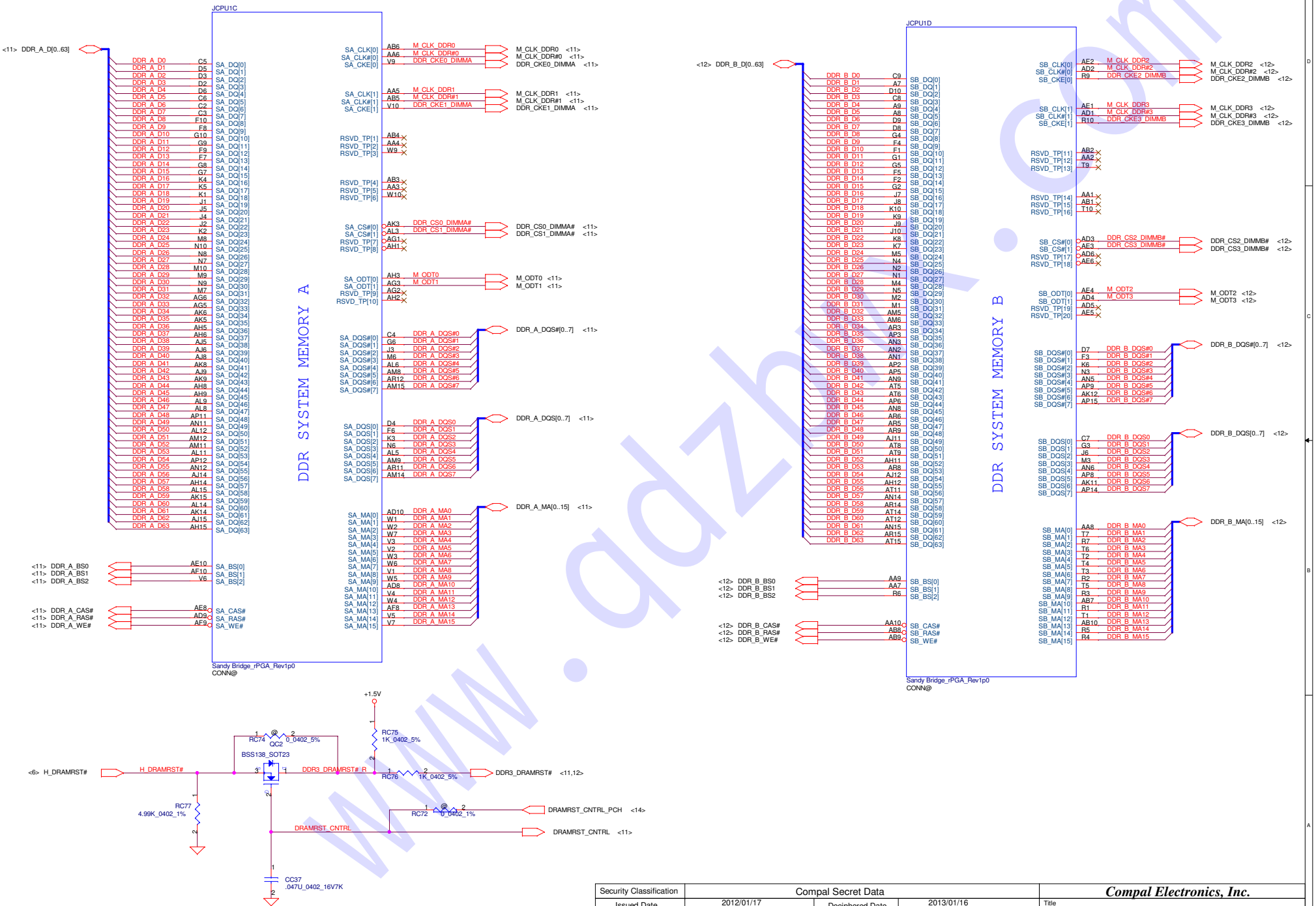
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	PROCESSOR(1/6) DMI,FDI,PEG		
Size	Document Number	LA-8241P	Rev 1.0
Date:	Wednesday, February 01, 2012	Sheet 5 of 56	



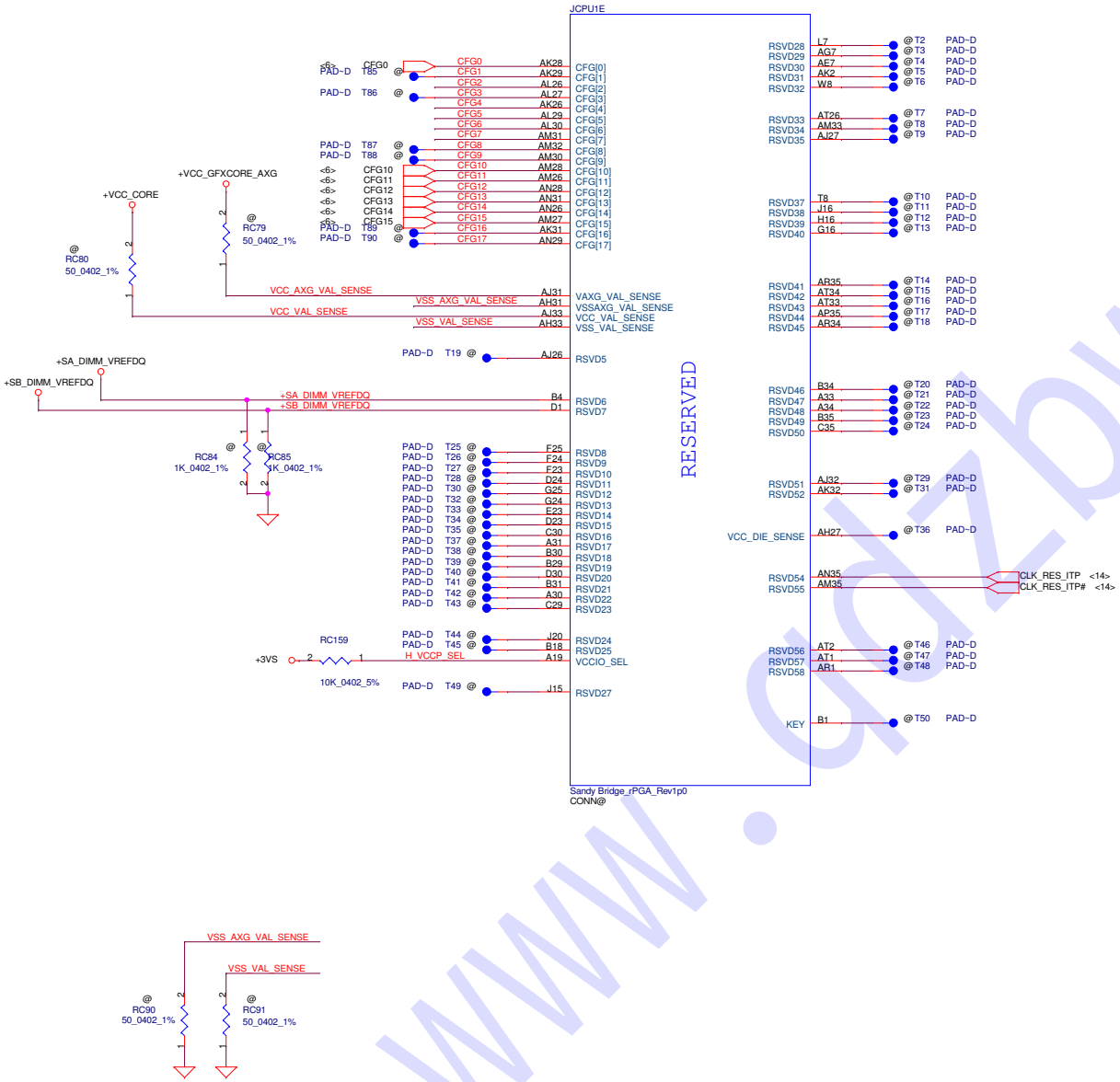
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.	
Title	PROCESSOR(2/6) PM,XDP,CLK
Size	Document Number: LA-8241P
Rev	1.0
Date: Wednesday, February 01, 2012	Sheet 6 of 56



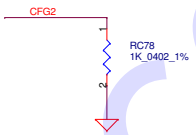
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	PROCESSOR(3/6) DDRIII		
Size	Document Number		Rev
	LA-8241P		1.0
Date:	Wednesday, February 01, 2012	Sheet	7 of 56

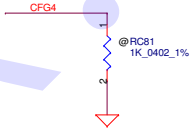


INTEL 12/28 recommand
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1

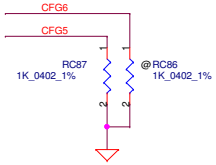
CFG Straps for Processor



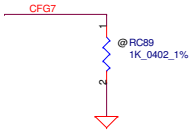
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition *0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled *10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PROCESSOR(4/6) RSVD,CFG

Size | Document Number: LA-8241P | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 8 of 56

POWER

JCPU1F

QC=94A
DC=53A

+VCC_CORE

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

+VCCP

8.5A

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

+VCCP

RC95 130_0402_1%~D — RC95 close to CPU

RC93 75_0402_5%

Place the PU resistors close to CPU

VIDALERT#	AJ29	H_CPU_SVIDALRT#	RC94	43_0402_1%
VIDSCLK	AJ30	H_CPU_SVIDCLK	RC92	0_0402_1%
VIDSOUT	AJ28	H_CPU_SVIDDAT	RC96	0_0402_1%

VR_SVID_ALRT# <50>
VR_SVID_CLK <50>
VR_SVID_DAT <50>

+VCC_CORE

RC97 100_0402_1%

VCC_SENSE	AJ35	VCCSENSE_R	RC98	0_0402_1%
VSS_SENSE	AJ34	VSSSENSE_R	RC99	0_0402_1%

VCCSENSE <50>
VSSSENSE <50>

RC100 100_0402_1%

VCCIO_SENSE	B10	
VSSIO_SENSE	A10	

+VCCP

RC108 10_0402_1%

RC111 10_0402_1%

VCCIO_SENSE <47>

Sandy Bridge_rPGA_Rev1p0
CONN@

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PROCESSOR(5/6) PWR,BYPASS

Size | Document Number: LA-8241P | Rev: 1.0

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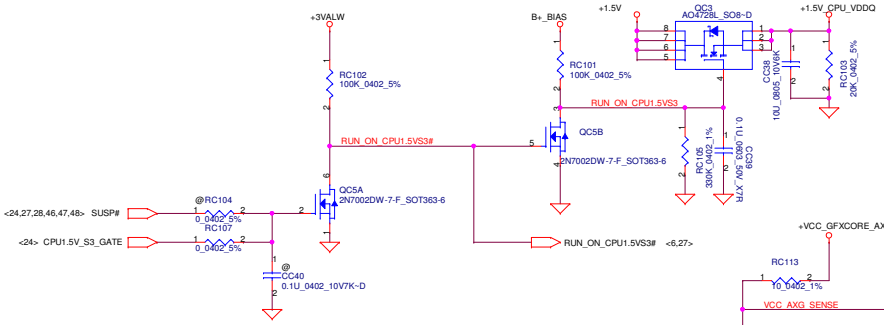
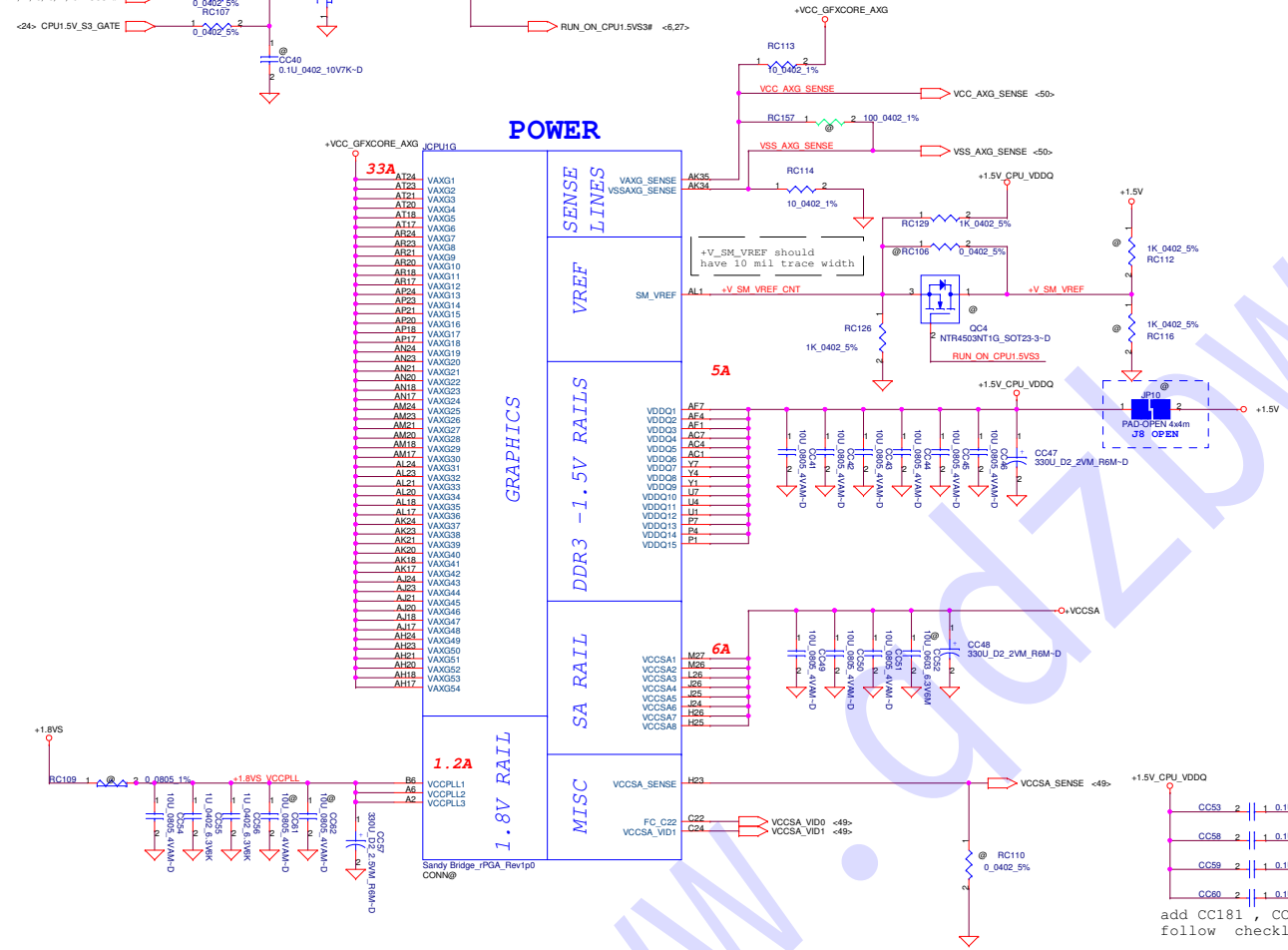
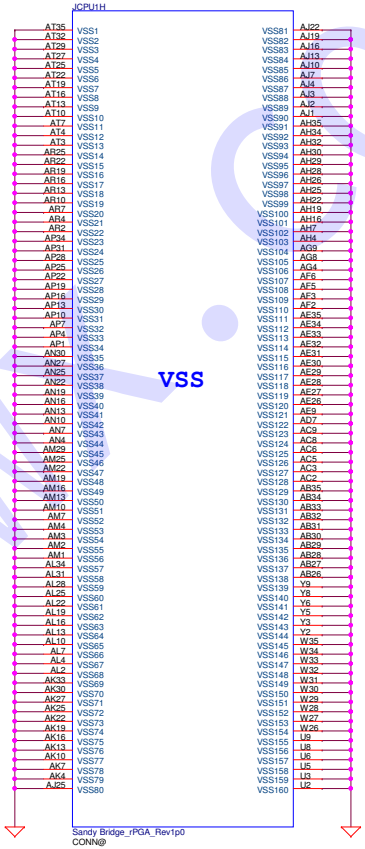
+1.5V_CPU_VDDQ Source



POWER



VSS



add CC181 , CC182, 4 caps are all pop.
follow checklist 1.0 5/24

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/01/17	Deciphered Date 2013/01/16	Title: PROCESSOR(6/6) PWR,VSS
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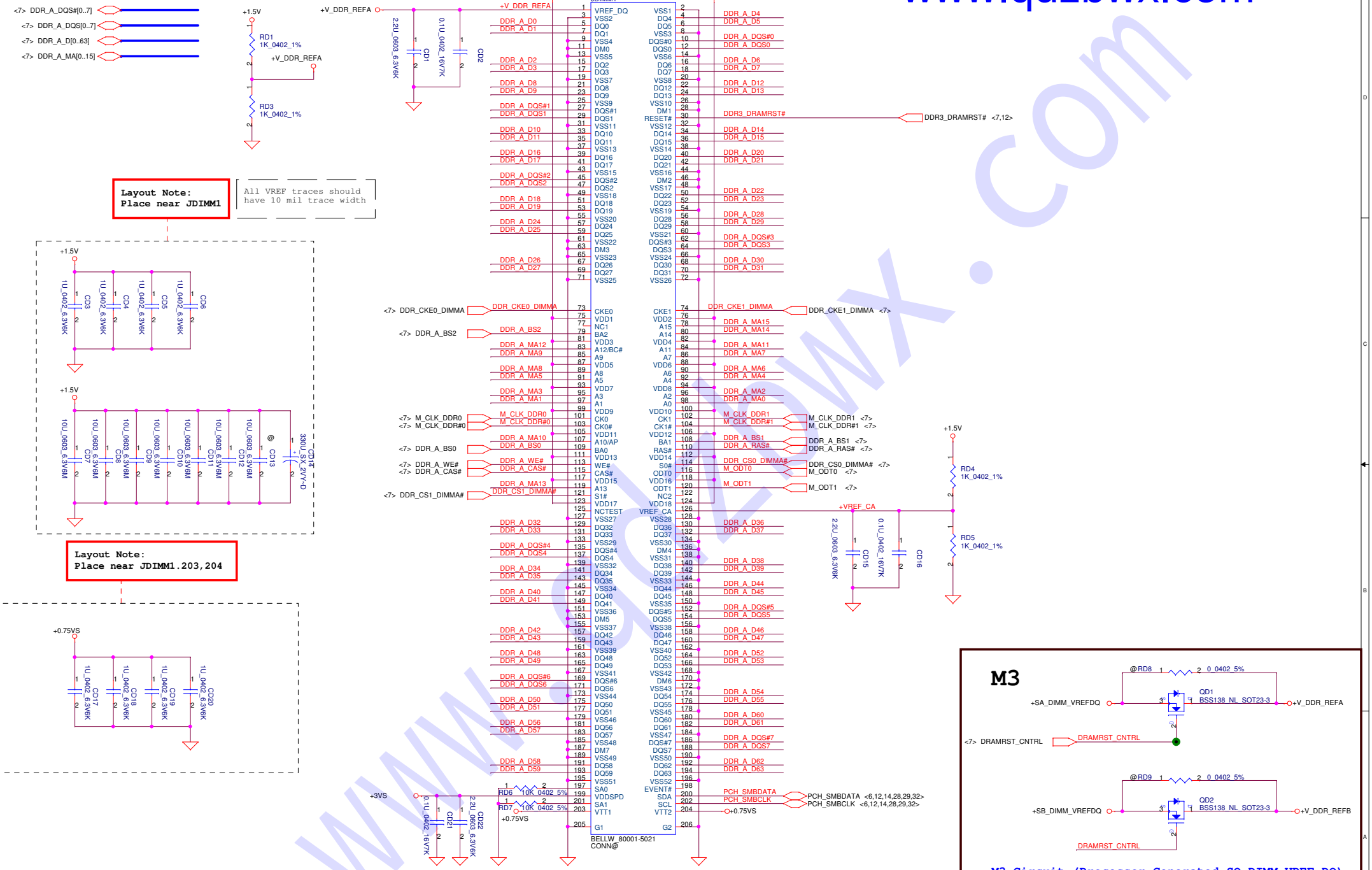
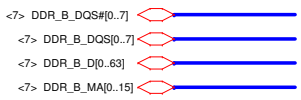
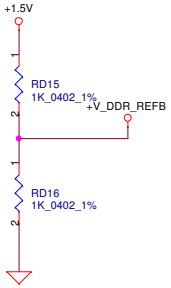
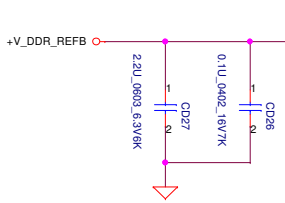
			Date: Wednesday, February 01, 2012 Sheet 10 of 56



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/01/17	Deciphered Date 2013/01/16	Title: DDRIII DIMMA
			Size: Document Number: LA-8241P Rev: 1.0
			Date: Wednesday, February 01, 2012 Sheet 11 of 56



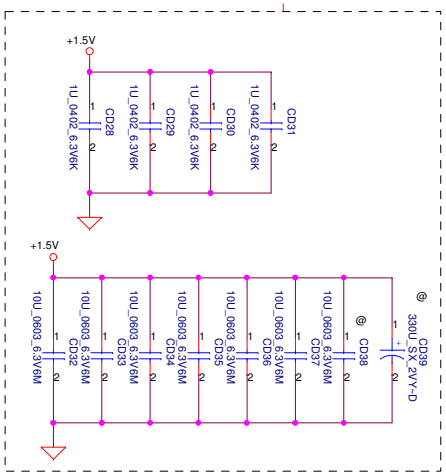




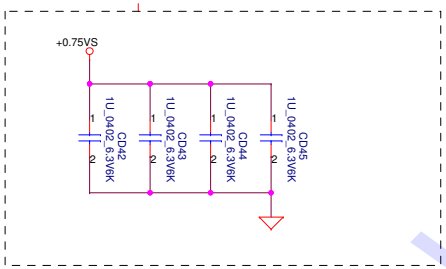
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

All VREF traces should have 10 mil trace width

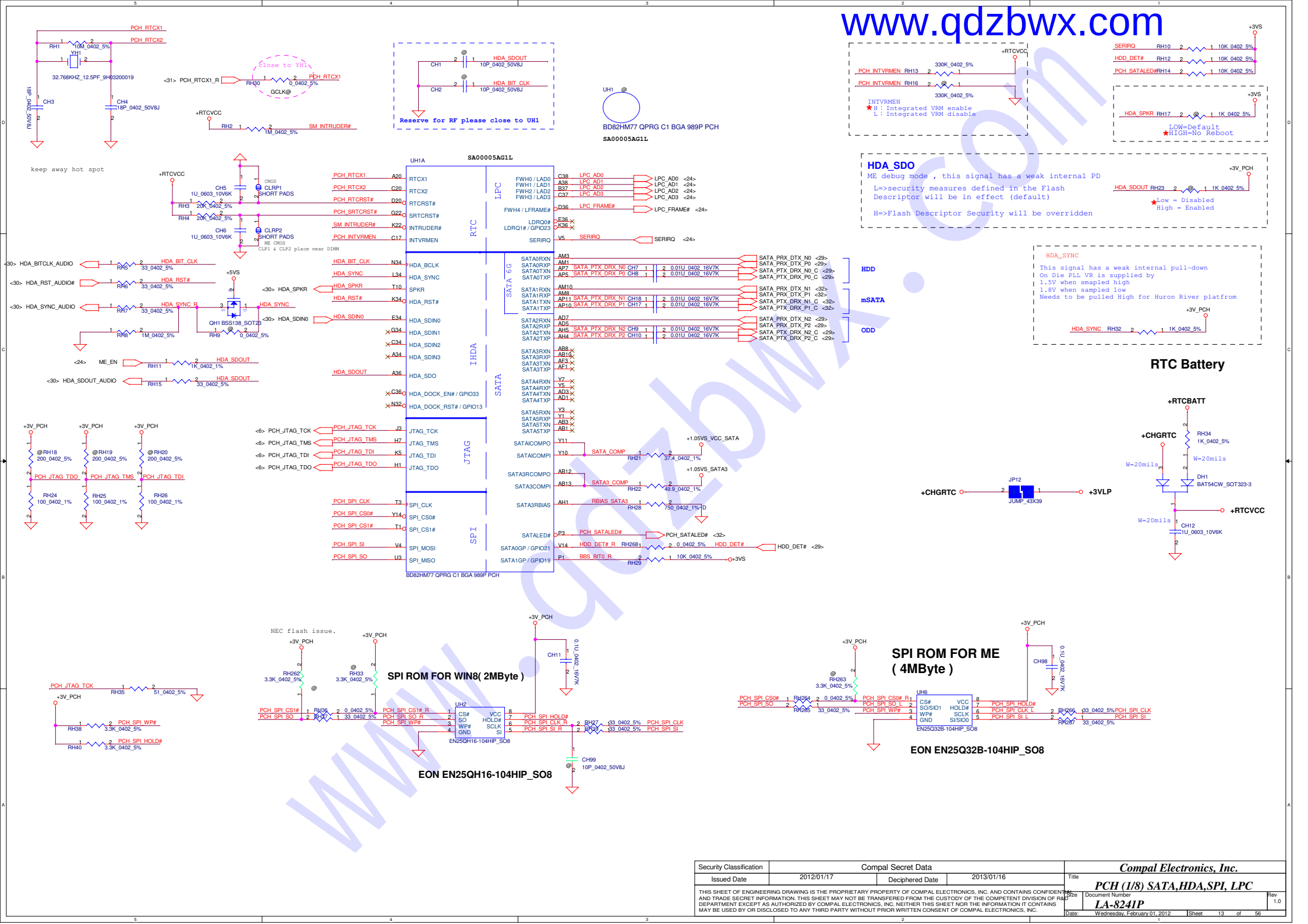
Layout Note:
Place near JDIMM8



Layout Note:
Place near JDIMM8.203,204

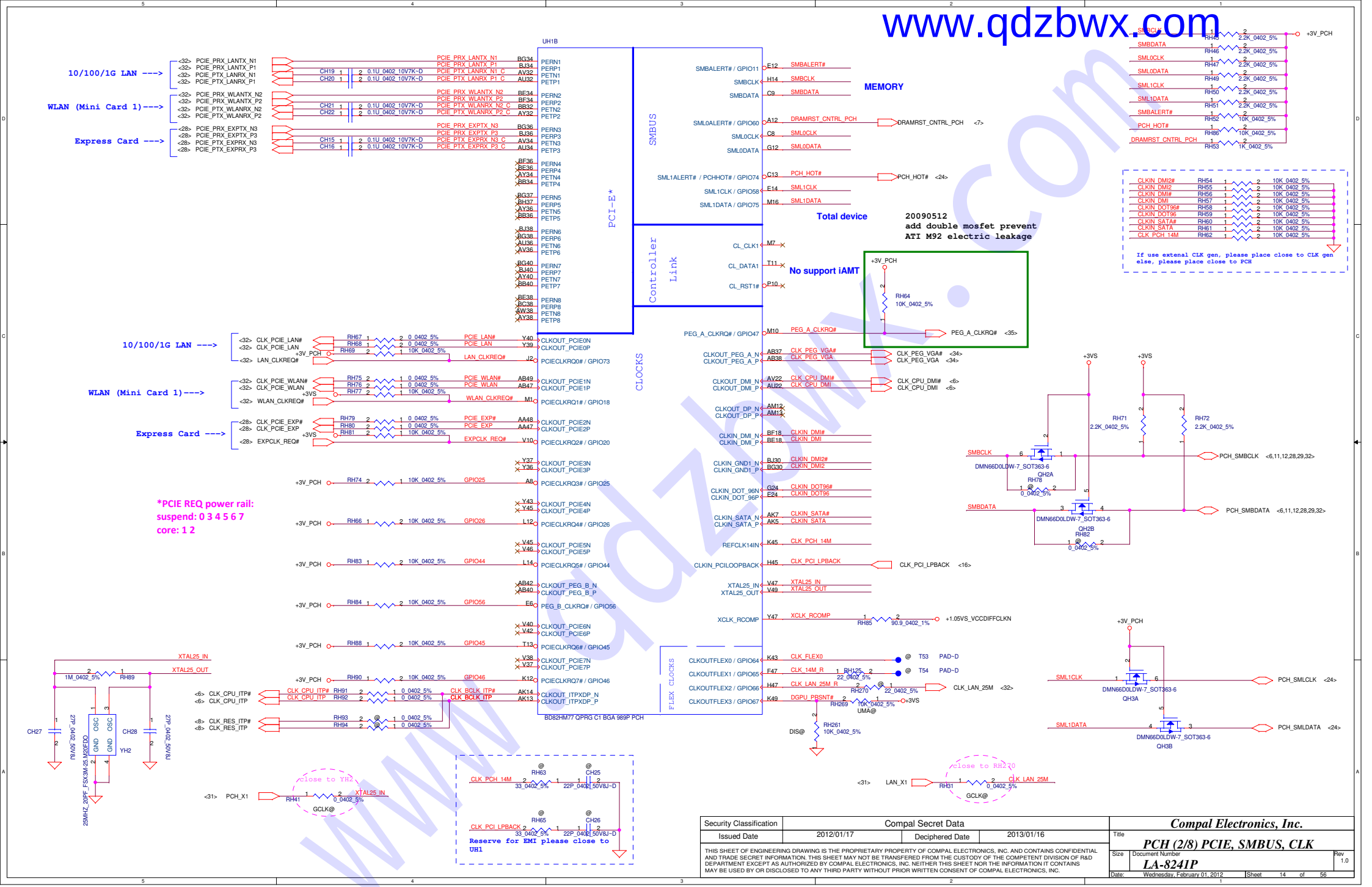


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/01/17	Deciphered Date 2013/01/16	Title: DDRIII DIMMB
			Size: Document Number: LA-8241P Rev: 1.0
			Date: Wednesday, February 01, 2012 Sheet 12 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	PCH (1/8) SATA,HDA,SPI, LPC		
Size	Document Number LA-8241P		Rev 1.0
Date: Wednesday, February 01, 2012	Sheet 13 of 56		



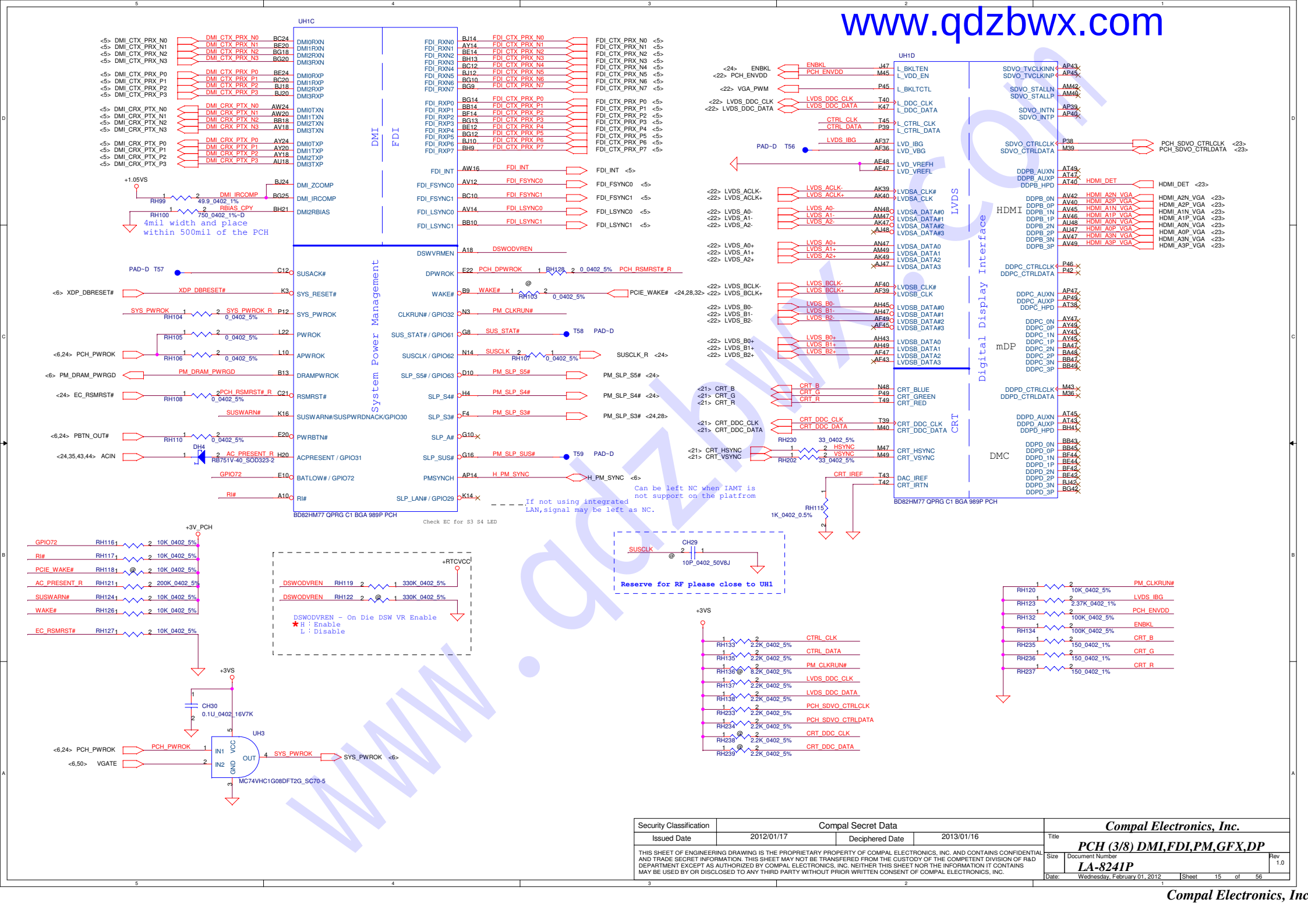
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size	Document Number	Rev
	LA-8241P	1.0

Date: Wednesday, February 01, 2012 | Sheet 14 of 56



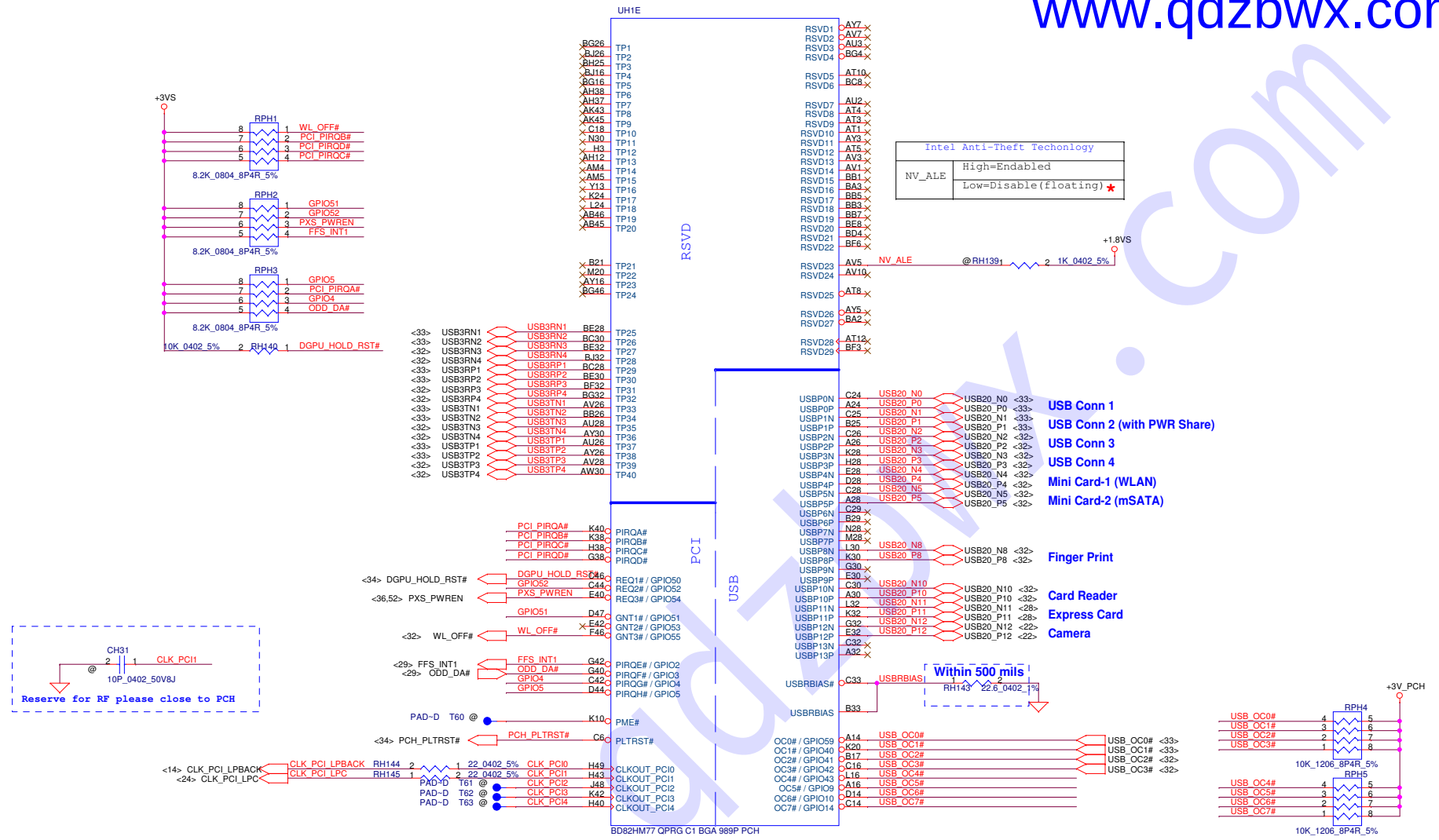
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size	Document Number	Rev
	LA-8241P	1.0

Date: Wednesday, February 01, 2012 Sheet 15 of 56



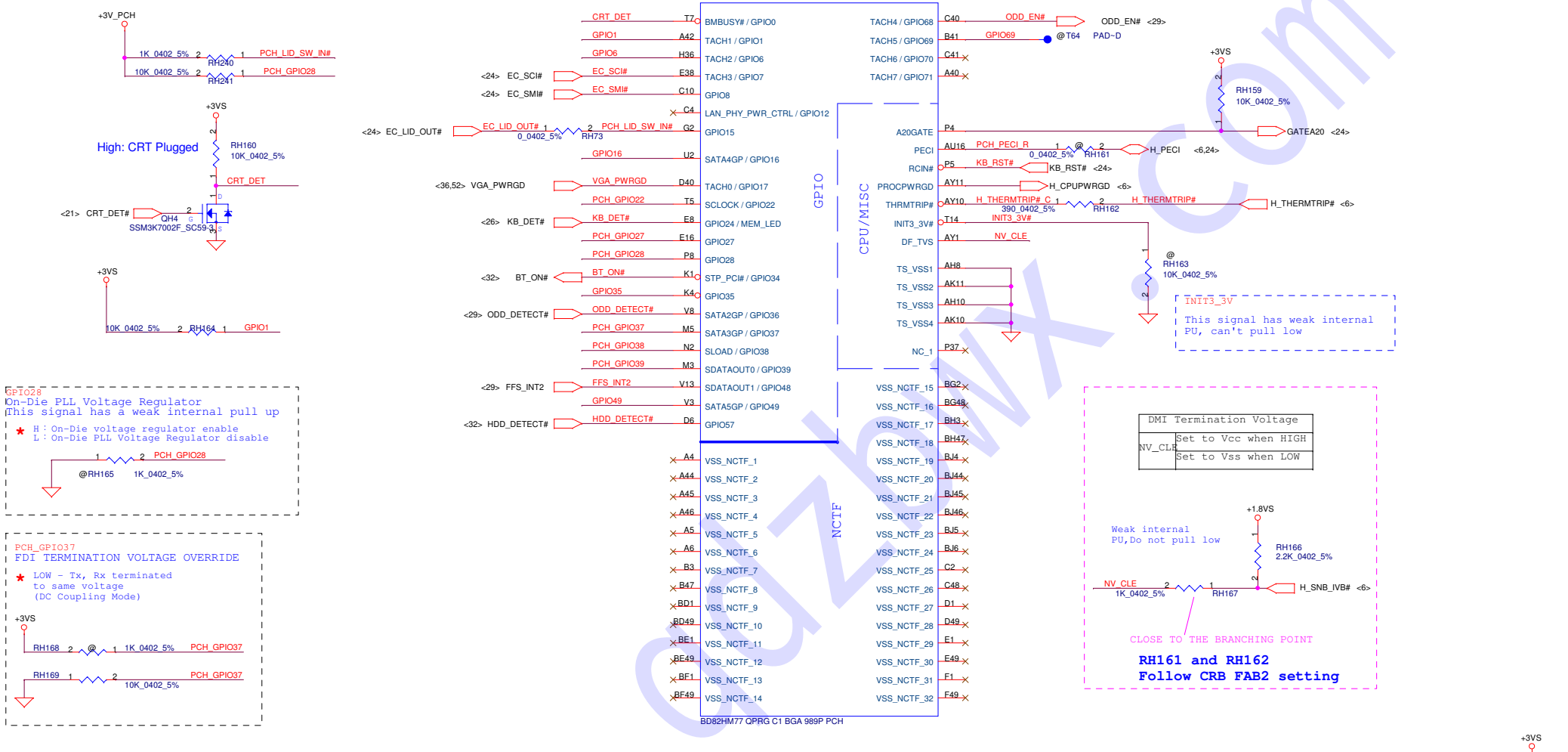
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: **PCH (4/8) PCI, USB, NVRAM**

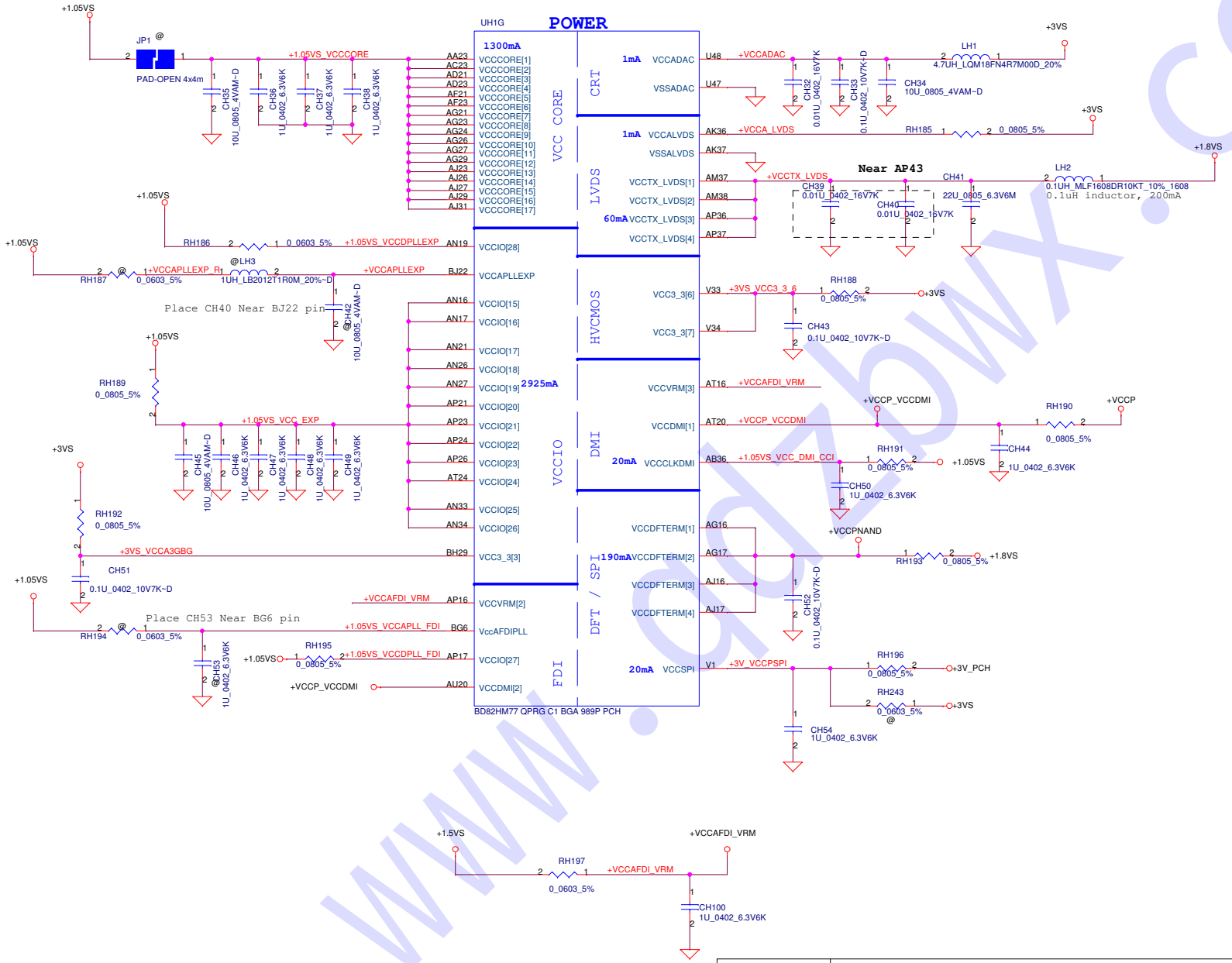
Size: | Document Number: **LA-8241P** | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 16 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	PCH (5/8) GPIO, CPU, MISC		
Size	Document Number		Rev
	LA-8241P		1.0
Date:	Wednesday, February 01, 2012	Sheet	17 of 56



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: | Document Number: LA-8241P | Rev: 1.0

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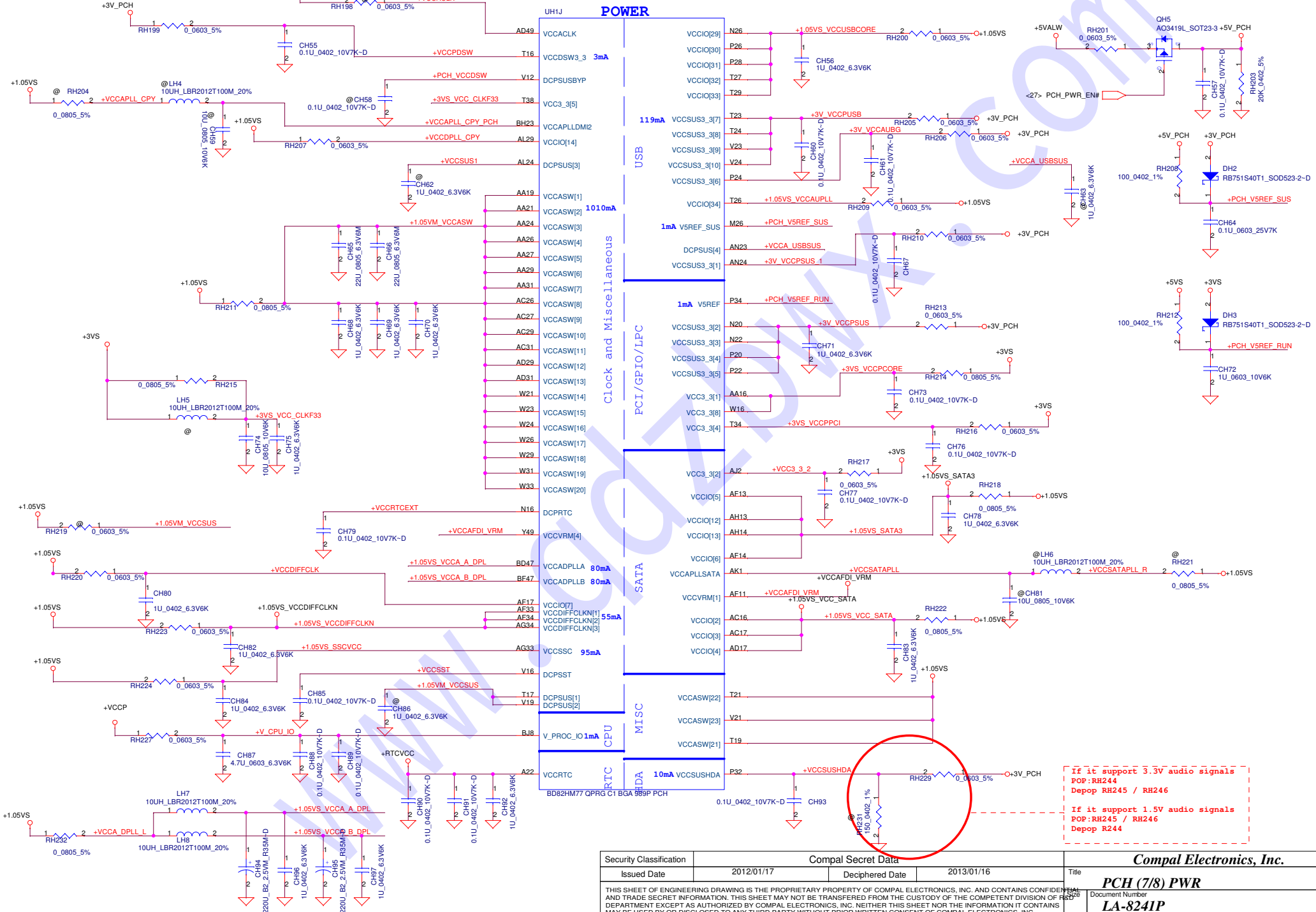
VCC3_3 = 266mA detal waiting for newest spec

VCCDMI = 42mA detal waiting for newest spec



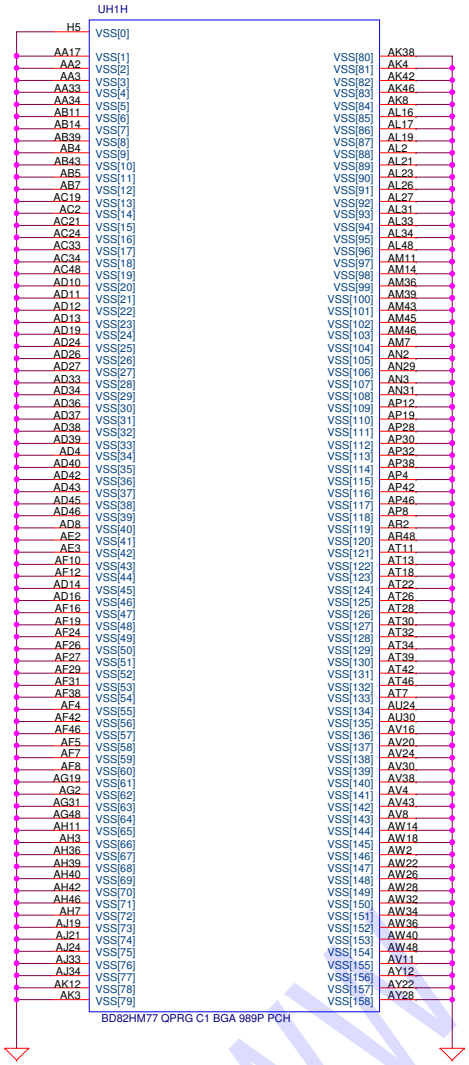
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

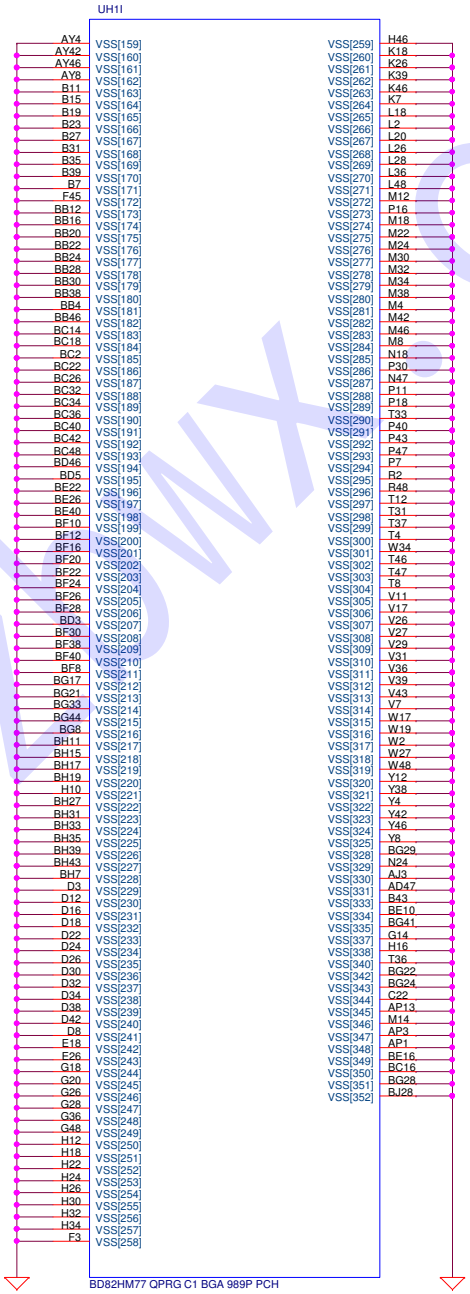
Compal Electronics, Inc.

Title: PCH (7/8) PWR

Size: | Document Number: LA-8241P | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 19 of 56

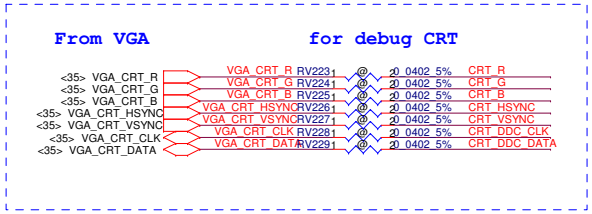


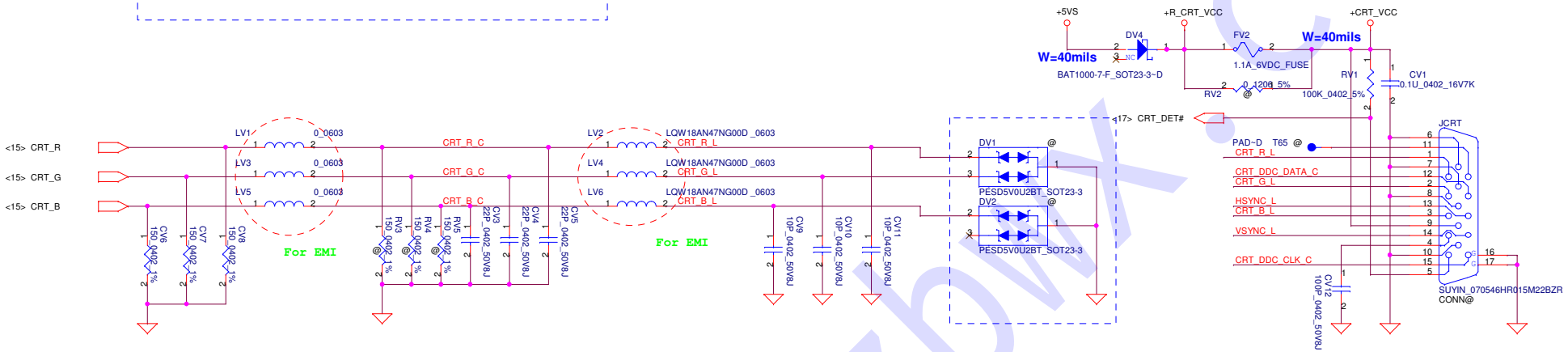


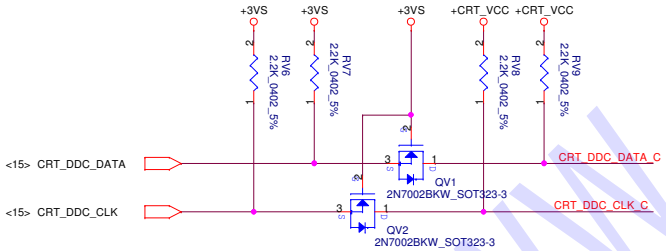
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

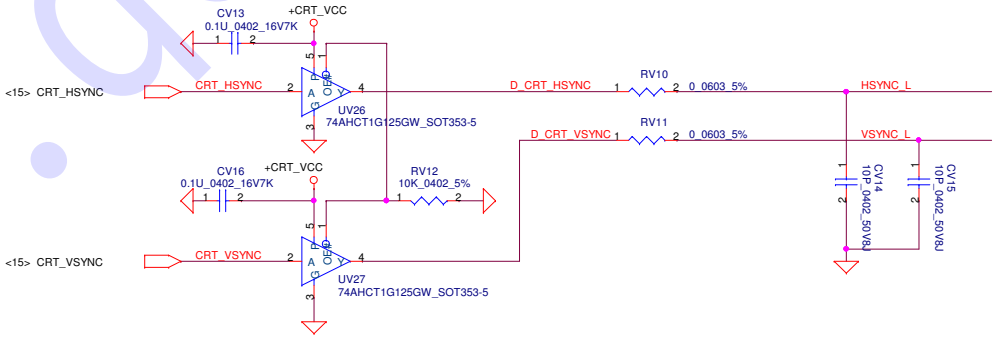
Compal Electronics, Inc.		
Title: PCH (8/8) VSS		
Size:	Document Number: LA-8241P	Rev: 1.0
Date: Wednesday, February 01, 2012	Sheet 20 of 56	

C R T









Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	VGA / LVDS /camera conn.		
Size	Document Number	LA-8241P	Rev 1.0
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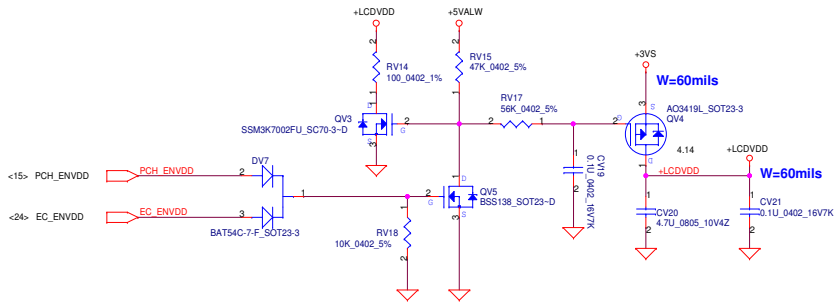
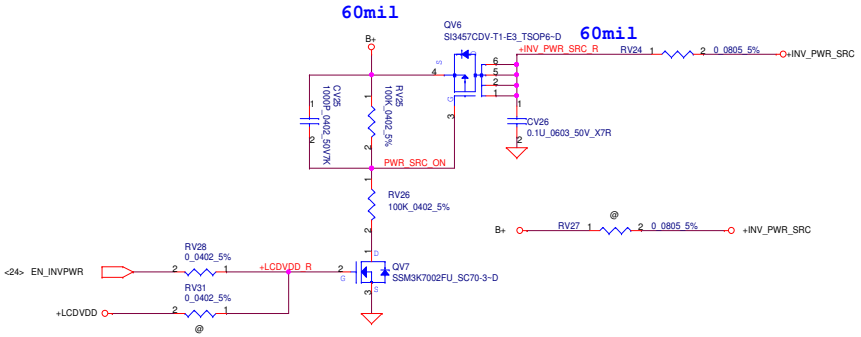
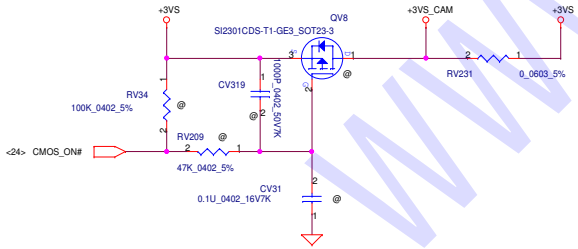
LCD PWR CTRL



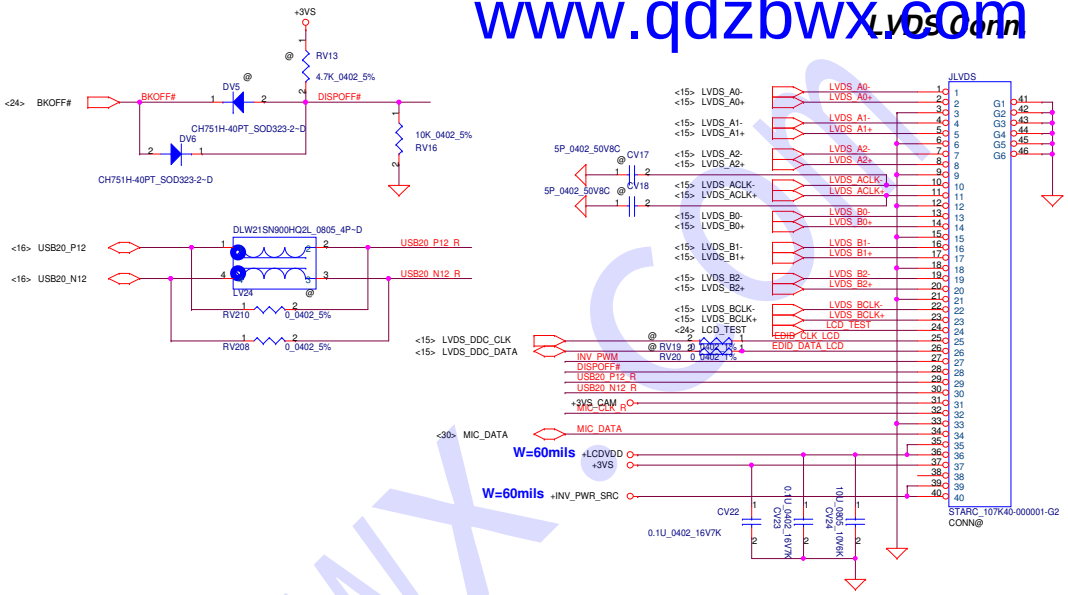
LCD backlight PWR CTRL



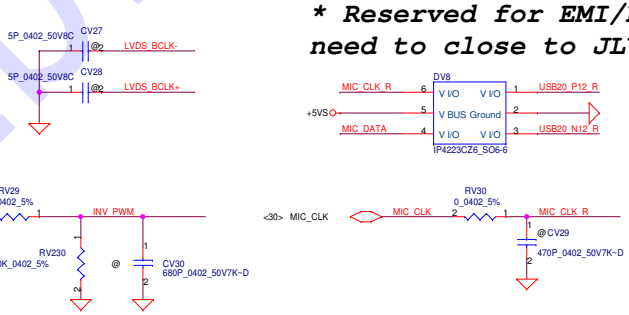
Wedcam PWR CTRL



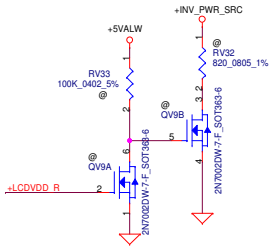
LVDS conn



* Reserved for EMI/ESD/RF need to close to JLVDS



* Reserved for LCD sequence tuning



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	LVDS /camera conn.		
Size	Document Number	LA-8241P	Rev 1.0
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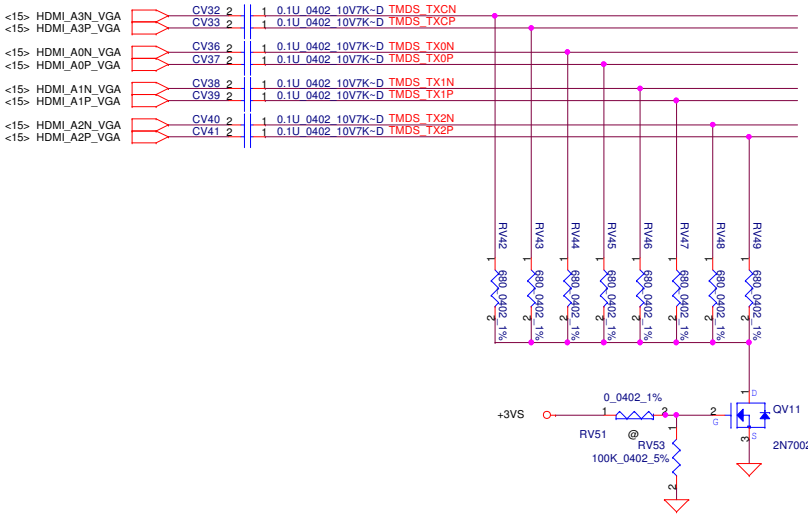
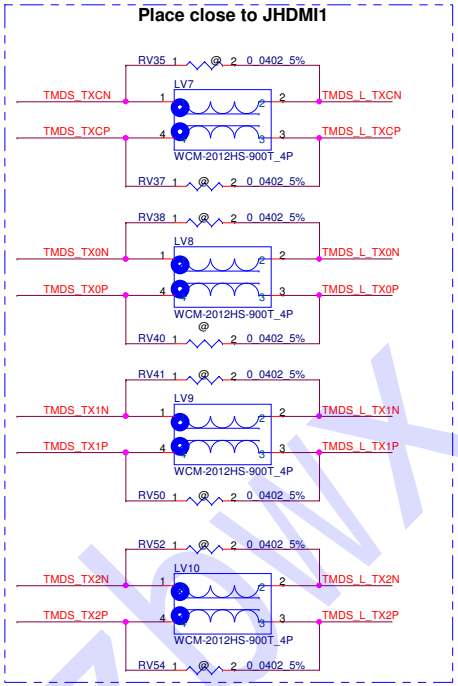
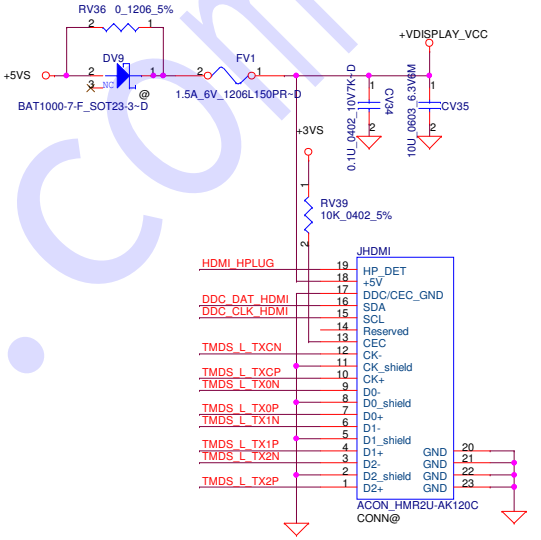
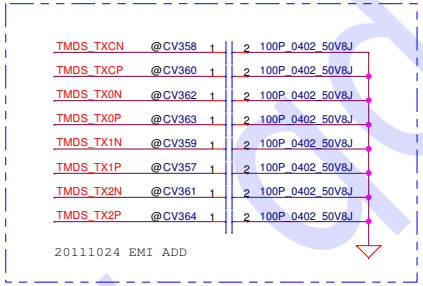


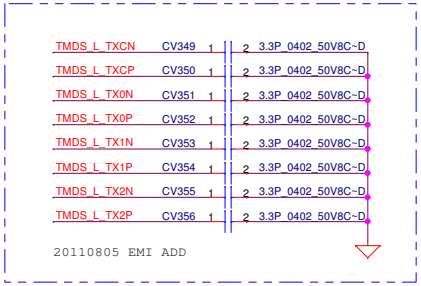


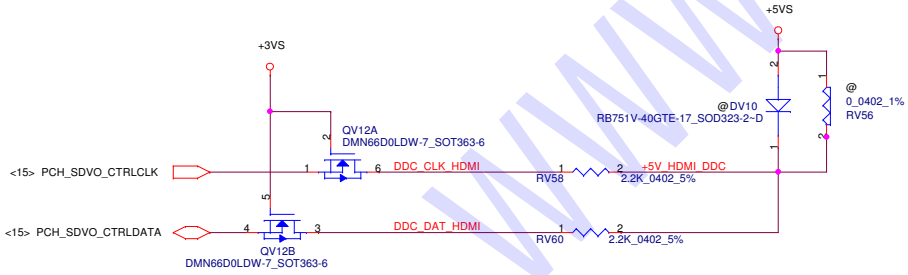


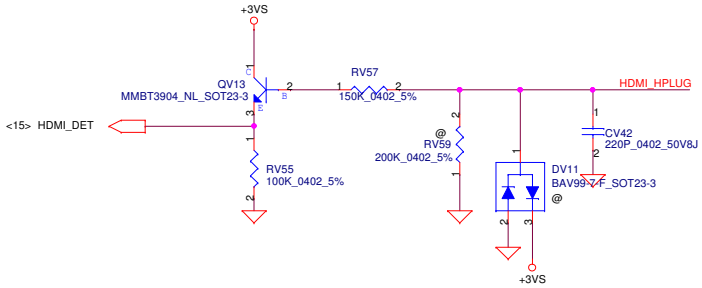
46@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM









Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: HDMI

Size	Document Number	Rev
Custom	LA-8241P	1.0

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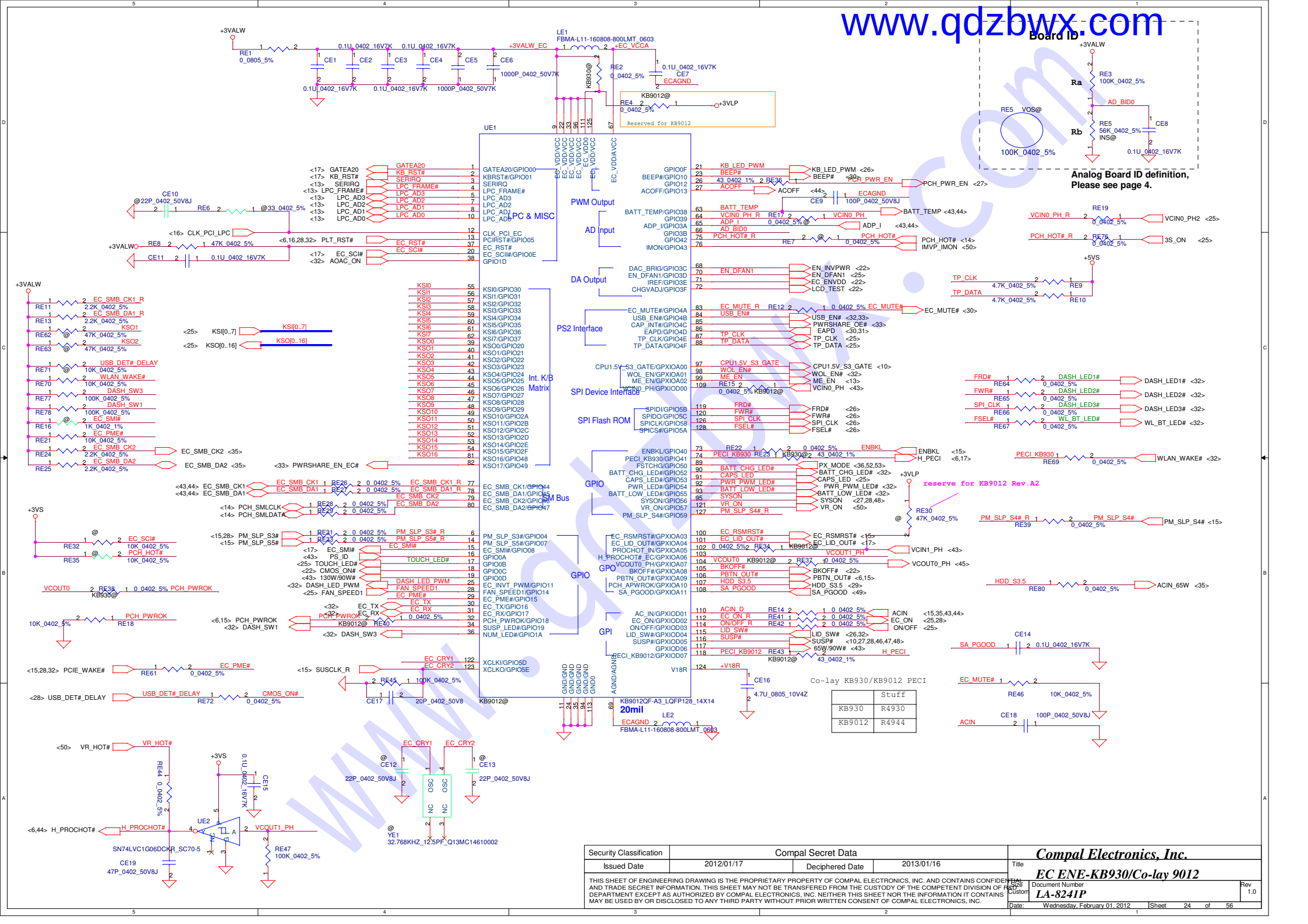
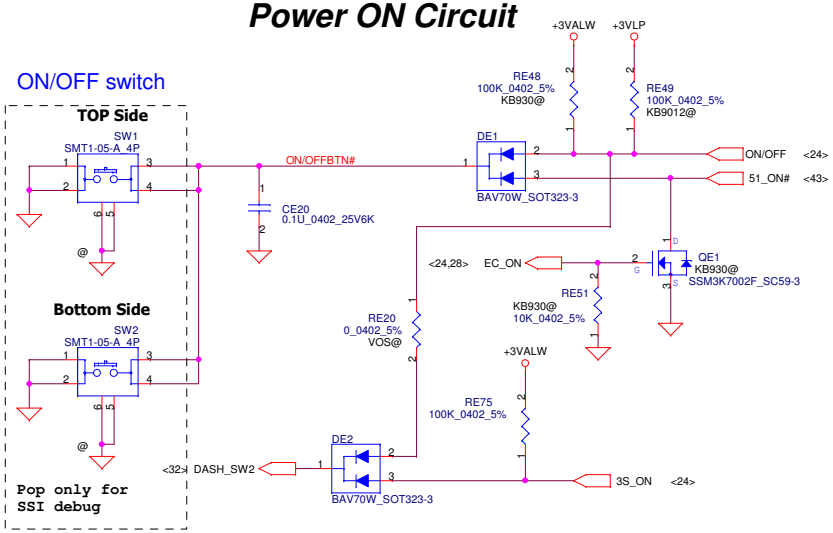
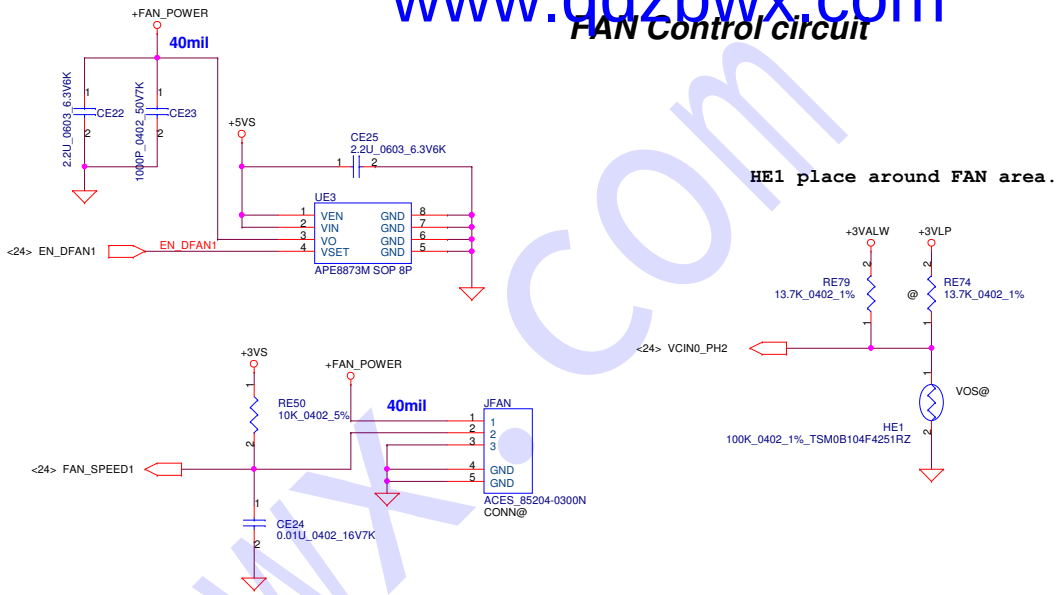


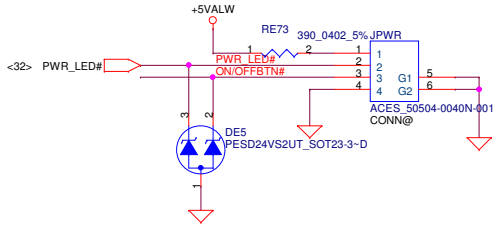
Power ON Circuit



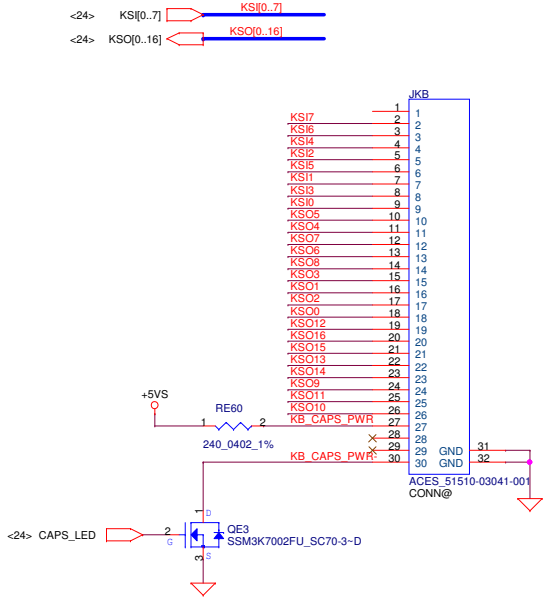
FAN Control circuit



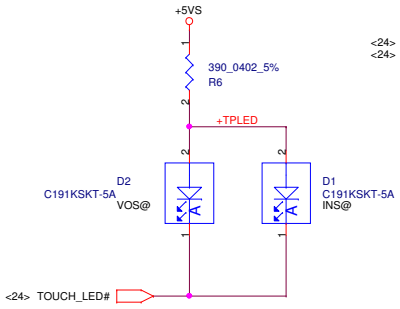
To POWER/B



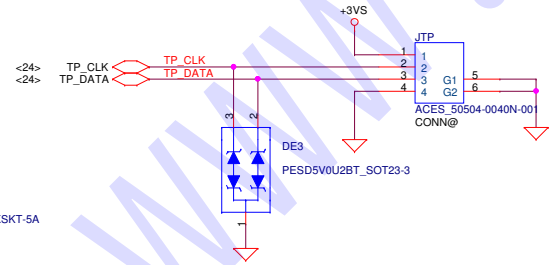
INT_KBD Conn.



Touch Pad LED



Touch pad



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	SW/TP/SCREW		
Size: Custom	Document Number: LA-8241P		Rev: 1.0
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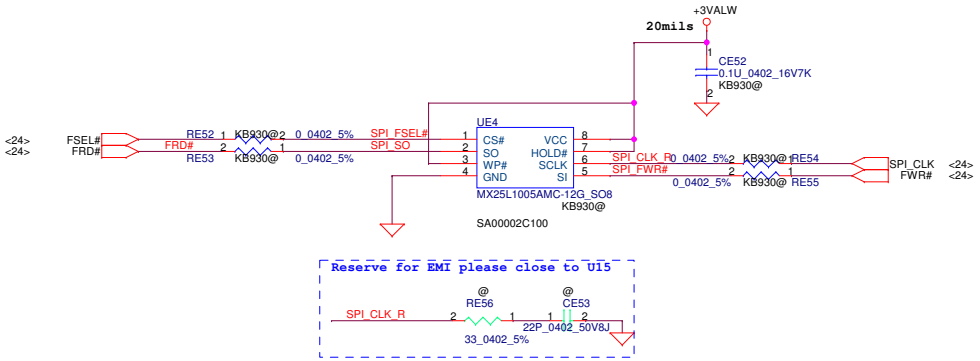
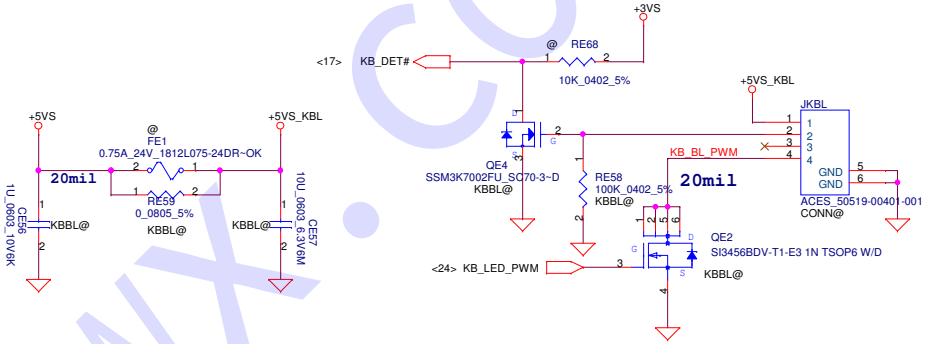
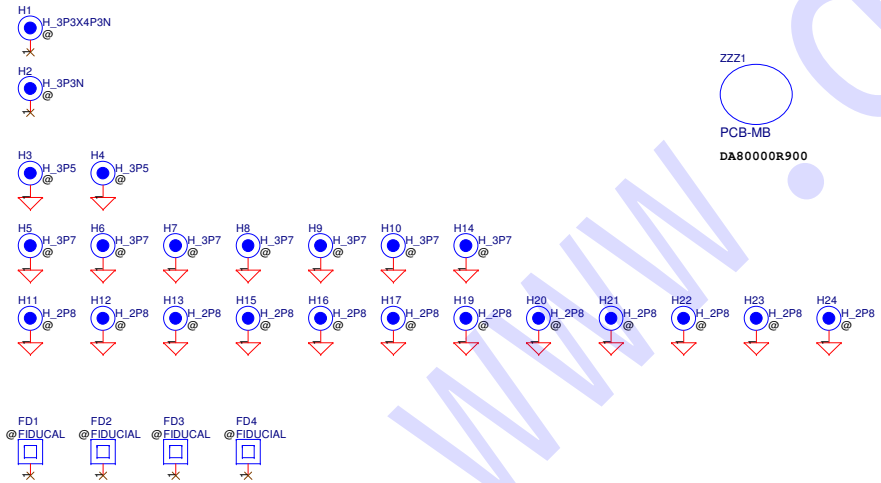
SPI ROM 128KB



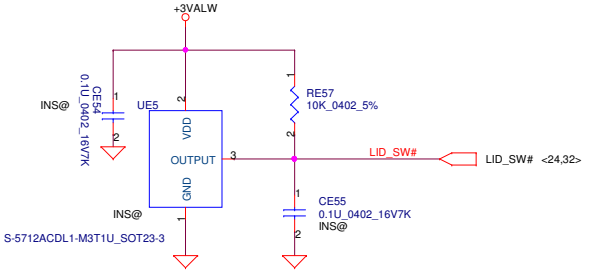
Keyboard back light



Screw Hole



Lid Switch



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	CONN & LID		
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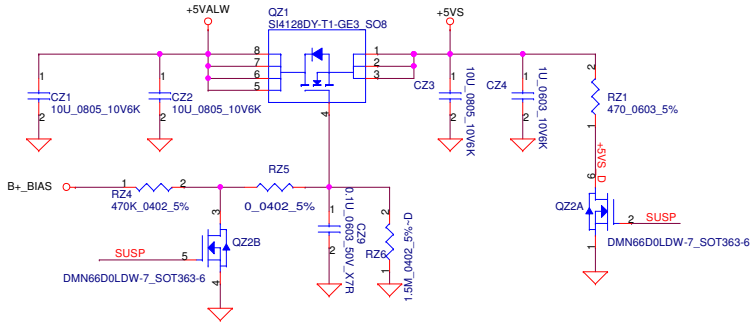
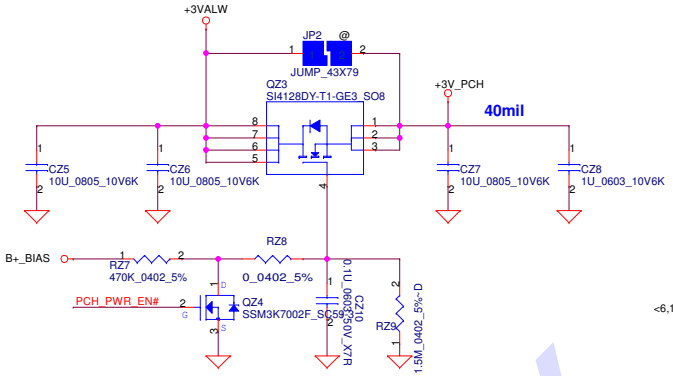
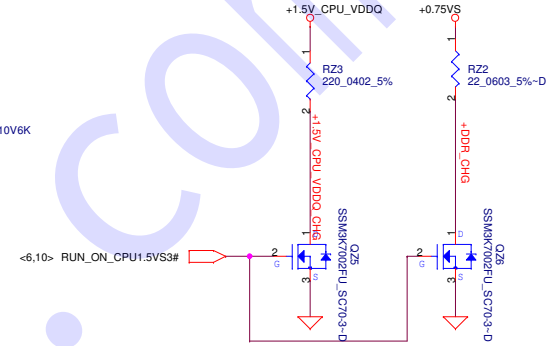
+5VALW to +5VS

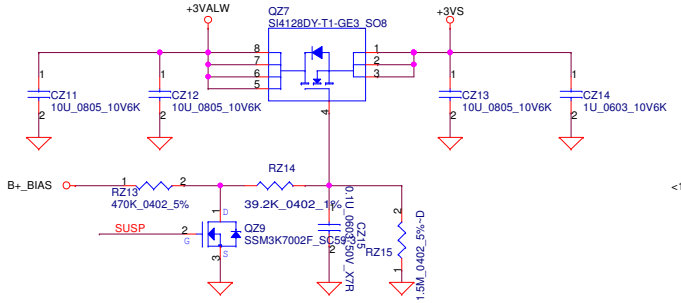


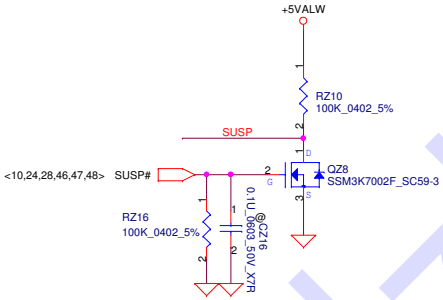
+3VALW to +3V_PCH

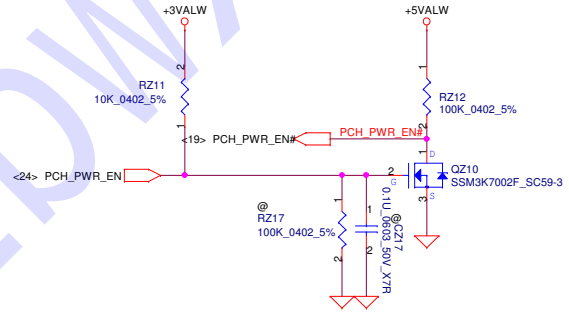




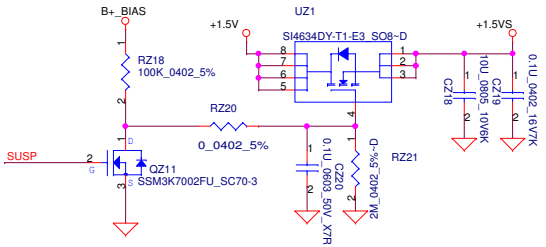
+3VALW to +3VS

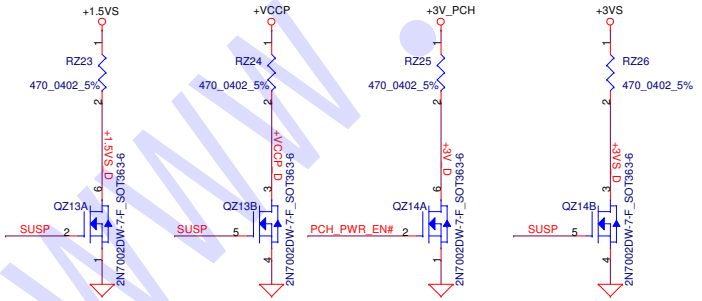


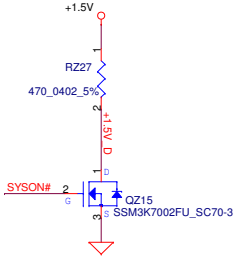


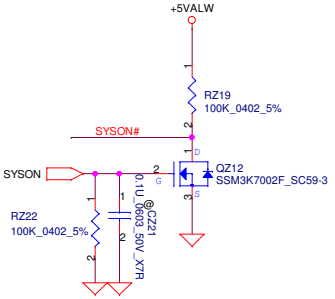


+1.5V To +1.5VS









Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.	
Title	DC/DC Interface
Size	Document Number: LA-8241P
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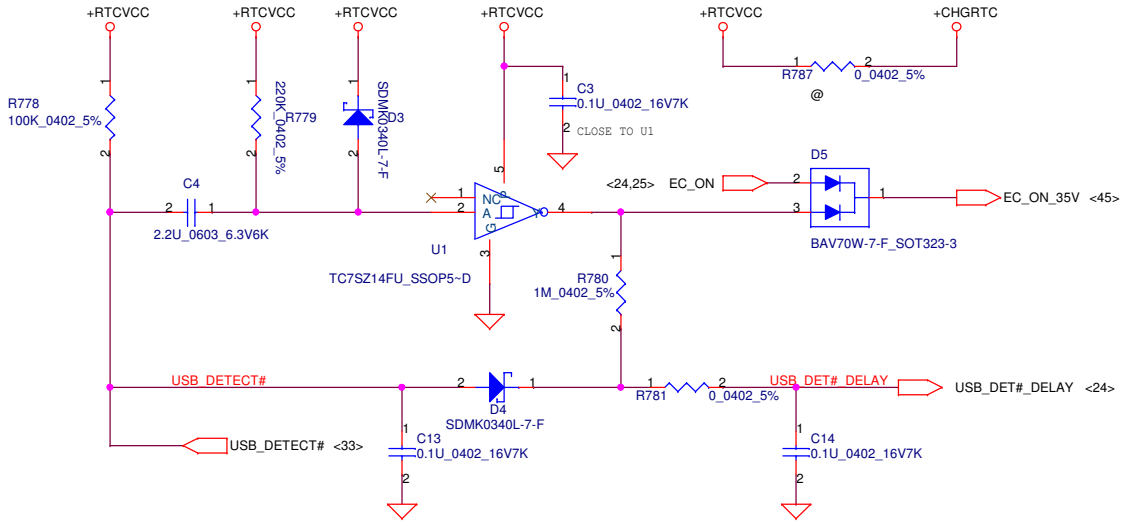
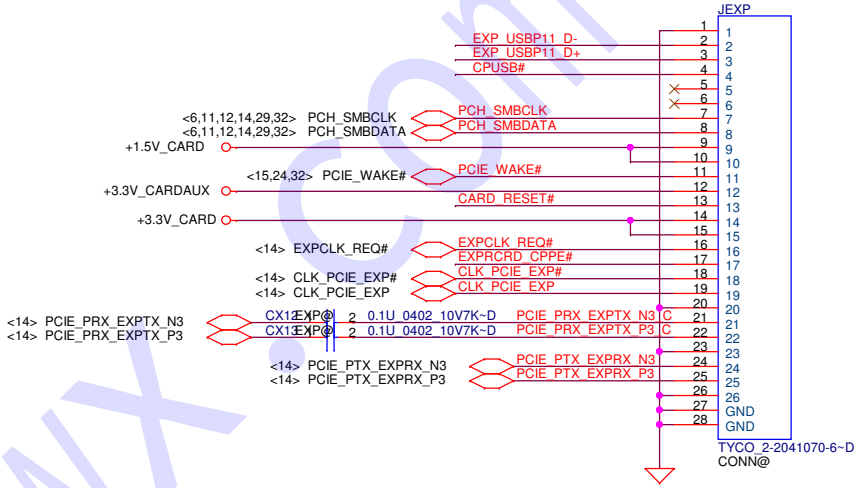
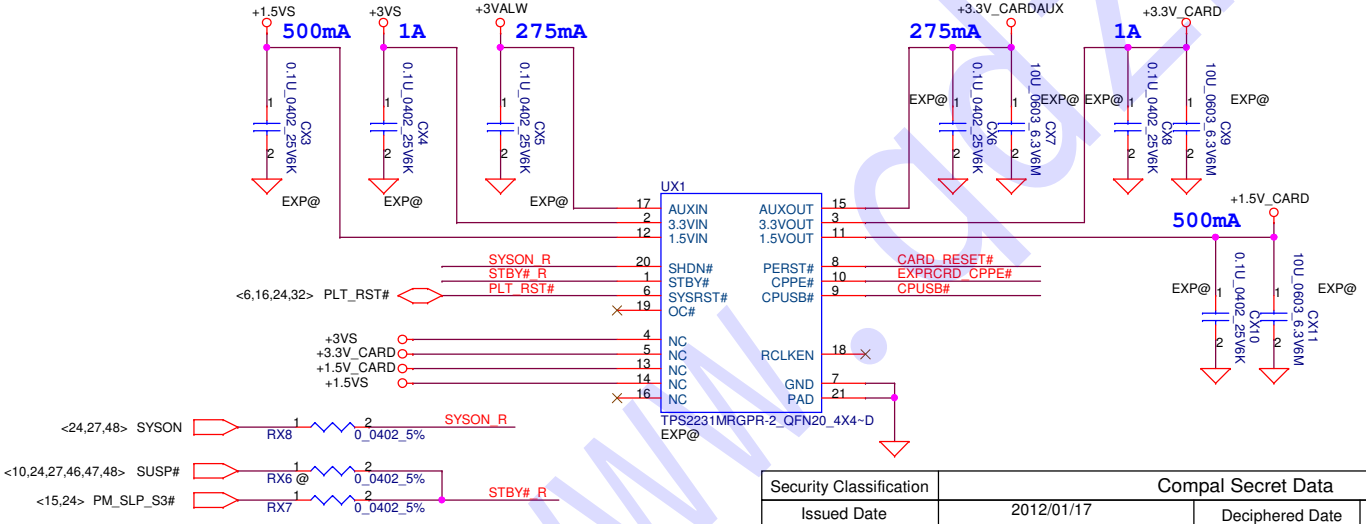
USB Detected for PWR Share

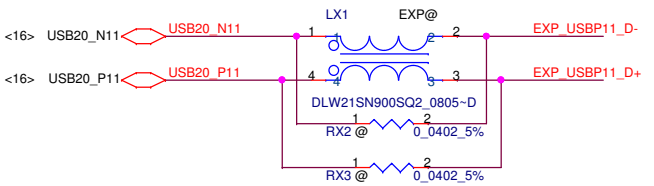


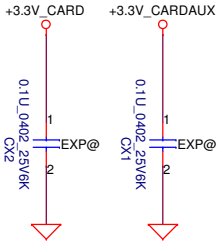
Express Card

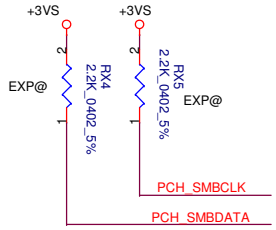


Express Card PWR S/W









Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PROCESSOR(1/6) DMI,FDI,PEG

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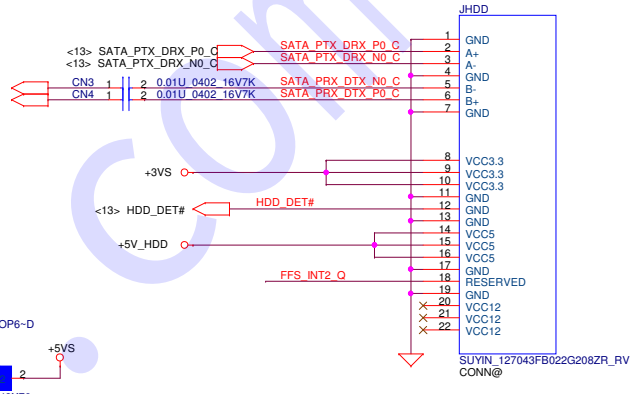
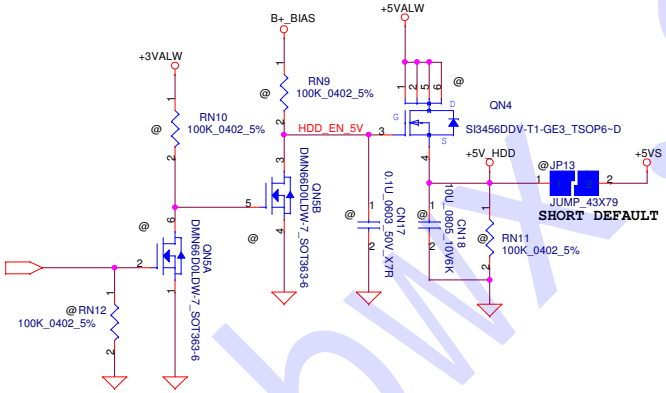
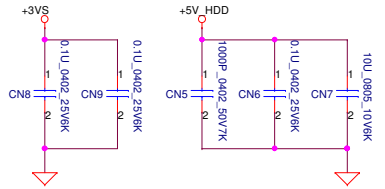
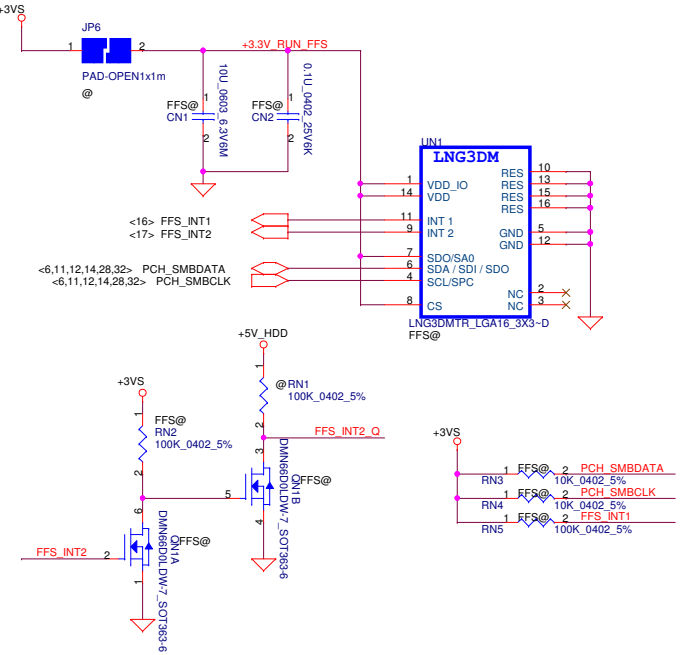
SATA HDD Conn.



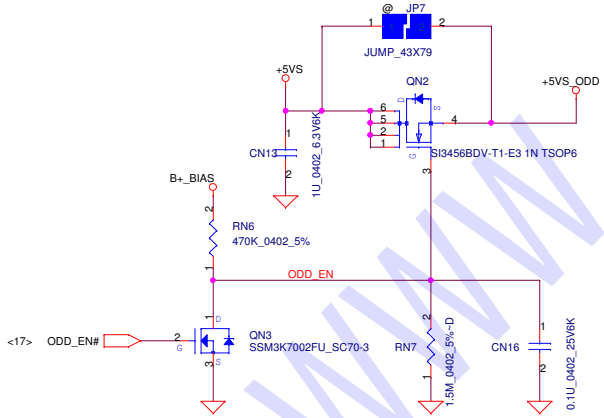
+5V_HDD Source



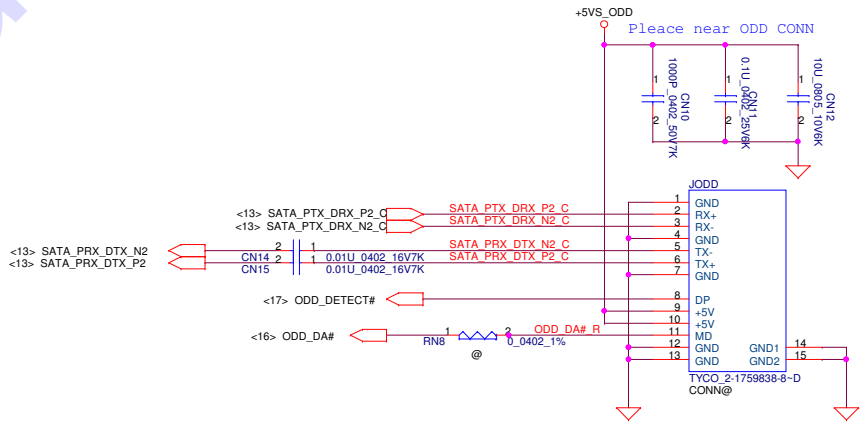




ODD Power Control



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	HDD/ODD/FAN		
Size	Document Number		Rev
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AVDD_3.3 pinis output of internal LDO. NOT connect to external supply.

Please bypass caps very close to device.

Vendor recommend VDD_IO is the same with HDA

UA1

CX20672-21Z_QFN40_6X6

Reserve for EMI

Internal SPEAKER

OUTPUT 1Vrms

MIC JACK

HeadPhone JACK

Close to UA1 Pin11,13,14,16

close to Codec

wide 30MIL

EC Beep <24> BEEP#

ICH Beep <13> HDA_SPKR

PC Beep

for EMI

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PROCESSOR(1/6) DMI,FDI,PEG

Size | Document Number: LA-8241P | Rev: 1.0

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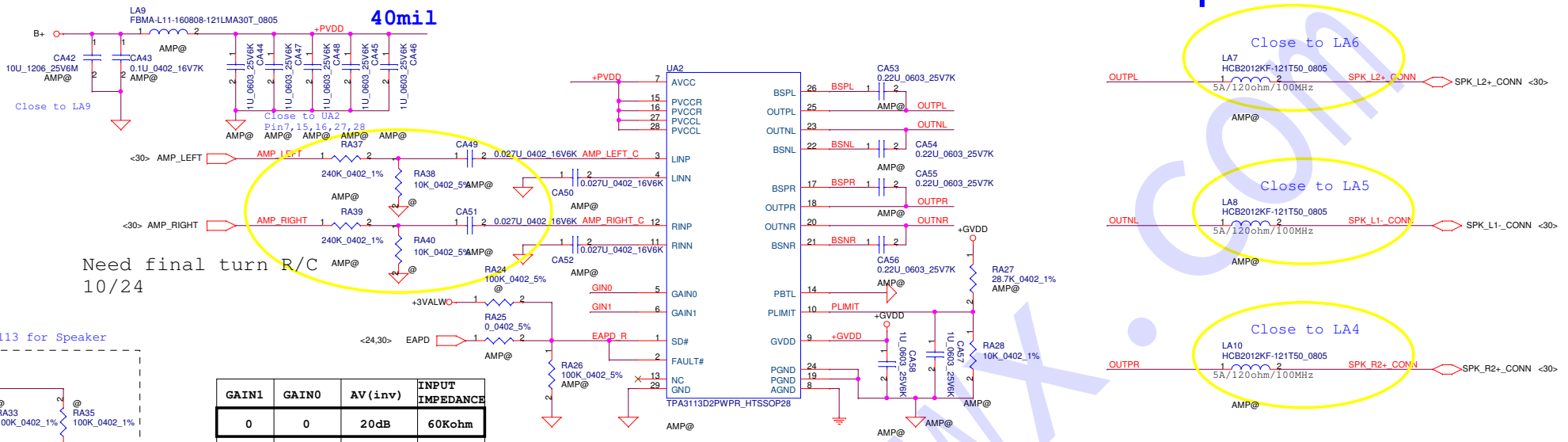
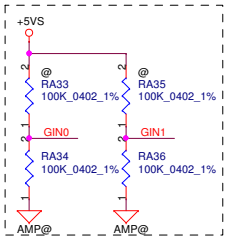
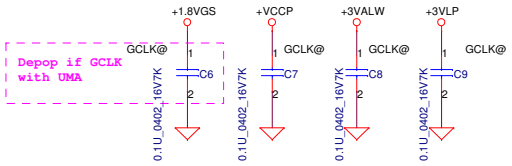


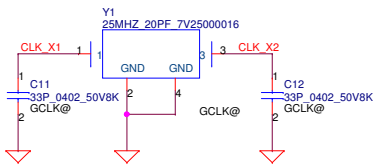
Need final turn R/C
10/24

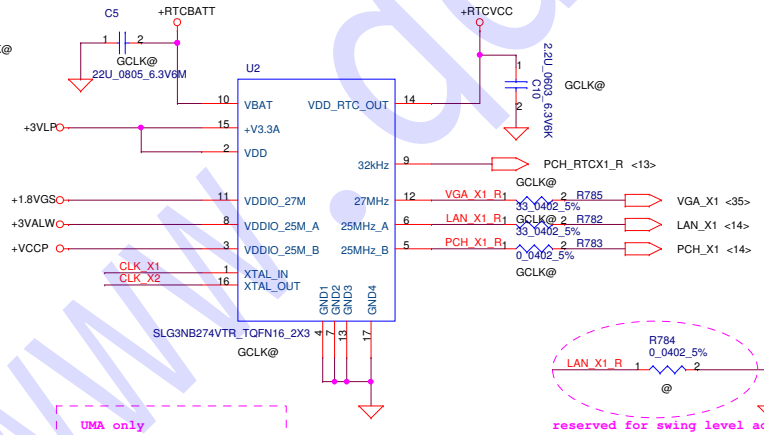
TPA3113 for Speaker

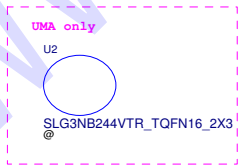


GAIN1	GAIN0	AV(inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm









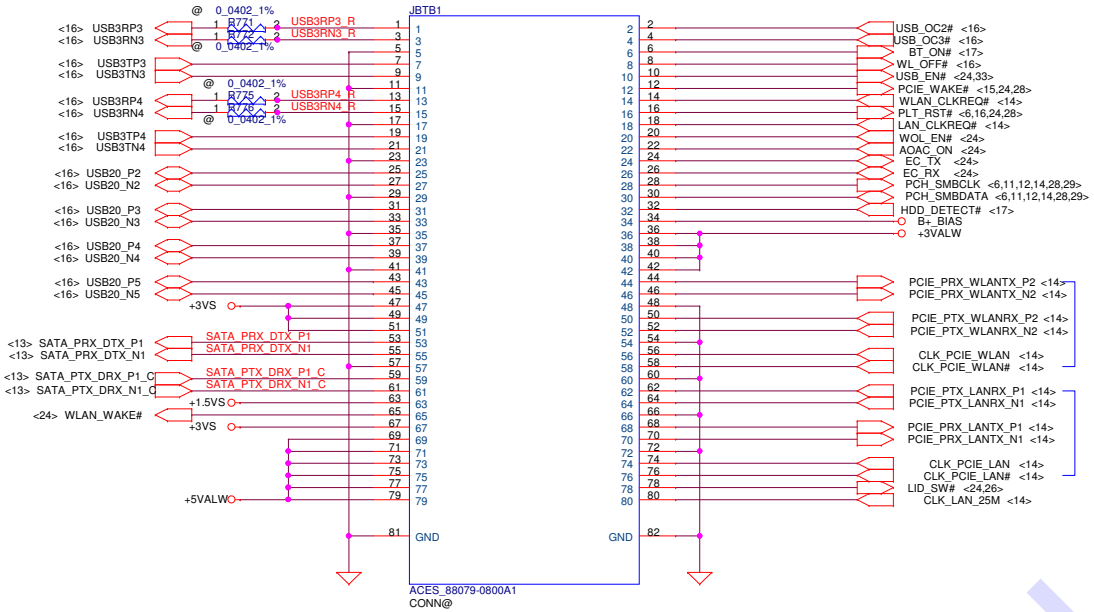
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: AMP

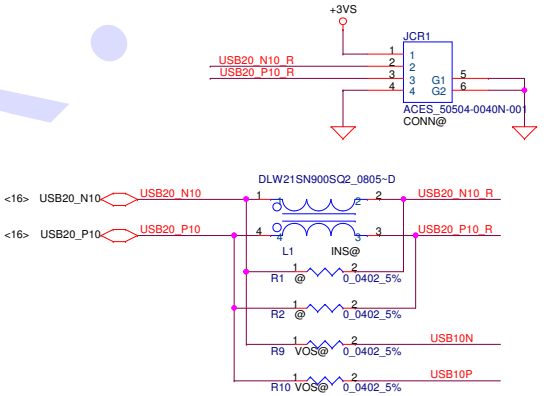
Size: Custom | Document Number: LA-8241P | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 31 of 56



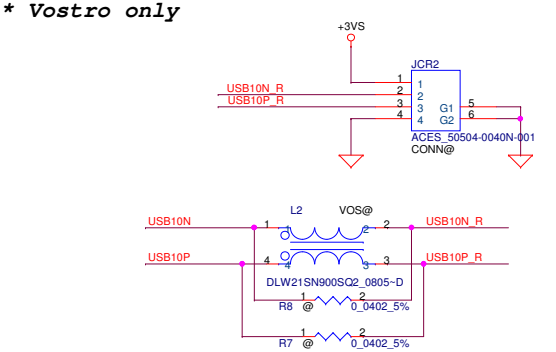
To CardReader/B

*** Inspiron only**

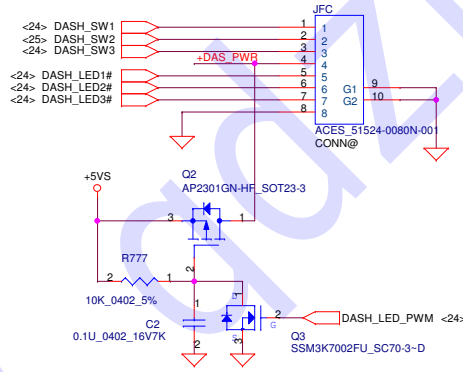


To CardReader/B

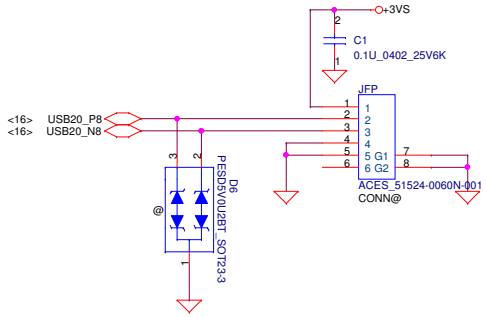
*** Vostro only**



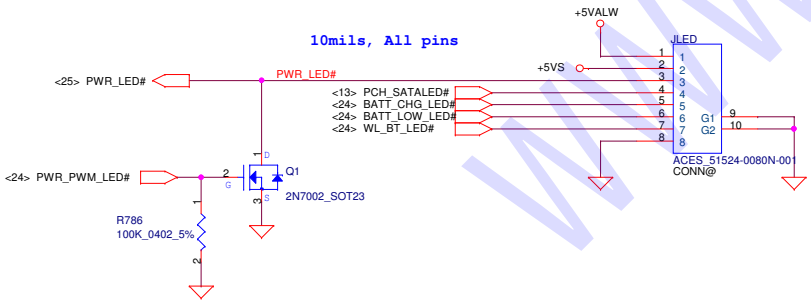
TO Function/B

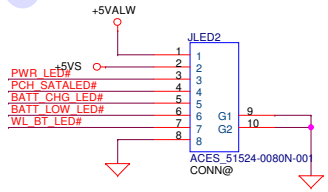


To Finger Print



To LED/B





Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.	
Title	PROCESSOR(1/6) DMI,FDI,PEG
Size	Document Number: LA-8241P
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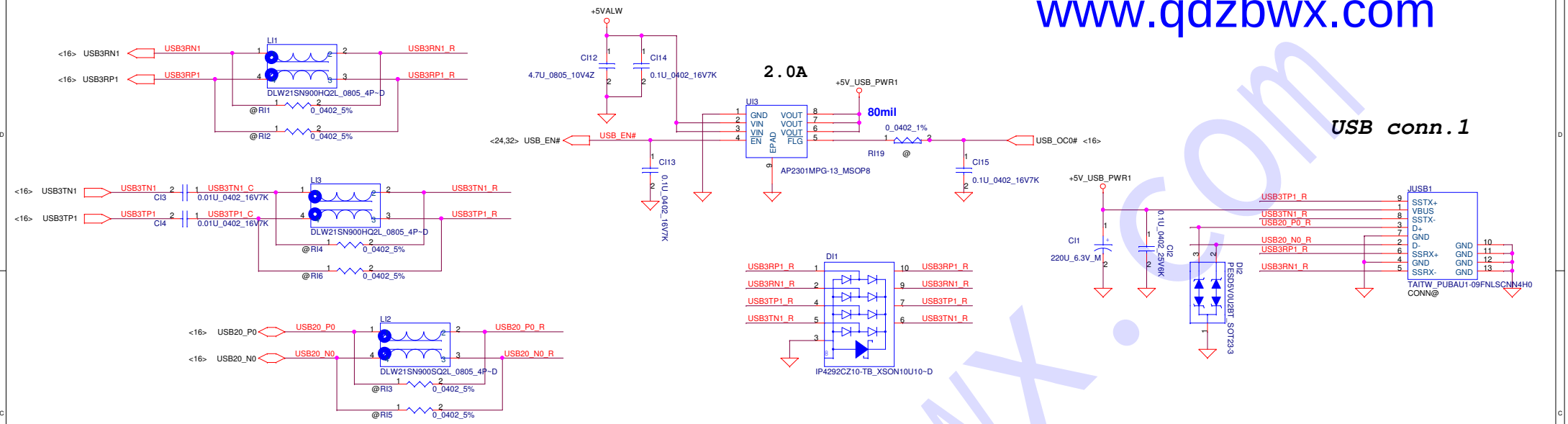

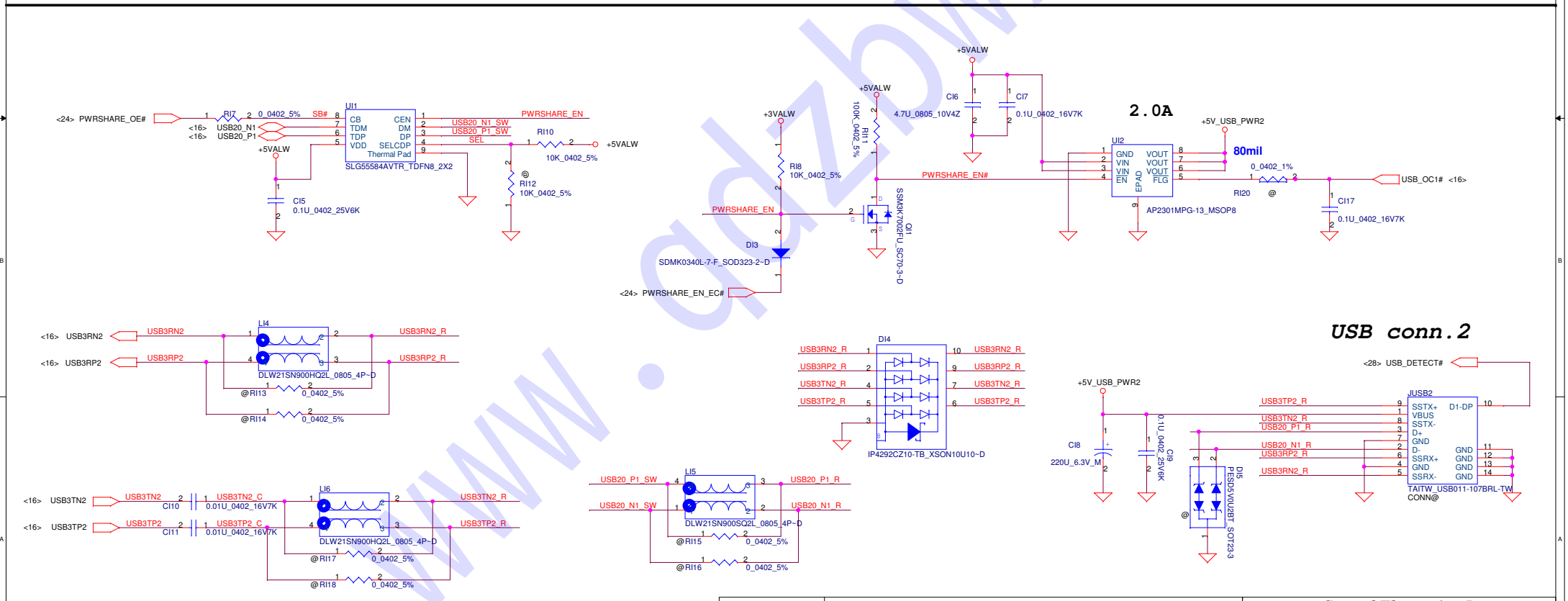

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	PROCESSOR(1/6) DMI,FDI,PEG		
Size	Document Number	LA-8241P	Rev 1.0
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GFX PCIE LANE REVERSAL

<5> PEG_HTX_C_GRX_P[7..0]
<5> PEG_HTX_C_GRX_N[7..0]

PEG_HTX_C_GRX_P[7..0]
PEG_HTX_C_GRX_N[7..0]

UV1A

PEG_GTX_C_HRX_P[7..0]
PEG_GTX_C_HRX_N[7..0]

PEG_GTX_C_HRX_P[7..0] <5>
PEG_GTX_C_HRX_N[7..0] <5>

PEG_HTX_C_GRX_P0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PCIE_CRX_C_GTX_P0	220nF_0402_16V7K	CV43	DIS@	PEG_GTX_C_HRX_P0
PEG_HTX_C_GRX_N0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PCIE_CRX_C_GTX_N0	220nF_0402_16V7K	CV44	DIS@	PEG_GTX_C_HRX_N0
PEG_HTX_C_GRX_P1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PCIE_CRX_C_GTX_P1	220nF_0402_16V7K	CV45	DIS@	PEG_GTX_C_HRX_P1
PEG_HTX_C_GRX_N1	W36	PCIE_RX1N	PCIE_TX1N	W32	PCIE_CRX_C_GTX_N1	220nF_0402_16V7K	CV46	DIS@	PEG_GTX_C_HRX_N1
PEG_HTX_C_GRX_P2	W38	PCIE_RX2P	PCIE_TX2P	U33	PCIE_CRX_C_GTX_P2	220nF_0402_16V7K	CV47	DIS@	PEG_GTX_C_HRX_P2
PEG_HTX_C_GRX_N2	V37	PCIE_RX2N	PCIE_TX2N	U32	PCIE_CRX_C_GTX_N2	220nF_0402_16V7K	CV48	DIS@	PEG_GTX_C_HRX_N2
PEG_HTX_C_GRX_P3	V35	PCIE_RX3P	PCIE_TX3P	U30	PCIE_CRX_C_GTX_P3	220nF_0402_16V7K	CV49	DIS@	PEG_GTX_C_HRX_P3
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	N38	PCIE_RX8P	PCIE_TX8P	N33					
	M37	PCIE_RX8N	PCIE_TX8N	N32					
	M35	PCIE_RX9P	PCIE_TX9P	N30					
	L36	PCIE_RX9N	PCIE_TX9N	N29					
	L38	PCIE_RX10P	PCIE_TX10P	L33					
	K37	PCIE_RX10N	PCIE_TX10N	L32					
	K35	PCIE_RX11P	PCIE_TX11P	L30					
	J36	PCIE_RX11N	PCIE_TX11N	L29					
	J38	PCIE_RX12P	PCIE_TX12P	K33					
	H37	PCIE_RX12N	PCIE_TX12N	K32					
	H35	PCIE_RX13P	PCIE_TX13P	J33					
	G36	PCIE_RX13N	PCIE_TX13N	J32					
	G38	PCIE_RX14P	PCIE_TX14P	K30					
	F37	PCIE_RX14N	PCIE_TX14N	K29					
	F35	PCIE_RX15P	PCIE_TX15P	H33					
	E37	PCIE_RX15N	PCIE_TX15N	H32					

PCI EXPRESS INTERFACE

12/8 Remove RX8~15

12/8 Remove CV59~CV74 TX8~15

CLOCK

<14> CLK_PEG_VGA
<14> CLK_PEG_VGA#

CLK_PEG_VGA AB35 PCIE_REFCLKP
CLK_PEG_VGA# AA36 PCIE_REFCLKN

RV64 DIS@ 1K_0402_5% AH16 PWRGOOD

GPU_RST# AA30 PERSTB

DIS@ RV66 100K_0402_5%

THAMES XT M2 TH@

UV1 CH@
Chelsea Pro

CALIBRATION

PCIE_CALRP Y30 1.27K_0402_1% DIS@ RV63
PCIE_CALRN Y29 2K_0402_1% DIS@ RV65
1K_0402_1% CH@ RV203 +1.0VGS

Chelsea Only
RV198 CH@1.69K_0402_1%~D +1.0VGS

Thames/seymour Only

Install 2K for Thames/Seymour

LVDS Interface

UV1G

LVDS CONTROL
VARY_BL AK27
DIGON AJ27

TXCLK_UP_DPF3P AK35
TXCLK_UN_DPF3N AL36
TXOUT_U0P_DPF2P AJ38
TXOUT_U0N_DPF2N AK37
TXOUT_U1P_DPF1P AH35
TXOUT_U1N_DPF1N AJ36
TXOUT_U2P_DPF0P AG38
TXOUT_U2N_DPF0N AH37
TXOUT_U3P AF35
TXOUT_U3N AG36

LVTMDP

TXCLK_LP_DPE3P AP34
TXCLK_LN_DPE3N AR34
TXOUT_L0P_DPE2P AW37
TXOUT_L0N_DPE2N AU35
TXOUT_L1P_DPE1P AR37
TXOUT_L1N_DPE1N AU39
TXOUT_L2P_DPE0P AP35
TXOUT_L2N_DPE0N AR35
TXOUT_L3P AN36
TXOUT_L3N AP37

THAMES XT M2 @

RV61 @ 0_0402_5%
+3VGS

<16> PCH_PLTRST#
<16> DGPU_HOLD_RST#

UV13
DIS@ MC74VHC1G08DFT2G SC70 5P

GPU_RST#

CV326 0.1U_0402_25V6K DIS@

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_PCIE/LVDS

Size: Custom | Document Number: LA-8241P | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 34 of 56

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTING:
0 = DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DON'T CARE
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS		RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS	0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test	0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED		0
BIF_VGA DIS	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS		0
RSVD	H2SYNC			0
RSVD	GENERICC			0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI		11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2	
64MX16 (1G) ★Hynix 1GB PN:SA000041S3L	RV67	RV70	RV72	PT
64MX16 (1G) ★Samsung 1GB PN:SA00004GS1L	RV68	RV69	RV72	PT
128M16 (2G) Hynix 2GB PN:SA00003YQ1L	RV67	RV70	RV71	
128M16 (2G) Samsung 2GB PN:SA000047Q1L	RV68	RV69	RV71	
64MX16 (1G) ★Micron 1GB PN:SA00004Y20L	RV67	RV69	RV71	PT

STRAPS

Internal VGA Thermal Sensor

VGA Thermal Sensor ADM1032ARMZ

Closed to GPU

Address:100_1101

12/8 Add external thermal sensor BOM

Add 12/6 for MLPS

Add 12/8

Reserved test pad of CRT Signals for debug

Not share via for other GND

NC_TSVSSQ should be tied to GND on Thames/Seymour

CRT

(Thames 75mA)

(Thames 125mA) 0.935V@Chelsea

(Thames 5mA)

(1.8V@20mA TSVDD)

(1.8V@100mA VDD1DI)

(1.8V@65mA AVDD)

65mA

100mA

10mil

20mil

0.60 V level, Please VREFG Divider ans cap close to ASIC

XTALIN Voltage Swing: 1.8 V

THAMES XT M2

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

Security Classification	Compal Secret Data	
Issued Date	2012/01/17	Deciphered Date 2013/01/16

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Main_MSIC

Size: Custom | Document Number: LA-8241P | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 35 of 56

Circuits to support BACO

Switch circuits in BACO designs for Thames/Seymour only

55mA@1.0V, in BACO mode

for PX4.0

for PX4.0 and PX5.0

for PX5.0

PX_MODE=1 for Normal Operation

PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

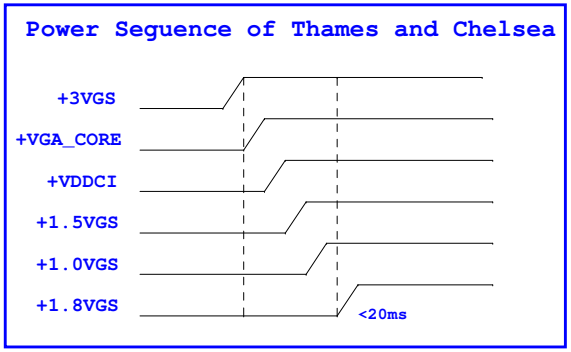
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON

PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF

PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

Power Seguence of Thames and Chelsea

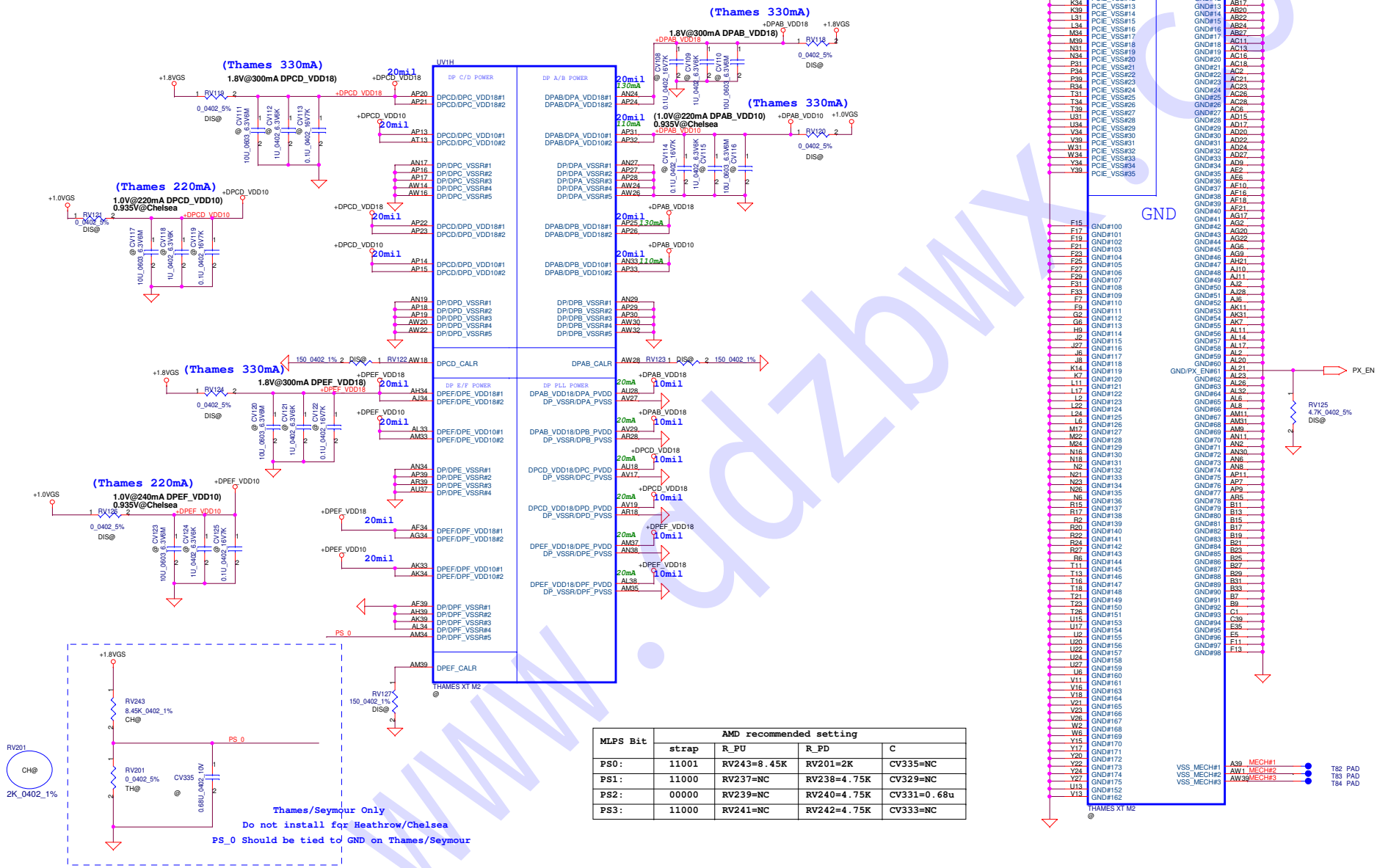


+1.8VS TO +1.8VGS

+1.5VS TO +1.5VGS

+3.3VS TO +3.3VGS

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/01/17	Deciphered Date	2013/01/16
Title	ATI_SeymourXT_M2_BACO POWER		
Size C	Document Number LA-8241P		Rev 1.0
Date: Wednesday, February 01, 2012	Sheet 36 of 56		



MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: ATI_SetmourXT_M2_PWR_GND

Size	Document Number	Rev
C	LA-8241P	1.0

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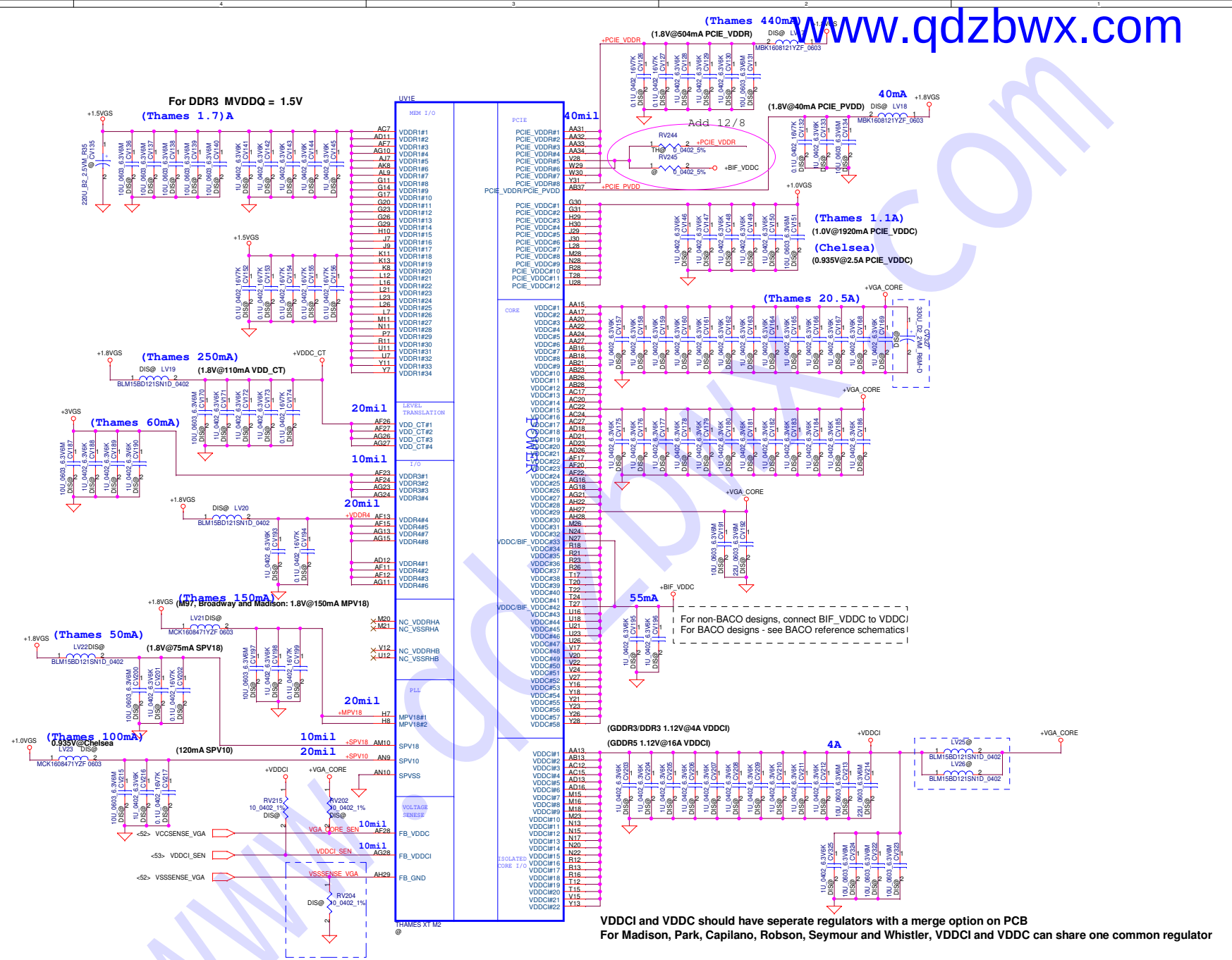
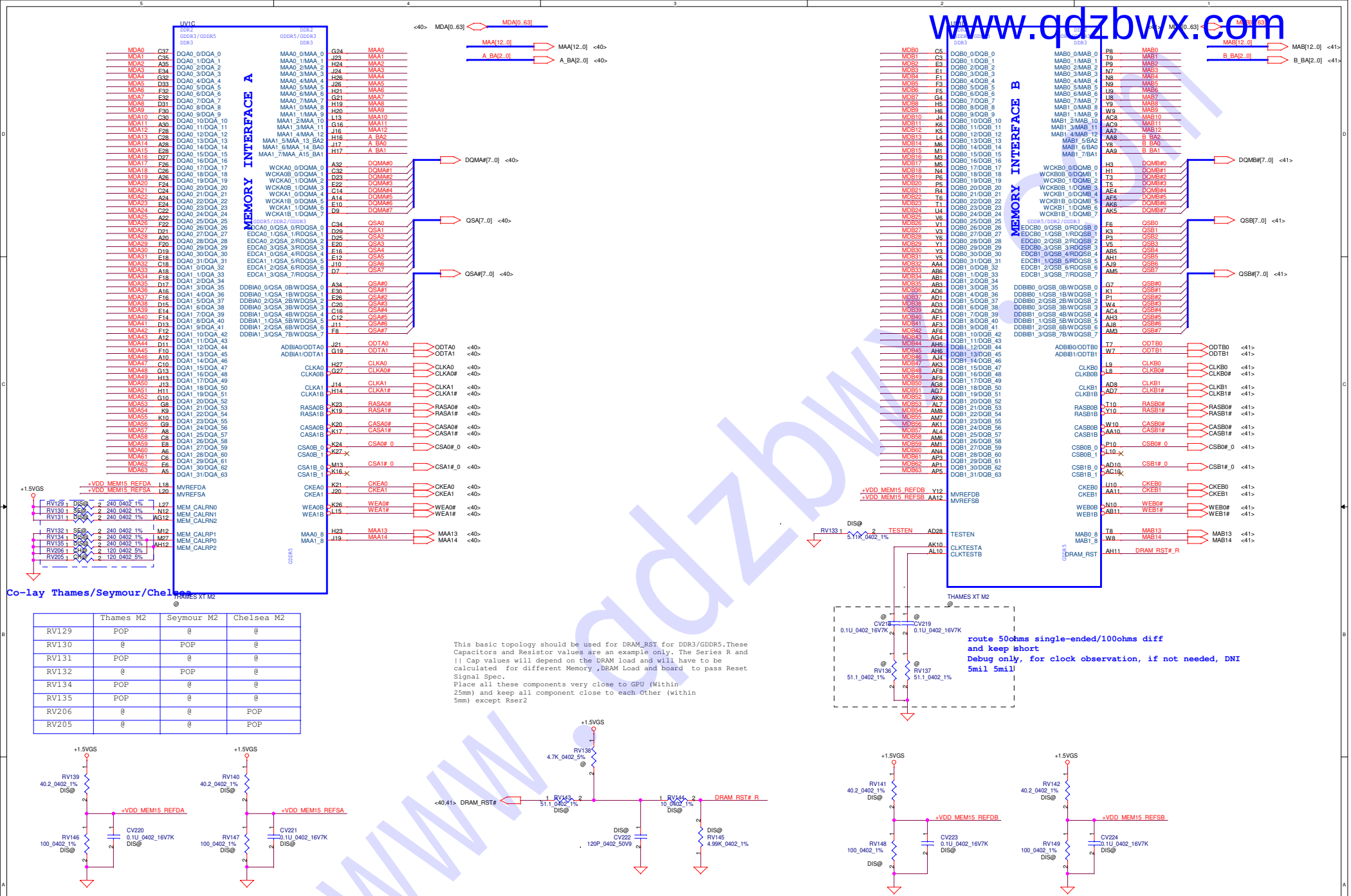


Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	ATI_SeymourXT_M2_Power		
Size C	Document Number LA-8241P		Rev 1.0
Date: Wednesday, February 01, 2012		Sheet 38 of 56	



Co-lay Thames/Seymour/Chelsea

	Thames M2	Seymour M2	Chelsea M2
RV129	POP	@	@
RV130	@	POP	@
RV131	POP	@	@
RV132	@	POP	@
RV134	POP	@	@
RV135	POP	@	@
RV206	@	@	POP
RV205	@	@	POP

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil

Security Classification	Compal Secret Data
Issued Date	2012/01/17
Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_MEM IF

Size	Document Number	Rev
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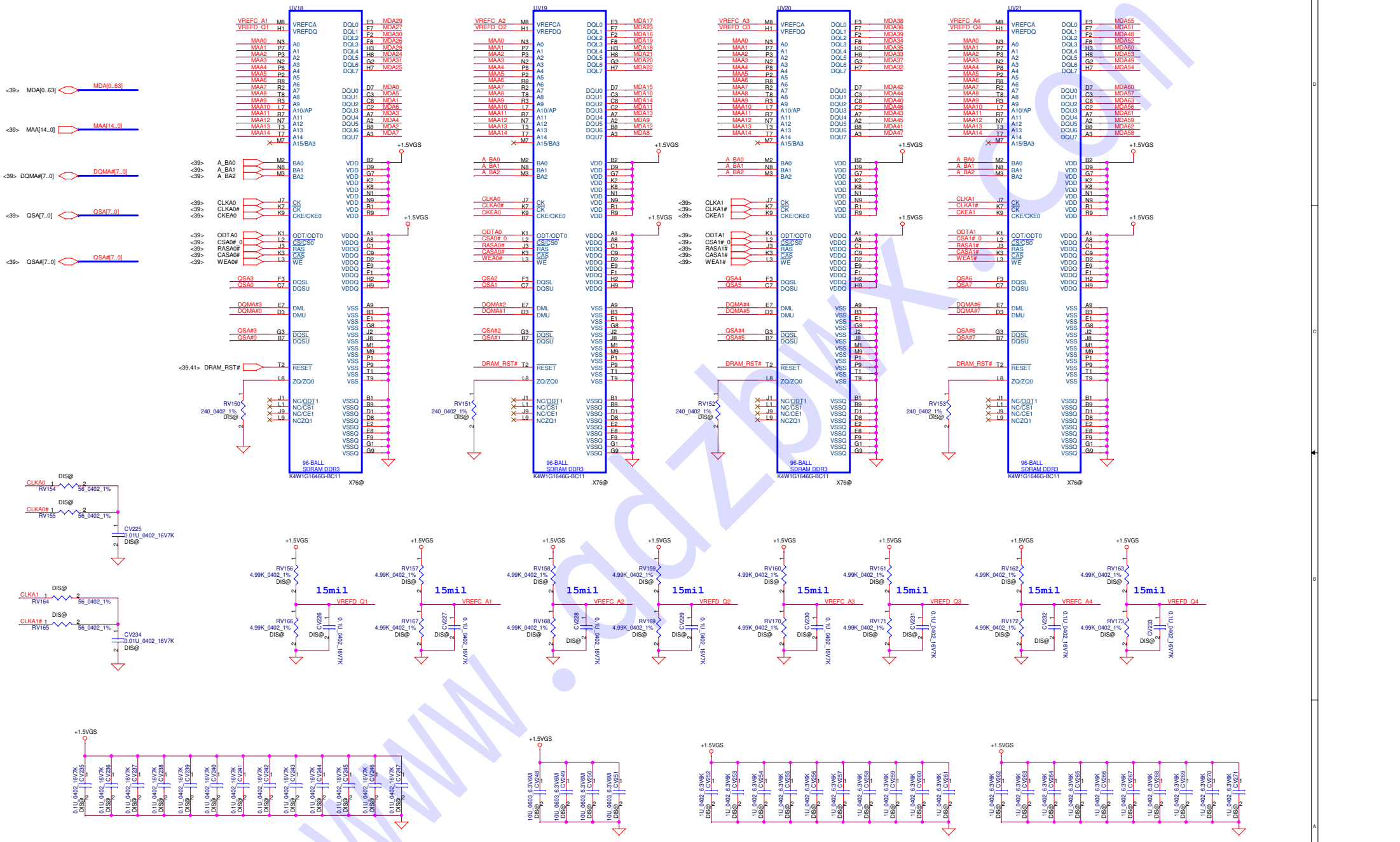
CHANNEL A: 256MB/512MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_A

Size	Document Number	Rev
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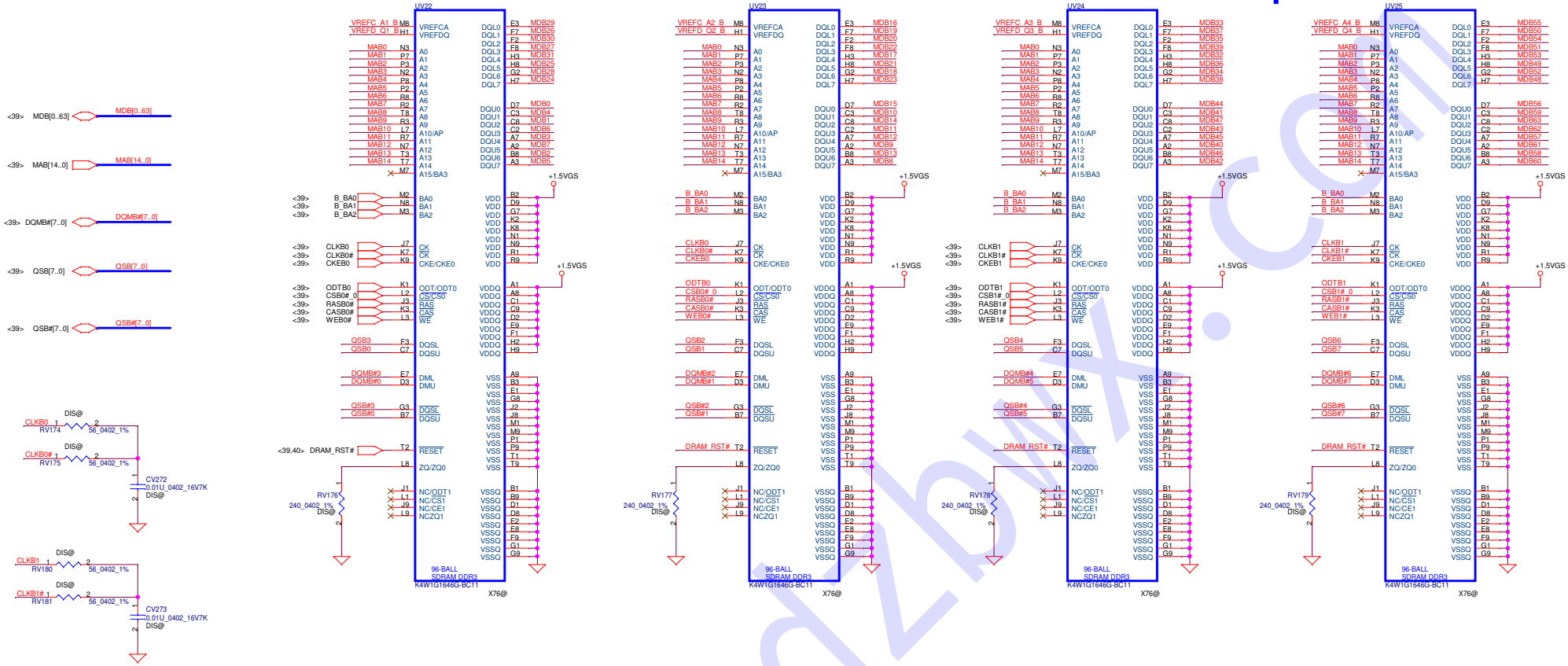
CHANNEL B: 256MB/512MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_B

Size	Document Number	Rev
C	LA-8241P	1.0

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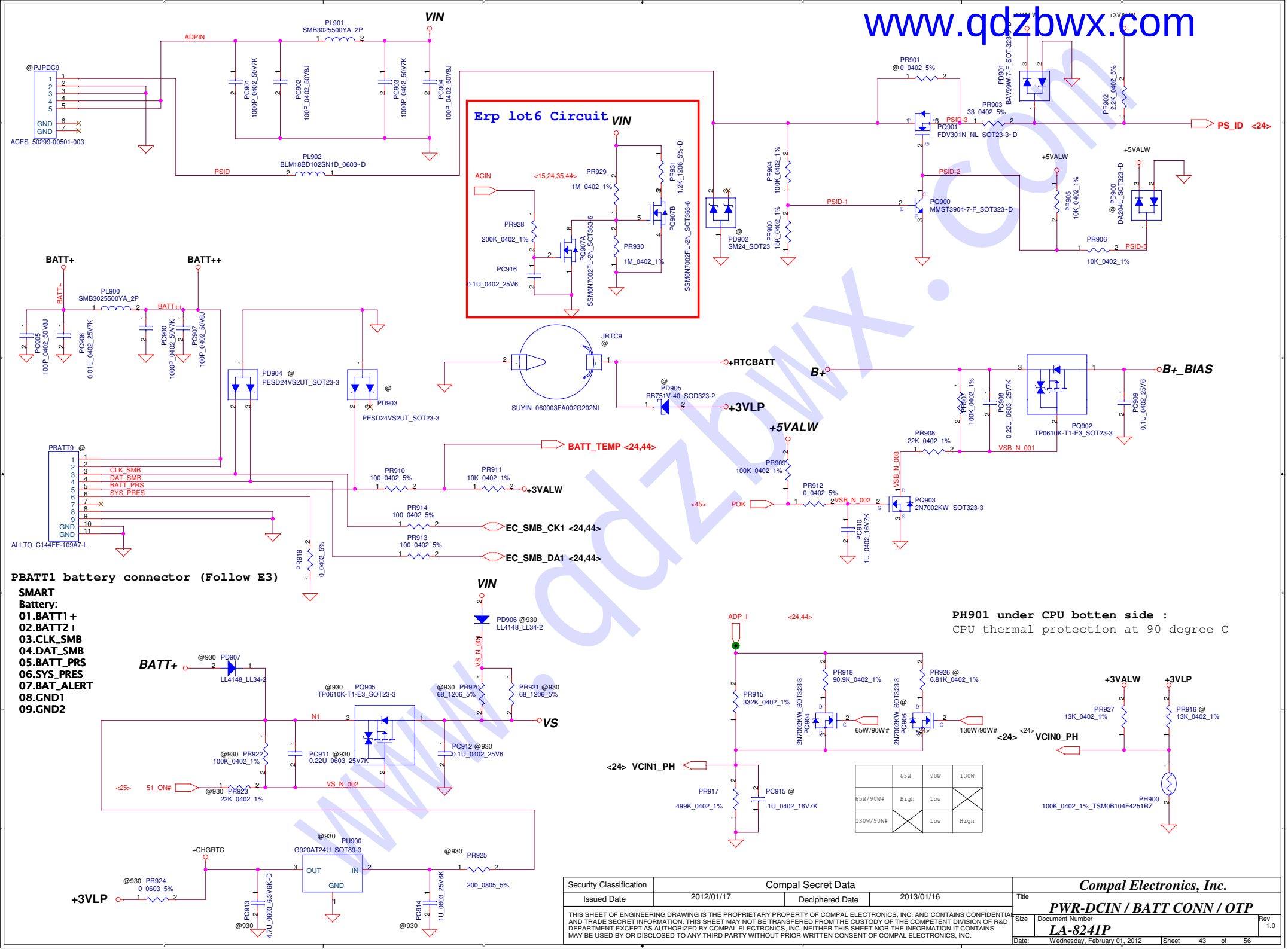
Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	08,11,12	DIMM	11/07/28	COMPAL	The M3 traces are routed to the Sandy Bridge Processor reserved pins for DDR3 VREF	Intel CHKLST Rev1.5 required	0.1
2	18,19	PCH	11/07/28	COMPAL	VCCDMI, V_PROC_IO change to +VCCP from +1.05VS	Intel CHKLST Rev1.5 required	0.1
3	09,10	CPU	11/07/28	COMPAL	remove decoupling cap for +VCC_CORE, +VCCP, +VCC_GFXCORE_AXG, owner change to PWR	Intel CHKLST Rev1.5 required	0.1
4	10	CPU	11/07/28	COMPAL	VCCSA_SELECT[0:1] which should be connected to VID[1:0] of the System Agent (SA) VR controller.	Intel CHKLST Rev1.5 required	0.1
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/01/17	Deciphered Date 2013/01/16	Title HW-PIR
			Size / Document Number / Rev 1.0
			Date: Wednesday, February 01, 2012 Sheet 42 of 56



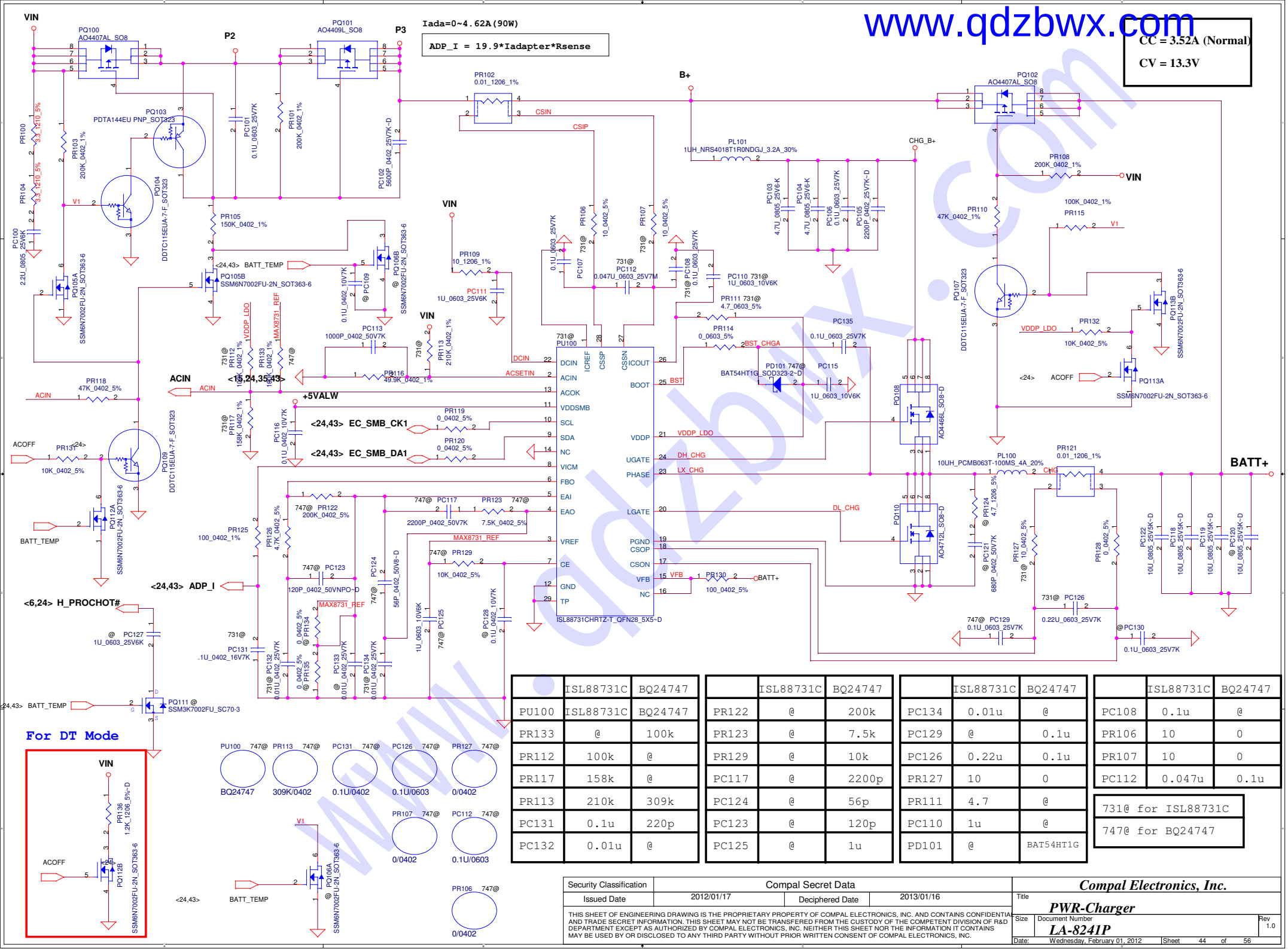
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

Size: | Document Number: LA-8241P | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 43 of 56



	ISL88731C	BQ24747
PU100	ISL88731C	BQ24747
PR133	@	100k
PR112	100k	@
PR117	158k	@
PR113	210k	309k
PC131	0.1u	220p
PC132	0.01u	@

	ISL88731C	BQ24747
PR122	@	200k
PR123	@	7.5k
PR129	@	10k
PC117	@	2200p
PC124	@	56p
PC123	@	120p
PC125	@	1u

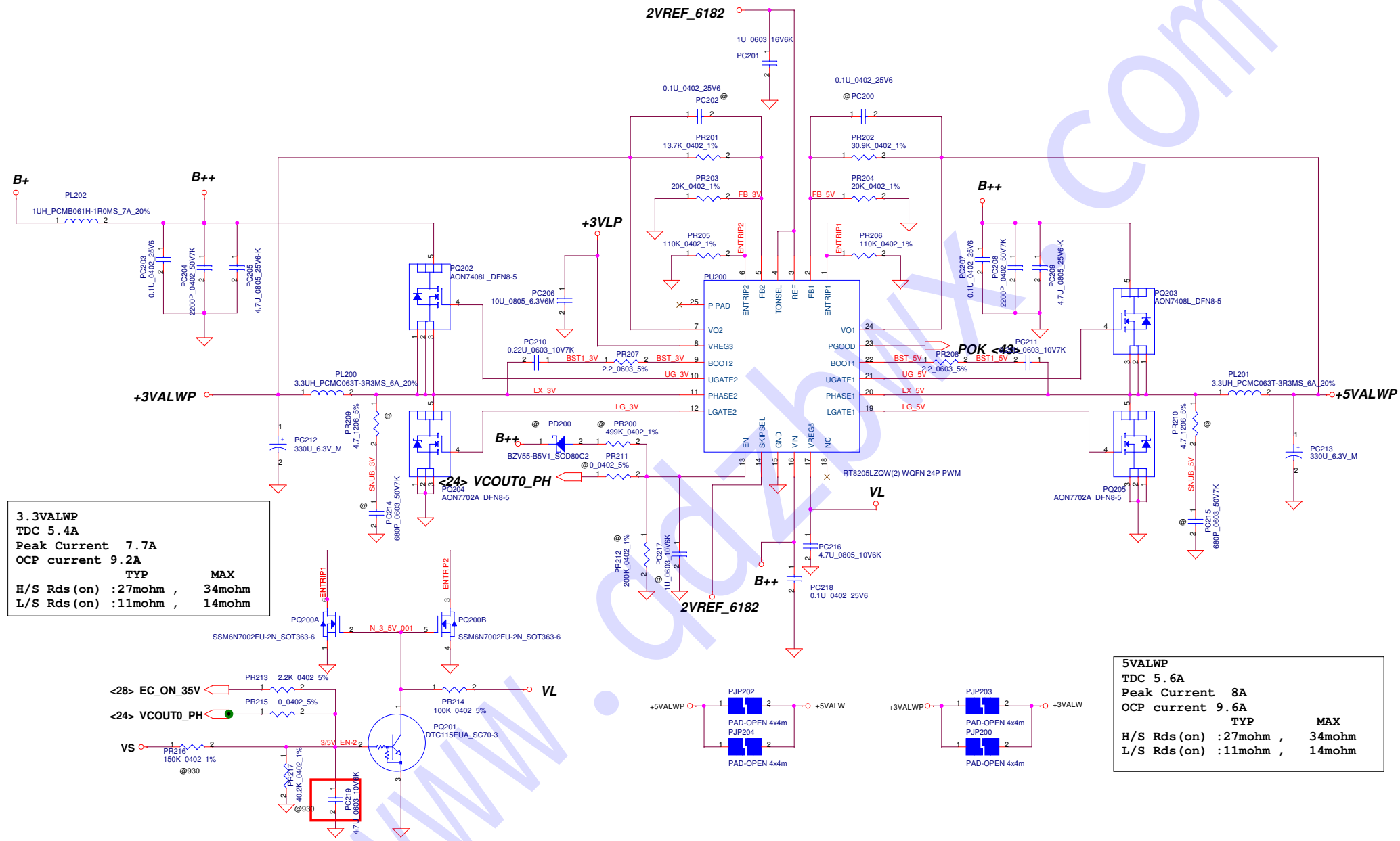
	ISL88731C	BQ24747
PC134	0.01u	@
PC129	@	0.1u
PC126	0.22u	0.1u
PR127	10	0
PR111	4.7	@
PC110	1u	@
PD101	@	BAT54HT1G

	ISL88731C	BQ24747
PC108	0.1u	@
PR106	10	0
PR107	10	0
PC112	0.047u	0.1u

731@ for ISL88731C
747@ for BQ24747

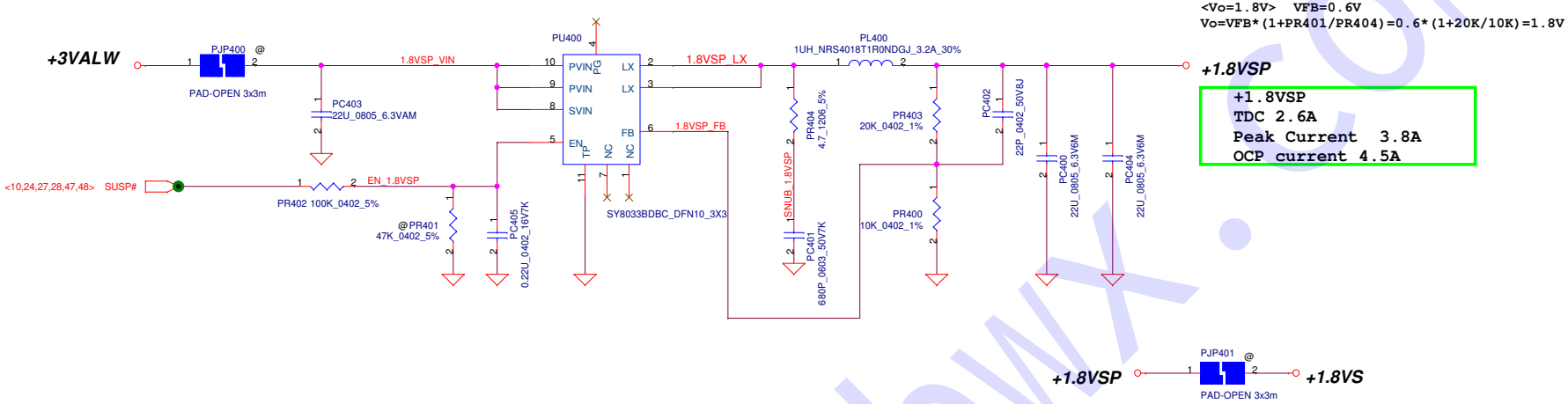
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title: PWR-Charger			
Size	Document Number: LA-8241P		Rev: 1.0
Date: Wednesday, February 01, 2012		Sheet 44 of 56	



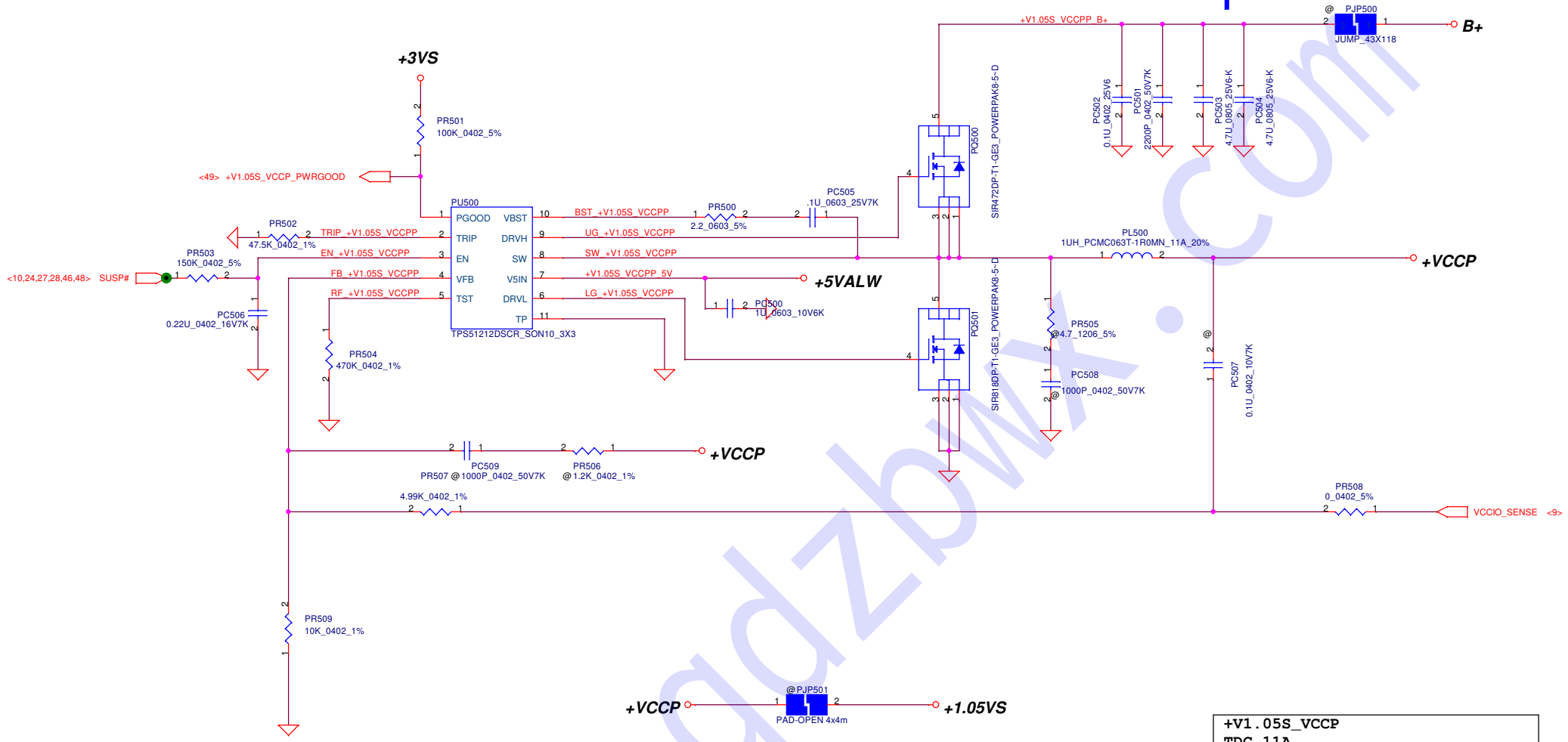
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	PWR-3VALWP/5VALWP		
Size	Document Number	LA-8241P	Rev 1.0
Date:	Wednesday, February 01, 2012	Sheet	45 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	PWR-1.8VSP		
Size	Document Number	LA-8241P	Rev 1.0
Date:	Wednesday, February 01, 2012	Sheet 46 of 56	



+V1.05S_VCCP		
TDC 11A		
Peak Current 16A		
OCP current 19A		
	TYP	MAX
H/S Rds(on)	10mohm ,	14.5mohm
L/S Rds(on)	:3mohm ,	3.6mohm

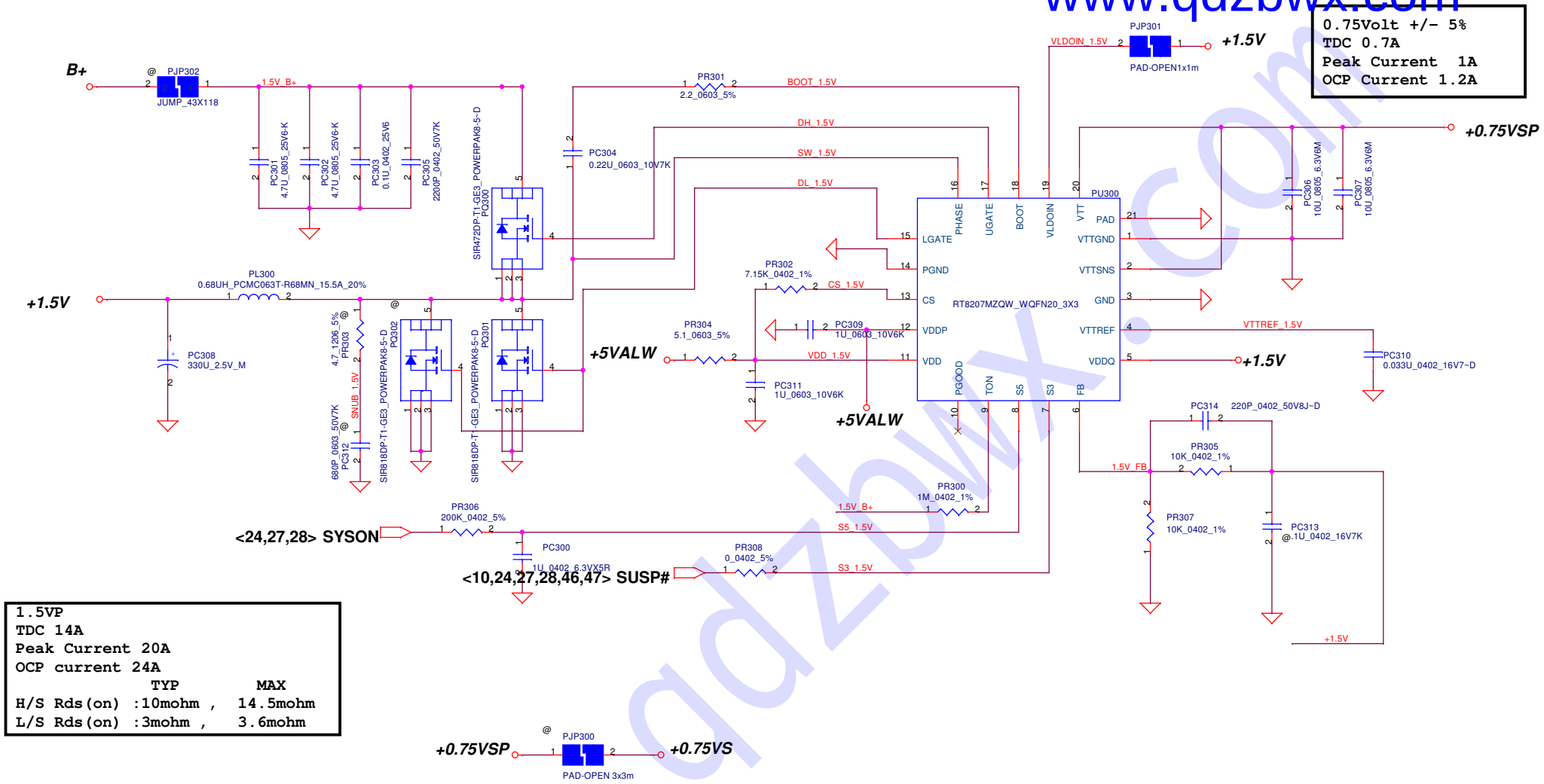
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PWR-V1.05S_VCCPP

Size | Document Number: LA-8241P | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 47 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	PWR-1.5V/0.75VSP		
Size	Document Number		Rev
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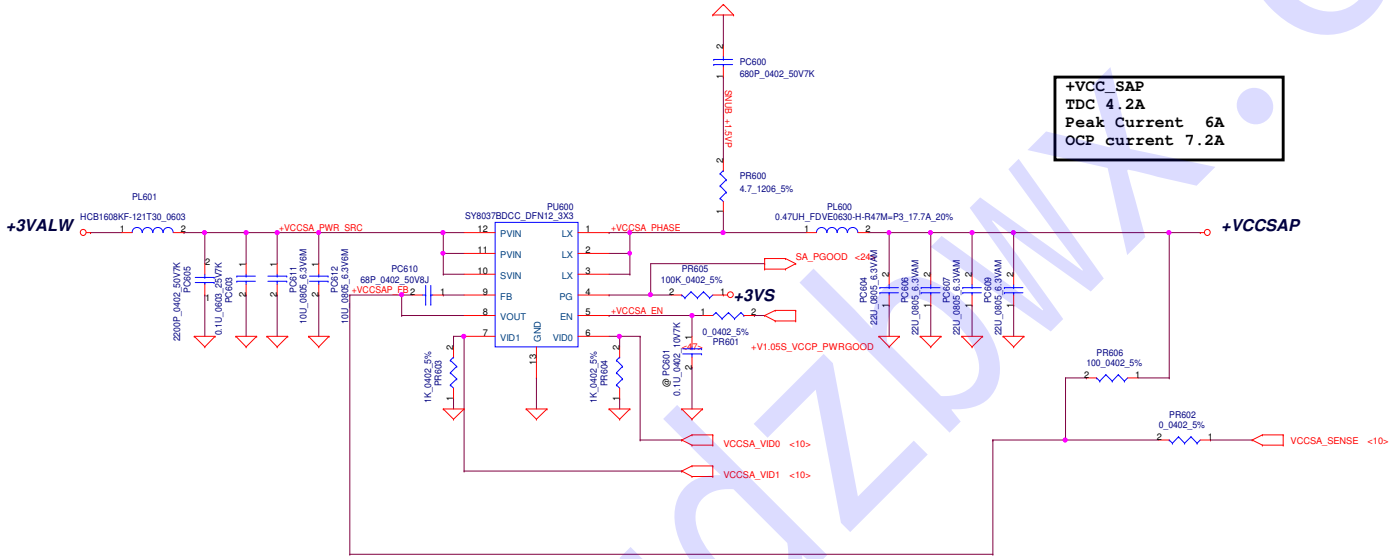
Date:	Wednesday, February 01, 2012	Sheet	48 of 56

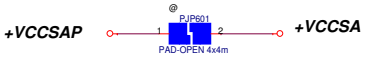
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



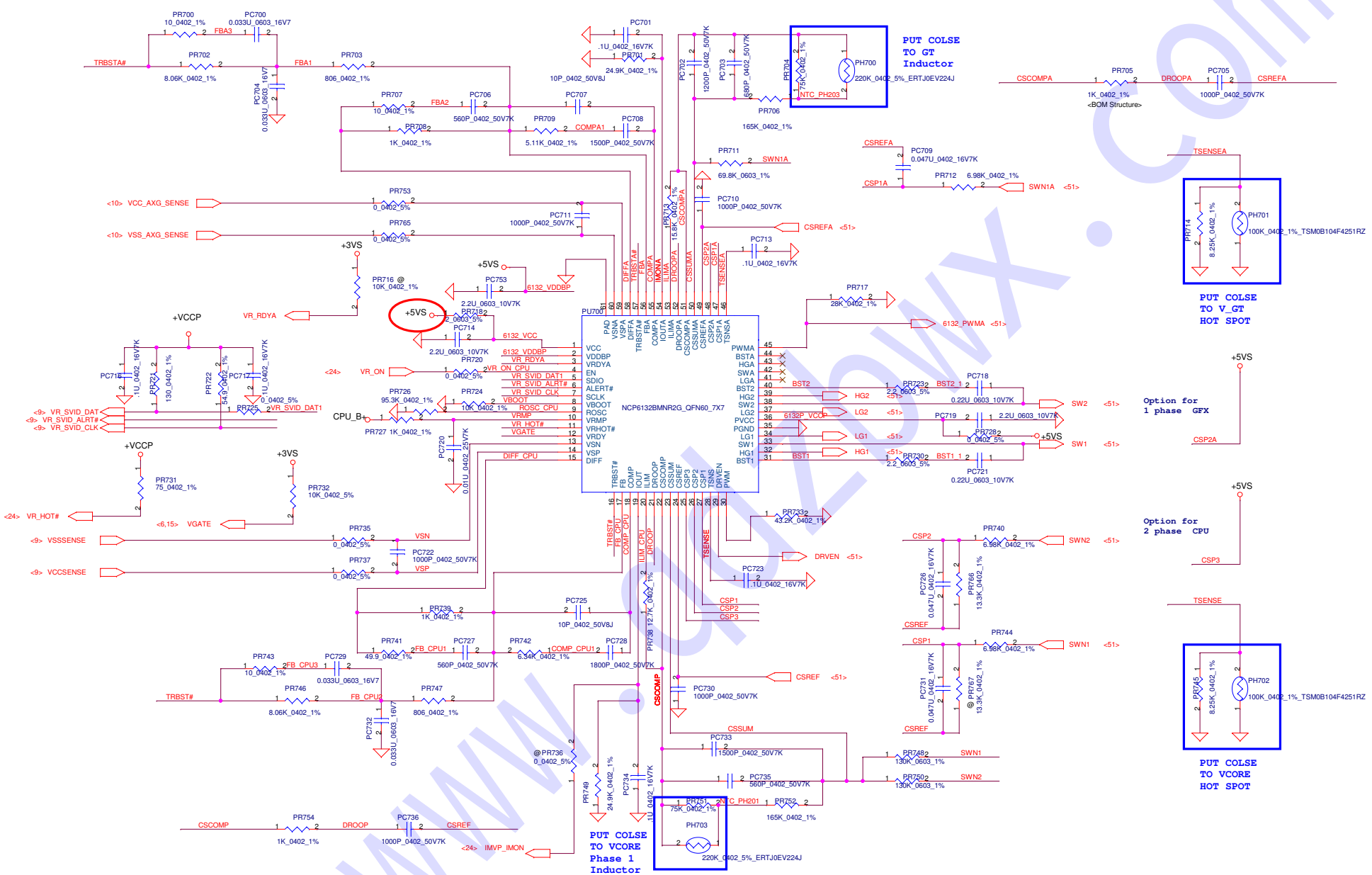
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PWR-VCC_SAP

Size: | Document Number: LA-8241P | Rev: 1.0

Date: Wednesday, February 01, 2012 | Sheet 49 of 56

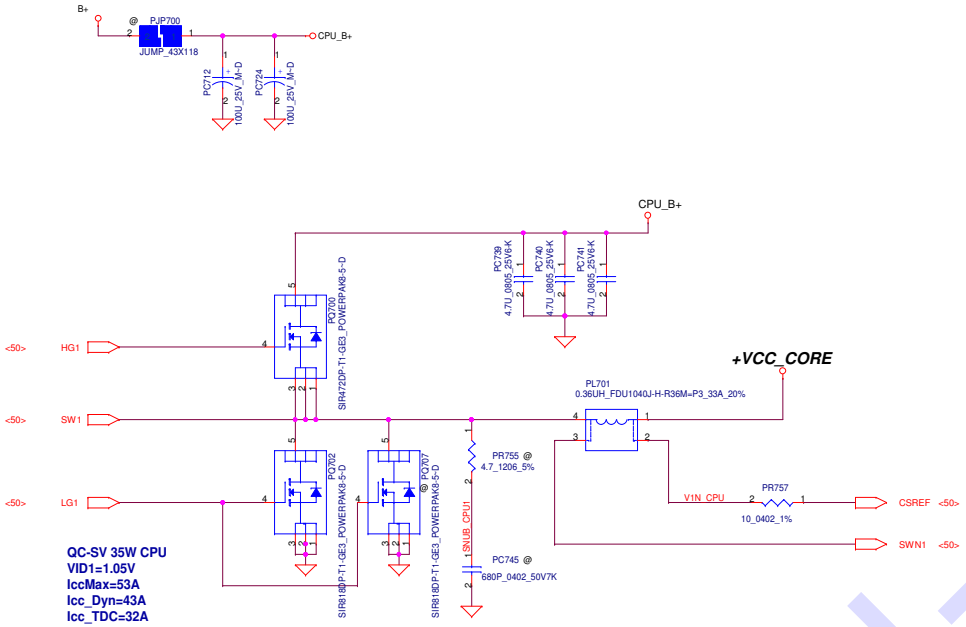


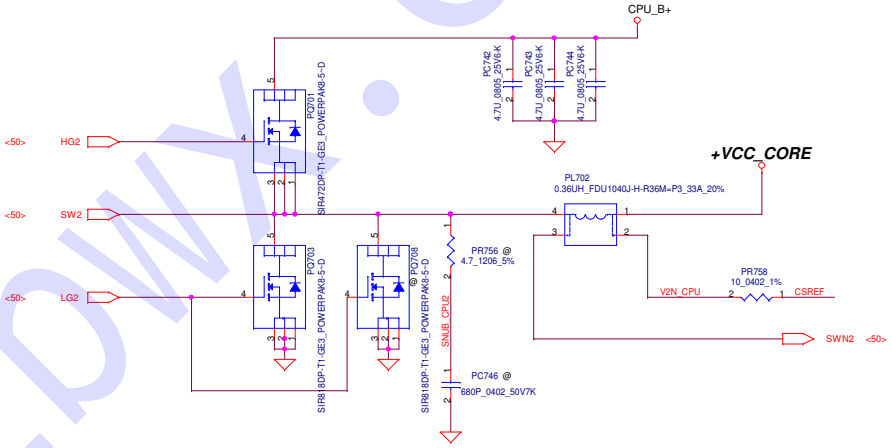
Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title: CPU Core			
Size	Document Number: LA-8241P		Rev: 1.0
Date: Wednesday, February 01, 2012		Sheet 50 of 56	

VCC_core
TDC 32A
Peak Current 53A
OCP current 65
Load line -1.9mV/A
FSW=300kHz
DCR 1.1mohm +/-5%

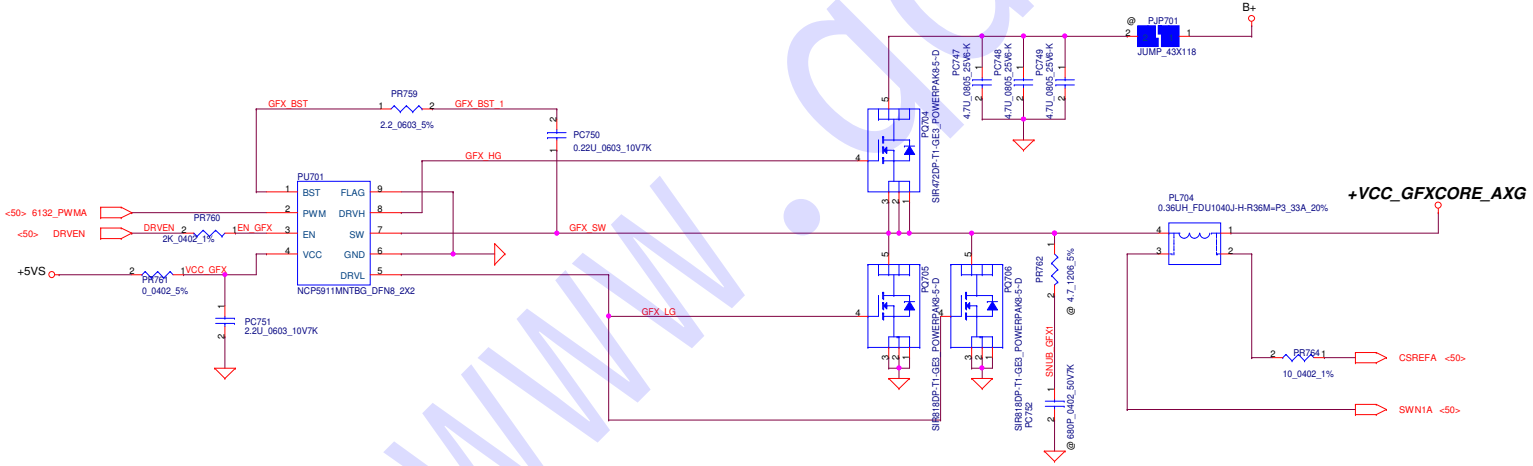
	TYP	MAX
H/S Rds(on)	:10mohm ,	14.5mohm
L/S Rds(on)	:3mohm ,	3.6mohm





+VCC_GFXCORE_AXG
TDC 21.5A
Peak Current 33A
OCP current 40A
Load line -3.9mV/A
FSW=300kHz
DCR 1.1mohm +/-5%

	TYP	MAX
H/S Rds(on)	:10mohm ,	14.5mohm
L/S Rds(on)	:3mohm ,	3.6mohm



Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PWR-VCC_SAP

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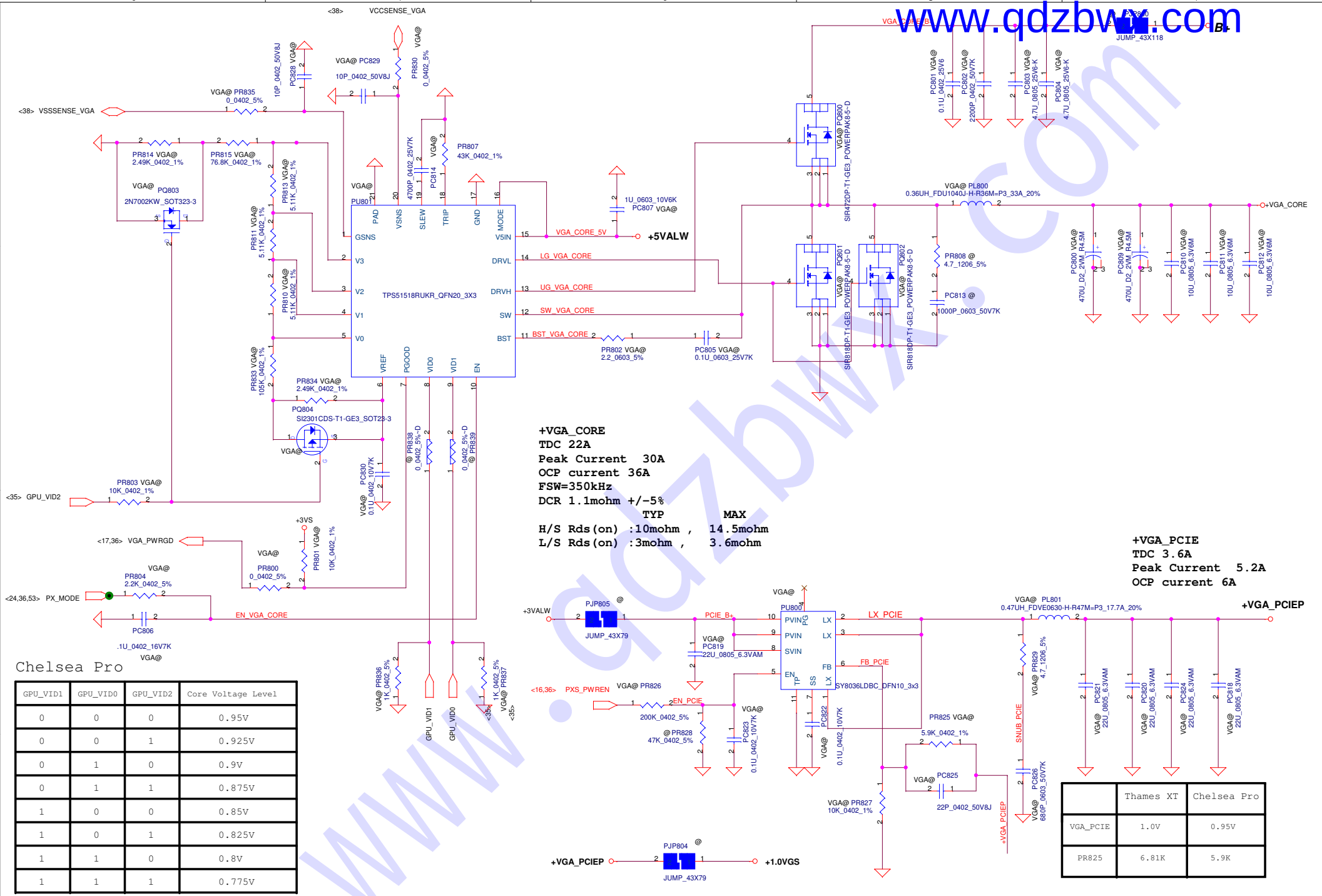

+VGA_CORE
TDC 22A
Peak Current 30A
OCP current 36A
FSW=350kHz
DCR 1.1mohm +/-5%

	TYP	MAX
H/S Rds(on)	:10mohm ,	14.5mohm
L/S Rds(on)	:3mohm ,	3.6mohm

+VGA_PCIE
TDC 3.6A
Peak Current 5.2A
OCP current 6A

Chelsea Pro

GPU_VID1	GPU_VID0	GPU_VID2	Core Voltage Level
0	0	0	0.95V
0	0	1	0.925V
0	1	0	0.9V
0	1	1	0.875V
1	0	0	0.85V
1	0	1	0.825V
1	1	0	0.8V
1	1	1	0.775V

	Thames XT	Chelsea Pro
VGA_PCIE	1.0V	0.95V
PR825	6.81K	5.9K

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.	
Title	VGA_COREP
Size	Document Number: LA-8241P
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Date:	Wednesday, February 01, 2012
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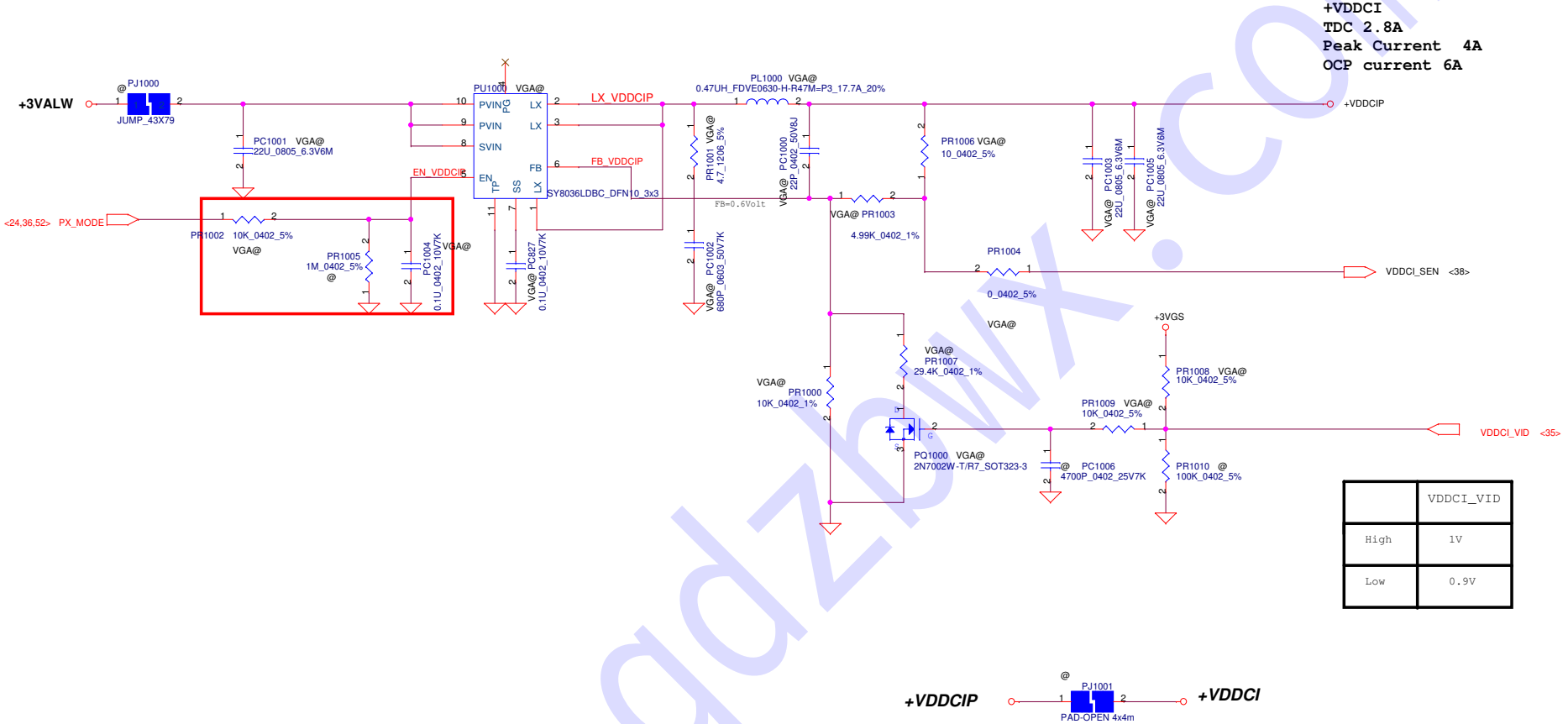

	VDDCI_VID
High	1V
Low	0.9V

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.			
Title	+VDDCIP		
Size	Document Number	LA-8241P	Rev 1.0
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+VCC_CORE

+VCC_CORE

+VCC_GFXCORE_AXG

Follow PDG 4285U_CRB_PDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

+VCC_CORE

PC1201 10U_0805_6.3VAM
PC1202 10U_0805_6.3VAM
PC1203 10U_0805_6.3VAM
PC1204 10U_0805_6.3VAM
PC1205 10U_0805_6.3VAM
PC1206 10U_0805_6.3VAM
PC1207 10U_0805_6.3VAM
PC1208 10U_0805_6.3VAM
PC1209 10U_0805_6.3VAM
PC1210 10U_0805_6.3VAM

+VCC_CORE

PC1219 22U_0805_6.3V6M
PC1220 22U_0805_6.3V6M
PC1221 22U_0805_6.3V6M
PC1222 22U_0805_6.3V6M
PC1223 22U_0805_6.3V6M
PC1238 22U_0805_6.3V6M
PC1239 22U_0805_6.3V6M
PC1240 22U_0805_6.3V6M
PC1241 22U_0805_6.3V6M
PC1242 22U_0805_6.3V6M
PC1249 22U_0805_6.3V6M
PC1250 22U_0805_6.3V6M
PC1251 22U_0805_6.3V6M
PC1252 22U_0805_6.3V6M
PC1253 22U_0805_6.3V6M
PC1256 22U_0805_6.3V6M

+VCC_CORE

PC1257 330U_D2_2VM_R9M
PC1258 330U_D2_2V_Y
PC1259 330U_D2_2VM_R9M
PC1260 330U_D2_2V_Y
PC1261 @ 330U_D2_2V_Y
PC1262 @ 330U_D2_2V_Y

+VCC_GFXCORE_AXG

PC1211 22U_0805_6.3V6M
PC1212 22U_0805_6.3V6M
PC1213 22U_0805_6.3V6M
PC1214 22U_0805_6.3V6M
PC1215 22U_0805_6.3V6M
PC1216 22U_0805_6.3V6M
PC1217 22U_0805_6.3V6M
PC1218 22U_0805_6.3V6M
PC1234 22U_0805_6.3V6M
PC1235 22U_0805_6.3V6M
PC1236 22U_0805_6.3V6M
PC1237 22U_0805_6.3V6M
PC1246 330U_D2_2V_Y
PC1247 330U_D2_2V_Y

+VCCP

+VCCP
PC1224 22U_0805_6.3V6M
PC1225 22U_0805_6.3V6M
PC1226 22U_0805_6.3V6M
PC1227 22U_0805_6.3V6M
PC1228 22U_0805_6.3V6M
PC1229 22U_0805_6.3V6M
PC1230 22U_0805_6.3V6M
PC1231 22U_0805_6.3V6M
PC1232 22U_0805_6.3V6M
PC1233 22U_0805_6.3V6M
PC1243 22U_0805_6.3V6M
PC1244 22U_0805_6.3V6M
PC1245 22U_0805_6.3V6M
PC1200 330U_D2_2VM_R9M
PC1254 330U_D2_2VM_R9M
PC1255 330U_D2_2VM_R9M

Security Classification	Compal Secret Data		
Issued Date	2012/01/17	Deciphered Date	2013/01/16

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

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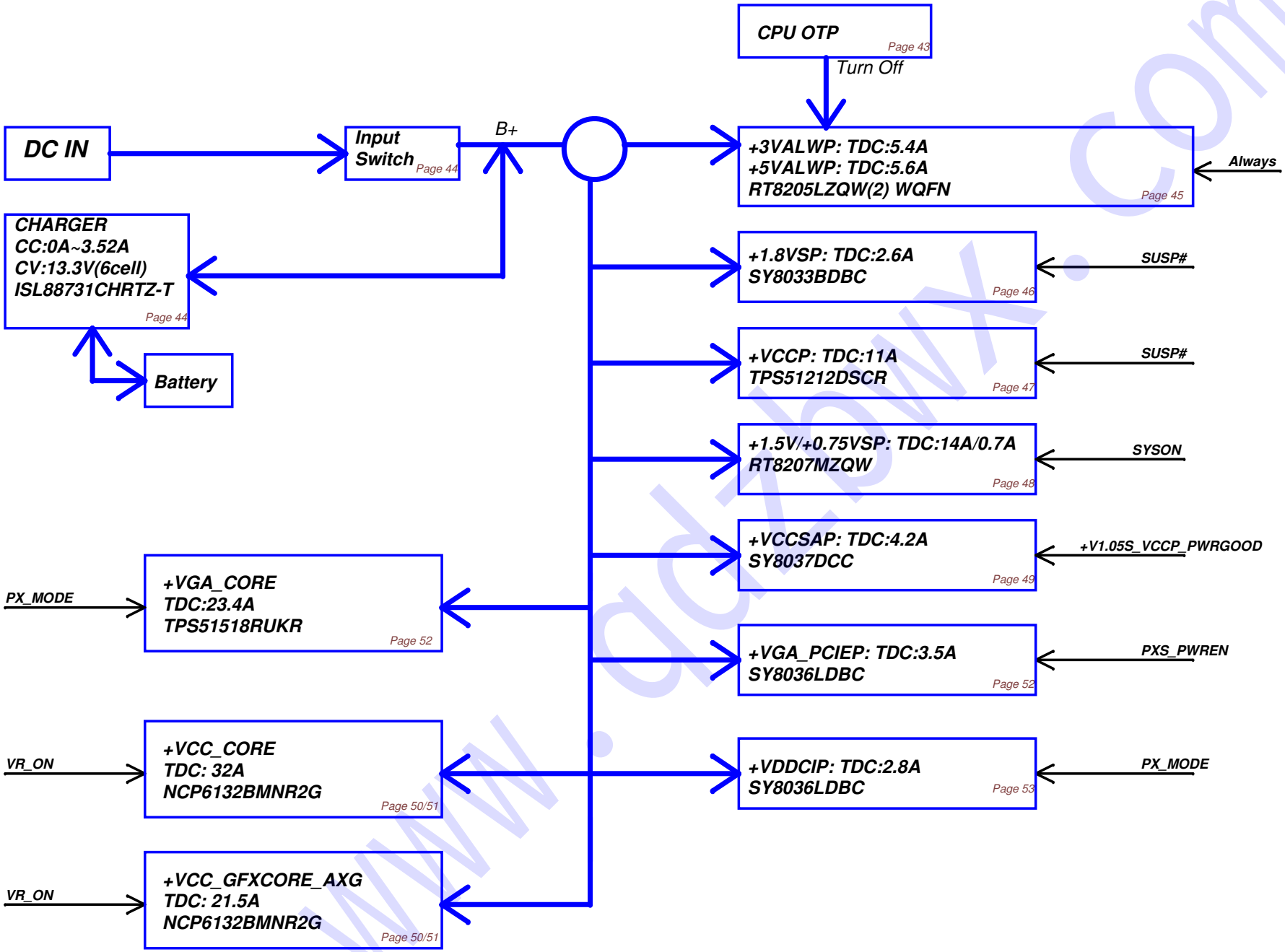
Power block



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/1/17	Deciphered Date 2013/1/16	Title: PROCESSOR DECOUPLING

Size: B2B	Document Number: LA-8241P		Rev: 0.2
Date: Wednesday, February 01, 2012	Sheet 55 of 56		

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	Charger.	11/12/08	Frank	Change PR113 for temperature and voltage test.	Change PR113 from 316k to 309k for Charger IC BQ24747RHDR. Remove PR132.	X00
2	45	3.3VALWP/5VALWP	11/12/08	Frank	Design change.	Change PC219 from 1uF to 4.7uF.	X00
3	53	+VDDCIP	11/12/08	Frank	Fine tune time sequence.	Change PR1002 from 100k to 0ohm. Remove PR1005 and PC1004.	X00

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/01/17	Deciphered Date 2013/01/16	Title PWR-PIR
			Size Document Number LA-8241P Rev 1.0
			Date: Wednesday, February 01, 2012 Sheet 56 of 56