

# COMPAL CONFIDENTIAL

MODEL NAME : *QAM00*

PCB NO : *LA-7731P*

BOM P/N : *4319ET31L01*

GPIO MAP:

## Dalmore 12 UMA

*Ivy Bridge + Panther POINT*

**2011-8-30**

**REV : 0.3 (X01)**

**@ : Nopop Component**

**CONN@ : Connector Component**

MB Type	BOM P/N	
M/B SPI ROM		5@
TAA SPI ROM		6@
SATA re-driver with CD function		7@
Normal E-SATA re-driver		8@

#### MB PCB

Part Number	Description
DA6000P700	PCB OFH LA-7731P REV0 M/B UMA

#### @HDMI Royalty

Part Number	Description
RO000002HM	HDMI Royalty

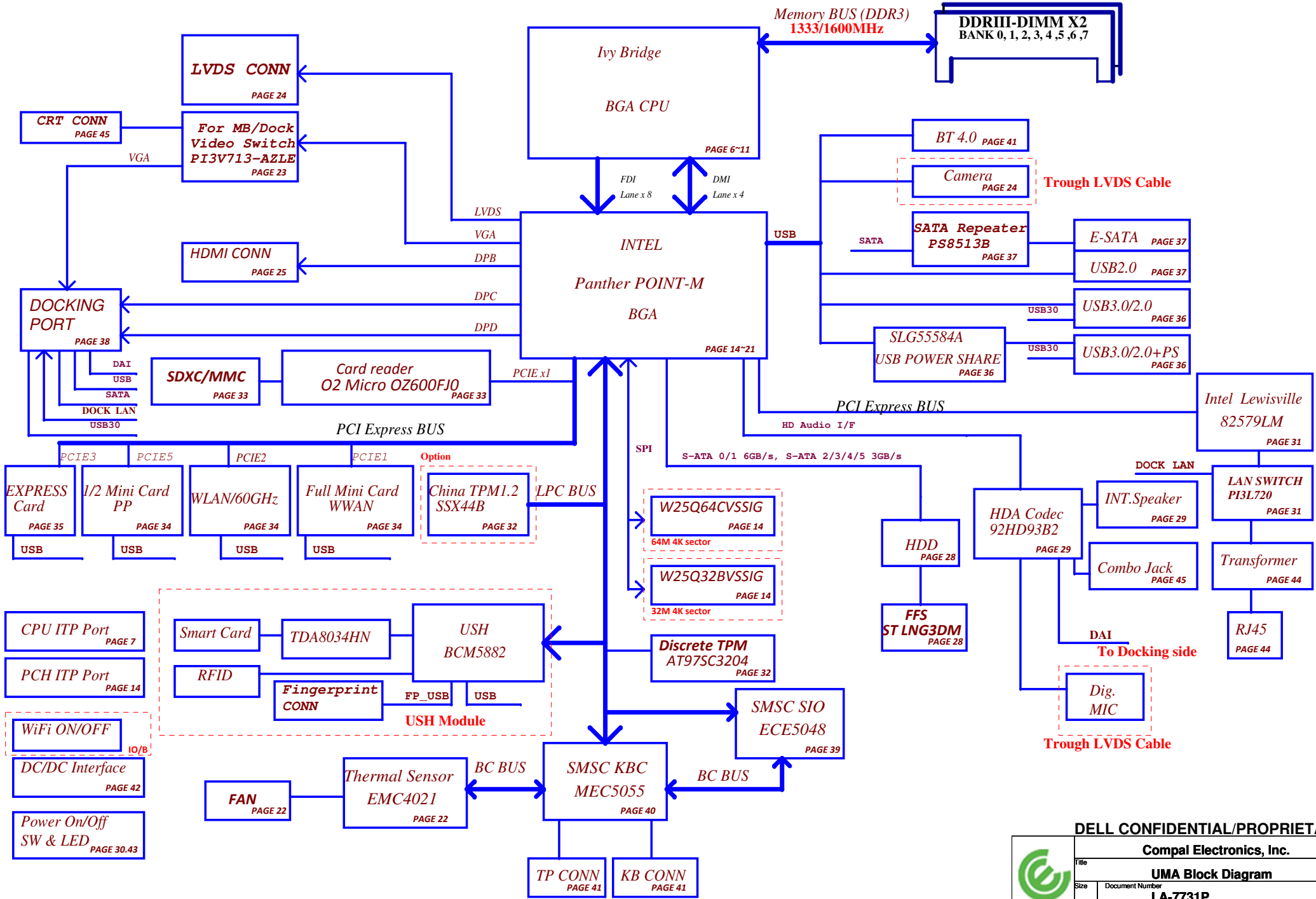
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Title	Cover Sheet		
Size	Document Number	Rev	
	<b>LA-7731P</b>	<b>0.3</b>	
Date:	Thursday, September 01, 2011	Sheet	1 of 99

# Block Diagram



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Title	<b>UMA Block Diagram</b>	
Size	Document Number	Rev
	<b>LA-7731P</b>	0.3
Date	Thursday, September 01, 2011	Sheet 2 of 59

**POWER STATES**

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

**PM TABLE**

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		1.00
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
3	Slg 1		Copper foil	1oz	1.35
		4.7	Prepreg	7628HRC+2116HRCx2+7628HRC	23.80
4	Slg 2		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
5	GND/PWR		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.60
6	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.00
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)				47.6	46.32000

SATA	DESTINATION
SATA 0	HDD
SATA 1	NA
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Right side )
	1	JUSB2 (Bot side)
	2	NA
	3	MLK DOCK
	4	WLAN
	5	WWAN
	6	JMINI3(PP)
	7	USH->BIO
	8	DOCKING
	9	JESATA1 ( Left)
	10	Express card
	11	Bluetooth
	12	Camera
13	NA	

USH	0	BIO
	1	NA

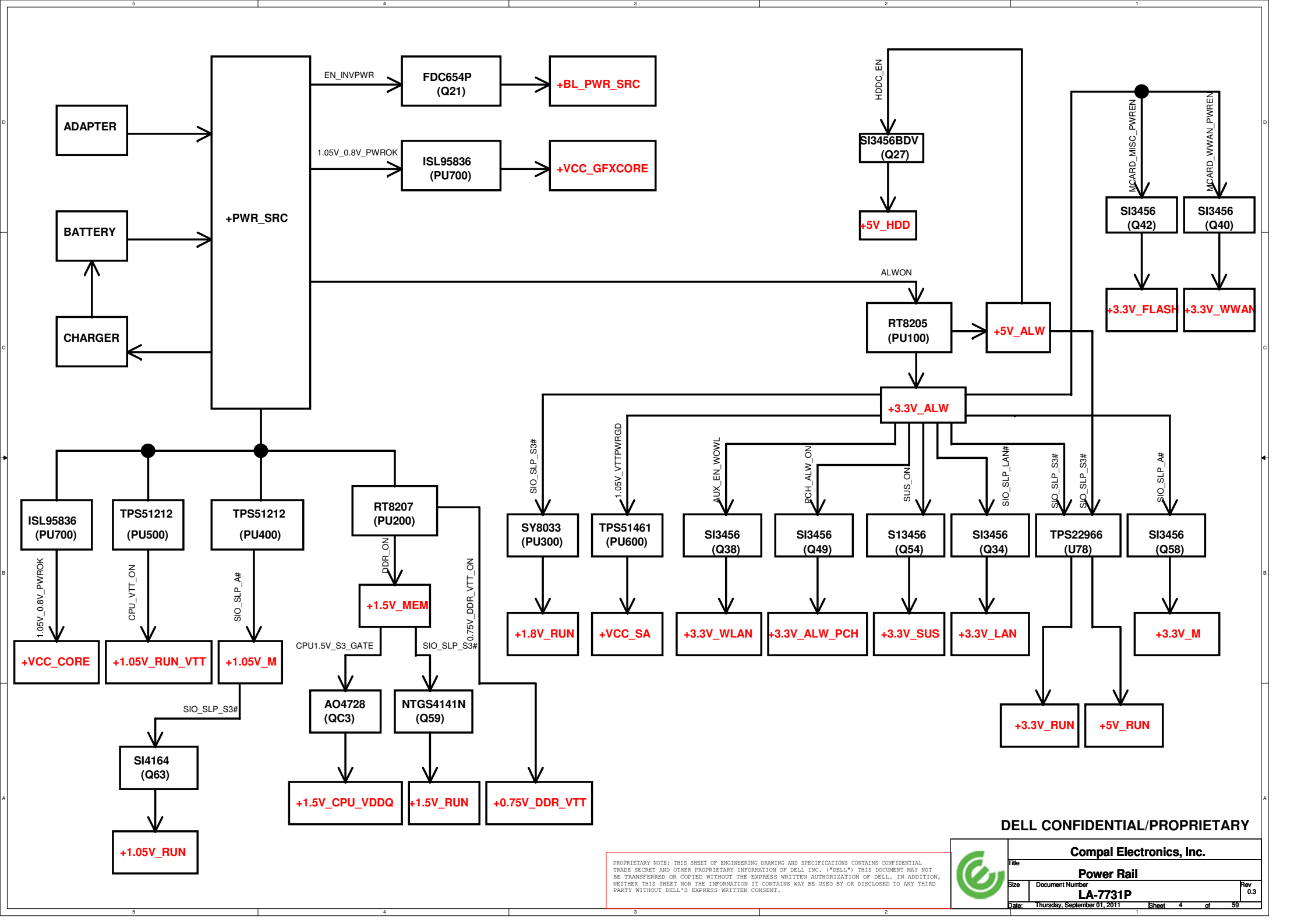
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	None
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

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<b>Index and Config.</b>	
File	Rev 0.3
Size	Document Number
<b>LA-7731P</b>	
Date:	Thursday, September 01, 2011 ESheet 3 of 59

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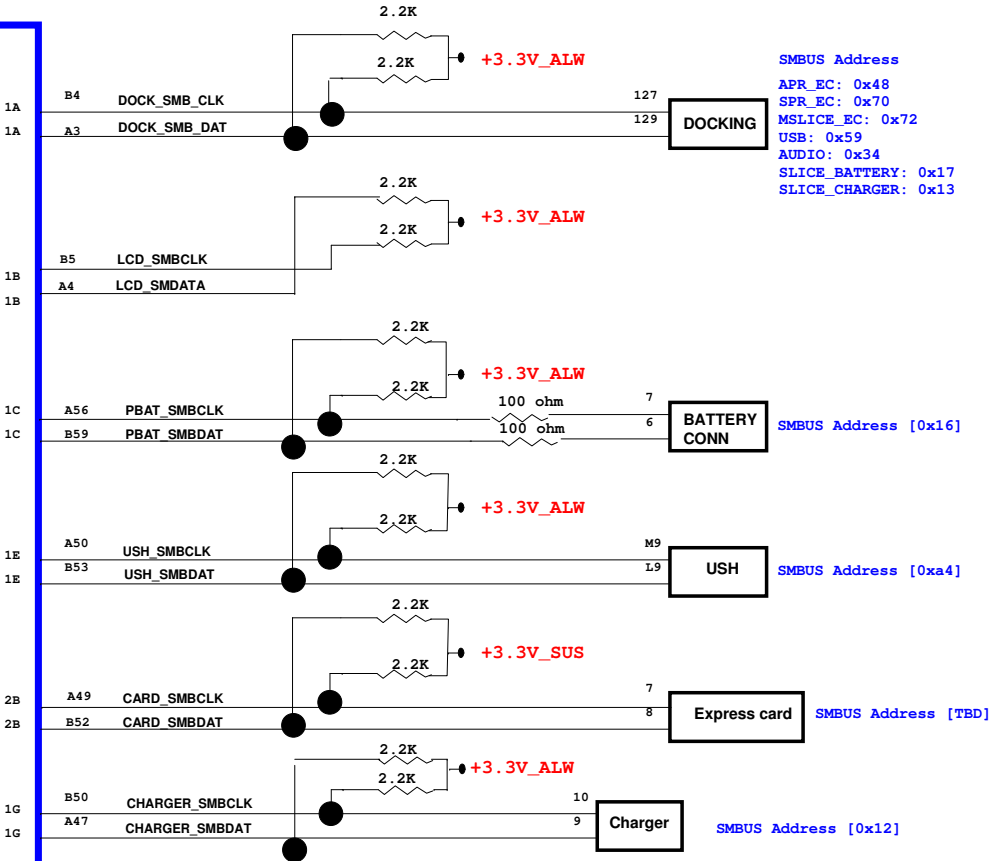
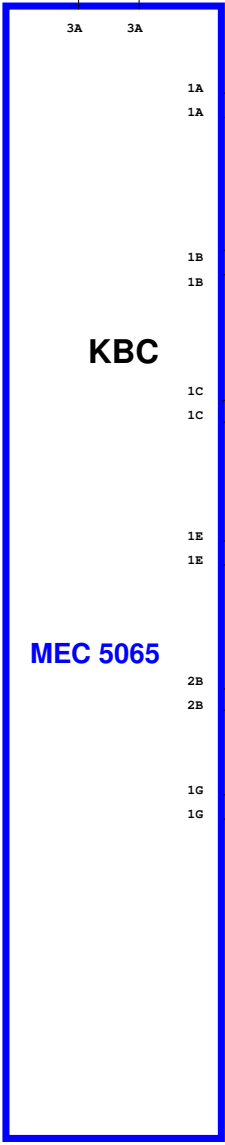
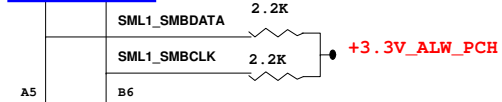
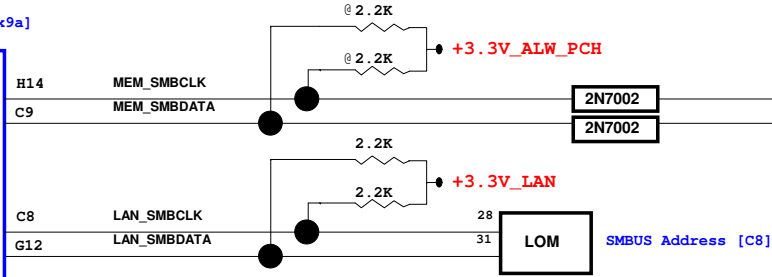
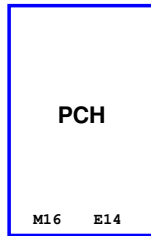
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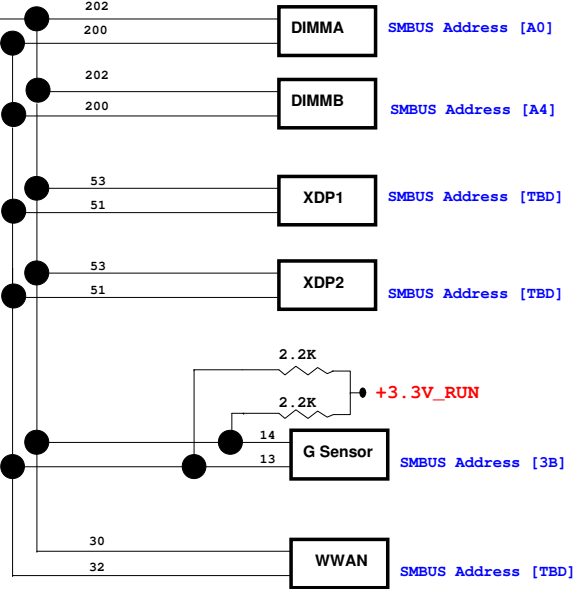
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<b>Power Rail</b>			
File			
Size	Document Number	Rev	
	<b>LA-7731P</b>	0.3	
Date:	Thursday, September 01, 2011	Sheet	4 of 59

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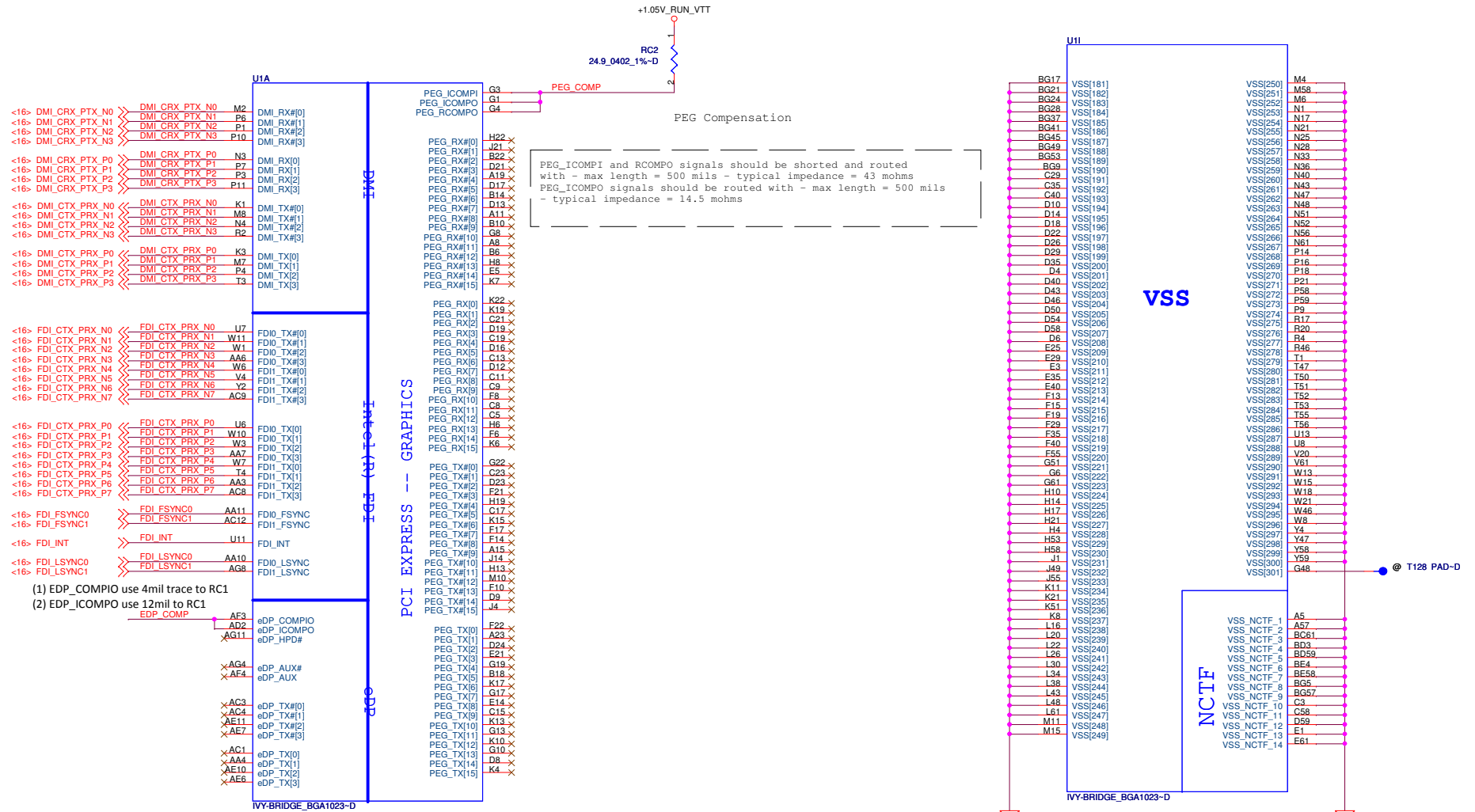
SMBUS Address [0x9a]



SMBUS Address  
 APR\_EC: 0x48  
 SPR\_EC: 0x70  
 MSLICE\_EC: 0x72  
 USB: 0x59  
 AUDIO: 0x34  
 SLICE\_BATTERY: 0x17  
 SLICE\_CHARGER: 0x13

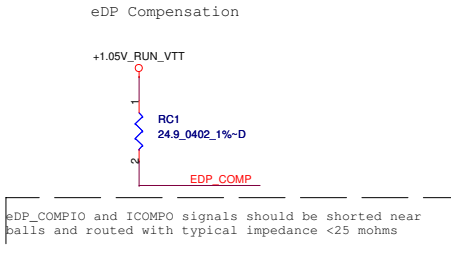
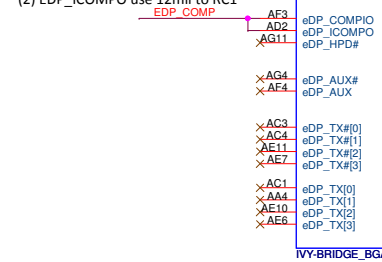


- (1) PEG\_RCOMP0 (G4) use 4mil connect to PEG\_ICOMPI, then use 4mil connect to RC2.
- (2) PEG\_ICOMPO use 12mil connect to RC2.



(1) EDP\_COMPIO use 4mil trace to RC1

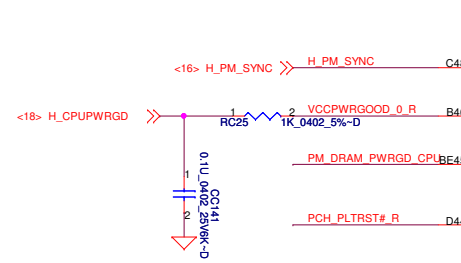
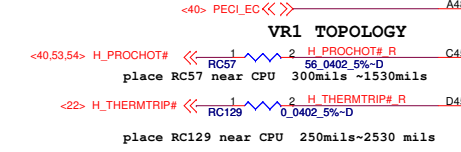
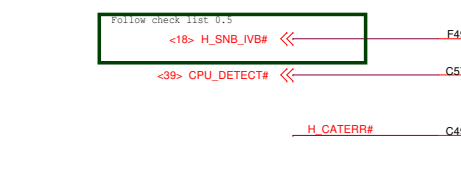
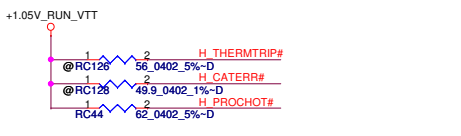
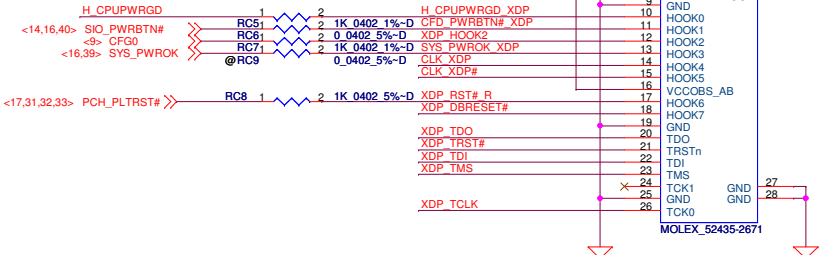
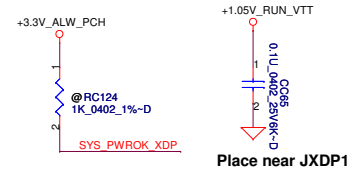
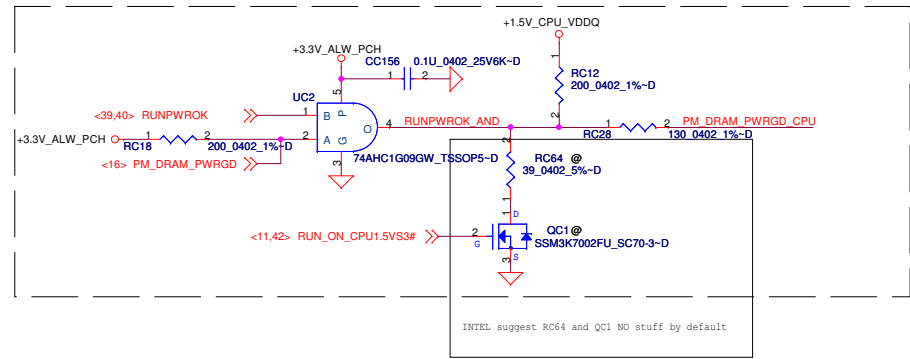
(2) EDP\_ICOMPO use 12mil to RC1



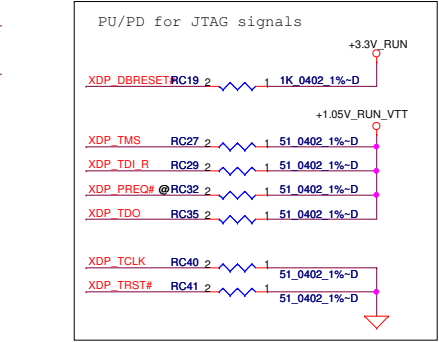
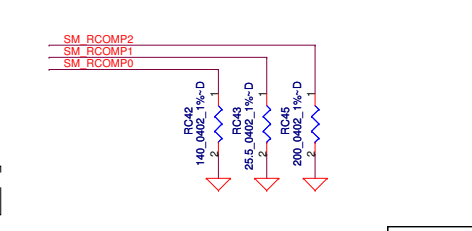
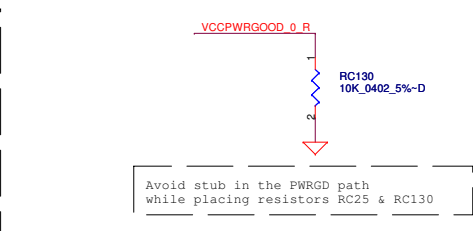
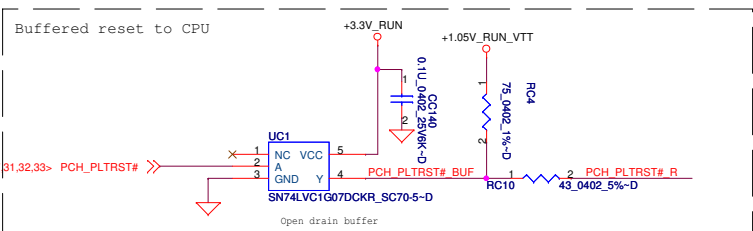
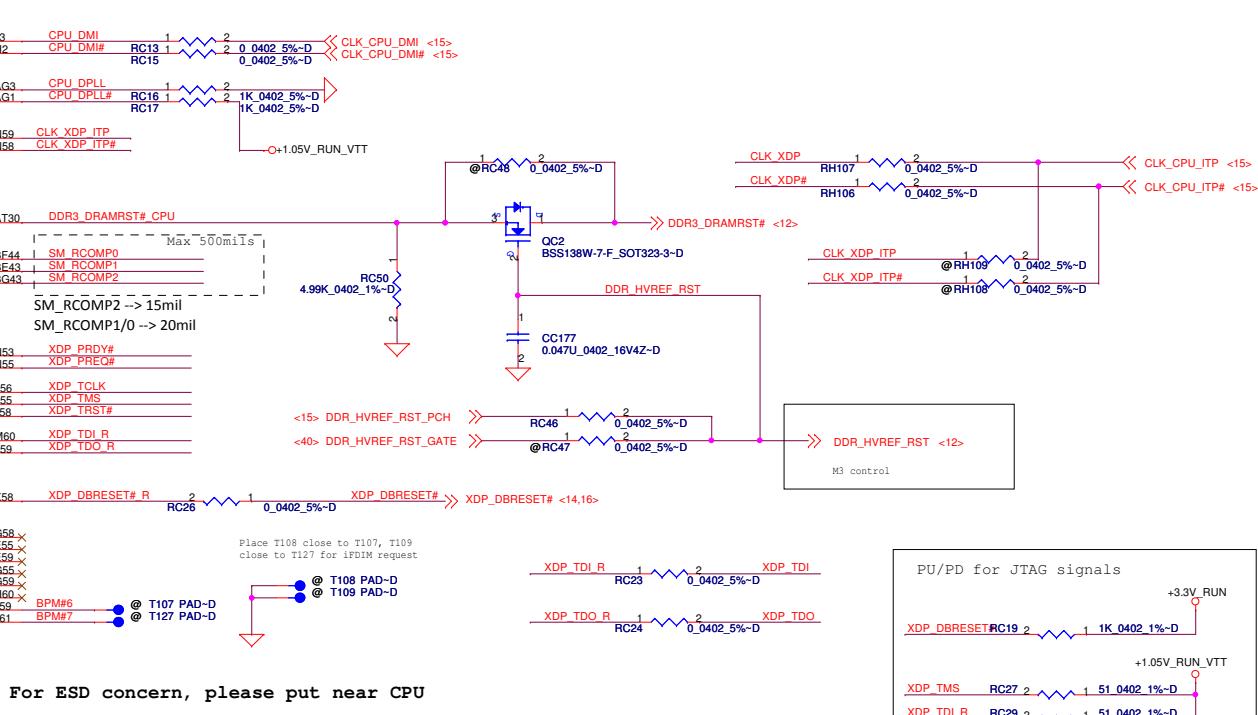
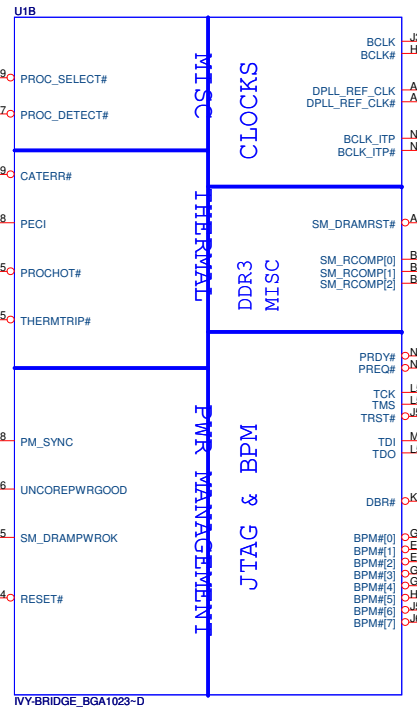
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**Sandy Bridge (1/6)**  
**LA-7731P**  
 Date: Thursday, September 01, 2011 Sheet 6 of 59

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EMI request to reserve CC141



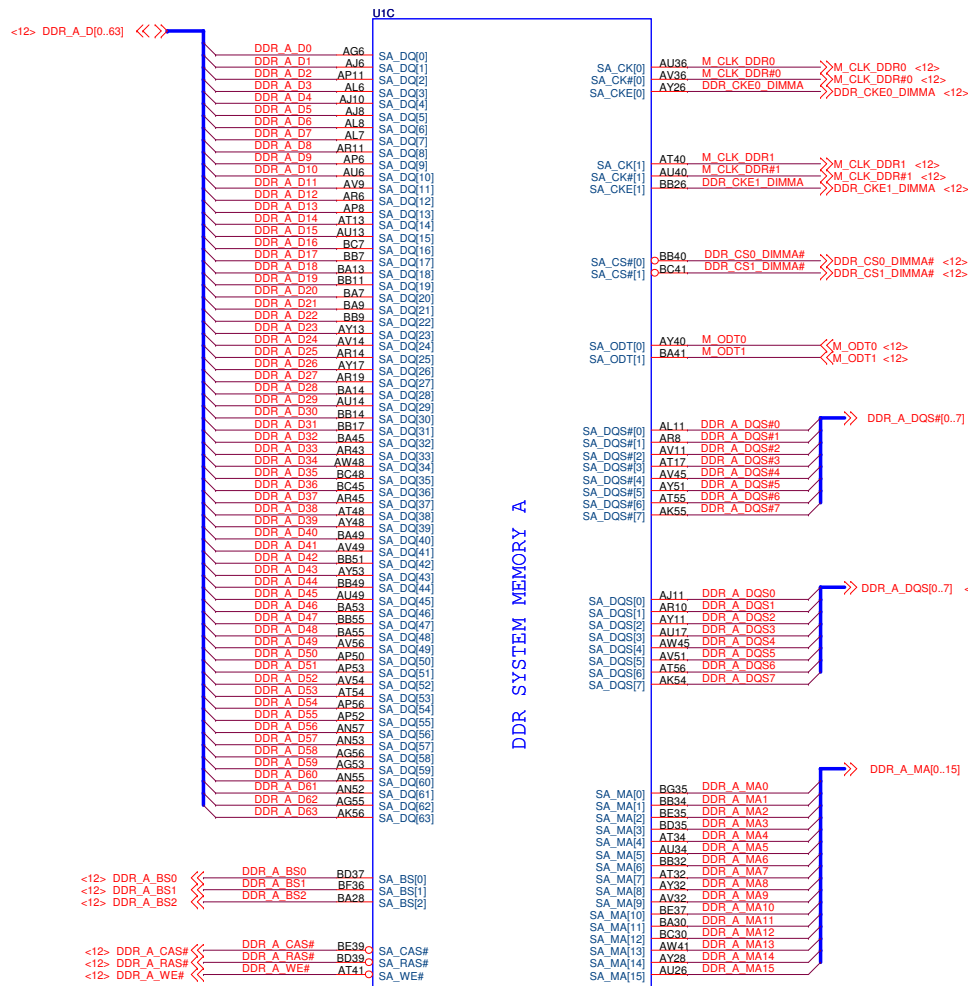
For ESD concern, please put near CPU

Avoid stub in the PWRGD path while placing resistors RC25 & RC130

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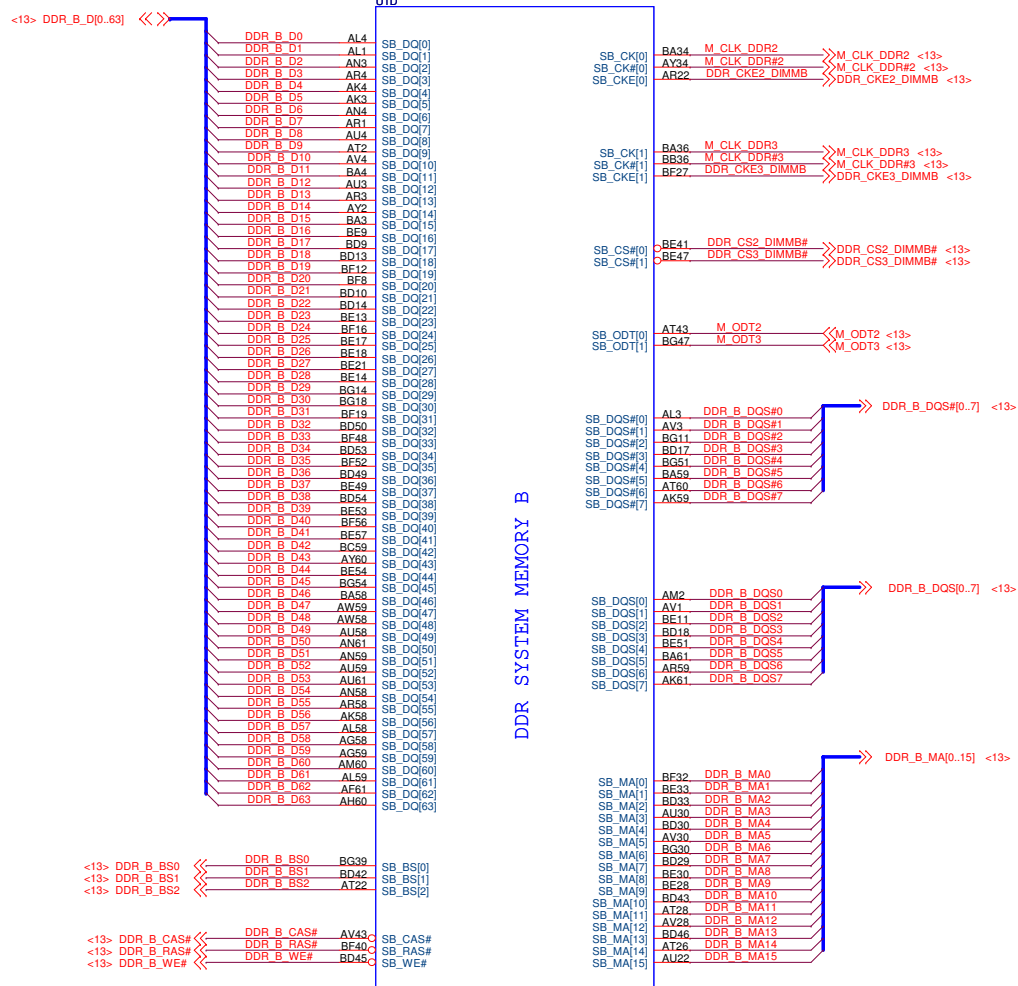
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LA-7731P  
Date: Thursday, September 01, 2011 Sheet 7 of 59

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DDR SYSTEM MEMORY A

IVY-BRIDGE\_BGA1023-D



DDR SYSTEM MEMORY B

IVY-BRIDGE\_BGA1023-D

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Sandy Bridge (3/6)

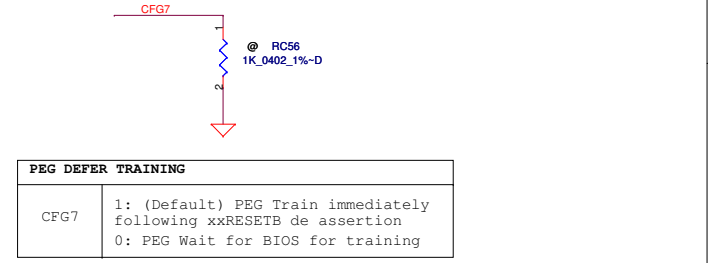
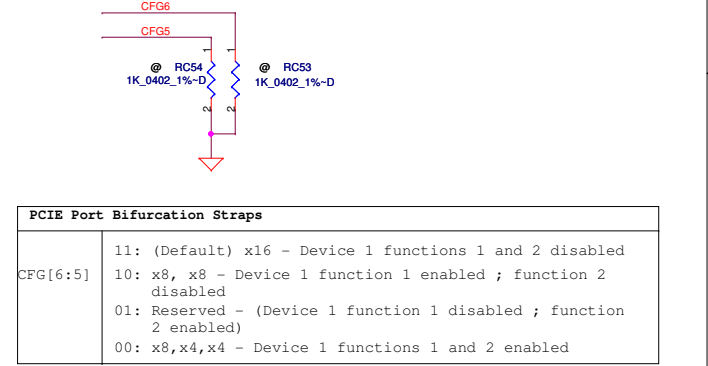
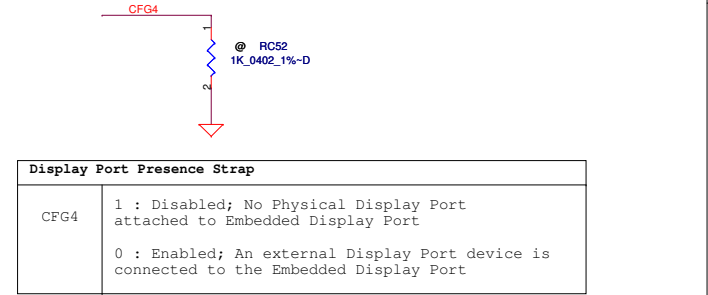
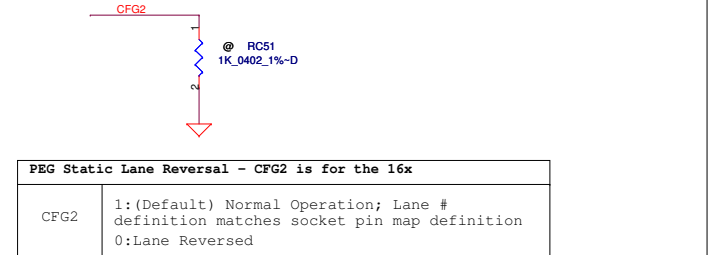
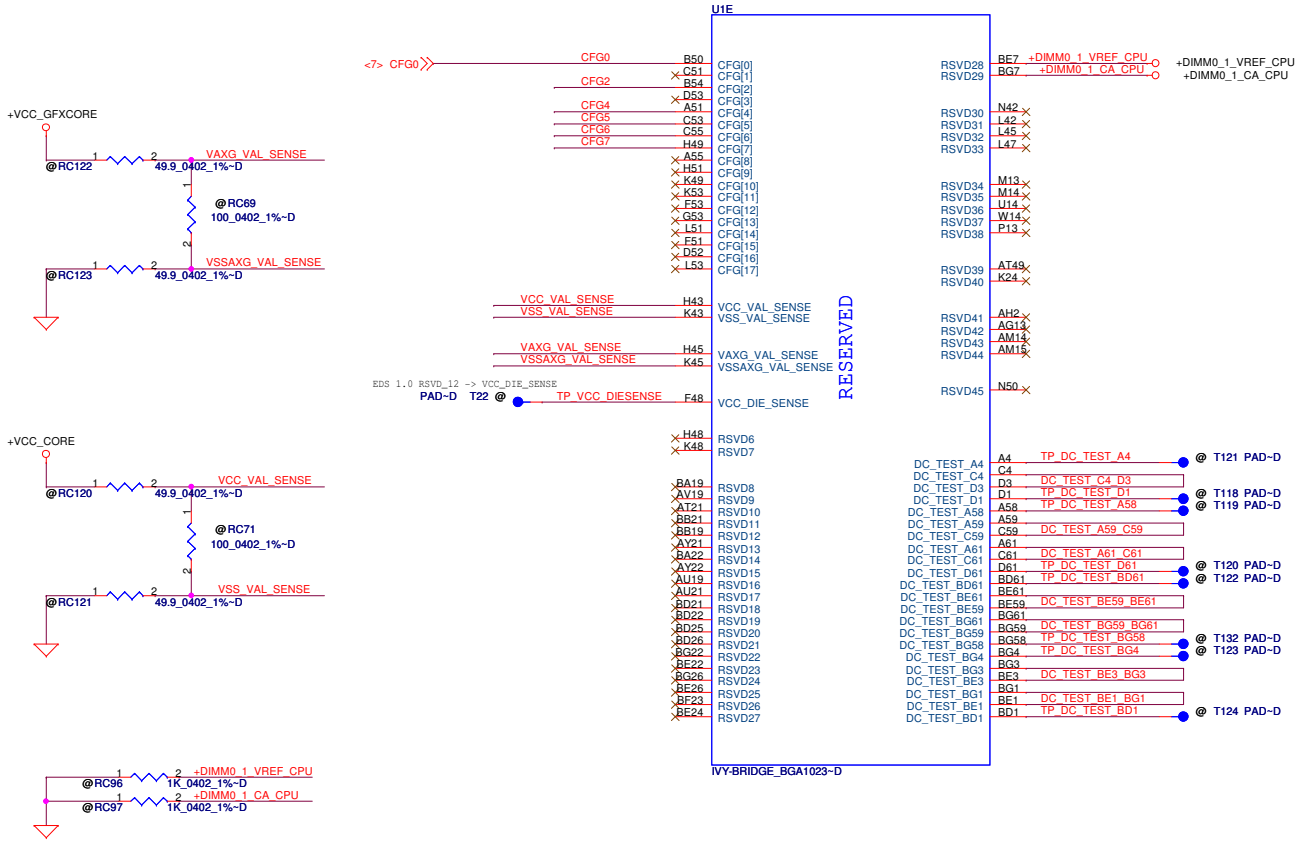
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Title	Sandy Bridge (3/6)		
Size	Document Number	Rev	
	LA-7731P	0.3	
Date	Thursday, September 01, 2011	Sheet	8 of 59





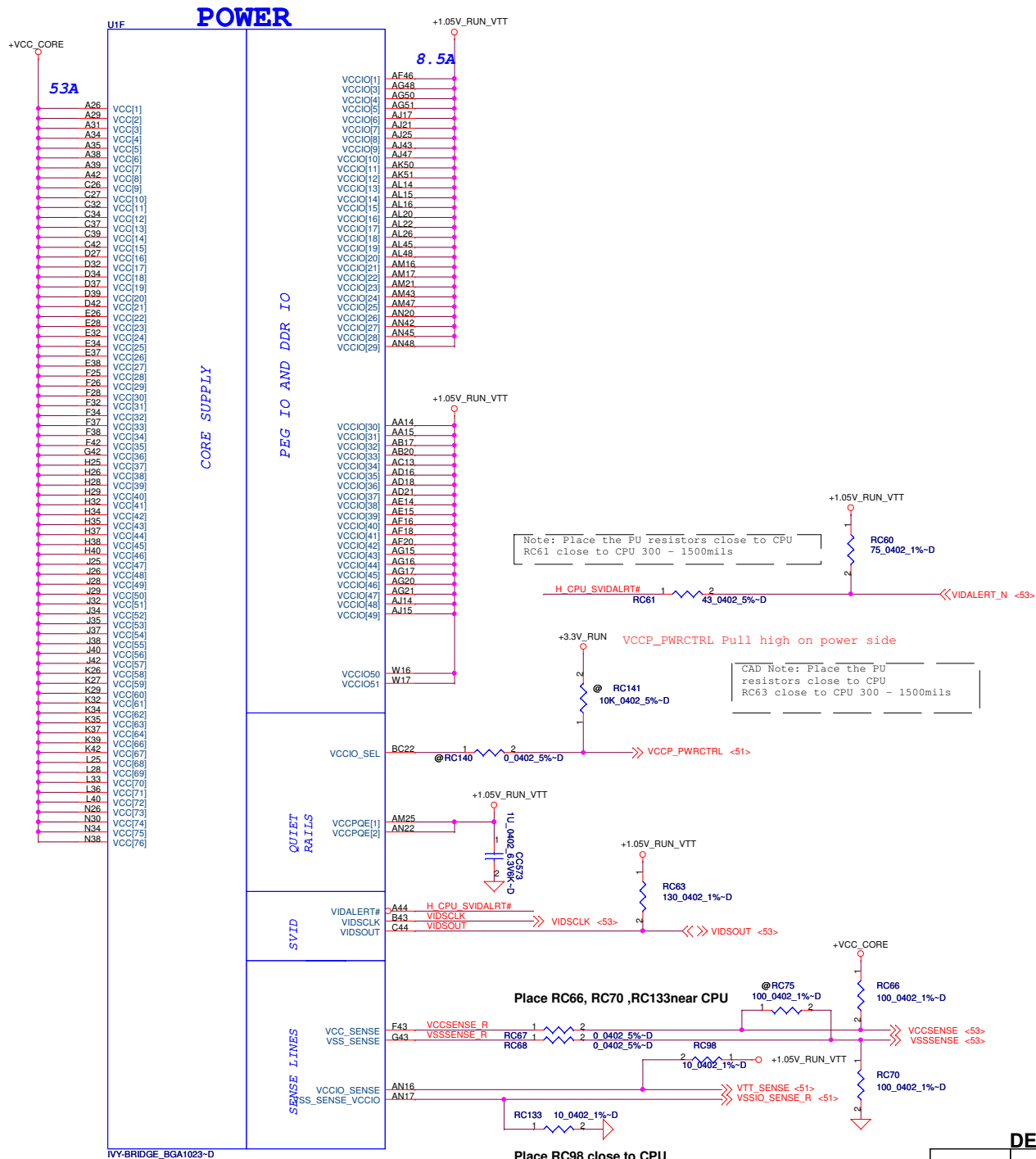
# CFG Straps for Processor



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		<b>Sandy Bridge (4/6)</b>	
Size	Document Number	<b>LA-7731P</b>	
Date:	Thursday, September 01, 2011	Esheet	9 of 59

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Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *

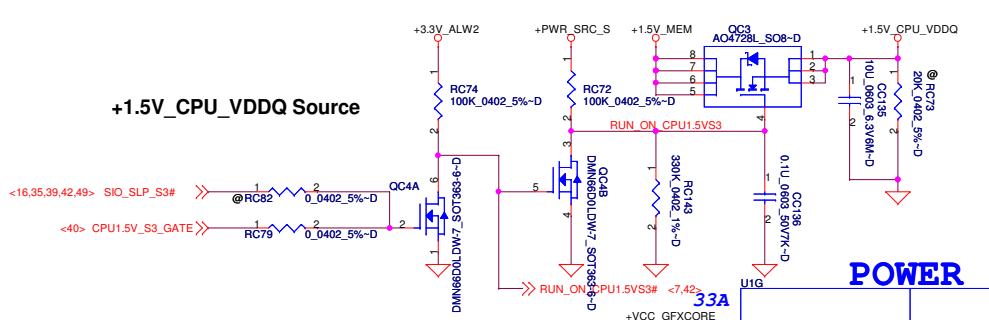
\* Description  
 5A to Mem controller(+1.5V\_CPU\_VDDQ)  
 5-6A to 2 DIMMs/channel  
 2-5A to +1.5V\_RUN & +0.75V\_DDR\_VTT

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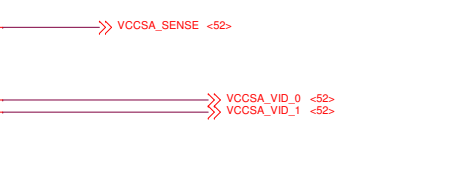
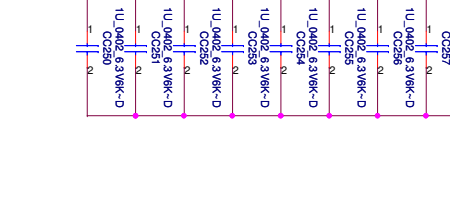
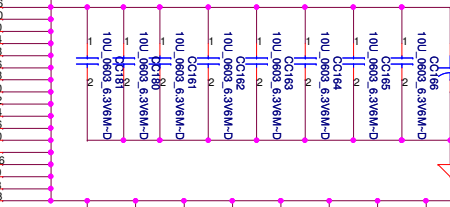
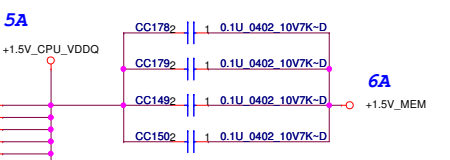
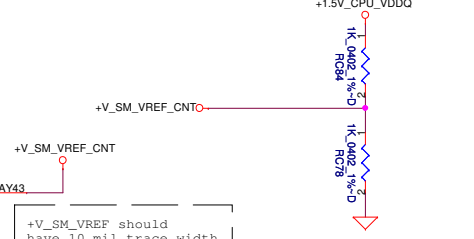
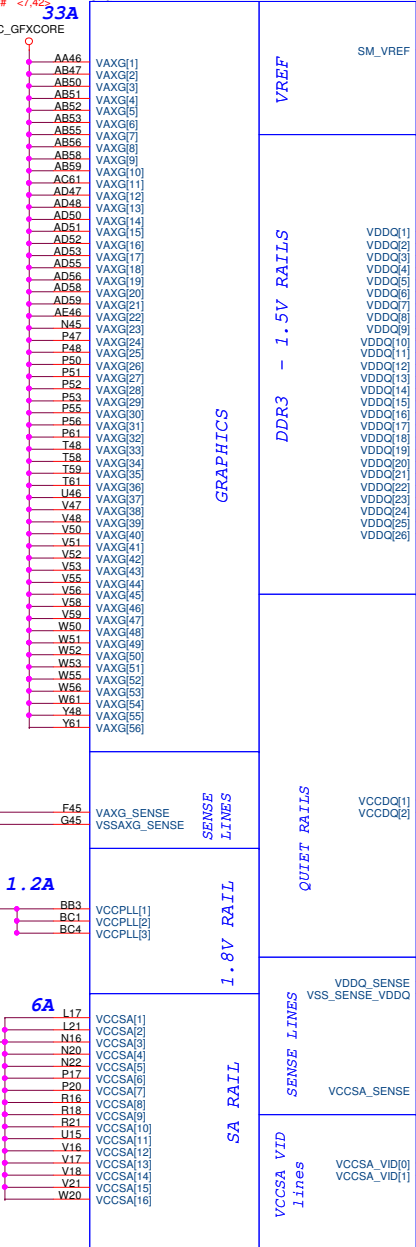
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 Sandy Bridge (5/6)  
 LA-7731P  
 Thursday, September 01, 2011 Sheet 10 of 59

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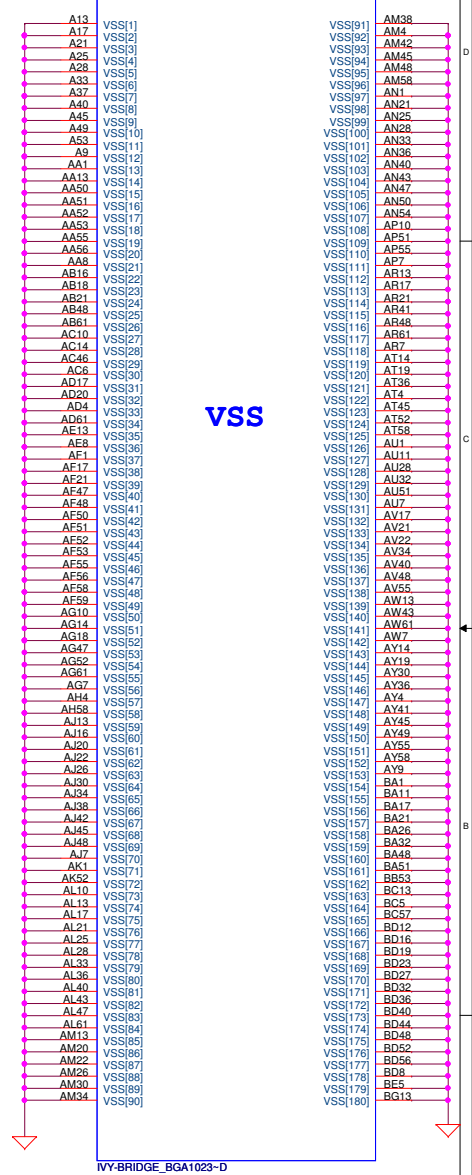
**+1.5V\_CPU\_VDDQ Source**



**POWER**



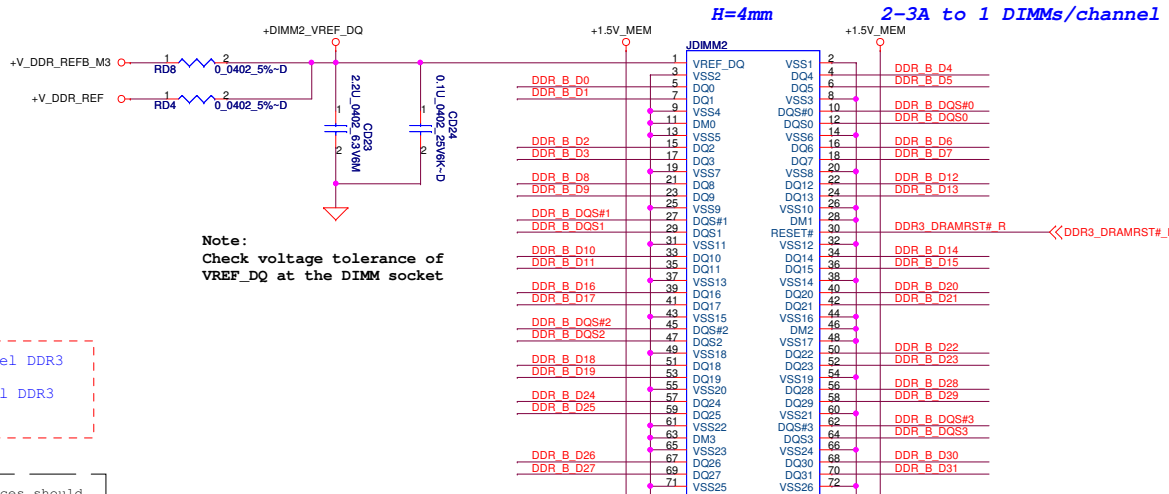
**UIH**



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**Sandy Bridge (6/6)**  
**LA-7731P**  
 Date: Thursday, September 01, 2011 Sheet 11 of 59





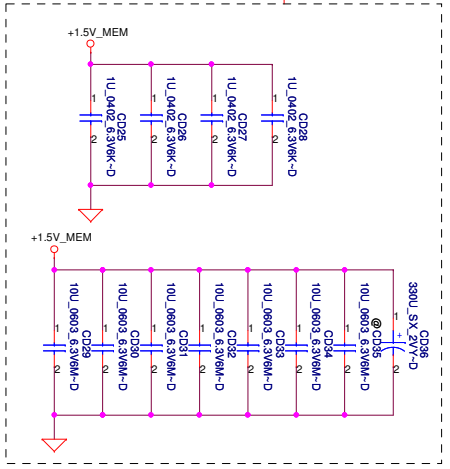
Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

Populate RD4, De-Populate RD8 for Intel DDR3  
VREFDQ multiple methods M1  
Populate RD8, De-Populate RD4 for Intel DDR3  
VREFDQ multiple methods M3

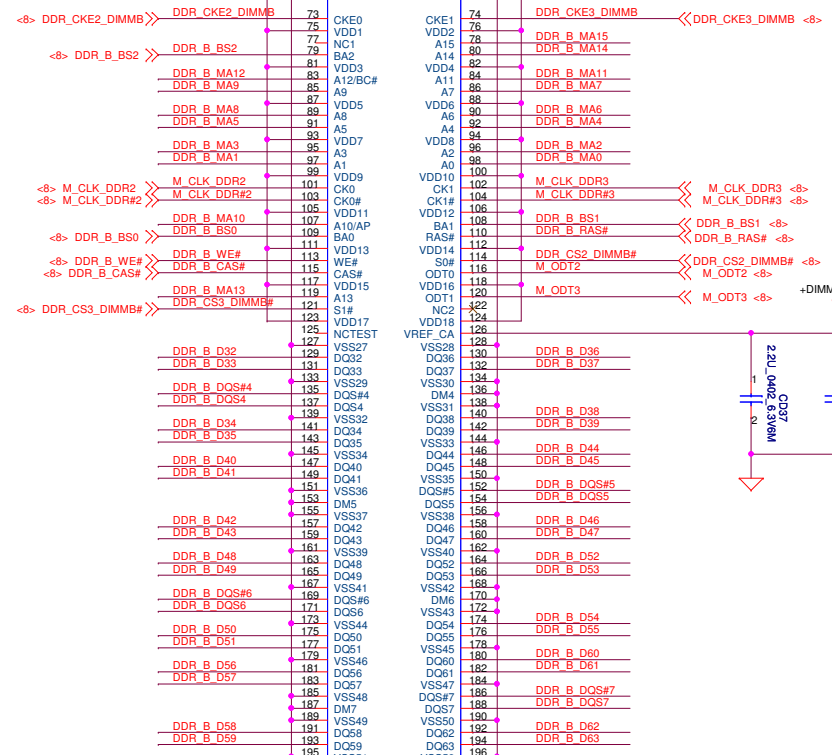
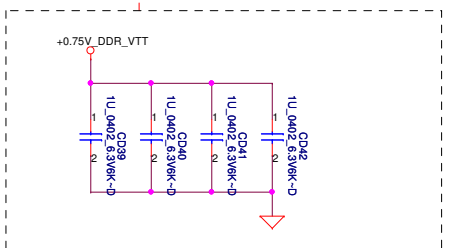
- <<-> DDR\_B\_DQS#[0..7] <<>>
- <<-> DDR\_B\_DQ[0..63] <<>>
- <<-> DDR\_B\_DQS#[0..7] <<>>
- <<-> DDR\_B\_MA[0..15] <<>>

All VREF traces should  
have 10 mil trace width

Layout Note:  
Place near JDIMM2



Layout Note:  
Place near JDIMM2.203, 204



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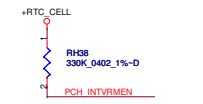


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Title <b>DDRIII-SODIMM SLOT2</b>			
Size	Document Number <b>LA-7731P</b>	Rev 0.3	
Date	Thursday, September 01, 2011	Sheet	13 of 59

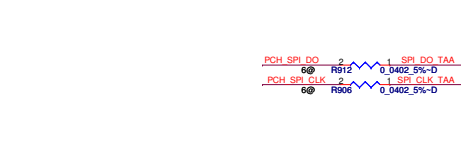
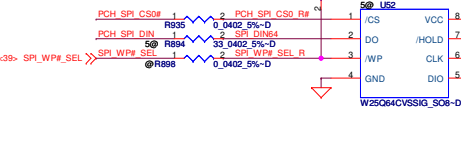
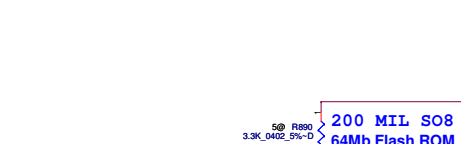
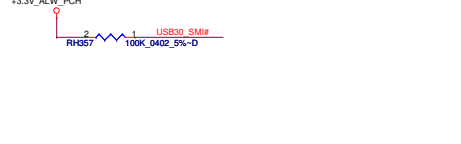
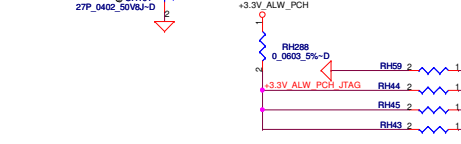
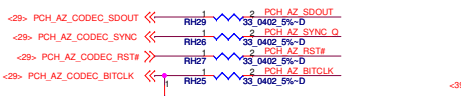
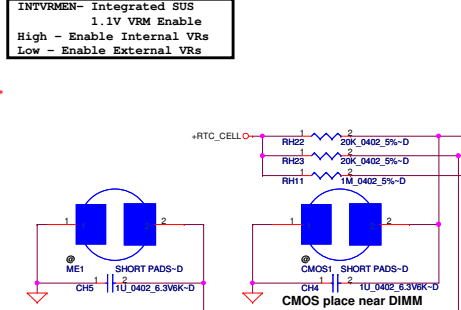
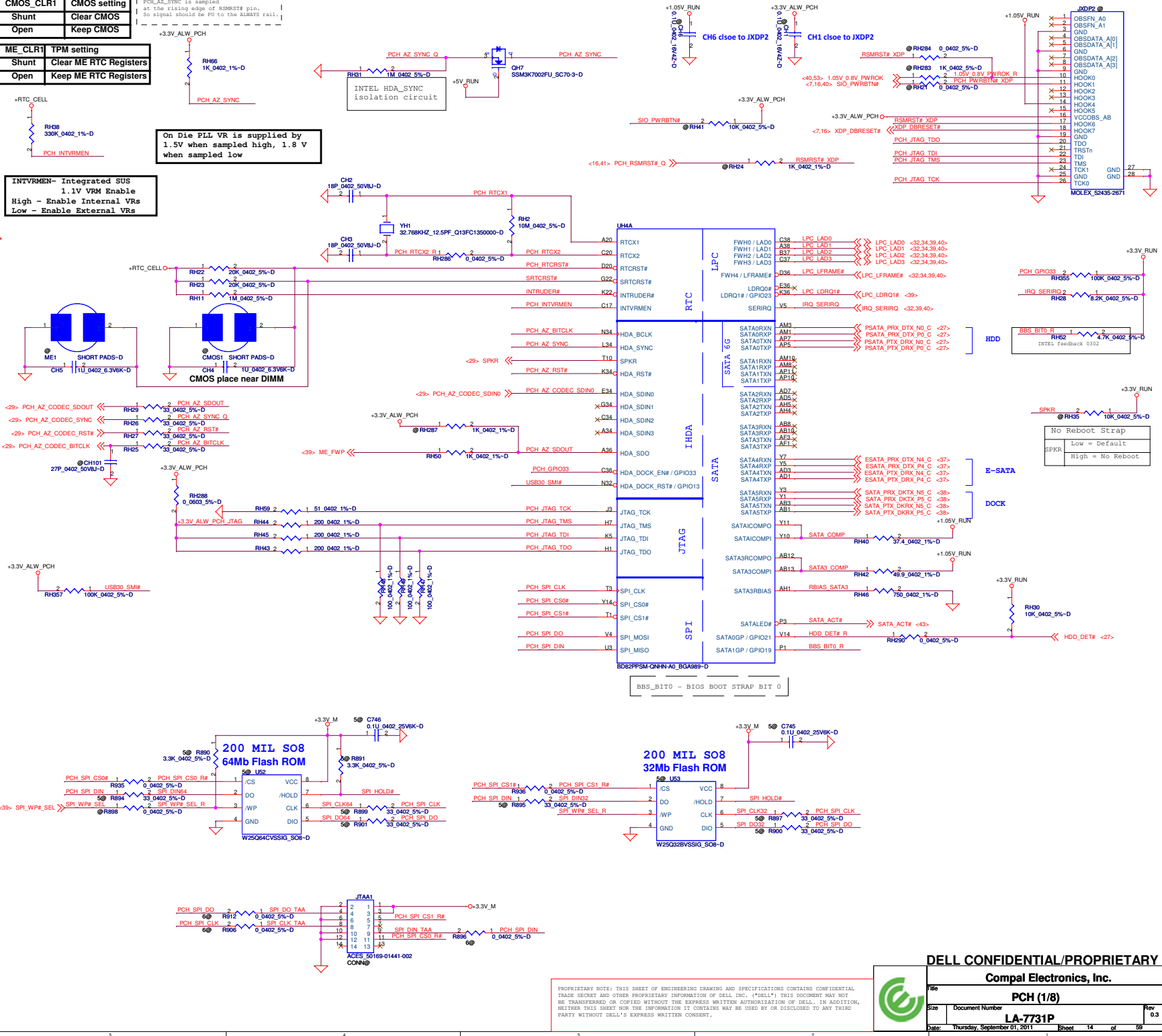
CMOS CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



On Die PLL VR is supplied by 1.5V when sampled high, 1.8 v when sampled low

INTVRMEN- Integrated SUS  
1.1V VRM Enable  
High - Enable Internal VRs  
Low - Enable External VRs



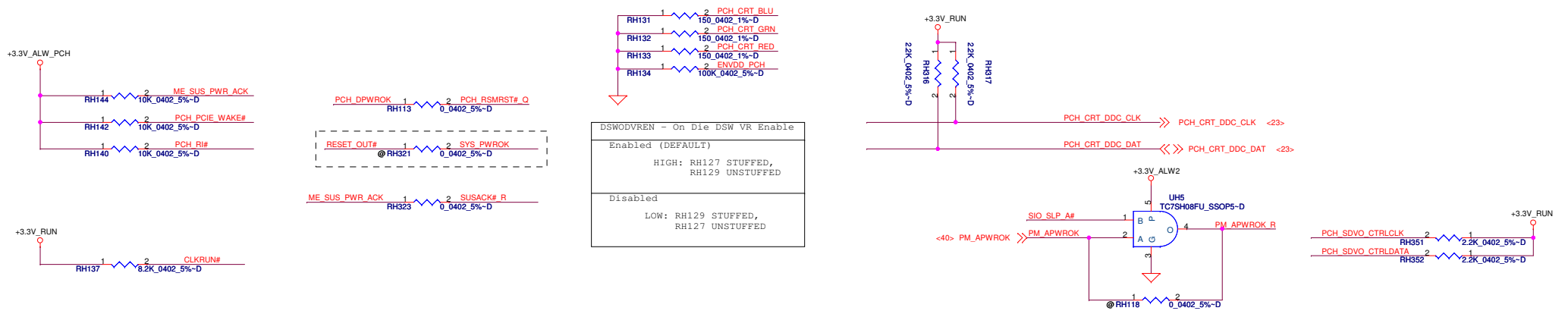
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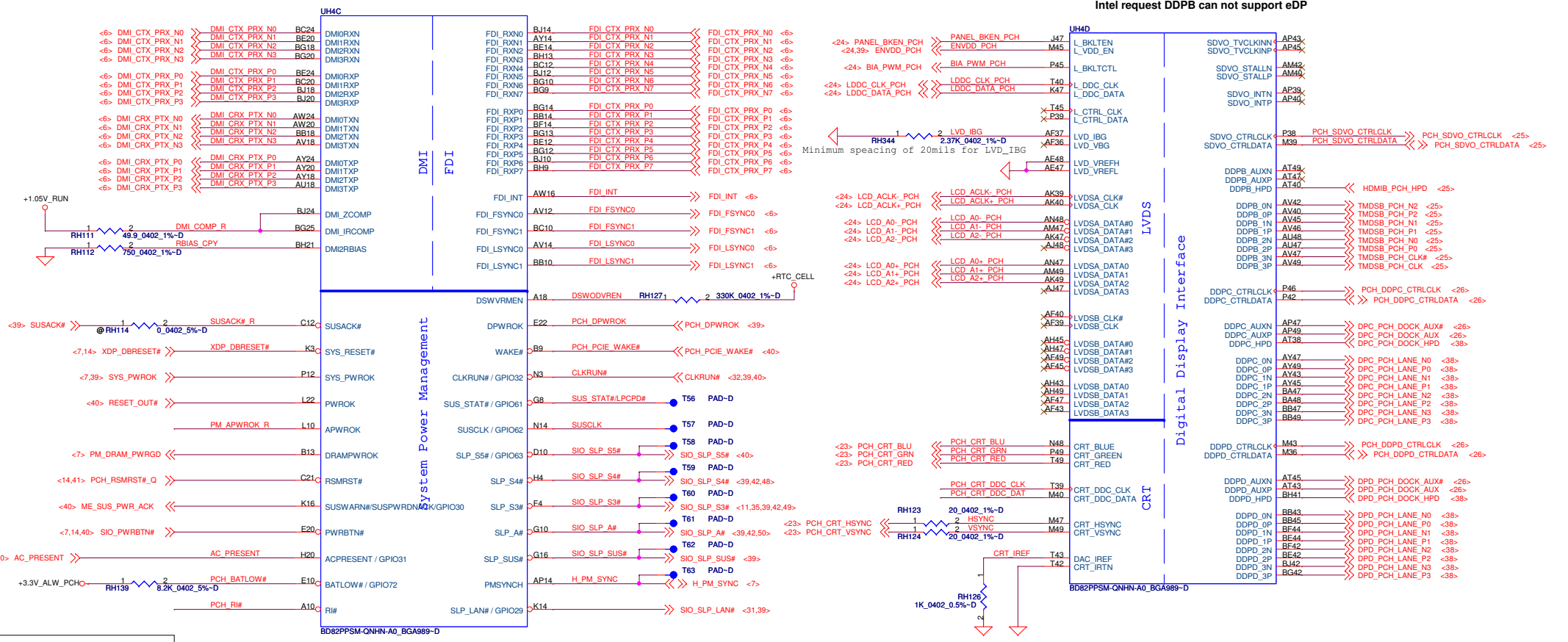
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PCH (1/8)		
File	Document Number	Rev
	LA-7731P	0.3
Date:	Thursday, September 01, 2011	Sheet 14 of 59





DSWODVREN - On Die DSW VR Enable	
Enabled (DEFAULT)	HIGH: RH127 STUFFED, RH129 UNSTUFFED
Disabled	LOW: RH129 STUFFED, RH127 UNSTUFFED

Intel request DDPB can not support eDP



Remove RH116, RH117, RH118, RH320, RH120, RH121, RH122 to save room for D4 12" only

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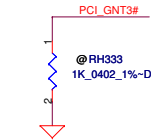
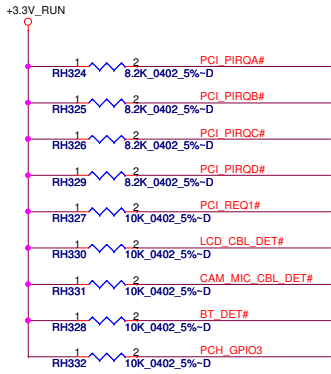
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Size: Document Number: **LA-7731P**

Date: Thursday, September 01, 2011 Sheet 16 of 59

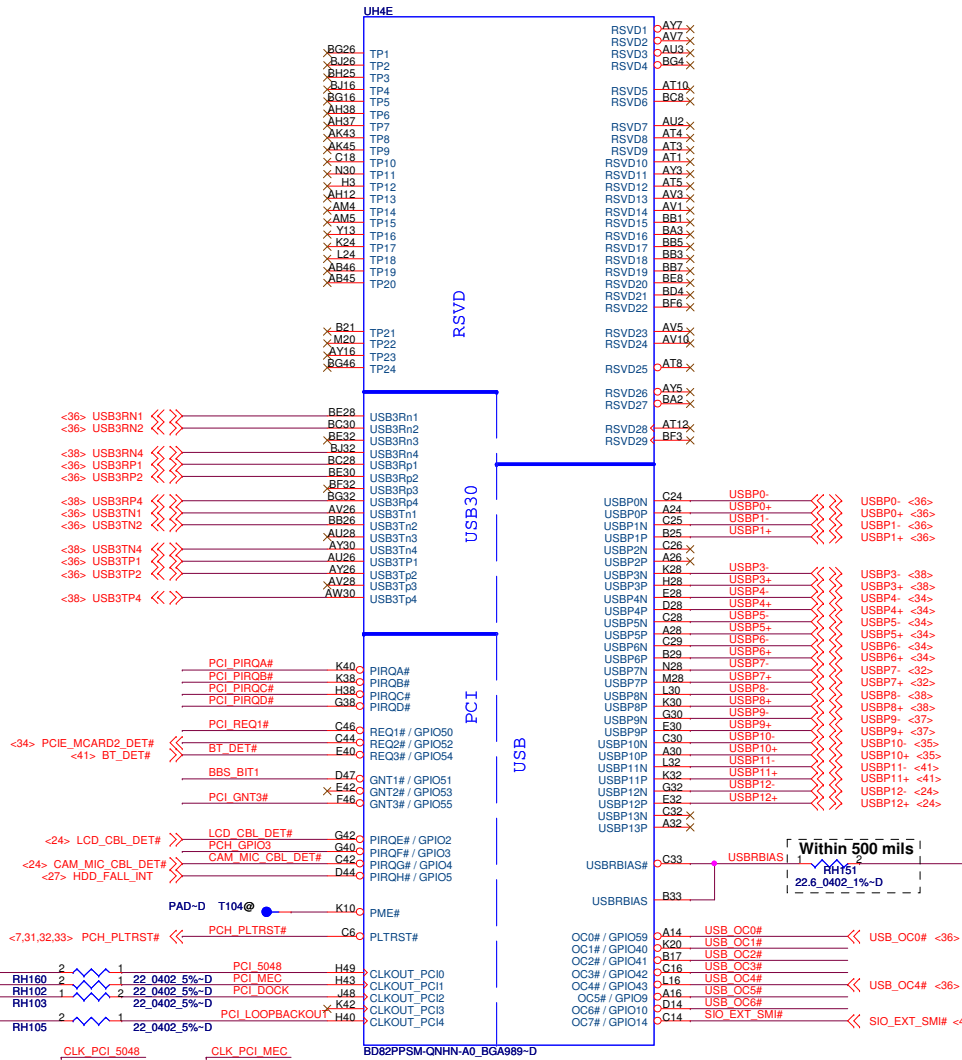
Rev: 0.3



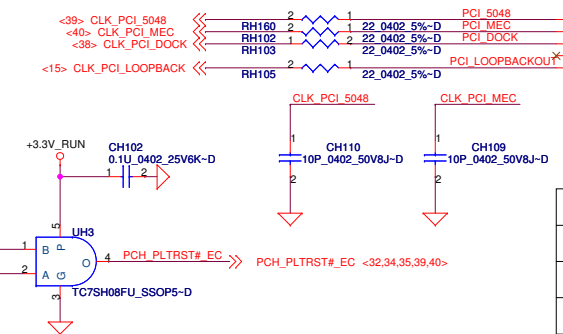
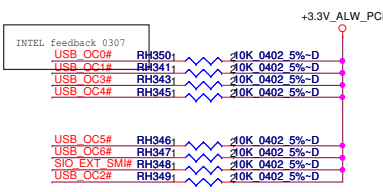


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

Remove RH335, RH336, RH337, RH338 to save room for D12" only



- >Right Side Top
- >Right Side Bottom
- >MLK DOCK
- >WLAN/WIMAX
- >WWAN/UWB
- >Flash
- >USH
- >DOCK
- >Left side E-SATA
- >Express Card
- >Blue Tooth
- >Camera



BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

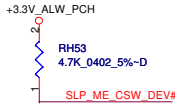
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**PCH (4/8)**

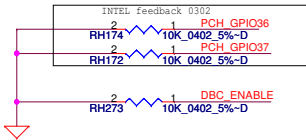
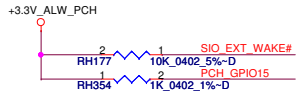
**LA-7731P**

Date: Thursday, September 01, 2011 Sheet 17 of 59

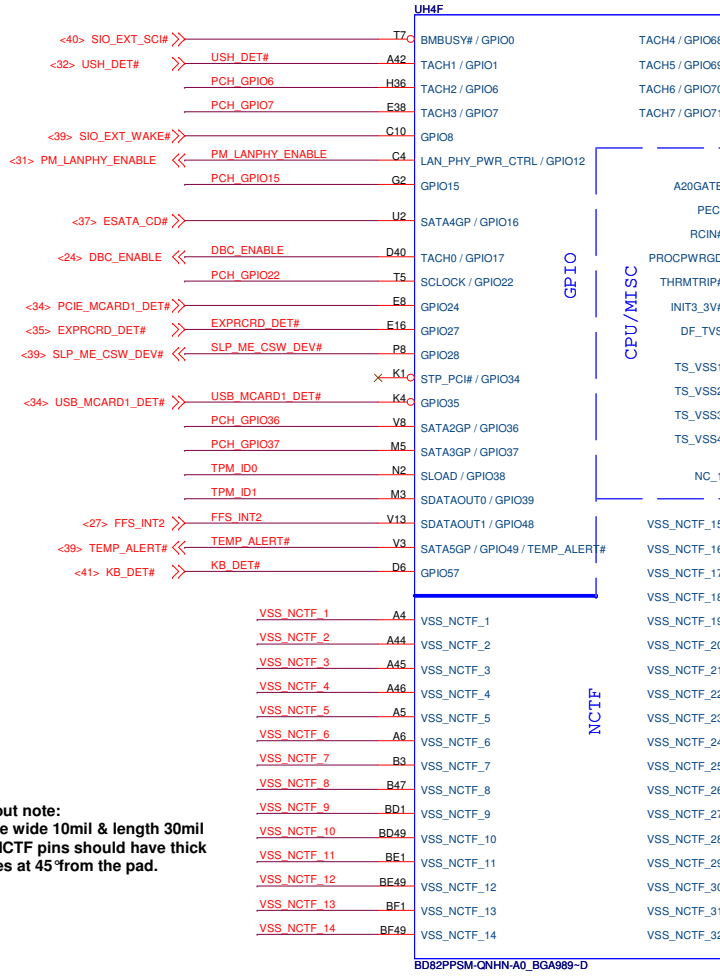
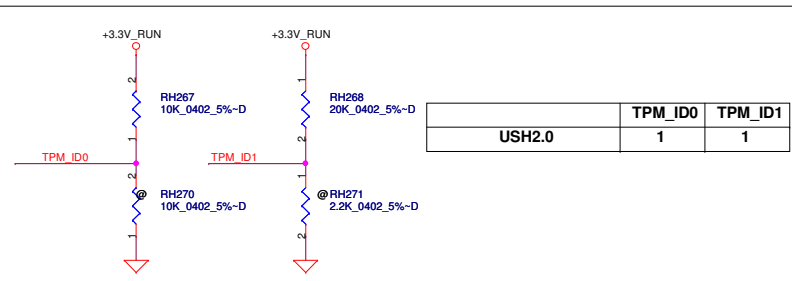
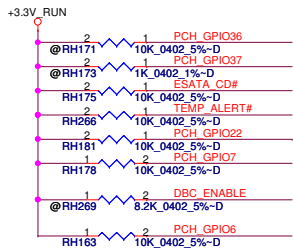
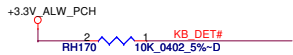


Note: PCH has internal pull up 20k ohm on E3\_PAID\_TS\_DET# (GPIO27)

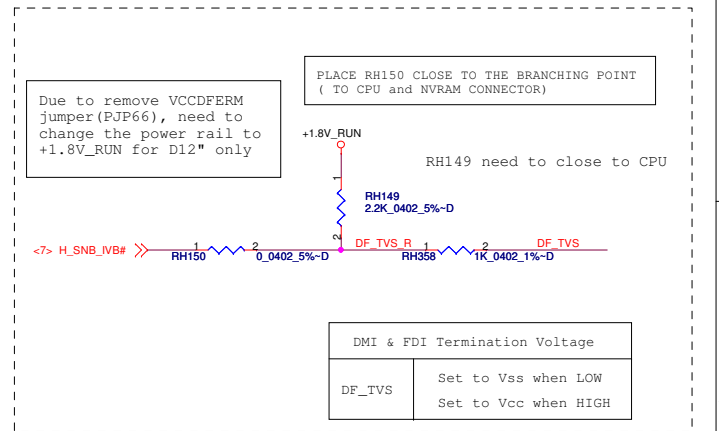
SLP_ME_CSW_DEV#	PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT	
DISABLED - LOW	



Layout note:  
Trace wide 10mil & length 30mil  
All NCTF pins should have thick traces at 45° from the pad.



Layout note:  
Trace wide 10mil & length 30mil  
All NCTF pins should have thick traces at 45° from the pad.



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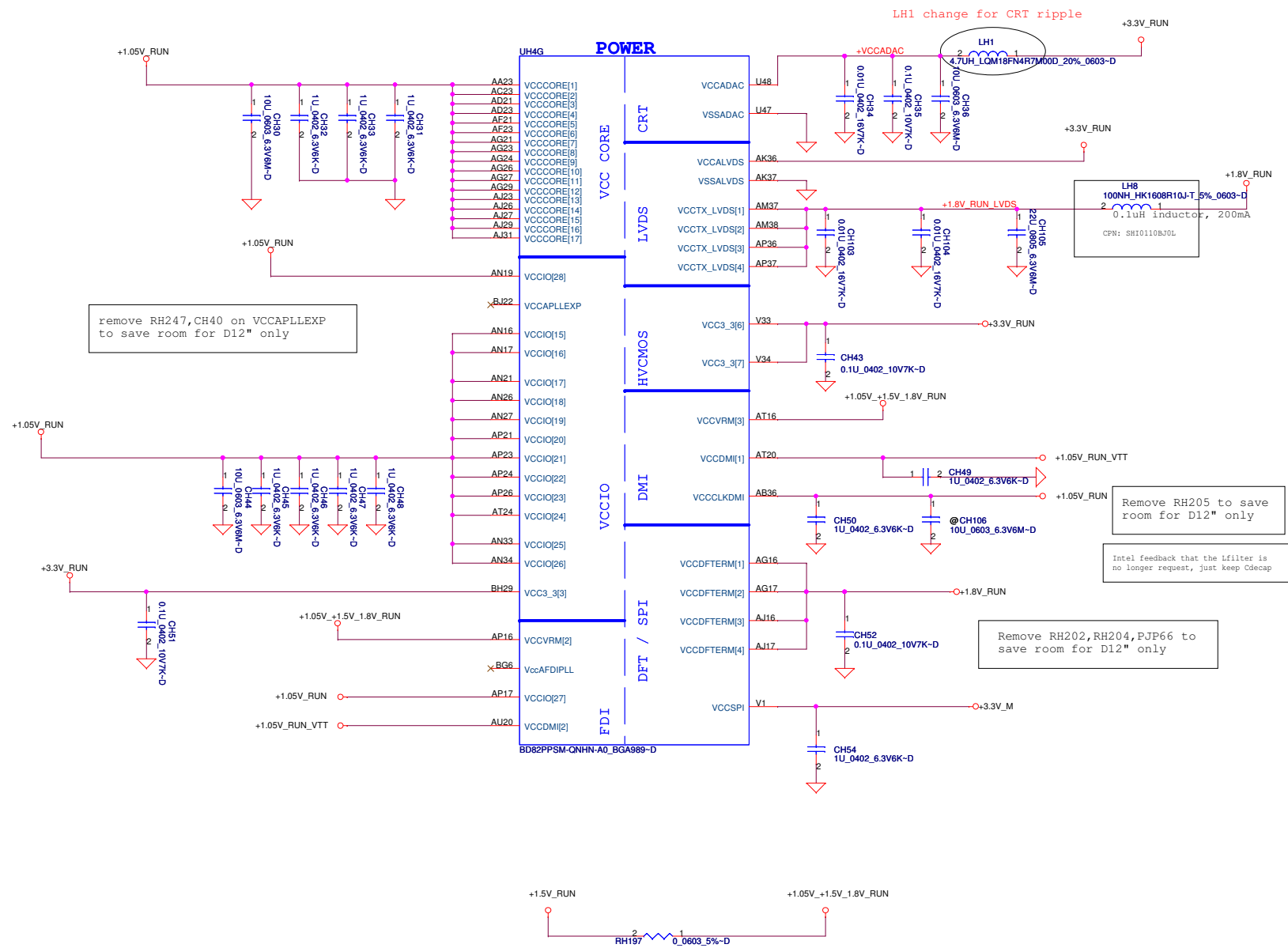
Compal Electronics, Inc.

PCH (5/8)

LA-7731P

Rev 0.3

Date: Thursday, September 01, 2011 Sheet 18 of 59



PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.003
VCCDFTERM	1.8	0.19
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.119
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06
VccAPLLEXP	1.05	0.05

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Remove RH253 to save room for D12" only

Remove LH3,CH58 on VCCAPLLDMI2 to save room for D12" only

remove LH5,CH80 on VCCAPLLSATAta to save room for D12" only

### POWER

#### USB

#### Clock and Miscellaneous

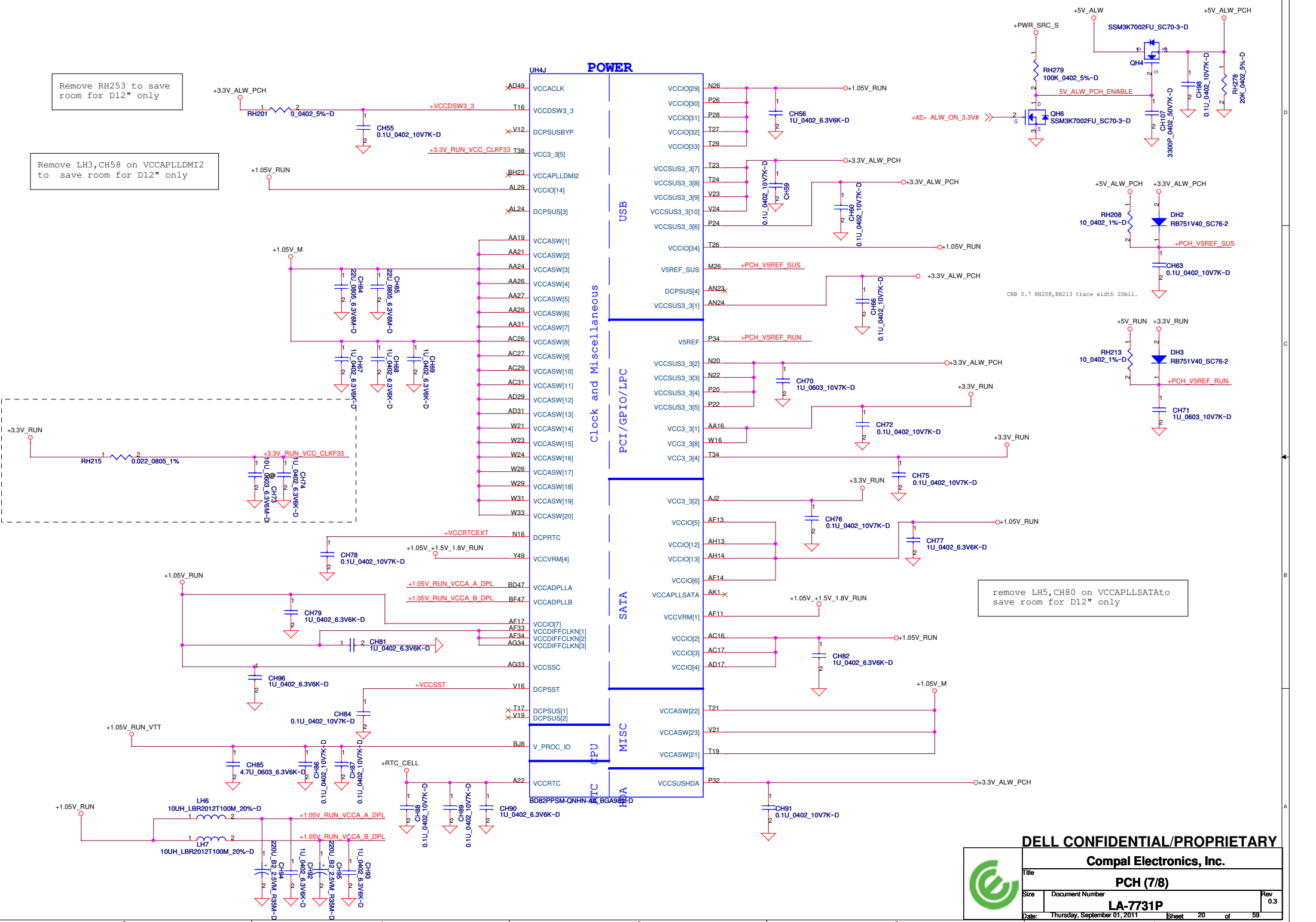
#### PCI/GPIO/LPC

#### SATA

#### MISC

#### ICP CPU

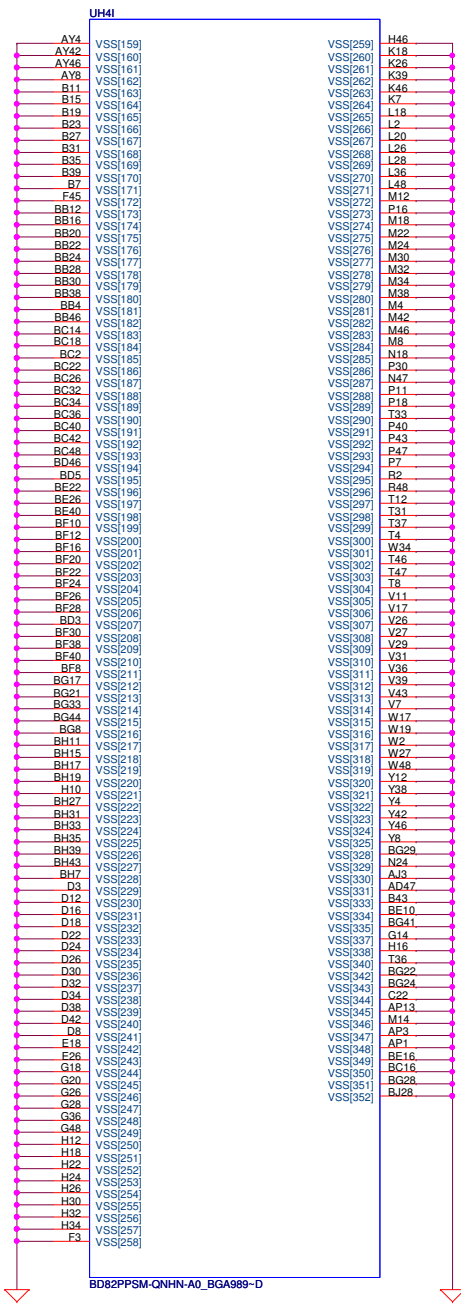
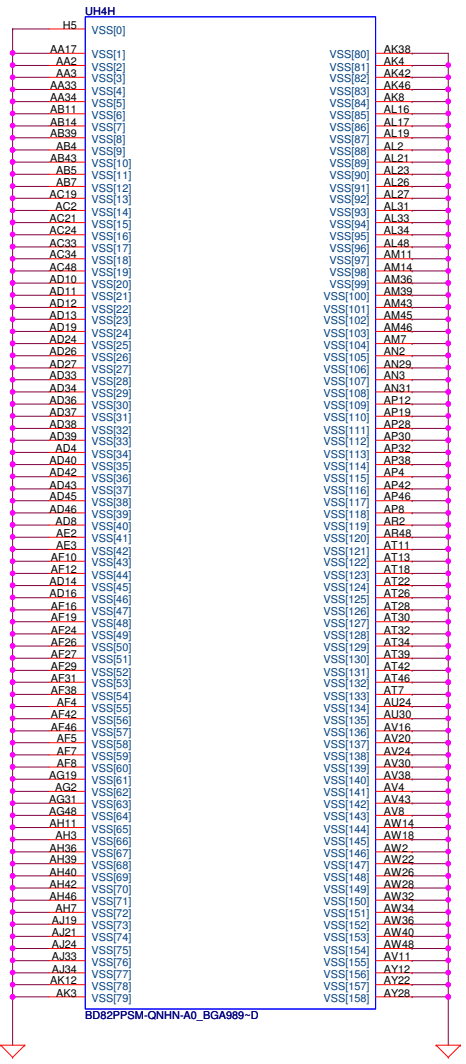
#### HA



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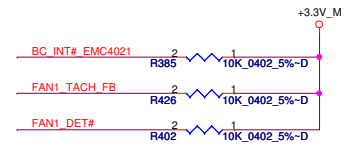
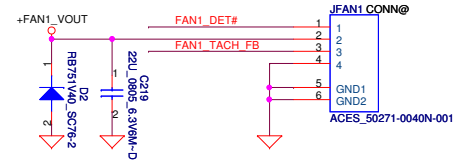
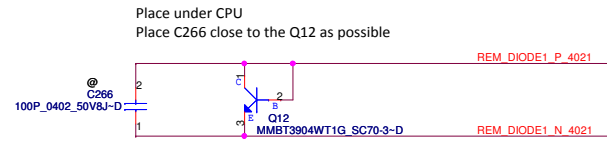
**Compal Electronics, Inc.**

Title: **PCH (8/8)**

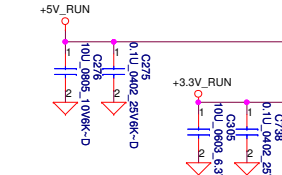
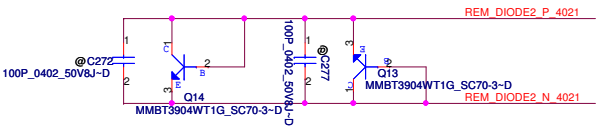
Size: **LA-7731P**

Date: **Thursday, September 01, 2011** Sheet **21** of **59**

Rev: **0.3**

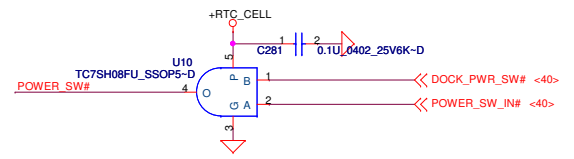
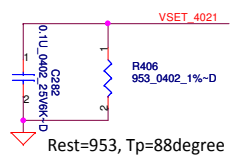
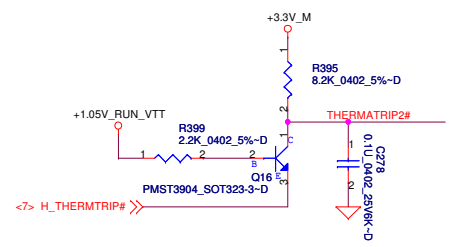
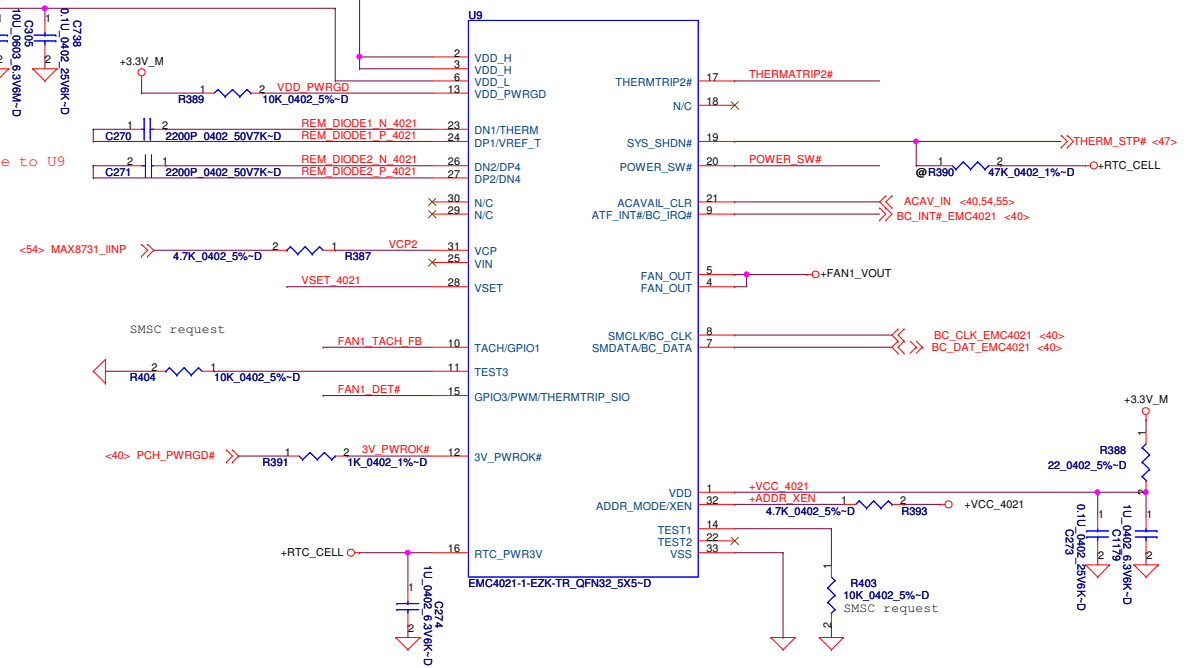


- (1) DP2/DN2 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
- (2) DP4/DN4 for Skin on Q13, place Q13 close to Vcore VR choke.



place C270/C271 close to U9

Change to EMC4021 for cost saving

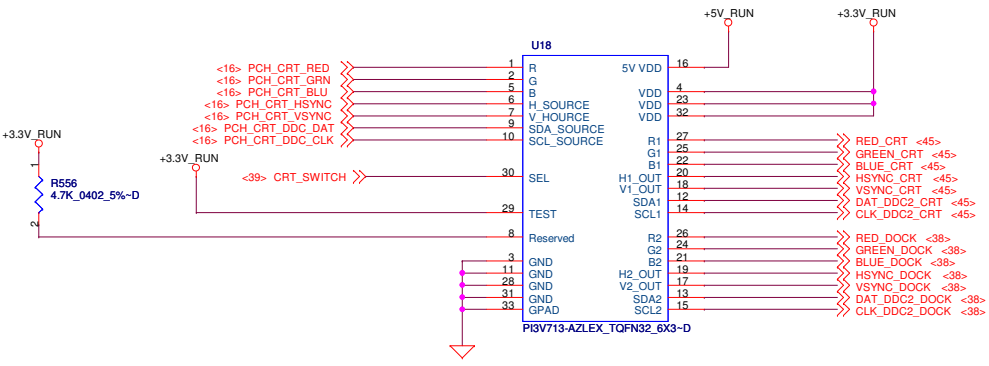


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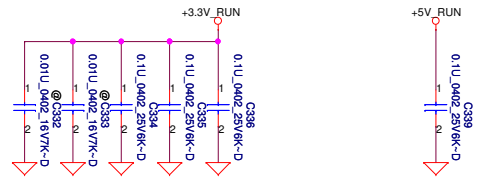
<b>Compal Electronics, Inc.</b>			
<b>FAN &amp; Thermal Sensor</b>			
<b>LA-7731P</b>			
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Date:	Thursday, September 01, 2011	Sheet	22 of 59

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# SW for MB/DOCK

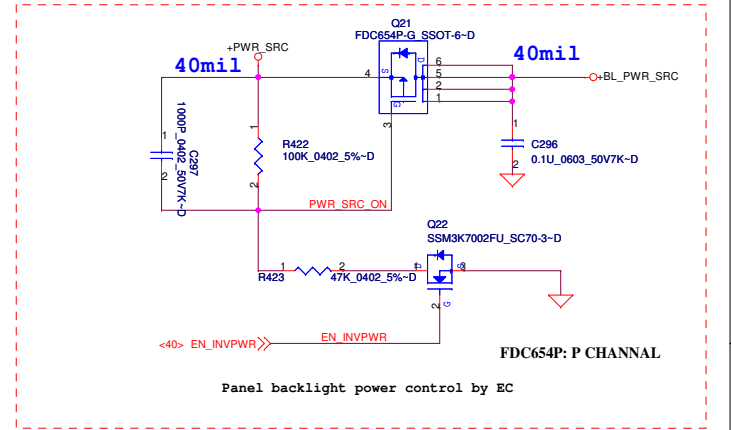
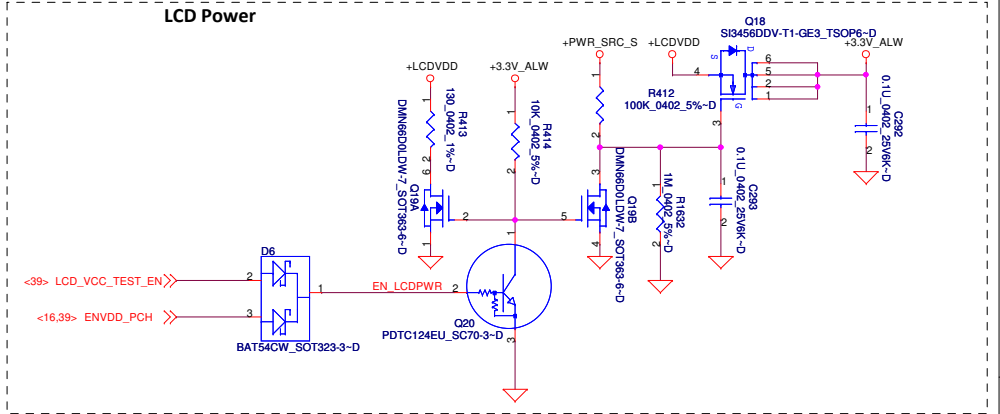
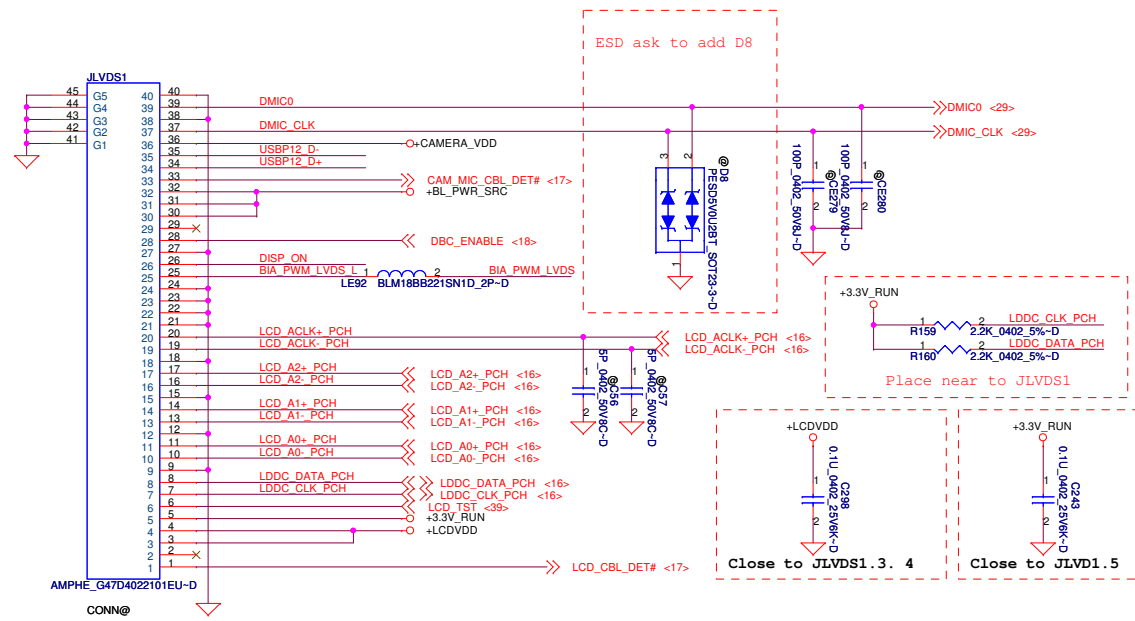


SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

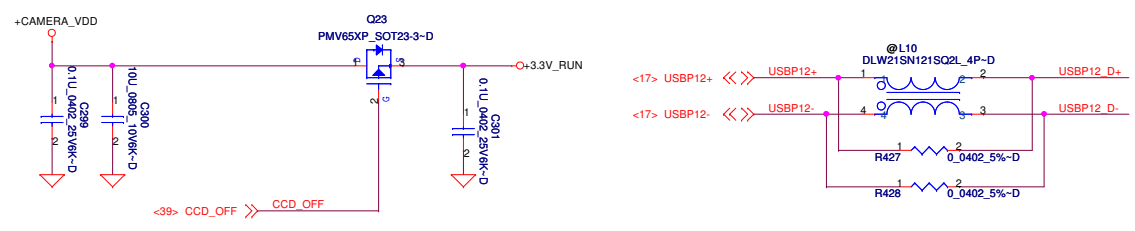


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	<b>CRT/Video switch</b>		
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		<b>LA-7731P</b>	0.3
Date:	Thursday, September 01, 2011	Sheet	23 of 59



**For Webcam**



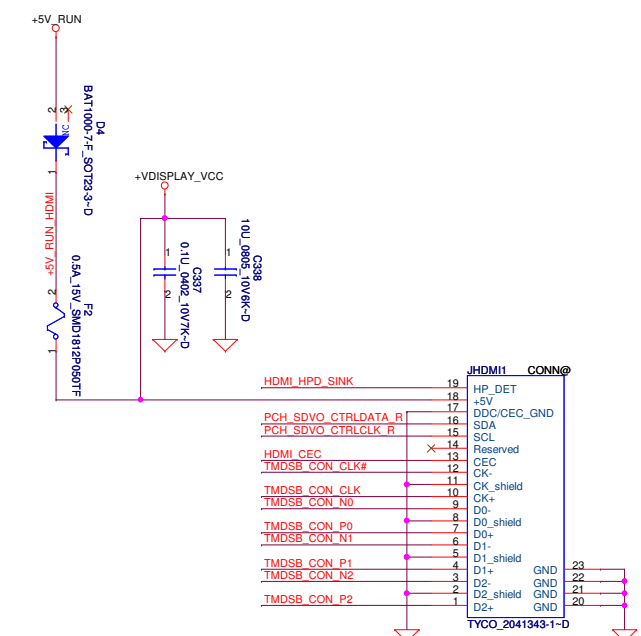
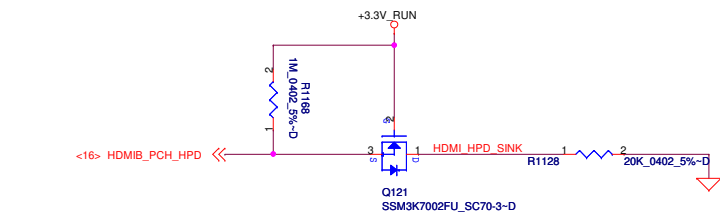
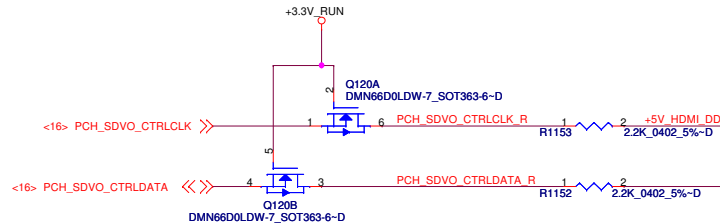
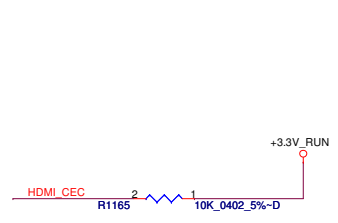
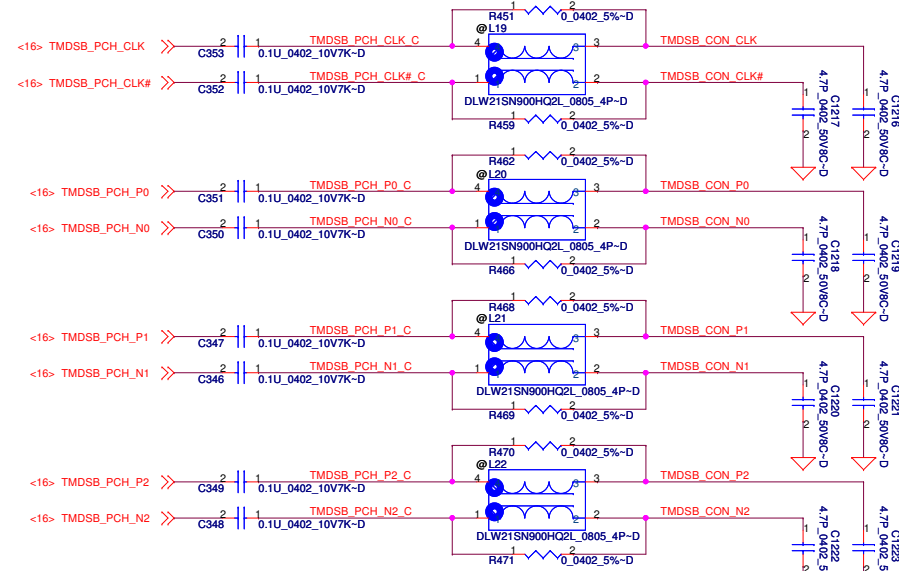
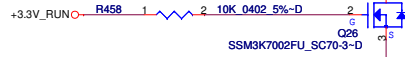
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	<b>LA-7731P</b>	<b>0.3</b>
Date:	Thursday, September 01, 2011	Sheet 24 of 59



TMDSB_PCH_P2_C	R452	1	2	680_0402_5%-D	HDMI_OB
TMDSB_PCH_N2_C	R450	1	2	680_0402_5%-D	
TMDSB_PCH_P1_C	R448	1	2	680_0402_5%-D	
TMDSB_PCH_N1_C	R449	1	2	680_0402_5%-D	
TMDSB_PCH_P0_C	R454	1	2	680_0402_5%-D	
TMDSB_PCH_N0_C	R453	1	2	680_0402_5%-D	
TMDSB_PCH_CLK_C	R456	1	2	680_0402_5%-D	
TMDSB_PCH_CLK#_C	R455	1	2	680_0402_5%-D	



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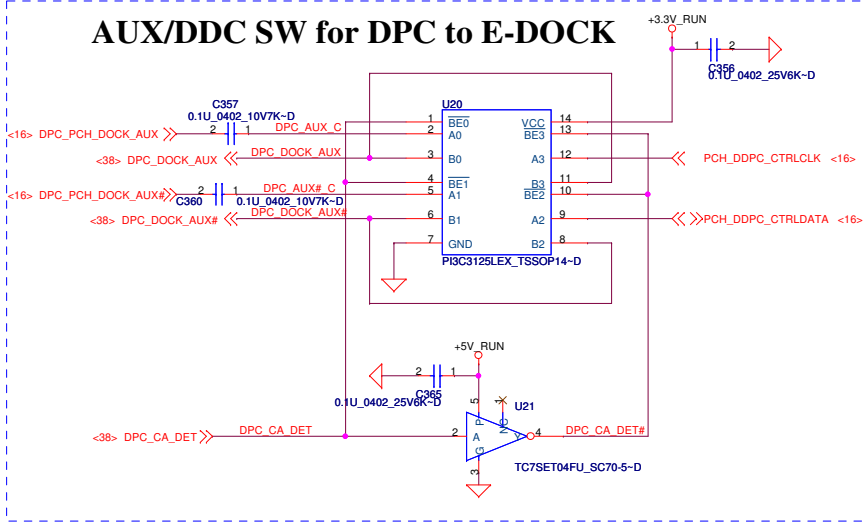
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**HDMI port**

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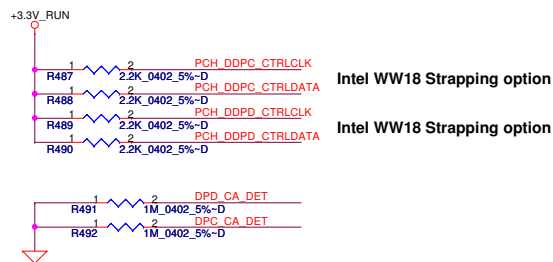
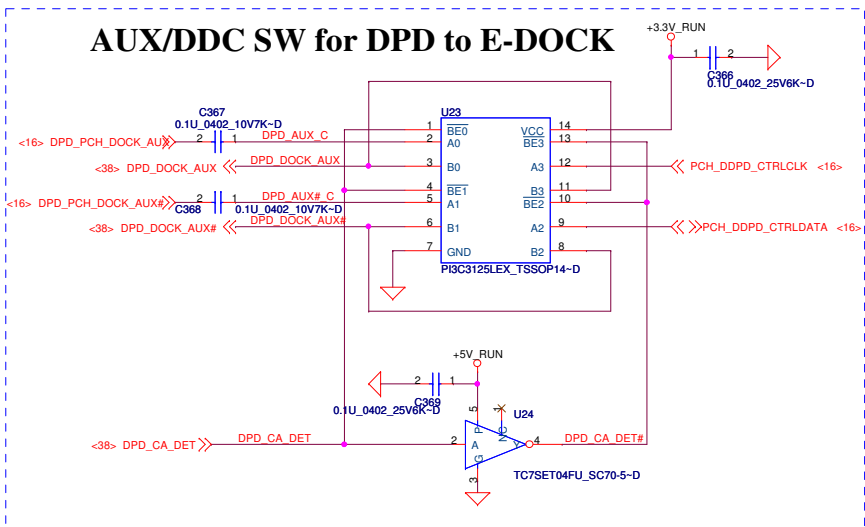
Thursday, September 01, 2011 Sheet 25 of 59

## AUX/DDC SW for DPC to E-DOCK



**There is a new die for PI3C3125. Sample available on May.**

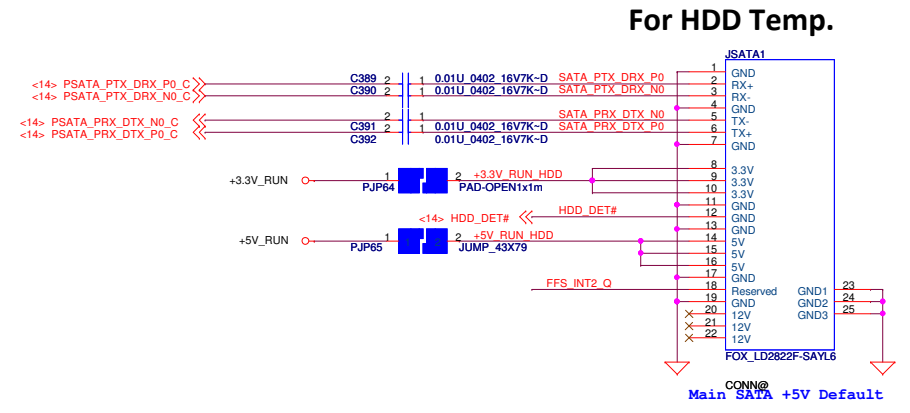
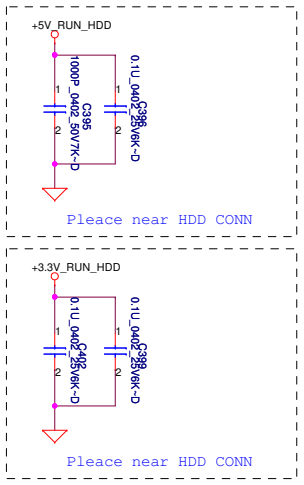
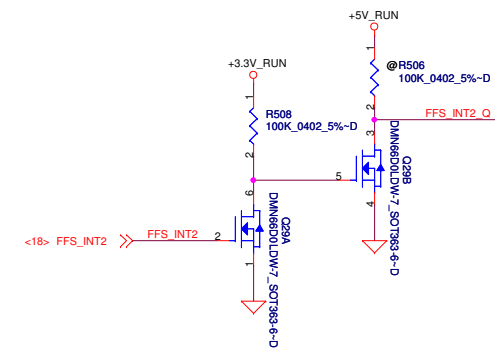
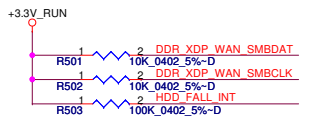
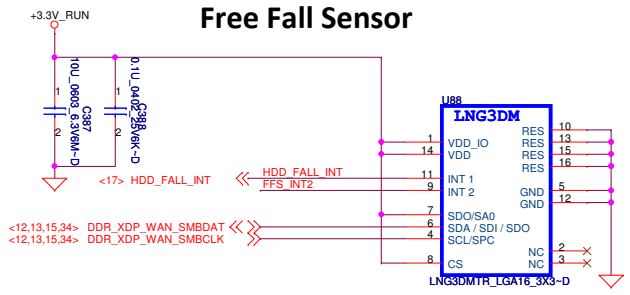
## AUX/DDC SW for DPD to E-DOCK



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Size	Document Number	Rev <b>0.3</b>	
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Title: **HDD CONNECTOR**

Size: Document Number **LA-7731P** Rev **0.3**

Date: Thursday, September 01, 2011 Sheet 27 of 59

5

4

3

2

1

D

D

C

C

B

B

A

A

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<b>ODD CONNECTOR</b>		
Size	Document Number	Rev
	<b>LA-7731P</b>	<b>0.3</b>
Date:	Thursday, September 01, 2011	
	Sheet	28 of 59

5

4

3

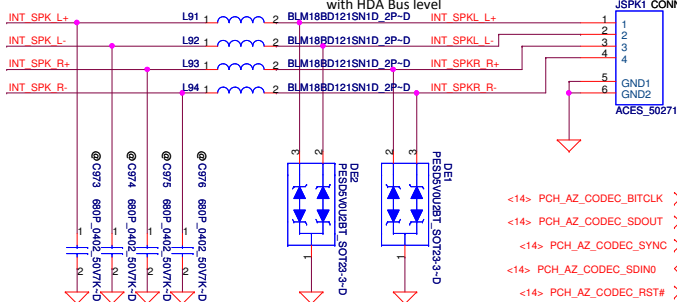
2

1

# Internal Speakers Header

15 mils trace

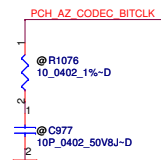
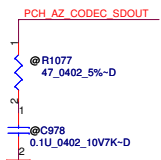
DVDD\_IO should match with HDA Bus level



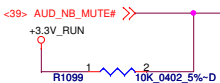
ESD ask to add DE1, DE2

Close to U72 pin5

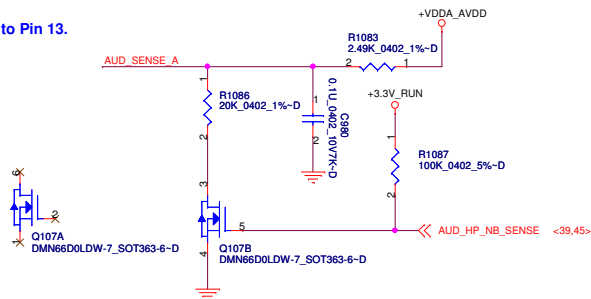
Close to U72 pin6



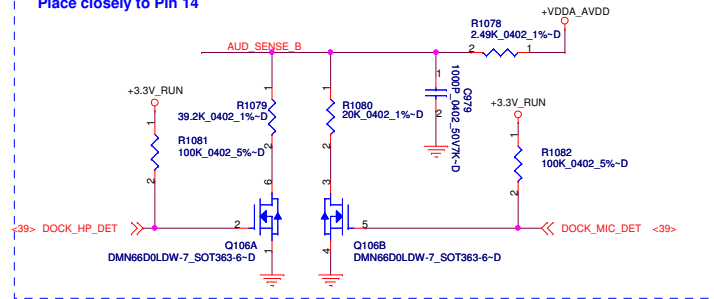
BCLK: Audio serial data bus bit clock input/output  
LRCLK: Audio serial data bus word clock input/output



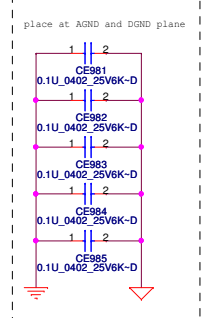
Place closely to Pin 13.



Place closely to Pin 14



EMI request to add C984, C985



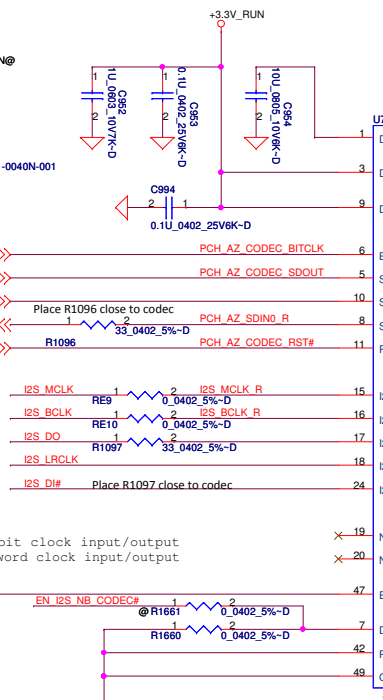
PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Intel
PORT D	Internal SPK
PORT E	DOCK
PORT F	DOCK

Notes:  
Keep PVDD supply and speaker traces routed on the DGNL plane.  
Keep away from AGND and other analog signals

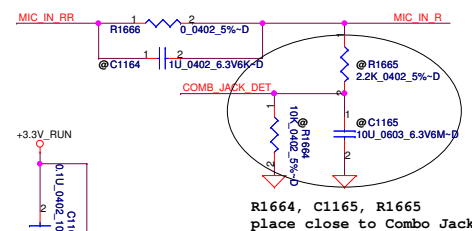
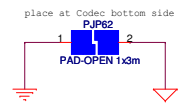
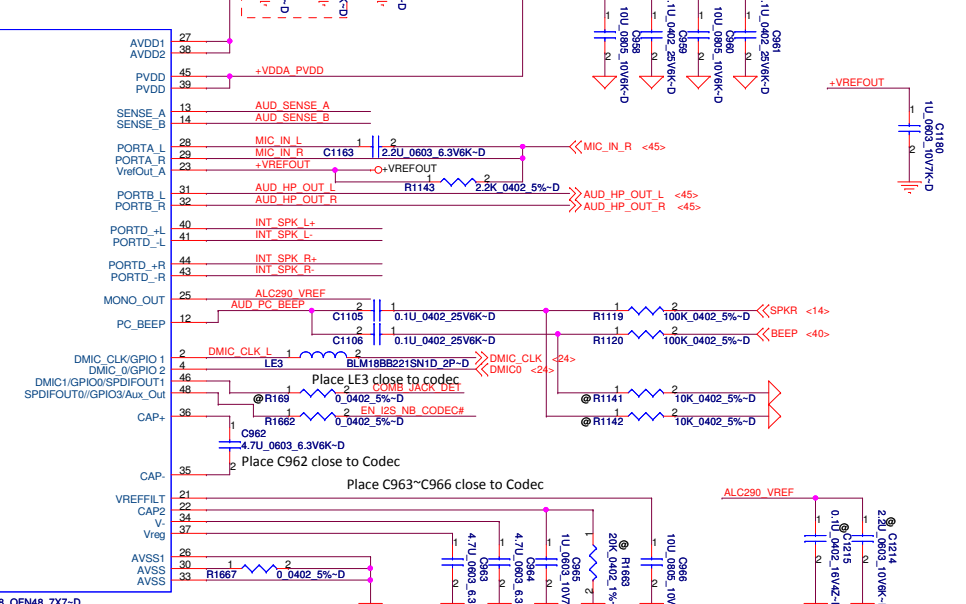
Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMICO
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

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Place C994, C952~C957 close to Codec

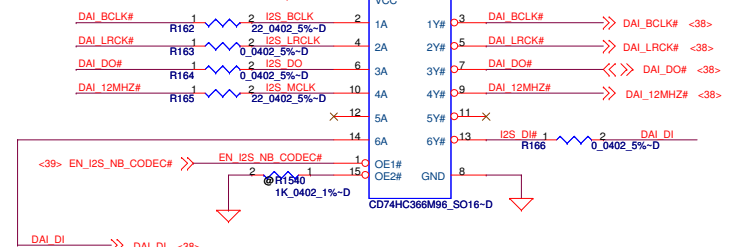


place close to pin27 place close to pin38



R1664, C1165, R1665 place close to Combo Jack

R162, R163, R164, R165, R166 CO-Lay with U73

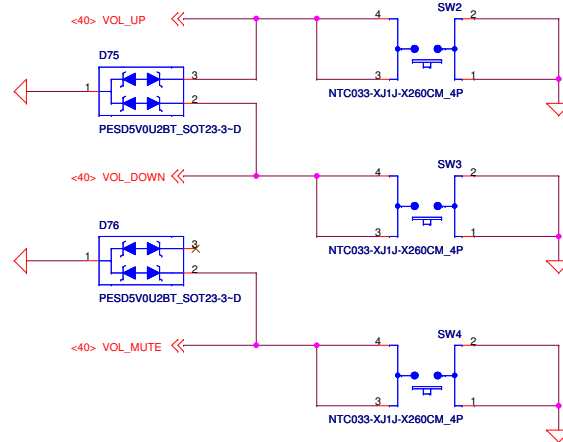
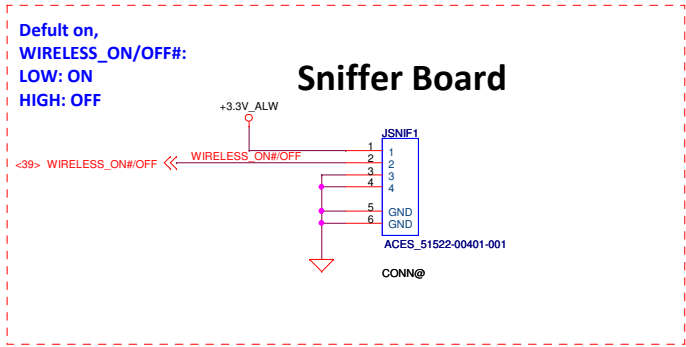
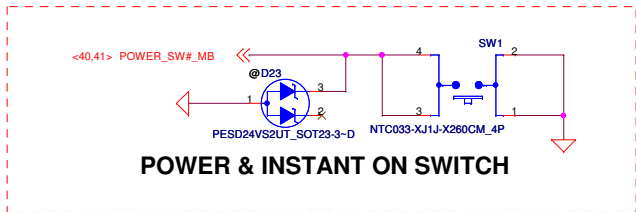


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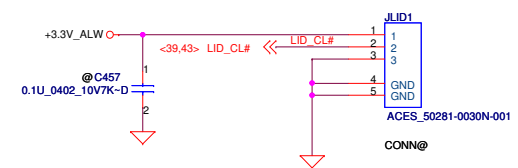
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Azalia (HD) Codec

Title	Document Number	Rev
	LA-7731P	0.3
Date	Thursday, September 01, 2011	Sheet 29 of 59



### Lid board



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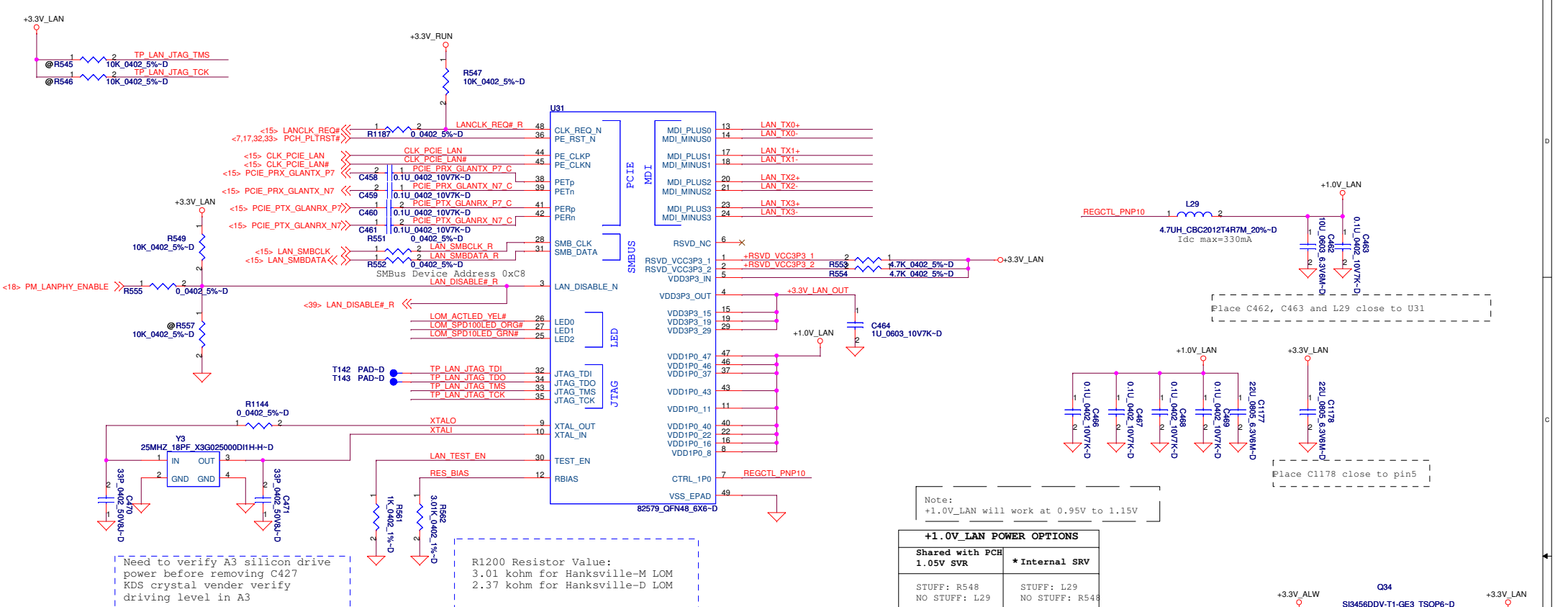
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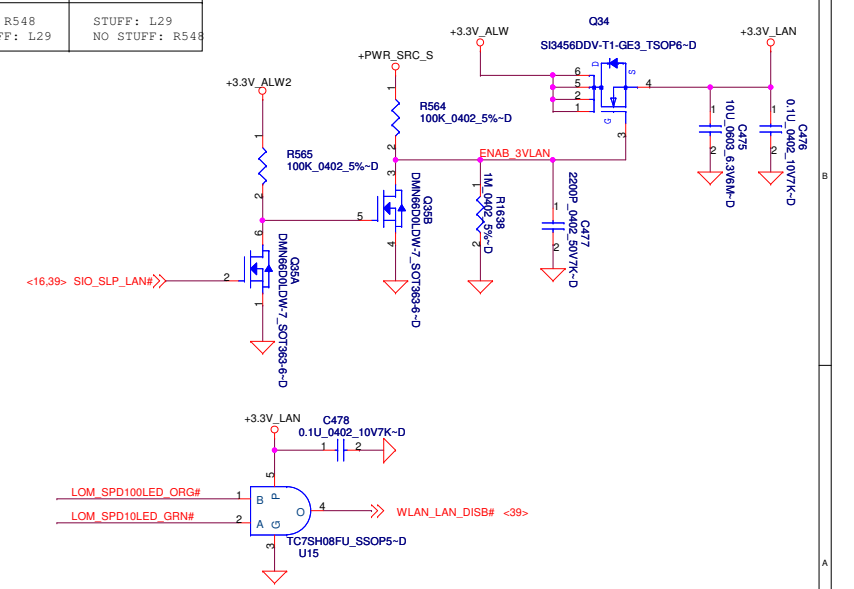
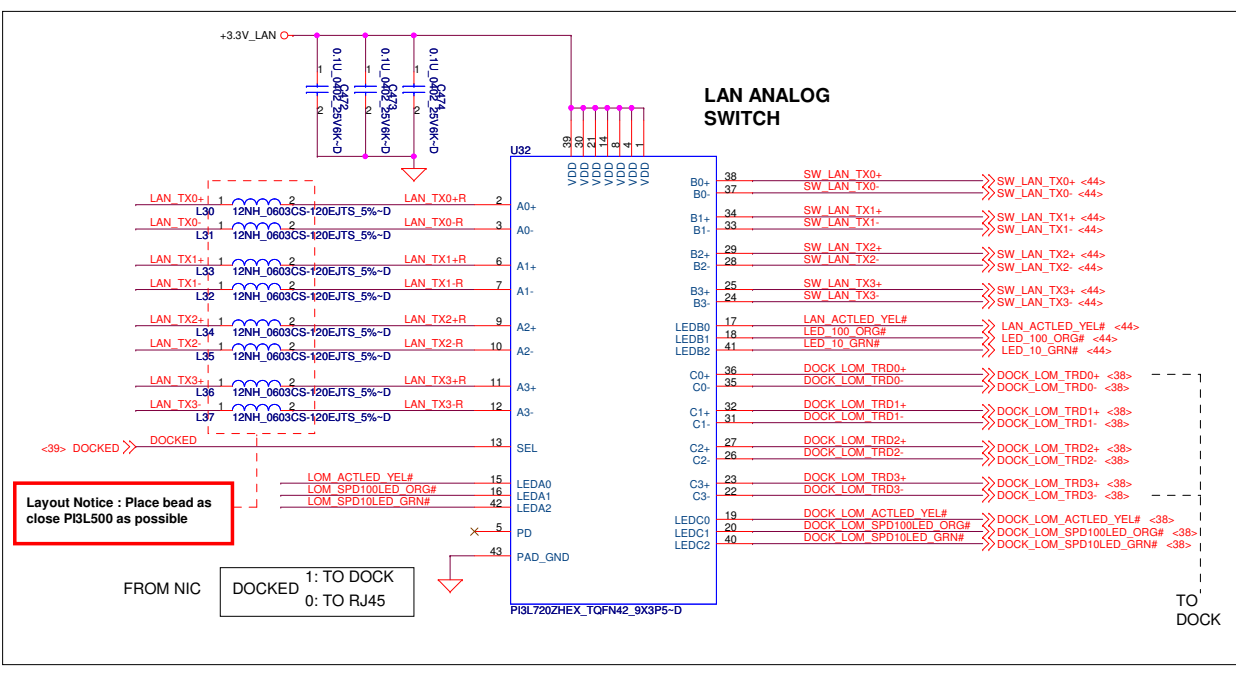
Title: **PWR SW/Sub-board Connector**

Size: **LA-7731P** Rev: **0.3**

Date: **Thursday, September 01, 2011** Sheet: **30** of **59**



+1.0V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	* Internal SRV
STUFF: R548 NO STUFF: L29	STUFF: L29 NO STUFF: R548



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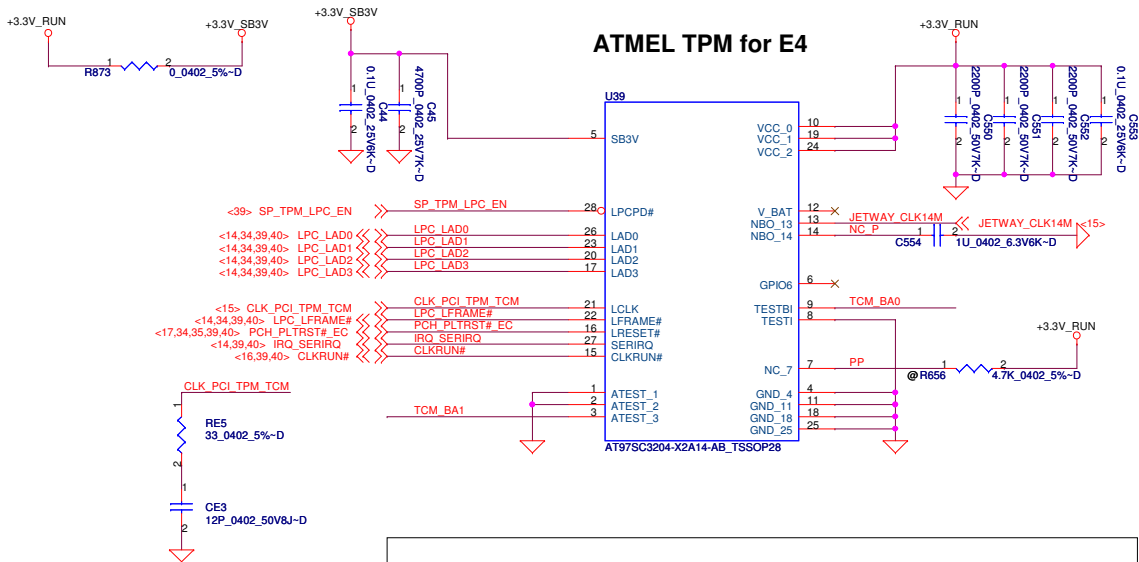
Title: **Intel 82579 (Hanksville) / LAN SW**

Size: **LA-7731P**

Document Number: **LA-7731P**

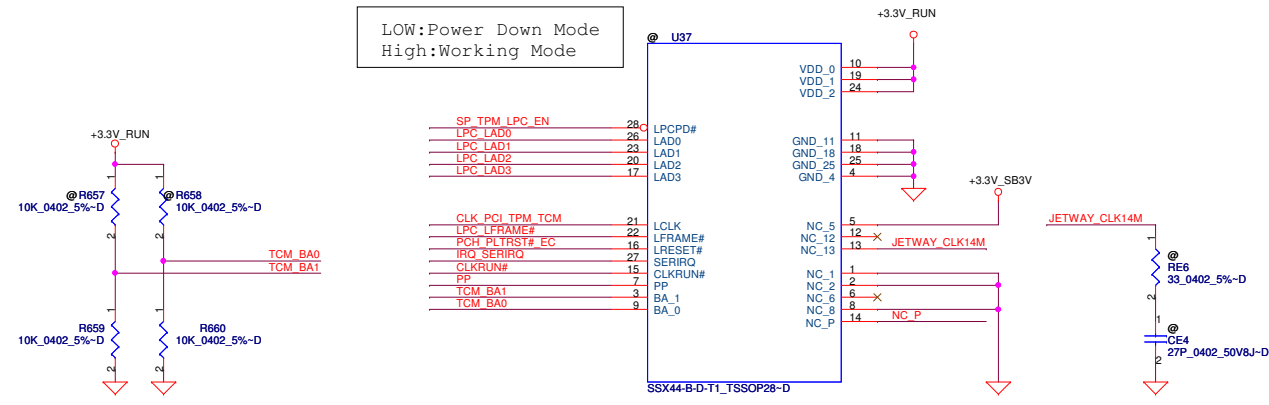
Date: Thursday, September 01, 2011

Sheet 31 of 59

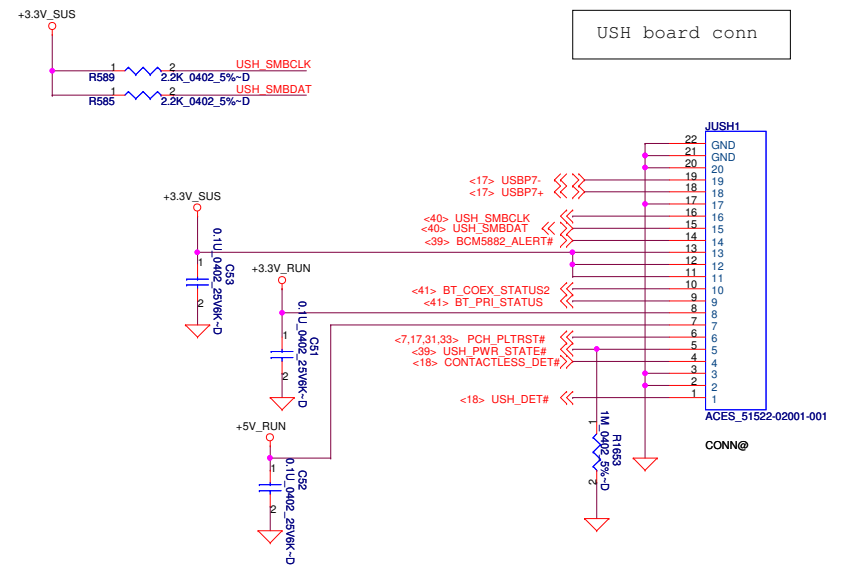


**Co-lay U37 and U39**  
**LPC layout: Place TCM first and then end LPC with TPM.**

**China TCM: NationZ & Jetway co-lay**



LOW:Power Down Mode  
 High:Working Mode



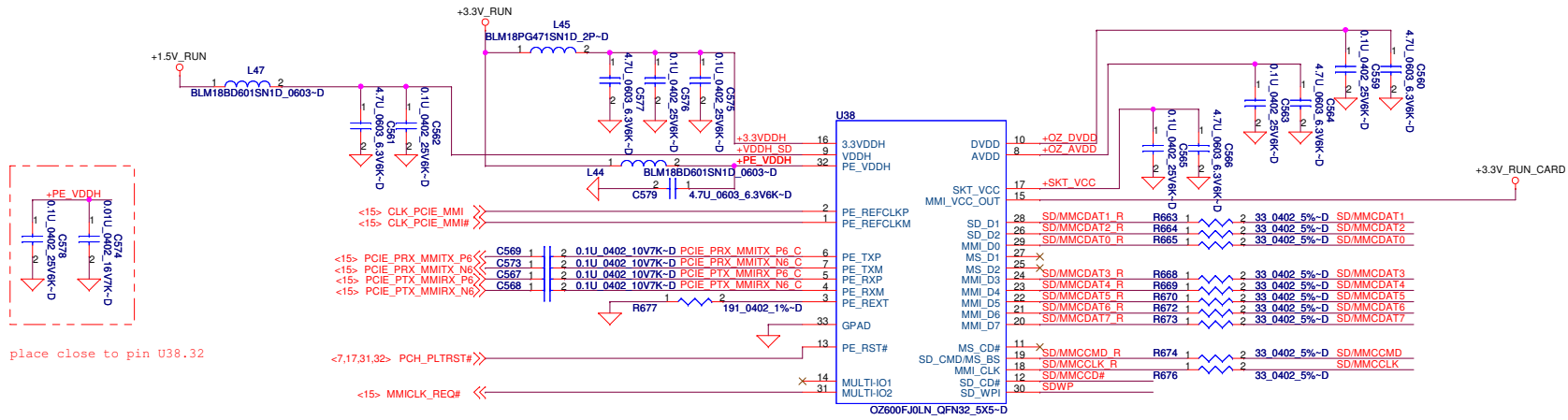
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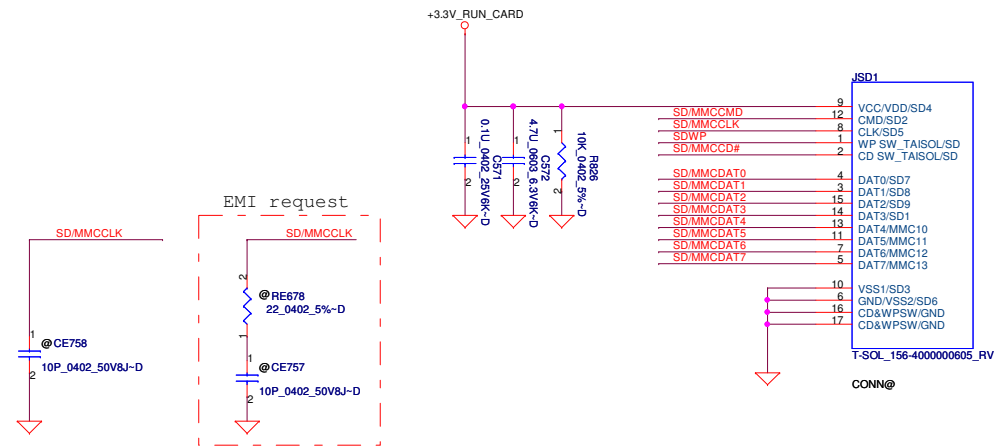
Title: **TPM/TCM**  
 Size: **LA-7731P**  
 Date: Thursday, September 01, 2011 Sheet 32 of 59

Rev: **0.3**





place close to pin U38.32



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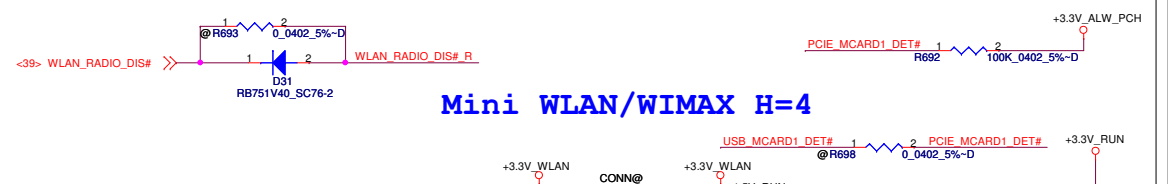
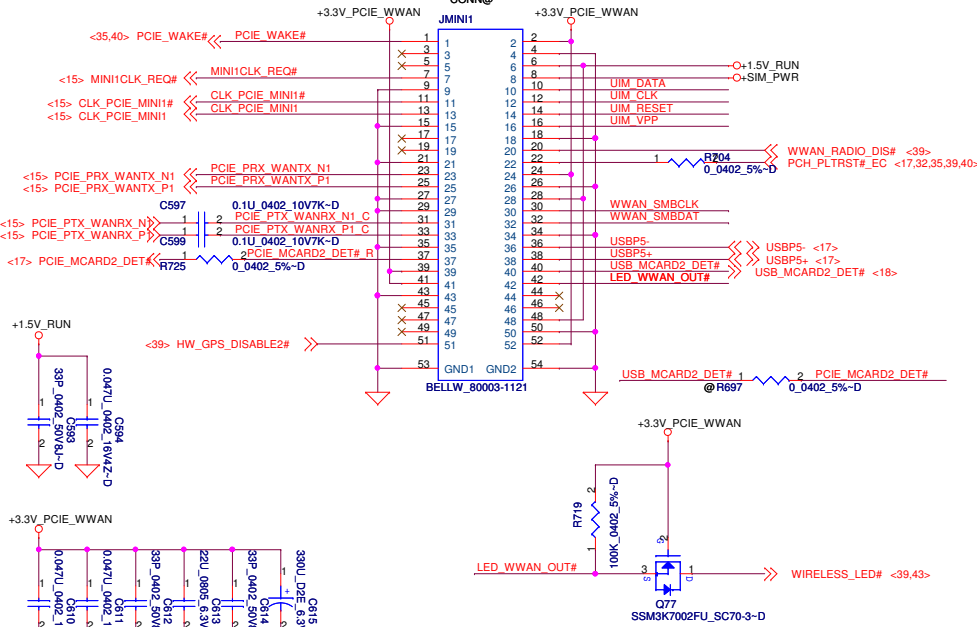
Compal Electronics, Inc.

Title			
Card Reader			
LA-7731P			
Size	Document Number	Rev	0.3
Date:	Thursday, September 01, 2011	Sheet	33 of 59

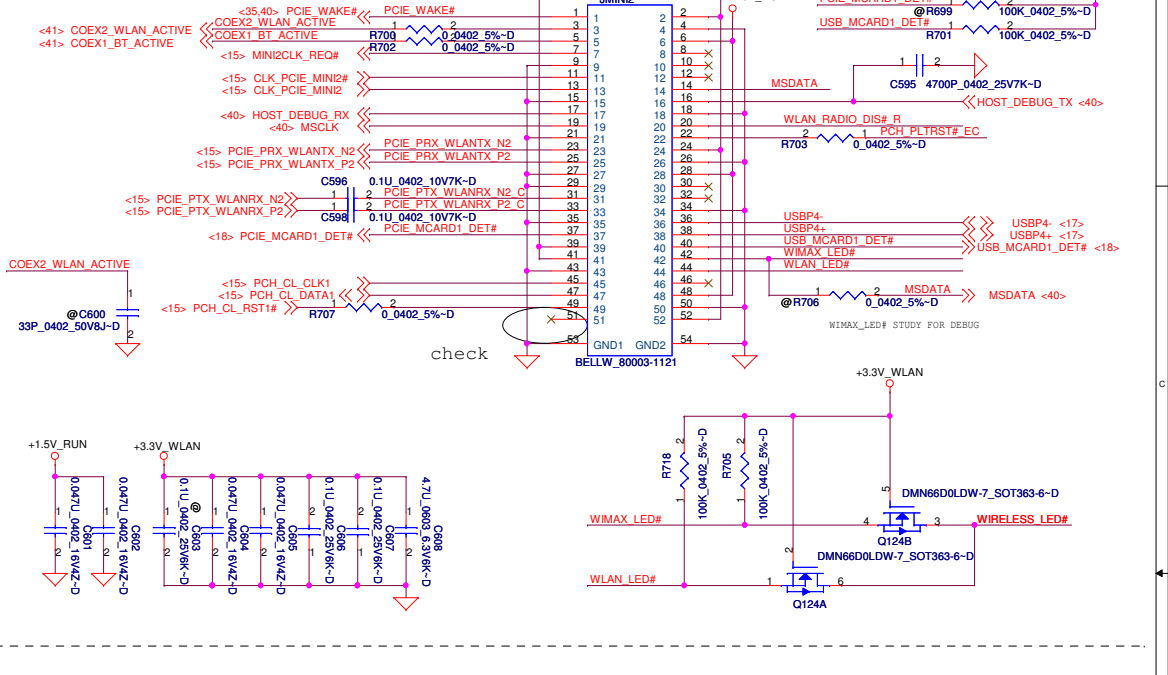
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**Mini WWAN/GPS/LTE/UWB H=5.2**

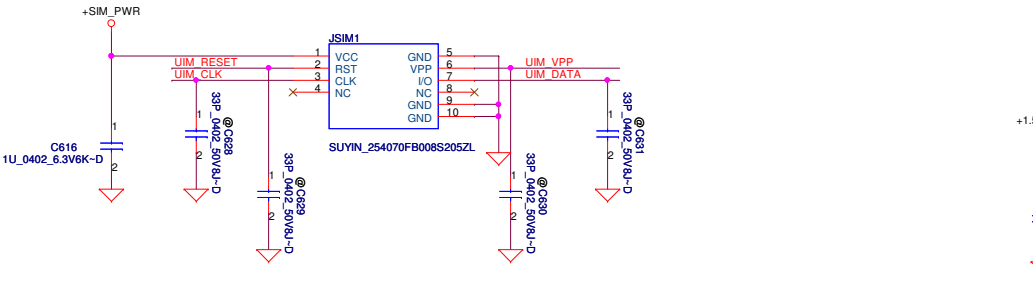


**Mini WLAN/WIMAX H=4**

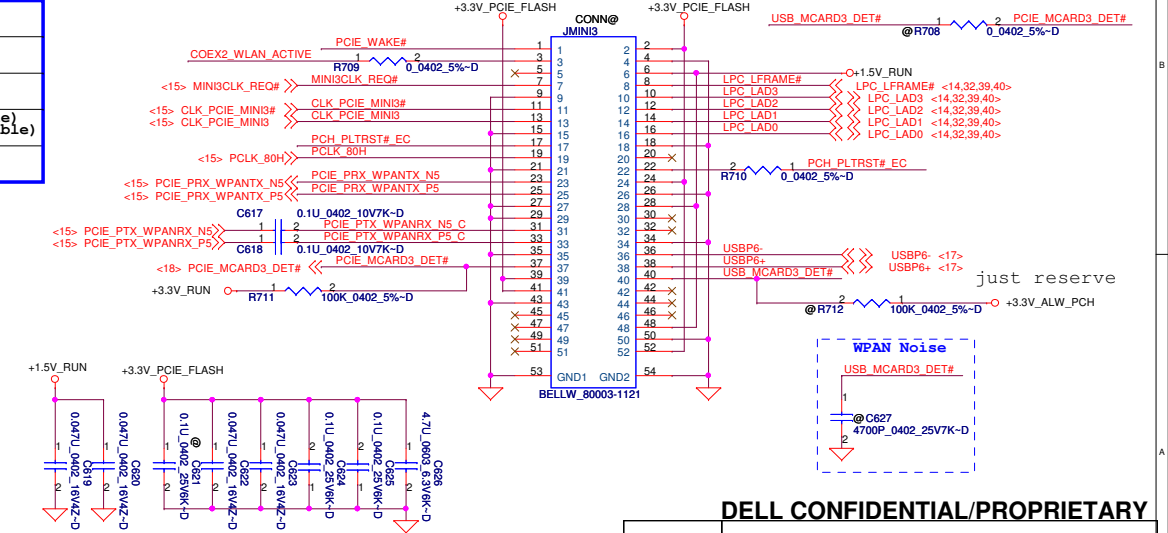


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250 (Wake enable) 5 (Not wake enable)	
+1.5V	+5%	500	375	NA

**SIM Card Push-Push**



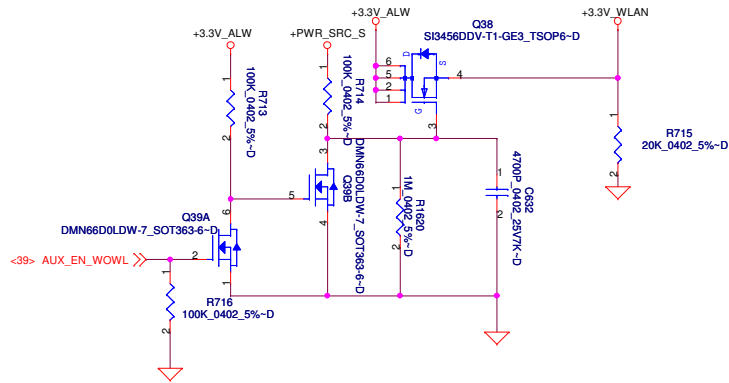
**1/2 Minicard Flash Card H=4**



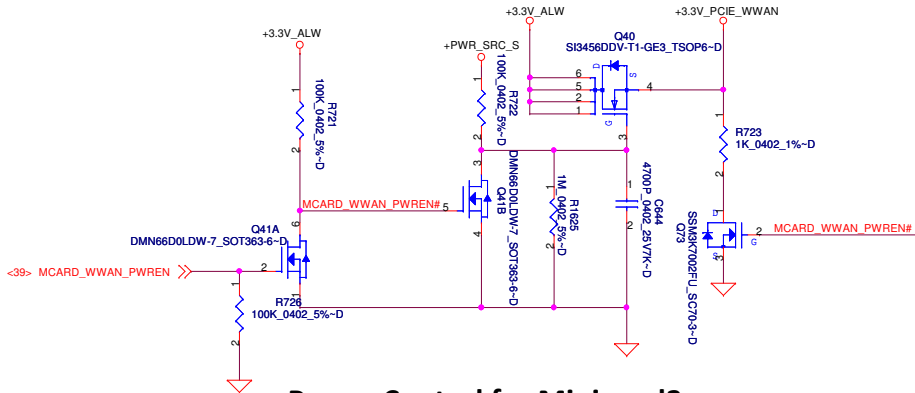
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**Mini Card**  
**LA-7731P**  
 Date: Thursday, September 01, 2011 Sheet 34 of 59

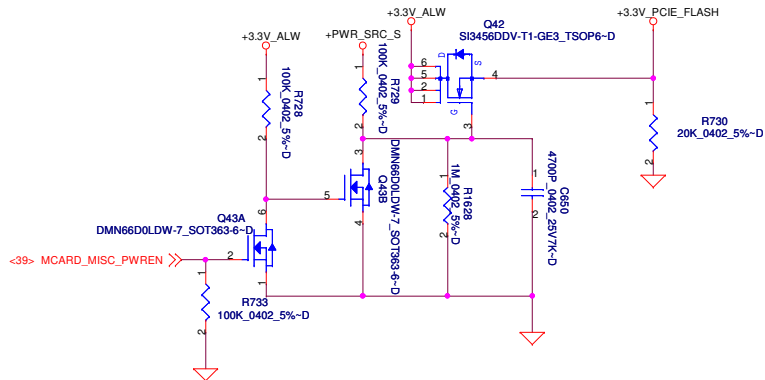
### Power Control for Mini card1



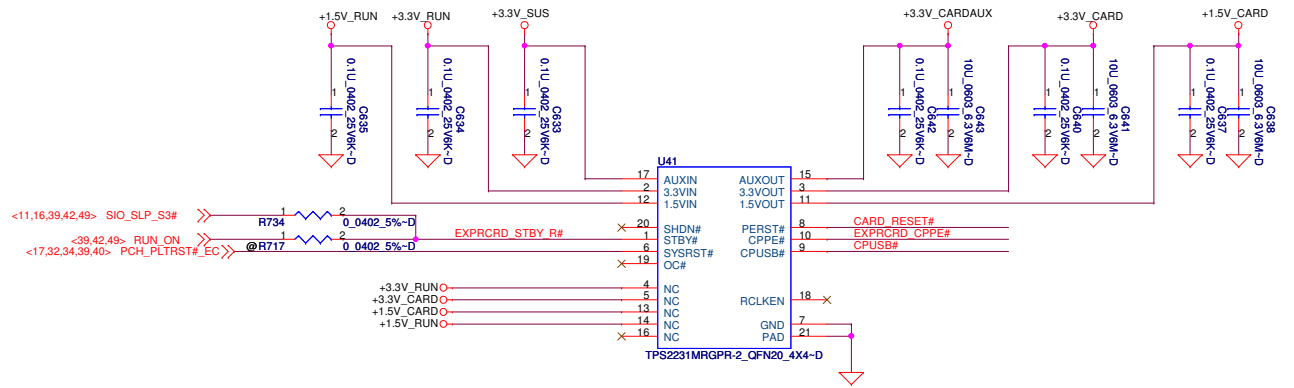
### Power Control for Mini card2



### Power Control for Mini card3

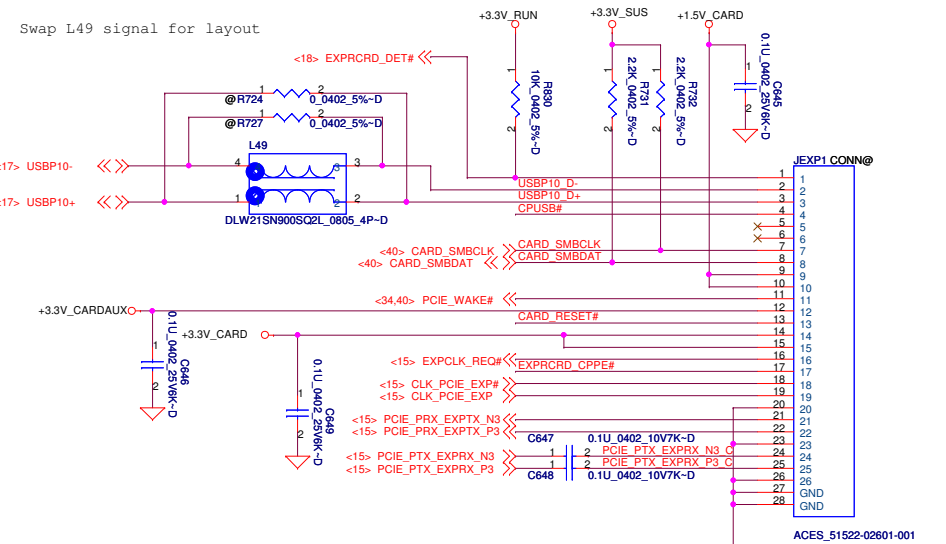


### Express Card PWR S/W



[Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part]

### Express Card Conn.

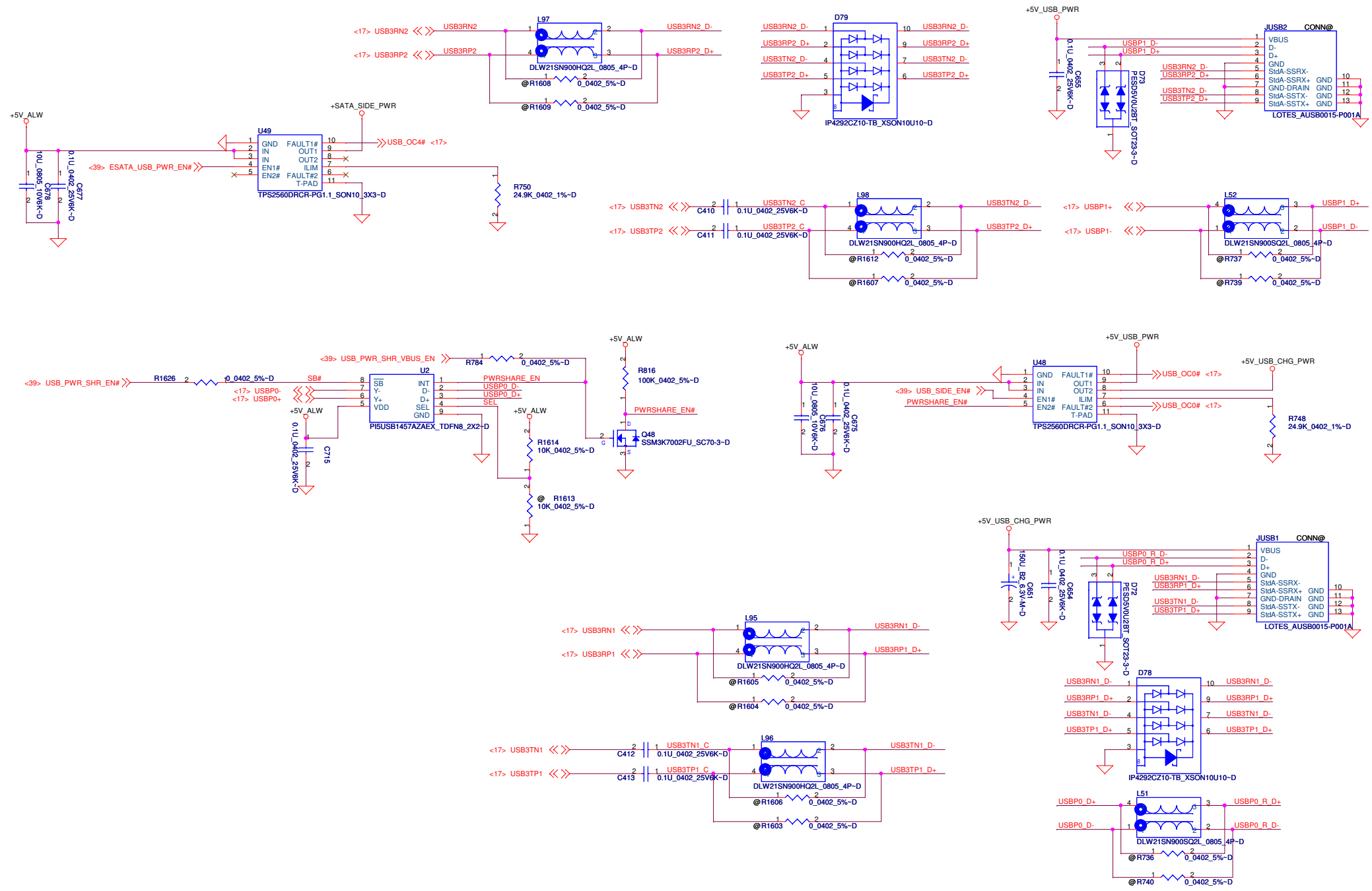


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Title			
PCIE-SATA SW / PCIE PWR			
Size	Document Number	Rev	
	LA-7731P	0.3	
Date:	Thursday, September 01, 2011	Sheet	35 of 59

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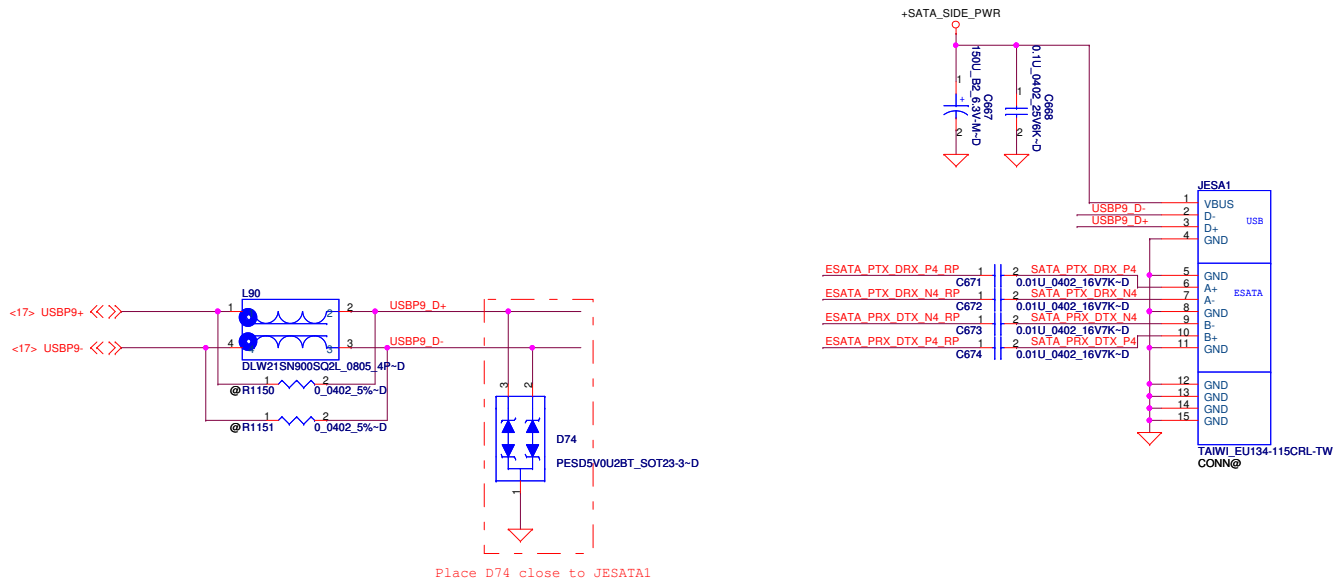
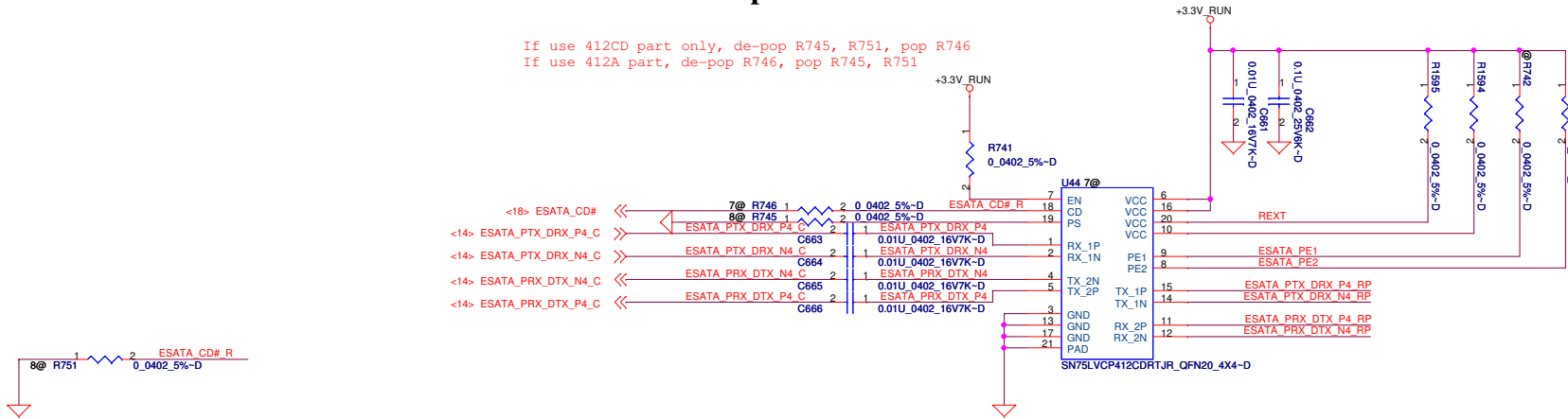
<b>Compal Electronics, Inc.</b>			
<b>USB 3.0 x2</b>			
Size	Document Number	Rev	
	<b>LA-7731P</b>	0.3	
Date:	Thursday, September 01, 2011	Sheet	36 of 59

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# ESATA Repeater

8@ U44  
 PS8513BTQFN20GTR-A0  
 SA00004WR00

If use 412CD part only, de-pop R745, R751, pop R746  
 If use 412A part, de-pop R746, pop R745, R751



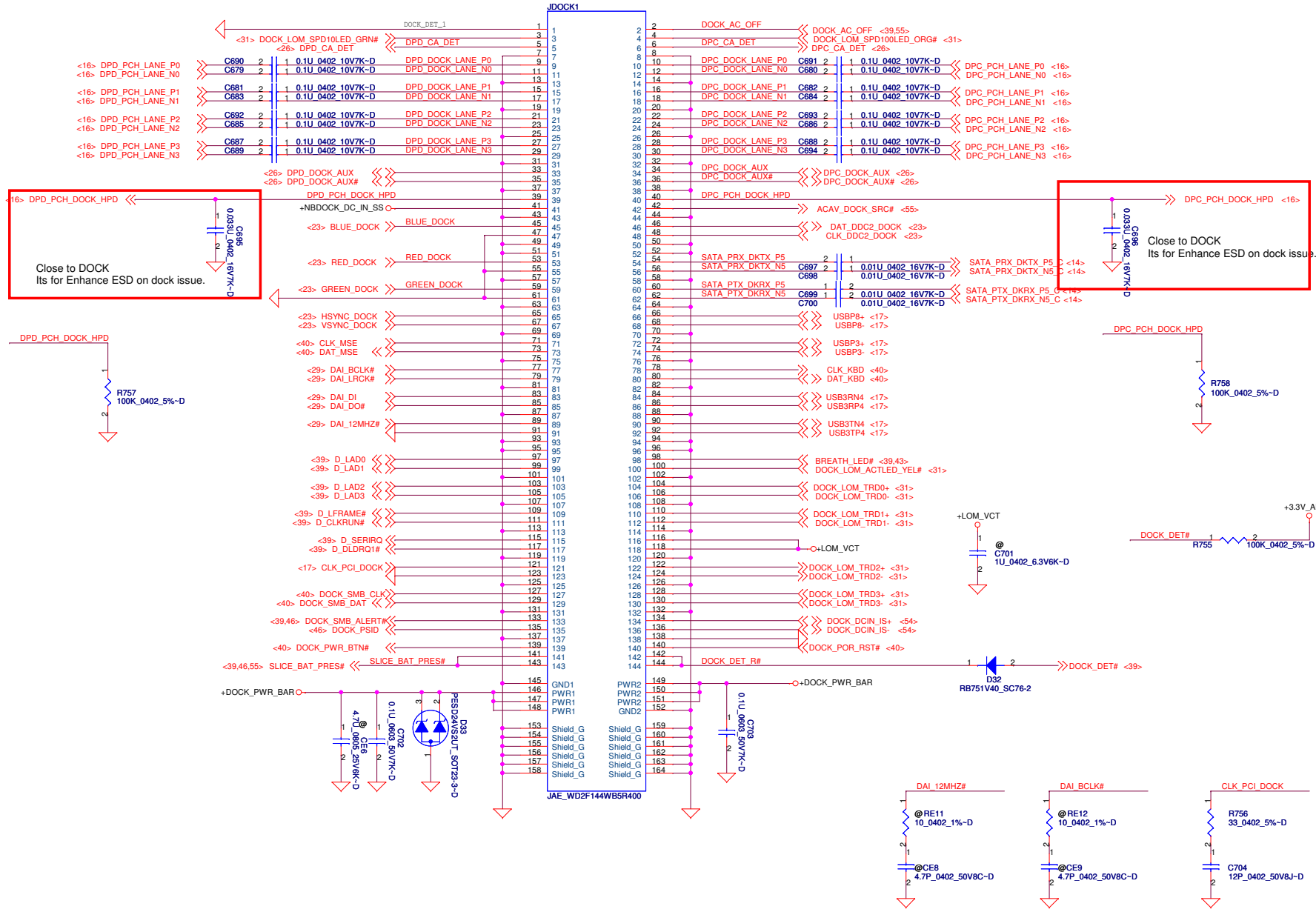
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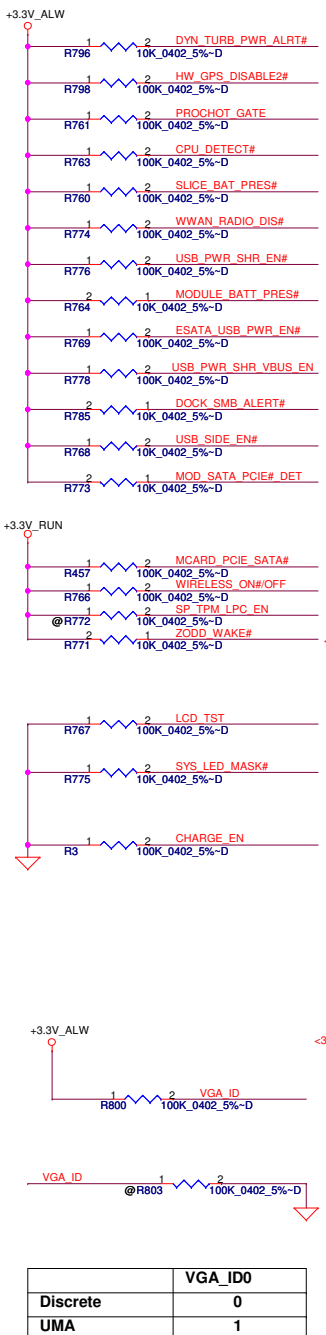
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Title			Rev
USB/ESATA/IO/MDC			0.3
Size	Document Number	Date	
	LA-7731P	Thursday, September 01, 2011	
		Sheet	37 of 59

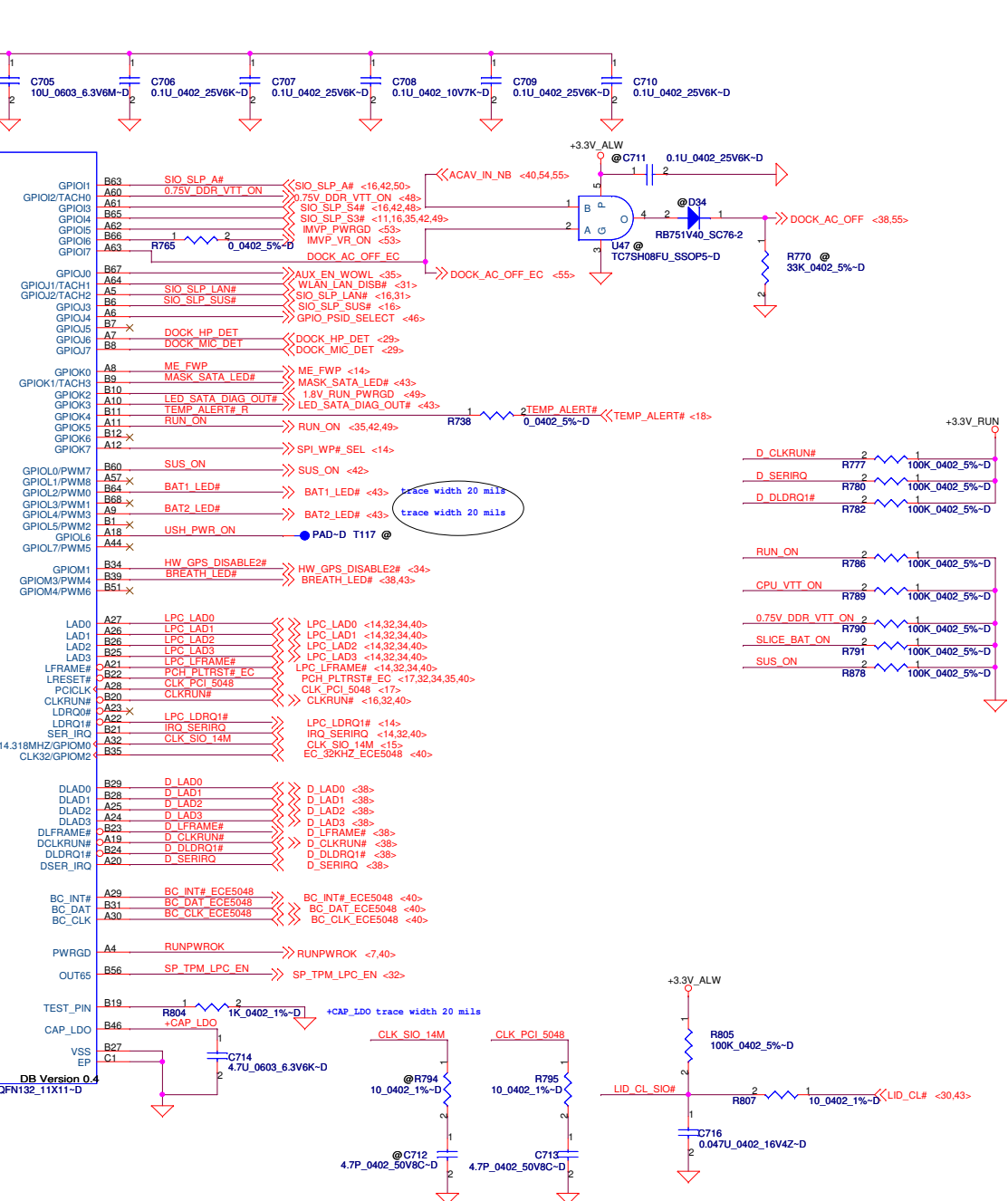
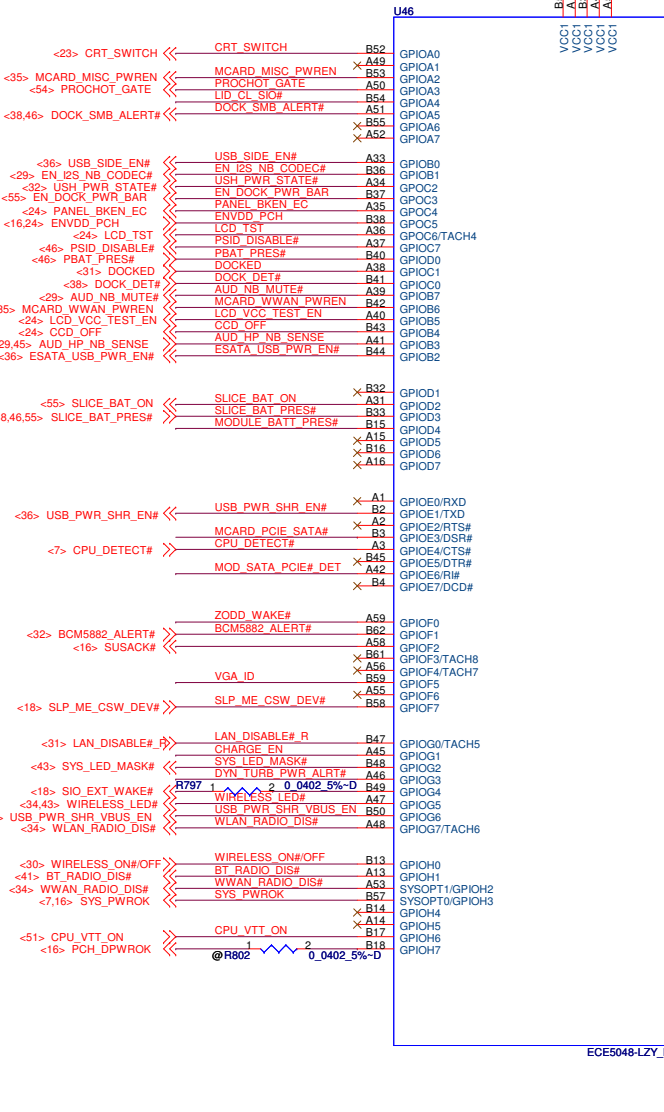


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<b>Compal Electronics, Inc.</b>			
<b>DOCKING CONN</b>			
<b>LA-7731P</b>			
Size	Document Number	Rev 0.3	
Date:	Thursday, September 01, 2011	Sheet	38 of 59

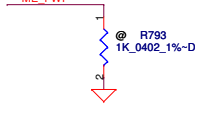


D12" does not support E-Module, ECE5048(U46) pin B7,A15,B15,A16,B32,A42,A49 not used, but do not assign GPIO for these pins.



	VGA_ID0
Discrete	0
UMA	1

ME\_FWP PCH has internal 20K PD. (suspend power rail)



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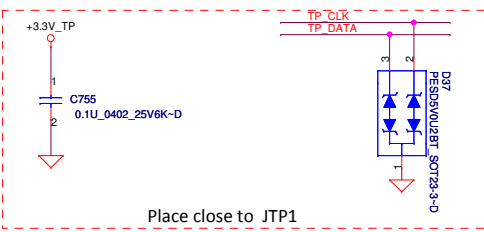


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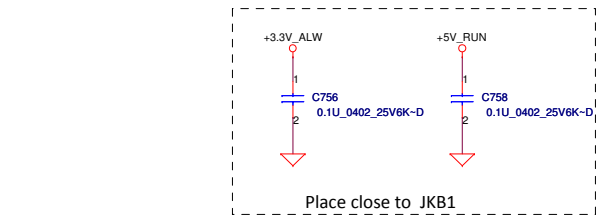
Compal Electronics, Inc.		
Title <b>ECE5048</b>		
Size	Document Number <b>LA-7731P</b>	Rev <b>0.3</b>
Date:	Thursday, September 01, 2011	Sheet 39 of 59



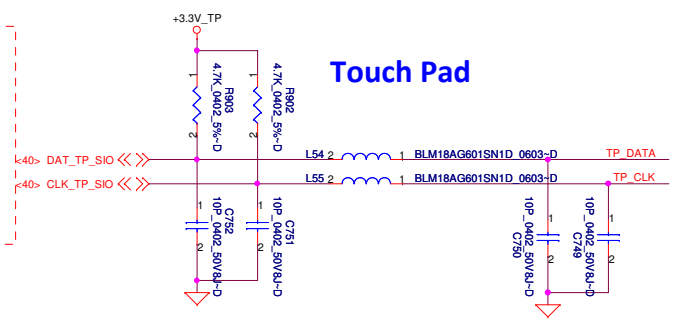




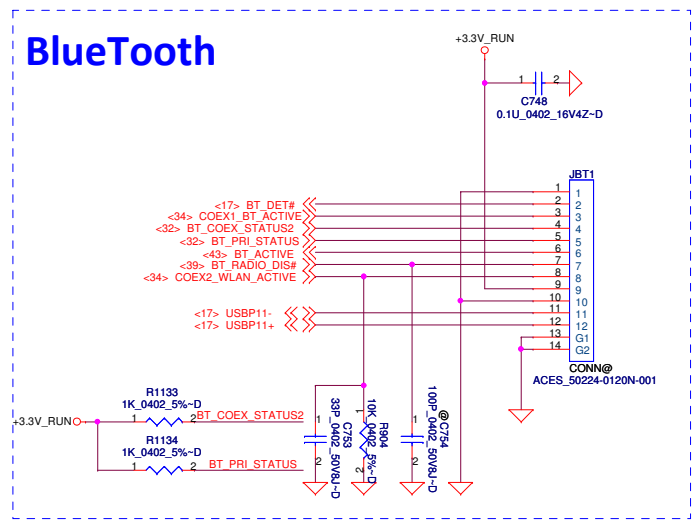
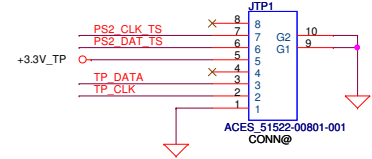
D37 ESD ask to change to SOT23-3



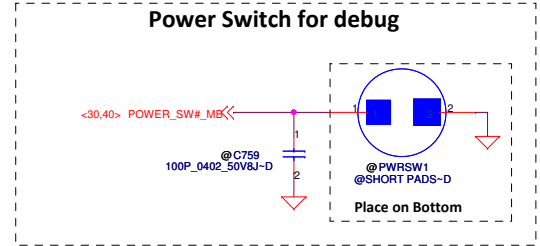
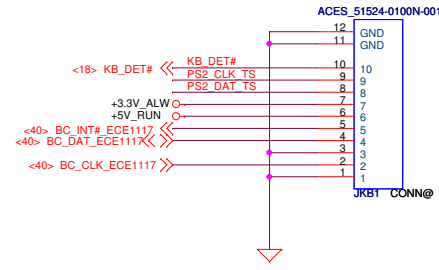
Place close to JKB1



### Touch Pad

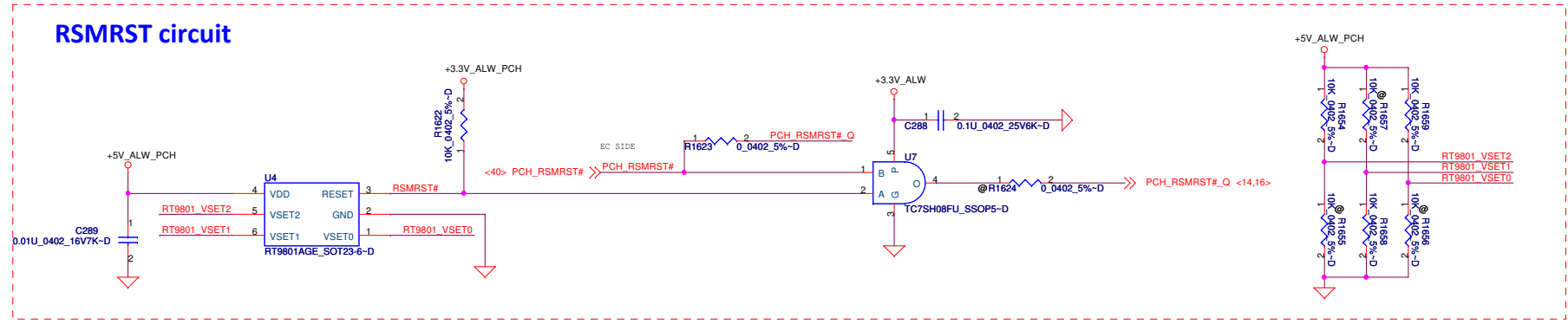


### BlueTooth



### Power Switch for debug

Place on Bottom



### RSMRST circuit



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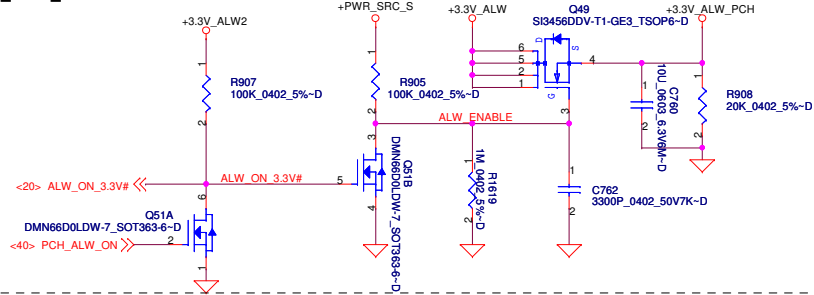
Touch PAD/Int KB/BT

LA-7731P

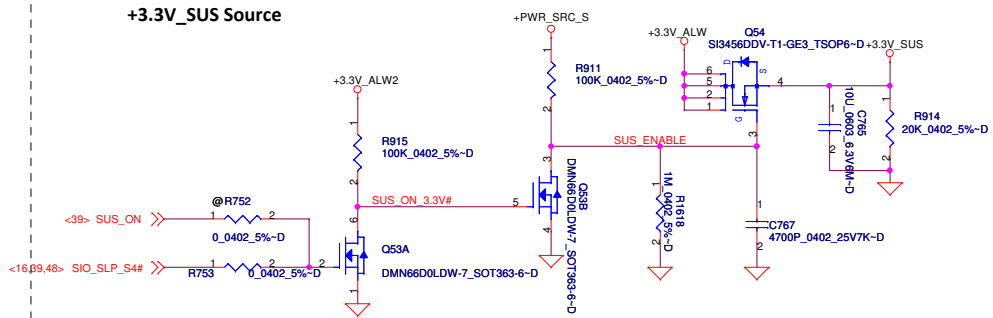
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Size	Document Number	Rev
	LA-7731P	0.3
Date:	Thursday, September 01, 2011	Sheet 41 of 59

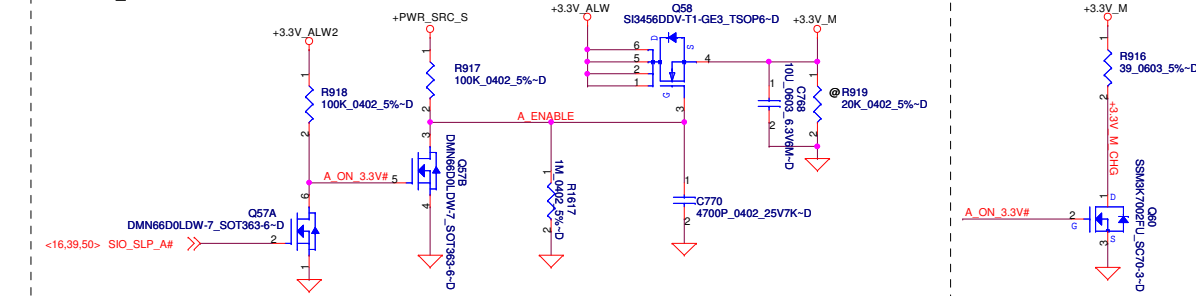
### +3.3V\_ALW\_PCH Source



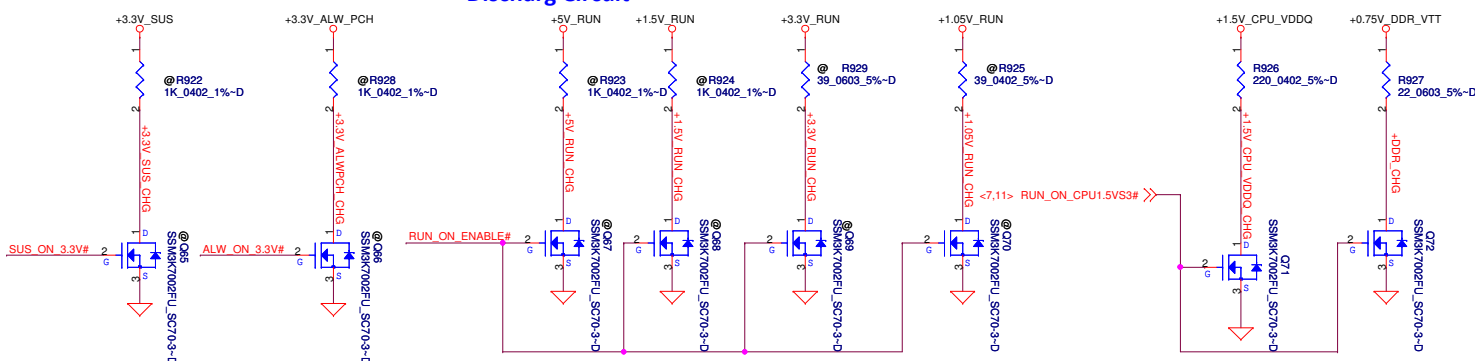
### +3.3V\_SUS Source



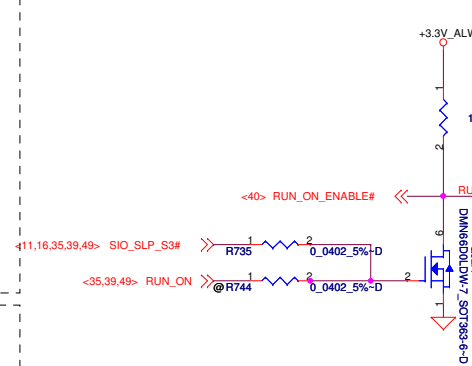
### +3.3V\_M Source



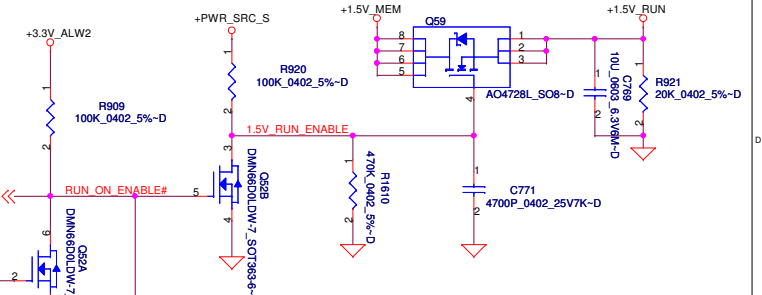
### Discharg Circuit



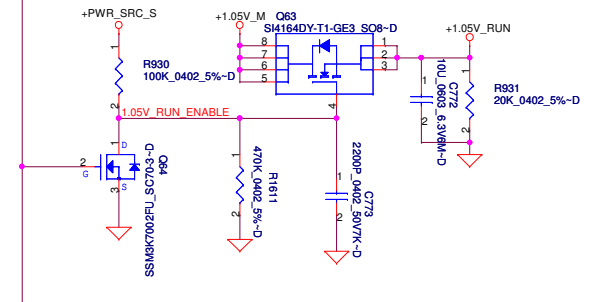
### DC/DC Interface



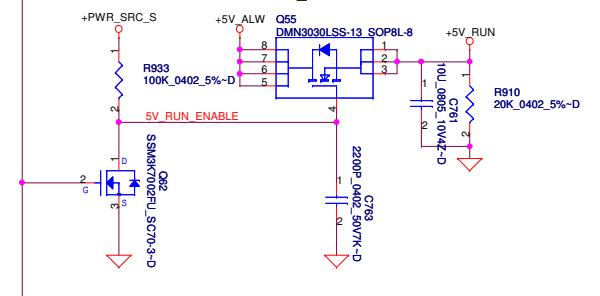
### +1.5V\_RUN Source



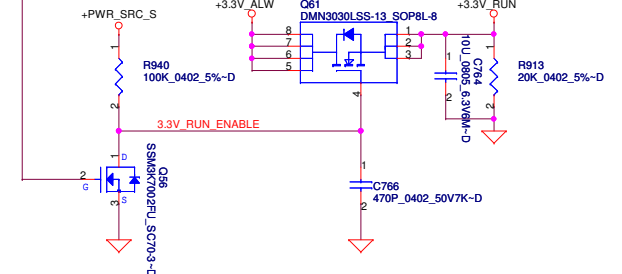
### +1.05V\_RUN Source



### +5V\_RUN Source



### +3.3V\_RUN Source

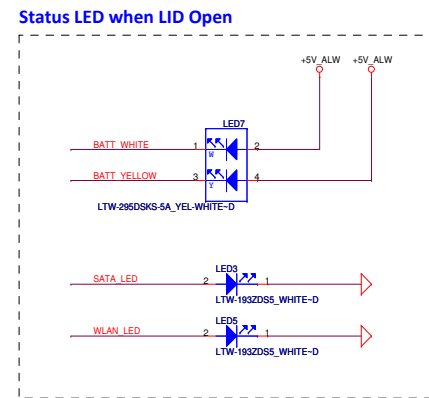
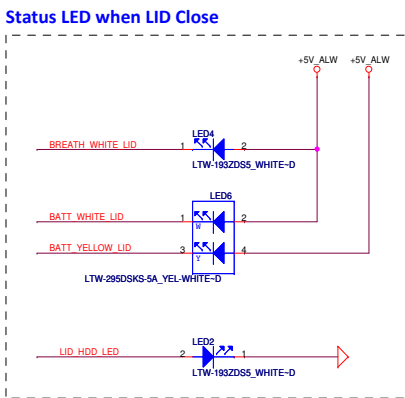
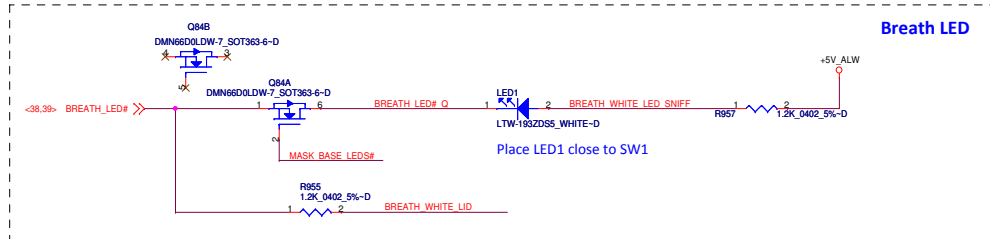
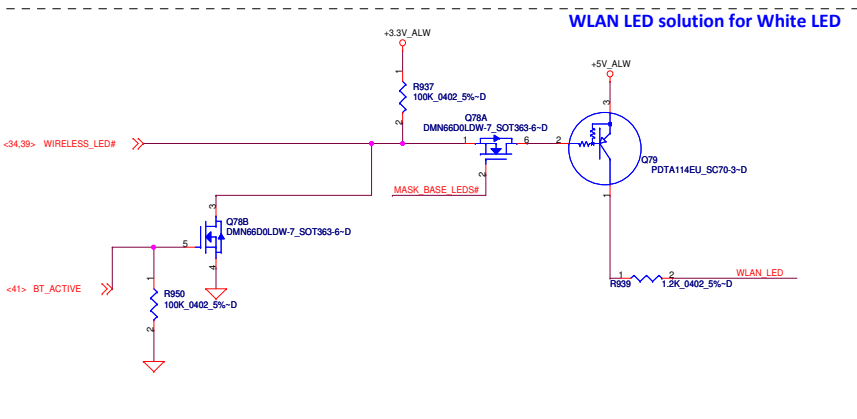
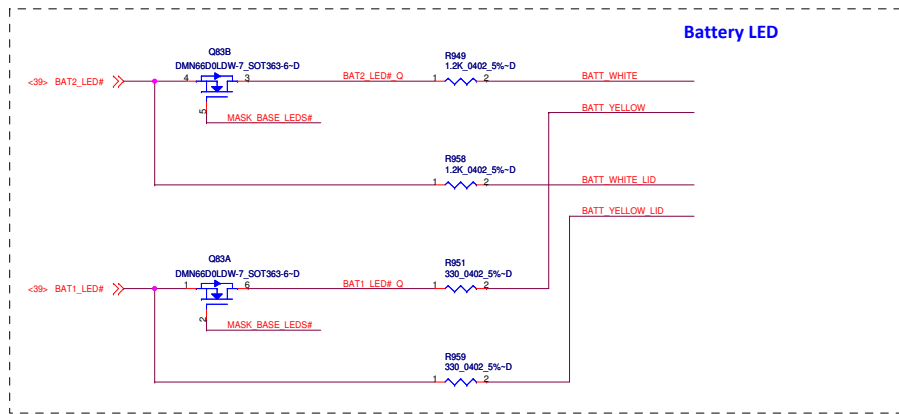
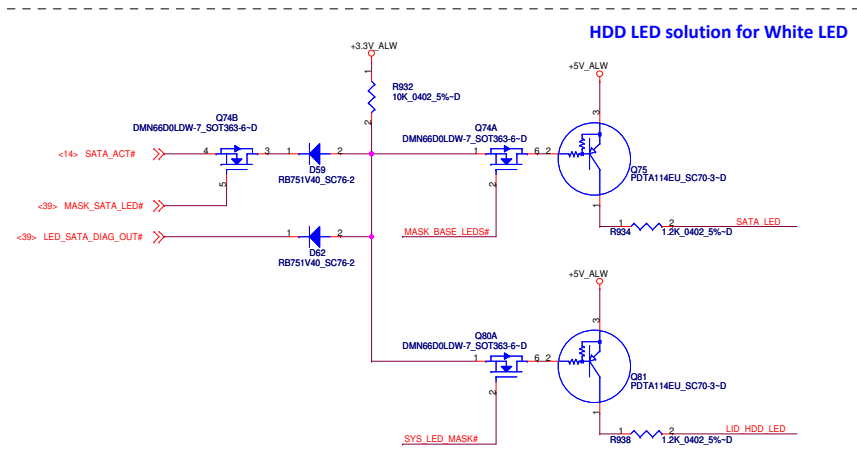


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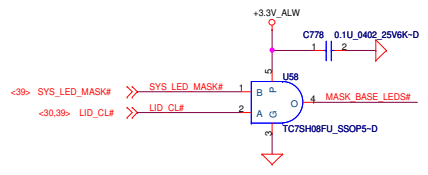
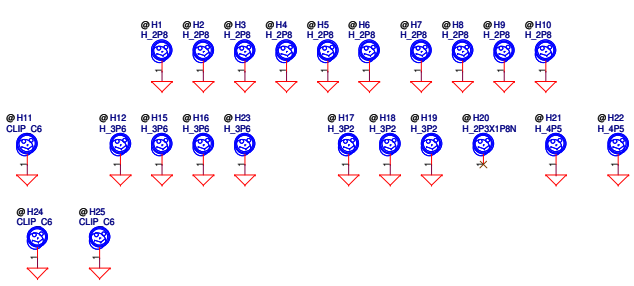
Title			Rev 0.3
POWER CONTROL			
Size	Document Number	LA-7731P	
Date:	Thursday, September 01, 2011	Sheet 42 of 59	

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	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

- Fiducial Mark**
- ⊙ FD1 FIDUCIAL MARK-D
  - ⊙ FD2 FIDUCIAL MARK-D
  - ⊙ FD3 FIDUCIAL MARK-D
  - ⊙ FD4 FIDUCIAL MARK-D



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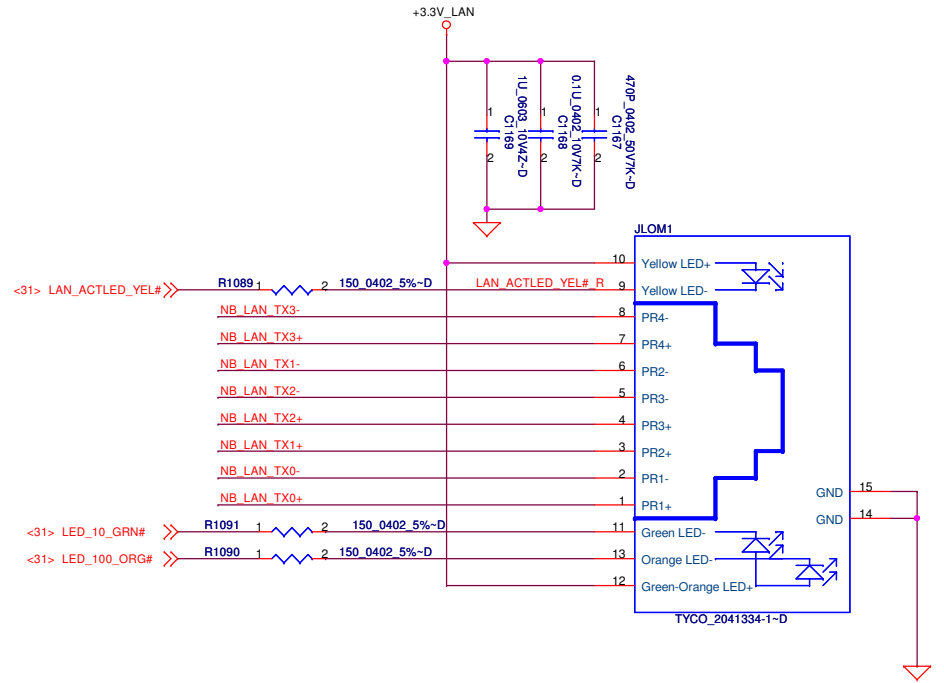
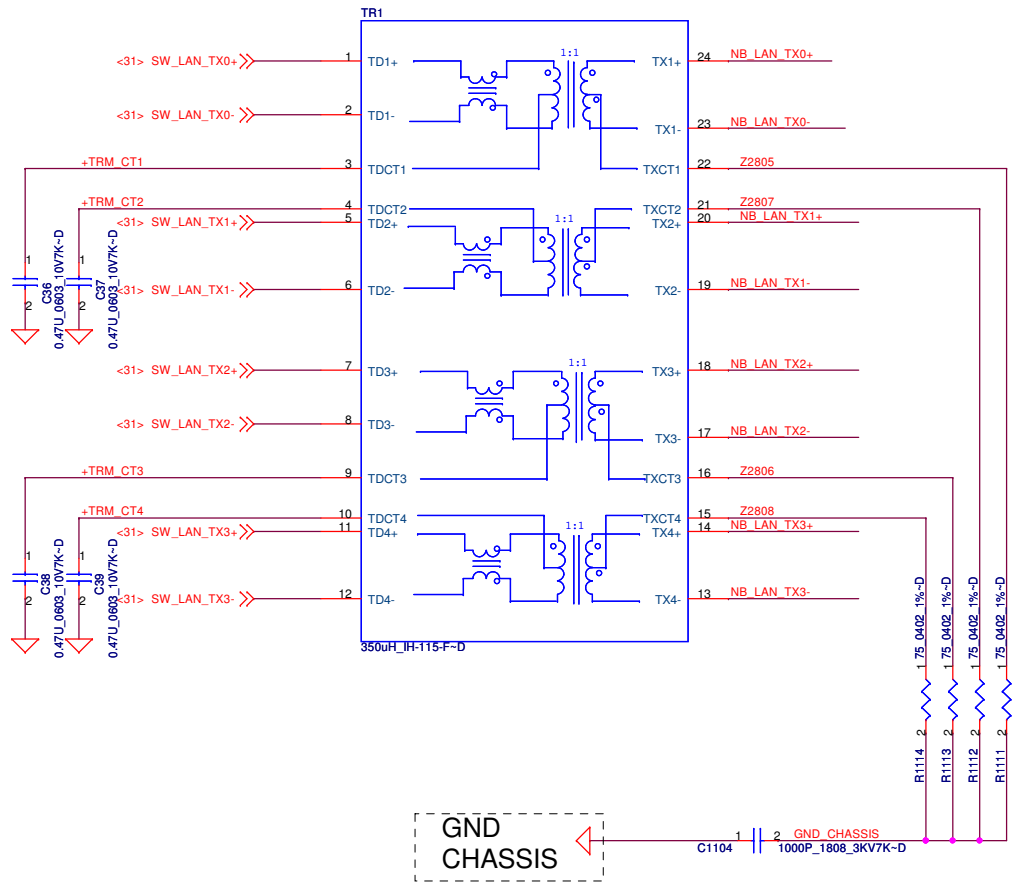
**Compal Electronics, Inc.**

**PAD and Standoff**

Document Number: **LA-7731P**

Size: **LA-7731P**

Date: Thursday, September 01, 2011 Sheet 43 of 59



GND CHASSIS

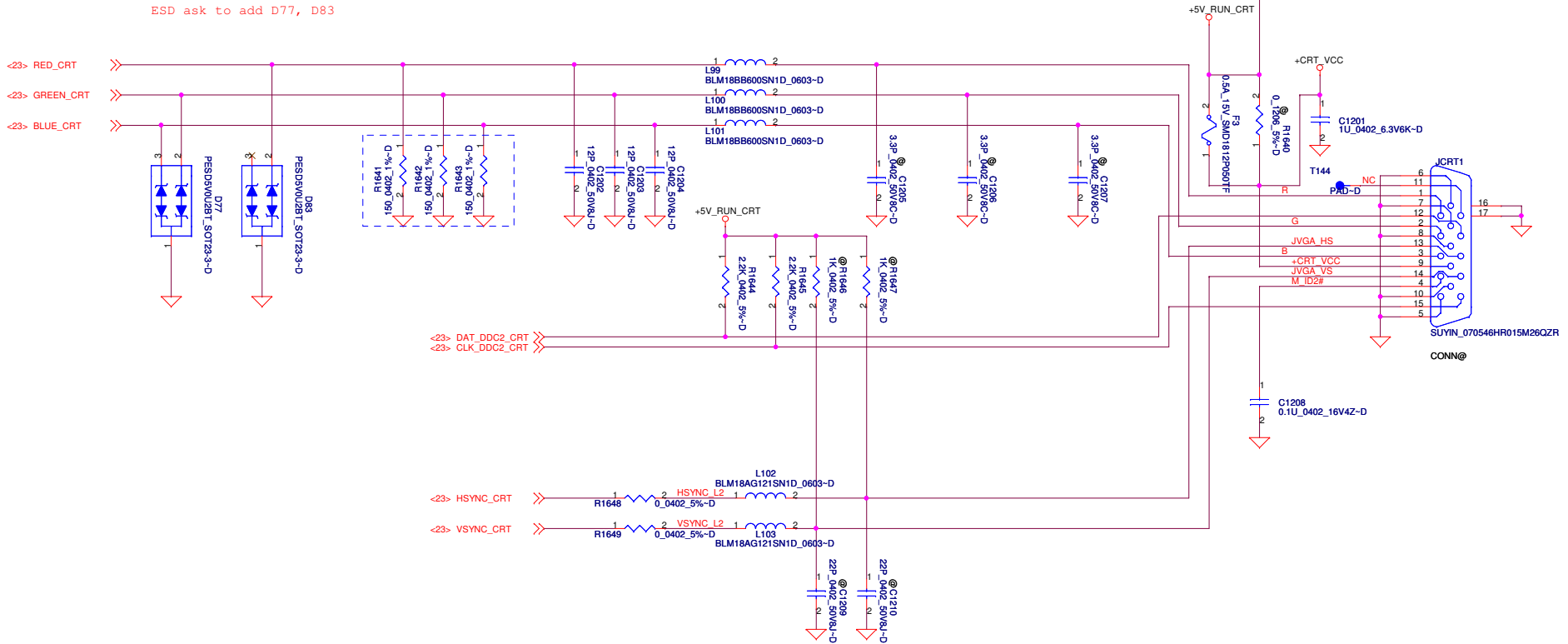
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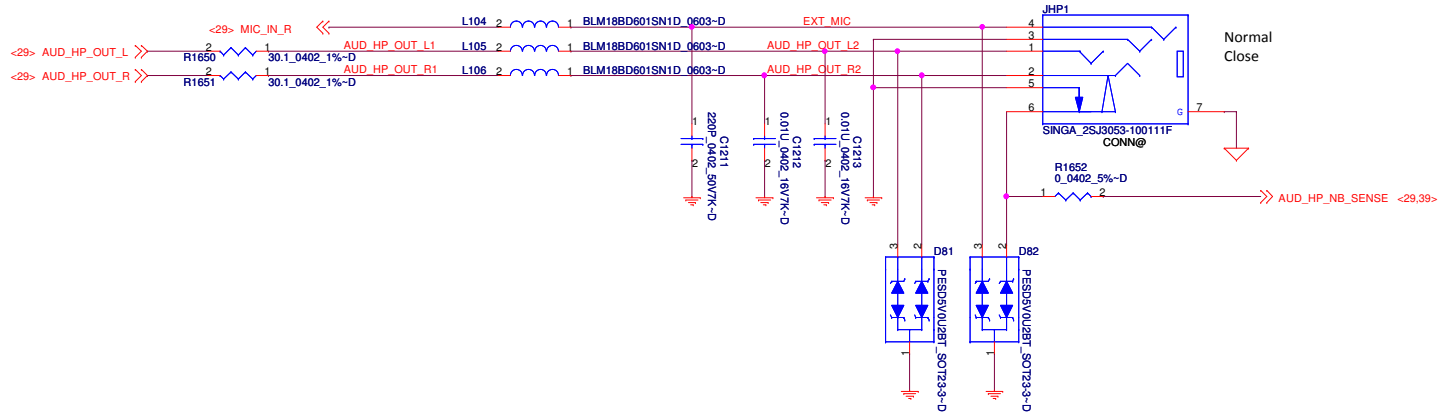
Compal Electronics, Inc.



Title		RJ45	
Size	Document Number	LA-7731P	
Date:	Thursday, September 01, 2011	Sheet	44 of 59
		Rev	0.3

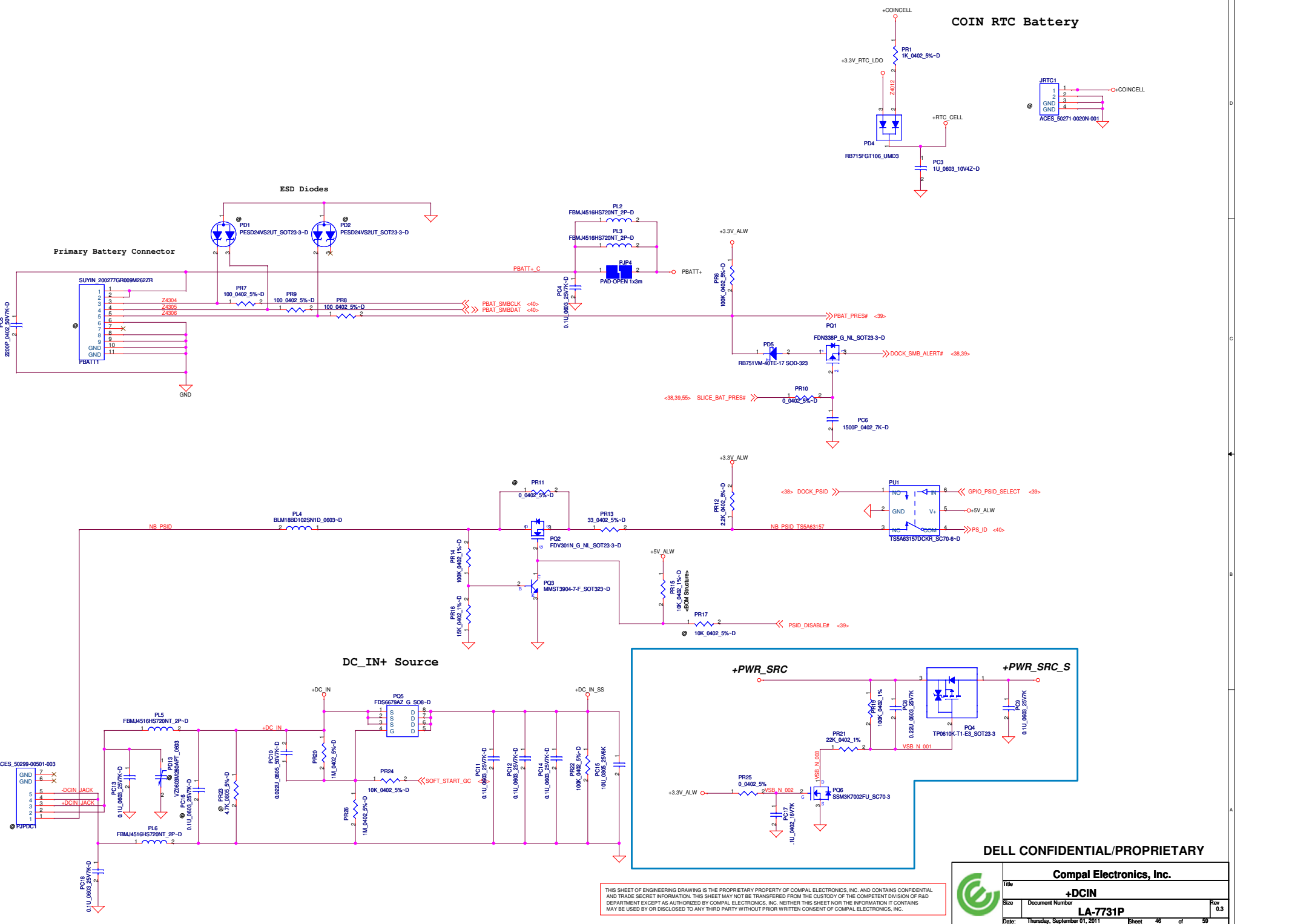


### Combo Jack

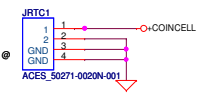


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		<b>Compal Electronics, Inc.</b>		
		<b>CRT &amp; Combo Jack</b>		
Title	LA-7731P		Rev	0.3
Size	Document Number	Date: Friday, September 02, 2011		Sheet 45 of 59



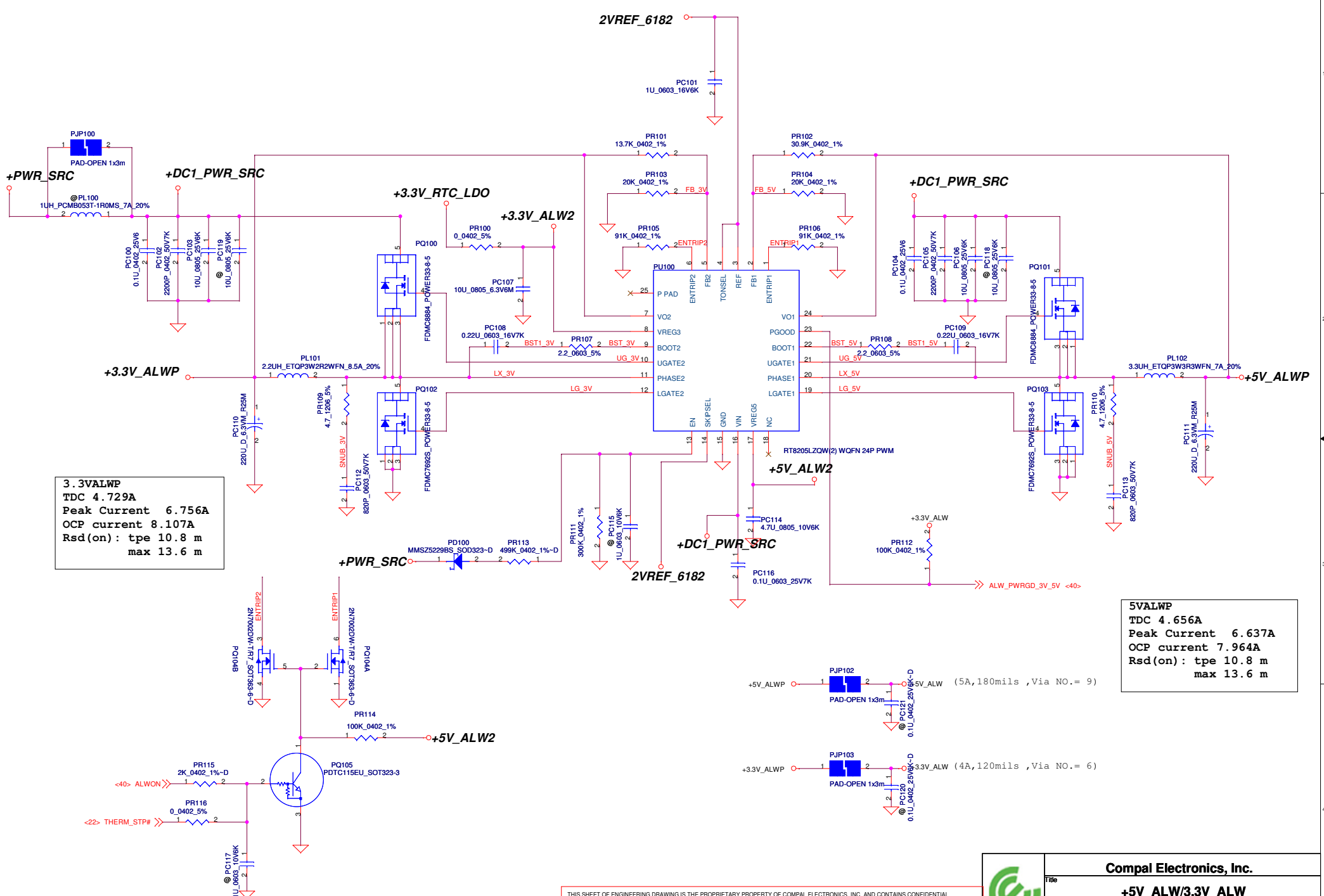
**COIN RTC Battery**



**DELL CONFIDENTIAL/PROPRIETARY**

		<b>Compal Electronics, Inc.</b>	
		<b>+DCIN</b>	
Size	Document Number	<b>LA-7731P</b>	
Date	Thursday, September 01, 2011	Sheet	46 of 59

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**3.3VALWP**  
 TDC 4.729A  
 Peak Current 6.756A  
 OCP current 8.107A  
 Rsd(on): tpe 10.8 m  
 max 13.6 m

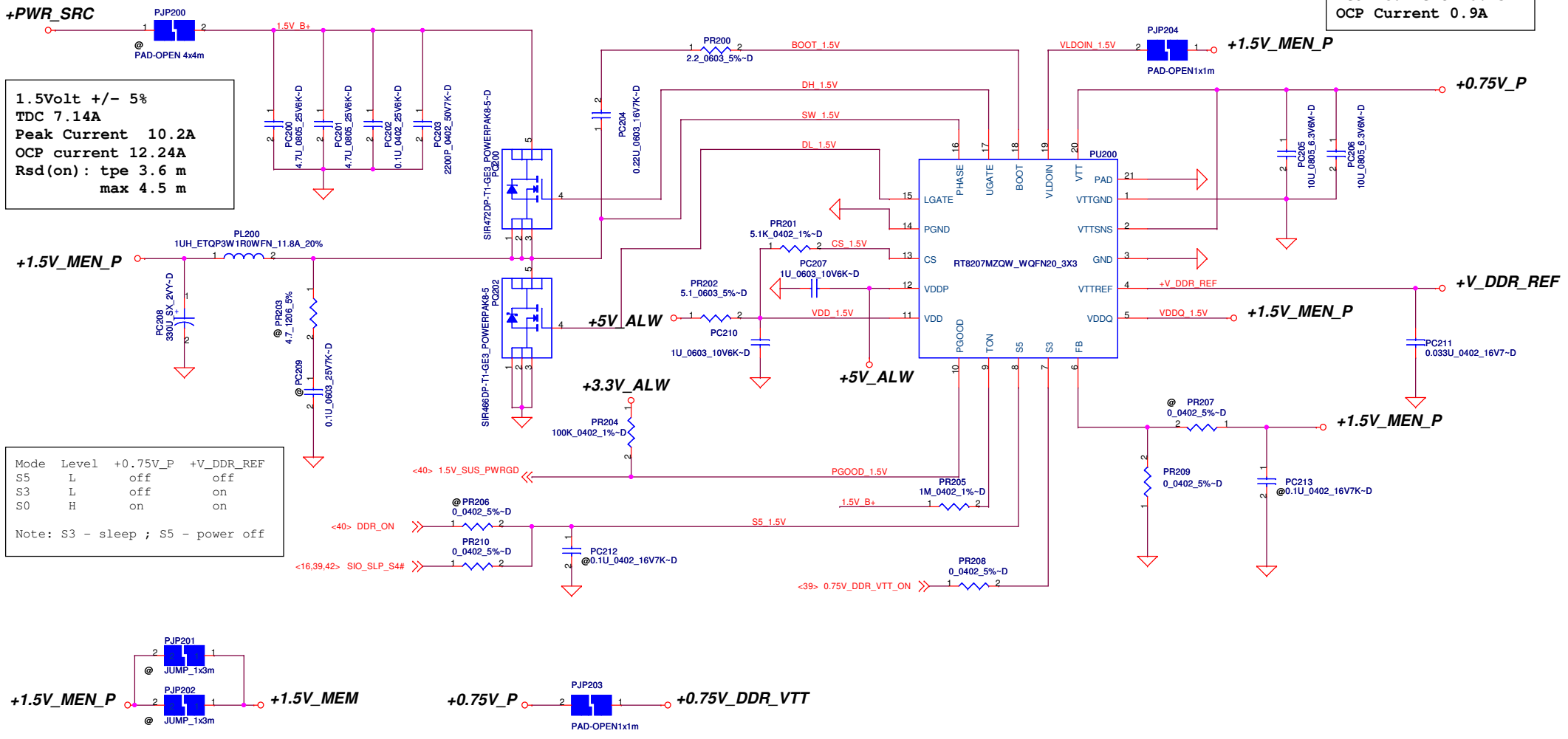
**5VALWP**  
 TDC 4.656A  
 Peak Current 6.637A  
 OCP current 7.964A  
 Rsd(on): tpe 10.8 m  
 max 13.6 m

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<b>Compal Electronics, Inc.</b>			
<b>+5V_ALW/3.3V_ALW</b>			
Title			
Size	Document Number	Rev	
	<b>LA-7731P</b>	<b>0.3</b>	
Date:	Thursday, September 01, 2011	Sheet	47 of 59

0.75Volt +/- 5%  
 TDC 0.525A  
 Peak Current 0.75A  
 OCP Current 0.9A



1.5Volt +/- 5%  
 TDC 7.14A  
 Peak Current 10.2A  
 OCP current 12.24A  
 Rsd(on) : tpe 3.6 m  
 max 4.5 m

Mode	Level	+0.75V_P	+V_DDR_REF
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

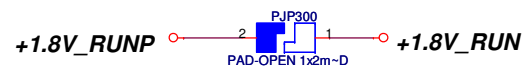
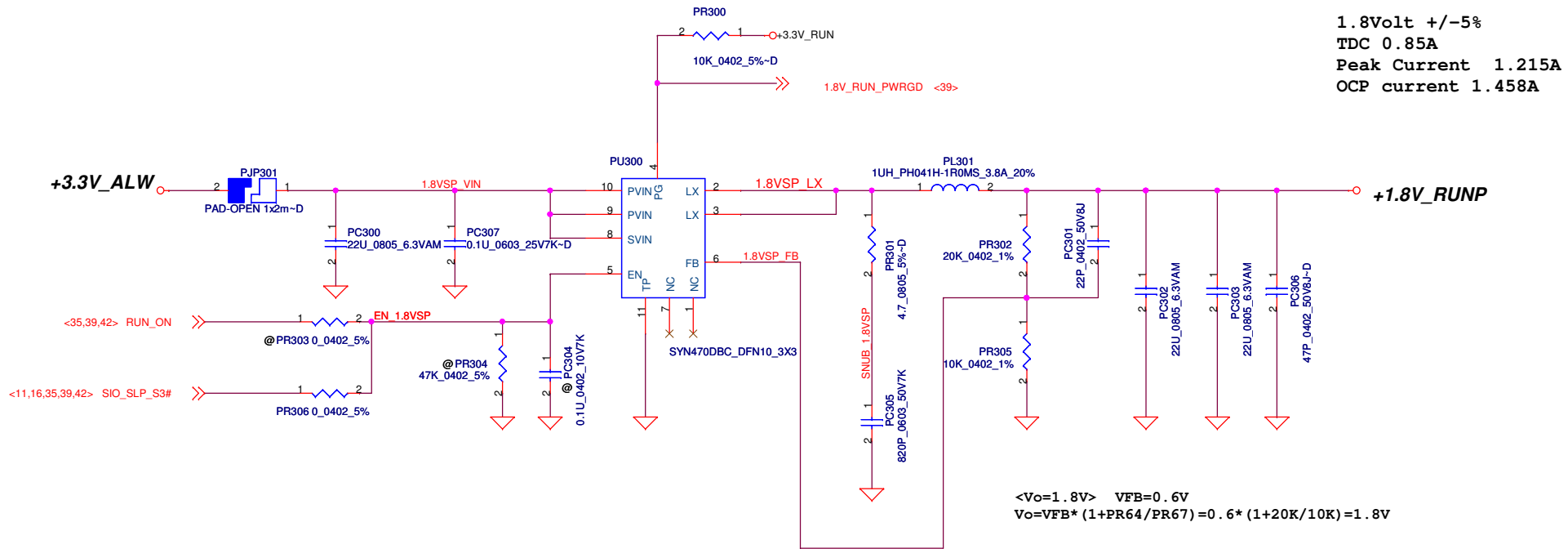
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Compal Electronics, Inc.		
Title	+1.5V_MEN/+0.75V_DDR_VTT	
Size	Document Number	Rev
	LA-7731P	0.3
Date:	Thursday, September 01, 2011	Sheet 48 of 59

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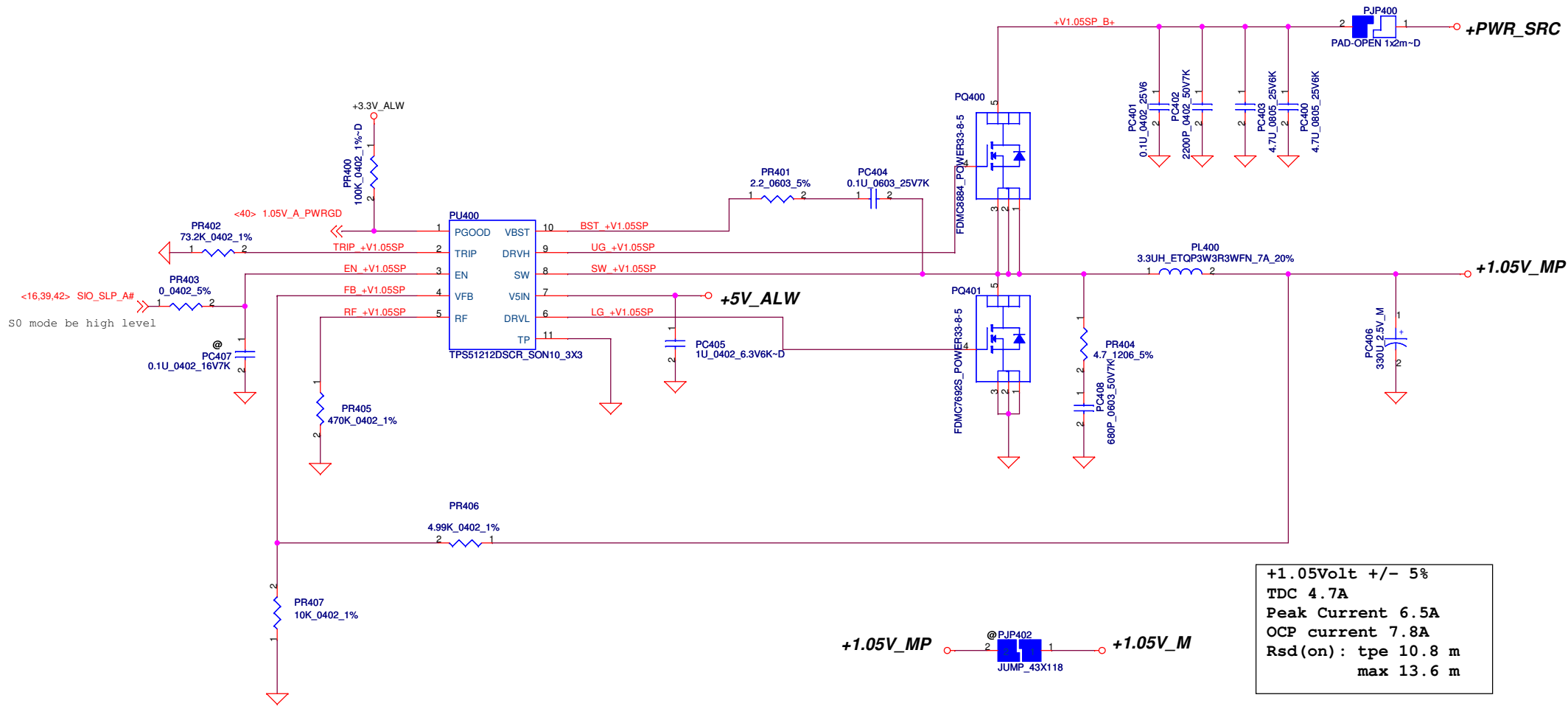




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<b>Compal Electronics, Inc.</b>		
<b>+1.8V_RUN</b>		
Size	Document Number	Rev
	<b>LA-7731P</b>	<b>0.3</b>
Date:	Thursday, September 01, 2011	Sheet 49 of 59

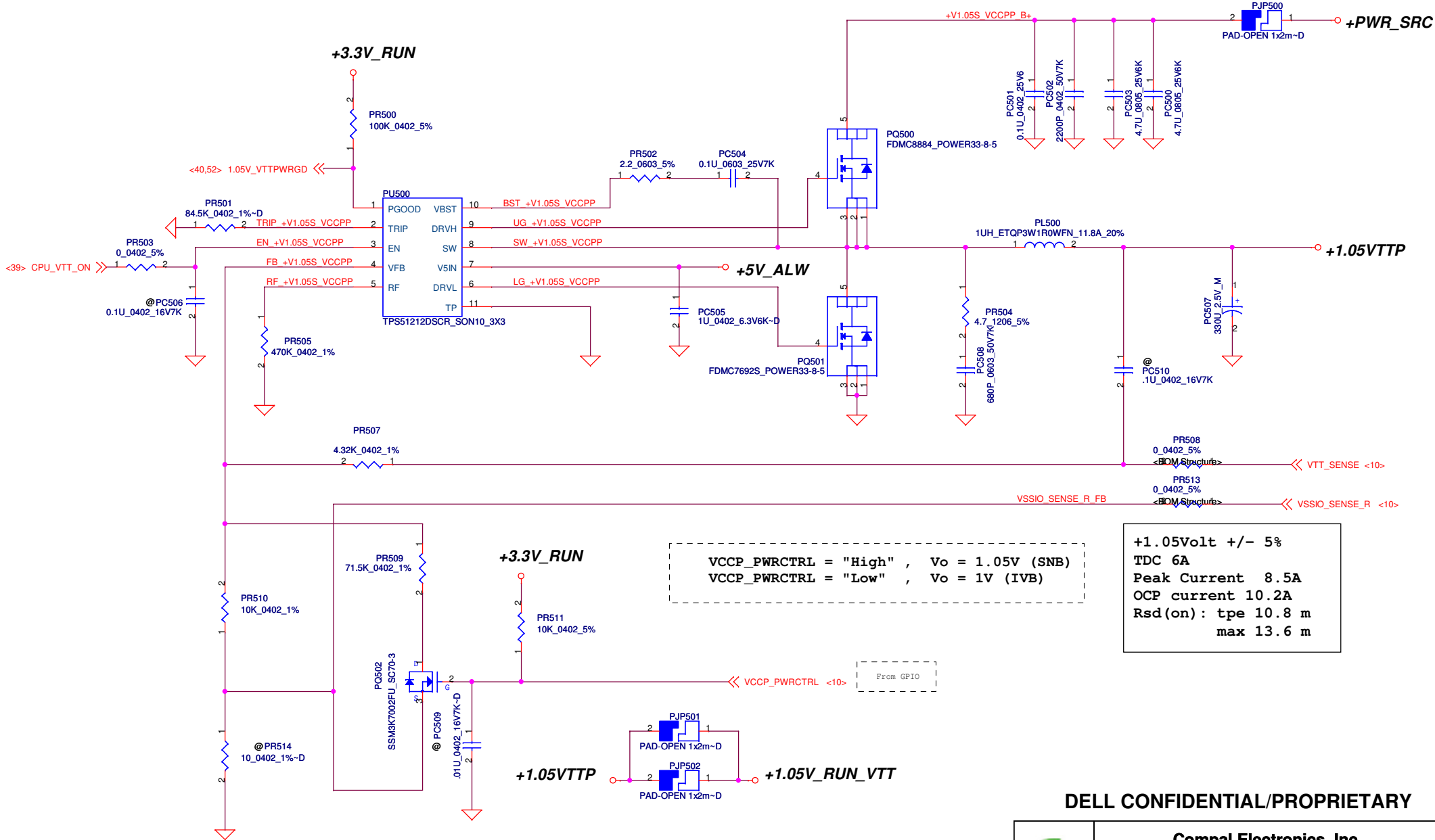


+1.05Volt +/- 5%  
 TDC 4.7A  
 Peak Current 6.5A  
 OCP current 7.8A  
 Rsd(on): tpe 10.8 m  
 max 13.6 m

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			<b>Compal Electronics, Inc.</b>	
			<b>+1.05V_M</b>	
Size	Document Number			Rev
		<b>LA-7731P</b>		0.3
Date:	Thursday, September 01, 2011	Sheet	50	of 59




VCCP\_PWRCTRL = "High" , Vo = 1.05V (SNB)  
 VCCP\_PWRCTRL = "Low" , Vo = 1V (IVB)

+1.05Volt +/- 5%  
 TDC 6A  
 Peak Current 8.5A  
 OCP current 10.2A  
 Rsd(on): tpe 10.8 m  
 max 13.6 m

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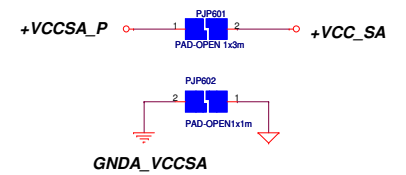
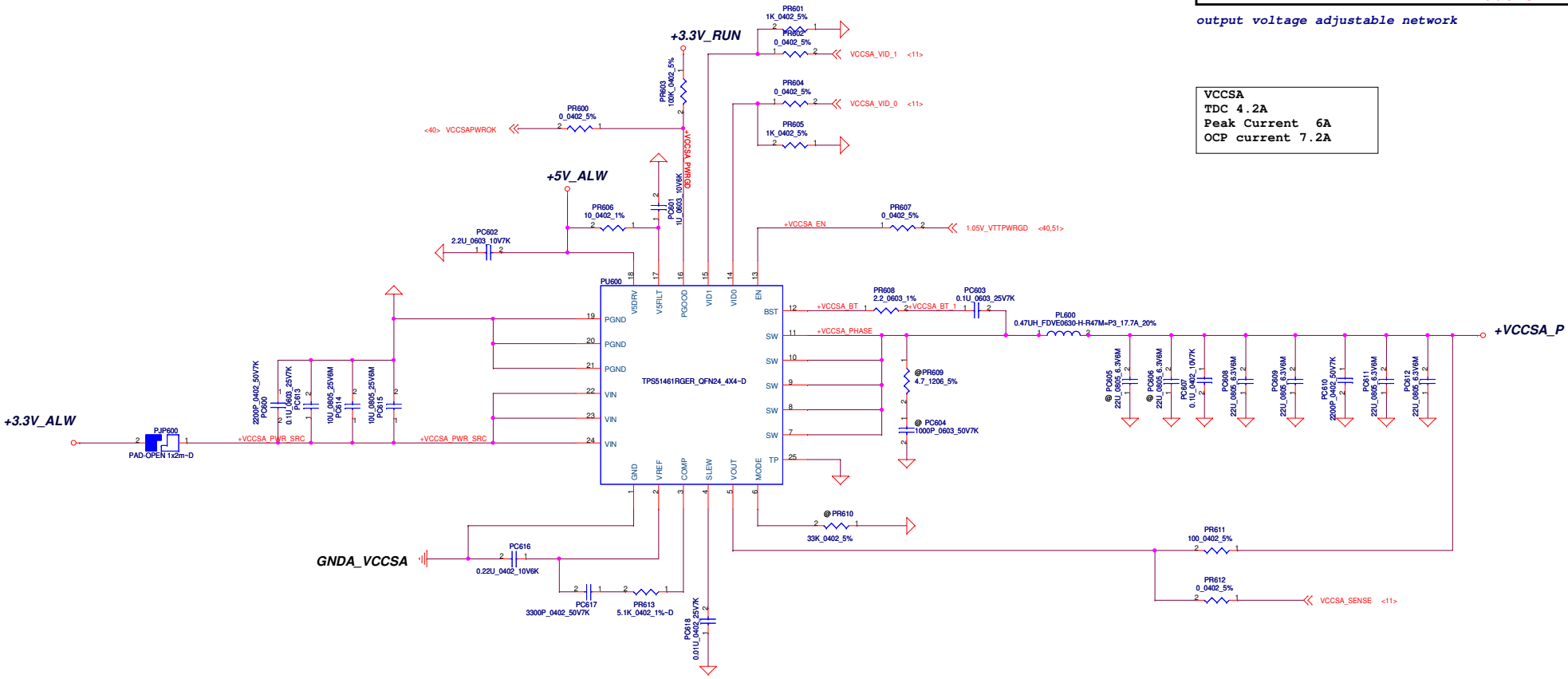
		<b>Compal Electronics, Inc.</b> Title <b>+1.05V_RUN_VTT</b>	
		Size <b>LA-7731P</b>	Rev <b>0.3</b>
Date: Thursday, September 01, 2011		Sheet 51 of 59	

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

The 1k PD on the VCCSA VIDs are empty.  
These should be stuffed to ensure that  
VCCSA VID is 00 prior to VCCIO stability.

output voltage adjustable network

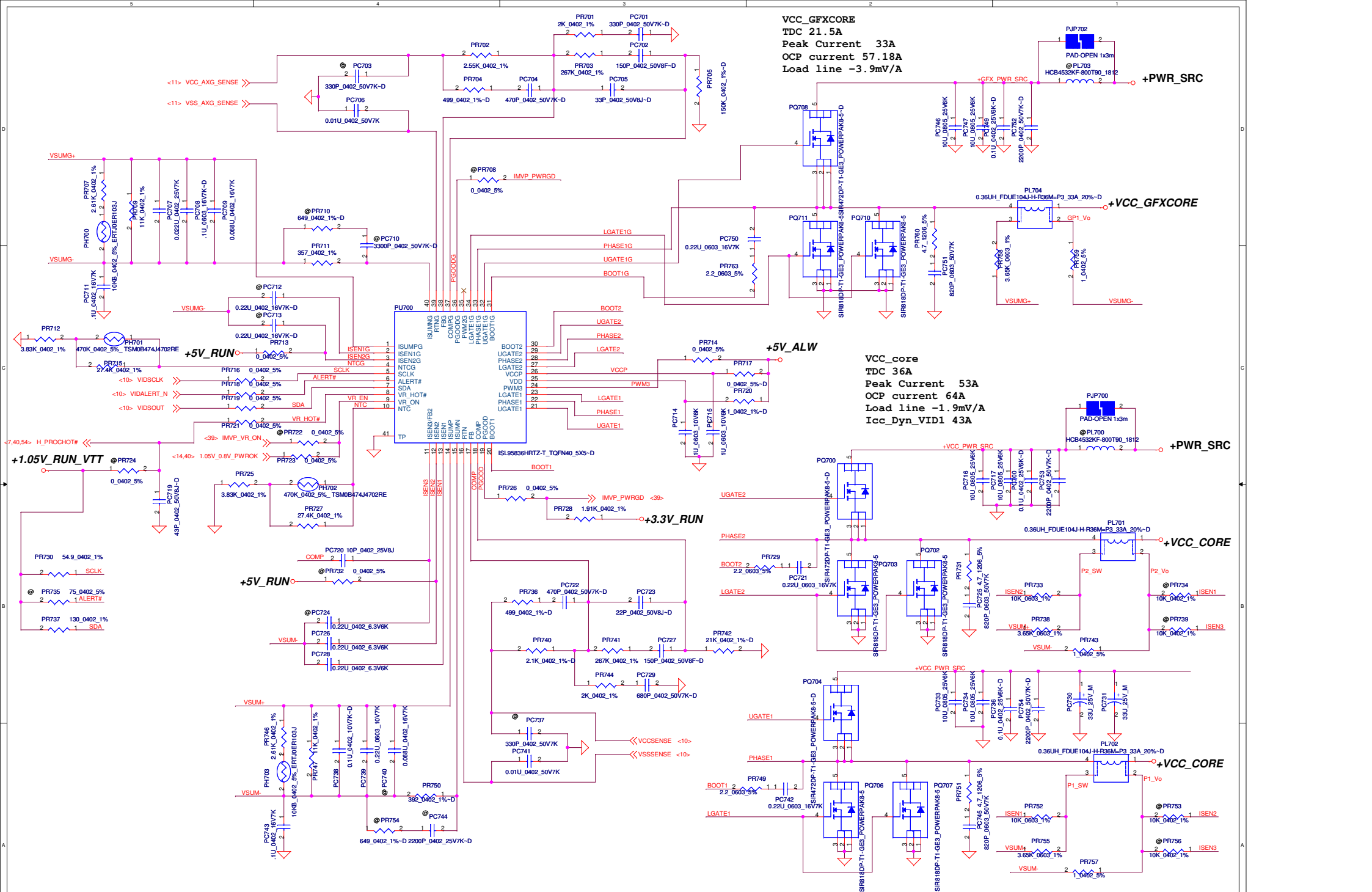
VCCSA  
TDC 4.2A  
Peak Current 6A  
OCP current 7.2A



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		<b>Compal Electronics, Inc.</b>	
		<b>+VCC SA</b>	
Size	Document Number	LA-7731P	Rev
Date	Thursday, September 01, 2011	Sheet 52	of 59

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**VCC\_GFXCORE**  
**TDC 21.5A**  
**Peak Current 33A**  
**OCp current 57.18A**  
**Load line -3.9mV/A**

**VCC\_core**  
**TDC 36A**  
**Peak Current 53A**  
**OCp current 64A**  
**Load line -1.9mV/A**  
**Icc\_Dyn\_VID1 43A**

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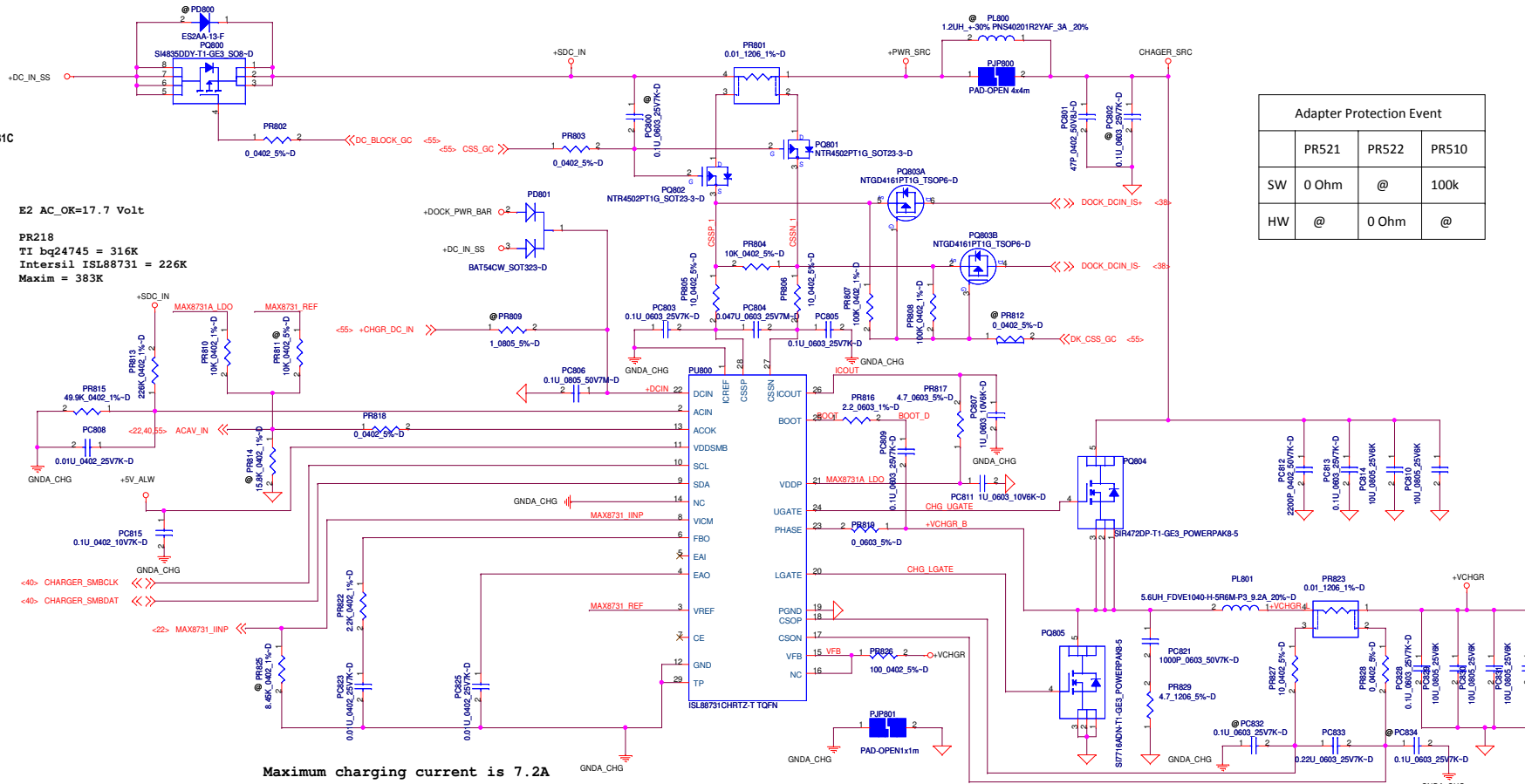
File	<b>+VCC_CORE</b>	
Size	Document Number	Rev
	<b>LA-7731P</b>	0.3
Date:	Thursday, September 01, 2011	Sheet 33 of 59

ISL88731C

E2 AC\_OK=17.7 Volt

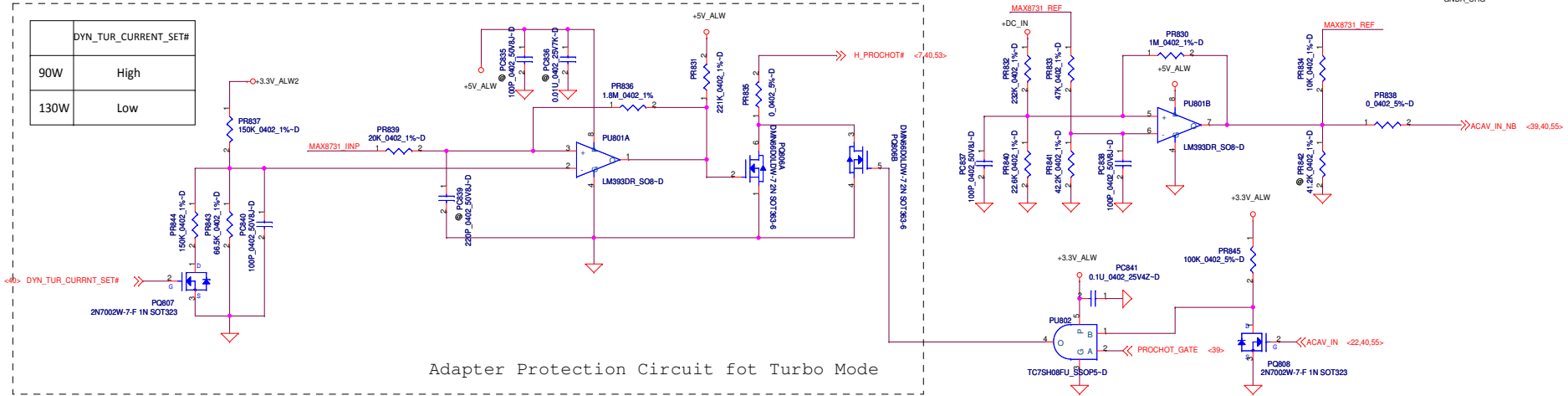
PR218  
TI bq24745 = 316K  
Intersil ISL88731 = 226K  
Maxim = 383K

Adapter Protection Event			
	PR521	PR522	PR510
SW	0 Ohm	@	100k
HW	@	0 Ohm	@



Maximum charging current is 7.2A


DYN_TUR_CURRENT_SET#	
90W	High
130W	Low



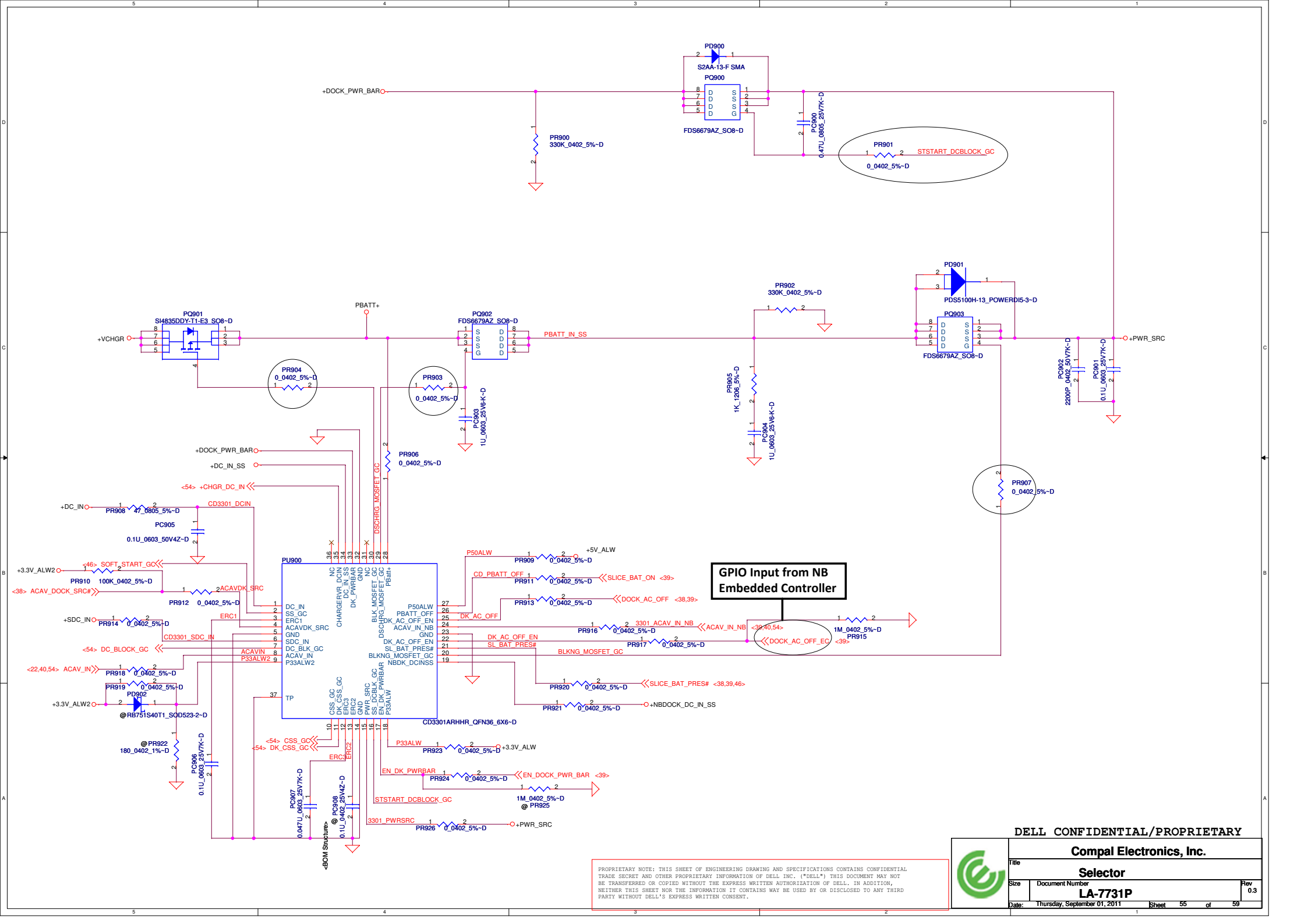
Adapter Protection Circuit for Turbo Mode

To preset system to throttle switching from AC to DC

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	Charger		
File	Document Number	Rev	
Size	LA-7731P	0.3	
Date	Thursday, September 01, 2011	Sheet	54 of 59

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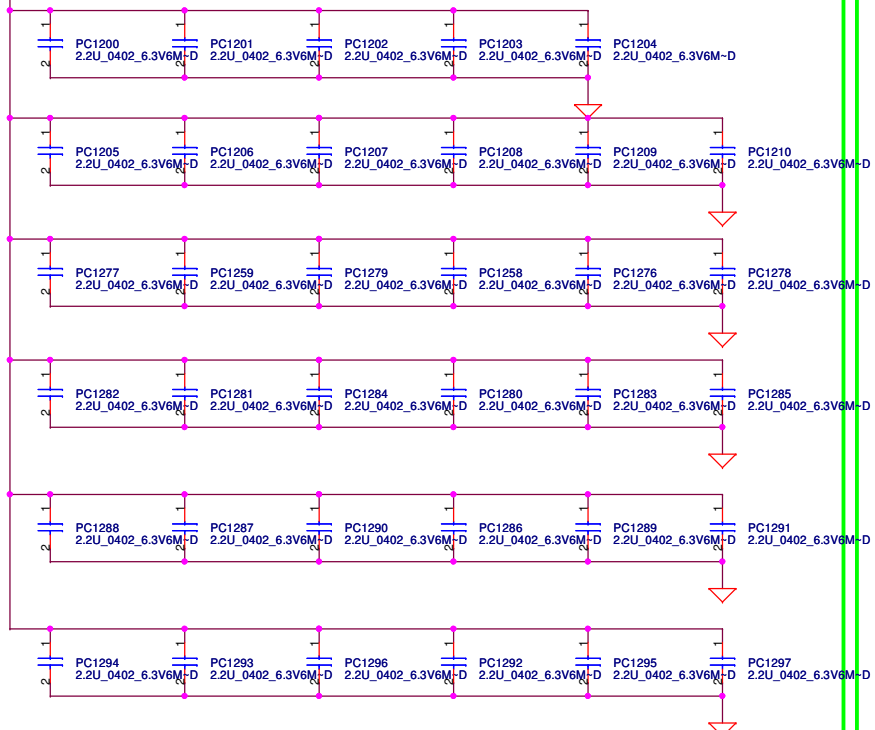
**Selector**

**LA-7731P**

Title			
Size	Document Number	Rev	
		<b>0.3</b>	
Date:	Thursday, September 01, 2011	Sheet	55 of 59

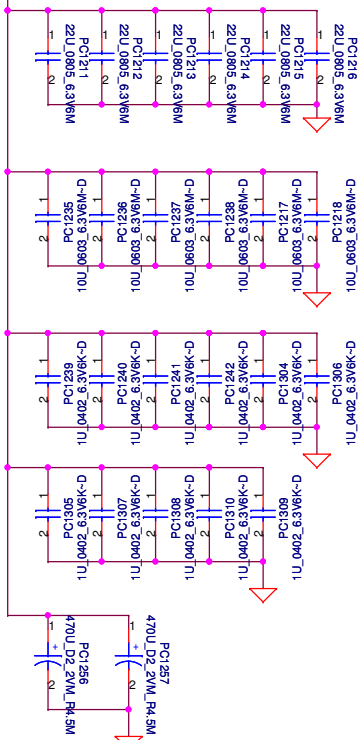
+VCC\_CORE

+VCC\_CORE



+VCC\_GFXCORE

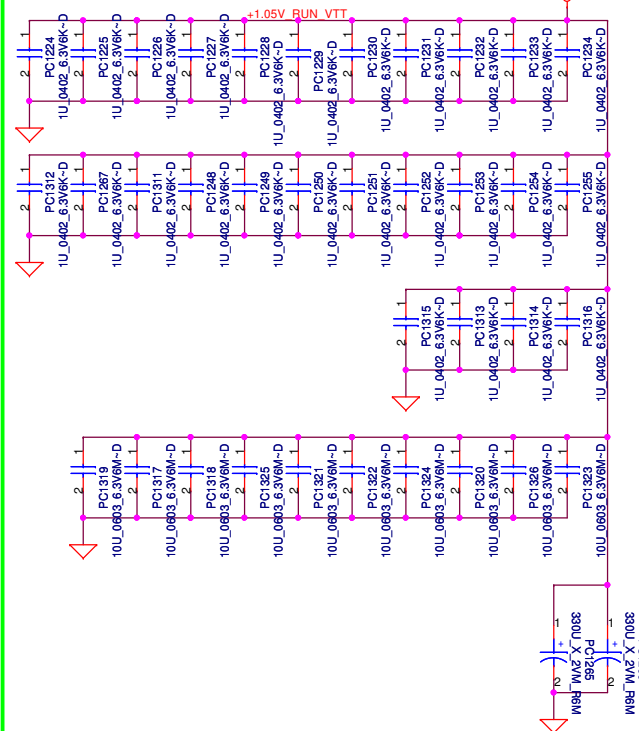
+VCC\_GFXCORE



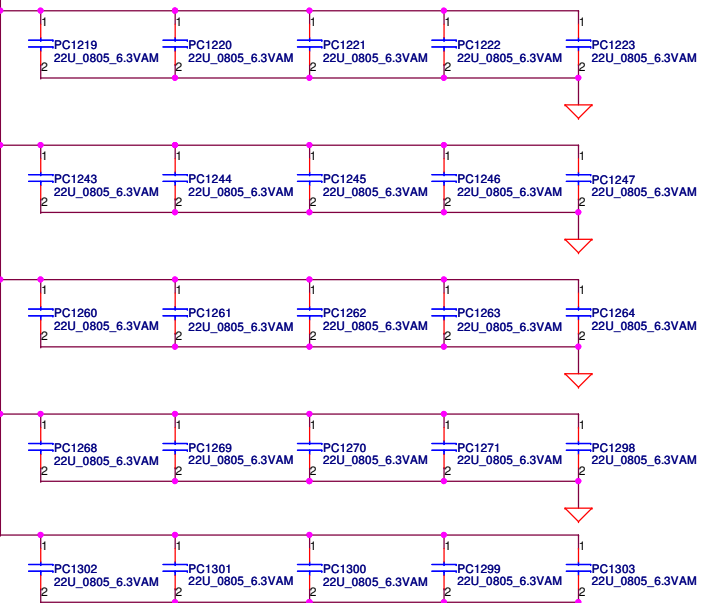
Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites

+1.05V\_RUN\_VTT

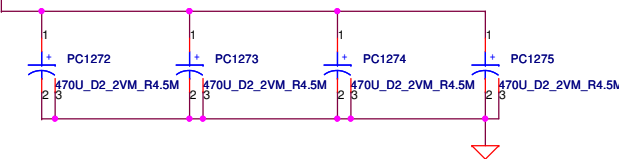


+VCC\_CORE



+VCC\_CORE

+VCC\_CORE



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PROCESSOR DECOUPLING

Title	PROCESSOR DECOUPLING	
Size	Document Number	Rev
	LA-7731P	0.3
Date:	Thursday, September 01, 2011	Sheet 56 of 59


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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	48	+1.5V_MEN	8/16	Dell	Follow VC , enable use SIO_SLP_S4#.	Add PR210 for net "SIO_SLP_S4#"	X01
2	46	DCIN	8/16	Dell	ME design change.	PJPDC1 change from 7pin to 5pin	X01
3	47	+5V/3.3V	8/16	Dell	Main and 2nd IC common setting.	De-pop PD100,PR113,PR111	X01
4	53	Vcore/GFX core	8/16	Compal RF_team	Suppress WWAN BB noise.	Pop PC751,PR760,PC725,PR731,PC745,PR751(680pF 0603, 4.7 ohm 1206)	X01
5	50 51	+1.05VM/ +1.05VTT	8/16	Compal	COS concern, change from D2 Polymer cap to OScon cap	PC406, PC507	X01
6	53	Vcore/GFX core	8/16	Compal	Prevent output voltage glitch when power up.	PU700 VCCP and VDD change form +5V_RUN to +5V_ALW	X01
7	47, 53 , 54	Vcore, Charger +5V/3.3V	8/16	Compal RF_team	EMI solution.	Pop PL700.PL1300,PL100	X01
8	53	Vcore/GFX core	8/16	Compal	adjust OCP and DC load line.	PR740 change to 2.1k ohm, PR750 change to 392 ohm.	X01
9							X01
10							X01
11							X01
12							X01

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<b>Compal Electronics, Inc.</b>		
<b>Title</b> PWR_PIR 1		
<b>Size</b>	<b>Document Number</b> LA-7731P	<b>Rev</b> 0.3
<b>Date:</b> Thursday, September 01, 2011 <b>Sheet</b> 57 <b>of</b> 59		

# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39, 40, 42	HW	7/14/2011	DELL	E4 uses SIO_SLP_S4# for power control	Add @R752, R753	X01
2	11	HW	7/14/2011	Compal	Change DDR channel A signal to DSL	Add CC149, CC152, CC178, CC179	X01
3	18	HW	7/26/2011	DELL	Follow GPIO map rev1.0	Change RH273 from 1k to 10k	X01
4	29	HW	7/26/2011	Compal	EMI request	Pop CE981, CE982, CE983	X01
5	35	HW	7/26/2011	Compal	Solve Express card PAID issue	Add R830	X01
<del>6</del>	<del>7,22</del>	<del>HW</del>	<del>7/27/2011</del>	<del>Compal</del>	<del>Solve ESD issue</del>	<del>Reserve D84, D85</del>	<del>X01</del>
7	25	HW	7/27/2011	Compal	Layout routing	Swap HDMI trace connection on L19, L20, L21, L22 for layout routing	X01
8	29	HW	7/28/2011	Compal	EMI request	Add CE984, CE985	X01
9	7	HW	8/1/2011	Compal	EMI request	Reserve CC141	X01
10	17	HW	8/3/2011	Intel	Request from Intel review feedback	Pop RH332	X01
11	14, 39	HW	8/4/2011	SMSC	SMSC request to delete LPC_LDRQ0#	Leave LDRQ0# no connection on both of 5048 and PCH side	X01
12	20, 42	HW	8/4/2011	Compal	Vgs less than cut-in voltage in battery mode	Add QH6, RH279, CH107	X01
13	42	HW	8/4/2011	Compal	Load SW sources output rising time mismatch and COS. cost concern.	Change back to E3 +3.3V/5V RUN discrete solution. Add Q55, Q56, Q61, Q62, R933, R940, R1627, remove U78, R749, R747, C1199, C1198, C1197, C1196, change C761, C764 to 10uF	X01
14	10	HW	8/4/2011	Compal	Follow INTEL PDDG 0_8	De-pop RC140	X01
15	32	HW	8/4/2011	Compal	RESET_OUT# power sequence issue	Add R1653, 1M ohms pull down for USH_PWR_STATE# at M/B side	X01
16	40	HW	8/4/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
17	34	HW	8/4/2011	COMPAL	PCH GPIO52 need 8.2~10K pull up +3.3VS	Change R695 from 100K to 10Kohms	X01
18	23	HW	8/4/2011	COMPAL	CRT SW 2nd source TI, TS3V713 pin29 is VDD	Connect pin29 to +3.3V_RUN	X01
19	16	HW	8/4/2011	COMPAL	+1.05V M turn off before APWROK de-assert	Add UH5 circuit for backup HW solution	X01
20	41	HW	8/4/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable)	X01
21	29	HW	8/4/2011	COMPAL	Co-lay 92HD93 with ALC290	Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642 Reserve for ALC290 only: C1204, C1205, R171, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963	X01
22	29	HW	8/4/2011	COMPAL	Codec is change to 92HD93	Pop R162~R166 and de-pop U73	X01
<del>23</del>	<del>40</del>	<del>HW</del>	<del>8/8/2011</del>	<del>COMPAL</del>	<del>Please depop VOL MUTE/UP/DOWN due to EC code enable internal PU resistors (3V_ALW)</del>	<del>De-pop R1169, R1197, R1118</del>	<del>X01</del>
24	41	HW	8/8/2011	COMPAL	For debug purpose	Add R1624	X01
25	42	HW	8/8/2011	COMPAL	power suggestion	Change Q59 to A04728L	X01
26	43	HW	8/9/2011	COMPAL	Align with E4	Change LED6, LED7 power source from +3.3V_ALW to +5V_ALW	X01
27	14, 40	HW	8/10/2011	COMPAL	Crystal EA result	Change C741, C743 from 22p to 39p, CH2, CH3 from 15p to 18p, CH18, CH19 from 12p to 10p for crystal EA	X01
28	41	HW	08/11/2011	COMPAL	For RSMRST# debug	Reserve R1655 and pop R1623	X01
29	26	HW	08/11/2011	COMPAL	DPX_CA_DET voltage too low through dongle	Change U21 and U24 to SA000055G0L	X01
<del>30</del>	<del>43</del>	<del>HW</del>	<del>08/11/2011</del>	<del>COMPAL</del>	<del>Tune white light LED brightness</del>	<del>Change R934, R938, R939, R949, R958, R957 and R955 to 2.2K ohm</del>	<del>X01</del>

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<b>EE P.I.R (1/2)</b>		
Size	Document Number	Rev
	<b>LA-7731P</b>	<b>0.3</b>
Date:	Thursday, September 01, 2011	Sheet 58 of 59

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
31	20, 22, 34 38, 39, 43	HW	8/11/2011	COMPAL	Cost saving	Change D2, D31, D32, D34, D59, D62, DH2, DH3, D65, D66, D67, D68, D69, D70 to SCS00002G00	X01
32	11	HW	8/12/2011	COMPAL	Solve S3 wake up issue	Pop RC79 and de-pop RC82	X01
33	36, 41	HW	8/14/2011	ME	ME change connector	Change JUSB1, JUSB2, JBT1	X01
34	30	HW	8/16/2011	ME	ME change connector	Change JLID1	X01
35	17, 32 39, 40	HW	8/18/2011	COMPAL	RF request	Pop R885, C747, R795, C713, RE5 and change CE3 to 12pF and pop it, and add CH109, CH110	X01
36	36	HW	8/19/2011	COMPAL	Follow Intel design guide	Change C410~C413 from 0.01uF to 0.1uF	X01
37	25	HW	8/24/2011	COMPAL	EMI request to solve HDMI issue	Add C1216~C1223	X01
38	7	HW	8/25/2011	COMPAL	ESD request	Change RC25 to 1k and pop CC141	X01
39	40	HW	8/26/2011	SMSC	SMSC request	Reserve R941, R942	X01
40	24, 33	HW	8/26/2011	EMI	EMI request to solve SD/DMIC issue	Reserve CE758, CE279, CE280	X01
41	43	HW	8/27/2011	ME	Solve standoff shift issue	Change H11, H24, H25 to 6mm	X01
42	43	HW	8/29/2011	COMPAL	Tune white light LED brightness	Change R934, R938, R939, R949, R958, R957 and R955 to 1.2K ohm	X01
42	14	HW	8/29/2011	ME	change TAA connector	Change JTAA1	X01

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**EE P.I.R (2/2)**

**LA-7731P**

Date: Thursday, September 01, 2011 Sheet 59 of 59



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