

POWER Page 28-- 35

- AC/BATT CONNECTOR
- BATT CHARGER
- CPU CORE
- +5V_SUS / +3.3V_ALW
- +1.5V_SUS / +0.75V_VTT
- +1.1V_RUN
- +0.9V_RUN LDO
- +1.8V_RUN LDO
- +2.5V_RUN LDO
- +1.1V_ALW_SB LDO

THERMAL Page 26

SMSC EMC1423

- CPU Thermal Diode
- OTP Sensor

Side Port with 128M (MAX) Page 11

Dual/ Single Core CPU
AMD Nile
Single: 12W/ Dual:15W
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North Bridge
ATI RS880M
Page 9, 10, 11, 12

South Bridge
ATI SB820M
Page 15, 16, 17, 18

Panel Page 13

HDMI Conn Page 14

Mini DP Conn Page 14

WLAN Half MINI-CARD Page 22

WWAN MINI-CARD Page 22

USB 2.0 Page 20

USB 2.0 Page 20

eSATA/ USB Conn Page 20

Blue Tooth Conn Page 24

Crystal 25M

LAN Controller (10/100M) & Card Reader
Realtek RTL8401 Page 21

Crystal 32.768K

SIO ITE ITE8502E Page 25

FLASH Memory 2MB (8 Pin SO8W) Page 19

Keyboard Page 24

Touchpad Page 24

T/P Board

Crystal 25M 32.768K

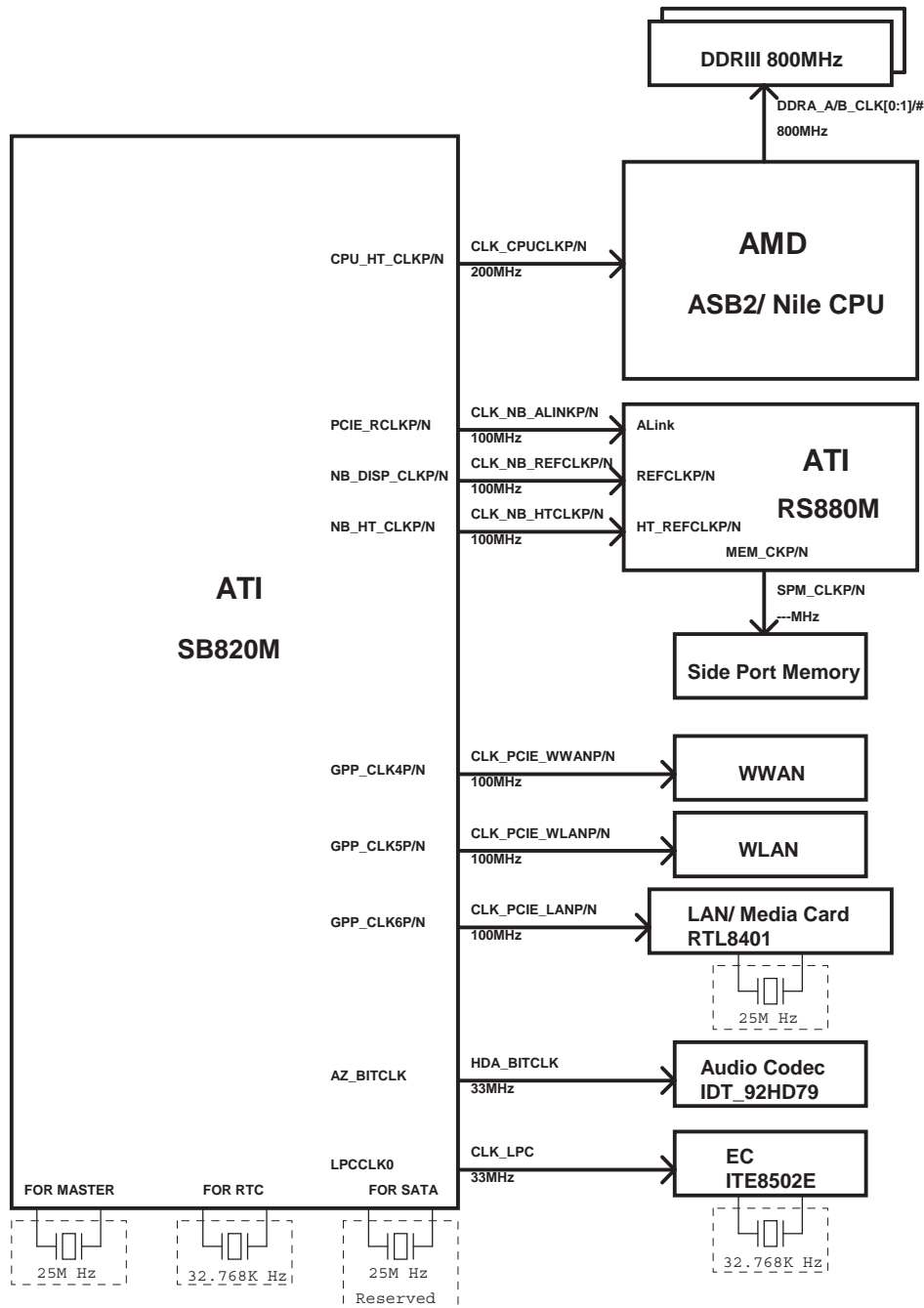
LED/ Hall sensor Page 24

Indicator Board

Power SW Page 24

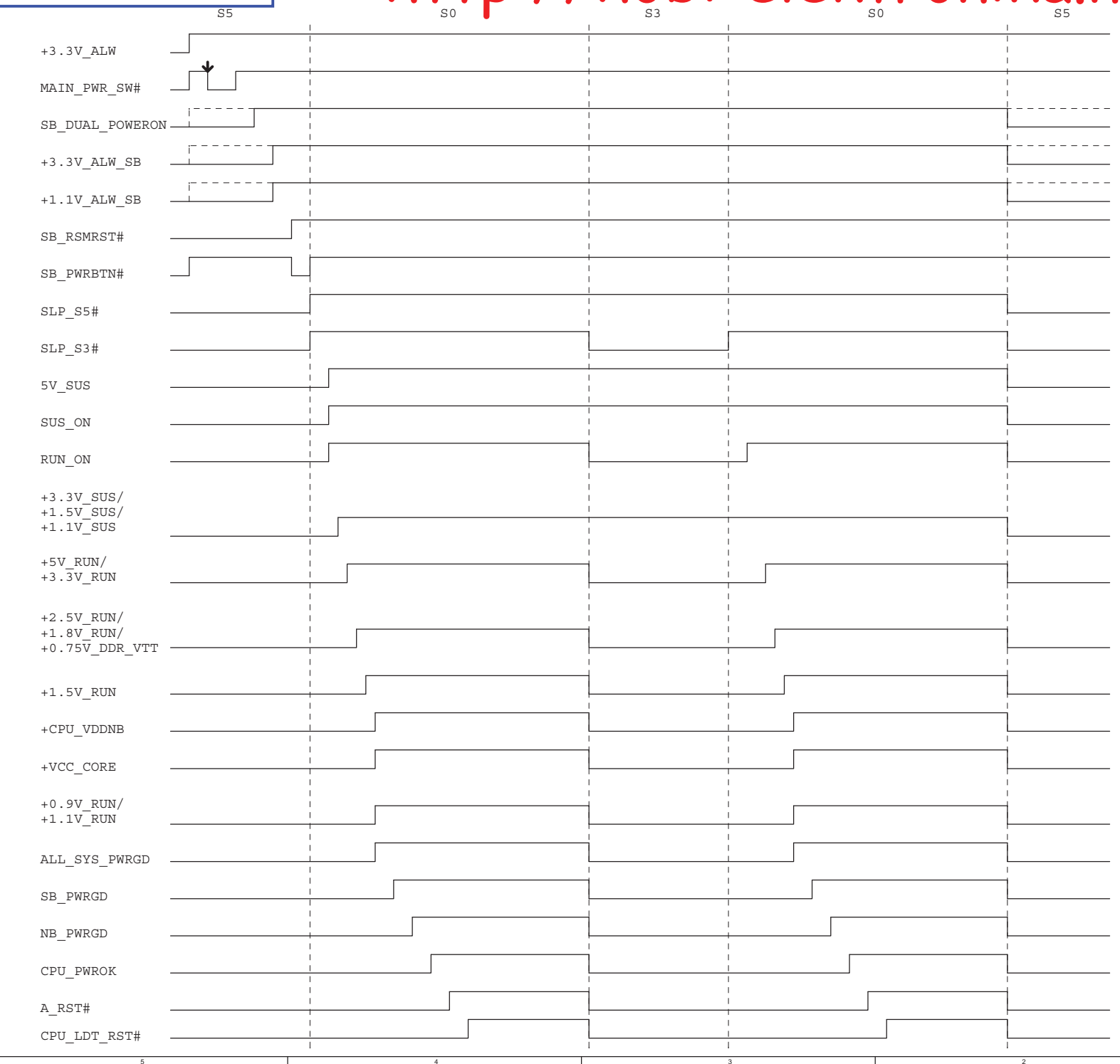
Power SW Board

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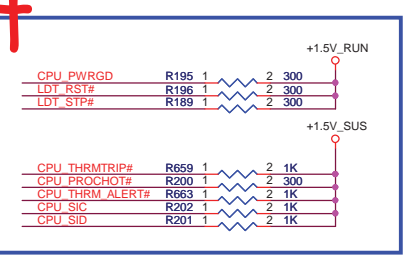
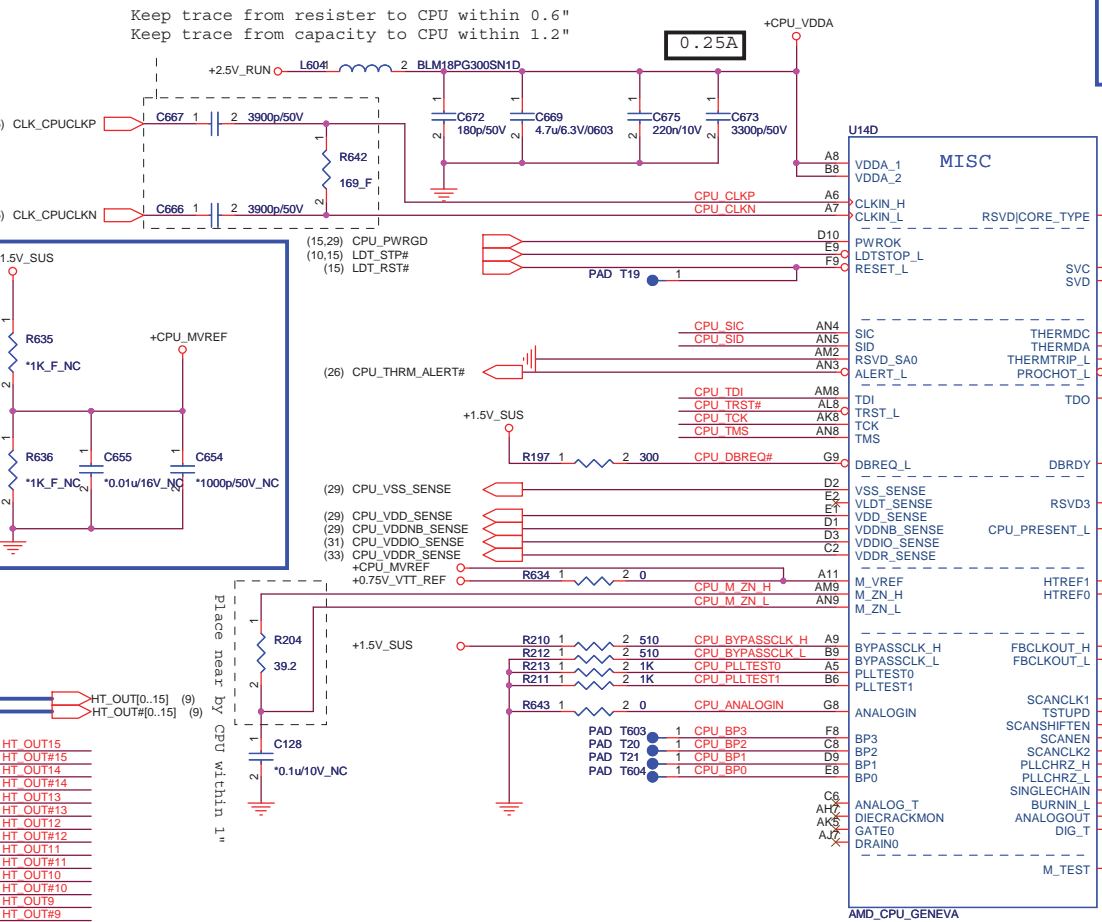


Power States							
Power Rail	Control Signal	S0	S3	S4	S5	G3/ AC-in	G3/ Battery Only
+PWR_SRC	N/A	V	V	V	V		
+0.75V_DDR_VTT	RUN_ON	V					
+0.9V_RUN	RUN_ON	V					
+1.1V_ALW_SB	SB_DUAL_PWRON	V	V	V	V		
+1.1V_SUS	SUS_ON	V	V				
+1.1V_RUN	RUN_ON	V					
+1.5V_SUS	SUS_ON	V	V				
+1.5V_RUN	RUN_ON	V					
+1.8V_RUN	RUN_ON	V					
+2.5V_RUN	RUN_ON	V					
+3.3V_ALW	+3.3V_EN2	V	V	V	V		
+3.3V_ALW_SB	SB_DUAL_PWRON	V	V	V			
+3.3V_SUS	SUS_ON	V	V				
+3.3V_RUN	RUN_ON	V					
+3.3V_KBVCC	N/A	V	V	V	V		
+5V_LDO	N/A	V	V	V	V		
+5V_SUS	5V_SUS_ON	V	V				
+5V_RUN	RUN_ON	V					
+GFX_PWR_SRC	N/A	V					
+LCDVCC	LCD_DIGON	V					
+CPU_VDDNB	2.5V_PWRGD	V					
+VCC_CORE	2.5V_PWRGD	V					
+RTC_CELL	N/A	V	V	V	V	V	V
+USB_RIGHT_PWR	USB_EN#	V	V				
+USB_LEFT_PWR	USB_EN#	V	V				

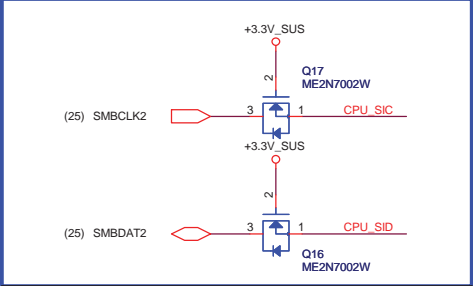
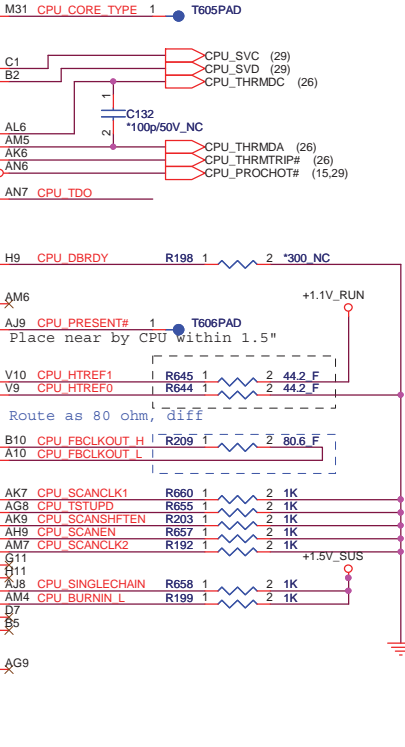
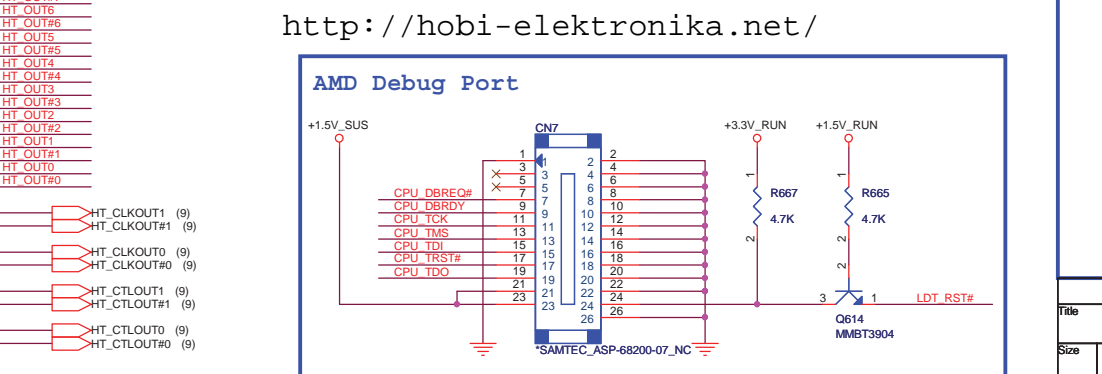
Power On Sequence

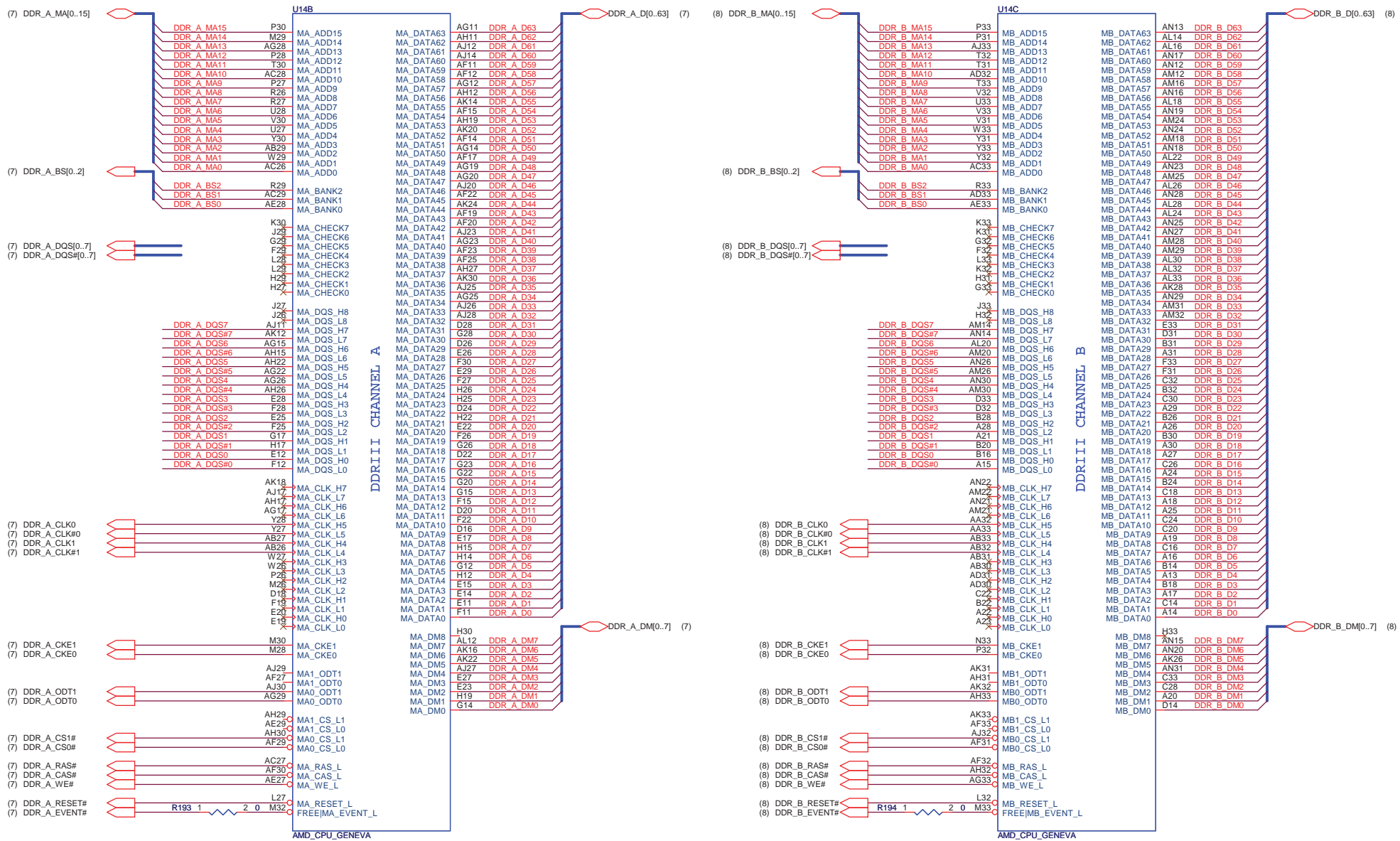


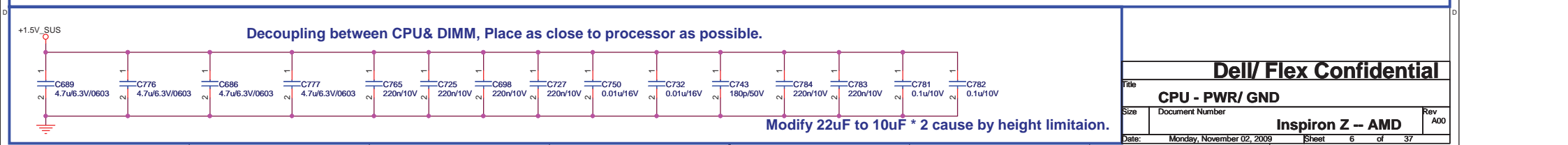
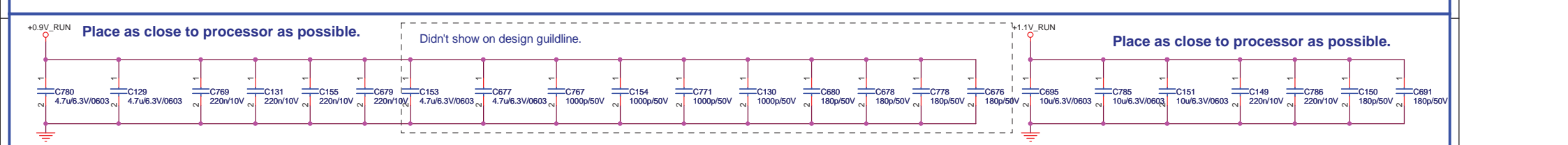
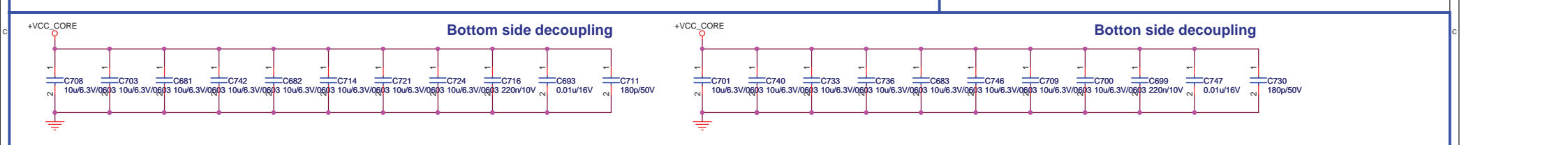
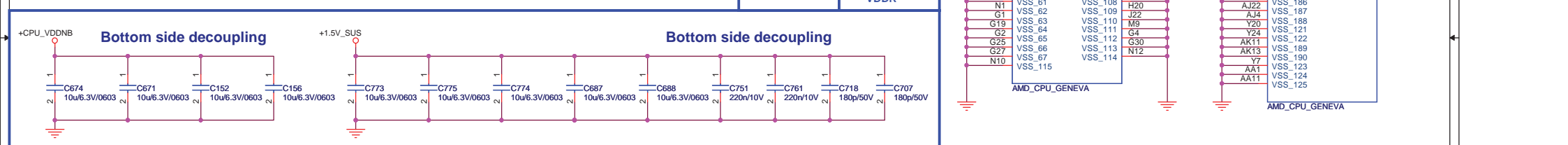
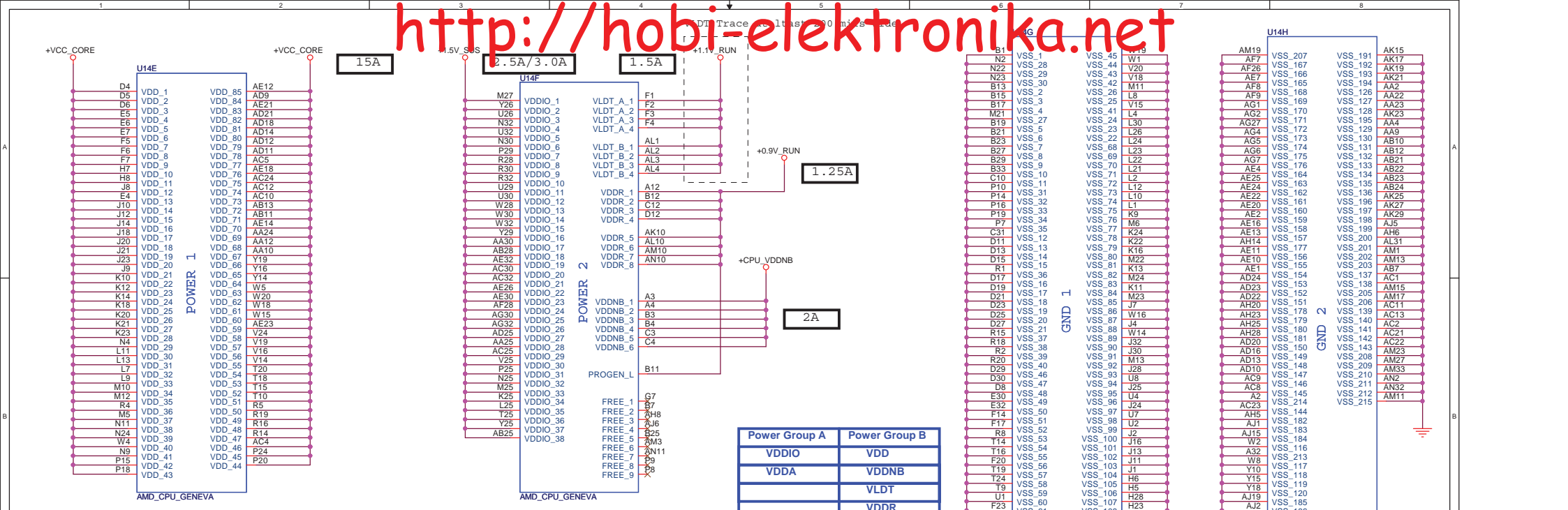
Signal Name	Type	Header	Termination	Level Shift ⁴	Term Voltage
TEST2	DRAIN0	-	Unconnected	-	-
TEST3	GATE	-	Unconnected	-	-
TEST6	DIECRACKMON	-	Unconnected	-	-
TEST7	ANALOG_I	-	Unconnected	-	-
TEST8	DIG_I	-	Unconnected	-	-
TEST9	ANALOGIN	-	Tie to VSS	-	-
TEST10	ANALOGOUT	-	Unconnected	-	-
TEST14	BP0	O P/P	BP, Pin 1 or TP	-	-
TEST15	BP1	O P/P	BP, Pin 3 or TP	-	-
TEST16	BP2	O P/P	BP, Pin 5 or TP	-	-
TEST17	BP3	O P/P	BP, Pin 7 or TP	-	-
TEST18	PLLTEST1	SCAN, pin 7 and HDT+, pin 20	1 KΩ	-	VSS
TEST19	PLLTEST0	SCAN, pin 9 and HDT+, pin 18	1 KΩ	-	VSS
TEST20	SCANCLK2	SCAN, pin 19	1 KΩ	-	VSS
TEST21	SCANEN	SCAN, pin 11	1 KΩ	-	VSS
TEST22	SCANSHIFTEN	SCAN, pin 13	1 KΩ	-	VSS
TEST23	TSTUPD	TP	1 KΩ	-	VSS
TEST24	SCANCLK1	SCAN, pin 17	1 KΩ	-	VSS
TEST25_H	BYPASSCLK_H	TP	510 Ω	-	VDDIO
TEST25_L	BYPASSCLK_L	TP	510 Ω	-	VSS
TEST26	BURNIN_L	Termination only	1 KΩ	-	VDDIO
TEST27	SINGLECHAIN	TP	1 KΩ	-	VDDIO
TEST28_H	H_PLLCHRZ_P	Unconnected	-	-	-
TEST28_L	L_PLLCHRZ_N	Unconnected	-	-	-
TEST29_H	H_FBCLKOUT_P	-	-	-	-
TEST29_L	L_FBCLKOUT_N	-	-	-	-



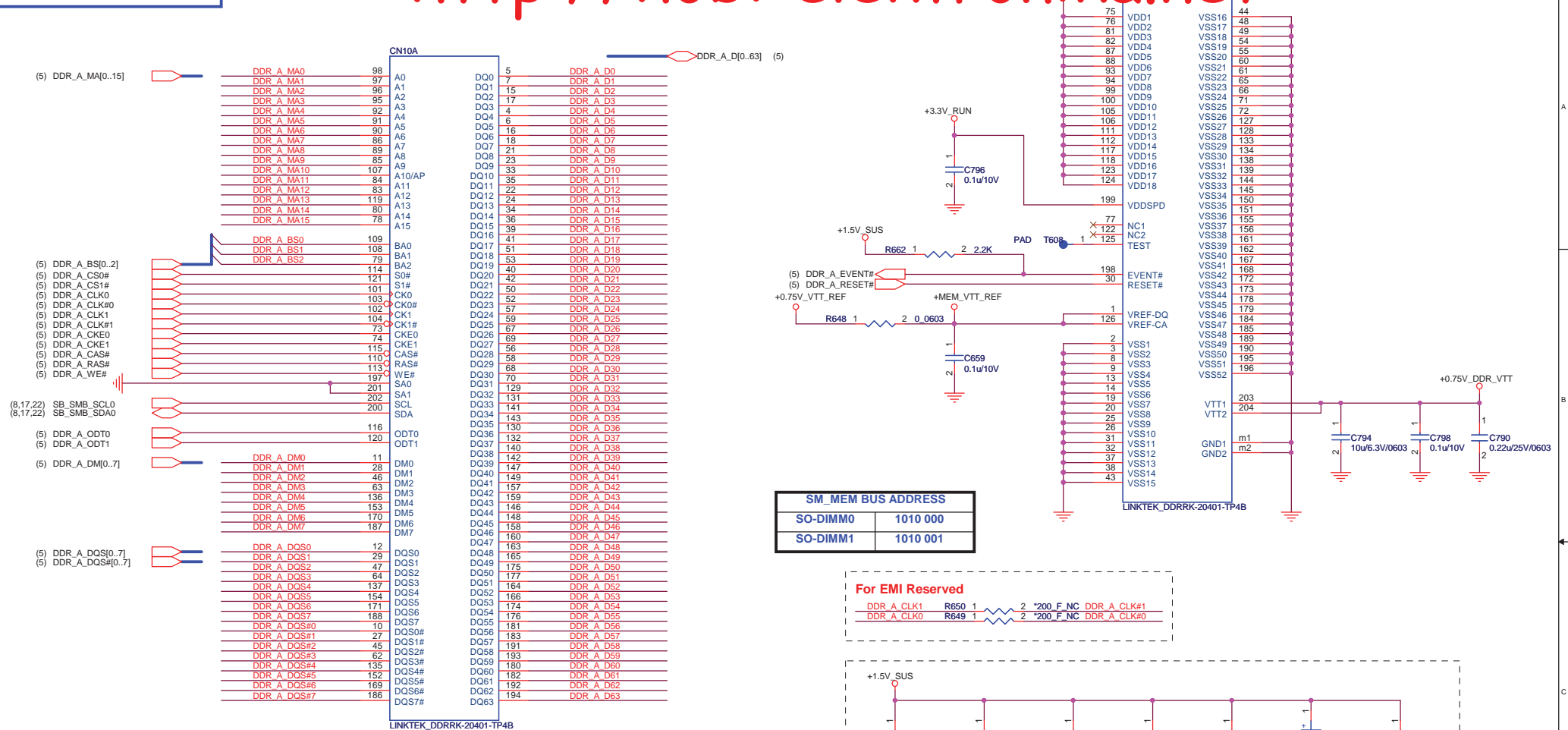
Signal Name	Type	Header	Termination	Level Shift ⁴	Term Voltage
(9) HT_IN[0..15]	I	HT_IN#0..HT_IN#15	-	-	-
(9) HT_OUT[0..15]	O	HT_OUT#0..HT_OUT#15	-	-	-
(9) HT_CLKIN#1	I	M8	L0_CLKIN_H1	-	-
(9) HT_CLKIN#0	I	M7	L0_CLKIN_L1	-	-
(9) HT_CLKIN#0	I	M3	L0_CLKIN_H0	-	-
(9) HT_CLKIN#0	I	M4	L0_CLKIN_L0	-	-
(9) HT_CTLIN#1	I	Y6	L0_CTLIN_H1	-	-
(9) HT_CTLIN#0	I	Y5	L0_CTLIN_L1	-	-
(9) HT_CTLIN#0	I	V2	L0_CTLIN_H0	-	-
(9) HT_CTLIN#0	I	V1	L0_CTLIN_L0	-	-



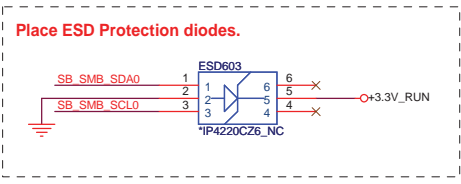
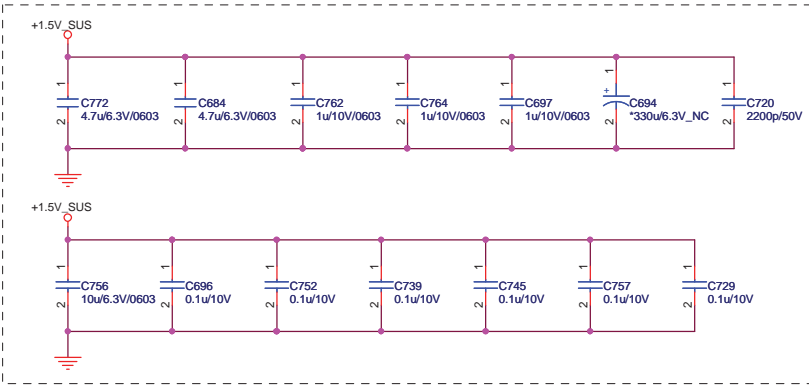
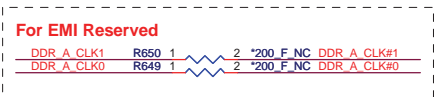




DDR3 DIMM A



SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001



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Title: **SO-DIMM1**

Size: Document Number

Inspiron Z -- AMD

Date: Monday, November 02, 2009 Sheet 7 of 37

(4) HT_OUT[0..15]
(4) HT_OUT# [0..15]

HT_OUT0	Y25	HT_RXCAD0P
HT_OUT#0	Y24	HT_RXCAD0N
HT_OUT1	V22	HT_RXCAD1P
HT_OUT#1	V23	HT_RXCAD1N
HT_OUT2	V25	HT_RXCAD2P
HT_OUT#2	V24	HT_RXCAD2N
HT_OUT3	U24	HT_RXCAD3P
HT_OUT#3	U25	HT_RXCAD3N
HT_OUT4	T25	HT_RXCAD4P
HT_OUT#4	T24	HT_RXCAD4N
HT_OUT5	P22	HT_RXCAD5P
HT_OUT#5	P23	HT_RXCAD5N
HT_OUT6	P25	HT_RXCAD6P
HT_OUT#6	P24	HT_RXCAD6N
HT_OUT7	N24	HT_RXCAD7P
HT_OUT#7	N25	HT_RXCAD7N
HT_OUT8	AC24	HT_RXCAD8P
HT_OUT#8	AC25	HT_RXCAD8N
HT_OUT9	AB25	HT_RXCAD9P
HT_OUT#9	AB24	HT_RXCAD9N
HT_OUT10	AA24	HT_RXCAD10P
HT_OUT#10	AA25	HT_RXCAD10N
HT_OUT11	Y22	HT_RXCAD11P
HT_OUT#11	Y23	HT_RXCAD11N
HT_OUT12	W21	HT_RXCAD12P
HT_OUT#12	W20	HT_RXCAD12N
HT_OUT13	V21	HT_RXCAD13P
HT_OUT#13	V20	HT_RXCAD13N
HT_OUT14	U20	HT_RXCAD14P
HT_OUT#14	U21	HT_RXCAD14N
HT_OUT15	U19	HT_RXCAD15P
HT_OUT#15	U18	HT_RXCAD15N

HYPER TRANSPORT CPU I/F

(4) HT_CLKOUT0
(4) HT_CLKOUT#0
(4) HT_CLKOUT1
(4) HT_CLKOUT#1

T22	HT_RXCLK0P
T23	HT_RXCLK0N
AB23	HT_RXCLK1P
AA22	HT_RXCLK1N
M22	HT_RXCTL0P
M23	HT_RXCTL0N
R21	HT_RXCTL1P
R20	HT_RXCTL1N

HT_OUTCAL# C23
HT_OUTCAL# A24

HT_TXCAD0P	D24	HT_IN#0
HT_TXCAD0N	D25	HT_IN#0
HT_TXCAD1P	E24	HT_IN#1
HT_TXCAD1N	E25	HT_IN#1
HT_TXCAD2P	F24	HT_IN#2
HT_TXCAD2N	F25	HT_IN#2
HT_TXCAD3P	F23	HT_IN#3
HT_TXCAD3N	F22	HT_IN#3
HT_TXCAD4P	H23	HT_IN#4
HT_TXCAD4N	H22	HT_IN#4
HT_TXCAD5P	J25	HT_IN#5
HT_TXCAD5N	J24	HT_IN#5
HT_TXCAD6P	K24	HT_IN#6
HT_TXCAD6N	K25	HT_IN#6
HT_TXCAD7P	K23	HT_IN#7
HT_TXCAD7N	K22	HT_IN#7
HT_TXCAD8P	F21	HT_IN#8
HT_TXCAD8N	G21	HT_IN#8
HT_TXCAD9P	G20	HT_IN#9
HT_TXCAD9N	H21	HT_IN#9
HT_TXCAD10P	J20	HT_IN#10
HT_TXCAD10N	J21	HT_IN#10
HT_TXCAD11P	J18	HT_IN#11
HT_TXCAD11N	K17	HT_IN#11
HT_TXCAD12P	L19	HT_IN#12
HT_TXCAD12N	J19	HT_IN#12
HT_TXCAD13P	M19	HT_IN#13
HT_TXCAD13N	L18	HT_IN#13
HT_TXCAD14P	M21	HT_IN#14
HT_TXCAD14N	P21	HT_IN#14
HT_TXCAD15P	P18	HT_IN#15
HT_TXCAD15N	M18	HT_IN#15

(4) HT_TXCLK0P
(4) HT_TXCLK0N
(4) HT_TXCLK1P
(4) HT_TXCLK1N

HT_TXCALP
HT_TXCALN

HT_CLKIN#0 (4)
HT_CLKIN#1 (4)
HT_CLKIN#1 (4)

HT_CTLIN#0 (4)
HT_CTLIN#0 (4)
HT_CTLIN#1 (4)
HT_CTLIN#1 (4)

R128 2 1 301 F HT_OUTCAL# A24

B24 HT_INCAL# R129 1 2 301 F

ATI_RS880M

U10B

PART 2 OF 6

PCIE I/F GFX

X4	GFX_RX0P
X3	GFX_RX0N
X3	GFX_RX1P
X2	GFX_RX1N
X1	GFX_RX2P
X1	GFX_RX2N
X5	GFX_RX3P
X5	GFX_RX3N
X6	GFX_RX4P
X5	GFX_RX4N
X6	GFX_RX5P
X5	GFX_RX5N
X6	GFX_RX6P
X5	GFX_RX6N
X7	GFX_RX7P
X5	GFX_RX7N
X6	GFX_RX8P
X5	GFX_RX8N
X7	GFX_RX9P
X5	GFX_RX9N
X7	GFX_RX10P
X5	GFX_RX10N
X8	GFX_RX11P
X6	GFX_RX11N
X8	GFX_RX12P
X6	GFX_RX12N
X8	GFX_RX13P
X6	GFX_RX13N
X9	GFX_RX14P
X7	GFX_RX14N
X9	GFX_RX15P
X7	GFX_RX15N

A5	HDMI_TX2_P_C
B5	HDMI_TX2_N_C
B4	HDMI_TX1_P_C
C3	HDMI_TX0_P_C
B2	HDMI_TX0_N_C
D1	HDMI_CLK_P_C
E2	DP_LANE0_P_C
E1	DP_LANE0_N_C
F4	DP_LANE1_P_C
F3	DP_LANE1_N_C
F1	DP_LANE2_P_C
F2	DP_LANE2_N_C
H4	DP_LANE3_P_C
H3	DP_LANE3_N_C
H1	X
H2	X
J2	X
K4	X
K3	X
K1	X
K2	X
M3	X
M1	X
M2	X
N2	X
N1	X
P1	X
P2	X

C76	1	2	0.1u/10V	HDMI_TX2_P (14)
C79	1	2	0.1u/10V	HDMI_TX2_N (14)
C71	1	2	0.1u/10V	HDMI_TX1_P (14)
C75	1	2	0.1u/10V	HDMI_TX1_N (14)
C65	1	2	0.1u/10V	HDMI_TX0_P (14)
C66	1	2	0.1u/10V	HDMI_TX0_N (14)
C67	1	2	0.1u/10V	HDMI_CLK_P (14)
C68	1	2	0.1u/10V	HDMI_CLK_N (14)
C69	1	2	0.1u/10V	DP_LANE0_P (14)
C96	1	2	0.1u/10V	DP_LANE0_N (14)
C96	1	2	0.1u/10V	DP_LANE1_P (14)
C91	1	2	0.1u/10V	DP_LANE1_N (14)
C82	1	2	0.1u/10V	DP_LANE2_P (14)
C86	1	2	0.1u/10V	DP_LANE2_N (14)
C87	1	2	0.1u/10V	DP_LANE3_P (14)
C83	1	2	0.1u/10V	DP_LANE3_N (14)
C94	1	2	0.1u/10V	DP_LANE3_N (14)

C263, C264, C260, C261, C265, C266, C208, C262:
Near by HDMI Conn -- CN6
C258, C259, C256, C257, C254, C255, C206, C253:
Near by DP Conn -- CN7

WWAN
WLAN
LAN/ Media Card

AE3	GPP_RX0P
AD4	GPP_RX0N
AE2	GPP_RX1P
AD3	GPP_RX1N
AD1	GPP_RX2P
AD2	GPP_RX2N
V5	GPP_RX3P
W6	GPP_RX3N
U5	GPP_RX4P
U6	GPP_RX4N
U8	GPP_RX5P
U7	GPP_RX5N
X	GPP_RX5N

PCIE I/F GPP

GPP_TX0P	AC1	PCIE_TX0_P_C
GPP_TX0N	AC2	PCIE_TX0_N_C
GPP_TX1P	AB4	PCIE_TX1_P_C
GPP_TX1N	AB3	PCIE_TX1_N_C
GPP_TX2P	AA2	PCIE_TX2_P_C
GPP_TX2N	AA1	PCIE_TX2_N_C
GPP_TX3P	Y1	X
GPP_TX3N	Y2	X
GPP_TX4P	Y3	X
GPP_TX4N	V1	X
GPP_TX5P	V2	X
GPP_TX5N	X	X

C108	1	2	0.1u/10V	PCIE_TX0_P (22)
C109	1	2	0.1u/10V	PCIE_TX0_N (22)
C106	1	2	0.1u/10V	PCIE_TX1_P (22)
C107	1	2	0.1u/10V	PCIE_TX1_N (22)
C103	1	2	0.1u/10V	PCIE_TX2_P (21)
C104	1	2	0.1u/10V	PCIE_TX2_N (21)

(15) PCIE_ALINK_RX0_P
(15) PCIE_ALINK_RX0_N
(15) PCIE_ALINK_RX1_P
(15) PCIE_ALINK_RX1_N
(15) PCIE_ALINK_RX2_P
(15) PCIE_ALINK_RX2_N
(15) PCIE_ALINK_RX3_P
(15) PCIE_ALINK_RX3_N

AA8	SB_RX0P
Y8	SB_RX0N
AA7	SB_RX1P
Y7	SB_RX1N
AA5	SB_RX2P
Y5	SB_RX2N
AA6	SB_RX3P
Y5	SB_RX3N
Y5	SB_RX3N

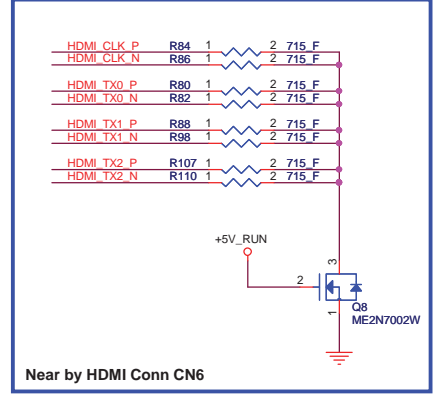
PCIE I/F SB

SB_TX0P	AD7	PCIE_ALINK_TX0_P_C
SB_TX0N	AE7	PCIE_ALINK_TX0_N_C
SB_TX1P	AE6	PCIE_ALINK_TX1_P_C
SB_TX1N	AD6	PCIE_ALINK_TX1_N_C
SB_TX2P	AB6	PCIE_ALINK_TX2_P_C
SB_TX2N	AC6	PCIE_ALINK_TX2_N_C
SB_TX3P	AD5	PCIE_ALINK_TX3_P_C
SB_TX3N	AE5	PCIE_ALINK_TX3_N_C

C114	1	2	0.1u/10V	PCIE_ALINK_TX0_P (15)
C113	1	2	0.1u/10V	PCIE_ALINK_TX0_N (15)
C112	1	2	0.1u/10V	PCIE_ALINK_TX1_P (15)
C111	1	2	0.1u/10V	PCIE_ALINK_TX1_N (15)
C119	1	2	0.1u/10V	PCIE_ALINK_TX2_P (15)
C118	1	2	0.1u/10V	PCIE_ALINK_TX2_N (15)
C116	1	2	0.1u/10V	PCIE_ALINK_TX3_P (15)
C117	1	2	0.1u/10V	PCIE_ALINK_TX3_N (15)

PCE_CALRP R684 2 1 1.27K F
PCE_CALRN R685 1 2 2K F +1.1V_RUN

ATI_RS880M

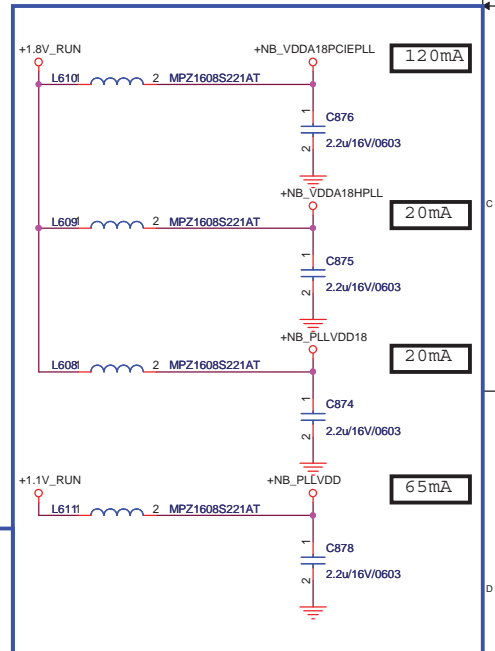
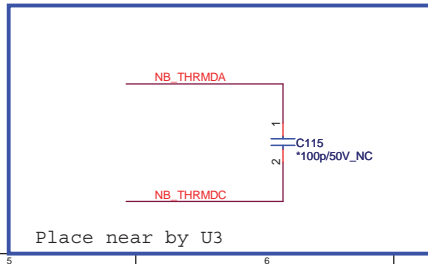
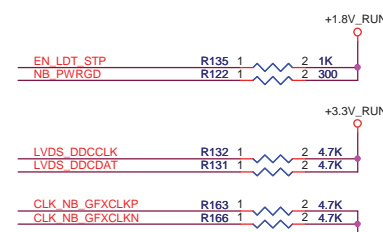
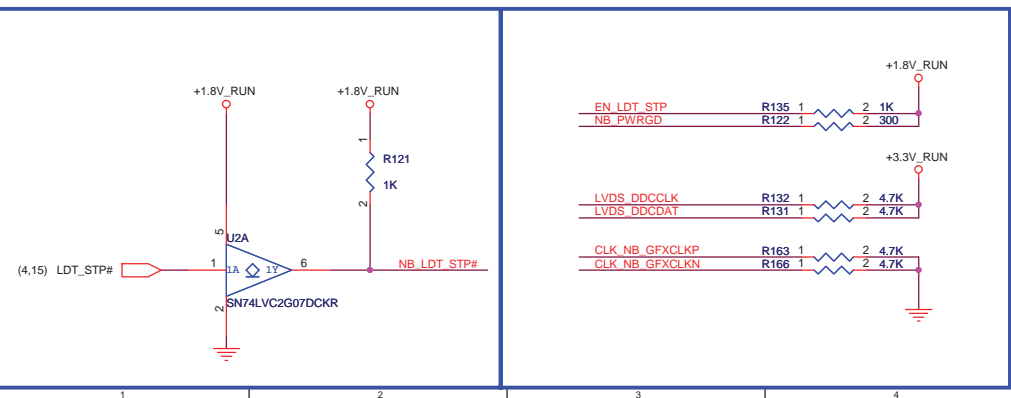
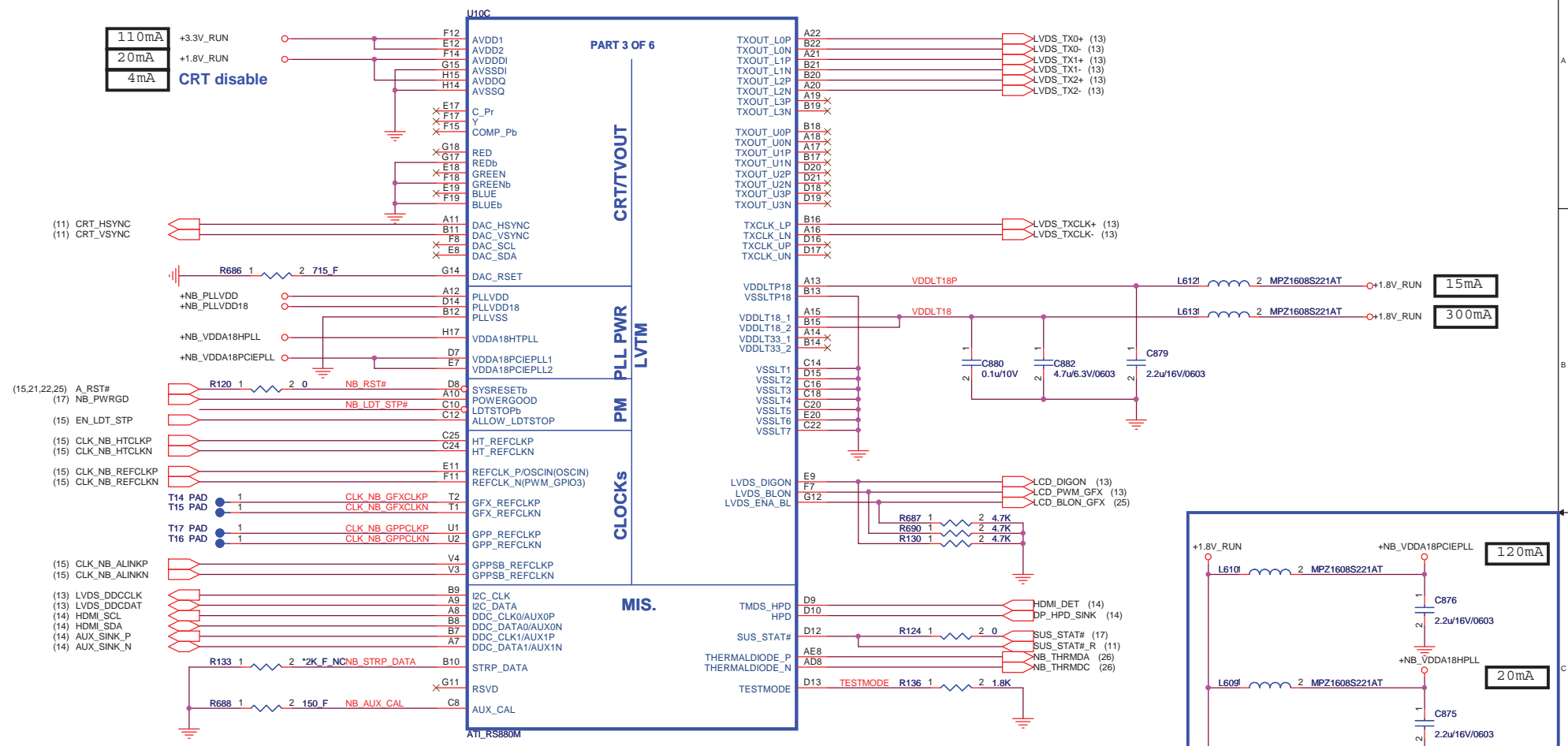


WWAN
WLAN
LAN/ Media Card

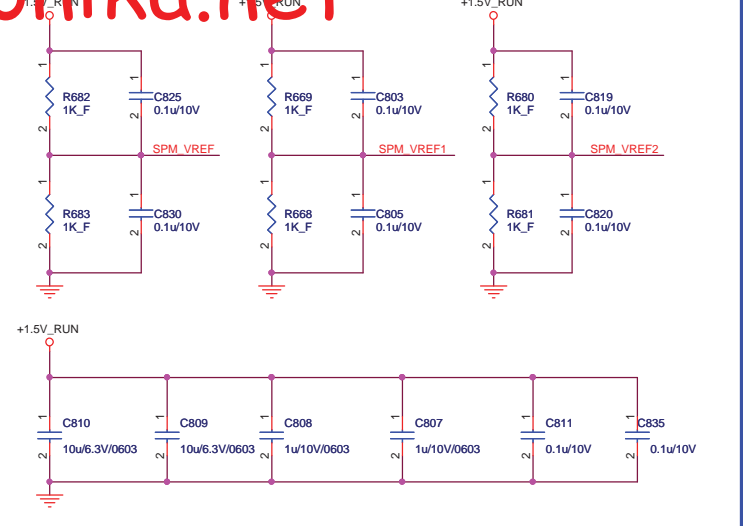
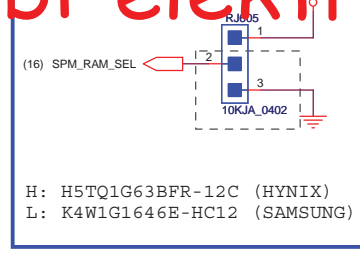
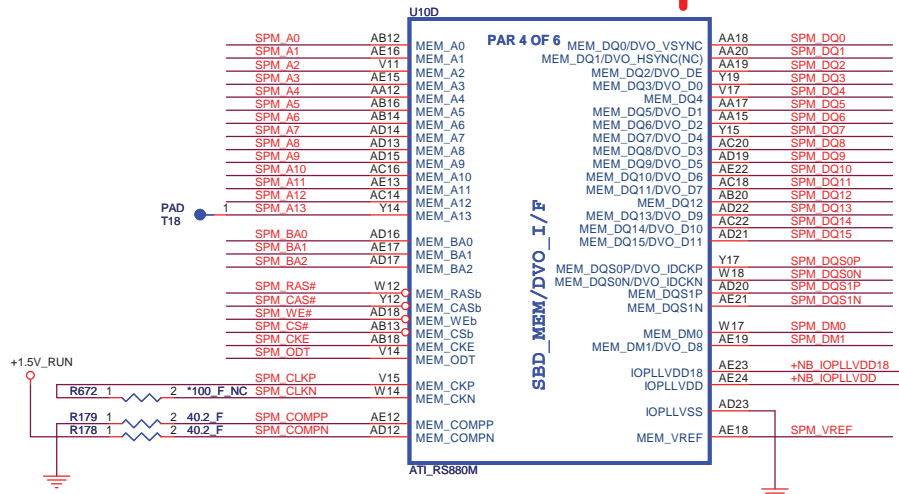
NB LVDS/ PM

- 110mA +3.3V_RUN
- 20mA +1.8V_RUN
- 4mA CRT disable

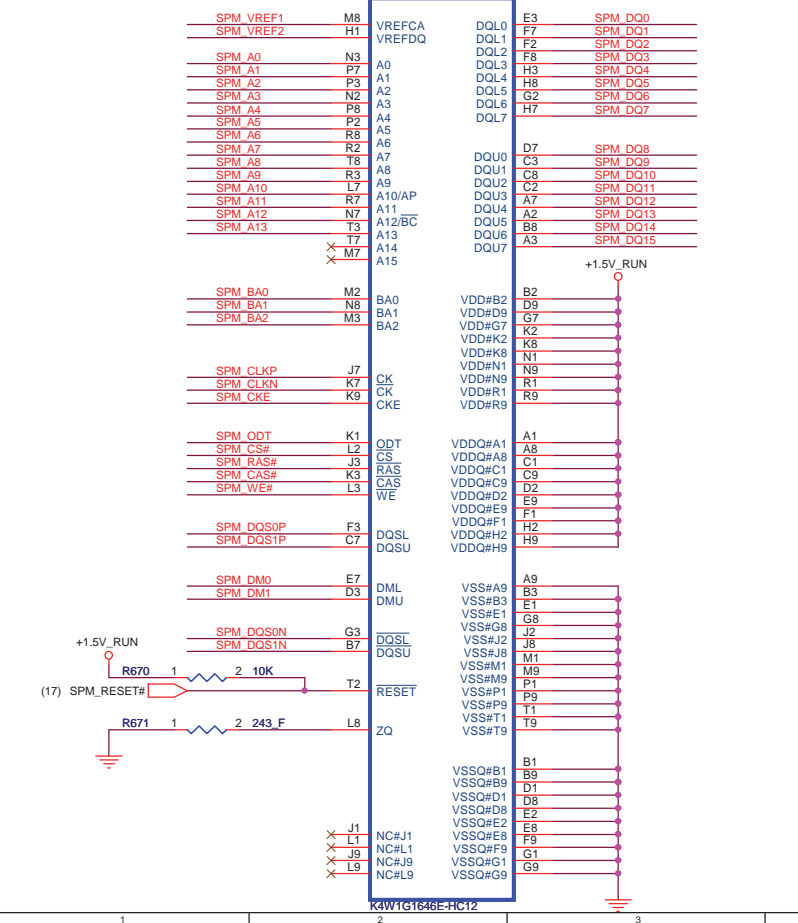
U10C
PART 3 OF 6



Side Port/ Strapping



2'nd source:
DELH-14D00A0000003G -- IC DDR3 H5TQ1G63BFR-12C 1Gbits FBGA-36



RS880M H/W STRAPS

STRAP_DEBUG_BUS_GPIO_ENABLEB

Enables the Test Debug Bus using GPIO.
DAC_VSYNC (RS880.Pin B11)
1 = Disable (default)
0 = Enable



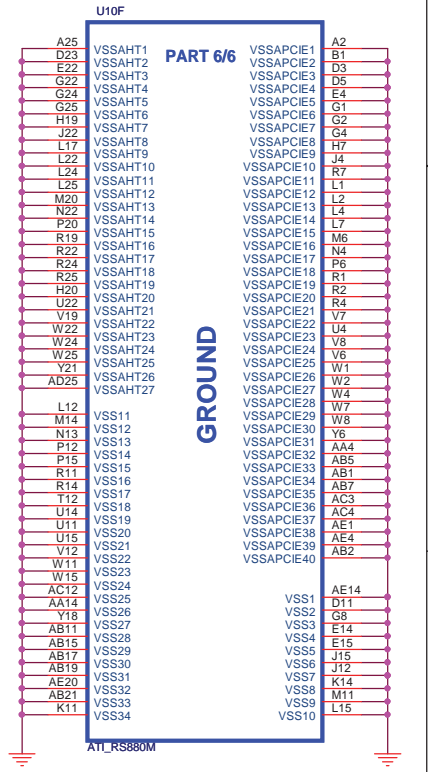
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EEPROM.
SUS_STAT# (RS880.Pin D12)
1 = Bypass the loading of EEPROM straps and use Hardware Default Values
0 = I2C Master can load strap values from EEPROM if connected, or use default values if not connected

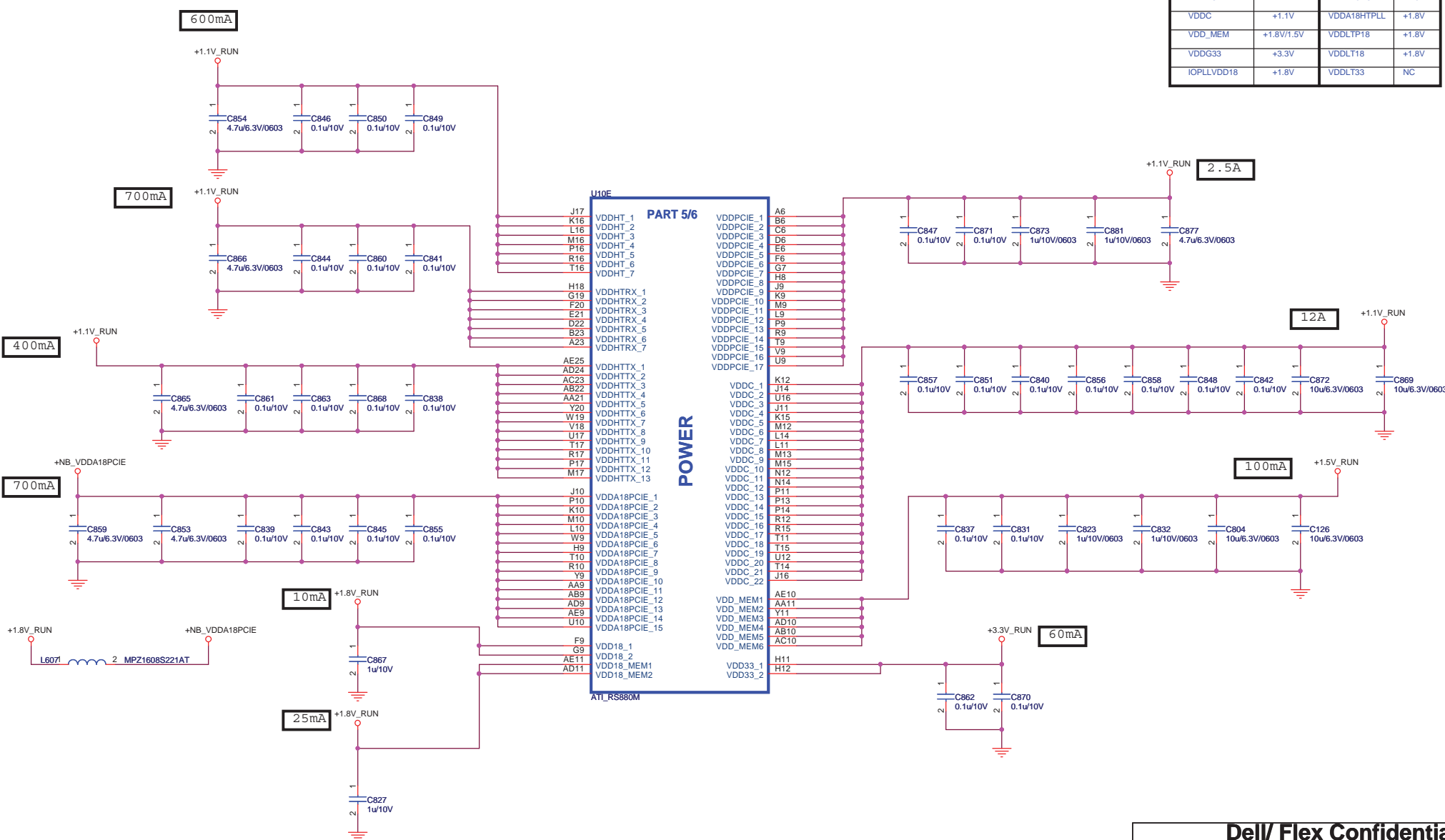


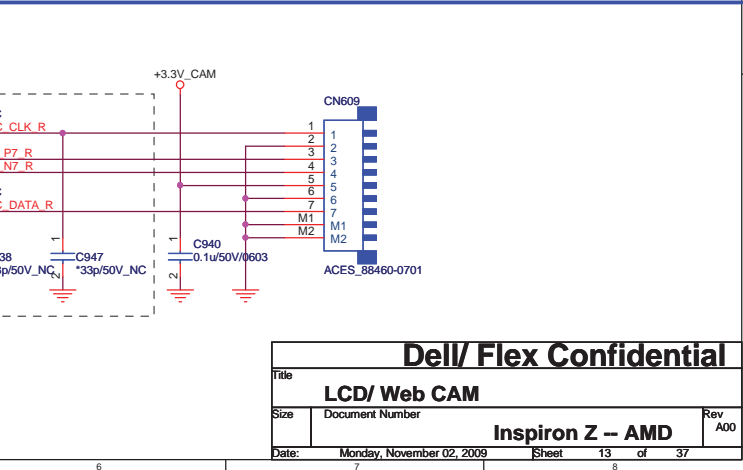
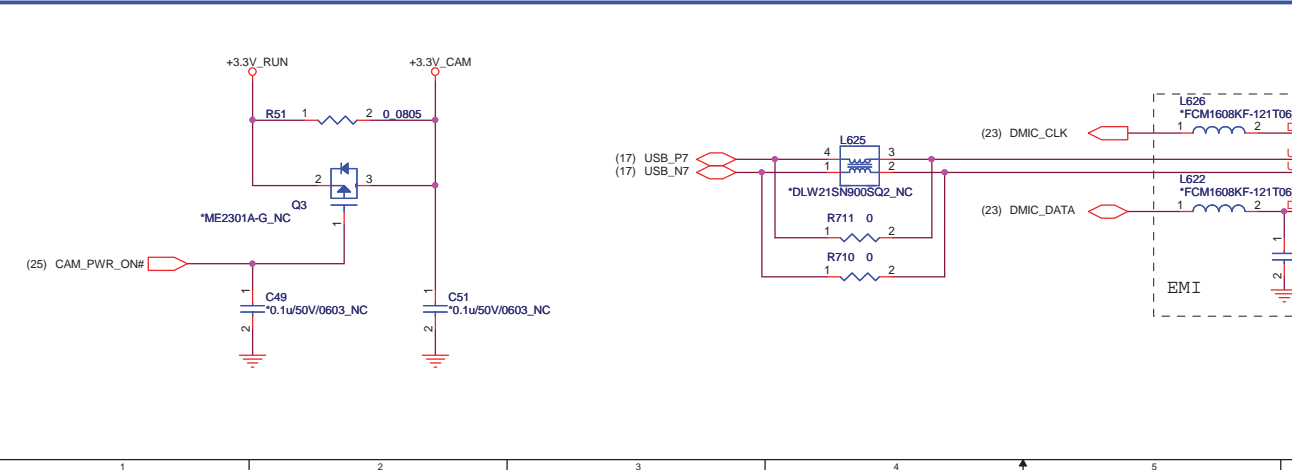
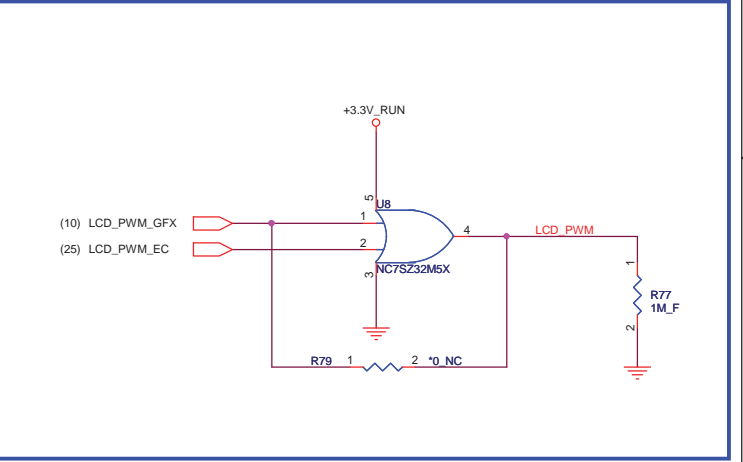
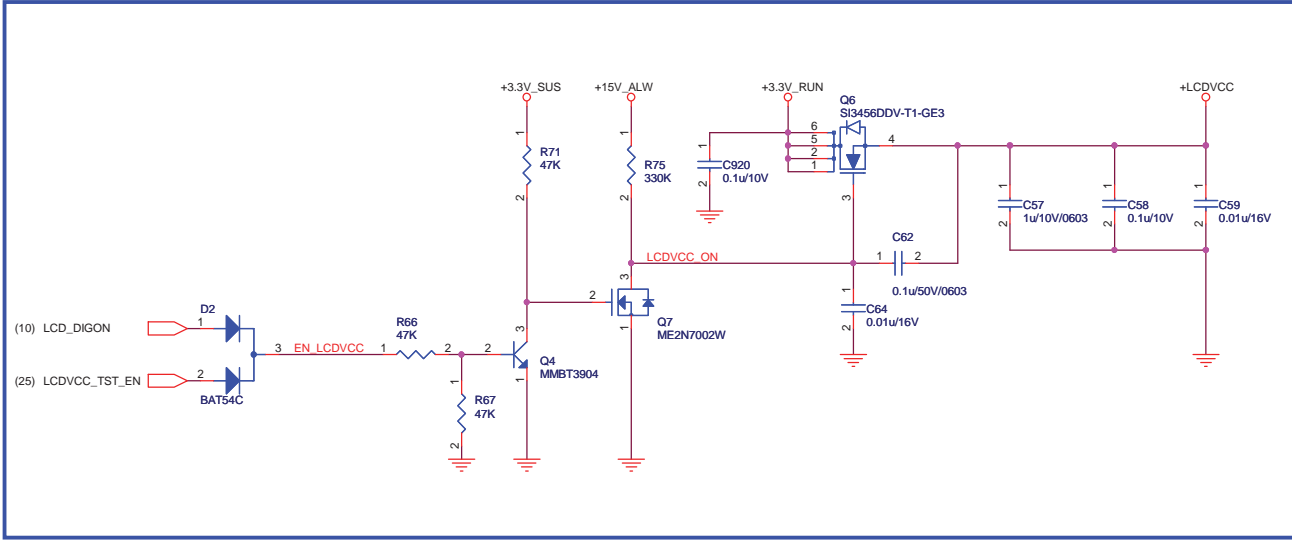
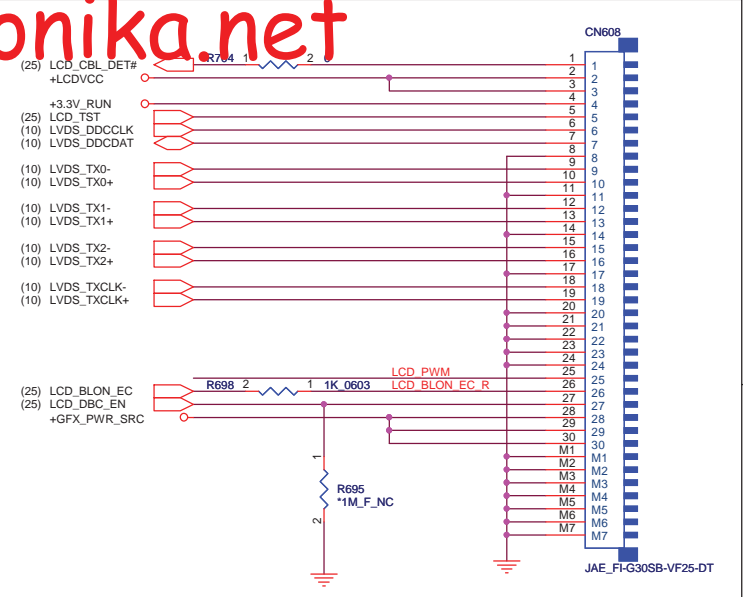
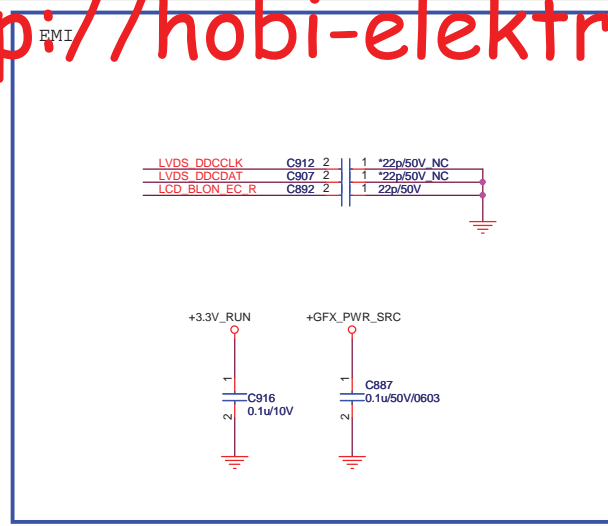
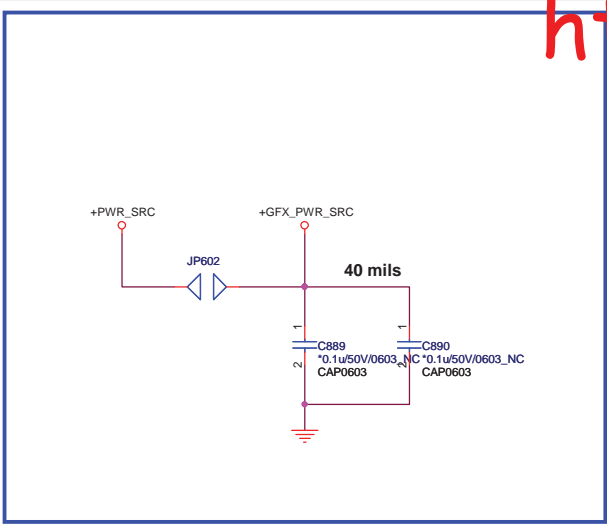
RS880: Enable Side Port Memory

Selects if Memory SIDE PORT is available or not
DAC_HSYNC (RS880.Pin A11)
1 : Disable (default)
0 : Enable
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

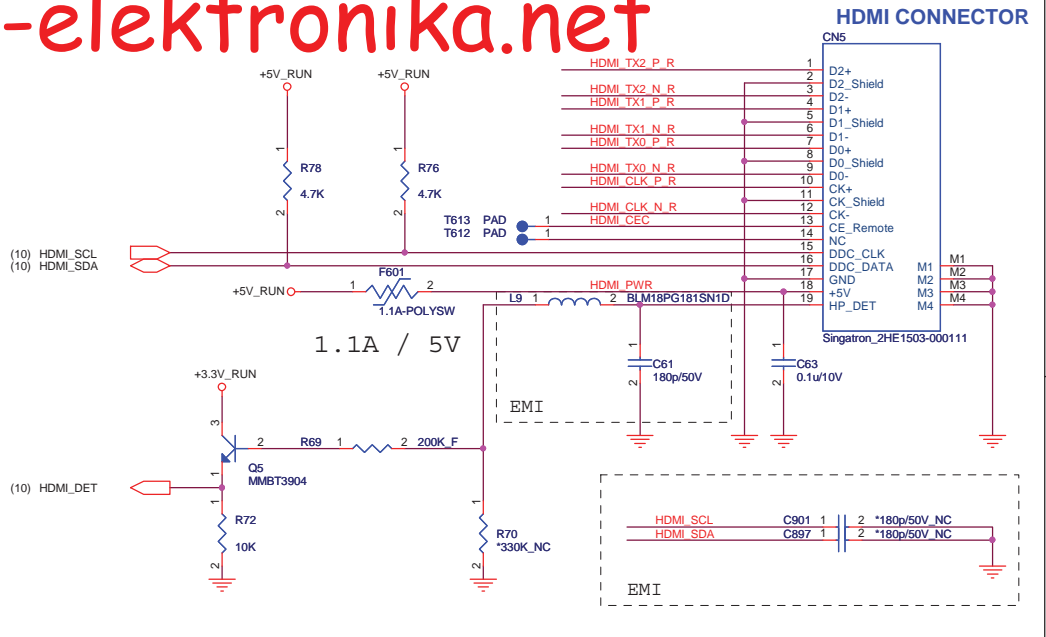
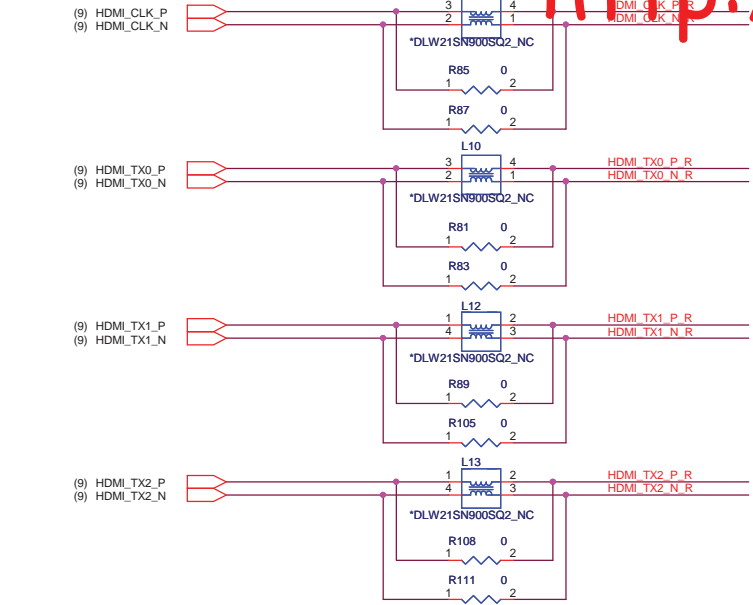


PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.1V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC

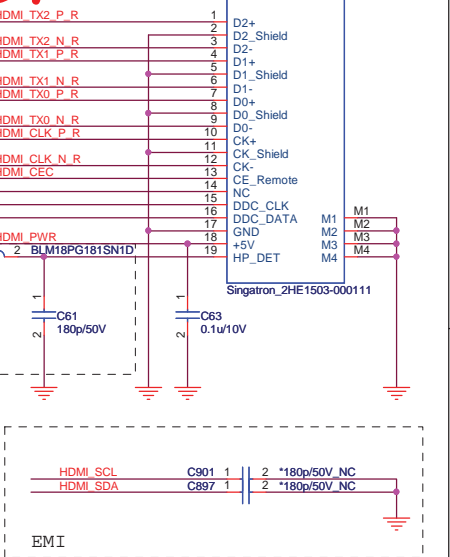




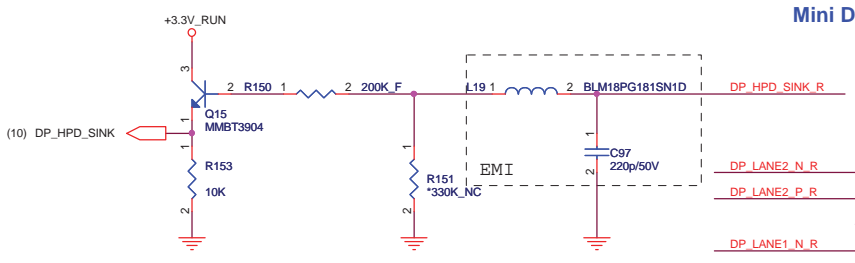
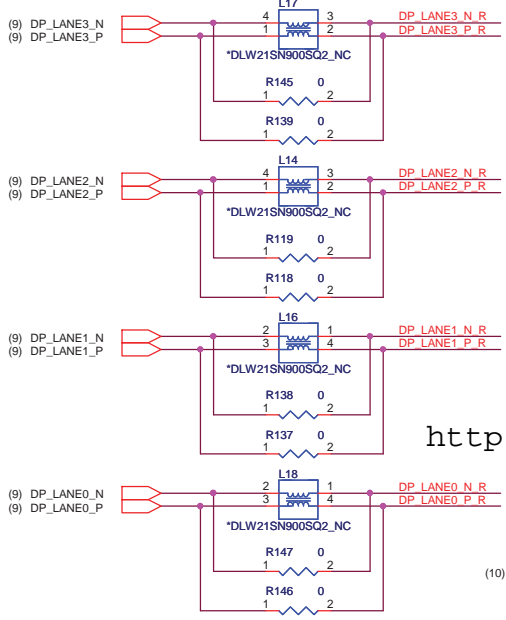
Reserve For EMI



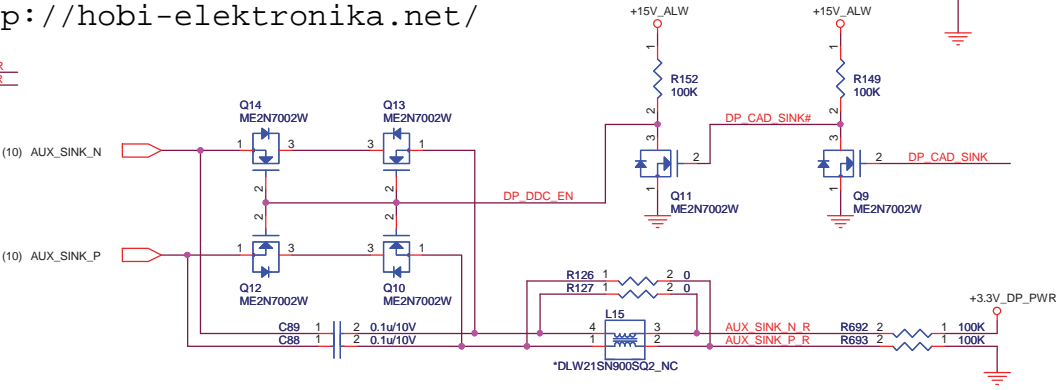
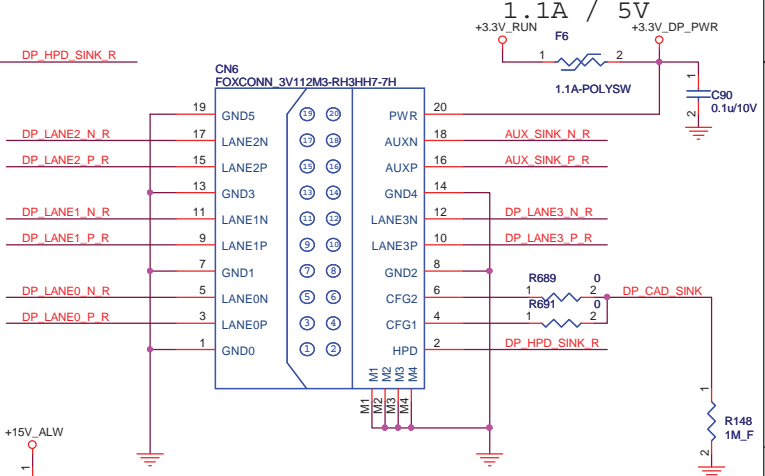
HDMI CONNECTOR

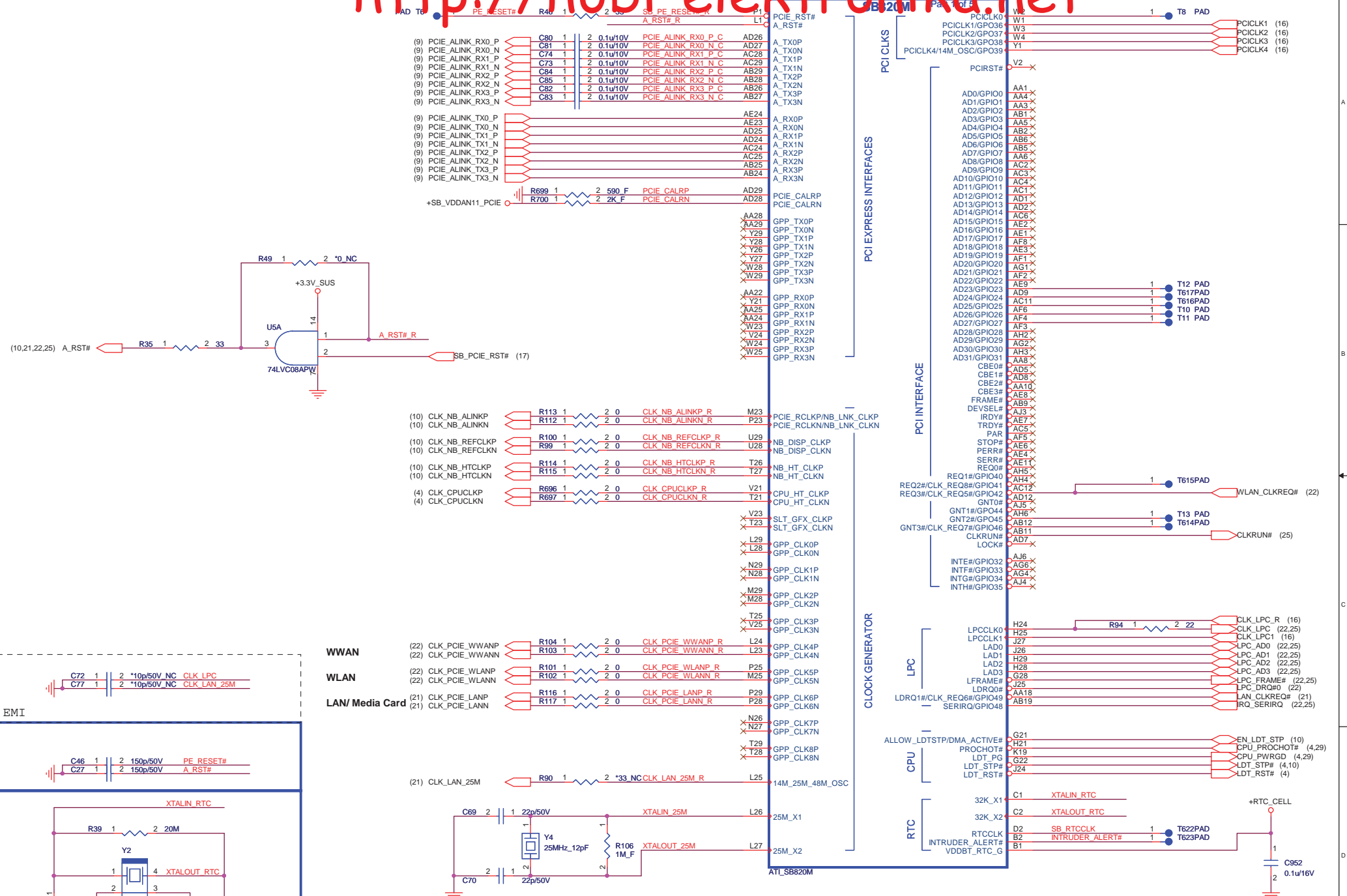


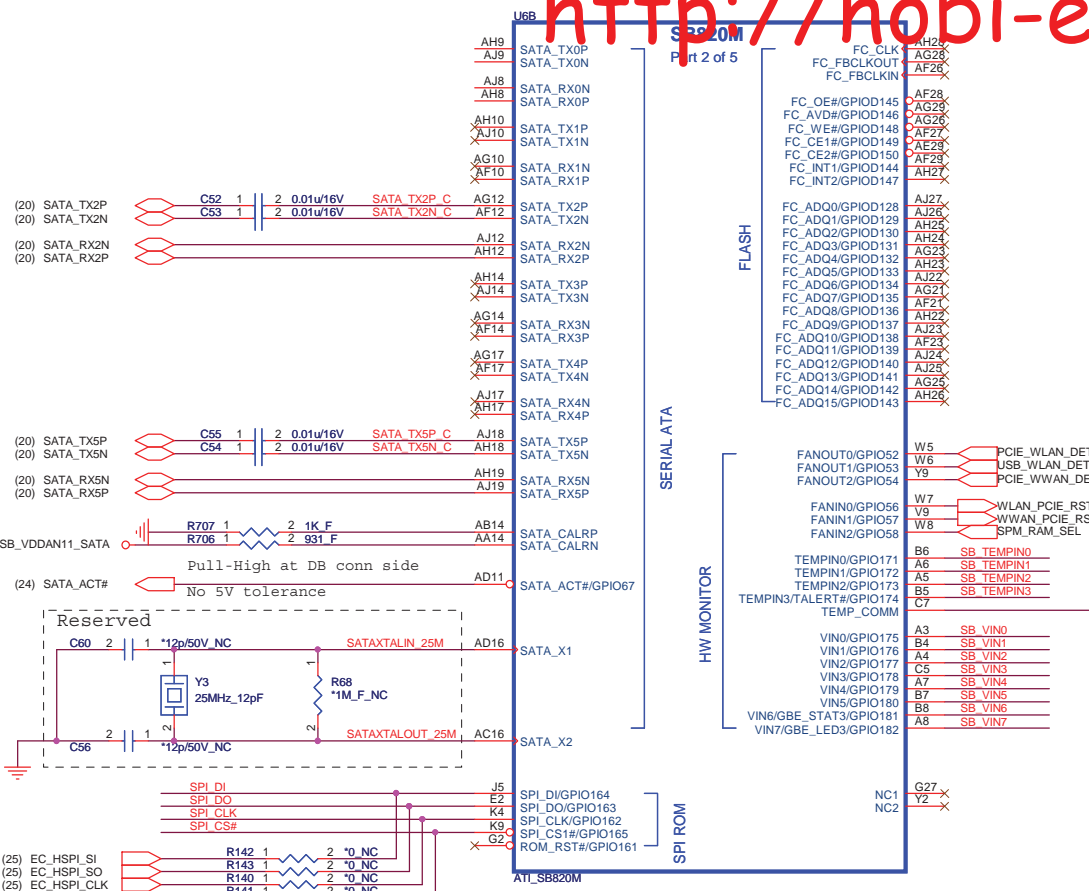
Reserve For EMI



Mini DISPLAY PORT CONNECTOR







ECEnableStrap (LPCCLK0)

Embedded Controller (EC):
L: Disable
H: Enable

(15) CLK_LPC_R

CLKGEN (LPCCLK1)

Define Clock Generator:
L: External clock mode
H: Internal clock mode

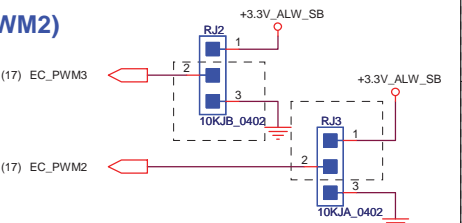
(15) CLK_LPC1

ROMTYPE_1&0 (EC_PWM3& EC_PWM2)

ROMTYPE_1	ROMTYPE_0	ROM type
0	0	FWH
0	1	LPC& PMC ROM
1	0	SPI
1	1	Reserve

(17) EC_PWM3

(17) EC_PWM2



BIF_GEN2_COMPLIANCE_Strap (PCI CLK1)

Set PCIe to Gen II mode:
SB820M: Only provision for Pull down is required, not install by default.

(15) PCICLK1

BootFailTmrEn (PCI CLK2)

Watchdog function:
L: Disable BootFailtmr function
H: Enable BootFailtmr function

(15) PCICLK2

DefaulStrapMode (PCI CLK3)

Default Debug Straps:
L: Disable Debug Straps
H: Select external Debug Straps

(15) PCICLK3

CPUClkSel (PCI CLK4)

CPU/ NB HT Clock Selection:
L: Reserved
H: Required setting for integrated clock mode

(15) PCICLK4

SB820M Debug Straps

PciIIByp (PCI AD27)

Bypass PCI PLL
(Used in functional test at tester):
L: Bypass internal PLL clock
H: Use internal PLL generated PLL CLK
(Internal Pull-Up of 15Kohm)

ILAAutorunEnB (PCI AD26)

ILA Auto run Enable
L: ILA Auto run enable
H: ILA Auto run disable
(Internal Pull-Up of 15Kohm)

FCCKByP (PCI AD25)

Bypass FC CLK
L: Bypass internal FC CLK
(Used in functional test at tester)
H: Use internal FC CLK

I2CROMEn (PCI AD24)

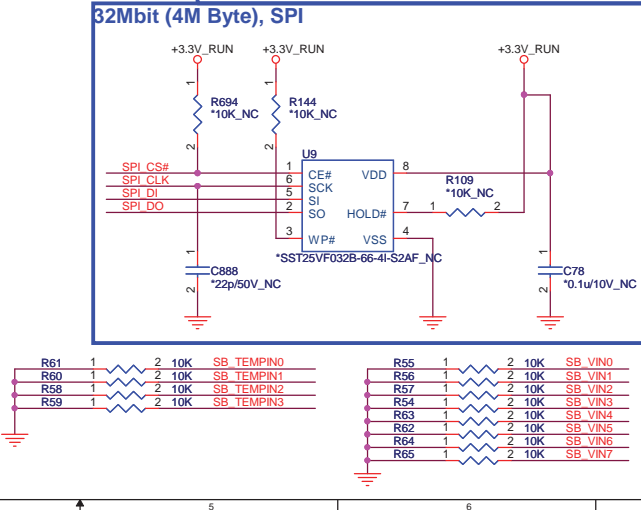
I2C ROM Enable. Load the setting for A-Link Express/ PLL/ music control from I2C ROM
L: Getting the value from I2C EPROM
H: Disable I2C ROM
(Internal Pull-Up of 15Kohm)

PCI_ROM_BOOT (PCI AD23)

Bootting from PCI memory
L: Route ROM fetch tp PCI bus on the very first boot. Use ROMTYPE to determine the ROM type on the subsequent boots.
H: Use ROMTYPE straps to determine the ROM type
(Internal Pull-Up of 15Kohm)

PCIe EEPROM Data/ Clock (PCI_REQ3/ PCI_GNT3)

PCIe EEPROM Data/ Clock
Connected to PCIe EEPROM SDA/ SCL pin or provided test point access for lad use.



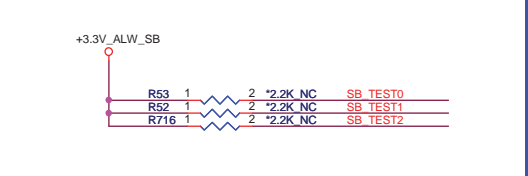
CoreSpeedMode (AZ_SDOUT)

Slow down core clock for low power mobile platform:
L: Performance Mode
H: Low Power Mode

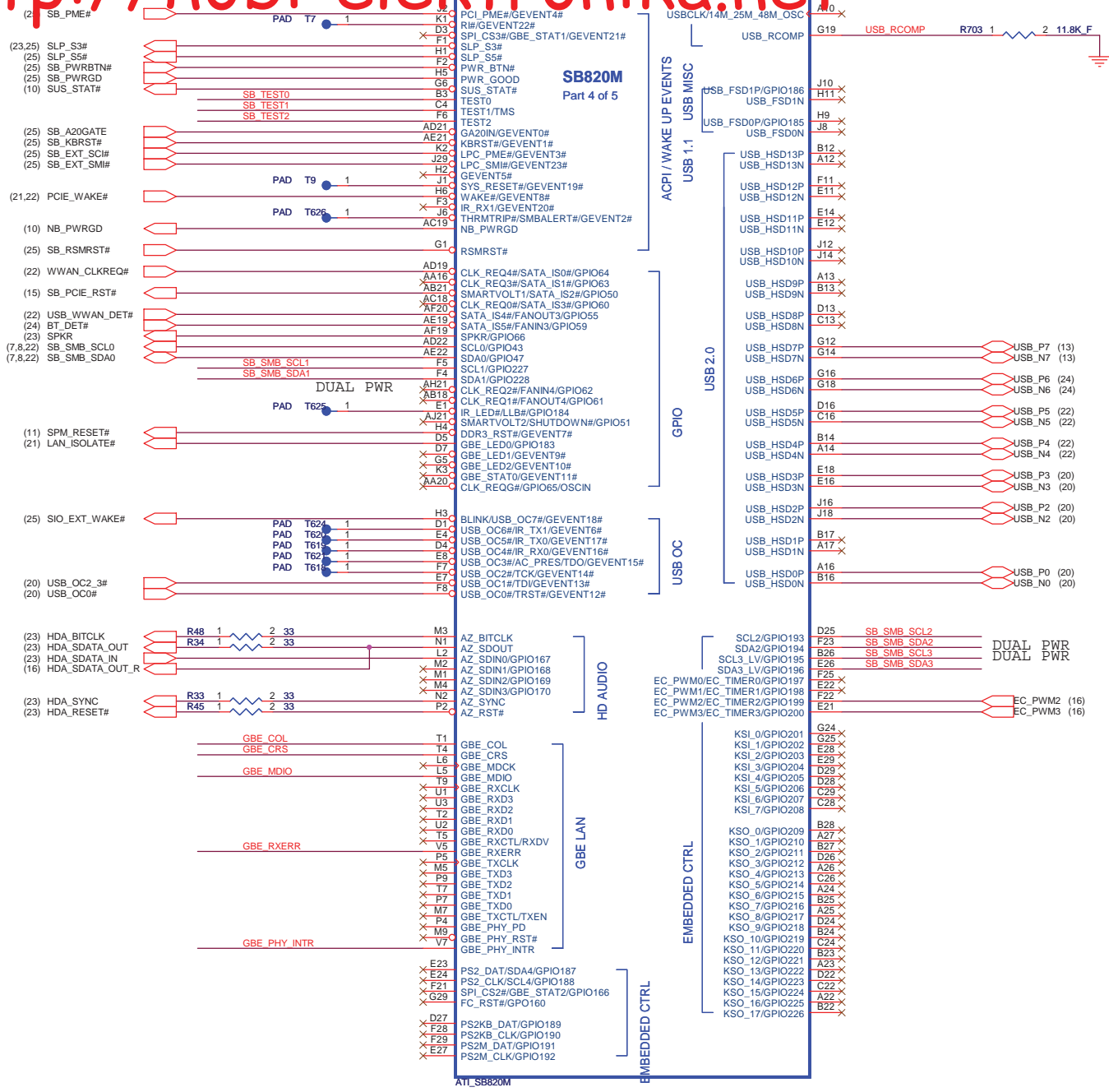
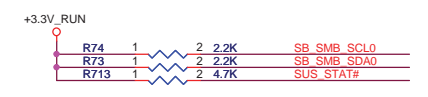
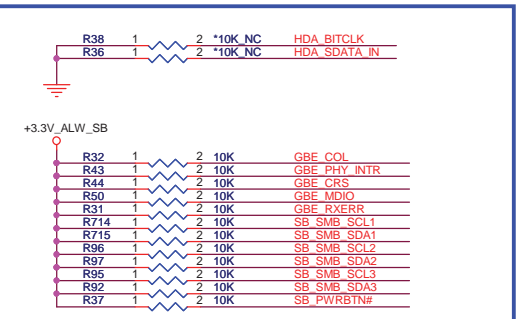
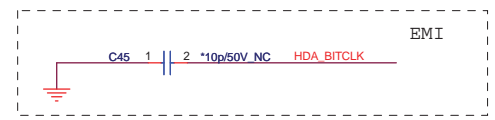
(17) HDA_SDATA_OUT_R

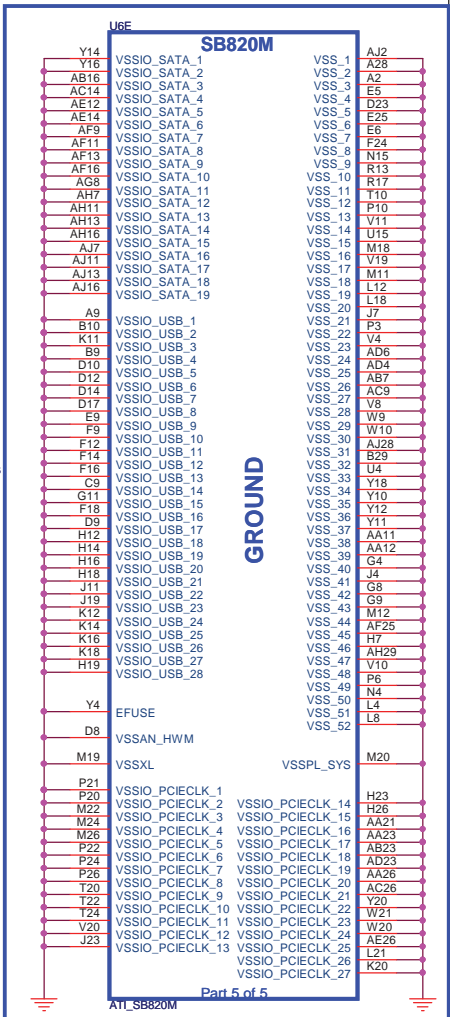
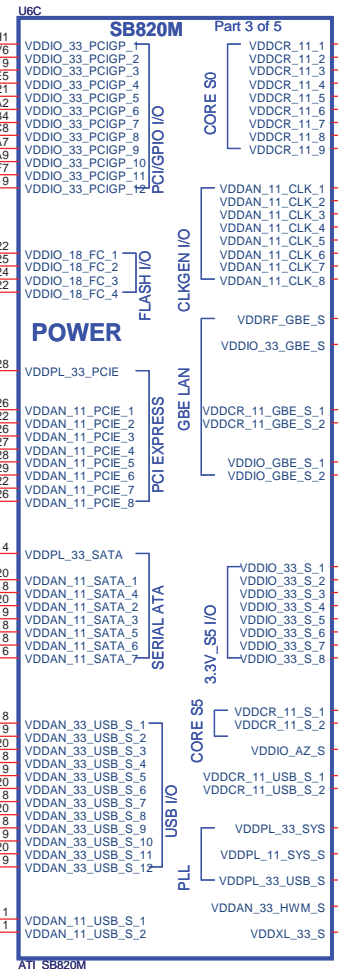
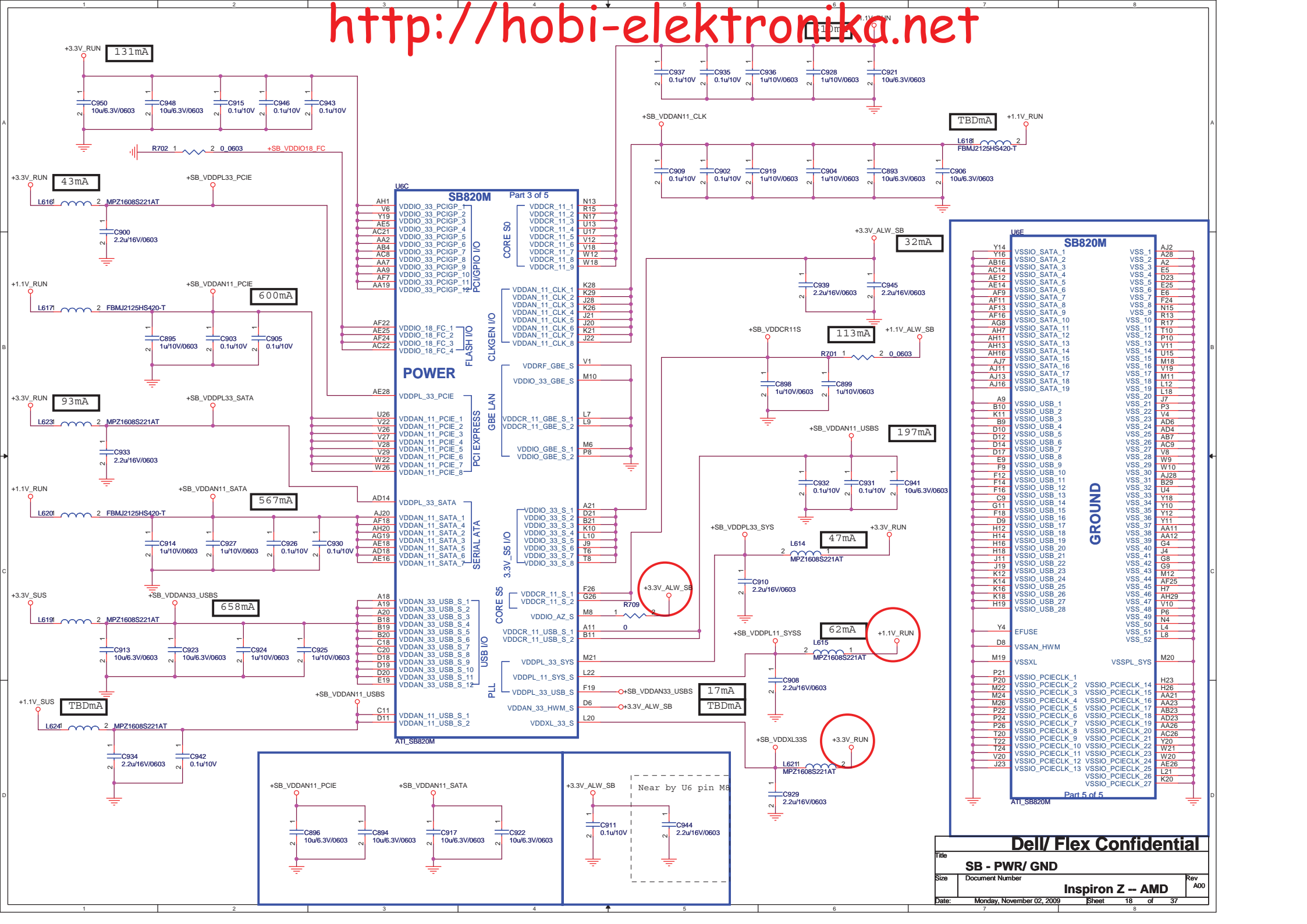
SB820M Debug Straps

SB820M
Part 4 of 5



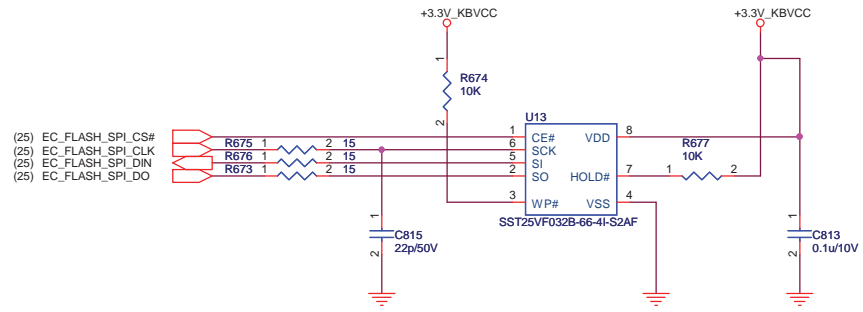
RUN PWR
DUAL PWR



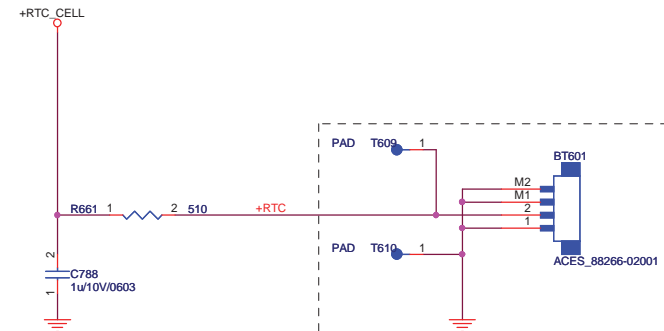


RTC/ SPI

32Mbit (4M Byte), SPI



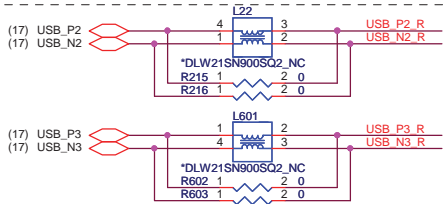
RTC BATTERY



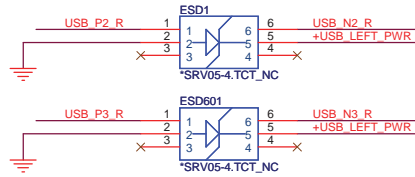
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Title		RTC/ SPI	
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USB Jack x 2

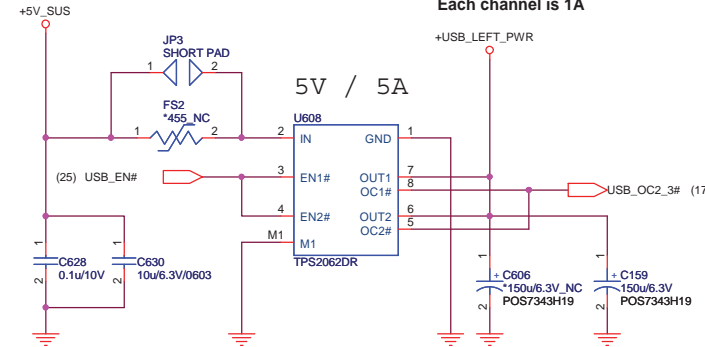


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



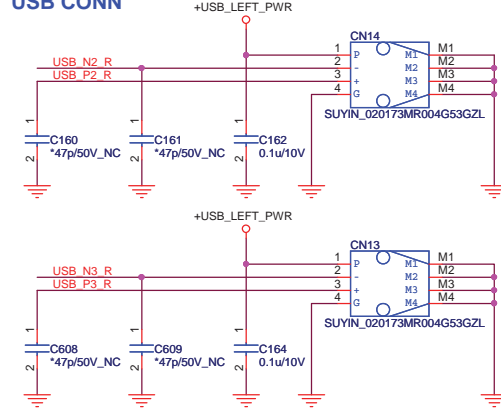
Place ESD diodes as close as USB connector.

USB POWER SW



Place one 150uF cap by each USB connector.

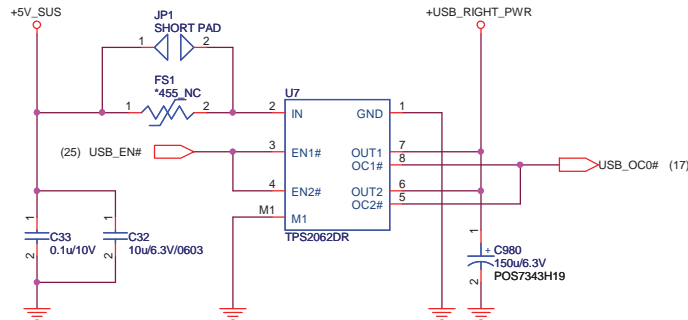
USB CONN



eSATA Connector

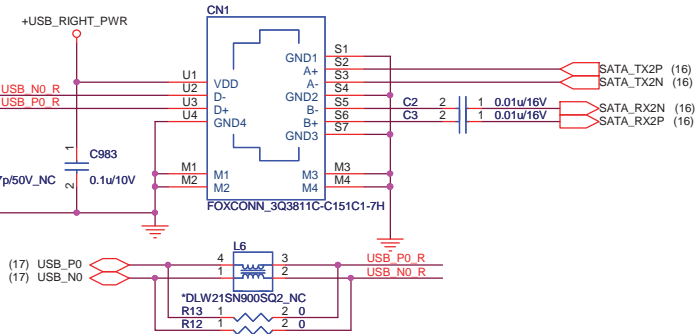
USB POWER SW

Each channel is 1A

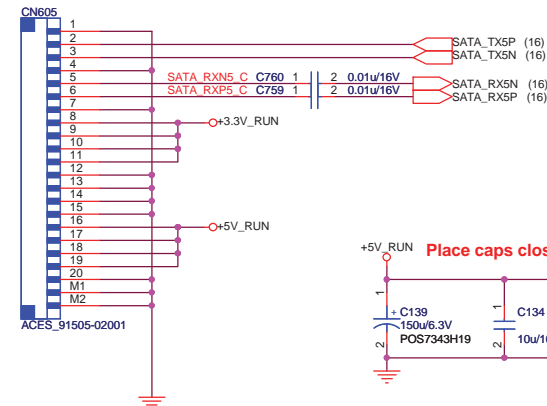


Place one 150uF cap by each USB connector.

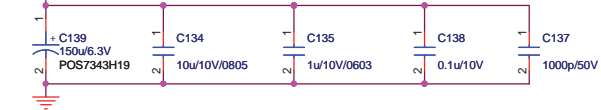
ESATA/B CONN



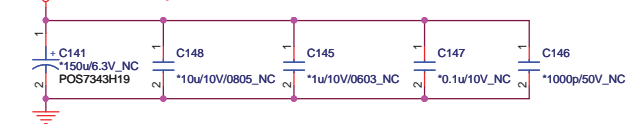
SATA HDD Connector



Place caps close to connector.

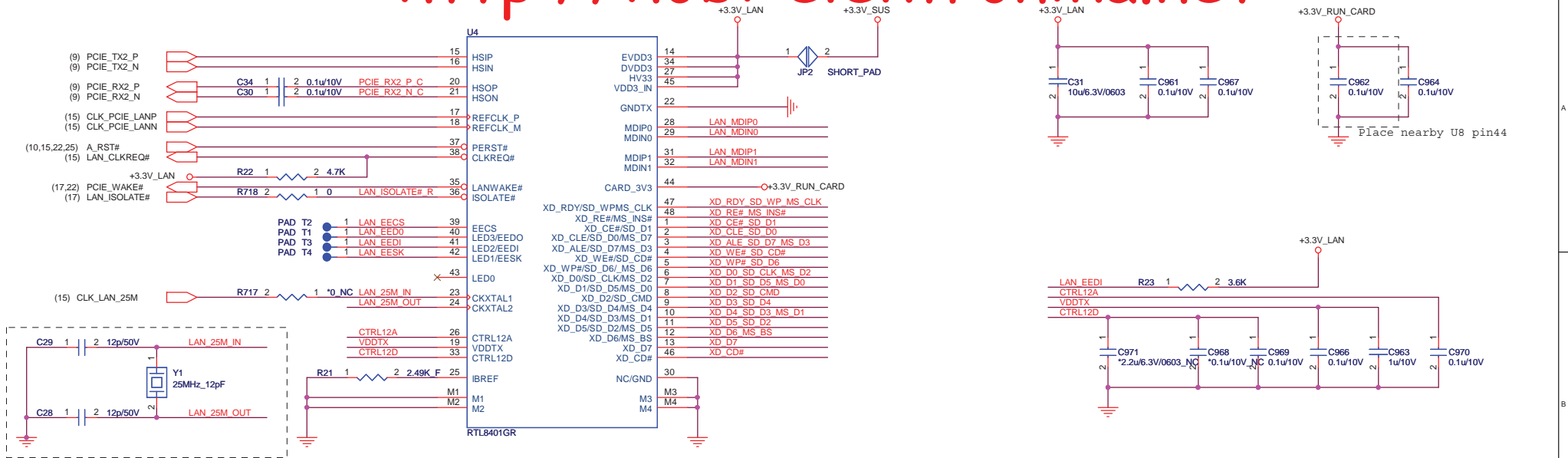


Place caps close to connector.



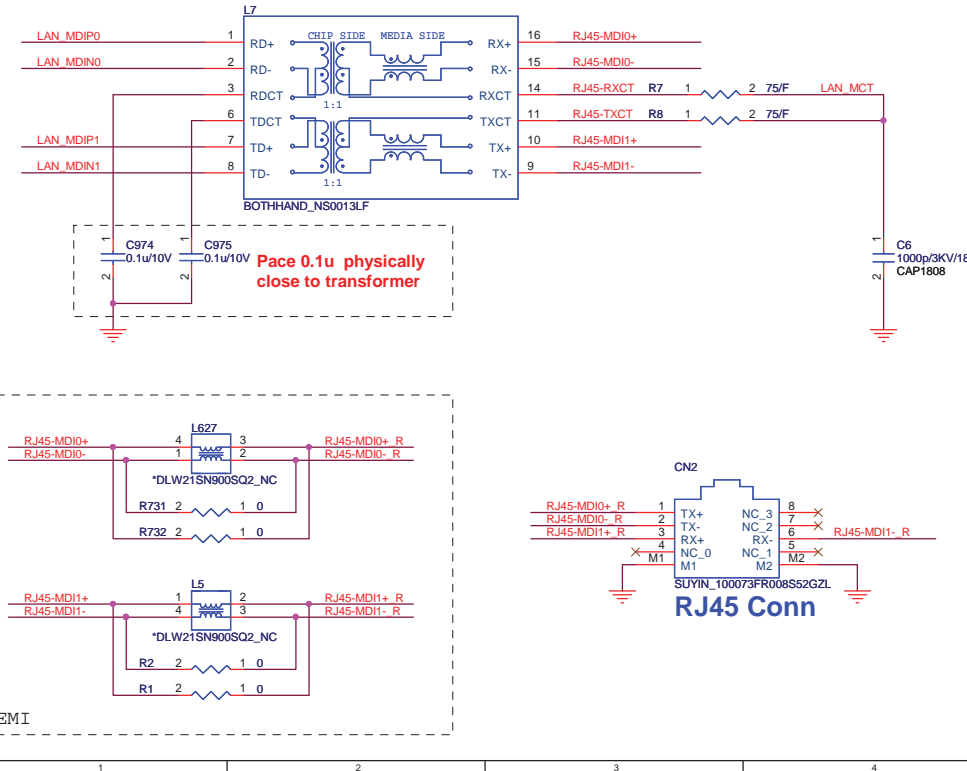
Dell/ Flex Confidential

Title		USB/ eSATA/ HDD	
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		Rev	A00



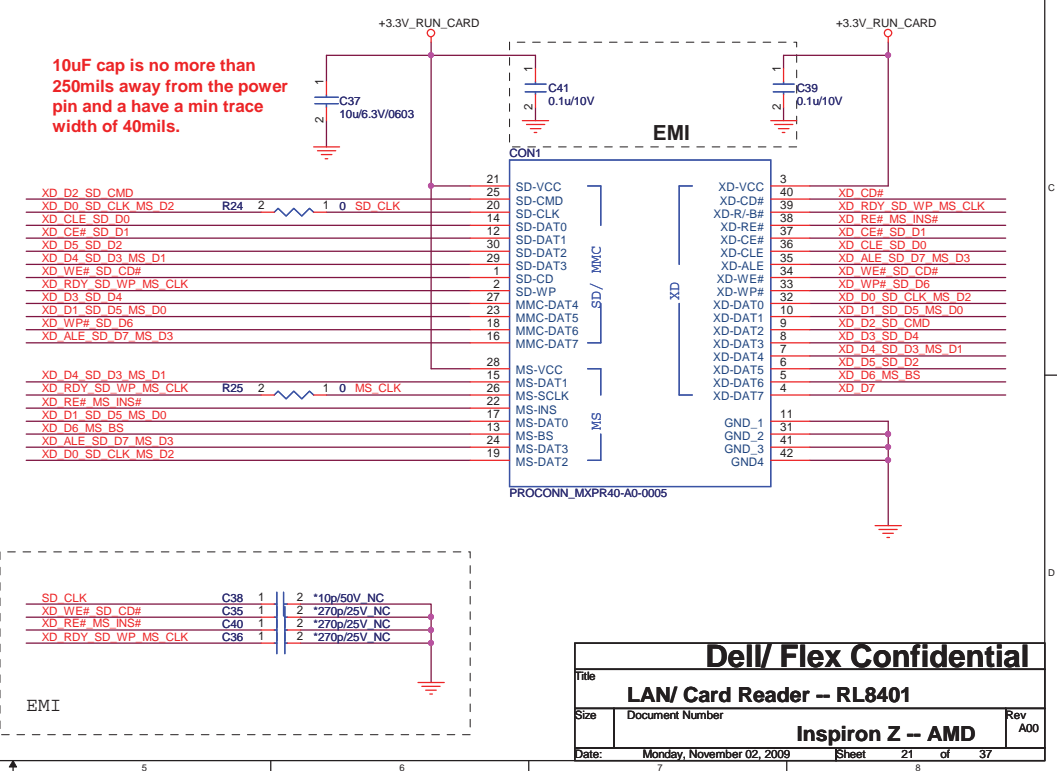
TRANSFORMER

Layout Note:
Route MDI+/- pairs with 100 ohm differential trace impedance.



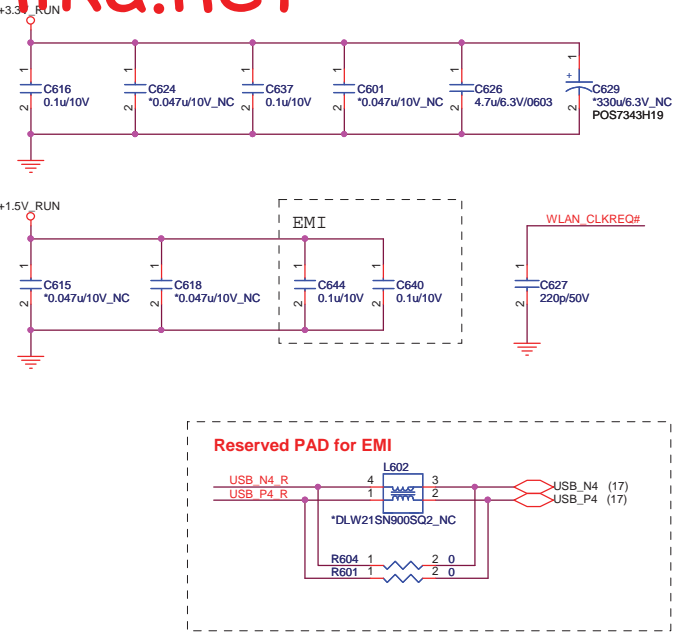
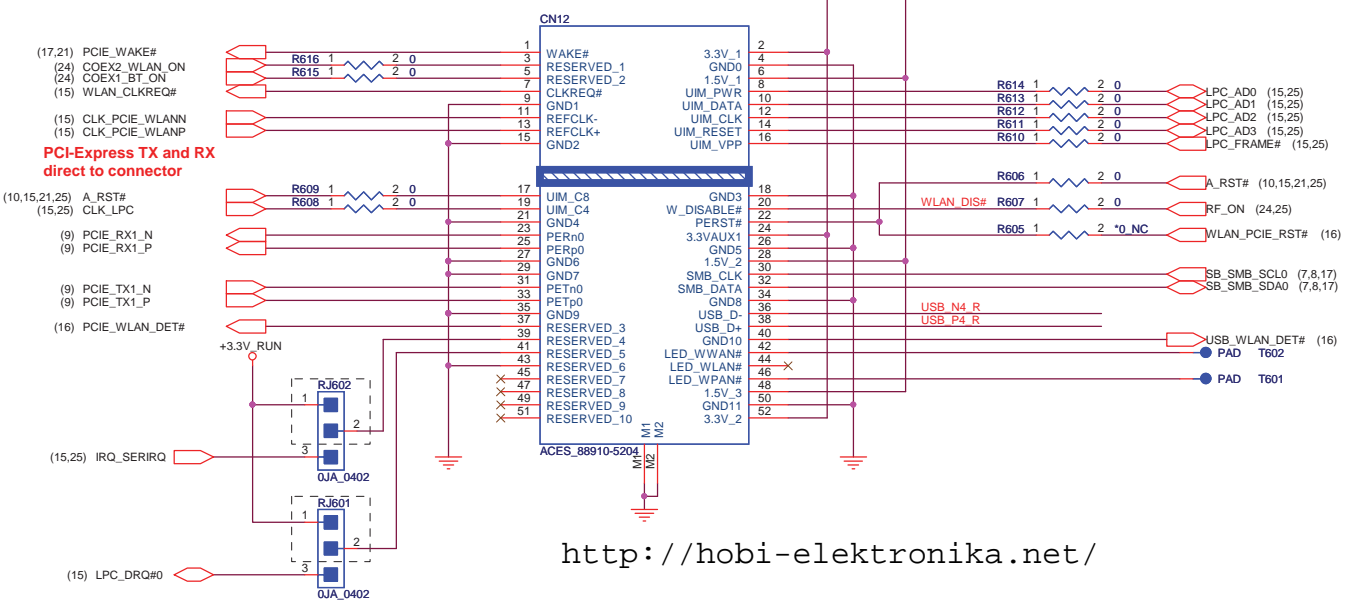
Card Reader Conn

10uF cap is no more than 250mils away from the power pin and have a min trace width of 40mils.



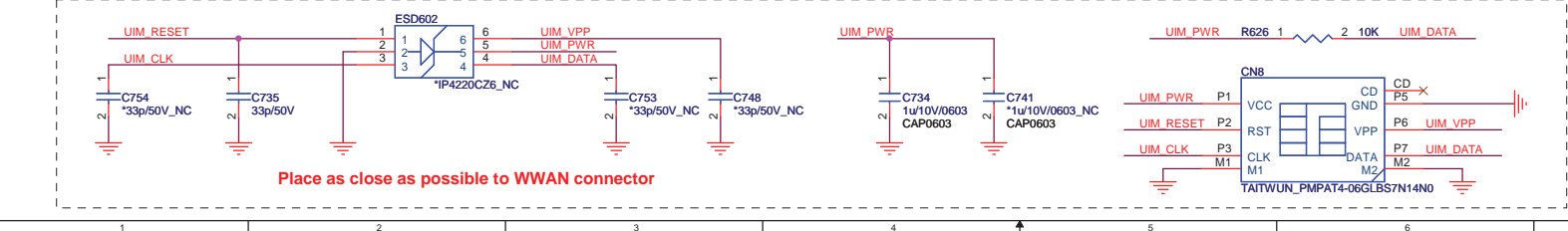
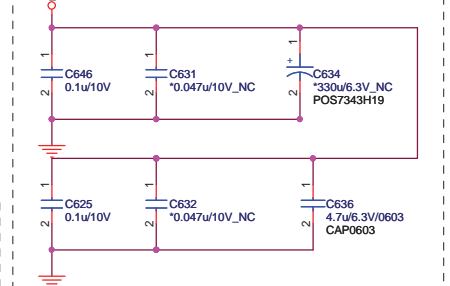
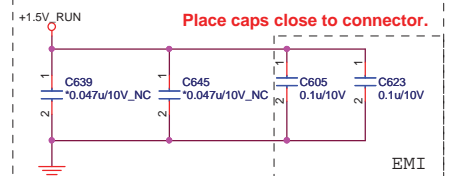
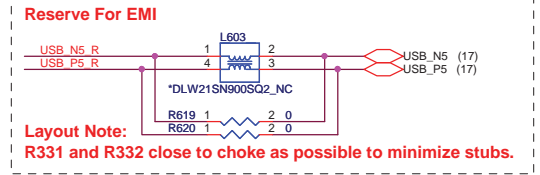
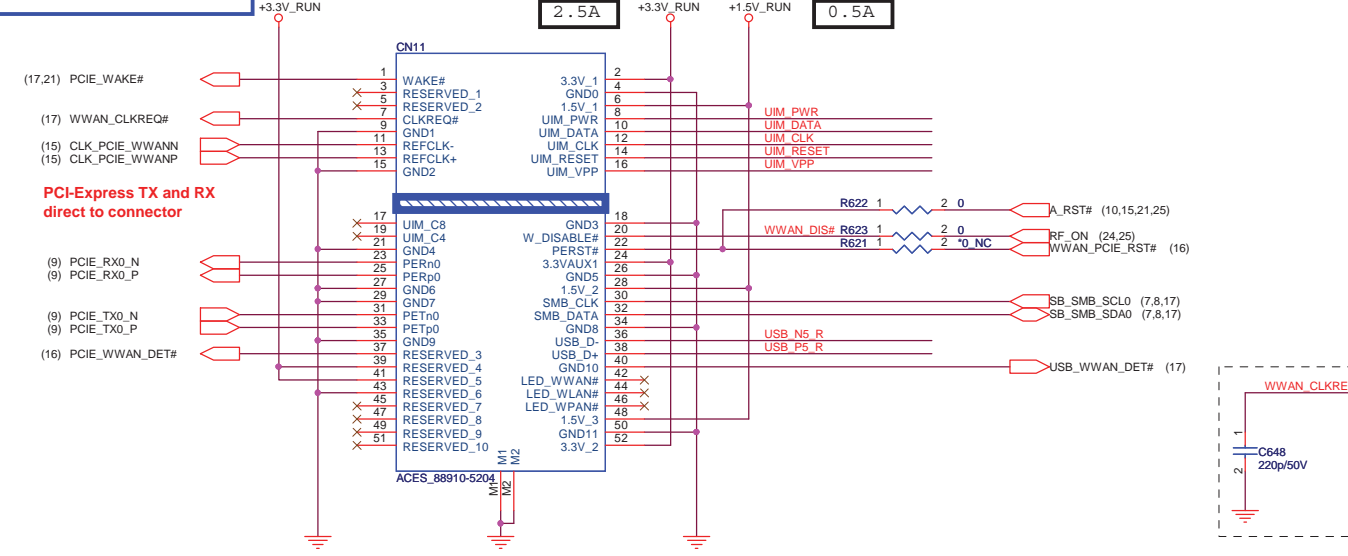
MiniCard WLAN

Place caps close to connector.

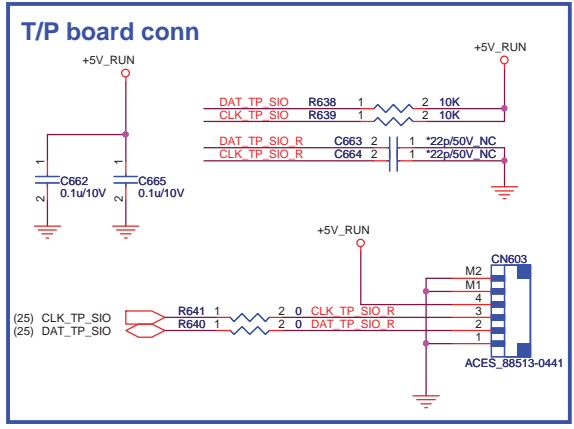
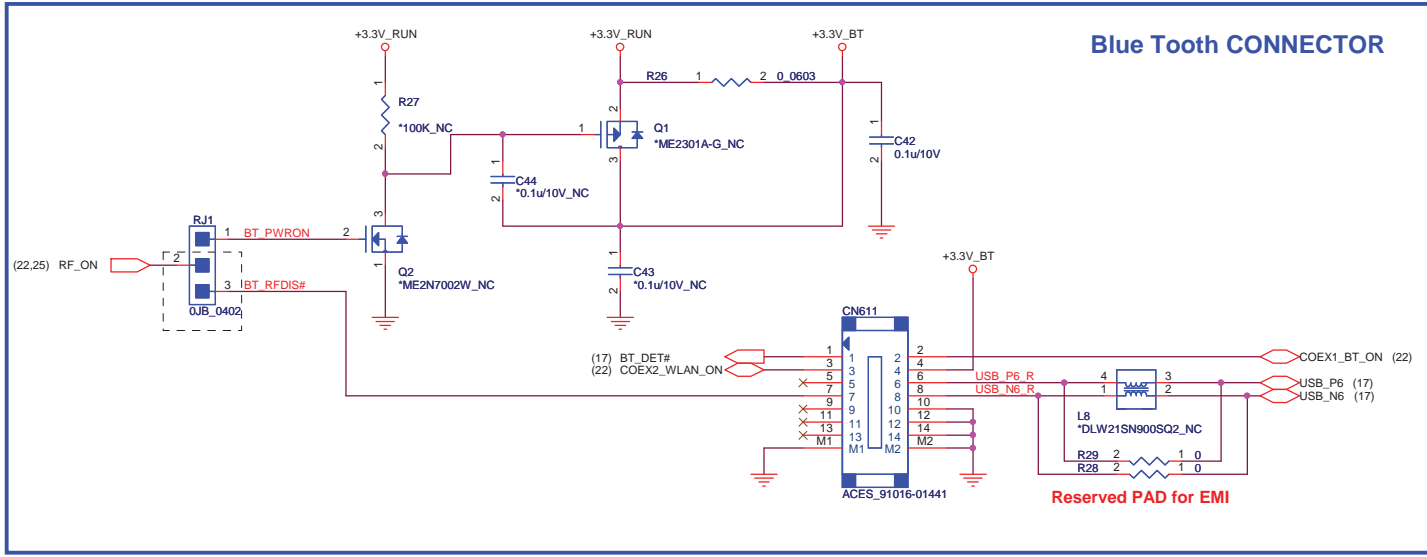
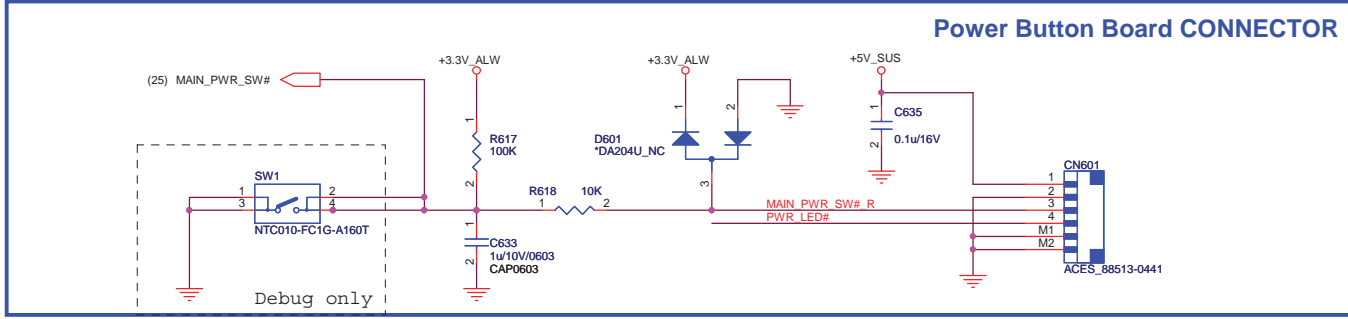
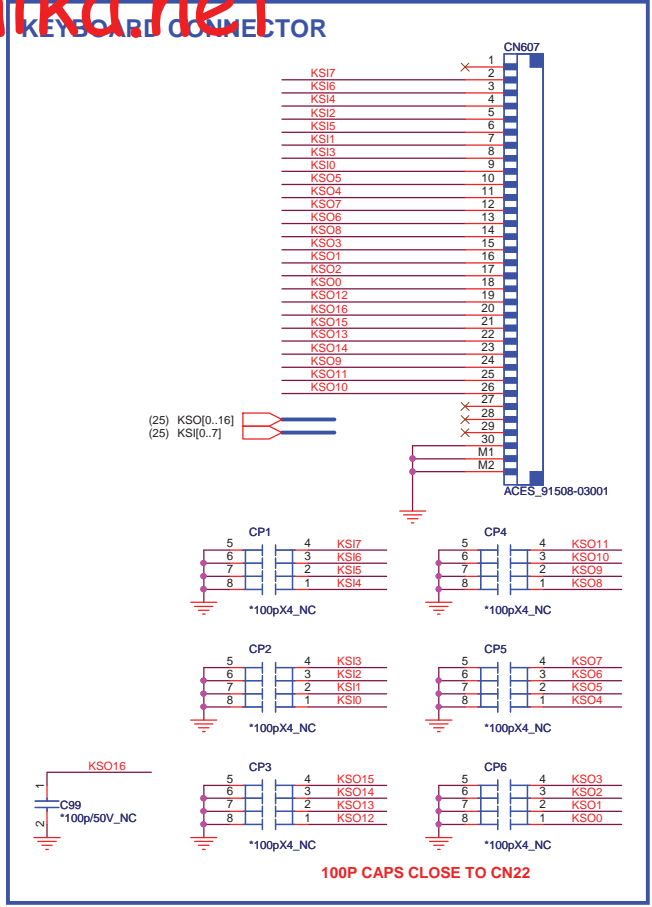
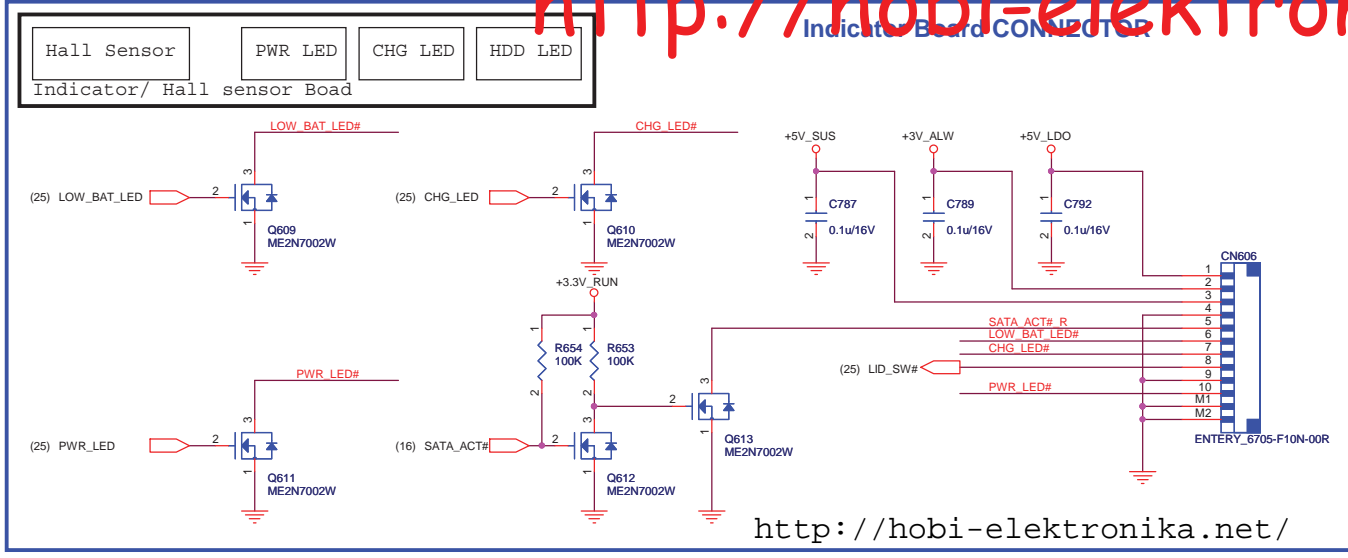


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MiniCard WWAN



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Title: WLAN/ WWAN			
Size:	Document Number:	Inspiron Z -- AMD	Rev: A00
Date:	Monday, November 02, 2009	Sheet: 22	of 37



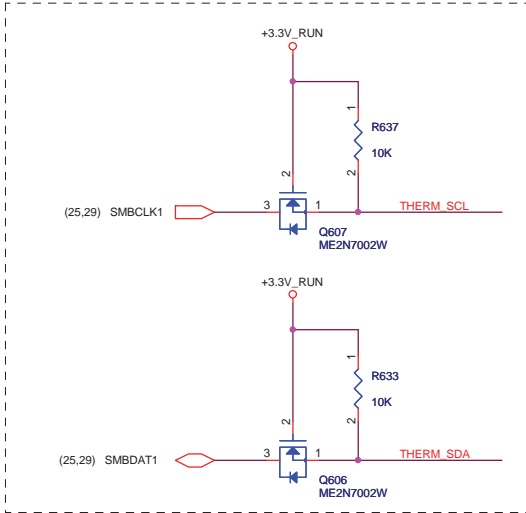
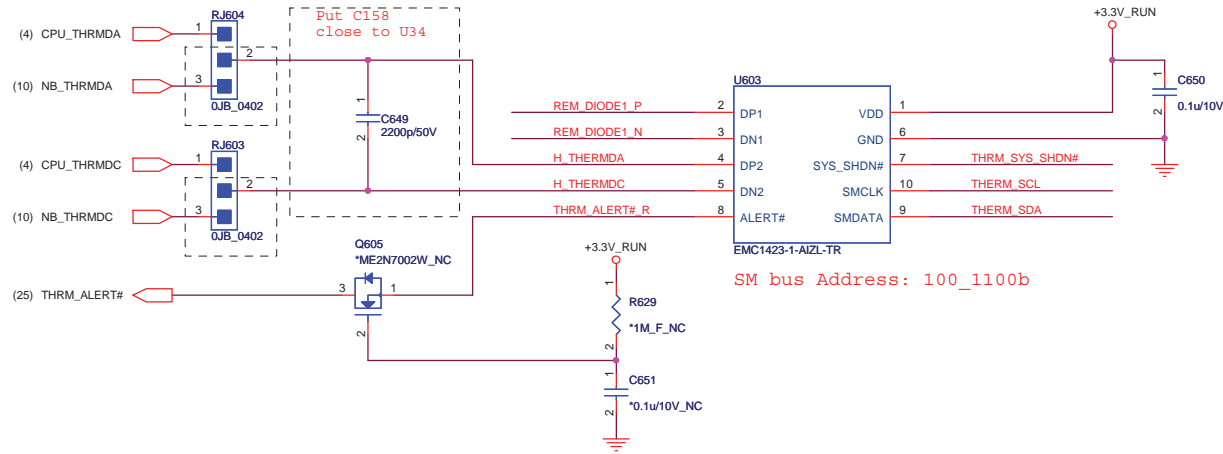
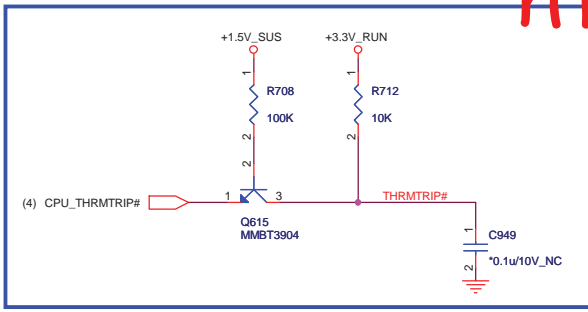
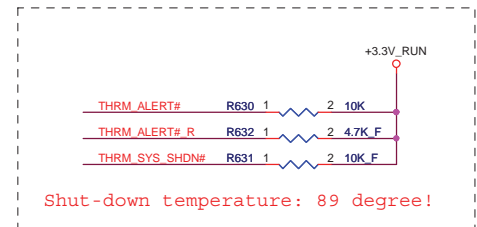
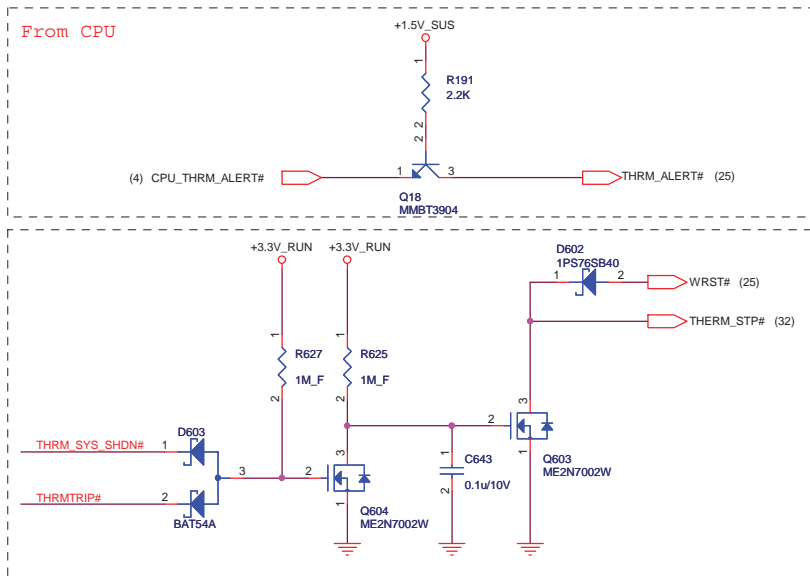
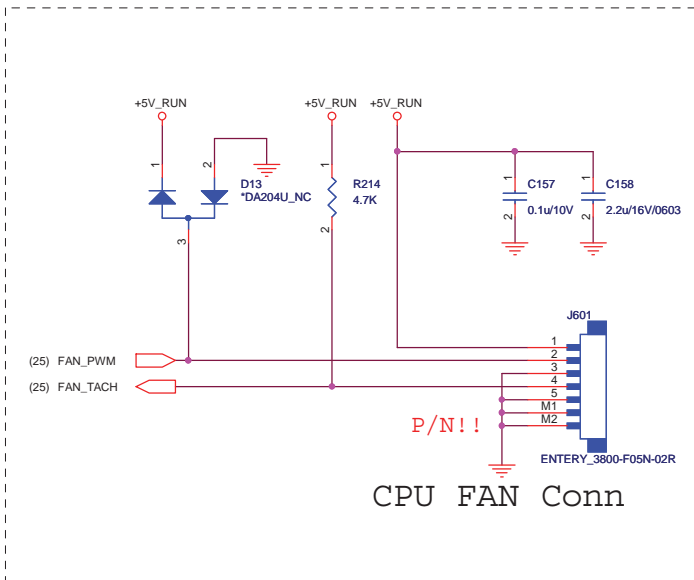


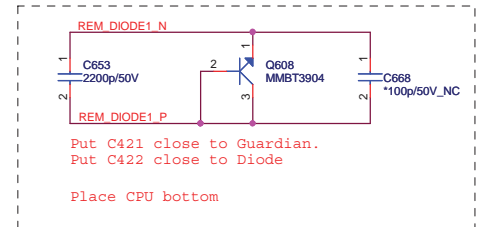
Table 5.2 SYS_SHDN Threshold Temperature

SYS_SHDN PULL-UP ALERT PULL-UP	SYS_SHDN Threshold Temperature					
	4.7K OHM ±10%	6.8K OHM ±10%	10K OHM ±10%	15K OHM ±10%	22K OHM ±10%	33K OHM ±10%
4.7K OHM ±10%	77°C	83°C	89°C	95°C	101°C	107°C
6.8K OHM ±10%	78°C	84°C	90°C	96°C	102°C	108°C
10K OHM ±10%	79°C	85°C	91°C	97°C	103°C	109°C
15K OHM ±10%	80°C	86°C	92°C	98°C	104°C	110°C
22K OHM ±10%	81°C	87°C	93°C	99°C	105°C	111°C
33K OHM ±10%	82°C	88°C	94°C	100°C	106°C	112°C

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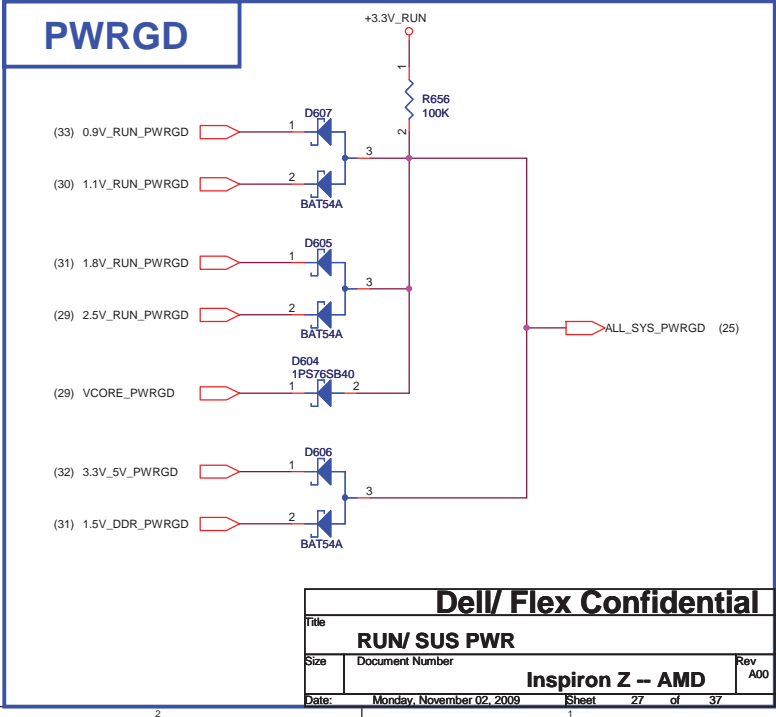
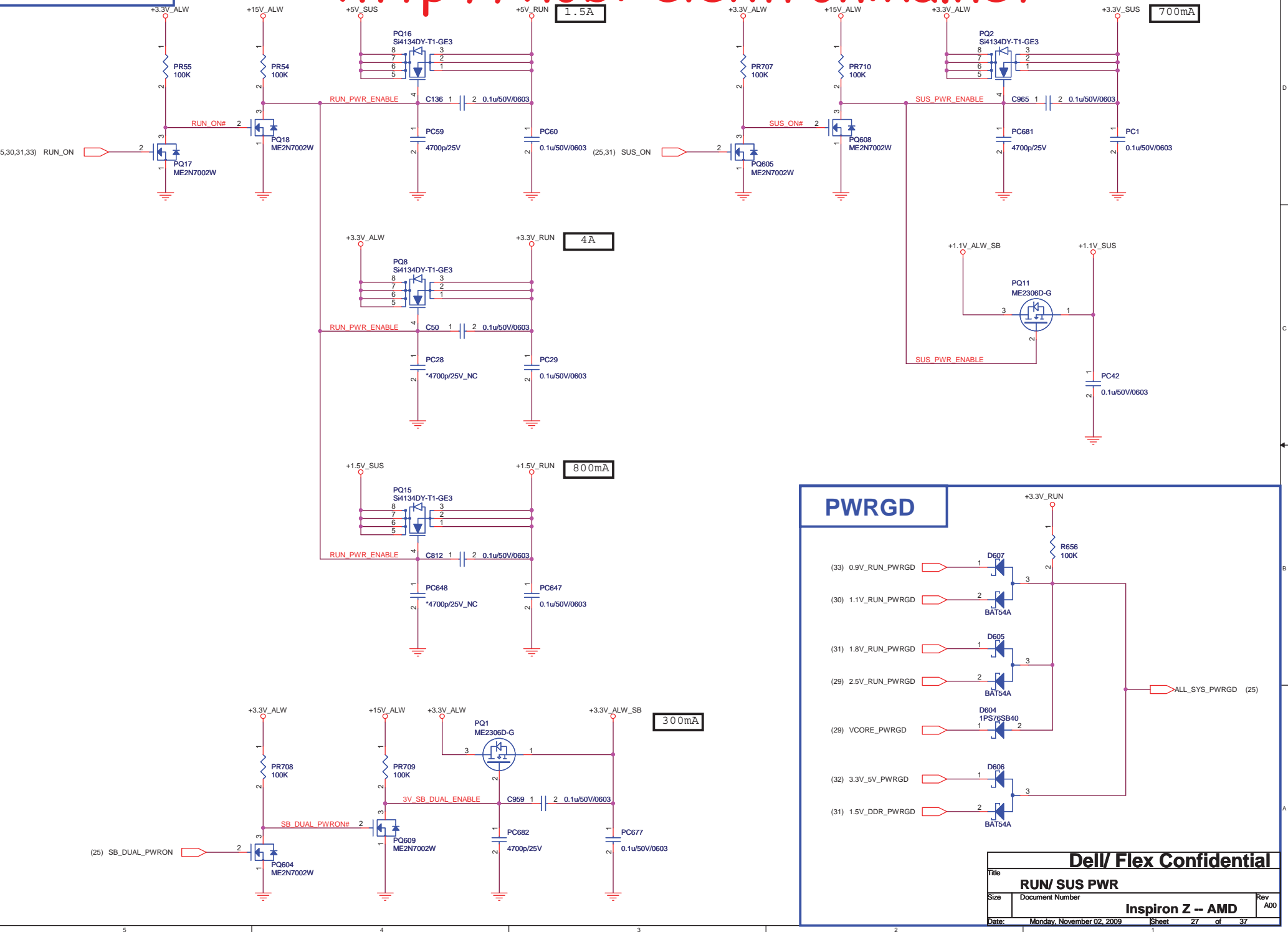


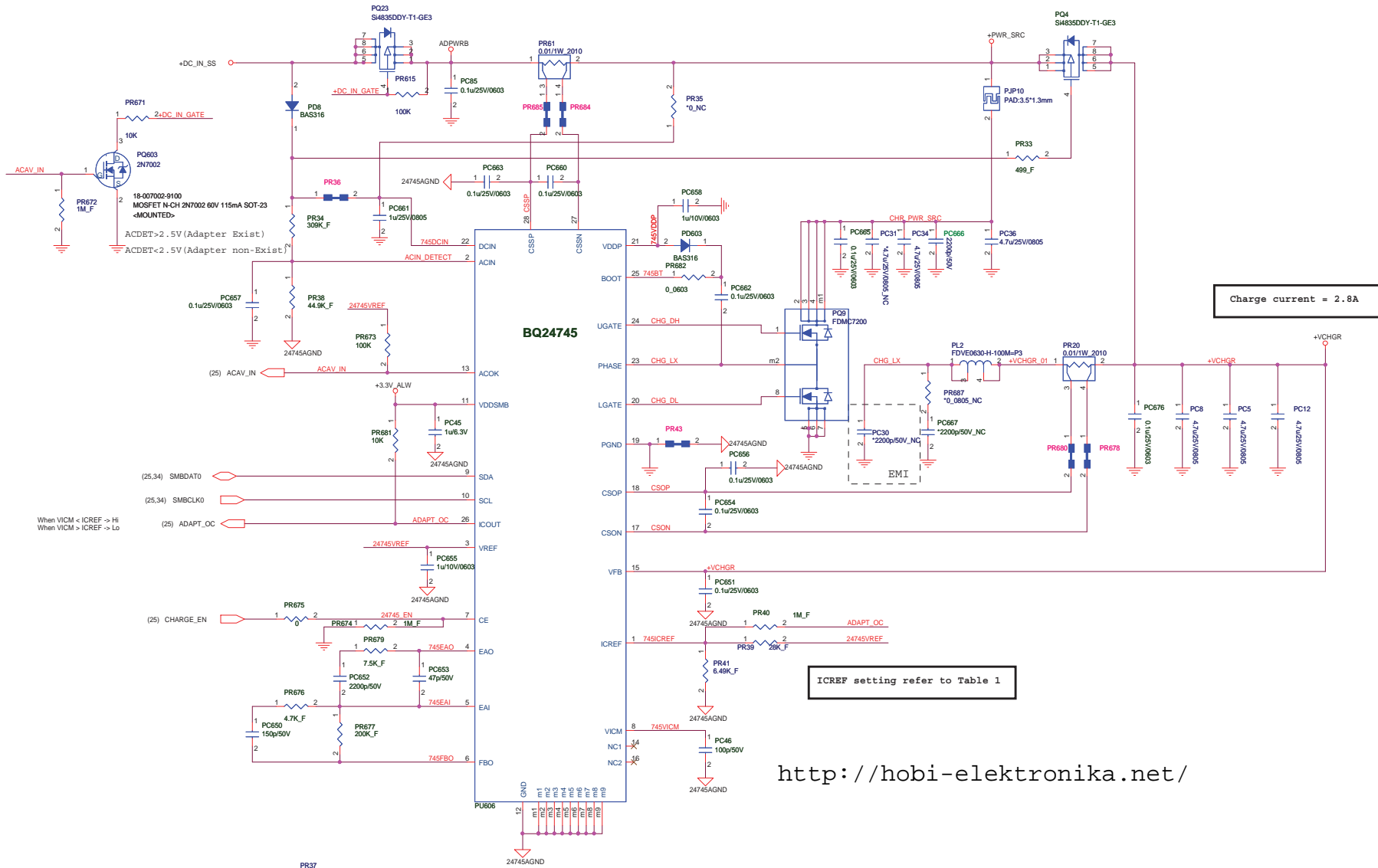
Shut-down temperature: 89 degree!



Put C421 close to Guardian.
Put C422 close to Diode
Place CPU bottom

RUN/ SUS CKT





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TABLE1

ADAPTER(W)	TRIP CURRENT(A)	PQ6	PR28	PR25
65W	3.13	NA	NA	6.49K
90W	4.34	2N7002	19.1K	10K

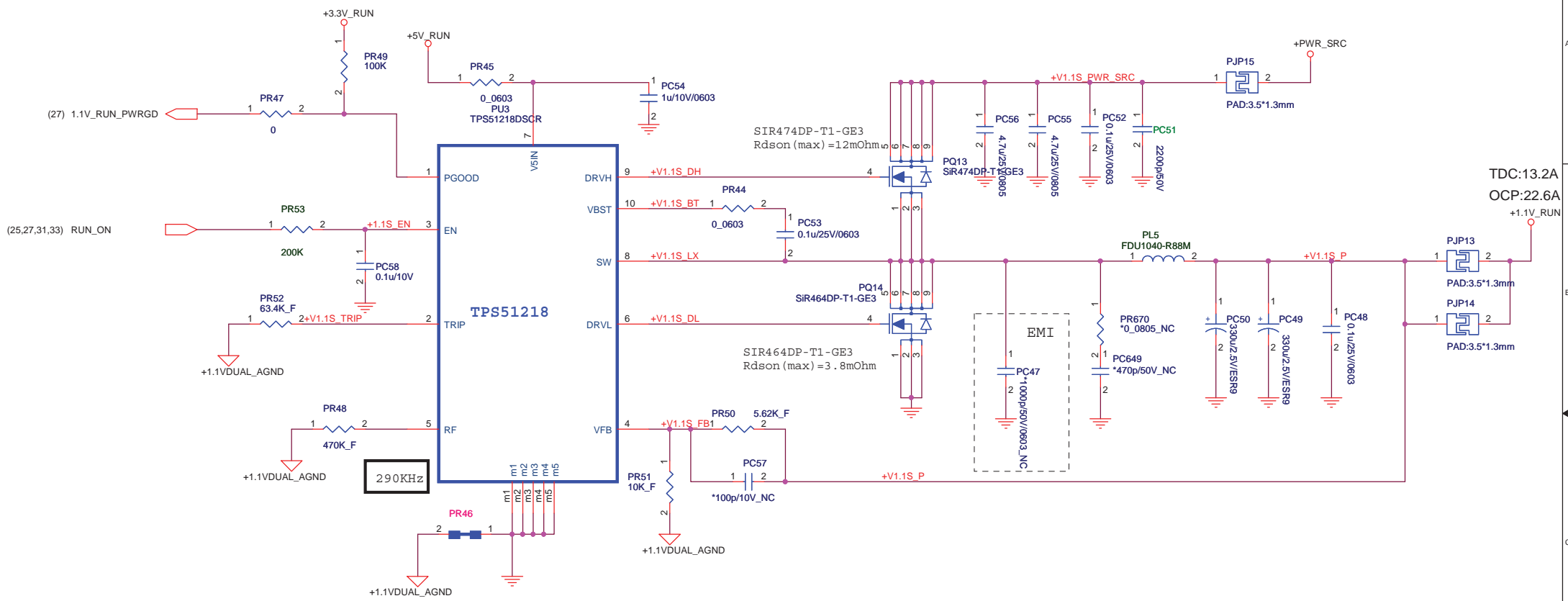
Note 1 : PR28 is populated if ADAPT_TRIP_SET is used to program for the next lower adapter.
ADAPT_TRIP_SET is floating for the higher adapter , grounded for the lower adapter.

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ADAPT_TRIP_SET:
 AC 65W --> H
 Battery mode --> H
 AC 90W --> L

+V1.1V_RUN

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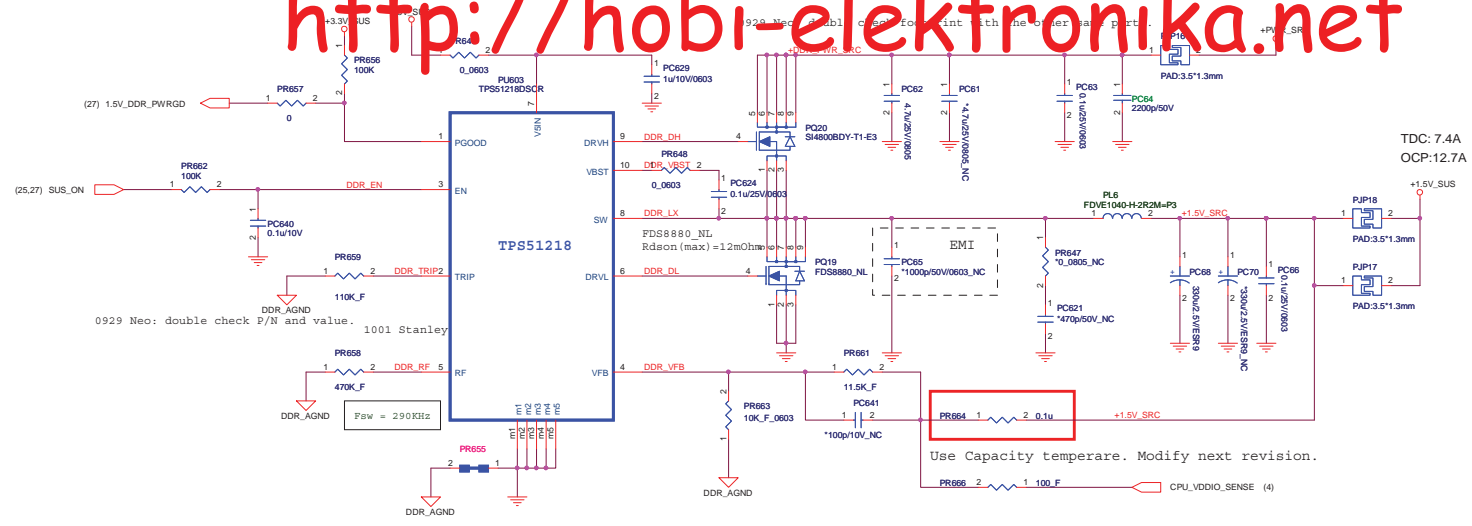


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1.5VDDR



0.75VS

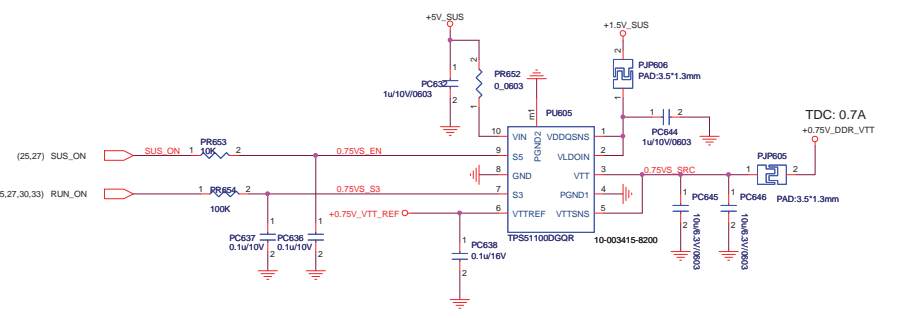
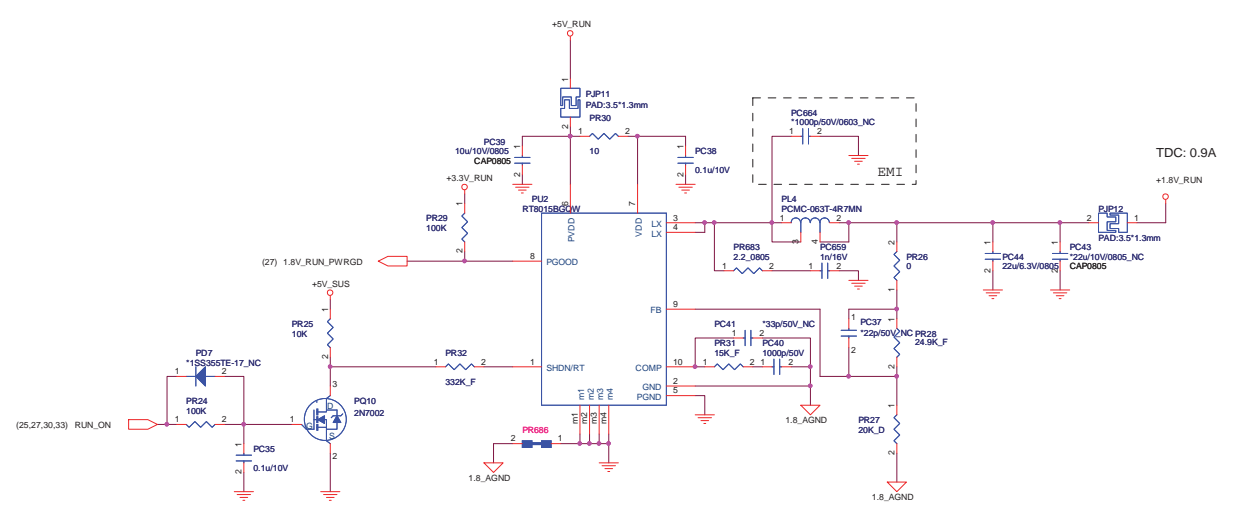
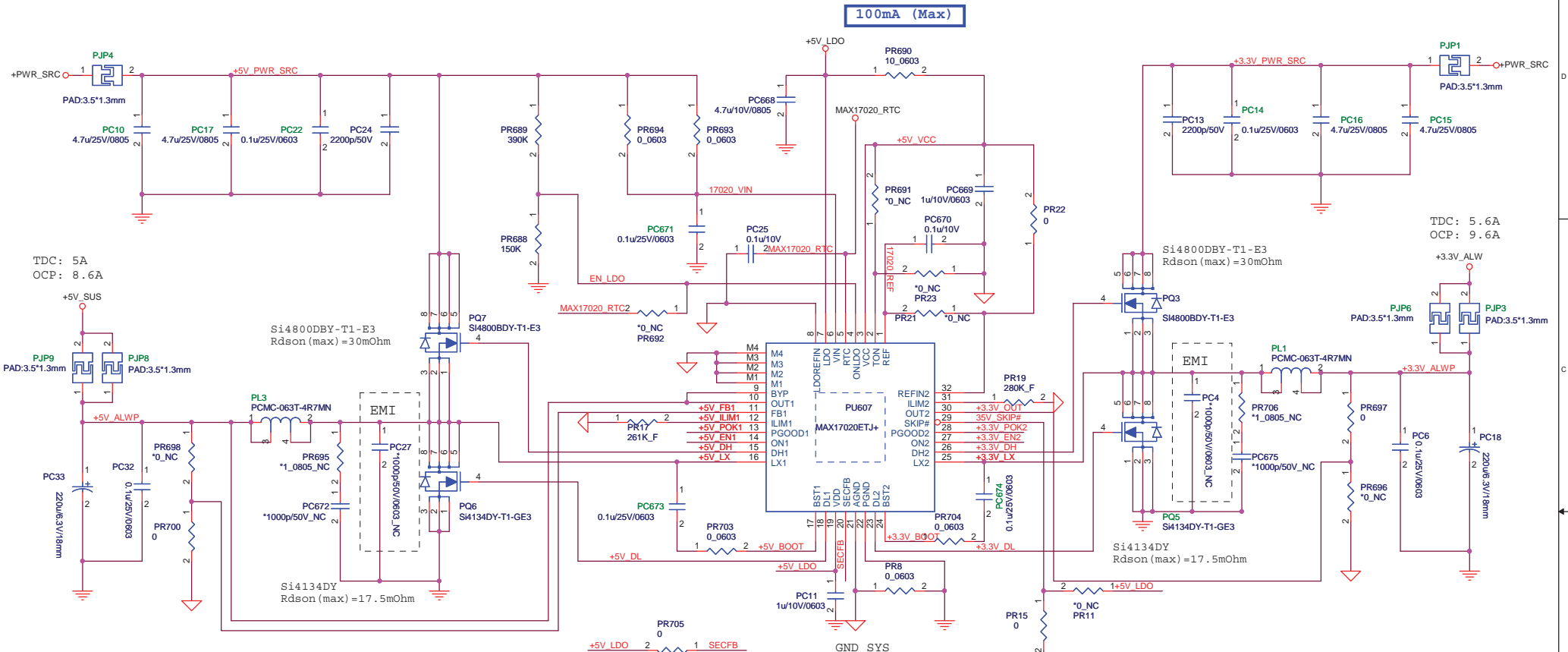


Table 1. S3 and S5 Control Table

STATE	S3	S5	VTT	VREF
Normal	Hi	Hi	1.25V/0.9V	1.25V/0.9V
Standby	Lo	Hi	12mV/6mV (High-Z)	1.25V/0.9V
Shutdown	Lo	Lo	0V (Discharge)	0V (Discharge)
Shutdown	Hi	Lo	0V (Discharge)	0V (Discharge)

1.8VS



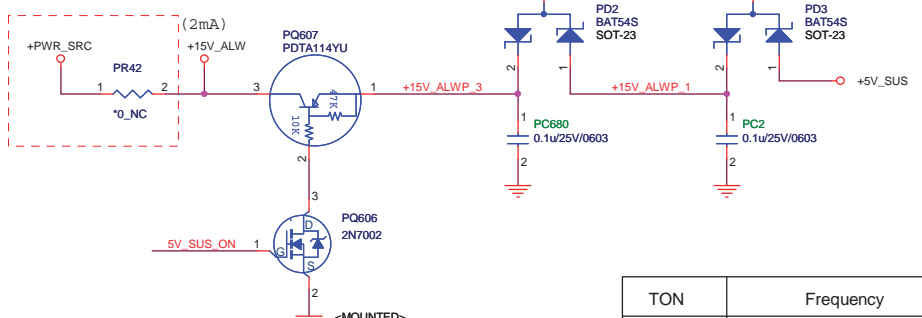


TDC: 5A
OCP: 8.6A

TDC: 5.6A
OCP: 9.6A

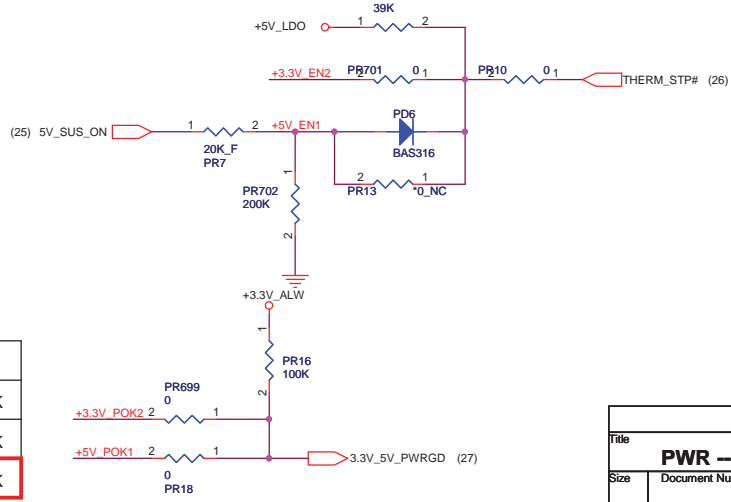
+15V_ALW may be disabled on S3, S4, S5; saving 1mA. But the control signal needs to be separate.

http://hobi-elektronika.net/



0930 Stanley

TON	Frequency
GND	OUT1@400K, OUT2@500K
VCC	OUT1@200K, OUT2@300K
OPEN	OUT1@400K, OUT2@300K



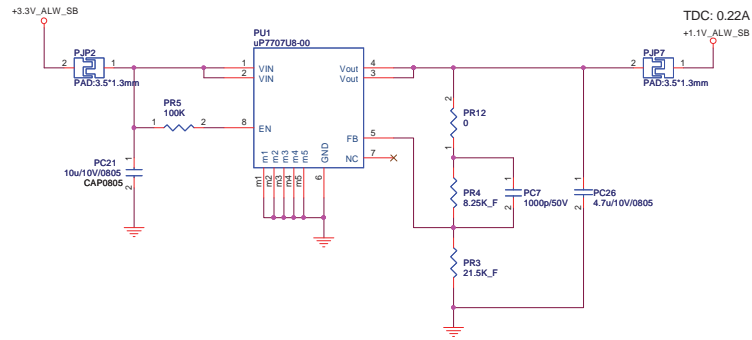
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Title: **PWR -- SYS 5V/ 3V**

Size: Document Number **Inspiron Z -- AMD** Rev A00

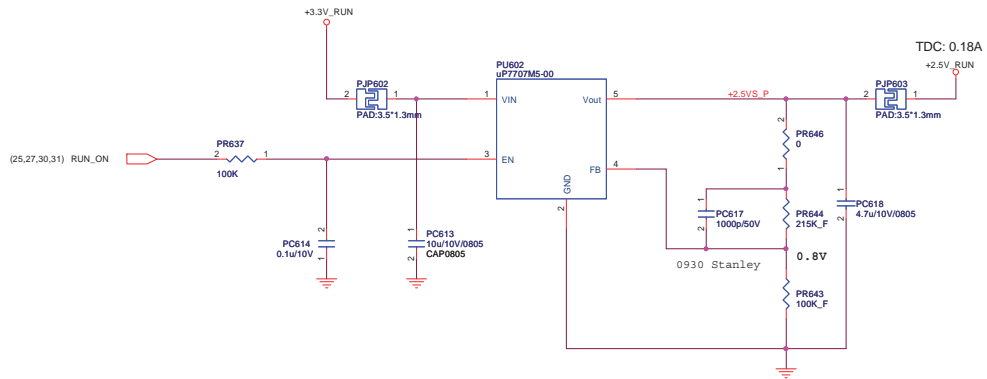
Date: Monday, November 02, 2009 Sheet 32 of 37

+1.1V_ALW_SB

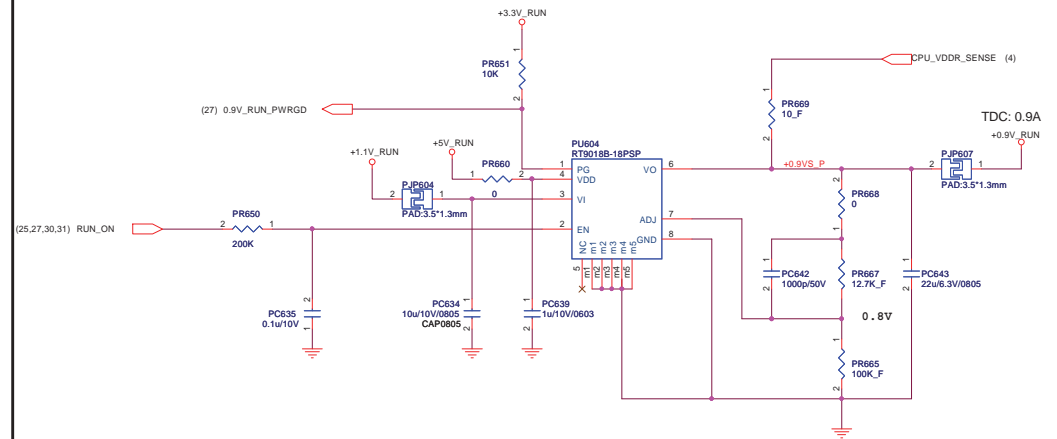


http://hobi-elektronika.net/

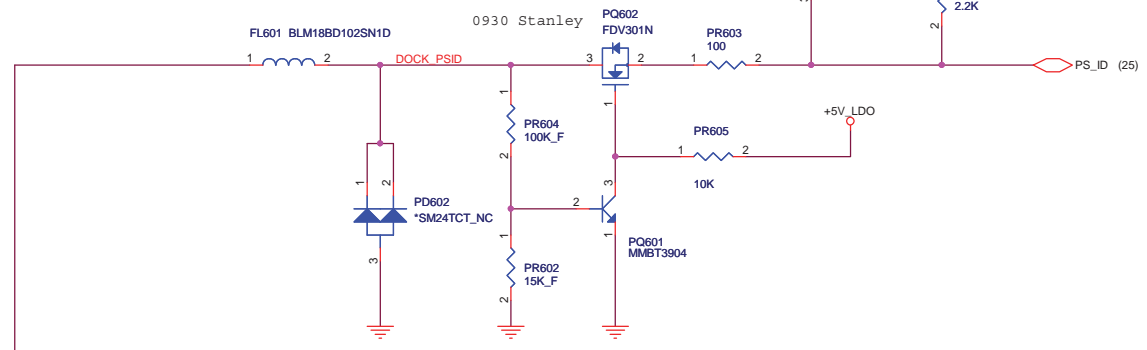
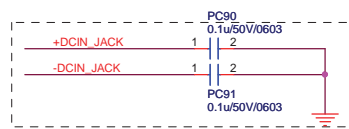
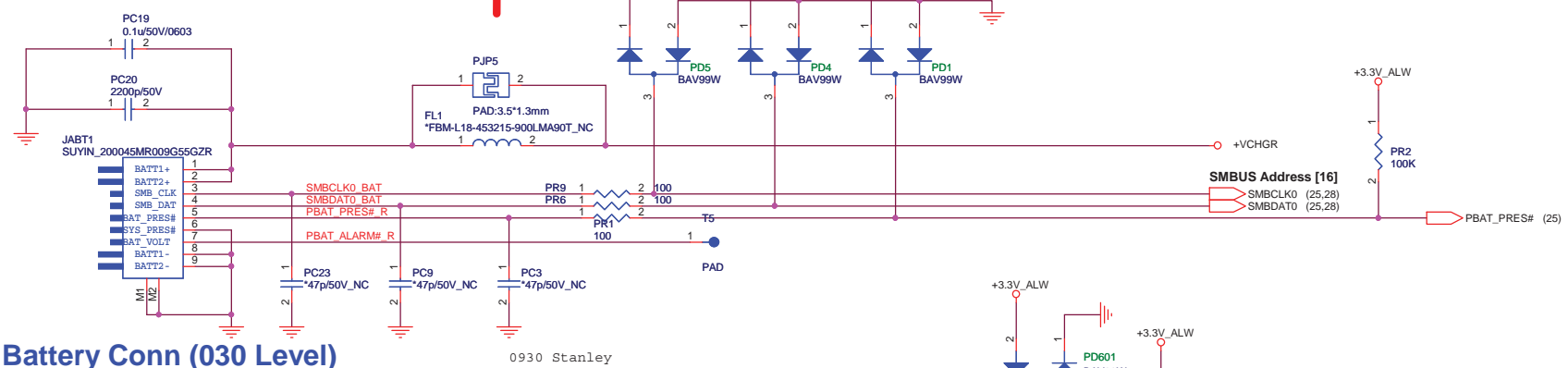
+2.5V_RUN



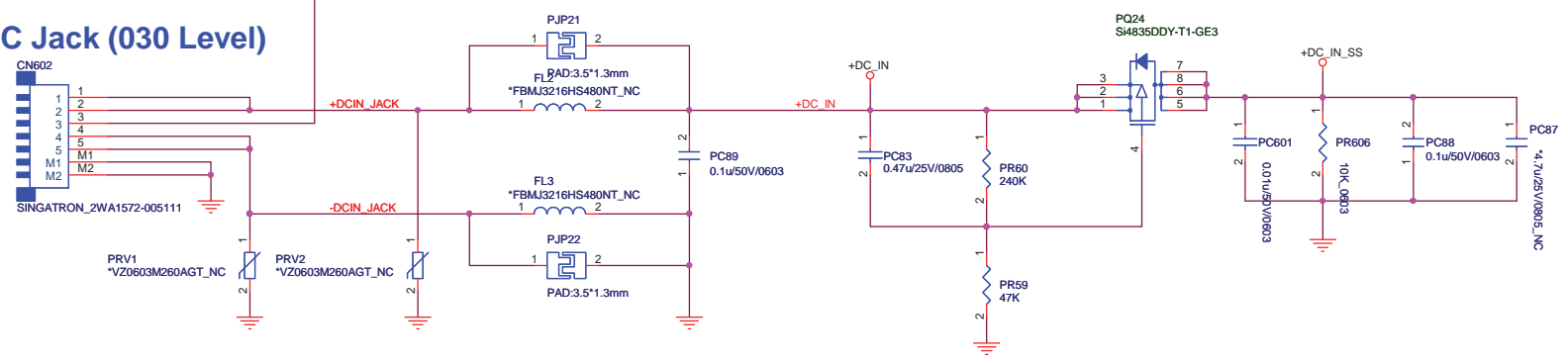
+0.9V_RUN



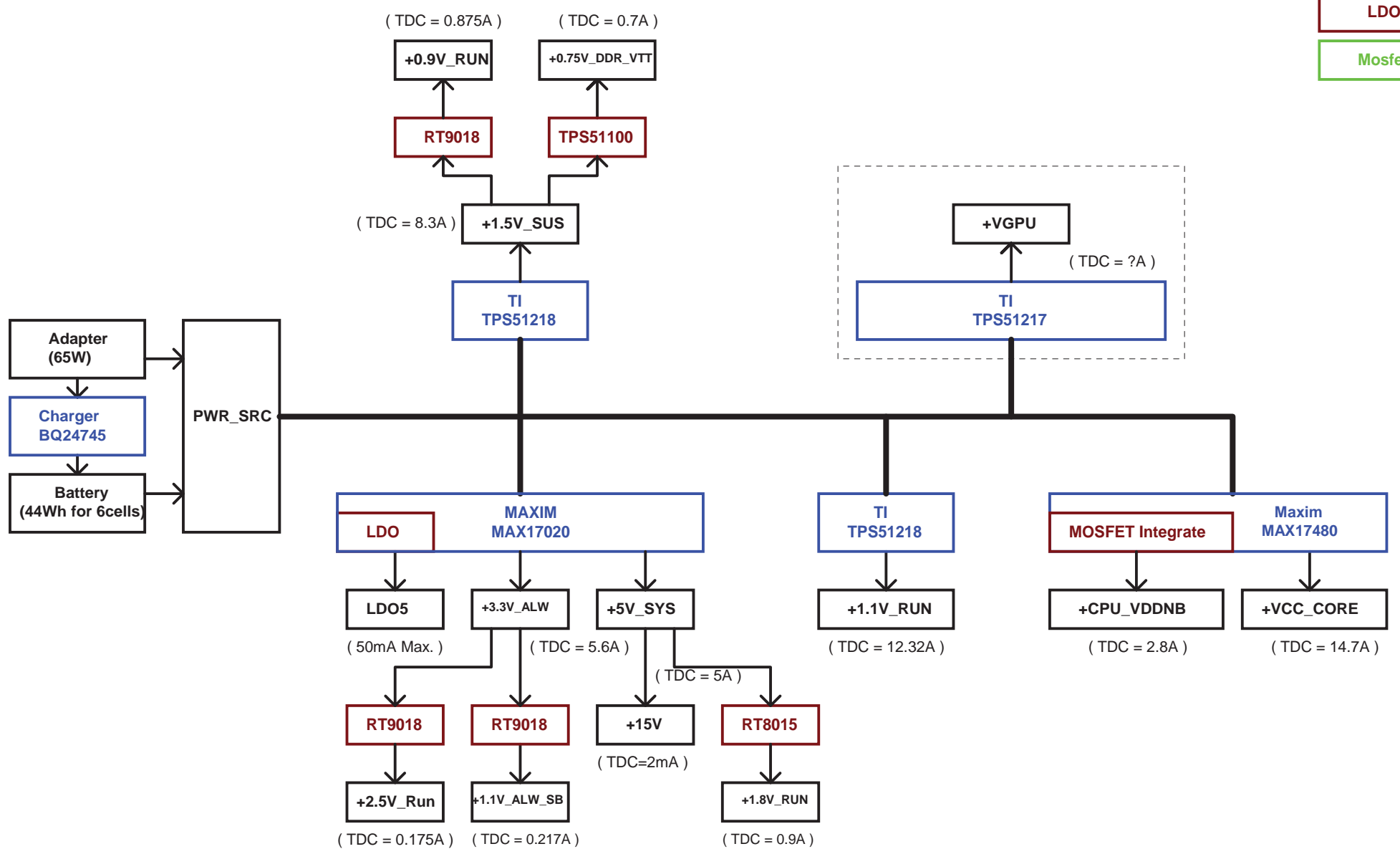
Dell/ Flex Confidential



DC Jack (030 Level)

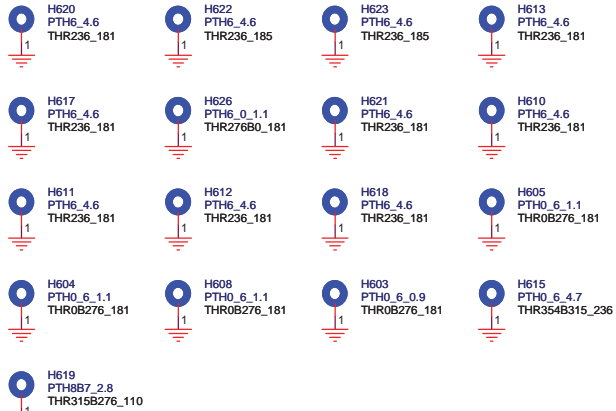


PWM Switching
LDO
Mosfet

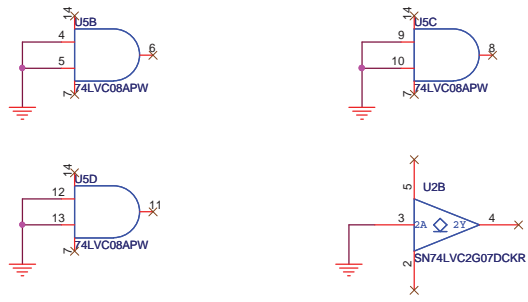


Title			Cover Sheet		
Size	Document Number			Rev	A00
	M11z				
Date:	Monday, November 02, 2009	Sheet	35	of	37

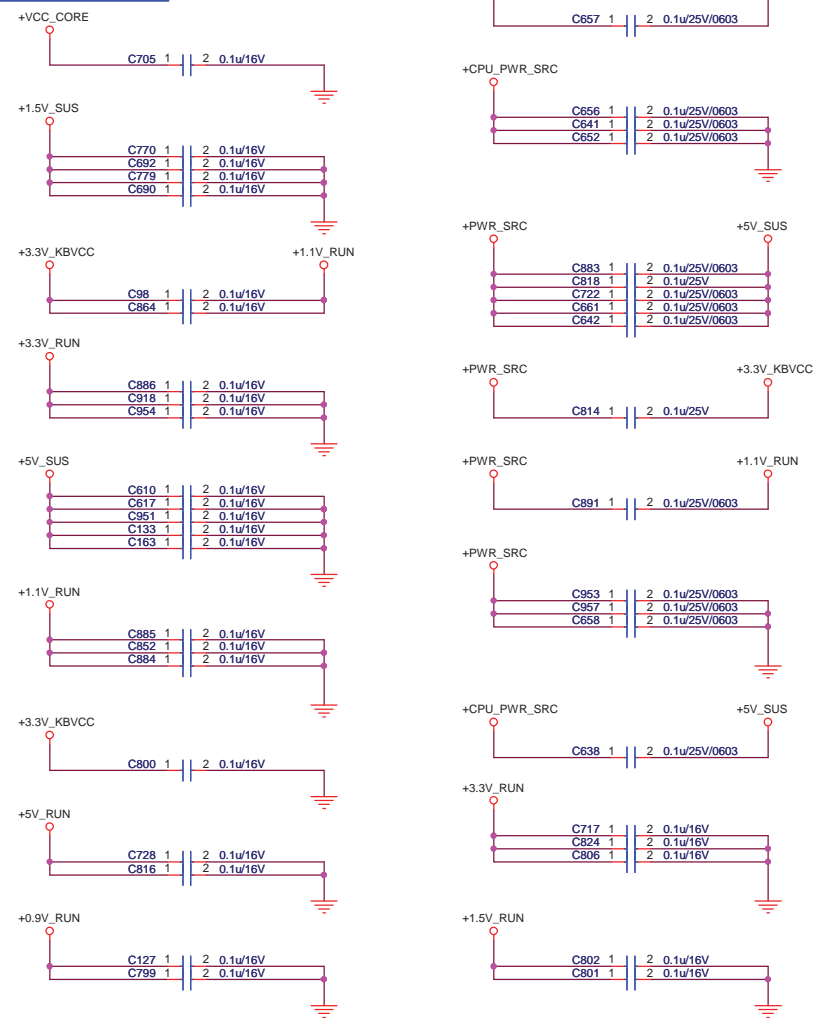
Screw Hole



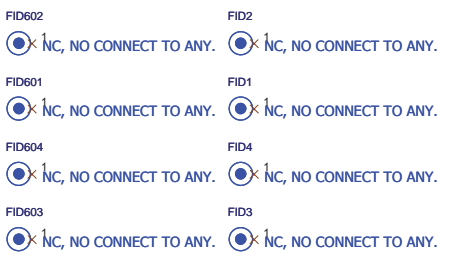
Unused Gates



EMI Solution



FID



Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phase
1			X00		X00 Schematic Official Release	X00	SSI