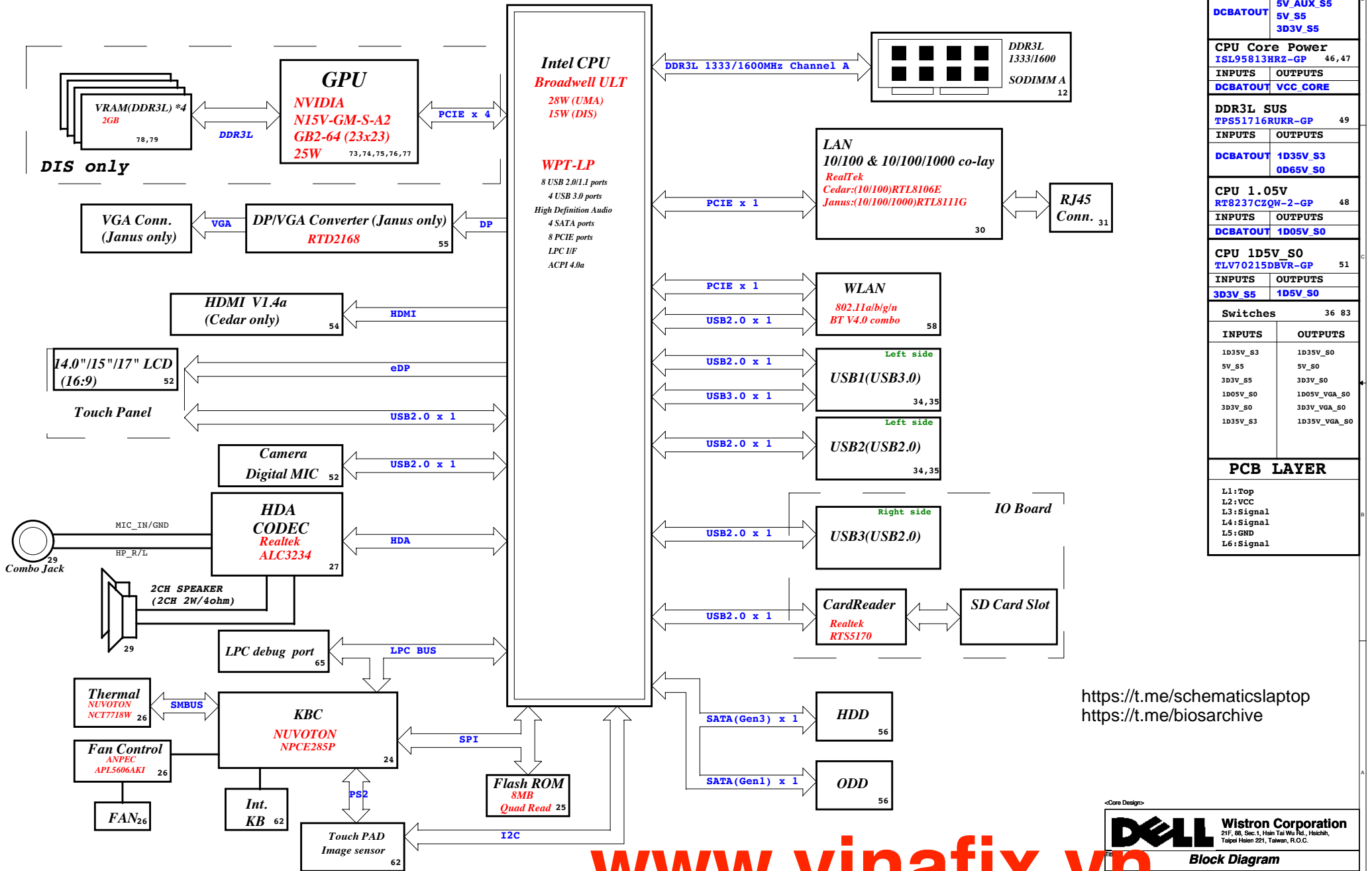


Project code:4PD00I010001
 PCB P/N: 12314-1
 Revision: -1

Cedar/Janus Block Diagram



| CHARGER | |
|---|--|
| HPA02224RGRR-1-GP 44 | |
| INPUTS | OUTPUTS |
| AD+ | DCBATOUT |
| BT+ | |
| SYSTEM DC/DC | |
| TPS51225RUKR-GP 45 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5 |
| CPU Core Power | |
| ISL95813HR2-GP 46,47 | |
| INPUTS | OUTPUTS |
| DCBATOUT | VCC_CORE |
| DDR3L SUS | |
| TPS51716RUKR-GP 49 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D35V_S3 0D65V_S0 |
| CPU 1.05V | |
| RT8237CZQW-2-GP 48 | |
| INPUTS | OUTPUTS |
| DCBATOUT | 1D05V_S0 |
| CPU 1D5V_S0 | |
| TLV70215DBVR-GP 51 | |
| INPUTS | OUTPUTS |
| 3D3V_S5 | 1D5V_S0 |
| Switches | |
| 36 83 | |
| INPUTS | OUTPUTS |
| 1D35V_S3 | 1D35V_S0 |
| 5V_S5 | 5V_S0 |
| 3D3V_S5 | 3D3V_S0 |
| 1D05V_S0 | 1D05V_VGA_S0 |
| 3D3V_S0 | 3D3V_VGA_S0 |
| 1D35V_S3 | 1D35V_VGA_S0 |
| PCB LAYER | |
| L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Signal | |

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Block Diagram
 Document Number: Janus HSW 40/50/70 Rev X02
 Date: Friday, February 07, 2014 Sheet 2 of 104

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Title

(Reserved)

Size
A4

Document Number

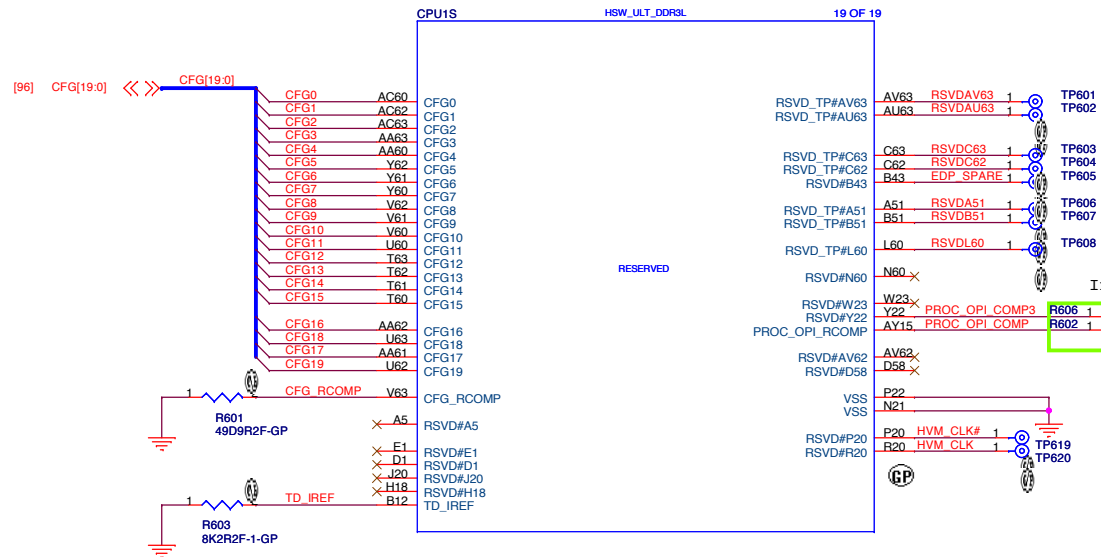
Janus HSW 40/50/70

Rev
A00

Date: Friday, February 07, 2014

Sheet 3 of 104

SSID = CPU

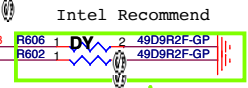


#514405

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left unconnected

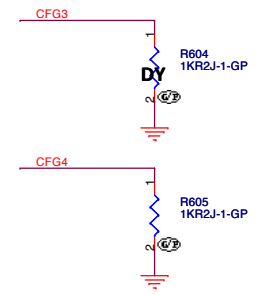


Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12-15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

#514405 PCH strap pin:

| Signal Name | Description | Direction / Buffer Type |
|-------------|--|-------------------------|
| CFG[19:0] | <p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none"> • CFG[2:0]: Reserved configuration lane. A test point may be placed on the board for these lanes. • CFG[3]: MSR Privacy Bit Feature <ul style="list-style-type: none"> - 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting - 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden • CFG[4]: eDP enable <ul style="list-style-type: none"> - 1 = Disabled - 0 = Enabled • CFG[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands. | I/O GTL |



| PHYSICAL_DEBUG_ENABLED (DFX PRIVACY) | |
|--------------------------------------|--|
| CFG[3] | 0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED |

| DISPLAY PORT PRESENCE STRAP | |
|-----------------------------|---|
| CFG[4] | 0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT |

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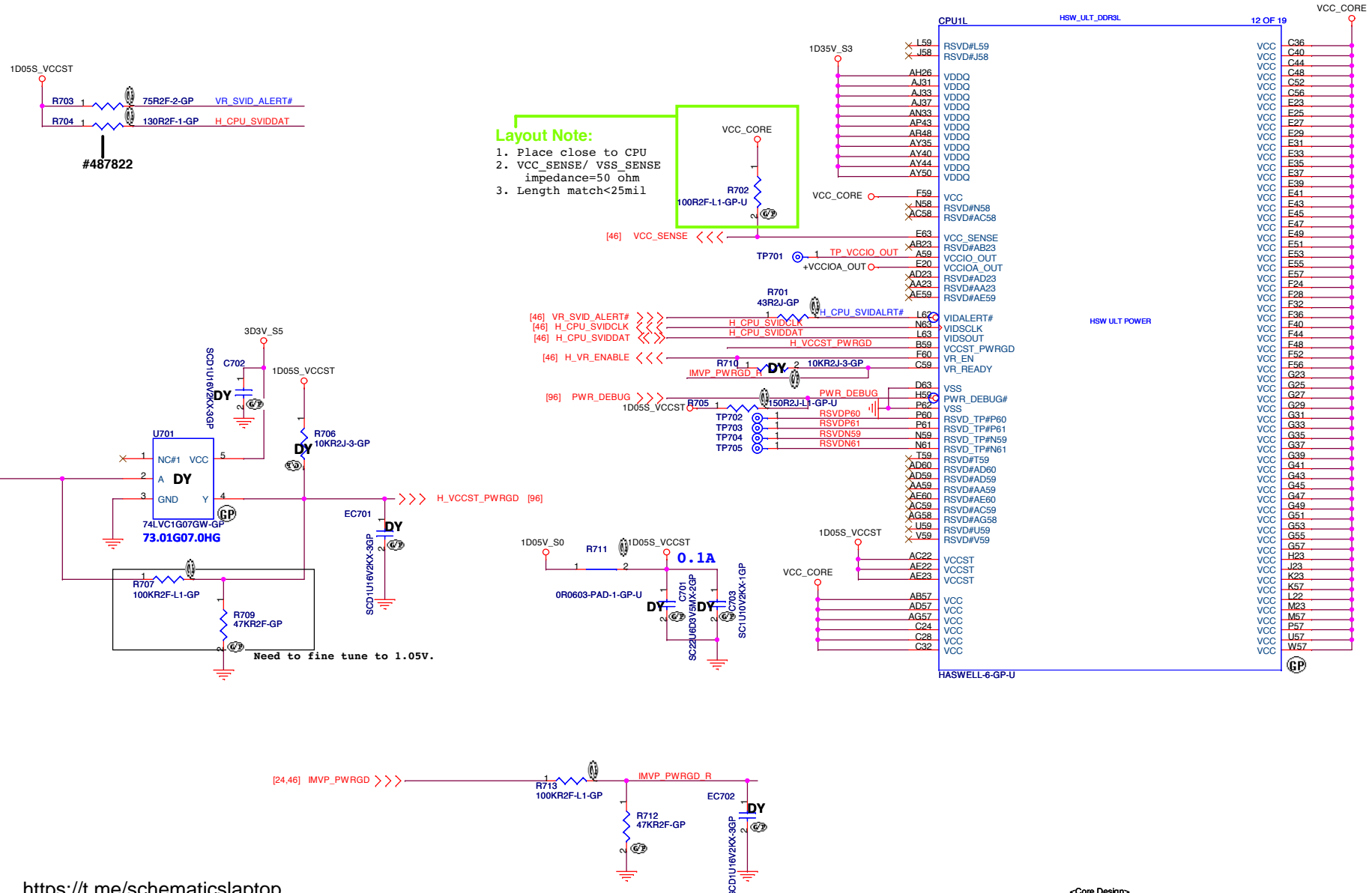
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Title: **CPU (CFG)**

| | | |
|---------------------------------|---|----------------|
| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 6 of 104 | |

SSID = CPU

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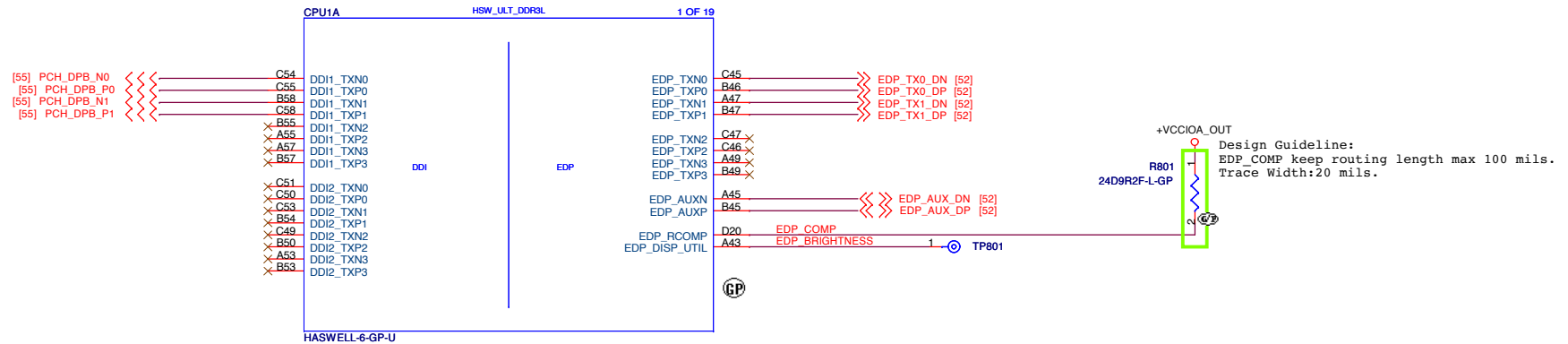


SSID = CPU

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DP to VGA Converter

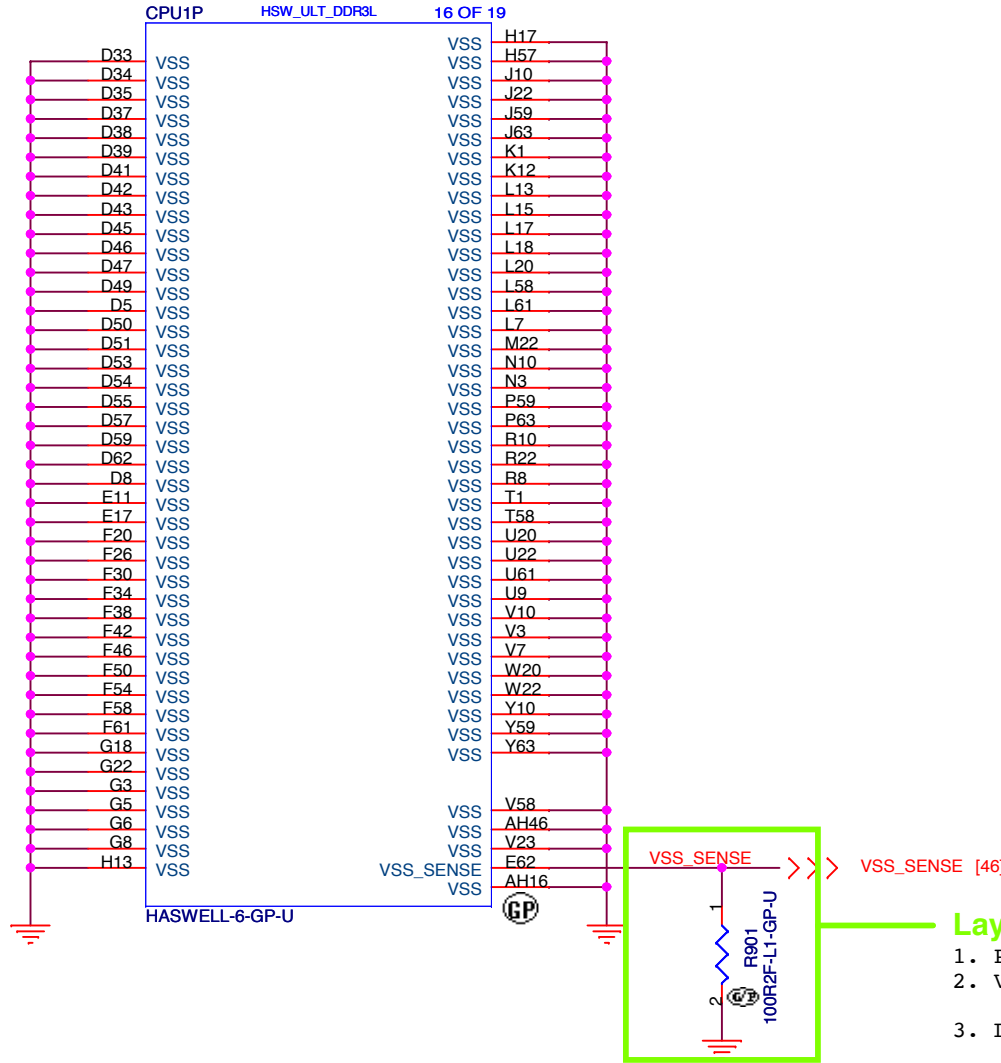


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| | | | |
|----------------------|---------------------------|--|----------|
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| Title | | | |
| CPU (DDI/EDP) | | | |
| Size | Document Number | Rev | |
| A3 | Janus HSW 40/50/70 | X02 | |
| Date: | Friday, February 07, 2014 | Sheet | 8 of 104 |

SSID = CPU



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Layout Note:

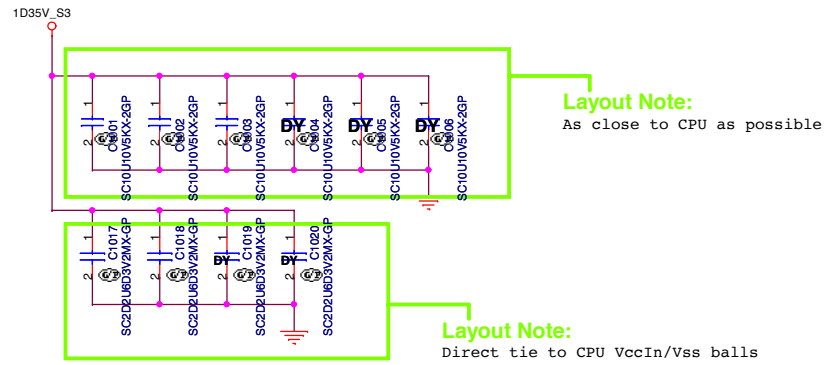
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

<Core Design>




| | | |
|---------------------------------|--|-------------------|
| Title | | |
| CPU (VSS) | | |
| Size A4 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 9 | of 104 |

SSID = CPU



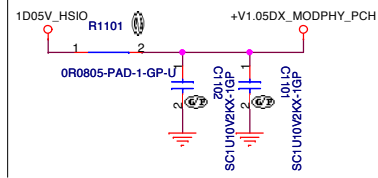
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| | | | | | |
|---|---------------------------|-------|--|----|------------|
|  | | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title | | | | | |
| CPU (Power CAP1) | | | | | |
| Size | Document Number | | | | Rev |
| A3 | Janus HSW 40/50/70 | | | | A00 |
| Date: | Friday, February 07, 2014 | Sheet | 10 | of | 104 |

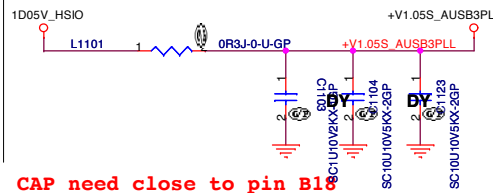
MAX: 1.92A

1.838A



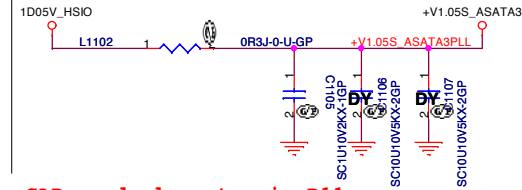
CAP need close to pin K9 L10

41mA



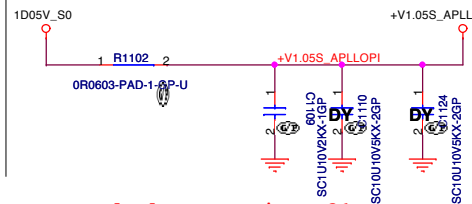
CAP need close to pin B18

42mA



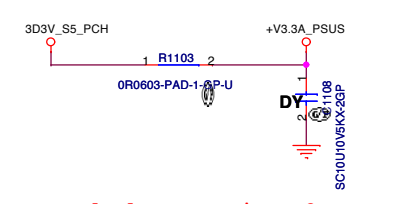
CAP need close to pin B11

57mA



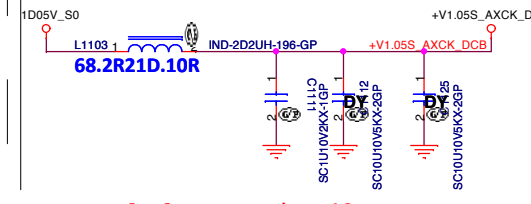
CAP need close to pin AA21

62mA



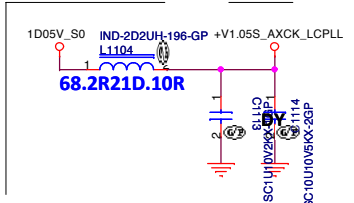
CAP need close to pin AC9

185mA



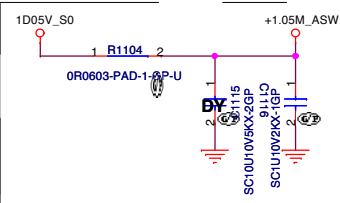
CAP need close to pin J18

31mA



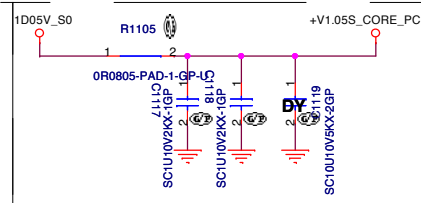
CAP need close to pin A20

658mA



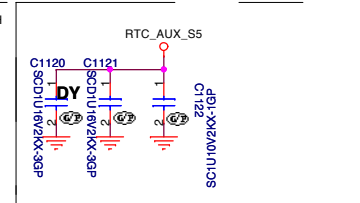
CAP need close to pin AE9

1.632A



CAP need close to pin AE8 J11


1mA



CAP need close to pin AG10

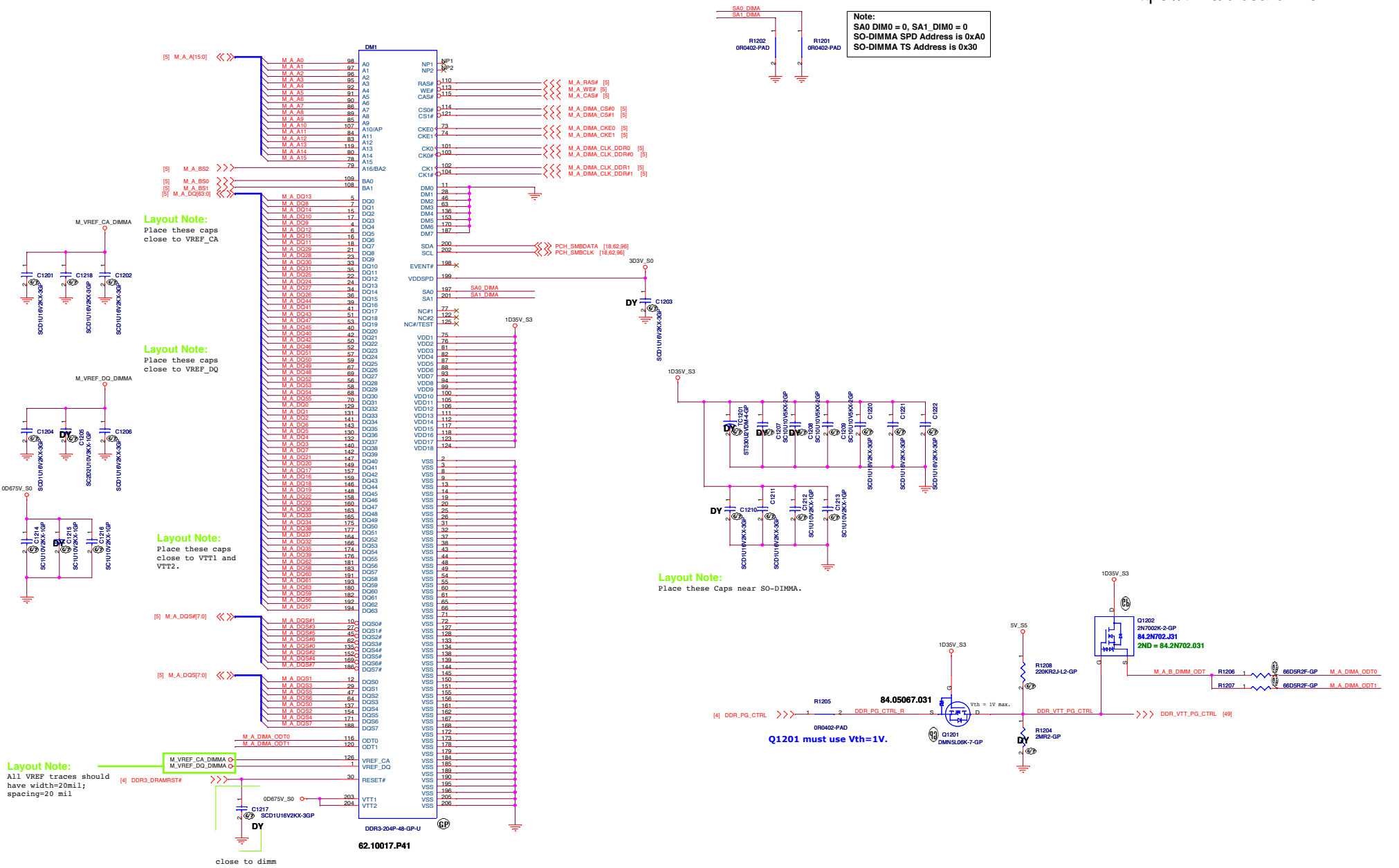
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|--|---------------------------|-----------------|
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| | | |
| Size | Document Number | Rev |
| A3 | Janus HSW 40/50/70 | A00 |
| Date: | Friday, February 07, 2014 | Sheet 11 of 104 |

SSID = MEMORY


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|---|--|--|
|  | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title (Reserved)DDR3-SODIMM2 | | |
| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 13 | of 104 |

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|---|--|---|
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title (Reserved)_SODIMM _SODIMM4 | | |
| Size A4 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 14 | of 104 |

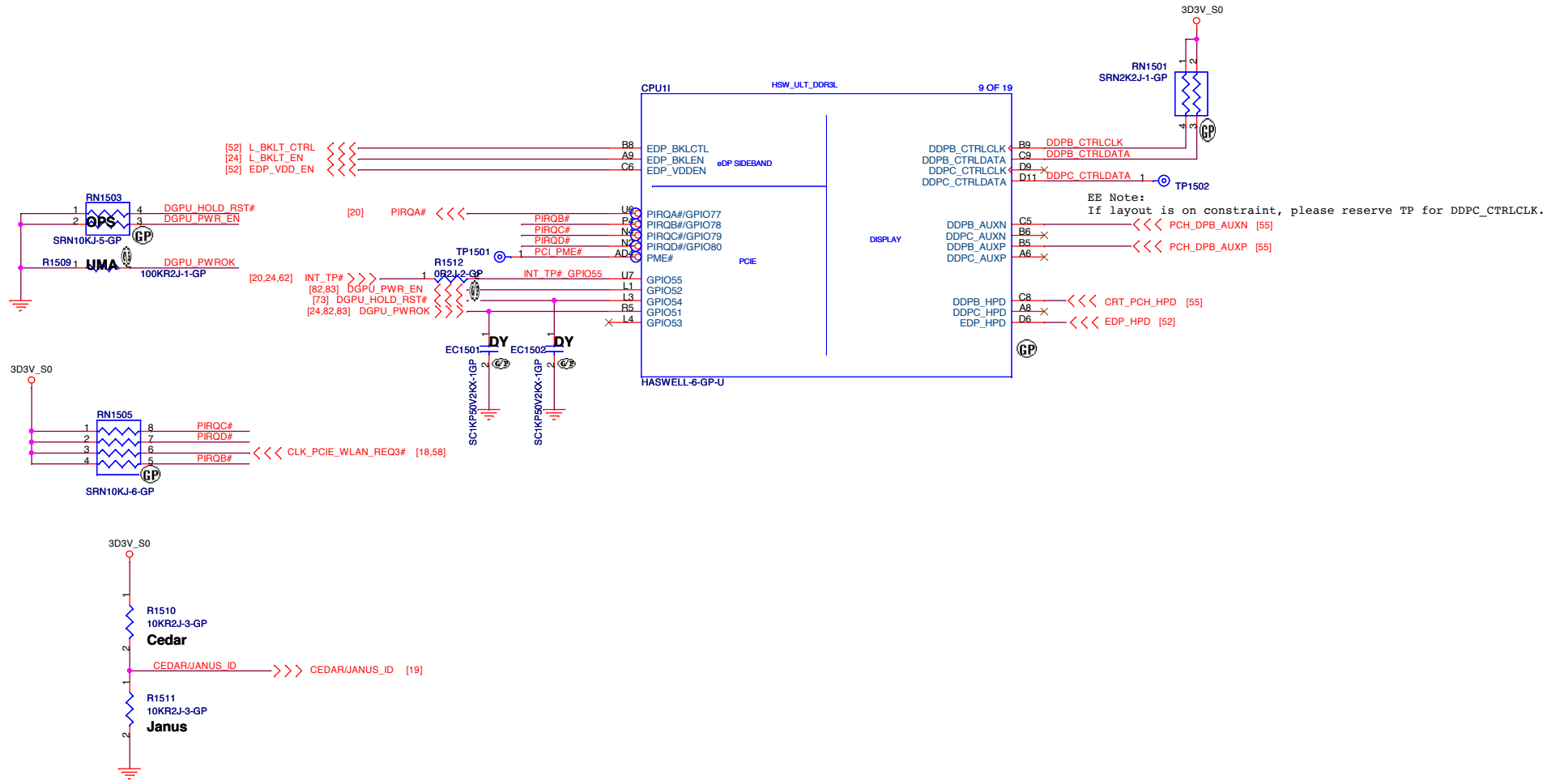
SSID = CPU

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PCH strap pin:

| Port B Detected | |
|-----------------|--|
| DDPB_CTRLDATA | Low = Disable Port B (default) * High = Enable Port B |
| DDPC_CTRLDATA | * Low = Disable Port C (default) High = Enable Port C |

The internal pull-down is disabled after PLTRST# deasserts



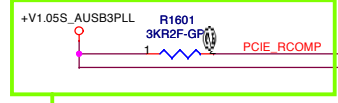
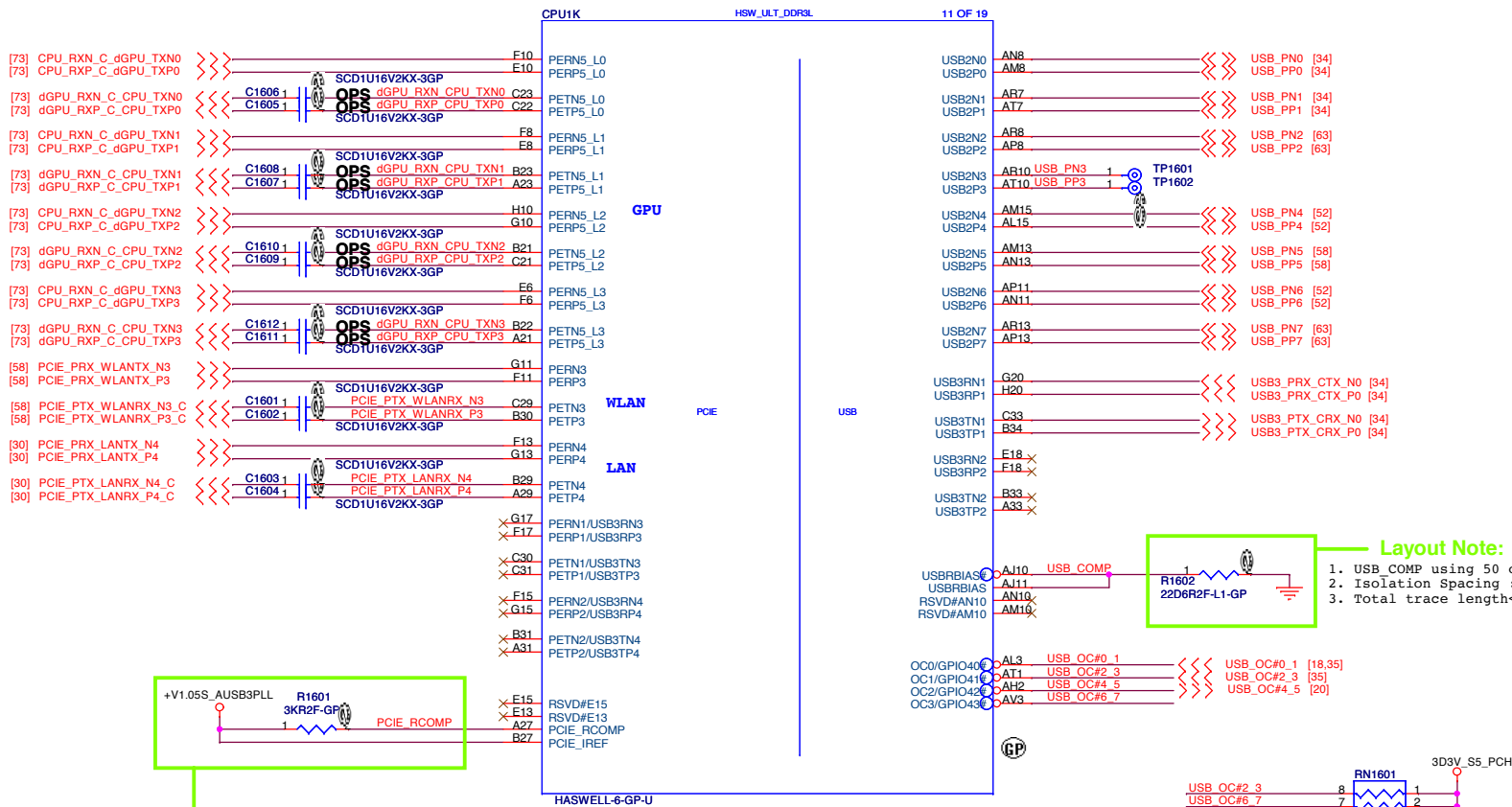
<Core Design>

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Title: **PCH (EDP/GPIO/DDI)**

| | | |
|---------------------------------|--|-----------------|
| Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: X02 |
| Date: Friday, February 07, 2014 | Sheet: 15 | of: 104 |

SSID = PCH



Layout Note:

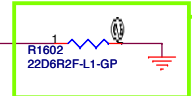
1. PCIE_RCOMP/ PCIE_IREF trace width=12-15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

USB 2.0 Table

| Pair | Device |
|------|---------------------------|
| 0 | USB3.0 port1 |
| 1 | USB2.0 Port2 (Debug Port) |
| 2 | USB2.0 Port3 (IOBD) |
| 3 | X |
| 4 | CAMERA |
| 5 | WLAN |
| 6 | Touch Panel |
| 7 | Card Reader |

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil



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PCIE Table

| Port | Device | Share BUS |
|-----------|--------|-----------|
| 1 | N/A | USB3.0_3 |
| 2 | N/A | USB3.0_4 |
| 3 | WLAN | |
| 4 | LAN | |
| 5 (L0-L3) | GPU | |
| 6 (L3) | HDD | SATA0 |
| 6 (L2) | ODD | SATA1 |
| 6 (L0-L1) | N/A | |

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

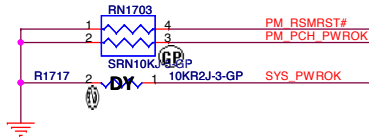
| SKU | High Speed I/O Ports | | | | | | | | | | | | | |
|---------|----------------------|----------------|----------------|----------------|--------------|--------------|-------------------------|-------------------------|---------------------|---------------------|-------------------------|-------------------------|---------------------|---------------------|
| | Port 1 | Port 2 | Port 3 | Port 4 | Port 5 | Port 6 | Port 7 | Port 8 | Port 9 | Port 10 | Port 11 | Port 12 | Port 13 | Port 14 |
| Premium | USB 3.0 Port 1 | USB 3.0 Port 2 | USB 3.0 Port 3 | USB 3.0 Port 4 | PCIe* Port 3 | PCIe* Port 4 | PCIe* Port 5 Lane 0 SSD | PCIe* Port 5 Lane 1 SSD | PCIe* Port 5 Lane 2 | PCIe* Port 5 Lane 3 | SATA 6Gb/s Port 3 | SATA 6Gb/s Port 2 | SATA 6Gb/s Port 1 | SATA 6Gb/s Port 0 |
| Base | USB 3.0 Port 1 | USB 3.0 Port 2 | USB 3.0 Port 3 | USB 3.0 Port 4 | PCIe* Port 3 | PCIe* Port 4 | PCIe* Port 5 Lane 0 SSD | PCIe* Port 5 Lane 1 SSD | PCIe* Port 5 Lane 2 | PCIe* Port 5 Lane 3 | PCIe* Port 6 Lane 0 SSD | PCIe* Port 6 Lane 1 SSD | PCIe* Port 6 Lane 2 | PCIe* Port 6 Lane 3 |

<Core Design>



SSID = PCH

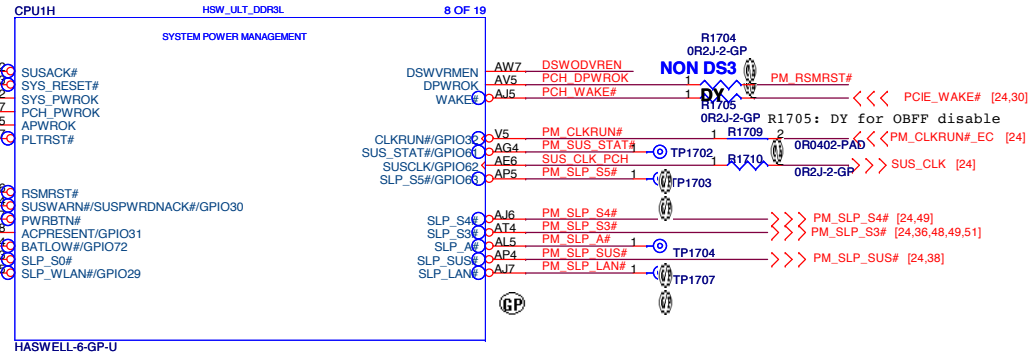
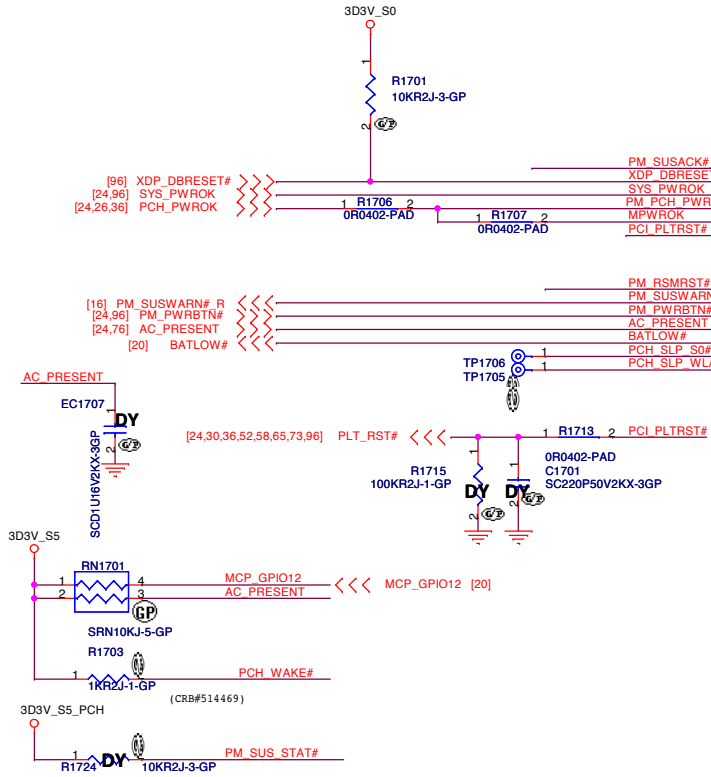
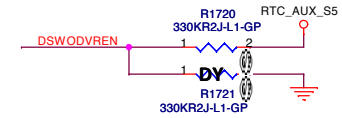
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<https://t.me/biosarchive>



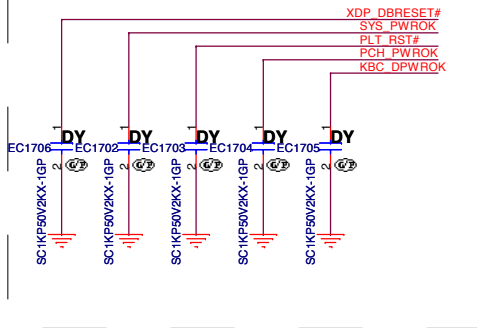
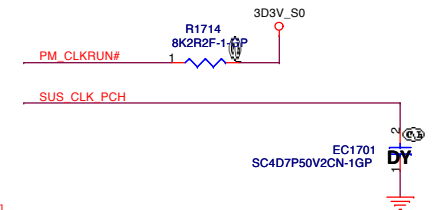
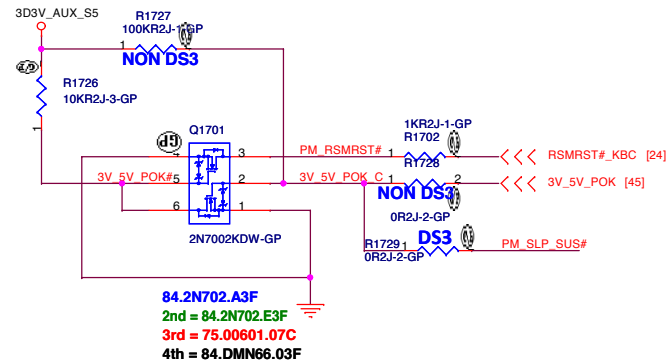
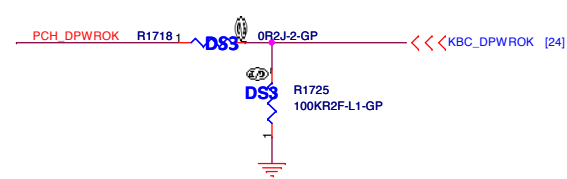
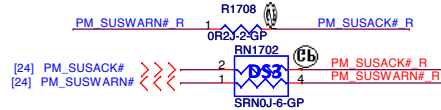
PCH strap pin:

| On Die DSW VR Enable | |
|----------------------|--|
| DSWVRMEN | Low = Disable High = Enable (default) |

This signal has no integrated pull-up/pull-down.



NON DS3



84.2N702.A3F
 2nd = 84.2N702.E3F
 3rd = 75.00601.07C
 4th = 84.DMN66.03F

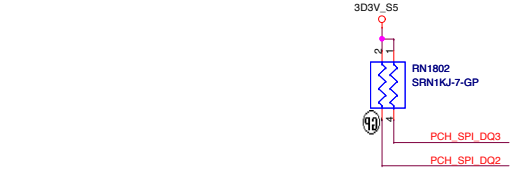
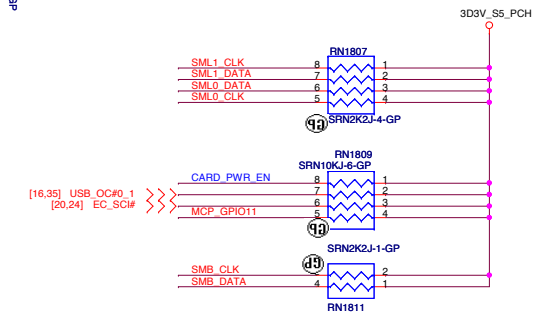
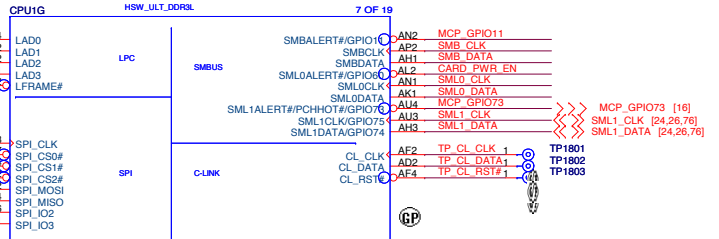
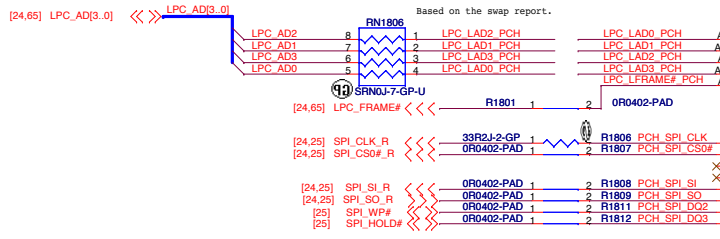
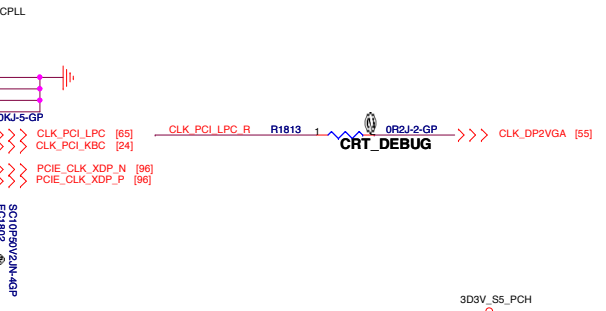
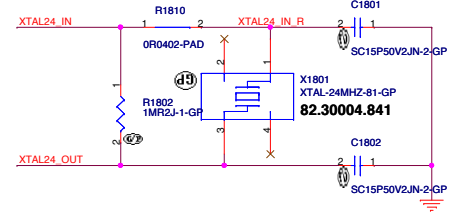
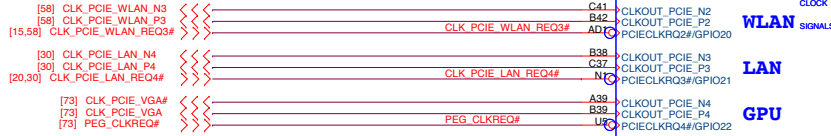
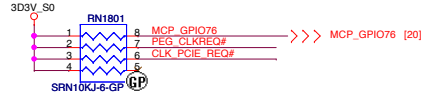
<Core Design>

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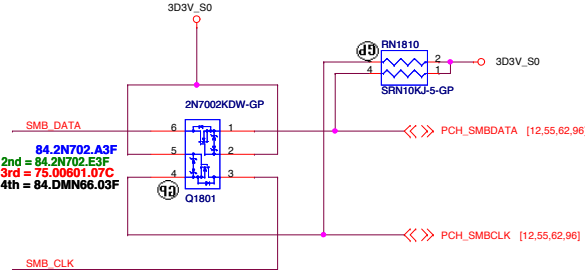
Title: **PCH (PM)**

| | | |
|---------------------------------|--|-----------------|
| Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00 |
| Date: Friday, February 07, 2014 | Sheet: 17 | of: 104 |

SSID = PCH



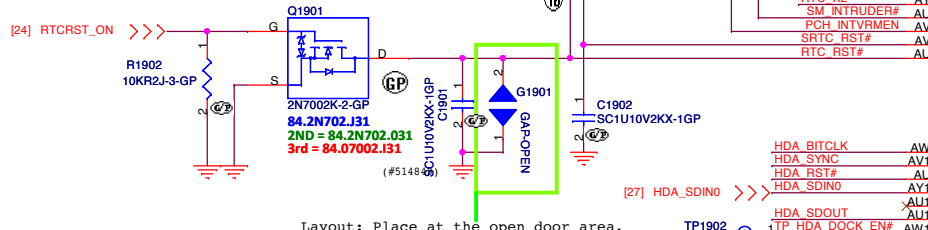
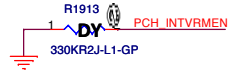
<https://t.me/schematics4laptop>
<https://t.me/biosarchive>



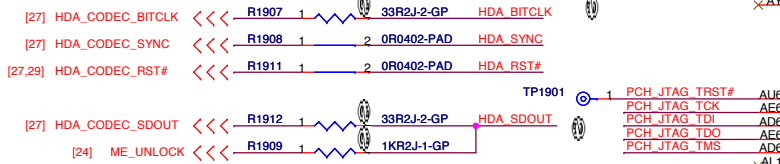
SSID = CPU

PCH strap pin:

| Integrated SUS 1V VRM Enable | |
|------------------------------|--|
| INTVRMEN | Low = External VRs High = Internal VRs* |



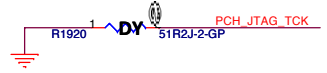
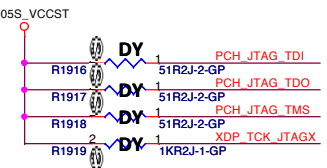
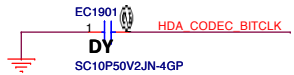
Layout: Place at the open door area.



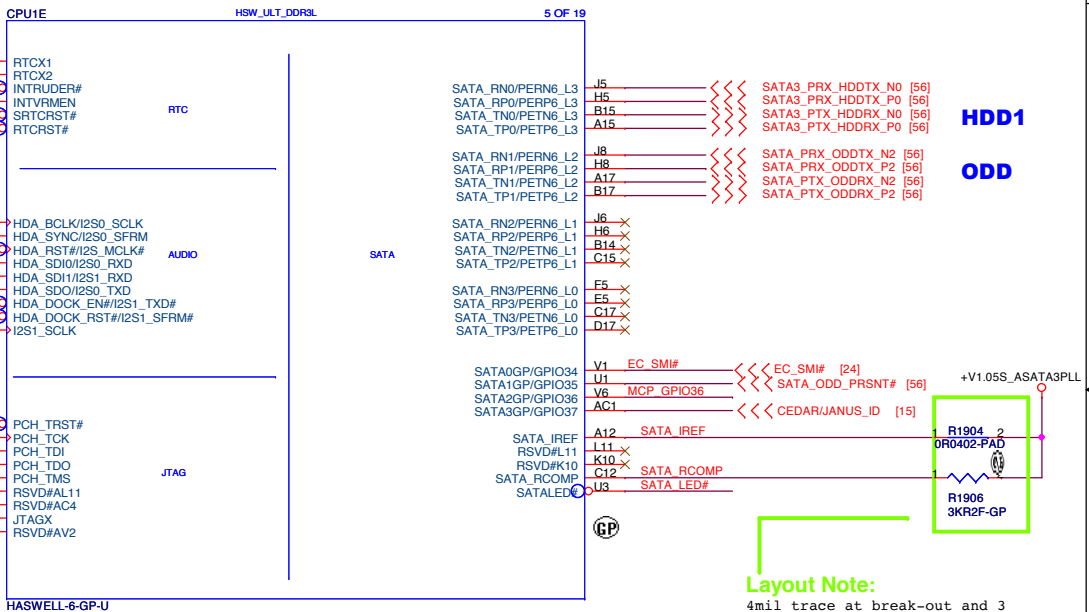
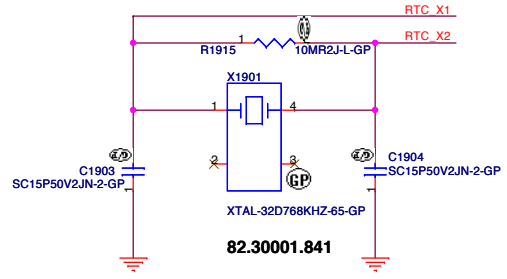
PCH strap pin:

| Flash Descriptor Security Override/ Intel ME Debug Mode | |
|--|----------------------------------|
| HDA_SDOUT | Low = Default * High = Enable |

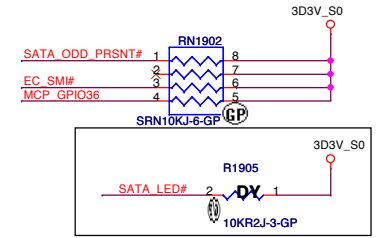
The internal pull-down is disabled after PLTRST# deasserts



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Layout Note:
4mil trace at break-out and 3 12-15mil trace with <0.2 ohms and length total <= 500mils.



Unused SATA[3:0]GP pins must be terminated to either 3.3V rail or GND using 8.2K to 10K on the motherboard. Either pull-up or pull-down is acceptable.

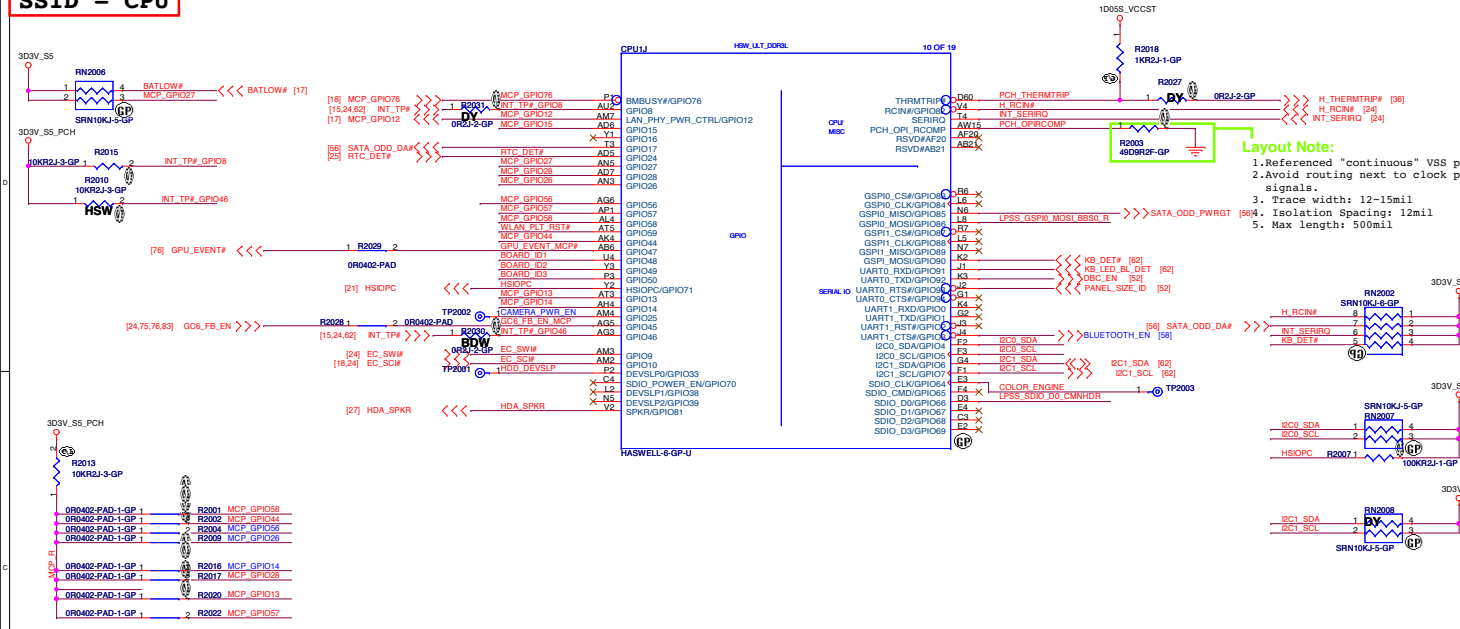
<Core Design>

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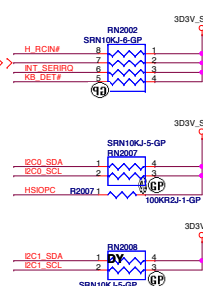
Title: **PCH (RTC/SATA/HDA/JTAG)**

| | | |
|---------------------------------|--|-----------------|
| Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00 |
| Date: Friday, February 07, 2014 | Sheet: 19 | of: 104 |

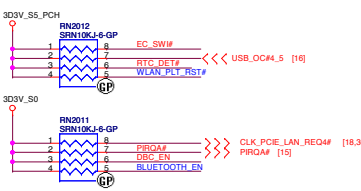
SSID = CPU



Layout Note:
 1. Referenced "continuous" VSS plane only.
 2. Avoid routing next to clock pins or noisy signals.
 3. Trace width: 12-15mil
 4. Isolation Spacing: 12mil
 5. Max length: 500mil



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PCH strap pin:

| | |
|-----------|--|
| NO REBOOT | |
| HDA_SPKR | * Low = Enable (Default) High = Disable |

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

| | |
|------------------------------|--|
| Top-Block Swap Override mode | |
| SDIO_D0 / GPIO66 | * High = Enable "Top-Block swap" mode * Low = Disable "Top-Block swap" mode (Default) |

The internal pull-down is disabled after PLTRST# deasserts

Need SW double confirm if that's needed Top-Block swap

PCH strap pin:

| | |
|---------------------|--|
| TLS Confidentiality | |
| GPIO15 | * Low = Disable Intel ME Crypto TLS (Default) * High = Enable Intel ME Crypto TLS |

The internal pull-down is disabled after RSMRST# deasserts.

PCH strap pin:

| | |
|-------------------------|---------------------------------------|
| Boot BIOS Strap Bit BBS | |
| Boot BIOS Destination | * Low = SPI (Default) * High = LPC |

The internal pull-down is disabled after PLTRST# deasserts

Need double confirm, GPIO table set to GPI if that's needed PH or PL

BIOS strap pin:

| BIOS VRAM Size Strap pin | BOARD_ID1 |
|--------------------------|-----------|
| 1G | 0 |
| 2G | 1 |

BIOS strap pin:

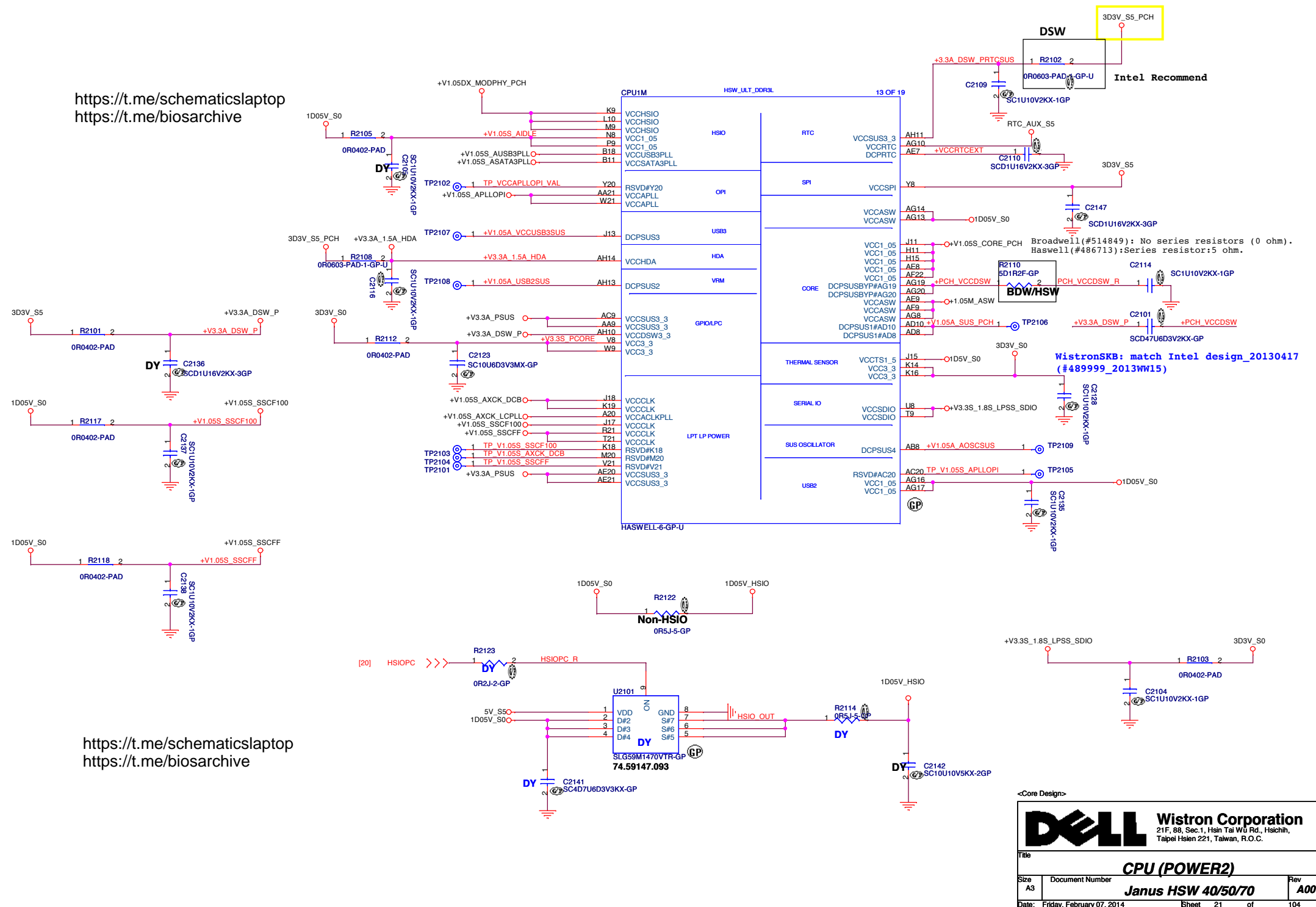
| BIOS UMA/DIS Strap pin | BOARD_ID2 |
|------------------------|-----------|
| UMA | 0 |
| DIS | 1 |

BIOS strap pin:

| BIOS UMA/DIS Strap pin | BOARD_ID3 |
|------------------------|-----------|
| N15V-GM-S(DVC40/50) | 0 |
| N15S-GT (DVC70) | 1 |

SSID = CPU

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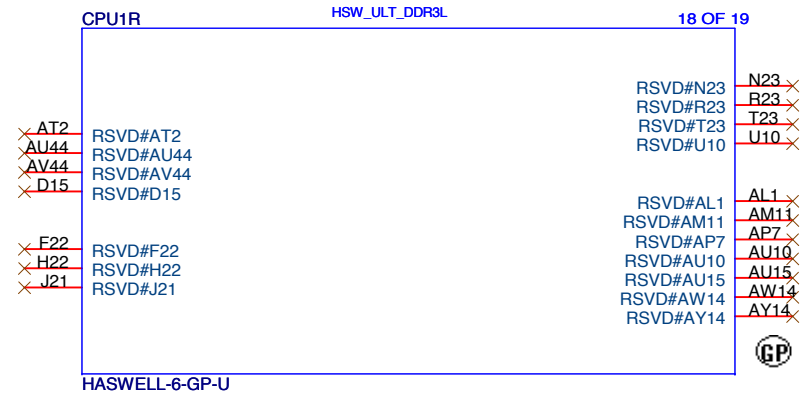
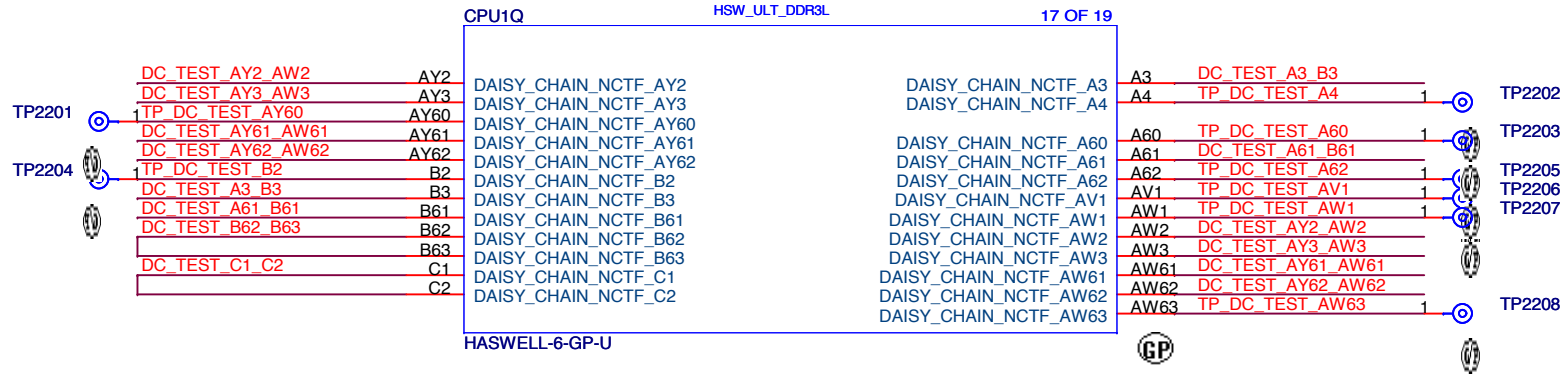
<Core Design>

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Title: **CPU (POWER2)**

| | | |
|---------------------------------|--|-----------------|
| Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00 |
| Date: Friday, February 07, 2014 | Sheet: 21 of 104 | |

SSID = PCH

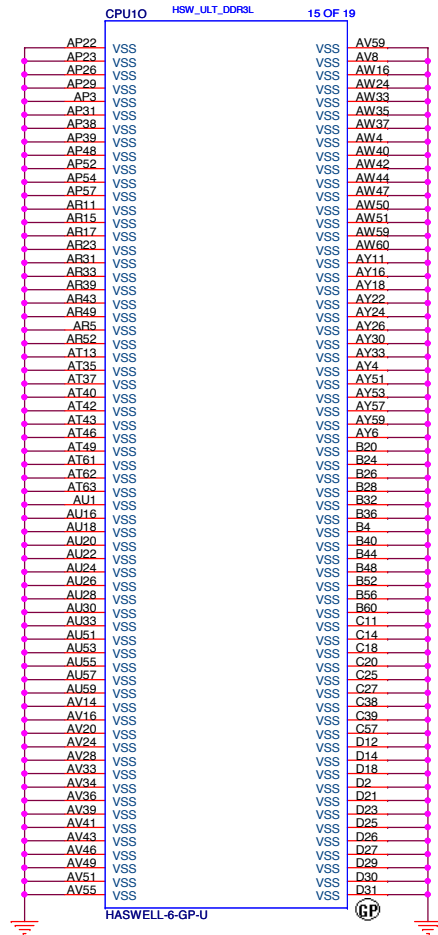
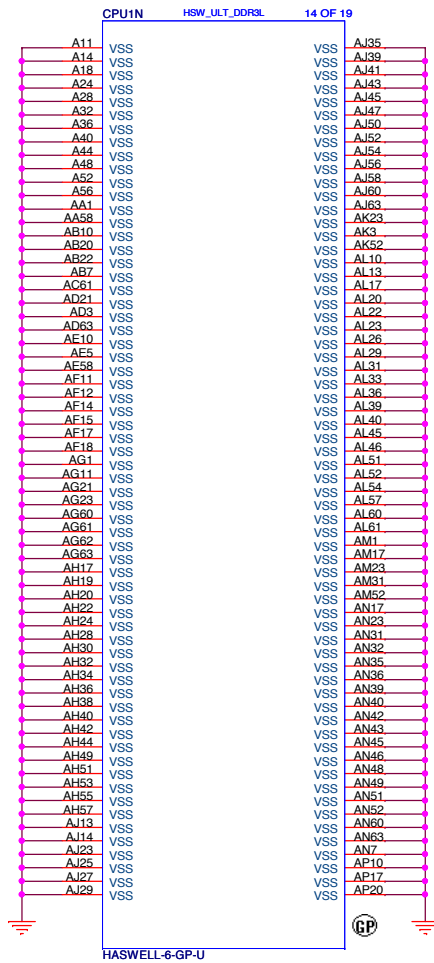


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| | | | |
|-------------------|---------------------------|--|-----------|
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| Title | | | |
| CPU (RSVD) | | | |
| Size | Document Number | Rev | |
| A4 | Janus HSW 40/50/70 | A00 | |
| Date: | Friday, February 07, 2014 | Sheet | 22 of 104 |

SSID = PCH

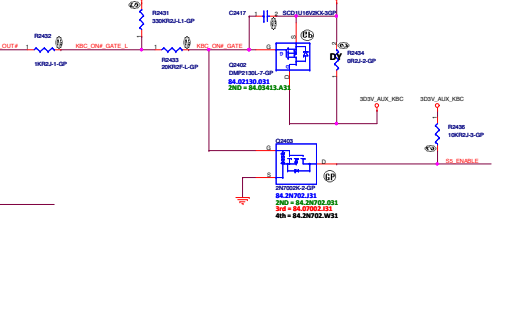
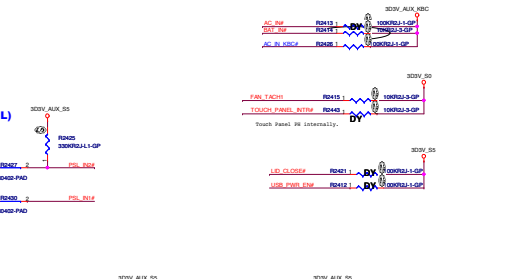
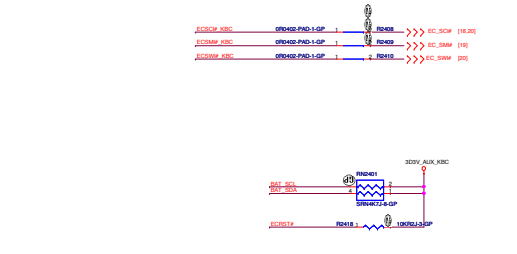
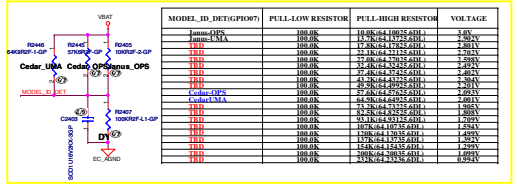
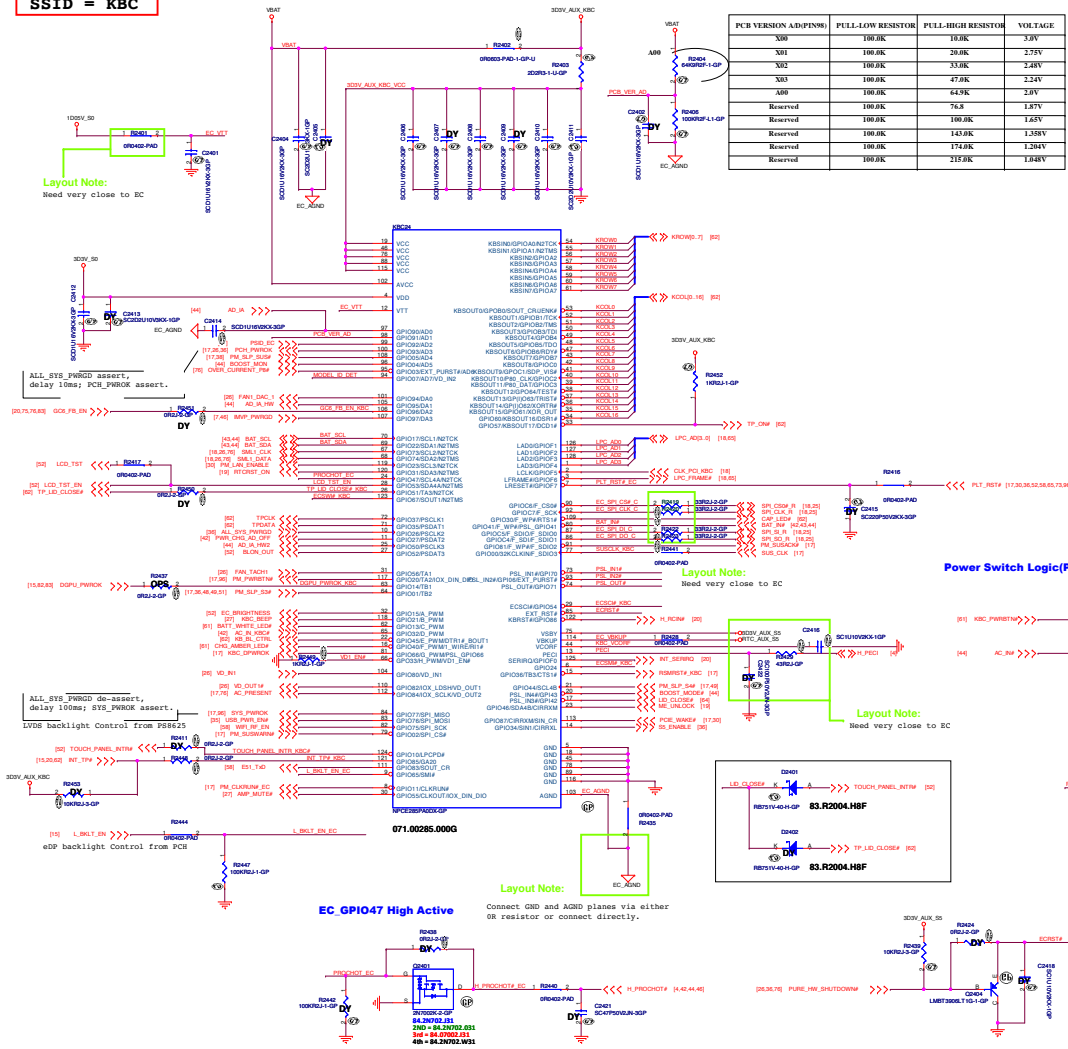


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| | | | | | |
|---|---------------------------|--|--|-------|-----------|
|  | | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title | | | | | |
| CPU(VSS) | | | | | |
| Size | Document Number | | | | Rev |
| A3 | Janus HSW 40/50/70 | | | | A00 |
| Date: | Friday, February 07, 2014 | | | Sheet | 23 of 104 |

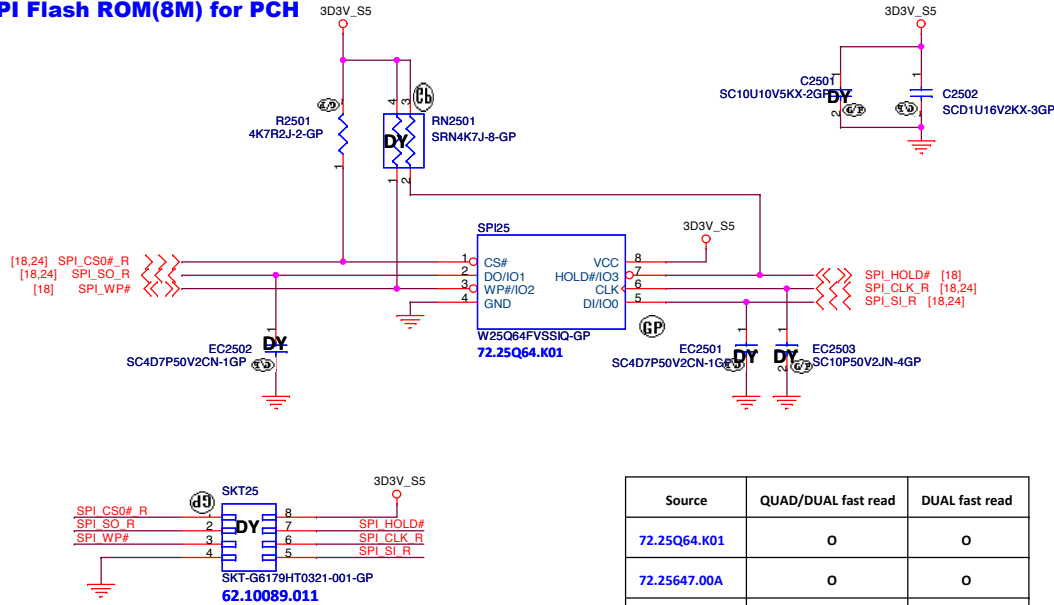
SSID = KBC



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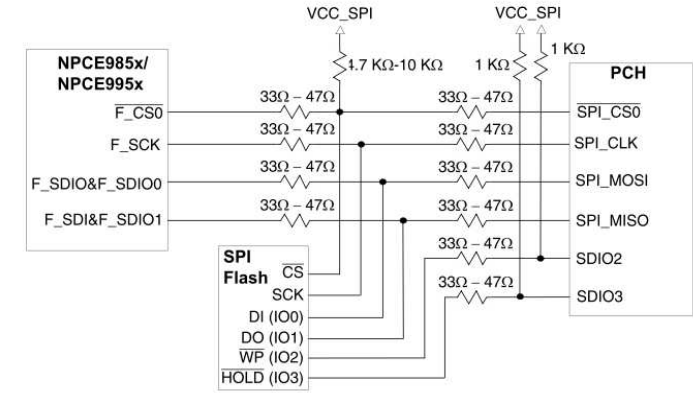
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



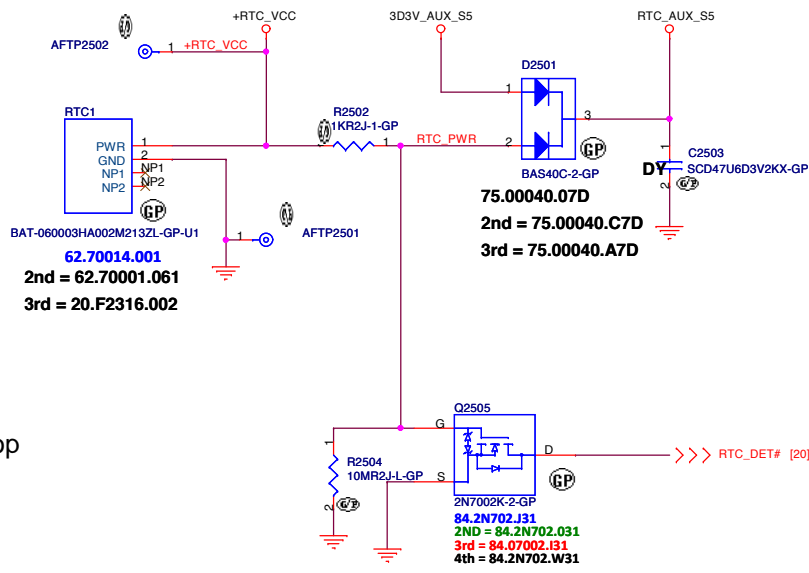
| Source | QUAD/DUAL fast read | DUAL fast read |
|----------------|---------------------|----------------|
| 72.25Q64.K01 | o | o |
| 72.25647.00A | o | o |
| 072.25B64.0001 | o | o |

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NPCE985x/ NPCE995x board design reference guide"

SSID = RBATT



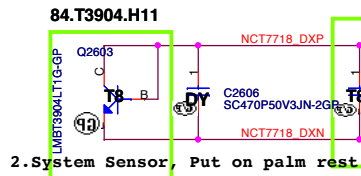
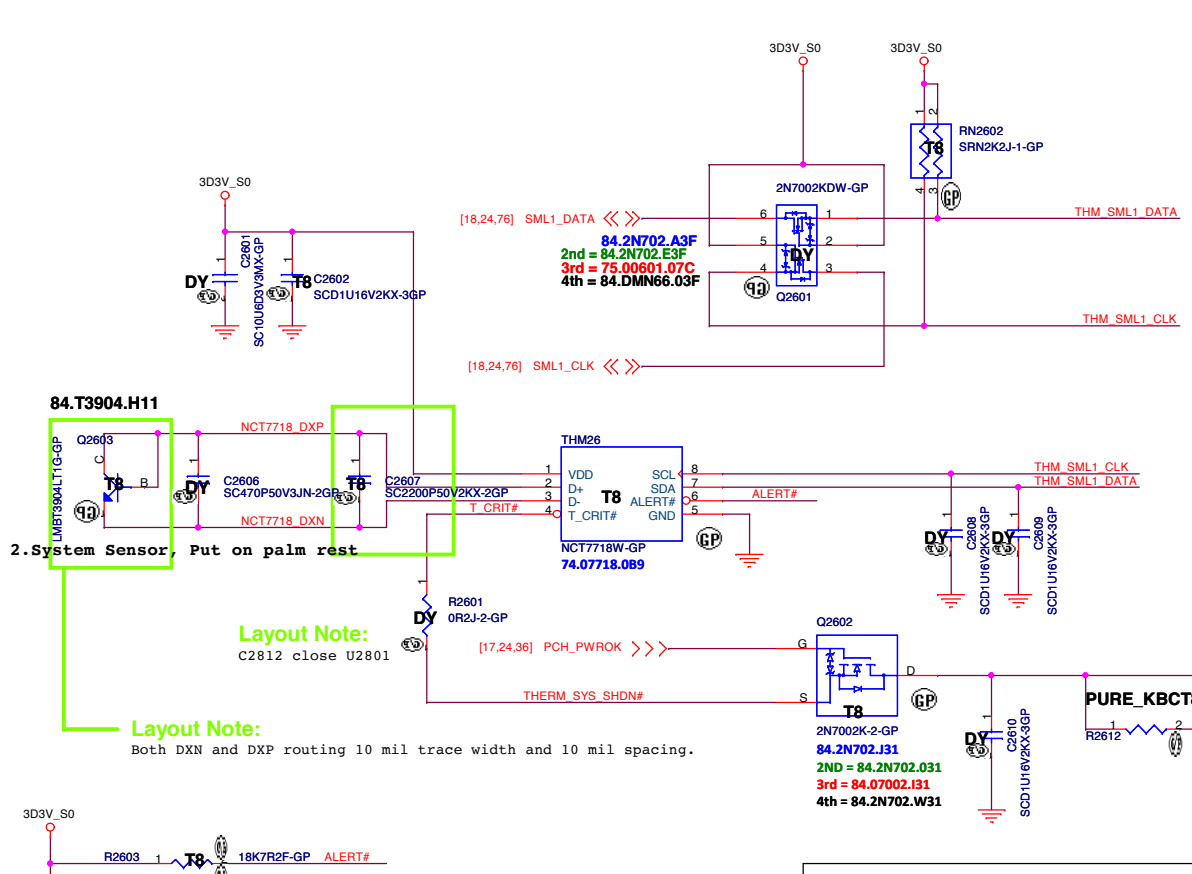
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Title: **Flash/RTC**

| | | |
|---------------------------------|---------------------------|------------|
| Size A3 | Document Number | Rev |
| | Janus HSW 40/50/70 | A00 |
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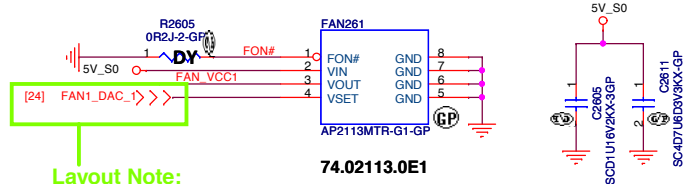
Layout Note:
C2812 close U2801

Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

| TEMPERATURE (°C) | T_CRIT# | | | | |
|------------------|---------|-------|--------|------|--------|
| | 2KΩ | 7.5KΩ | 10.5KΩ | 14KΩ | 18.7KΩ |
| ALERT# | 2KΩ | 77 | 87 | 97 | 107 |
| | 7.5KΩ | 79 | 89 | 99 | 109 |
| | 10.5KΩ | 81 | 91 | 101 | 111 |
| | 14KΩ | 83 | 93 | 103 | 113 |
| | 18.7KΩ | 85 | 95 | 105 | 115 |

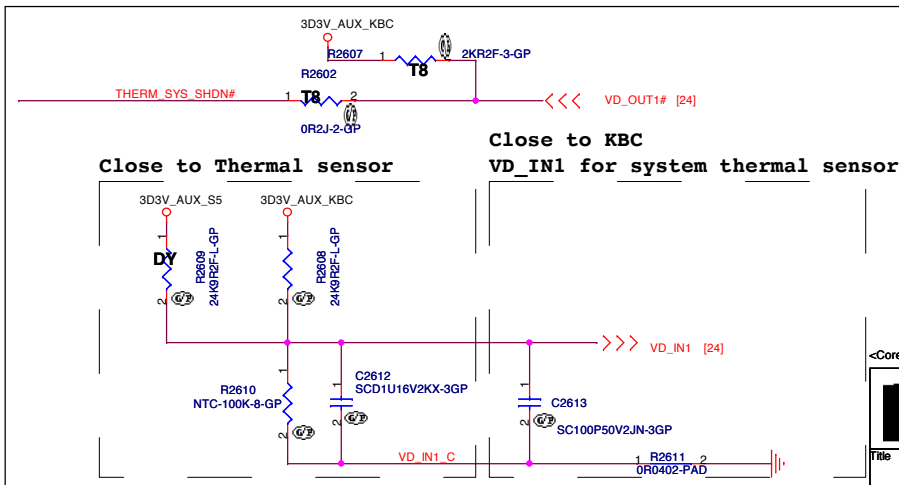
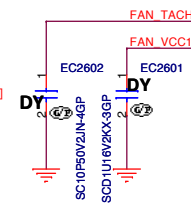
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Fan controller1



Layout Note:
Need 10 mil trace width.

Layout Note:
Signal Routing Guideline:
Trace width = 15mil



Close to Thermal sensor

Close to KBC
VD_IN1 for system thermal sensor

<Core Design>

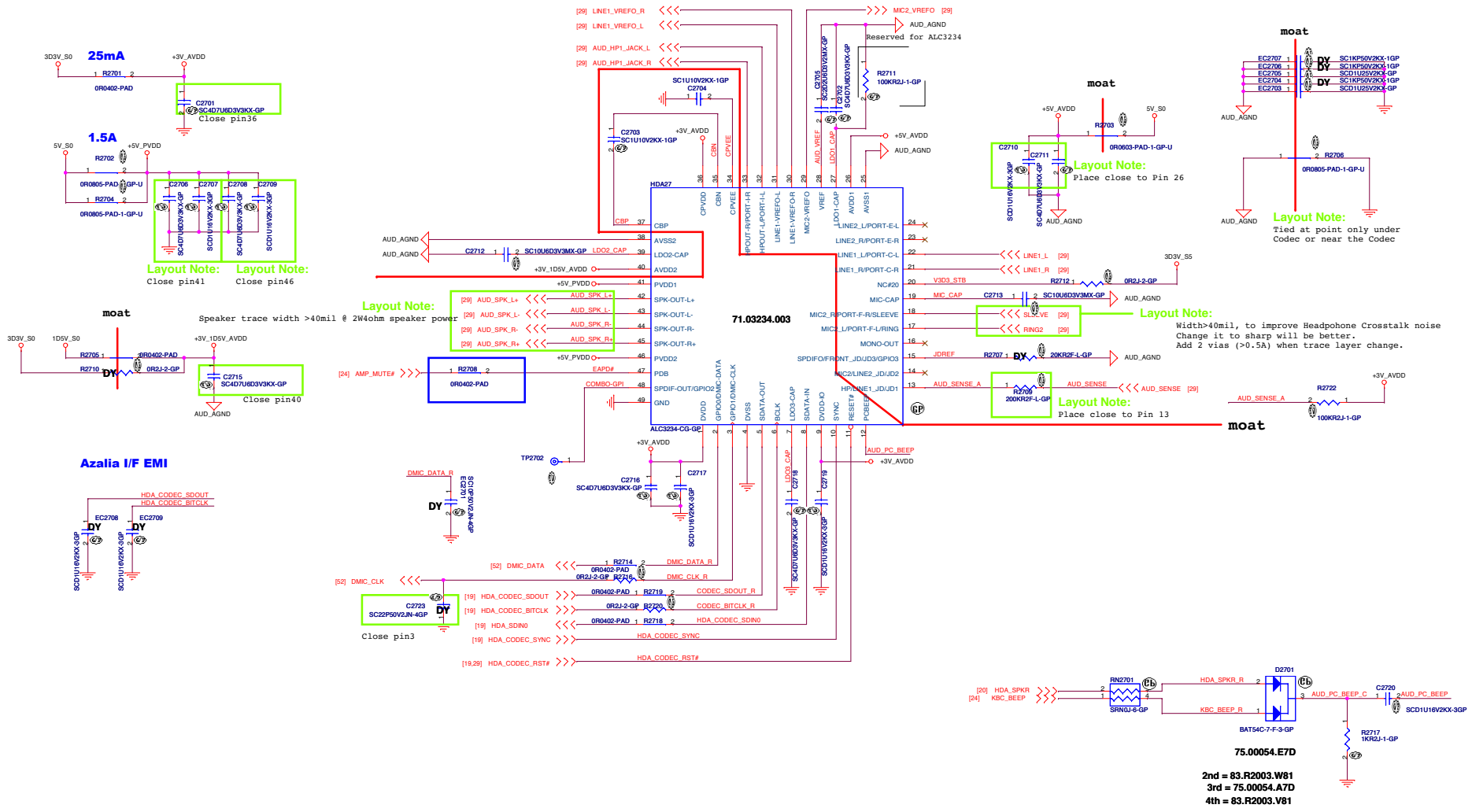
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Title: **THERMAL NCT7718W/Fan**

Size A3 Document Number: **Janus HSW 40/50/70** Rev: **A00**

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SSID = AUDIO



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Title

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A4

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Rev
A00

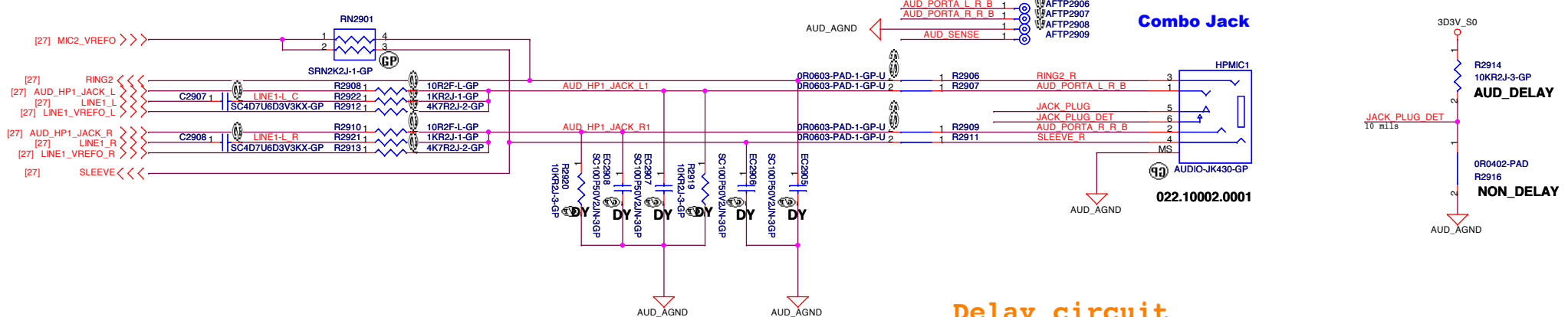
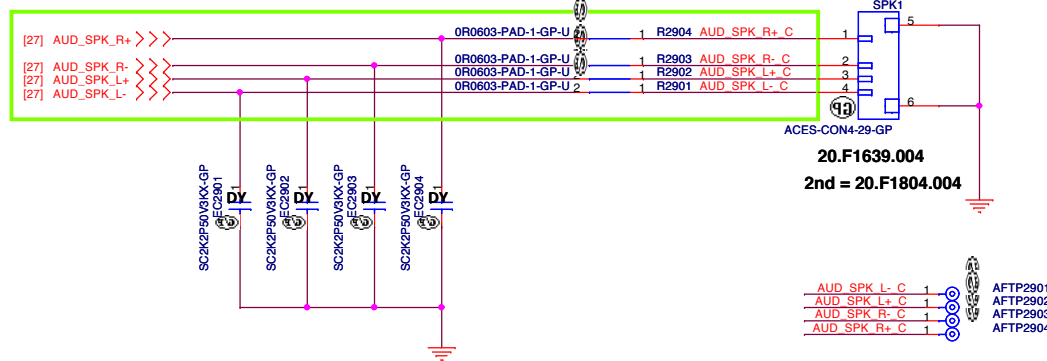
Date: Friday, February 07, 2014

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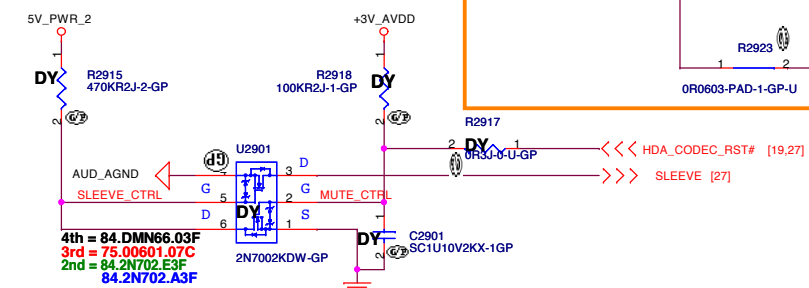
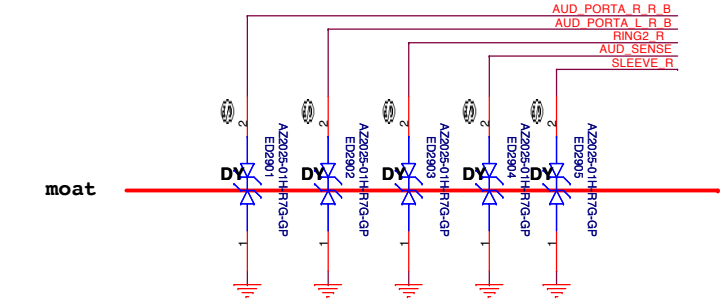
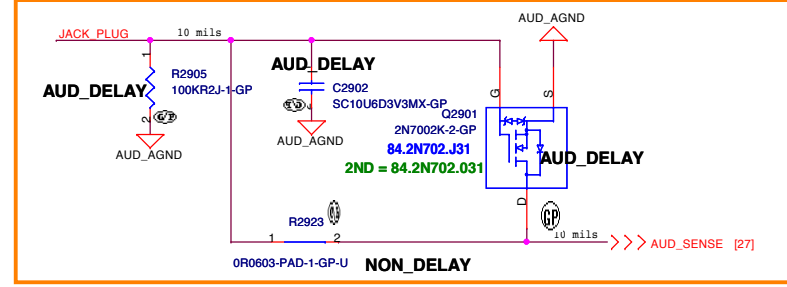
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Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power



Delay circuit



<Core Design>

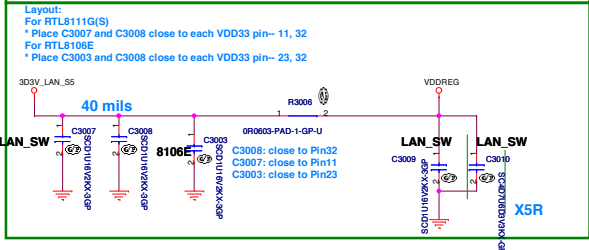
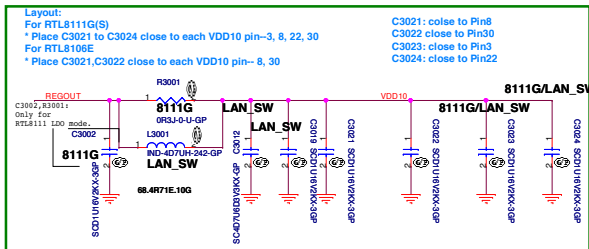
DELL Wistron Corporation
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Title: **Speaker/HPMIC**

Size A3 Document Number: **Janus HSW 40/50/70** Rev: **A00**

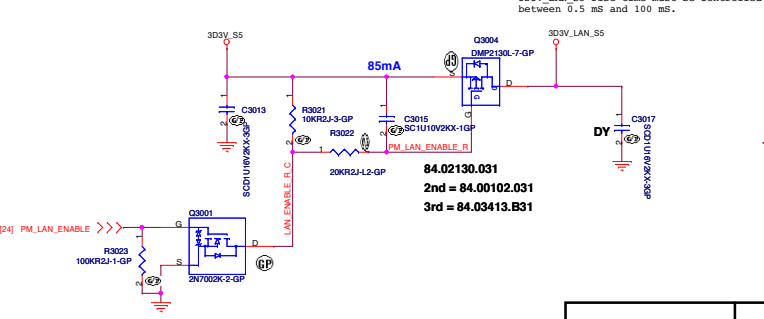
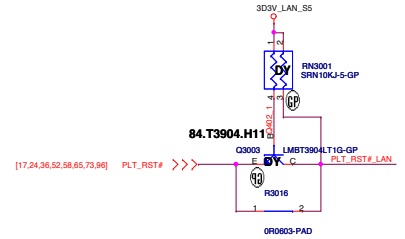
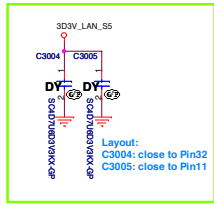
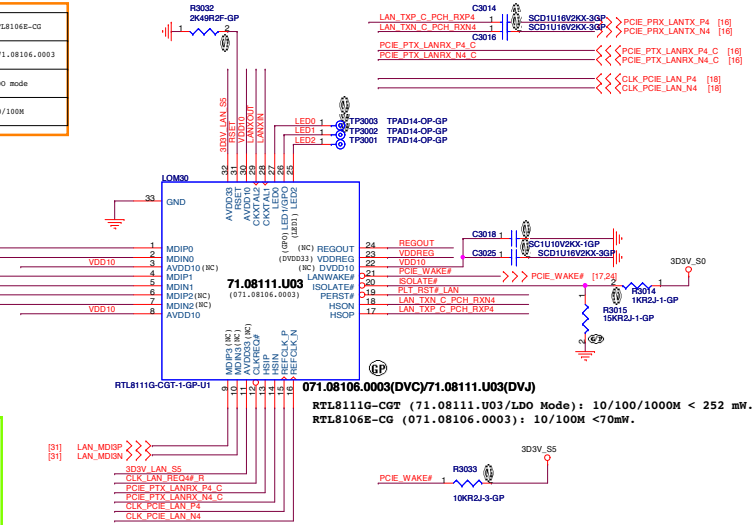
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LAN CHIP (10/100/1000M & 10/100M co-lay)



| RTL811100B-CG | RTL8111G-CGT | RTL8106EUS-CG | RTL8106E-CG |
|---------------|--------------|---------------|----------------|
| 71.08111.W03 | 71.08111.003 | 71.08106.003 | 071.08106.0003 |
| SWR mode | LDO mode | SWR mode | LDO mode |
| 10/100/1000M | 10/100/1000M | 10/100M | 10/100M |

- [31] LAN_MDSP >>>
- [31] LAN_MDIN >>>
- [31] LAN_MDIN >>>
- [31] LAN_MDIN >>>
- [31] LAN_MDIN >>>
- [31] LAN_MDIN >>>
- [31] LAN_MDIN >>>



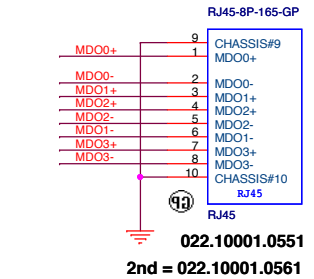
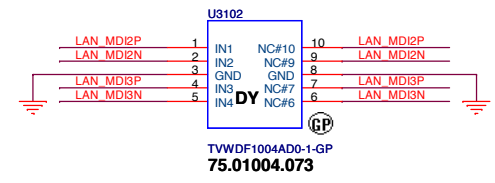
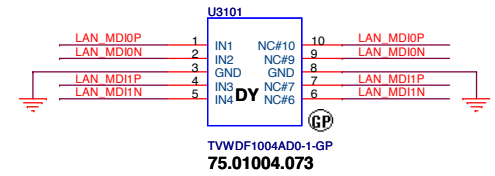
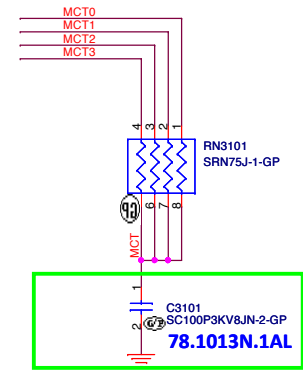
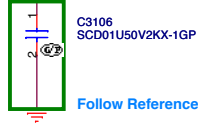
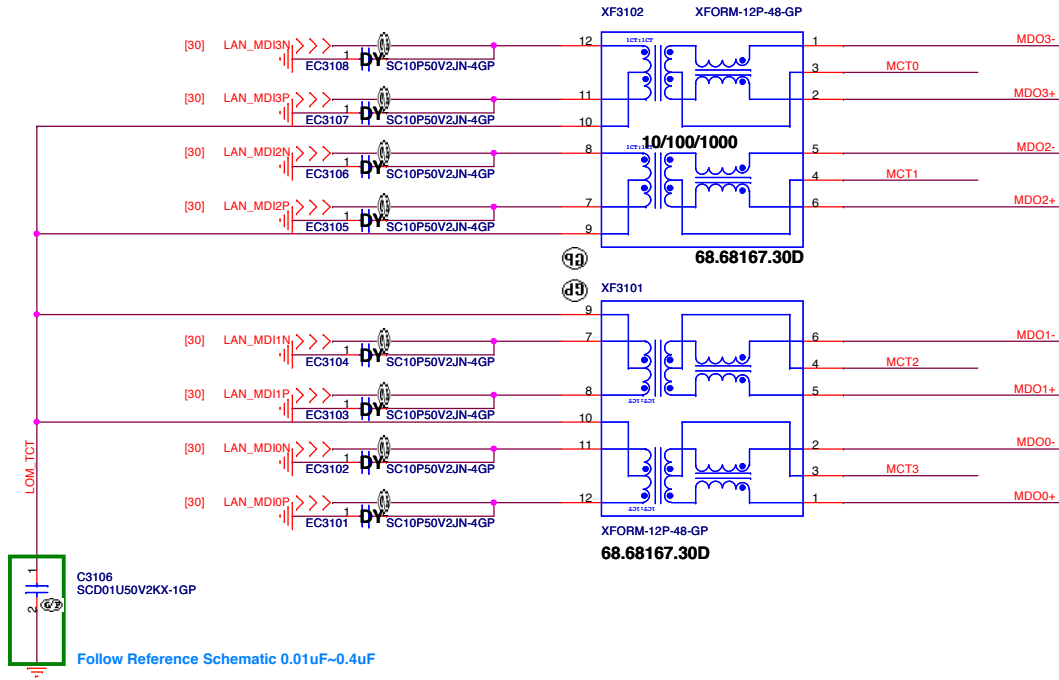
| | 1.0V Source | R3001 | C3002 | C3023 | C3024 | C3007 | L3001 | C3012 | C3019 | C3009 | C3010 | C3003 |
|---|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| RTL8111G-CGT (71.08111.U03) | LDO | O | O | O | O | O | X | X | X | X | X | X |
| RTL8111GUS-CG (71.08111.W03) / RTL8106EUS-CG (71.08106.003) | SWR | X | X | O | O | O | O | O | O | O | O | X |
| RTL8106E-CG (071.08106.0003) | LDO | X | X | X | X | X | X | X | X | X | X | O |

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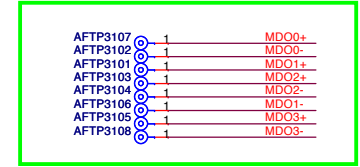
SSID = LOM

LAN Transformer (10/100/1000M & 10/100M co-lay)

Layout note:
30 mil spacing between MDI differential pairs.



Layout:
Place near RJ45



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Title: **XFOM&RJ45**

| | | |
|---------------------------------|--|-----------------|
| Size: A3 | Document Number: Janus HSW 40/50/70 | Rev: A00 |
| Date: Monday, February 10, 2014 | Sheet 31 of 104 | |

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| | | |
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| Title <i>(Reserved)Card Reader</i> | | |
| Size A4 | Document Number <i>Janus HSW 40/50/70</i> | Rev <i>A00</i> |
| Date: Friday, February 07, 2014 | Sheet 32 of | 104 |

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Title

(Reserved)

Size
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Document Number

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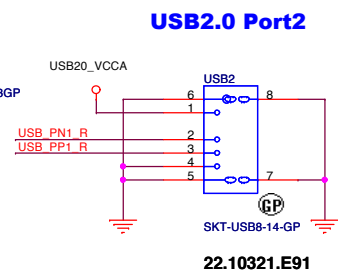
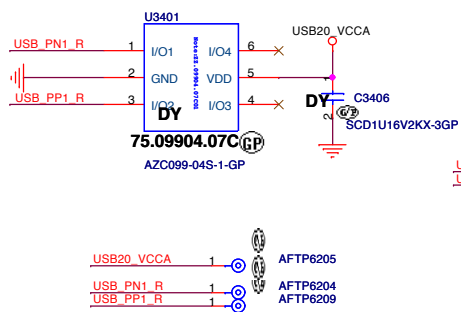
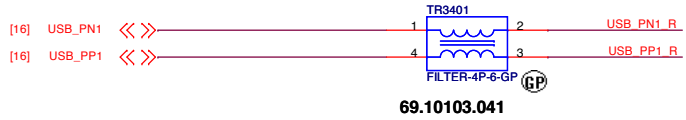
Rev
A00

Date: Friday, February 07, 2014

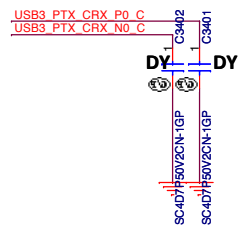
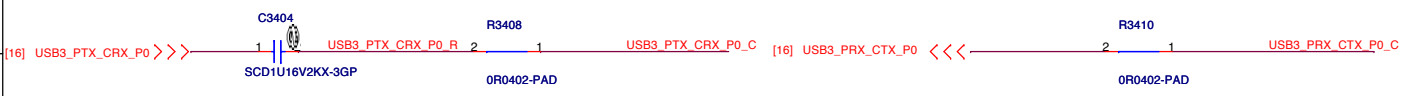
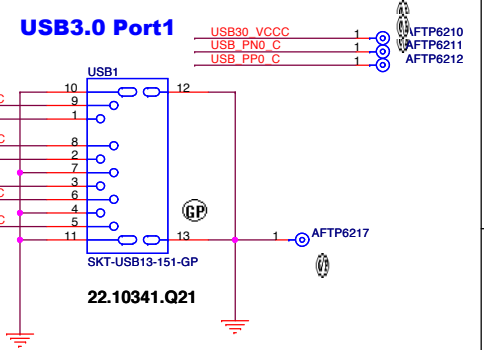
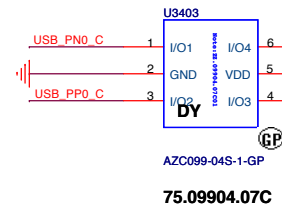
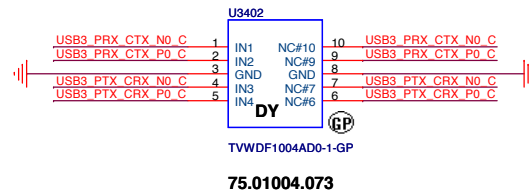
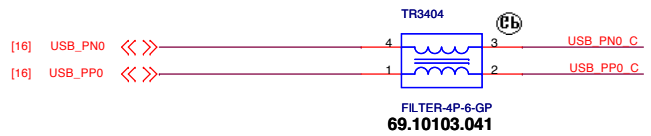
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SSID = USB



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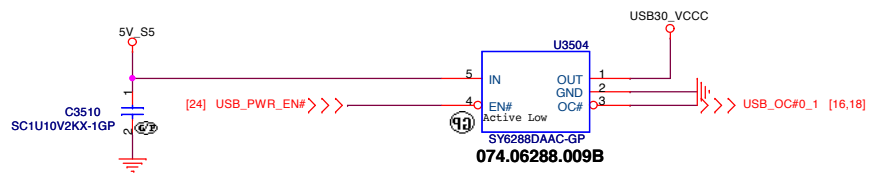
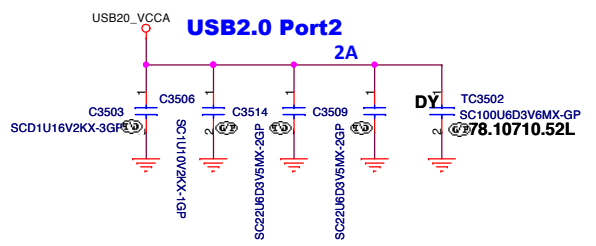
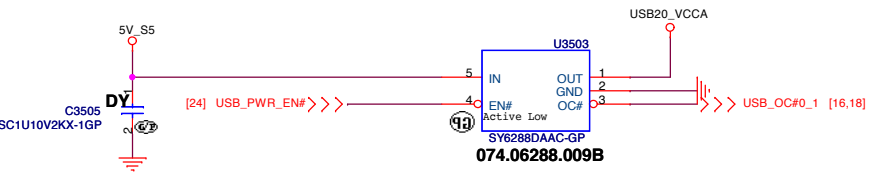
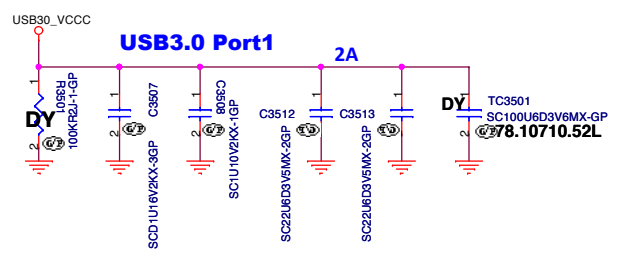
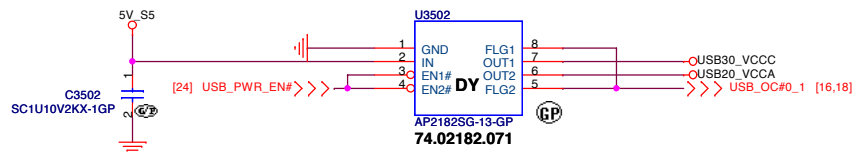
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DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

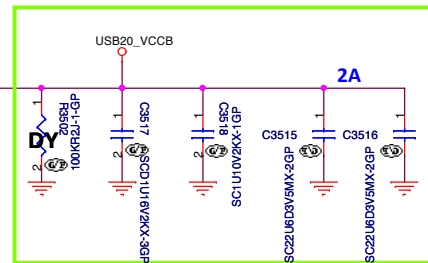
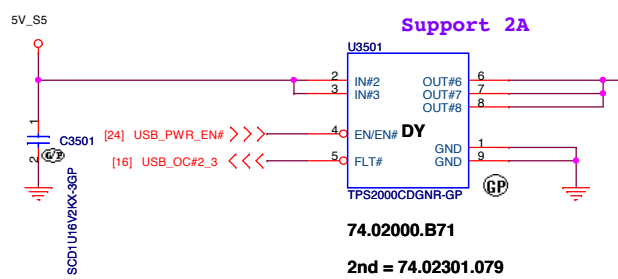
Title: **USB 3.0**

| | | |
|--------|---------------------------|------------|
| Size | Document Number | Rev |
| Custom | Janus HSW 40/50/70 | A00 |

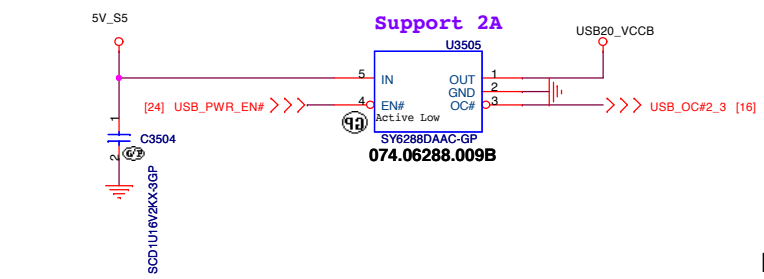
Date: Monday, February 10, 2014 Sheet 34 of 104



Layout Note: Close CON1



USB2.0 Port3 (IO Board)



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<https://t.me/biosarchive>

<Core Design>

Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Power SW**

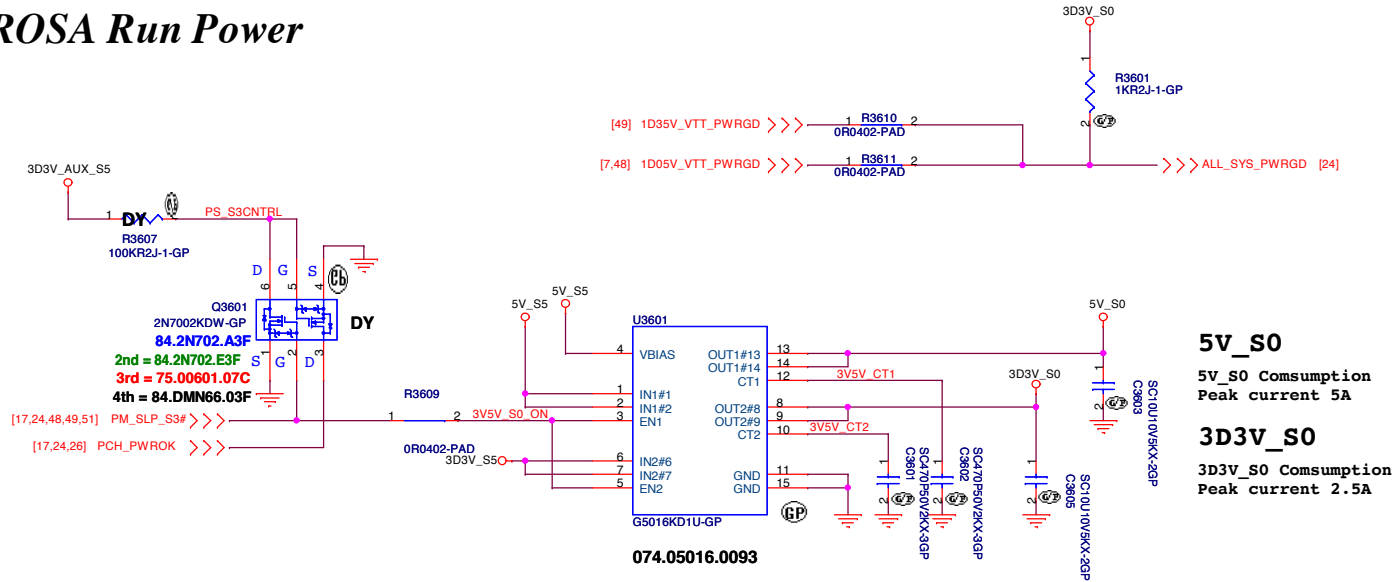
| | | |
|------|---------------------------|------------|
| Size | Document Number | Rev |
| | Janus HSW 40/50/70 | A00 |

Date: Friday, February 07, 2014 Sheet 35 of 104

SSID = Reset.Suspend

Power Good

ROSA Run Power

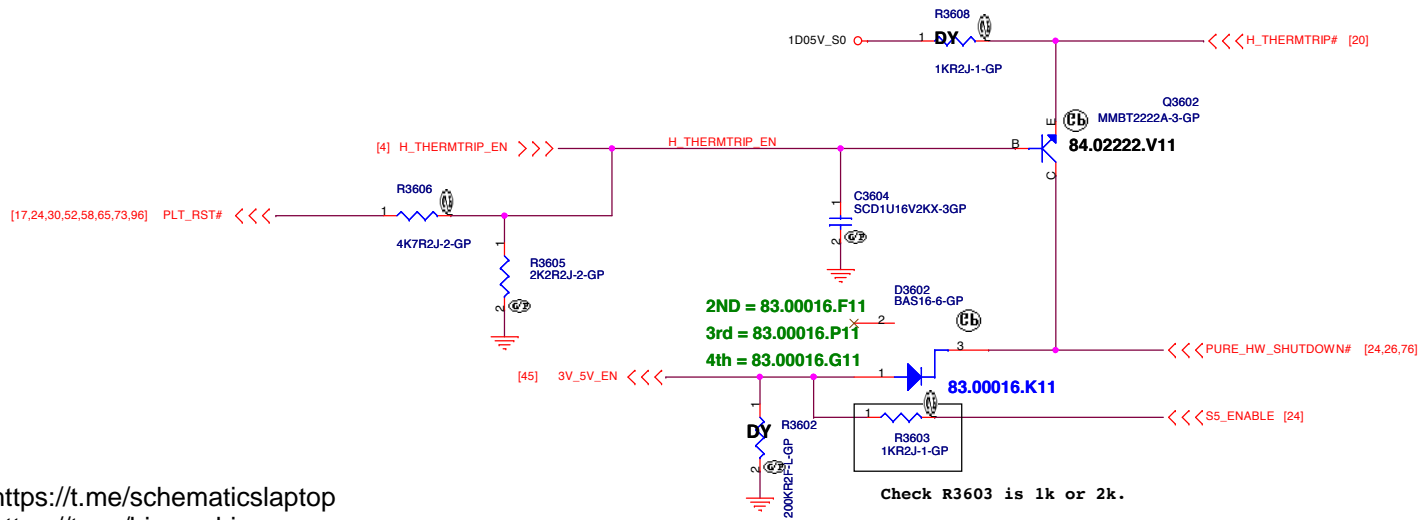


5V_S0

5V_S0 Consumption
Peak current 5A

3D3V_S0

3D3V_S0 Consumption
Peak current 2.5A



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<https://t.me/biosarchive>

<Core Design>

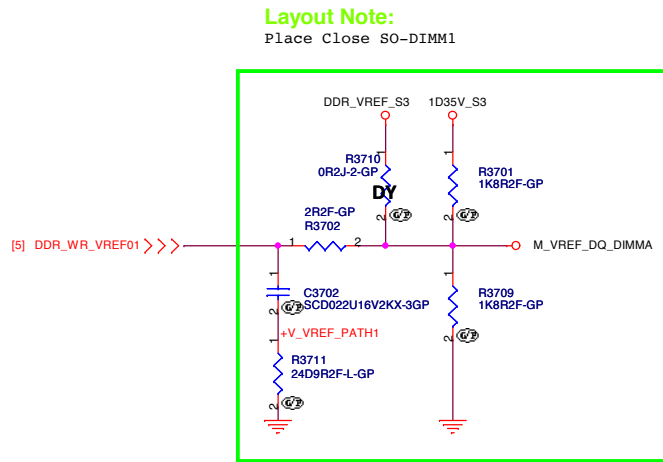
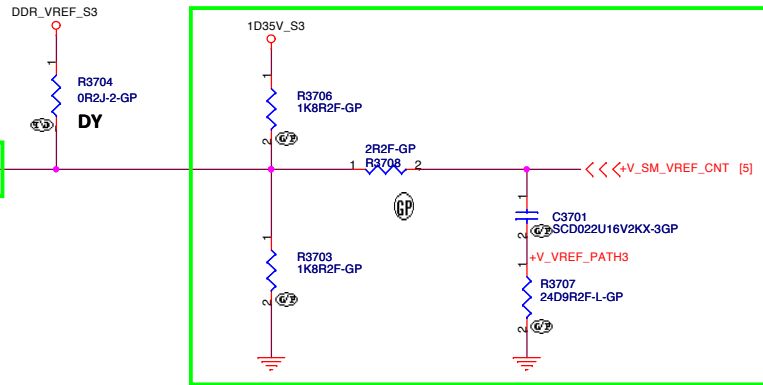
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

| | | |
|---------------------------------|--|-----------------|
| Size A3 | Document Number: Janus HSW 40/50/70 | Rev: A00 |
| Date: Monday, February 10, 2014 | Sheet 36 of 104 | |

SSID = Reset.Suspend

SODIMM1
M_VREF_CA_DIMMA

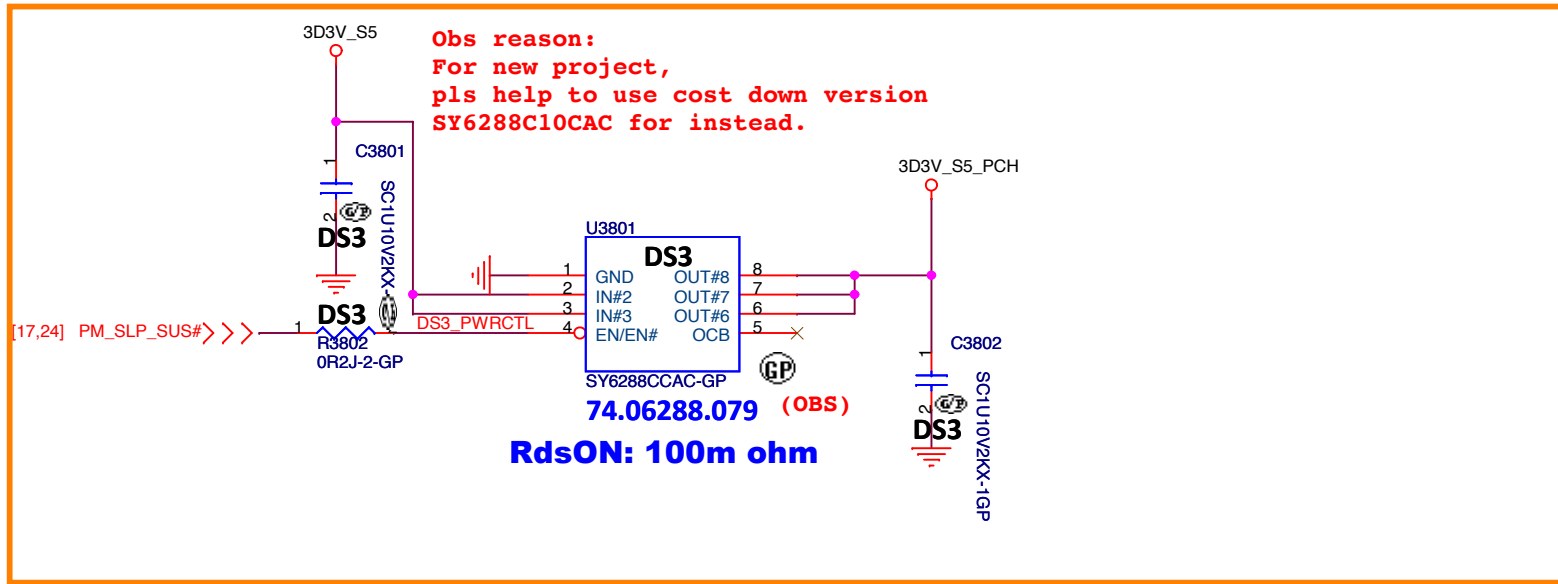


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<Core Design>

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| | | |
|---------------------------------|-----------------|------------|
| Title | | |
| S3 Reduction Circuit | | |
| Size A3 | Document Number | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 97 | of 104 |



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<https://t.me/biosarchive>

<Core Design>

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|---------------------------------|--|---|
| DELL | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title DSW | | |
| Size A4 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 38 of | 104 |

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved) 1D05_M


| | | |
|------------|--|-------------------|
| Size A4 | Document Number Janus HSW 40/50/70 | Rev A00 |
|------------|--|-------------------|

Date: Friday, February 07, 2014 Sheet 39 of 104

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<Core Design>

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|---|--|---|
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | | |
| Reserved | | |
| Size A4 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 40 of | 104 |

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Title

Reserved

Size
A4

Document Number

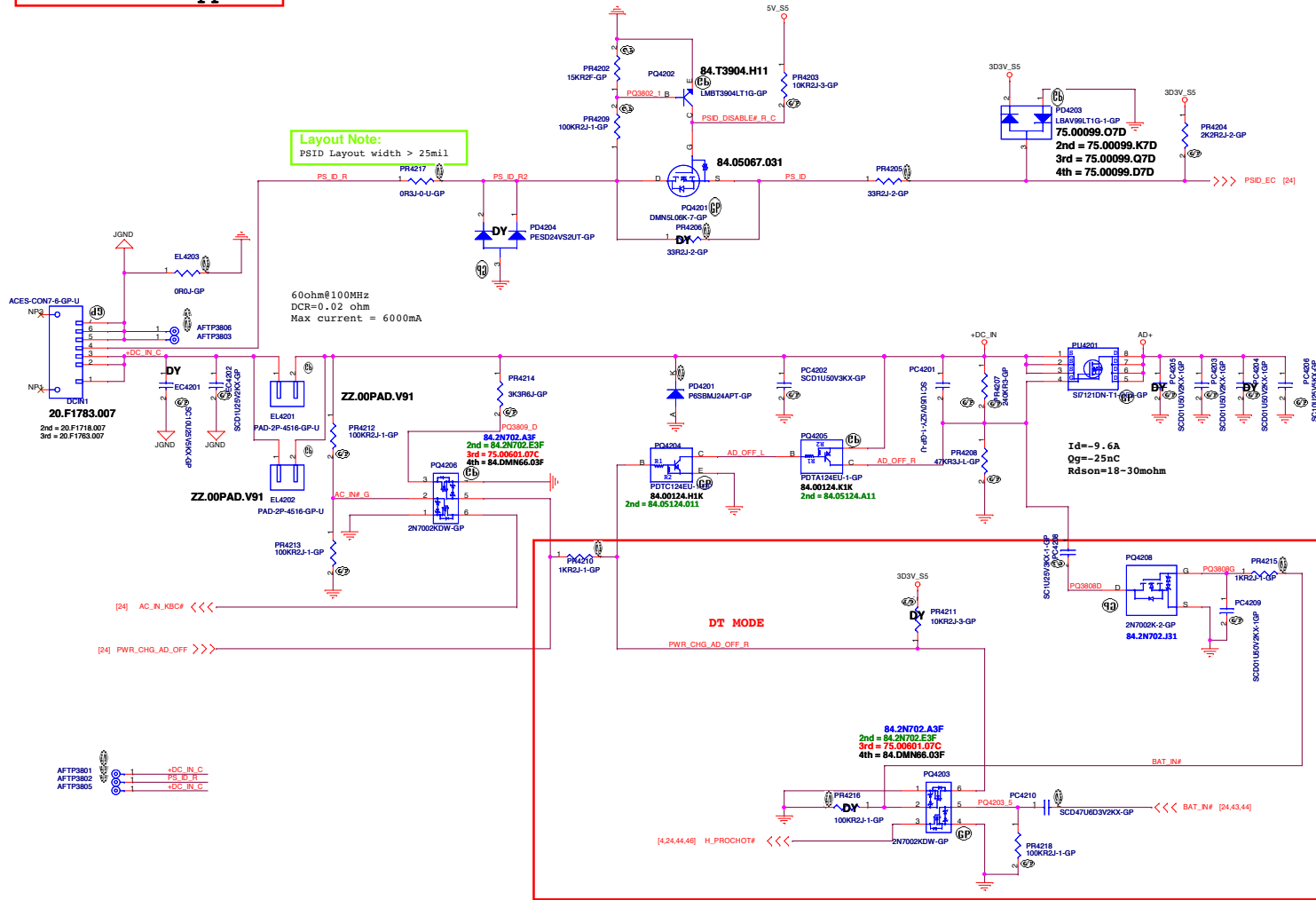
Janus HSW 40/50/70

Rev
A00

Date: Friday, February 07, 2014

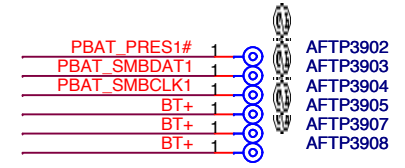
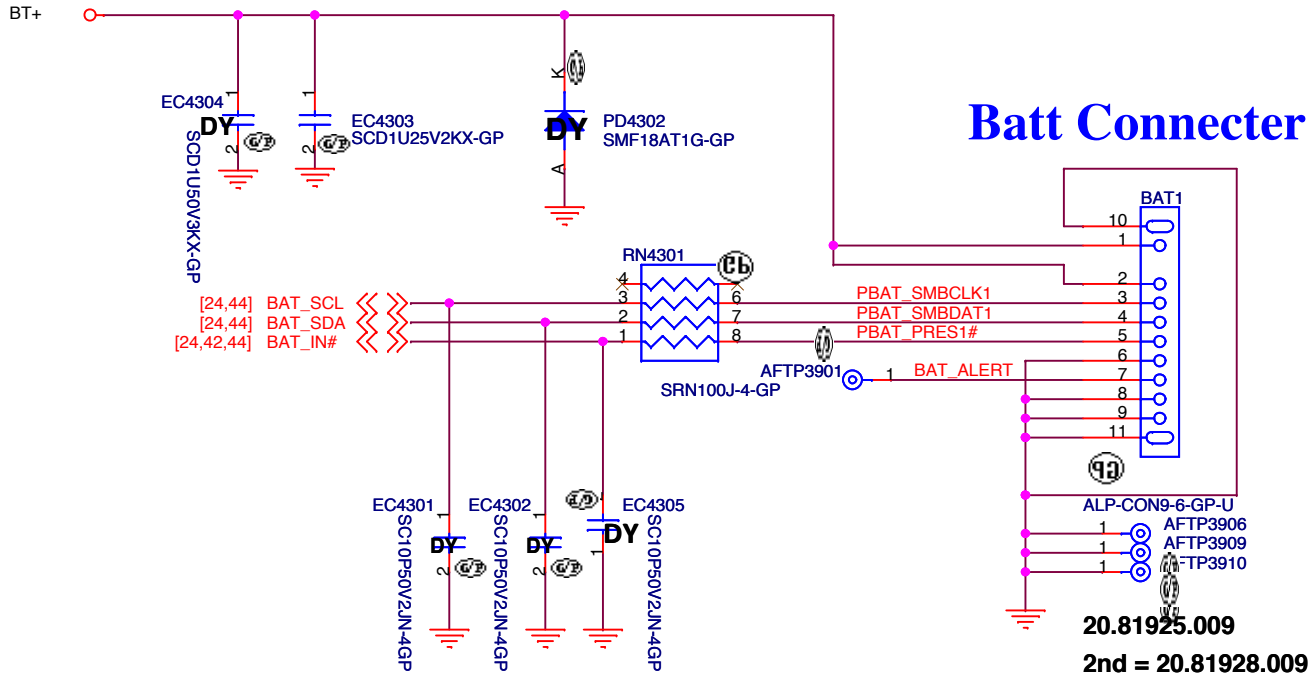
Sheet 41 of 104

SSID = PWR.Support



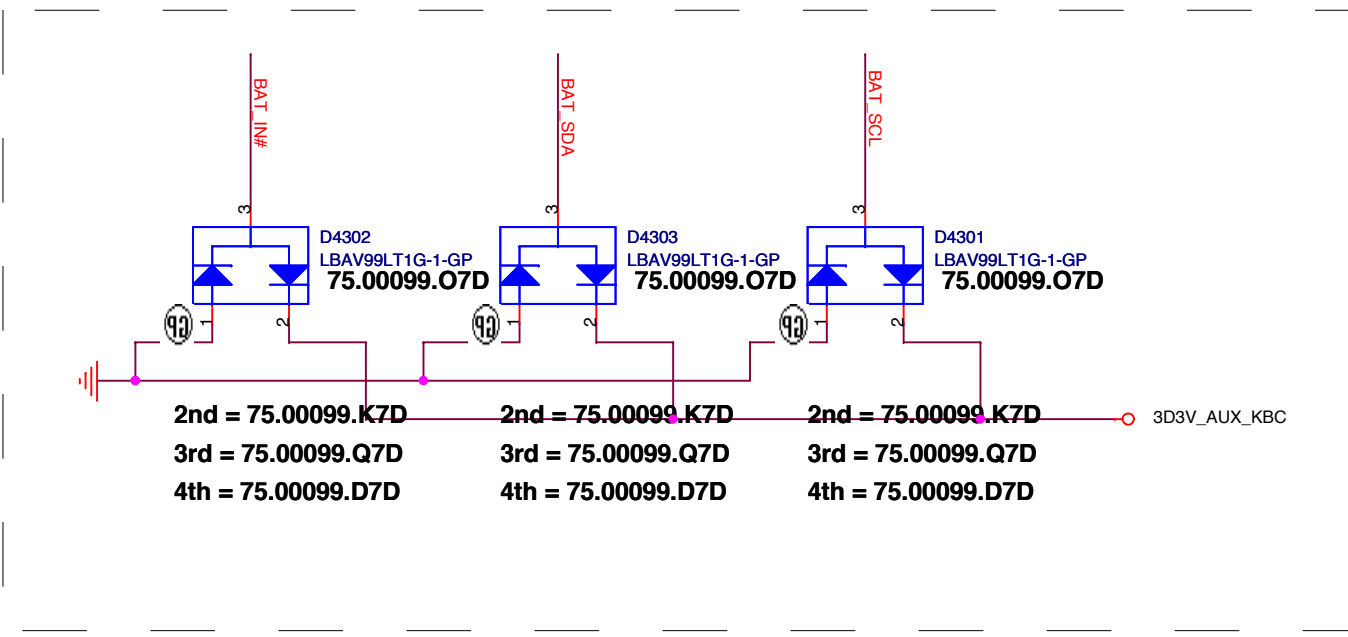
<https://t.me/schematicsLaptop>
<https://t.me/biosarchive>

SSID = PWR.Support




<https://t.me/schematics-laptop>
<https://t.me/biosarchive>

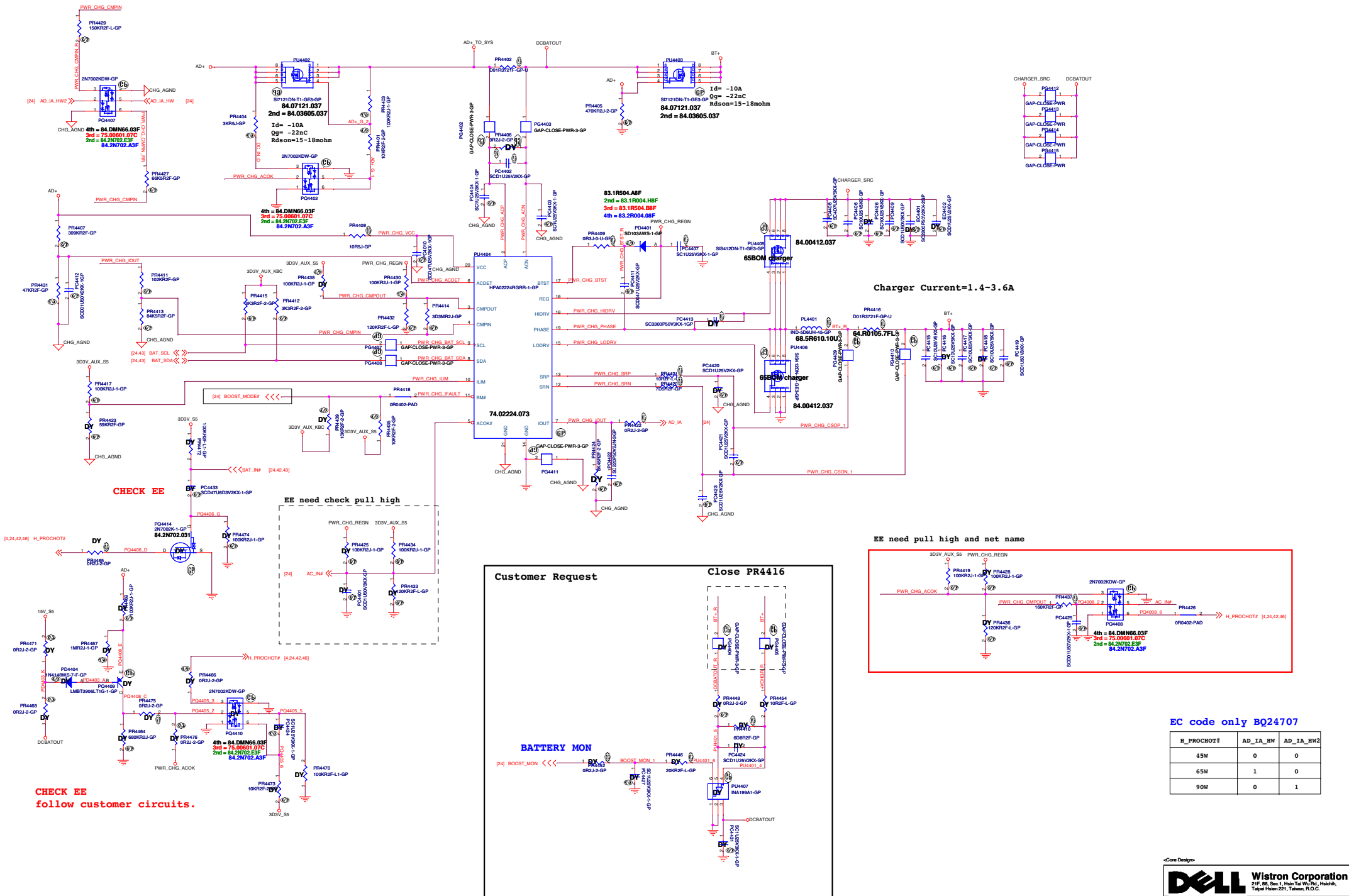
Placement: Close to Batt Connector



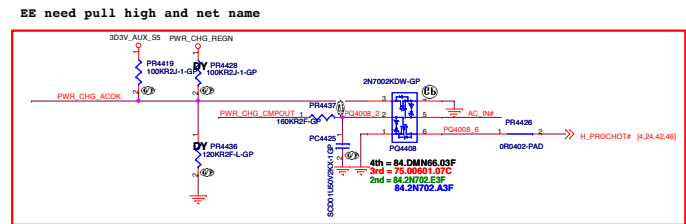
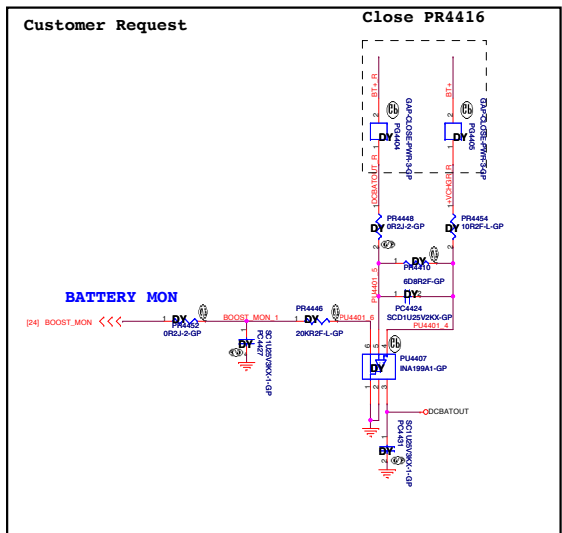
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|---|--|---|-------------------|
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| | | Title <h2 style="text-align: center;">BATT CONN</h2> | |
| Size A4 | Document Number <h3 style="text-align: center;">Janus HSW 40/50/70</h3> | | Rev A00 |
| Date: Friday, February 07, 2014 | | Sheet 43 of 104 | |

SSID = Charger



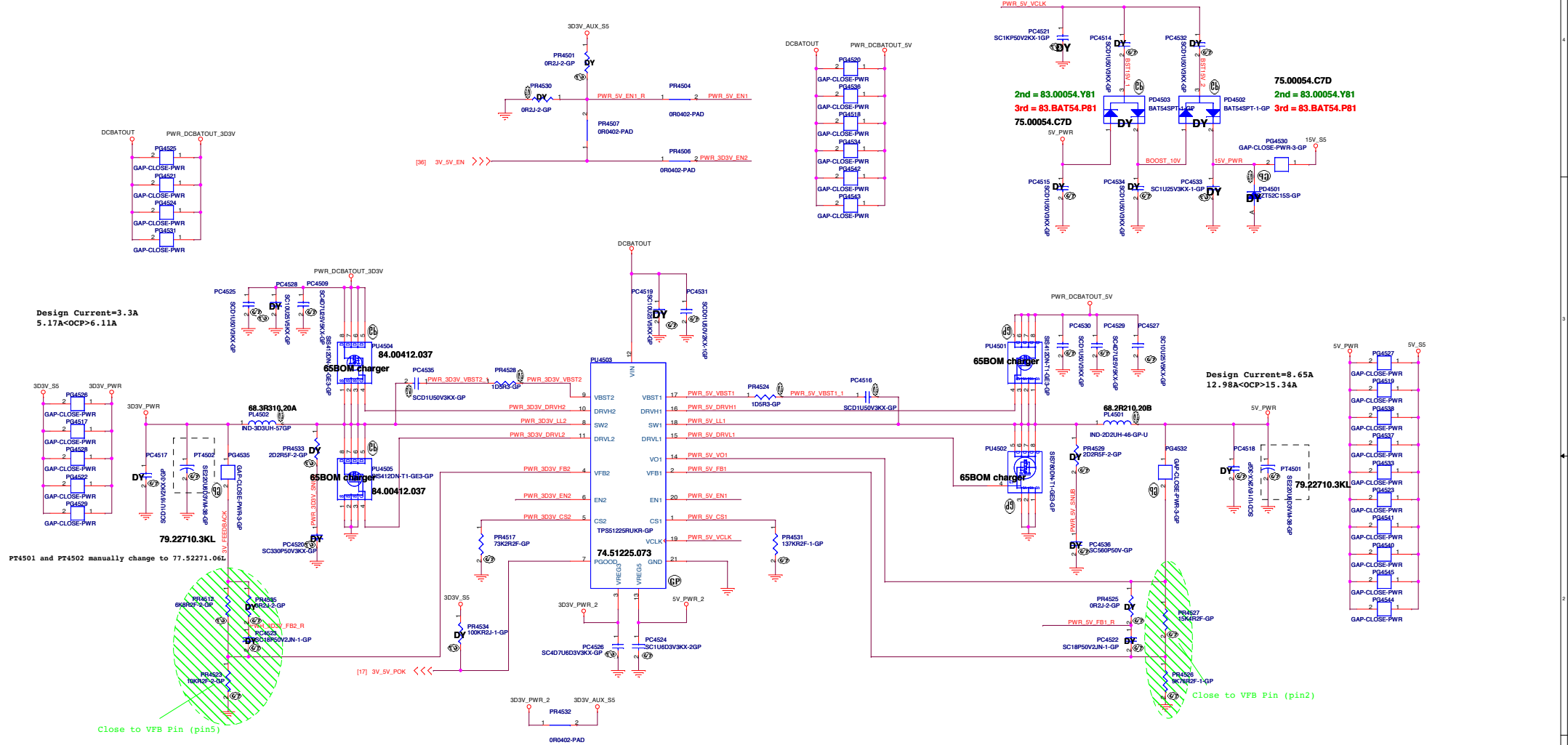
CHECK EE
EE need check pull high



EC code only BQ24707

| H_PROCHOT# | AD_IA_HW | AD_IA_HW2 |
|------------|----------|-----------|
| 45W | 0 | 0 |
| 65W | 1 | 0 |
| 90W | 0 | 1 |

SSID = PWR.Plane.Regulator_5v3p3v



Design Current=3.3A
5.17A<OCP>6.11A

Design Current=8.65A
12.98A<OCP>15.34A

TPS51225 & TPS51285 Co-Lay

| | TPS51225 | TPS51285 |
|--------|----------|----------|
| PR4510 | 45.3KK | 9.09K |
| PR4511 | 110K | 22.1K |

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP IND 3.3UH PCMC063T-3R3M Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
 O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
 H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037
 L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHOK 2.2U PCMC063T-2R2M 18mohm/20mohm Isat =14Arms 68.2R210.20B
 O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
 H/S:SIS412 / 24mOhm/30mOhm4.5Vgs / 84.00412.037
 L/S:SIS780 / 14.5mOhm/17.5mOhm4.5Vgs / 84.00780.037

<Core Design>

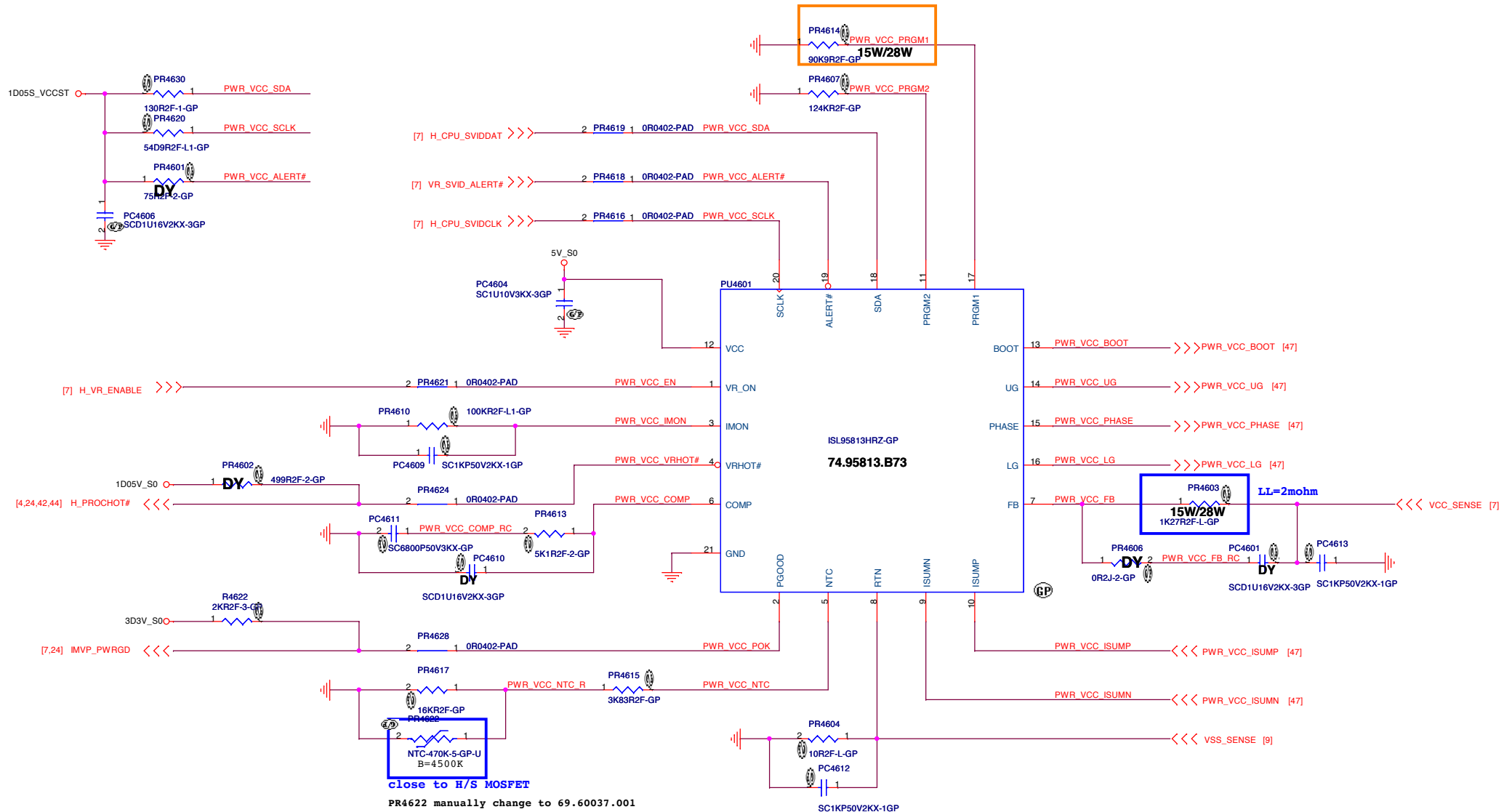
DELL Wistron Corporation
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Title: **3V/5V TPS51225**

Size: 42 Document Number: **Janus HSW 40/50/70** Rev: **ADD**

Date: Friday, February 07, 2014 Sheet: 35 of 103

SSID = CPU.Regulator

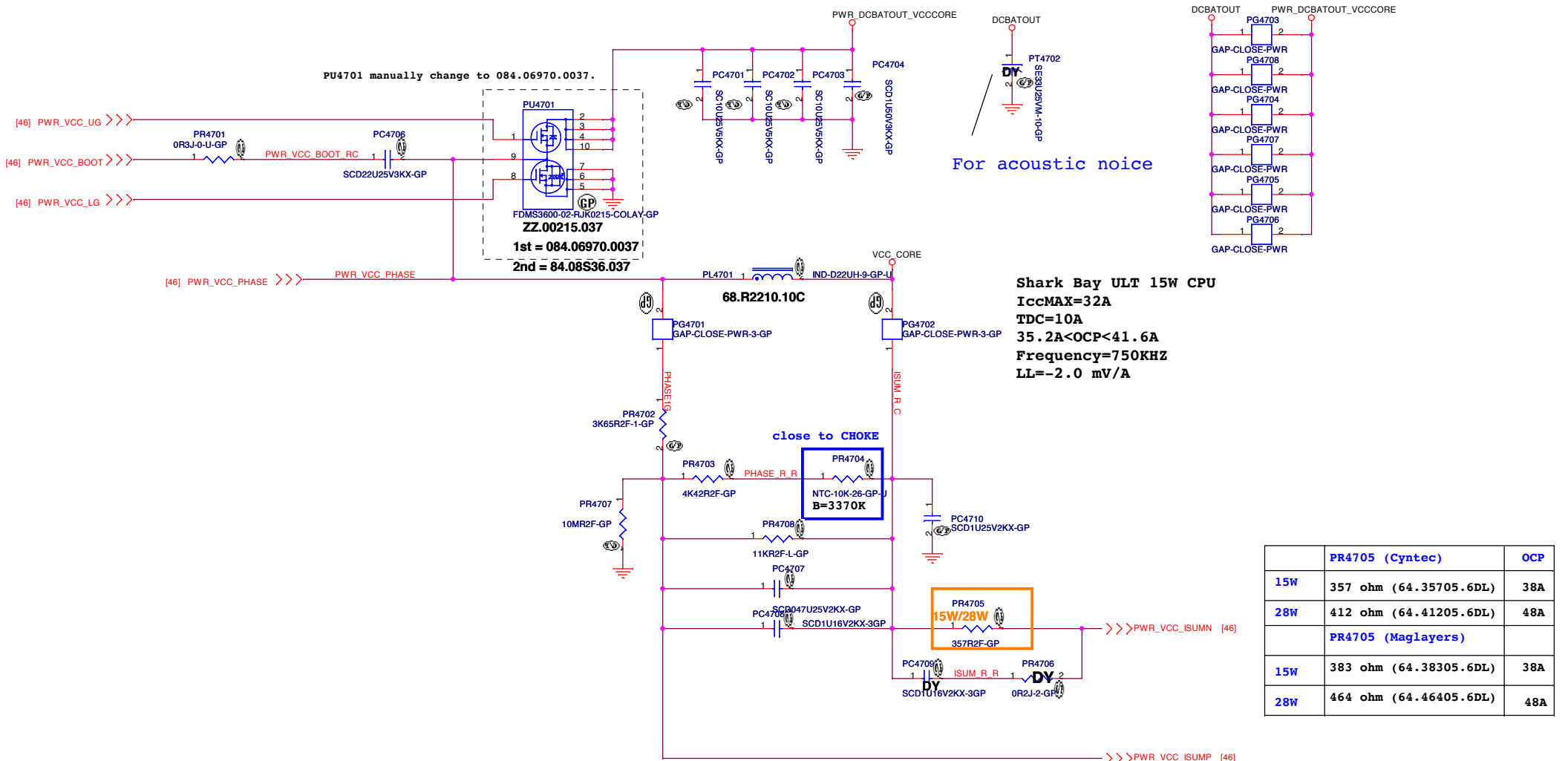


| | PR4603 | PR4614 |
|-----|-----------------------|-----------------------|
| 15W | 1.27K 64.12715.6DL | 90.9K 64.90925.6DL |
| 28W | 1.58K 64.15815.6DL | 113K 64.11335.6DL |

<Core Design>

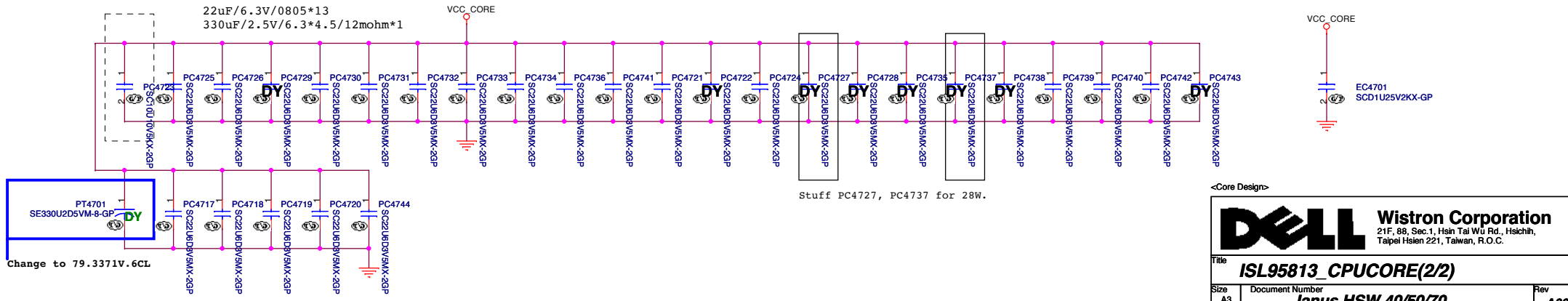


| | | |
|---------------------------------------|--|-------------------|
| Title ISL95813_CPUCORE(1/2) | | |
| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 46 | of 104 |



| | PR4705 (Cyntec) | OCP |
|-----|------------------------|-----|
| 15W | 357 ohm (64.35705.6DL) | 38A |
| 28W | 412 ohm (64.41205.6DL) | 48A |
| | PR4705 (Maglayers) | |
| 15W | 383 ohm (64.38305.6DL) | 38A |
| 28W | 464 ohm (64.46405.6DL) | 48A |

Change PC4723 to 10U from 22U based on PI Simulation.



<Core Design>

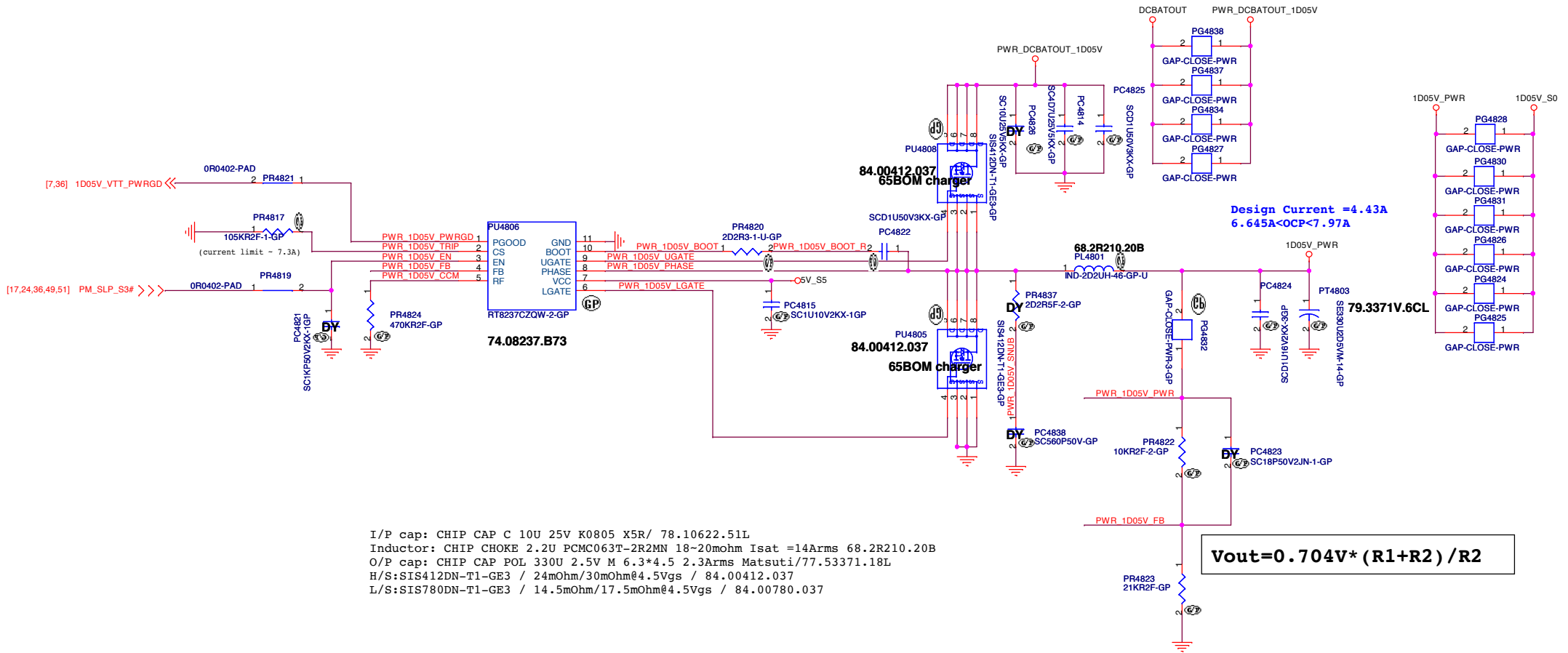
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL95813_CPUCORE(2/2)**

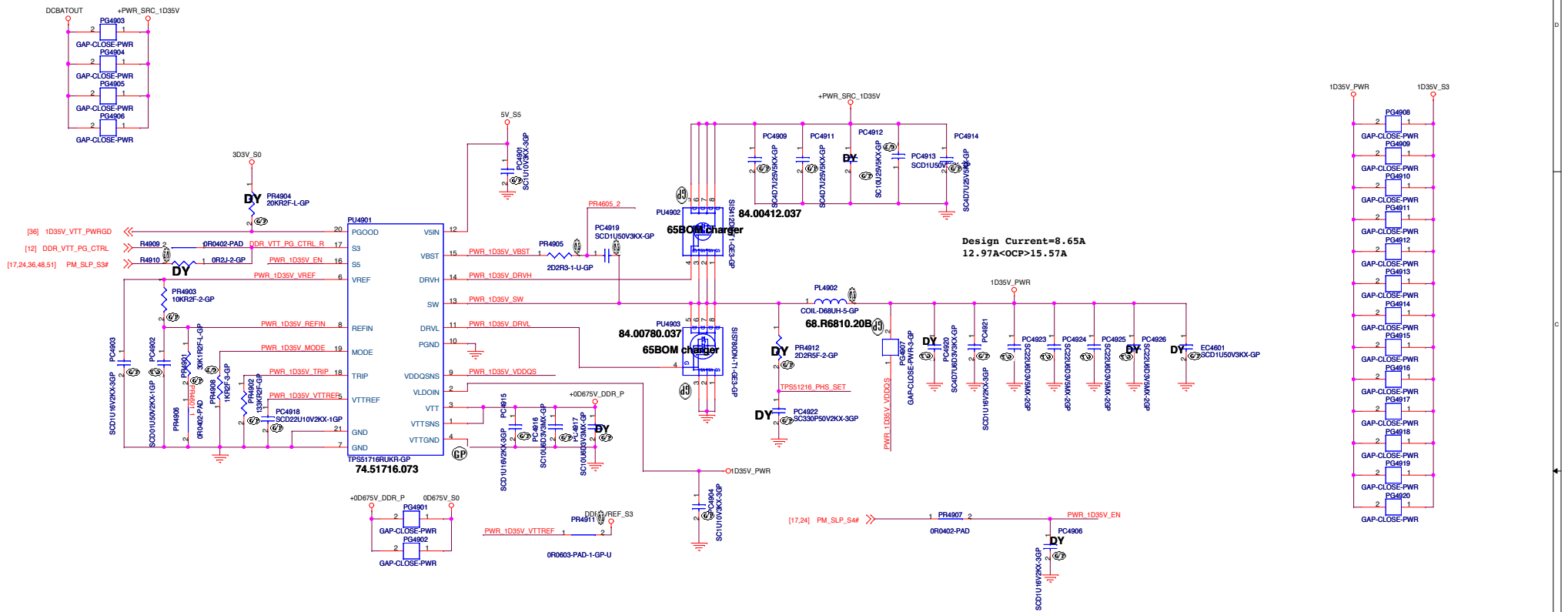
Size: A3 Document Number: **Janus HSX 40/50/70** Rev: **A00**

Date: Friday, February 07, 2014 Sheet 47 of 104

SSID = PWR.Plane.Regulator_1p05v



SSID = PWR.Plane.Regulator Ip35vOp675v



[36] 1D35V_VTT_PWRGD
 [12] DDR_VTT_PG_CTRL
 [17,24,36,48,51] PM_SLP_S3#

Design Current=8.65A
 12.97A<OCP>15.57A


| State | S3 | S5 | VDDR | VTTREF | VTT |
|-------|----|----|------|--------|-----------|
| S0 | Hi | Hi | On | On | On |
| S3 | Lo | Hi | On | On | Off(Hi-Z) |
| S4/S5 | Lo | Lo | Off | Off | Off |

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP IND 0.1UH M PCM063T-R10MN 1.5-1.7mohm Isat =60Arms 68.R1010.10T
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
 MOS: FET MOS FDM33664S NC POWER56 / 84.03664.037 / Q1: 8.5-11mohm @Vgs=4.5V Q2: 2.6-3.2mohm @Vgs=4.5V

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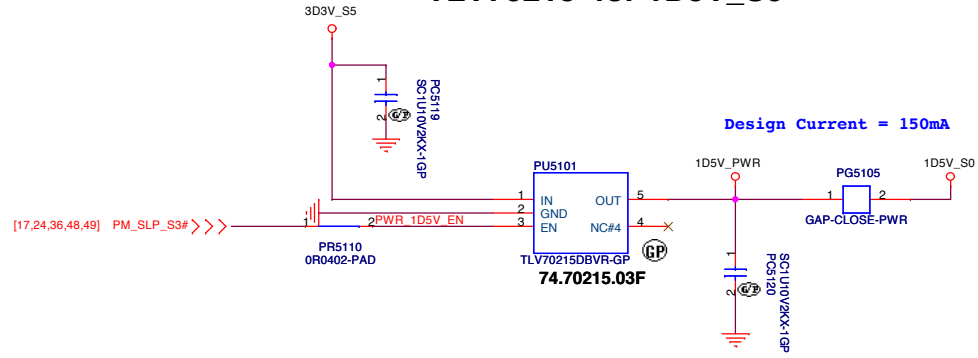
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| | | |
|---|---------------------------|--|
|  | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | | |
| Reserved | | |
| Size | Document Number | Rev |
| A3 | Janus HSW 40/50/70 | A00 |
| Date: Friday, February 07, 2014 | Sheet 50 | of 104 |

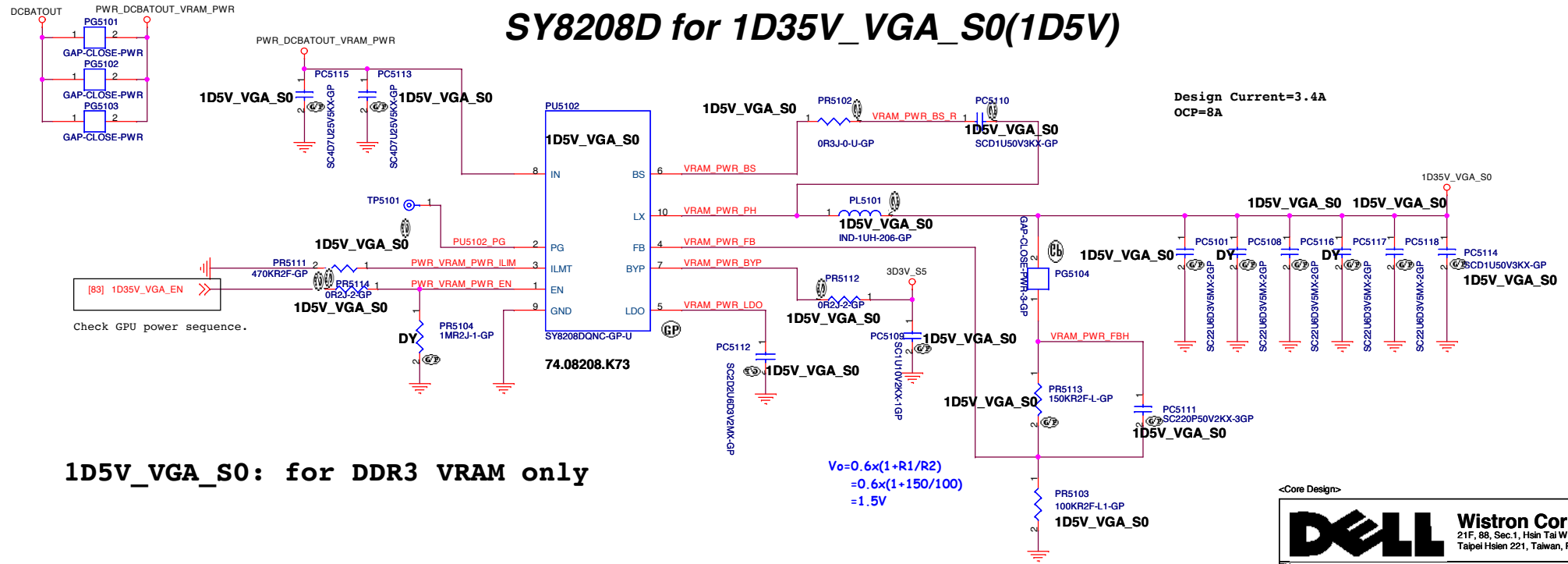
SSID = PWR.Plane.Regulator_1p5v

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<https://t.me/biosarchive>

TLV70215 for 1D5V_S0



SY8208D for 1D35V_VGA_S0(1D5V)



1D5V_VGA_S0: for DDR3 VRAM only

$$V_o = 0.6 \times (1 + R1/R2) = 0.6 \times (1 + 150/100) = 1.5V$$

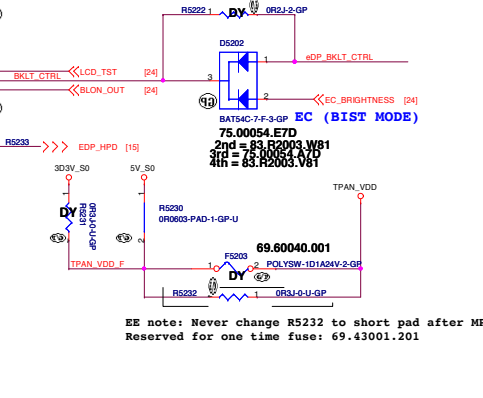
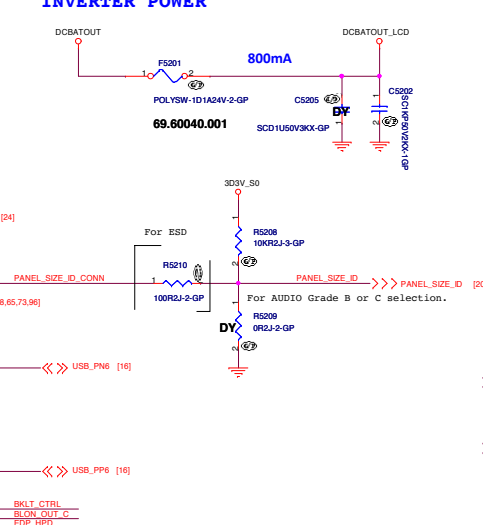
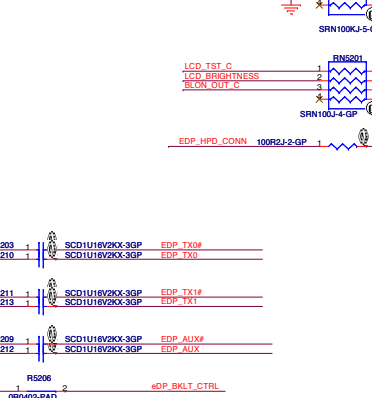
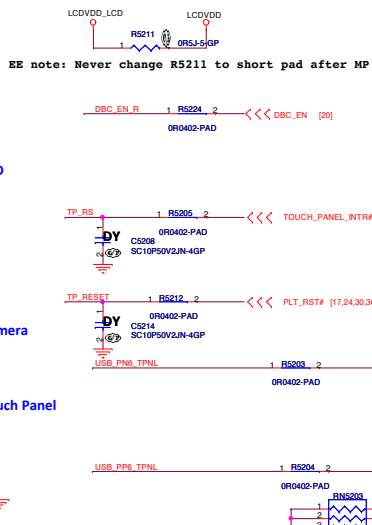
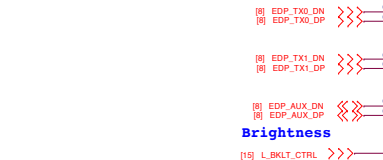
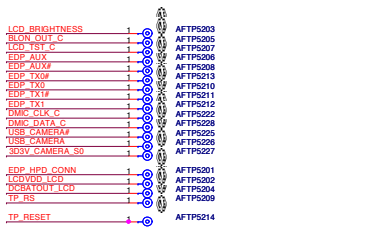
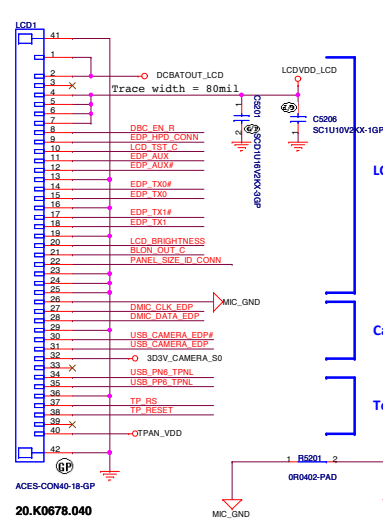
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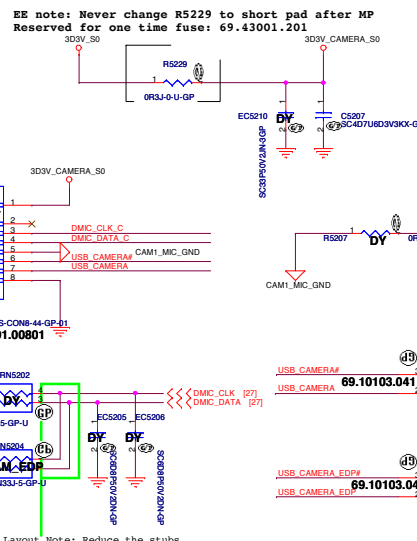
Title: **TLV70215_1D5V / SY8208D_1D5V(VGA)**

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| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
|---------|---|----------------|

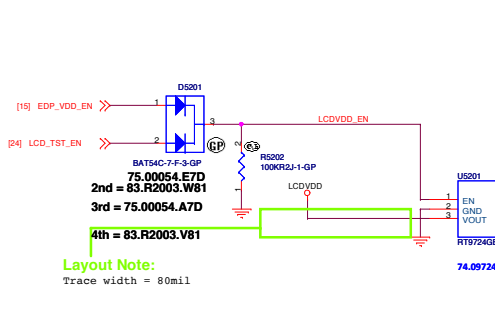
Date: Friday, February 07, 2014 Sheet 51 of 104



CAM1




LCDVDD



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<https://t.me/biosarchive>

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<Core Design>

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| Title (Reserved) | | |
| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | | Sheet 53 of 104 |

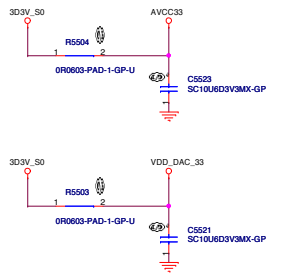
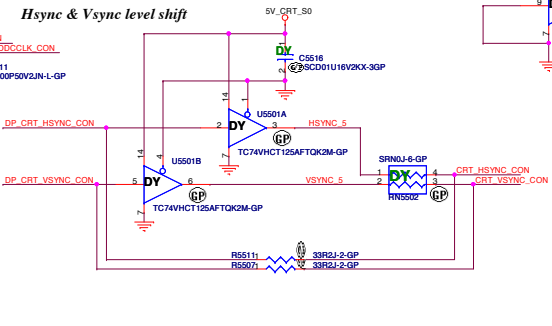
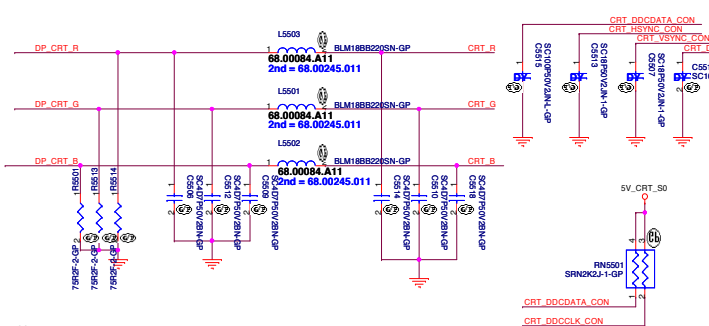
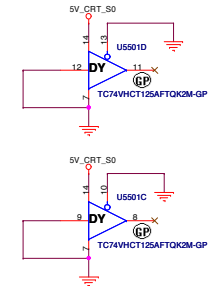
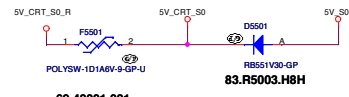
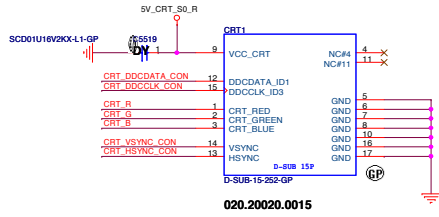
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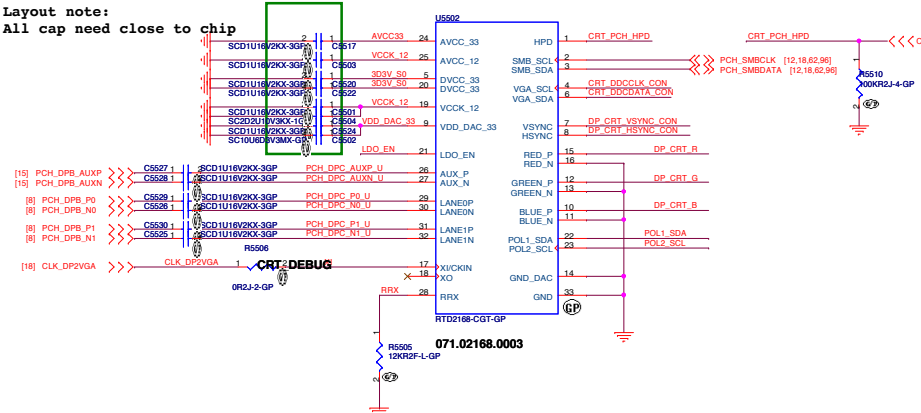


| | | |
|-------------------------------------|---------------------------|-----------------|
| Title | | |
| HDMI Level Shifter/Connector | | |
| Size | Document Number | Rev |
| A3 | Janus HSW 40/50/70 | X02 |
| Date: | Friday, February 07, 2014 | Sheet 54 of 104 |

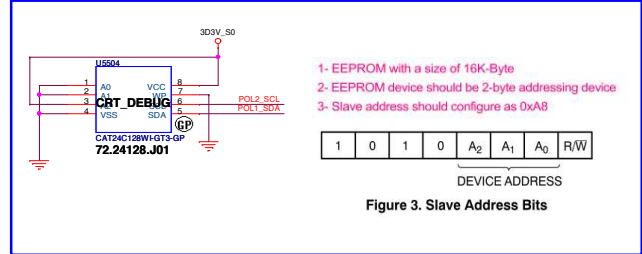
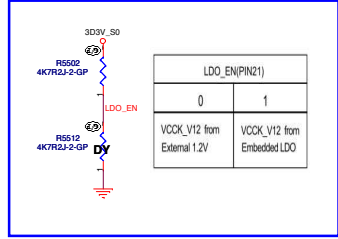
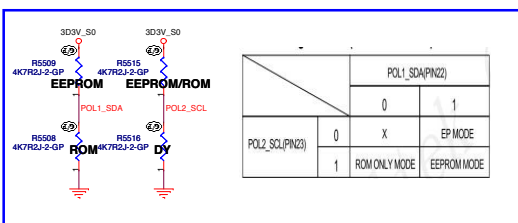
CRT Board Connector



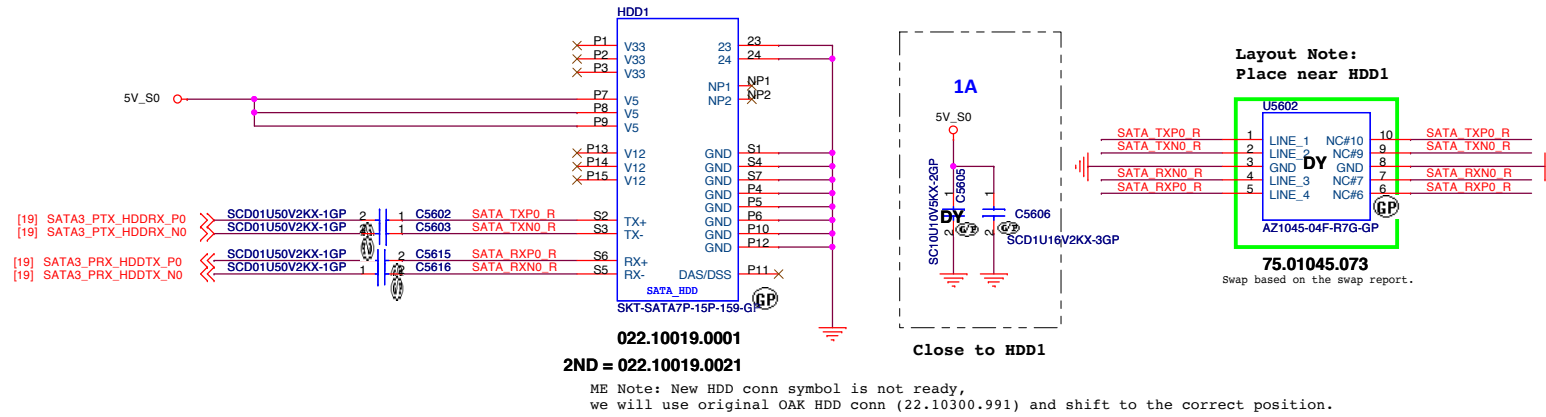
Layout note:
 All cap need close to chip



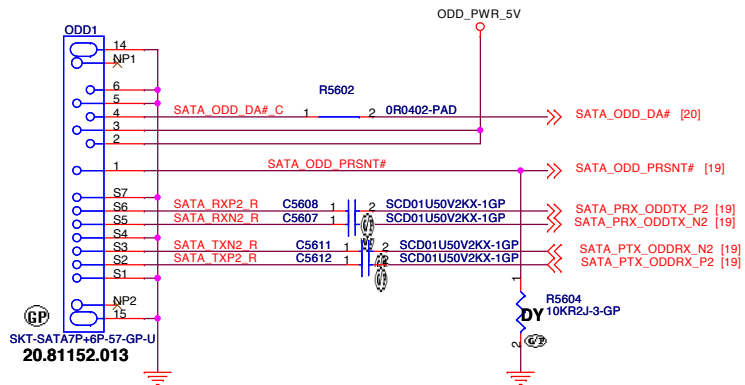
<https://t.me/schematics4laptop>
<https://t.me/biosarchive>



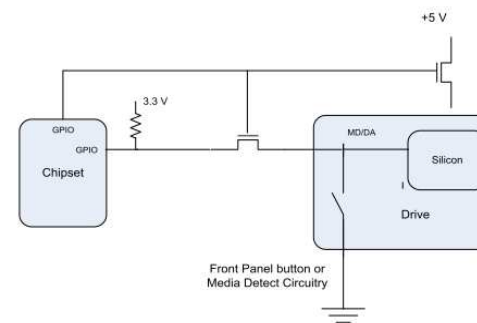
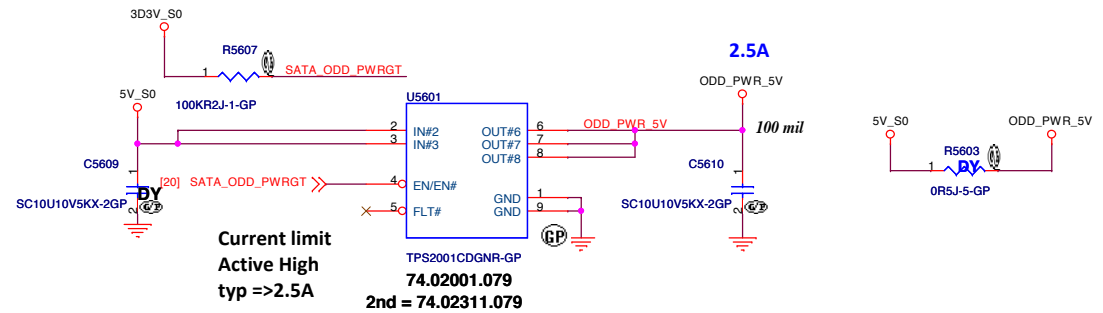
SATA HDD Connector



ODD Connector



SATA Zero Power ODD




<Core Design>



SSID = ESATA

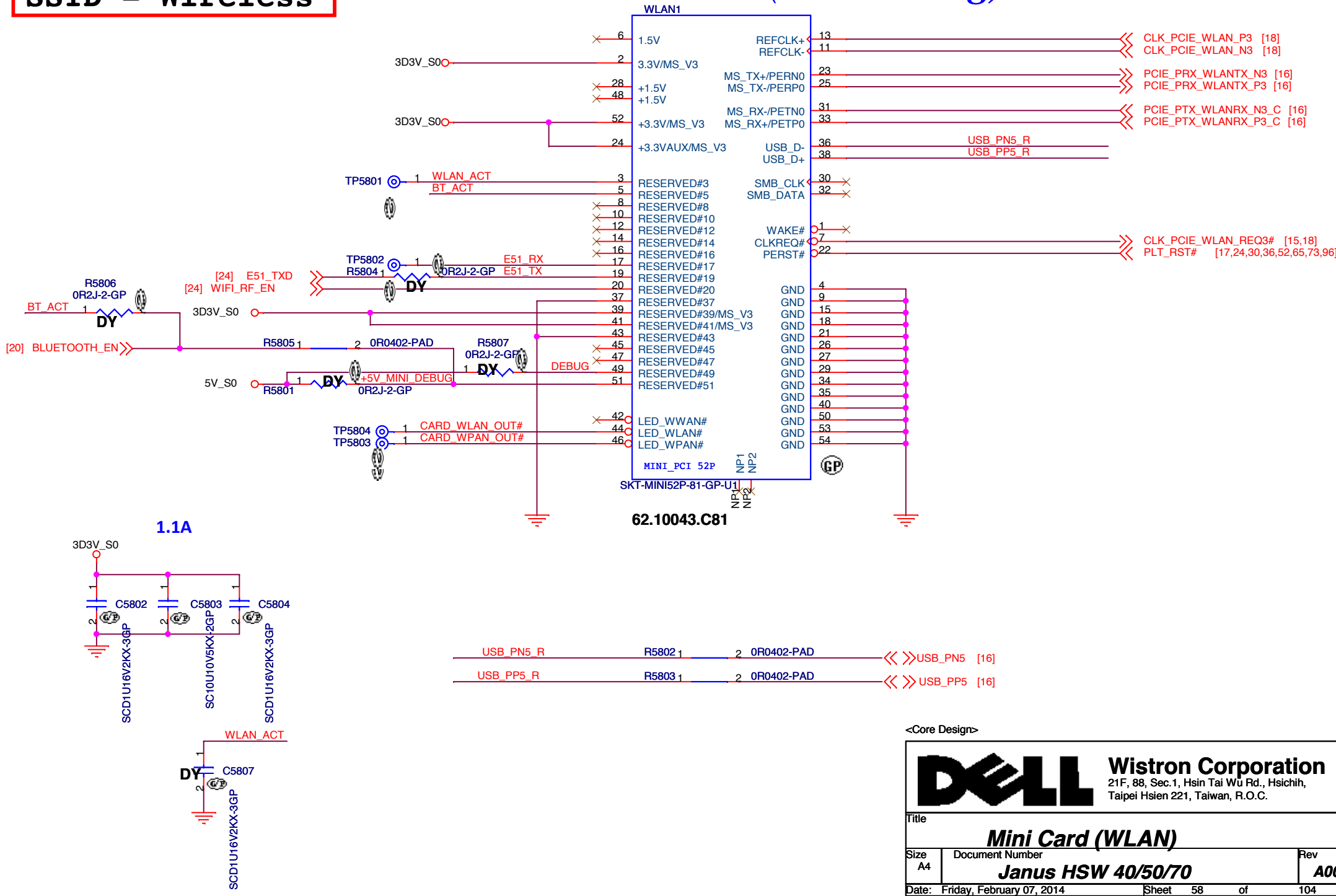
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|  | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | | ESATA |
| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 57 | of 104 |

SSID = Wireless

Mini Card Connector(802.11a/b/g)




<Core Design>

| | | | |
|---------------------------------|--|---|--------|
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| | | Title <h3>Mini Card (WLAN)</h3> | |
| Size A4 | Document Number <h3>Janus HSW 40/50/70</h3> | Rev A00 | |
| Date: Friday, February 07, 2014 | | Sheet 58 | of 104 |


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| Title Reserved | | |
| Size A4 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 59 of | 104 |

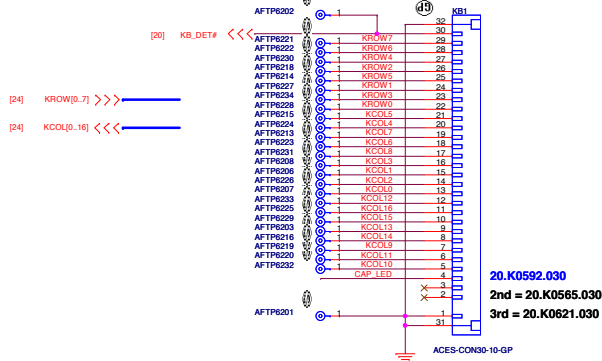
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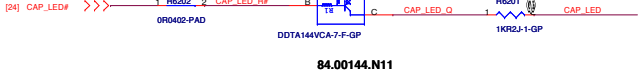
| | | | | | |
|---|--|--|---|-------------------|-----|
|  | | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title | | | (Reserved) | | |
| Size A4 | Document Number Janus HSW 40/50/70 | | | Rev A00 | |
| Date: Friday, February 07, 2014 | | | Sheet 60 | of | 104 |

SSID = KBC

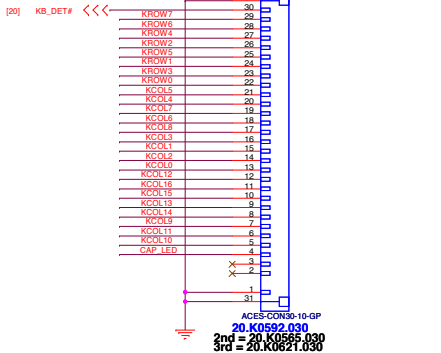
Internal Keyboard Connector (DVC40)



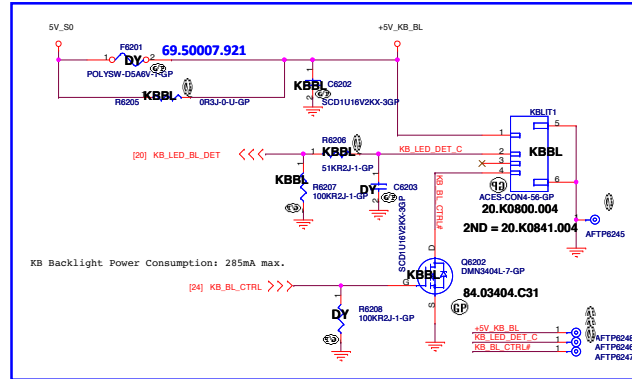
CAP LED Control
LOW activated from KBC GPIO



Internal Keyboard Connector (DVC50/DVC70)

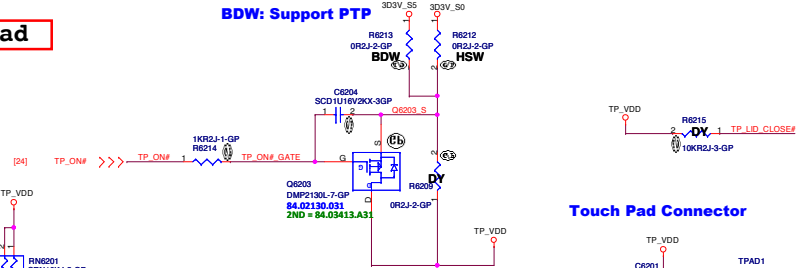


Keyboard Backlight (DVC70)



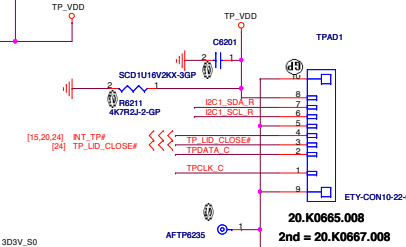
SSID = Touch.Pad

BDW: Support PTP

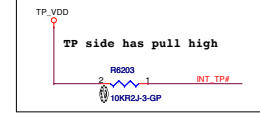


Touch Pad Connector

| Pin number | Pin name |
|------------|-----------|
| 1 | VDD |
| 2 | DAT (I2C) |
| 3 | CLK (I2C) |
| 4 | GND |
| 5 | A*PTN |
| 6 | GPIO |
| 7 | DAT (PS2) |
| 8 | CLK (PS2) |

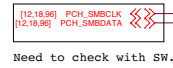


Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



PS2
I2C

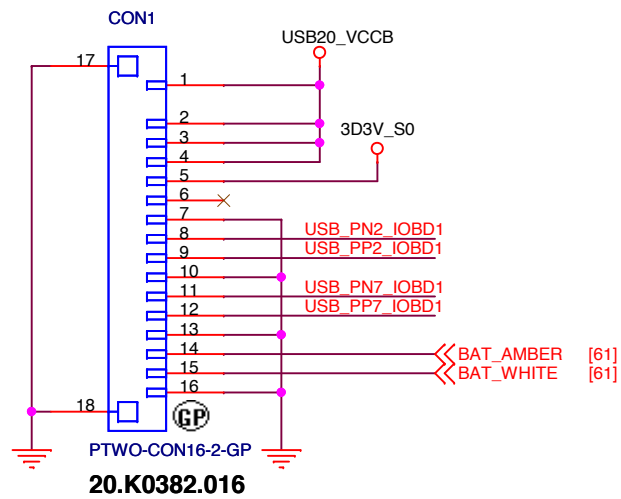
SMBUS



84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00001.07C
4th = 84.DMN66.03F

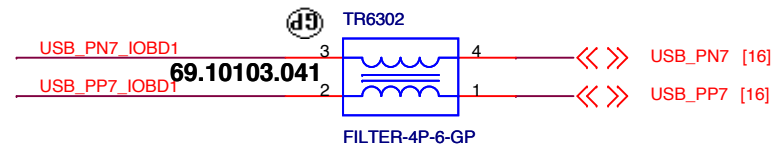
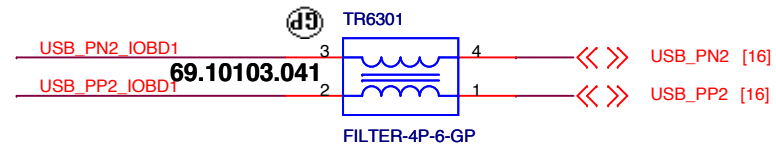
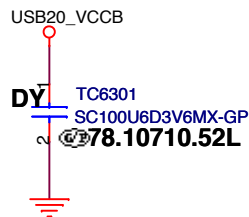
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**USB2.0 Port3
Card Reader
LED**

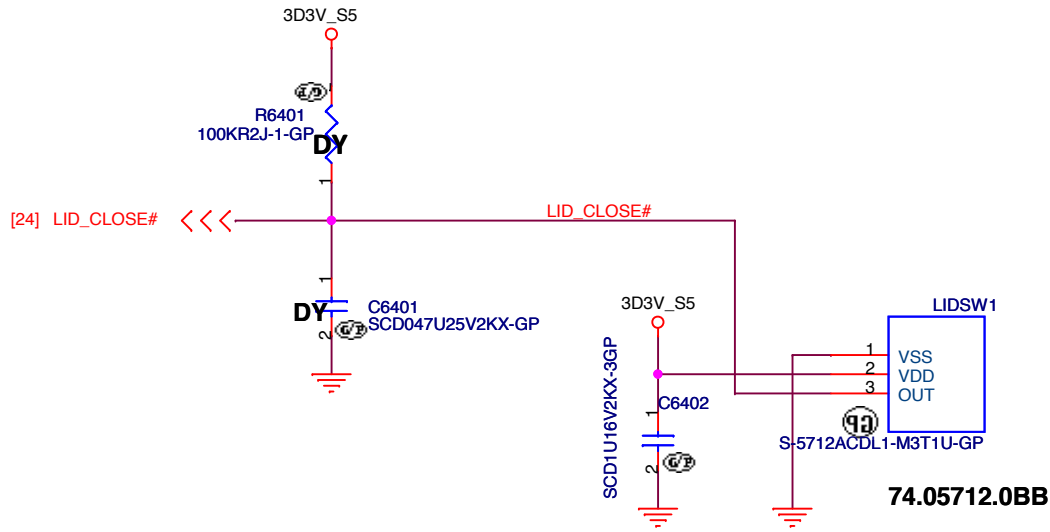
The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA



<Core Design>

| | | | |
|---------------------------|---------------------------|--|-----------|
| DELL | | Wistron Corporation | |
| | | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| IO Board Connector | | | |
| Size | Document Number | Rev | |
| A4 | Janus HSW 40/50/70 | A00 | |
| Date: | Friday, February 07, 2014 | Sheet | 63 of 104 |

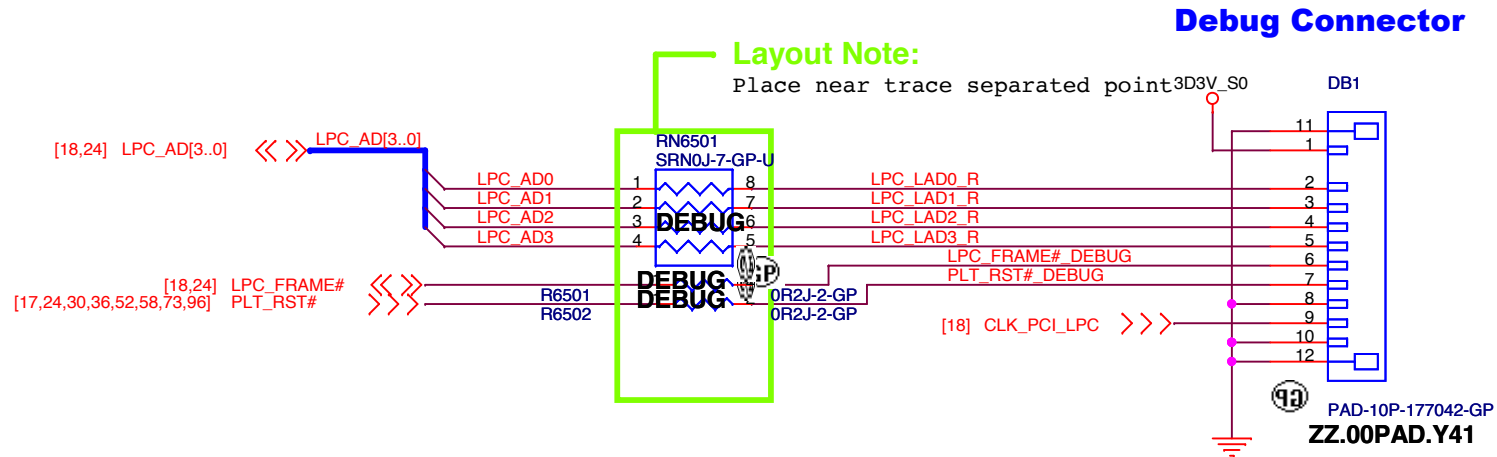
SSID = User.Interface



<Core Design>

| | | | |
|---------------------------------|--|---|-----|
| DELL | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title Hall Sensor | | | |
| Size A4 | Document Number Janus HSW 40/50/70 | Rev A00 | |
| Date: Friday, February 07, 2014 | Sheet 64 | of | 104 |


SSID = DEBUG PORT



Layout Note:
Place near trace separated point 3D3V_S0

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

| | | | |
|---|---|---|--|
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| | | Title <p style="text-align: center;">Dubug connector</p> | |
| Size A4 | Document Number <p style="text-align: center;">Janus HSW 40/50/70</p> | Rev <p style="text-align: center;">A00</p> | |
| Date: Friday, February 07, 2014 | | Sheet 65 of 104 | |

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<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Janus HSW 40/50/70


Rev
A00

Date: Friday, February 07, 2014

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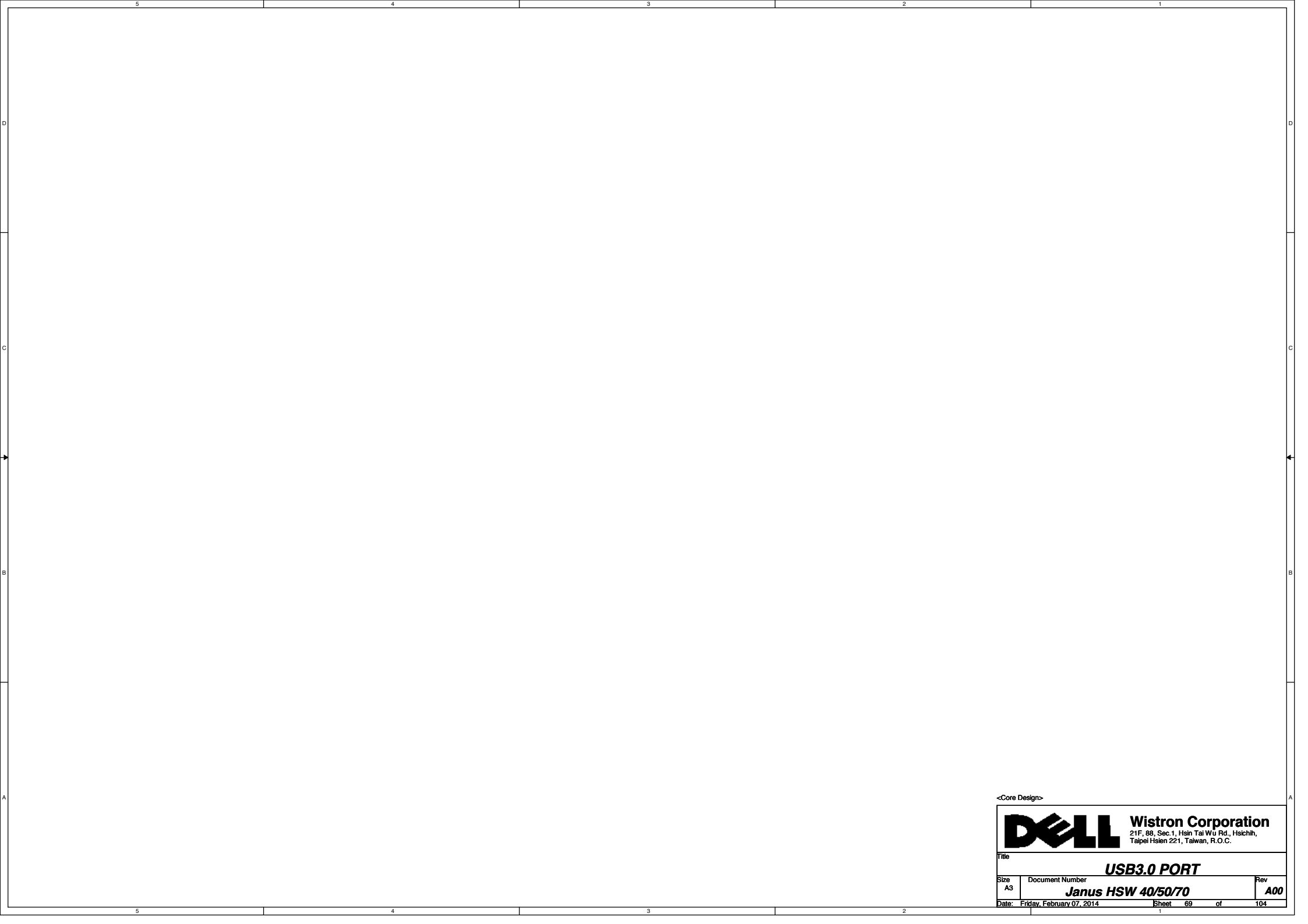
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|---|--|--|
|  | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | | |
| Reserved | | |
| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 67 | of 104 |

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<Core Design>

| | | |
|---|--|---|
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title RESERVED | | |
| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 68 | of 104 |




<Core Design>

| | | |
|---|---------------------------|--|
|  | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | | |
| USB3.0 PORT | | |
| Size | Document Number | Rev |
| A3 | Janus HSW 40/50/70 | A00 |
| Date: Friday, February 07, 2014 | Sheet 69 | of 104 |


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|---|--|--|
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| Title | | |
| Reserved | | |
| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 70 | of 104 |


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<Core Design>

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|---|---------------------------|--|
|  | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | | |
| Reserved | | |
| Size | Document Number | Rev |
| A3 | Janus HSW 40/50/70 | A00 |
| Date: Friday, February 07, 2014 | Sheet 71 of | 104 |

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<Core Design>

| | | |
|---|--|--|
|  | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title | | |
| Reserved | | |
| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 72 | of 104 |

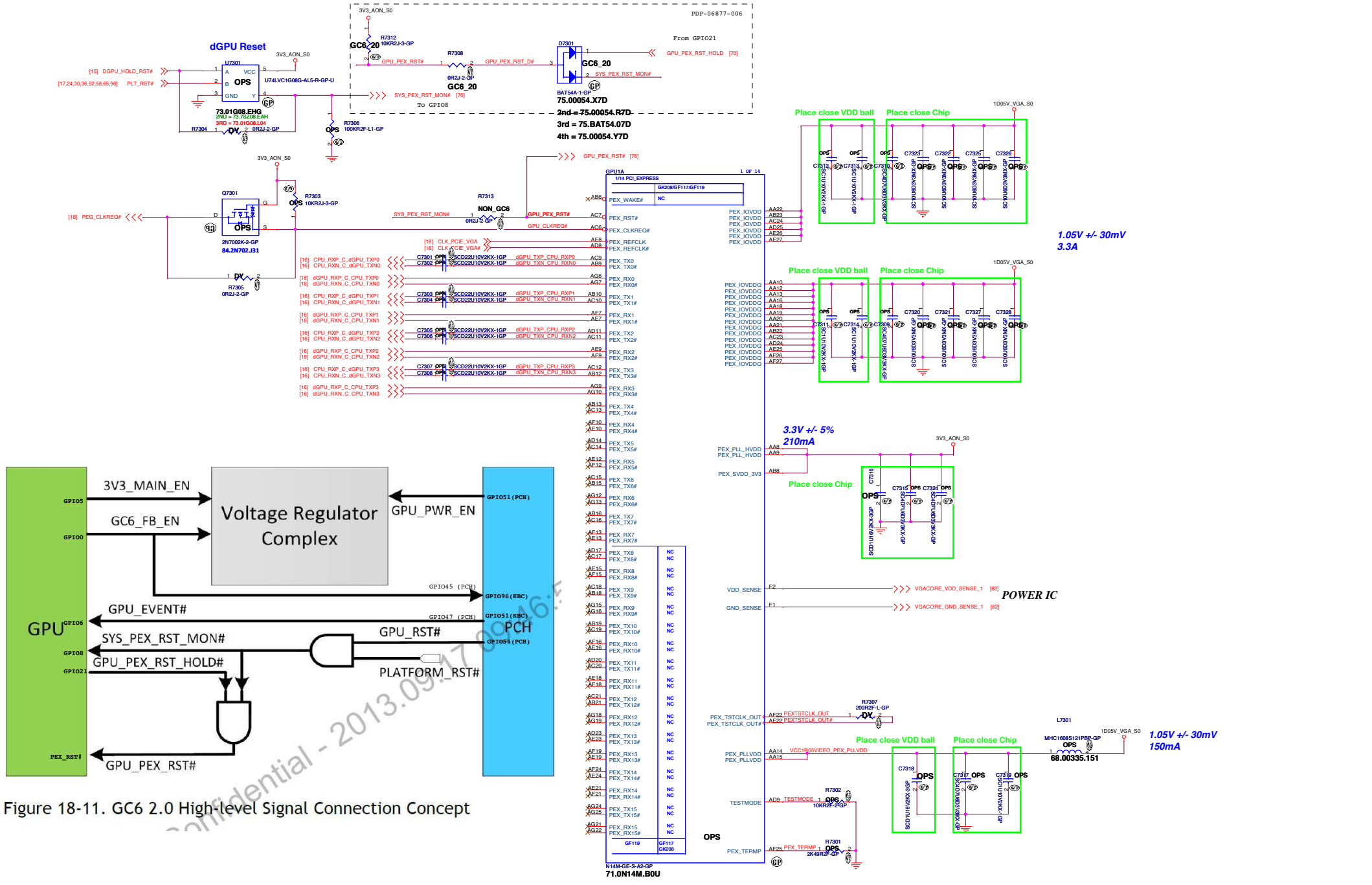
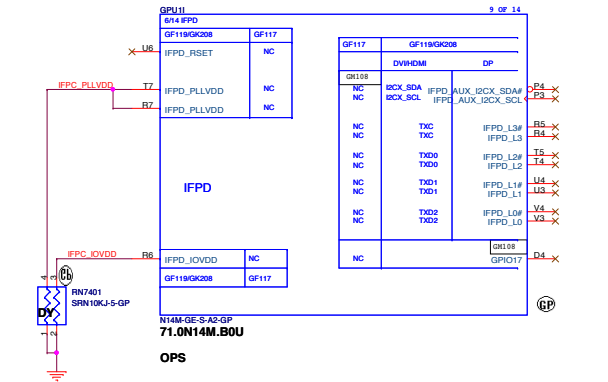
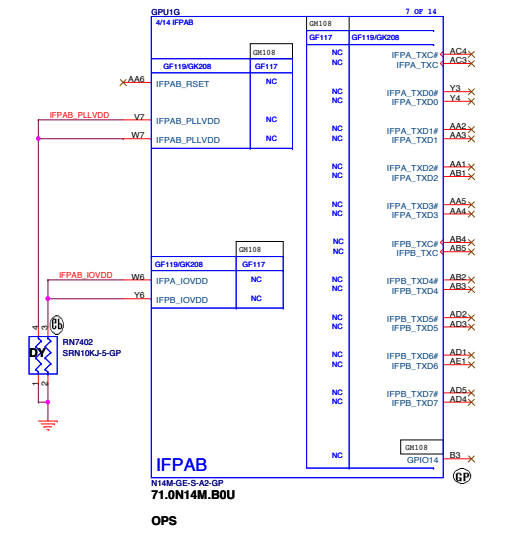


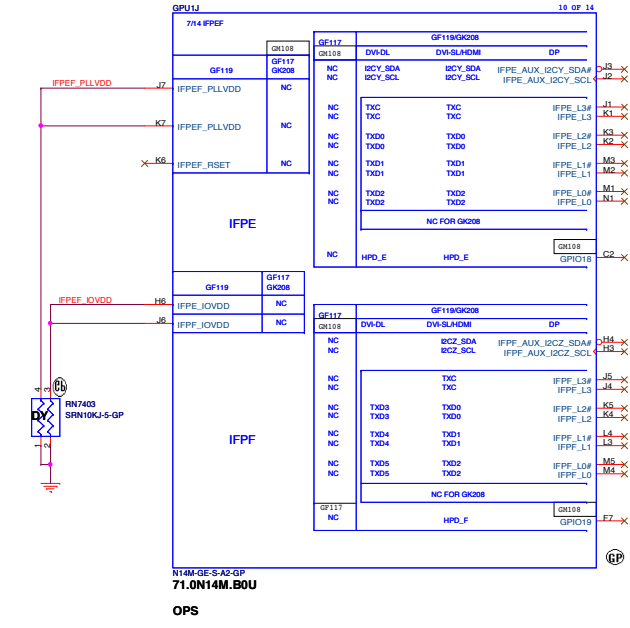
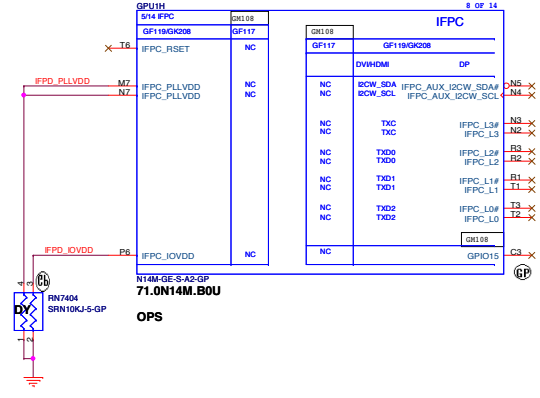
Figure 18-11. GC6 2.0 High-level Signal Connection Concept

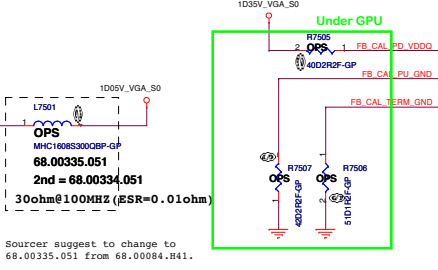
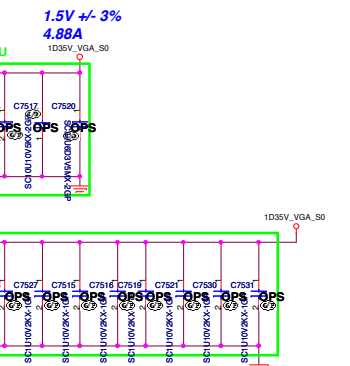
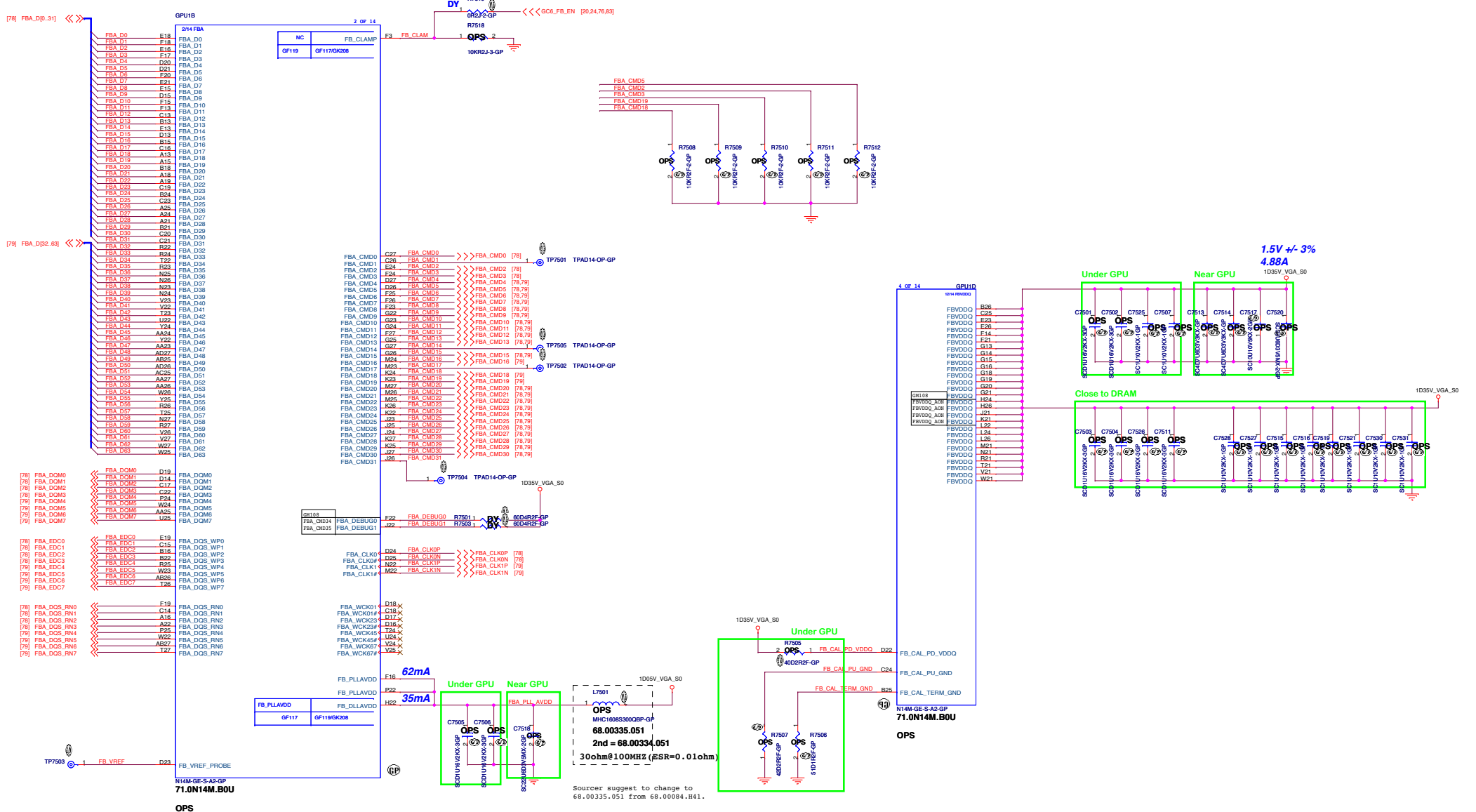
N15V-GM-S-A2: 071.0N15V.0A0U
 N15V-GM-S is GF117.
 N15S-GT is GM108.

LVDS Interface



HDMI Interface





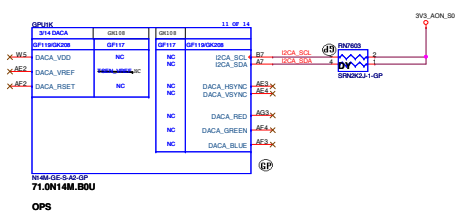
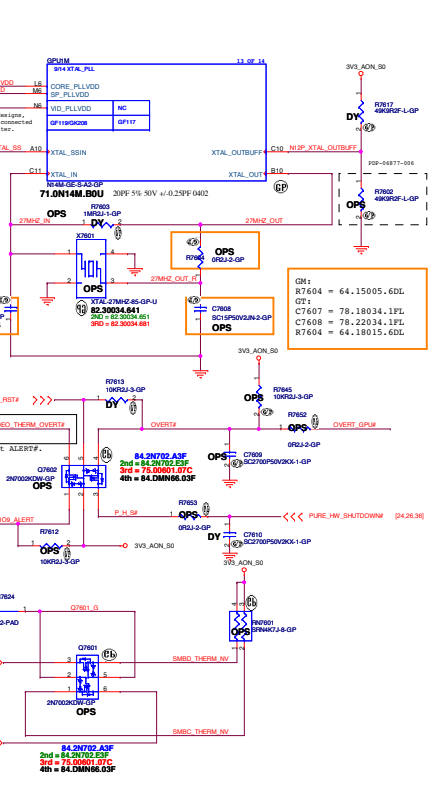
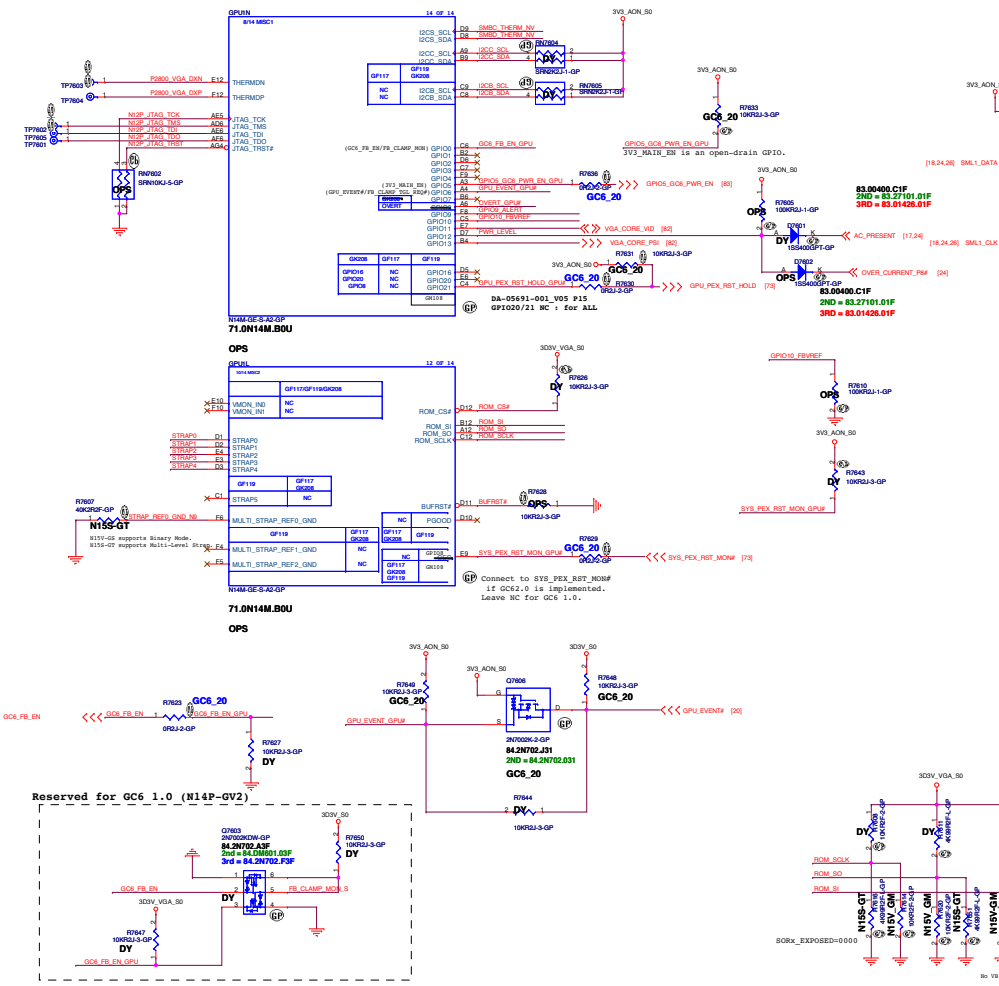


Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

| GPU Package | PLL Rail | Capacitor Type | Footprint | Population | Location | |
|----------------------|----------|------------------|-----------|------------|----------|-----------|
| GB2B-64 and GB4B-128 | PLLVDD | 0.1 µF | X7R | 0402 | 1 | Under GPU |
| | | 22 µF | X5R | 0805 | 1 | Near GPU |
| | | Bead Type | | | | |
| | | 30 Ω (ESR=0.05) | 0402 | 1 | | Hear GPU |

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Combined

| GPU Package | PLL Rails | Capacitor Type | Footprint | Population | Location | |
|--------------------------------|------------------------|------------------|-----------|------------|----------|-----------|
| GB2B-64 GB4B-128 GB3-256 | SP_PLLVDD + VID_PLLVDD | 0.1 µF | X7R | 0402 | 1 | Under GPU |
| | | 4.7 µF | X5R | 0603 | 1 | Near GPU |
| | | 22 µF | X5R | 0805 | 1 | Near GPU |
| | | Bead Type | | | | |
| | | 180 Ω (ESR=0.2) | 0603 | 1 | | Hear GPU |



(RVL-06891-001)N15V-GT-S DDR3L Recommended Memories

| | Strap | | | | |
|---------------|---------|-----|----------------------|---|---|
| 128Mx16 DDR3L | Hynix | 0x9 | H5TC2G63FPR-11C | 1 | 0 |
| | Micron | 0xA | MT41K128M16JT-107G:K | 0 | 1 |
| | Samsung | 0xB | K4W2G1646E-BY11 | 0 | 1 |
| 256Mx16 DDR3L | Hynix | 0x3 | H5TC4G63AFR-11C | 1 | 0 |
| | Micron | 0x4 | MT41K256M16HA-107G:E | 1 | 0 |
| | Samsung | 0x5 | K4W4G1646D-BC1A | 1 | 0 |

Table 15-2. Resistance Mapping to Hex Values

| Resistor Values | Pull-Up to 3V3_MAIN | Pull-Down to GND |
|-----------------|---------------------|------------------|
| 4.99 kΩ | 1000 | 0000 |
| 10.0 kΩ | 1001 | 0001 |
| 15.0 kΩ | 1010 | 0010 |
| 20.0 kΩ | 1011 | 0011 |
| 24.9 kΩ | 1100 | 0100 |
| 30.1 kΩ | 1101 | 0101 |
| 34.8 kΩ | 1110 | 0110 |
| 45.3 kΩ | 1111 | 0111 |

Straps

(DS-06814-001)

Table 9. N15V-GM Binary Strap Mode Mapping

| Strap Pin Name | Strap Mapping | Resistance | Polarity |
|----------------|----------------|------------|--|
| ROM_SCLK | SMB_ALT_ADDR | 10kΩ | Pull-down to GND |
| ROM_SI | SUB_VEHODOR | 10kΩ | +Pull-up to 3V3 if VBIOS ROM exists +Pull-down to GND if no VBIOS ROM |
| ROM_SO | VGA_DEVICE | 10kΩ | Pull-down to GND (no display) |
| STRAP0 | RAM_CFG[0] | 10kΩ | See note below |
| STRAP1 | RAM_CFG[1] | 10kΩ | See note below |
| STRAP2 | RAM_CFG[2] | 10kΩ | See note below |
| STRAP3 | RAM_CFG[3] | 10kΩ | See note below |
| STRAP4 | PCIE_MAX_SPEED | 10kΩ | Pull-down to GND |

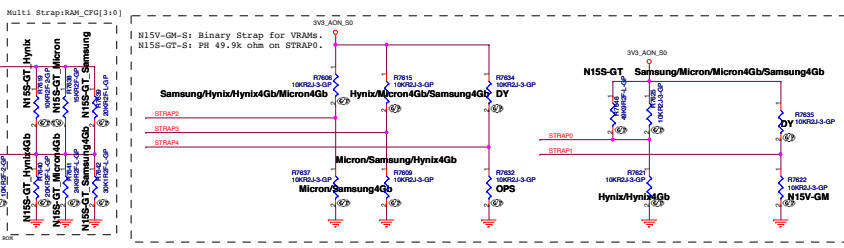
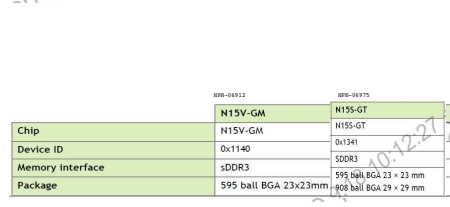
(RVL-06891-001)N15V-GM-S DDR3L Recommended Memories

| | Strap | | STRAP3 | STRAP2 | STRAP1 | STRAP0 |
|---------------|---------|-----|----------------------|--------|--------|--------|
| 128Mx16 DDR3L | Hynix | 0xC | H5TC2G63FPR-11C | 1 | 1 | 0 |
| | Micron | 0x1 | MT41K128M16JT-107G:K | 0 | 0 | 1 |
| | Samsung | 0x5 | K4W2G1646E-BY11 | 0 | 1 | 0 |
| 256Mx16 DDR3L | Hynix | 0x4 | H5TC4G63AFR-11C | 0 | 1 | 0 |
| | Micron | 0xD | MT41K256M16HA-107G:E | 1 | 1 | 0 |
| | Samsung | 0x9 | K4W4G1646D-BC1A | 1 | 0 | 1 |

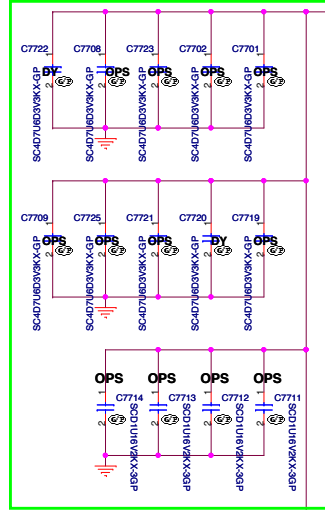
(DS-06814-001)

Table 10. Multi-Level Strap Differences

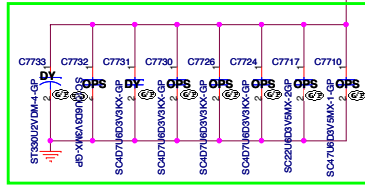
| Physical Strapping Pin | GPU | Logical Strapping Bit 3 | Logical Strapping Bit 2 | Logical Strapping Bit 1 | Logical Strapping Bit 0 |
|------------------------|-----------------------------------|--|--|--|--|
| ROM_SCLK | H155-GV | PCI_DEVID[4] | SUB_VEHODOR | PCI_DEVID[5] | PEX_PLL_EN_TERM |
| ROM_SI | All GB2-64 H144 GB2B-64 H15 | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| ROM_SO | H155-GV | FB[1] | FB[0] | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | H155-GM/-GT | USER[2] | USER[2] | USER[1] | USER[0] |
| STRAP1 | H155-GM/-GT | Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up) | Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up) | 3GIO_PADCFCG[1] | 3GIO_PADCFCG[0] |
| STRAP2 | H155-GM/-GT | Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default) | Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default) | Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default) | Reserved (Keep pull-up and pull-down footprints and leave them not stuffed by default) |
| STRAP3 | H155-GV | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| STRAP4 | H155-GM/-GT | RESERVED | PCIE_SPEED_CHA | PCIE_MAX_SPEED | PULL_VDD033V |



Under GPU

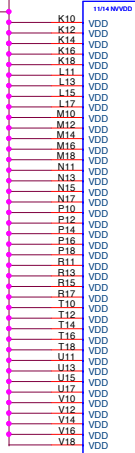


Near GPU



VGA_CORE

GPU1E 5 OF 14

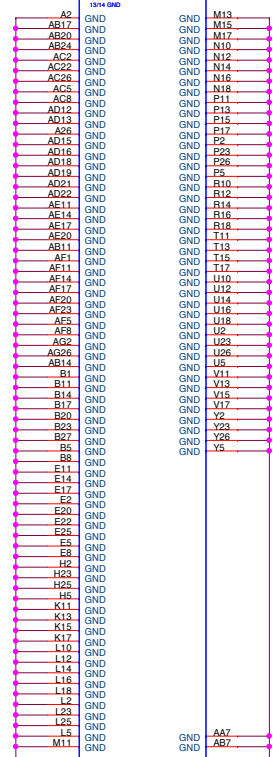


N14M-GE-S-A2-GP

71.0N14M.B0U

OPS

GPU1F 6 OF 14



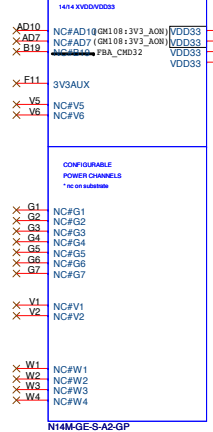
N14M-GE-S-A2-GP

71.0N14M.B0U

OPS

G10,G12:
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC62.0 is NOT implemented, connect to the same rail as VDD33.

GPU1C 3 OF 14



N14M-GE-S-A2-GP

71.0N14M.B0U

OPS

3V3_AON_S0

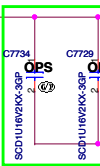
G10

G12

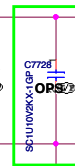
G8

G9

Under GPU



Near GPU



3.3V +/- 5%
85mA

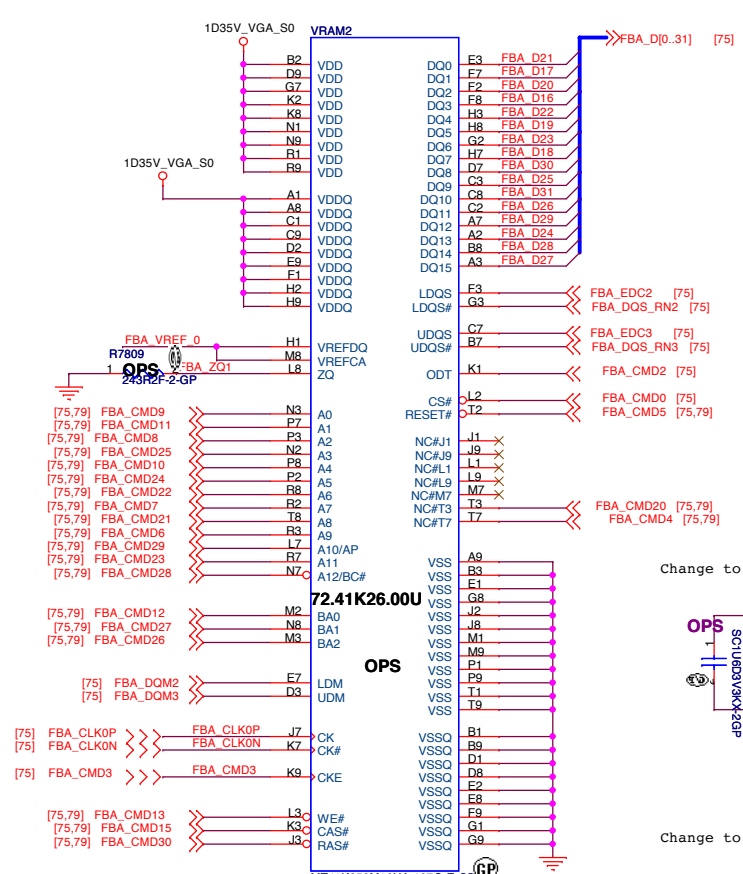
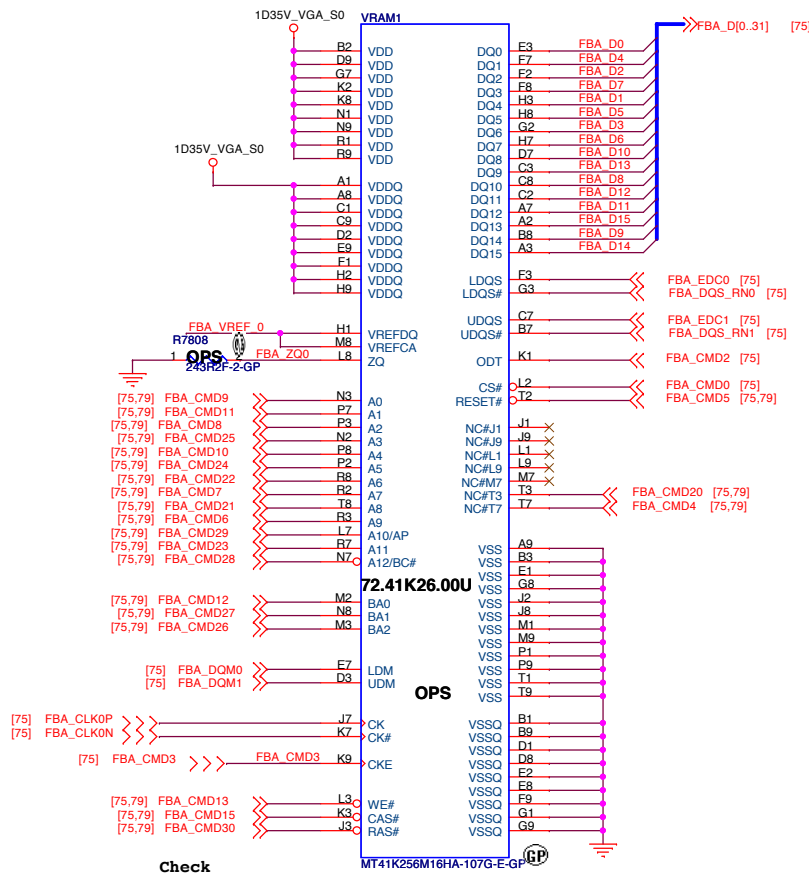
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DELL Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

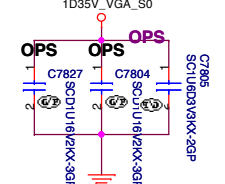
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Size: Document Number
Custom: **Janus HSW 40/50/70** Rev: **A00**

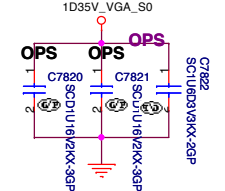
Date: Friday, February 07, 2014 Sheet: 77 of 104



Place close VRAM1 VDD ball

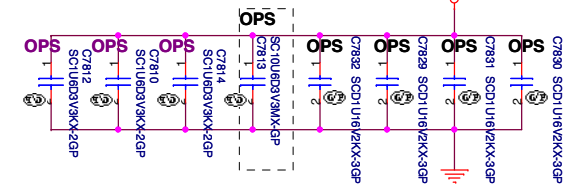


Place close VRAM2 VDD ball



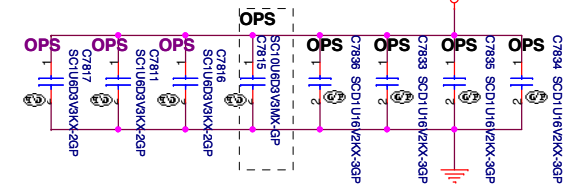
Place close VRAM1VDDQ ball

Change to 10U 0603 for height limit issue.

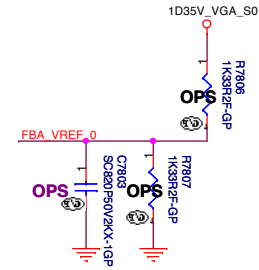


Place close VRAM1VDDQ ball

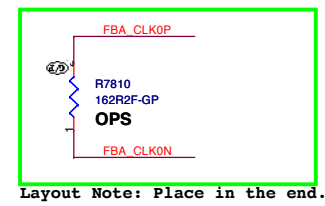
Change to 10U 0603 for height limit issue.



Frame Buffer Partition A-Lower Half



FBCLK Termination place on VRAM side



Layout Note: Place in the end.

FBVREF Termination

| Type | FBVREF% | Voltage | GPU_GPIO10 |
|----------------|---------|---------|------------|
| Un-termination | 50% | 0.749V | High |
| Termination | 70% | 1.0617V | Low |

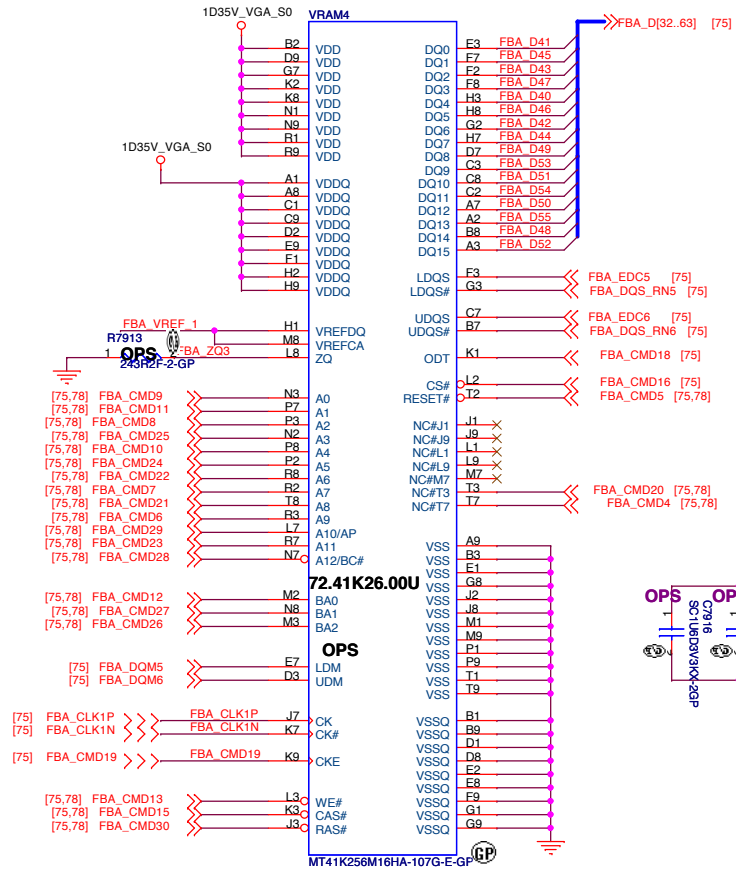
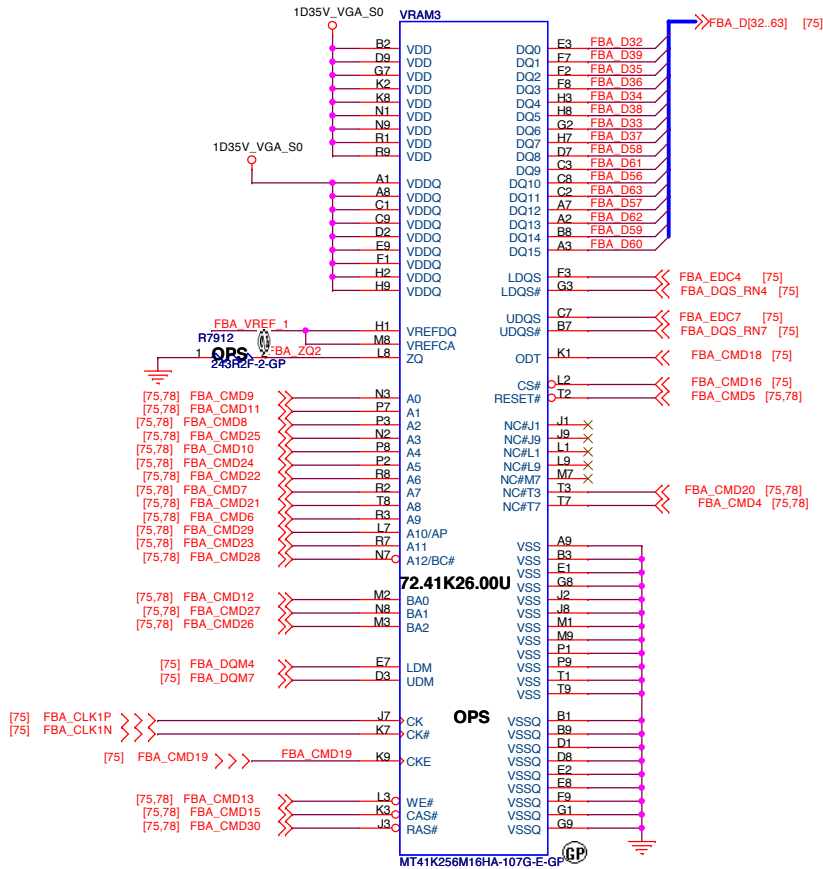
20110613

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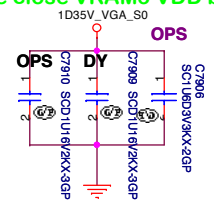
Wistron Corporation
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Title: **GPU-VRAM1,2 (1/4)**

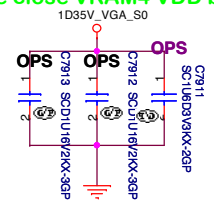
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| Size A3 | Document Number | Rev |
| | Janus HSW 40/50/70 | A00 |
| Date: Friday, February 07, 2014 | Sheet 78 | of 104 |



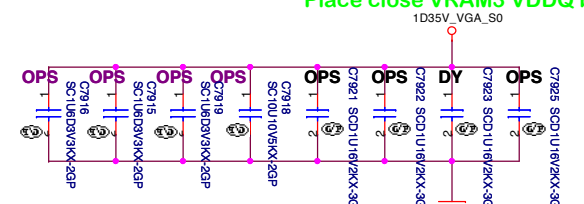
Place close VRAM3 VDD ball



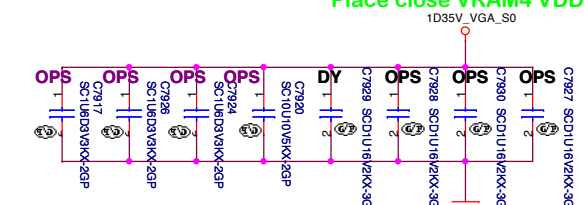
Place close VRAM4 VDD ball



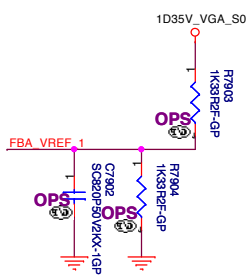
Place close VRAM3 VDDQ ball



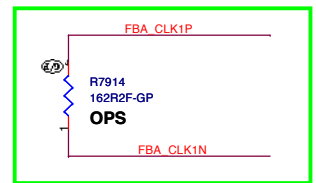
Place close VRAM4 VDDQ ball



Frame Buffer Partition A-Lower Half



FBCLK Termination place on VRAM side



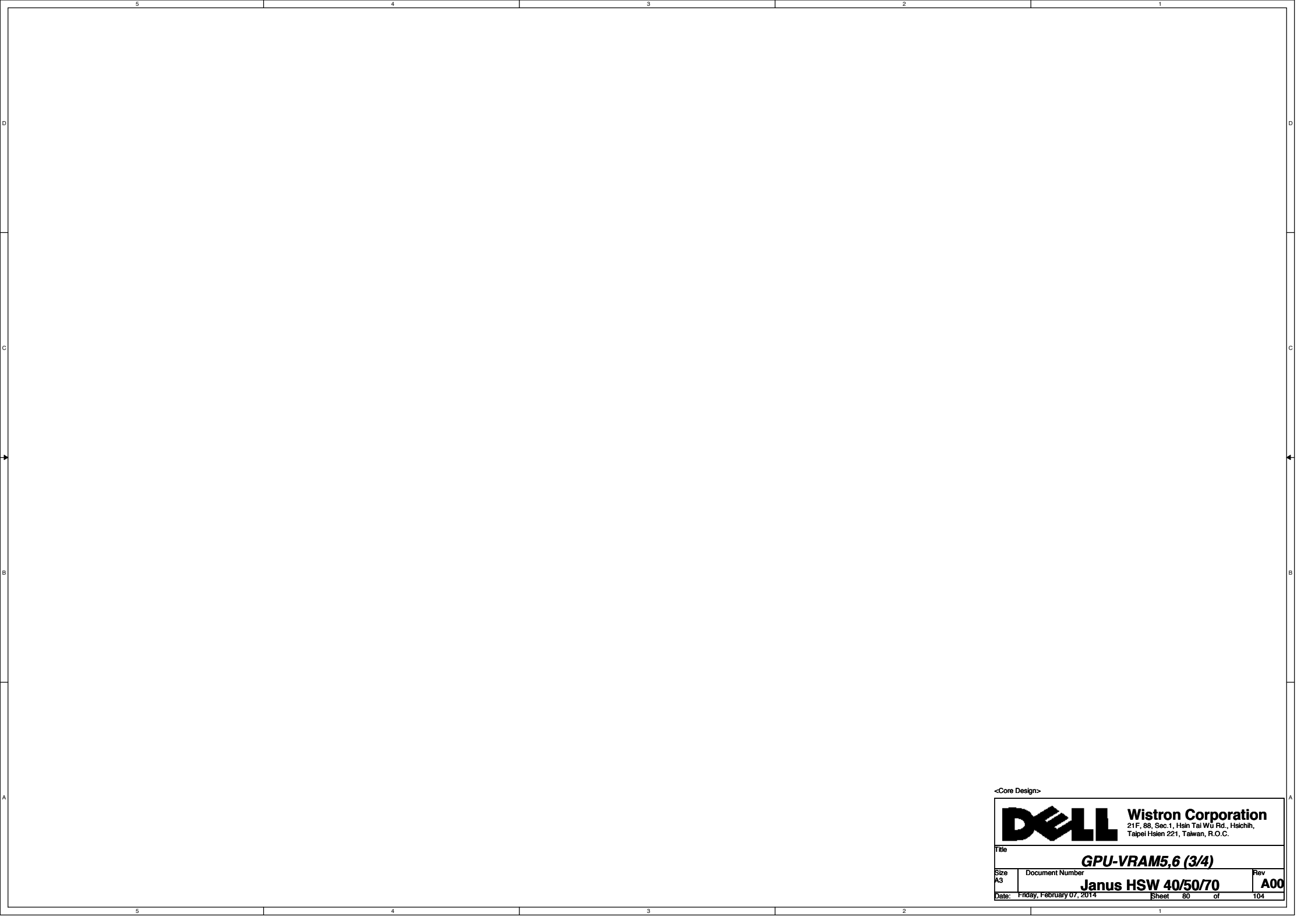
Layout Note: Place in the end.

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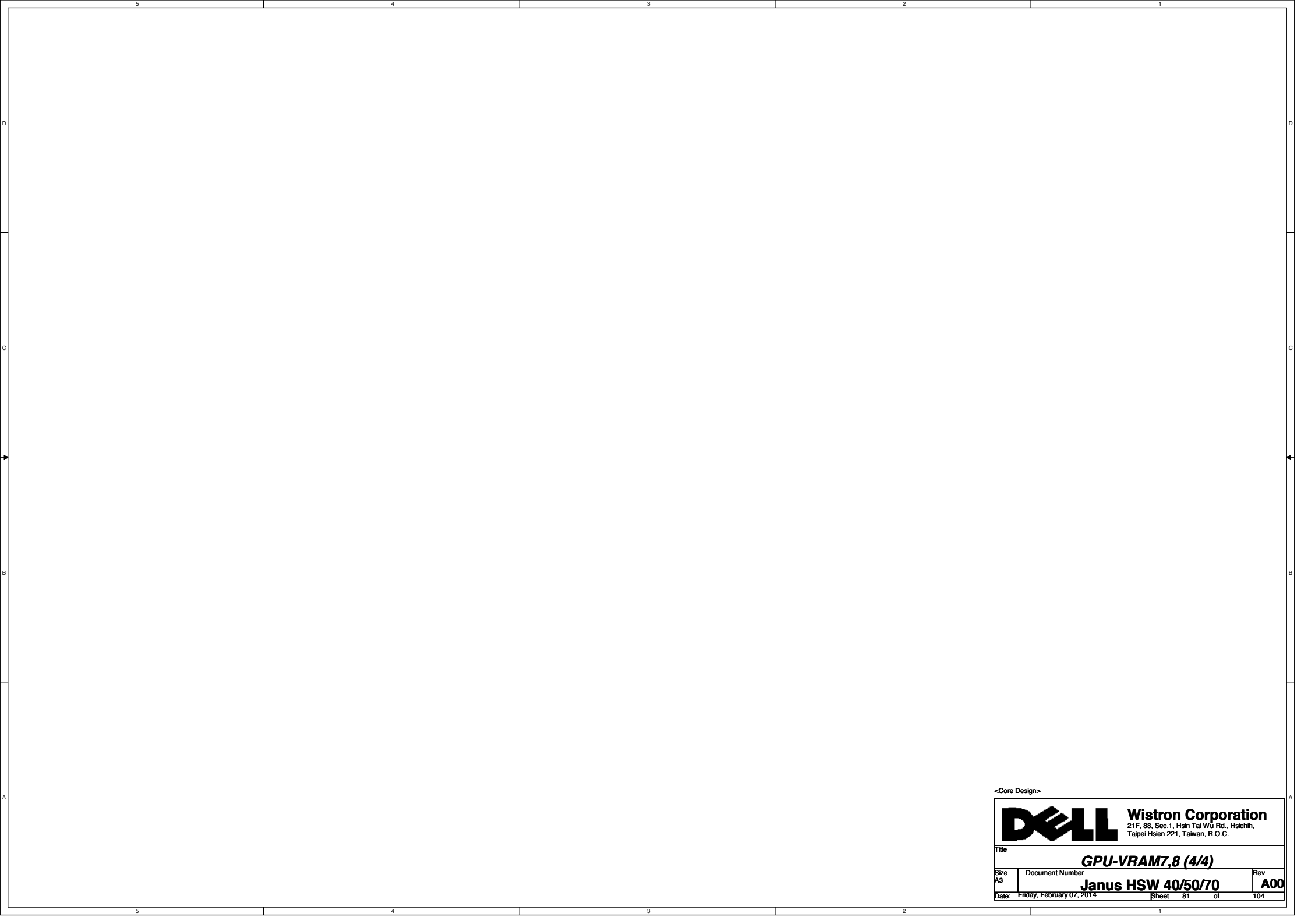
Title: **GPU-VRAM3,4 (2/4)**

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| Size A3 | Document Number | Rev |
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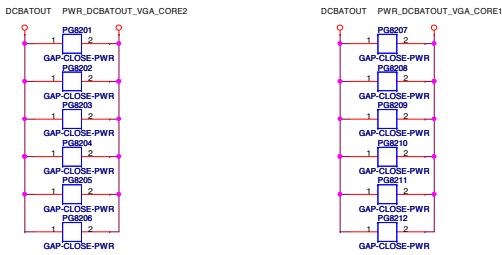
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|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
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| GPU-VRAM5,6 (3/4) | | | |
| Size | Document Number | Rev | |
| A3 | Janus HSW 40/50/70 | A00 | |
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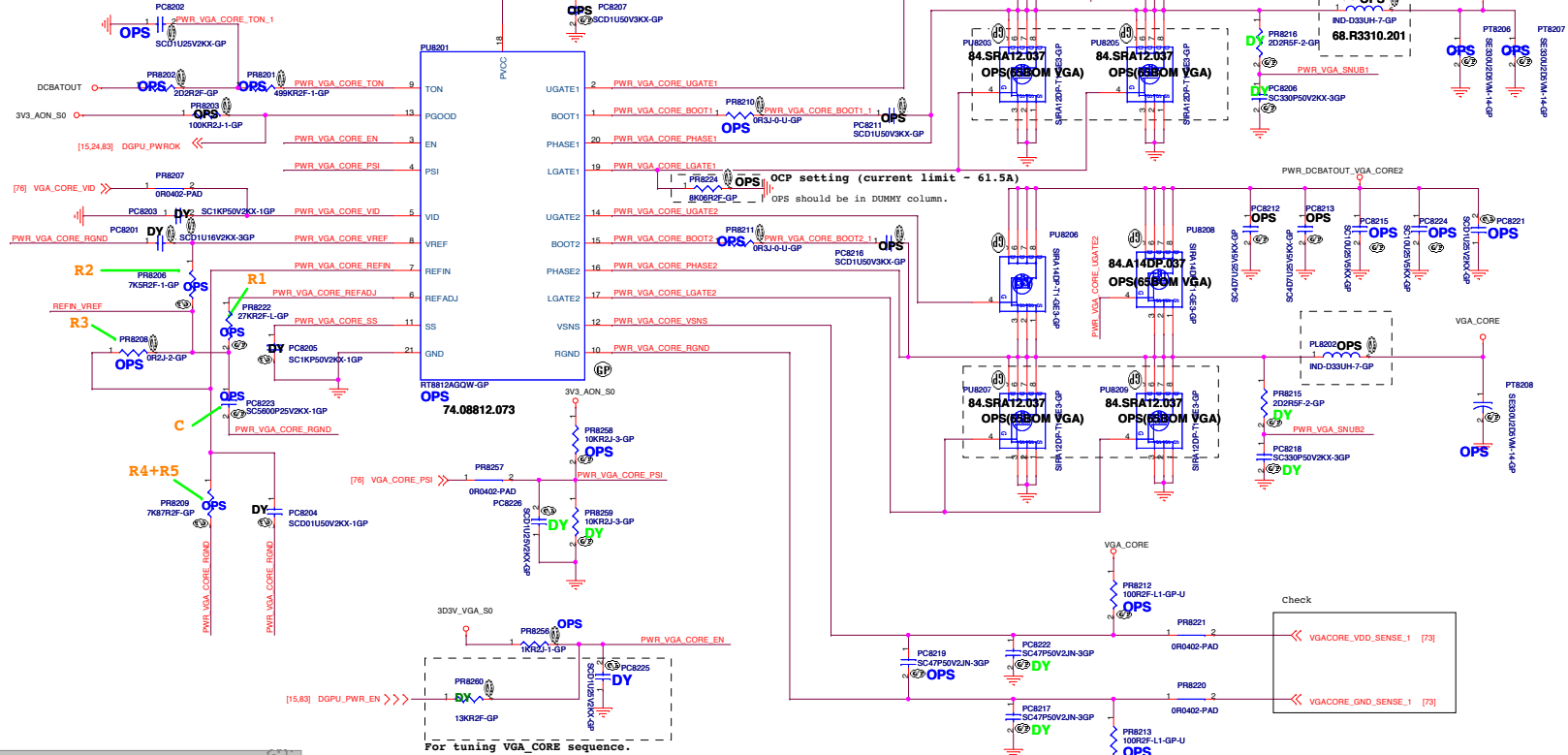


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| Title | | | |
| GPU-VRAM7,8 (4/4) | | | |
| Size | Document Number | | Rev |
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| Date: | Friday, February 07, 2014 | Sheet | 81 of 104 |



PUR203, PUR205, PUR207 and PUR209 manually change to 84.SRA12.037



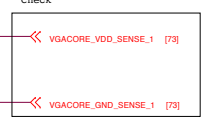
N15V_GM_S Config D
 Design Current=33.5A
 56.65A <OPC< 66.7A

| Component | N15V-GM-S Config D | N15-S-0T-S Config B |
|----------------|--------------------|---------------------|
| R1 (PRR222) | 27K | 20K |
| R2 (PRR206) | 64.27025.60L | 64.20025.60L |
| R3 (PRR208) | 7.5K | 20K |
| R4+R5 (PRR209) | 64.7515.60L | 64.20025.60L |
| C (PCR223) | 0 | 2K |
| | 63.80034.10L | 64.20015.60L |
| | 7.377K | 10K |
| | 64.78715.60L | 64.18025.60L |
| | 5.6P | 2.7P |
| | 78.56222.2FL | 78.27224.2FL |

| PWM-VID Specification | Config A | Config B | Config C | Config D |
|--|----------|----------|----------|----------|
| Vmin | 0.5 | 0.5 | 0.5 | 0.5 |
| Vmax | 1.2 | 1.2 | 1.15 | 1.15 |
| Vboot | 0.875 | 0.9 | 0.9 | 1.028 |
| Voltage Step Vstep | 6.25 | 6.25 | 25 | 12.5 |
| Number of Voltage Levels N | level | 96 | 20 | 20 |
| PWM Frequency F _{min} | MHz | 1.125 | 0.676 | 0.676 |
| PWM Minimum Pulse Width T _{min} | ns | 9.26 | 74 | 74 |
| VID Transient Time T | <100 | <100 | <100 | <100 |

| Component Value | Config A | Config B | Config C | Config D |
|-----------------|----------|----------|----------|----------|
| R1 (1k) | KQ 39 | 20 | 39 | 27 |
| R2 (1k) | KQ 39 | 20 | 30 | 7.5 |
| R3 (1k) | KQ 1.5 | 2 | 3 | 0 |
| R4 (1k) | KQ 30 | 18 | 24 | 6.2 |
| R5 (1k) | KQ 1.5 | 0 | 3 | 1.74 |
| C | nF | 1.5 | 2.7 | 5.6 |

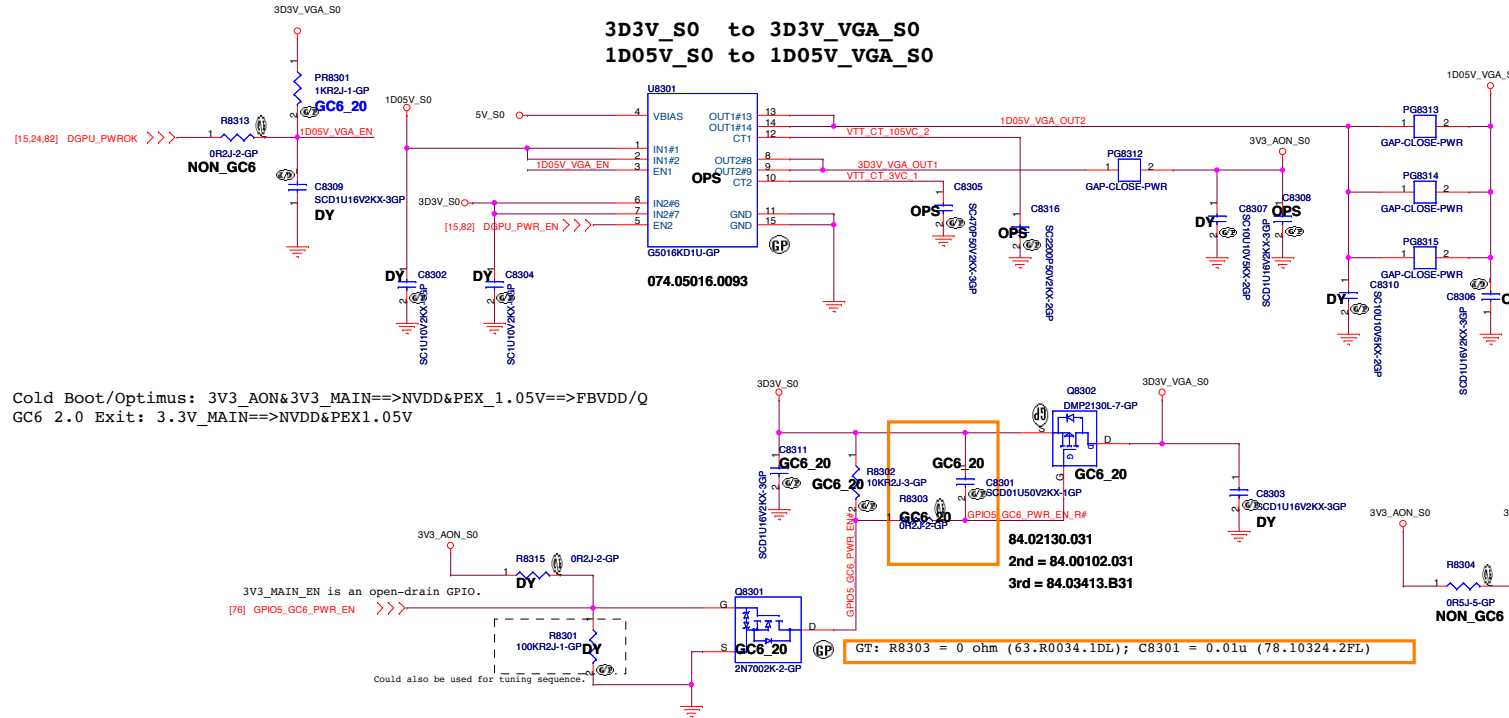
I/P cap: 10u 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHORE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
 O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
 H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm4.5Vgs/ 84.A14DP.037
 L/S: SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm4.5Vgs/ 84.SRA06.037



3D3V_VGA_S0 1D05V_VGA_S0

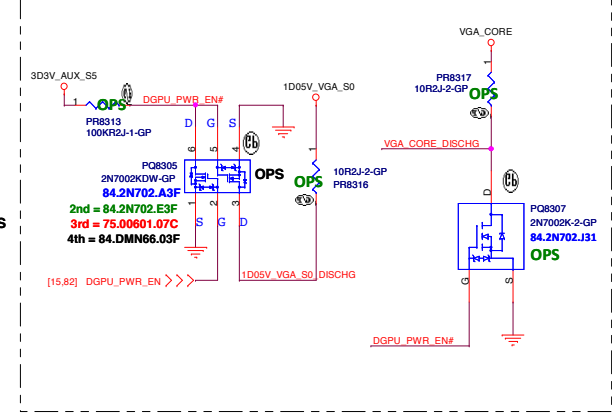
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

3D3V_S0 to 3D3V_VGA_S0 1D05V_S0 to 1D05V_VGA_S0

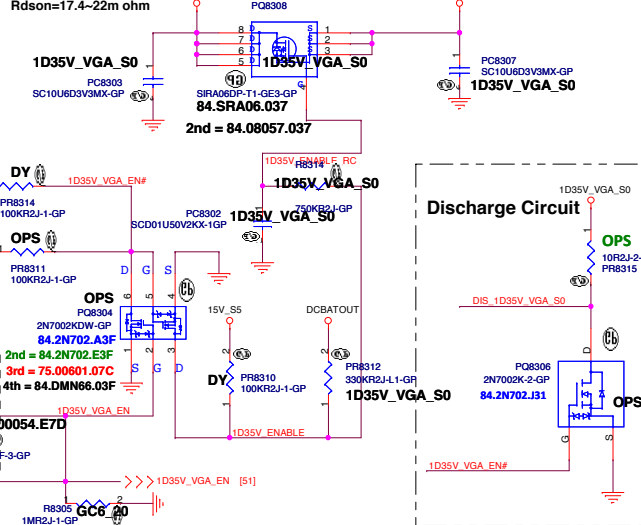


Cold Boot/Optimus: 3V3_AON&3V3_MAIN=>NVDD&PEX_1.05V=>FBVDD/Q
GC6 2.0 Exit: 3.3V_MAIN=>NVDD&PEX1.05V

VGA_CORE&1D05V_VGA_S0 Discharge Circuit



A04468, SO-8
Id=?A, Qg=9-12nC
Rdson=17.4-22m ohm



| CTx (pF) | Rise Time (µs) 10% - 90%, COUT = 0.1µF @ VIN; VOUT=0 ohm load | | | | | | | |
|----------|---|-------|------|------|------|-------|------|------|
| | Typical values @ 25°C, 25V X7R 10% ceramic cap | | | | | | | |
| | 5V | 3.3V | 1.8V | 1.5V | 1.2V | 1.05V | 1V | 0.8V |
| 0 | 107 | 72 | 46 | 41 | 36 | 34 | 33 | 29 |
| 220 | 425 | 276 | 146 | 122 | 103 | 91 | 88 | 74 |
| 270 | 489 | 316 | 172 | 139 | 121 | 107 | 104 | 84 |
| 470 | 774 | 487 | 272 | 224 | 181 | 159 | 154 | 123 |
| 680 | 1108 | 708 | 375 | 317 | 242 | 221 | 213 | 168 |
| 1000 | 1561 | 1007 | 546 | 441 | 364 | 314 | 299 | 234 |
| 2200 | 3600 | 2289 | 1240 | 1019 | 817 | 681 | 665 | 539 |
| 4700 | 7757 | 5092 | 2674 | 2203 | 1808 | 1592 | 1516 | 1177 |
| 10000 | 15700 | 10310 | 5601 | 4659 | 3674 | 3401 | 3197 | 2562 |

Table 1. Rise time vs. CTx value

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Title: **DISCRETE VGA POWER**

Size: Custom Document Number: **Janus HSW 40/50/70** Rev: **A00**

Date: Monday, February 10, 2014 Sheet: 83 of 104

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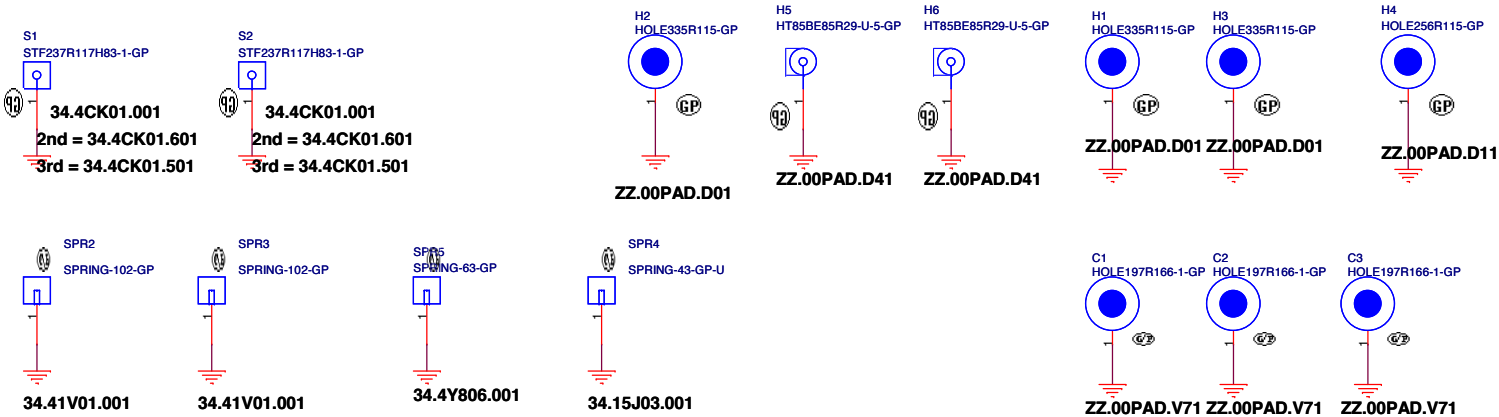
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| Title | | |
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| Date: Friday, February 07, 2014 | Sheet 84 of | 104 |

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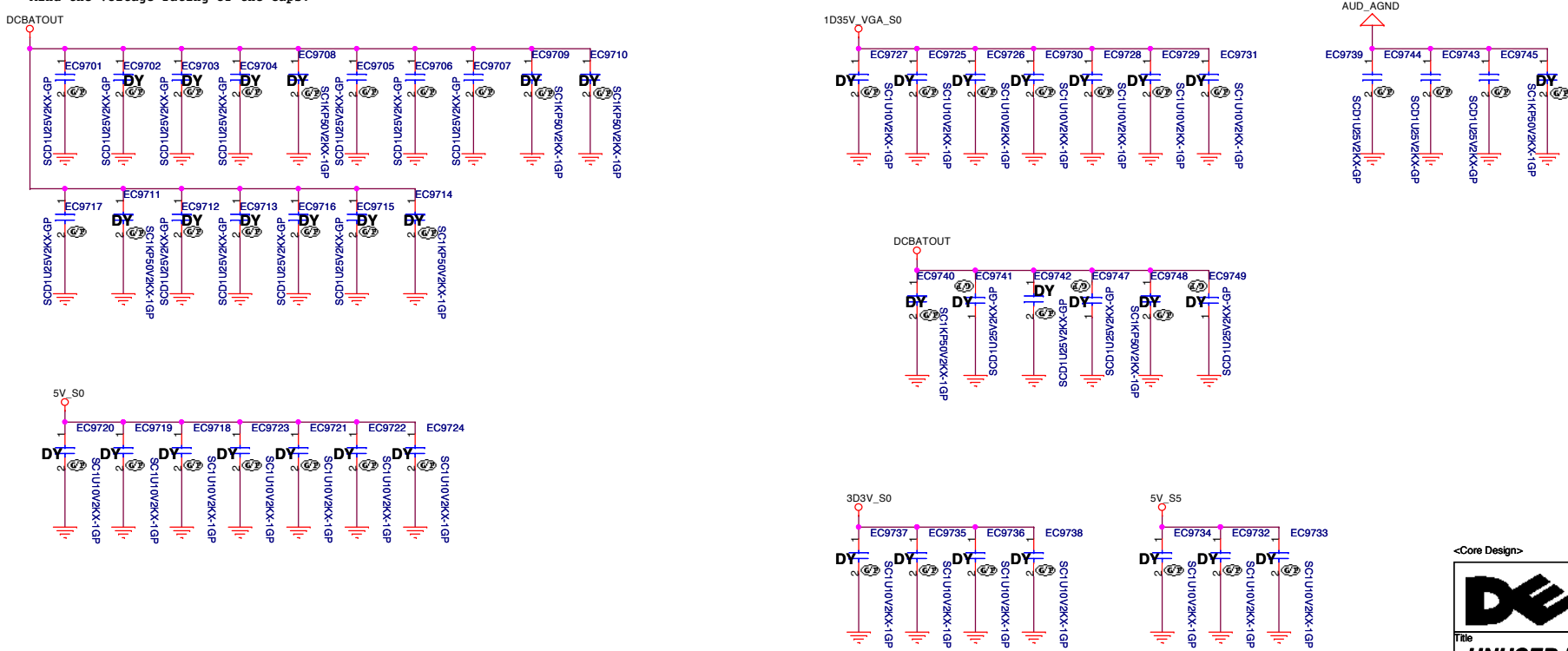
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| Title | | |
| Reserved | | |
| Size A3 | Document Number Janus HSW 40/50/70 | Rev A00 |
| Date: Friday, February 07, 2014 | Sheet 85 | of 104 |

SSID = Mechanical



SSID = EMI

Mind the voltage rating of the caps.



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Title: **UNUSED PARTS/EMI Capacitors**

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| Title | | | Free Fall Sensor | | |
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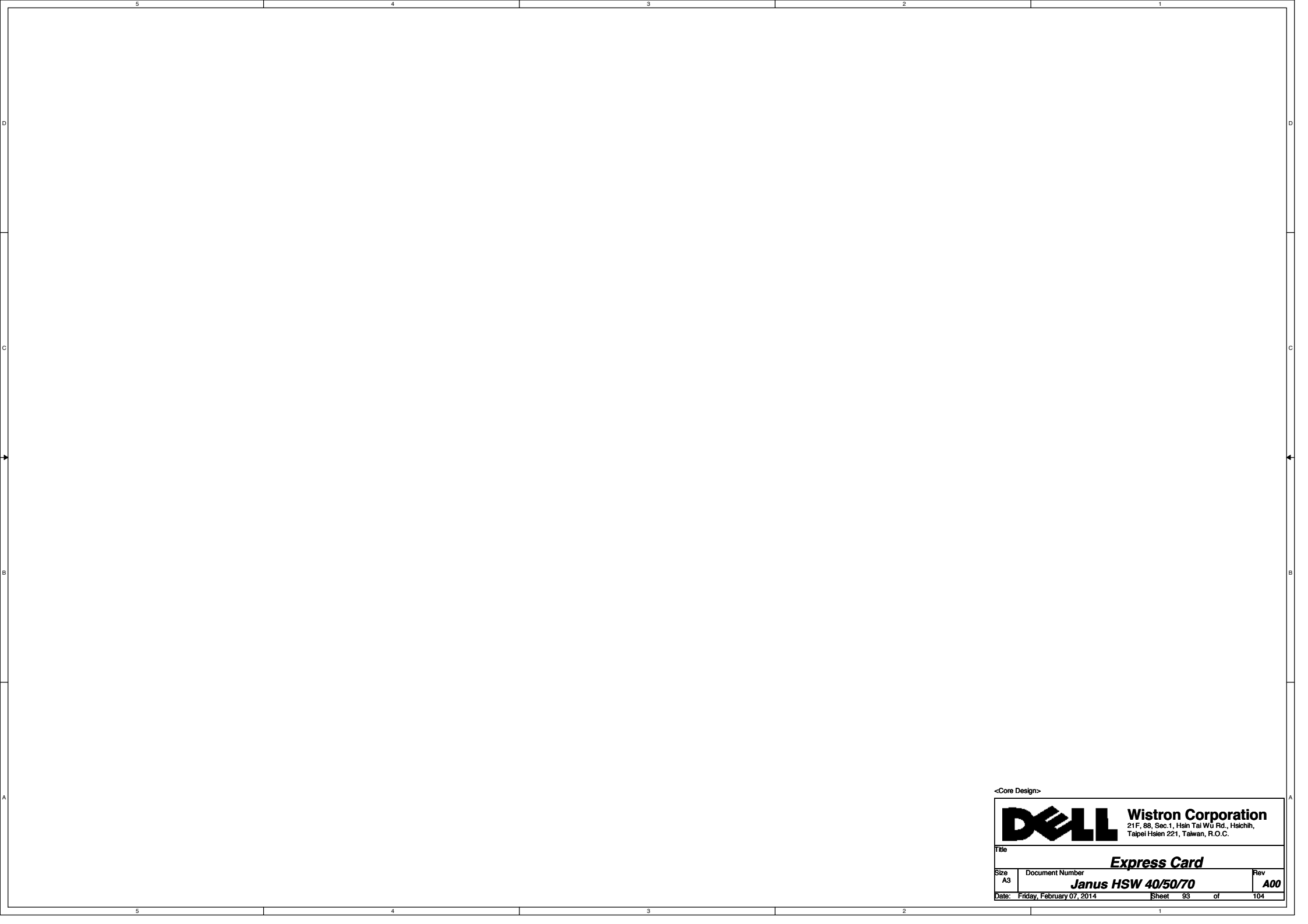
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| Title | | |
| LVDS Switch | | |
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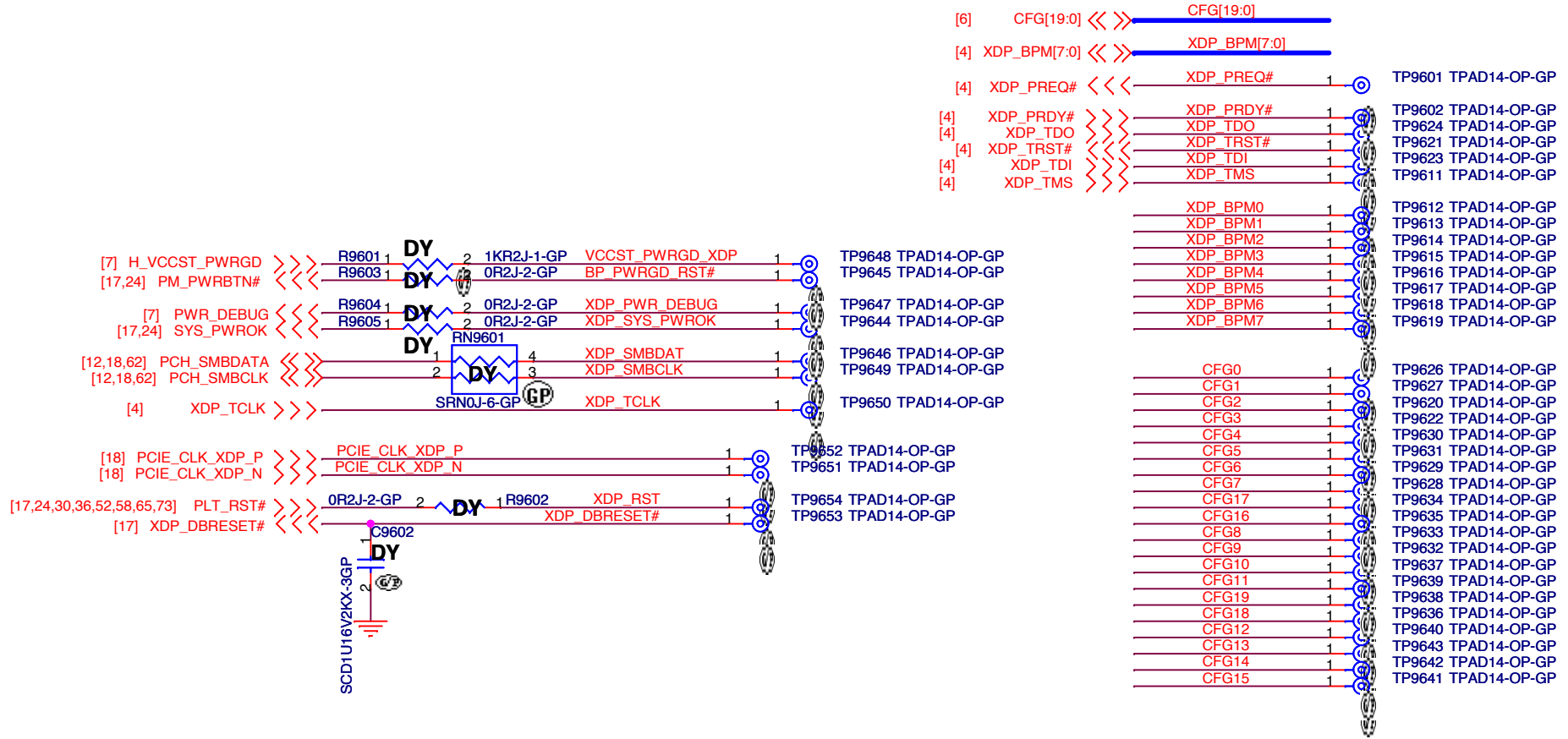
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| Title | | | | | |
| CRT Switch | | | | | |
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| A3 | Janus HSW 40/50/70 | | | | A00 |
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SSID = XDP

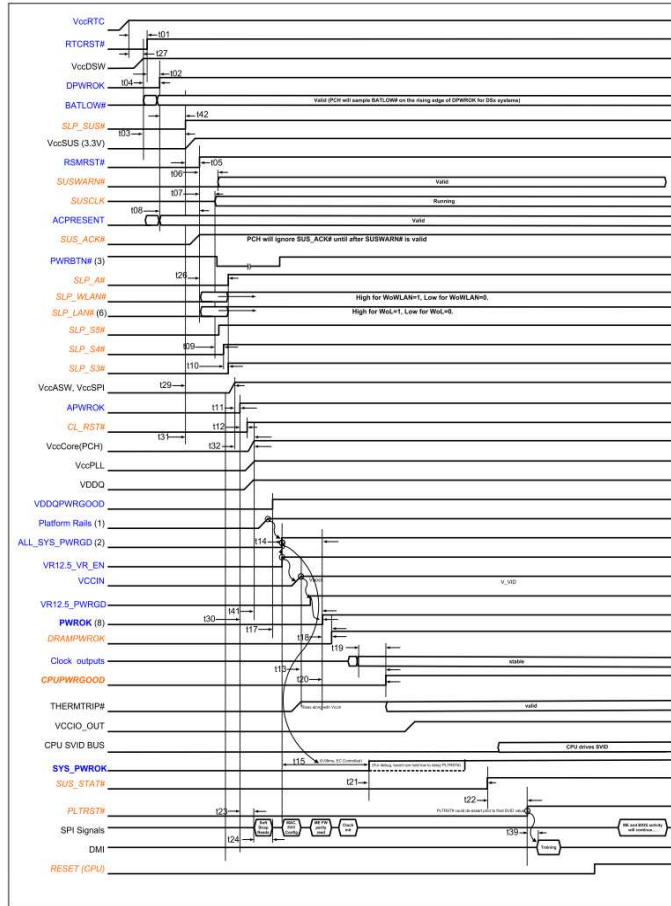
CPU XDP



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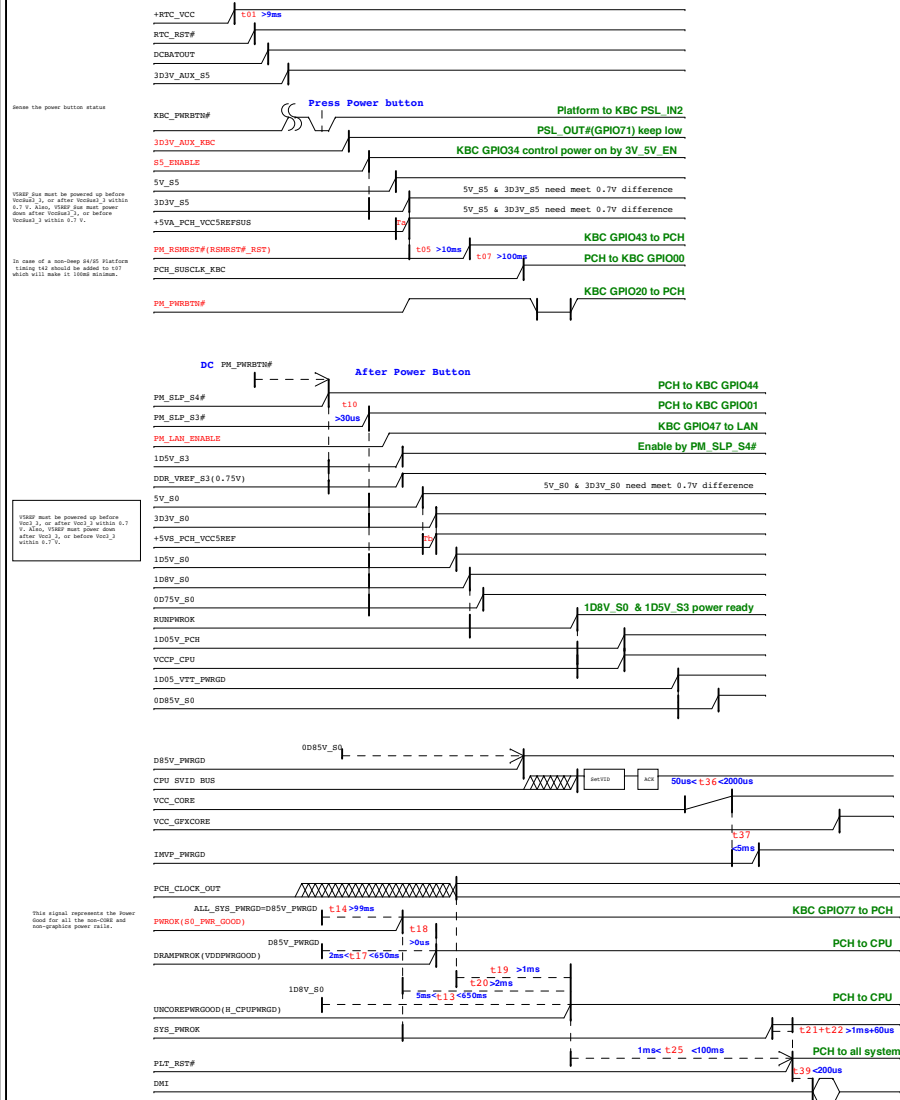
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| | | Wistron Corporation | |
| | | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| CPU/PCH XDP | | | |
| Size | Document Number | | Rev |
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Shark Bay Platform Power Sequence

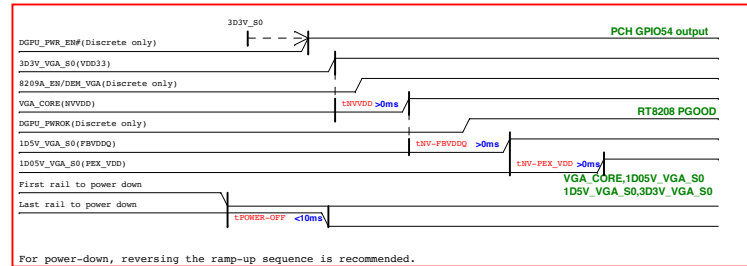


(DC mode)

Red Words: Controlled by RC GPIO

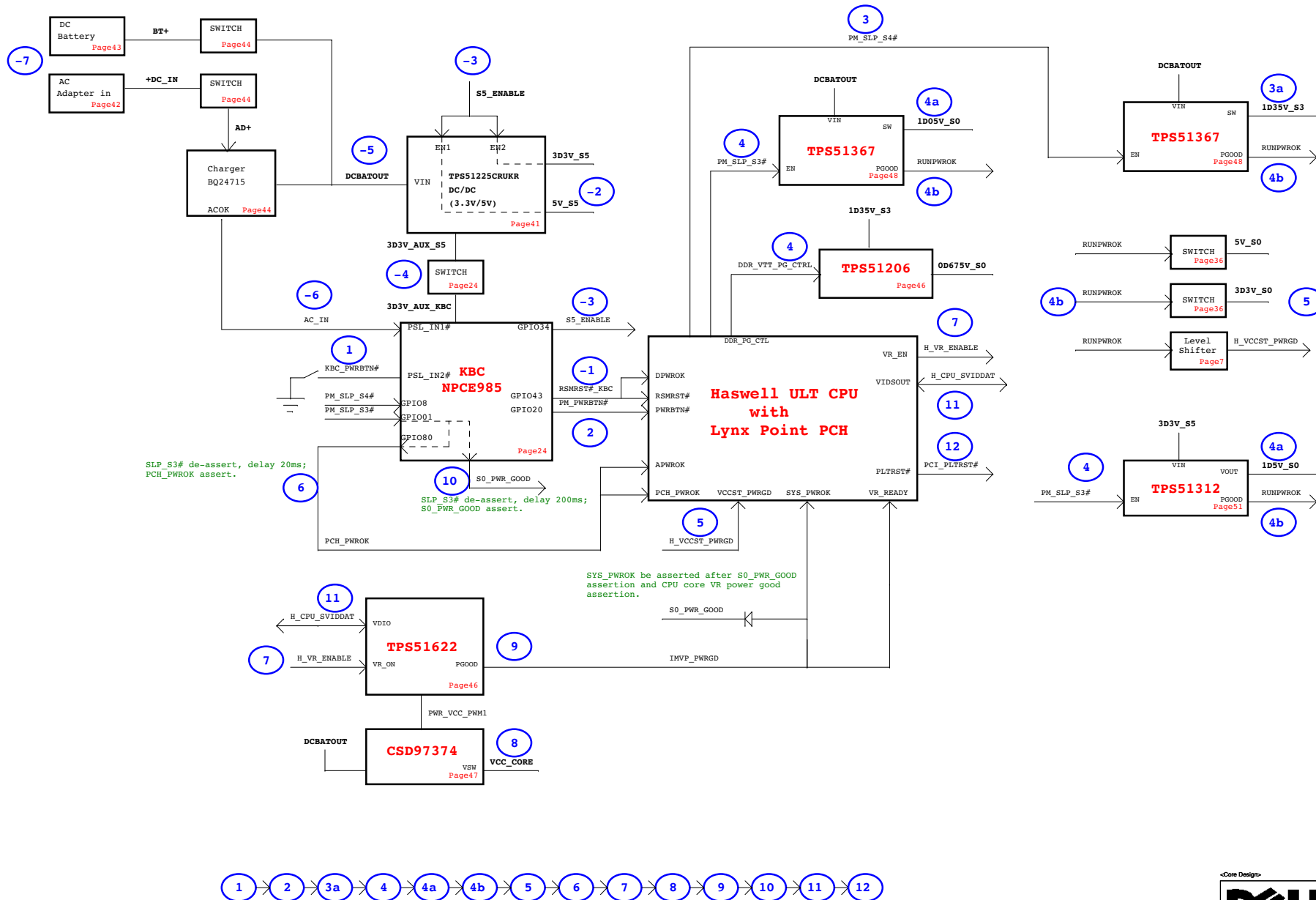


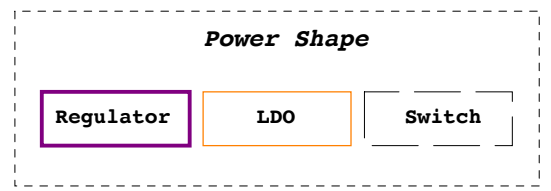
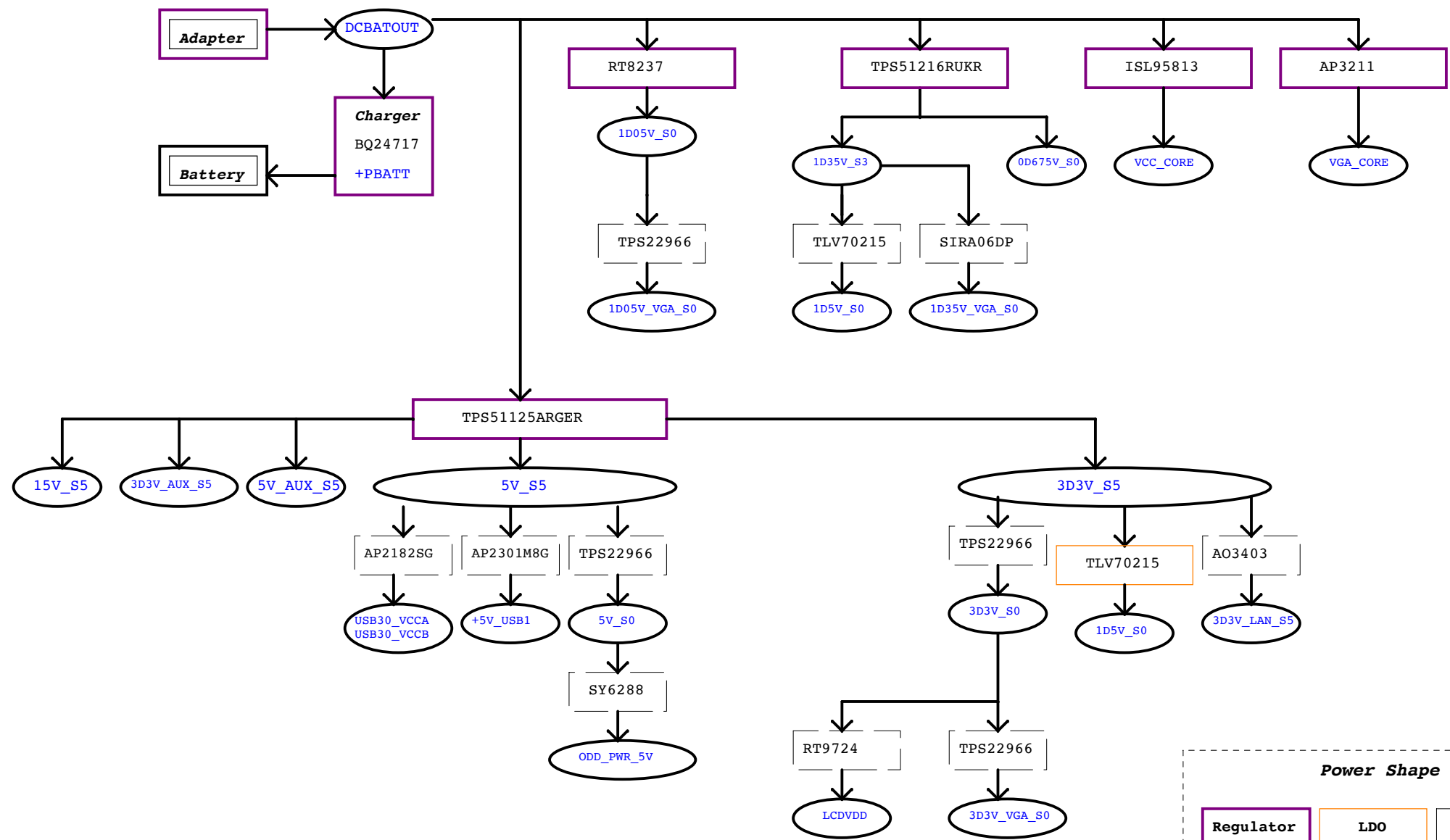
N14P-GT Power-Up/Down Sequence



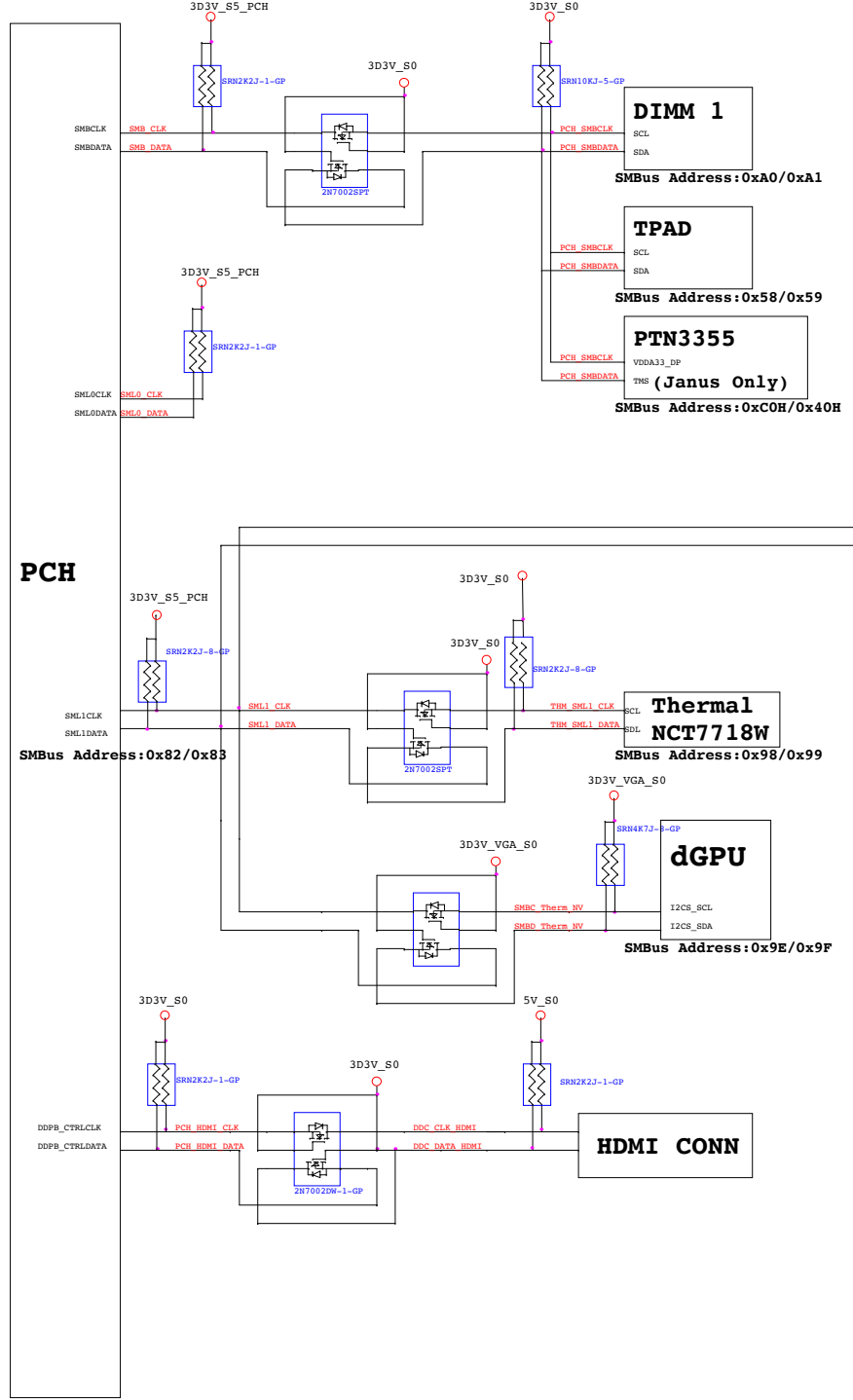
For power-down, reversing the ramp-up sequence is recommended.

Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM

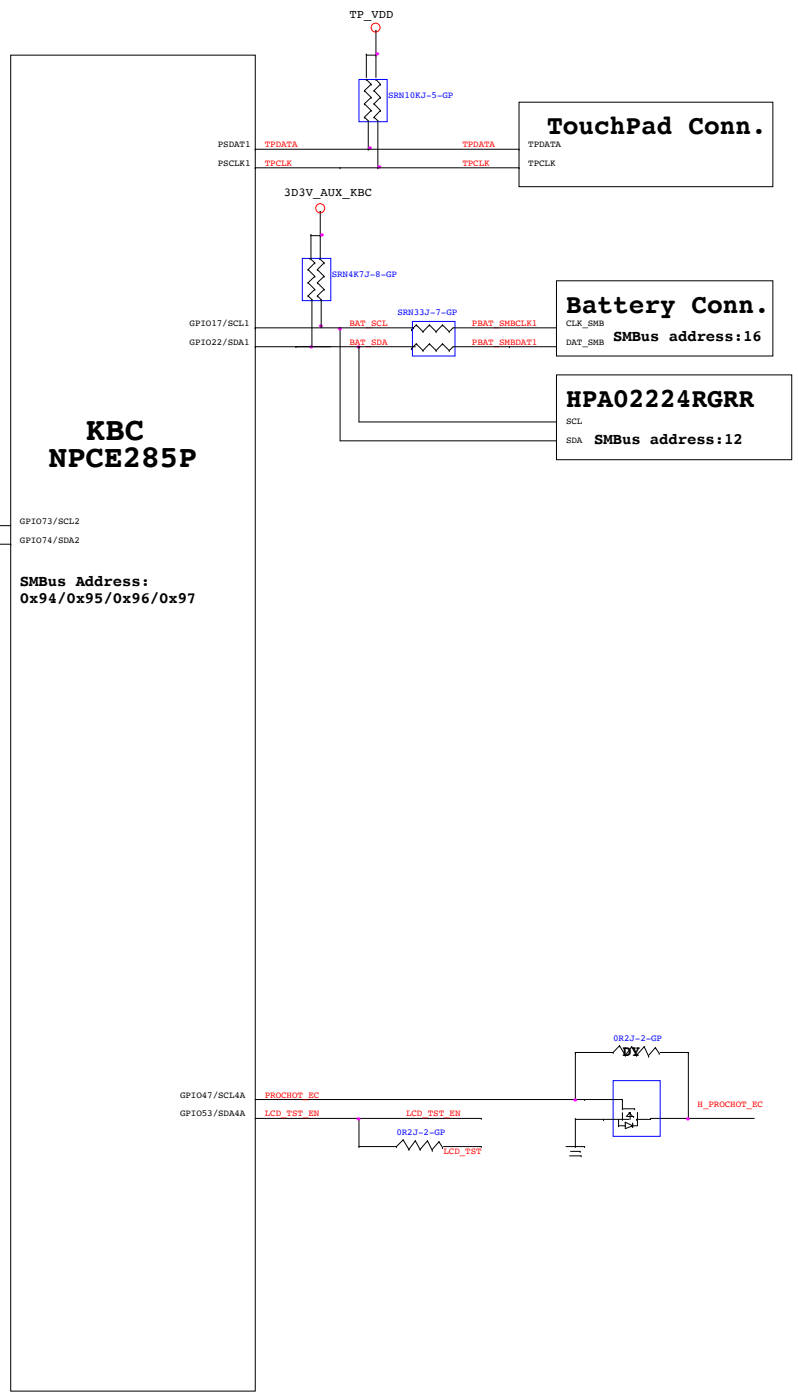




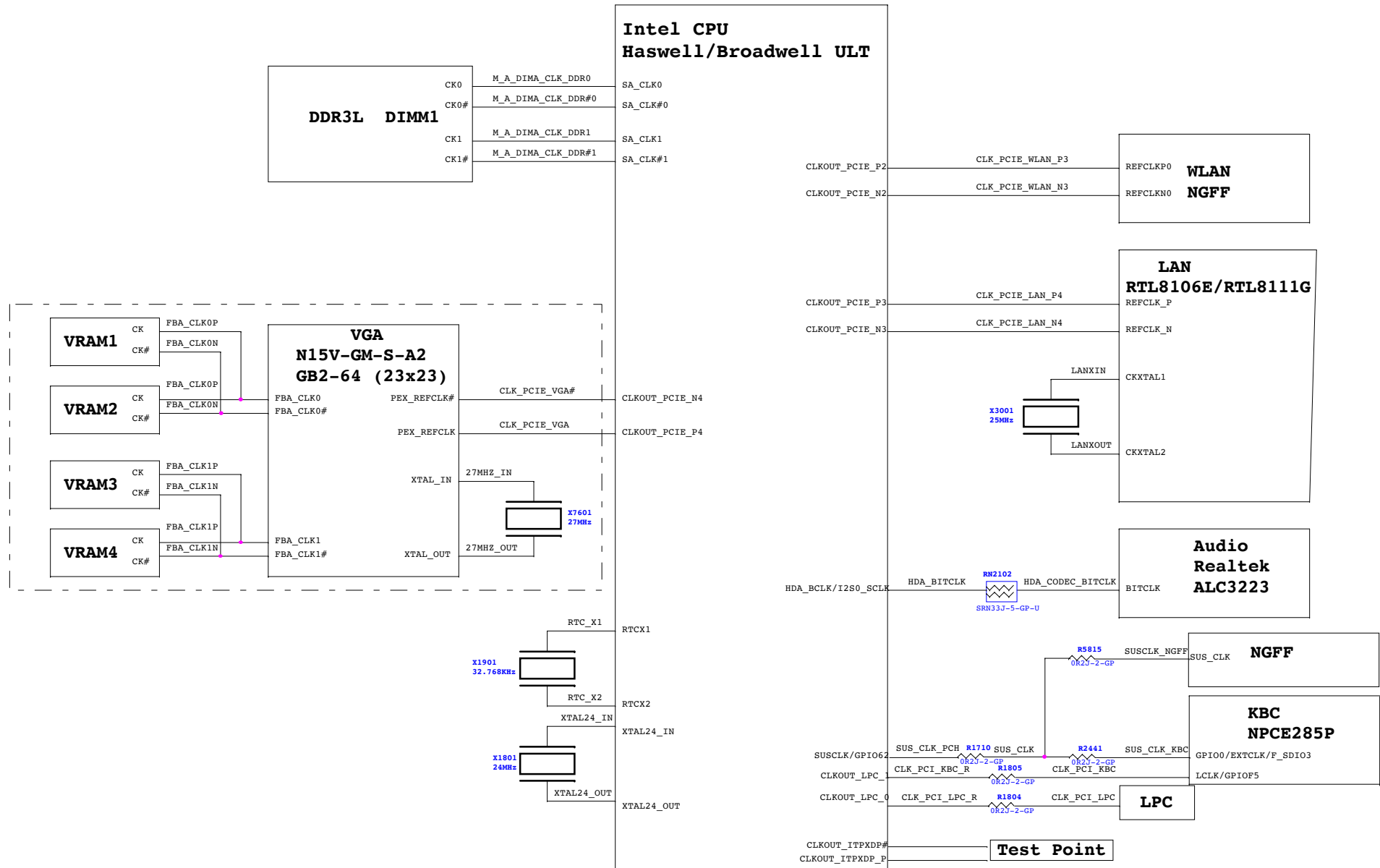
PCH SMBus Block Diagram



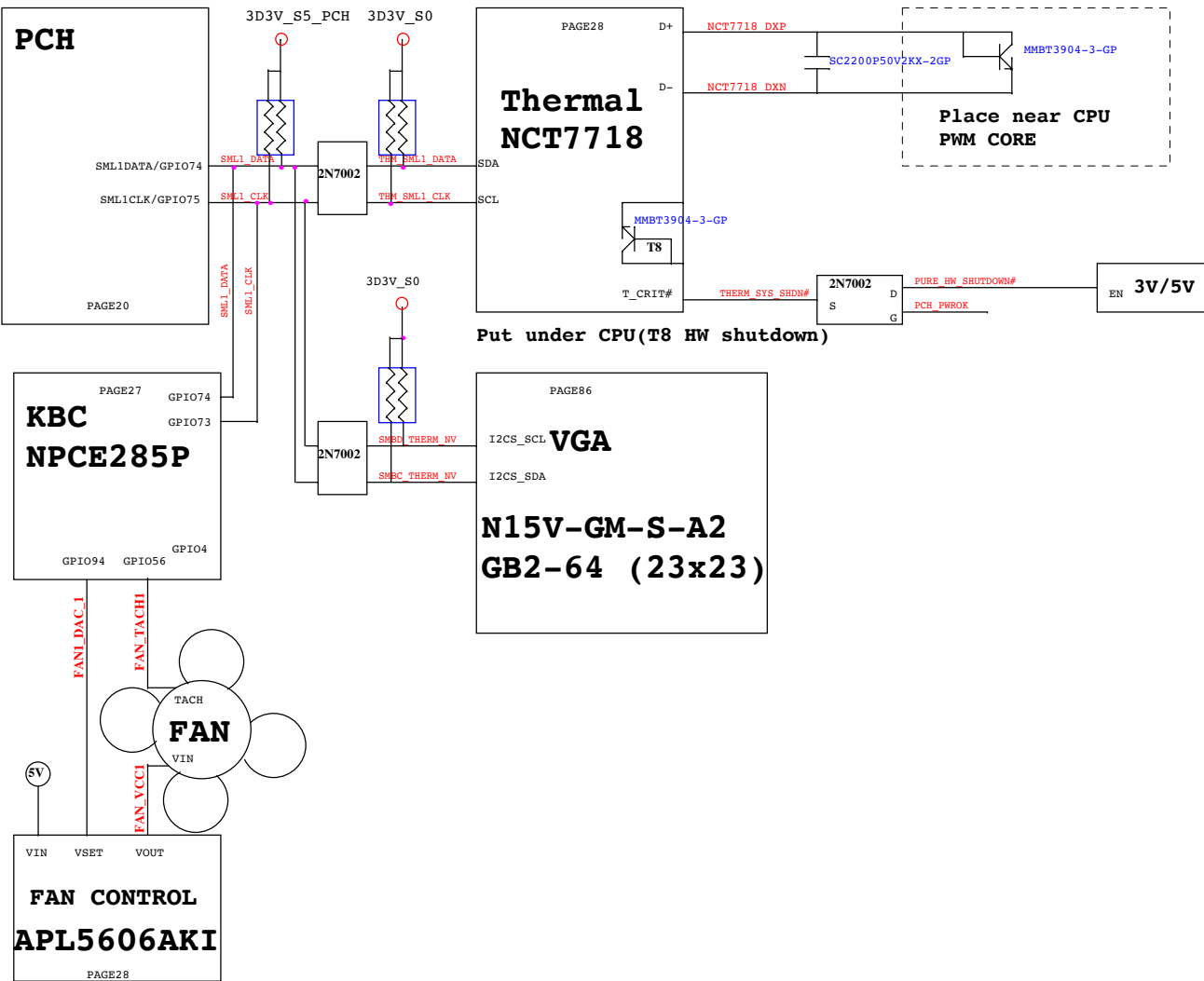
KBC SMBus Block Diagram



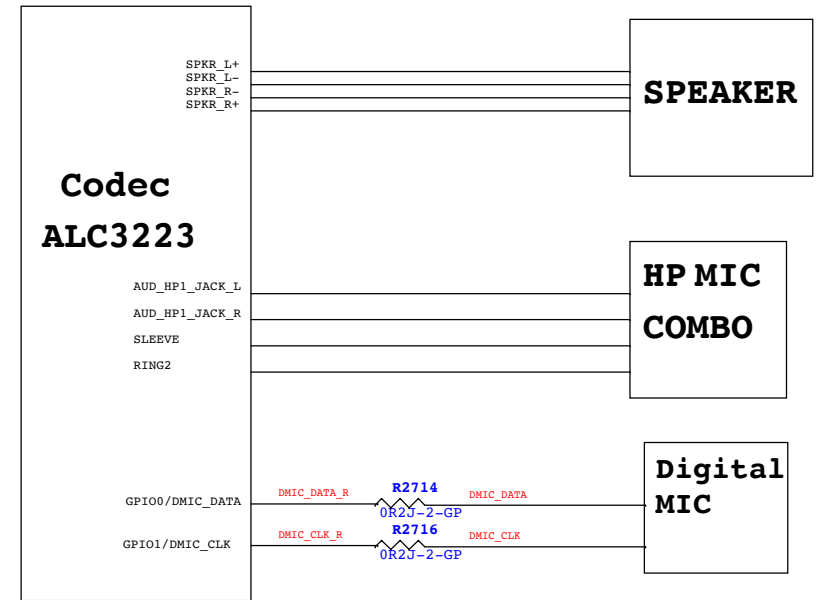
CLK Block Diagram



Thermal Block Diagram



Audio Block Diagram




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Change notes -

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