Discrete/UMA Schematics Document

Sandy Bridge

Intel PCH

2011-01-19

REV : XXX

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX

BOM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

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A3	LZ57	-1

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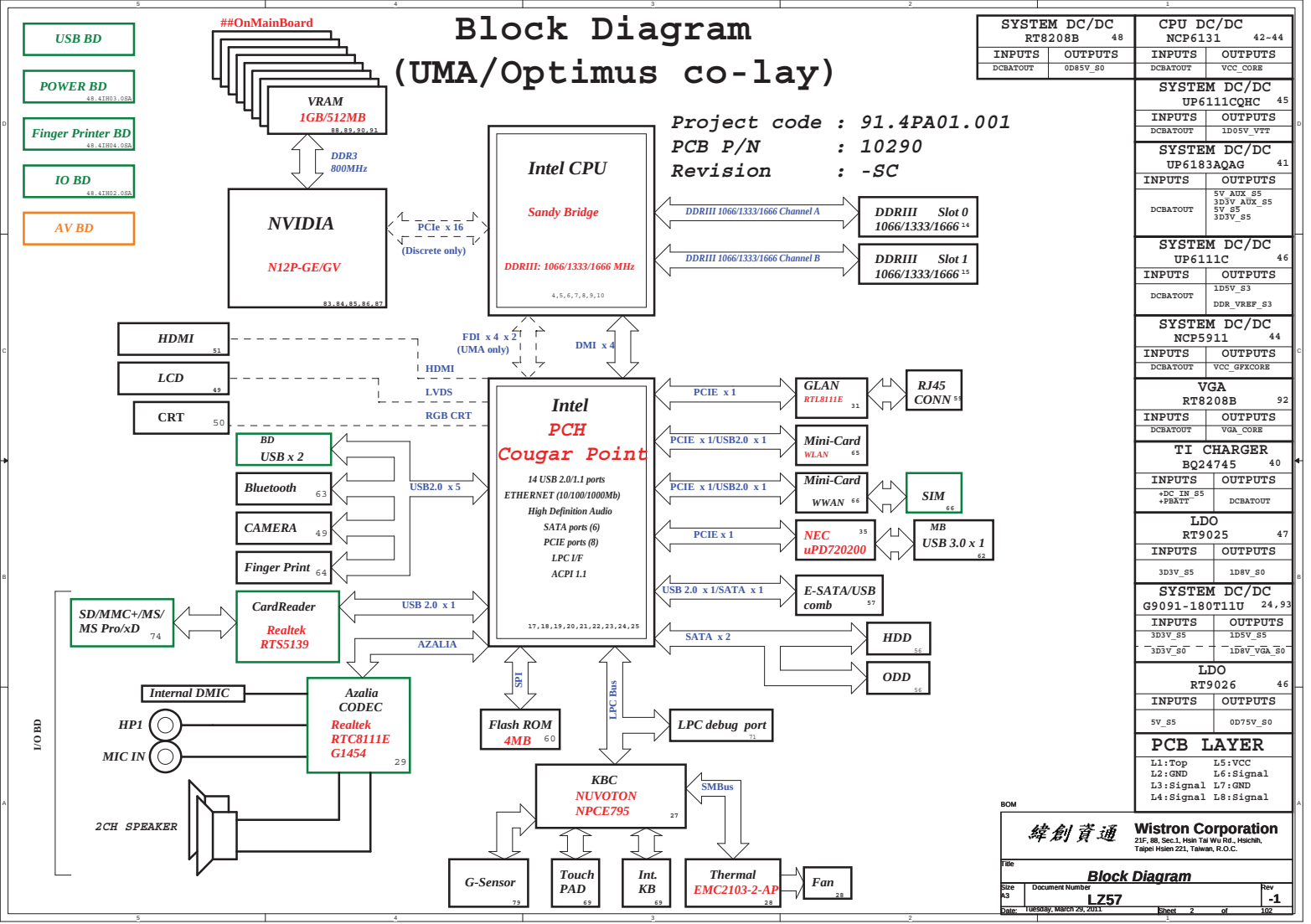
Block Diagram (UMA/Optimus co-lay)



Project code : 91.4PA01.001
PCB P/N : 10290
Revision : -SC

SYSTEM DC/DC RT8208B 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42-44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6111CQHC 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183AQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6111C 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

LDO RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S5
3D3V_S0	1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ ~~10 kΩ weak pull-up resistor~~
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I2 C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

BOM

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_ICOMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

delete R404&RN 401 @20100630

62.10055.321

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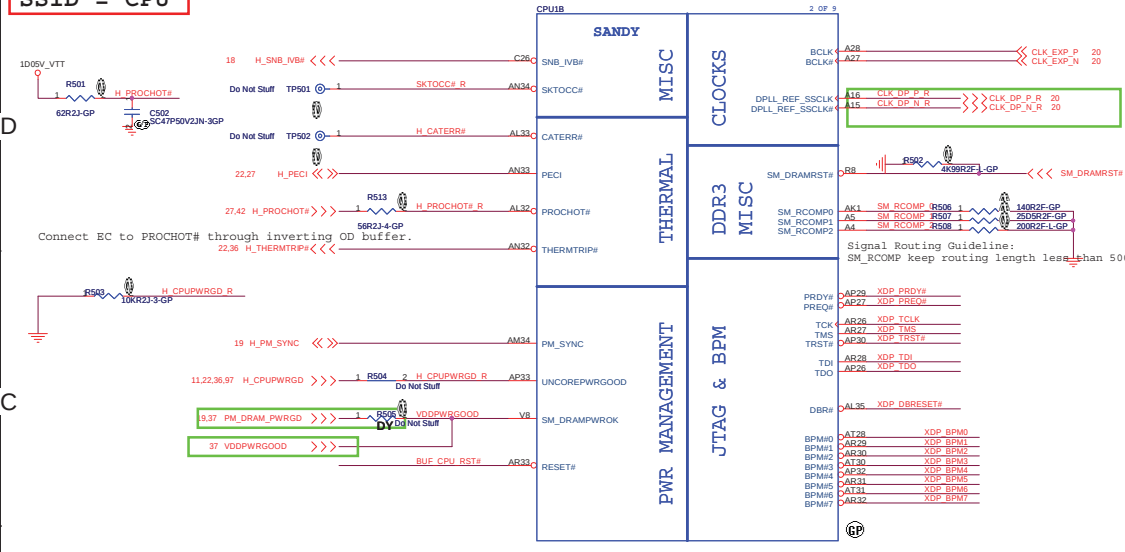
Title: CPU (PCIE/DMI/FDI)		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 4 of 102	

SSID = CPU



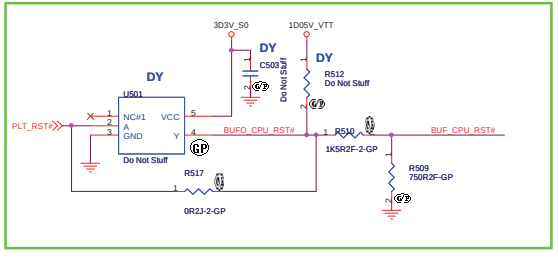
Connect EC to PROCHOT# through inverting OD buffer.

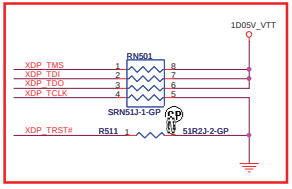
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

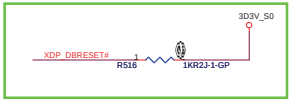
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

20100722 SA confirm.

20100722 follow Astro add buffer







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Title	CPU (THERMAL/CLOCK/PM)
Size A3	Document Number LZ57 Rev -1
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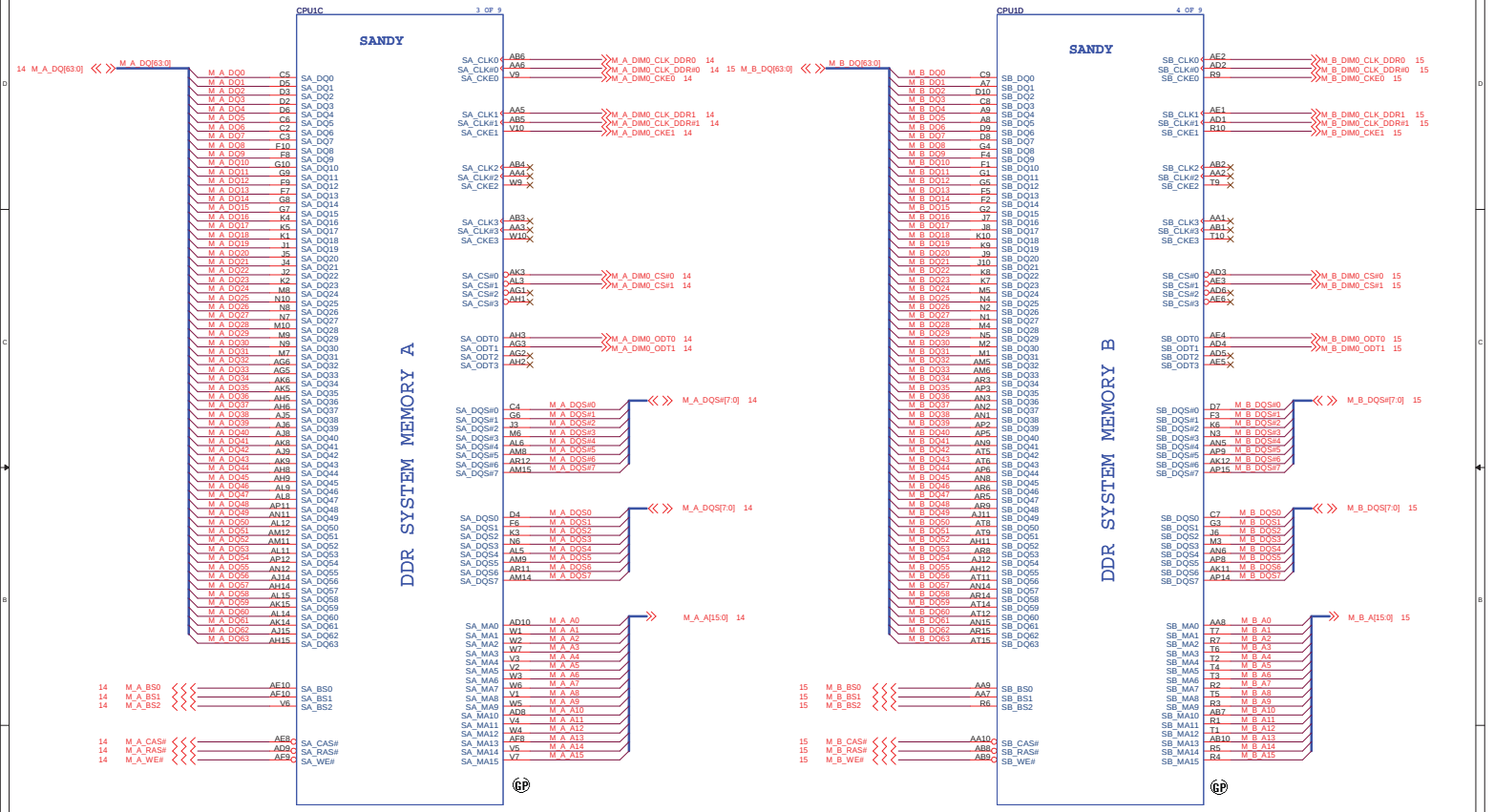
SSID = CPU



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Title: CPU (DDR)

Size	Document Number	Rev
A3	LZ57	-1

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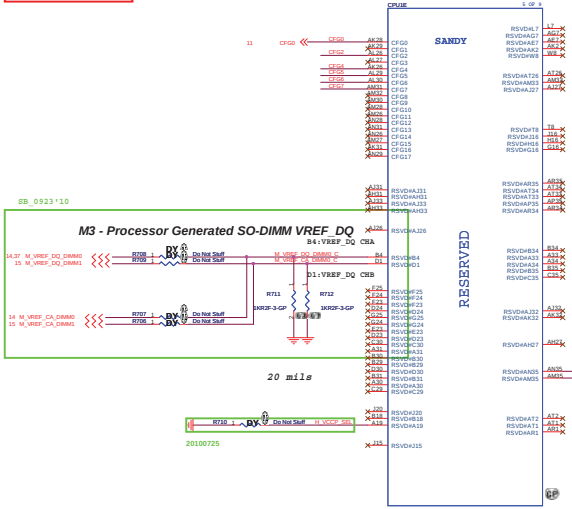
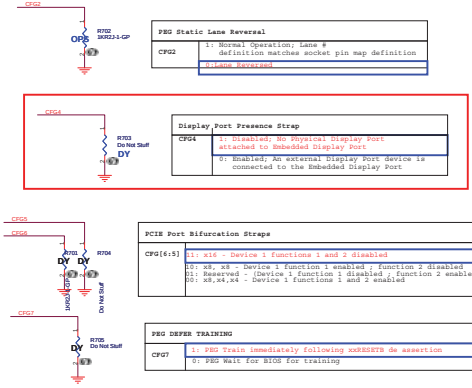
SSID = CPU





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Title: CPU (RESERVED)

Size	Document Number	Rev
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SSID = CPU

PROCESSOR CORE POWER

53A

VCC_CORE

C801 C802 C803 C804 C811 — SC10U6D3V5KX-1GP

C815 C817 C818 C819 C820 — SC10U6D3V5KX-1GP

C816 C821 C822 C823 C824 C825 C826 C827 — SC10U6D3V5KX-1GP

C837 C836 C835 C834 C833 C832 C831 C828 — SC10U6D3V5KX-1GP

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

POWER

CPU1F — SANDY — 6 OF 9

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

PEG AND DDR

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 — VCCIO

C805 C806 C807 C808 C809 C810 C838 C839 C840 C841 — SC10U6D3V5KX-1GP — Do Not Stuff

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 — VCCIO

C812 C813 C814 C829 C830 C842 C843 C844 C845 — SC10U6D3V5KX-1GP — Do Not Stuff

J23 — VCCIO

R804 need to close to CPU

1D05V_VTT

H_CPU_SVIDDAT — R804 1 — 130R2F-1-GP

S-HS_20100610 V1.0

CORE SUPPLY

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT# — R803 1 — 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK — H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT — H_CPU_SVIDDAT 42

SENSE LINES

VCC_CORE

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 — VCCSENSE 42
VSS_SENSE AJ34 — VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 — VCCIO_SENSE 45
VSSIO_SENSE A10 — VSSIO_SENSE 45

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Title: CPU (VCC_CORE)

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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

POWER

CPU1G — SANDY — GRAPHICS

PROCESSOR VAXG: 24A

VCC_GFXCORE

C301 Do Not Stuff, C302 SCU(U6D)V6KX-1GP, C303 Do Not Stuff, C304 SCU(U6D)V6KX-1GP, C305 SCU(U6D)V6KX-1GP, C306 SCU(U6D)V6KX-1GP

C307 SCU(U6D)V6KX-1GP, C308 SCU(U6D)V6KX-1GP, C318 SCU(U6D)V6KX-1GP, C319 SCU(U6D)V6KX-1GP, C320 SCU(U6D)V6KX-1GP, C321 SCU(U6D)V6KX-1GP

VAXG: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17

SENSE LINES

VAXG_SENSE — AK35
VSSAXG_SENSE — AK34
→ VCC_AXG_SENSE 42, VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

VREF

+V_SM_VREF_CNT should have 10 mil trace width

SM_VREF — AL1 — +V_SM_VREF_CNT → +V_SM_VREF_CNT 37

Close to CPU

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

S-HR_20100609 V1.0

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

VDDQ: AE7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

C309 SCU(U6D)V6KX-1GP, C310 SCU(U6D)V6KX-1GP, C311 SCU(U6D)V6KX-1GP, C312 Do Not Stuff, C313 Do Not Stuff, C314 SCU(U6D)V6KX-1GP

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

C316 Do Not Stuff, C315 SCU(U6D)V5KX-1GP, C317 SCU(U6D)V5KX-1GP, TC903 ST330U2VDM-4-GP

VCCSA: M27, M26, L26, J26, J25, J24, H26, H25

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0
R902 100R2F-L1-GP-U Notice:pull-high 100k or 10k

MISC

VCCSA_SENSE — H23 → VCCSA_SENSE 48

FC_C22 — C22
VCCSA_VID1 — C24 → H_FC_C22 48, VCCSA_SEL 48

RN901 SRN1KJ-7-GP

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

TC902 ST330U2VDM-4-GP, C823 SCU(U6D)V6KX-1GP, C822 SCU(U6D)V6KX-1GP, C824 Do Not Stuff

VCCPLL: B6, A6, A2

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

20100721 standard schematic update

BOM

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Title: CPU (VCC_GFXCORE)

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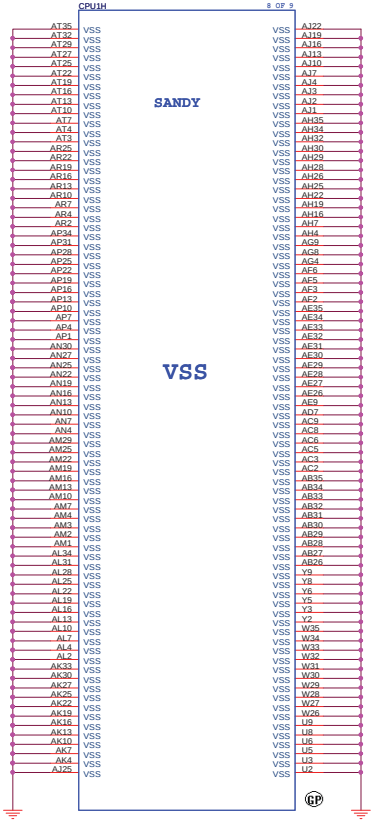
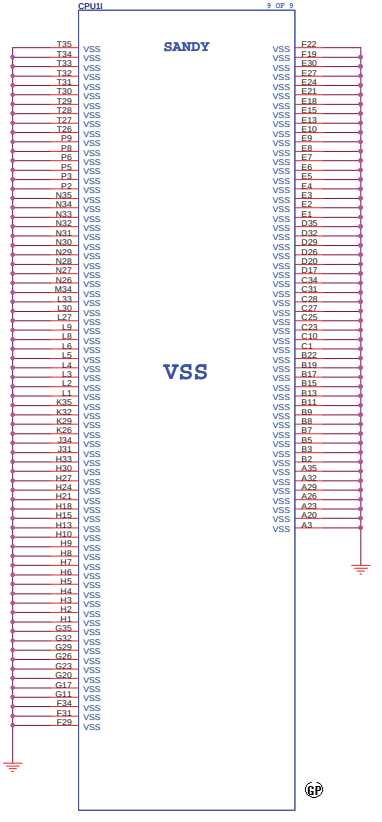
SSID = CPU





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Title: **CPU (VSS)**

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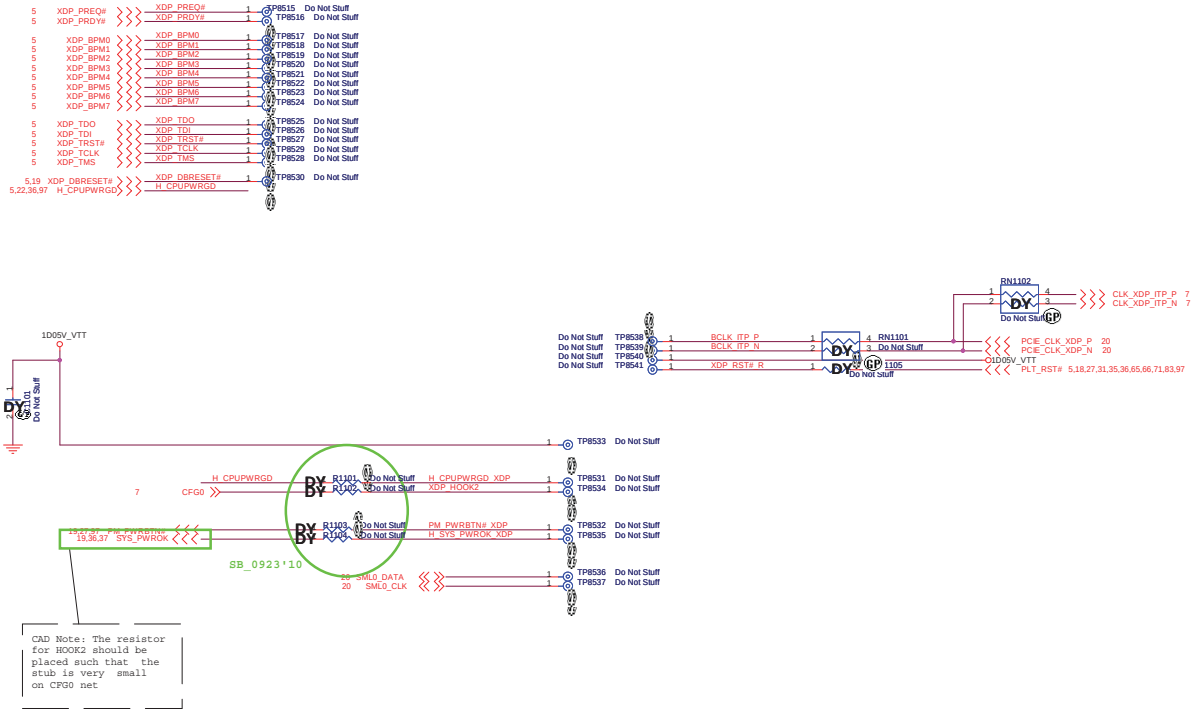

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Title	XDP	
Size: A3	Document Number: LZ57	Rev: -1
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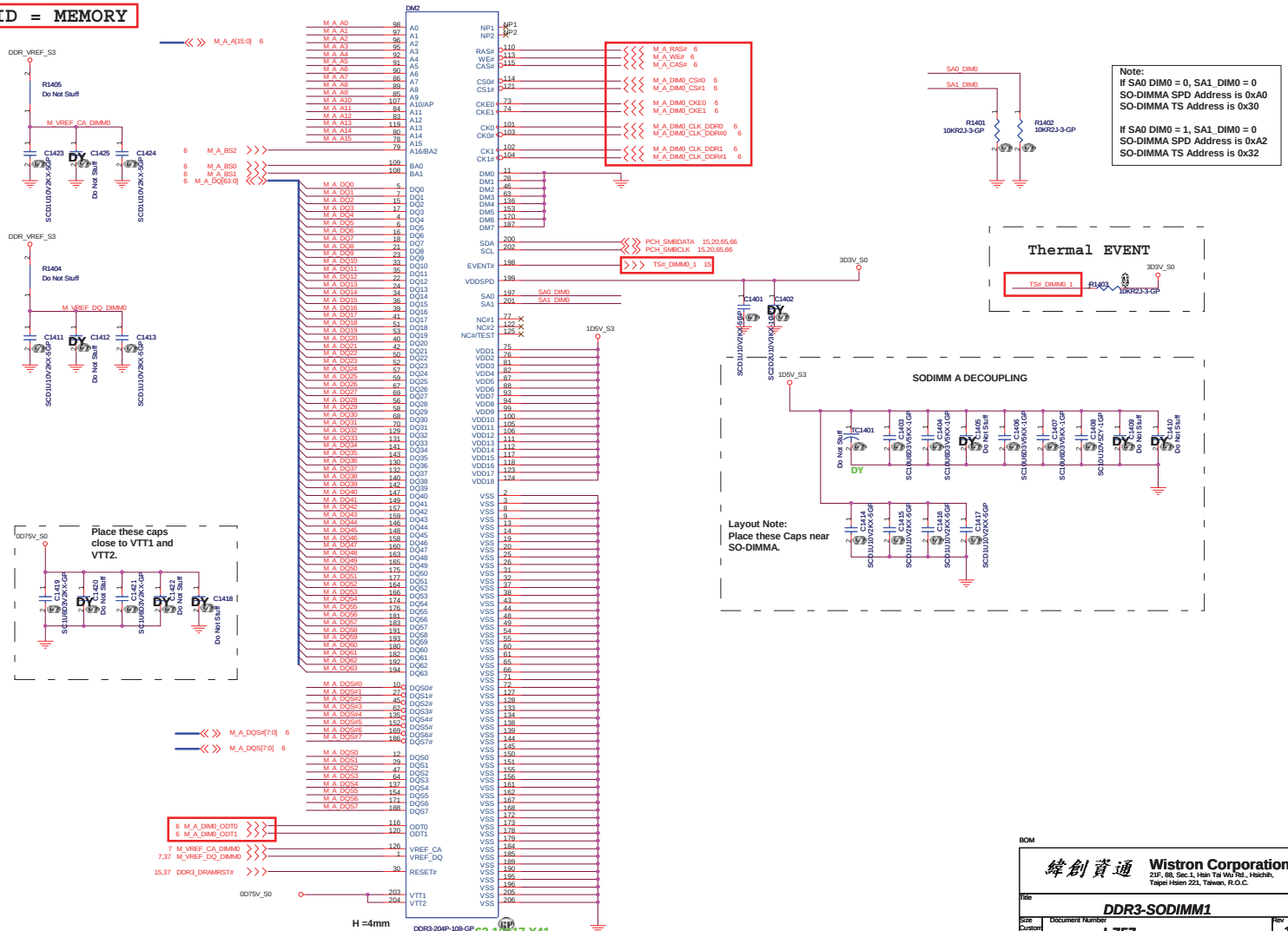
SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

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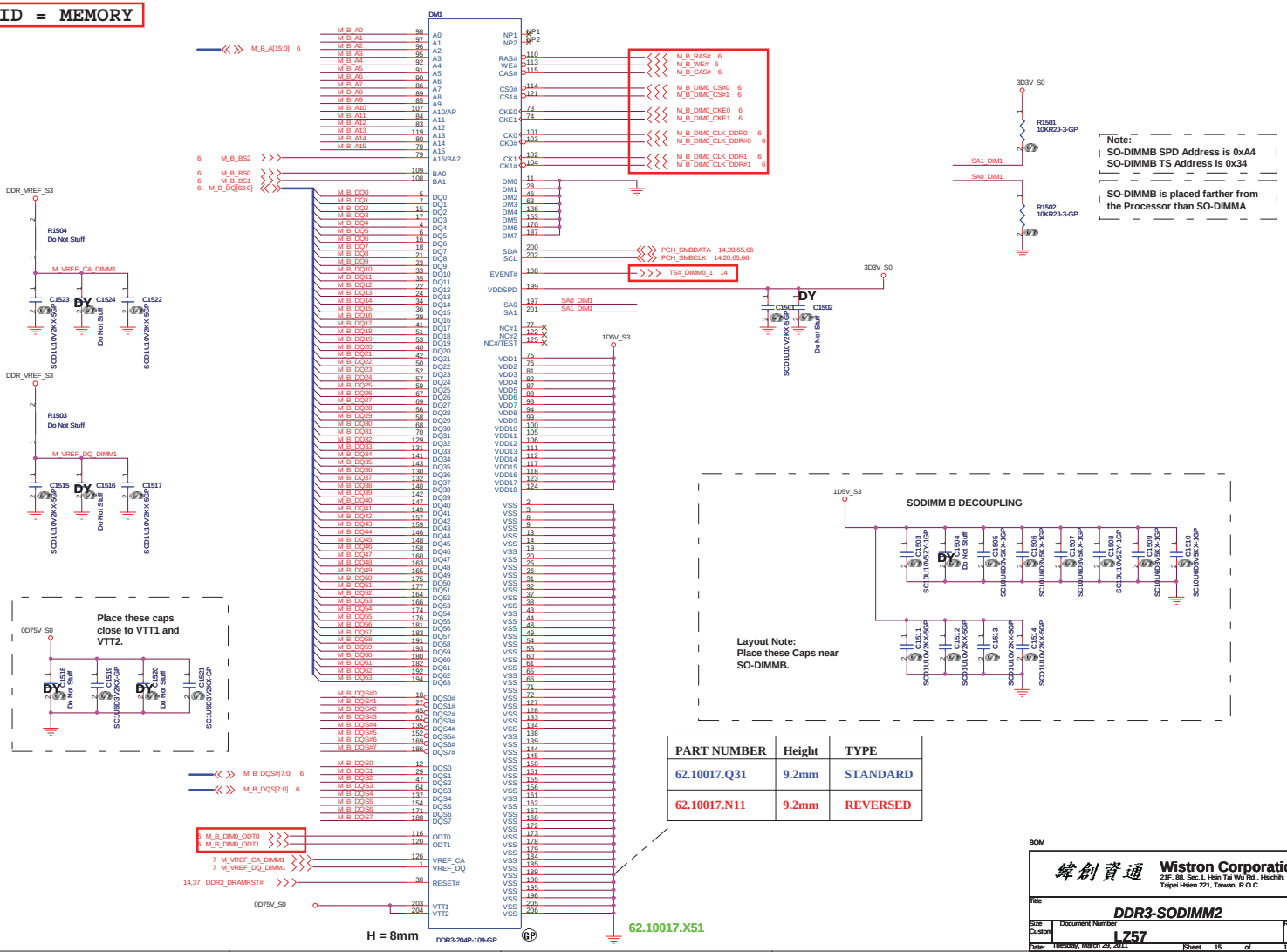
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM1**

Size	Document Number	Rev
Custom	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 14 of 102

SSID = MEMORY



DDR_VREF_S3

R1504 Do Not Stuff

M_VREF_CA_DIMM1

C1523 SCD1U10V2KX-3GP · C1524 DY Do Not Stuff · C1522 SCD1U10V2KX-3GP

DDR_VREF_S3

R1503 Do Not Stuff

M_VREF_DQ_DIMM1

C1515 SCD1U10V2KX-3GP · C1516 DY Do Not Stuff · C1517 SCD1U10V2KX-3GP

Place these caps close to VTT1 and VTT2.

0D75V_S0

C1518 DY Do Not Stuff · C1519 SCU1U603V2KX-GP · C1520 DY Do Not Stuff · C1521 SCU1U603V2KX-GP

3D3V_S0

R1501 10KR2J-3-GP

R1502 10KR2J-3-GP

SA1_DIM1

SA0_DIM1

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

3D3V_S0

C1501 SCD1U10V2KX-3GP · C1502 DY Do Not Stuff

1D5V_S3

SODIMM B DECOUPLING

C1503 SCU10U6D3Y-LGP · C1504 DY Do Not Stuff · C1505 SCU1U603V5KX-1GP · C1506 SCU1U603V5KX-1GP · C1507 SCU1U603V5KX-1GP · C1508 SCU10U6D3Y-LGP · C1509 SCU1U603V5KX-1GP · C1510 SCU1U603V5KX-1GP

C1511 SCD1U10V2KX-3GP · C1512 SCD1U10V2KX-3GP · C1513 SCD1U10V2KX-3GP · C1514 SCD1U10V2KX-3GP

Layout Note:
Place these Caps near SO-DIMMB.

PART NUMBER	Height	TYPE
62.10017.Q31	9.2mm	STANDARD
62.10017.N11	9.2mm	REVERSED

BOM

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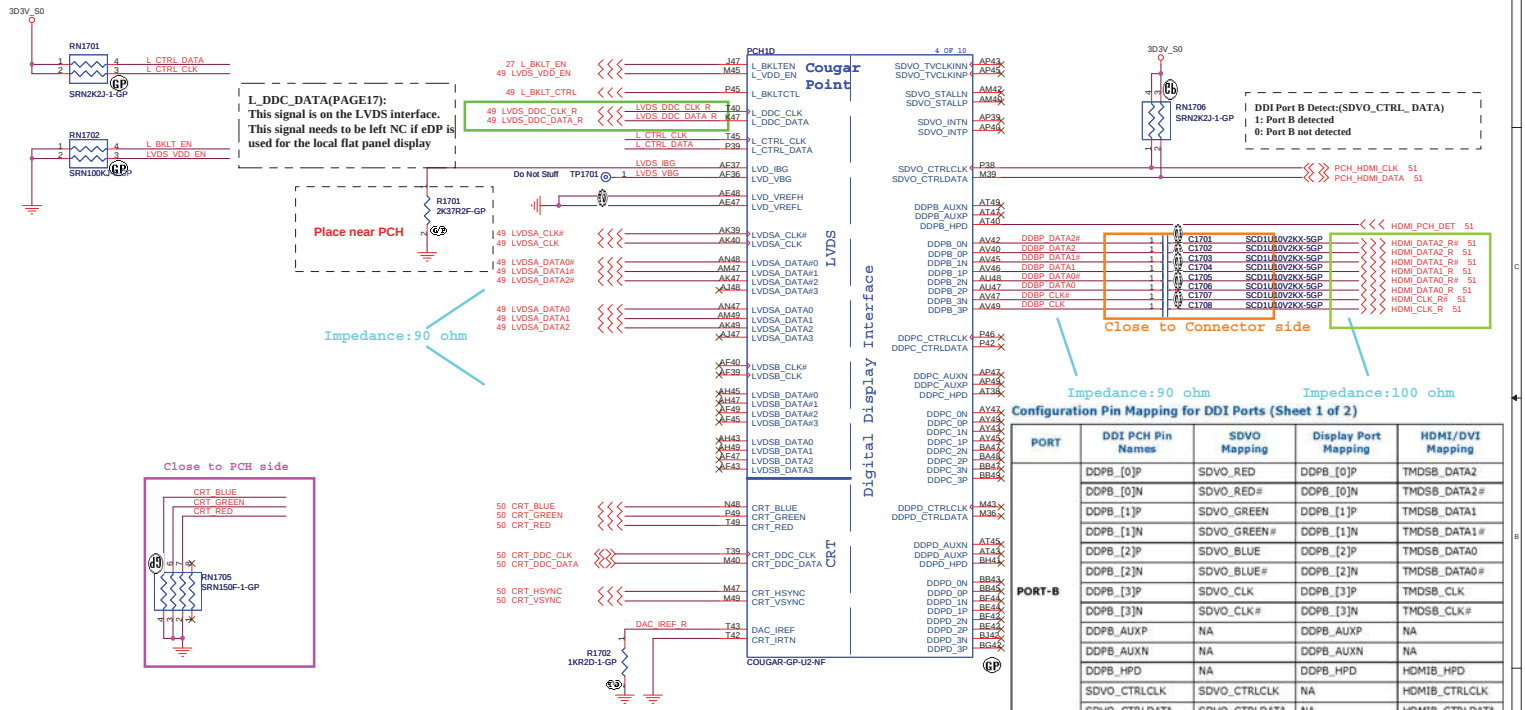
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 15 of 102



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

BOM

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Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 17 of 102

SSID = PCH

20100725 Annie modify

CRB : 2.2K
CEKLT: 1K

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Danbury Technology:
Disabled when Low.
Enable when High.

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	X
1	USB Ext. port 1 (Left Side)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	E-SATA /USB Ext. port 4
9	USB Ext. port 2(CardReader BD
10	USB Ext. port 3(RJ45_BD)
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SW programing USB_OC#12_13 for USB 9

KBC CLK EMI

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

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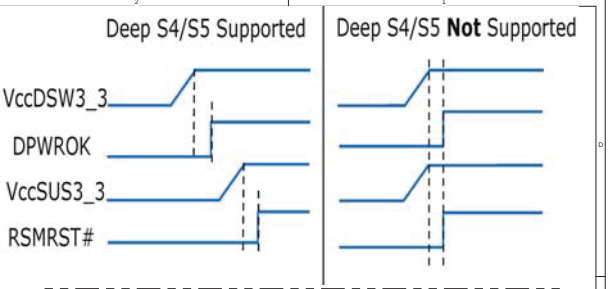
Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: LZ57 | Rev: -1
Date: Tuesday, March 29, 2011 | Sheet 18 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1. VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2. DPWROK and RSMRST# will rise at the same time (connected on board)
3. SLP_SUS# and SUSACK# are left as 'no connect'
4. SUSWARN# used as SUSPWRDNACK/GPIO30

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

PWRBTN#
This signal has an internal pull-up resistor

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

20100729

84.2N702.A3F
2nd = 84.DM601.03F

BOM

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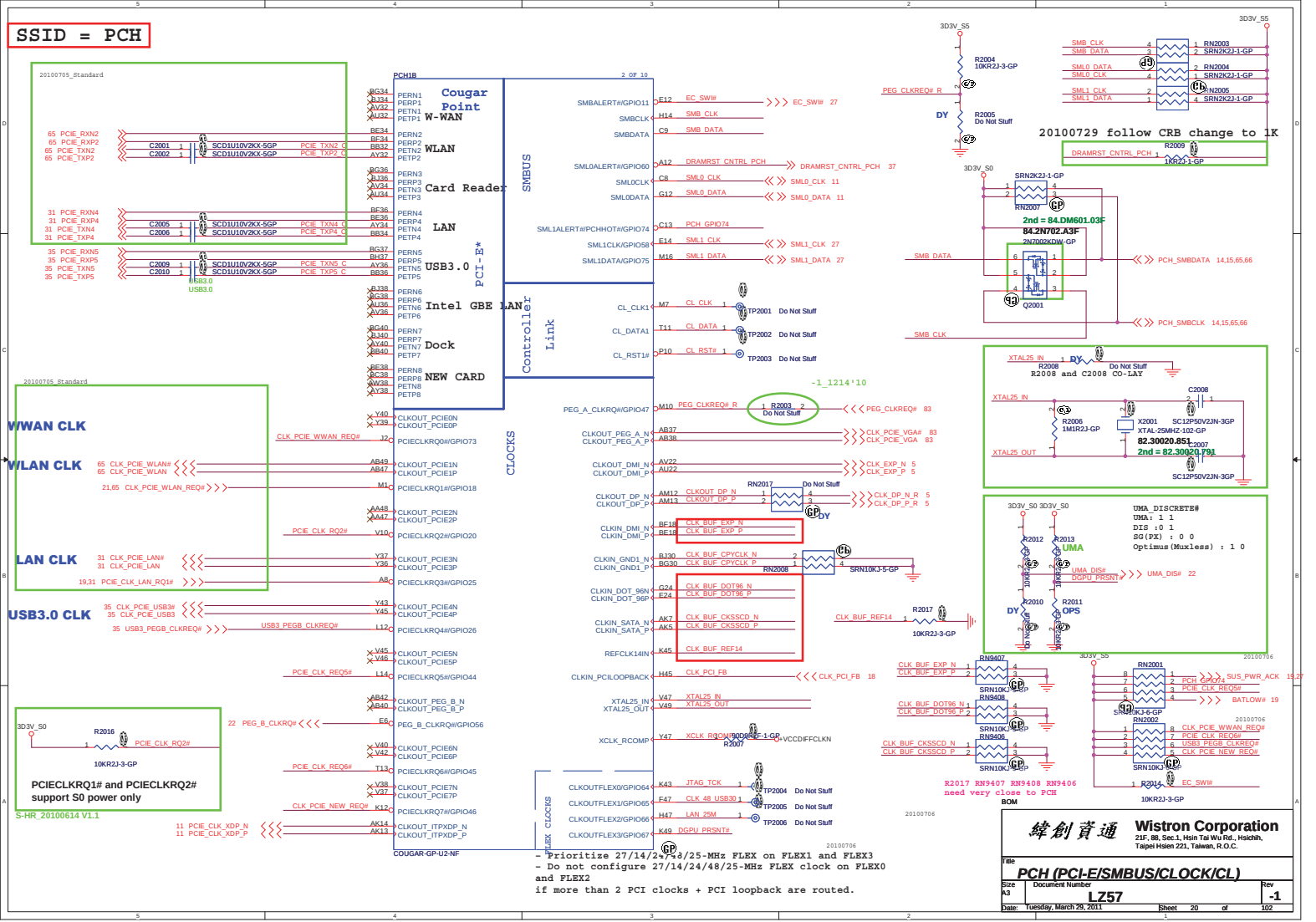
Title: PCH (DM I/FDI/PM)

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 19 of 102

SSID = PCH



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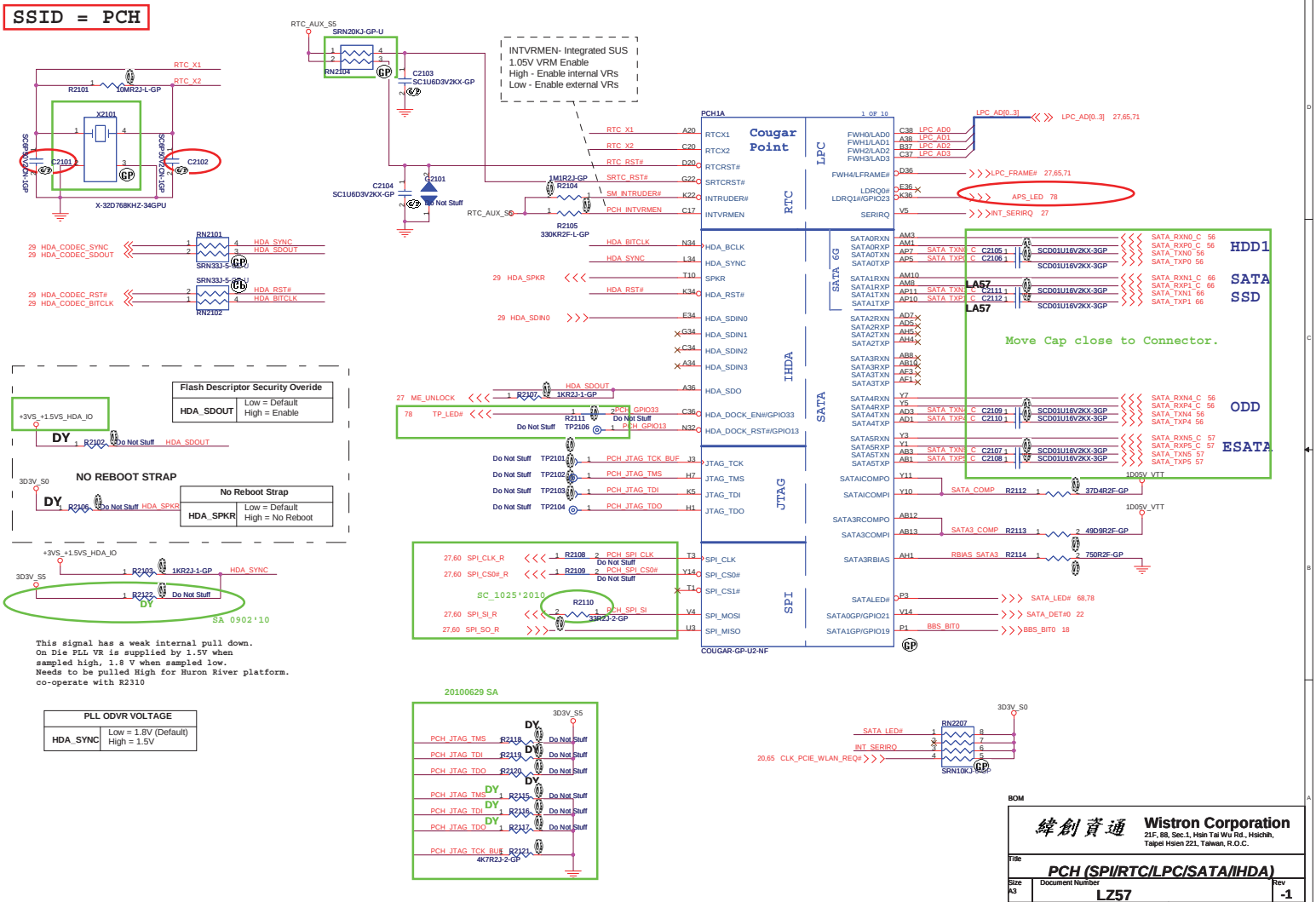
Title	PCH (PCI-E/SMBUS/CLOCK/CL)
Size	A3
Document Number	LZ57
Rev	-1
Date	Tuesday, March 29, 2011
Sheet	20 of 102

SSID = PCH



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH (SPI/RTC/LPC/SATA/IHDA)	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 21 of 102	

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

20100720 SW

SB 0923'10

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

20100729 follow Annie CRB

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

BOM

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Title: PCH (GPIO/CPU)

Size	Document Number	Rev
A3	LZ57	-1

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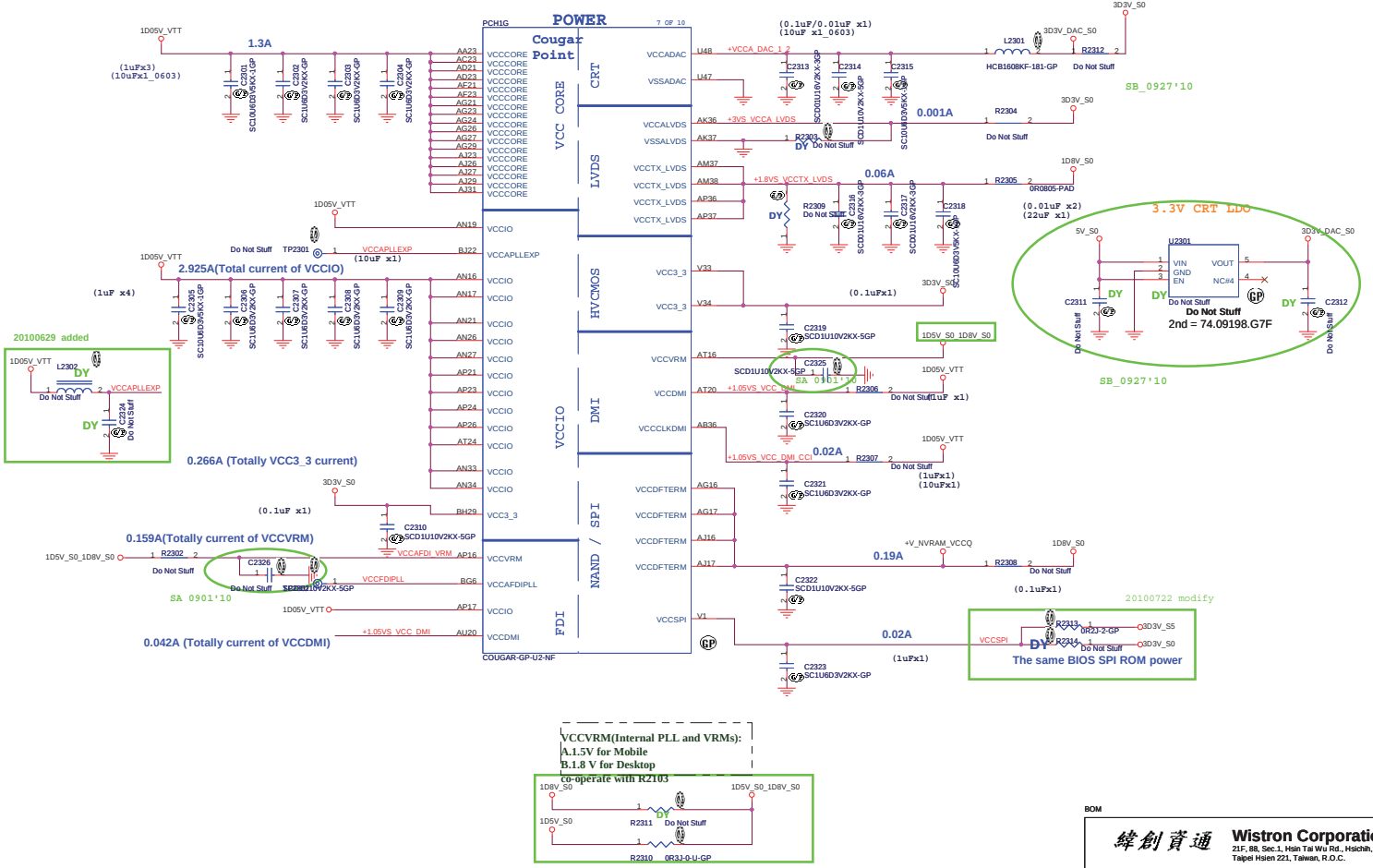
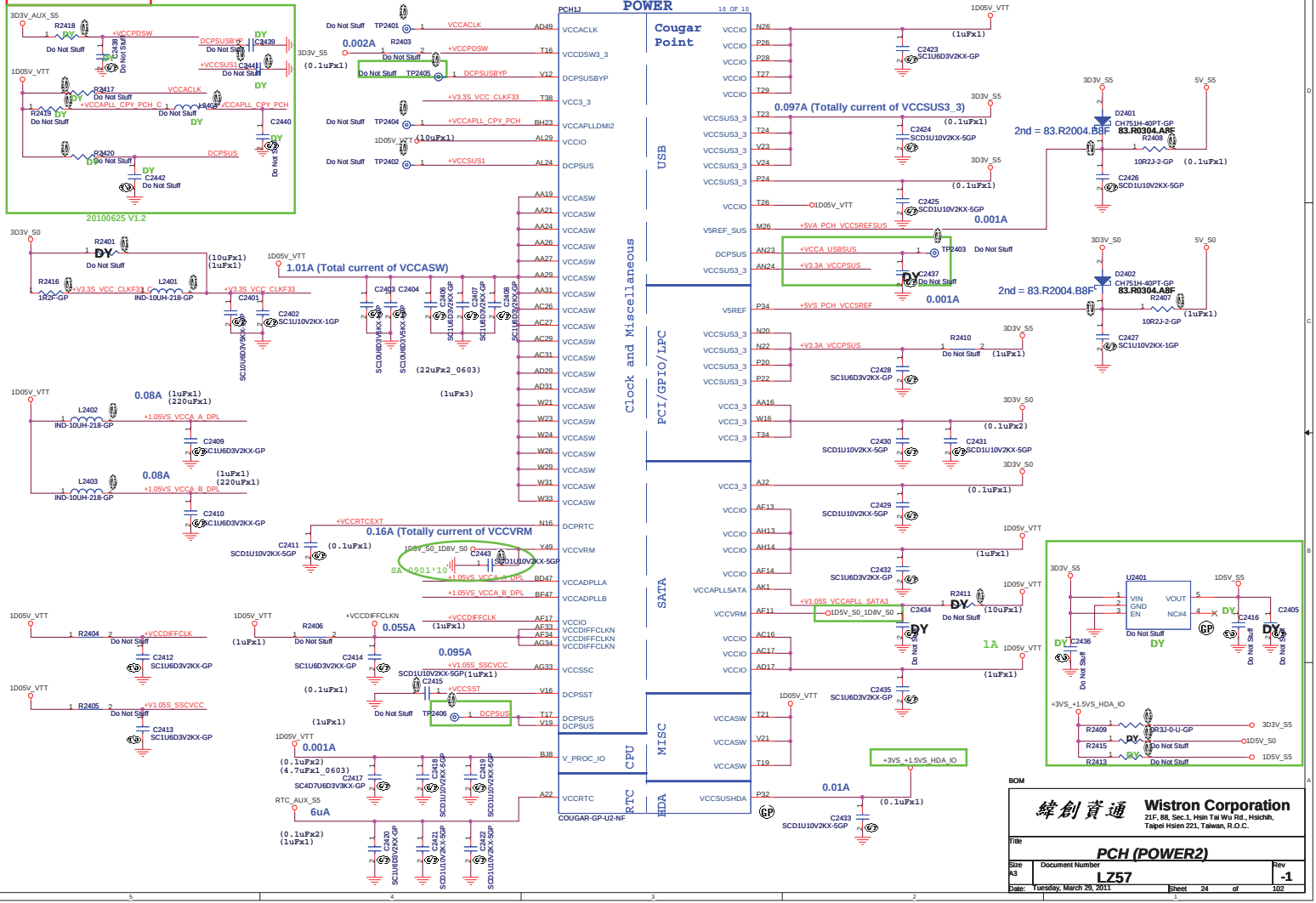
SSID = PCH 6A



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (POWER1)		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 23 of 102	

SSID = PCH


POWER
PCH1J
10 OF 10
Cougar Point
COUGAR-GP-U2-NF
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU MISC
RTC
HDA
0.002A
0.097A (Totally current of VCCSUS3_3)
1.01A (Total current of VCCASW)
0.08A
0.16A (Totally current of VCCVRM)
0.055A
0.095A
0.001A
6uA
0.01A
1A
2nd = 83.R2004.I5F
2nd = 83.R2004.B8F
20100625 V1.2
Do Not Stuff
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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PCH (POWER2)
LZ57
-1
Tuesday, March 29, 2011
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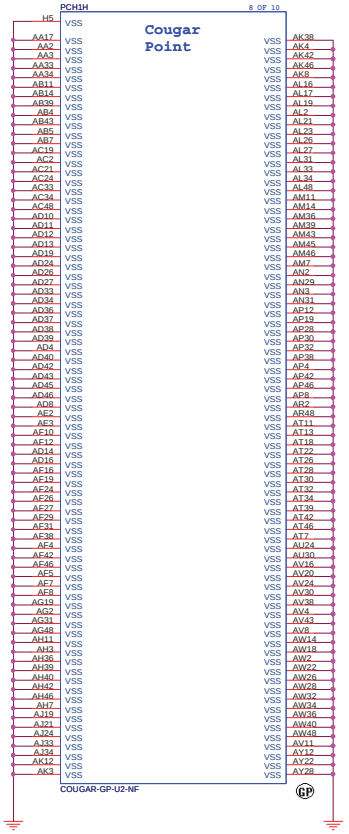
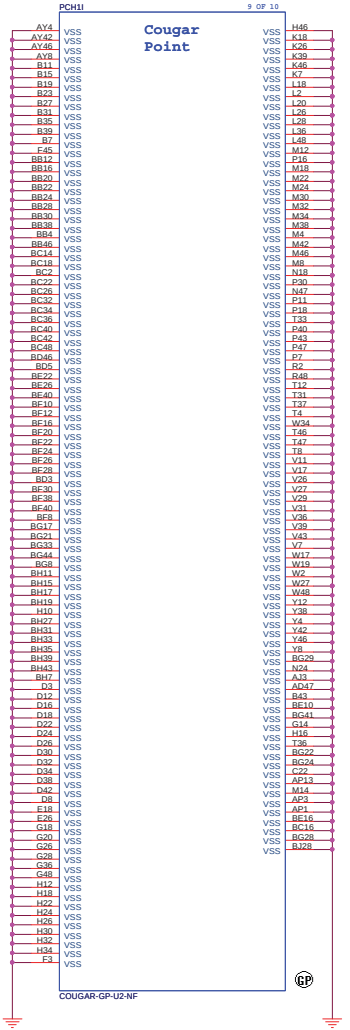
102

SSID = PCH





BOM

緯創資通 **Wistron Corporation**
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Title: **PCH (VSS)**

Size	Document Number	Rev
A3	LZ57	-1

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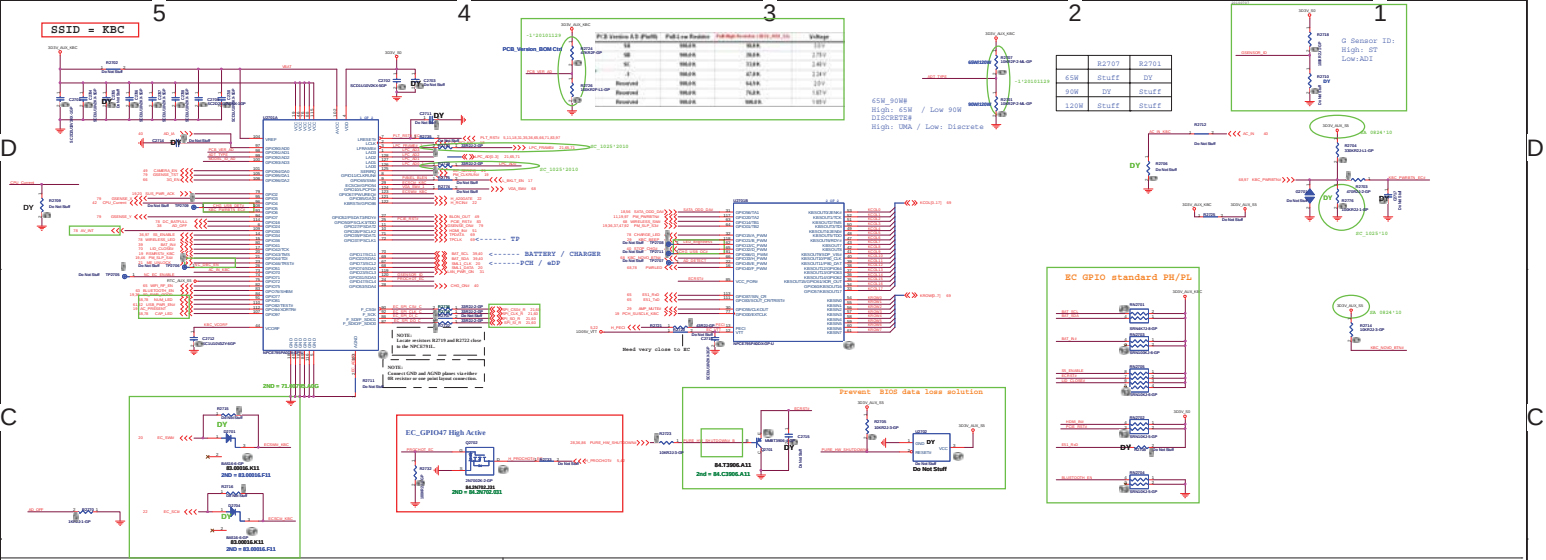


	R2707	R2701
65W	Stuff	DY
90W	DY	Stuff
120W	Stuff	Stuff

PCB Version A3 (Pad5)	Pull-Low Resistor	Pull-High Resistor (3V/3_AUX_S5)	Voltage
L	100.0 K	64.9 K	2.001 V
M	100.0 K	35.7 K	1.751 V
N	100.0 K	73.2 K	2.451 V
I	100.0 K	47.5 K	2.184 V
Reserved	100.0 K	54.9 K	2.01 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

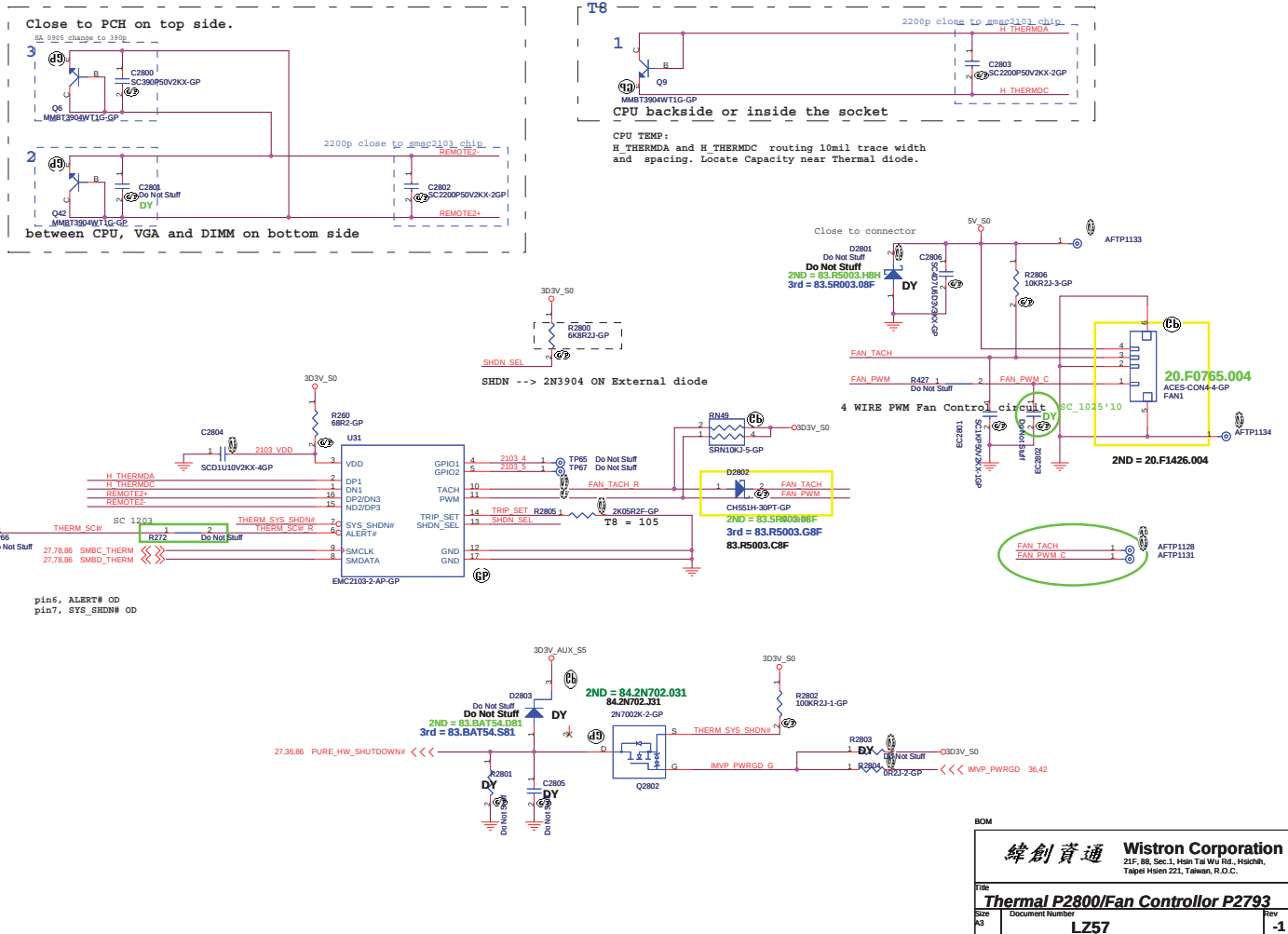
LILI Multi GPIO setting

Model_ID_BOM Ctrl OPS: 64.14335.6DL			
MODEL_ID_AD(Pin100)	Pull-Low Register	Pull-High Register	Voltage
V/W G7 UMA	100.0 K	64.9 K	2.001 V
V/W G7 OPTIMUS	100.0 K	76.8 K	1.867 V
Z G7 UMA	100.0 K	100.0 K	1.650 V
Z G7 OPTIMUS	100.0 K	143.0 K(64.14335.5DL)	1.32 V

Wistron Corporation	KBC Nuvoton NPCE795	
L757		-1

SSID = Thermal

Thermal sensor



BOM

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Title: **Thermal P2800/Fan Controllor P2793**

Size	Document Number	Rev
A3	LZ57	-1

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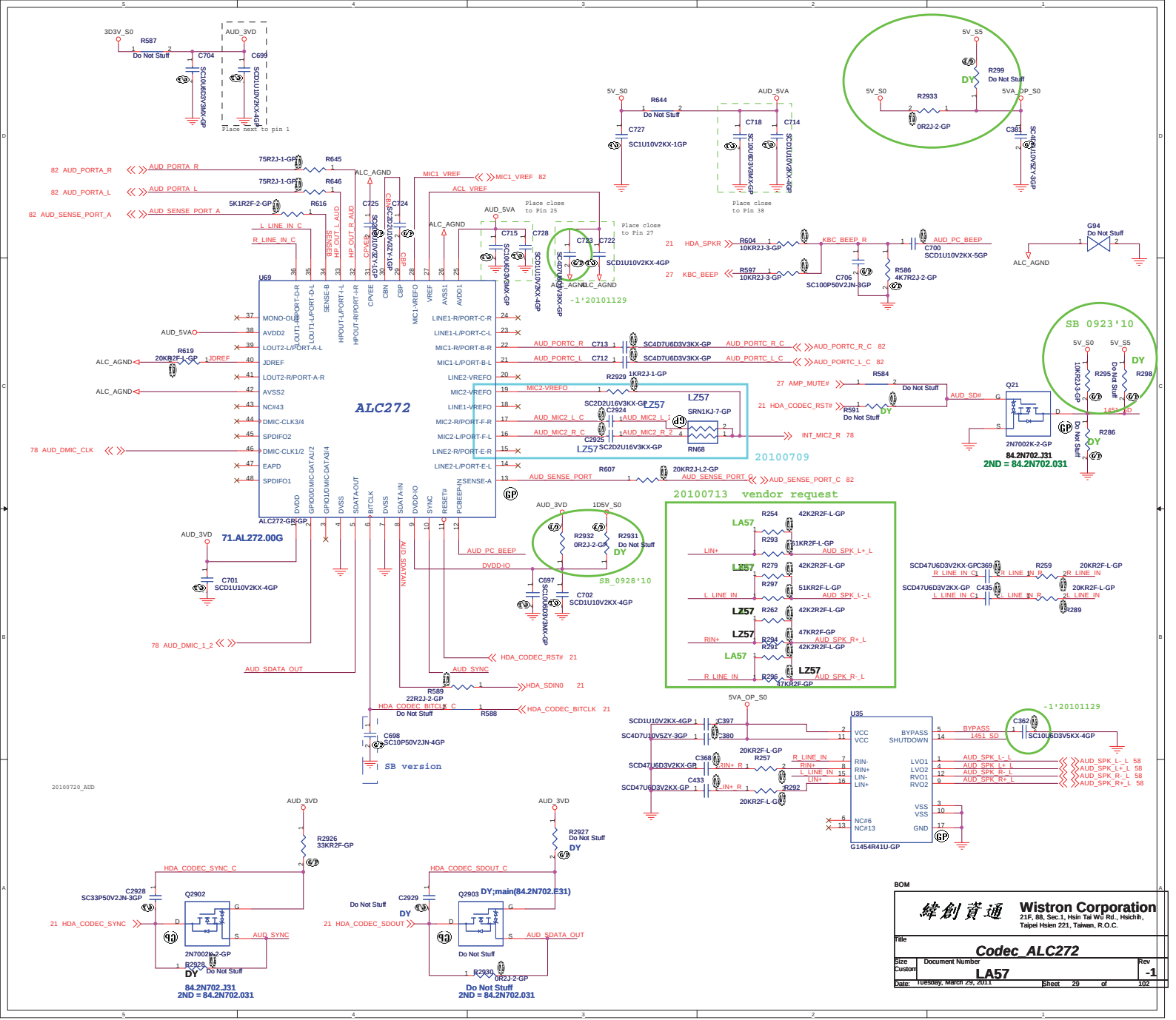
ALC272
71.AL272.00G
20100709
20100713 vendor request
SB 0923'10
SB 0928'10
SB version
Do Not Stuff
DY
Place next to pin 1
Place close to Pin 25
Place close to Pin 27
Place close to Pin 38
-1'20101129
84.2N702.J31
2ND = 84.2N702.031
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Codec_ALC272
LA57
Tuesday, March 29, 2011
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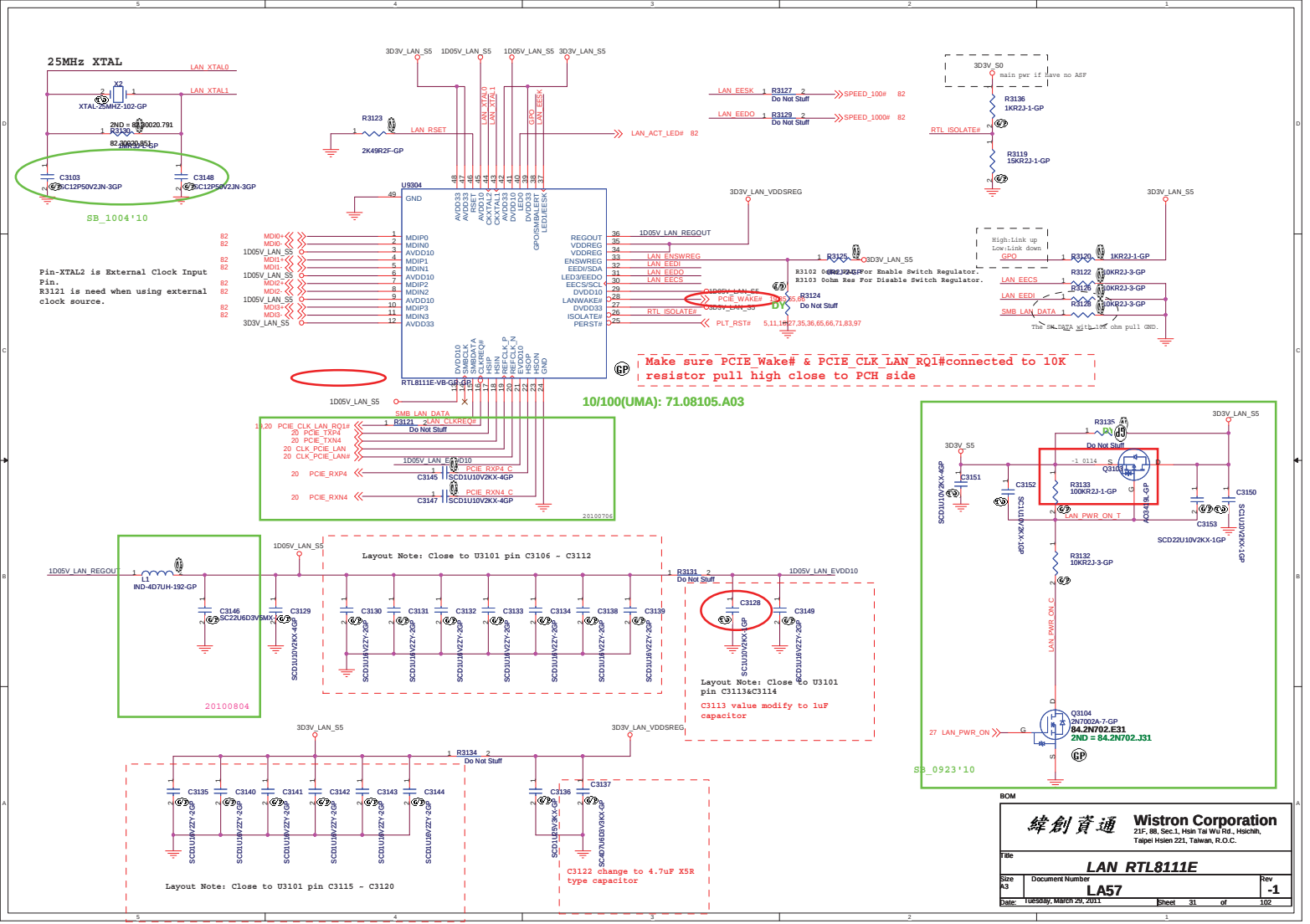
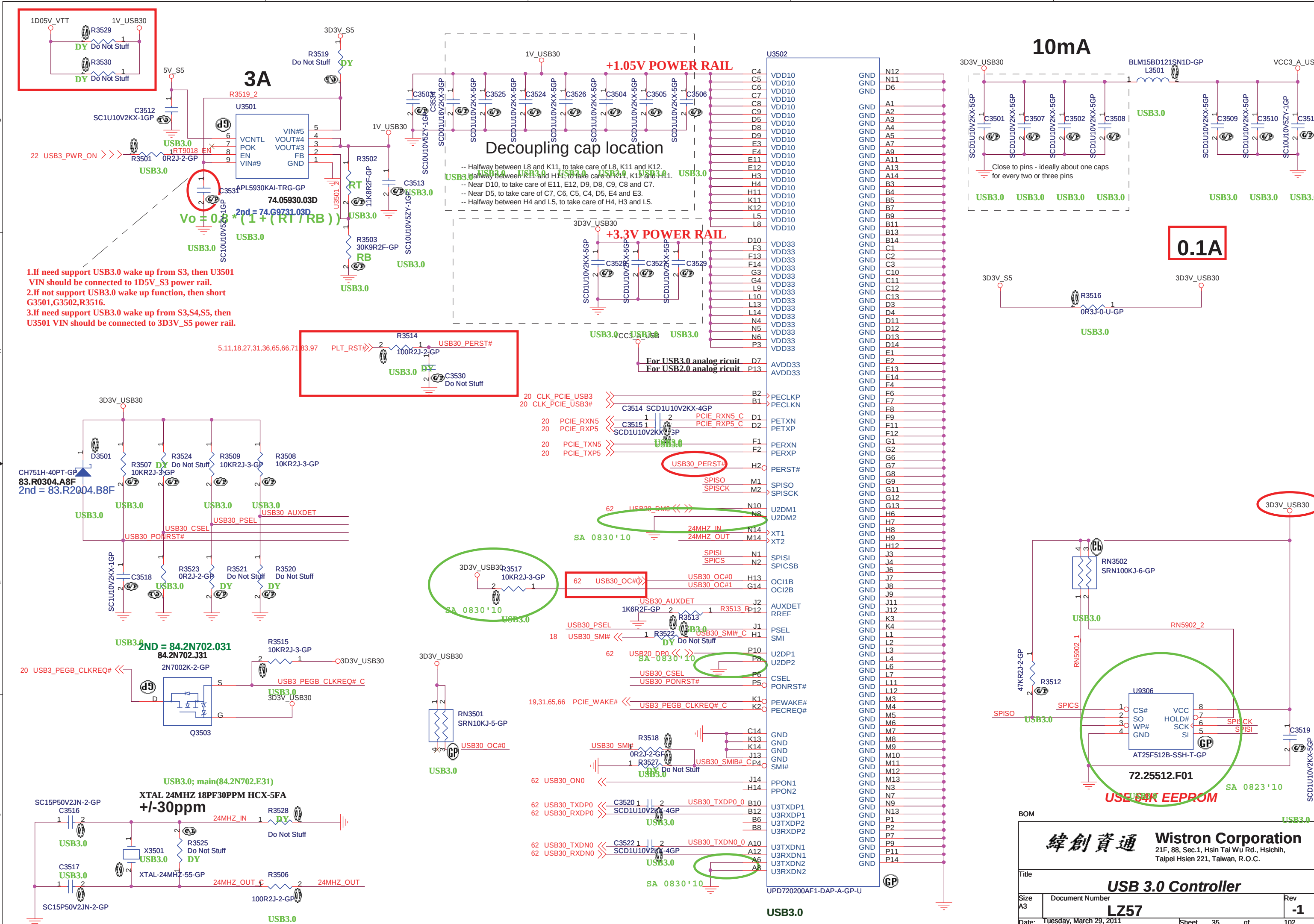


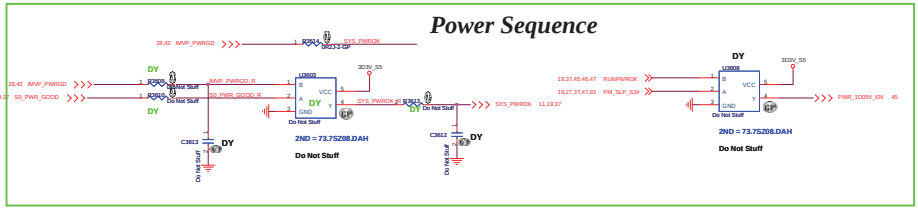
BOM

緯創資通	Wistron Corporation 21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LAN_RTL8111E	
Size: A3	Document Number: LA57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 31 of 102	



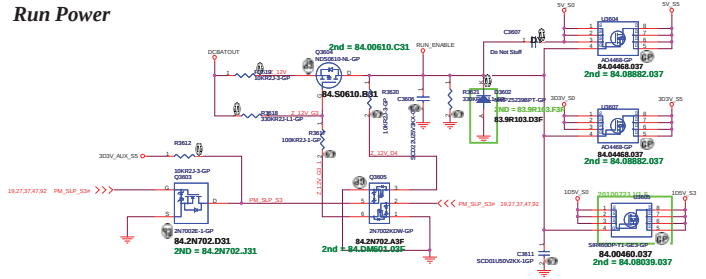
10mA
3A
0.1A
+1.05V POWER RAIL
+3.3V POWER RAIL
Decoupling cap location
-- Halfway between L8 and K11, to take care of L8, K11 and K12.
-- Halfway between K11 and H11, to take care of K11, K12 and H11.
-- Near D10, to take care of E11, E12, D9, D8, C9, C8 and C7.
-- Near D5, to take care of C7, C6, C5, C4, D5, E4 and E3.
-- Halfway between H4 and L5, to take care of H4, H3 and L5.
Close to pins - ideally about one caps for every two or three pins
Vo = 0.8 * (1 + (RT / RB))
1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to 1D5V_S3 power rail.
2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.
3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3D3V_S5 power rail.
For USB3.0 analog ricuit
For USB2.0 analog ricuit
U3501
APL5930KAI-TRG-GP
74.05930.03D
2nd = 74.G9731.03D
U3502
UPD720200AF1-DAP-A-GP-U
U9306
AT25F512B-SSH-T-GP
72.25512.F01
USB 64K EEPROM
XTAL 24MHZ 18PF30PPM HCX-5FA
+/-30ppm
X3501
XTAL-24MHZ-55-GP
Q3503
2N7002K-2-GP
2ND = 84.2N702.031
84.2N702.J31
USB3.0; main(84.2N702.E31)
D3501
CH751H-40PT-GP
83.R0304.A8F
2nd = 83.R2004.B8F
L3501
BLM15BD121SN1D-GP
RN3501
SRN10KJ-5-GP
RN3502
SRN100KJ-6-GP
SA 0830'10
SA 0823'10
1D05V_VTT
1V_USB30
3D3V_S5
5V_S5
3D3V_USB30
VCC3_A_USB
22 USB3_PWR_ON
PLT_RST#
USB30_PERST#
20 CLK_PCIE_USB3
20 CLK_PCIE_USB3#
20 PCIE_RXN5
20 PCIE_RXP5
20 PCIE_TXN5
20 PCIE_TXP5
62 USB20_DM0
24MHZ_IN
24MHZ_OUT
62 USB30_OC#0
USB30_AUXDET
USB30_PSEL
18 USB30_SMI#
62 USB20_DP0
USB30_CSEL
USB30_PONRST#
19,31,65,66 PCIE_WAKE#
USB3_PEGB_CLKREQ#_C
20 USB3_PEGB_CLKREQ#
62 USB30_ON0
62 USB30_TXDP0
62 USB30_RXDP0
62 USB30_TXDN0
62 USB30_RXDN0
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
USB 3.0 Controller
Size A3
Document Number LZ57
Rev -1
Date: Tuesday, March 29, 2011
Sheet 35 of 102

Power Sequence

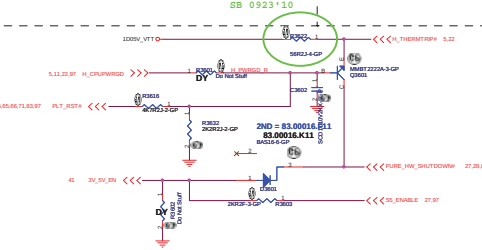


SSID = Reset.Suspend

Run Power



SB 0923'10



BOM

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Title: Power Plane Enable

Size	Document Number	Rev
A2	LZ57	-1

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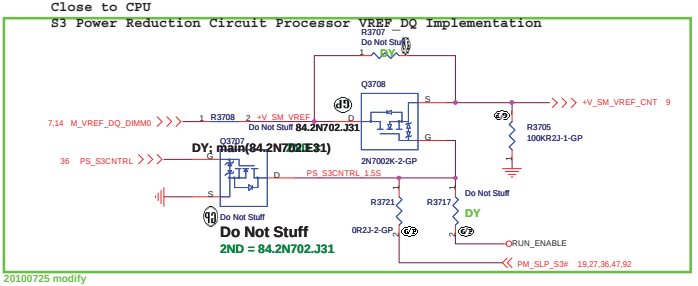
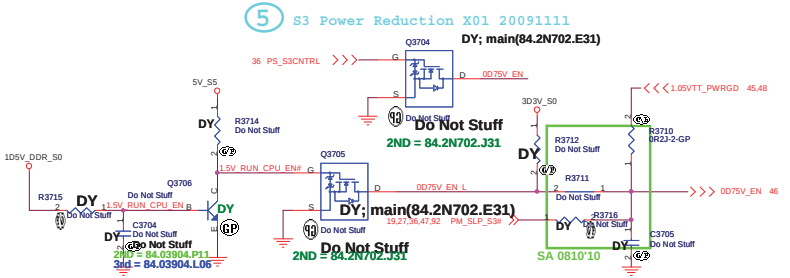
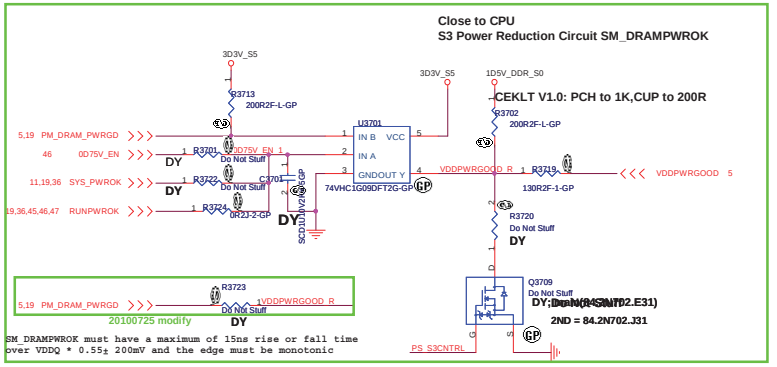
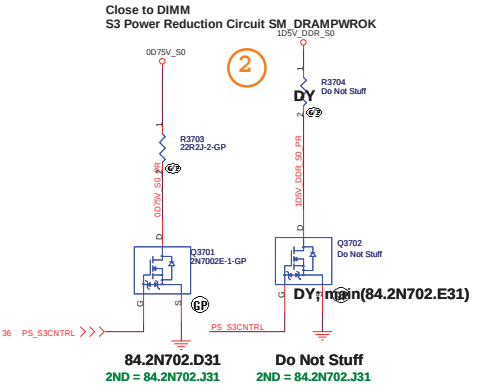
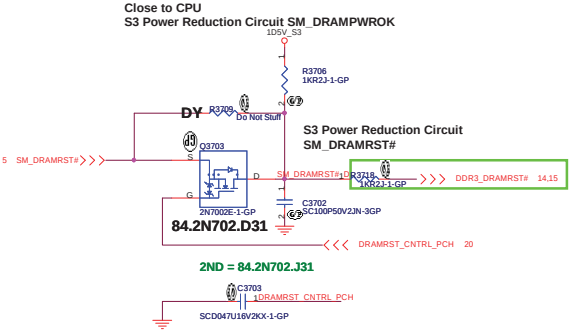










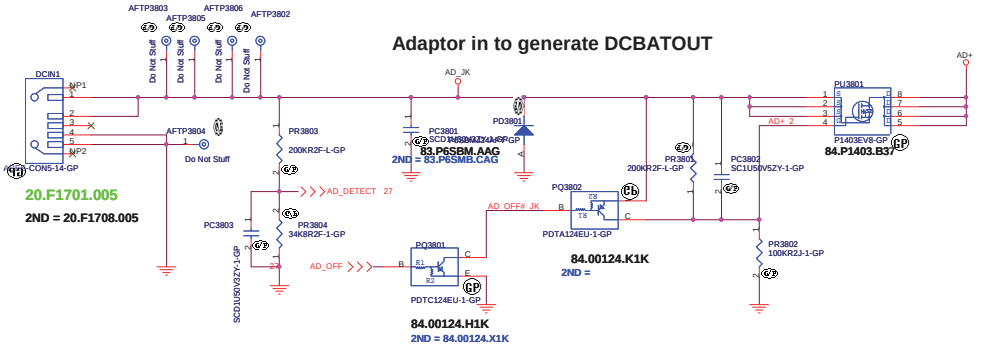
BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADAPTER**

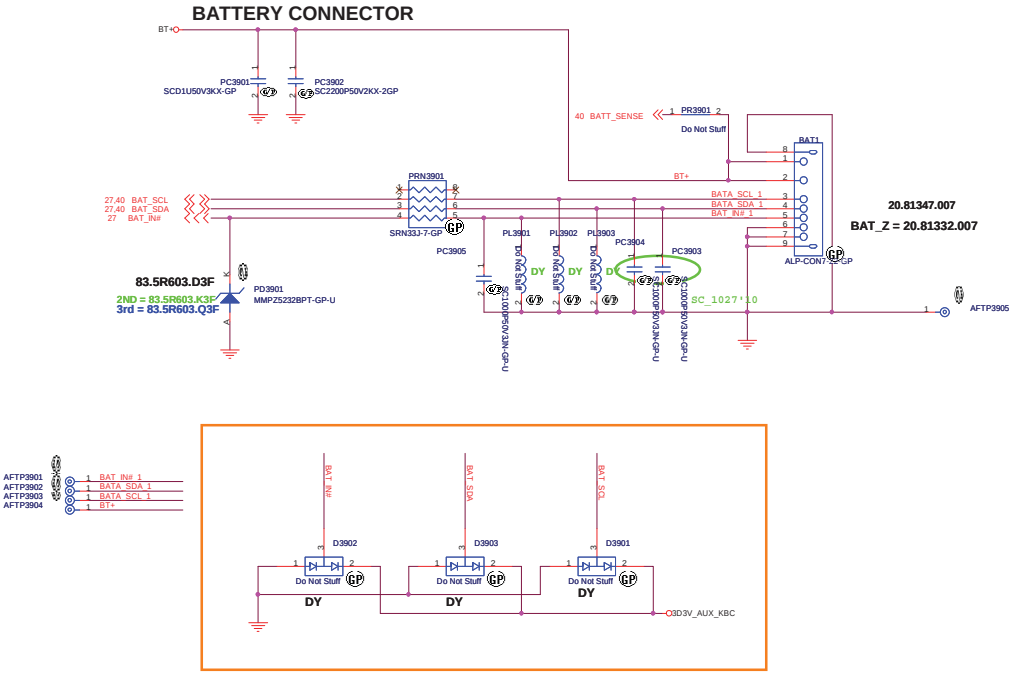
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 37 of 102



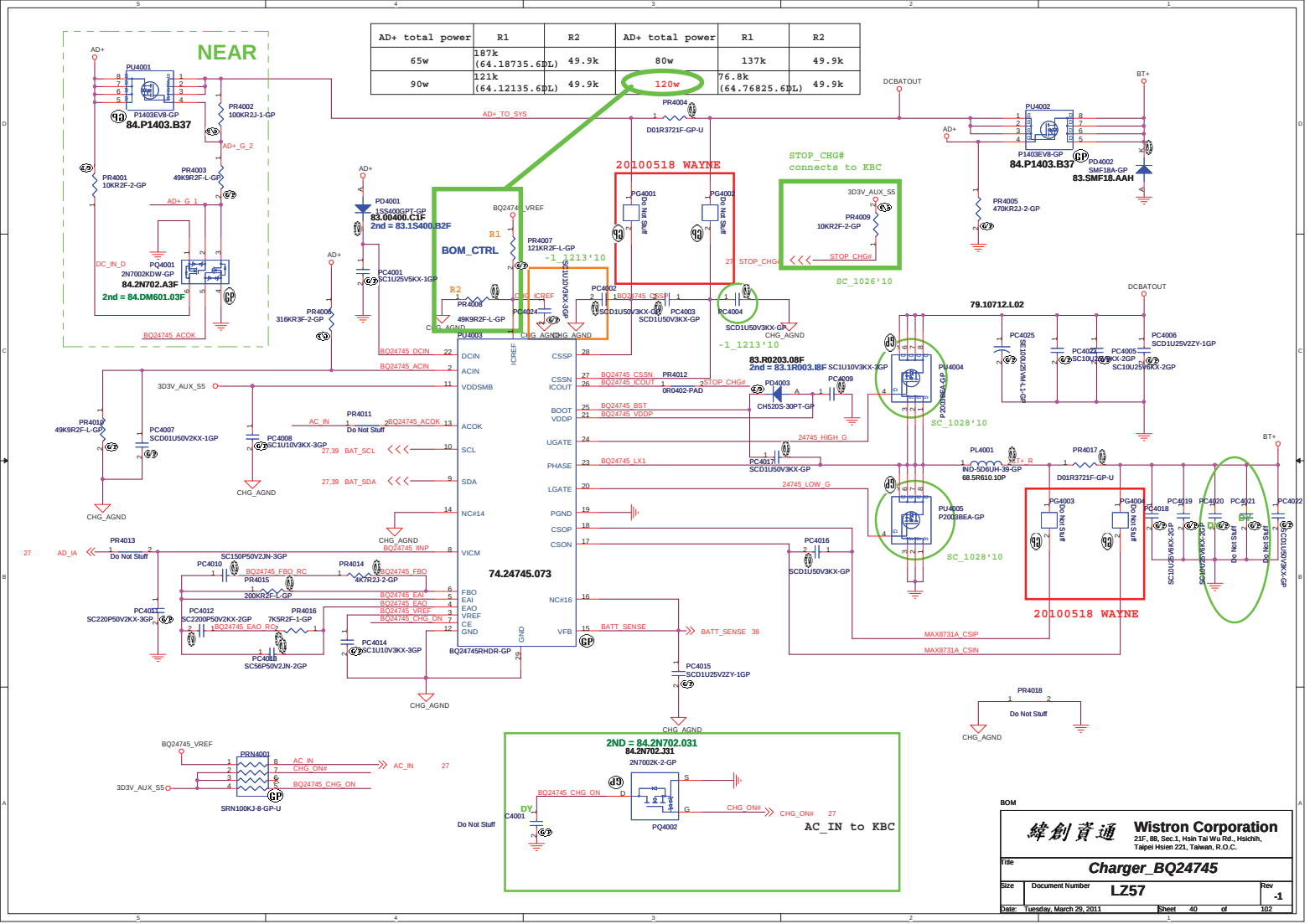
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DCIN_JACK		
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 38 of 102	

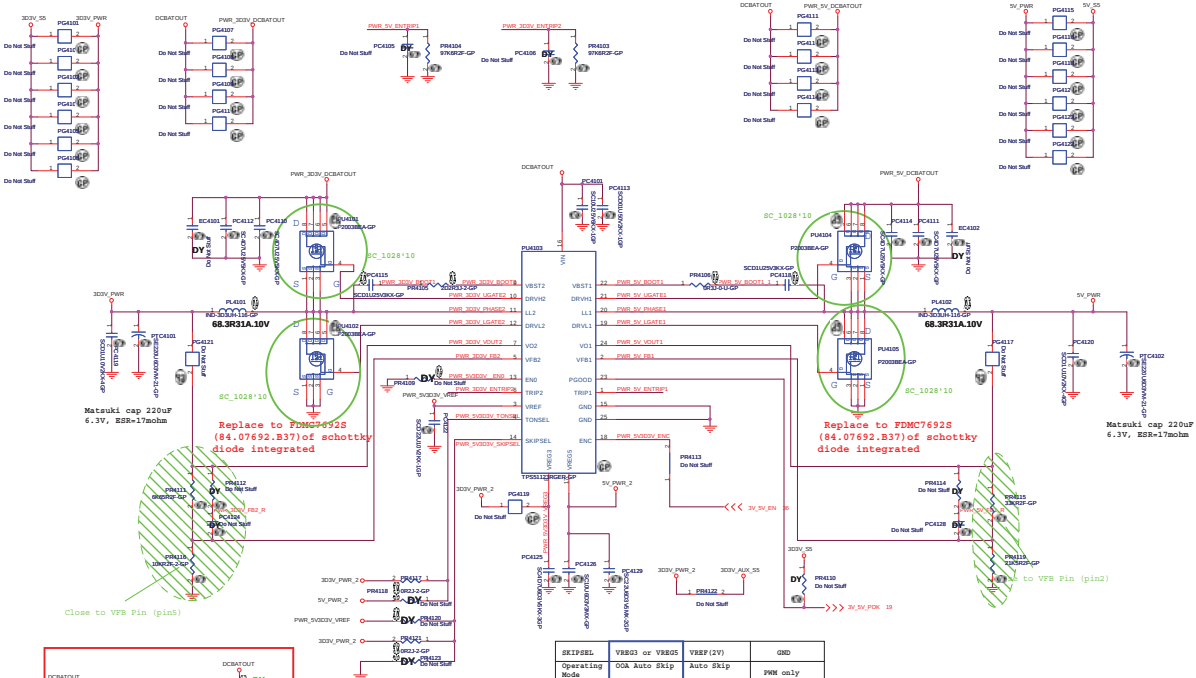


BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BATT_CONN		
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 39 of 102	


NEAR
AD+ total power | R1 | R2 | AD+ total power | R1 | R2
65w | 187k (64.18735.6DL) | 49.9k | 80w | 137k | 49.9k
90w | 121k (64.12135.6DL) | 49.9k | 120w | 76.8k (64.76825.6DL) | 49.9k
20100518 WAYNE
STOP_CHG# connects to KBC
BOM_CTRL
-1_1213'10
83.00400.C1F
2nd = 83.1S400.B2F
84.P1403.B37
83.SMF18.AAH
83.R0203.08F
2nd = 83.1R003.I8F
79.10712.L02
74.24745.073
2ND = 84.2N702.031
84.2N702.J31
AC_IN to KBC
SC_1026'10
SC_1028'10
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Charger_BQ24745
LZ57
Tuesday, March 29, 2011

SSID = PWR.Plane.Regulator_5v3p3v



SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

BOM

Wistron Corporation
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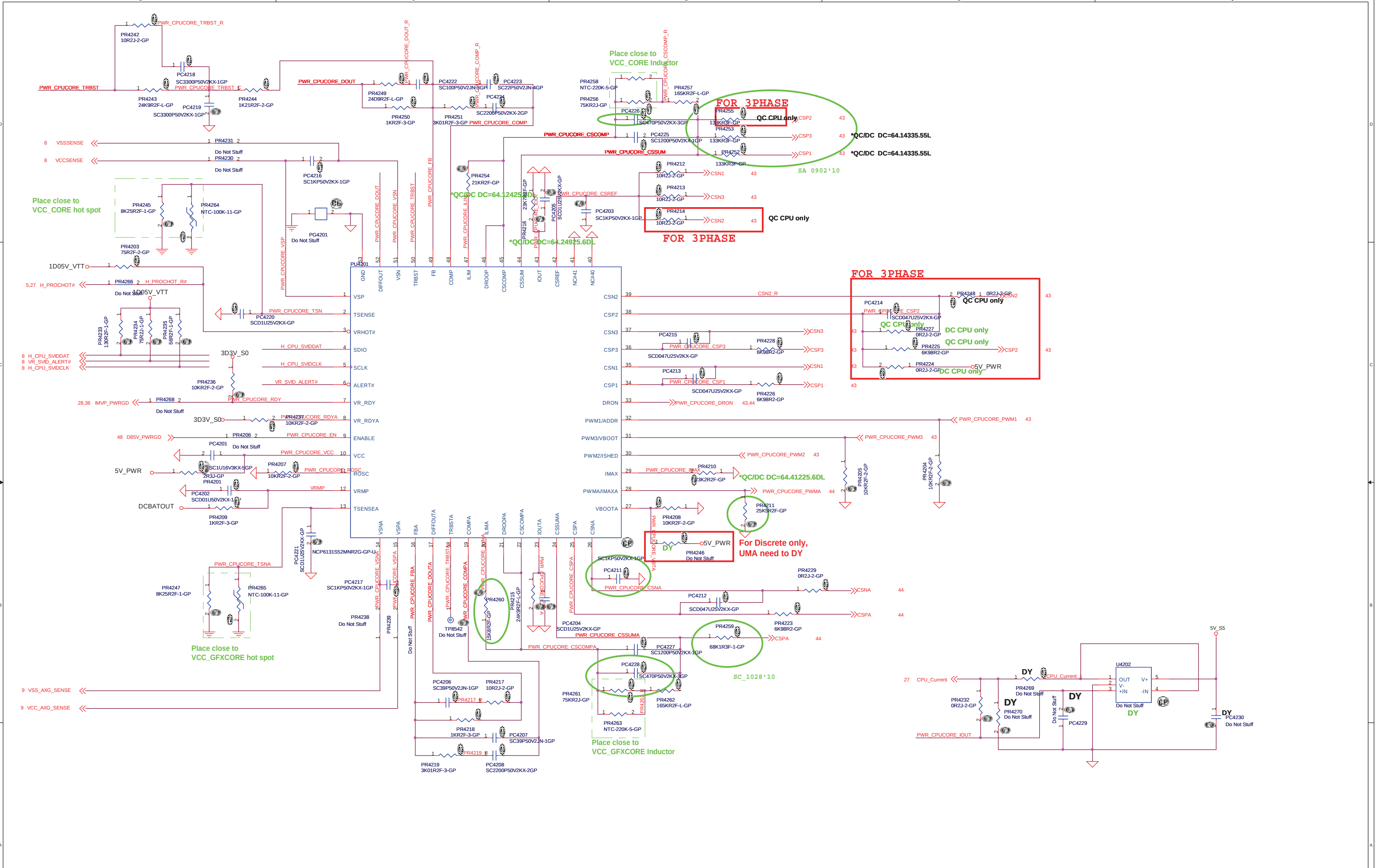
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 3D3V5V

Size	Document Number	Rev
	LZ57	-1

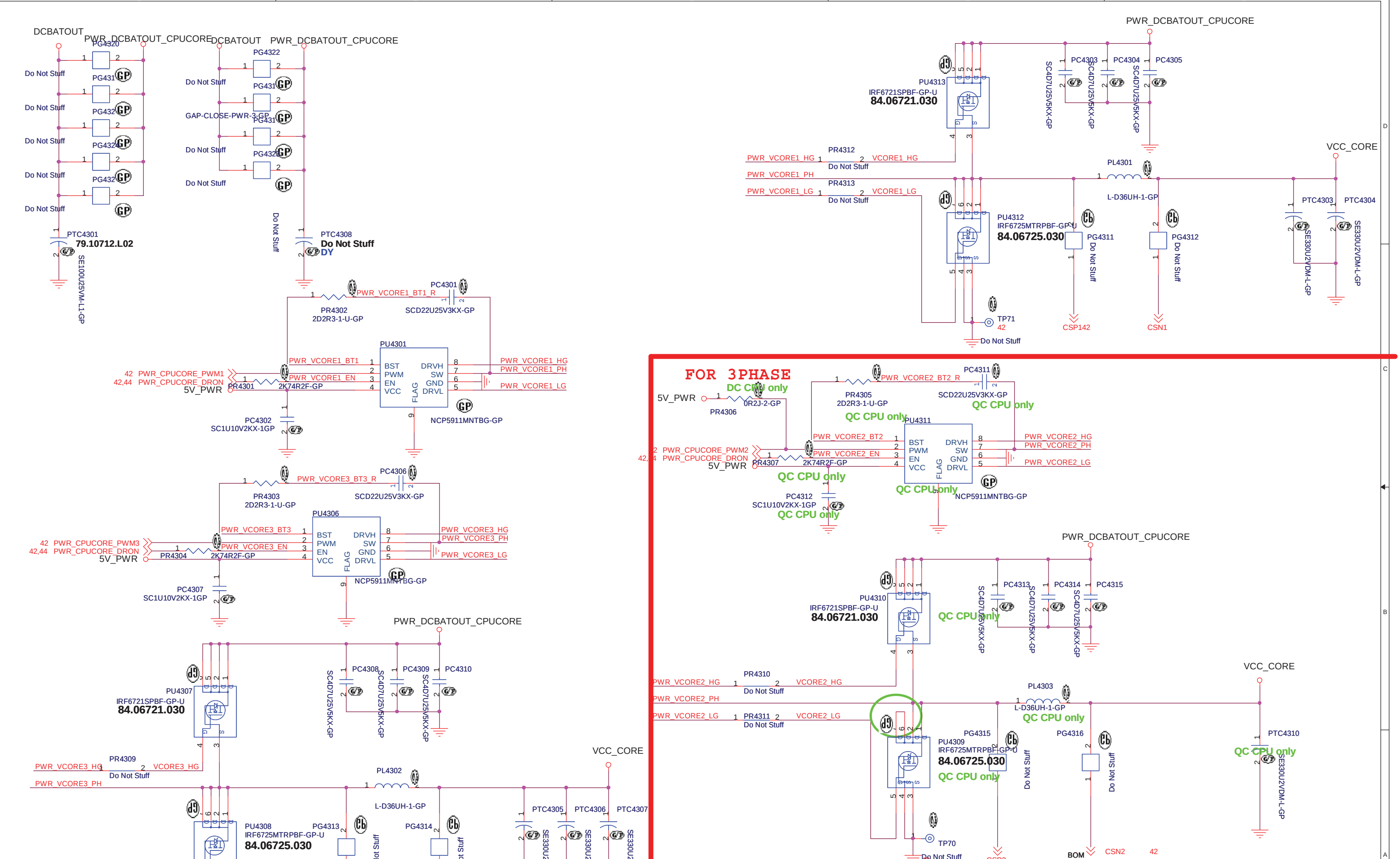
Date: Tuesday, March 29, 2011 Sheet 41 of 102



BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	DC/DC CPU CORE1 _NCP6131		
Size	Document Number: LZ57		Rev: -1
Date: Thursday, March 31, 2011	Sheet 42 of 102		

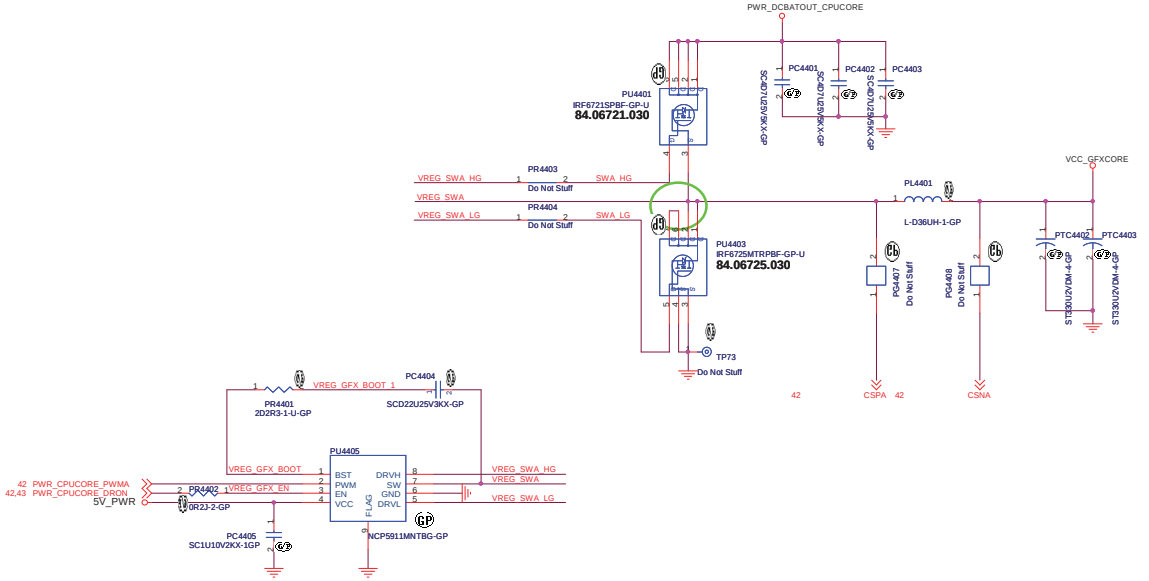


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
DC/DC CPU CORE2 _NCP6131

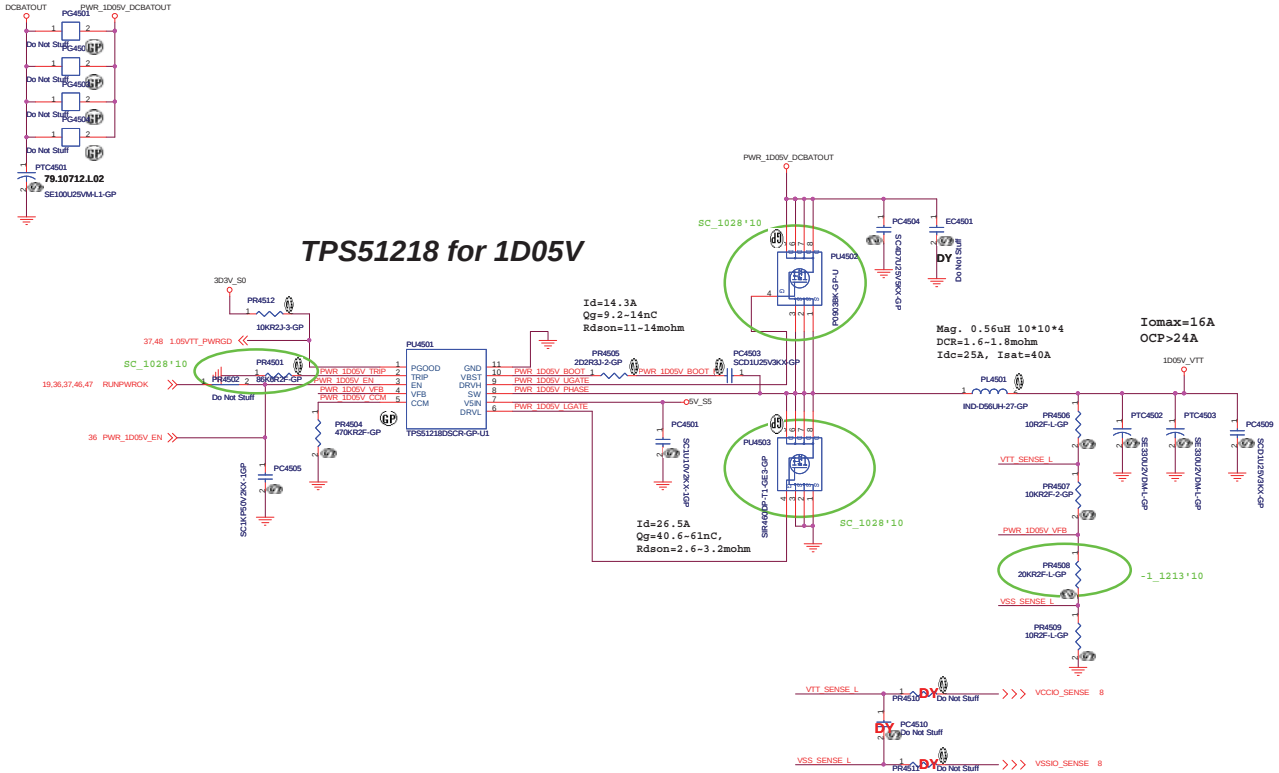
Size | Document Number **LZ57** | Rev **-1**

Date: Tuesday, March 29, 2011 | Sheet 43 of 102



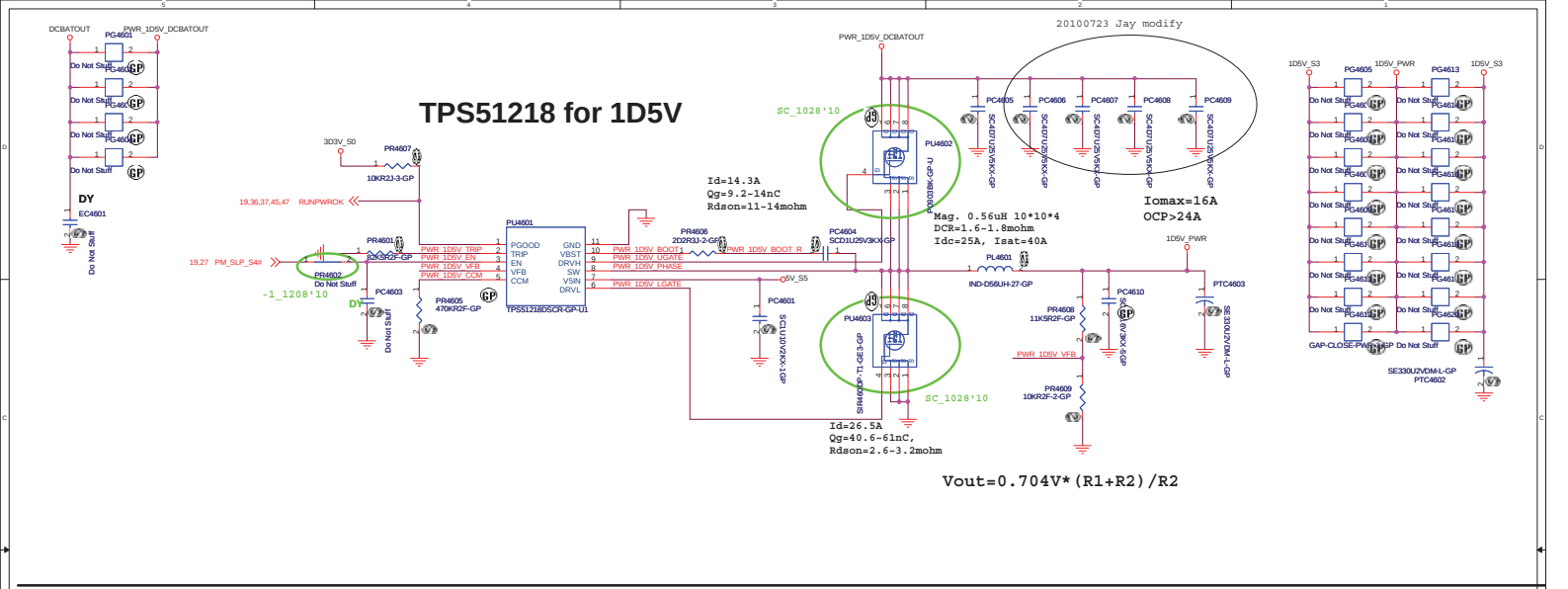
BOM

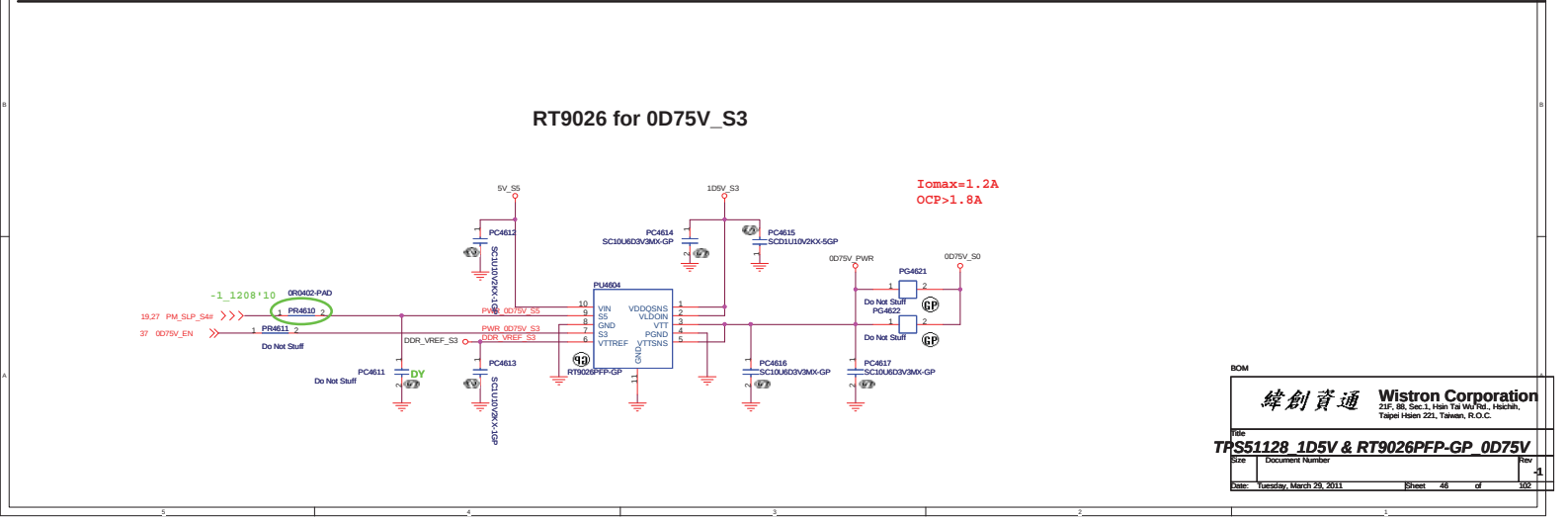
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DC/DC CPU CORE3 _NCP6131***	
Size	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 44 of 102	



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***TPS51218_1D05V***	
Size	Document Number	Rev -1
Date: Tuesday, March 29, 2011	Sheet 45 of 102	





BOM

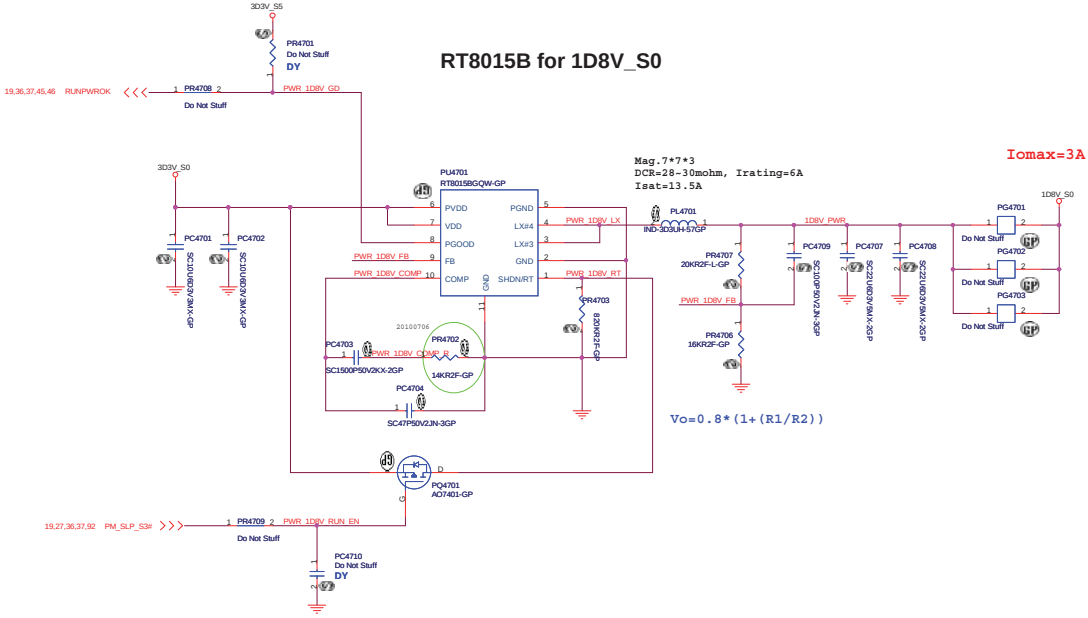
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51128_1D5V & RT9026PFP-GP_0D75V

Size	Document Number	Rev
		-1

Date: Tuesday, March 29, 2011 Sheet 46 of 102

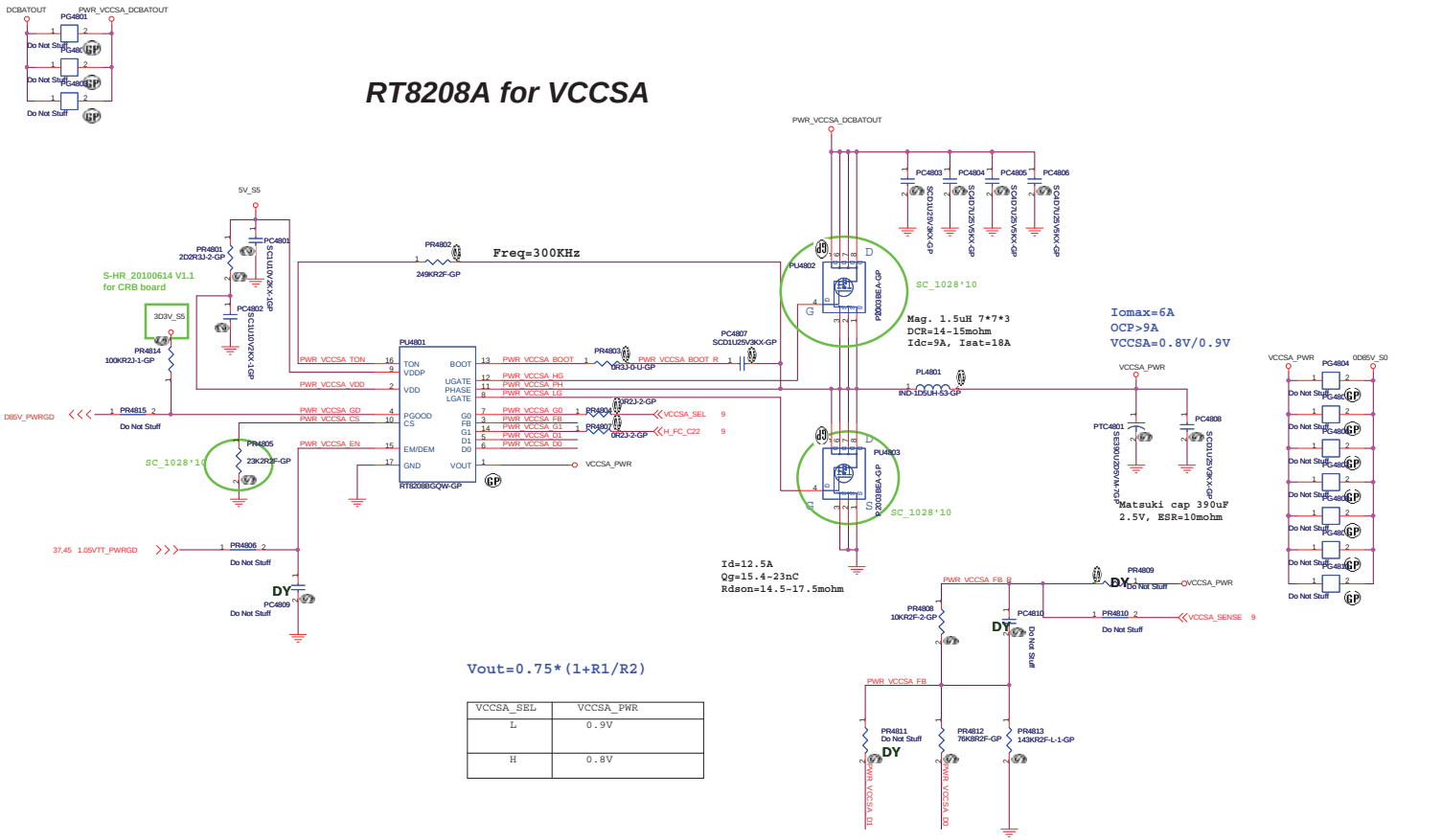
RT9025 for 1D8V_S0



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D8V_RT9025		
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 47 of 102	

RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

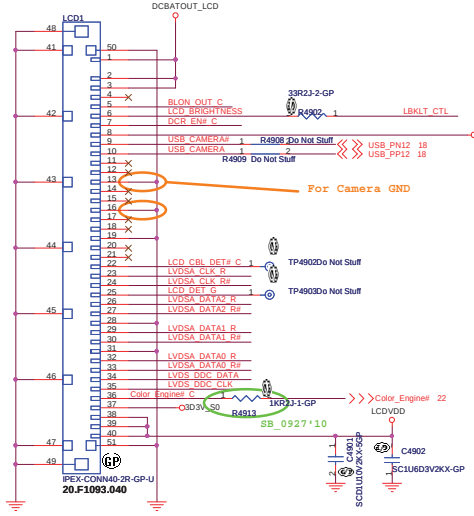
BOM

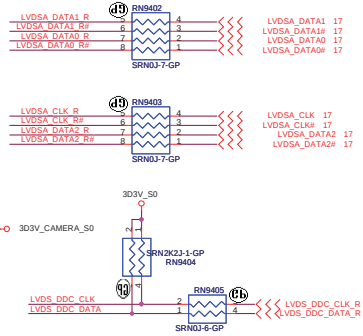
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8208B_VCCSA	
Size	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 48 of 102	

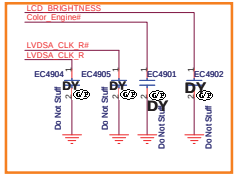
SSID = VIDEO

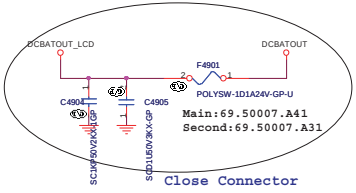
LVDS CONNECTOR

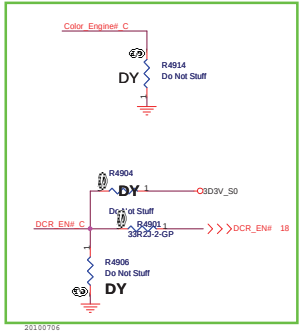




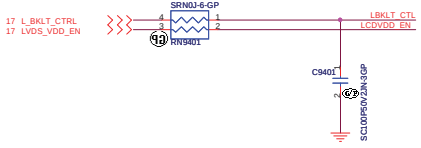
For EMI request
Close to LVDS connector



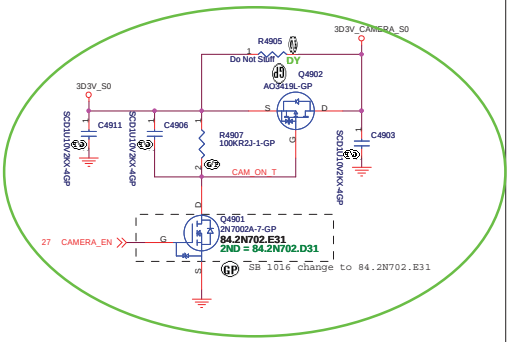




Panel BL brightness/Power En/BL En

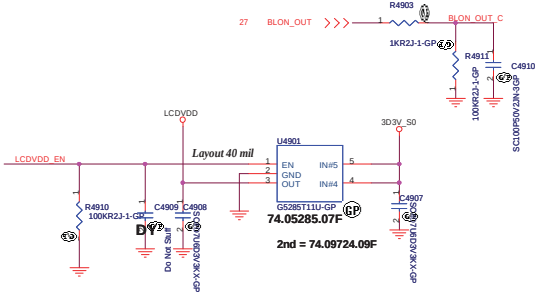


CAMERA POWER



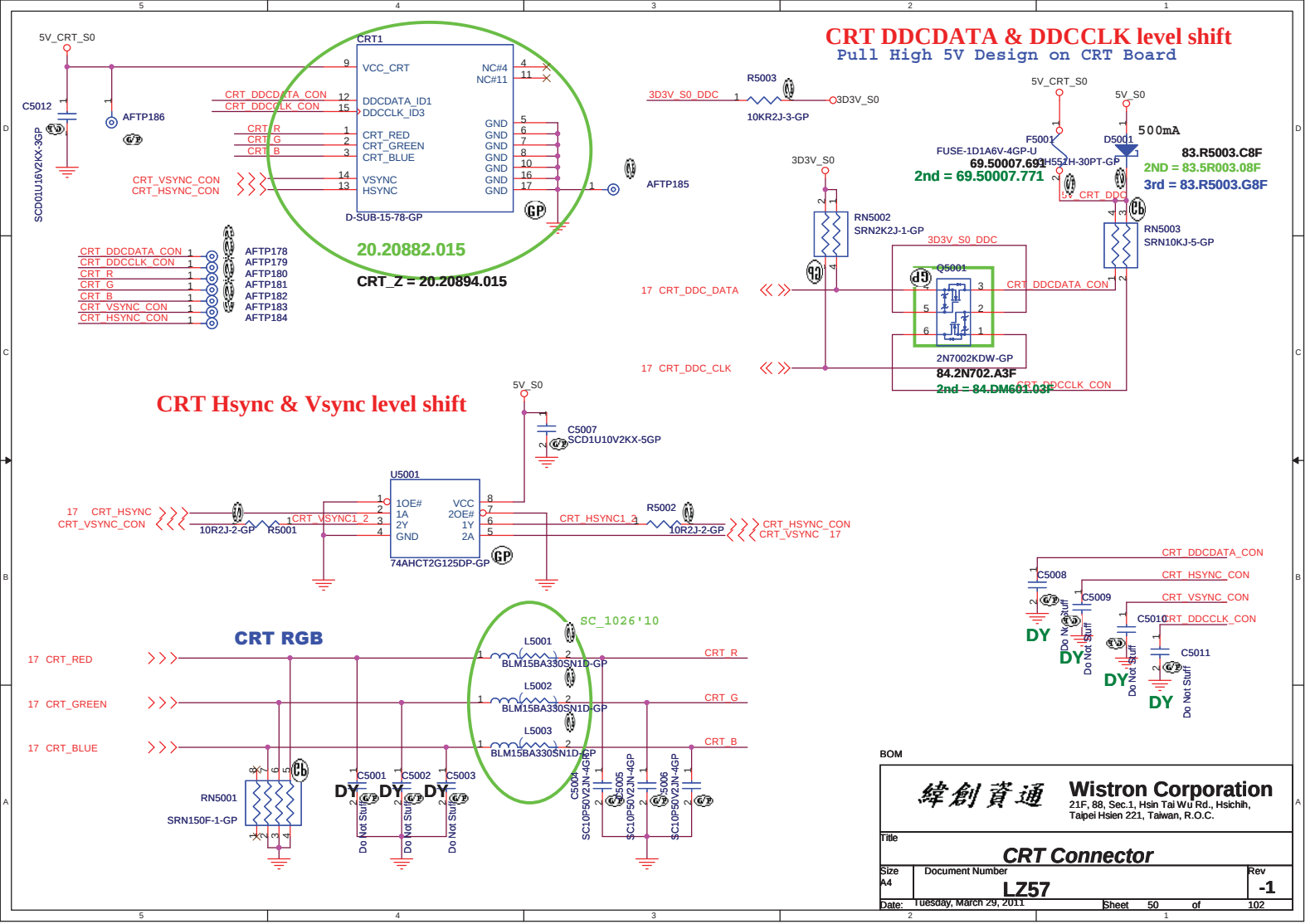
SB 0923'10

SSID = VIDEO



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD Connector		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 49 of 102	

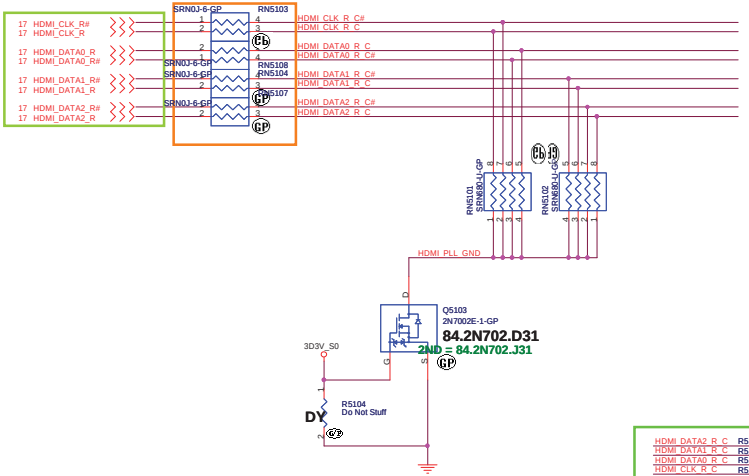

CRT DDCDATA & DDCCLK level shift
Pull High 5V Design on CRT Board
CRT Hsync & Vsync level shift
CRT RGB
5V_CRT_S0
CRT1
VCC_CRT
NC#4
NC#11
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
GND
D-SUB-15-78-GP
C5012
AFTP186
AFTP185
SCD01U16V2KX-3GP
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_R
CRT_G
CRT_B
CRT_VSYNC_CON
CRT_HSYNC_CON
AFTP178
AFTP179
AFTP180
AFTP181
AFTP182
AFTP183
AFTP184
20.20882.015
CRT_Z = 20.20894.015
3D3V_S0_DDC
3D3V_S0
R5003
10KR2J-3-GP
F5001
FUSE-1D1A6V-4GP-U
D5001
CH552H-30PT-GP
500mA
69.50007.691
2nd = 69.50007.771
83.R5003.C8F
2ND = 83.5R003.08F
3rd = 83.R5003.G8F
RN5002
SRN2K2J-1-GP
RN5003
SRN10KJ-5-GP
Q5001
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
17 CRT_DDC_DATA
17 CRT_DDC_CLK
C5007
SCD1U10V2KX-5GP
U5001
74AHCT2G125DP-GP
1OE#
1A
2Y
GND
VCC
2OE#
1Y
2A
17 CRT_HSYNC
CRT_VSYNC_CON
10R2J-2-GP
R5001
R5002
CRT_HSYNC_CON
CRT_VSYNC 17
SC_1026'10
L5001
L5002
L5003
BLM15BA330SN1D-GP
17 CRT_RED
17 CRT_GREEN
17 CRT_BLUE
RN5001
SRN150F-1-GP
C5001
C5002
C5003
C5004
C5005
C5006
SC10P50V2JN-4GP
Do Not Stuff
DY
C5008
C5009
C5010
C5011
CRT_DDCDATA_CON
CRT_HSYNC_CON
CRT_VSYNC_CON
CRT_DDCCLK_CON
BOM
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT Connector
Size
A4
Document Number
LZ57
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 50 of 102

SSID = VIDEO

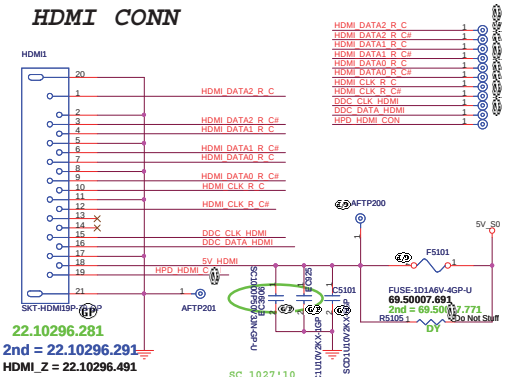
HDMI CONNECTOR

HDMI Passive Level Shifter

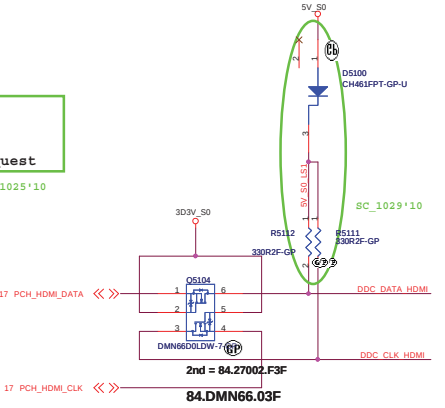
Close to HDMI Connector



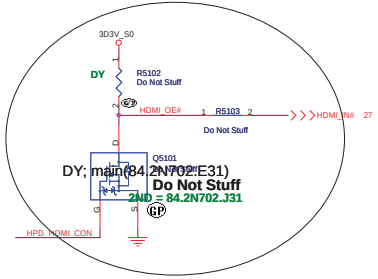
HDMI CONN



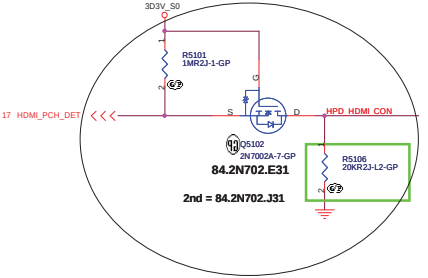
HDMI DDC Passive Level Shifter



20100727 modify, KBC isn't use.



20100727 follow intel design guide



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

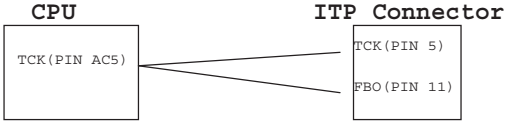
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 51 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP

Size: A4 | Document Number: LZ57 | Rev: -1

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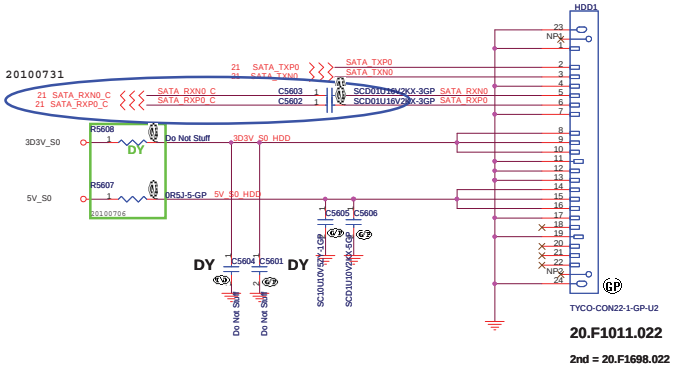
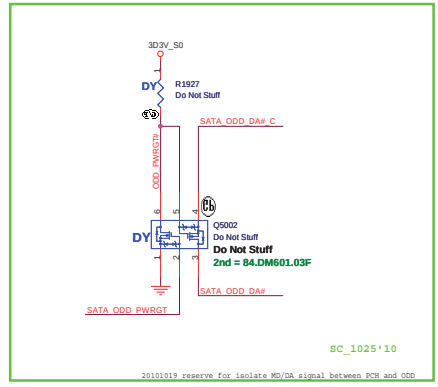
SSID = SATA

SATA HDD Connector

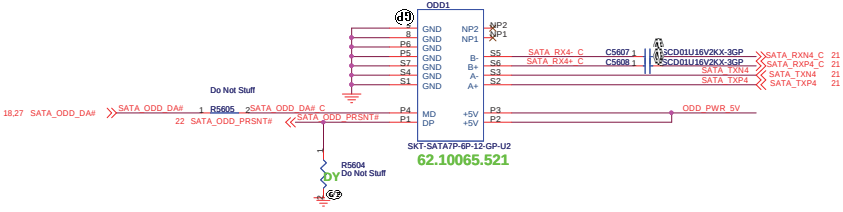


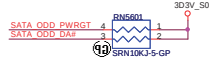


ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

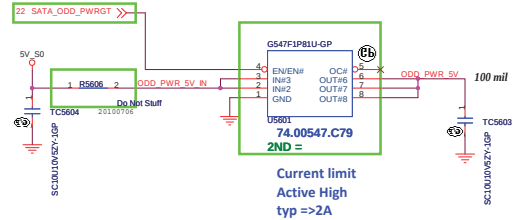
Mars:
Exchange ODD and ESATA differential pair each other.





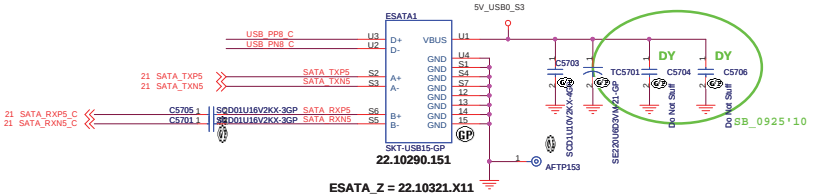
SUPPORT ZERO SATA ODD

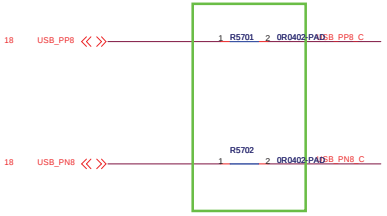
SATA Zero Power ODD

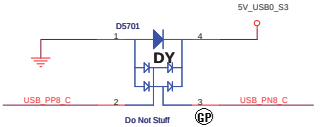


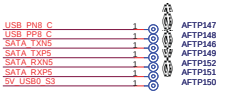
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 56 of 102	





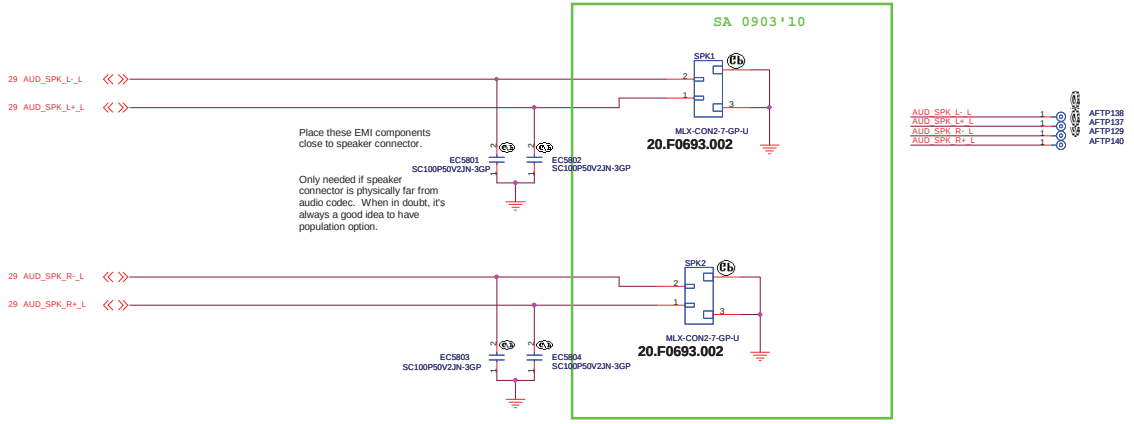




BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	E-SATA/USB	
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 57 of 102	

INTERNAL STEREO SPEAKERS

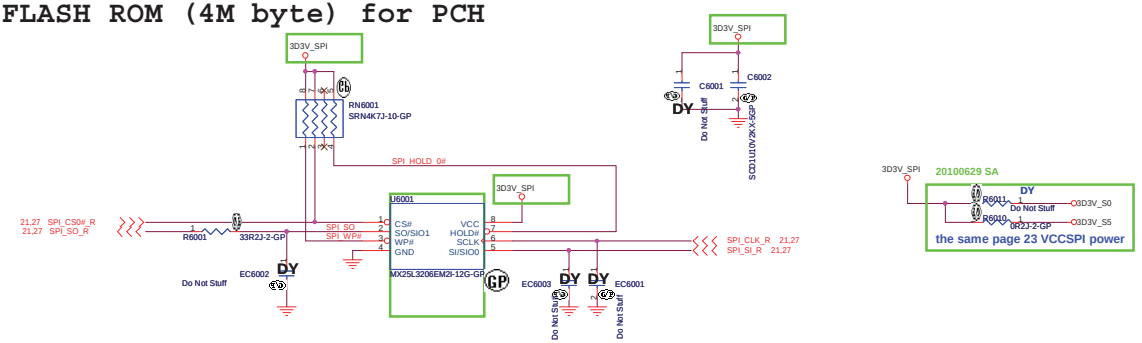


BOM

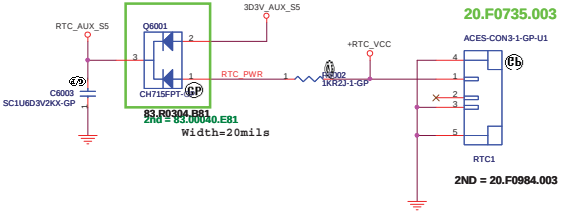
緯創資通 Wistron Corporation 21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MIC/SPEAKER/AUDIO JACK		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 58 of 102	

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT

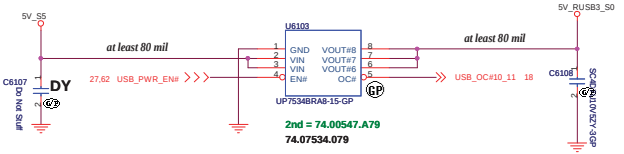


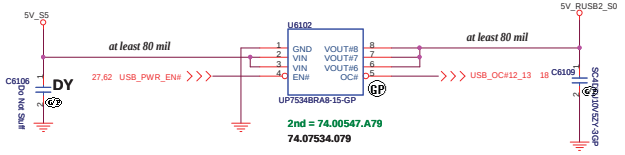
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Flash/RTC*		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 60 of 102	

SSID = USB

RJ45_USB Board USB Power



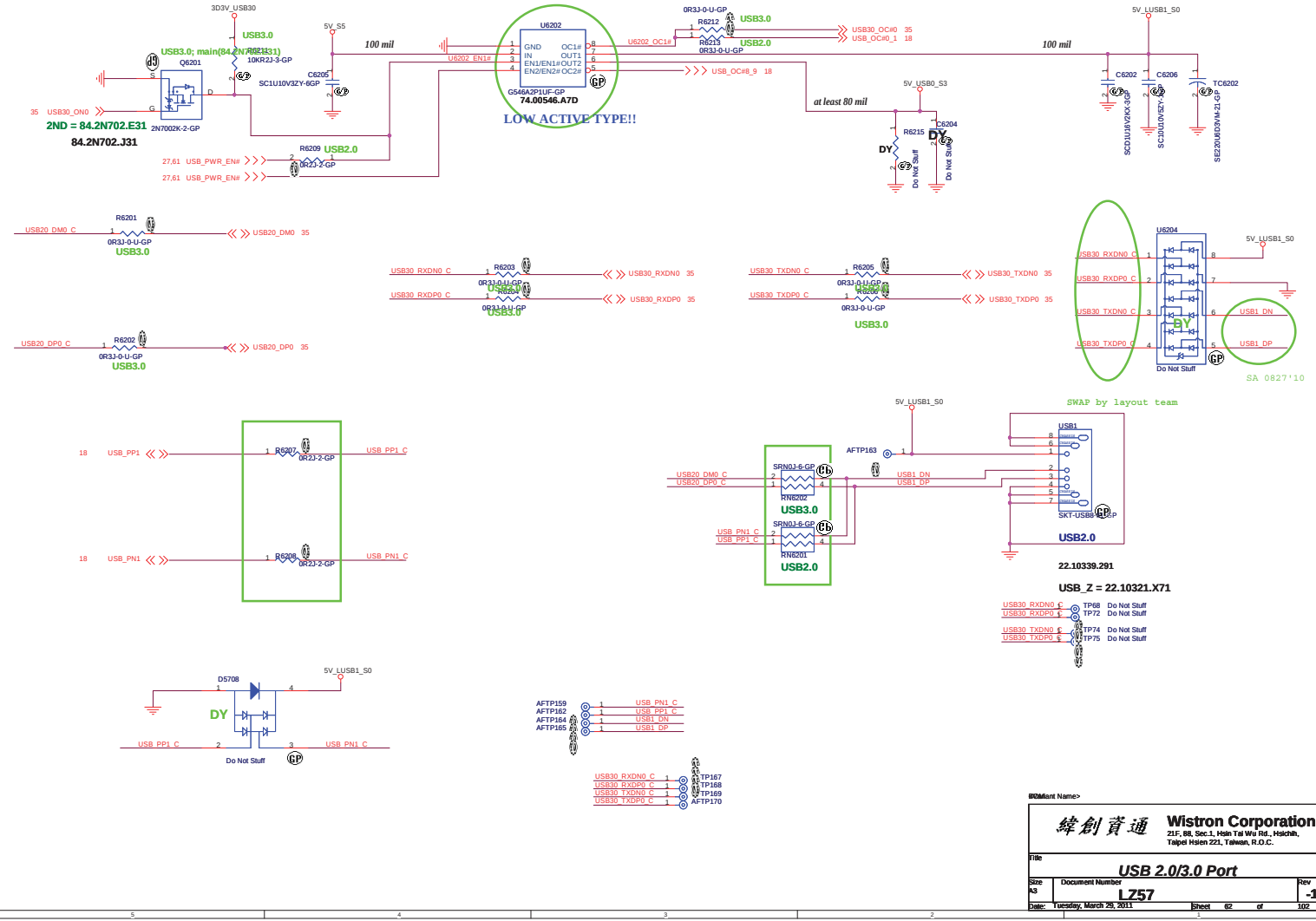


I/O Board USB Power

BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB Power SW		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 61 of 102	

Left Side USB Power Switch



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 2.0/3.0 Port

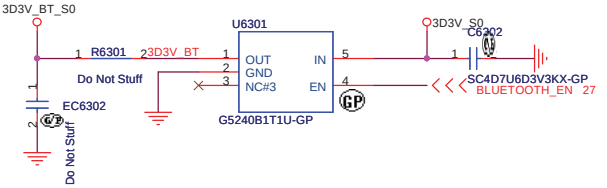
Size: A3 | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 62 of 102

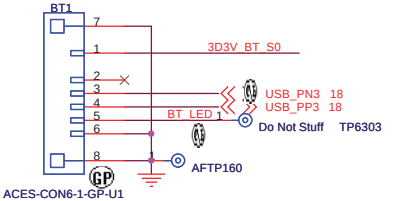
SSID = User.Interface

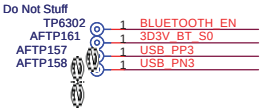
Bluetooth Module conn.

Bluetooth Module



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request





20.F0772.006

2ND = 20.F1804.006

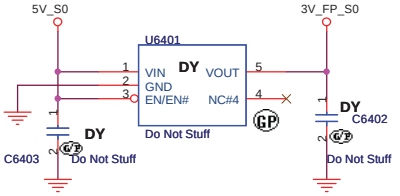
BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth

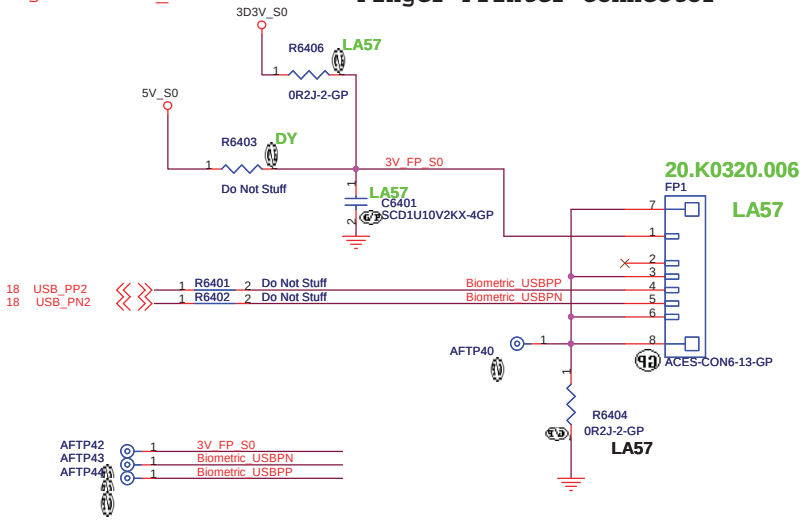
Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 63 of 102



LA47 change to 3D3V_S0

Finger Printer Connector



BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

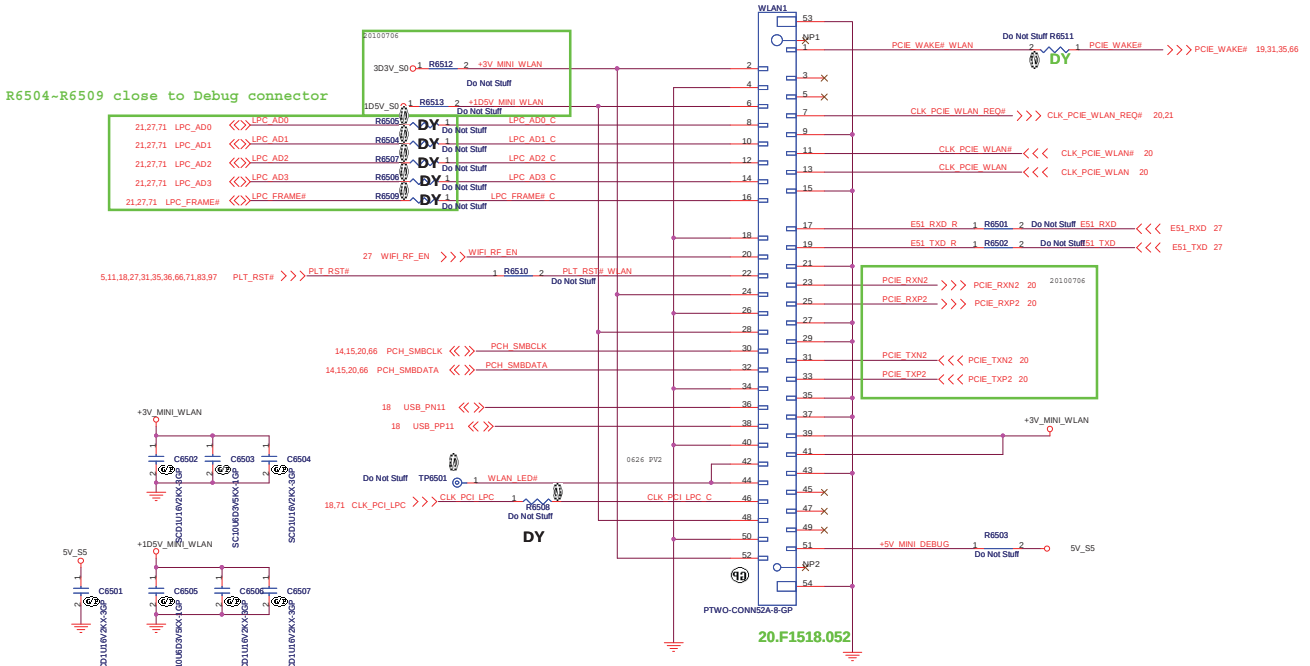
Title: **RESERVED**

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 64 of 102

SSID = Wireless

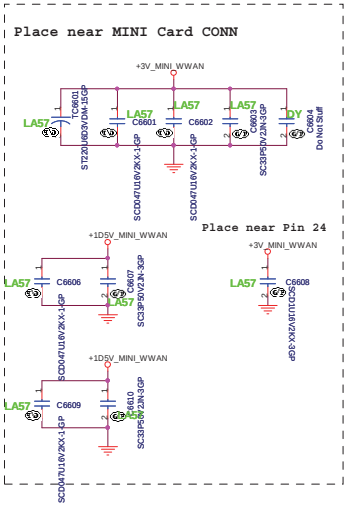
Mini Card Connector(802.11a/b/g/n)

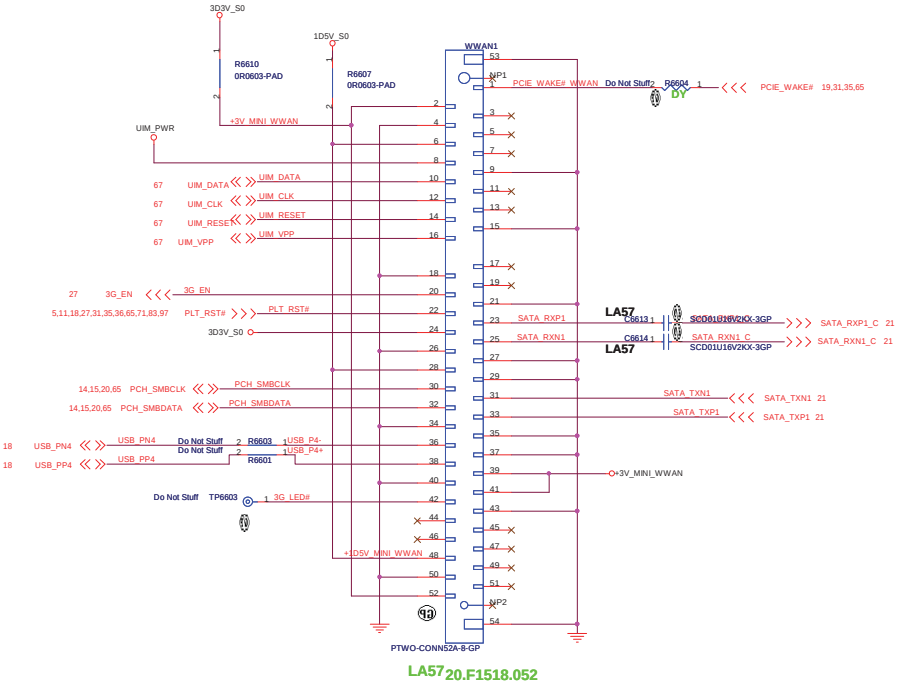


BOM			
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	MINICARD(WLAN)/ITP CONN		
Size A3	Document Number LZ57		Rev -1
Date: Tuesday, March 29, 2011		Sheet 65 of 102	

SSID = Wireless

Mini Card Connector(WWAN)

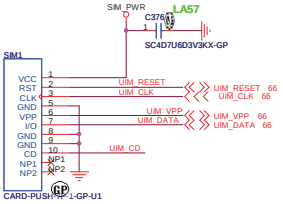




LA57 20.F1518.052

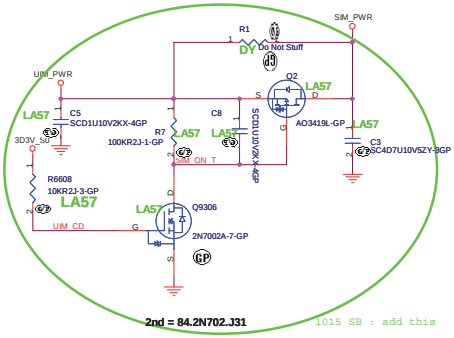
BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	WWAN Connector	
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 66 of 102	



LA57

20.I0073.001



2nd = 84.2N702.J31

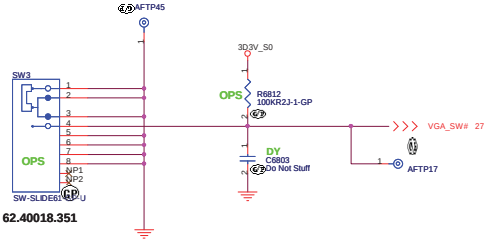
1015 SB : add this

84.2N702.E31

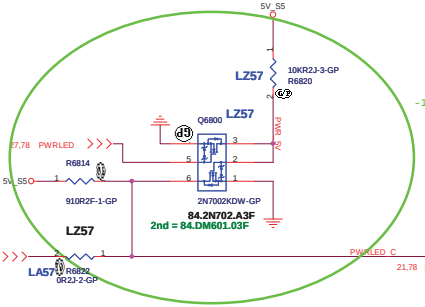
BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SIM CARD***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 67 of 102	

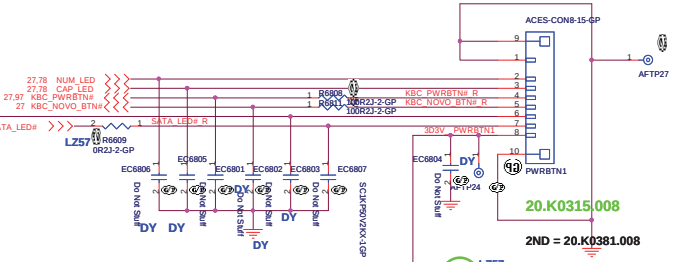
SSID = User.Interface

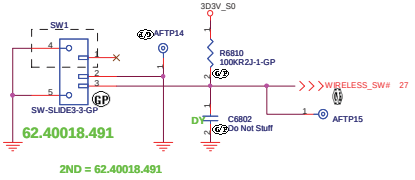


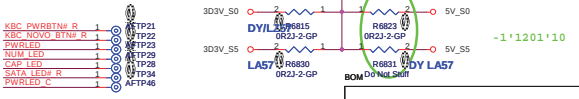
Power button LED(White)



-1_1209'10





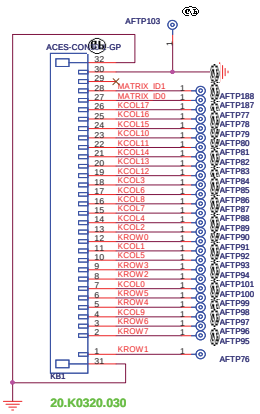


-1'1201'10

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED Bard/Power Button	
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 68 of 102	

SSID = KBC

Internal KeyBoard Connector

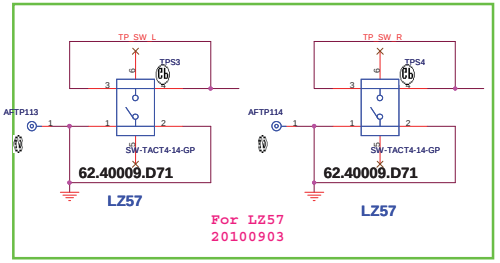


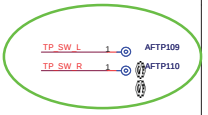
20.K0320.030

ID KEY MATRIX	SENSE			
	27	28	29	30
	IDO	ID1	ID2	GND
US	GND	GND	X	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

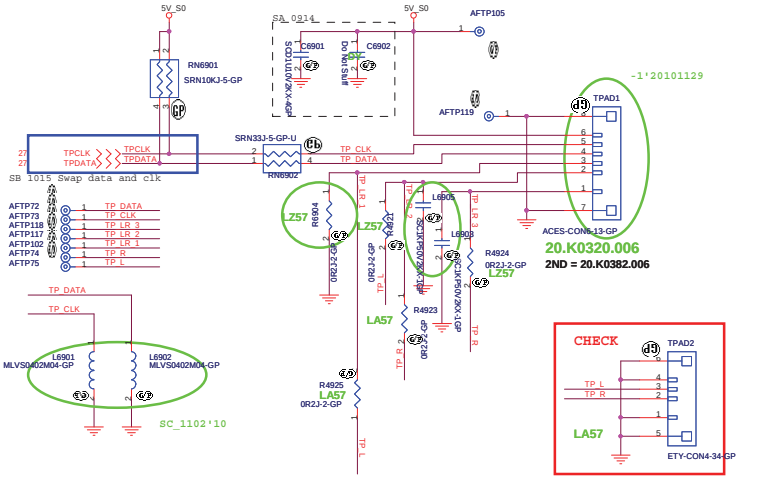
KROW[0..7] 27

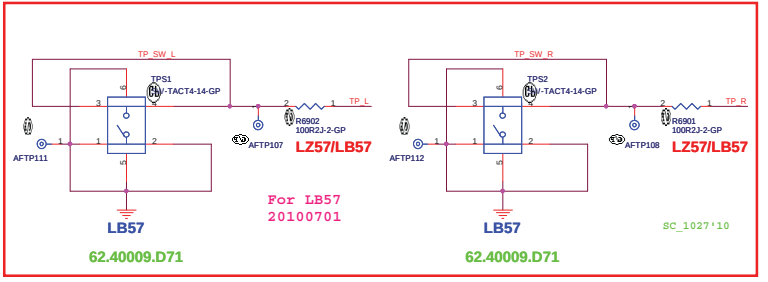
KCOL[0..17] 27





SSID = Touch.Pad





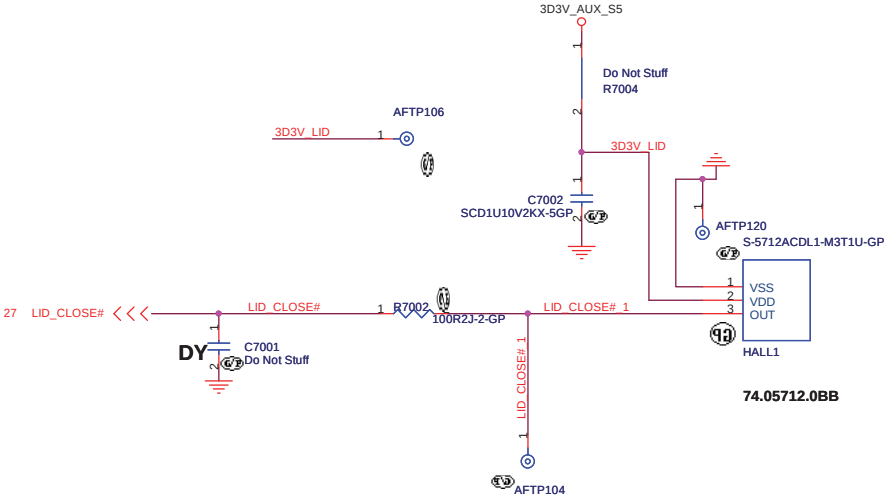
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

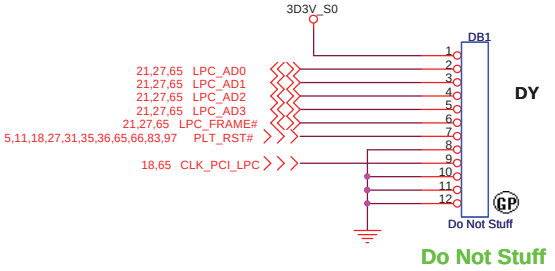
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 69 of 102



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Hall Sensor*		
Size: A4	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 70 of 102	



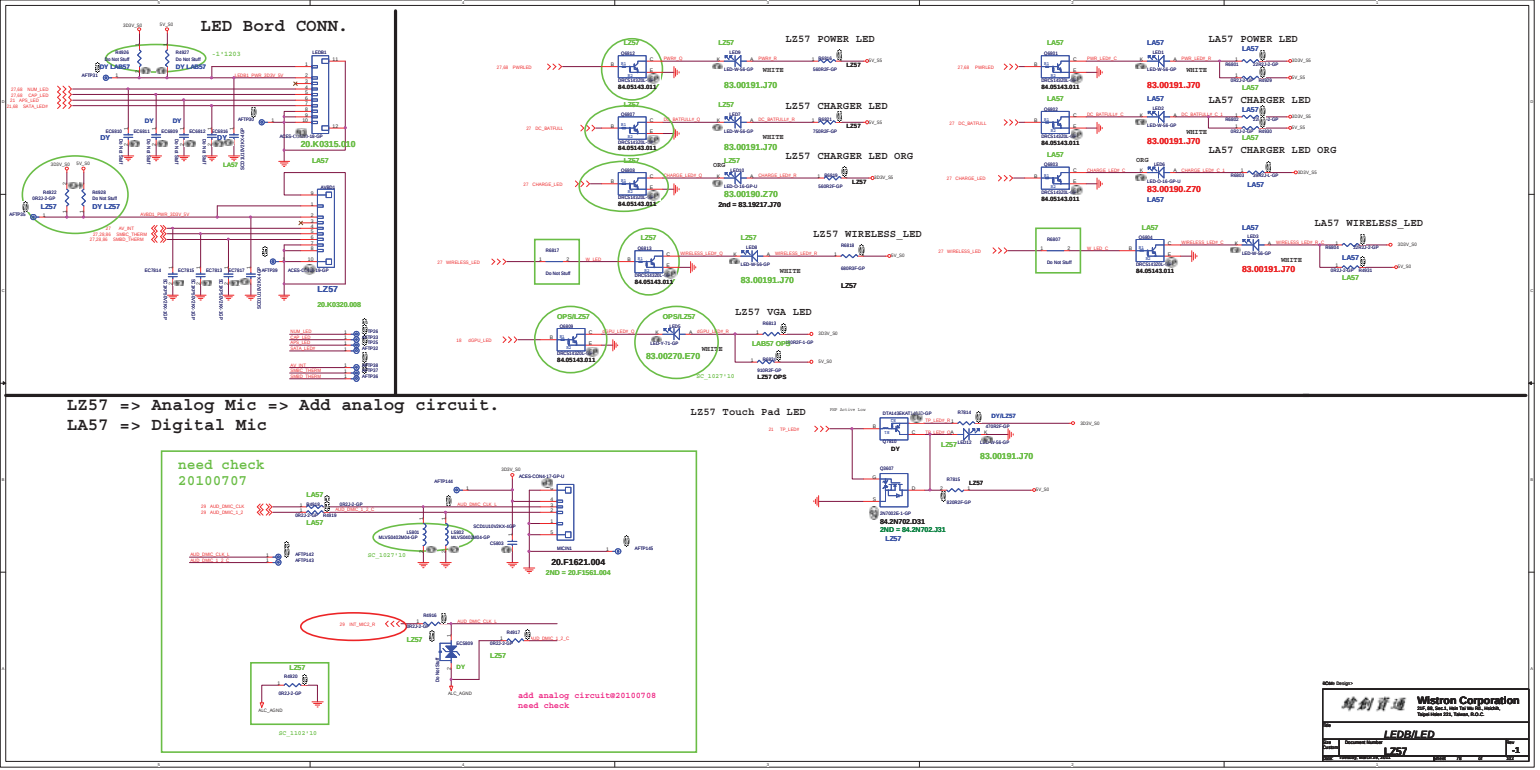
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

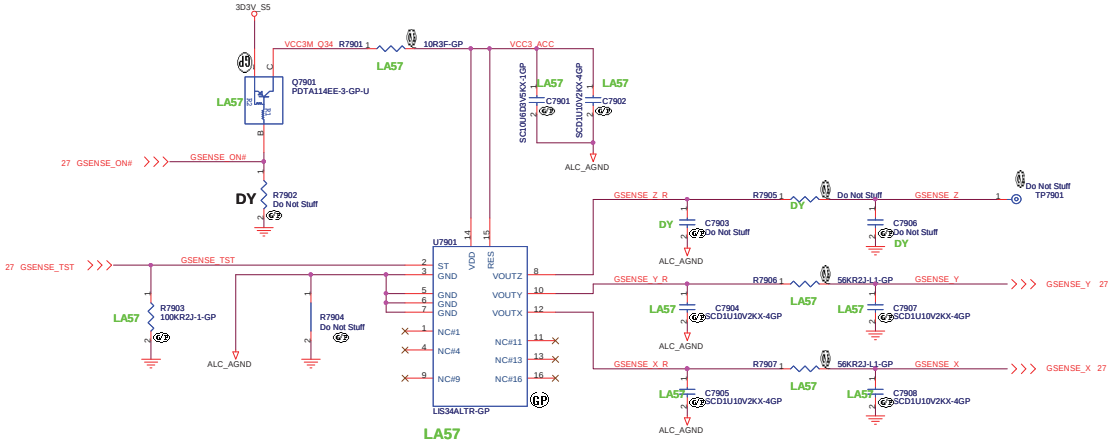
Title: ***Dubug connector***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 71 of 102


LED Bord CONN.
LZ57 POWER LED
LA57 POWER LED
LZ57 CHARGER LED
LA57 CHARGER LED
LZ57 CHARGER LED ORG
LA57 CHARGER LED ORG
LZ57 WIRELESS_LED
LA57 WIRELESS_LED
LZ57 VGA LED
LZ57 Touch Pad LED
LZ57 => Analog Mic => Add analog circuit.
LA57 => Digital Mic
need check
20100707
add analog circuit@20100708
need check
LED8/LED
LZ57
Wistron Corporation

G-Sensor



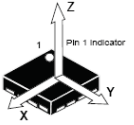
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **G-Sensor**

Size	Document Number	Rev
Custom	LZ57	-1

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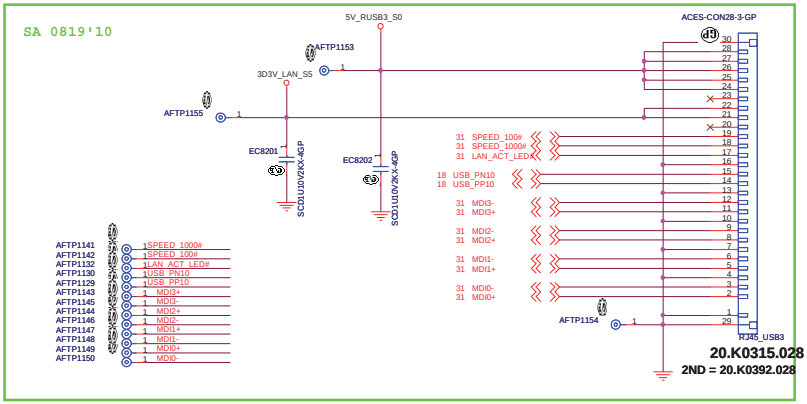
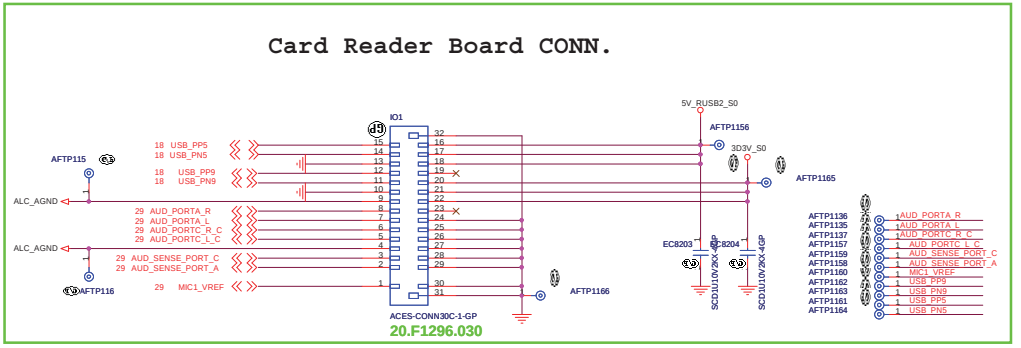
RJ45_USB CONN.



Card Reader Board CONN.



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	LZ57	-1

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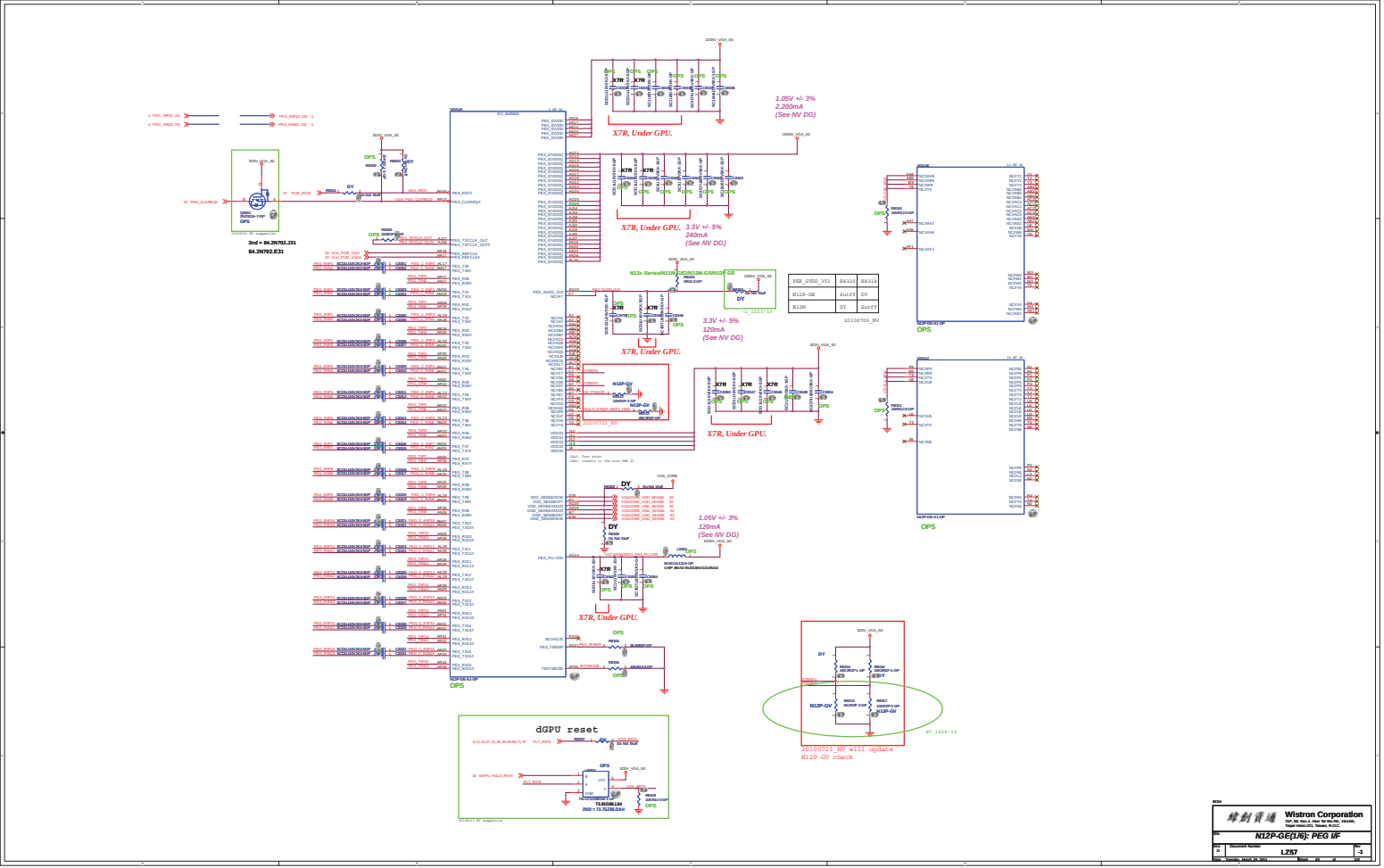
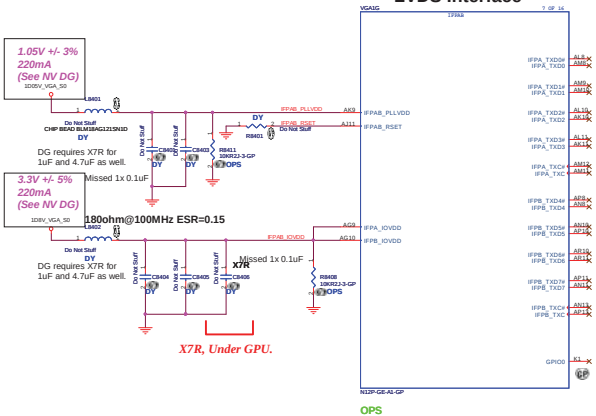
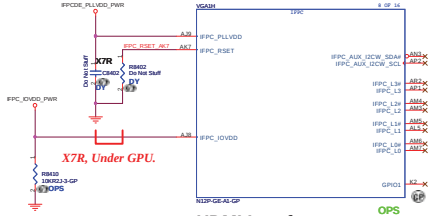
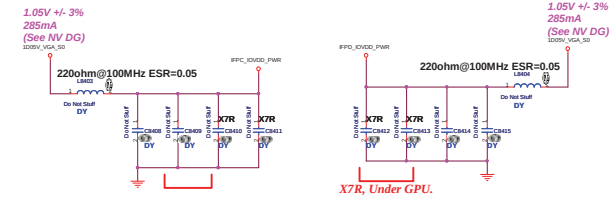

X7R, Under GPU.
1.05V +/- 3%
2,200mA
(See NV DG)
3.3V +/- 5%
240mA
(See NV DG)
N12x-SeriesN13P-GE2/N13M-GS/N12P-GE
3.3V +/- 5%
120mA
(See NV DG)
X7R, Under GPU.
1.05V +/- 3%
120mA
(See NV DG)
X7R, Under GPU.
X7R, Under GPU.
PEX_SVDD_3V3 R8325 R8318
N12P-GE Suffi DY
N12M DY Suffi
20100705_NV
2nd = 84.2N702.E31
84.2N702.E31
dGPU reset
20100721_NV will update
N12P-GV check
Wistron Corporation
N12P-GE(1/6): PEG IF
LZ57

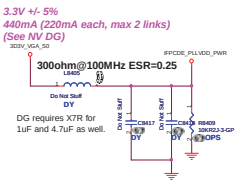
LVDS Interface

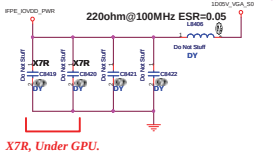


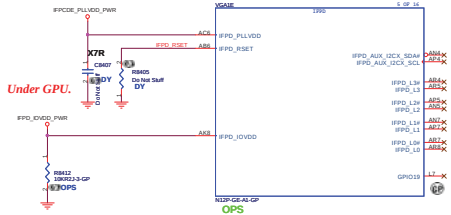
HDMI Interface

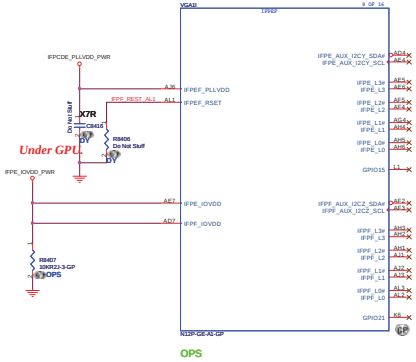






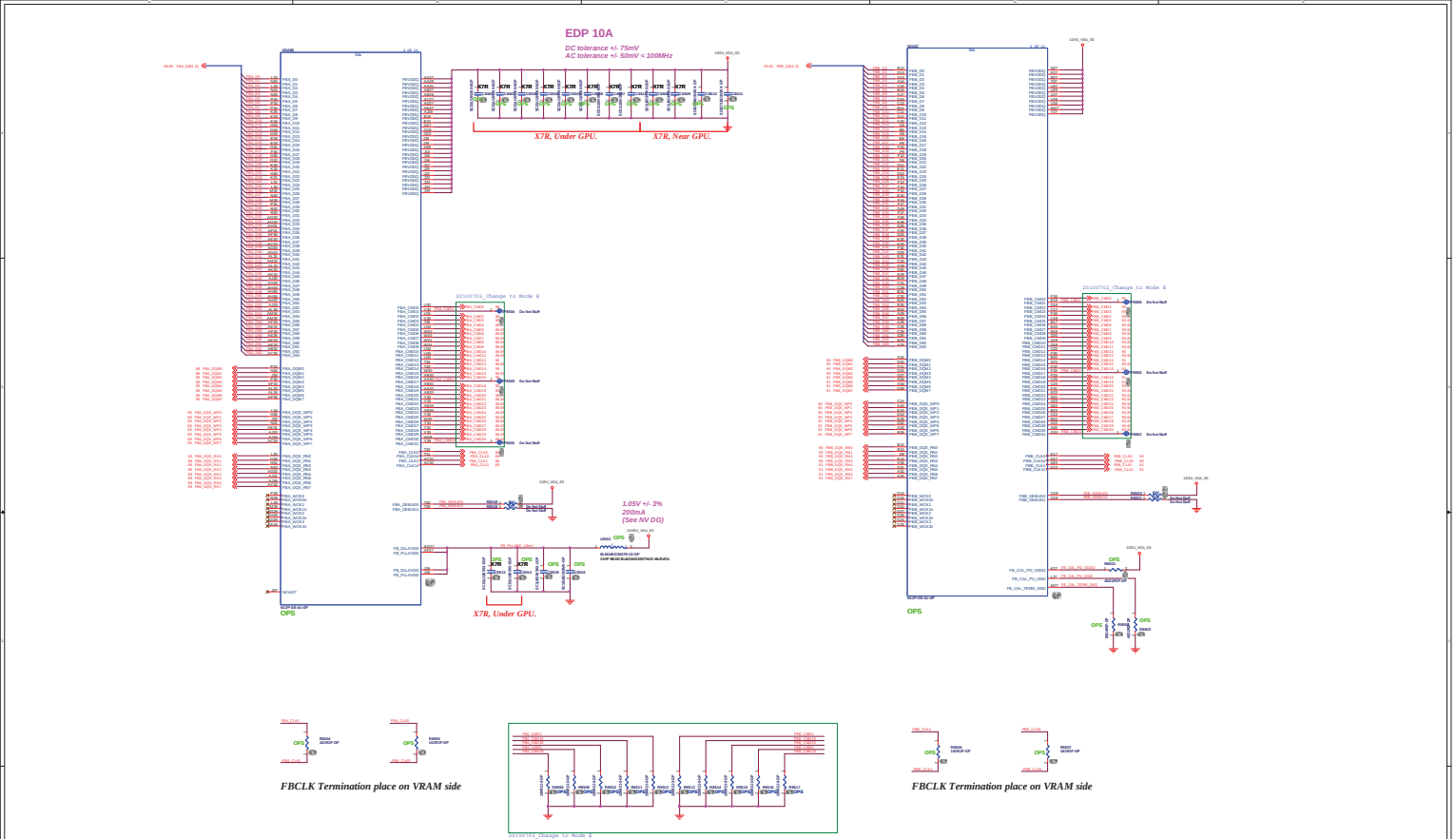






BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: N12P-Q1/Q3 (2/6): DIGITAL OUT		
Size: A2	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 84 of 102	



設計單位	Wistron Corporation		
	22F,88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	N12P-Q1/Q3 (3/6): VRAM I/F		
Size	Document Number		Rev
A	L257		A
Date: Tuesday, March 16, 2010	Sheet 46 of 58		

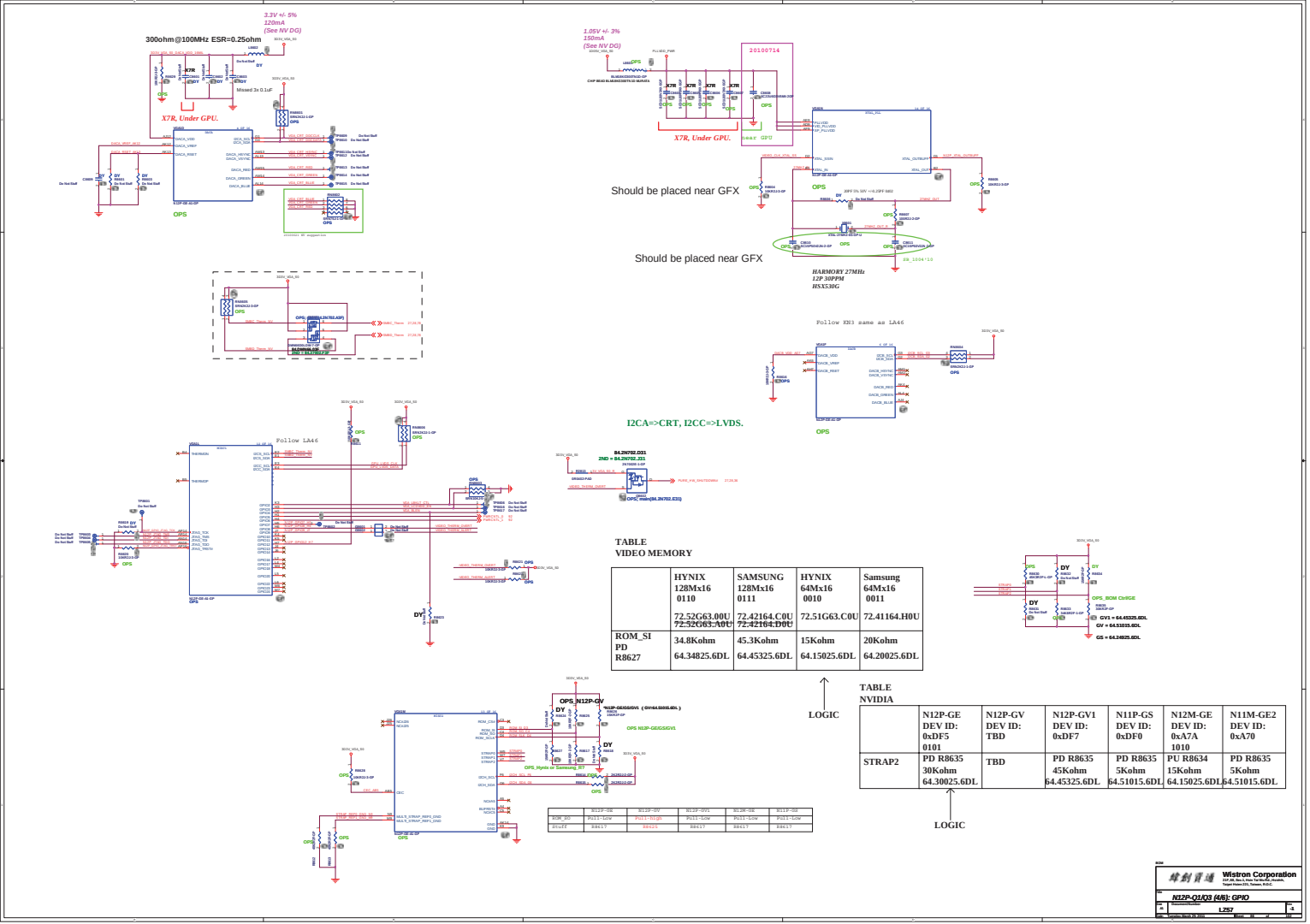


TABLE
VIDEO MEMORY

	HYNIX 128Mx16 0110 72.52G63.00U ~~72.52G63.A0U~~	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
		72.42164.C0U ~~72.42164.D0U~~	72.51G63.C0U	72.41164.H0U
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

LOGIC

TABLE
NVIDIA

	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: TBD	N12P-GV1 DEV ID: 0xDF7	N11P-GS DEV ID: 0xDF0	N12M-GE DEV ID: 0xA7A 1010	N11M-GE2 DEV ID: 0xA70
STRAP2	PD R8635 30Kohm 64.30025.6DL	TBD	PD R8635 45Kohm 64.45325.6DL	PD R8635 5Kohm 64.51015.6DL	PU R8634 15Kohm 64.15025.6DL	PD R8635 5Kohm 64.51015.6DL

LOGIC

	N12P-GE	N12P-GV	N12P-GV1	N12M-GE	N11P-GS
ROM_SO	Pull-Low	Pull-Up	Pull-Low	Pull-Low	Pull-Low
Stuff	R8617	R8625	R8617	R8617	R8617

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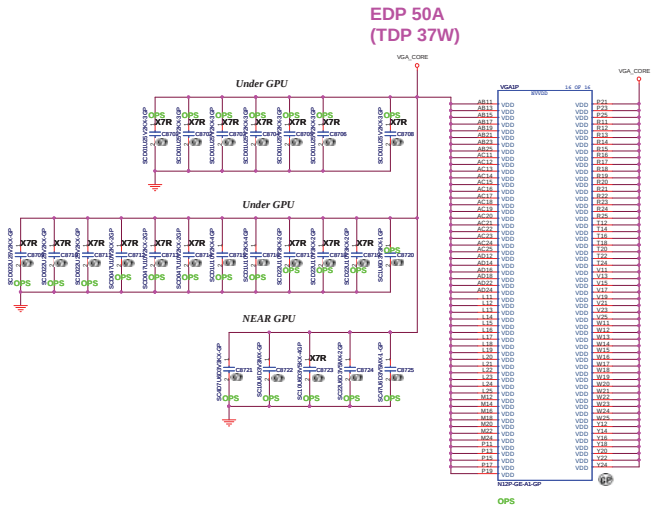
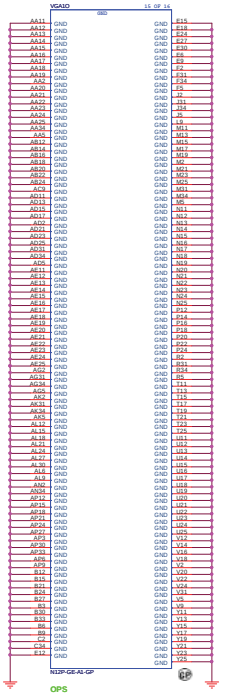
N12P-Q1/Q3 (4/6): GPIO

LZ57





BOM

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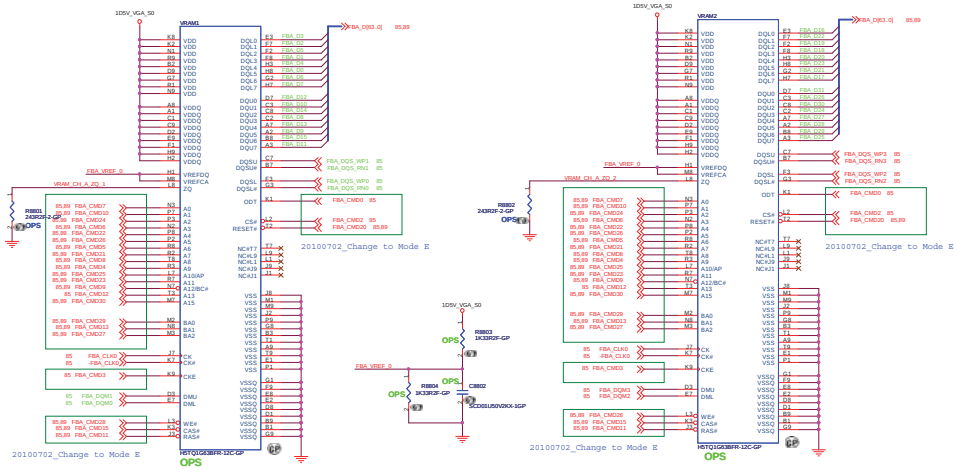
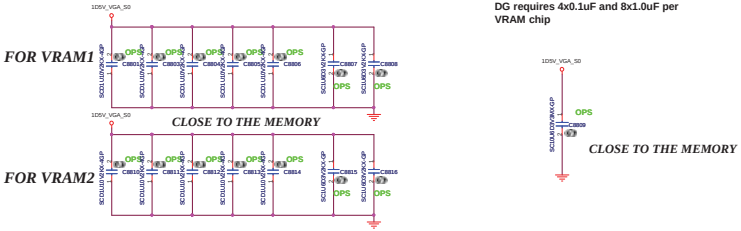
Title: N12P-Q1/Q3 (5/6): POWER

Size	Document Number	Rev
A0	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 87 of 102



FB CMD mapping Mode D-N12x



DG requires 4x0.1uF and 8x1.0uF per VRAM chip

VIDEO FRAME BUFFER PORT A

BOM

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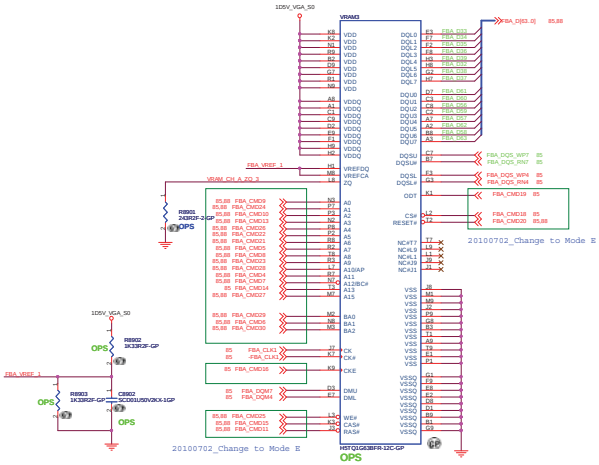
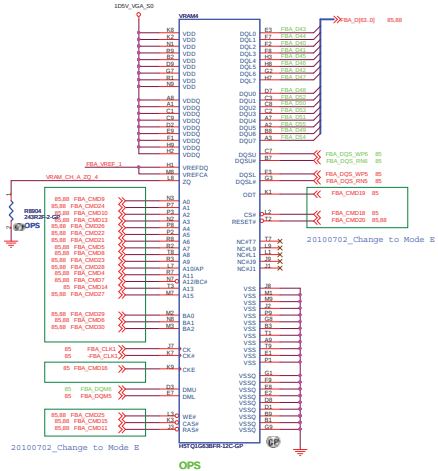
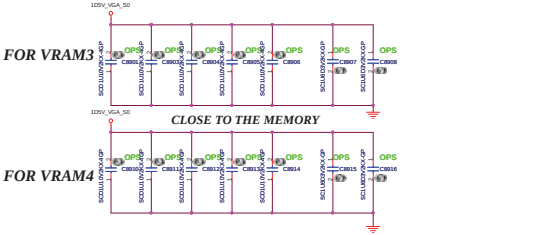
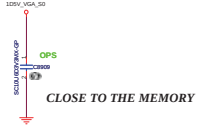
Title: *VRAM CHANNEL-A*		
Size: A2	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 88 of 102	





FB CMD mapping Mode D-N12x





VIDEO FRAME BUFFER PORT A

BOM

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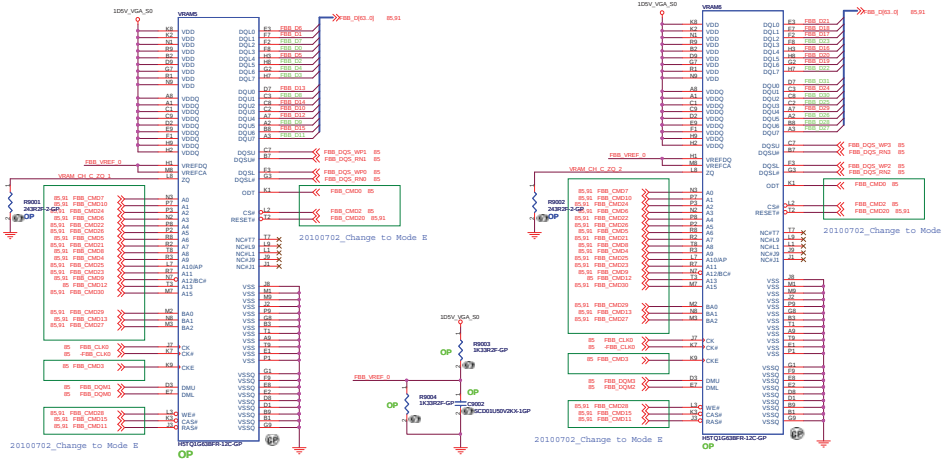
File: VRAM CHANNEL-A

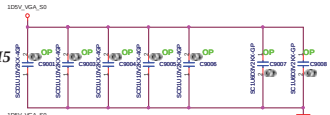
Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 89 of 102



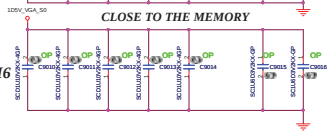
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

FOR VRAM5



CLOSE TO THE MEMORY

FOR VRAM6



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT C

BOM

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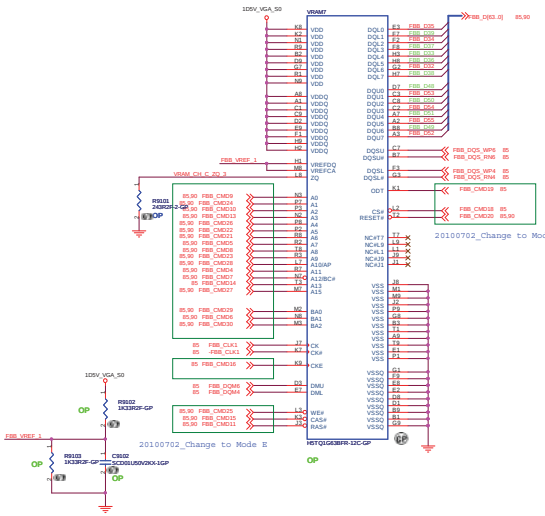
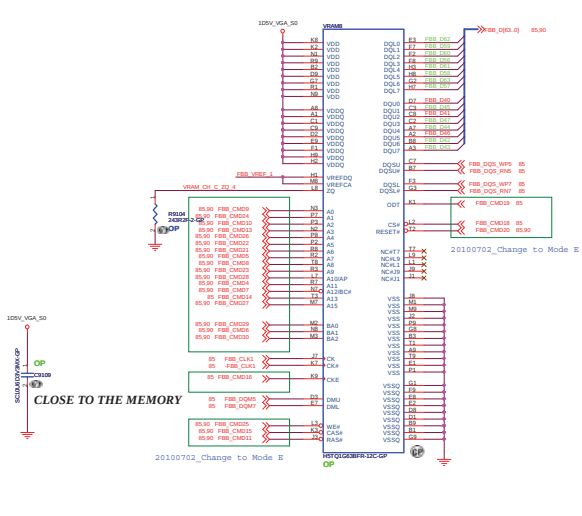
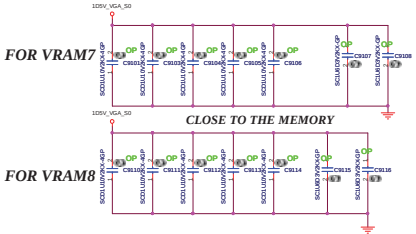
Title	VRAM CHANNEL-C		
Size	Document Number		Rev
A2	LZ57		-1
Date: Tuesday, March 29, 2011	Sheet 90 of 100		







VIDEO FRAME BUFFER PORT C

BOM

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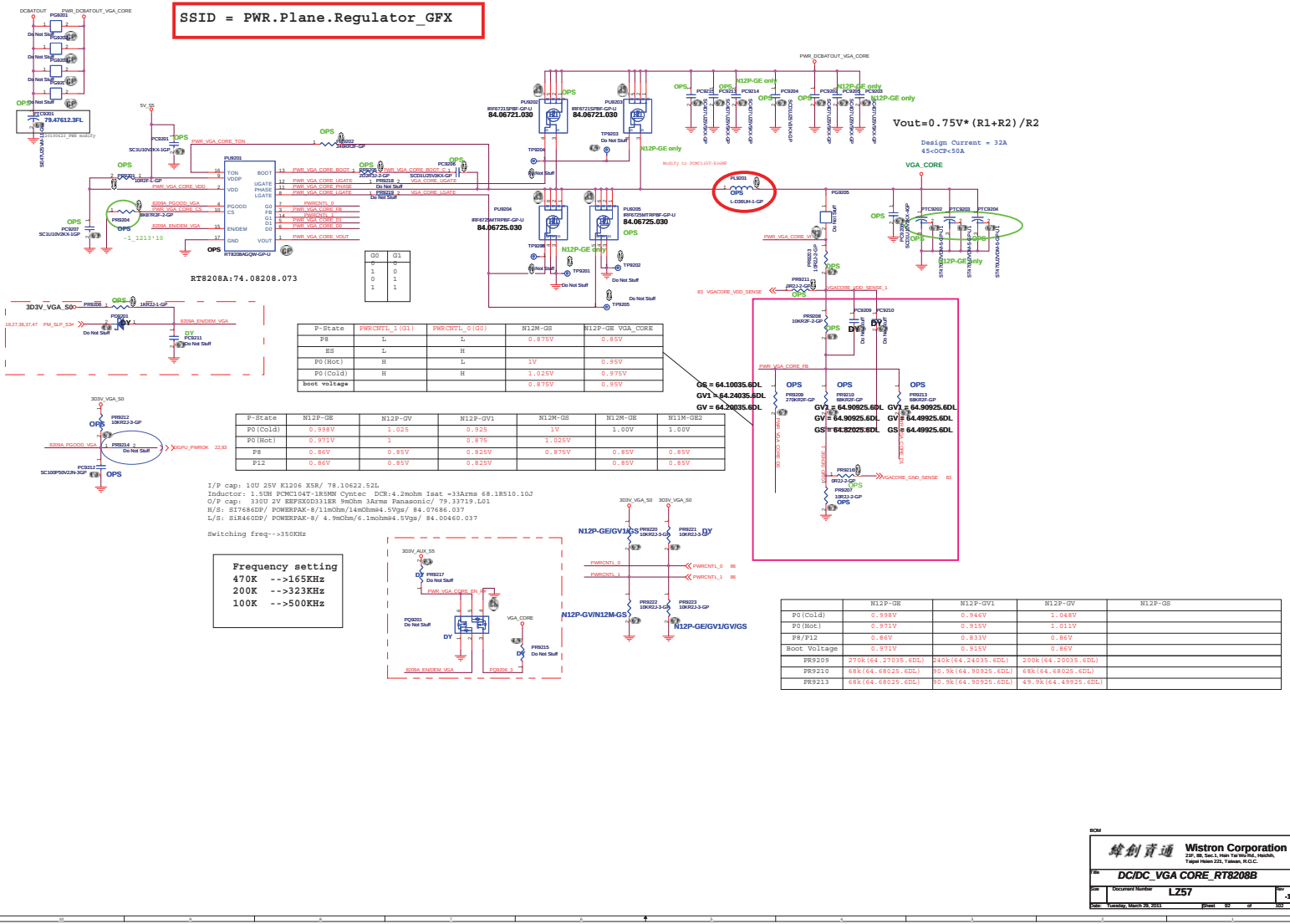
Title: *VRAM CHANNEL-C*

Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 91 of 102

SSID = PWR.Plane.Regulator_GFX



P-State	PWRCNTL_1 (G1)	PWRCNTL_0 (G0)	N12M-GS	N12P-GE VGA_CORE
P8	L	L	0.875V	0.85V
ES	L	H		
P0(Hot)	H	L	1V	0.95V
P0(Cold)	H	H	1.025V	0.975V
boot voltage			0.875V	0.95V

P-State	N12P-GE	N12P-GV	N12P-GV1	N12M-GS	N12M-GE	N11M-GE2
P0(Cold)	0.998V	1.025	0.925	1V	1.00V	1.00V
P0(Hot)	0.971V	1	0.875	1.025V		
P8	0.86V	0.85V	0.825V	0.875V	0.85V	0.85V
P12	0.86V	0.85V	0.825V		0.85V	0.85V

I/P cap: 10U 25V K1206 XSR/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq--350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

	N12P-GE	N12P-GV1	N12P-GV	N12P-GS
P0(Cold)	0.998V	0.946V	1.048V	
P0(Hot)	0.971V	0.915V	1.011V	
P8/P12	0.86V	0.833V	0.86V	
Boot Voltage	0.971V	0.915V	0.86V	
PR9209	270k(64.27035.6DL)	240k(64.24035.6DL)	200k(64.20035.6DL)	
PR9210	68k(64.68025.6DL)	80.9k(64.90925.6DL)	68k(64.68025.6DL)	
PR9213	68k(64.68025.6DL)	80.9k(64.90925.6DL)	49.9k(64.49925.6DL)	

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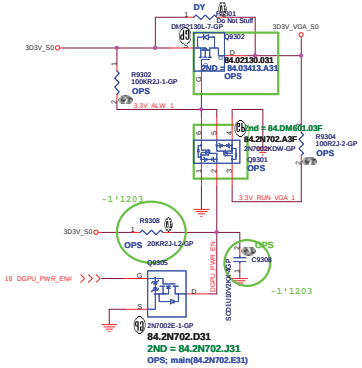
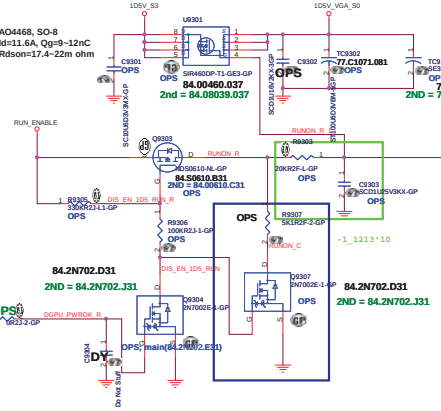
Title: DC/DC_VGA CORE_RT8208B
Size: Document Number: LZ57 Rev: -1
Date: Tuesday, March 29, 2011 Sheet 82 of 102

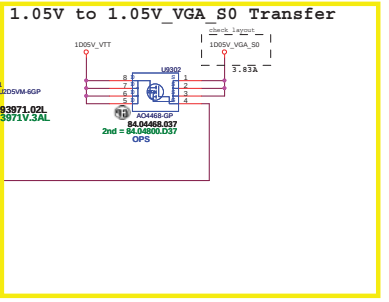
+3VS to 3.3V_DELAY Transfer



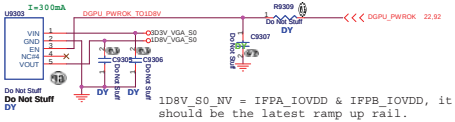
1D5V_VGA_S0



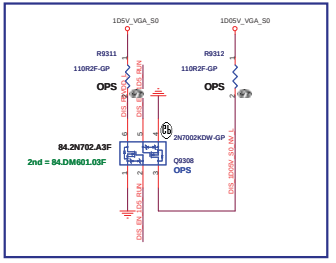
1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.



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Title	DISCRETE VGA POWER		
Size	Document Number	LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 93 of 102		

CPU Plate

H13 Do Not Stuff — Do Not Stuff
H14 Do Not Stuff — Do Not Stuff
H15 Do Not Stuff — Do Not Stuff

VGA Std-Off

H10 STF237R128H42-GP — OPS — 34.4GD01.101
H11 STF237R128H42-GP — 34.4GD01.101

Check test point

3D3V_S0		TP8507	Do Not Stuff
3D3V_AUX_S5		TP8508	Do Not Stuff
3D3V_S5		TP8509	Do Not Stuff
5V_S5		TP8510	Do Not Stuff
11,19,27	PM_PWRBTN#	TP8511	Do Not Stuff
5,11,22,36	H_CPUPWRGD	TP8512	Do Not Stuff
27,36	S5_ENABLE	TP8513	Do Not Stuff
5,11,18,27,31,35,36,65,66,71,83	PLT_RST#	TP8514	Do Not Stuff

Test Point放在Dimm Door打開可量測處

Structure boss

H1 Do Not Stuff — Do Not Stuff
H2 Do Not Stuff — Do Not Stuff
H3 Do Not Stuff — Do Not Stuff
H5 Do Not Stuff — Do Not Stuff
H6 Do Not Stuff — Do Not Stuff
H12 Do Not Stuff — Do Not Stuff
H7 Do Not Stuff — Do Not Stuff
H8 Do Not Stuff — Do Not Stuff

MiniPCI Std-Off

H4 STF237R113H63-GP — 34.44P03.101

Do Not Stuff
H16 — Do Not Stuff

H17 Do Not Stuff — Do Not Stuff

S1 SPRING-71-GP — DY
S2 SPRING-63-GP
S3 SPRING-63-GP
34.4Y806.001 34.4Y806.001

SC_1101'10

POWER TESTING POINT--TOP

27,68 KBC_PWRBTN#
TP9701 Do Not Stuff
TP9700 Do Not Stuff

POWER TESTING POINT--Bottom

27,68 KBC_PWRBTN#
TP9702 Do Not Stuff
TP9703 Do Not Stuff

AD+
EC9708 DY Do Not Stuff
EC9709 DY Do Not Stuff
EC9710 DY Do Not Stuff
EC9711 DY Do Not Stuff
EC9712 DY Do Not Stuff
EC9713 SCD1U25V2KX-GP

DCBATOUT
EC9720 DY Do Not Stuff
EC9719 DY Do Not Stuff
EC9718 SCD1U25V2KX-GP
EC9717 SCD1U25V2KX-GP
AD_JK
EC9716 SCD1U25V2KX-GP
EC9715 DY Do Not Stuff
SA 0904'10

DCBATOUT
EC9714 SCD1U25V2KX-GP
SA 0809'10

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Title: UNUSED PARTS/EMI Capacitors

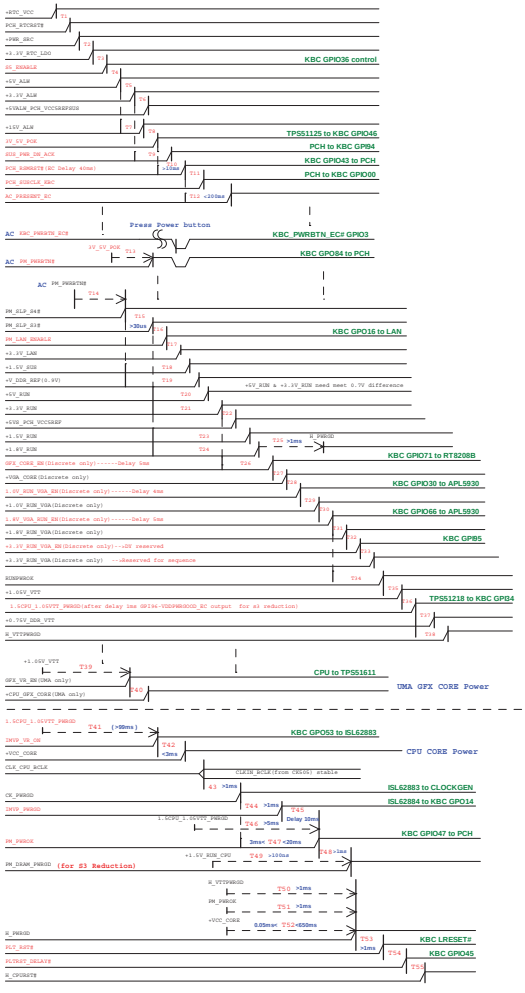
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 97 of 102

Intel-Power Up Sequence

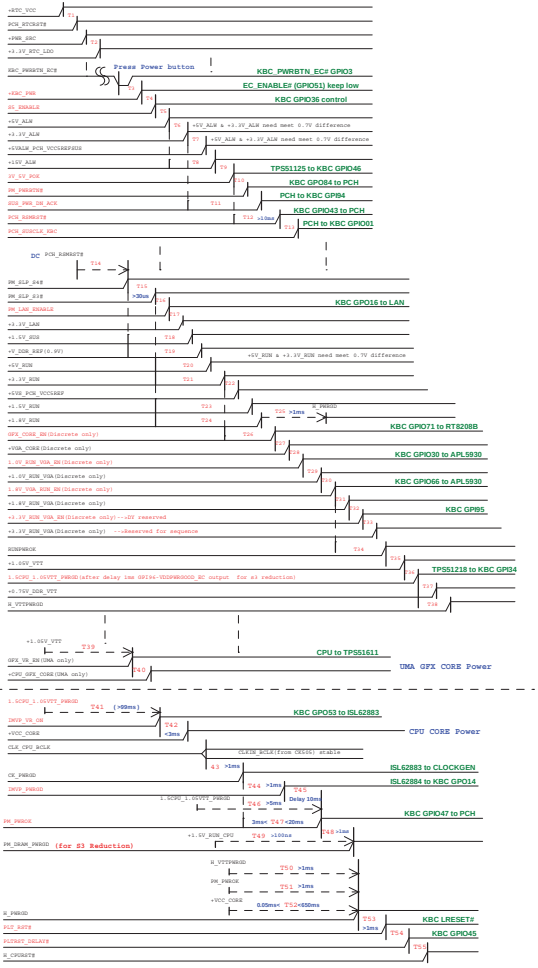
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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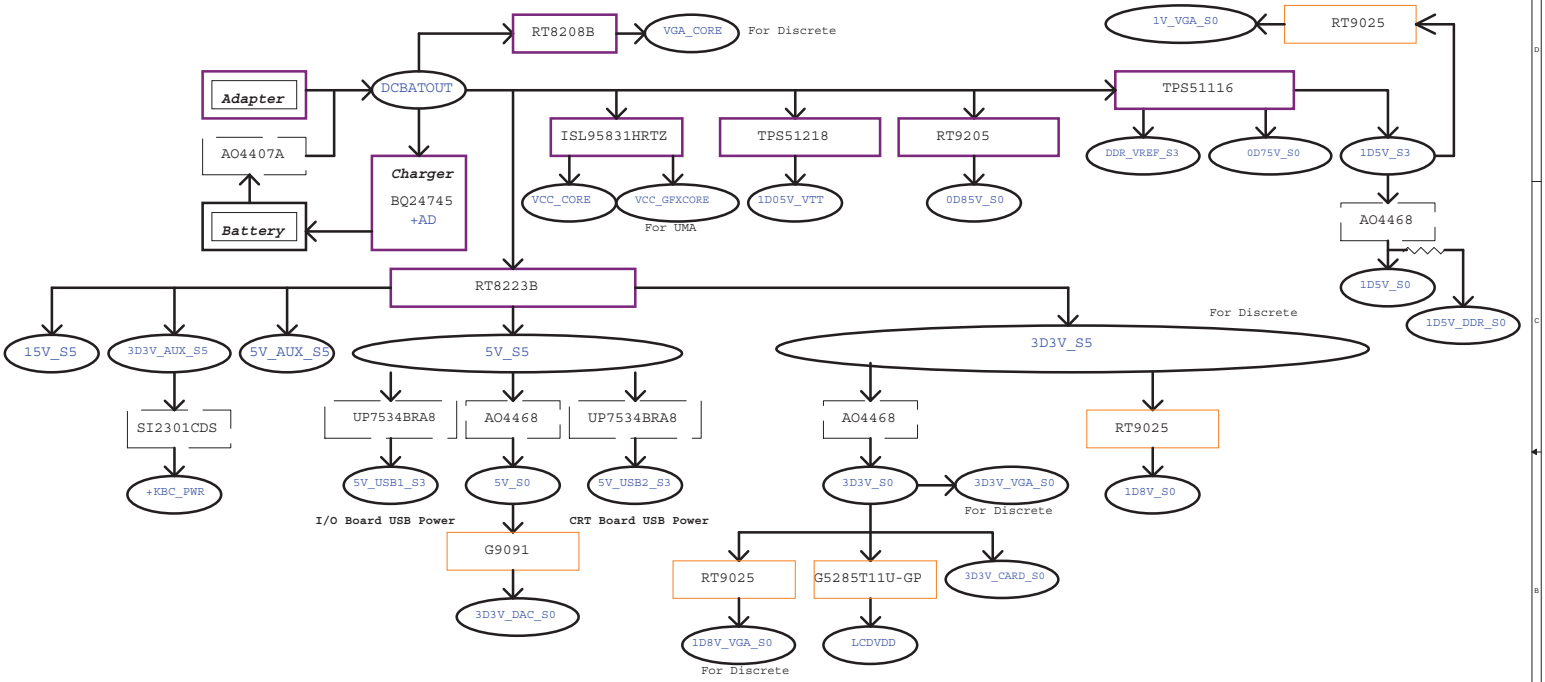
Power Sequence

LZ57

-3



Power Shape

Regulator | LDO | Switch

BOM

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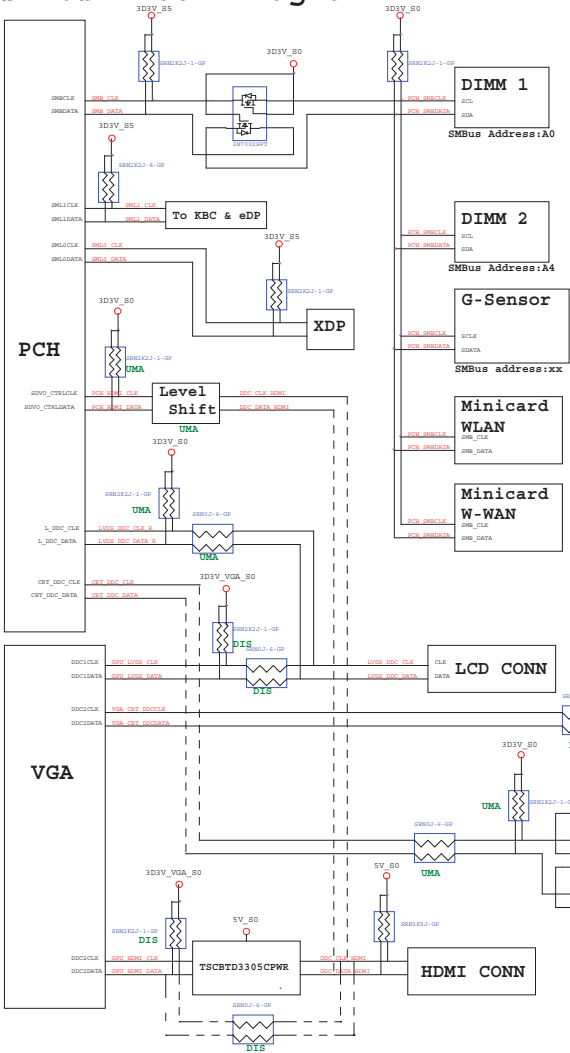
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

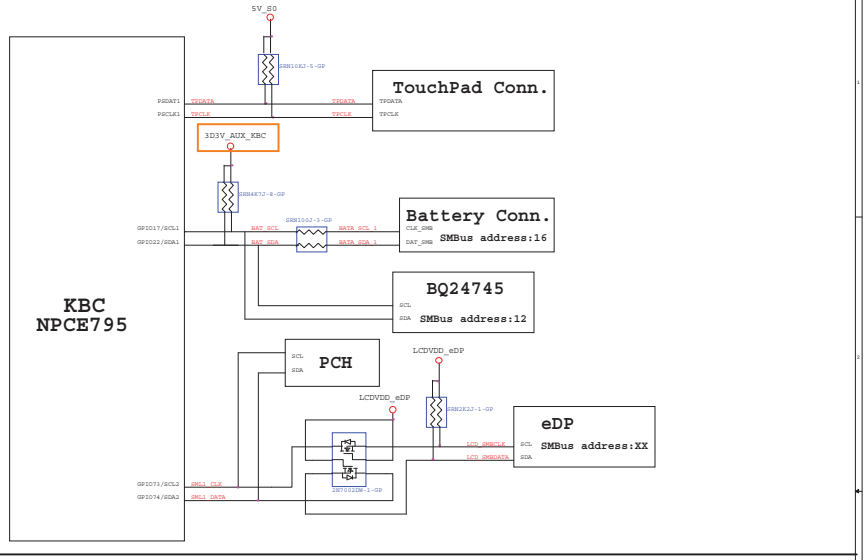
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 100 of 102

PCH SMBus Block Diagram

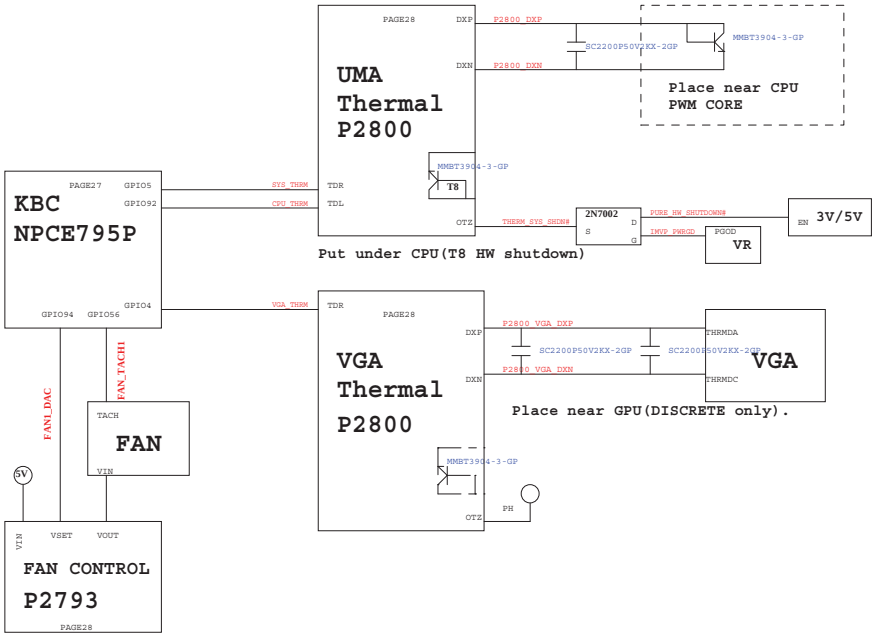


KBC SMBus Block Diagram

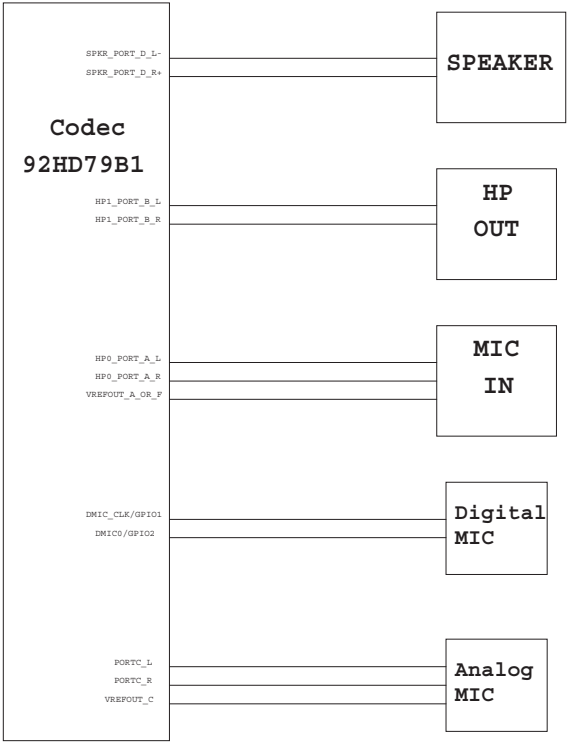


BOM			
緯創資通	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	SMBUS Block Diagram		
Size: M	Document Number: LZ57		Rev: -1
Date: Tuesday, March 29, 2011	Sheet 1(1) of 1(1)		

Thermal Block Diagram



Audio Block Diagram



BOM

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Title	Thermal/Audio Block Diagram	
Size: Custom	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 102 of 102	