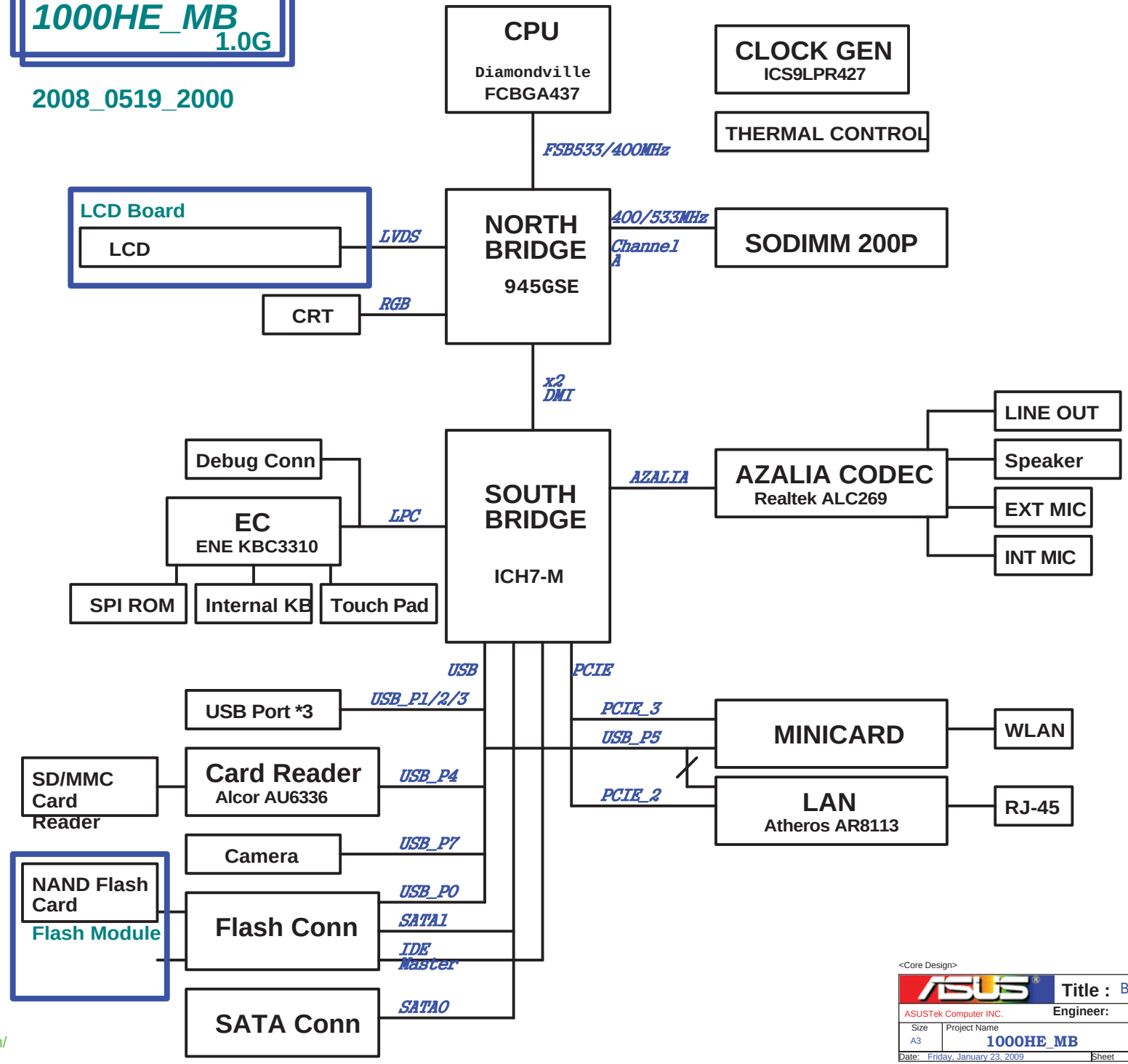
01_Block Diagram
02_System Setting
03_Power Sequence
04_Clock Gen_ICS9LPR426
05_Diamondville_BUS
06_Diamondville_PWR
07_NB-945GMS(HOST)
08_NB-945GMS(DMI)
09_NB-945GMS(GRAPHIC)
10_NB-945GMS(DDR2)
11_NB-945GMS(PWR)
12_NB-945GMS(PWR2)
13_NB-945GMS(GND)
14_SB-ICH7M(PWR)
15_SB-ICH7M(1)
16_SB-ICH7M(2)
17_SB-ICH7M(3)
18_DDR2 SODIMM
19_DDR2_Termination
20_Onboard VGA
21_LCD Conn_LID
22_PCIEx 3.5G & Ext. Antenna
23_Mini WIFI+ BT
24_LAN_Atheros AR8113
25_MDC_RJ11_RJ45
26_Flash Conn
27_SATA Hdd
28_USB Port
29_Camera Conn
30_Card Reader_AU6336C52
31_Codec_ALC269
32_Audio_AMP_Jack
33_EC_ENE KB3310
34_EC_UART controller
35_Switch_SPI ROM_Debug Conn
36_Thermal Sensor_FAN
37_KB_Touch Pad
38_LED_THERMTRIP
39_Discharge
40_PWR Jack
41_Srew Hole
42_EMI
43_POWER FLOW
44_Vcore
45_Power System
46_Power_+1.8V & VTTDDR
47_Power_VCCP
48_Power_+1.5VS & +2.5VS
49_Power_Charger
50_EC Pin Define
51_History

1000HE_MB 1.0G

2008_0519_2000

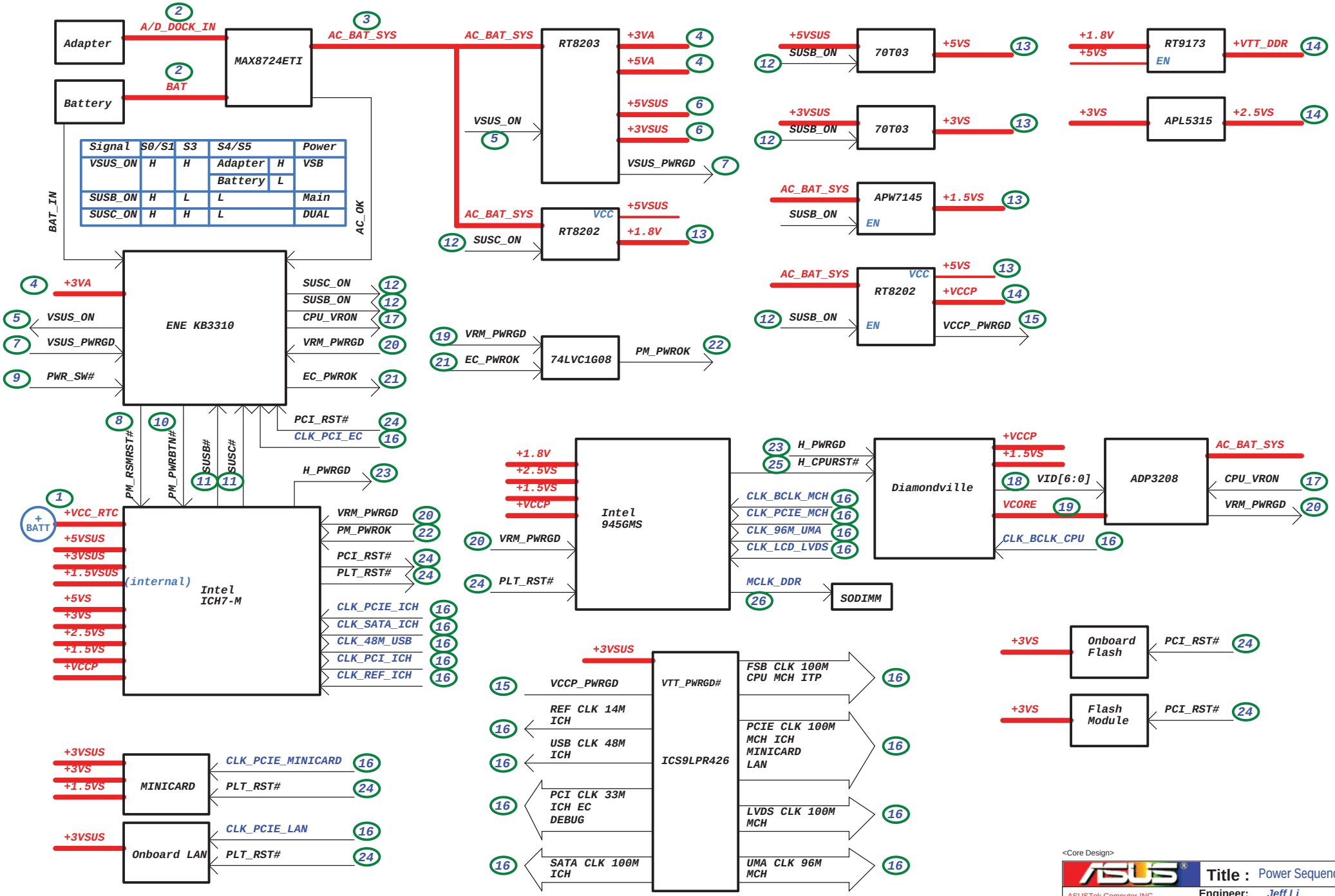


<Core Design>

ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: Echo_Huang	
Size: A3	Project Name: 1000HE_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 1 of 47	

<Core Design>

ASUSTek Computer INC.	Title : History	
	Engineer: KingCa_Jin	
Size: A3	Project Name: 1000HE_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 2 of 47	



<Core Design>

ASUSTek Computer INC.	Title : Power Sequence	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 3 of 47	

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMI#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SCI#	EXT_SCI#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configureation
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSAVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRL_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

<Core Design>

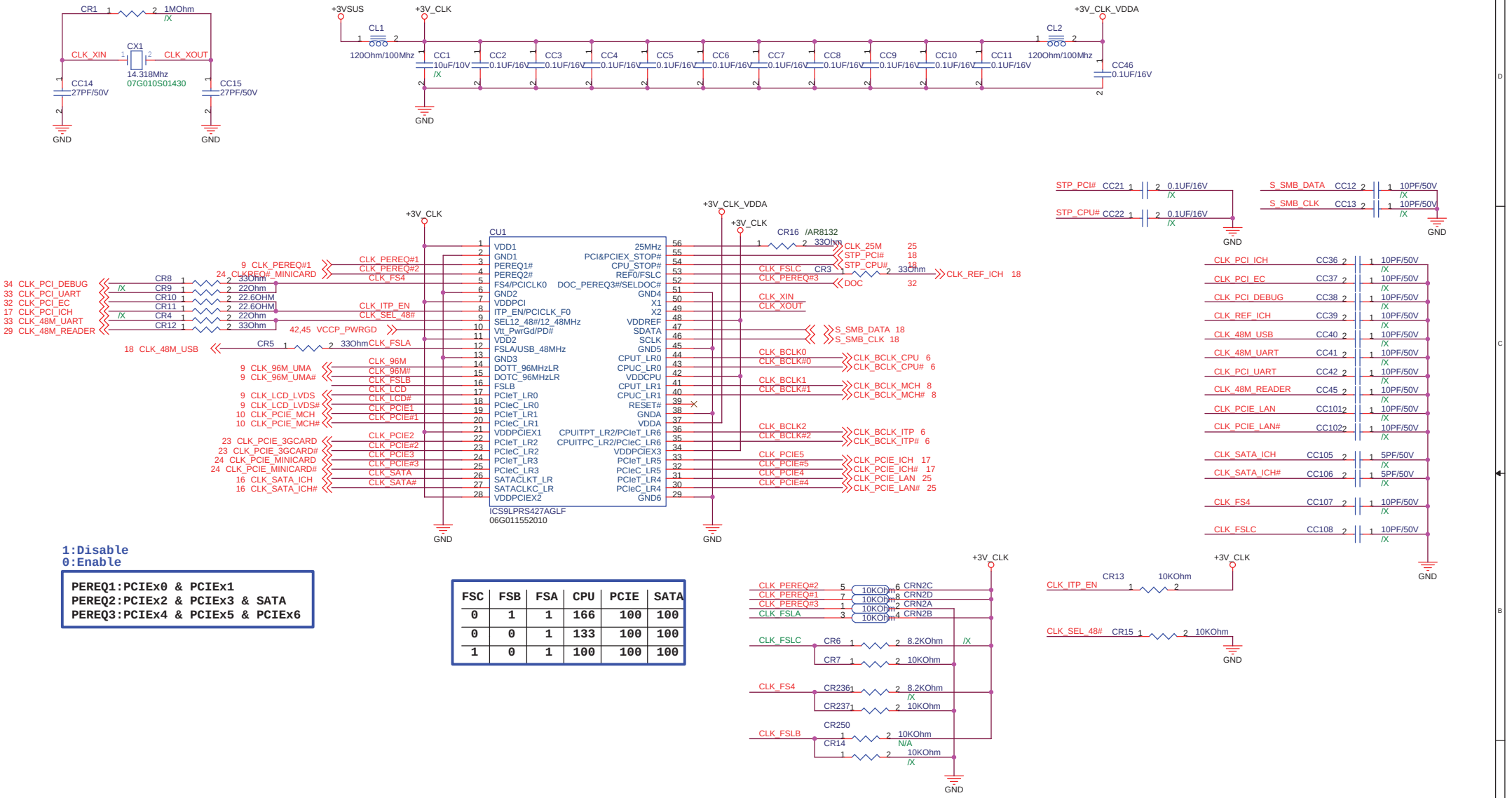
ASUSTek Computer INC.

Title : EC Pin Define

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 4 of 47



1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	1	1	166	100	100
0	0	1	133	100	100
1	0	1	100	100	100

<Core Design>

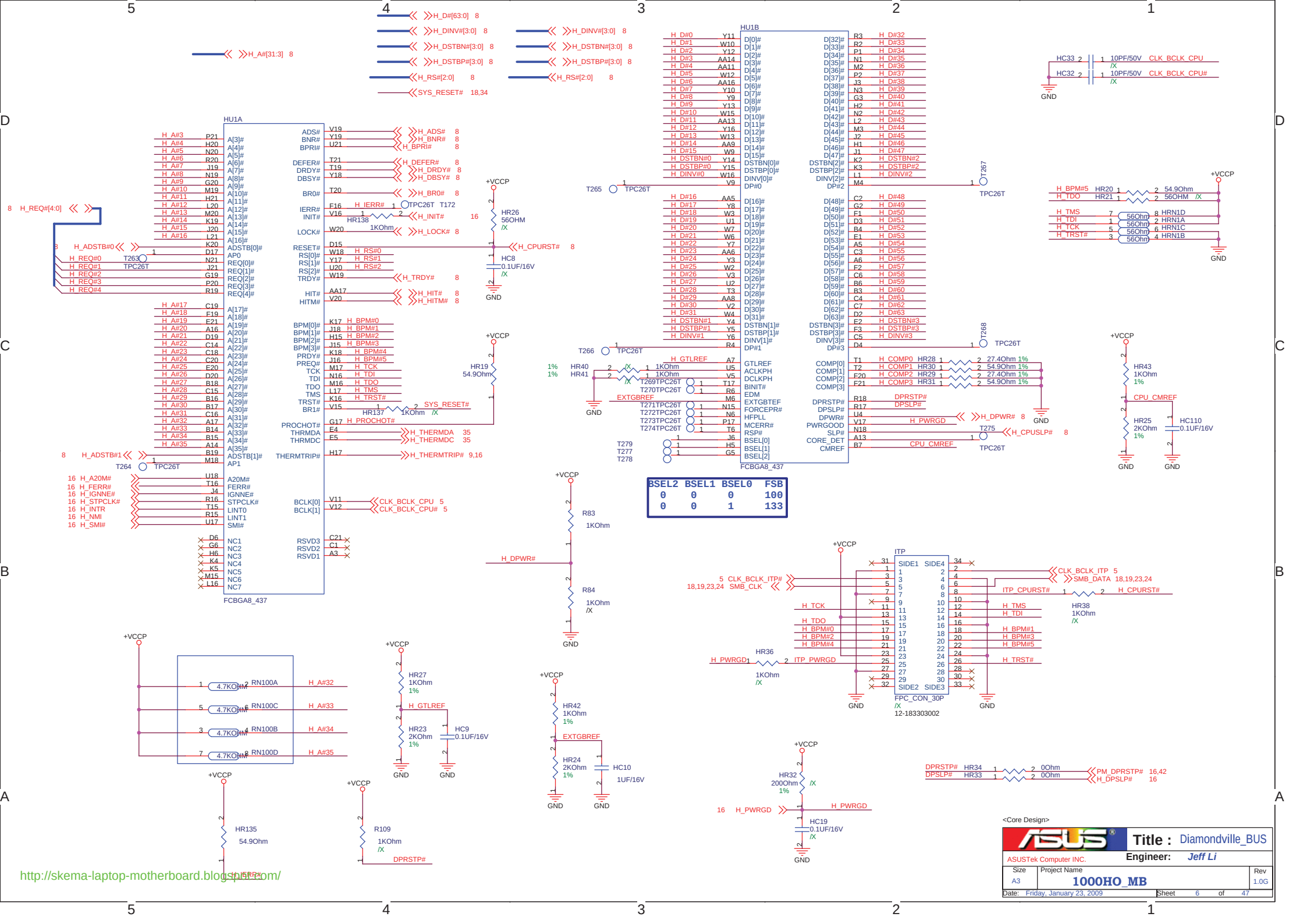
ASUSTek Computer INC.

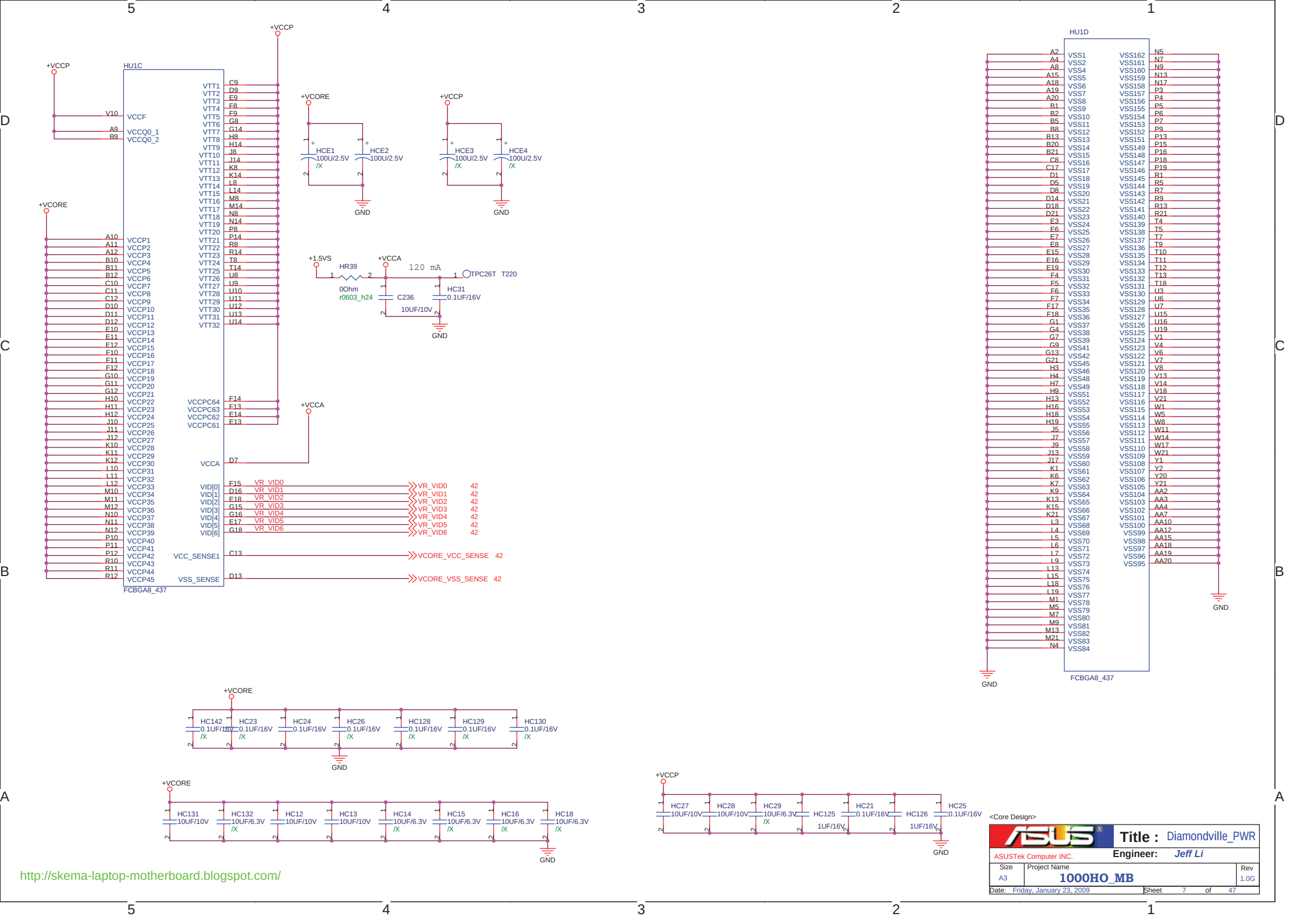
Title : Clock Gen_ICS9LPRS427

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 5 of 47





<Core Design>

Title : Diamondville_PWR

ASUSTek Computer INC.

Engineer: Jeff Li

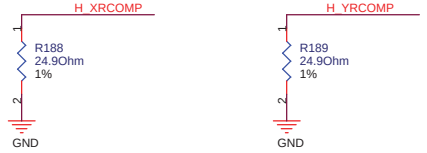
Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 7 of 47

Power :
+VCCP

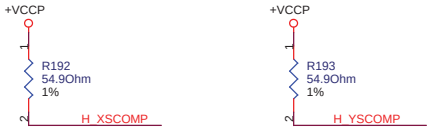
RCOMP

For Calibrating the FSB I/O Buffer



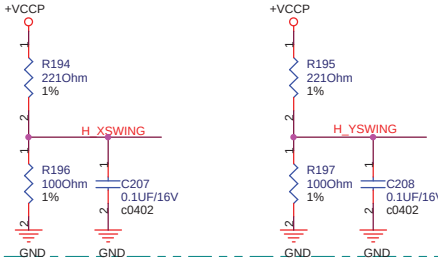
SCOMP

For Slew Rate Compenssation on the FSB

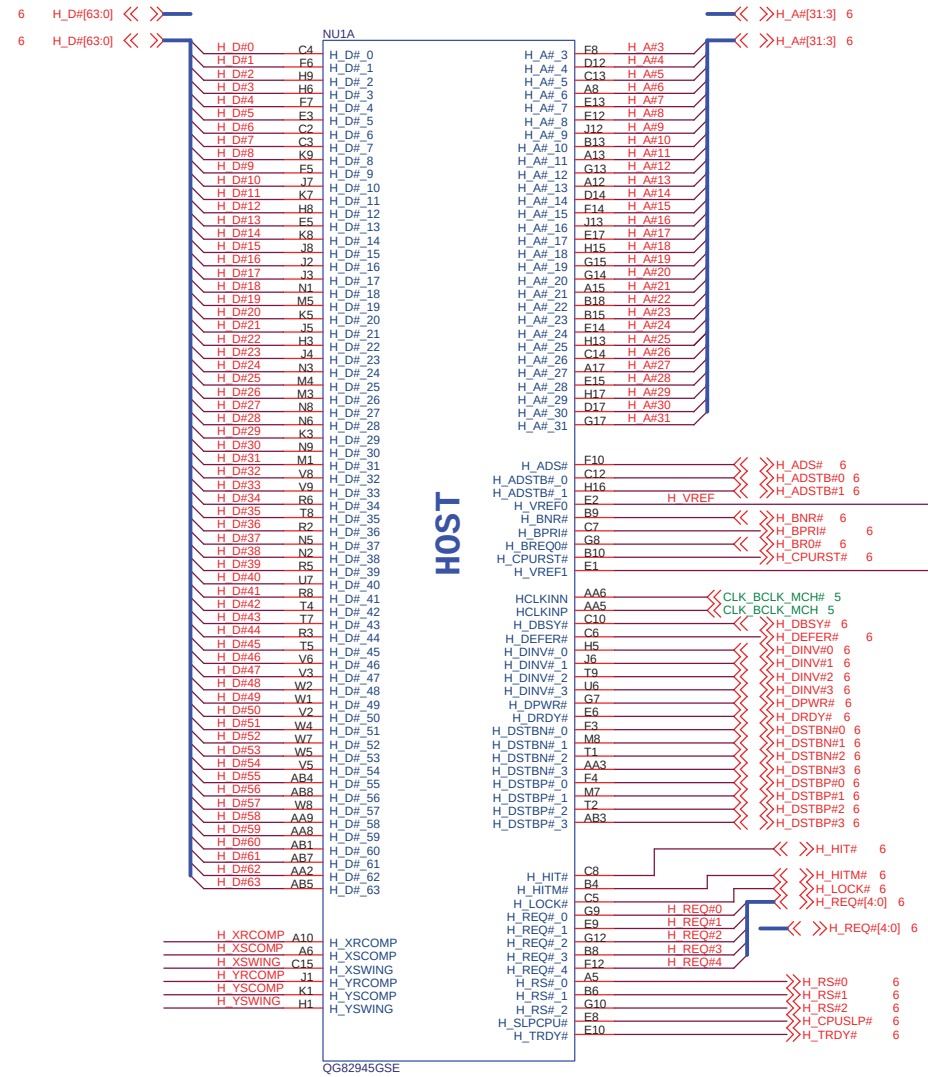


Voltage Swing

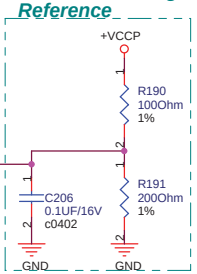
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing



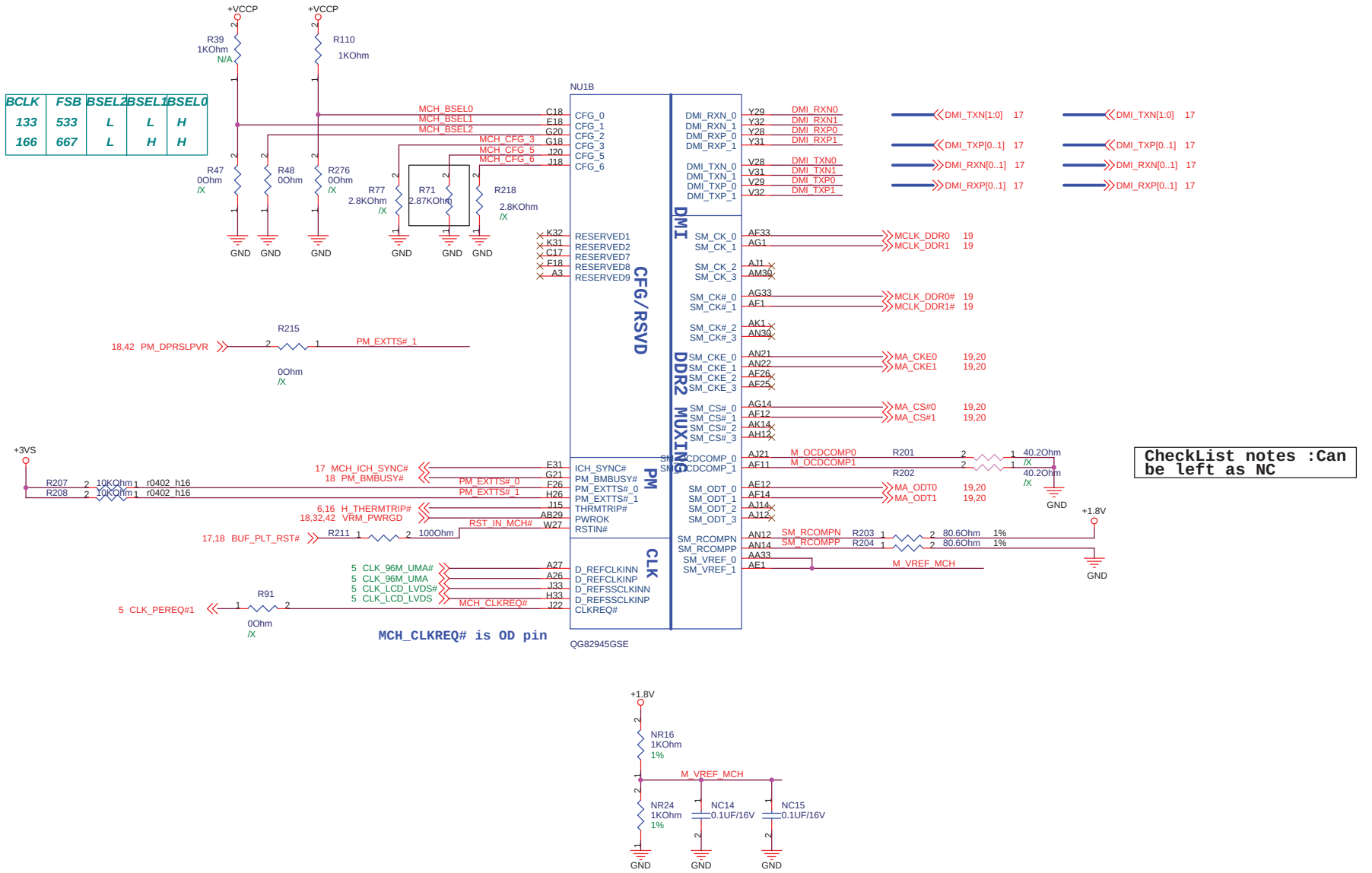
AGTL+ I/O Voltage Reference

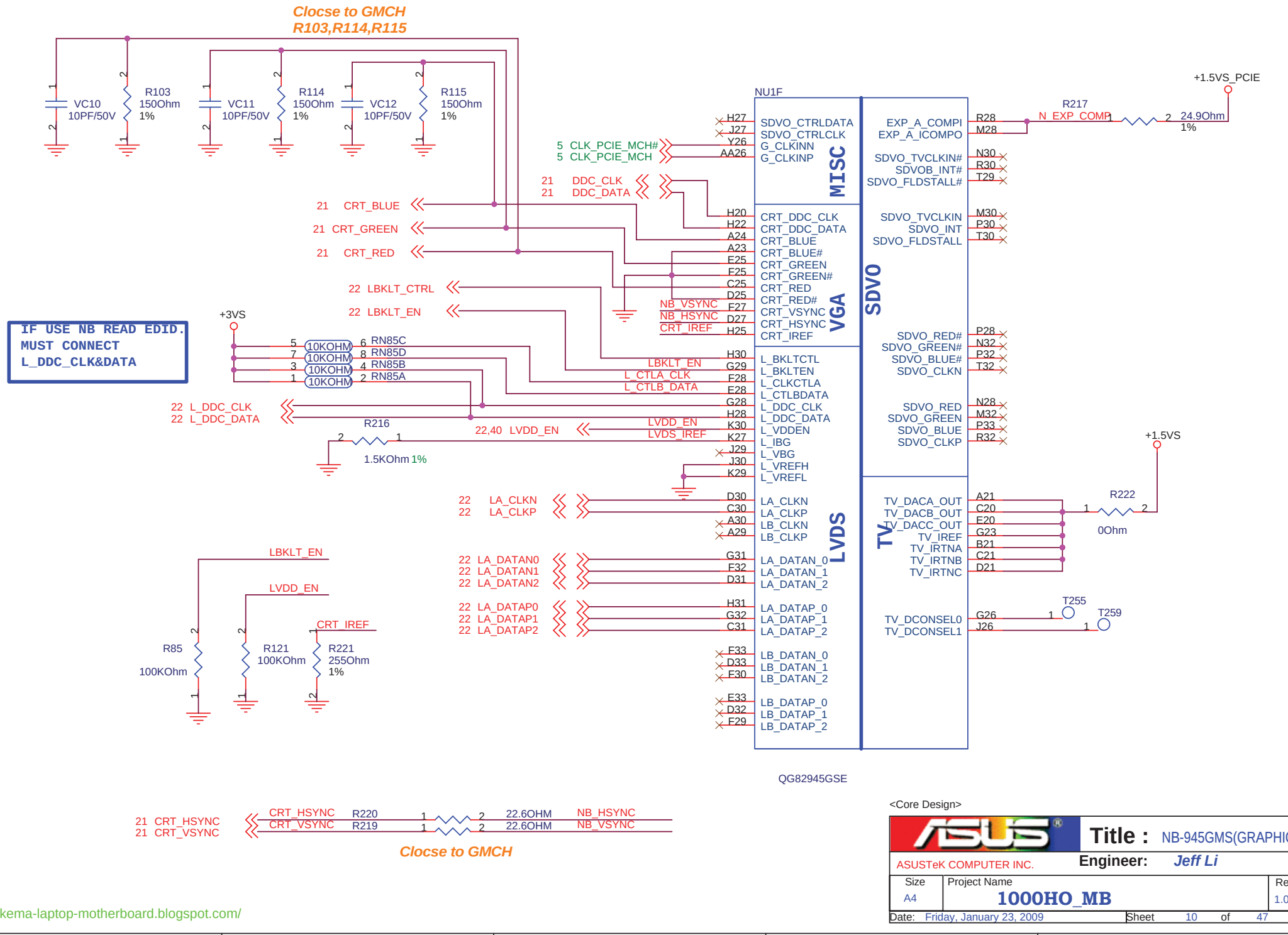


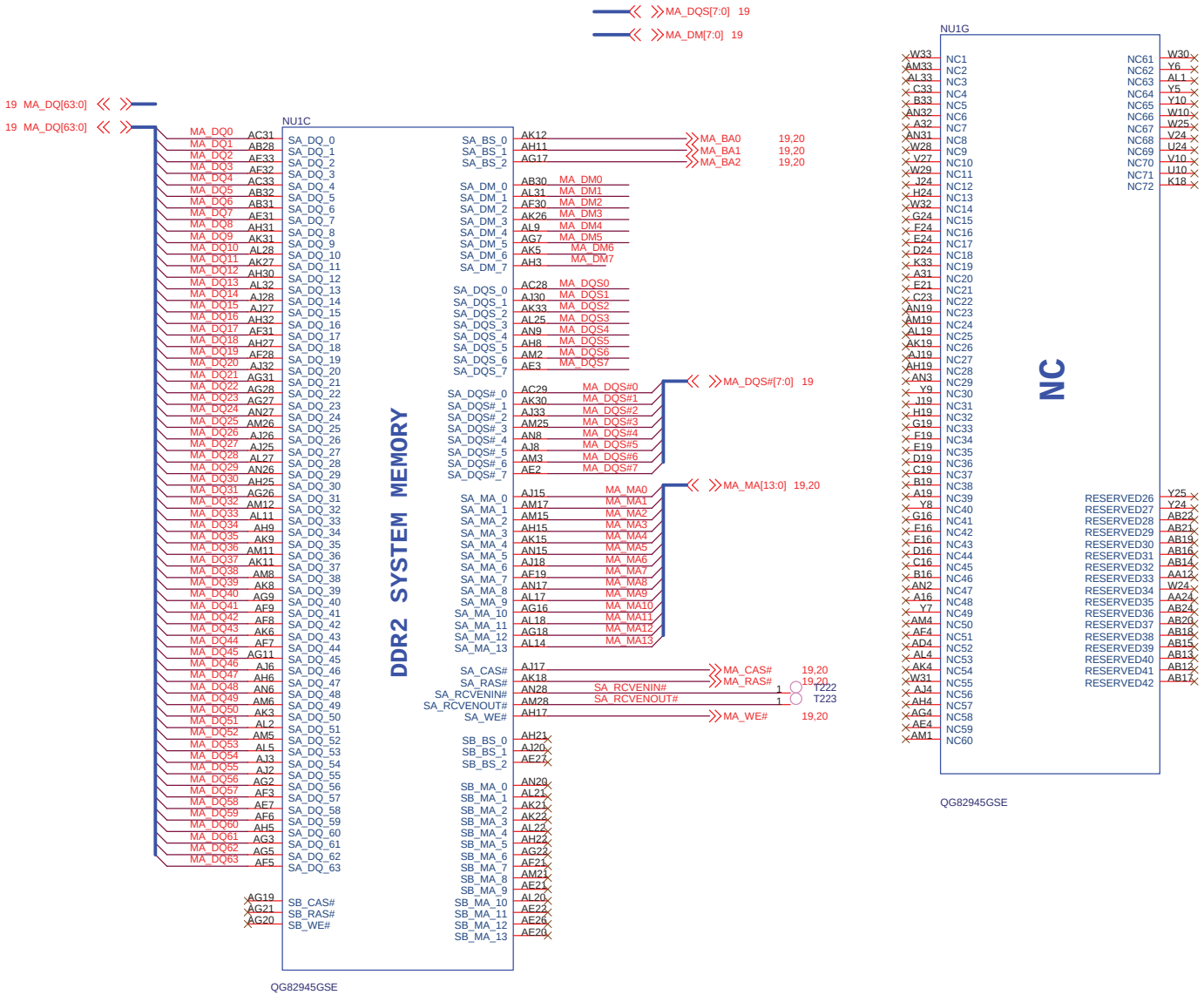
Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

<Core Design>

ASUSTeK COMPUTER INC.	Title : NB-945GMS(HOST)	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 8 of 47	




Clocse to GMCH
R103,R114,R115
VC10
10PF/50V
R103
150Ohm
1%
VC11
10PF/50V
R114
150Ohm
1%
VC12
10PF/50V
R115
150Ohm
1%
NU1F
MISC
SDVO_CTRLDATA
SDVO_CTRLCLK
G_CLKINN
G_CLKINP
5 CLK_PCIE_MCH#
5 CLK_PCIE_MCH
21 DDC_CLK
21 DDC_DATA
VGA
CRT_DDC_CLK
CRT_DDC_DATA
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_VSYNC
CRT_HSYNC
CRT_IREF
21 CRT_BLUE
21 CRT_GREEN
21 CRT_RED
22 LBKLT_CTRL
22 LBKLT_EN
NB_VSYNC
NB_HSYNC
CRT_IREF
IF USE NB READ EDID.
MUST CONNECT
L_DDC_CLK&DATA
+3VS
RN85C
RN85D
RN85B
RN85A
10KOHM
22 L_DDC_CLK
22 L_DDC_DATA
R216
1.5KOhm 1%
22,40 LVDD_EN
LVDS
L_BKLTCTL
L_BKLTEN
L_CLKCTLA
L_CTLBDATA
L_DDC_CLK
L_DDC_DATA
L_VDDEN
L_IBG
L_VBG
L_VREFH
L_VREFL
LBKLT_EN
L_CTLA_CLK
L_CTLB_DATA
LVDD_EN
LVDS_IREF
22 LA_CLKN
22 LA_CLKP
LA_CLKN
LA_CLKP
LB_CLKN
LB_CLKP
22 LA_DATAN0
22 LA_DATAN1
22 LA_DATAN2
LA_DATAN_0
LA_DATAN_1
LA_DATAN_2
22 LA_DATAP0
22 LA_DATAP1
22 LA_DATAP2
LA_DATAP_0
LA_DATAP_1
LA_DATAP_2
LB_DATAN_0
LB_DATAN_1
LB_DATAN_2
LB_DATAP_0
LB_DATAP_1
LB_DATAP_2
SDVO
EXP_A_COMPI
EXP_A_ICOMPO
SDVO_TVCLKIN#
SDVOB_INT#
SDVO_FLDSTALL#
SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL
SDVO_RED#
SDVO_GREEN#
SDVO_BLUE#
SDVO_CLKN
SDVO_RED
SDVO_GREEN
SDVO_BLUE
SDVO_CLKP
TV
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
TV_DCONSEL0
TV_DCONSEL1
+1.5VS_PCIE
R217
N_EXP_COMP
24.9Ohm
1%
+1.5VS
R222
0Ohm
T255
T259
LBKLT_EN
LVDD_EN
CRT_IREF
R85
100KOhm
R121
100KOhm
R221
255Ohm
1%
21 CRT_HSYNC
21 CRT_VSYNC
CRT_HSYNC
CRT_VSYNC
R220
R219
22.6OHM
NB_HSYNC
NB_VSYNC
Clocse to GMCH
QG82945GSE
<Core Design>
Title : NB-945GMS(GRAPHIC)
ASUSTeK COMPUTER INC.
Engineer: Jeff Li
Size A4
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 10 of 47
http://skema-laptop-motherboard.blogspot.com/



<Core Design>

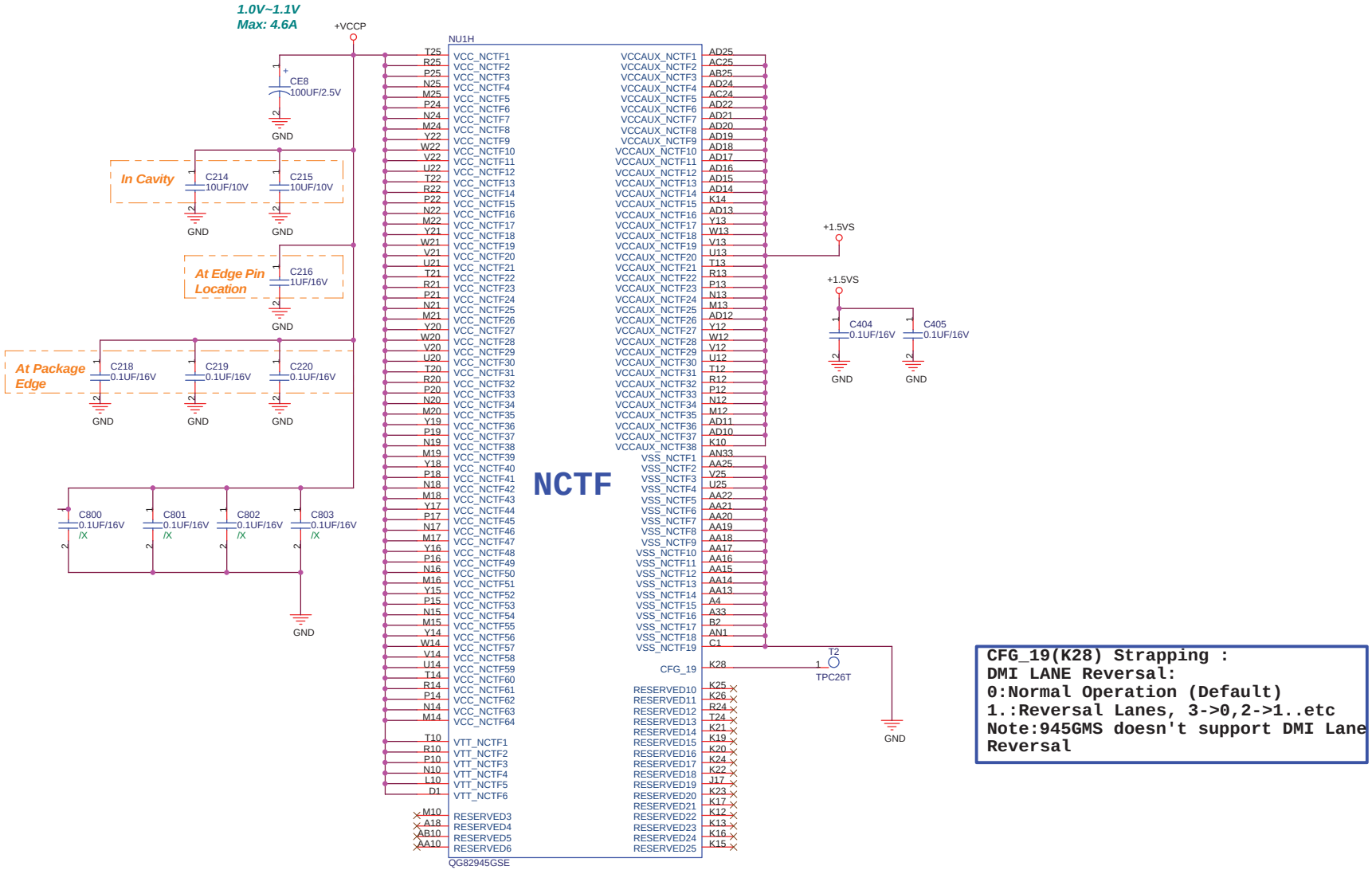
ASUSTeK COMPUTER INC.

Title : NB-945GMS(DDR2)

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 11 of 47



<Core Design>

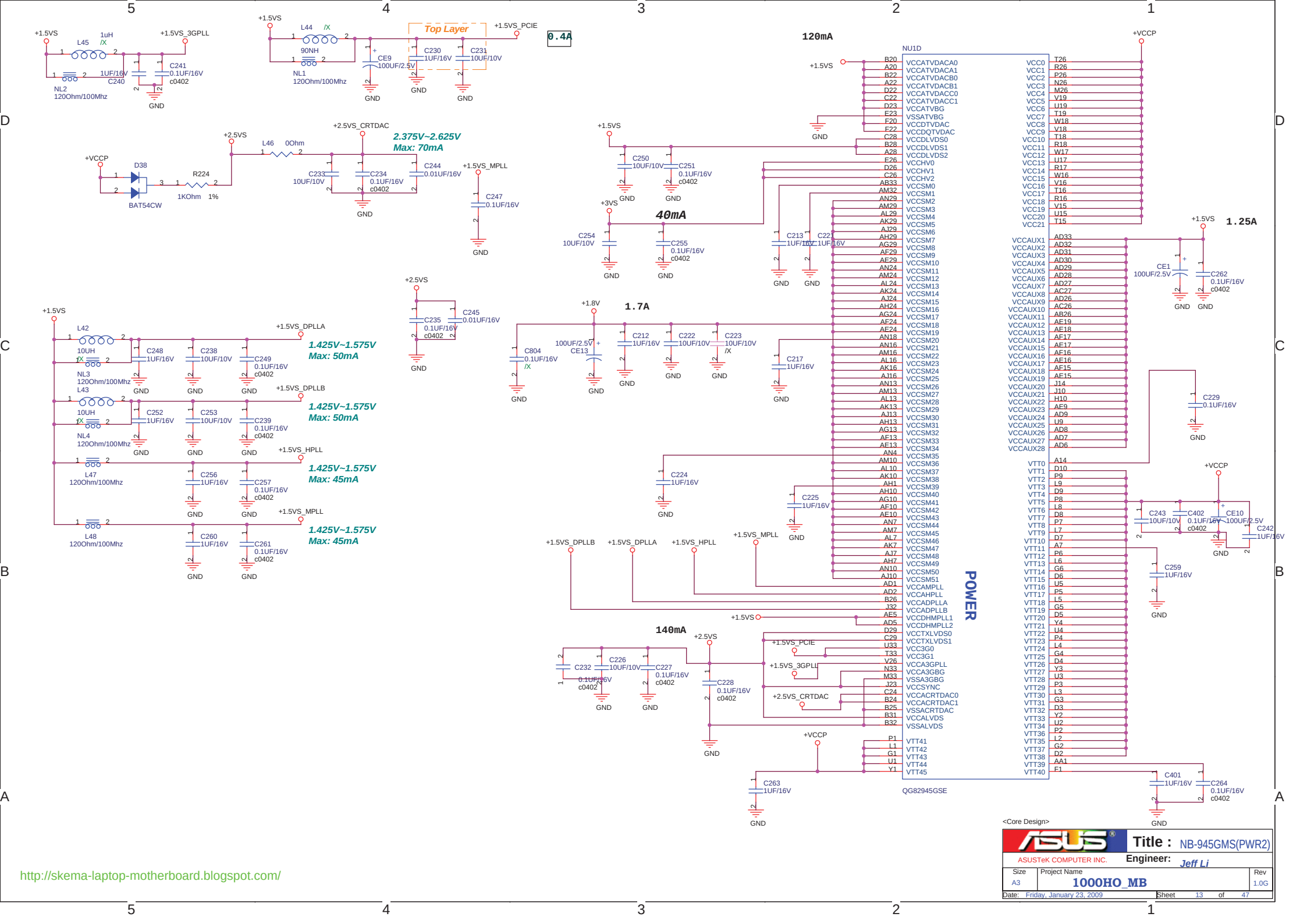
Title : NB-945GMs(PWR)

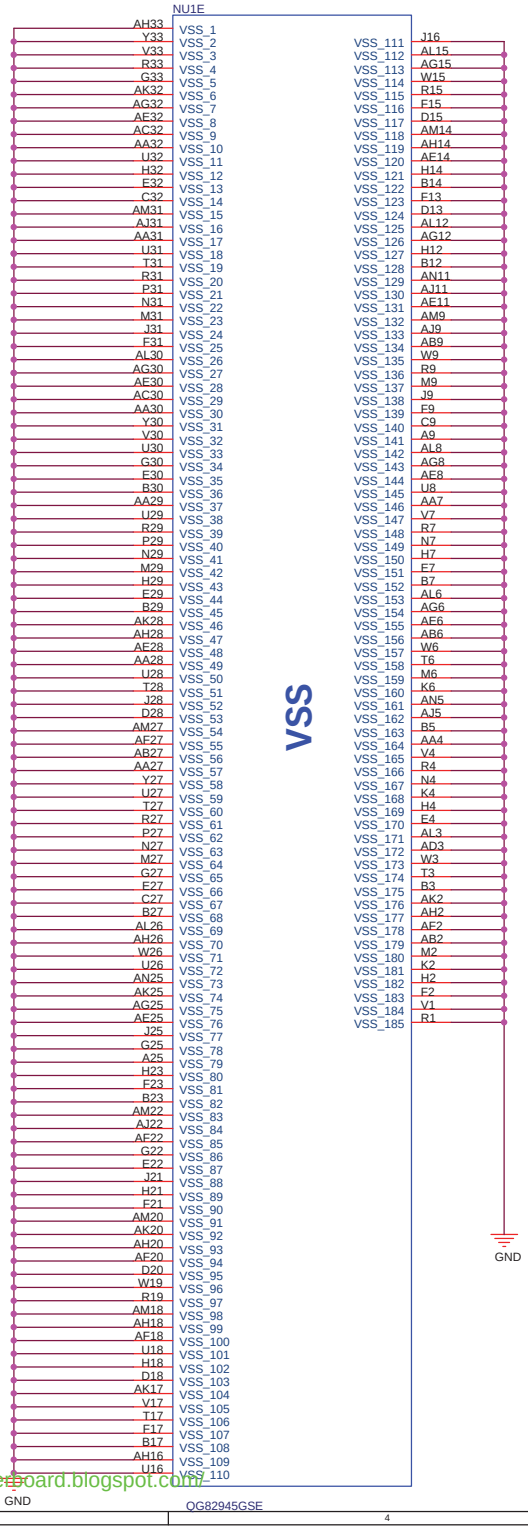
ASUSTeK COMPUTER INC.

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 12 of 47





<Core Design>

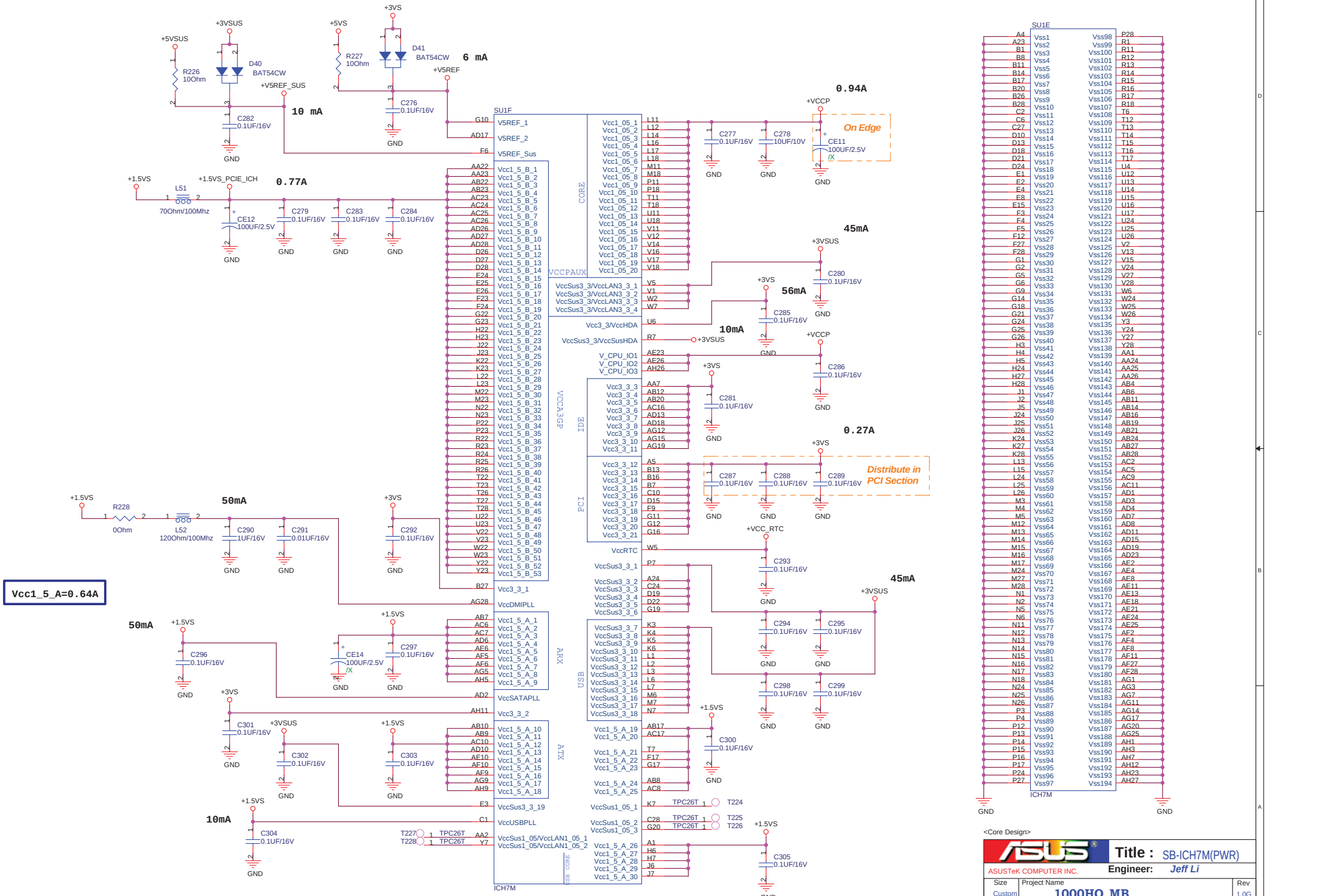
ASUSTeK COMPUTER INC.

Title : NB-945PMS(GND)

Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 14 of 47



<Core Design>

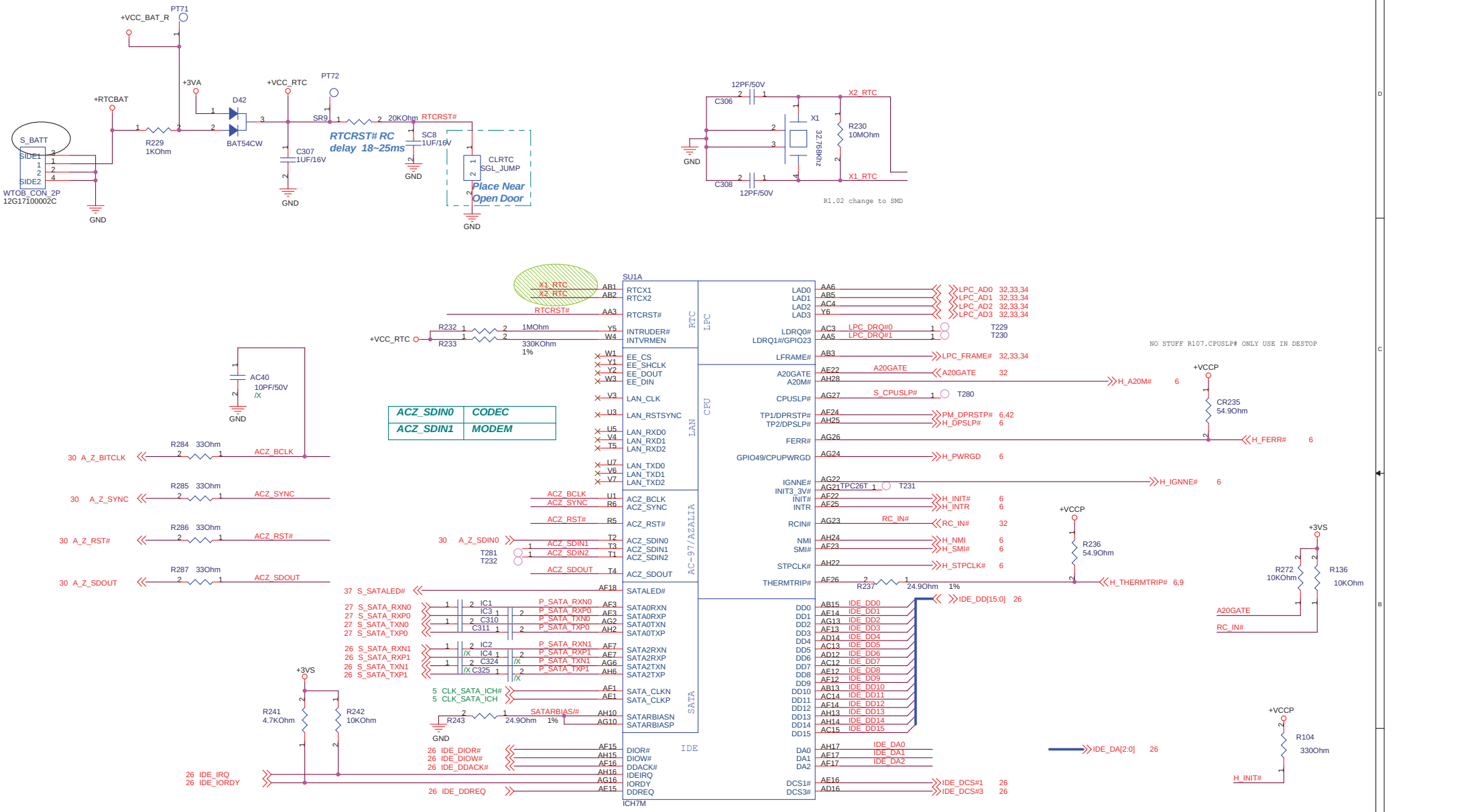
ASUSTeK COMPUTER INC.

Title : SB-ICH7M(PWR)

Engineer: Jeff Li

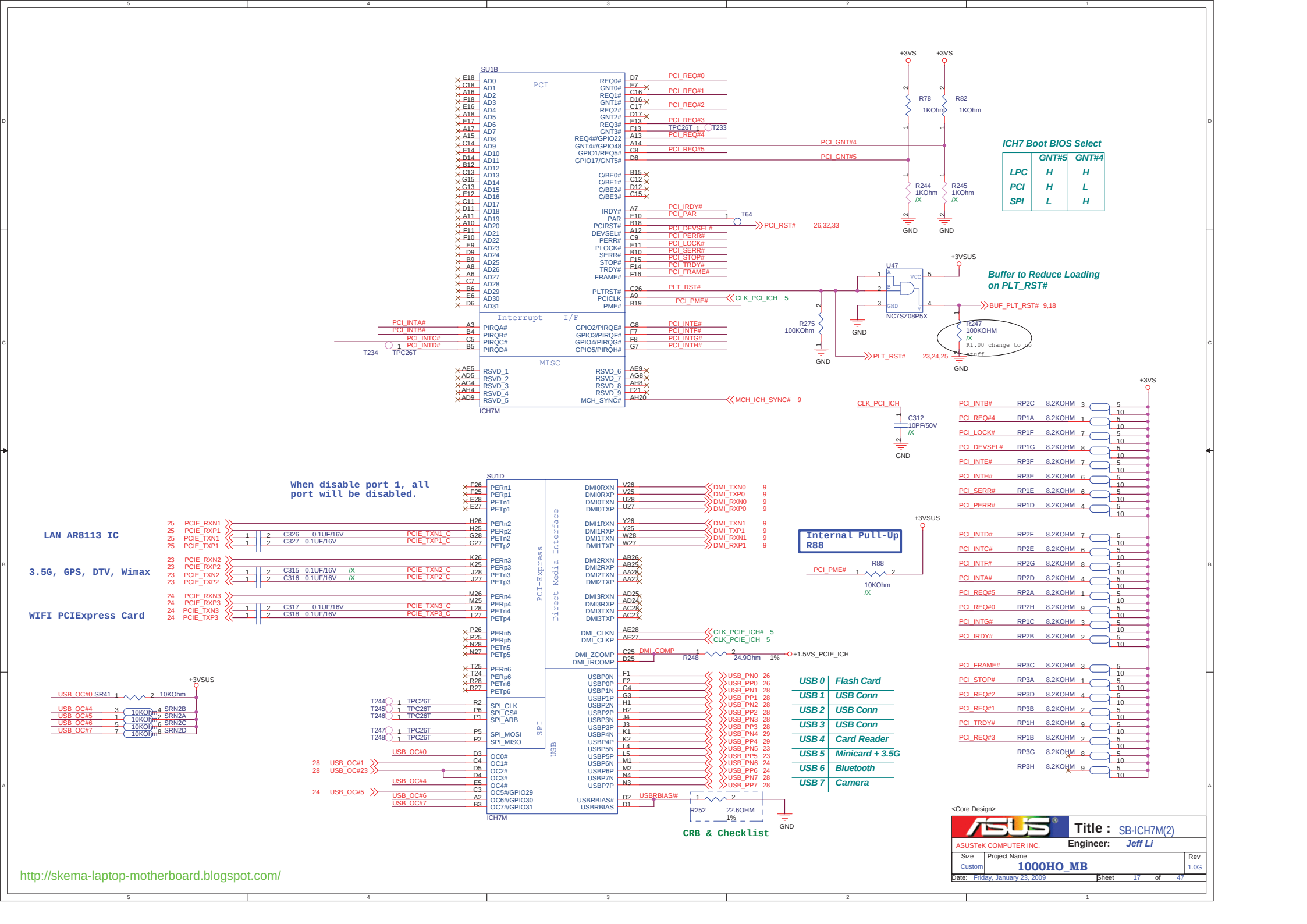
Size	Project Name	Rev
Custom	1000HO_MB	1.0G

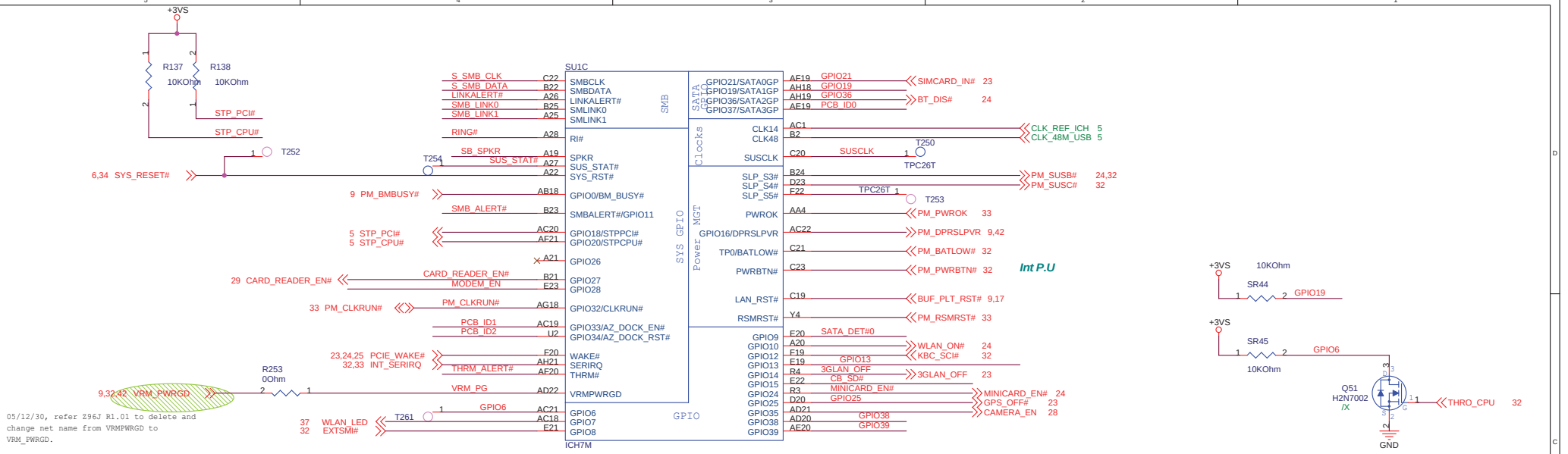
Date: Friday, January 23, 2009 Sheet 15 of 47

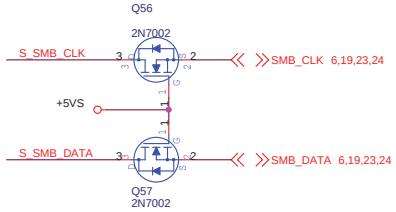


<Core Design>

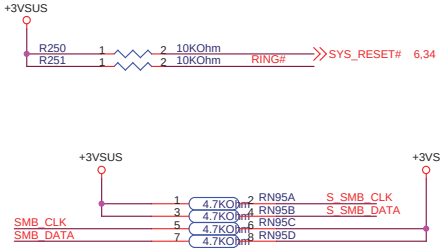
ASUSTeK COMPUTER INC.	Title : SB-ICH7-M(1)	
	Engineer: Jeff Li	
Size: Custom	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 16 of 47	

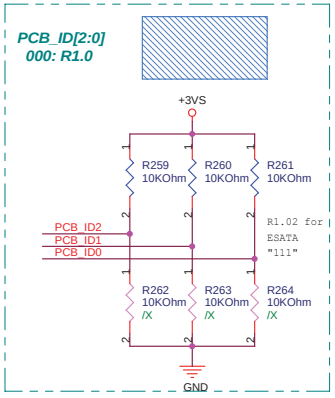






WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x





PCB_VID3 : PROJECT CODE

<Core Design>

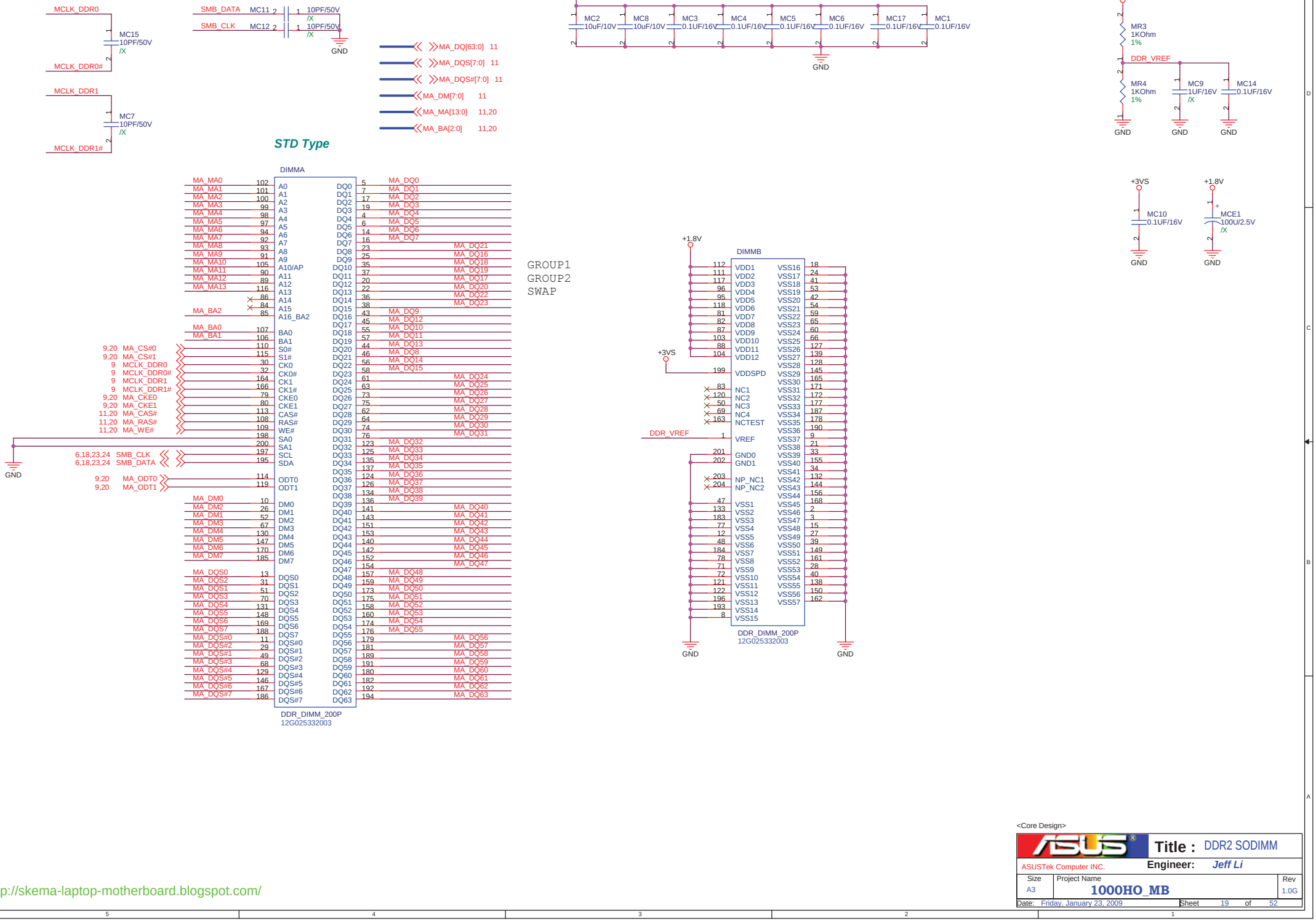
ASUSTeK COMPUTER INC

Title : SB-ICH7M(3)

Engineer: Jeff Li

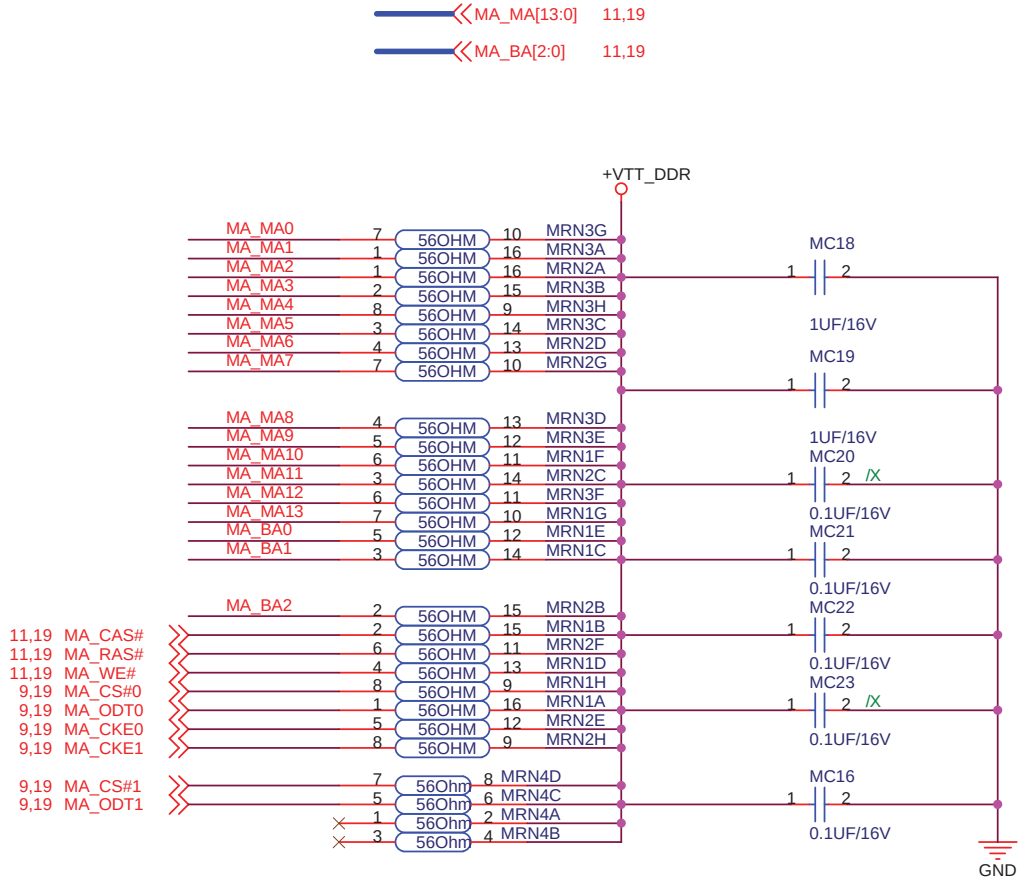
Size	Project Name	Rev
Custom	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 18 of 47



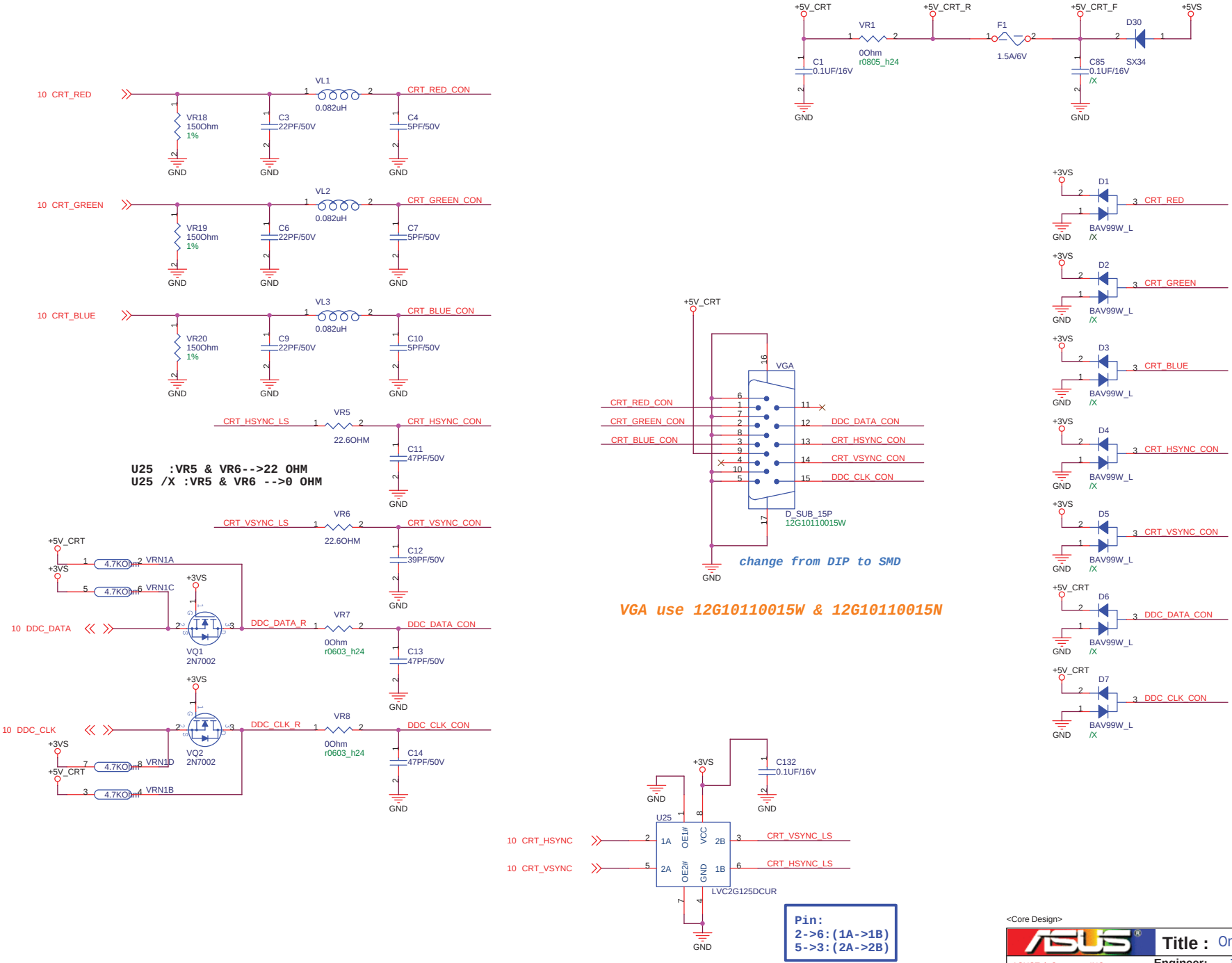
<Core Design>

ASUSTek Computer INC.	Title : DDR2 SODIMM	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 19 of 52	



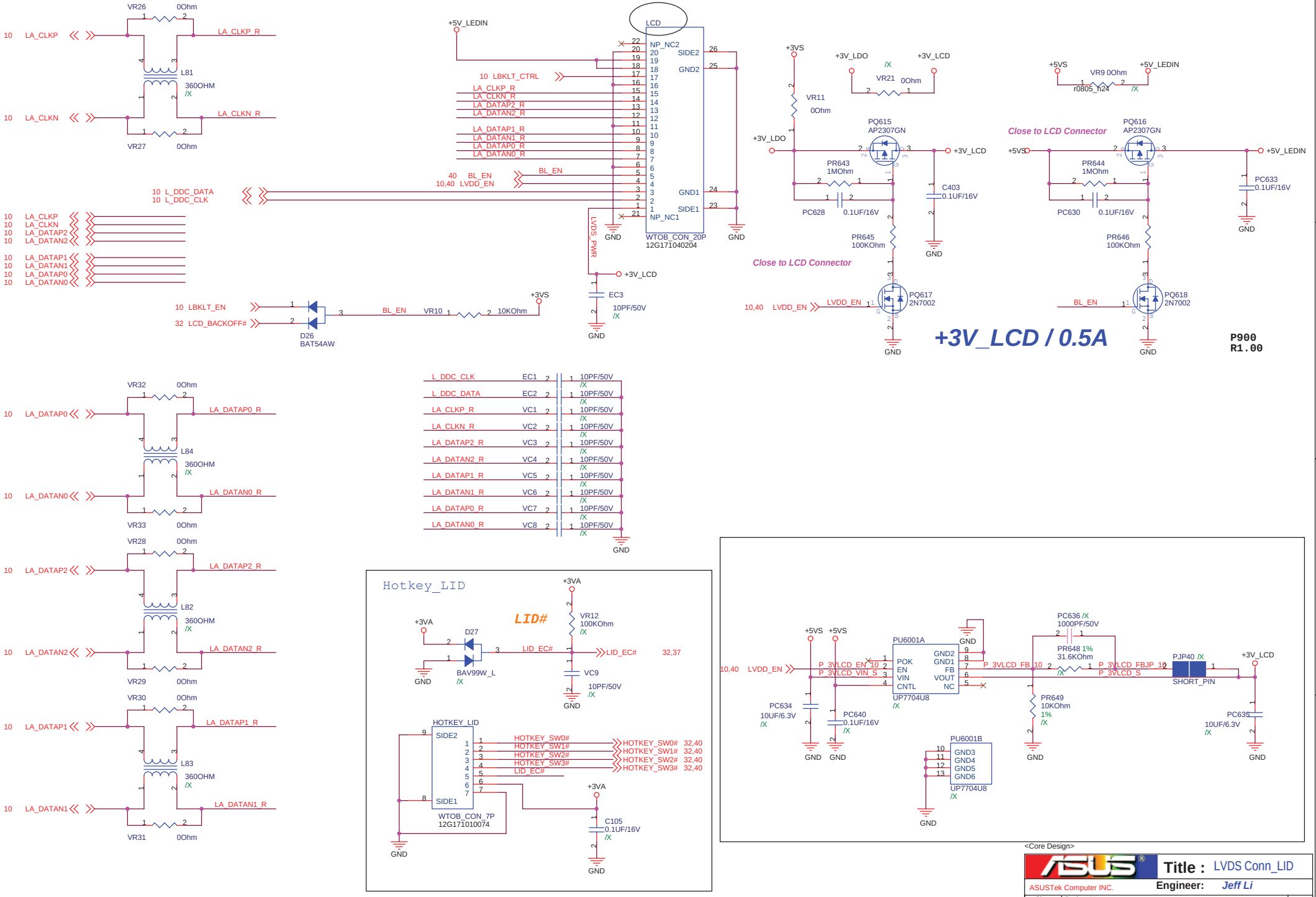
<Core Design>

ASUSTek Computer INC.	Title : DDR2_Termination	
	Engineer: *Jeff Li*	
Size: A4	Project Name: **1000HO_MB**	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 20 of 52	



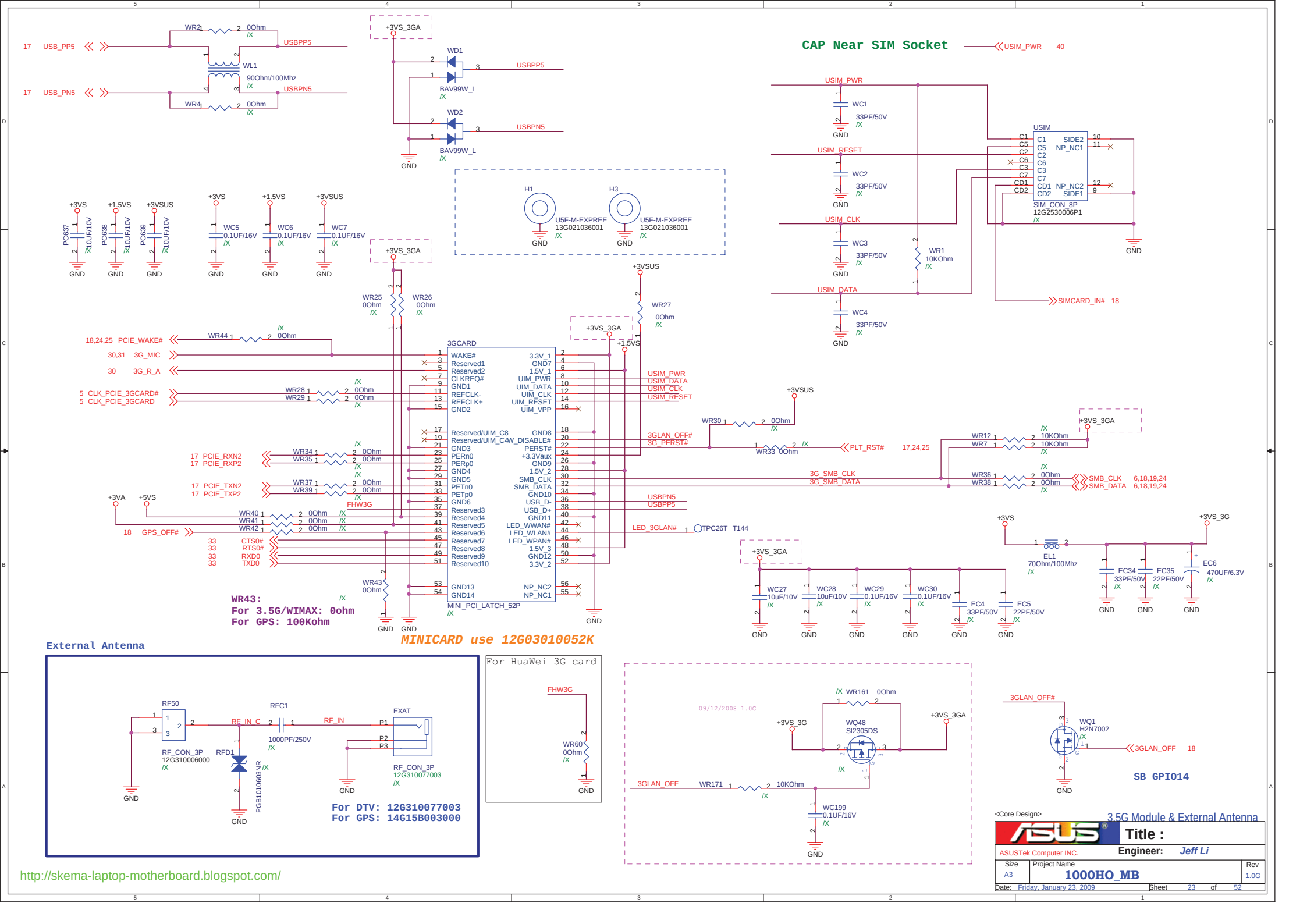
<Core Design>

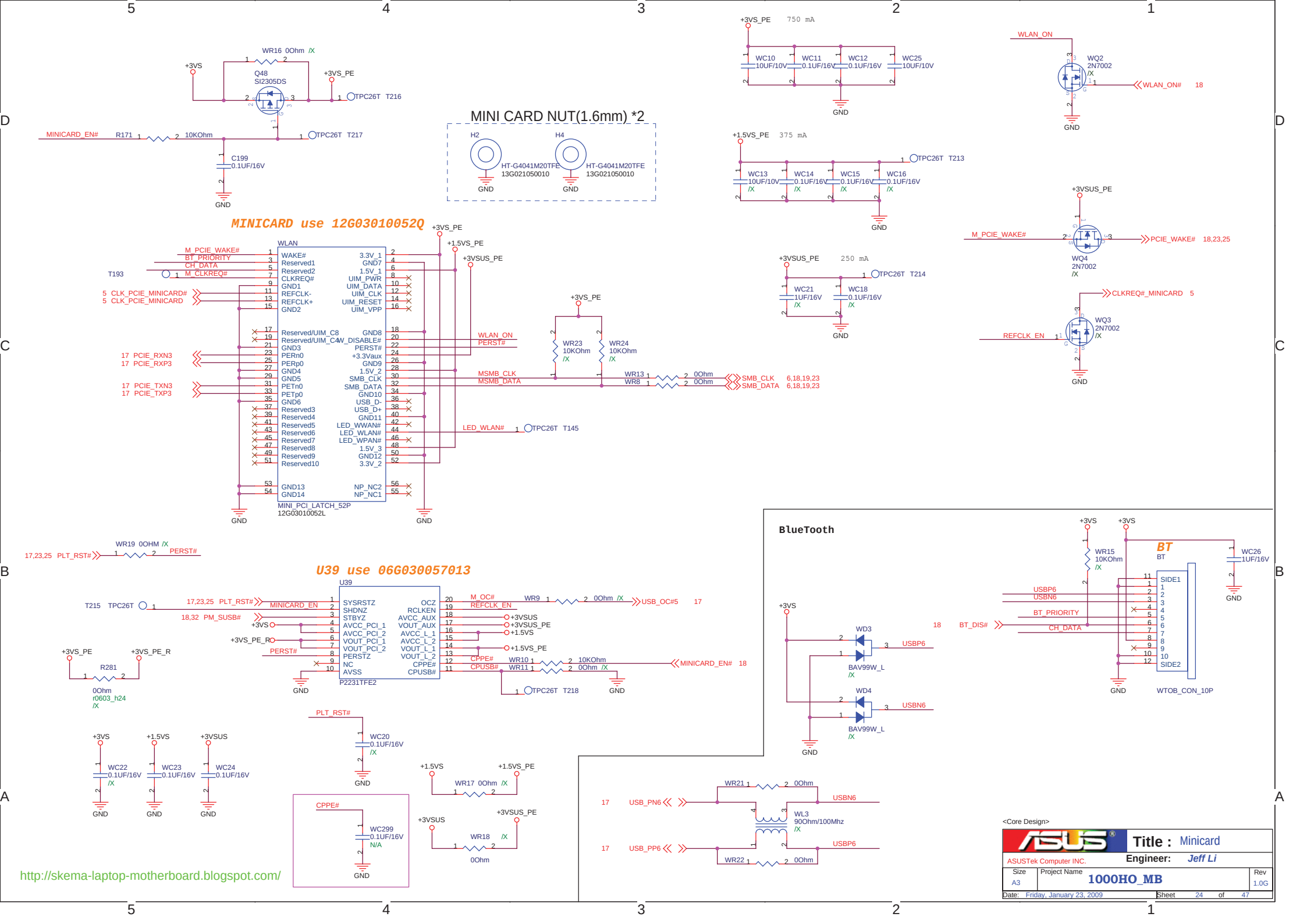
ASUSTek Computer INC.	Title : Onboard VGA	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 21 of 52	

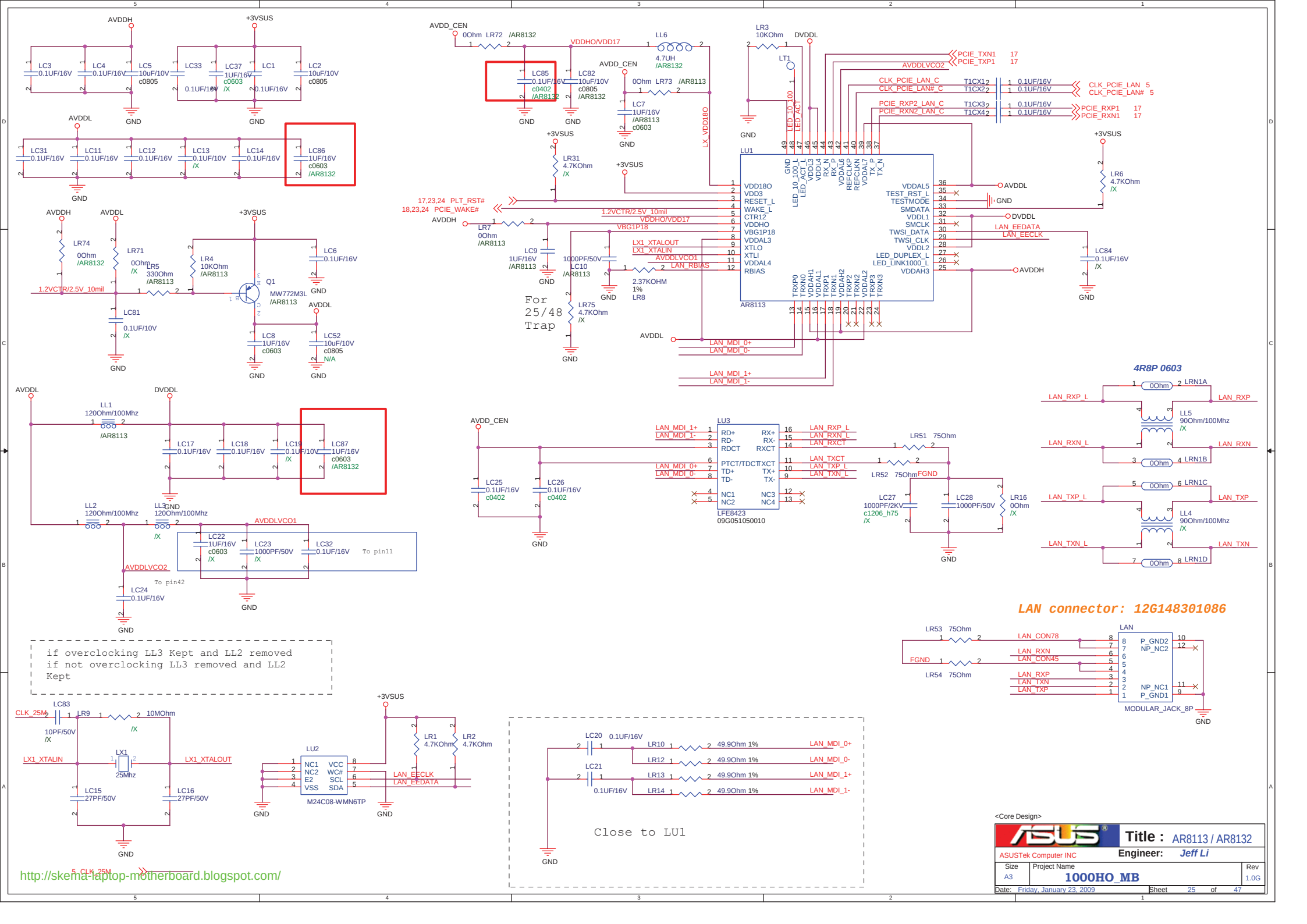


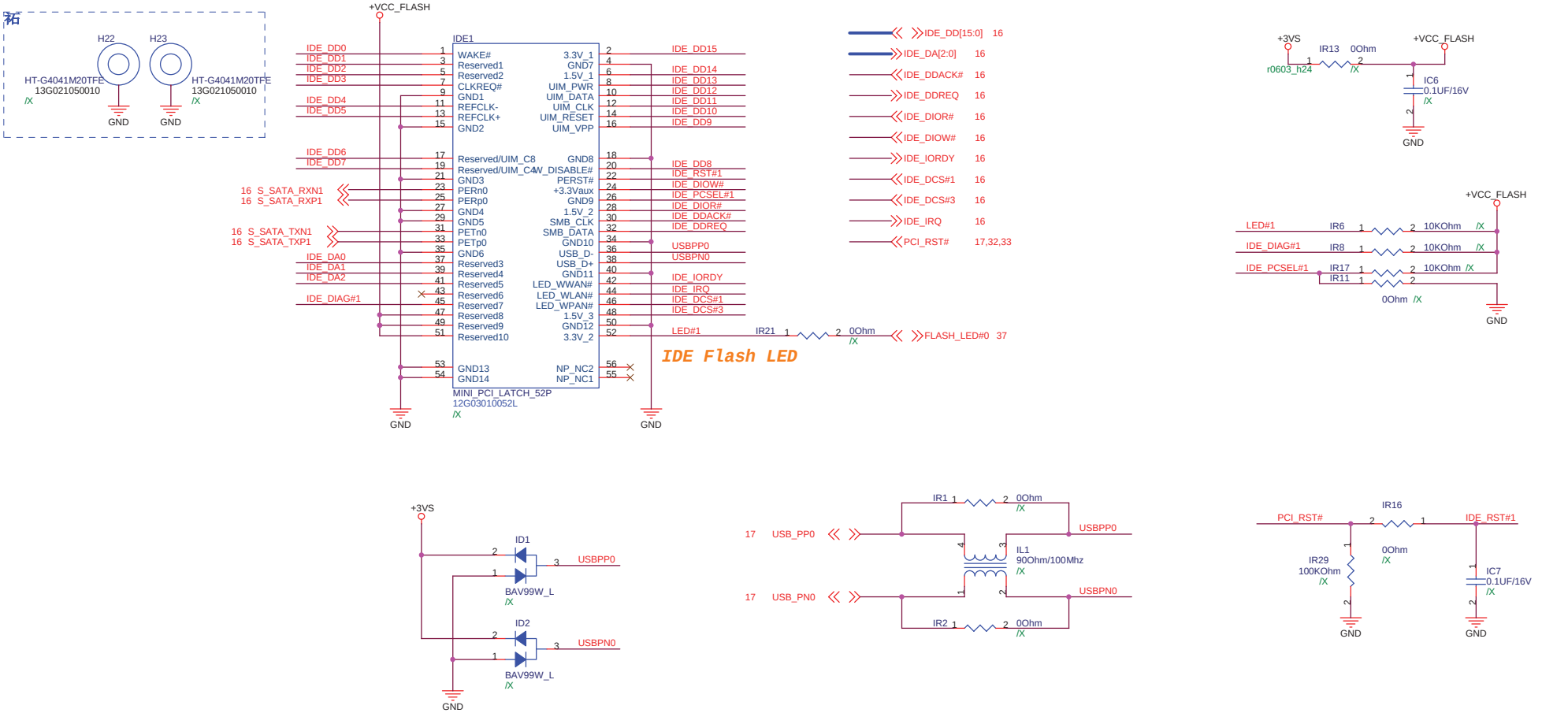
<Core Design>

ASUSTek Computer INC.	Title : LVDS Conn_LID	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 22 of 52	




MINI CARD NUT(1.6mm) *2
MINICARD use 12G03010052Q
U39 use 06G030057013
BlueTooth
WLAN
MINI_PCI_LATCH_52P
12G03010052L
U39
P2231TFE2
BT
WTOB_CON_10P
Title : Minicard
ASUSTek Computer INC.
Engineer: Jeff Li
1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 24 of 47
<Core Design>
http://skema-laptop-motherboard.blogspot.com/


AVDDH
+3VSUS
LC3 0.1UF/16V
LC4 0.1UF/16V
LC5 10uF/10V c0805
LC33 0.1UF/16V
LC37 1UF/16V c0603 /X
LC1 0.1UF/16V
LC2 10uF/10V c0805
GND
AVDDL
LC31 0.1UF/16V
LC11 0.1UF/16V
LC12 0.1UF/16V
LC13 0.1UF/16V /X
LC14 0.1UF/16V
LC86 1UF/16V c0603 /AR8132
LR74 0Ohm /AR8132
LR71 0Ohm /X
LR5 330Ohm /AR8113
LR4 10KOhm /AR8113
1.2VCTR/2.5V_10mil
Q1 MW772M3L /AR8113
LC6 0.1UF/16V
LC81 0.1UF/10V /X
LC8 1UF/16V c0603
LC52 10uF/10V c0805 N/A
AVDD_CEN
0Ohm LR72 /AR8132
VDDHO/VDD17
LL6 4.7UH /AR8132
LC85 0.1UF/16V c0402 /AR8132
LC82 10uF/10V c0805 /AR8132
0Ohm LR73 /AR8113
LC7 1UF/16V /AR8113 c0603
LX_VDD18O
LR3 10KOhm
DVDDL
LT1
LED_10_100
LED_ACT
PCIE_TXN1 17
PCIE_TXP1 17
AVDDLVCO2
CLK_PCIE_LAN_C
CLK_PCIE_LAN#_C
T1CX1 2
T1CX2 2
0.1UF/16V
CLK_PCIE_LAN 5
CLK_PCIE_LAN# 5
PCIE_RXP2_LAN_C
PCIE_RXN2_LAN_C
T1CX3 2
T1CX4 2
PCIE_RXP1 17
PCIE_RXN1 17
LR31 4.7KOhm /X
17,23,24 PLT_RST#
18,23,24 PCIE_WAKE#
LR7 0Ohm /AR8113
LC9 1UF/16V /AR8113
1000PF/50V
LC10 /AR8113
2.37KOHM 1% LR8
LR75 4.7KOhm /X
For 25/48 Trap
LU1
VDD18O
VDD3
RESET_L
WAKE_L
CTR12
VDDHO
VBG1P18
VDDAL3
XTLO
XTLI
VDDAL4
RBIAS
AR8113
1.2VCTR/2.5V_10mil
VDDHO/VDD17
VBG1P18
LX1_XTALOUT
LX1_XTALIN
AVDDLVCO1
LAN_RBIAS
VDDAL5
TEST_RST_L
TESTMODE
SMDATA
VDDL1
SMCLK
TWSI_DATA
TWSI_CLK
VDDL2
LED_DUPLEX_L
LED_LINK1000_L
VDDAH3
LAN_EEDATA
LAN_EECLK
LR6 4.7KOhm /X
LC84 0.1UF/16V /X
LAN_MDI_0+
LAN_MDI_0-
LAN_MDI_1+
LAN_MDI_1-
LL1 120Ohm/100Mhz /AR8113
LC17 0.1UF/16V
LC18 0.1UF/16V
LC19 0.1UF/10V /X
LC87 1UF/16V c0603 /AR8132
LL2 120Ohm/100Mhz
LL3 120Ohm/100Mhz /X
LC22 1UF/16V c0603 /X
LC23 1000PF/50V /X
LC32 0.1UF/16V
To pin11
AVDDLVCO2
To pin42
LC24 0.1UF/16V
LU3
RD+
RD-
RDCT
PTCT/TDCT
TD+
TD-
RX+
RX-
RXCT
TXCT
TX+
TX-
NC1
NC2
NC3
NC4
LFE8423
09G051050010
LAN_MDI_1+
LAN_MDI_1-
LAN_MDI_0+
LAN_MDI_0-
LAN_RXP_L
LAN_RXN_L
LAN_RXCT
LAN_TXCT
LAN_TXP_L
LAN_TXN_L
LC25 0.1UF/16V c0402
LC26 0.1UF/16V c0402
LR51 75Ohm
LR52 75Ohm FGND
LC27 1000PF/2KV c1206_h75 /X
LC28 1000PF/50V
LR16 0Ohm /X
4R8P 0603
LRN1A
LRN1B
LRN1C
LRN1D
LL5 90Ohm/100Mhz /X
LL4 90Ohm/100Mhz /X
LAN_RXP
LAN_RXN
LAN_TXP
LAN_TXN
LAN connector: 12G148301086
LR53 75Ohm
LR54 75Ohm
LAN_CON78
LAN_CON45
LAN
P_GND2
NP_NC2
NP_NC1
P_GND1
MODULAR_JACK_8P
if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2 Kept
CLK_25M
LC83 10PF/50V /X
LR9 10MOhm /X
LX1 25Mhz
LX1_XTALIN
LX1_XTALOUT
LC15 27PF/50V
LC16 27PF/50V
LU2
M24C08-WMN6TP
LR1 4.7KOhm
LR2 4.7KOhm
LAN_EECLK
LAN_EEDATA
LC20 0.1UF/16V
LC21 0.1UF/16V
LR10 49.9Ohm 1%
LR12 49.9Ohm 1%
LR13 49.9Ohm 1%
LR14 49.9Ohm 1%
Close to LU1
<Core Design>
Title : AR8113 / AR8132
ASUSTek Computer INC
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 25 of 47
http://skema-laptop-motherboard.blogspot.com/

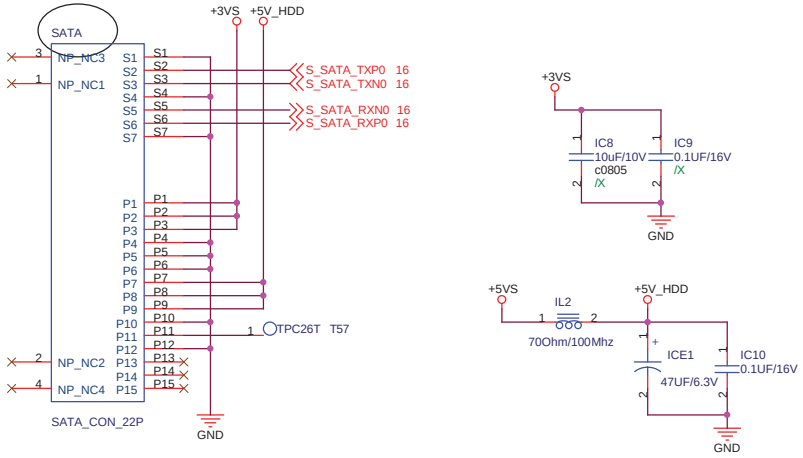


Naming Rule:
IC:IU?
R:IR?
C:IC?
L:IL?

<Core Design>

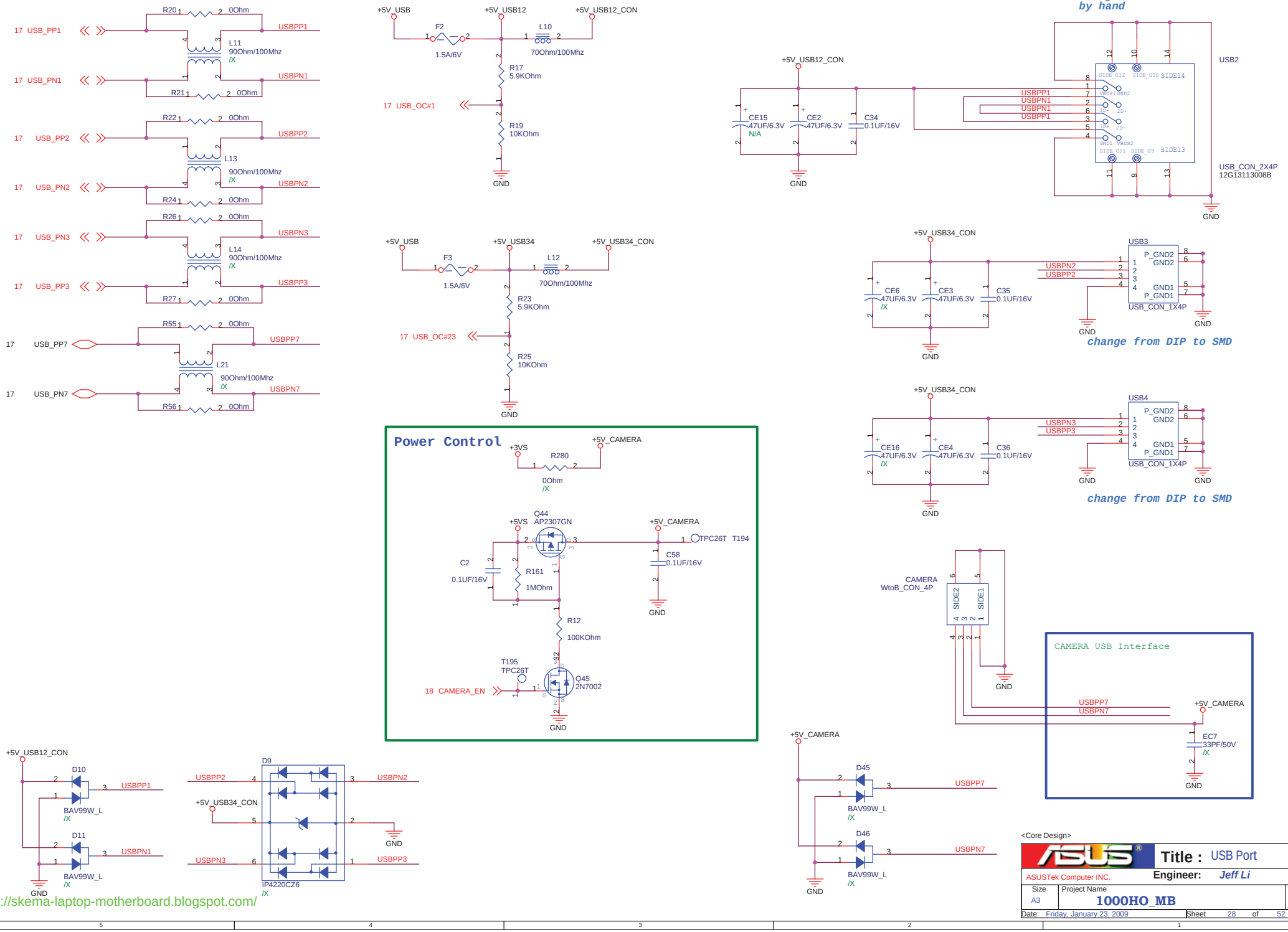
ASUSTek Computer INC.	Title : HD + Flash Conn	
	Engineer: Kell_Huang	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 26 of 47	

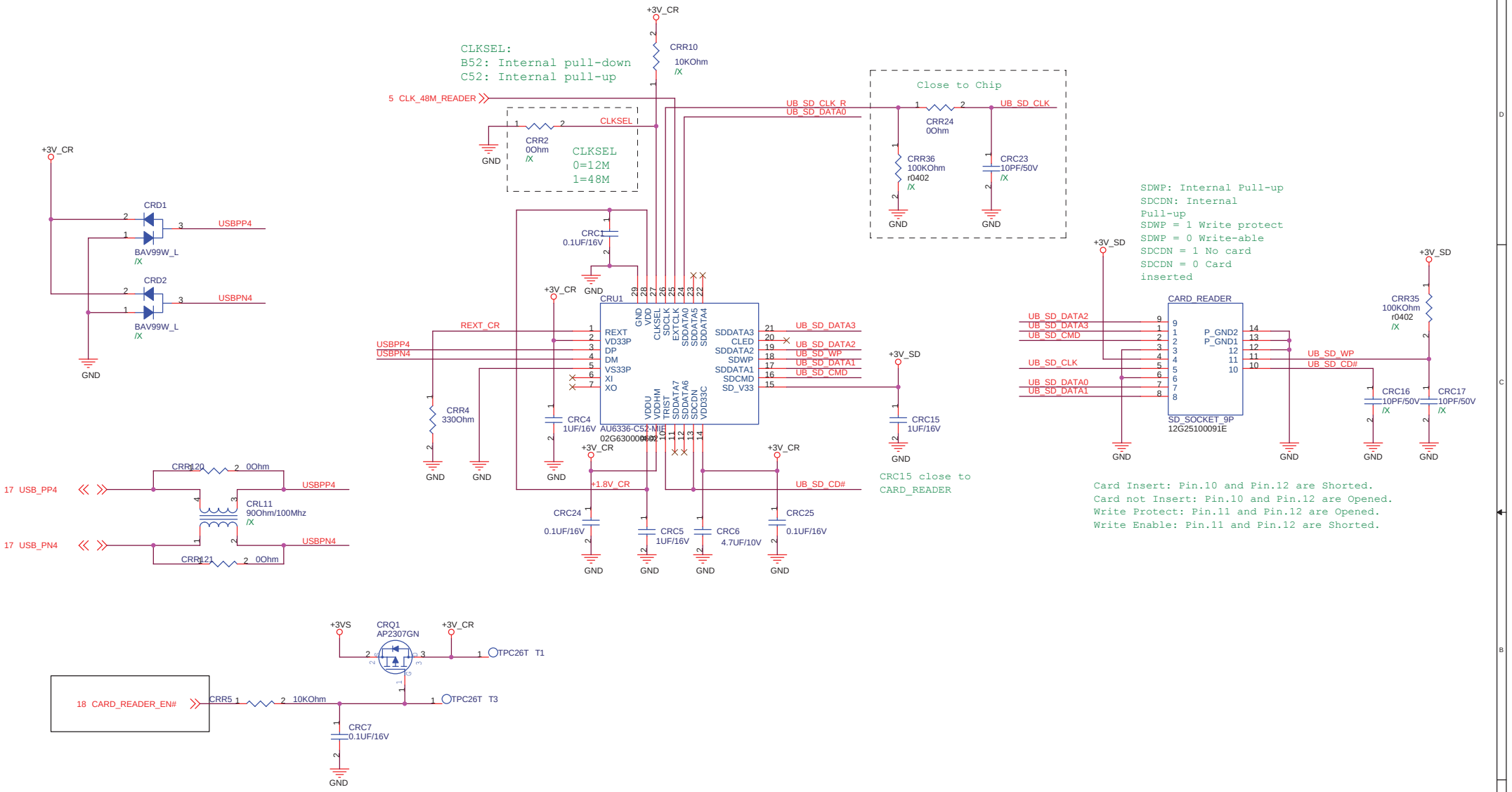
SATA HDD Connector



<Core Design>

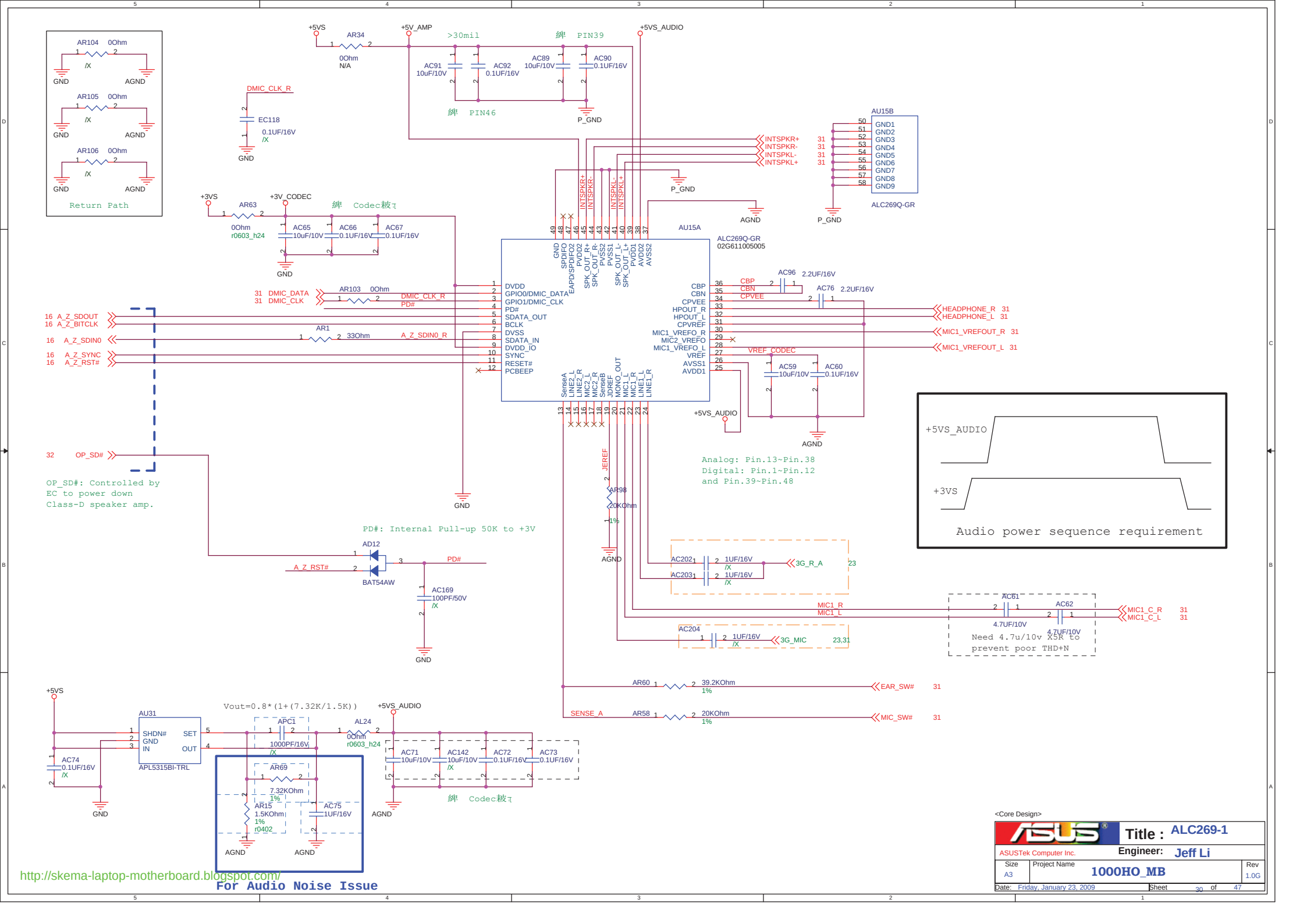
ASUSTek Computer INC.	Title : HDD	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 27 of 47	

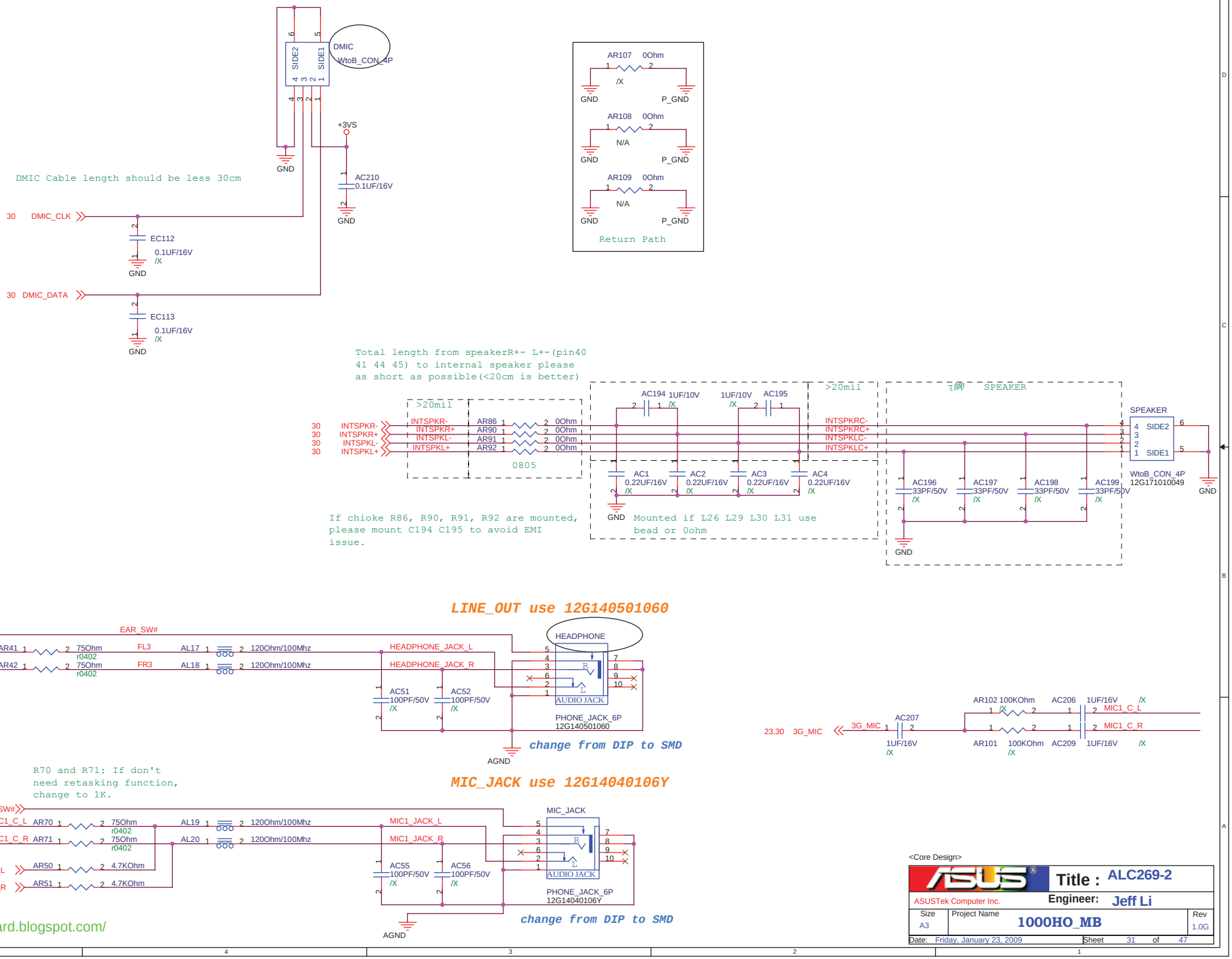

change from DIP to SMD by hand
USB2
USB_CON_2X4P
12G13113008B
USB3
USB4
USB_CON_1X4P
change from DIP to SMD
change from DIP to SMD
Power Control
Q44 AP2307GN
Q45 2N7002
TPC26T
CAMERA WtoB_CON_4P
CAMERA USB Interface
IP4220CZ6
BAV99W_L
Title : USB Port
ASUSTek Computer INC.
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 28 of 52
http://skema-laptop-motherboard.blogspot.com/

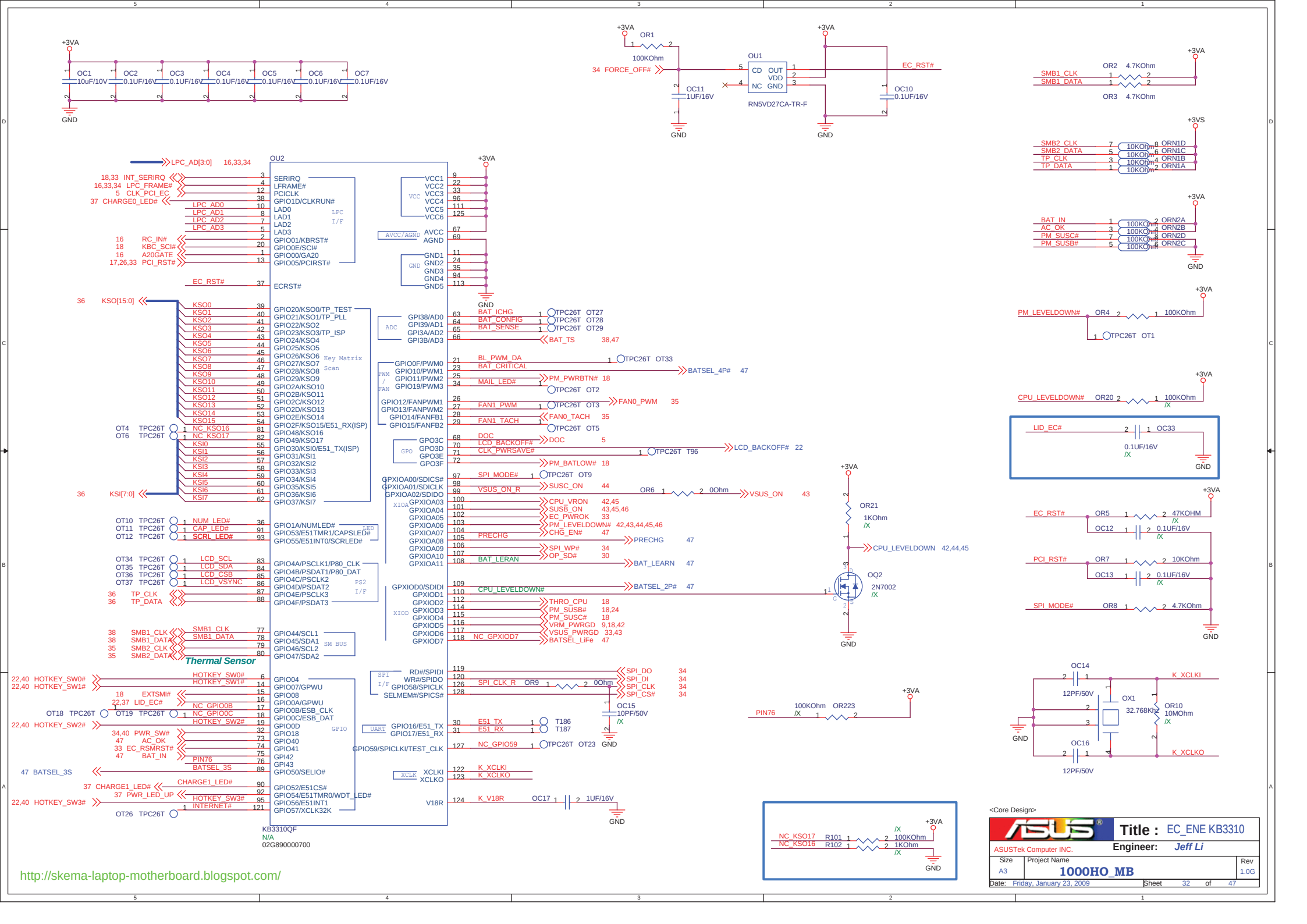


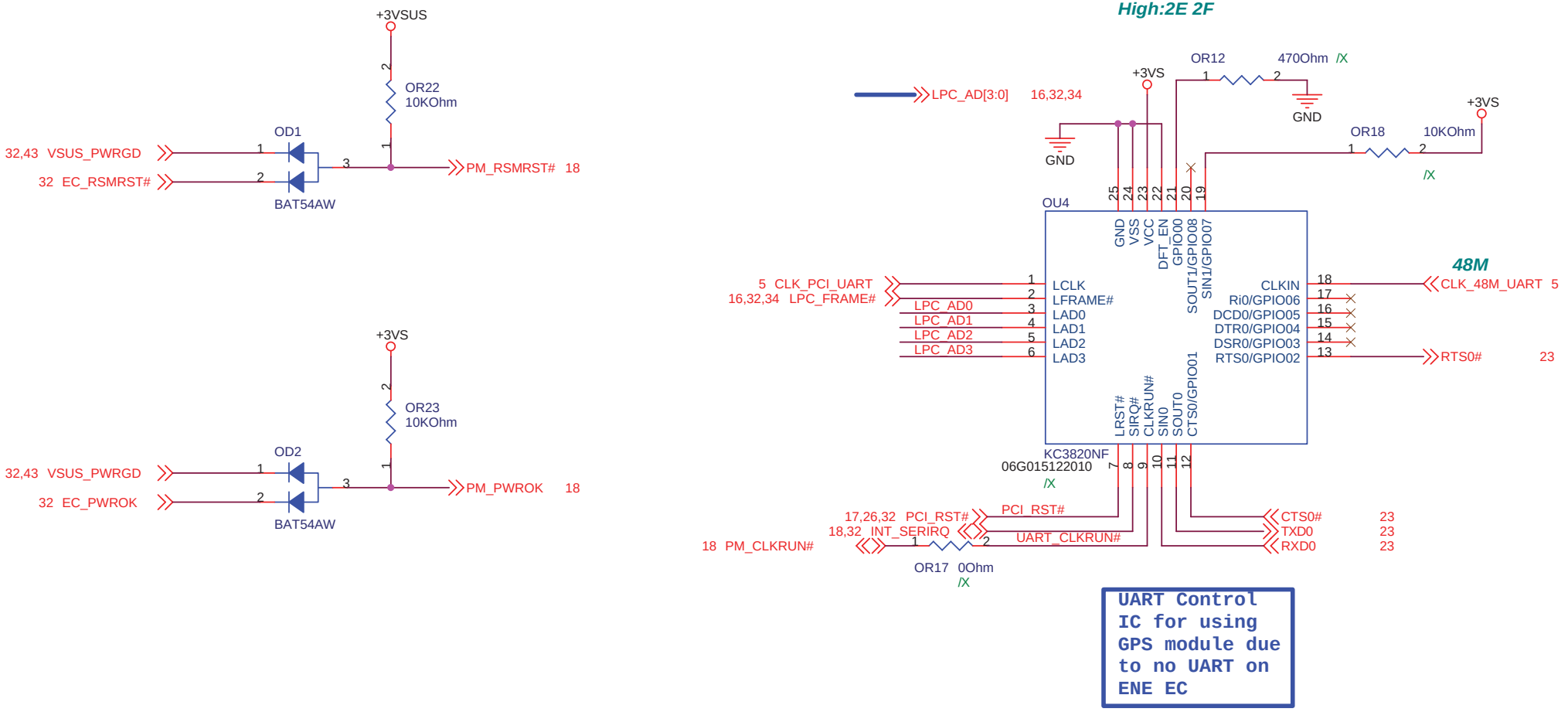
<Core Design>

ASUSTek Computer Inc.	Title : AU6336-C52	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 29 of 47	


AR104 0Ohm
/X
GND
AGND
AR105 0Ohm
/X
GND
AGND
AR106 0Ohm
/X
GND
AGND
Return Path
+5VS
AR34
0Ohm
N/A
+5V_AMP
>30mil
AC91
10uF/10V
AC92
0.1UF/16V
AC89
10uF/10V
AC90
0.1UF/16V
+5VS_AUDIO
P_GND
DMIC_CLK_R
EC118
0.1UF/16V
/X
GND
INTSPKR+
INTSPKR-
INTSPKL-
INTSPKL+
AU15B
ALC269Q-GR
+3VS
AR63
0Ohm
r0603_h24
+3V_CODEC
AC65
10uF/10V
AC66
0.1UF/16V
AC67
0.1UF/16V
AU15A
ALC269Q-GR
02G611005005
31 DMIC_DATA
31 DMIC_CLK
AR103 0Ohm
DMIC_CLK_R
PD#
DVDD
GPIO0/DMIC_DATA
GPIO1/DMIC_CLK
PD#
SDATA_OUT
BCLK
DVSS
SDATA_IN
DVDD_IO
SYNC
RESET#
PCBEEP
16 A_Z_SDOUT
16 A_Z_BITCLK
16 A_Z_SDIN0
16 A_Z_SYNC
16 A_Z_RST#
AR1
33Ohm
A_Z_SDIN0_R
CBP
CBN
CPVEE
HPOUT_R
HPOUT_L
CPVREF
MIC1_VREFO_R
MIC2_VREFO
MIC1_VREFO_L
VREF
AVSS1
AVDD1
AC96 2.2UF/16V
AC76 2.2UF/16V
HEADPHONE_R 31
HEADPHONE_L 31
MIC1_VREFOUT_R 31
MIC1_VREFOUT_L 31
VREF_CODEC
AC59
10uF/10V
AC60
0.1UF/16V
+5VS_AUDIO
AGND
Analog: Pin.13~Pin.38
Digital: Pin.1~Pin.12
and Pin.39~Pin.48
+5VS_AUDIO
+3VS
Audio power sequence requirement
32 OP_SD#
OP_SD#: Controlled by
EC to power down
Class-D speaker amp.
PD#: Internal Pull-up 50K to +3V
AD12
A_Z_RST#
BAT54AW
PD#
AC169
100PF/50V
/X
GND
JEREF
AR98
20KOhm
1%
AGND
AC202 1UF/16V
/X
AC203 1UF/16V
/X
3G_R_A
23
MIC1_R
MIC1_L
AC61
4.7UF/10V
AC62
4.7UF/10V
Need 4.7u/10v X5R to
prevent poor THD+N
MIC1_C_R 31
MIC1_C_L 31
AC204 1UF/16V
/X
3G_MIC
23,31
AR60 39.2KOhm
1%
EAR_SW# 31
SENSE_A
AR58 20KOhm
1%
MIC_SW# 31
+5VS
AU31
SHDN#
GND
IN
SET
OUT
APL5315BI-TRL
AC74
0.1UF/16V
/X
GND
Vout=0.8*(1+(7.32K/1.5K))
APC1
1000PF/16V
/X
AL24
0Ohm
r0603_h24
+5VS_AUDIO
AC71
10uF/10V
AC142
10uF/10V
/X
AC72
0.1UF/16V
AC73
0.1UF/16V
AR69
7.32KOhm
1%
AR15
1.5KOhm
1%
r0402
AC75
1UF/16V
AGND
AGND
AGND
Codec被ㄱ
http://skema-laptop-motherboard.blogspot.com/
For Audio Noise Issue
<Core Design>
Title : ALC269-1
ASUSTek Computer Inc.
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 30 of 47

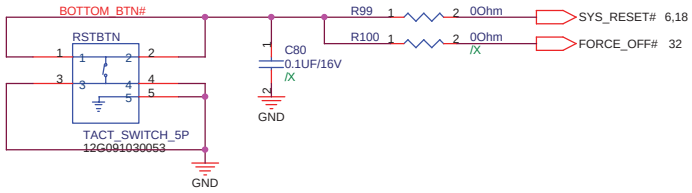

DMIC
WtoB_CON_4P
SIDE2
SIDE1
+3VS
AC210
0.1UF/16V
GND
DMIC Cable length should be less 30cm
30 DMIC_CLK
EC112
0.1UF/16V
/X
30 DMIC_DATA
EC113
AR107 0Ohm
AR108 0Ohm
AR109 0Ohm
N/A
P_GND
Return Path
Total length from speakerR+- L+-(pin40 41 44 45) to internal speaker please as short as possible(<20cm is better)
>20mil
INTSPKR-
INTSPKR+
INTSPKL-
INTSPKL+
AR86
AR90
AR91
AR92
0805
AC194 1UF/10V
AC195 1UF/10V
INTSPKRC-
INTSPKRC+
INTSPKLC-
INTSPKLC+
AC1 0.22UF/16V
AC2 0.22UF/16V
AC3 0.22UF/16V
AC4 0.22UF/16V
If chioke R86, R90, R91, R92 are mounted, please mount C194 C195 to avoid EMI issue.
Mounted if L26 L29 L30 L31 use bead or 0ohm
SPEAKER
AC196 33PF/50V
AC197 33PF/50V
AC198 33PF/50V
AC199 33PF/50V
WtoB_CON_4P
12G171010049
LINE_OUT use 12G140501060
EAR_SW#
HEADPHONE_L
HEADPHONE_R
AR41 75Ohm r0402
AR42 75Ohm r0402
FL3
FR3
AL17 120Ohm/100Mhz
AL18 120Ohm/100Mhz
HEADPHONE_JACK_L
HEADPHONE_JACK_R
HEADPHONE
AUDIO JACK
AC51 100PF/50V
AC52 100PF/50V
PHONE_JACK_6P
12G140501060
AGND
change from DIP to SMD
23,30 3G_MIC
AC207
1UF/16V
AR102 100KOhm
AR101 100KOhm
AC206 1UF/16V
AC209 1UF/16V
MIC1_C_L
MIC1_C_R
R70 and R71: If don't need retasking function, change to 1K.
MIC_SW#
MIC1_C_L
MIC1_C_R
AR70 75Ohm r0402
AR71 75Ohm r0402
AL19 120Ohm/100Mhz
AL20 120Ohm/100Mhz
AR50 4.7KOhm
AR51 4.7KOhm
MIC1_VREFOUT_L
MIC1_VREFOUT_R
MIC_JACK
MIC1_JACK_L
MIC1_JACK_R
AC55 100PF/50V
AC56 100PF/50V
PHONE_JACK_6P
12G14040106Y
MIC_JACK use 12G14040106Y
change from DIP to SMD
http://skema-laptop-motherboard.blogspot.com/
<Core Design>
ASUSTek Computer Inc.
Title : ALC269-2
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 31 of 47

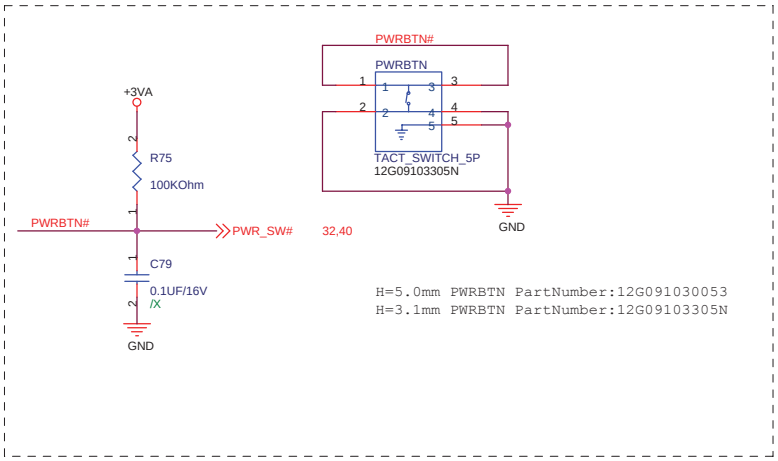

+3VA
OC1 10uF/10V
OC2 0.1UF/16V
OC3 0.1UF/16V
OC4 0.1UF/16V
OC5 0.1UF/16V
OC6 0.1UF/16V
OC7 0.1UF/16V
GND
OR1 100KOhm
34 FORCE_OFF#
OC11 1UF/16V
OU1
CD OUT
VDD
NC GND
RN5VD27CA-TR-F
EC_RST#
OC10 0.1UF/16V
SMB1_CLK
SMB1_DATA
OR2 4.7KOhm
OR3 4.7KOhm
+3VS
SMB2_CLK
SMB2_DATA
TP_CLK
TP_DATA
10KOhm
ORN1D
ORN1C
ORN1B
ORN1A
BAT_IN
AC_OK
PM_SUSC#
PM_SUSB#
100KOhm
ORN2A
ORN2B
ORN2D
ORN2C
PM_LEVELDOWN#
OR4 100KOhm
TPC26T OT1
CPU_LEVELDOWN#
OR20 100KOhm
/X
LID_EC#
OC33
0.1UF/16V
OU2
LPC_AD[3:0] 16,33,34
SERIRQ
LFRAME#
PCICLK
GPIO1D/CLKRUN#
LAD0
LAD1
LAD2
LAD3
LPC I/F
GPIO01/KBRST#
GPIO0E/SCI#
GPIO00/GA20
GPIO05/PCIRST#
ECRST#
KSO[15:0]
KSI[7:0]
Key Matrix Scan
GPIO20/KSO0/TP_TEST
GPIO21/KSO1/TP_PLL
GPIO22/KSO2
GPIO23/KSO3/TP_ISP
GPIO24/KSO4
GPIO25/KSO5
GPIO26/KSO6
GPIO27/KSO7
GPIO28/KSO8
GPIO29/KSO9
GPIO2A/KSO10
GPIO2B/KSO11
GPIO2C/KSO12
GPIO2D/KSO13
GPIO2E/KSO14
GPIO2F/KSO15/E51_RX(ISP)
GPIO48/KSO16
GPIO49/KSO17
GPIO30/KSI0/E51_TX(ISP)
GPIO31/KSI1
GPIO32/KSI2
GPIO33/KSI3
GPIO34/KSI4
GPIO35/KSI5
GPIO36/KSI6
GPIO37/KSI7
NUM_LED#
CAP_LED#
SCRL_LED#
GPIO1A/NUMLED#
GPIO53/E51TMR1/CAPSLED#
GPIO55/E51INT0/SCRLED#
LED
LCD_SCL
LCD_SDA
LCD_CSB
LCD_VSYNC
TP_CLK
TP_DATA
GPIO4A/PSCLK1/P80_CLK
GPIO4B/PSDAT1/P80_DAT
GPIO4C/PSCLK2
GPIO4D/PSDAT2
GPIO4E/PSCLK3
GPIO4F/PSDAT3
PS2 I/F
SMB1_CLK
SMB1_DATA
SMB2_CLK
SMB2_DATA
GPIO44/SCL1
GPIO45/SDA1
GPIO46/SCL2
GPIO47/SDA2
SM BUS
Thermal Sensor
HOTKEY_SW0#
HOTKEY_SW1#
EXTSMI#
LID_EC#
NC_GPIO0B
NC_GPIO0C
HOTKEY_SW2#
PWR_SW#
AC_OK
EC_RSMRST#
BAT_IN
PIN76
BATSEL_3S
CHARGE1_LED#
PWR_LED_UP
HOTKEY_SW3#
INTERNET#
GPIO04
GPIO07/GPWU
GPIO08
GPIO0A/GPWU
GPIO0B/ESB_CLK
GPIO0C/ESB_DAT
GPIO0D
GPIO18
GPIO40
GPIO41
GPIO42
GPIO43
GPIO50/SELIO#
GPIO52/E51CS#
GPIO54/E51TMR0/WDT_LED#
GPIO56/E51INT1
GPIO57/XCLK32K
GPIO
KB3310QF
N/A
02G890000700
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC
AVCC/AGND
AVCC
AGND
GND1
GND2
GND3
GND4
GND5
GND
ADC
GPI38/AD0
GPI39/AD1
GPI3A/AD2
GPI3B/AD3
BAT_ICHG
BAT_CONFIG
BAT_SENSE
BAT_TS 38,47
TPC26T OT27
TPC26T OT28
TPC26T OT29
PWM / FAN
GPIO0F/PWM0
GPIO10/PWM1
GPIO11/PWM2
GPIO19/PWM3
GPIO12/FANPWM1
GPIO13/FANPWM2
GPIO14/FANFB1
GPIO15/FANFB2
BL_PWM_DA
BAT_CRITICAL
MAIL_LED#
FAN1_PWM
FAN1_TACH
TPC26T OT33
TPC26T OT2
TPC26T OT3
TPC26T OT5
BATSEL_4P# 47
PM_PWRBTN# 18
FAN0_PWM 35
FAN0_TACH 35
GPO
GPO3C
GPO3D
GPO3E
GPO3F
DOC
LCD_BACKOFF#
CLK_PWRSAVE#
TPC26T T96
LCD_BACKOFF# 22
PM_BATLOW# 18
XIOA
GPXIOA00/SDICS#
GPXIOA01/SDICLK
GPXIOA02/SDIDO
GPXIOA03
GPXIOA04
GPXIOA05
GPXIOA06
GPXIOA07
GPXIOA08
GPXIOA09
GPXIOA10
GPXIOA11
SPI_MODE#
SUSC_ON
VSUS_ON_R
CPU_VRON
SUSB_ON
EC_PWROK
PM_LEVELDOWN#
CHG_EN#
PRECHG
SPI_WP#
OP_SD#
BAT_LERAN
TPC26T OT9
OR6 0Ohm
VSUS_ON 43
42,45
43,45,46
33
42,43,44,45,46
47
PRECHG 47
34
30
BAT_LEARN 47
XIOD
GPXIOD0/SDIDI
GPXIOD1
GPXIOD2
GPXIOD3
GPXIOD4
GPXIOD5
GPXIOD6
GPXIOD7
CPU_LEVELDOWN#
THRO_CPU
PM_SUSB#
PM_SUSC#
VRM_PWRGD
VSUS_PWRGD
BATSEL_LiFe
NC_GPXIOD7
BATSEL_2P# 47
18
18,24
9,18,42
33,43
47
OR21 1KOhm /X
CPU_LEVELDOWN 42,44,45
OQ2 2N7002 /X
SPI I/F
RD#/SPIDI
WR#/SPIDO
GPIO58/SPICLK
SELMEM#/SPICS#
SPI_CLK_R
OR9 0Ohm
SPI_DO 34
SPI_DI 34
SPI_CLK 34
SPI_CS# 34
OC15 10PF/50V /X
UART
GPIO16/E51_TX
GPIO17/E51_RX
E51_TX
E51_RX
T186
T187
GPIO59/SPICLK/TEST_CLK
NC_GPIO59
TPC26T OT23
XCLK
XCLKI
XCLKO
K_XCLKI
K_XCLKO
V18R
K_V18R
OC17 1UF/16V
PIN76
100KOhm /X
OR223
OC14 12PF/50V
OX1 32.768Khz
OR10 10MOhm /X
OC16 12PF/50V
NC_KSO17
NC_KSO16
R101 100KOhm
R102 1KOhm
/X
<Core Design>
ASUSTek Computer INC.
Title : EC_ENE KB3310
Engineer: Jeff Li
Size A3
Project Name 1000HO_MB
Rev 1.0G
Date: Friday, January 23, 2009
Sheet 32 of 47
http://skema-laptop-motherboard.blogspot.com/

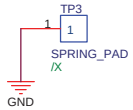


<Core Design>

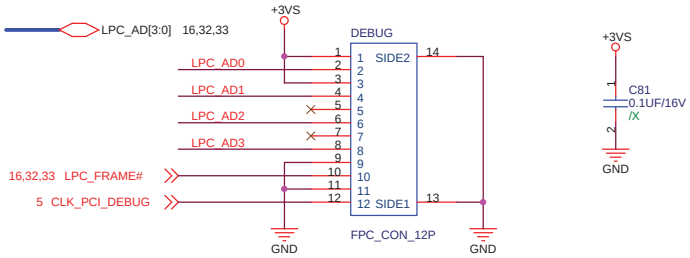
ASUSTek Computer INC.	Title : EC_UART_KC3820	
	Engineer: Jeff Li	
Size: A4	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 33 of 47	



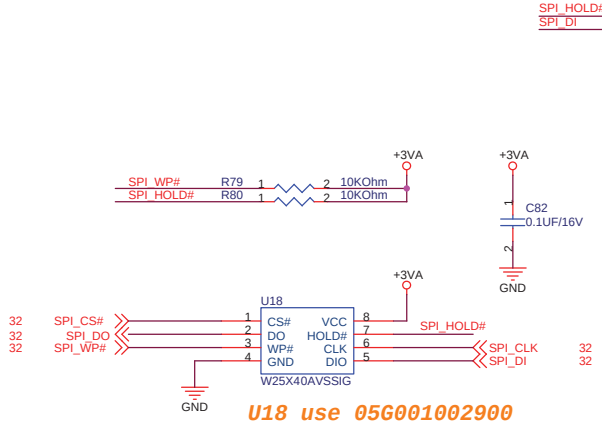




For Debug



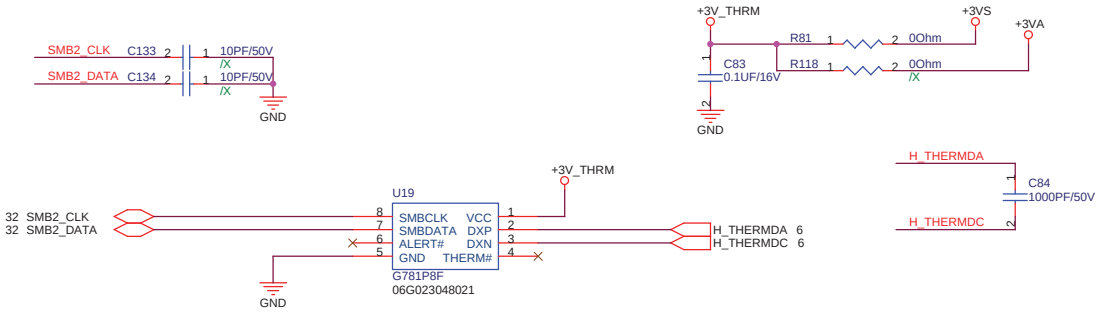
Debug Card cable use Z96 Touch Pad cable, P/N: 14G124110126, 14G124110120, 14G124110121 14G124110124, 14G124110125



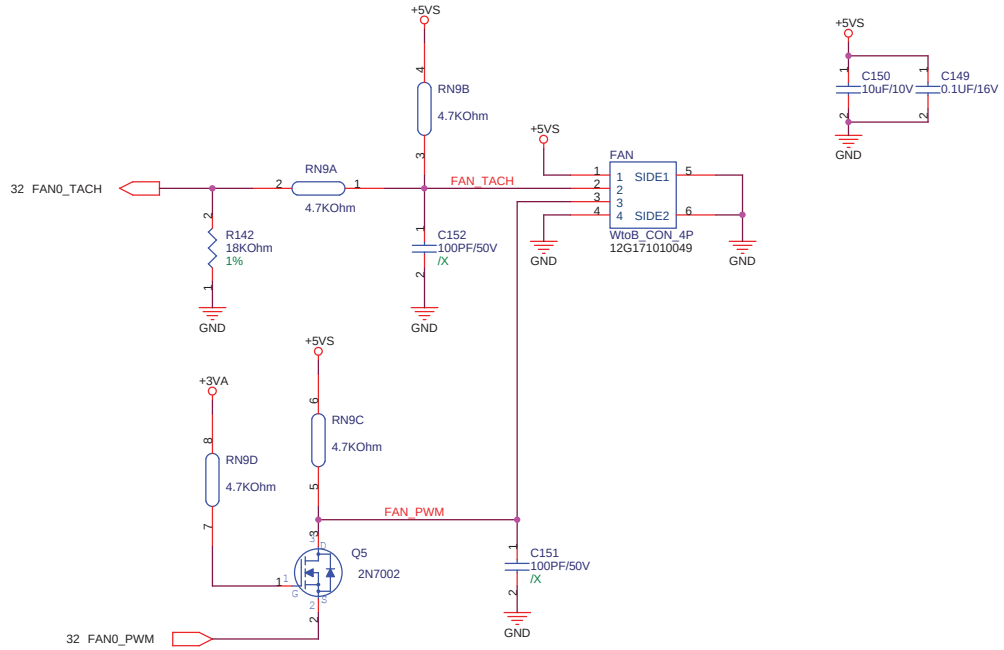
U18 use 05G001002900 & 05G00100F130

<Core Design>

ASUSTek Computer INC.	Title : Switch_SPI ROM_Debug	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 34 of 52	



U19 use 066023048021

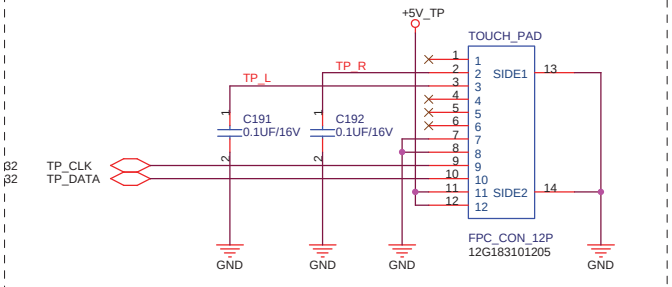


<Core Design>

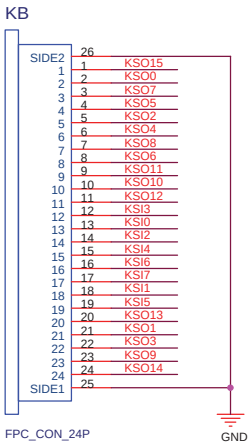
ASUSTek Computer INC.	Title : Thermal Sensor_FAN	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 35 of 52	

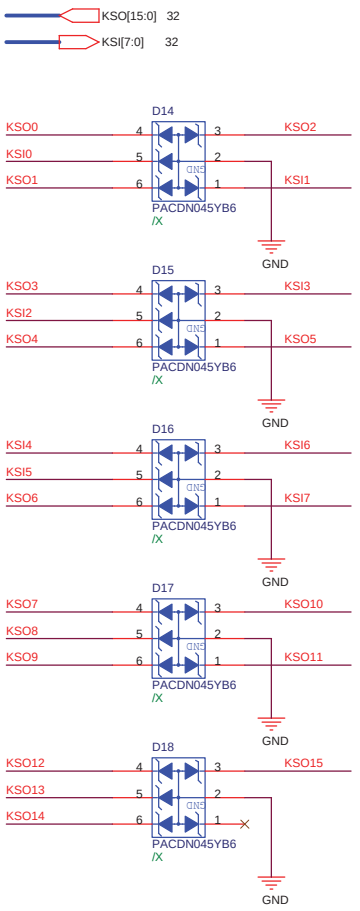
For Touch-Pad

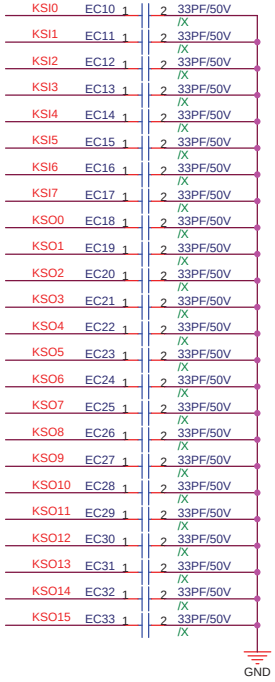
P900 R1.0G



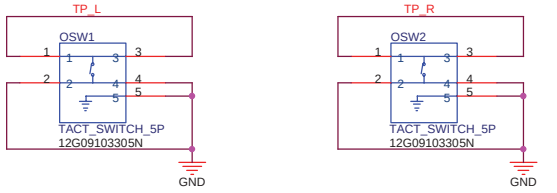
For Keyboard Connector

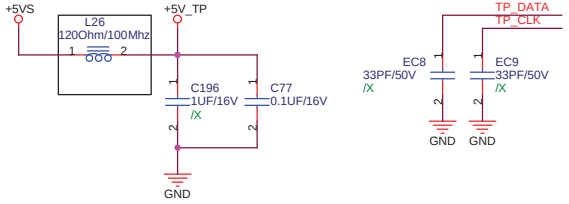


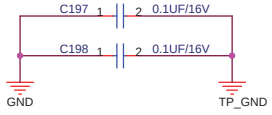


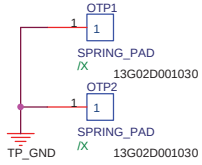


SW2, SW3 use 12G09103305N





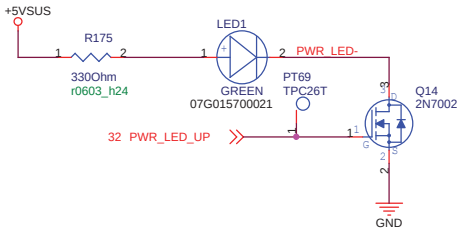




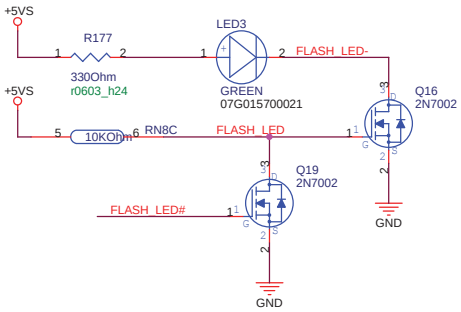
<Core Design>

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 36 of 52	

for POWER LED

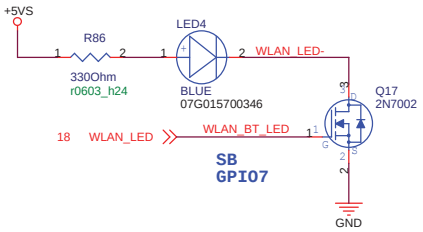


for FLASH LED

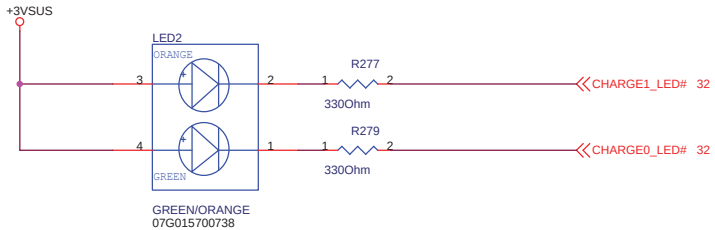


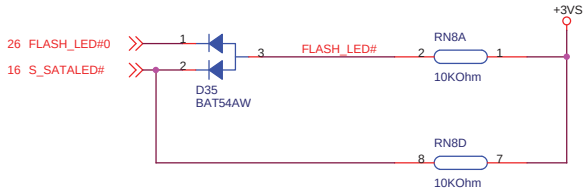
for WLAN/BlueTooth LED

R86 use 4.7K OHm 10G213472003030

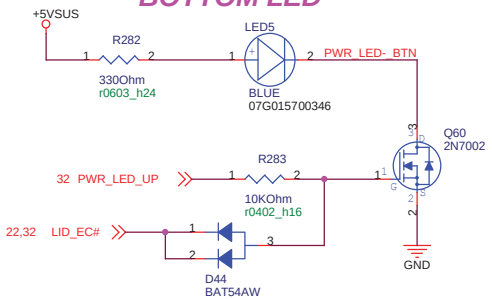


for CHARGE LED





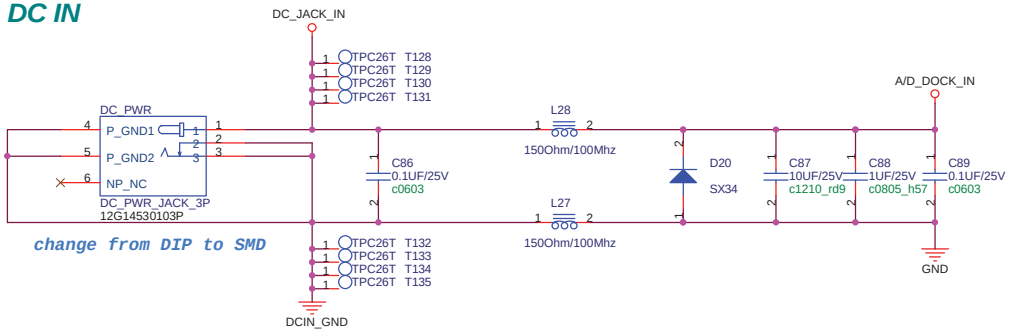
for POWER BOTTOM LED



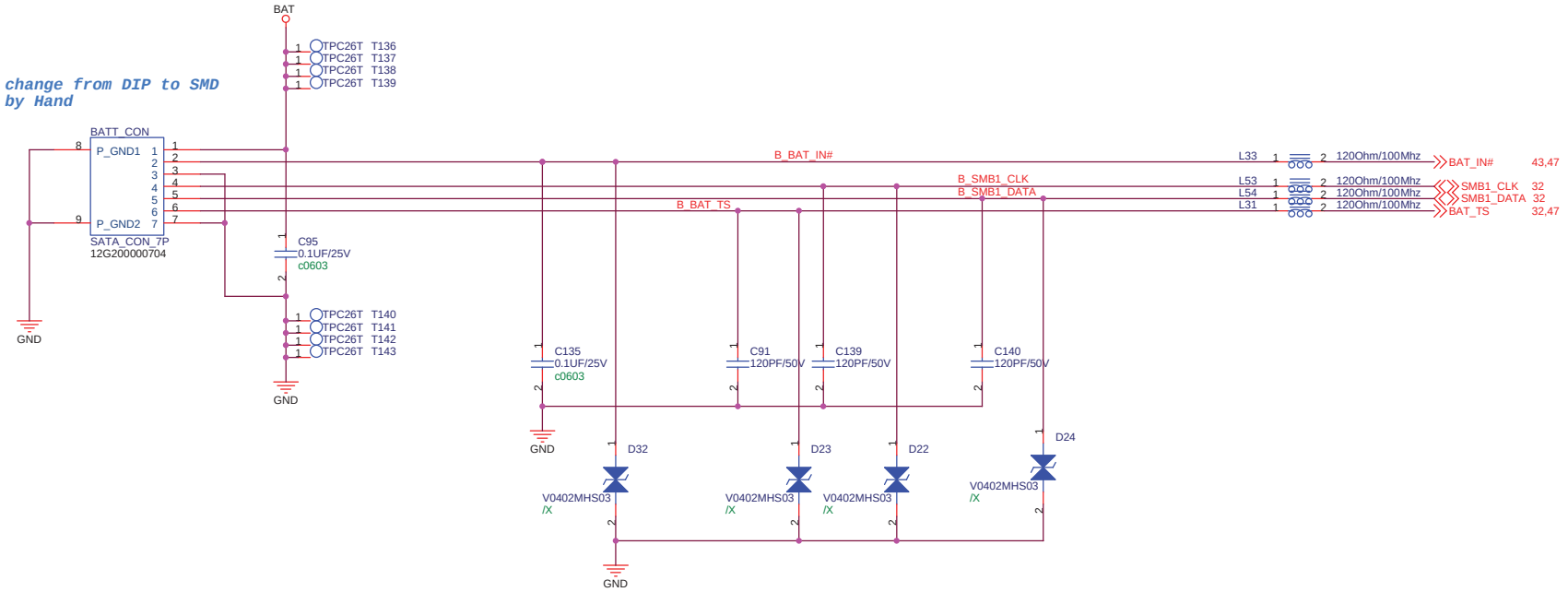
<Core Design>

ASUSTek Computer INC.	Title : LED	
	Engineer: Kell_Huang	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 37 of 47	

DC IN

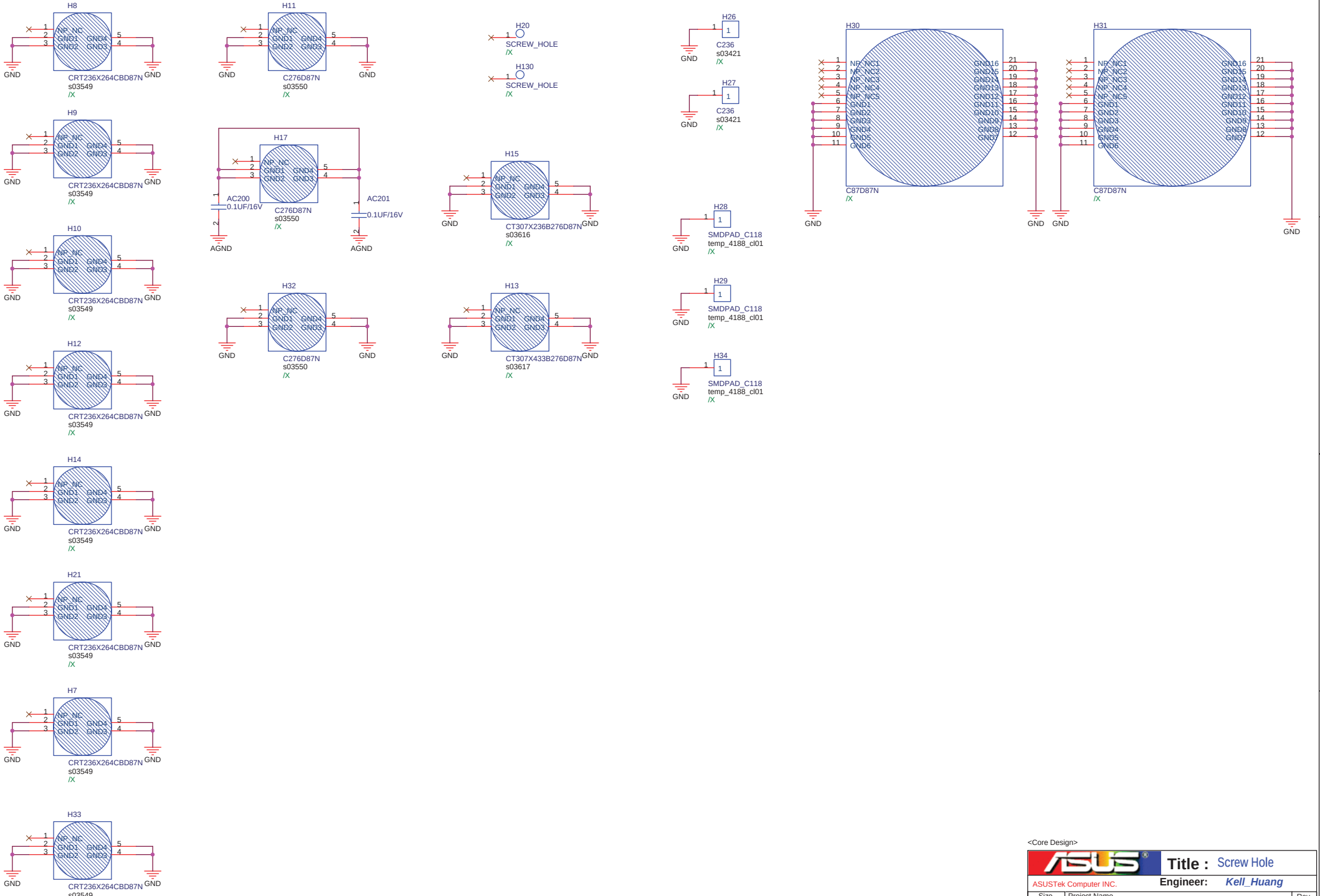


BAT IN



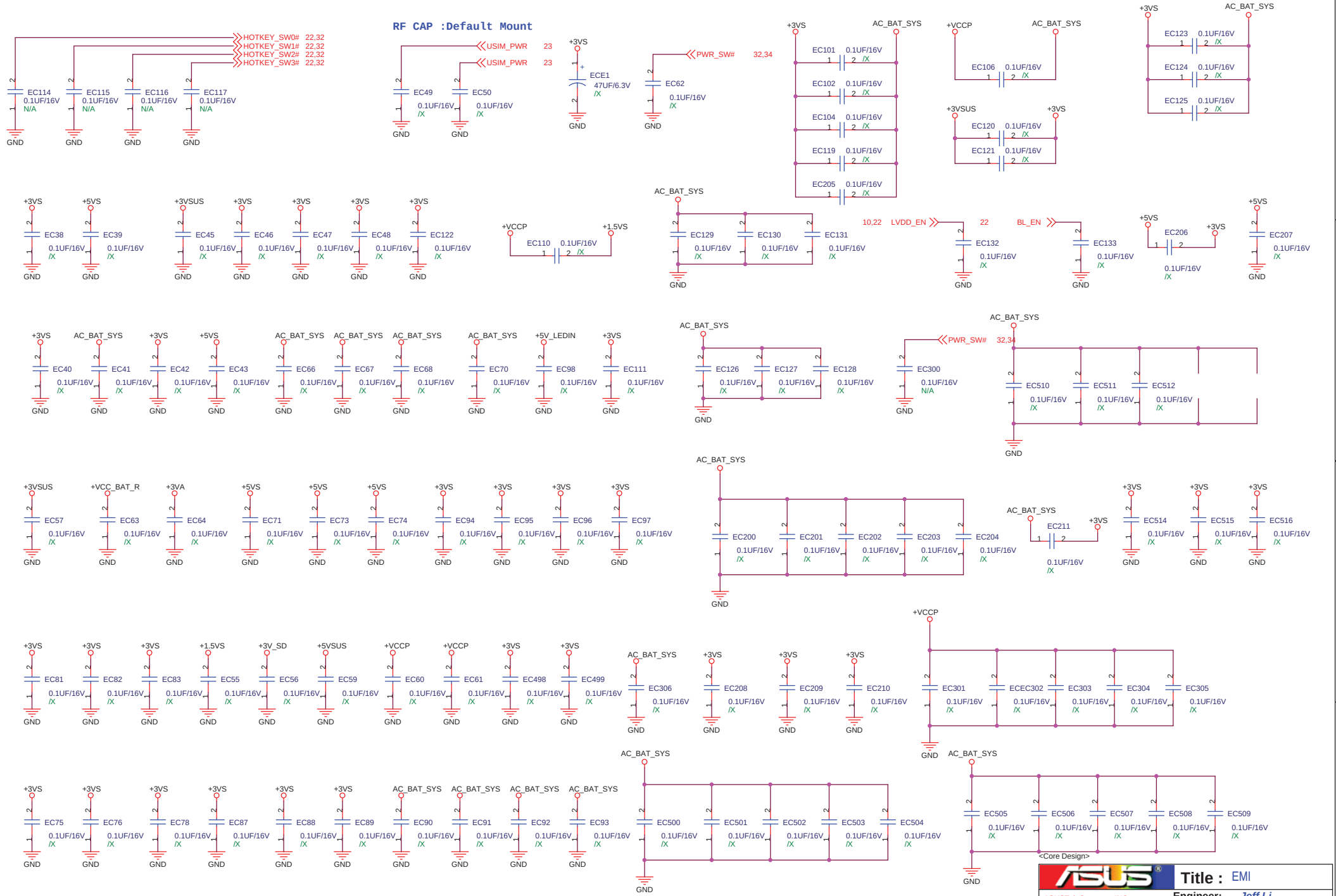
<Core Design>

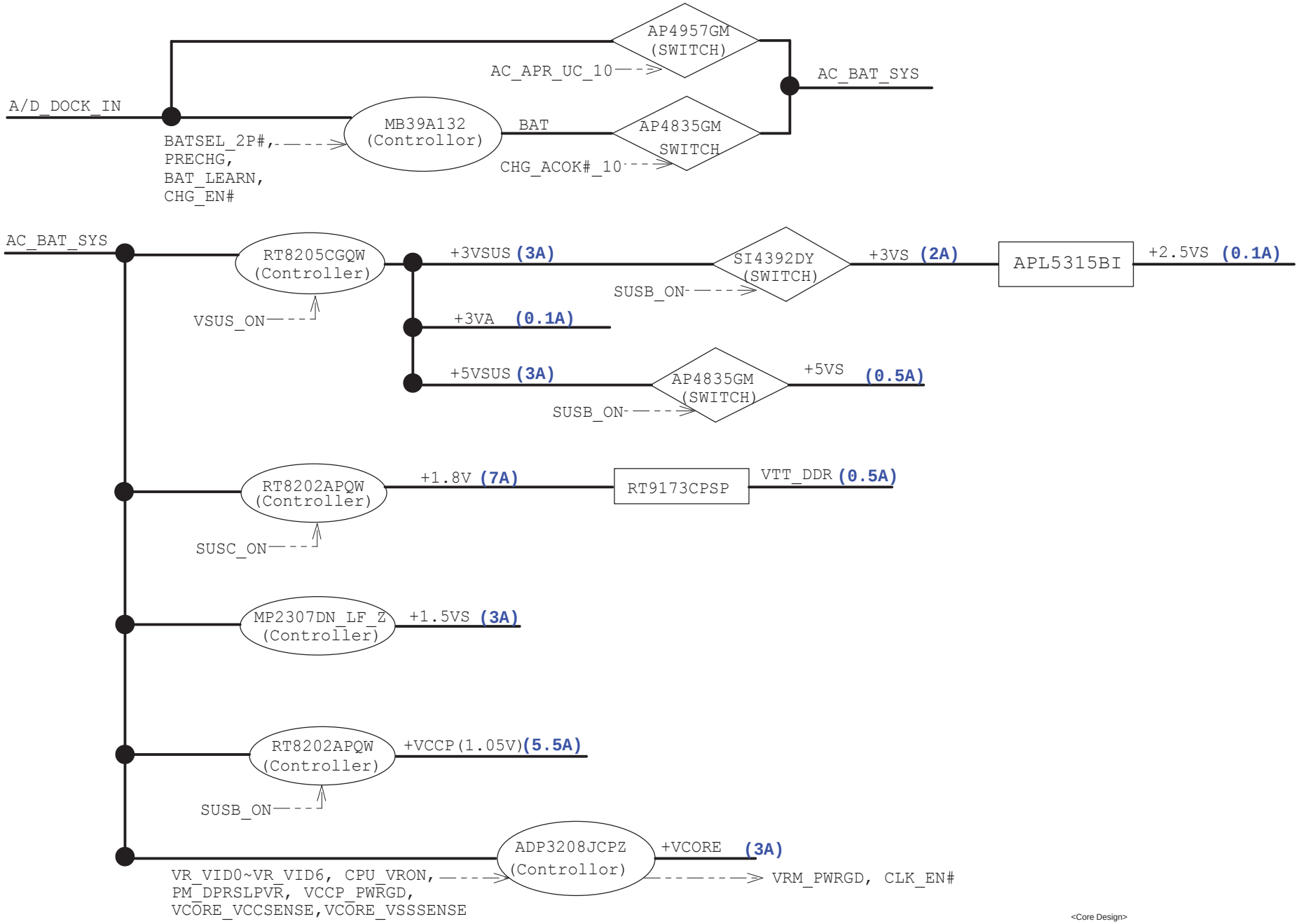
ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: Jeff Li	
Size: A3	Project Name: 1000HO_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 38 of 52	



<Core Design>

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: Kell_Huang	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 39 of 47	





<Core Design>

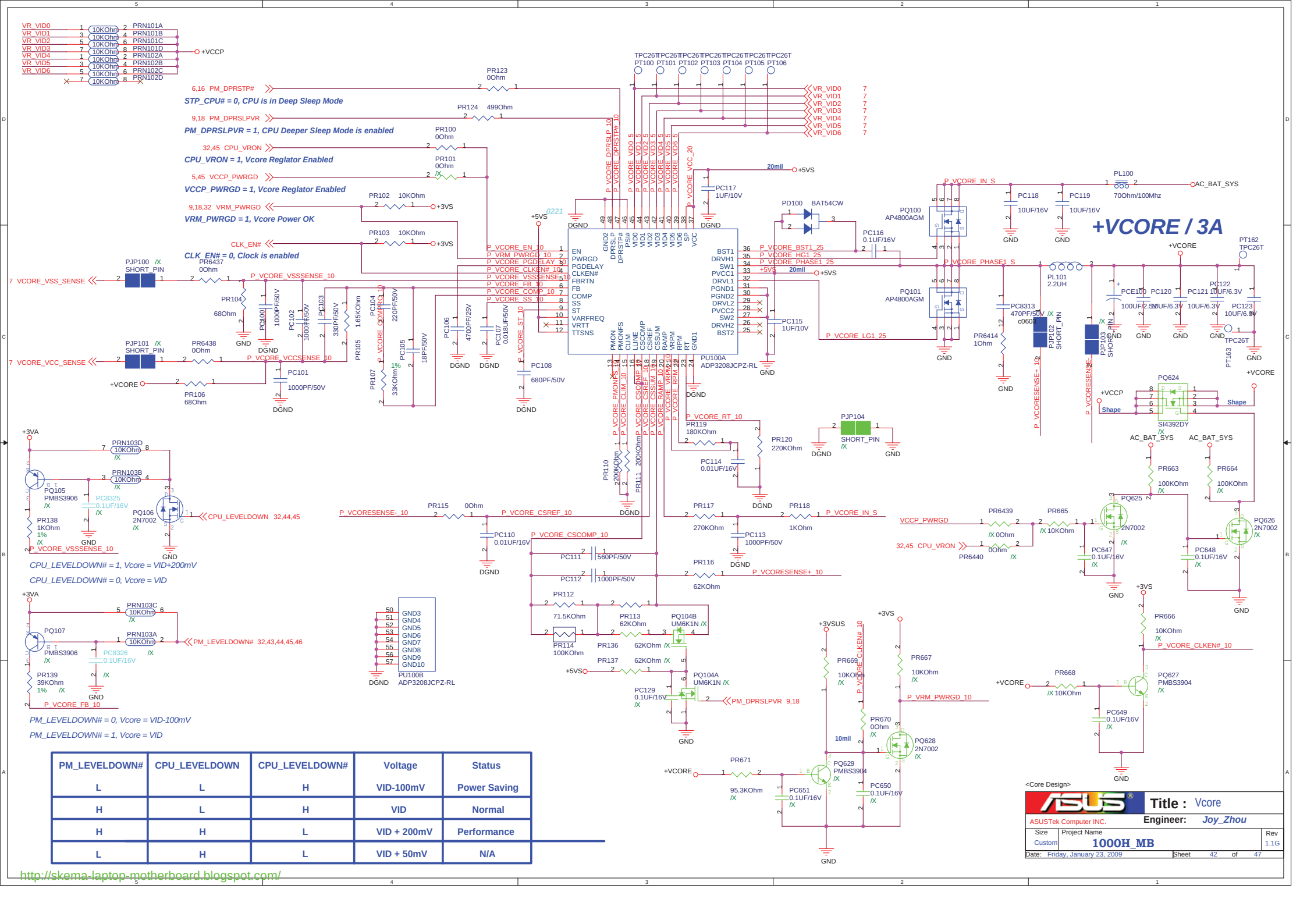
ASUSTek Computer INC.

Title : Power Flow

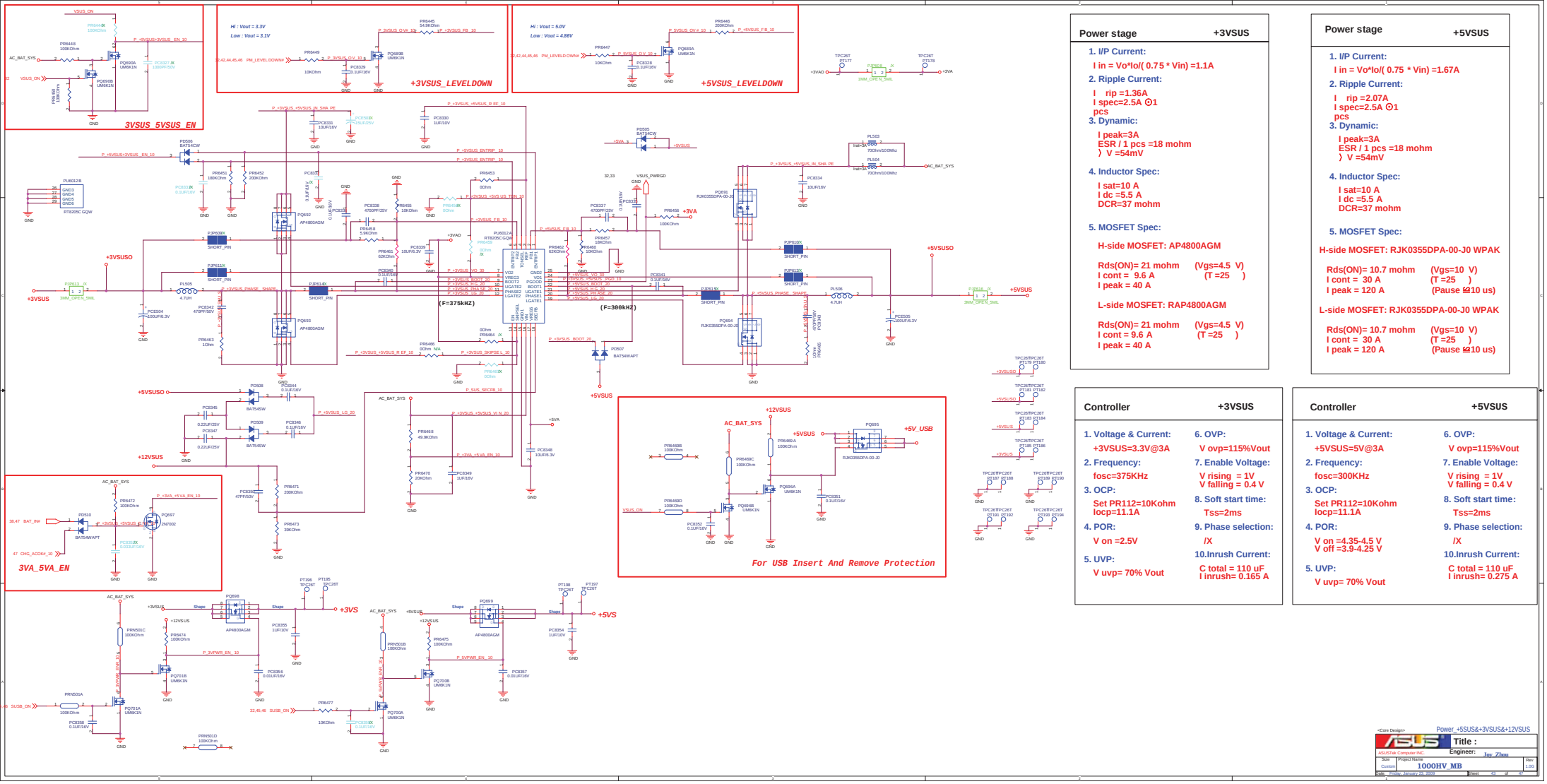
Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

Date: Friday, January 23, 2009 Sheet 41 of 47



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	VID-100mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A



Power stage +3VSUS

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.1A
2. Ripple Current:
   I rip =1.36A
   I spec=2.5A ⊙1 pcs
3. Dynamic:
   I peak=3A
   ESR / 1 pcs =18 mohm
   〉V =54mV
4. Inductor Spec:
   I sat=10 A
   I dc =5.5 A
   DCR=37 mohm
5. MOSFET Spec:
   H-side MOSFET: AP4800AGM
   Rds(ON)= 21 mohm (Vgs=4.5 V)
   I cont = 9.6 A (T =25)
   I peak = 40 A
   L-side MOSFET: RAP4800AGM
   Rds(ON)= 21 mohm (Vgs=4.5 V)
   I cont = 9.6 A (T =25)
   I peak = 40 A

Power stage +5VSUS

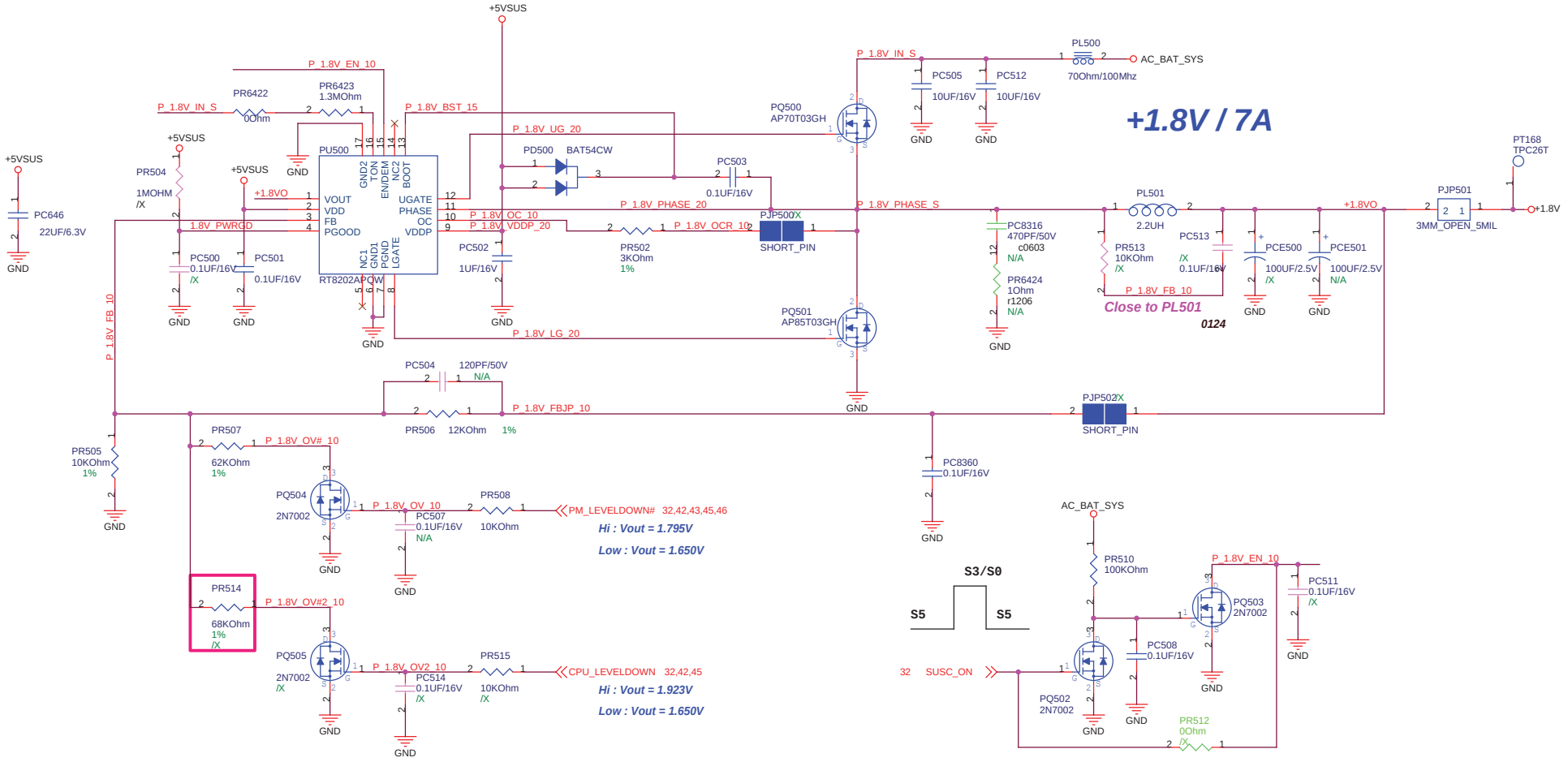
1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.67A
2. Ripple Current:
   I rip =2.07A
   I spec=2.5A ⊙1 pcs
3. Dynamic:
   I peak=3A
   ESR / 1 pcs =18 mohm
   〉V =54mV
4. Inductor Spec:
   I sat=10 A
   I dc =5.5 A
   DCR=37 mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA-00-J0 WPAK
   Rds(ON)= 10.7 mohm (Vgs=10 V)
   I cont = 30 A (T =25)
   I peak = 120 A (Pause ≦10 us)
   L-side MOSFET: RJK0355DPA-00-J0 WPAK
   Rds(ON)= 10.7 mohm (Vgs=10 V)
   I cont = 30 A (T =25)
   I peak = 120 A (Pause ≦10 us)

Controller +3VSUS

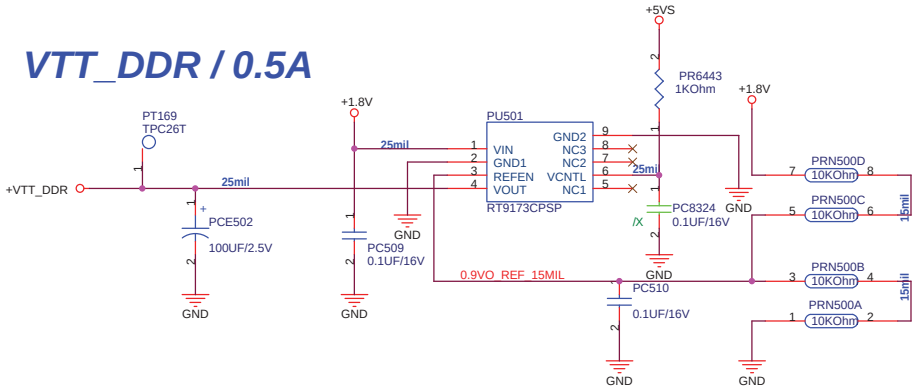
1. Voltage & Current:
   +3VSUS=3.3V@3A
2. Frequency:
   fosc=375KHz
3. OCP:
   Set PR112=10Kohm
   Iocp=11.1A
4. POR:
   V on =2.5V
5. UVP:
   V uvp= 70% Vout
6. OVP:
   V ovp=115%Vout
7. Enable Voltage:
   V rising = 1V
   V falling = 0.4 V
8. Soft start time:
   Tss=2ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 110 uF
    I inrush= 0.165 A

Controller +5VSUS

1. Voltage & Current:
   +5VSUS=5V@3A
2. Frequency:
   fosc=300KHz
3. OCP:
   Set PR112=10Kohm
   Iocp=11.1A
4. POR:
   V on =4.35-4.5 V
   V off =3.9-4.25 V
5. UVP:
   V uvp= 70% Vout
6. OVP:
   V ovp=115%Vout
7. Enable Voltage:
   V rising = 1V
   V falling = 0.4 V
8. Soft start time:
   Tss=2ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 110 uF
    I inrush= 0.275 A



VTT_DDR / 0.5A



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

<Core Design>

ASUSTek Computer INC.

Title : +1.8V & VTTDDR

Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

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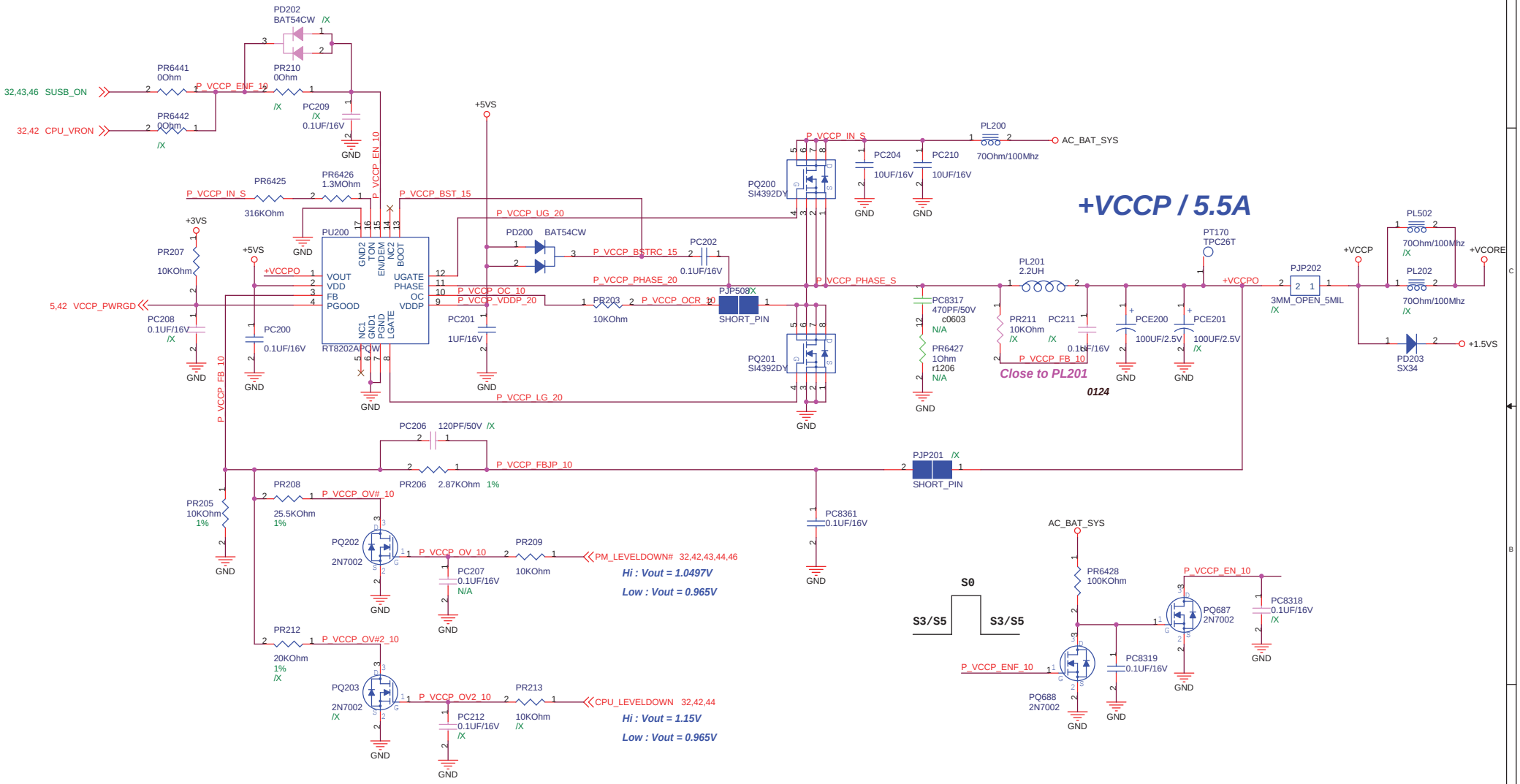

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A

<Core Design>

ASUSTek Computer INC.

Title : VCCP

Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

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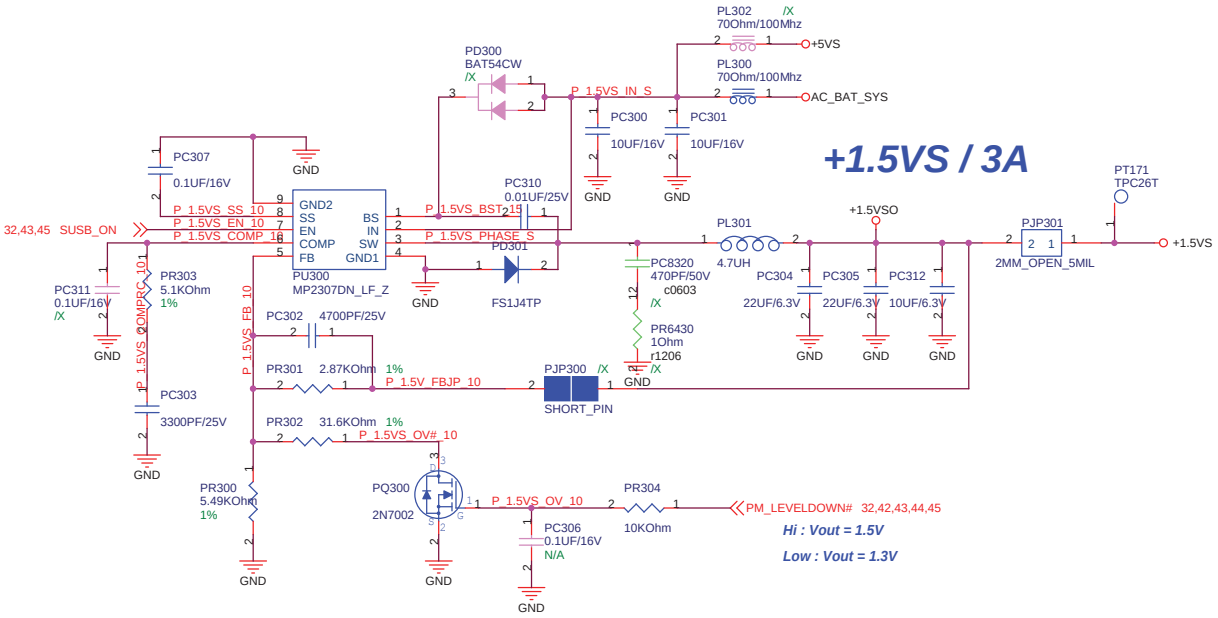
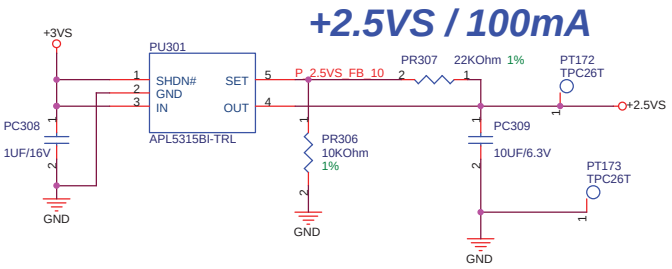
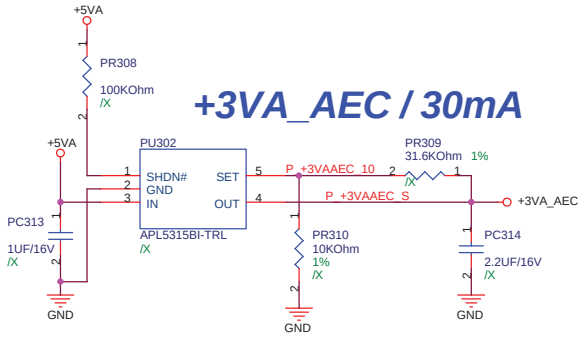
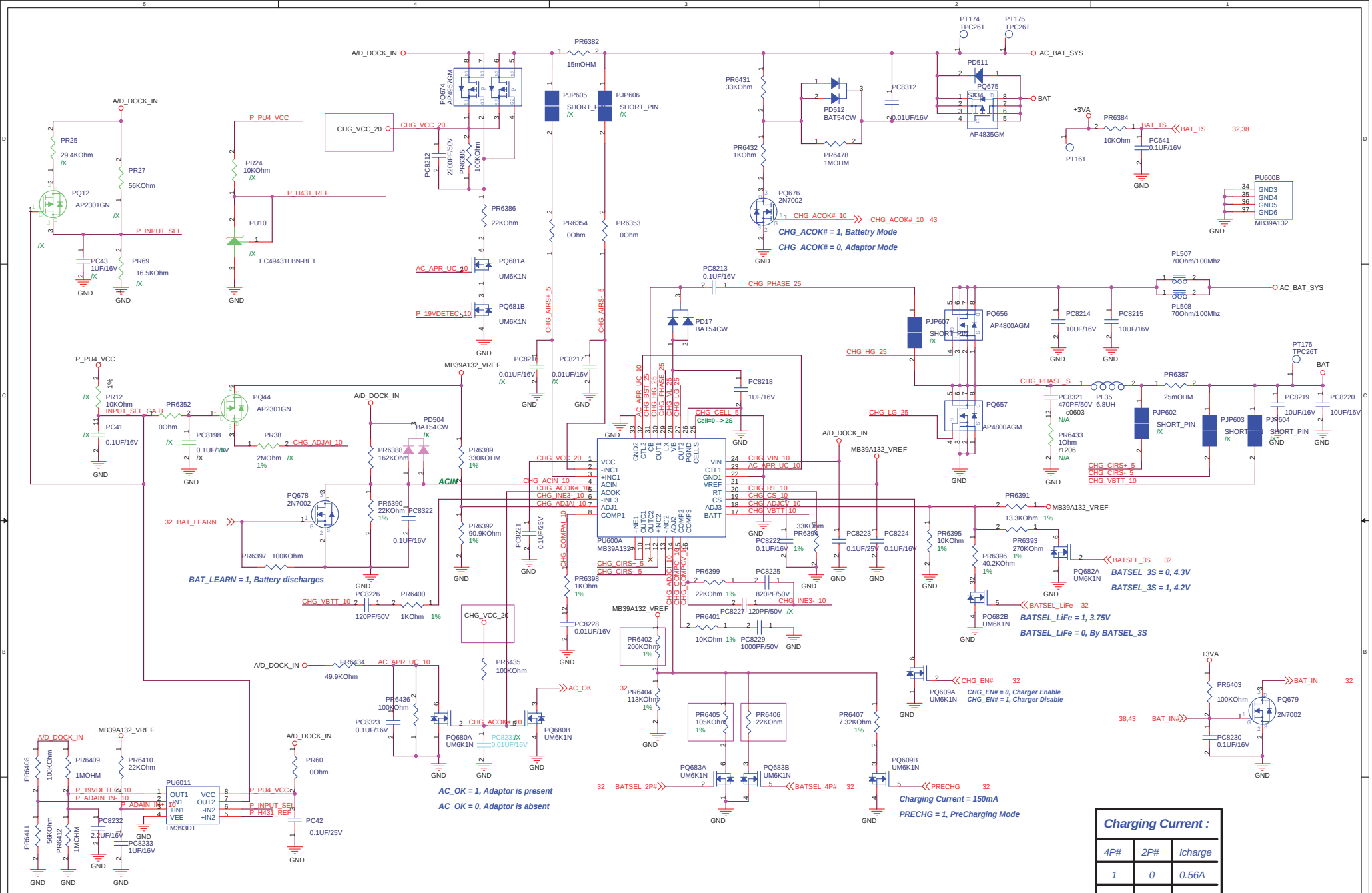






<Core Design>

ASUSTek Computer INC.	Title : +1.5VS & +2.5VS	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 1000H_MB	Rev: 1.1G
Date: Friday, January 23, 2009	Sheet 46 of 47	



Battery Charging Voltage :
Vadj3 > 4.1V ==> Vbat = 4.2V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Charging Current :
4.4V > Vadj2 >= 0V ==>
Ichg = (Vadj2-0.075)/(25*Rs)

Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)

Pre-Charging Mode :
Precharging current = 150mA
Vadj2 = 168.75mV

Adaptor Max. Current :
PR600=235.8K; Ilimit = 2.170A; 20.615W (9.5V/22W)
PR600=185.3K; Ilimit = 2.677A; 32.124W (12V/36W)

ACIN Threshold = 1.25V
Adaptor > 8.63V, System Powered by Adaptor
Adaptor < 8.63V, System Powered by Battery

Prevent Input from 19V :
Adaptor > 13.06V, PQ603B Turn-off
Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :
BAT_ID = 1, 2 Cells; Vadj2 = 0.998V
=> Icharge = 1.477A
BAT_ID = 0, 4/6 Cells; Vadj2 = 1.648V
=> Icharge = 2.517A

VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)

VTH of -IN1: 5V / 62 * (100+62) = 13.06V

VTH of ACIN: 1.25V / 25 * (185+25) = 10.5V
Change PR607 and PR608 value

Charging Current :

4P#	2P#	Icharge
1	0	0.56A
0	1	1.6A
0	0	2.8A

<Core Design>

ASUSTek Computer INC.

Title : Charger
Engineer: Joy_Zhou
Size: Custom
Project Name: 1000H_MB
Rev: 1.1G
Date: Friday, January 23, 2009
Sheet 47 of 47

<Core Design>

ASUSTek Computer INC.	Title : Note	
	Engineer: KingCa_Jin	
Size: A3	Project Name: 1000HE_MB	Rev: 1.0G
Date: Friday, January 23, 2009	Sheet 48 of 47	